Nanoelectromechanical Switch Design and Implementation in Back-End-of-Line Technology

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Technical Report No. UCB/EECS-2022-20
http://www2.eecs.berkeley.edu/Pubs/TechRpts/2022/EECS-2022-20.html

May 1, 2022

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by

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A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering- Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Tsu-Jae King Liu, Chair
Professor Vladimir Stojanović
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Spring 2021

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Abstract

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The emergence of the Internet of Things (IoT) has made energy efficiency a key requirement for integrated electronic systems. Nanoelectromechanical (NEM) switches have the ideal characteristics of zero OFF-state leakage and small subthreshold swing, making them promising candidates for ultra-low-power digital computing applications. IoT has also motivated the development of new computing architectures that are more energy-efficient than the classic von Neumann architecture. An "in-memory computing" architecture avoids the need for data communication between separate processing and memory units, and hence achieves more energy-efficient operation. For such a computing architecture, it is desirable to have compact non-volatile (NV) memory cells that can be programmed and read with very low energy.

Utilization of back-end-of-line (BEOL) metallic interconnect layers to implement non-volatile NEM switches is an attractive approach for monolithic integration with CMOS transistors, which can enable enhanced chip functionality with relatively low incremental manufacturing

cost. This dissertation addresses the fabrication challenges for realizing BEOL NEM switches and demonstrates their suitability for implementation of new computing architectures. Etch recipes and cleaning techniques are developed and optimized to successfully achieve BEOL NEM switches using standard 65 nm and 16 nm CMOS manufacturing processes, for the first time.

This dissertation also presents a new, vertically oriented NEM switch design implemented using multiple BEOL layers to achieve a more compact footprint. Design trade-offs are investigated, and design constraints for reliable and energy-efficient operation are discussed. A design optimization framework is presented to minimize the energy-delay product associated with the programming operation of a NEM switch.

Prototype reconfigurable hybrid CMOS-NEM circuits comprising arrays of BEOL NV-NEM switches are experimentally demonstrated for the first time, showing their promise for compact, energy-efficient and fast memory-based data searching and look-up table operation.

Scaling of NV-NEM switches to smaller dimensions is projected to lower their operating voltage, in order to be compatible with standard CMOS transistors, as well as to improve their energy-delay performance. The read/ write energy and read delay of the vertically oriented NV-NEM switch are projected to compare very favorably against the same performance parameters of other emerging embedded NV memory technologies.

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Acknowledgments

First of all, I would like to express my sincere gratitude to my advisor, Prof. Tsu-Jae King Liu. It would not have been possible to navigate the difficulties of my PhD research project without her continuous guidance, encouragement and resourcefulness. I truly appreciate how she always managed time to discuss research problems or manuscripts and provide guidance on teaching, despite her very busy schedule. I would like to especially thank her for her optimistic outlook, even in difficult situations, and giving me hope.

I am indebted to all my contemporaries from King Group for helping me with measurements in the Device Characterization Lab, wafer processing in the Marvell Nanofabrication Lab and coming up with new ideas for research. I am especially thankful to Dr. Benjamin Osoba, Dr. Zhixin Alice Ye and Lars P. Tatum for successful collaborations. I am thankful to the former postdoctoral researchers Dr. Sergio F. Almeida, Dr. Kimihiko Kato and Dr. Alexis Peschot for their generous mentorship. I also appreciate all the life and career advice from Dr. Xi (Robin) Zhang and Dr. Sergio Almeida. I am also thankful to Tsegereda K. Esatu, Xiaoer Hu, Dr. Fei Ding, Dr. Chuang Qian, Dr. Peng Zheng, Dr. Jaeseok Jeon, Dr. Thomas Rembrandt, Dr. Daniel Connelly, Dr. Yi-Ting (Dennis) Wu, Dr. Yenhao (Philip) Chen, and Dr. I-Ru (Tim) Chen for many helpful discussions. Lastly, I would like to thank King Group members not only for being great colleagues, but also for being absolutely amazing friends - exploring food with Dr. Zhang, discussing anime with Dr. Osoba, and debating pros and cons of RV life with Dr. Ye will be some of my most fond memories from graduate school.

I thank Prof. Junqiao Wu and Prof. Vladimir Stojanović for serving on my dissertation committee and PhD qualification committee and providing me with constructive feedback and generous advice over the years. Dr. Alice Ye and I had the good fortune of having Prof. Stojanović as a mentor when we applied for Qualcomm Innovation Fellowship and I truly appreciate his immense help with our project proposal. I am thankful to Prof. Clark T.-C. Nguyen for not only serving on my PhD qualification committee, but also for teaching

the courses on microfabrication and microelectromechanical (MEM) design, which provided the fundamental knowledge for this project. I worked closely with several members from Stojanović Group - Dr. Rawan Naous, Dr. Qichen Zhang, and Dr. Sajjad Moazeni - to design the devices for this work on multi-project wafers. I appreciate their help in guiding me through the *tape-out* process and troubleshooting various design problems. I also thank Dr. Bivas Saha and Dr. Sara Fathipour from Wu Group for many helpful discussions on device properties.

The 65 nm CMOS chips from this work were fabricated at Texas Instruments (TI), while the 16 nm chips were fabricated using MOSIS service in collaboration with Berkeley Wireless Research Center (BWRC). I am thankful to everyone from TI and BWRC, who aided me in accessing the multi-project wafer *shuttles* in order to design the circuits from this work. I am immensely grateful to Dr. Ting-Ta (Ernest) Yen from TI, whose help was pivotal to the completion of this work. A major part of this work was hinged upon accessing the wafer *shuttles* at TI Santa Clara, which would not have been possible without Dr. Yen's sponsorship and support.

I am very thankful for the fruitful collaborations with Dr. Louis Hutin, and Dr. Giulia Usai from CEA-Leti. I owe them for many useful discussions, brainstorming towards an optimized process and constructive input on my manuscripts. I would also like to thank Dr. Rebecca Mih for sharing her valuable expertise on cleanroom processes and her vision on the big picture.

This work was funded in part by NSF Center for Energy Efficient Electronics Science (E^3S) under Award 0939514 and in part by the France-Berkeley Fund. I would like to thank the administrative team of E^3S, especially Dr. Michael Bartl, Dr. Kedrick Perry, Lea Marlor, and Nicole McIntyre, for providing me with many opportunities for professional development. I would also like to thank Kelsey Horace-Herron, Emily Iwanski, and Mariana Martinez, who worked with me under E^3S summer undergraduate research internship programs, for contributing to this work.

A large part of this work was done in Marvell Nanofabrication Laboratory (Nanolab). I

would like to express my gratitude to the entire Nanolab staff, especially Dr. Bill Flounders, Dr. Allison Dove, Dr. Joanna Bettinger, and Ryan Rivers, for helping me with understanding the tools, optimizing my processes and often accommodating special requests. I would also like to thank the Biomolecular Nanotechnology Center (BNC) staff, especially Dr. Naima Azgui, and AJ Gubser, for helping with the imaging required for this work. I am also greatly indebted to the EECS Director for Graduate Affairs, Shirley Salanio, and the Research Support Assistant, Charlotte Jones, for helping me on numerous occasions.

During my graduate studies, I got the opportunity to be a Graduate Student Instructor for an introductory Electrical Engineering undergraduate class, developed and taught by Prof. Gireeja Ranade. I experienced Prof. Ranade's relentless efforts towards creating a comfortable learning environment for the students and boosting the course staff morale. I would like to wholeheartedly thank her for the invaluable learning experience and also for giving me the opportunity to instruct the same class during the Summer session. I very much appreciate my co-instructors- Grace Kuo, and Panagiotis Zarkos- for the genuine camaraderie and their utmost dedication towards the students.

I am grateful to two of my best friends, Dr. Mohammad Asif Zaman, and Dr. Naznin Sultana, for being my sources of inspiration and motivating me to do my best. I would like to also thank Dr. Mahsa Sadeghi, Dr. Sifat Sharmin Muin, Dr. Yasser Khan, Dr. Asif Islam Khan, Nadia Nusrat, Sifat-E-Tanzim Chowdhury, Maruf Ahmed, Israt Jahan Eshita and Zunaid Omair, for their generosity and friendship; their company is what makes Berkeley a place I can call home. And last but not the least, I would like to express my heartfelt gratitude to my family members, especially my parents, who had been always there for me with their unwavering love and support.

Chapter 1

Introduction

1.1 IC Technology Advancement

1.1.1 CMOS Scaling

For the past several decades, technology advancement in the semiconductor industry has been driven by Moore's Law. Complementary metal-oxide-semiconductor (CMOS) transistors have been scaled down in dimensions to enable doubling of the number of transistors in the most advanced integrated circuit (IC) chip every two years. This aggressive pace of technology advancement, illustrated in Fig. 1.1, has provided for exponential pace of improvement in computational speed while reducing the cost and energy consumed per function.

Reductions in CMOS digital IC operating voltage (V_{DD}) have not kept pace with miniaturization of transistor dimensions since the 90 nm technology node, however. The sluggish scaling of V_{DD} poses a fundamental challenge because of limitations in chip cooling technology that limit the maximum chip power density. The dynamic power consumption of a CMOS IC is proportional to V_{DD}^2; so reduction in V_{DD} is desirable for improving energy efficiency. Ideally the gate overdrive voltage V_{DD}-V_{TH} (where V_{TH} is the transistor threshold voltage) should be maintained with V_{DD} scaling, in order to maintain high transistor ON-

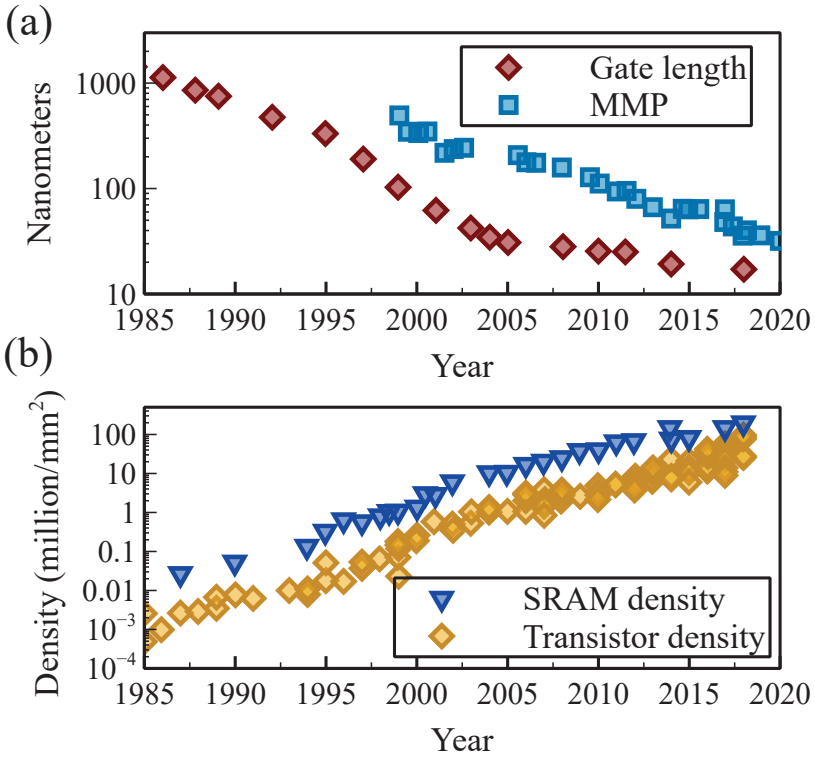

Figure 1.1: Evolution of CMOS technology over the years (adapted from [1, 2] showing the scaling trends of (a) gate length and minimum metal pitch (MMP). (b) Number of total transistors per unit area and density of Static Random Access Memory (SRAM) transistors, showing the density of transistors advancing by 2× on average per generation.

state current (I_{ON}) for fast circuit operation. This means that V_{TH} should be reduced along with V_{DD}. However, the OFF-state leakage current (I_{OFF}) increases exponentially with the reduction of V_{TH}, as shown in the drain current (I_{DS}) vs. gate voltage (V_{GS}) characteristics in Fig. 1.2 (a):

$$I_{OFF} \propto \exp(-V_{TH}/SS), \tag{1.1}$$

where SS is the subthreshold swing, which is the inverse of the slope of the $\log(I_{DS})$ vs. V_{GS} curve in the subthreshold region of operation. Increased I_{OFF} is undesirable, because it results in increased static power consumption in CMOS ICs. Therefore a trade-off exists between dynamic power consumption and static power consumption for CMOS digital ICs,

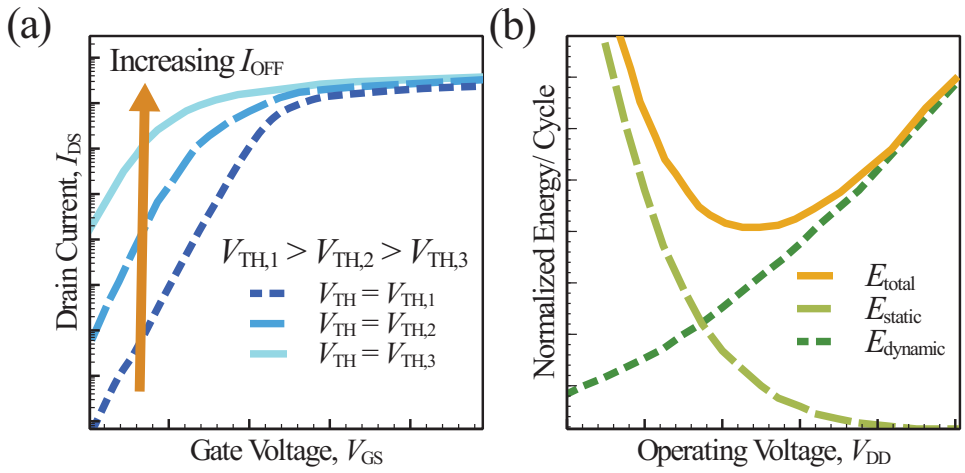

Figure 1.2: (a) Illustration of the switching current-voltage characteristics of an n-channel MOSFET for different threshold voltages; (b) dynamic, static, and total energy consumption of a CMOS-based digital logic circuit. The lower limit for CMOS energy efficiency exists due to MOSFET OFF-state leakage (reproduced from [3]).

which is illustrated in Fig. 1.2 (b). The total energy consumed per digital operation is minimized when V_{DD} is reduced to V_{TH}.

For a fixed value of I_{OFF}, V_{TH} can be decreased to facilitate V_{DD} scaling if SS can be reduced, *i.e.*, if the transistor switches ON/OFF more steeply with changing gate voltage. The fundamental lower limit of SS for CMOS devices is 60 mV/dec at room temperature, which is not practically achievable with planar CMOS transistor structures for very short (sub-25 nm) gate lengths. This led to the adoption of the three-dimensional (3D) FinFET structure for improved gate control (hence steeper SS), beginning at the 22 nm technology node. The 2017 edition of International Roadmap for Devices and Systems (IRDS) predicted FinFET to be a viable candidate for high-performance digital logic applications until technology scaling diminishes the fin width to practical limits [4]. The 2020 edition of the IRDS anticipates a transition to gate-all-around (GAA) transistor structures around 2025, for improved gate control at sub-10 nm gate lengths [5]. As transistor miniaturization approaches ultimate limits, the adoption of *Beyond CMOS* technologies will be needed to

achieve further improvements in chip functionality and energy efficiency.

1.1.2 Beyond CMOS Scaling

The emergence of the Internet of Things (IoT) has driven *Beyond CMOS* technological innovations, as more steeply switching devices and new computing architectures are needed to improve information processing speed and energy efficiency beyond the limits of CMOS technology. Spin-FETs, negative capacitance FETs (NCFETs), nano-electro-mechanical (NEM) switches and 2D topological insulator devices are emerging alternative switching devices for ultra-low-voltage digital computation. Neuromorphic computing architectures and quantum computing using alternative digital/multi-level/entangled state variables potentially offer performance advantages over the conventional von Neumann computing architecture, for specific applications.

Monolithic integration of emerging new devices with CMOS circuitry enables implementation of hybrid circuits that can achieve functionality and energy efficiency beyond the limits of CMOS technology. A major technological challenge is the development of nanometer-scale non-volatile (NV) memory devices that can be monolithically integrated (*i.e.*, embedded) with CMOS circuitry. Phase-change RAM (PCRAM), resistive RAM (ReRAM), spin-transfer torque magnetic RAM (STT-MRAM), ferroelectric RAM (FeRAM) and novel selector devices have shown promise in overcoming this challenge.

1.2 NEM Switches for the Beyond CMOS Era

The operating principle of a micro/nano-electromechanical (M/NEM) switch is the making and breaking of mechanical contact between two conductive electrodes. After the demonstration of the first MEM relay in 1979 [6], electro-mechanical switches of different actuation mechanisms have been demonstrated; these include electrostatic, electrothermal, magnetic and piezoelectric switches/relays. Electrothermal relays employ pre-buckled beams or can-

tilevers comprising a bi-layer stack of materials with different thermal expansion coefficients that result in bending under the effect of heating [7–9]. Their switching speed is usually slow (milliseconds) and their switching energy is high due to the current required for Joule heating. Recently, a non-volatile Phase Change NEM Relay (PCNR) was proposed based on the mechanical expansion of a heated phase change material [10]. Magnetic relays use ferromagnetic materials in the movable electrode to actuate it with the application of a magnetic field. Piezoelectric switches use an electric field to physically deform a piezoelectric material. A beam constructed of a stack of ultra-thin piezoelectric AlN layers sandwiched between two metallic electrodes was demonstrated to actuate with 520 mV; the actuation voltage was decreased to as low as 10 mV with a body bias voltage applied [11–14]. However, the footprint of a piezoelectric relay is comparatively large. Electrostatic M/NEM switches functioning as digital logic devices or non-volatile reconfigurable interconnects have been reported in the literature. Digital logic NEM switches have been demonstrated to switch with sub-1 V voltage signals [15–17], while reconfigurable interconnects have been shown to operate with CMOS-compatible operating voltage [18]. Electrostatic MEM relays can operate reliably across a wide temperature range (−150 °C to 300 °C) [19]. They also have been demonstrated to operate with sub-25 mV signals at temperatures below 100 K [20].

1.2.1 Electrostatically Actuated NEM Switch

In a NEM switch the conducting electrodes are separated physically by an air gap in the OFF-state; hence no current flows between them, resulting in zero OFF-state leakage current. Switching between OFF-state and ON-state occurs abruptly, *i.e.*, the effective subthreshold swing is very small. These properties enable NEM switch based digital ICs to be operated with very low V_{DD}. The prospect of improved energy efficiency has renewed interest in mechanical switches for logic and memory applications [21–23].

The simplest form of an electrostatic NEM switch has three terminals, consisting of a movable cantilever beam, a fixed actuation electrode and a fixed contact electrode (as

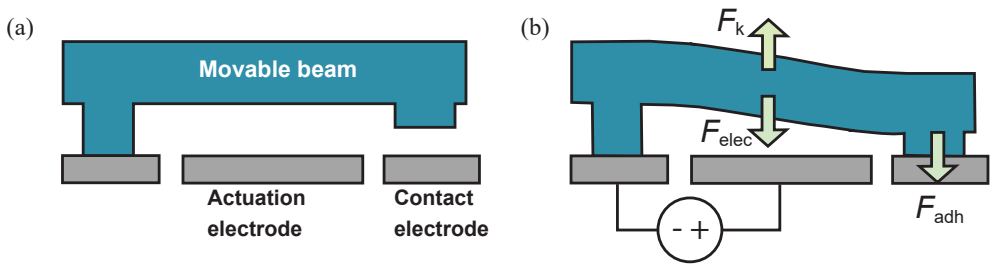

Figure 1.3: Schematic cross-section of a three-terminal electrostatic NEM switch (a) in non-contacting OFF-state (b) in contacting ON-state, showing various forces exerted on the movable beam.

illustrated in Fig. 1.3). In the OFF-state (Fig. 1.3(a)), an air gap exists between the tip of the cantilever beam and the contact electrode, preventing any current flow, if a voltage difference exists between them. If a voltage is applied between the fixed actuation electrode and the cantilever beam, an electrostatic force (F_{elec}) is exerted on the beam towards the direction of the fixed electrode. When the applied voltage exceeds a certain threshold, the electrostatic force becomes large enough to pull the tip of the cantilever into contact with the contact electrode (Fig. 1.3(b)). The physical contact between the contact electrode and the cantilever allows current to flow, if a voltage difference is applied across them. The sharp turn-on characteristics *i.e.*, the steep subthreshold slope, potentially enables low-voltage operation without the penalty of higher static power consumption.

Meanwhile, the displacement of the beam from its equilibrium position produces a spring restoring force (F_{k}) opposing the electrostatic force (F_{elec}), which has a magnitude governed by Hooke's Law:

$$F_{\text{k}} = kx, \tag{1.2}$$

where k is the spring stiffness of the beam and x is the displacement of the beam from its original position. When the beam and contact electrode are in physical contact, adhesive force (F_{adh}) exists between the contacting surfaces, which acts against breaking the contact. The adhesive force is due to a combination of Van der Waals force, electrostatic force, and chemical bonding at the material surfaces [24]; therefore the magnitude of the adhesive force

depends on the contact materials and contact area.

When the actuation voltage is removed after contact is established, the relation between F_k and F_{adh} determines whether the contact breaks or not. If $F_k < F_{adh}$, contact is maintained when F_{elec} goes to zero; this results in a non-volatile switch that can be leveraged to implement non-volatile memory, reconfigurable interconnects or sticky logic [18, 25–27]. Conversely, if $F_k > F_{adh}$, contact is broken when the actuation voltage goes to zero; this results in a volatile switch that can be used for digital computing and power gating [28–32].

1.2.1.1 Electrostatic NEM Logic Switches

In a digital logic circuit, the voltages applied to the conductive electrodes are not fixed; therefore it is not desirable to have the state of a NEM switch be dependent on these applied voltages. A NEM logic switch, comprising four terminals: gate, body, drain and source, can solve this issue [29, 33]. Fig. 1.4(a) shows the schematic cross-section of a four-terminal logic switch with a poly-SiGe movable electrode structure. The movable structure is referred to as the body, while the underlying fixed electrode is referred to as the gate. A voltage

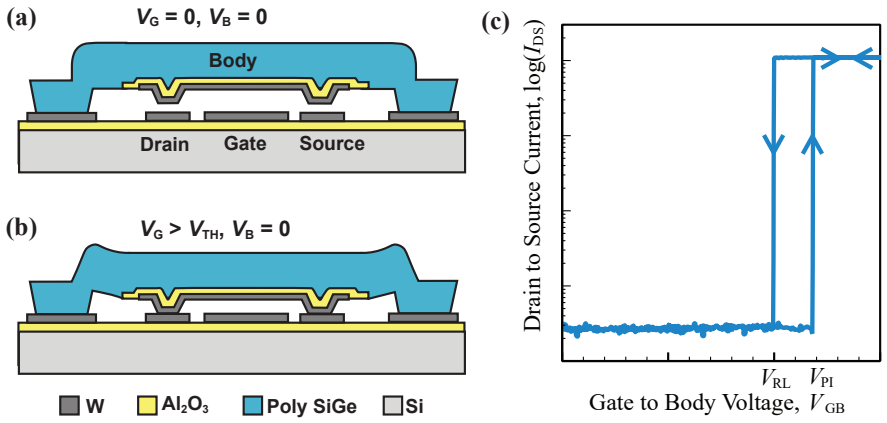

Figure 1.4: Schematic cross-section of a four terminal NEM logic switch (a) in OFF-state with higher drain-source resistance (b) in ON-state, with lower drain-source resistance. (c) Typical switching current-voltage characteristics of a NEM logic for switch bidirectional voltage sweep.

difference between the gate and body terminals ($V_{GB} = V_G - V_B$) generates electrostatic force (F_{elec}) attracting the body towards the gate. A conductive strip of metal, which functions as the "channel," is physically attached to the movable body with an intermediary dielectric insulating layer (Al_2O_3 for this example). The drain and source terminals are physically separated in non-contacting OFF-state, as shown in Fig. 1.4(a), leading to zero drain-source current I_{DS}. If V_{GB} exceeds a certain threshold called the pull-in voltage (V_{PI}), a path for current flow is established between the drain and source terminals through the channel strip, as shown in Fig. 1.4(b). Hence current I_{DS} can flow between these terminals, if a non-zero drain-to-source voltage (V_{DS}) is applied. When V_{GB} is reduced below a certain level such that $F_k > F_{elec} + F_{adh}$, the physical contacts between the channel and the source/drain terminals will break and I_{DS} will drop to zero. This voltage is called the release voltage (V_{RL}). Due to the existence of F_{adh} between the contacting surfaces, V_{RL} is always smaller than V_{PI}. The difference between these two voltages is called the hysteresis voltage:

$$V_H = V_{PI} - V_{RL}. \tag{1.3}$$

Fig. 1.4(c) illustrates a typical current-voltage characteristics for a four-terminal logic switch, labelling the pull-in and release voltages. A negative bias voltage can be applied to the body to reduce the value of V_G required and hence the switching energy required to operate a logic NEM relay [34, 35]. If $V_B = -V_{RL}$, the logic switch can be turned ON and OFF by varying V_G between 0 Volt and V_H.

1.2.1.2 Electrostatic NEM Non-Volatile Memory Devices

A non-volatile NEM switch can be achieved by tailoring the geometry of the movable structure so that the spring restoring force in the contacting state is lower than the contact adhesive force. The basic structure and operation of a NEM memory cell is illustrated in Fig. 1.5. The single-pole-double-throw (SPDT) design comprising two opposing actuation electrodes ensures reprogrammability. The cell consists of five terminals: a movable cantilever beam, two actuation/ *program* electrodes (Program 0 and Program 1) and two

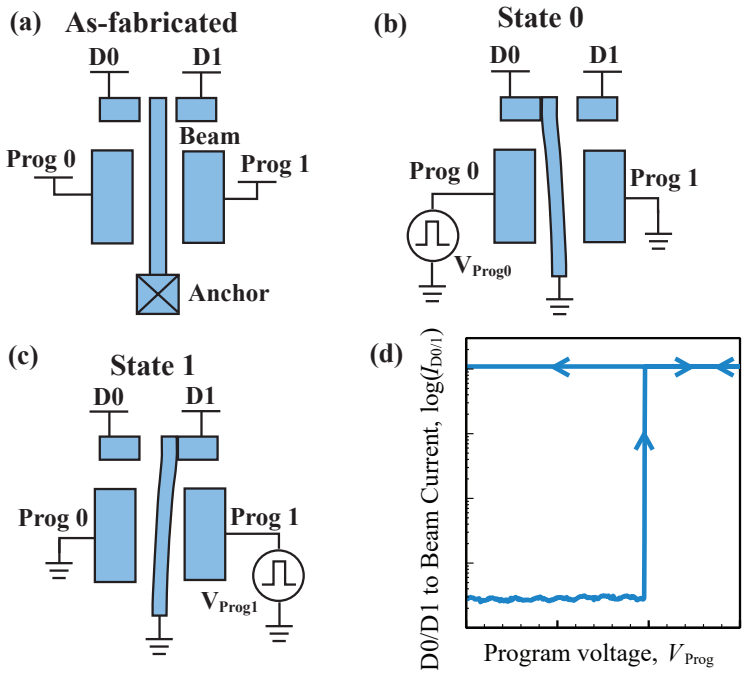

Figure 1.5: Schematic of a non-volatile NEM memory cell (a) in as-fabricated neutral state (b) programmed in state "0", and (c) reprogrammed to state "1."(d) Switching current-voltage characteristics of a typical NV-NEM memory cell is shown for bidirectional voltage sweep.

conducting/*data* electrodes (D0 and D1). In the as-fabricated neutral state (Fig. 1.5(a)), the free tip of the cantilever beam does not contact either of the two data electrodes. The cell can be programmed into state "0" or "1" by applying a voltage pulse to the Program 0 or Program 1 electrode, respectively. To program the cell into state "0," a voltage higher than V_{PI} is applied to Program 0, to establish contact between the tip of the beam and D0 electrode (Fig. 1.5(b)). Since the cantilever beam spring restoring force satisfies the condition for non-volatility, the contact does not break when the applied voltage is dropped to zero. In order to change the programmed state of the memory cell, a voltage must be applied to the opposite program electrode. The condition for reprogrammability dictates that the program voltage should generate enough electrostatic force so that the combination of the electrostatic force and spring restoring force can overcome the contact adhesive force. For

this example, the voltage applied to the Program 1 electrode will cause the tip of the beam to break contact with D0 and bring it into contact with D1 (Fig. 1.5(c)). Reprogramming to a non-volatile contacting state results in the typical current-voltage characteristics illustrated in Fig. 1.5(d).

1.3 CMOS-NEM Hybrid Circuits

Hybrid CMOS-NEM technologies have been demonstrated for CMOS power gating [32], field programmable gate arrays (FPGAs) [36], reconfigurable logic circuits [37] and energy-efficient look-up tables (LUTs) [26].

The negligibly low OFF-state leakage of M/NEM switches makes them attractive for usage as power gates, which can reduce the total energy consumption of a chip. M/NEM switches acting as power-gates for CMOS circuitry have been reported in the literature: Fariborzi *et al.* demonstrated power-gating of a functional CMOS chip with 4-terminal MEM logic relays [32]. Henry *et al.* compared the effectiveness of CMOS and NEM switch power gates for different power-gating schemes [31].

Dadgour *et al.* proposed hybrid NEM/CMOS dynamic-OR gates, placing NEM switches in the pull-down network in order to reduce the leakage current [38, 39]. A hybrid NEMS/CMOS SRAM cell was also proposed by them, replacing the NMOS pull-down transistors and the PMOS pull-up transistors with their NEM switch counterparts. Chong *et al.* also proposed a NEM/CMOS hybrid SRAM cell architecture with NEM relays replacing only the pull-down NMOSFETs, predicting considerable increase in the hold and read static noise margins of SRAM cells [40].

A new FPGA architecture utilizing NEM logic relays for programmable routing was proposed by Chen *et al.* [36]. Specifically, the hysteretic switching behavior of NEM switches was leveraged to replace a FPGA routing switch and the corresponding routing SRAM cell entirely with a single NEM relay. The simulation results predicted 28% reduction in critical path delay, 37% reduction in leakage power and 43.6% reduction in area compared

to a CMOS-only FPGA at the 22 nm technology node. Sirigir *et al.* predicted similar improvements at the 180 nm node [41].

Xu *et al.* proposed leveraging multiple back-end-of-line (BEOL) metallic layers for fabricating compact NEM switches in a standard CMOS process [25]. Additionally, hybrid CMOS/BEOL-NEMS circuits were proposed for a digital logic buffer, a non-volatile SRAM cell and a Content Addressable Memory (CAM) cell. A new hybrid CMOS-NEM neuron circuit was reported by Moradi *et al.* for mixed-signal neuromorphic computing, and was predicted to be 35% more energy-efficient than existing CMOS designs.

Kato *et al.* proposed fast and energy-efficient parallel data searching operation for processing of large data sets based on non-volatile NEM switches [27]. Additionally, energy efficient look-up tables (LUTs) implemented with arrays of BEOL NEM switches were proposed by Kato *et al.* [26]. Choi and Kim experimentally demonstrated 3D CMOS-NEM hybrid reconfigurable circuits for the first time by utilizing the BEOL metallic layers in a standard CMOS process to fabricate non-volatile NEM routing switches over CMOS logic circuits [42]. Kwon *et al.* demonstrated operation of similar hybrid reconfigurable circuits at a CMOS compatible operating voltage of 1.2 V [18]. Recently Kwon *et al.* have demonstrated island-style CMOS–NEM reconfigurable logic circuit blocks and proposed monolithically integrated switch blocks and connection blocks implemented with BEOL NEM switches for fast and energy-efficient FPGAs [37].

1.3.1 Dissertation Overview

This dissertation focuses on implementation of NEM switches with standard CMOS fabrication processes using multiple BEOL metallic interconnect layers, and their application in hybrid CMOS-NEM circuits. A large part of the research work involves process development and optimization to fabricate multi-layered NEM switches with high manufacturing yield. The other part is devoted to optimizing the design of BEOL NEM switches for low-voltage operation and to demonstrating hybrid CMOS-NEM circuits. The remainder of this

dissertation is organized as follows.

Chapter 2 describes the geometry and operating principles of BEOL NEM switches. Different topologies of the BEOL switch are also introduced. Chapter 3 discusses the challenges associated with the BEOL NEM switch fabrication process and presents solutions. A design optimization methodology is presented to achieve device functionality and meet design specifications. Chapter 4 covers the experimental demonstration and characterization of hybrid CMOS-NEM circuits for different applications. NEM switches fabricated together with CMOS circuitry using a standard 65 nm manufacturing process are utilized to demonstrate reconfigurable logic circuits, specifically a parallel data searching circuit and a reconfigurable LUT.

Chapter 5 discusses the benefits of technology scaling on various BEOL NEM switch performance parameters. Experimental results for BEOL NEM switches fabricated using a standard 16 nm manufacturing process are presented. Scaling challenges are also outlined, including the impact of scaling on contact resistance and contact adhesive force. The chapter also considers the impact of technology scaling trends for BEOL NEM switches. BEOL NEM switches are benchmarked against other embedded non-volatile memory devices in terms of read/write delay and energy. Chapter 6 summarizes the key findings and contributions of this dissertation. Suggestions for future work are also presented in this chapter.

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Chapter 2

BEOL NEM Switch Design

2.1 Introduction

For Internet of Things (IoT) applications, energy efficiency is a key requirement. Nanoelectromechanical (NEM) switches are considered an attractive option for IoT applications due to their negligible OFF-state power consumption, non-volatile (NV) switching capability and abrupt switching characteristics [1–8]. As compared with resistive NV memory devices, NV-NEM switches offer a very large resistance ratio between programmed states. As a result, NEM switches can enable longer battery life for IoT devices, *e.g.*, used in wireless sensor networks. NEM devices used in conjunction with CMOS circuitry can provide for enhanced chip functionality and/or energy efficiency [9–15]. However, the larger footprint of NEM switches as compared with transistors, as well as the incremental cost of their integration with CMOS circuitry, pose a barrier for their adoption. Monolithic integration of NEM switches using a conventional state-of-the-art IC manufacturing process can enable compact NEM switches at low incremental cost. Specifically, the back-end-of-line metallic interconnect layers in a conventional CMOS process can be leveraged to implement NEM switches [6, 16–23].

In this chapter, the operating principle of a NEM switch is introduced in Section 2.2. Section 2.3 describes the the process of leveraging the back-end-of-line metallic layers to build

NEM switches. Two different topologies of NEM switch, *i.e.* the lateral and the vertical switch designs are introduced in sections 2.4 and 2.5 respectively. Section 2.6 summarizes this chapter.

2.2 Reconfigurable NV-NEM Switch Design

A bistable single-pole-double-throw (SPDT) NEM switch can be programmed into either of two contacting states. The switch comprises five terminals:two fixed actuation/program electrodes (labeled "Prog0" or "Prog1") on either side of the movable beam, and two corresponding fixed contact/data (conducting) electrodes (labeled "D0" or "D1"). The movable beam can be modeled as a cantilever beam with a spring stiffness of k_{eff}. In an unprogrammed as-fabricated state, the beam stays in the neutral position without making any physical contact, as shown in Fig. 2.1(a). All the electrodes are separated physically by air gaps at this neutral OFF-state; so no current flows through the gaps at normal operating voltages, resulting in zero OFF-state leakage current.

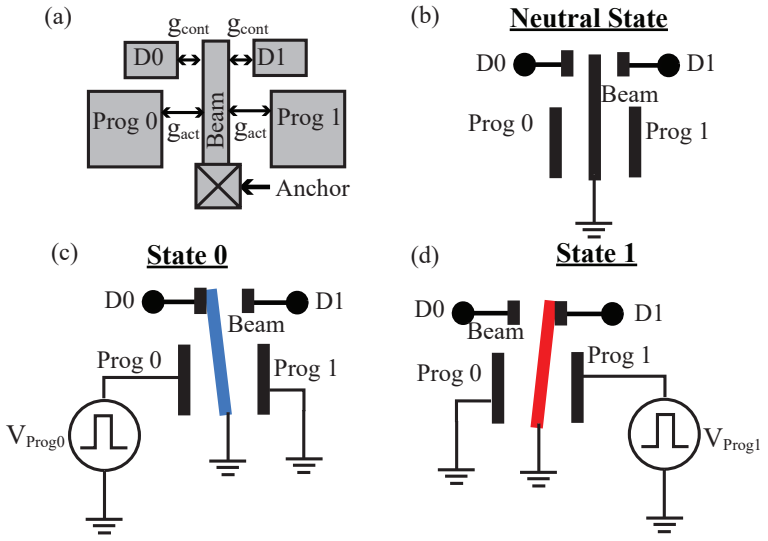

Figure 2.1: Schematic illustrating (a) design parameters of a bistable NEM switch, (b) a NEM switch in neutral state, (c) programming operation to state "0", and (d) state "1".

The actuation electrodes Prog0/1 on either side of the beam can electrostatically actuate the beam into contact with either of the contacting electrodes D0/D1. When a program voltage V_{Prog0} is applied to electrode Prog0, an attractive electrostatic force F_{elec} is induced between the beam and Prog0. $g_{0/1}$ is the size of the variable air gap between the beam and Prog0/1. Without an applied voltage, the switch is in neutral state (Fig. 2.1(b)) and the gap between the beam and either Prog0 or Prog1 is equal to the actuation gap size, g_{act}. In this state, the gap between the beam and either D0 or D1 is equal to the contact gap size, g_{cont}. With a voltage applied to Prog0/1, the electrostatic force exerted on the beam is given by

$$F_{\text{elec}} = \frac{\epsilon_0 A_{\text{act}} {V_{\text{Prog0/1}}}^2}{2g_{0/1}^2}, \tag{2.1}$$

where A_{act} is the effective actuation area, ϵ_0 is the vacuum permittivity. The electrostatic force is counteracted by the spring restoring force given by Hooke's law:

$$F_{\text{k}} = k_{\text{eff}} x = k_{\text{eff}}(g_{\text{act}} - g_{0/1}). \tag{2.2}$$

Here $x = g_{\text{act}} - g_{0/1}$ is the displacement of the beam from the neutral position towards the program electrode with applied voltage. Hence the net force on the beam is given by

$$F_{\text{net}} = F_{\text{elec}} - F_{\text{k}}. \tag{2.3}$$

When $F_{\text{elec}} > F_{\text{k}}$, the net force moves the movable beam towards the corresponding program electrode. As a result, the actuation gap shrinks below g_{act}. The decrease of actuation gap boosts F_{elec} and consequently F_{net}, which causes the gaps to shrink even further through a positive feedback effect. The minimum voltage required for F_{elec} to overcome F_k is called the pull-in voltage V_{PI}. If $V_{\text{Prog0}} \geq V_{\text{PI}}$, the beam tip actuates into contact with the corresponding contact electrode D0, which is denoted by state "0", as shown in Fig. 2.1(c). Alternatively, the NEM switch could have been programmed into state "1" by applying a voltage V_{Prog1} to electrode Prog1. The pull-in voltage V_{PI} can be minimized by maximizing the net force F_{net}, which can be done by either maximizing the actuation area A_{act} and/or reducing the actuation gap g_{act} and contact gap g_{cont}.

When the beam comes in contact with the contact electrodes, contact adhesive force F_{adh}, which is a function of contact area, contact material and surface roughness, exists between the contacting surfaces, opposing the spring restoring force F_{k}. If F_{k} at the contacting position is larger than F_{adh}, when $V_{\text{Prog0/1}}$ is reduced below V_{PI}, at a critical value of $V_{\text{Prog0/1}} = V_{\text{RL}}$, F_{k} overcomes $F_{\text{elec}} + F_{\text{adh}}$ and contact breaks, where V_{RL} is the release voltage. In this case, the switch is *volatile* and has a hysteresis voltage V_{H}, as described in the previous chapter. The switch is *non-volatile* when the spring restoring force F_{k} of the movable beam during contact, is designed to be lower than F_{adh}, *i. e.*

$$F_{\text{k}}|_{x=g_{\text{cont}}} = F_{\text{k, cont}} = k_{\text{eff}} g_{\text{cont}} < F_{\text{adh}}. \tag{2.4}$$

The non-volatile switch remains in the contacting position even when $V_{\text{Prog0/1}}$ drops to zero. For $V_{\text{Prog0/1}} = 0\,\text{V}$, the net force on the beam at the contacting position towards the equilibrium position is given by

$$F_{\text{k, cont}} - F_{\text{adh}} = k_{\text{eff}} g_{\text{cont}} - F_{\text{adh}} < 0. \tag{2.5}$$

To reprogram the switch, electrostatic force is required to make sure the net force towards the opposite contact is positive:

$$F_{\text{elec}} + k_{\text{eff}} g_{\text{cont}} - F_{\text{adh}} > 0 \tag{2.6}$$

It is to be noted that the spring restoring force assists the reprogramming process by pulling the beam towards the equilibrium position. Hence the voltage required to program the switch from state "0" to state "1" should satisfy the condition:

$$\frac{\epsilon_0 A_{\text{act}} {V_{\text{Prog1}}}^2}{2 g_1^2} + k_{\text{eff}} g_{\text{cont}} > F_{\text{adh}}. \tag{2.7}$$

Here $g_1 > g_{\text{act}}$, *i. e.* the gap between Prog1 and the movable beam at state "0" is larger than the as-fabricated value. Fig. 2.1(d) shows the reprogramming of the NEM switch from state "0" to state "1." The minimum V_{Prog} required to reprogram the switch from state "0/1" to state "1/0" is higher than the voltage required to program the switch from the neutral state. The non-volatile NEM switch can function as a reprogrammable non-volatile memory cell or a reconfigurable interconnect.

2.3 CMOS BEOL Layers for NEM Design

A CMOS IC manufacturing process can be broadly divided into two parts: front-end-of-line (FEOL) process and back-end-of-line (BEOL) process. The FEOL process forms the semiconductor devices, while the BEOL process forms the metallic wires interconnecting the semiconductor devices to determine chip functionality and to form input/output ports for the chip.

The BEOL material stack comprises layers of metallic wire and via features embedded in low-permittivity (low-κ) dielectric insulating material. The schematic cross-sectional diagram from Fig. 2.2 shows a typical BEOL stack for the 65 nm process technology generation. The BEOL process comprises the following main steps:

- Firstly, photolithography and etching processes are used to pattern trenches for vias/ metal lines in the low-κ dielectric layer. Low-κ dielectrics are usually chosen as inter-metal dielectric (IMD) and inter-layer dielectric (ILD) materials because their low permittivity helps to reduce the parasitic capacitances between interconnects, leading

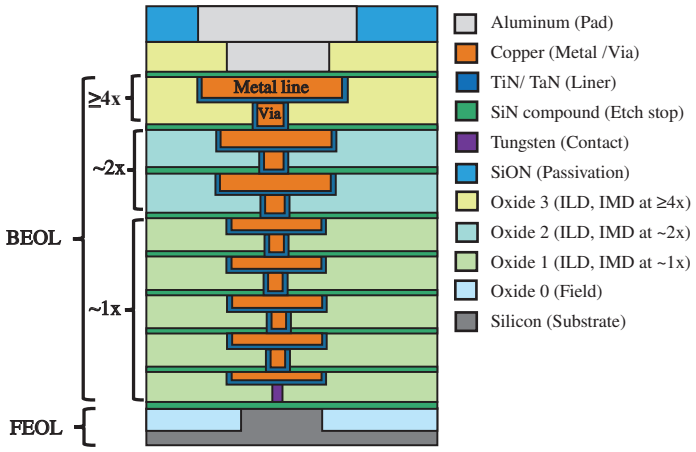

Figure 2.2: Schematic cross-section illustrating BEOL metallic interconnect layers formed in a standard CMOS IC manufacturing process, including metal and via layers, inter-metal dielectric (IMD) and inter-layer dielectric (ILD) layers.

to faster voltage signal propagation speed.

- Afterwards a few nanometers of liner material is conformally deposited, followed by the deposition of a thin copper film. The copper film acts a seed layer for subsequent copper electroplating process.

- The next step is electroplating copper to conformally fill out the trenches. Copper is commonly chosen as the interconnect material due to its high electrical conductivity. Because copper a highly diffusive material, the liner layer acts as a diffusion barrier between the copper and the low-κ dielectric. Often BEOL processes involve depositing a separate barrier layer before the liner layer, which can function as a diffusion barrier between the copper and the low-κ dielectric. TiN and TaN are good barrier materials; hence they are usually preferred as the liner material.

- Finally, chemical mechanical polishing (CMP) is used to planarize the surface in preparation for the formation of the next layer. Dummy metal structures are used to maintain uniform metal density all over the chip, improving the uniformity of the CMP process.

The number of metal/via layers have been increasing with the continuous scaling of device dimensions. State-of-the-art 10 nm and 7 nm process technologies provide up to 12 BEOL metal layers [24], [25]. The pitch of any metal layer, *i.e.* the minimum feature size/spacing of corresponding structures, depend on the position of the layer within the stack. The *minimum metal pitch* (MMP) is available for the lowermost layer of the stack, which means the feature size is the smallest at the bottom of the stack and it becomes increasingly larger towards the top of the stack. In Fig. 2.2, the ∼1x metal layers offer tightest metal pitches close to the MMP. The ∼2x metal layers have pitches close to twice the MMP, while ≥4x layers have the largest pitches. The tight-pitch metallic layers at the bottom of the BEOL stack are advantageous for facilitating small gaps for NEM structures, resulting in increased electrostatic force and lower-voltage operation.

BEOL metallization options can be leveraged to monolithically integrate NEM switches with CMOS technology [18–22]. The introduction of air gaps in the BEOL of state-of-the-art CMOS technology [26] provides the opportunity to construct multi-layer NEM devices with relative ease. The movable structure and the fixed electrodes in a NEM switch can be constructed by the metal/via lines. The ultra-scaled pitch of the metals layers from advanced technology nodes can be advantageous for creating small actuation gaps and contact gaps, leading to a smaller operating voltage. The operating voltage can be scaled down by maximizing the actuation area of the NEM switches. However, larger actuation area necessitates a larger footprint of the device. Hence a trade-off exists between the energy consumption and the chip area. Kwon *et al.* demonstrated the operation of laterally-actuated BEOL devices at a CMOS-compatible voltage, at the cost of a large footprint [21]. In order to facilitate a smaller operating voltage despite a small actuation area, the movable structure can be designed to be very compliant. Higher compliance, however, leads to reliability issues due to increased possibility of catastrophic pull-in [1, 23]. A potential solution to this problem is utilizing multiple metal and via layers for constructing the actuation electrode. A stack of multiple metal layers can provide a larger actuation area within a compact footprint, enabling low voltage operation without compromising the reliability. Sections 2.4 and 2.5 describe the geometry of NEM switches constructed with multiple metal/via layers.

2.4 Lateral BEOL NEM Switches

Fig. 2.3 illustrates the structure of a laterally-actuated BEOL NEM switch, simulated using Coventor MEMS+ compact model. The simulation model utilizes the bottom five metal layers and intermediary via layers of a standard 65nm BEOL stack, as shown in Fig. 2.3(a). The actuation area of the switch is formed by the overlap between the movable beam and actuation electrodes Prog0/1. The movable beam and Prog0/1 electrodes are constructed using five metal layers to maximize the actuation area within a limited footprint. The contact area can be controlled by changing the overlap length between the beam and D0/D1. To

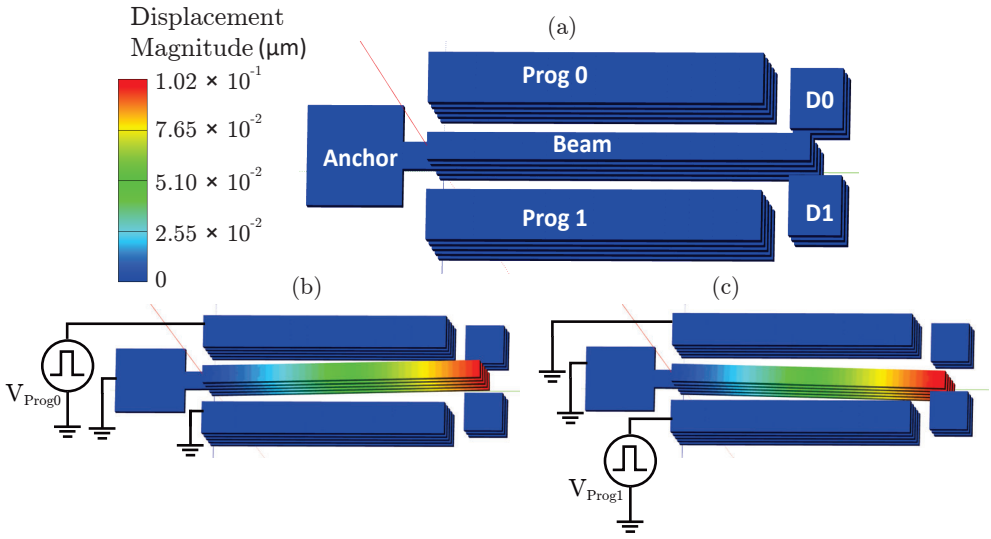

Figure 2.3: Simulated lateral NEM switch: (a) as- fabricated, (b) in state "0", and (c) in state "1", modeled using MEMS+. The color scale indicates displacement due to electrostatic actuation.

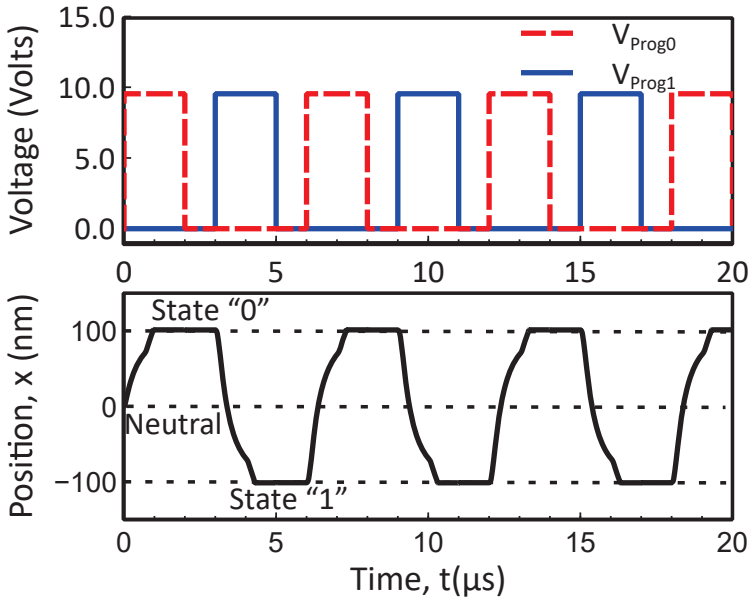

Figure 2.4: Simulated transient response of a lateral NEM switch: program voltage waveforms and beam tip position *vs.* time showing non-volatile and reprogrammable characteristics.

program the device into state "0", a voltage pulse is applied to Prog0 to electrostatically actuate the beam laterally into contact with data line D0. To change the programming state to "1", a voltage pulse is applied to Prog1. Figures 2.3(b) and 2.3(c) show programming into state "0" and state "1" respectively.

The transient response of a lateral NEM switch is simulated using the 3D compact model in Coventor MEMS+. Voltage pulses are applied alternately to Prog0 and Prog1 in order to reprogram the switch into state "0" and "1" respectively. The transient characteristics shown in Fig. 2.4 shows the position of the beam tip plotted in response to a series of voltage pulses applied to program electrodes Prog0 and Prog1. The neutral state of the NEM switch is represented by zero position of the beam tip. When the beam tip positioned at +100 nm, that indicates that it has contacted data line D0. Similarly contact with D1 is represented by the beam tip positioned at −100 nm. Here the as-fabricated contact gap g_{cont} is assumed to be 100 nm, which is very close to the minimum spacing facilitated by a typical 65 nm CMOS process. The switch is designed to be non-volatile and reprogrammable, which is evident from the characteristics. The beam retains its position at D0/D1 even after a voltage applied at Prog0/Prog1 is discontinued.

After the wafer comes out of the CMOS fabrication facility (the "foundry"), the dielectric stack around the movable beam must be selectively removed using plasma etch process in order to allow for physical movement and device actuation. Fig. 2.5(a) shows a schematic cross-section of a lateral NEM switch after typical 65 nm CMOS and BEOL metallization steps. Highly anisotropic plasma etch can be used to create high aspect-ratio trenches to remove the dielectric stack around the movable beam, as shown in Fig. 2.5(b). An etch process with low degree of anisotropy can be used to undercut the dielectric underneath the beam and complete the release process, which is illustrated in Fig. 2.5(c). This is referred to as the *release etch* process.

The upper metal layers, which have more relaxed pitches, are utilized for connecting the switch to the probe pads used for characterizing the devices. The etch process is masked by upper-level metal dummy structures. The Scanning Electron Microscope (SEM) image

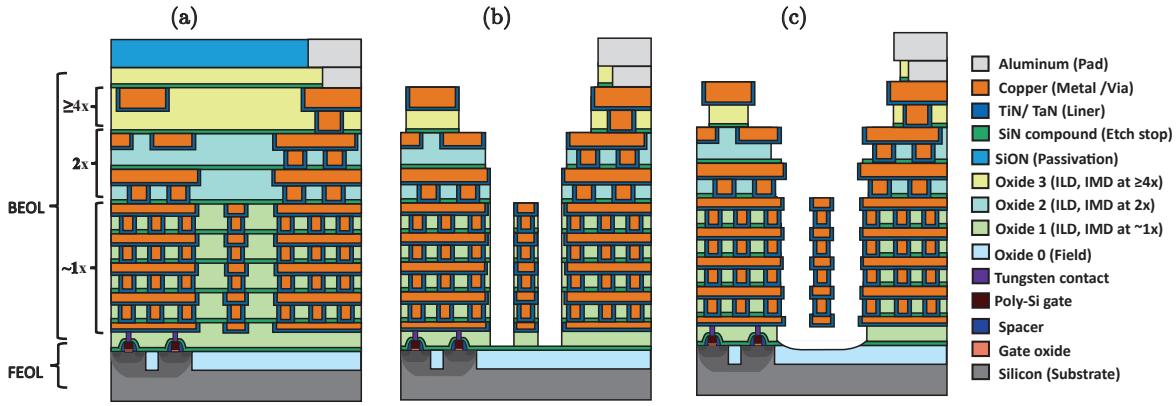

Figure 2.5: Schematic cross-section illustrating the release etch scheme for a lateral NEM switch showing (a) the lateral switch and corresponding BEOL metallic interconnect layers after standard CMOS and BEOL fabrication and (b) after anisotropic etch process and (c) after isotropic etch process.

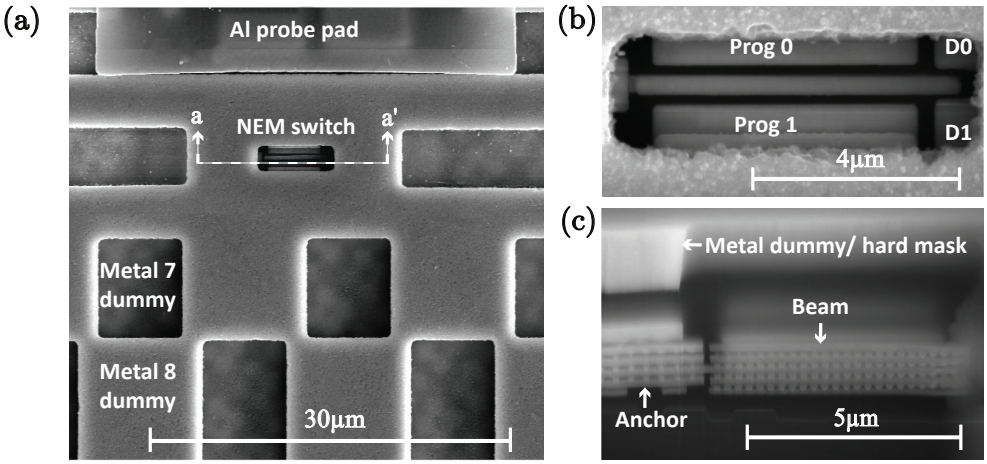

Figure 2.6: Scanning Electron Microscope (SEM) images of fabricated lateral NEM switch: (a) plan view showing the NEM switch, metal hard mask and probe pad, (b) zoomed-in plan view of the switch in as-fabricated neutral state, and (c) cross-sectional view along cutline a-a'.

in Fig. 2.6(a) demonstrates the plan view of a lateral NEM switch fabricated in a standard 65 nm CMOS node. Dummy structures from *Metal 8* and *Metal 7* layers are strategically placed to form a metal mask, so that a blanket etch process can be used for releasing the beam without any additional photolithographically defined masks. Fig. 2.6(b) shows a zoomed-in plan view of the NEM switch in as-fabricated neutral state, which is constructed utilizing *Metal 1-5* layers. Here the dielectric stack around the beam is removed using fluorine-based etch processes. The structural material for the electrodes and movable structure is copper with a thin outer layer of TaN liner. $CF_4 - CHF_3 -$ He plasma was used for highly anisotropic etching and $SF_6 - O_2$ plasma was used to provide the necessary undercut to release the movable beam. These etch processes, which are fully compatible with standard BEOL materials, will be discussed in greater details in the following chapter. The cross-sectional SEM image in Fig. 2.6(c) provides the lateral view of the movable beam showing the metal and via layers used to construct it. While multiple metal layers are used to maximize the actuation area, the contact gap is designed to be equal to the minimum spacing facilitated by the metal layers.

2.5 Vertical BEOL NEM Switches

The BEOL NEM switch can be designed more compactly by orienting the movable beam vertically. Fig. 2.7(a) shows the structure of the single-pole-double-throw (SPDT) vertical NEM switch simulated using Coventor MEMS+. The device is formed using five metal layers (*Metal 1-5*) and intermediary via layers. The bottom four layers (*Metal 1-4*) are used to construct the actuation electrodes Prog0 and Prog1. The top device layer *Metal 5* is used to make contact electrodes D0 and D1. To program the device, a voltage pulse is applied to either of the actuation electrodes, *i.e.* Prog0 or Prog1 to electrostatically actuate the beam into contact with a data line (D0 or D1 respectively). Figures 2.7(b) and 2.7(c) show programming into state "0" and state "1" respectively.

Fig. 2.8(a) and Fig. 2.8(b) demonstrate the schematic cross-section of a vertical NEM

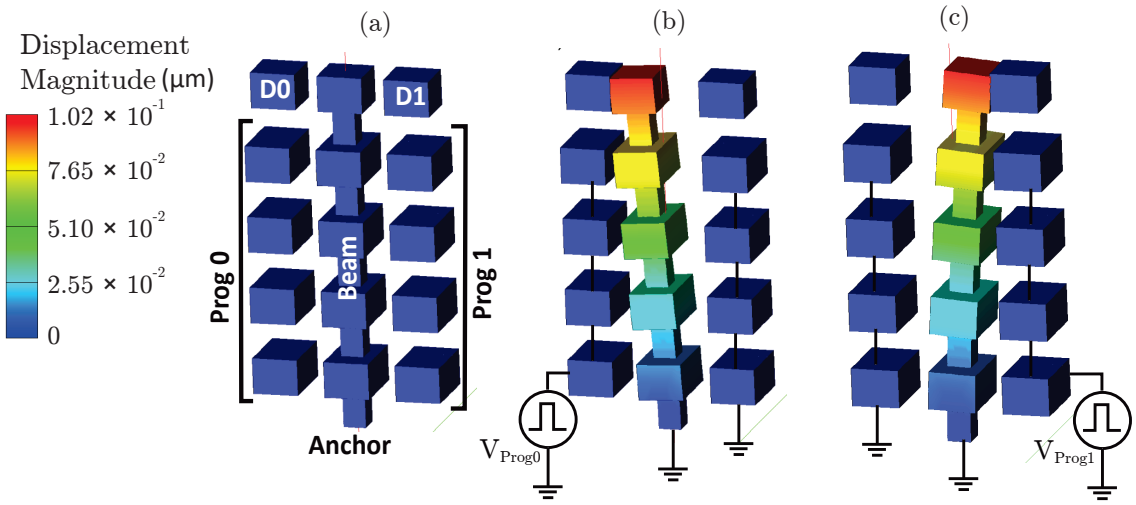

Figure 2.7: Simulated vertical NEM switch: (a) as-fabricated, (b) in state "0" and (c) in state "1", modeled using MEMS+. The color scale indicates displacement due to electrostatic actuation.

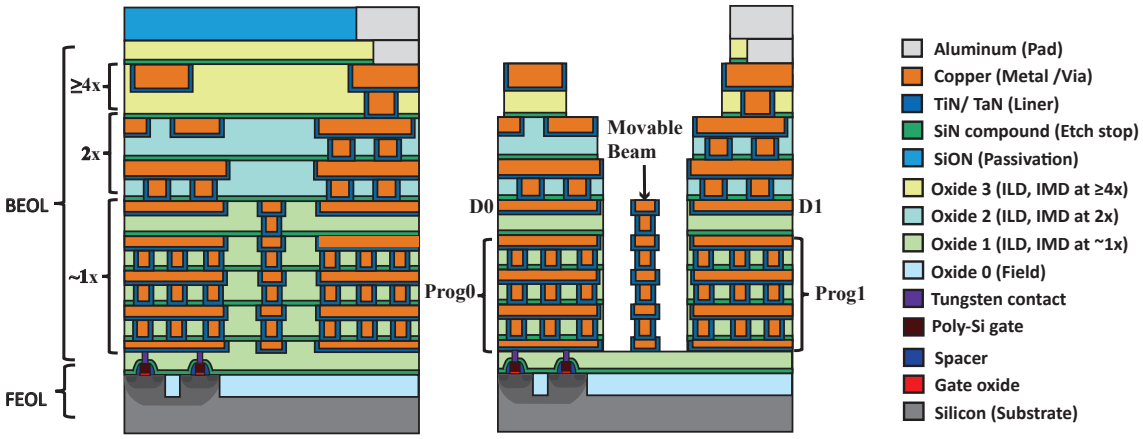

Figure 2.8: Schematic cross-section illustrating the release etch scheme for a vertical NEM switch showing (a) the vertical switch and corresponding BEOL metallic interconnect layers after standard CMOS and BEOL fabrication, and (b) after highly anisotropic release etch process.

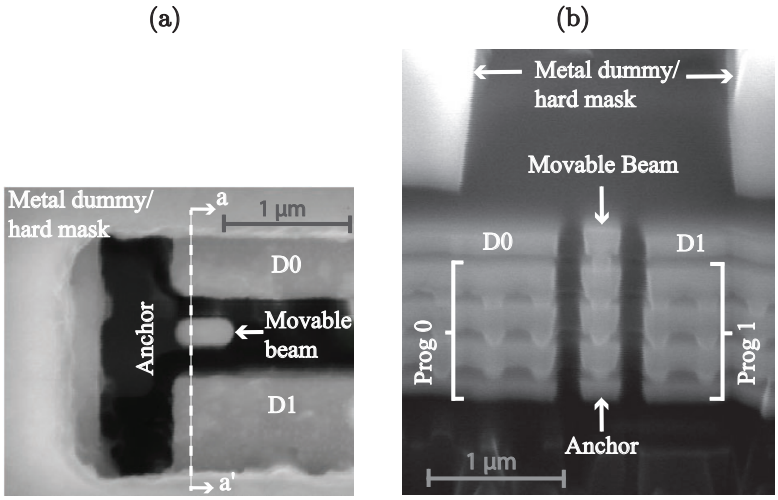

Figure 2.9: SEM images of fabricated vertical NEM switch showing (a) plan view of as-fabricated neutral state, and (b) cross-sectional view along cutline a-a' after standard CMOS and BEOL fabrication.

switch before and after the release etch process respectively. The vertical movable beam is anchored at the bottom; so it is not necessary to undercut the dielectric underneath the beam. The ILD layers between the metal layers of the beam need to be undercut by a small amount in order to make the beam more compliant and assist its movement. Hence the release etch process should have a high degree of anisotropy facilitating a small amount of undercut.

Fig. 2.9(a) shows an SEM image of a vertical NEM switch in the as-fabricated neutral state, where the movable beam is separated from the program and contact electrodes by air gaps. The switch is fabricated using a standard 65 nm CMOS process and subsequent etch steps with fluorine-based plasma. No additional lithography steps were employed. Similar to the lateral switch, the structural material for the electrodes and movable structure is copper with a thin outer layer of TaN liner. Longer $CF_4 - CHF_3 - He$ plasma etch steps were combined with shorter $SF_6 - O_2$ plasma etch steps to control the anisotropy of the etch process. The high degree of anisotropy makes sure that the movable beam is sufficiently compliant and anchor underneath is not damaged. Fig. 2.9(b) shows the cross-section of the

fabricated vertical NEM switch showing all the metal/ via structures from the interconnect layers. The contact electrodes, D0/1, are isolated from the corresponding program electrodes (Prog0/1) by an ILD layer.

2.6 Summary

The switching energy and the operating voltage of a NEM switch can be lowered by maximizing the actuation area, minimizing the actuation gap and the contact gap. The BEOL NEM switch increases the actuation area within a limited footprint by utilizing multiple layers of metal for actuation. The minimum values of contact gap and actuation gap are limited by the design constraints of the CMOS process. A BEOL movable beam can be designed to actuate either laterally or vertically. Whether the NEM switch is volatile or non-volatile depends on the relationship between the spring stiffness of the beam and the contact adhesive force between the beam and contact electrodes. The contact adhesive force can be changed by modifying the contact area, while the movable beam design can be tailored to change the stiffness. NEM switches can be designed to function as NV-memory cells by increasing the contact area and/or making the beam design more compliant. After finishing the CMOS processing, a release etch process is required to free the movable beam by removing the stack of dielectric around it. The etch process for the vertical design needs to have a greater degree of anisotropy, compared to that required for the lateral design. The vertical design has a more compact footprint than the lateral design, however the actuation area of the vertical design is also limited. The next chapter presents a comparative analysis of the performances of the vertical and lateral switches and their respective optimization methods.

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Chapter 3

Optimzation of BEOL NEM Switches

3.1 Introduction

The minimum metal pitch (MMP) is available at the lowermost metal layer in the back-end-of-line (BEOL) material stack, and the metal pitch becomes increasingly relaxed towards the top of the stack. To take advantage of the MMP for achieving the smallest electrode gaps (desirable for achieving the largest electrostatic force per Volt and per unit layout area), then, NEM switches should be built utilizing the lowermost layers of the BEOL stack. Earlier demonstrations of BEOL NEM switches include torsionally actuated [1] and laterally actuated switches [2–4], fabricated using the topmost layers of the BEOL stack, which makes the release process straightforward. The corresponding release methods involved isotropic etch processes with either wet hydrofluoric (HF) acid [2] or HF vapor [1, 4]. However, wet etch processes are not suitable for NEM devices with smaller dimensions, since capillary forces can draw the released structures into contact and cause stiction-induced failure [5]. The standard BEOL stack contains silicon-nitride compounds and low-κ dielectrics, which are not compatible with HF vapor etching. Hence the release-etch process needs to be optimized for compatibility with the BEOL stack materials and for etching high-aspect-ratio trenches to release NEM switches at the bottom of the BEOL stack.

The design parameters of a BEOL NV-NEM switch determine the minimum program voltage and program/readout speed. The movable beam should be compliant/ less stiff to achieve non-volatile behavior. However, the more compliant the beam is, the greater are the chances of *catastrophic failure*, occurring due to pull-in of the beam into contact with a program electrode, and resulting in stiction. Also, a compliant design increases the possibility of stuck-on failure due to stiction between the beam and a contact electrode. Decreasing the contact area is helpful to lower the contact adhesive force and thereby the chances of stuck-on failure; however, this can result in larger contact resistance, which generally is undesirable. (The contact resistance is preferred to be small to achieve a low RC readout delay.) Hence there is a trade-off between the readout speed and switch reliability. Moreover, another trade-off exists between the program energy and program delay. Since mechanical delay dominates the program delay, a larger program voltage is advantageous for achieving a smaller program delay, because it generates a stronger electrostatic force between the beam and the program electrode. But this is achieved at the cost of larger program energy. Hence the device geometry must be optimized to meet multiple NV-NEM switch performance specifications.

3.2 Process Challenges

Compared to wet-etching processes, anhydrous HF vapor etching has a lower risk of causing stiction due to capillary forces and hence is a common release-etch process for M/NEM structures. However, HF vapor etch is not a viable method for etching deep trenches in a standard BEOL dielectric material stack since the etch-stop layers usually contain silicon-nitride compounds, which cannot be etched away effectively by HF. Moreover, advanced BEOL processes use a number of different low-κ dielectrics as the inter-metal dielectric (IMD) and inter-layer dielectric (ILD) materials. Often these dielectrics do not form volatile compounds upon exposure to HF and as a result form undesirable etch residues. The scanning electron microscope (SEM) images in Fig. 3.1 show a plan view and cross-sectional view of a lateral

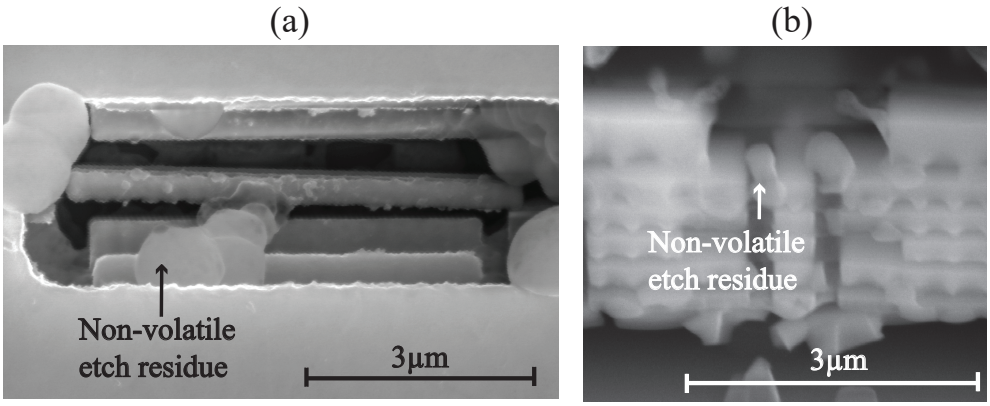

Figure 3.1: (a) Planar and (b) cross-sectional SEM images of a fabricated lateral NEM switch showing non-volatile etch residue resulting from exposure to anhydrous HF vapor and ethanol.

NEM switch implemented with multiple BEOL layers, after exposure to anhydrous HF vapor and ethanol. The silicon-nitride-containing dielectric layers are deformed upon exposure to anhydrous HF vapor and ethanol. Additionally, non-volatile residual compounds can be seen inside the actuation gap and contact gap, causing device failure by impeding movement of the beam.

The release-etch process of a NEM switch fabricated in the bottom layers of the BEOL stack requires removal of a dielectric stack consisting of IMD, ILD and etch-stop layers. This dielectric stack is typically a few microns thick. The etch process requires good selectivity to etch all BEOL dielectric materials preferentially over the BEOL metallic materials. Since isotropic etch processes have the same etch rate in both vertical and lateral directions, they are not suitable for etching narrow (sub-100 nm wide) and high-aspect-ratio trenches. Moreover, small metal dummy structures are embedded in each IMD layer to ensure surface uniformity during CMP; long isotropic etch processes will undercut the ILD layers underneath the dummy structures, causing them to float away and land elsewhere, effectively contaminating the sample. Therefore a highly anisotropic etch process is required. A capacitively coupled plasma (CCP) reactive ion etching (RIE) process is well-suited [6]. Typical chal-

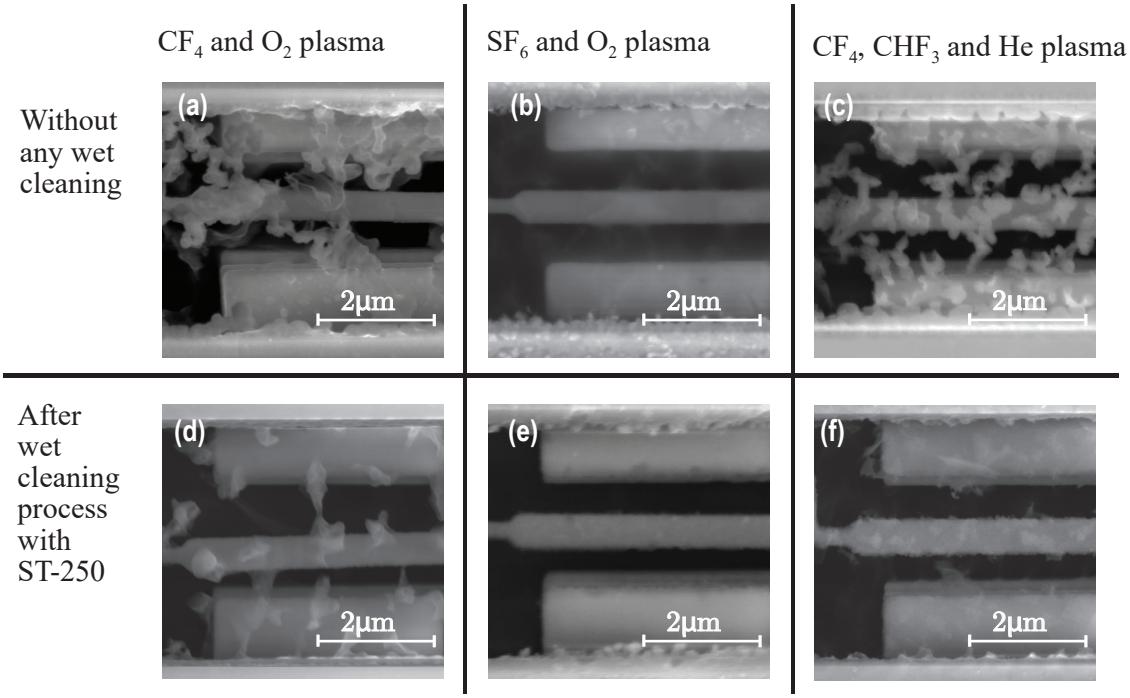

Figure 3.2: SEM images showing a portion of a BEOL NEM switch after etching with different plasma recipes.

lenges associated with the anisotropic etch process include production of non-volatile etch residue and a tapered (non-vertical) etched-sidewall profile. The etch process is optimized in this work to overcome these challenges and achieve gaps $\leq 100\,\text{nm}$.

3.3 Release-Etch Process Optimization

The low-κ dielectrics used for BEOL IMD and ILD often consist of doped silicon glass which can be etched by fluorine-based plasma gas mixtures, *e.g.* CF_4-O_2 plasma, SF_6-O_2 plasma [7] and CF_4-CHF_3-He [8]. Fig. 3.2 compares the results of etching a sample BEOL stack with different plasma gas mixtures, *i.e.* CF_4-O_2, SF_6-O_2 and CF_4-CHF_3-He, before and after wet cleaning with an amine-based copper compatible cleaning solution (ST-250). All the samples were etched for a total duration of 40 minutes. The wet process included soaking

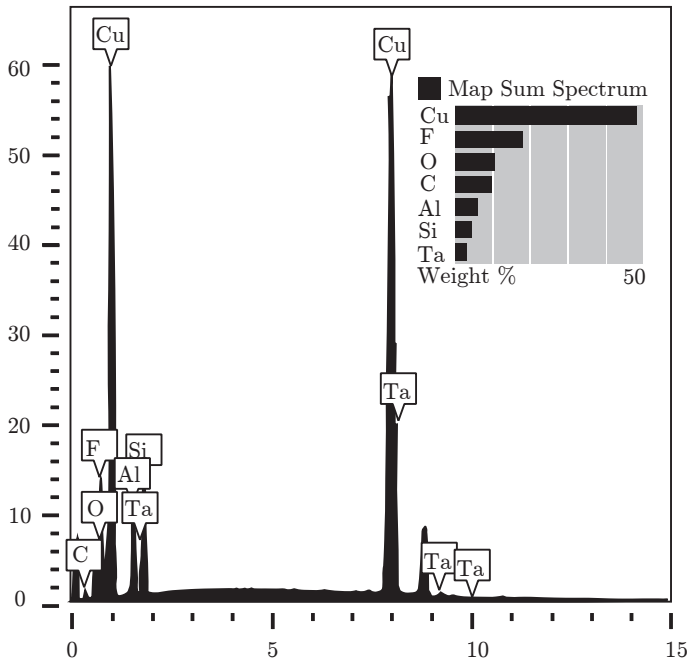

Figure 3.3: Energy-dispersive X-ray spectroscopy (EDS) spectrum of a section of a BEOL NEM switch after etch with CF_4-CHF_3-He CCP.

the sample in ST-250 solution for 20 minutes at 35^{o}C and rinsing with DI water. It can be observed that the recipes including O_2 result in a cleaner metal surface, as O_2 reduces build-up of fluorocarbon polymer residue on the etched sidewalls. Moreover, SF_6 offers the highest concentration of reactive species. Hence SF_6-O_2 etch chemistry is observed to generate the least amount of non-volatile etch products, while the etch recipes with CF_4 or CHF_3 leave a large amount of visible fluorocarbon polymer residue. The wet cleaning step is found to be effective for reducing the amount of non-volatile etch residue on the samples.

Energy-dispersive X-ray spectroscopy (EDS) is used to characterize the etch residue. Fig. 3.3 shows the EDS results of a sample after etching with CF_4-CHF_3-He CCP. It is evident from the corresponding elemental distribution maps in Fig. 3.4 that Cu, Ta, Al, F, O and Si atoms/ions are present in the etch residue. The presence of metal ions, *i.e.* Cu, Ta and Al increases the electrical conductivity of the residue. Hence metal-contaminated

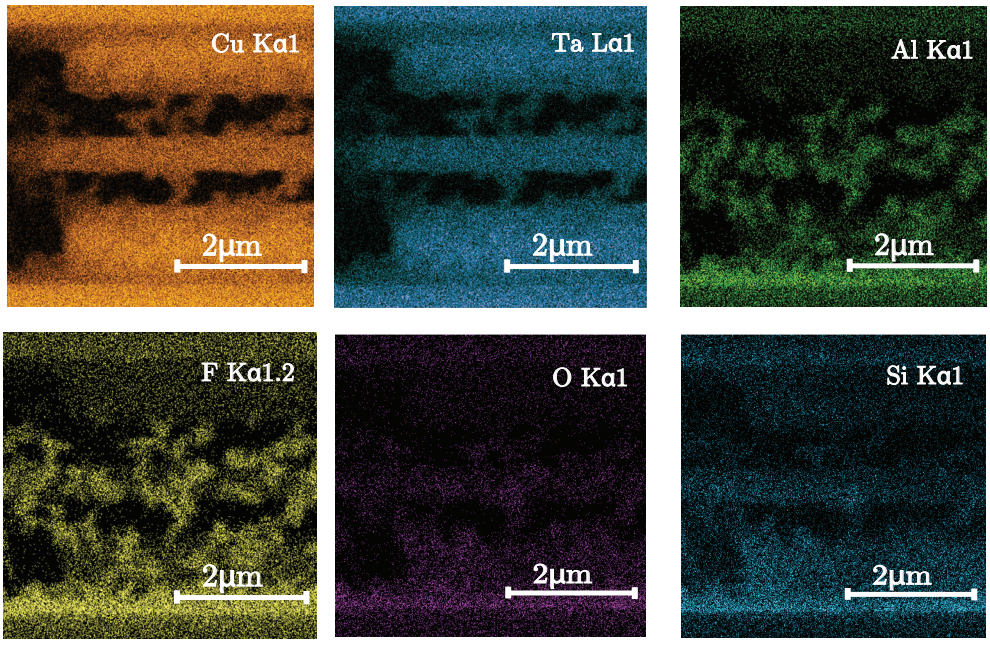

Figure 3.4: Energy-dispersive X-ray spectroscopy (EDS) elemental distribution maps of a section of a BEOL NEM switch after etch with CF_4-CHF_3-He CCP.

etch compounds create parasitic conduction paths between electrodes leading to leakage current. Typically the presence of parasitic conduction is evident through abnormally high gate (program electrode) leakage currents. The leakage is observed to be worse when O_2 is introduced in the plasma, which might be caused by ionization of copper ions through oxidation of the metal mask surface [9].

The polymeric etch by-products also contribute towards undesirable micromasking of the etch process. The amount of re-sputtered etch compound decreases with the distance between metal mask and trench bottom, as the compounds have limited mobility in plasma [10]. Hence cleaning the non-volatile etch compounds during the initial stage of etching can prevent micro-masking for the rest of low-κ dielectric etch process [6, 10].

Table 3.1 shows the etch recipe optimized for a lateral BEOL NEM switch fabricated using a standard 65 nm process. A cleaning step with ST-250 takes place after a total etch time of 60 minutes to remove the non-volatile etch residue. The local etch rate depends

Table 3.1: Optimized process for post-CMOS-fabrication release of lateral BEOL NEM switches. The etch tool used for this process is a *Plasma-Therm PK-12 RIE*.

Process details	**Total duration**
40 sccm CF_4, 10 sccm CHF_3 and 40 sccm He, 150 Watts, 89 mTorr	60 minutes
Wet cleaning with ST-250 soak, 35^{o}C	30 minutes
DI water rinse	
40 sccm CF_4, 10 sccm CHF_3 and 40 sccm He, 150 Watts, 89 mTorr	20 minutes
60 sccm SF_6 and 6 sccm O_2, 150 Watts, 93 mTorr	20 minutes
40 sccm CF_4, 10 sccm CHF_3 and 10 sccm He, 150 Watts, 89 mTorr	40 minutes
60 sccm SF_6 and 6 sccm O_2, 150 Watts, 93 mTorr	20 minutes

on the size of metal hard-mask opening and the etching depth, and it gradually reduces as the etch goes deeper. This results in a tapered sidewall etch profile. The first SF_6-O_2 etch step aims to open up the narrow trench with less anisotropy compared to the CF_4-CHF_3-He CCP. The last SF_6-O_2 CCP step in Table 3.1 provides the necessary undercut to the lateral BEOL NEM switch in order to allow the beam to move.

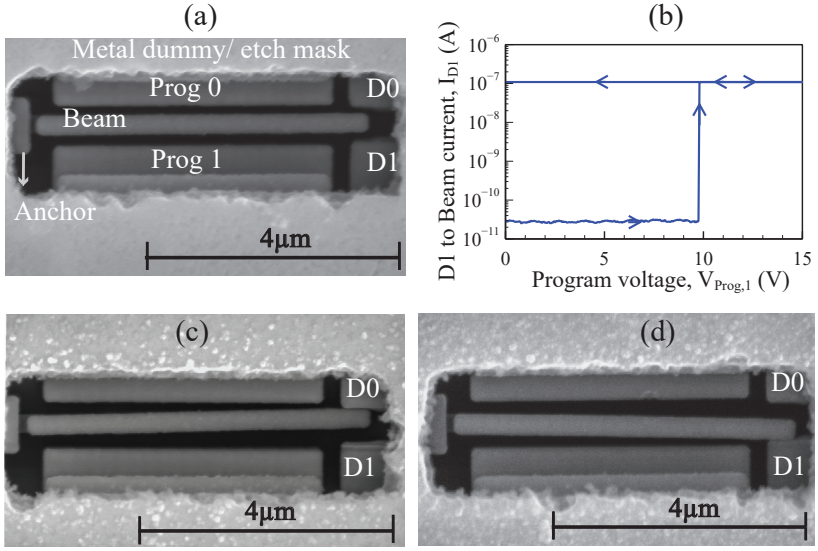

Figure 3.5: (a) SEM image of a lateral BEOL NEM switch in as-fabricated neutral state after the release-etch process, (b) corresponding current *vs.* voltage characteristics showing programming to state "1" from state "0", and SEM images of the programmed switch in (c) state "0" and (d) state "1".

Fig. 3.5 (a) shows the SEM image of a lateral BEOL NEM switch in neutral state after going through the release etch process. The measured current-*vs.*-voltage characteristics from Fig. 3.5 (b) show the programming of the lateral NEM switch from state "0" into state "1". The programming voltage, V_{Prog1} was swept bidirectionally with 1.2 V applied between contact electrode D1 and the beam to demonstrate the abrupt change of state from "0" to "1" when V_{Prog1} exceeds 9.75 V. The current is artificially limited to 100 nA to avoid Joule-heating-induced contact welding during quasi-static measurement. Fig. 3.5 (c) Fig. (d) show planar SEM images of the lateral BEOL NEM switch programmed to state "0" and to state "1", respectively.

A vertical NEM switch has a vertically-oriented movable beam anchored at its bottom end, so undercutting of the movable beam is not needed. Hence the SF_6-O_2 etch time is shorter for the vertical NEM switch, as can be seen in the optimized recipe in Table 3.2. A SEM image of a vertical BEOL NEM switch in as-fabricated neutral state is shown in Fig. 3.6 (a). Measured current-*vs.*-voltage characteristics for a programming operation are shown in Fig. 3.6 (b). Note that the vertical switch requires a higher voltage to be programmed, compared to the lateral switch. This is because the actuation area of a vertical switch is typically smaller. However, the vertical switch has the advantage of a smaller footprint. SEM images of a vertical BEOL NEM switch programmed to state "0" and state "1" are

Table 3.2: Optimized process for post-CMOS-fabrication release of vertical BEOL NEM switches. The etch tool used for this process is a *Plasma-Therm PK-12 RIE*.

Process details	**Total duration**
40 sccm CF_4, 10 sccm CHF_3 and 40 sccm He, 150 Watts, 89 mTorr	60 minutes
Wet cleaning with ST-250 soak, 35^{o}C	30 minutes
DI water rinse	
40 sccm CF_4, 10 sccm CHF_3 and 40 sccm He, 150 Watts, 89 mTorr	20 minutes
60 sccm SF_6 and 6 sccm O_2, 150 Watts, 93 mTorr	10 minutes
40 sccm CF_4, 10 sccm CHF_3 and 10 sccm He, 150 Watts, 89 mTorr	20 minutes
60 sccm SF_6 and 6 sccm O_2, 150 Watts, 93 mTorr	10 minutes
40 sccm CF_4, 10 sccm CHF_3 and 10 sccm He, 150 Watts, 89 mTorr	20 minutes

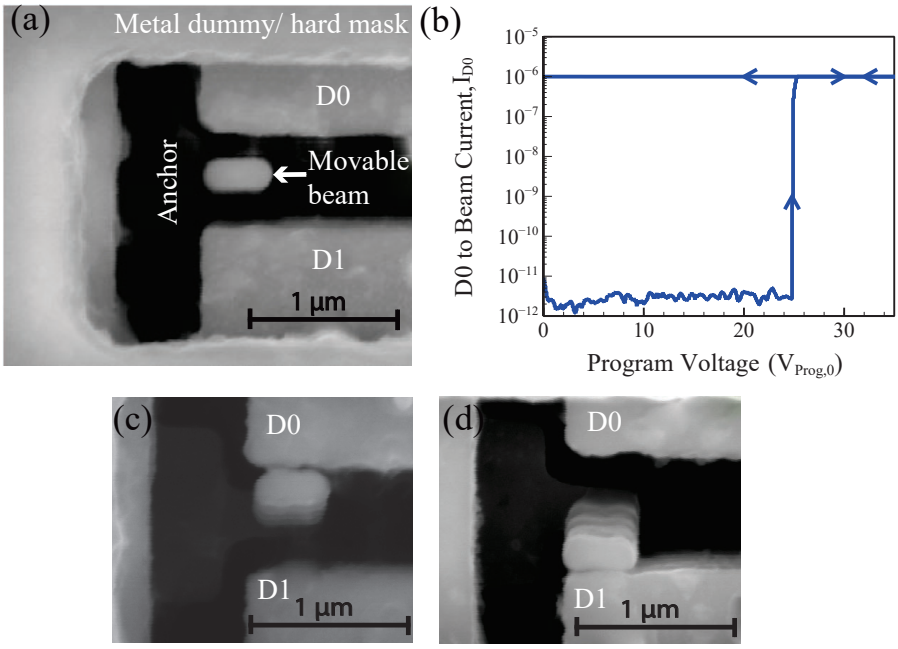

Figure 3.6: (a) SEM image of a vertical BEOL NEM switch in as-fabricated neutral state after the release-etch process, (b) corresponding current *vs.* voltage characteristics showing programming to state "0" from state "1", and SEM images of the programmed switch in (c) state "0" and (d) state "1".

shown in Fig. 3.6 (c) and (d) respectively.

3.4 Design Optimization

3.4.1 Lateral NV-NEM switch

The spring restoring force of a movable beam, given by Equation 2.2, is a function of effective stiffness of the beam (k_{eff}) and displacement from the as-fabricated neutral position (x). Hence F_{k} can be tuned to be larger by increasing the effective stiffness (k_{eff}) of the beam. The effective stiffness of a simple cantilever beam, with a point load applied to the tip, is given by

$$k_{\text{eff}} = \frac{EW_b^3 H_b}{4L_b^3}, \tag{3.1}$$

where E is the Young's modulus or the modulus of elasticity. W_b, L_b and H_b are the width, length and height of a lateral beam, as shown in Fig. 3.7. The height and length of the laterally actuated beam contribute to the actuation area and footprint of the NEM switch. A larger actuation area is preferred within a limited footprint, in order to keep the minimum program voltage lower. So modifying the width W_b is a simple way of tuning the stiffness of a laterally actuated beam, without changing the actuation area or footprint. Assuming the contact asperities to be evenly distributed, the contact area A_{cont} can be increased to boost F_{adh}, which can be accomplished by increasing the overlap between the beam and the contact electrodes.

For non-volatile operation of the BEOL NEM switch, the design has to ensure that $F_{\text{k, cont}} < F_{\text{adh}}$, where F_{adh} is the contact adhesive force between the beam and the contact electrode. Fig. 3.8 shows measured current *vs.* voltage characteristics for three lateral BEOL NEM switches with varied beam stiffness and contact area values. All three characteristics were obtained by sweeping V_{Prog1} up and down, with 1.2 V and 0 V applied to D1 and the beam, respectively. The maximum ON-current I_{D1} is artificially limited to 100 nA for all three cases. Among the three switch characteristics, Fig. 3.8 (a) demonstrates the highest effective stiffness k_{eff} and smallest contact area A_{cont}. Hence $F_{\text{k, cont}}$ is very large compared to F_{adh}, as evident by the large switching voltage ($\sim$ 27V) and the small hysteresis voltage, V_H ($\sim$ 2V). The switch in Fig. 3.8 (b) has lower k_{eff}, reducing the switching voltage to

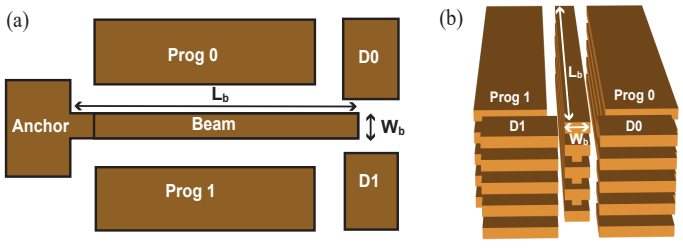

Figure 3.7: (a) Schematic plan view and (b) 3D model of a laterally actuated NEM switch showing different dimensions.

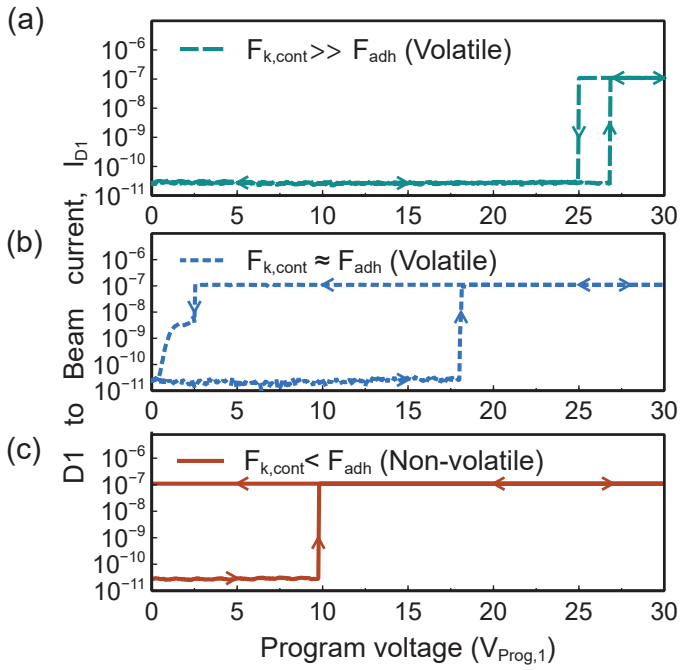

Figure 3.8: Measured current *vs.* voltage characteristics for three different lateral BEOL NEM switches showing volatile or non-volatile switching behavior.

$\sim$ 17V, however, k_{eff} is not low enough to satisfy the condition for non-volatile behavior. A smaller k_{eff} results in the non-volatile switch characteristics shown in Fig. 3.8 (c).

To ensure non-volatile operation across a range of F_{adh} values, the beam can be made very compliant *i.e.* k_{eff} can be designed to be very low. However, a larger $F_{\text{adh}}/F_{\text{k, cont}}$ necessitates a larger F_{elec}, *i.e.*, a larger V_{Prog} to change the state of the NEM switch. This means that a larger $V_{\text{Prog}}/V_{\text{PI}}$ is required for reprogramming. Here V_{PI} is the initial voltage required to program the switch quasi-statically from its as-fabricated neutral state to either of the contacting states, as described in Section 2.2. If $V_{\text{Prog}}/V_{\text{PI}}$ is too large, however, catastrophic pull-in (CPI) will occur. Moreover, larger $V_{\text{Prog}}/V_{\text{PI}}$ results in larger program energy, which is undesirable. A wide design window for $V_{\text{Prog}}/V_{\text{PI}}$ is desirable. The device design parameters also should be chosen to provide for $V_{\text{CPI}}/V_{\text{PI}} \gg 1$, where V_{CPI} is the program voltage leading to catastrophic pull-in.

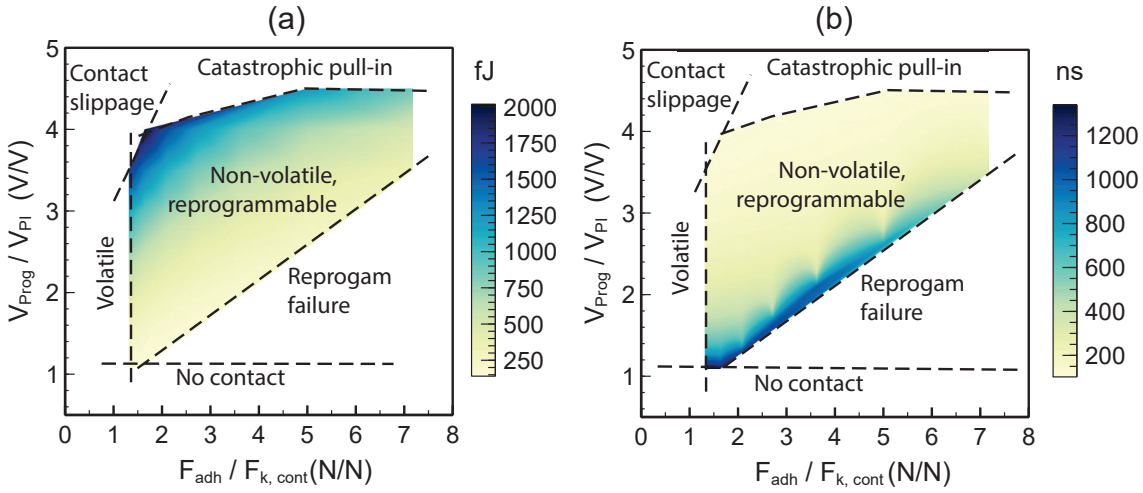

Figure 3.9: Simulated (a) energy and (b) delay contour plots as functions of $V_{\mathrm{Prog}}/V_{\mathrm{PI}}$ and $F_{\mathrm{adh}}/F_{\mathrm{k,\,cont}}$, showing various regions of operation delineated by the dashed lines.

The simulation results presented in Fig. 3.9 show how the program energy and program delay depend on the $V_{\mathrm{Prog}}/V_{\mathrm{PI}}$ and $F_{\mathrm{adh}}/F_{\mathrm{k,\,cont}}$ ratios. The MEMS+ 3D compact simulation model assumes a lateral BEOL NEM switch comprising five BEOL metal layers and intermediary via layers in a 65 nm process technology. The contact adhesive force F_{adh} is assumed to be 100 nN, while k_{eff} is modified by changing the width of the lateral beam. The regions in the contour plots showing finite energy/delay values, correspond to functional switches. Fig. 3.10(a) and (b) show simulated program voltage waveforms and resulting beam tip position for the *non-volatile, re-programmable* design region bounded by various design constraints. In the *volatile* design region, $F_{\mathrm{adh}}/F_{\mathrm{k,\,cont}} < 1.3$, which makes F_{adh} insufficient to retain the contacting state without any applied voltage, as shown in the simulated beam position waveform in Fig. 3.10(c). It is notable that the *volatile* design region starts at $F_{\mathrm{adh}}/F_{\mathrm{k,\,cont}} = 1.3$ rather than unity, since structural oscillations make the device volatile unless F_{adh} is sufficiently larger than $F_{\mathrm{k,\,cont}}$. The *no contact* design region is defined by $V_{\mathrm{Prog}}/V_{PI} < 1.1$. This region is characterized by insufficient electrostatic force to establish good contact. In the *reprogram failure* design region, the switch cannot be reprogrammed by the applied voltage

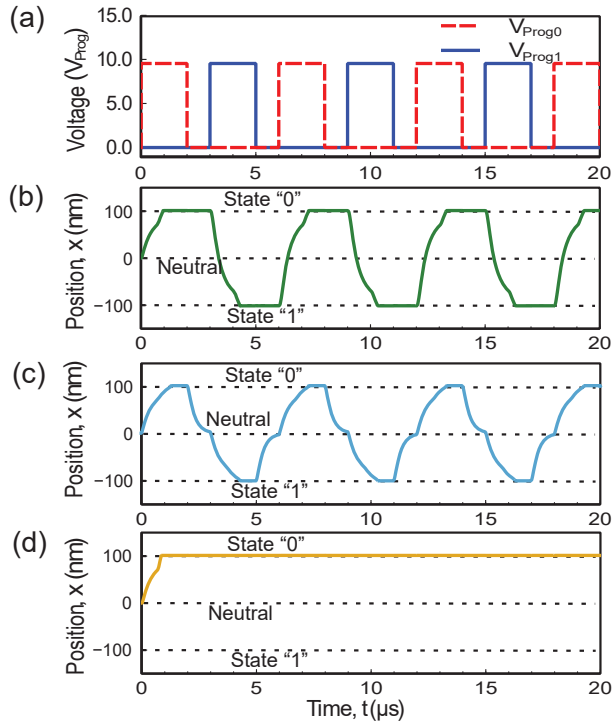

Figure 3.10: Simulated transient response of lateral BEOL NEM switches showing (a) program voltage waveforms, and the corresponding position of the beam tip for (b) non-volatile and re-programmable operation, (c) volatile operation, and (d) reprogram failure.

and it is stuck in one contacting state. The minimum $V_{\text{Prog}}/V_{\text{PI}}$ required to change the programmed state increases with increased $F_{\text{adh}}/F_{\text{k, cont}}$, since the program voltage has to compensate for the increased adhesive force. Fig. 3.10(d) shows the simulated waveform for the *reprogram failure* design region. The *catastrophic pull-in* region is defined by very high values of $V_{\text{Prog}}/V_{\text{PI}}$. Low $F_{\text{adh}}/F_{\text{k, cont}}$ at higher values of $V_{\text{Prog}}/V_{\text{PI}}$ makes the switch less prone to catastrophic pull-in; however, the beam can slip out of contact for excessively large program voltages. This phenomenon occurs in the *contact slippage* region.

All the different regions of operation are mapped into the energy and delay contour plots in Fig. 3.11(a) and (b), respectively, as a function of effective stiffness k_{eff} and program voltage V_{Prog}. As seen from these plots, program energy is minimized for lower values of program voltage V_{Prog}, while program delay is minimized for higher values. It should be

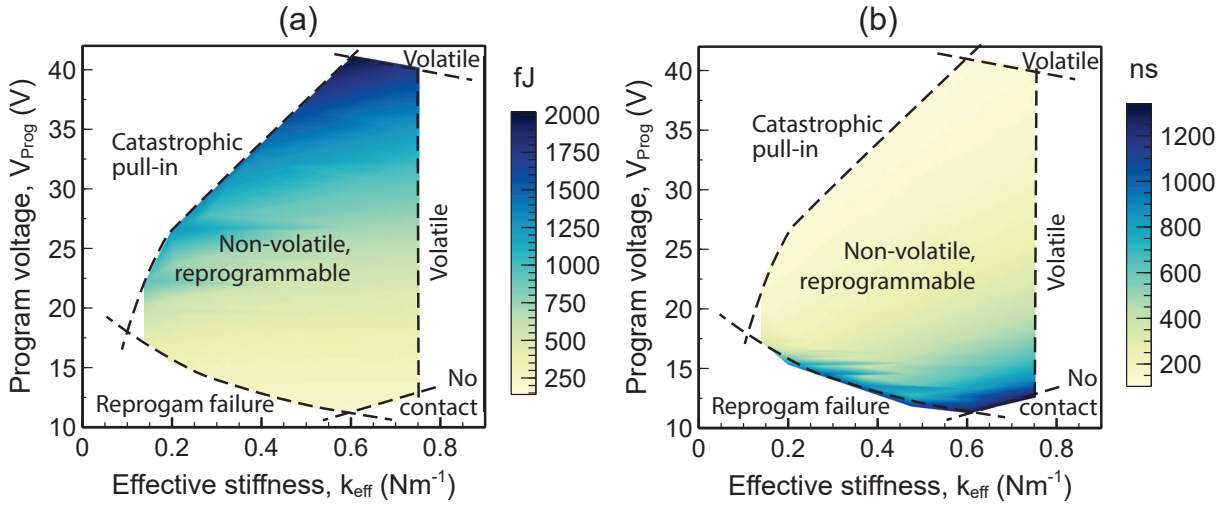

Figure 3.11: Simulated (a) energy and (b) delay contour plots for a lateral BEOL NEM switch as functions of $V_{\rm Prog}$ and $k_{\rm eff}$, showing various regions of operation delineated by the dashed lines. F_{adh} is assumed to be 100nN.

noted that the range of operational $V_{\rm Prog}$ diminishes as the effective stiffness is decreased. Hence NEM switch designs with stiffer beams offer better reliability.

Simulated *minimum* reprogramming energy contour, as a function of $k_{\rm eff}$ for different values of contact adhesive force $F_{\rm adh}$ (ranging from 60 nN to 1100 nN) is plotted in Fig. 3.12 (a). $k_{\rm eff}$ is varied by changing the beam width $W_{\rm b}$, while contact adhesive force $F_{\rm adh}$ is varied by changing the contact area $A_{\rm cont}$, assuming $F_{\rm adh}$ per unit area is constant at1800 nN/µm^2 for different contact sizes, *i.e.*, assuming uniform distribution of contact asperities. The contour plot has three distinct design regions. The NEM switch is fully functional in the *non-volatile and reprogrammable* region, where $F_{\rm k,\,cont} < F_{\rm adh}$ and reprogramming voltage can be raised high enough to ensure that $F_{\rm elec} + F_{\rm k,\,cont} > F_{\rm adh}$ without causing catastrophic pull-in. Catastrophic pull-in and stuck-on failure prevent proper operation when the beam is too compliant, as shown by the *stuck* region. $F_{\rm k,\,cont} > F_{\rm adh}$ in the *volatile* region, hence the switch does not retain its programmed state. The NEM switch is found to be most energy-efficient when both $k_{\rm eff}$ and $F_{\rm adh}$ are small.

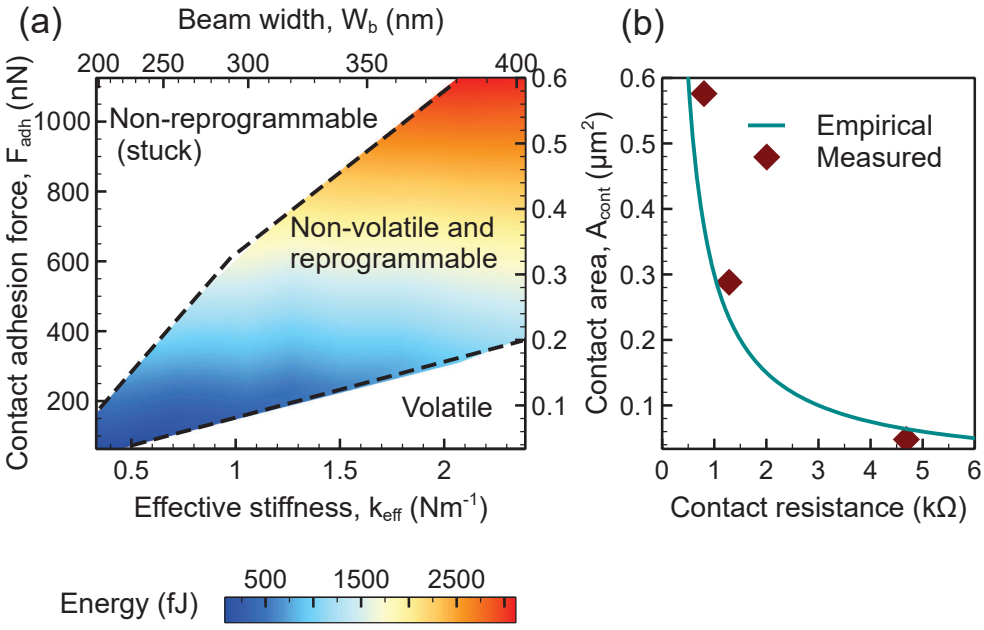

Figure 3.12: (a) Minimum reprogramming energy contour plot as a function of effective stiffness or beam width and contact adhesive force or contact area and (b) contact resistance R_{cont} as a function of contact area [11].

However, smaller F_{adh} also corresponds to smaller contact area A_{cont}, which leads to a higher contact resistance R_{cont}, as shown in Fig. 3.12(b). Smaller contact resistance R_{cont} is desirable for minimizing the RC readout delay of the NV-NEM switch. The contact resistance is measured to be in the range of 0.8-4.7 kΩ for a NEM switch implemented with 65 nm process technology [11]. A NEM switch design should be optimized to have both contact resistance and program energy within the acceptable range.

3.4.2 Vertical NV-NEM switch

A similar design optimization methodology can be followed for BEOL vertical NEM switches. The effective stiffness of the vertically oriented beam is a function of the dimensions of the vias and the height of the beam, which is dependent on the number of metal/via layers used

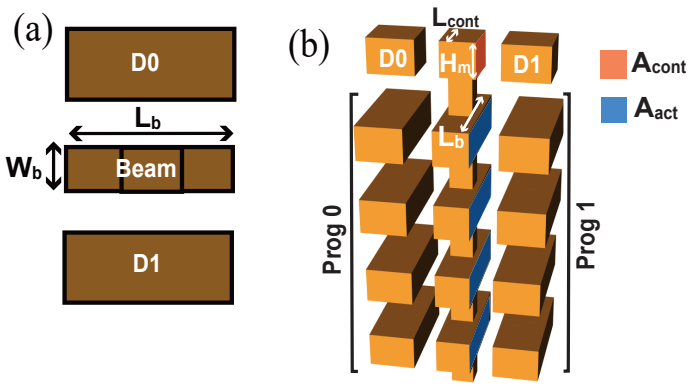

Figure 3.13: (a) Schematic plan view and (b) 3D model of a vertical NEM switch showing different dimensions.

to construct the beam. Hence k_{eff} can only assume discrete values and cannot be set to an arbitrary value using design parameters. For an optimized design, the contact adhesive force F_{adh} should be moderately higher than the spring restoring force at contact, $F_{\text{k, cont}}$. A_{cont} is defined by the overlap area between the beam and the D0/D1 electrodes at the top metal layer, as shown in Fig. 3.13, which is given by

$$A_{\text{cont}} = L_{\text{cont}} H_{\text{m}}, \tag{3.2}$$

where L_{cont} is the beam overlap length at the top metal layer and H_{m} is the thickness of the top metal layer. Hence F_{adh} can be adjusted by tuning L_{cont}. The program voltage can be minimized by increasing the actuation area A_{act} and minimizing the actuation gap. A_{act}, which is shown in Fig. 3.13 (b), is a function of the overlap length between the beam and program electrodes, thickness of the metal layers and the number of metal layers used for actuation. A_{act} can be maximized by increasing the overlap length, L_{b}. It should be noted that increasing L_{b} increases the footprint of the NEM switch and the risk of catastrophic pull-in.

3.5 Summary

The release-etch process is optimized to successfully release the first multi-layer BEOL NEM switches with minimal non-volatile etch residue. The etch chemistry is optimized to achieve the necessary undercut required to release both lateral and vertical NV-NEM switches. A wet cleaning process is necessary to remove re-sputtered/ non-volatile etch compounds that cause micromasking to occur during the etch process; however, it has to be used during the first stage of the release-etch process to prevent capillary force-induced stiction failure.

Design of BEOL NEM switches is investigated via MEMS+ 3D device simulations, in order to guarantee non-volatile and reprogrammable operation without catastrophic pull-in and to optimize program/readout energy and delay. A design minimizing program voltage/energy, which requires low spring stiffness k_{eff} and low contact area A_{cont}, is susceptible to catastrophic failure and high contact resistance. A stiffer structure is required to solve this problem, which results in a reliable design at the cost of increased program voltage. In conjunction with a stiffer structure, a larger contact area can be used to achieve a lower contact resistance. For a certain contact area and corresponding contact adhesive force, the stiffness can be tuned to a moderately high value to achieve the largest range of viable programming voltages.

3.6 References

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Chapter 4

CMOS-NEM Hybrid Circuits

4.1 Introduction

NV-NEM switches show promise for ultra-low-power digital integrated circuit applications because of their very low OFF-state leakage current and abrupt switching behavior. By using the BEOL layers of a conventional CMOS manufacturing process, NV-NEM switches can be monolithically integrated with CMOS circuitry to provide for enhanced chip functionality at relatively low incremental cost. Also, the relatively low ON-state resistance of NV-NEM switches facilitates fast readout of the programmed state. In-memory computing (IMC) architecture incorporating arrays of NV-NEM switches has been proposed for high-speed real-time computation on large data sets. For example, NV-NEM-based parallel computing scheme has been proposed for fast and energy-efficient data-string searching [1]. As another example, a fast and energy-efficient look-up table (LUT) implemented with arrays of BEOL NV-NEM switches has been proposed. [2].

BEOL NV-NEM switches also can be leveraged to implement reconfigurable circuits, such as a field-programmable gate array (FPGA). Since most of the static and dynamic power consumption happens in the interconnect fabric of an FPGA [3], integration of NV-NEM routing interconnects above the CMOS logic blocks can be advantageous for decreasing the

dynamic power consumption and chip area [4].

In Section 4.2 of this chapter, a hybrid circuit comprising a monolithically integrated BEOL NV-NEM switch and a CMOS inverter is experimentally demonstrated as a proof-of-concept. Section 4.3 presents an array of BEOL NV-NEM switches programmed to store different data strings and demonstrates a data-string searching operation on the array. Section 4.4 describes the operation a 2-input/1-output hybrid CMOS-NEM LUT incorporating an array of NV-NEM switches, programmed to emulate digital logic functionality. In this chapter, all of the NEM switches are fabricated using multiple BEOL metallic layers, while the CMOS parts are implemented in FEOL layers using a standard 65 nm-generation manufacturing process. Section 4.5 summarizes this chapter and discusses ideas for circuit performance improvement.

4.2 Reconfigurable Circuits

A non-volatile SPDT NEM switch can function as a 2-to-1 multiplexer, routing a voltage signal applied to the beam to either data electrode D0 or D1. Fig. 4.1 shows the schematic of a proof-of-concept hybrid CMOS-NEM circuit, comprising a BEOL NEM switch and a FEOL CMOS inverter. The NEM switch first needs to be programmed in order to route the input signal V_{IN}. This is accomplished by grounding the beam and applying a program voltage V_{Prog} pulse to either Prog0 or Prog1 electrode to actuate the movable beam into contact with D0 or D1, respectively. The state of the switch can be determined by measuring V_{OUT}. In this circuit, D0 is connected to V_{OUT} directly, whereas D1 is connected to V_{OUT} through a CMOS inverter. Hence V_{OUT} is either identical to V_{IN} or its complement, depending on the state of the NEM switch.

The NEM switch used in this circuit is a lateral switch fabricated in a 65 nm process technology, using the bottom five BEOL metal layers and intermediary via layers. The device structure is the same as for the switch demonstrated in Fig. 3.5. It is designed to have a relatively low contact resistance of a few hundreds of ohms. V_{IN} is set to be a 100 kHz

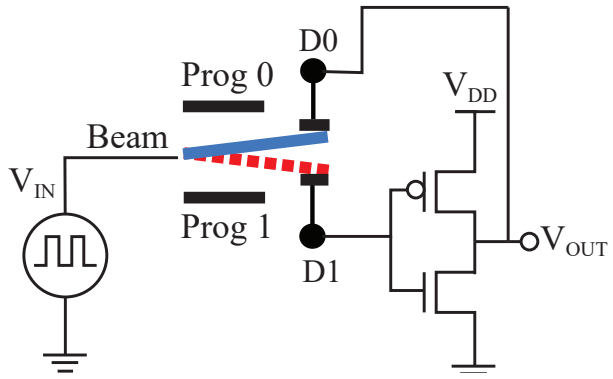


Figure 4.1: Schematic diagram of a hybrid CMOS-NEM circuit consisting of a lateral NV-NEM switch and a CMOS inverter.

square wave voltage signal swinging between 0 V and V_{DD}. V_{DD} is chosen to be 1.2 V, which is compatible with 65 nm CMOS core transistors. With the NEM switch programmed to the "0" state, V_{IN} is passed directly to V_{OUT}, as demonstrated by the waveforms in Fig. 4.2 (a). The signal propagation delay or the readout delay is measured to be < 100 ns. The probe pads used to measure the input and output signals add parasitic capacitances to the circuit, which is the main contributor to this RC delay. It is to be noted that programming or *write delay*, which is larger than *read delay*, is dominated by the mechanical delay rather than the RC delay. Also note that during a program operation, the D0/D1 electrodes can be electrically floating so that no direct current flows in the NEM switch; hence the energy consumed by the programming process is only due to the displacement current used to charge up the program electrode capacitance for electrostatic actuation. When the interconnect is programmed to the "1" state, V_{OUT} is the complementary signal of V_{IN}, as seen in Fig. 4.2 (b). This demonstrates the functionality of the CMOS inverter fabricated in the FEOL layers underneath the NEM switch. The inverted V_{OUT} has a large RC delay due to the relatively high on-state resistances and parasitic capacitances of the CMOS transistors, which was verified by characterizing the standalone CMOS inverter.

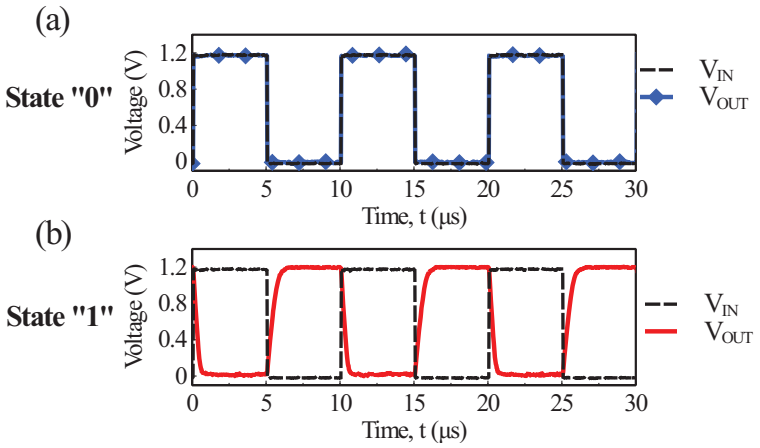


Figure 4.2: Input and output voltage waveforms showing signal transmission in (a) state "0" and (b) state "1".

4.3 Data Searching Operation with NV-NEM Array

An array of NV-NEM switches is demonstrated herein to be efficacious for memory-based parallel data searching. The number of columns is equal to the length of the data string, while the number of rows is equal to the number of stored data strings. Fig. 4.3 shows schematic circuit of a 4×2 array of NV-NEM switches that can be used to find a 2-bit data string stored within the array. The NV-NEM switches along the same column share contact electrodes D0 and D1. Prog0 and Prog1 electrodes are also shared along a single column, but are not shown in Fig. 4.3 for simplicity. Programming of each of the switches in a single row is accomplished by grounding the corresponding bit line O'$_x$ ($x = 0, 1, 2, 3$) and then applying a programming voltage V_{Prog} to the appropriate program electrode. A half-select cross-point array addressing scheme also can be used to program the NV-NEM switches [5]. The four rows (bit lines: O'$_0$, O'$_1$, O'$_2$ and O'$_3$) in Fig. 4.3 are programmed to store the data strings "00", "10", "01" and "10", respectively. A and B are the most-significant and least-significant bits, respectively. In order to find the row(s) that stores data matching an input string, a read operation is performed on the array, across all of the programmed columns in parallel, as follows. First the data string being sought is applied to the columns

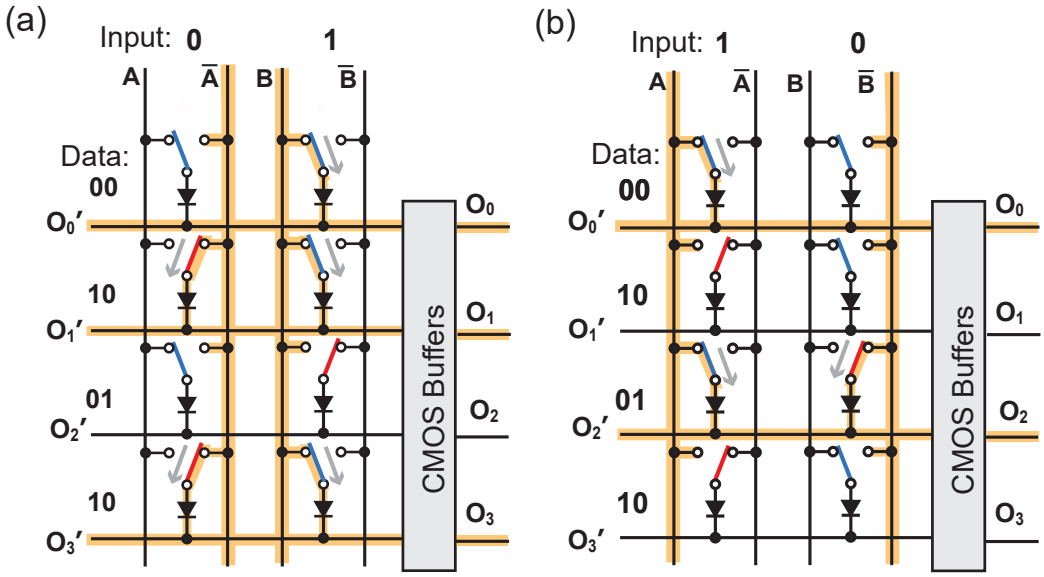


Figure 4.3: (a) Circuit diagram of a lateral NV-NEM switch array for memory-based parallel data searching. Data string matching operations are shown for input string "01" and (b) input string "10". The highlighted lines show the wires that are driven to high voltage.

of the array: For an input bit "0" in the string, the corresponding D0 line in the columns stays low (*i.e.* 0 V is applied), while the corresponding D1 line is driven high (*i.e.* V_{DD} is applied); conversely, for an input bit "1", the D0 line is driven high, while the D1 line stays low. With the input voltages applied, all O'_x lines except the one(s) matching the input data string are charged high (these lines are highlighted in the figure). Fig. 4.3 (a) and (b) show data searching operation for two different input strings "01" and "10", respectively. In Fig. 4.3 (a) input string "01" sets input lines A low and B high; the complementary inputs $\bar{\mathrm{A}}$ and $\bar{\mathrm{B}}$ are set high and low, respectively. The output signals O_x are read through CMOS buffer gates. Hence all the O_x lines, except the one programmed to match the input string "01", are driven high. Note that a PN-junction diode is integrated with each NEM switch beam to prevent sneak leakage current paths in the array and accidental discharge of the lines that are driven high.

In the example in Fig. 4.3 (a), the data on O_2 corresponds to data string "01", leading to

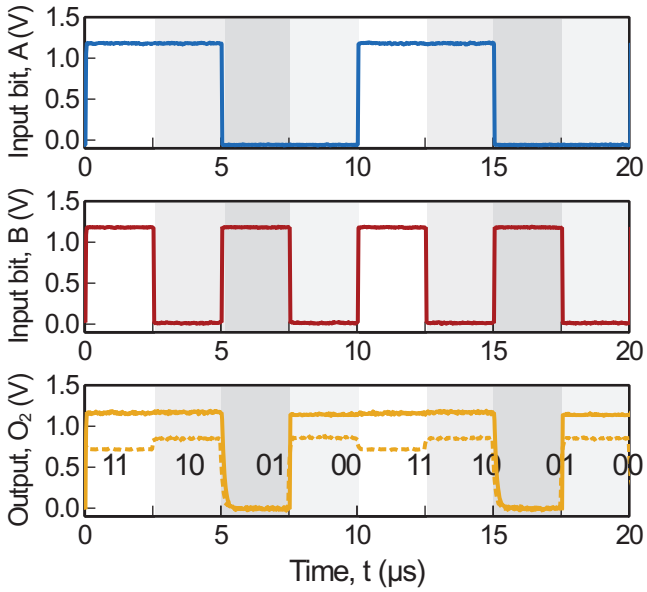


Figure 4.4: Measured input and output voltage waveforms demonstrating data search operation for input string "01". Voltage waveform of output line O_2 goes low when the input data string is "01", indicating storage of "01" on the corresponding row. (The dashed line represents the voltage on line O_2' before it is passed through a CMOS buffer to line O_2.)

O_2 staying low, while $O_{0,1,3}$ are all driven high. Similarly in Fig. 4.3 (b), the data strings on both O_1 and O_3 match input data string "10", leading to only those two output lines staying low. Sense amplifiers can be used to detect the state of each O_x line. It is notable that the demonstrated circuit requires a single read operation to match a data string, instead of two read operations, as proposed by Kato *et.* al. [1].

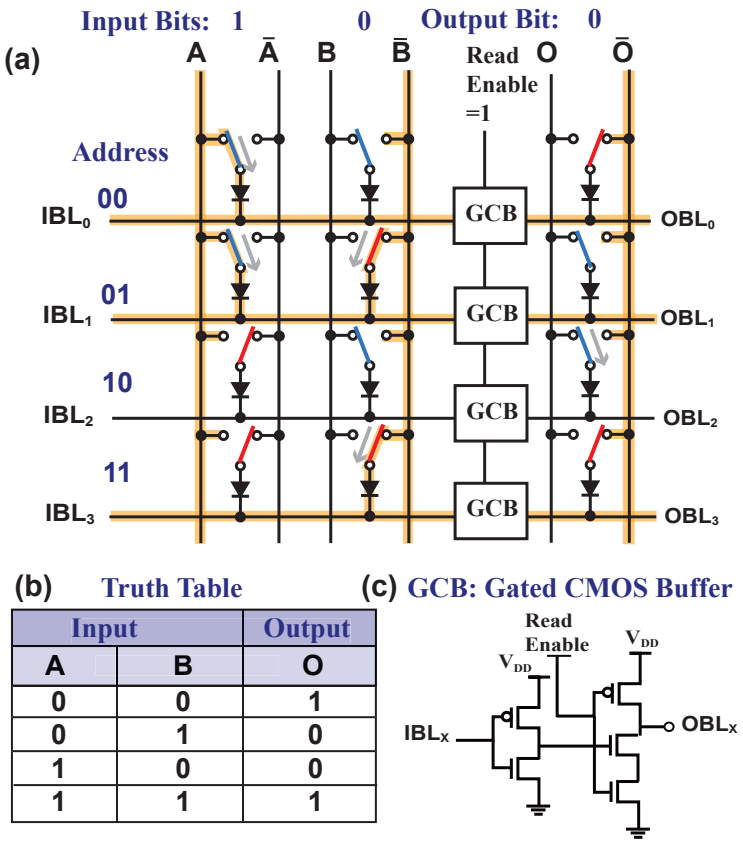
Fig. 4.4 shows the experimental results for a data search operation using a 4×2 array of lateral NV-NEM switches fabricated using 65 nm process technology, with the NV-NEM switches programmed as in Fig. 4.3 (a) to store data strings "00", "10", "01" and "10". The integrated PN-junction diodes are fabricated using n- and p-diffusion steps in the FEOL process. Voltage signals applied to A and B are chosen to be square waves swinging between 0 V and $V_{DD} = 1.2$ V with frequencies 100 kHz and 200 kHz, respectively, which generates all possible combinations of input bits. The measured voltage waveforms in Fig. 4.4 show the

O_2 and O_2' voltages for each possible combination of input bits A and B; they are low only when the input data string is matched ("01"). The dashed line and the solid line represent the voltages on lines O_2' and O_2, respectively. The propagation delay between the inputs A/B and output O_2 is found to be 100-200 ns, which is dominated by large parasitic capacitance associated with the probe pads.

4.4 Reconfigurable Look-Up Table

A hybrid CMOS-NEM circuit comprising an array of NV-NEM switches can be used to construct a reconfigurable LUT to implement any logic functionality. Fig. 4.5(a) illustrates the schematic diagram for a 2-bit input/1-bit output LUT implemented with an array of NV-NEM switches and gated CMOS buffers. Similar to the circuit for data searching, the NV-NEM switches on a single column have shared contact electrodes D0/D1 and program electrodes Prog0/Prog1. The number of columns in the array is equal to $N + M$, where N is the number of input bits, *i.e.* length of the address word, and M is the number of output bits. The number of rows corresponds to the number of possible input bit combinations, *i.e.* 2^N. Each combination of input bits and its corresponding output is shown in the truth table in Fig. 4.5(b). In the program phase, each NV-NEM switch is programmed one row at a time by grounding the corresponding input bit line IBL_x ($x = 0, 1, ...2^N - 1$) or output bit line OBL_x ($x = 0, 1, ...2^N - 1$), and then applying a programming voltage V_{Prog} to the appropriate program electrodes (which are not shown in the circuit diagram for simplicity), so that programmed states reflect the truth table. A gated CMOS buffer (GCB) isolates each IBL_x from the corresponding OBL_x. The internal circuit diagram of each buffer is shown in Fig. 4.5(c) [2]. The read enable signal RE is used to control the gated CMOS buffers. When RE is driven high, the state of IBL_x propagates to OBL_x; otherwise OBL_x stays high at V_{DD}. The operation in the readout phase or the *look-up* phase takes place in three steps:

- With read enable signal grounded, all the output bit lines OBL_{0-3} are pulled to V_{DD}



Input		Output
A	B	O
0	0	1
0	1	0
1	0	0
1	1	1

Figure 4.5: Schematic of a 2-input/1-output look-up table (LUT), based on non-volatile vertical NEM switches. (a) Input bits "10" are used to address the array and an output bit "0" is read out. The highlighted lines maintain a voltage of V_{DD} during readout. (b) Truth table for the LUT, and (c) the gated CMOS buffer used to discharge the output bit line, O.

through the PMOSFETs in the GCBs. Both the output lines O and $\bar{O}$ are also pre-charged high.

- The input/address string is used to drive the columns of the input side of the array. For an input of AB = "10", the address line A is driven high to V_{DD}, while the address line B stays at 0V. Accordingly, $\bar{A}$ and $\bar{B}$ are pulled low are high respectively. As the input lines are driven, IBL_x corresponding to the selected address row stays low while the others are driven high, as indicated by the arrows on the input side in Fig. 4.5(a). For example, the input "10" pulls-up all the input bit lines except IBL_2, which

corresponds to the address word 10.

- The gated CMOS buffers are enabled by setting RE to V_{DD}, causing only one OBL_x, corresponding to the low IBL_x, to be pulled low. An output line is discharged through this OBL_x, as indicated by the arrow on the output side. The example shown in Fig. 4.5(a) shows OBL_2 being pulled low and the output line O discharging through it, resulting in a readout of output bit "0" for an input of "10".

Similarly as in the data search circuit, a PN-junction diode is introduced in series with each movable beam to prevent sneak leakage paths that can result in readout error due to undesired discharging of bit lines [2].

The circuit shown in Fig. 4.5(a) is fabricated using vertically oriented NV-NEM switches implemented using five metallic interconnect layers in a standard 65 nm-generation CMOS process and programmed according to the truth table in Fig. 4.5(b). The device structure is the same as the switch demonstrated in Fig. 3.6. PN-junction diodes and GCBs fabricated in FEOL layers are integrated monolithically with the NEM switches. Voltage signals applied to A and B are chosen to be square wave voltage signals swinging between 0 V and $V_{\mathrm{DD}} = 1.2\,\mathrm{V}$ with frequencies 25 kHz and 50 kHz respectively, which generates all possible combinations of input bits. Fig. 4.6 shows the measured voltage waveforms for each possible combination of input bits A and B. Each output bit line OBL_x goes low only when the input matches an address. As an example, OBL_2 is plotted in Fig. 4.6. For each combination, the corresponding output bit is reflected in output voltage O. The output O is passed through a buffer gate (not shown in the Fig. 4.5(a)) to lower the logic "low" to 0 V; hence the dashed and solid lines represent the output O before and after passing through the buffer respectively. The NV-NEM switch contributes a relatively small contact resistance to the readout signal path, so the intrinsic readout delay should be small. In this work the lookup operation delay is found to be $1 - 3\,\mu\mathrm{s}$, which is dominated by the large parasitic capacitances associated with the probe pads and the relatively high on-state resistances and

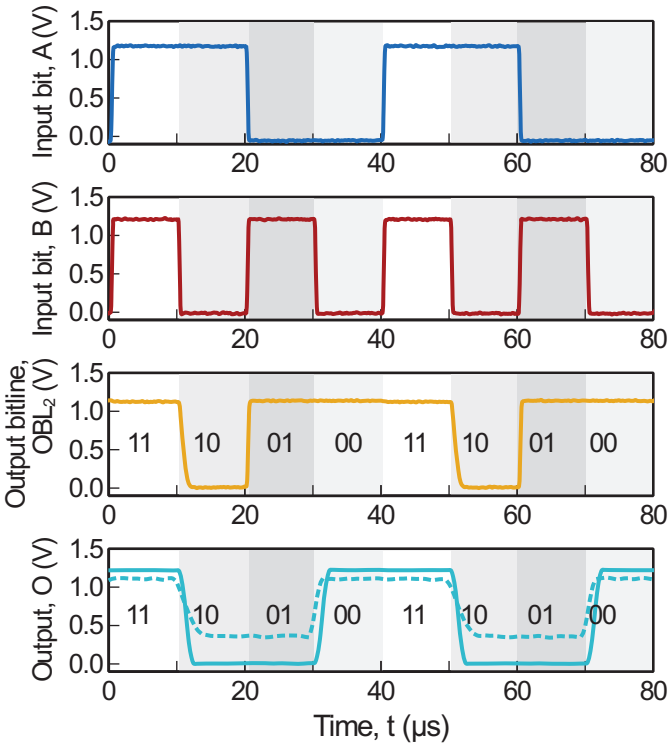


Figure 4.6: Measured voltage waveforms demonstrating the operation of the 2 input-1 output look-up table (LUT). The read enable signal RE is kept high. Voltage waveform of output bit line OBL_2 is shown. Output O reflects the truth table in Fig. 4.5(b).

parasitic capacitances of the GCBs and diodes. These delays were verified by characterizing standalone GCBs and diodes.

4.5 Summary

In this chapter, monolithically integrated hybrid CMOS-NEM circuits are experimentally demonstrated using 65 nm process technology. Functionality of an array of NV-NEM switches is successfully demonstrated in hybrid circuits for data searching and LUT operations. The NV-NEM arrays can be scaled up (to have more rows and columns) to process larger data strings.

It should be noted that the input/output voltages of the demonstrated circuits are compatible with core CMOS transistors at the 65 nm process technology node. However, the required V_{Prog} value is greater than the CMOS-compatibility limit. Technology scaling is beneficial for reducing V_{Prog} and the program delay, which will be discussed in the following chapter.

4.6 References

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Chapter 5

Scaling Trend and Performance Analysis

5.1 Introduction

As Chapter 4 experimentally demonstrates a pathway to energy-efficient and fast hybrid CMOS-NEM circuits, this chapter focuses on achieving compact, energy-efficient and reliable NEM switches at advanced CMOS technology nodes. Pawashe *et al.* projected ultra-scaled NEM devices to be more energy-efficient than conventional CMOS devices if either the contact adhesive force is very small or the actuation area is extremely large compared with its contacting area, leading to very low voltage operation [1]. The effect of scaling on the energy efficiency, speed and footprint of a non-volatile NEM switch is explored in the Section 5.2. BEOL NEM switches fabricated using 16 nm process technology are also demonstrated and the experimental results are compared to the NEM switches fabricated using 65 nm process technology. Although miniaturization is crucial for minimizing the operating voltage, switching energy and switching delay of a NEM switch, it not only poses design challenges, but also deteriorates the contact resistance and probability of stiction-induced failure [2]. These issues are discussed in Section 5.3. The cycling endurance of a NEM switch [3]

depends on the structural/contact material and the operating voltage. Section 5.4 presents a comparative study of various BEOL metallization options as prospective materials for NEM switches. BEOL NEM switches are benchmarked against other embedded non-volatile memory technologies in terms of read/write delay and energy in Section 5.5. Finally, Section 5.6 concludes this chapter with a short summary.

5.2 BEOL Switch Design at Advanced CMOS Technology Nodes

With each new generation/node of CMOS IC manufacturing technology, the minimum feature size and pitch are reduced, enabling smaller actuation gap and contact gap sizes for BEOL NEM switches. Fig. 5.1 shows the minimum metal pitch (MMP) and and 1x metal thickness for different CMOS technology nodes [4–10]. It can be seen from Fig. 5.1 that the metal pitch shrinks faster than the metal thickness with the advancement of technology nodes. The thickness of the metal layers contributes to the actuation area A_{act} and contact area A_{cont}, while the metal pitch dictates the minimum contact gap, g_{cont} and actuation gap, g_{act}. Hence, at advanced nodes, the contact/actuation gaps are scaled down by a larger factor than the scaling factor for actuation area/contact area.

5.2.1 Lateral NV-NEM Switches

Coventor MEMS+ is used to create a compact model of a lateral NV-NEM switch comprising five BEOL metal layers, similar to the NEM device described in Section 2.4. The physical dimensions of the lateral NV-NEM switch are obtained from the device fabricated using a 65 nm CMOS process, as shown in Table 5.1. The contact adhesive force per unit area is considered to be constant for different contact sizes, assuming uniform distribution of contact asperities. The value is chosen to be 1800 $\text{nN}/\mu\text{m}^2$, which is extracted by empirically fitting

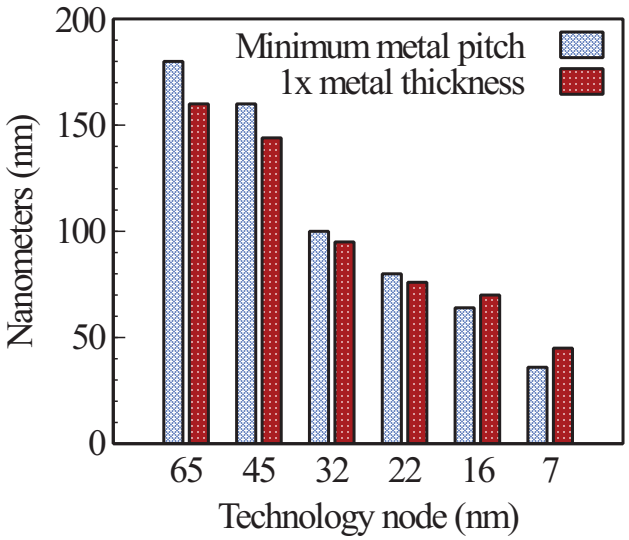

Figure 5.1: Scaling trend of BEOL minimum metal pitch (MMP) and thickness of the 1x metal layer (*i.e.* minimum pitch metal layer).

the simulated current-voltage characteristics to experimental data. This extracted value is similar to previously reported values for metallic contacts [11].

The beam width W_b and the contact area A_{cont} are varied to extract the minimum program voltage for each (W_b, A_{cont}) pair, as elaborated in the contour plot in Fig. 3.12. Hence the optimum (W_b, A_{cont}) pair is determined and the achievable minimum program voltage is calculated for the optimized NV-NEM design. The model is scaled down for advanced technology nodes using the scaling trend of MMP and 1x metal thickness shown in Fig. 5.1. Then the minimum program voltage is calculated for optimized designs at different technology nodes. Fig. 5.2 (a) shows the minimum program voltage for optimized devices using 5 metal layers. The programming voltage is observed to scale down rapidly with MMP and it is projected to be within the range compatible with input/output (I/O) CMOS devices for technology nodes 22 nm and beyond. Fig. 5.2 (b), (c) and (d) show the minimum program energy, mechanical program delay (assuming high vacuum environment) and cell area respectively, for the designs optimized for operation at minimum voltage, calculated via

Table 5.1: Design parameters used in the simulation for Fig. 5.2. Here F is the minimum metal half-pitch and H_m is the thickness of M2 metal layer.

Design Parameter	Specification
Metal layer used for contact	M2-M4
Metal layer used for actuation	M1-M5
Contact gap, g_{cont}	$1.1 \times F$
Actuation gap, g_{act}	$2.5 \times F$
Beam length,L_{b}	$65 \times F$
Minimum contact area, A_{cont}	$\sim 1.5F \times H_m$
Contact adhesion force per unit area, $F_{\text{adh}}/A_{\text{cont}}$	$1800\,\text{nN}/\mu\text{m}^2$

transient simulation.

The smaller program voltage and beam-to-program electrode capacitance contribute towards the decrease of program energy with scaling. The mechanical program delay also diminishes with scaling since the smaller contact gap requires smaller beam displacement and the reduced mass of the movable beam leads to a higher acceleration during electrostatic actuation. The accuracy of the program delay trend depends on the frequency response of the NEM switch. For the transient simulation, the viscous damping of the NEM switch is modeled using Rayleigh damping coefficients. The resonant frequencies of the NEM structure are calculated for each technology node using modal simulation. The mass-dependent Rayleigh damping coefficient β is scaled inversely proportional to the first eigenfrequency. The resonant frequencies increase as the NEM switch becomes smaller in dimension, which means that the Rayleigh damping becomes less pronounced. Consequently the movable beam experiences higher acceleration which contributes to the smaller mechanical delay. It is to be noted that the mechanical program delay of a ultra-scaled NEM switch can be as low as 10's of nanoseconds in high vacuum; so the electrical delay can be comparable to the mechanical delay for NEM switches fabricated using an advanced process technology. The capacitance between the beam and program electrode is $< 1\,\text{fF}$, which is smaller than typical logic gate capacitance. Hence the electrical program delay due to the gate electrode capacitance and other parasitic capacitances is expected to be small.

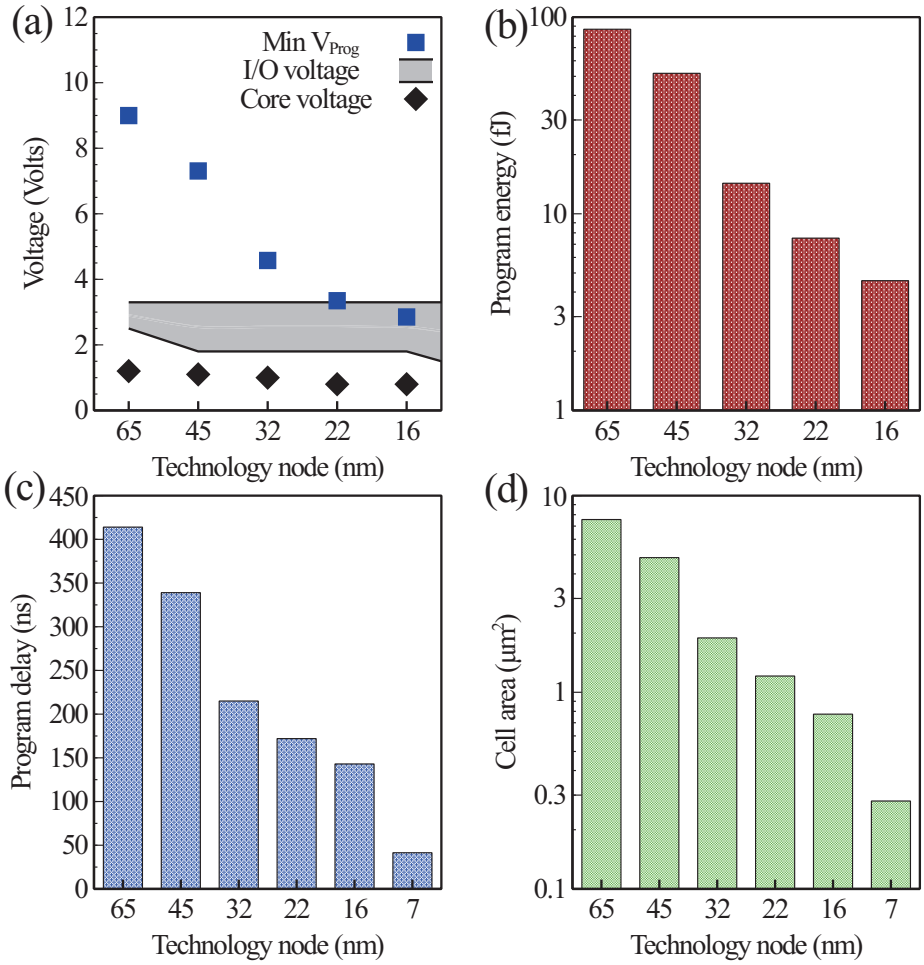

Figure 5.2: Simulated values (using Coventor MEMS+) of (a) minimum programming voltage of an optimized lateral NEM switch for different CMOS technology nodes, and corresponding (b) minimum program energy, (c) mechanical program delay in high vacuum and (d) footprint of a cell.

Current *vs.* voltage characteristics of NEM switches fabricated using 65 nm and 16 nm process technologies are obtained through quasi-static measurements, as demonstrated in Fig. 5.3 (a), showing non-volatile characteristics. In this case, the currents through D0/D1 terminals are artificially limited to 100 nA to avoid contact degradation due to Joule heating. The switch functionality was verified for ON-state DC current up to 10 μA. The NEM switch

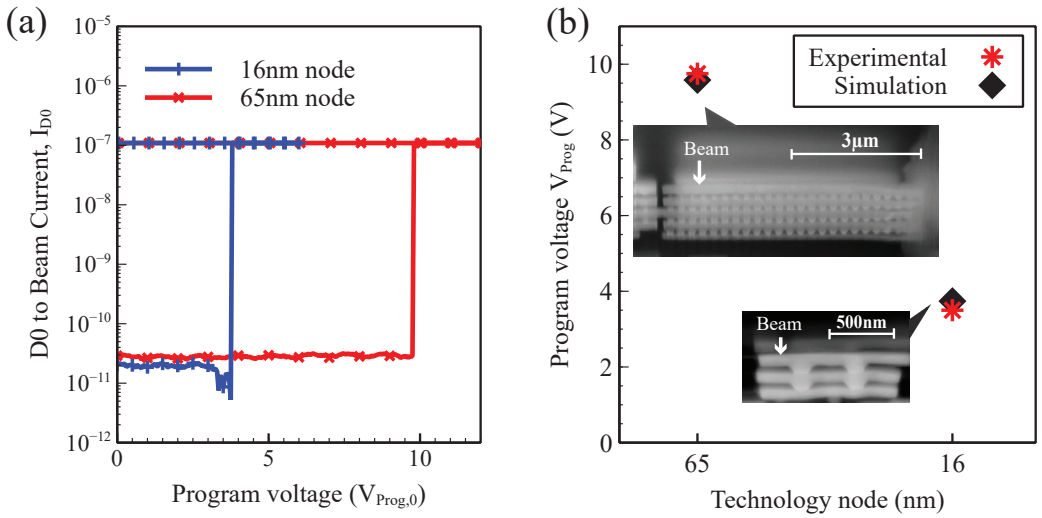

Figure 5.3: (a) Quasi-static current-voltage characteristics of laterally actuated NV-NEM switches programmed to state "0" from state "1", fabricated using 65 nm and 16 nm process technologies. (b) Experimentally extracted program voltages are compared to the simulated voltages for 65 nm and 16 nm NEM switches. Cross-sectional SEM images of the fabricated devices are shown in the insets.

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fabricated using 16 nm process technology can be operated with considerably lower program voltage than does the NEM switch fabricated using 65 nm process technology. The simulated program voltages are compared with experimentally measured values for both 65 nm and 16 nm process technologies. The 16 nm switch design utilizes three metal layers, which have a pitch equal to MMP $= 2 \times F$ (F= minimum metal half-pitch), to accommodate the design rules of the 16 nm process technology used in this work. The contact gap is designed to be minimum, which is equal to F.

5.2.2 Vertical NV-NEM Switches

In this subsection, the quasi-static and transient responses of a vertically oriented NV-NEM switch are simulated using Coventor MEMS+. The compact model parameters are obtained from a vertically oriented switch fabricated using 65 nm process technology, comprising five

Table 5.2: Design parameters used in the simulation for Fig. 5.4. Here F is the minimum metal half-pitch.

Design Parameter	Specification
Metal layer used for contact	M5
Metal layer used for actuation	M1-M4
Contact gap, g_{cont}	$1.1 \times F$
Actuation gap, g_{act}	$1.3 \times g_{\text{cont}}$ at M4
	$1.15 \times g_{\text{cont}}$ at M3
	$1 \times g_{\text{cont}}$ at M1-M2
Beam length,L_{b}	$3 \times F$, $5 \times F$, $7 \times F$
Beam width,W_{b}	$1.67 \times F$
Contact adhesion force, F_{adh}	$1800\,\text{nN}/\mu\text{m}^2$

BEOL metal layers, as described in Section 2.5. The design parameters of the NV-NEM switch are shown in Table 5.2. The contact area for vertically oriented switches are typically smaller than for laterally oriented switches; it is still assumed that the contact adhesive force scales with the contact area and that the force per unit area stays constant. This assumption holds until the scaled contact area has only one contact asperity[1].

For a given process technology, the stiffness k_{eff} of a vertical beam depends on its height *i.e.* the number of metal/via layers utilized for its construction and the dimensions of the vias. So the number of metal/via layers utilized for a design should be chosen based on the range of contact adhesion force F_{adh} available for typical values of contact area A_{cont}. As described in Section 3.4, the minimum programming voltage depends on the required electrostatic force for reprogramming, *i.e.* $(F_{\text{adh}} - k_{\text{eff}} g_{\text{cont}})$. The electrostatic force generated by the program voltage can be boosted by decreasing the actuation gaps (g_{act}) and increasing the actuation area (A_{act}), both of which unfortunately contribute towards catastrophic pull-in. Hence the actuation gaps, as shown in Table 5.2, are chosen to be larger for the upper metal layers to raise the catastrophic pull-in voltage V_{CPI} and lower the probability of stiction-induced failure. Increasing A_{act} is accomplished by increasing the device length L_b. However, larger L_b also can lead to catastrophic pull-in at smaller V_{CPI} due to torsional eigenmodes.

In this subsection, A_{cont} is varied to extract the minimum program voltage using the

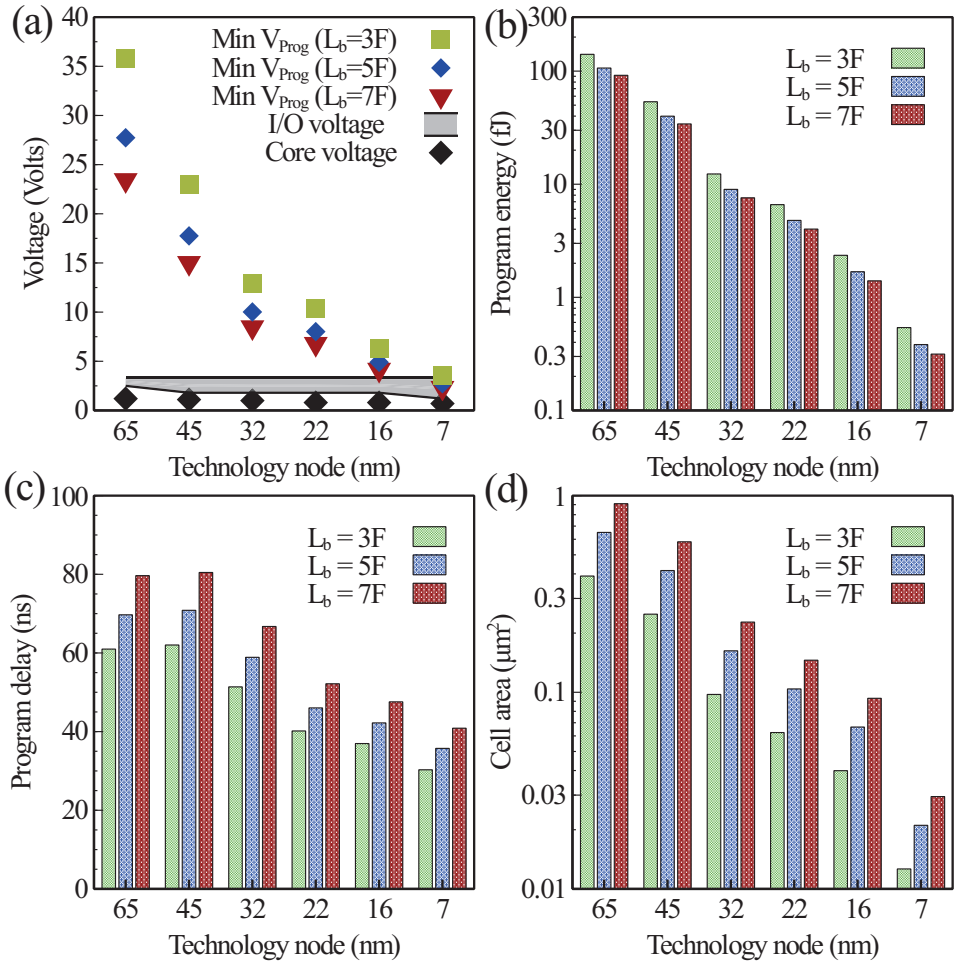

Figure 5.4: Simulated values (using Coventor MEMS+) of (a) minimum programming voltage of optimized vertical NEM switches with different lengths for various CMOS process technology nodes, and corresponding (b) minimum program energy, (c) mechanical program delay in high vacuum and (d) cell footprint.

compact model; hence the corresponding optimum A_{cont} is noted for different values of L_b. Then the model is scaled down for advanced process technology nodes using the scaling trend of MMP and 1x metal thickness shown in Fig. 5.1. Minimum program voltage is calculated for optimized designs at each node. Fig. 5.4 (a) shows the minimum program voltages for optimized vertical switches, which are evidently larger than the voltage required to program

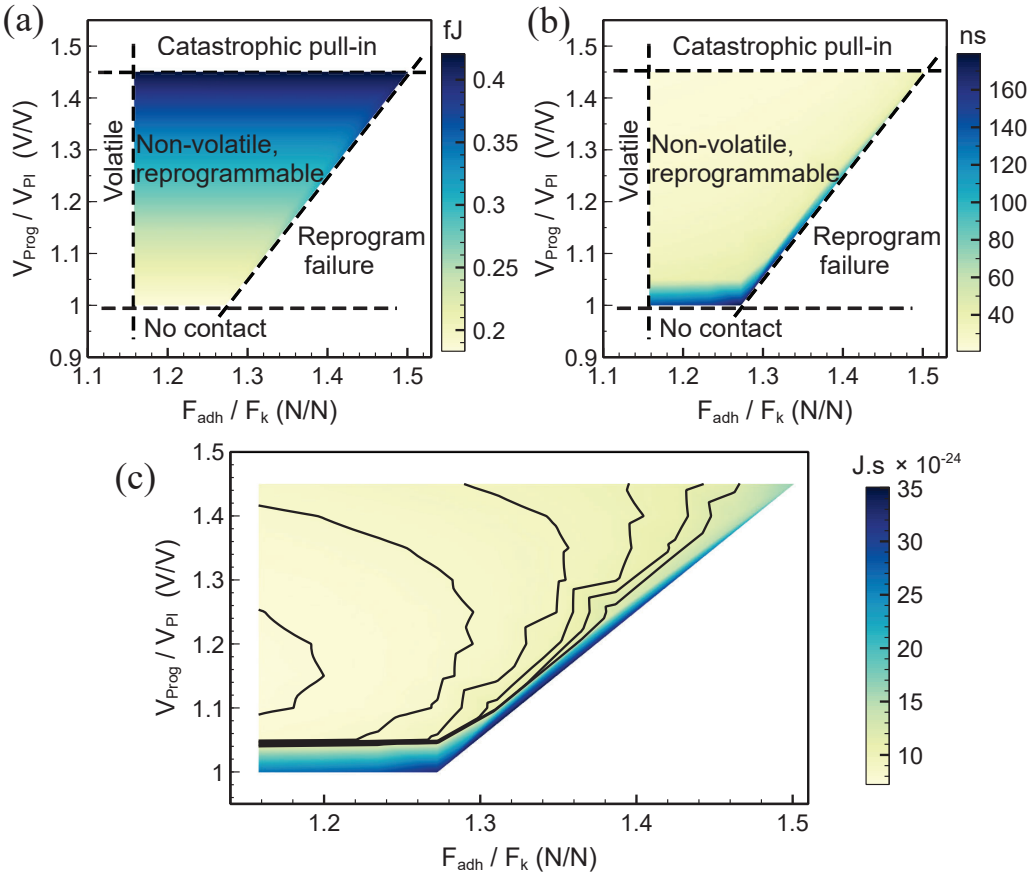

Figure 5.5: Contour plots of (a) program energy, (b) mechanical program delay assuming 7 nm process technology, showing various regions of operation delineated by the dashed lines. (c) Contour showing the minimum energy-delay product.

optimized lateral NEM switches. The vertical beam typically offers higher k_{eff} and lower A_{act}, compared to a lateral beam, leading to a higher program voltage. However, the smaller program electrode capacitance of the vertical design (< 0.1 fF) compensates for the higher V_{Prog} so that the program energy for both designs are similar, as observed by comparing Fig. 5.2 (b) and Fig 5.4 (b). Fig. 5.4 (c) and (d) show the mechanical program delay and cell area respectively, for the designs optimized for operation at minimum voltage, calculated via transient simulation. All the performance parameters, especially the program energy and

cell area, are observed to improve rapidly with MMP scaling. These projected performance parameters are competitive with other embedded NV memory technologies at the 7 nm node and beyond.

Fig. 5.4 shows the performance parameters of NEM switches optimized for minimum voltage operation, but typically the NEM devices are operated above the minimum voltage for faster operation. As the program voltage is increased, the beam experiences higher electrostatic force and higher acceleration, leading to smaller mechanical program delay. Switching energy and mechanical delay contour plots are generated using a compact model for a vertical NEM switch assuming 7 nm process technology. Different regions of operation are determined. The contact area (*i.e.* contact adhesive force F_{adh}) and program voltage V_{Prog} are varied and the corresponding program energy and delay are calculated through transient simulation. As seen from the contour plots in Fig. 5.5 (a) and (b), the program energy is minimized at lower V_{Prog} *i.e.* at $V_{\mathrm{Prog}}/V_{\mathrm{PI}} = 1$, however, the delay is minimized for higher V_{Prog} and lower F_{adh}, *i.e.* at $V_{\mathrm{Prog}}/V_{\mathrm{PI}} = 1.45$ and $F_{\mathrm{adh}}/F_{\mathrm{k}} = 1.16$. It can be observed that the widest design window for contact adhesion is achieved if the device is operated at a higher V_{Prog}. Fig. 5.5 (c) shows that the optimal design is obtained at $V_{\mathrm{Prog}}/V_{\mathrm{PI}} = 1.15$ and $F_{\mathrm{adh}}/F_{\mathrm{k}} = 1.16$, for a minimum energy-delay product ($7 \times 10^{-24} J.s$).

Fig. 5.6 (a) shows experimentally measured current *vs.* voltage characteristics of vertical NEM switches fabricated using 65 nm and 16 nm process technologies. The minimum V_{Prog} values are significantly higher than the program voltages of their lateral counterparts, as expected. The minimum program voltages for 65 nm and 16 nm devices are 25.5 V and 6 V respectively, which are close to simulated values, as can be seen from Fig. 5.6 (b). Cross-sectional SEM images of both of the vertical devices are shown in the insets. It should be noted that the actuation area is underestimated by the compact model used for simulation, as it ignores the electrostatic force exerted on the vias comprising the beam. The stiffness is also underestimated by the simulation, since it does not account for the tapered shape of the vias. However, these opposing phenomena do not show significant effects on the simulation results; hence the simulated program voltages do not deviate far from the experimental

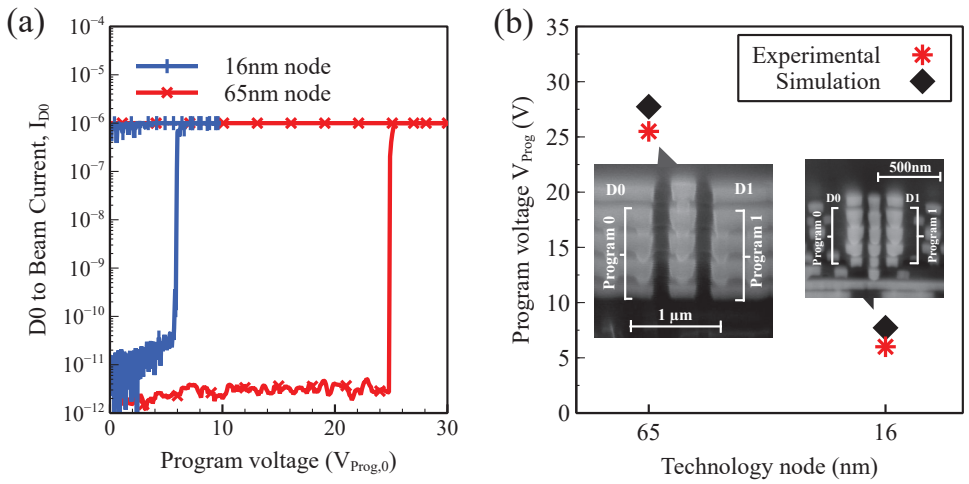

Figure 5.6: (a) Quasi-static current-voltage characteristics of vertical NV-NEM switches programmed to state "0" from state "1", fabricated using 65 nm and 16 nm process technologies. The currents through D0/D1 terminals are artificially limited to 1 µA to avoid contact degradation due to Joule heating. (b) Experimentally extracted program voltages are compared to the simulated voltages for NEM switches fabricated using 65 nm and 16 nm process technologies. Cross-sectional SEM images of the fabricated devices are shown in the insets.

values. It can be observed from the SEM image of the 16 nm device that it comprises seven metal layers and intermediary via layers. Since the effective stiffness of the beam is a function of its height, it can be modified by controlling the depth of release etch. The contact gap is designed to be minimum, which is equal to $\sim 2 \times F$, where F is the minimum metal half-pitch. The contact gap can be as small as $1 \times F$ if only the bottom three metal layers are utilized.

A hybrid CMOS-NEM reconfigurable circuit (similar to that shown in Fig. 4.1) is fabricated using 16 nm process technology, comprising the aforementioned vertical NEM switch design and a FinFET-based CMOS inverter. The NEM switch routes an input signal V_{IN} through the movable beam to D0 when the switch is programmed to state "0". D0 is connected to V_{OUT} directly in this state, which is plotted in Fig. 5.7 (a). D1 is routed to V_{OUT} through the inverter, hence V_{OUT} and V_{IN} are complementary signals when the switch

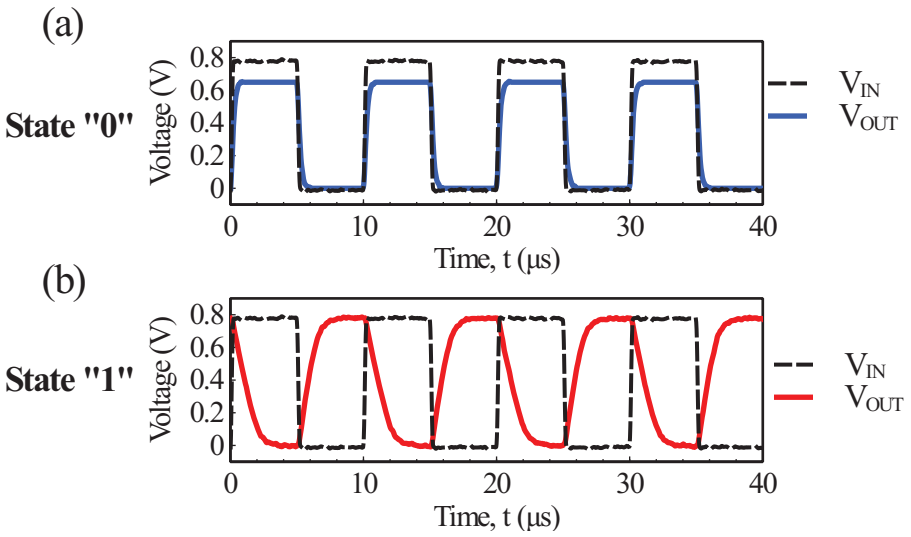

Figure 5.7: Measured input and output voltage waveforms showing signal transmission in (a) state "0" and (b) state "1" for a reconfigurable circuit employing a vertical NV-NEM switch in 16nm process technology.

is programmed to state "1" (Fig. 5.7 (b)). V_{IN} is a 100kHz square wave voltage signal swinging between 0V and $V_{\mathrm{DD}} = 0.8\,\mathrm{V}$. Here V_{DD} is chosen to be compatible with the core transistor operating voltage for the 16 nm node. It can be seen from Fig. 5.7 (a) that V_{OUT} does not the reach the peak input voltage of 0.8 V, which suggests a high contact resistance between the beam and D0. The signal propagation delay through the contact, *i.e.* the RC delay, is measured to be a few hundreds of nanoseconds. Parasitic capacitance associated with the probe pads dominate this RC delay, which is exacerbated by the parasitic capacitance associated with the long interconnects and electrostatic discharge (ESD) protection circuitry. The ON-state resistance is calculated using voltage measurements from a voltage divider circuit. The ON-state resistance is 167 kΩ-250 kΩ, which is substantially higher than the value predicted by the empirical contact resistance model (74 kΩ) from Fig. 3.12. This discrepancy originates from the disproportionate increase of interconnect resistance at scaled dimensions due to the reduced volume fraction of copper with respect to the high-resistivity diffusion-barrier and liner layers.

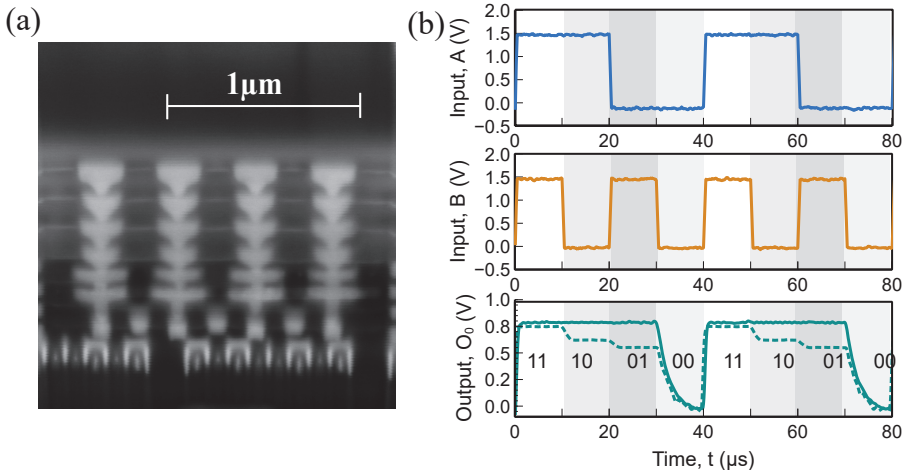

Figure 5.8: (a) Cross-sectional SEM image showing a column in a 4×2 array of vertical NEM switches fabricated using 16 nm process technology. (b) Measured input and output voltage waveforms demonstrating data search operation using the circuit in Fig. 4.3 at 16 nm node. Voltage waveform of output line O_0 goes low to show the presence of data string "00".

Fig. 5.8(a) is a cross-sectional SEM image showing four movable beams from a 4×2 array of vertical NV-NEM switches fabricated using 16nm process technology. Fig. 5.8(b) shows experimentally measured voltage waveforms demonstrating data search operation using the same array. The programmed state of the four rows corresponds to the circuit diagram in Fig. 4.3 (a). Similarly as in the previous chapter, the voltage signals applied to inputs A and B are chosen to be square waves swinging between 0 V and 1.5 V with frequencies 25 kHz and 50 kHz, respectively, which generates all possible combinations of input bits. The measured output voltage waveform O_0 is shown in Fig. 5.8(b) for each possible combination of input bits AB, demonstrating low voltage only when input data matches the programmed data "00". The dashed and solid lines represent the output before and after passing through buffer gates respectively. The propagation delay is found to be a few microseconds, which is worse than for the 65 nm node circuit due to larger ON-state resistance.

Table 5.3: Effects of scaling. γ, γ_1, γ_2 are scaling constants which are greater than 1.

NEM Switch Parameters	Uniform Scaling	Non-uniform Scaling (Lateral NEM Switch)	Non-uniform Scaling (Vertical NEM Switch)
Effective stiffness, k_{eff}	$1/\gamma$	$1/\gamma_2$	γ_2^3/γ_1^4
Actuation area, A_{act}	$1/\gamma^2$	$1/\gamma_1\gamma_2$	$1/\gamma_1\gamma_2$
Contact area, A_{cont}	$1/\gamma^2$	$1/\gamma_1\gamma_2$	$1/\gamma_1\gamma_2$
As-fabricated contact gap, g_{cont}	$1/\gamma$	$1/\gamma_1$	$1/\gamma_1$
As-fabricated actuation gap, g_{act}	$1/\gamma$	$1/\gamma_1$	$1/\gamma_1$
Beam mass	$1/\gamma^3$	$1/\gamma_1^2\gamma_2$	$1/\gamma_1^2\gamma_2$
Contact adhesion force, F_{adh}	$1/\gamma^2$	$1/\gamma_1\gamma_2$	$1/\gamma_1\gamma_2$
Spring restoring force at contact, $F_{\text{k, cont}} = k_{\text{eff}}g_{\text{cont}}$	$1/\gamma^2$	$1/\gamma_1\gamma_2$	γ_2^3/γ_1^5
Program electrode capacitance, C_{Prog}	$1/\gamma$	$1/\gamma_2$	$1/\gamma_2$
Minimum program voltage, $V_{\text{Prog, min}}$	$1/\gamma$	$1/\gamma_1$	$> 1/\gamma_1$
Minimum program energy	$1/\gamma^3$	$1/\gamma_1^2\gamma_2$	$> 1/\gamma_1^2\gamma_2$
Device footprint	$1/\gamma^2$	$1/\gamma_1^2$	$1/\gamma_1^2$

5.3 Scaling Challenges

Scaling is most advantageous for improving the device density, switching energy and switching delay of NEM switches. Constant-field scaling methodology, *i.e.* maintaining the electric field across the as-fabricated actuation gap at a constant value while all of the dimensions of the NEM switch are reduced by the factor $1/\gamma$, has been proposed to enhance performance [12]. Table 5.3 shows the effect of constant-field scaling by a factor of γ on different physical and performance parameters. The table also demonstrates the effect of non-uniform dimensional scaling on BEOL NEM switches, where the minimum pitch is scaled by $1/\gamma_1$ and the metal/via layer thickness is scaled by $1/\gamma_2$. Typically the metal pitch scales more aggressively than the thickness, *i.e.* $\gamma_1 > \gamma_2$ The electrostatic force generated by program voltage V_{Prog} is given by

$$F_{\text{elec}} = \frac{\epsilon_0 A_{\text{act}} V_{\text{Prog}}^2}{2g_{0/1}^2}, \tag{5.1}$$

where $g_{0/1}$ is the variable gap between the beam and Prog0/1. The minimum electrostatic force required to reprogram a NEM switch needs to balance the difference between contact adhesion force and spring restoring force, *i.e.*

$$F_{\text{adh}} - F_{\text{k, cont}} = \frac{\epsilon_0 A_{\text{act}} V_{\text{Prog,min}}^2}{2g_{0/1}^2}, \tag{5.2}$$

F_{adh} and $F_{\text{k, cont}}$ are scaled by the same factor ($= 1/\gamma_1\gamma_2$) for a lateral NEM switch; hence, the required minimum F_{elec} can be scaled by the same amount by reducing V_{Prog} by $1/\gamma_1$. However, for a vertical NEM switch, $F_{\text{k, cont}}$ scales down more aggressively than F_{adh}. So the F_{elec} required to balance the forces (*i.e.*, the program voltage) does not scale as well as for a lateral switch. For optimum performance of the vertical switches, F_{adh} needs to be scaled down by a factor larger than $\gamma_1\gamma_2$ in order to achieve operating voltage scaling at advanced technology nodes. Although scaling of the contact area is necessary for low-voltage operation, the effect on contact resistance is adverse, as discussed in the next subsection.

5.3.1 Contact Properties

Barrier layers for copper interconnects are required to prevent diffusion of copper into the surrounding low-κ dielectric insulating material. The barrier also must form a high-quality interface with copper to mitigate vacancy diffusion and electromigration. Line and via sidewall roughness, barrier roughness, and copper surface roughness all adversely affect electron scattering in copper lines and cause increases in resistivity. As the copper interconnect dimensions are shrinking due to technology scaling, the high-resistivity barrier and pre-deposition liner layers cannot be thinned as aggressively as the minimum metal pitch [13, 14]. Hence the volume fraction of copper inside the interconnect is reduced. Consequently, the line resistance increases disproportionately at advanced technology nodes. Lossy electron scattering at surfaces and grain boundaries also add to the increasing effective resistivity. Process challenges also contribute to the added resistivity, since etching, cleaning, and filling high aspect ratio structures using dual-damascene process are becoming increasingly difficult for

shrinking feature sizes. The metal surface roughness causes metal-metal contact to happen at only a few asperities [15]. The contact resistance of a single asperity R_c is given by [16]

$$R_c = \frac{4\rho\lambda}{3\pi a^2} + \frac{1 + 0.83(\lambda/a)}{1 + 1.33(\lambda/a)} \frac{\rho}{2a}, \tag{5.3}$$

where ρ is the electrical resistivity of the bulk metal, λ is the mean free path of an electron, and a is the radius of the contact spot. Contact resistance in a BEOL NEM switch is dependent on the number of contact asperities and the bulk resistivity [17]. Hence the factors increasing the bulk resistivity also contribute to the deterioration of contact resistance at advanced nodes.

The theoretical scaling limit of the operating voltage and switching energy of a NEM switch is dictated by the adhesive force at the contact interface. F_{adh} scales proportionately with the geometric contact area A_{cont} when the contact area contains many asperities. In this case, A_{real}/A_{cont} is constant, where A_{real} is the real contact area at the asperities. However, as A_{cont} is scaled down to contain only a single asperity, F_{adh} cannot be reduced by geometrical scaling anymore. In this scaling regime, A_{real}/A_{cont} starts to increase with decreasing feature size and F_{adh} remains constant [1]. However, the spring restoring force F_k keeps scaling for proportionately scaled NEM switches. In this scenario, the condition for reprogrammability, *i.e.* $F_{elec} + F_{k,\,cont} > F_{adh}$, cannot be satisfied if $V_{Prog,\,min}$ is scaled according to Table 5.3. Consequently, $V_{Prog,\,min}$ would not monotonically decrease for proportionately scaled NEM switches. Hence the actuation area A_{act} has to scale less aggressively at advanced nodes to compensate for the F_{adh} and continue the trend of $V_{Prog,\,min}$ scaling.

5.3.2 Process Design Challenges

As the MMP is scaled down for advanced process technology nodes, the minimum footprint of a BEOL NEM switch usually cannot be scaled proportionately. This is because the minimum area of a metal pattern, allowed by the design rules, does not scale as aggressively as the MMP. Fig. 5.9 shows the minimum achievable footprint of a vertical NEM switch cell designed in 65 nm and 16 nm technologies. While the minimum footprint allowed by the

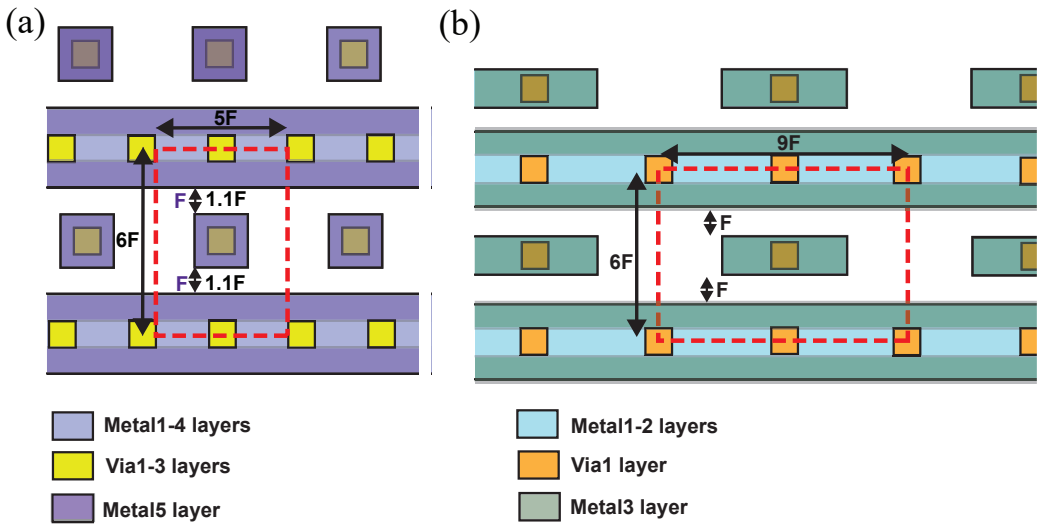

Figure 5.9: Layout view showing the minimum NV-NEM switch cell size for (a) 65 nm technology node and (b) 16 nm technology node.

design rules of a 65 nm process design kit (PDK) is $30F^2$, it is $54F^2$ for 16 nm node, where F is the minimum metal half-pitch. Consequently, the minimum achievable contact area also does not scale according to the scaling of the MMP. Hence the device density for BEOL vertical NEM switches with minimum footprint would increase even less aggressively than suggested by Table 5.3.

5.4 Reliability and Endurance

The cycling endurance of a NEM switch is usually limited by structural fatigue, contact micro-welding or deterioration of ON-resistance. Joule heating at the contacting asperities can lead to device failure due to micro-welding. The device endurance depends not only on the contact material, but also on the operating voltage, series resistance, capacitive load and other operating conditions [3]. Moreover, the electrical and mechanical properties of the structural and contact materials play a significant role in determining the lifetime of the device.

5.4.1 Structural Fatigue

As NEM switches are scaled down in dimensions, the properties of the structural material deviates increasingly from the bulk material properties. Mechanical properties of thin films depend on the microstructural characteristics, *i.e.*, grain size and orientation, and grain boundaries [18, 19]. Various metal thin films exhibit lower Young's modulus compared to their bulk counterparts. This phenomena, referred to as *modulus deficit*, might occur due to incomplete cohesion of grain boundaries, presence of voids or microcracks, and compliant grain boundaries [20]. Electroplated copper films have been reported to show significant modulus deficit [21]. Meanwhile Xiang *et al.* reported negligible modulus deficit for electroplated copper films, while showing increasing *yield stress* at room temperature, as the films become thinner [22]. Yield stress is the threshold value of stress at which the metal deformation becomes permanent (*i.e.*, plastic). Hence scaled BEOL NEM switches utilizing copper interconnects may suffer from increased compliance, however, the increased yield stress can offer protection from plastic deformation.

Creep of nano-crystalline copper at low temperatures has been reported in the literature [23], and may be caused by increased tendency of grain boundary sliding [24]. Therefore the change in pull-in voltage V_{PI} of a volatile BEOL NEM switch at room temperature was monitored over 200 switching cycles to investigate the creep behavior. V_{PI} is observed to decrease with increasing number of cycles, as shown in Fig. 5.10(a), suggesting a decrease in spring stiffness k_{eff}. The decreasing k_{eff} results in a slight increase in hysteresis voltage over time (Fig. 5.10(b)) The creep behavior is expected to be more pronounced for NV NEM switches, since they are subjected to longer period of stress in the programmed state.

A drop in spring stiffness, together with contact microwelding, eventually results in stiction-induced failure of a NEM switch. A stuck movable beam can be reprogrammed by vibrating it with a small voltage pulse train. Fig. 5.11 shows the reprogram operation of a vertical NV-NEM switch (fabricated using 65 nm process technology) after it had succumbed to stiction-induced failure after a few switching cycles. This was accomplished by applying

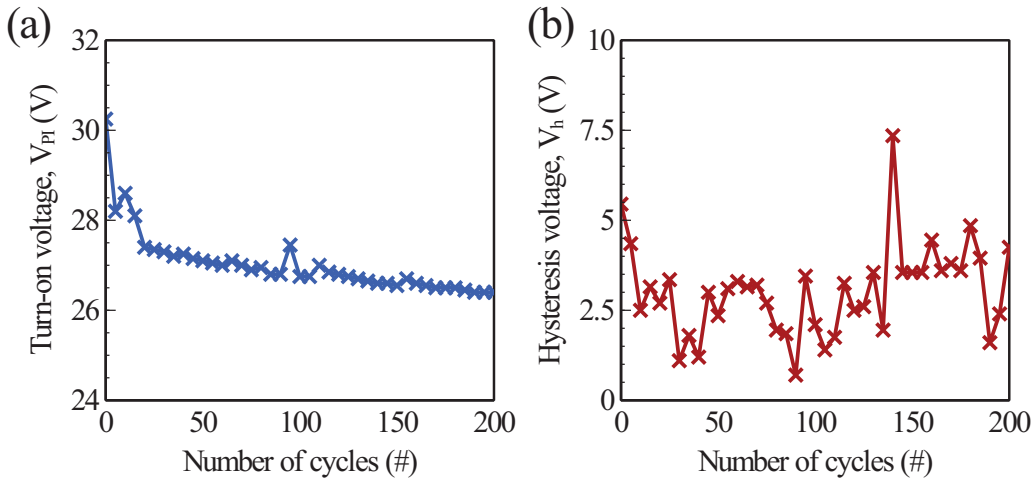

Figure 5.10: Measured (a) pull-in voltage V_{PI} and (b) hysteresis voltage V_{H} as a function of the number of ON/OFF switching cycles. The characteristics are obtained through quasi-static current-voltage measurements of a volatile lateral NEM switch fabricated using 65 nm process technology.

a 30 MHz, 1 V square wave to the beam, while applying V_{Prog} and 0 V to Prog0 and Prog1 electrodes, respectively. The oscillatory nature of the electrostatic force applied to the beam assists in reducing the intimacy of the mechanical contact, while the program voltage pulls the beam away from the contact. The vibration-aided reprogramming operation requires a smaller V_{Prog}, compared to a regular reprogramming operation. This approach is most effective if the frequency of the applied voltage signal matches the resonant frequency of the movable beam in the programmed state, since this would maximize the beam displacement for a given voltage magnitude.

5.4.2 Strain Effects

Large strain gradients within the movable beam structure of a NEM switch can result in significant deformation of the beam. The BEOL movable beam is built of multiple layers of interconnect metal and liner material. Due to the thermal expansion mismatch of different materials, the composite beam can deform without any external loading. This problem is

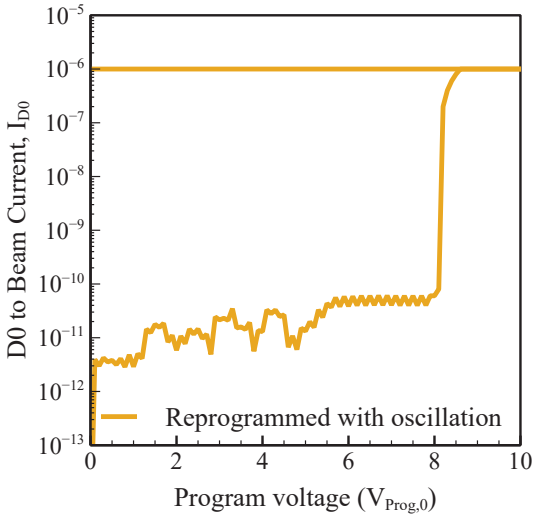

Figure 5.11: Quasi-static reprogramming of a vertical NV-NEM switch (65 nm node) using vibrations of the movable beam.

pronounced for the lateral NEM switch design. Eyoum *et al.* experimentally measured the deformation of a composite beam of SiN, Cu, TaN and Ta films, 100 µm long and 40 µm wide, and found the average deformation to be 2.1-4.7 µm [25]. In this work, a MEMS+ compact model of a lateral NEM switch implemented at the 65 nm node, as described in Table 5.1, is used to simulate the stress-induced deflection of the movable beam. The stress gradient is assumed to be 200 MPa/µm for all layers. The beam tip is found to bend up by 6.5 nm due to the bending strain. This upwards displacement of the beam tip reduces the overlap between the metal layers in the beam and the fixed actuation/ contact electrodes, effectively reducing the actuation area A_{act} and contact area A_{cont}. This would reduce the electrostatic force F_{elec} generated by V_{Prog} and the contact adhesion force F_{adh}. Therefore BEOL NEM switches should be designed to compensate for these effects of strain gradient.

5.4.3 Contact Degradation and Microwelding

Achieving good contact reliability and low contact resistance simultaneously is the major challenge for mechanical contacts. The NEM switch contacts are subjected to continuous

impact during switching cycles, which makes them vulnerable to mechanical degradation. Adhesive wear is the mechanism causing the mechanical wear in NEM switches [26, 27], which is defined by the adhesive transfer or removal of surface material during contact between two surfaces. The rate of adhesive transfer depends on the nature of the contact material. The amount of adhesive wear debris generated during contact is lower for harder contact materials [2]. Softer contact materials offer lower resistance; however, there are prone to plastic deformation and microwelding-induced failure. In contrast, harder contact materials provide higher endurance and better reliability, in spite of their high contact resistance. Table 5.4 lists the electrical and mechanical properties of materials that are compatible with standard CMOS BEOL processes.

It can be observed from the material hardness values in Table 5.4 that TiN and TaN are harder than Cu. Hence the presence of the TiN/TaN liner on the sidewall of the BEOL copper interconnect structure improves the contact endurance. Materials with low hardness values, *i.e.* Al and Cu can offer low electrical resistance as structural materials; however, their comparatively low Young's moduli and hardness values suggest a higher probability of

Table 5.4: Mechanical and electrical properties of metals and compounds compatible with BEOL metallization process [2, 28–32]

Material	**Bulk Young's Modulus** (GPa)	**Resistivity** ($\mu\Omega$**.cm**)	**Thin film hardness** (GPa)
Al	70	2.8	1.2
Cu	120	1.7	1.3
Ti	116	42	1.60 ± 0.20
TiN	210-320	50-550	17-24
Ta	185 ± 5	52 ± 4	10.4 ± 1.3
TaN	191-280	116-6000	15-27.8
Co	209	6.24	8.2
W	405	5.3	4.1
Ru	292	7.1	15.3
Rh	256	4.3	9.8

stiction failure. Ru is one of the hardest metals on the table with an extremely high Young's modulus; hence it is predicted to have the highest reliability and lifetime [2]. Refractory metals generally have a high value of hardness and they have demonstrated good endurance (10^{11} cycles) as the structural material for BEOL NV-NEM switches [33]. Ru, Rh and Co are considered to be candidates for replacing Cu at technology nodes beyond 7 nm [13]. Although these materials have higher bulk resistivity than pure Cu, they can provide for lower metal line resistance at ultra-scaled dimensions. This is because Cu interconnect technology requires highly resistive barrier/liner layers, which cannot not be scaled aggressively; hence barrier-less metal technologies, such as Ru, are projected to outperform Cu at nanometer-scale dimensions [13]. Ru also helps to alleviate the problem of contact degradation due to contact metal oxidation. This is because Ru forms an electrically conductive oxide, which could prevent a large increase in contact resistance after long duration of operation.

Moreover, the contacts in smaller NEM devices age more quickly than in larger devices. The *zero wear limit* of a contact, which is defined as the number of cycles required for the depth of wear deformity to reach half the original surface roughness, is an indicator of the lifetime of the NEM switch. Zero wear limit decreases with scaling; hence scaled devices are predicted to have a shorter lifetime [2]. Hence more robust BEOL materials like Ru and Rh are attractive for realizing more reliable NEM switches at advanced technology nodes.

The mean number of cycles to failure (MCTF) for a NEM switch depends on the voltage applied to the contacting electrodes during switching. MCTF increases exponentially with decreasing contact voltage [3]. MCTF and the cycling endurance of a NEM switch can be extended by *cold-switching*, that is, switching without applying a voltage between the beam and contact electrode. Cold-switching lifetime of a NEM switch is typically a few orders of magnitude better than the hot-switching lifetime [34]. Moreover, limiting the current flowing through the contact electrodes during a read operation helps to reduce Joule-heating-induced contact degradation and thereby increases the device lifetime.

5.5 Performance Benchmarking

Table 5.5: Performance benchmarking of vertical NEM switches against embedded non-volatile memory technologies

Technology	**Embedded bitcell size**	**Write energy/bit**	**Write delay/bit**	**Read energy/bit**	**Read delay/bit**
Vertical BEOL NEM switch	$0.055\,\mu m^2$ (16 nm)	$< 10\,fJ$	$< 50\,ns$	$< 1\,fJ$	$< 1\,ns$
STT-MRAM	$0.033\,\mu m^2$ (16 nm) [35]	$< 1\,pJ$ [36]	$0.5 - 11\,ns$ [37]	$< 1\,pJ$ [36]	$< 1\,ns$ [36]
OxRAM	$0.008\,\mu m^2$ (22 nm) [38]	$< 1\,pJ$ [36]	100 ps [36]	-	$< 1\,ns$ [36]
FeRAM	$0.1\,\mu m^2$ (180 nm) [39]	15 pJ [40]	$< 1\,ns$ [40]	15.5 pJ [40]	$< 1\,ns$ [40]

The performance of a vertical NV-NEM switch implemented with 16 nm process technology is benchmarked against different embedded NV memory technologies, specifically Spin Transfer Torque Magnetic Memory (STT-MRAM), Oxide-based Resistive Memory (OxRAM), and Ferroelectric Memory (FeRAM) in Table 5.5. The delays of the NEM switch are estimated by considering the line resistance and line capacitance to be $30\,\Omega/\mu m$ and $0.2\,fF/\mu m$, respectively [13]. It should be noted that the tabulated bitcell area corresponds to embedded memory, often integrated with the BEOL process. However, the tabulated read/write energy and delay values for each bit are collected from both embedded/standalone demonstrations, so the values might be overestimated for embedded memory. Although the cell area of the BEOL NEM switch is larger than other state-of-the-art embedded NV memory cells, both write and read operations achieve better energy efficiency. The read delay for each bit is also comparable to other technologies. This makes the BEOL NEM switch a good candidate for applications requiring embedded NV memory.

5.6 Summary

Scaling of physical dimensions is necessary to aggressively reduce the operating voltage and switching energy of a BEOL NEM switch. Vertical NEM switches, with a footprint of 0.055 µm^2 and an operating voltage of a few volts, are experimentally demonstrated for 16 nm process technology. Contact stiction appears to be the main failure mechanism for the NV-NEM switches. Structural fatigue is shown to affect the programming voltage over a number of switching cycles. The write/ read energy and read delay of 16 nm vertical NEM switches are found to be competitive with other embedded non-volatile memory technologies, *i.e.* STT-MRAM, OxRAM, FeRAM.

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Chapter 6

Conclusion

In addition to diversifying computational functionality of an IC, the hybrid CMOS-NEM platform has immense potential to improve the energy efficiency of electronic devices. These hybrid circuits can enable versatile sensing, computing, and communication systems for IoT applications. To fully leverage their potential, however, the NEM switches must have stable characteristics for many operating cycles to ensure reliable circuit operation. This chapter summarizes the contributions of this work and offers suggestions for future research directions.

6.1 Contributions of This Work

This thesis presents the design, fabrication, and circuit demonstration of NEM switches in BEOL interconnect layers of a standard CMOS process. The integration process of NEM switches on a CMOS platform is optimized within a low thermal budget and low incremental cost. A combination of plasma etch processes and wet cleaning is proposed after the standard CMOS fabrication, in order to release the movable parts of the NEM switches. Using this method, a vertically oriented BEOL NEM switch is demonstrated for the first time. This dissertation also includes the first-time demonstration of hybrid CMOS-NEM circuits with

a functional array of NEM switches. Effects of scaling of NEM switches are predicted using compact model based simulation. NEM switches fabricated with a 16 nm process are experimentally compared and contrasted against switches fabricated with a 65 nm process. The switches fabricated using 16 nm technology operate with smaller voltage; however, the hot-switching endurance of these NEM switches is lower, possibly due to Young's modulus deficit and ceased down-scaling of the contact adhesive force at scaled dimensions. ON-resistance degradation due to contact oxidation and stiction due to micro-welding were identified to be the primary issues which practically limit the switching endurance of NEM switches. For TaN/Cu contacting electrodes, the ON-state resistance increases with time due to contact oxidation, necessitating higher read voltages on the contact electrodes to break through the thin oxidized surface layer. The possibility of micro-welding increases with read current and the number of read cycles in a particular contacting state.

6.2 Suggestions for Future Work

Further work is suggested for improving the performance and lifetime of BEOL NEM switches, in order to expand the range of applications.

6.2.1 Structural Material

At ultra-scaled dimensions, harder metals with larger values of Young's modulus are preferred as structural/contact materials. These materials offer low contact adhesive force to balance the reduced stiffness due to Young's modulus deficit of the scaled structural materials. The NEM switch design for the 16 nm process demonstrated in this thesis can be optimized further to compensate for the reduced stiffness and the high contact adhesive force. Ruthenium, which is a potential candidate to replace copper interconnect technology at advanced nodes, is a particularly attractive option for structural/contact material. It forms a conductive oxide and has a very high Young's modulus; hence it is suitable as both the structural and

the contact material. Other hard BEOL-compatible metals are also good candidates for investigation.

6.2.2 Contact Reliability

In this work, the performance of the NEM switches are only explored through hot-switching, which severely degrades their switching endurance. Cold-switching endurance of BEOL NEM switches should be investigated in future work. One way to reduce probability of stiction-induced failure is to coat the contacting surface with lower-adhesive-force material. Self-assembled molecular coating can reduce the contact adhesive force in M/NEM switches [1, 2]. It would be worthwhile to use molecular coatings on BEOL NEM switches in order to prolong their lifetime. Ruthenium should also be explored as a contact material, which might offer better immunity to degradation due to oxidation.

6.2.3 Scaling

Implementation of NEM switches at process technology nodes beyond 16 nm can reduce the operating voltage and switching energy even further. Optimization of devices is required to account for the change of material properties at the nanoscale. Additional challenges for advanced nodes will include optimization of the release-etch process for compatibility with novel materials used in the BEOL stack. Avoiding interconnect routing congestion and design rule violations is also crucial for designing a circuit with a large array of NEM switches at advanced process technology nodes.

6.2.4 Applications

Various applications of hybrid CMOS-NEM circuits have been proposed in the literature, including power gating [3], non-volatile SRAM cells [4], analog-to-digital converter (ADC), digital-to-analog converter (DAC) [5], and sequential logic circuits [6]. Experimental demon-

stration of these hybrid circuits on a standard CMOS platform would be worthwhile to explore the suitability of BEOL NEM switches for IoT application.

6.3 References

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