Circuits and Control for High-Performance Grid-tied Ac-Dc Conversion Systems

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Circuits and Control for High-Performance Grid-tied Ac-Dc Conversion Systems

by

Zitao Liao

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University of California, Berkeley

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Abstract

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Ac-dc (and dc-ac) power converters are the interfaces between the electrical grid and the systems for emerging applications such as electric vehicle (EV) charging, renewable energy source integration, data center power delivery, consumer electronics and numerous other applications. In this dissertation, new circuit topologies and control techniques to improve the performance for both single-phase and three-phase grid-tied converters are explored for three major conversion scenarios: high power bidirectional single-phase ac-dc converters for EV charging and data center applications, low power single-phase ac-dc converters for consumer electronics, and high power three-phase ac-dc converters. For single-phase conversion, the challenge of twice-line frequency energy buffering is addressed with active buffering techniques that can significantly reduce the required capacitor size compared to conventional solutions. Through the development of active buffers with systematic multi-objective optimization methods and associated advanced digital control, the energy utilization ratios of the passive components are much improved, and the system losses are optimized. For three-phase conversion, control and modulation techniques to reduce computational complexity and inductor current ripple are proposed and validated. The proposed circuit topologies and control techniques for both single-phase and three-phase are all validated with high performance hardware demonstrations. Some of the highlighted ones in this dissertation are: a 6 kW, 400 V_{dc} single-phase liquid-cooled EV charger with optimized series-stacked buffer, achieving record power density; a 6 kW 400 V_{dc} three-phase multilevel rectifier with advanced digital control techniques; an active single-phase buffer with the smallest reported capacitor size for 2 kW, 400 V_{dc} inverters; a compact active buffer for 65 W USB-C charger.

"Learning without thinking is labor lost, thinking without learning is perilous"

- Confucius

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Acknowledgments

This dissertation not only concludes my six-year graduate school journey, but also marks the tenth year since I came to the United States for studying. Ten years ago, I only knew that it would be cool to work on electric vehicle related fields in the future. Never could I have imagined that I would have the opportunities to work alongside and learn from some of the best minds in the field of power electronics and EVs, and work on projects that have truly pushed the boundary of existing technologies in fundamental ways.

I would like to direct my first thank you to my advisor Professor Robert Pilawa-Podgurski. Robert is a visionary researcher, a resourceful and supporting mentor, and a caring friend. I am extremely grateful to Robert for always inspiring me to solve challenging and meaningful problems, providing me the freedom and support to explore, and encouraging and comforting me after many failures in the lab. Moreover, his enthusiasm, humor and care always give me a sense of belonging to a large family in the research group, filling the everyday life of graduate school with laughter and joy. I would also like to thank my committee members, Professor Seth Sanders, Professor Duncan Callaway and Professor Minjie Chen for valuable suggestions throughout the course of this work.

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Chapter 1

Introduction

1.1 Grid-tied Ac-dc and Dc-ac Conversion

Power electronics based ac-dc and dc-ac power conversion systems are critical links in the power delivery chains of today's electrical grid: With the recent increasing market penetration of electric vehicles, high-efficiency ac-dc converters become vital to deliver power from the ac grid to the high voltage dc battery in the vehicle; As human beings are generating more data than ever before, the energy consumption from the data centers, in which the servers are dc-powered, are becoming more and more significant; Delivering power to today's massive amount of consumer electronics products with more computing power and larger batteries also requires more efficient ac-dc converters; To integrate more renewable sources to cope with the increasing energy demand, photovoltaic (PV) systems and battery energy storage systems are often coupled together to provide a stable energy generation, which also requires bidirectional ac-dc power flow between the ac grid and the dc PV panels and batteries.

In the aforementioned applications and among many others, the ac grid voltage can be single-phase, three-phase or multi-phase with different regional voltage levels and frequencies, and the dc voltage can range from a few kilo-volts for solar inverters, to a few hundreds volts for EV battery charging, and a few volts for consumer electronics. While power electronics systems for these different specifications vary in the actual hardware designs, there are many desirable features and fundamental challenges in common. In all these systems, there are energy-storage components that are processing line-frequency power flows, and there are power converters that are operated at much higher frequencies, which contain both active switching devices and passive energy storage components. How to best utilize the energy in these components with the right circuit topology and architecture, and control the power converters accordingly become key to improve the power density and efficiency of the overall systems, which are desirable to reduce wasted energy and be more compliant with space and weight constraints.

Conventional solutions such as two-level based power converters and passive filtering

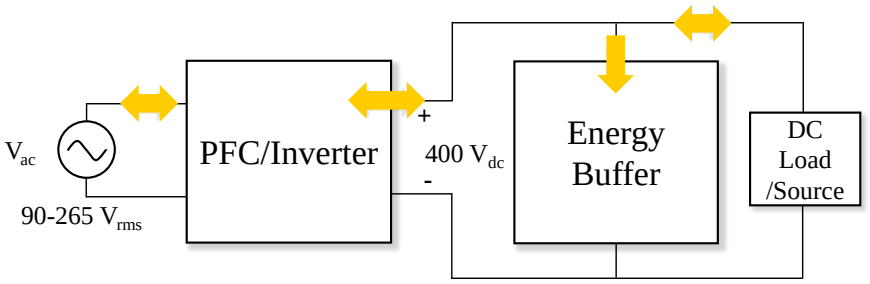

Figure 1.1: Typical single-phase conversion system block diagram for EV charging, data center power delivery and solar inverter applications.

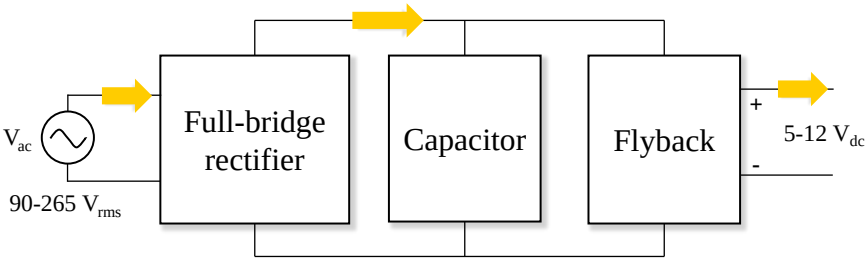

Figure 1.2: Typical single-phase conversion system block diagram for low power USB-C adapter applications

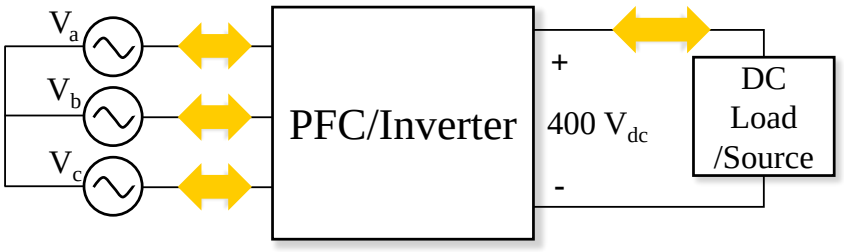

Figure 1.3: Typical three-phase conversion system block diagram for EV charging, data center and solar inverter applications

solutions at the line frequency have many limitations that prevent them from achieving higher power density and efficiency. As such, a more fundamental design philosophy that considers the energy utilization and the energy density of both low and high-frequency components, and the associate power electronics circuits and controls is needed to overcome the limitations of conventional designs.

1.2 Research Scope and Goals

In this dissertation, techniques to improve the power density and efficiency of both single-phase (ac-dc or dc-ac) and three-phase converters are explored.

For single-phase conversion, one of the most common conversion scenarios is between the universal single-phase ac (90-265 V_{rms}) and a dc load or source with voltage around 400 V_{dc} (depending on the direction of the power flow), as depicted in Fig. 1.1. It can be used for emerging applications such as on-board EV charging, data center power delivery, and solar inverters. In such conversion scenarios, since the ac side has to deliver power at kilowatt level, the power factor is usually controlled to be close to unity with a Power Factor Correction (PFC) converter or current-controlled inverter. As such, there will be instantaneous power mismatch between the dc-side and ac-side, and an energy buffering device is needed to compensate for such mismatch. In conventional solutions, this energy buffering device is usually implemented with a large capacitor bank across the dc-bus, which dominates the volume of the overall system. In this thesis, we investigate the design and control of active buffer solutions that can significantly reduce the size of the energy buffer in level-II EV charging and data center power delivery applications. Moreover, by applying similar buffer topologies to other applications such as USB-C flyback adapter chargers in Fig. 1.2 for consumer electronics, the line-frequency energy storage capacitor size can also be much reduced.

Three-phase conversion is usually intended to deliver higher power than single-phase conversion in similar applications such as EV charging, data centers and so on as shown in Fig. 1.3. One of the major benefits of three-phase ac power is that the ac power of the three phases can be summed up to be a dc value, given that the power from the three phases are balanced. As a result, no energy buffering device is needed as in single-phase conversion. In many high-switching-frequency three-phase converters, the immediate effort to reduce the size of the overall system is not the filter capacitors on the dc-bus, but rather the power converters themselves. Multilevel converters have been demonstrated to improve the power density and efficiency in dc-dc and single-phase applications, yet there are challenges to utilize them for three-phase conversions. One of the major challenge of using multilevel converters in three-phase configuration is the modulation strategy to control all the switches in the converters to achieve minimum inductor current ripple. Simply scaling up the modulation technique for conventional two-level three-phase converters will quickly become very complicated to implement in real digital controllers as the number of levels increases. In this thesis, we explore modulation techniques and associate digital control architectures that can significant reduce the computational complexity for three-phase multilevel inverter/PFCs, while achieving minimum inductor current ripple.

1.3 Organization of Thesis

Chapter 2 begins the single-phase energy buffer topic with background review of basic power and energy relations within the single-phase conversion and classic passive and active buffer solutions. Chapter 3 to 7 discuss the first main active buffer topology – Series-Stacked Buffer (SSB) in this thesis. Chapter 3 introduces the operating principles and component sizing constraints of the SSB. The more accurate operating constraint is one of the key findings in this thesis that the SSB can be designed with much higher capacitor energy utilization than prior works. In Chapter 4, the basic voltage and current relations in the SSB are modeled as a RLC network, from which a much simpler voltage control method is proposed. With the constraints and control methods in Chapter 3 and 4, a multi-objective design method is carried out to study the design tradeoffs among loss, volume and dc-current ripple of the SSB, and generates pareto front with the design constraints. Detailed volume and loss modeling, as well as the setup for the multi-objective optimization problem are provided.

Chapter 6 presents two high power density single phase converters implemented with the SSB. Within the complete ac-dc or dc-ac systems, we found that the control of the SSB can be more simplified by utilizing existing system control parameters. Detailed hardware and control design of each converter are provided. Chapter 7 discusses the buffer topologies and applications that are inspired by the fundamental operating principle of the SSB. Specifically, a half-bridge SSB concept is proposed to be an active solution for non-PFC type (no active control over the ac current) low-power (65 W) USB-C flyback adapters. Chapter 8 begins the discussion of a new type of active buffer, the bipolar multilevel full ripple port buffer. The unique challenge of using nonlinear capacitors in the buffer is explored. A control scheme that compensates for the nonlinear capacitance is purposed to maintain low extra power harmonics in the system. With high energy density ceramic capacitors, the size of the buffer capacitor is smaller than any reported active buffer work with identical conversion specifications. Detail hardware and control implementations of a high power density buffer hardware are provided.

Chapter 9 switches the topic to three-phase applications. While multilevel converters have been demonstrated in single-phase applications, applying conventional modulation scheme of two-level three-phase converters to multilevel converters is complicated as the level increases. In this chapter, a modulation strategy that is equivalent yet simpler than conventional modulation schemes is purposed for multilevel converters, which can reduce the needed filtering in the three-phase multilevel converters.

Chpater 10 identifies the remaining issues of the covered topics, as well as potential solutions for future works. Finally, Chapter 11 concludes this thesis.

Chapter 2

Single-Phase Energy Buffer Background

This chapter aims to provide an overview of the energy buffering methods for different application scenarios, and identify corresponding challenges.

2.1 Ideal Energy Buffering in Single-phase Converters

In single-phase ac-dc and dc-ac conversion scenario in Fig. 2.1, the ac current is controlled to have certain phase relation with the ac voltage to deliver desired power waveform. To simplify the analysis in this work, we consider the ac voltage and current are controlled to be low-distortion, and they can be defined with sinusoidal functions as

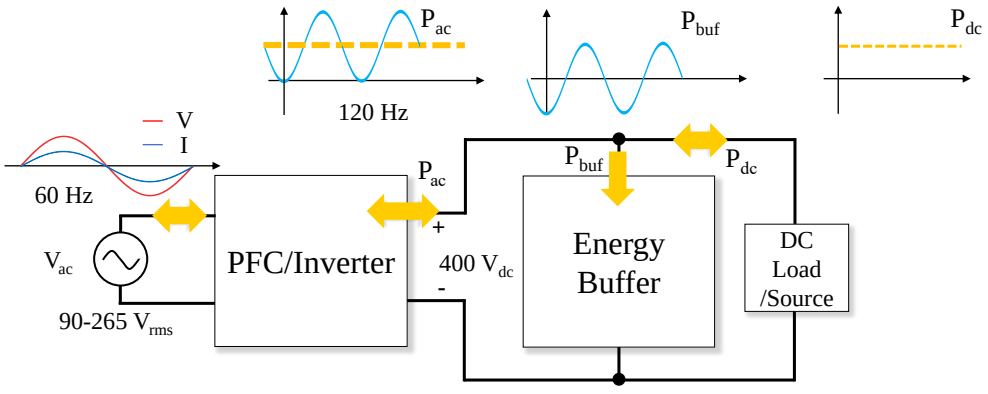

Figure 2.1: Typical single-phase conversion system block diagram for EV charging, data center power delivery and solar inverter applications.

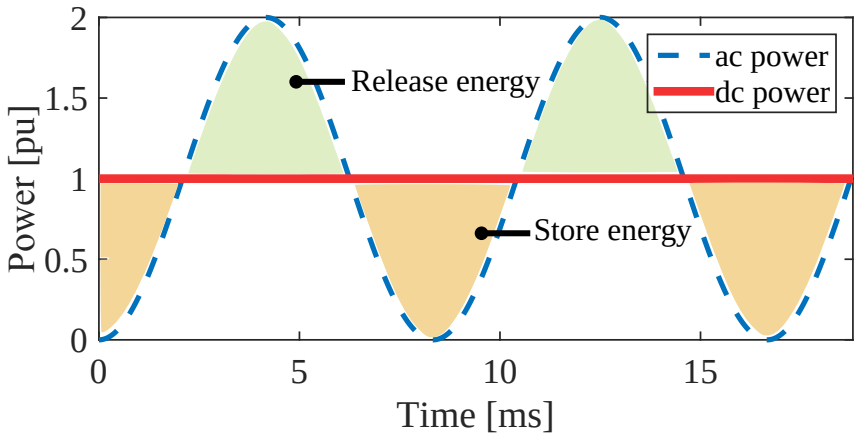

Figure 2.2: Typical dc-ac power waveform and energy flow of the energy buffering device.

$$\begin{aligned} P_{\text{ac}} &= v_{\text{ac}} i_{\text{ac}} = V_{\text{ac}} \sin(\omega_L t) \times I_{\text{ac}} \sin(\omega_L t + \phi) \\ &= \frac{1}{2} V_{\text{ac}} I_{\text{ac}} \cos(\phi) - \frac{1}{2} V_{\text{ac}} I_{\text{ac}} \cos(2\omega_L t + \phi), \end{aligned} \tag{2.1}$$

where ω_L is the ac line frequency and ϕ is the angle between the ac voltage and current. As can been seen, there is a dc power term $\frac{1}{2} V_{\text{ac}} I_{\text{ac}} \cos(\phi)$, and an ac rippling power term $\frac{1}{2} V_{\text{ac}} I_{\text{ac}} \cos(2\omega_L t + \phi)$ at the twice line frequency. We define the dc power to be

$$P_{\text{dc}} = \frac{1}{2} V_{\text{ac}} I_{\text{ac}} \cos(\phi) \tag{2.2}$$

While the dc power should be delivered to the dc side, the ac rippling power is usually not desired on the dc side. For example, the rippling power will introduce voltage ripple on the dc bus, and current ripple in the dc-side current, which might cause damage to the converters and dc load or source in the system, if they are not overly rated for the peak V/A values introduced by the ripple. As such, it is key for the single-phase converter to absorb the rippling power with an energy buffering device. The power that goes into the energy buffer can be defined as:

$$P_{\text{buf}} = P_{\text{dc}} - P_{\text{ac}} = \frac{1}{2} V_{\text{ac}} I_{\text{ac}} \cos(2\omega_L t + \phi) = \frac{P_{\text{dc}}}{\cos(\phi)} \cos(2\omega_L t + \phi) \tag{2.3}$$

And the needed energy to buffer is the area within half cycle, which can be derived as

$$E_{\text{buf, min}} = \int_{\frac{T}{4}}^{\frac{3T}{4}} |P_{\text{buf}}| = \frac{P_{\text{dc}}}{\cos(\phi)\omega_L}. \tag{2.4}$$

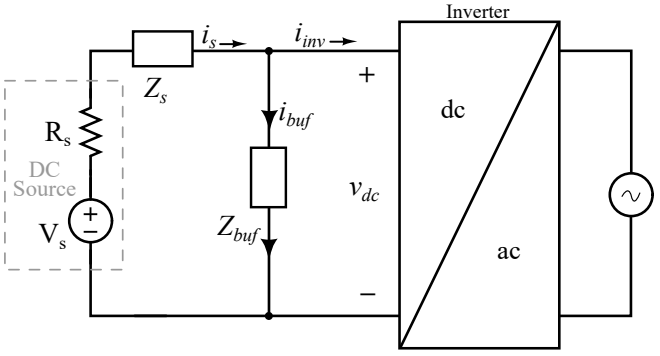

Figure 2.3: General schematic of passive filter solutions for single-phase inverters.

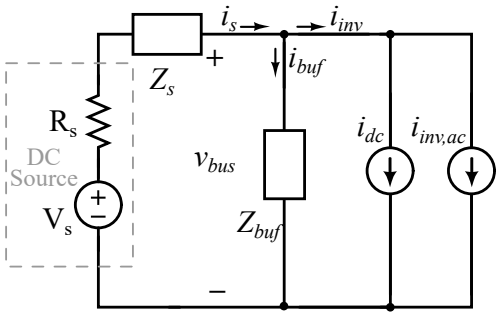

Figure 2.4: Equivalent circuit of single-phase energy buffering with inverter load modeled as current loads.

This is the minimum energy that the buffer has to absorb and supply for correct single-phase operation. Yet, as will be discussed in later chapters, with different buffer topologies and control, the energy buffer can or has to store more energy than $E_{\text{buf, min}}$ during normal operation for different purposes and constraints. In Fig. 2.2, the energy buffering process is visualized for dc-ac conversion scenario with unity power factor ($\phi = 0$). For instance, if the dc power is lower than the ac power, the energy buffer releases energy to the ac-side compensate for the difference.

In the discussion so far, assumption is made that all the rippling power (2.3) goes into the buffer and the energy storage requirement of the buffer can be derived by integrating the power. This assumption is valid in most single-phase conversion scenarios such as ac-dc PFC converter with a constant power or constant current load, and inverter with high dc source impedance [1]. In these cases, the power/current relation at the dc-bus is well-defined and P_{buf} can be directly calculated with the power relation at the dc-bus to be (2.3).

Yet, in the case where the dc-side impedance is very low, the assumption that all the rippling power goes into the buffer is not accurate. With lower dc-side impedance, a larger portion of the ripple current will be flowing into the dc source or load instead of the buffer branch. For ac-dc conversion, this scenario would be direct battery charging using the output of the PFC converter. For dc-ac conversion, this would be operating the inverter with a dc source with very low source impedance.

2.2 Passive Solutions

In this section, different buffer solutions are discussed, and associate challenges with low dc-side impedance will be addressed. For simplicity in the derivations, only inverter mode in Fig. 2.3 is considered, and the power factor angle ϕ is set to zero (unity power factor)

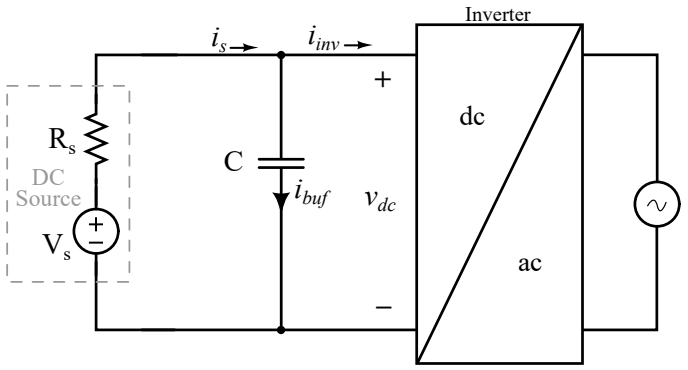

Figure 2.5: Dc-link capacitor bank solution.

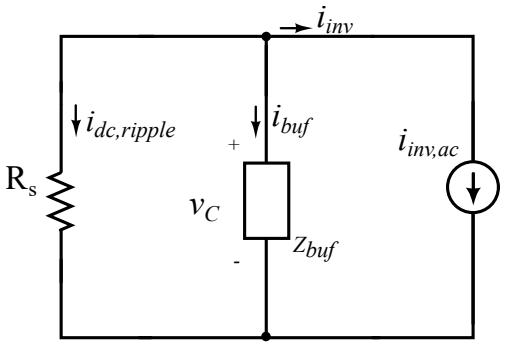

Figure 2.6: Ac equivalent circuit of the capacitor bank solution at twice-line frequency.

in this section. Nevertheless, the analysis is applicable to ac-dc PFC and non-unity power factor applications.

Since the average dc-bus voltage $V_{\rm dc}$ is much higher than the ripple voltage in most single-phase inverter applications, the dc-bus voltage can be regarded as constant in the derivation, and the inverter current drawn at the dc-bus can be modeled from the ac power as:

$$i_{\rm inv} = \frac{P_{\rm ac}}{V_{\rm dc}} = I_{\rm dc} - I_{\rm dc}\cos(2\omega_L t) = i_{\rm dc} + i_{\rm inv,ac} \tag{2.5}$$

From (2.5), the inverter load current can then be modeled as a dc current load $i_{\rm dc}$ and an ac current load $i_{\rm inv,ac}$. The equivalent circuit with buffer branch impedance $Z_{\rm buf}$ and dc-side source impedance Z_s is shown in Fig. 2.4. With passive filter solutions, the desired behavior of $Z_{\rm buf}$ and Z_s can be obtained from the fundamental current relations at the dc-bus. Ideally, we would like all the ac inverter current $i_{\rm inv,ac}$ to be absorbed into the buffer branch, with no dc current component. In the meantime, we would like all the dc current to flow only from the dc-side, and no ac current component is allowed into the dc source branch. As a result, the requirements for $Z_{\rm buf}$ and Z_s to achieve such current flow are: $Z_{\rm buf}$ should have very low impedance at the frequency of the ac component (twice-line frequency), and very high impedance at dc; Z_s should have very high impedance at the twice-line frequency, yet very low impedance at dc. With linear passive components, different combinations of RLC have been explored to achieve the desired $Z_{\rm buf}$ and Z_s. In the rest of this section, some common passive filtering solutions are discussed.

Large dc-link capacitor

The most common buffer solution for single-phase conversion is to deploy a very large capacitor bank at the dc-bus, as shown in Fig. 2.5. The large capacitor bank has to buffer the

twice-line frequency ripple power and maintain a low dc-bus voltage ripple. To start with, in the ideal case where the majority of the ripple power goes into the capacitor branch, as the capacitor stores and releases energy, the capacitor voltage ripples accordingly. Using the fundamental energy storage equation of a capacitor $\frac{1}{2}CV^2$, the change in energy in a capacitor is

$$\begin{aligned}\Delta E_C &= E_{\text{C, max}} - E_{\text{C, max}} = \frac{1}{2}C(V_{\text{max}}^2 - V_{\text{min}}^2) \\ &= \frac{1}{2}C(V_{\text{max}} + V_{\text{min}})(V_{\text{max}} - V_{\text{min}}) \\ &= CV_{\text{dc}}V_{\text{r-pk-pk}} = E_{\text{buf, min}},\end{aligned} \tag{2.6}$$

where V_{dc} is the average dc-bus voltage, $V_{\text{r-pk-pk}}$ is the peak-to-peak ripple voltage. The dc ripple current magnitude can be calculated as

$$I_{\text{dc-r-p-kpk}} = \frac{V_{\text{r-pk-pk}}}{R_s} = \frac{E_{\text{buf, min}}}{CV_{\text{dc}}R_s} = \frac{I_{\text{dc}}}{\omega_L R_s C} \tag{2.7}$$

where R_s is the source resistance,and I_{dc} is the average dc current $\frac{P_{\text{dc}}}{V_{\text{dc}}}$. However, as will be shown below, this result for calculating the ripple voltage and current is not valid when the dc resistance R_s is very low.

With superposition analysis, the circuit can be analyzed independently at dc and at twice-line frequency. Since in ac circuit analysis, dc voltage source is shorted, and dc current source is open circuit, the ac equivalent circuit at twice-line frequency of the inverter is shown in Fig. 2.6. The inverter ac current at the dc-bus is divided between the dc source and the buffer with the ratio determined by the impedances of each branch. With the current constraints at the dc-bus, the current dividing ratio defined as γ can be derived as:

$$\gamma = \frac{I_{\text{dc, ripple}}}{I_{\text{inv,ac}}} = \frac{I_{\text{dc, ripple}}}{I_{\text{dc}}} = \frac{|Z_{\text{buf}}|}{|R_s + Z_{\text{buf}}|} = \frac{1}{|1 + \frac{R_s}{Z_{\text{buf}}}|}, \tag{2.8}$$

where the magnitude of the ac portion of the inverter current $i_{\text{inv, ac}}$ is I_{dc}. and since $Z_{\text{buf}} = \frac{1}{j\omega_{2L}C}$, this ratio can be rewritten as

$$\gamma = \frac{1}{|1 + j\omega_{2L}R_sC|} = \frac{1}{\sqrt{1 + (\omega_{2L}R_sC)^2}} \tag{2.9}$$

For ratio γ to be very small so that the majority of the ac ripple goes into the buffer, Z_{buf} has to be much smaller than R_s. It is obvious that with smaller R_s, lower Z_{buf} or larger C is needed to maintain the same ratio. A new dc-side peak-to-peak ripple can thus be derived with γ as

$$I_{\text{dc-r-pk-pk, new}} = 2I_{\text{dc, ripple}} = 2I_{\text{dc}}\gamma = \frac{2I_{\text{dc}}}{\sqrt{1 + (\omega_{2L}R_sC)^2}} \tag{2.10}$$

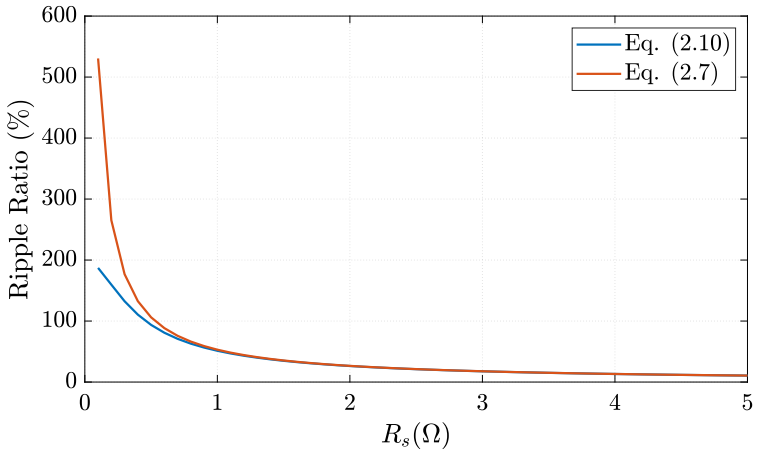

Figure 2.7: Ripple ratio comparison using (2.7) and (2.10), with $C = 5000\mu F$, $I_{\text{dc}} = 5\ A$, $\omega_{2L} = 2\pi \times 120$ rad/s.

The dc current ripple equations in (2.7) and (2.10) are then compared with a numerical example: $C = 5000\ \mu F$, $I_{\text{dc}} = 5\ A$, and R_s ranging from 0.1 Ω to 5 Ω. The dc-side current ripple ratio $\frac{I_{\text{dc-r-pk-pk, new}}}{I_{\text{dc}}}$ with both equations versus R_s is plotted in Fig. 2.7. It can be seen that with very low R_s, (2.10) shows a more reasonable limit of 200%, which corresponds to the situation that all ripple current is shorted to the dc source, and the ratio between the peak-to-peak ripple current and the dc average current is 2. The results generated with (2.7) show a ripple ratio above two, which is impossible in reality. With higher R_s, the results from these two equations become much closer. This result concludes that with very small R_s, (2.10) has to be used to properly size the dc-link capacitor. From a filter point of view, the dc resistance R_s and the capacitor bank C form a low-pass RC filter that aims to attenuate the twice-line frequency current into the dc source. With smaller R_s, it requires much higher capacitance to maintain a low cut-off frequency and high attenuation at twice-line frequency.

LC low-pass filter

From (2.8), it can be seen that a higher source impedance Z_s is desired to reduce the ripple current flowing to the dc-side. To losslessly increase the source impedance, an inductor can be added in series to the source impedance R_s, as shown in Fig. 2.8. However, since the power ripple is at twice-line frequency, the inductance has to be very high to actually reach an effective impedance. For instance, for $|Z_L| = 1\ \Omega$ at 120 Hz, the corresponding inductance is 1.3 mH. Moreover, the inductor has to carry the full dc current. As a result, the energy storage on this filter inductor $\frac{1}{2}LI^2$ is very high, leading to very large and heavy inductor design. It should also be noted that if R_s is too low, there might not be enough damping to the LC filter, causing unknown behavior near the resonant frequency $\frac{1}{2\pi\sqrt{LC}}$ caused by

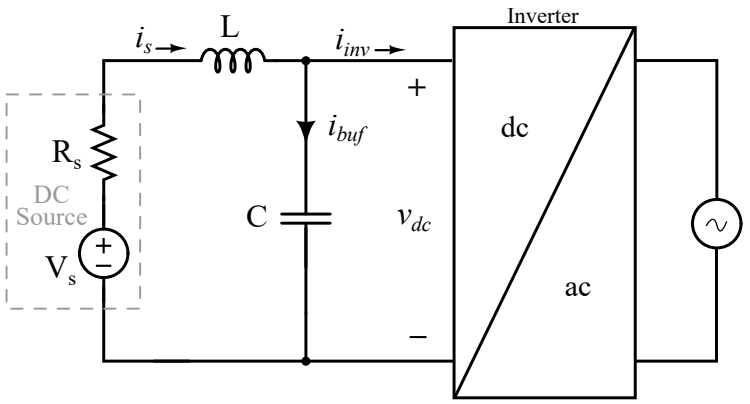

Figure 2.8: LC low-pass filter solution.

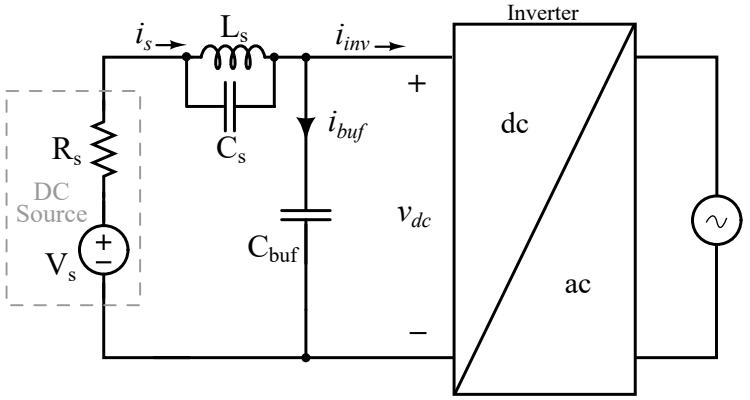

Figure 2.9: Parallel LC notch filter solution.

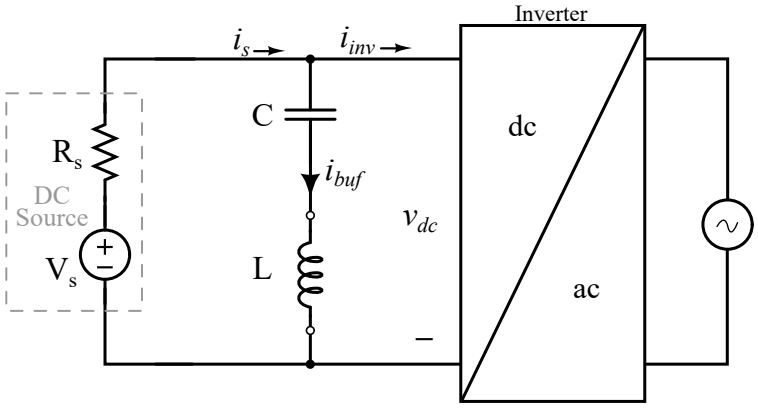

Figure 2.10: Series LC notch filter solution.

infinite gain. As such, it is critical to carefully study the frequency response of the LC low-pass filter and avoid low-damping resonant behavior.

Parallel LC notch filters on the dc-side

As discussed, the frequency response of Z_s should have very high impedance at twice-line frequency and zero dc impedance. One corresponding passive solution is to have Z_s implemented with a parallel LC resonant tank at twice-line frequency as shown in Fig. 2.9. With parallel LC resonance, the impedance at twice-line frequency is infinite. Meanwhile, the dc impedance is zero. However, similar to the LC low-pass filter, the LC resonant tank is at twice-line frequency and the inductor is carrying the full dc current, leading to very large and heavy inductor design. Moreover, a buffer capacitor is still needed to absorb $i_{\text{inv,ac}}$, which needs to be sized properly using (2.6) to limit the voltage ripple seen by the inverter.

Series LC notch filters in buffer branch

To obtain a low ripple ratio, another approach is to minimize Z_{buf}. A common solution that can achieve very low impedance at twice-line frequency is a LC resonant tank in Fig. 2.10, with resonant frequency at twice line frequency. With series LC resonance, the ideal impedance is zero at twice-line frequency, shorting all the ripple current through the buffer branch. However, similar to the LC low-pass filter and parallel LC notch filter, the size of the resonant tank is still large, and it cannot absorb high frequency noise because of the inductive impedance after the resonant frequency.

2.3 Active Solutions

Active buffer solutions leverage extra power converters to achieve the target twice-line frequency energy buffering behavior. While the topology and operation vary among different active buffer solutions, they in general improve the energy utilization of the energy storage device, and decouple any voltage and current ripple from appearing on the dc-side with active control of the auxiliary power converters. In this dissertation, two main approaches for active buffering are discussed. The first is to control the buffer to emulate an ideal impedance that can eventually block all ac ripple from the dc-side. This approach controls the buffer based on the voltage and current relations defined in the passive buffering methods. The second is controlling the buffer to directly draw the reactive power as a power port regardless of the impedances in the network. In other words, the first approach is defining an impedance relation at the dc-bus to indirectly define the power flow, while the second approach is directly defining a power relation at the dc-bus. Both methods are briefly discussed in this section. Moreover, in this thesis, two active buffer topologies designed with both operating principles are explored.

Impedance-Emulating Buffer

With linear passive RLC components, while they do not require any active control, the frequency response of the components cannot be adjusted freely to fit specific single-phase energy buffering requirement at particular frequencies of interests. Since for single-phase energy buffering application, the main voltage and current of the passive components are at twice-line frequency, active power converters switching at higher frequencies (hundreds of kilohertz) can be controlled to recreate the desired low frequency voltage and current behavior. The impedance of the active converter can be controlled to be not linearly dependent on operating frequencies to avoid unwanted behaviors at other frequencies. The approach can also utilize passive components with higher energy density as the main energy storage device to improve power density of the buffer. Moreover, by replacing just part of the passive filter network with an active converter, the converter often does not need to process the full buffer power in (2.3), resulting in high system efficiency.

Buffer emulating a high dc-side series impedance

With the parallel LC notch filter in Fig. 2.9, the goal is to increase the source impedance at twice-line frequency such that the ac current sees a very high impedance path on the dc-side, forcing the ac current to go to the buffer branch. However, high inductance is needed because of the low operating frequency, which results in physically large and heavy inductors.

With an auxiliary converter connected as in Fig. 2.11, the desired source impedance behavior of high ac (at twice-line frequency) and low dc impedance can be emulated. The series compensator in [2] is controlled such that the output voltage of the auxiliary converter equals the ripple on buffer capacitor C, with zero dc voltage bias to allow dc current to flow. By analyzing the equivalent ac circuit in Fig. 2.12, it can be seen that having the auxiliary converter voltage to be identical to the capacitor voltage is essentially the same as if Z_{aux} is open-circuit at twice-line frequency.

Buffer emulating a low impedance across dc-bus

In the passive LC notch filter solution in Fig. 2.10, with the series-resonant LC tank, the impedance at twice-line frequency is zero so that all the ripple current is shorted to the buffer branch. However, the low-frequency inductor usually dominates the physical size of the filter. Moreover, the impedance of the LC notch filter is inductive ($j\omega L$) in the frequency range above the resonant frequency $1/\sqrt{LC}$, which means it cannot attenuate higher frequency contents.

The series-stacked buffer (SSB) and similar concept proposed in [3], [4] replace the passive inductor with an auxiliary converter and an extra support capacitor as the energy source. The auxiliary converter generates a voltage that is anti-phase with the capacitor voltage ripple with zero voltage bias. In both SSB and the dc-side series-compensator, the auxiliary converters only process a small portion of the total buffer power.

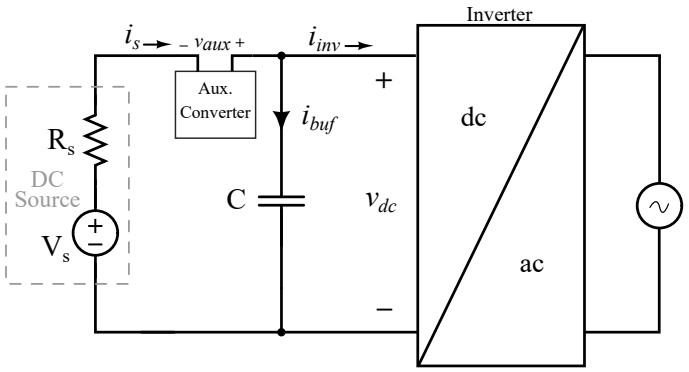

Figure 2.11: Dc-side series compensator solution.

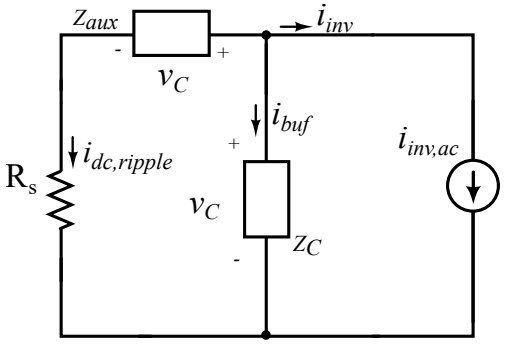

Figure 2.12: Ac equivalent circuit of the dc-side series compensator.

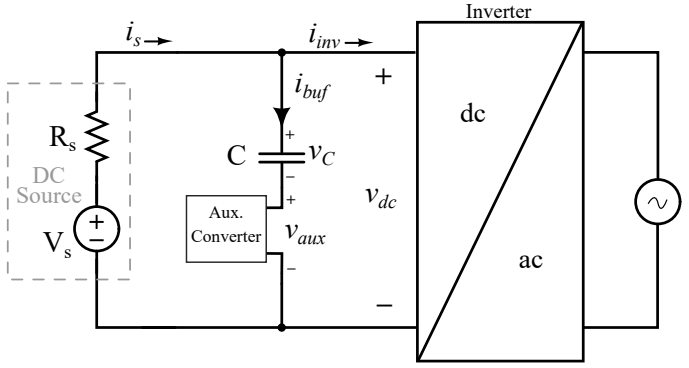

Figure 2.13: Buffer branch compensator solution.

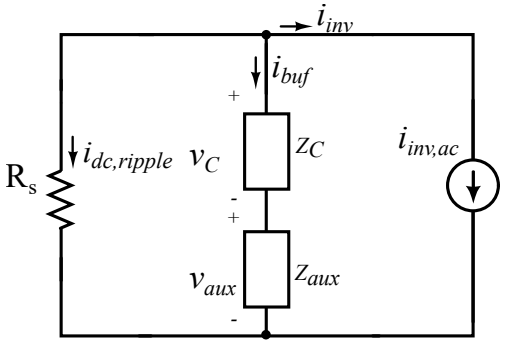

Figure 2.14: Ac equivalent circuit of the buffer branch series-stacked compensator solution.

Figure 2.14 shows the ac equivalent circuit of the series-stacked buffer. If the impedance of the auxiliary converter is controlled to resonate as an inductor with the capacitor, the impedance of the buffer branch is zero.

In the dc-side series compensator, the input voltage to the inverter is the buffer capacitor voltage, which still has significant voltage ripple. Such ripple will increase the voltage and current stress in the inverter. Whereas with the SSB, the input dc voltage to the inverter is maintained to be a pure dc voltage. Moreover, since the auxiliary converter is on the low side, the common mode voltage of the converter is much reduced compared to the dc-side series compensator, making it easier to design level-shifting and gate driving circuitry. In this thesis, the design, control and implementation of the SSB will be discussed in detail.

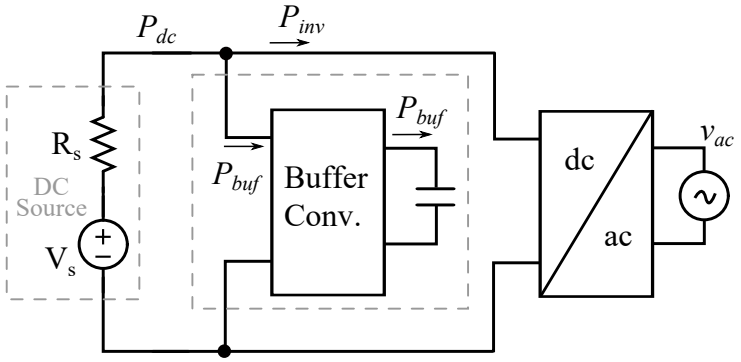

Figure 2.15: Power port buffer architecture.

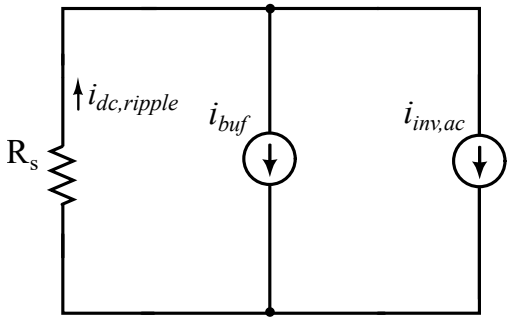

Figure 2.16: Equivalent ac circuit of the power port buffer architecture.

Power-Port Buffer

Power converters can be controlled to be constant-power loads or sources. For instance, in PFC applications, since the ac voltage and current are regulated, the power output at the dc port is equivalent to the ac-side power. Similarly, for inverter applications, if the output ac voltage is driving a resistive load (or the current is controlled to be in phase with the voltage when connecting to the grid), the power drawn into the inverter at the dc-bus P_{inv} is determined by the ac-side regardless of the impedance network at the dc-bus. As such, if another converter is controlled to draw only reactive power that can cancel the power ripple from the inverter or PFC as the energy buffer, the twice-line frequency energy buffering would be independent of the dc source impedance.

Figure. 2.15 shows the general architecture of power-port buffers. A capacitive-loaded converter is connected to the dc-bus, drawing a controlled power of P_{buf} at the dc-bus. If P_{buf} is controlled to be (2.3), the resultant P_{dc} is a pure dc value. Essentially, as long as the main buffer capacitor at the output of the buffer converter is charged and discharged to draw P_{buf} on the dc-side, the converter can operate the capacitor in many different ways: The buffer converter can be another inverter that generates a line-frequency ac voltage

to drive the capacitor [5], [6]; It can also be a buck converter operating the capacitor with certain dc-bias such that the capacitor voltage is unipolar with voltage ripple [7]; For inverter applications with relatively low dc-bus voltage, a boost converter can also be used to improve the operating voltage range of the buffer capacitor [8]. A more detailed review of power-port buffers is provided in Chapter 8 where the multilevel bipolar ripple port buffer is discussed.

The ac equivalent circuit analysis of the power-port buffers can also be performed to study the relation between the dc-source impedance and the buffer. By again assuming that the voltage ripple on the dc-bus is small, the controlled buffer power P_{buf} can be modeled as a controlled current load in Fig. 2.16, drawing the ideal buffer current i_{buf} that cancels $i_{\text{inv, ac}}$ in (2.5). In other words, if $i_{\text{buf}} + i_{\text{inv, ac}} = 0$, the dc-side ripple current would be zero regardless of R_s. As a result, as will be shown in Chapter 8, the power-port buffer can achieve very low dc-side current ripple.

Compared to the impedance-emulating buffer, power-port buffers in general have to process the full reactive power in the system to control the desired power waveform. Consequently, the loss from the buffer converter will be relatively high, and the actual converter implementation is usually larger. Nevertheless, as will be shown in Chapter 8, general techniques to design high efficiency and power density converters can be applied to improve the performance of the buffer converters.

2.4 Energy Storage, Passive Components and Converter Sizing

Energy utilization ratio

In both passive and active energy buffer solutions, the required energy in (2.4) has to be stored and supplied by the buffers. Yet, with different energy buffer solutions, the maximum stored energy in buffers are different. To quantify the relation between the required buffering energy and the maximum energy storage in buffers, the energy utilization ratio (EUR) is defined as:

$$\Gamma_{\text{EUR}} = \frac{E_{\text{buf,min}}}{\sum E_{\text{C1,C2,C3...}}(V_{\max}) + \sum E_{\text{L1,L2,L3...}}(I_{\max})}, \tag{2.11}$$

where the denominator is the sum of the peak energy of all the energy storage passive devices in the buffer. The achievable EUR is largely dependent on the buffer topologies and the properties of the passive devices themselves. Starting with the simplest capacitor bank solution, the EUR can be calculated from the capacitor energy at the peak dc-bus voltage. In most single-phase applications, the dc-bus is required to have low voltage ripple. From (2.6), we can get the expression for the voltage ripple with regard to $E_{\text{buf, min}}$ to be:

$$V_{\text{r-pk-pk}} = \frac{E_{\text{buf,min}}}{CV_{\text{dc}}} = \frac{P_{\text{dc}}}{\omega_{\text{L}} CV_{\text{dc}}} \tag{2.12}$$

A numerical example can be given to demonstrate the EUR of the capacitor bank solution. If the ripple voltage is required to be below 3% of the average dc-bus voltage, for a conversion specification of $P_{\text{dc}} = 2$ kW, line frequency of 60 Hz, and dc-bus of 400 V, the required dc-bus capacitance is 1.1 mF, and the maximum capacitor voltage is $400+0.5V_{\text{r-pk-pk}} = 406$ V. By plugging into (2.11), the EUR can be obtained as:

$$\Gamma_{\text{EUR, cap-bank}} = \frac{E_{\text{buf,min}}}{\frac{1}{2}CV_{\text{max}}^2} = \frac{5.3\ J}{90\ J} = 5.9\%. \tag{2.13}$$

This result shows that only around 6% of the capacitor energy is used for single-phase energy buffering. Fundamentally, this is because with capacitor bank, the EUR is directly tied to the low voltage-ripple ratio on the dc-bus. With the help of extra power converters, the EUR can be decoupled with the voltage or current ripple ratio requirements, and less energy can be stored in the passive devices during normal operation. For instance, the power port buffer in Fig. 2.15 can apply a high voltage swing on the buffer capacitor to improve EUR and maintain the input voltage to be dc on the two sides of the buffer converter respectively.

Passive component and converter sizing in active buffers

To shrink the size of passive components, the first effort, as discussed, is to reduce the energy storage, or improve the EUR in the passive components. Yet, what is equally important is the energy density (energy per volume) of the particular passive component technologies themselves. In recent efforts to pursue the design of high power density converters, ceramic capacitors are found to have orders of magnitude higher energy density than inductors [9]. As such, it is also desirable to utilize capacitive energy storage in the buffer application. Among capacitors, different technologies also have different energy density and other related properties: while the electrolytic capacitors have very high dc energy density (energy holding a dc voltage), they do not allow very large voltage ripple due to the high series resistance in the capacitor; For ceramic capacitors, their energy density is dependent on the operating voltage waveforms [10]; Film capacitors have much lower dc energy density, but since their series resistance is very low, the allowed voltage ripple could be very high. Among active buffer topologies, the topologies that can achieve very high EUR and small capacitor size are not always the overall smallest and best performing buffer solutions, if the size and loss of the extra buffer converters are considered. That is, in many buffer applications, higher EUR on the main buffer capacitor will either introduce more loss or require the buffer converter to process more power, resulting in larger converter design. For this reason, the two main buffer topologies explored in this thesis are designed with different philosophies to improve the overall system performance:

- The SSB topology discussed in Chapter 3 to 6 can only achieve around 50% EUR, but since the extra converter processes only less than 10% of the total reactive power, the converter size and the extra loss from the converter is very low, which means the total capacitor plus converter volume can potentially be very small.

- The bipolar multilevel full ripple port in Chapter 8 can achieve 100% EUR. Yet, the buffer converter has to process the full ripple power. With conventional two-level solution, the buffer converter is lossy and large. However, if high performance multilevel converters are deployed as the buffer converter to improve efficiency and power density, the overall capacitor and converter size, as well as the efficiency would also be attractive.

Chapter 3

Operation Principle and Constraints of the Series-Stacked Buffer

3.1 Introduction to the Series-Stacked Buffer Topology

The series-stacked buffer (SSB), shown in Fig. 3.1, is a type of active energy buffer. The energy buffering capacitor C_1 stores and releases energy at the twice-line frequency with a large voltage ripple, which allows a high energy utilization ratio to reduce the required capacitance, compared to the passive capacitor bank solution. A bi-directional converter is connected in series with C_1 and generates a terminal voltage $v_{\rm ab}$ that cancels the ripple component on $v_{\rm C1}$ such that the dc-bus is ripple-free. Moreover, since the bi-directional converter only processes a fraction of the total power in the dc-ac conversion stage, the resulting high overall system efficiency is comparable to the passive capacitor bank solution. The high power density and high efficiency characteristics of the SSB have been demonstrated in [3], [11].

3.2 Operation Principle

In this section, the ideal operation of the SSB is demonstrated with a dc to ac conversion scenario for a 400 W load and a 200 V dc-bus.

With a resistively-loaded inverter and a dc-bus with small voltage ripple, the inverter load is modeled as a dc-shifted sinusoidal current $i_{\rm inv}$ as

$$i_{\rm inv} = I_{\rm dc}\sin(\omega_{\rm 2L}t) + I_{\rm dc}, \tag{3.1}$$

whose amplitude and dc offset equal the ideal dc source current $I_{\rm dc}$, and $\omega_{\rm 2L} = 2\pi \times 120$ rad/s, which is twice of the line frequency (i.e., 100 or 120 Hz). The corresponding $I_{\rm dc}$ in this example is 2 A. (Note that this is essentially the same equation as (2.5), yet since in

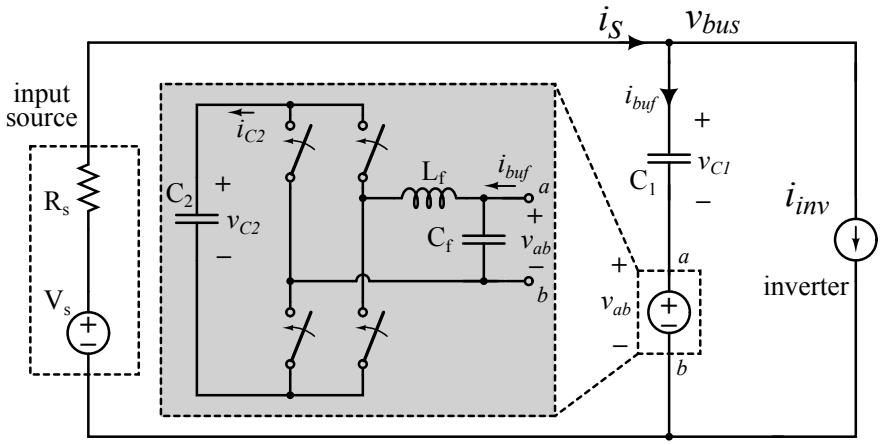

Figure 3.1: The series-stacked buffer architecture with a dc source and an inverter (represented as a current load).

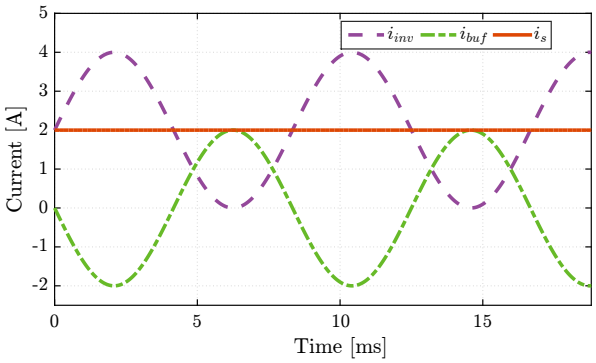

Figure 3.2: The ideal current waveforms for the SSB. $C_1 = 80$ μF, $V_{\text{bus}} = 200$ V, 400 W load power.

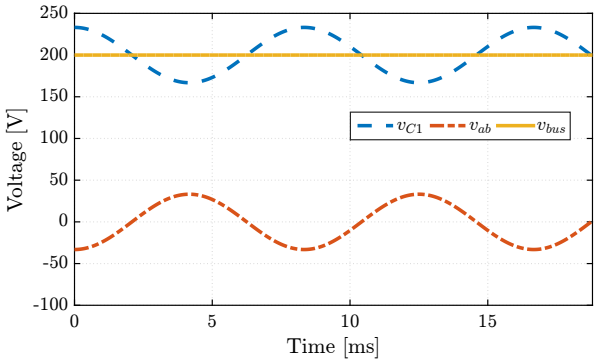

Figure 3.3: The ideal voltage waveforms for the SSB. $C_1 = 80$ μF, $V_{\text{bus}} = 200$ V, 400 W load power.

this chapter we focus on the internal voltage and current relations of the SSB, the phase reference is set differently. Nevertheless, as long as the inverter current is modeled with a dc shifted sinusoidal function, the passive component sizing is not affected.)

Since current constraints at the dc-bus give

$$i_{\text{S}} = i_{\text{inv}} + i_{\text{buf}}, \tag{3.2}$$

for the current from the dc source i_{S} to be a pure dc current (i.e., $i_{\text{S}} = I_{\text{dc}}$), the current flowing into the buffer branch i_{buf} should cancel the ac portion of the inverter current,

$$i_{\text{buf}} = -I_{\text{dc}} \sin(\omega_{2\text{L}} t). \tag{3.3}$$

The waveforms for i_{inv}, i_{buf} and i_{S} for ideal SSB operation are shown in Fig. 3.2. The capacitor C_1 instantaneously stores and releases the twice-line frequency energy with corresponding voltage ripple. Moreover, since v_{ab} is controlled with no dc-offset, the dc-bus voltage V_{bus} appears completely on C_1. We can obtain the expression for the instantaneous charge on C_1 to be

$$q_{\text{C1}} = \int i_{\text{buf}}\, dt = \frac{I_{\text{dc}}}{\omega_{\text{2L}}} \cos(\omega_{\text{2L}} t) + Q_{\text{init}} = \Delta q_{\text{C1}} + C_1 V_{\text{bus}}, \tag{3.4}$$

where Δq_{C1} can be used to calculate the instantaneous voltage ripple to be

$$\Delta v_{\text{C1}} = \frac{\Delta q_{\text{C1}}}{C_1} = \frac{I_{\text{dc}}}{\omega_{\text{2L}} C_1} \cos(\omega_{\text{2L}} t). \tag{3.5}$$

The expression for v_{C1} can be found as

$$v_{\text{C1}} = V_{\text{bus}} + \Delta v_{\text{C1}}. \tag{3.6}$$

For $v_{\text{C1}} + v_{\text{ab}}$ to equal the dc value V_{bus}, the output voltage from the buffer converter v_{ab} should cancel the ripple voltage on C_1. The expression for v_{ab} is then

$$v_{\text{ab}} = -\Delta v_{\text{C1}} = -\frac{I_{\text{dc}}}{\omega_{\text{2L}} C_1} \cos(\omega_{\text{2L}} t). \tag{3.7}$$

The voltage waveforms for v_{C1}, v_{ab} and V_{bus} for ideal SSB operation are shown in Fig. 3.3. To generate the ideal v_{ab} using the full-bridge converter, v_{C2} has to be actively maintained by a feedback control loop, which will be presented in detail in later chapters.

3.3 Operation Constraints for Major Passive Components

In previous works on the SSB [3], [12]–[14] or similar concepts [4], [15], the bi-directional converter has been implemented with a full-bridge inverter that generates a pure ac waveform across terminal *ab*, as shown in the shaded area in Fig. 3.1. Ignoring the converter power loss, there is no net-energy flow from or into the full-bridge converter in one twice-line frequency cycle. As a result, no active power source is needed and a support capacitor C_2 can instead function as the dc voltage source. A series of design guidelines that determines the minimum passive component values (i.e., C_1 and C_2) were derived in [3], [12], [13].

In this thesis, a set of new design constraints are derived by analyzing the power flow through the buffer, which show that the SSB can actually operate with much smaller C_1 and C_2 combinations than the minimal values calculated in [3], [12], [13], given the same operating conditions. The derived results thus enables more optimized system solutions for the SSB architecture, compared to previous hardware demonstrations, which were overly conservative in the design [3], [4], [12]–[15].

Derivation of the Design Constraint

While an appropriate value for C_1 can be chosen based on (7.5) for a given load, the value for C_2 must also satisfy certain conditions to ensure that the buffer converter is able to generate the correct v_{ab} in (3.7).

Note that since the switching frequency of the full-bridge converter is usually three orders of magnitude higher than the twice-line frequency, and the filter inductor and capacitor in the full-bridge converter are also chosen appropriately to only filter the switching ripple, all the voltage and current expressions in this section are time-average values over one switching cycle.

Assuming no loss in the buffer converter, the instantaneous power transferred to (or from) C_2 should equate to the power at the output terminals ab as

$$v_{\mathrm{C2}} i_{\mathrm{C2}} = v_{\mathrm{ab}} i_{\mathrm{buf}}. \tag{3.8}$$

Since v_{C2} and i_{C2} can be related by the capacitance of C_2 as

$$i_{\mathrm{C2}} = C_2 \frac{dv_{\mathrm{C2}}}{dt}, \tag{3.9}$$

by substituting in (3.3) and (3.7), (3.8) can be rewritten as

$$C_2 v_{\mathrm{C2}} \frac{dv_{\mathrm{C2}}}{dt} = \frac{I_{\mathrm{dc}}^2}{\omega_{\mathrm{2L}} C_1} \cos(\omega_{\mathrm{2L}} t) \sin(\omega_{\mathrm{2L}} t), \tag{3.10}$$

which is a first-order differential equation. The general solution of v_{C2} can be found as

$$v_{\mathrm{C2}} = \sqrt{\frac{2K}{C_2} - \frac{I_{\mathrm{dc}}^2}{2\omega_{\mathrm{2L}}^2 C_1 C_2} \cos(2\omega_{\mathrm{2L}} t)}, \tag{3.11}$$

where the constant K is determined from the particular solution for v_{C2}. It can be observed that within the square root in (3.11), there is a constant term and a sinusoidal term. When $cos(2wt) = 0$, v_{C2} is defined as $V_{\mathrm{C2,\,dc}}$. Correspondingly, the constant K in (3.11) can be derived as

$$K = \frac{1}{2} C_2 V_{\mathrm{C2,\,dc}}^2, \tag{3.12}$$

and a particular solution for v_{C2} in (3.10) can be found as

$$v_{\mathrm{C2}} = \sqrt{V_{\mathrm{C2,\,dc}}^2 - \frac{I_{\mathrm{dc}}^2}{2\omega_{\mathrm{2L}}^2 C_1 C_2} \cos(2\omega_{\mathrm{2L}} t)}. \tag{3.13}$$

Notice that the expression in (3.12) suggests that K can be regarded as the dc energy that C_2 holds during normal operation.

Since the buffer converter is a full-bridge converter, the conversion ratio m and the duty ratio d are related as

$$m = 2d - 1 = \frac{v_{\mathrm{ab}}}{v_{\mathrm{C2}}}. \tag{3.14}$$

To avoid over-modulation, the conversion ratio m must satisfy $|m| \leq 1$. Since the expressions for both v_{ab} and v_{C2} are known, this constraint can be expressed with the inequality

$$\frac{v_{\mathrm{ab}}}{v_{\mathrm{C2}}} = \frac{|\frac{I_{\mathrm{dc}}}{\omega_{2\mathrm{L}} C_1} \cos(\omega_{2\mathrm{L}} t)|}{\sqrt{V_{\mathrm{C2,\,dc}}^2 - \frac{I_{\mathrm{dc}}^2}{2\omega_{2\mathrm{L}}^2 C_1 C_2} \cos(2\omega_{2\mathrm{L}} t)}} \leq 1. \tag{3.15}$$

The maximum value of $|\frac{v_{\mathrm{ab}}}{v_{\mathrm{C2}}}|$ can be obtained when $wt = 0, \pi, 2\pi, ...$, and as long as it is less than or equal to one, (3.15) is satisfied and over-modulation is avoided. This condition is expressed as

$$\frac{v_{\mathrm{ab}}}{v_{\mathrm{C2\,max}}} = \frac{\frac{I_{\mathrm{dc}}}{\omega_{2\mathrm{L}} C_1}}{\sqrt{V_{\mathrm{C2,\,dc}}^2 - \frac{I_{\mathrm{dc}}^2}{2\omega_{2\mathrm{L}}^2 C_1 C_2}}} \leq 1, \tag{3.16}$$

which can be further simplified to

$$\frac{I_{\mathrm{dc}}}{\omega_{2\mathrm{L}}} = \Delta q_{\mathrm{C1,\,max}} \leq C_1 V_{\mathrm{C2,\,dc}} \sqrt{\frac{2C_2}{2C_2 + C_1}}. \tag{3.17}$$

3.4 Comparison to Previous Work on Component Sizing

Design Constraints

The constraint in (3.17) relates the passive component values and load current for ideal buffer operation. A similar design constraint for the SSB derived and utilized in [3], [12], [13] is defined below as

$$\Delta q_{\mathrm{C1,\,max}} \leq V_{\mathrm{C2,\,dc}} \frac{C_1 C_2}{C_2 + C_1}. \tag{3.18}$$

To compare the two constraints given in (3.17) and (3.18), the power level for the dc-ac conversion is set to 400 W, with a 200 V dc-bus voltage. This condition will give a corresponding I_{dc} of 2 A. Once I_{dc} is determined, C_1, C_2, and $V_{\mathrm{C2,\,dc}}$ are free variables that must satisfy (3.17) or (3.18). If two of these variables are fixed, the requirements for the remaining variable can be determined. In this section, C_1 and $V_{\mathrm{C2,\,dc}}$ are chosen to be 80 μF and 42 V, respectively. Equation (3.17) and (3.18) will produce different requirements for the capacitance value of C_2, which are

$$C_2 \geq 68\ \mu F \tag{3.19}$$

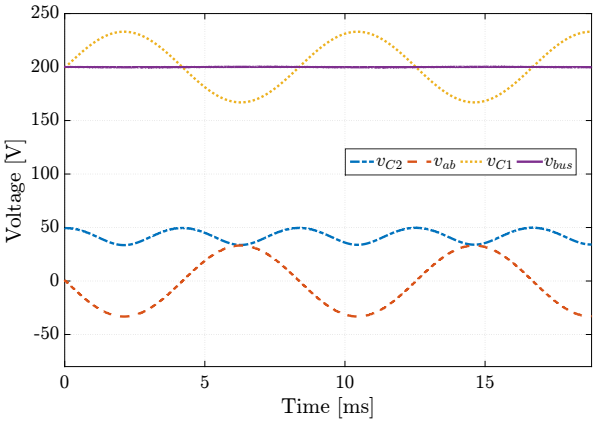

Figure 3.4: Simulated voltage waveforms of the SSB in PLECS for the test case: $C_1 = 80$ μF, $C_2 = 68$ μF, $V_{\mathrm{C2,\,dc}} = 42$ V, $I_{\mathrm{dc}} = 2$ A.

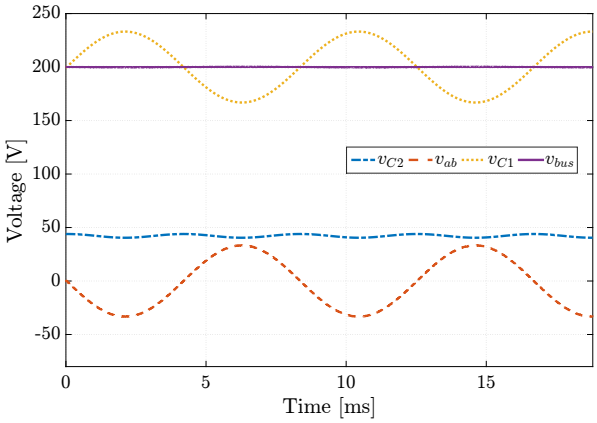

Figure 3.5: Simulated voltage waveforms of the SSB in PLECS for the test case: $C_1 = 80$ μF, $C_2 = 307$ μF, $V_{\mathrm{C2,\,dc}} = 42$ V, $I_{\mathrm{dc}} = 2$ A.

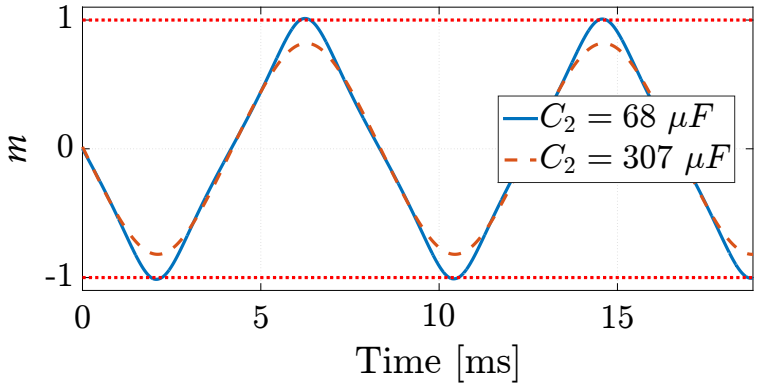

Figure 3.6: Corresponding conversion ratios for $C_2 = 68$ μF and $C_2 = 307$ μF for the test case: $C_1 = 80$ μF, $V_{\mathrm{C2,\,dc}} = 42$ V, $I_{\mathrm{dc}} = 2$ A.

for (3.17), and

$$C_2 \geq 307\ \mu F \tag{3.20}$$

for (3.18).

The resultant simulated waveforms of v_{bus}, v_{ab}, v_{C1}, and v_{C2} when $C_2 = 68$ μF are illustrated in Fig. 3.4. It can be seen that the peak of v_{ab} overlaps with the minimum value of v_{C2}, indicating a conversion ratio m that is very close to one at this point. Figure 3.5 shows the resultant voltage waveforms when $C_2 = 307$ μF. Compared to the waveforms in Fig. 3.4, the peak of v_{ab} in Fig. 3.5 is still 10 V below the minimum value of v_{C2}, which indicates that the conversion ratio m is not as close to one. The corresponding conversion

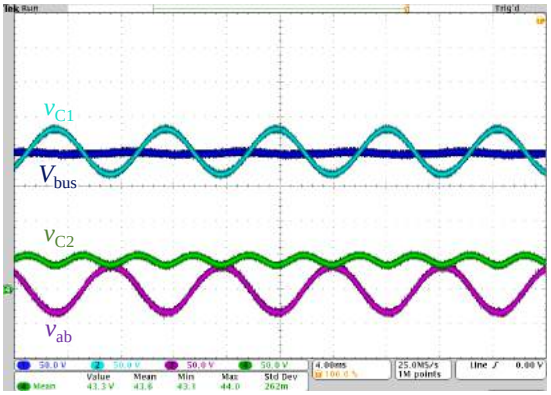

Figure 3.7: Experimental voltage waveforms of the SSB for the test case: $C_1 = 80\ \mu$F, $C_2 = 68\ \mu$F, $V_{C2,\,dc} = 42$ V, $I_{dc} = 2$ A.

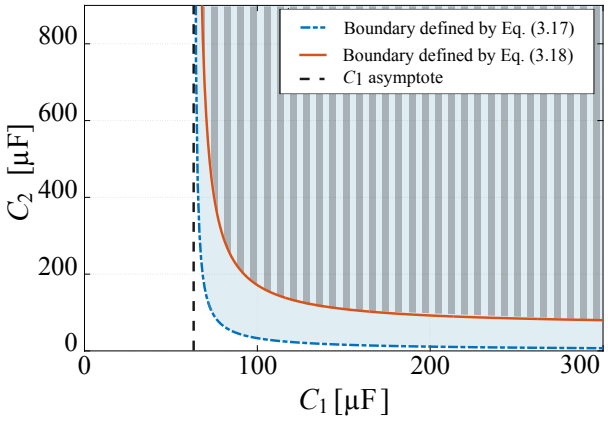

Figure 3.8: Design space for C_1 and C_2 under the constraints: $V_{C2,\,dc} = 42$ V, $I_{dc} = 2$ A (solid-filled shaded area is confined by (3.17), and striped area is confined by (3.18)).

ratios for these two test cases are plotted in Fig. 3.6 for comparison. As shown in Fig. 3.6, the peak conversion ratio when $C_2 = 68\ \mu$F is approximately one, while the peak conversion ratio when $C_2 = 307\ \mu$F is only 0.8. The required C_2 in (3.19) is also experimentally verified as shown in Fig. 3.7.

The simulation and the experimental results show that the design constraint in (3.18) generates a relatively conservative result regarding sizing C_2. We can further compare the allowed design space for C_1 and C_2 by (3.17) and (3.18) for the condition $V_{C2,\,dc} = 42$ V and $I_{dc} = 2$ A. The over-modulation boundary condition curves defined by (3.17) and (3.18) are illustrated in Fig. 3.8, and the areas above these two curves are the allowed design space for C_1 and C_2. It can be seen that the design space confined by (3.18) is within the one confined by (3.17). Moreover, we can see that these two boundary condition curves share the same asymptote for C_1 as C_2 increases. This is because as C_2 approaches infinity, the right-hand-side (RHS) of both (3.17) and (3.18) have the same limit as

$$\begin{aligned}\lim_{C_2\to\infty} C_1 V_{C2,\,dc}\sqrt{\frac{2C_2}{2C_2+C_1}} &= \lim_{C_2\to\infty} V_{C2,\,dc}\frac{C_1C_2}{C_2+C_1}\\ &= V_{C2,\,dc}C_1,\end{aligned} \tag{3.21}$$

which determines the asymptote for C_1 at the boundary condition as

$$C_1 \geq \frac{\Delta q_{C1,\,max}}{V_{C2,\,dc}}. \tag{3.22}$$

Equation (3.21) and (3.22) show that only when $C_2 \gg C_1$ will (3.18) produce similar component sizing requirements to (3.17). In other words, it can only approximate the over-modulation boundary condition for the SSB when $C_2 \gg C_1$.

Conclusions

In summary, the derived design constraint (3.17) in this work more accurately identifies the limiting operating conditions of the SSB, which enables better optimized component sizing than previous hardware demonstrations. In later chapters, this constraint is used in the multi-objective design and optimization study of the SSB.

Chapter 4

Control and Modeling of the Series-Stacked Buffer

4.1 Equivalent Impedance Modeling for the SSB

RLC resonant tank model

In the ideal operation of the SSB in last chapter, by controlling v_{ab} to have zero dc-offset and be in antiphase with Δv_{C1}, the SSB can be shown to behave as an LC resonant tank at the twice-line frequency, where the buffer converter emulates an inductor that resonates with C_1 [16], as shown in Fig. 4.1.

If the full-bridge converter voltage is only emulating inductor, the power into the full-bridge is purely reactive, i.e., no dc component and the net change in energy within one half line cycle is zero. However, in real implementation, in order to generate the correct voltage v_{ab}, the voltage on the supporting capacitor C_2 has to be actively maintained above v_{ab}. Since the converter is lossy, real power or positive net energy has to be drawn into the buffer to maintain v_{C2}. This can be done by adding a voltage term that is in-phase with the buffer current i_{buf}. The in-phase voltage and current relation can also be modeled as having an equivalent series resistance R_{ab} in the SSB as shown in Fig. 4.2.

Phasor representation of the steady-state voltage and current

To visually analyze the voltage and current in impedance networks at a single frequency in steady state, voltage and current in the network can be represented with the phasor notation. The phasor diagrams at the twice-line frequency for both the ideal LC model and the RLC model with loss compensation are shown in Fig. 4.3.

The phase of the buffer current is set to be $\frac{3}{2}\pi$ as an example (which is the same phase as in last chapter's derivation, yet this phase can be arbitrary as long as the phase is consistent in the derivation). As can be seen in Fig. 4.3, in the ideal loss case with the series LC resonant tank model, the voltage phasors of v_{C1} and v_{ab} are equal in magnitude and opposite in phase,

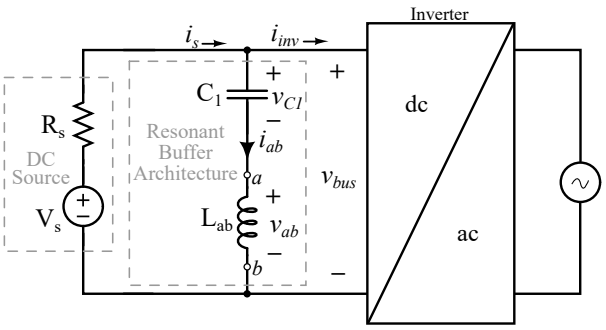

Figure 4.1: Equivalent LC circuit of the SSB (figure created in collaboration with Nathan Brooks).

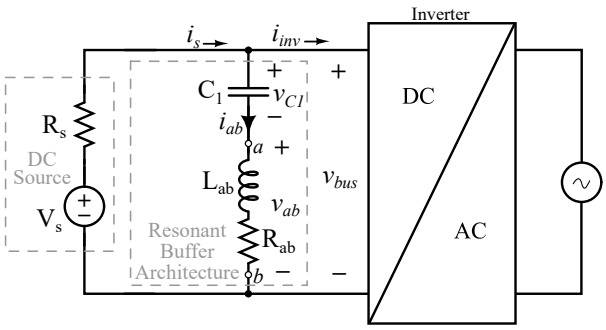

Figure 4.2: Equivalent RLC circuit of the SSB, with v_{C2} loss compensation (figure created in collaboration with Nathan Brooks).

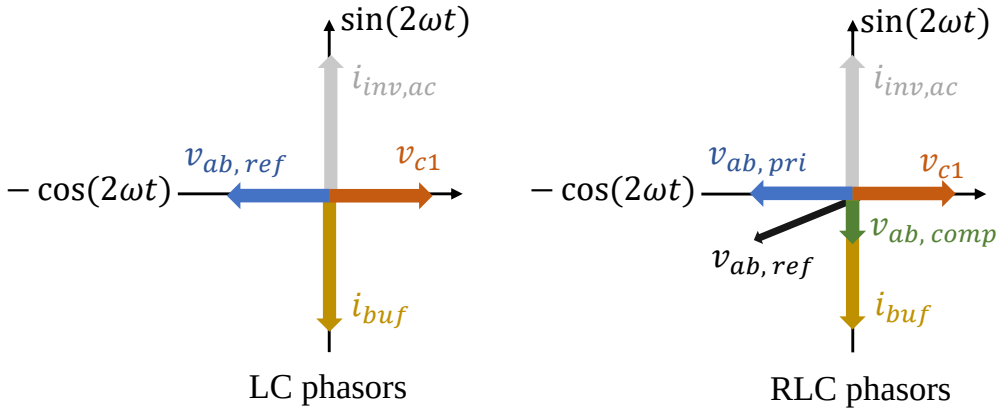

Figure 4.3: Phasor diagrams at 120 Hz for both LC and RLC models of the SSB.

and they are perpendicular to the buffer current as they are both reactive. In the case where real power has to be drawn into the buffer, the resistive voltage term is in-phase with the buffer current, noted as $v_{\text{ab, comp}}$. The inductive voltage term, noted as $v_{\text{ab, pri}}$, is still the primary component of the final reference voltage $v_{\text{ab, ref}}$, which is the vector sum of $v_{\text{ab, pri}}$ and $v_{\text{ab, comp}}$.

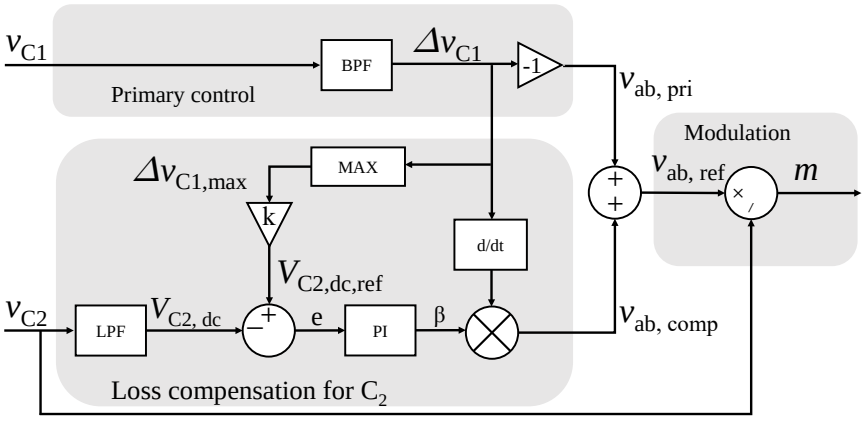

Figure 4.4: Voltage control method for the SSB [16].

4.2 Voltage Control of the SSB Based on the RLC Model

Voltage reference generation

To generate the needed $v_{\text{ab, pri}}$ and $v_{\text{ab, comp}}$, a voltage based control is proposed [16], as shown in the control diagram in Fig. 4.4. To generate $v_{\text{ab, pri}}$, the ripple of v_{C1} is extracted with a band-pass filter, with a center frequency at the twice-line frequency. Once the ripple is obtained, $v_{\text{ab, pri}}$ will just be the negative of the ripple.

To generate the correct $v_{\text{ab, comp}}$, the magnitude of the resistive voltage $v_{\text{ab, comp}}$ is controlled by a PI compensator that monitors the dc value of v_{C2}. To obtain the phase of the buffer current, since the ripple on v_{C1} is measured, a voltage term that is in phase with the buffer current can be obtained using the fundamental capacitor voltage/current relation $i_c = C\frac{\mathrm{d}V_c}{\mathrm{d}t}$. To take the derivative in the digital controller, a differentiator has to be implemented [16]. Finally, $v_{\text{ab, pri}}$ and $v_{\text{ab, comp}}$ are added to be the reference voltage for the full-bridge modulation.

This control method only uses internal voltage signals v_{C1} and v_{C2}. As such, it makes the SSB a true two-terminal device, as no outside information is needed for control. This is desirable for applications where the buffer needs to be relatively independent from the rest of the single-phase conversion systems. Yet, if the SSB is controlled together with the main PFC or inverter stage, the band-pass filter and the digital differentiator would occupy significant computing budgets. To simplify the system control, if the frequency, phase and power information in the full single-phase system can be accessed by the SSB controller, correct buffer voltages can also be computed and generated. Such controls are presented in Chapter 6 in more details.

SSB impedance defined by the band-pass filter

While the behavior of the SSB in the steady-state can be captured by the series RLC model, the behavior at frequencies other than the twice-line frequency is largely dependent on the actual transfer function of the band-pass filter. To simplify the analysis, an examplar second-order band-pass filter in continuous domain can be expressed as

$$\begin{aligned} G_{bpf}(s) = 1 - G_n(s) &= 1 - \frac{s^2 + \omega_{2L}}{s^2 + \frac{\omega_{2L}}{Q}s + \omega_{2L}^2} \\ &= \frac{\frac{\omega_{2L}}{Q}s}{s^2 + \frac{\omega_{2L}}{Q}s + \omega_{2L}^2}, \end{aligned} \tag{4.1}$$

where Q is the quality factor of the filter. Since the voltage term for loss compensation is much smaller than the primary inductive voltage, it can be ignored for a cleaner derivation. As a result, the reference voltage of v_{ab} in s-domain is thus

$$v_{\text{ab,ref}}(s) = -G_{bpf}(s)v_{\text{C1}}(s). \tag{4.2}$$

The total impedance of the SSB on the dc-bus can be calculated as

$$\begin{aligned} Z_{\text{buf}}(s) = \frac{v_{\text{bus}}(s)}{i_{\text{buf}}(s)} &= \frac{v_{\text{C1}}(s)}{i_{\text{buf}}(s)} + \frac{v_{\text{ab}}(s)}{i_{\text{buf}}(s)} \\ &= Z_{\text{C1}}(s) + Z_{ab}(s) \\ &= Z_{\text{C1}}(s)(1 - G_{bpf}) \\ &= Z_{\text{C1}}(s)G_n(s) = \frac{1}{sC_1}G_n(s) \end{aligned} \tag{4.3}$$

Essentially, $G(n)$ is a notch filter centered at the twice-line frequency, which has a very low gain near the twice-line frequency, and unity gain at other frequencies. The corresponding bode plot of the buffer impedance is presented in Fig. 4.5 It can be seen that because of the notch filter transfer function, the impedance at the twice-line frequency is very low, which is consistent with the resonant tank behavior. In other frequencies, the impedance is dominated by C_1. As such, it is reasonable to expect that at other frequencies, the SSB can be regarded as having C_1 across the dc-bus.

Relation between buffer converter power loss and $v_{\text{ab, comp}}$

With the phase angles defined in Fig. 4.3, the loss compensation voltage term can be expressed as

$$v_{\text{ab, comp}} = -V_{\text{comp}} \sin(\omega_{2\text{L}}t), \tag{4.4}$$

where V_{comp} is the magnitude. As the primary control path is canceling the ripple on C_1, the final reference voltage $v_{\text{ab, ref}}$ is

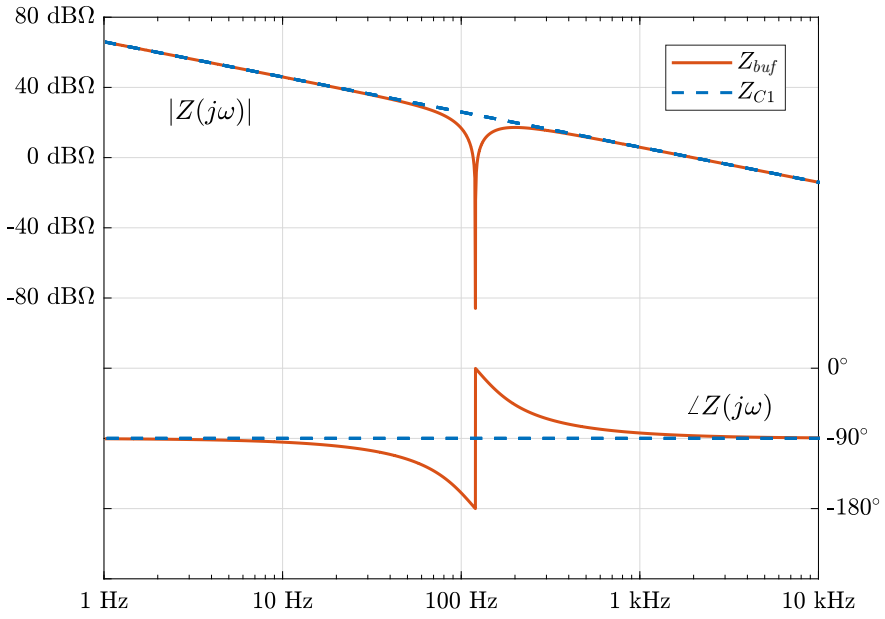

Figure 4.5: Bode plot of the SSB impedance with the band-pass filter (figure created in collaboration with Nathan Brooks).

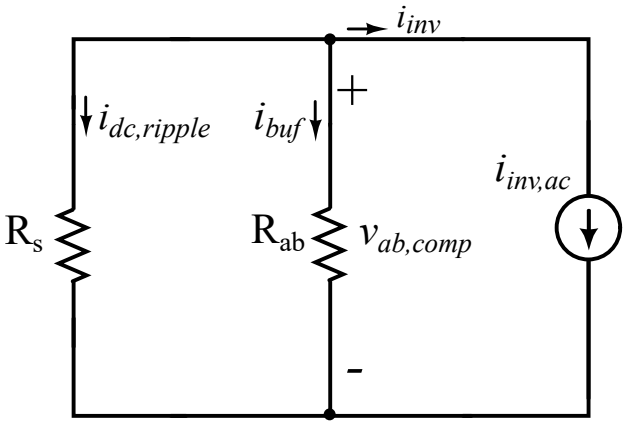

Figure 4.6: Equivalent ac impedance of the SSB. The LC resonant tank is omitted because of their zero ohm impedance at resonance.

$$v_{\text{ab, ref}} = -\Delta v_{\text{C1}} + v_{\text{ab, comp}} \tag{4.5}$$

Assuming the actual v_{ab} equals the reference voltage $v_{\text{ab, ref}}$, the dc-bus voltage equals to

$$\begin{aligned} v_{\text{bus}} = v_{\text{C1}} + v_{\text{ab}} &= (V_{\text{bus}} + \Delta v_{\text{C1}}) + (-\Delta v_{\text{C1}} + v_{\text{ab, comp}}) \\ &= V_{\text{bus}} + v_{\text{ab, comp}} \end{aligned} \tag{4.6}$$

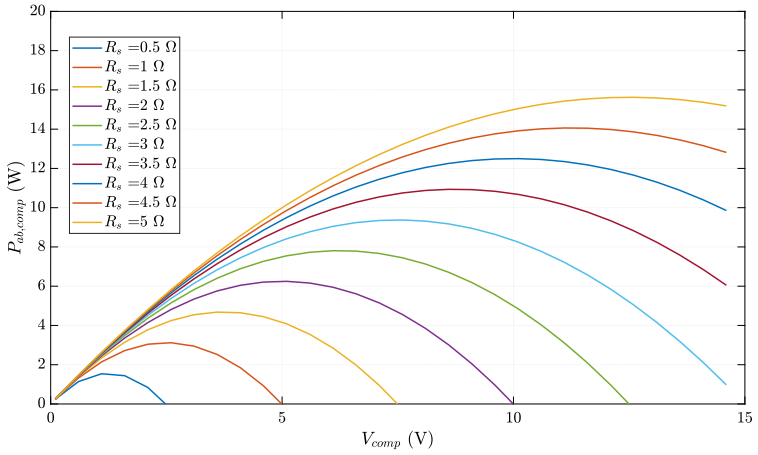

Figure 4.7: Real power at ab terminal v.s. V_{comp} with different R_s.

Thus, the ripple component on the dc-bus is exactly $v_{\text{ab, comp}}$. The dc-side source current then becomes

$$i_{\text{s}} = \frac{V_{\text{S}} - v_{\text{bus}}}{R_s} = \frac{V_{\text{S}} - V_{\text{bus}} - v_{\text{ab, comp}}}{R_s} = I_{\text{dc}} - \frac{v_{\text{ab, comp}}}{R_s} \tag{4.7}$$

Assuming that the majority of the buffer current still flows into the buffer, following the current constraint at the dc-bus voltage in (3.2), the updated buffer current including the loss compensation current is then

$$i_{\text{buf, comp}} = i_{\text{s}} - i_{\text{inv}} = -\frac{v_{\text{ab, comp}}}{R_s} - I_{\text{dc}} \sin(\omega_{2\text{L}} t) \tag{4.8}$$

The average real power for loss compensation into the full-bridge converter within one 120 Hz cycle can be calculated based on the analysis in [3] as

$$P_{\text{ab, comp}} = \frac{\omega_{2\text{L}}}{2\pi} \int_0^{1/120} v_{\text{ab, ref}} i_{\text{buf, comp}} \, dt \tag{4.9}$$

which can be further simplified to

$$P_{\text{ab, comp}} = \frac{V_{\text{comp}}}{2}(I_{\text{dc}} - \frac{V_{\text{comp}}}{R_s}) \tag{4.10}$$

Equation (4.10) can be rearranged as a quadratic equation with variable V_{comp}, whose solution can be found as

$$V_{\text{comp}} = \frac{I_{\text{dc}} R_s - \sqrt{(I_{\text{dc}} R_{\text{S}})^2 - 8 P_{\text{ab, comp}} R_s}}{2} \tag{4.11}$$

(Note that the same equation in [17] was wrong) While it is true that there are two positive roots for this equation, the ripple in reality is the smaller one, which will be explained from

a stability point of view in next section. It can be seen from the above analysis that the loss compensation voltage term will introduce extra voltage ripple on the dc-bus, or extra current ripple in the dc current. Since most single-phase applications have requirements on the minimum ripple ratio of the dc-side current [1], this analysis becomes critical for evaluating the practicality of the SSB. The extra voltage ripple in (4.11) will be used as a metric to calculate an equivalent capacitance on the dc-bus to compare the SSB with other buffer solutions.

4.3 Control Limitations with Small R_s

Available real power for loss compensation

In the ideal case when the dc source impedance is very large, the majority of the ac portion of the inverter current flows into the SSB. However, similar to the discussion in Fig. 2.6, the equivalent ac impedance network of the SSB can be simplified to only include resistive components, as shown in Fig. 4.6. if R_s is small, a large portion of the ripple current will directly flow into the dc source, and the real power available across the SSB branch will be reduced. In steady state, to maintain the desired v_{C2}, the real power drawn from the *ab* terminal $P_{\text{ab, comp}}$ has to equal to the power loss in the converter. In the case with low R_s, there will be chances that the maximum $P_{\text{ab, comp}}$ is still lower than the converter loss, resulting in continuing discharge on v_{C2}. In a numerical example where $I_{\text{dc}} = 5$ A, $P_{\text{ab, comp}}$ is plotted against V_{comp} in Fig. 4.7, under different values of R_s.

As can be seen, with lower R_s, the maximum available power for $P_{\text{ab, comp}}$ decreases. As such, if the converter loss is higher than maximum $P_{\text{ab, comp}}$, v_{C2} cannot be regulated.

Negative feedback region to ensure stability for v_{C2} control

For any value of R_s, the maximum power is achieved when $V_{\text{comp}} = 0.5 I_{\text{dc}} R_s$. Essentially, this is the case when $R_{\text{ab}} = R_s$, and maximum power is transferred. To ensure negative feedback, the value of V_{comp} has to be from zero to $0.5 I_{\text{dc}} R_s$, where the slope of (4.10) is positive. For this reason, the solution of (4.11) has to be the smaller root. For instance, if $V_{\text{C2, dc}}$ in the control diagram in Fig. 4.4 decreases, the error term will drive V_{comp} to be higher. If $V_{\text{comp}} \leq 0.5 I_{\text{dc}} R_s$, more power will be drawn into the buffer to drive $V_{\text{C2, dc}}$ higher so that the negative feedback is ensured. If V_{comp} is in the negative slope region, increasing V_{comp} will actually result in decreasing real power, making the control loop unstable. With smaller R_s, the range of V_{comp} for stable operation is also reduced together with the maximum available power. Moreover, with smaller R_s, if the maximum available power is still lower than the loss in the converter, v_{C2} will keep decaying in the stable region, and the controller will keep driving V_{comp} all the way passing $0.5 I_{\text{dc}} R_s$ and eventually enters the unstable region. For designing the feedback loop, it is also preferred to have slower control on $V_{\text{C2, dc}}$ such that

during transient, V_{comp} does not overshoot to the unstable region. Moreover, with smaller R_s, gains in the feedback loop should also be lower accordingly.

Chapter 5

Multi-Objective Design Optimization of the Series-Stacked Buffer

In this chapter, a methodology that quantifies and formalizes the SSB design process into a multi-objective optimization problem is proposed, from which the Loss-Volume Pareto front can be solved, and optimal control strategy for minimum loss can be determined. Design constraints, modeling of objective functions, and optimization algorithms are discussed. With realistic hardware parameters and constraints, this methodology is applied to the SSB design for a 1.5-kW, 400-V dc-bus single-phase system. The corresponding Pareto front results are studied with hardware prototypes. Compared to previous SSB hardware demonstrations, both power density and efficiency of the designed hardwares are substantially enhanced with the proposed method.

5.1 Motivation for Multi-Objective Design Approach

In ideal lossless operation described in Chapter 3, the SSB has no net energy change in one twice-line frequency cycle. As a result, no active power source is needed and a support capacitor C_2 can instead function as the energy source for the full-bridge. However, in any practical implementation, since the full-bridge converter is lossy, a compensation scheme [3], [14], [16] is needed to regulate v_{C2} by introducing a small voltage ripple on the dc-bus to draw real power into the buffer converter, preventing v_{C2} from decaying. As derived in Section 4.2, the magnitude of the dc-bus voltage ripple introduced by the SSB is positively correlated to the power loss in the full-bridge, which is determined by particular hardware design parameters and control strategies in the SSB. For example, one can design the SSB with smaller C_1 and C_2, which leads to larger voltage swing magnitudes during normal operation. Consequently, the voltage stress in the converter is increased, causing higher switching and inductor loss. Thus, inherently, there exists a tradeoff between passive component volumes and losses in the SSB.

However, in previous optimization work [18] on the SSB, the relations among the power

loss, bus ripple, and passive component size in the SSB have not been quantified and incorporated into the optimization process. Moreover, the single-constraint, single-objective optimization process based on the Lagrange Multiplier method is unable to solve for the optimal SSB hardware designs with multiple optimization objectives, and under multiple real component constraints. The lack of quantitative analysis on the relations among loss, bus ripple and volume also makes it difficult to comprehensively compare the SSB with other optimized active buffer designs [7], [19], [20].

Another limitation of previous optimization work is that the energy utilization ratio of C_2 is not optimized due to conservative design constraints [18][21] and a specific modulation strategy [21]. For a given value of C_1 under a certain load condition, C_2 should satisfy a minimal dc energy storage requirement such that the conversion ratio of the full-bridge is always less than one. Such constraint (3.17) is derived and verified in Section 3.3 [22]. However, in previous hardware demonstrations [3], [4], [21], the stored dc energy on C_2 is much higher than the minimal requirement, resulting from the overly conservative constraint (3.18). Furthermore, since the energy in a capacitor is $\frac{1}{2}CV^2$, there are two specific scenarios of storing excessive energy: either the capacitance of C_2 was oversized for a given dc voltage on C_2, or the dc voltage on C_2 is controlled at a much higher voltage than the lowest voltage defined by the constraint, considering a fixed C_2 capacitance. In the first case, the volume of C_2 is not optimized. In the second case, the loss in the full-bridge is higher than the optimized case due to higher voltage stress. As a result, all previous hardware demonstrations were not on the most optimized Loss-Volume Pareto front.

In this work, we formalize the SSB design process as a multi-objective optimization (MOO) problem under multiple non-linear constraints, which can be solved with numerical analysis tools (Matlab, Python, etc). The over-modulation constraint in Chapter 3 is utilized to obtain the designs with optimal energy utilization ratio, which allows the SSB to be compared with other optimized active buffer topologies on common performance metrics.

5.2 Series-Stacked Buffer Operation Constraints

In this section, the operation of the SSB is discussed, and four critical constraints that relate to component design choices are identified, which are noted as g_1, g_2, g_3 and g_4.

C_1 Voltage Rating Constraint – g_1

As shown in Fig. 3.3, the voltage on C_1 ripples around the dc-bus voltage with the sinusoidal current in (3.3) as

$$v_{\mathrm{C1}} = V_{\mathrm{bus}} + \frac{I_{\mathrm{dc}}}{\omega_{\mathrm{2L}} C_1} \cos(\omega_{\mathrm{2L}} t) \tag{5.1}$$

whose maximum can be found as

$$v_{\mathrm{C1,\,max}} = V_{\mathrm{bus}} + \frac{I_{\mathrm{dc}}}{\omega_{\mathrm{2L}} C_1}. \tag{5.2}$$

This maximum voltage has to be lower than the voltage rating on capacitor C_1. This constraint g_1 is expressed as (5.3) for the optimization problem as

$$g_1 = V_{\text{bus}} + \frac{I_{\text{dc}}}{\omega_{2\text{L}} C_1} - V_{\text{C1, rating}} \leq 0. \tag{5.3}$$

Full-Bridge Voltage Rating Constraint – g_2

The instantaneous voltage on C_2 can be solved by analyzing the power flow through the full-bridge converter in (3.13), where $V_{\text{C2, dc}}$ is the dc value of v_{C2}. This operating parameter is maintained with a feedback loop in practical implementations, and will be discussed in later sections. Correspondingly, the maximum value of v_{C2} can be found as

$$v_{\text{C2, max}} = \sqrt{V_{\text{C2, dc}}^2 + \frac{I_{\text{dc}}^2}{2\omega_{2\text{L}}^2 C_1 C_2}}. \tag{5.4}$$

Parameter $v_{\text{C2, max}}$ is the maximum voltage stress in the full-bridge converter, which should not be higher than the minimum of the voltage rating of capacitor C_2 ($V_{\text{C2, rating}}$) and the switch voltage rating $V_{\text{sw, rating}}$. This constraint g_2 is expressed as

$$g_2 = \sqrt{V_{\text{C2, dc}}^2 + \frac{I_{\text{dc}}^2}{2\omega_{2\text{L}}^2 C_1 C_2}} - min\{V_{\text{C2, rating}}, V_{\text{sw, rating}}\} \leq 0 \tag{5.5}$$

Over-Modulation Constraint – g_3

To ensure that the output voltage from the full bridge converter v_{ab} is generated correctly as in (3.7) to cancel the ripple voltage on v_{C1}, the conversion ratio of the full-bridge converter must not be higher than one. Expression (3.17) can be rewritten as the over-modulation constraint that describes the relation among the capacitance of C_1, C_2, dc voltage level $V_{\text{C2, dc}}$ of v_{C2}, and ideal dc side current I_{dc} as

$$g_3 = \frac{I_{\text{dc}}}{\omega_{2\text{L}}} - C_1 V_{\text{C2, dc}} \sqrt{\frac{2C_2}{2C_2 + C_1}} \leq 0. \tag{5.6}$$

This constraint is referred to as g_3 in the optimization problem.

Inductor Saturation Current Constraint – g_4

The current in the filter inductor L_f in the full-bridge converter should not exceed its saturation current limit. For the full-bridge inverter, the shape of the inductor current is dependent on the types of modulation strategies. The two common fixed-frequency modulation schemes are bipolar and unipolar modulation. Figure. 5.1 compares the gate signals, inductor voltage and current waveforms of these two modulation schemes with the same duty ratio and

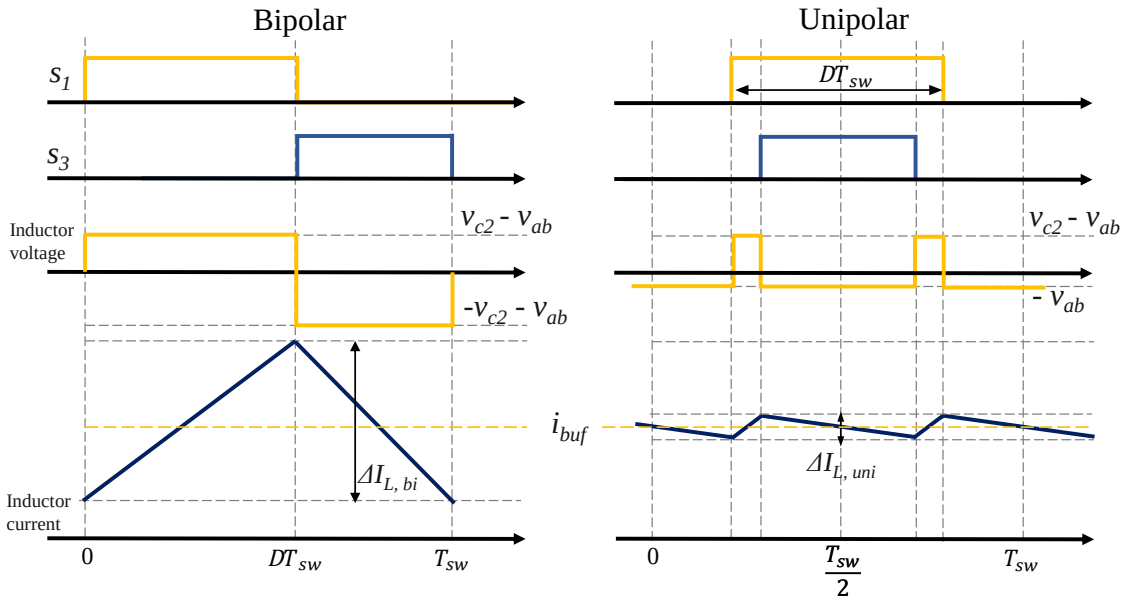

Figure 5.1: Gate signals for S_1 and S_3, inductor voltage and current waveforms of bipolar (left) and unipolar modulation (right) in a full-bridge with identical duty ratio and average inductor current.

average inductor current. If the full-bridge is modulated with bipolar modulation scheme, the inductor peak-to-peak current ripple can be expressed as

$$\Delta I_{\mathrm{L,\,bi}} = \frac{(v_{\mathrm{C2}} - v_{\mathrm{ab}})D}{L_f f_{\mathrm{sw}}} \tag{5.7}$$

where D is the duty ratio of S_1. Since in a full-bridge converter, $v_{\mathrm{ab}} = (2D-1)v_{\mathrm{C2}}$, (5.7) can be rewritten in terms of v_{ab} and v_{C2} as

$$\Delta I_{\mathrm{L,\,bi}} = \frac{(v_{\mathrm{C2}} + v_{\mathrm{ab}})(v_{\mathrm{C2}} - v_{\mathrm{ab}})}{2v_{\mathrm{C2}} L_f f_{\mathrm{sw}}}. \tag{5.8}$$

The maximum inductor current ripple occurs when v_{C2} is at its peak, and v_{ab} is at zero volt, which is expressed as

$$\Delta I_{\mathrm{L,\,bi,\,max}} = \frac{\sqrt{V_{\mathrm{C2,\,dc}}^2 + \frac{I_{\mathrm{dc}}^2}{2\omega_{2\mathrm{L}}^2 C_1 C_2}}}{2L_f f_{\mathrm{sw}}}. \tag{5.9}$$

This moment is also when the average inductor current i_{buf} is at its peak of I_{dc}. Consequently, the peak inductor current I_{peak} in one 120 Hz cycle is then

$$I_{\mathrm{peak,\,120Hz}} = I_{\mathrm{dc}} + \frac{\Delta I_{\mathrm{L,\,bi,\,max}}}{2} \tag{5.10}$$

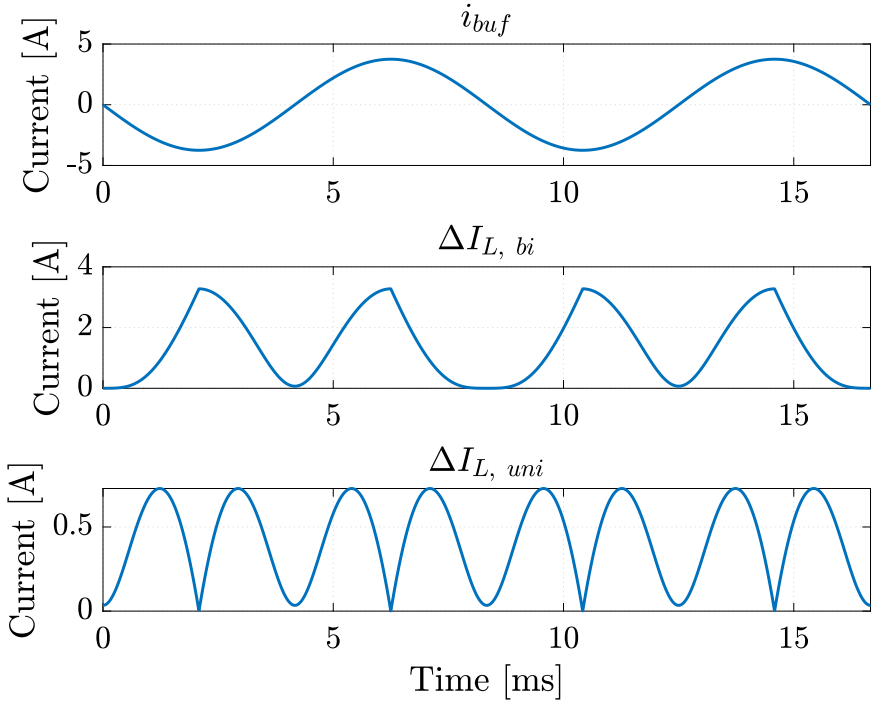

Figure 5.2: Waveforms of i_{buf}, $\Delta I_{\text{L, bi}}$, and $\Delta I_{\text{L, uni}}$ under the condition: $C_1 = 80$ μF, $C_2 = 68$ μF, $V_{\text{bus}} = 400$ V, L_f= 94 μH, 1.5 kW load power.

If the full-bridge is modulated with unipolar scheme, the inductor current ripple is

$$\Delta I_{\text{L, uni}} = \frac{v_{\text{ab}}(v_{\text{C2}} - v_{\text{ab}})}{2v_{\text{C2}}L_f f_{\text{sw}}}. \tag{5.11}$$

Notice that the maximum inductor ripple current and the average inductor current within one 120 Hz cycle do not happen simultaneously as in the bipolar case. Waveforms for i_{buf}, $\Delta I_{\text{L, bi}}$, and $\Delta I_{\text{L, uni}}$ are plotted for comparison in Fig. 5.2. Thus, the peak inductor current in one 120 Hz cycle is not as obvious as in the bipolar case. To find the peak inductor current in one 120 Hz cycle, the peak inductor current of each switching cycle is firstly found as (5.12).

The maximum of (5.12) is the maximum inductor current within one 120 Hz cycle, $I_{\text{peak, 120Hz}}$. However, the explicit solution of the maximum is complicated to derive. To solve the maximum of (5.12) numerically, (5.12) is discretized into an array within one 120 Hz cycle, and the maximum value in the array can be found using numerical analysis tools.

$$
\begin{aligned}
I_{\text{peak, sw}} &= \frac{1}{2}\Delta I_{\text{L, uni}} + i_{\text{buf}} \\
&= \frac{\frac{I_{\text{dc}}}{\omega_{2\text{L}} C_1}\cos(\omega_{2\text{L}} t)\left(\sqrt{V_{\text{C2, dc}}^2 - \frac{I_{\text{dc}}^2}{2\omega_{2\text{L}}^2 C_1 C_2}\cos(2\omega_{2\text{L}} t)} - \frac{I_{\text{dc}}}{\omega_{2\text{L}} C_1}\cos(\omega_{2\text{L}} t)\right)}{4\sqrt{V_{\text{C2, dc}}^2 - \frac{I_{\text{dc}}^2}{2\omega_{2\text{L}}^2 C_1 C_2}\cos(2\omega_{2\text{L}} t)}\, L_f f_{\text{sw}}} - I_{\text{dc}}\sin(\omega_{2\text{L}} t)
\end{aligned}
\tag{5.12}
$$

In both cases of modulation, the peak inductor current within one 120 Hz cycle $I_{\text{peak, 120Hz}}$ has to be lower than the saturation current limit $I_{\text{sat, limit}}$ of the inductor. This constraint g_4 is expressed as

$$g_4 = I_{\text{peak, 120Hz}} - I_{\text{sat, limit}} \leq 0. \tag{5.13}$$

To minimize filter capacitor size and inductor ripple current, unipolar modulation is studied in the optimization and applied to the hardware design.

5.3 Loss and Volume Objective Functions

To study the trade-off between loss and volume of the SSB, a loss function f_{loss} and a volume function f_{volume} are developed.

Loss function – f_{loss}

The loss function of the SSB is developed based on the loss model for full-bridge buck converters. Conduction loss P_{cond}, switching loss P_{sw} and inductor loss P_{L} are included. EPC2033 GaN switch is used in the loss modeling as well as the final hardware implementation. As both C_1 and C_2 are constructed with many individual capacitors in parallel, with correspondingly low equivalent series resistance (ESR), the loss from the capacitors are omitted. It should be noted that accurate loss modeling itself is a subject of research [23]. The objective here is to obtain high level loss models to be used in the optimization. More detailed loss models can be incorporated into the optimization technique as they become available and are validated against hardware.

Conduction loss P_{cond}

During the process to compute the optimization results, it is not guaranteed that the inductor current ripple is negligible in all designs. Thus, the inductor current ripple has to be considered to calculate the RMS current. Considering unipolar modulation, the amplitude of the current ripple varies with the voltage across the inductor within one 120 Hz cycle as expressed in (5.11). The RMS current of each switching cycle is computed, summed and averaged over one 120 Hz cycle. And since two transistors are conducting in both switching

states in one switching cycle in the full bridge converter, the 120 Hz cycle average conduction loss can be calculated as,

$$P_{\text{cond}} = 2R_{\text{ds, on}}(\frac{I_{\text{dc}}^2}{2} + \sum_{n=1}^{f_{\text{sw}}/f_{2\text{L}}} \frac{\Delta I_{\text{L, uni}}(t)^2}{12}\frac{f_{2\text{L}}}{f_{\text{sw}}}), t = \frac{n}{f_{\text{sw}}} \tag{5.14}$$

where $R_{\text{ds,on}}$ is the on-resistance of the transistor, and $f_{2\text{L}} = 120$ Hz. In this work, the EPC2033 GaN device was used in the design, and the dynamic $R_{\text{ds,on}}$ effect [24] has been taken into consideration in the loss model.

Switching loss P_{sw}

In the full-bridge converter, all switches need to block v_{C2} and carry the average inductor current i_{buf}. The overlap switching loss and C_{oss} loss of the GaN transistors are included in the loss model.

Since both v_{C2} and i_{buf} are periodic signals with 120 Hz frequency, in order to calculate the 120 Hz cycle average switching loss P_{sw}, first of all, the energy losses of all switching instants within one 120 Hz cycle are summed up as

$$E_{\text{overlap}} = \sum_{n=1}^{f_{\text{sw}}/f_{2\text{L}}} (v_{\text{c2}}(t)i_{\text{buf}}(t))(t_{\text{on}} + t_{\text{off}}),\ t = \frac{n}{f_{\text{sw}}} \tag{5.15}$$

where t_{on} and t_{off} are the transition times of each turn-on and turn-off switching actions, calculated from the gate charge in the device datasheet and the chosen gate resistance.

As the energy dissipation in the output capacitance C_{oss} of the GaN transistors also changes with v_{C2} for each switching cycle, the total energy loss in C_{oss} in one 120 Hz cycle E_{coss} is obtained in a similar way as the overlap energy loss. Consequently, the average switching power loss in one 120 Hz cycle can be obtained as

$$P_{\text{sw}} = (E_{\text{overlap}} + E_{\text{coss}})f_{2\text{L}}. \tag{5.16}$$

Inductor loss P_{L}

Similarly, as v_{C2}, v_{ab} and i_{buf} change for each switching cycle within one 120 Hz cycle, the core loss, ac loss and dc resistance loss in the inductor also need to be calculated as the 120 Hz cycle average. In this work, the loss model from Vishay [25] is used to obtain the loss from the voltage and current waveforms on the inductor. The model which includes core loss, ac loss, and DCR loss is expressed as

$$\begin{aligned} P_L &= P_{\text{core}} + P_{\text{ac}} + P_{\text{DCR}} \\ &= k_0 {f_e}^{k_f - 1} {B_{pk}}^{k_b} f_0 \times 10^{-14} + k_1 \Delta I^2 \sqrt{f_0} R_{\text{OPER}} + I_{\text{dc}}^2 R_{\text{OPER}}, \end{aligned} \tag{5.17}$$

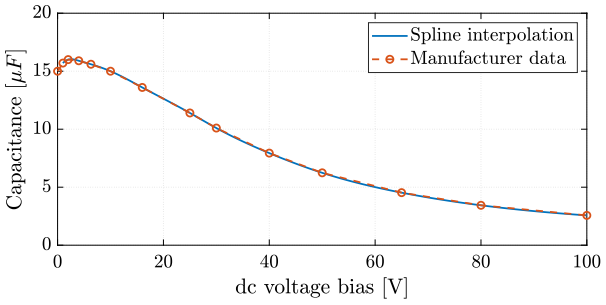

Figure 5.3: Manufacturer's data and spline interpolation for dc voltage bias v.s. Capacitance characteristic for TDK CGA9.

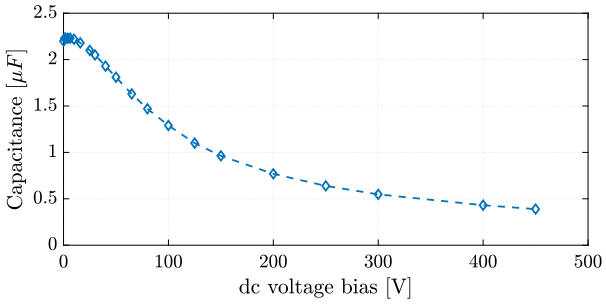

Figure 5.4: Manufacturer's data for dc voltage bias v.s. Capacitance characteristic for TDK C5750

where k_0, k_1, k_b, k_f and R_{OPER} are inductor parameters from the datasheet, f_0 is the switching frequency, B_{pk} is the peak magnetic field, ΔI is the peak-to-peak current ripple, and I_{dc} is the average dc current.

Volume function – f_{volume}

Since capacitor C_1 and C_2 dominate the total volume of the SSB, the volume function is modeled as the total volume of capacitors used for C_1 and C_2. To achieve state-of-the-art power density, X6S and X7S multi-layer ceramic capacitors (MLCC) with high energy density listed in Table 5.1 are chosen for hardware implementation. A suitable number of capacitors are connected in parallel to achieve the desired capacitance values for C_1 and C_2. As the capacitance of X6S and X7S ceramic capacitors decreases as the dc voltage bias increases, the characteristic data from the manufacturer are used to calculate C_2's capacitance as a function of dc voltage bias $V_{\text{C2, dc}}$. As 14 data points on the characteristic curves are provided by the manufacturer, spline interpolation is used to obtain values between the given data points, as shown in Fig. 5.3. For C_1, the capacitance at 400 V is used in the calculation. As discussed in [26], the change in capacitance with dc-bias voltage will distort current through the ceramic capacitors if a large voltage swing is applied. However, in the SSB operation, since both v_{C1} and v_{C2} already have relatively high dc-bias levels compared to their ripple components, the corresponding ranges of voltage swing will not cause too much change in the capacitance. Moreover, as the voltage swings below and above the dc-bias point in one 120 Hz cycle, the average effective capacitance is very close to the value at the dc-bias voltage. Finally, as the manufacturer's characteristic curve of C_1 (TDK C5750) in Fig. 5.4 suggests, above 350 V, the rate of change in capacitance vs. voltage is lower than that at lower voltages. For the above reasons, the non-linearity and distortion effect identified in [26] can be omitted in this work for optimization purposes.

Correspondingly, the number of ceramic capacitors needed and their total volume can be obtained by (5.18), where $\text{Vol}_{\text{C5750}}$ and Vol_{CGA9} are the volumes of individual capacitors as

Table 5.1: Ceramic Capacitors for implementing C_1 and C_2

	Part No.	Voltage rating	Capacitance (@ 0 V dc bias)	Volume
Capacitor for C_1	TDK C5750X6S2W225K250KA (X6S)	466 V	2.2 μF	79.8 mm^3
Capacitor for C_2	TDK CGA9P3X7S2A156M250KB (X7S)	100 V	15 μF	71.3 mm^3

Table 5.2: Constants in the optimization

f_{sw}	L_f	C_f	$I_{\text{sat, limit}}$	$V_{\text{C2, rating}}$	$V_{\text{C1, rating}}$
150 kHz	94 μH	4 μF	8.6 A	100 V	466 V

Table 5.3: Specifications of the inductor used in the design

Part No.	Vishay IHLP6767GZER470M11 × 2
Inductance	47 μH × 2
DCR	40.7 mΩ × 2
Saturation current	8.6 A
Dimensions	(17.15 mm × 17.15 mm × 7 mm) × 2

in Table 5.1.

$$\begin{aligned} f_{\text{volume}} =& \frac{C_1}{C_{\text{C5750, derated}}(V_{\text{bus}})}\text{Vol}_{\text{C5750}} \\ &+ \frac{C_2}{C_{\text{CGA9, derated}}(V_{\text{C2,dc}})}\text{Vol}_{\text{CGA9}}. \end{aligned} \tag{5.18}$$

5.4 Optimization Formulation

As power converter design is a multi-dimensional problem in both variable and objective space, there are certain tradeoffs between high order of dimensions and low order of dimensions for the optimization. For optimization that includes many variables and objectives, while the results are more comprehensive, they often do not provide an intuitive understanding of how a particular variable affects the optimization results, and what are the tradeoffs among certain design variables. For optimization that are constrained to fewer variables, though the results are not as comprehensive and might not capture the most optimized design, the effects of certain variables can be isolated and studied, and tradeoffs can be intuitively understood. The loss-volume, or Efficiency-Power Density Pareto front study is one of the common multi-objective studies to determine tradeoffs and the achievable design space of a power converter [7], [27].

Table 5.4: Upper limits of design vectors in the optimization

Design variables	C_1	C_2	$V_{\mathrm{C2,dc}}$
Limits	500 μF	900 μF	100 V

For this work, the goal is to quantitatively understand a few particular tradeoffs within the SSB design parameters and verify the models and optimization results with hardware, yet we would also like the results to simultaneously be close to the most optimized design. As such, the inductor is chosen to be fixed for the optimization procedure for mainly two reasons: 1) As briefly mentioned in the introduction, the SSB topology allows the use of lower voltage rating devices in the full bridge, operating at high switching frequencies. Moreover, the power processed by the full-bridge converter in the SSB is lower than a full ripple port buffer [7]. As such, the volume of L_f is relatively small compared to the total volume of C_1 and C_2. 2) Since C_1 and C_2 are constructed with many small MLCC capacitors, the relation between the total volume and capacitance can be well defined as a continuous function in (5.18). However, since the volume of an inductor depends on many practical considerations during construction, the relation between the physical volume of the inductor and the inductance are more complicated to model as a single closed-form function. While a simplified first-order model for the inductor volume can be used to study a general trend, the results are unlikely to be directly implemented in actual hardware designs.

Another parameter that is fixed in this optimization is the switching frequency of the full-bridge. As briefly discussed in the introduction, changing the relative size of C_1 and C_2 would change the voltage stress in the full-bridge. Moreover, for the same set of C_1 and C_2, controlling $V_{\mathrm{C2,\,dc}}$ to be at different levels also affects the voltage stress in the converter. To study the variables relevant to the voltage stress, the influence of the switching frequency on the losses has to be isolated from the study. Thus, three parameters: f_{sw}, L_f and C_f are fixed for a relatively conservative current ripple, and their values are presented in Table 5.2 with other component rating limits. The specifications for the inductor used in this design are also listed in Table 5.3. However, it should be noted that both inductor sizing and frequency variations can be incorporated into the general optimization techniques and circuit operating constraints developed in this work, if so desired.

Consequently, both design constraints and objectives are the functions of three variables: C_1, C_2, and $V_{\mathrm{C2,\,dc}}$. Thus, the design variable vector, $\mathbf{x}$, for the optimization is comprised as

$$\mathbf{x} = [C_1, C_2, V_{\mathrm{C2,\,dc}}]. \tag{5.19}$$

To identify the optimal design candidates on the Pareto front, the Weighted Sums method [28] is used. To improve the convergence of the weighted sums method, the design vector $\mathbf{x}$ and objectives (loss and volume) are normalized. The design variables are linearly scaled from zero to one. The physical limits of the design variables are presented in Table 5.4. Both objectives are normalized about their optimized objective values to bring the order of

both objectives near one. This is a common technique to improve the numerical stability of the optimization procedure. The loss objective function is normalized by the highest loss result $F_{\text{loss, max}}$. To obtain this value, the following single-objective non-linear programming optimization problem is solved with Matlab `fmincon()` function to find the design with the smallest volume and highest loss as

$$\begin{aligned} \min_{\mathbf{x}} \quad & f_{\text{volume}}(\mathbf{x}) \\ s.t. \quad & g_i(\mathbf{x}) \leq 0 \quad \forall i = 1, .., 4. \end{aligned} \tag{5.20}$$

Similarly, the volume objective function is normalized by the largest volume result $F_{\text{volume, max}}$, which is obtained by solving for the design with lowest loss and largest volume as

$$\begin{aligned} \min_{\mathbf{x}} \quad & f_{\text{loss}}(\mathbf{x}) \\ s.t. \quad & g_i(\mathbf{x}) \leq 0 \quad \forall i = 1, .., 4. \end{aligned} \tag{5.21}$$

The normalized loss-volume optimization problem can be then formalized as

$$\begin{aligned} \min_{\mathbf{x}} \quad & \alpha \cdot \frac{f_{\text{loss}}(\mathbf{x})}{F_{\text{loss, max}}} + (1-\alpha) \cdot \frac{f_{\text{volume}}(\mathbf{x})}{F_{\text{volume, max}}} \\ s.t. \quad & g_i(\mathbf{x}) \leq 0 \quad \forall i = 1, .., 4. \end{aligned} \tag{5.22}$$

where α is the weighting parameter in the Weighted Sums method. The Pareto front is generated by incrementally varying the weighting parameter α, from 0 to 1 between each optimization procedure. The previously solved two design cases with $F_{\text{volume, max}}$ and $F_{\text{loss, max}}$ are located at the two ends on the Pareto front. Intermediate values of α will result in designs that lie on a curve between these two anchor points, as shown in Fig. 5.5. The number of increments in α is the number of design points on the final Pareto front. For each value of α, the optimization problem in (5.22) is solved to convergence using the interior point algorithm in Matlab `fmincon()` function. To summarize and visualize the proposed methodology for modeling and optimization, a flow chart is developed as shown in Fig. 5.6. As illustrated in Fig. 5.6, there are three inputs to formulate a MMO problem: objective functions, design constraints and design variables. The component characteristics and control strategies are linked to the optimization formulation with the loss, volume functions of individual components, voltage and/or current ratings, and design variables to optimize.

5.5 Optimization Results

By sweeping α from 0 to 1 with $\frac{1}{30}$ increment, a Loss-Volume Pareto front for 1.5 kW, 400 V dc-bus SSB designs are generated with Matlab in Fig. 5.7. The purposes of this section are to interpret the Pareto front results to help understand the design process, discuss design trade-offs and establish comparison metrics with other buffer solutions.

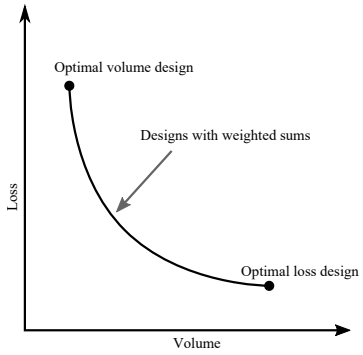

Figure 5.5: Pareto front example. The curve illustrates the trade-off between the loss and the volume within achievable design space.

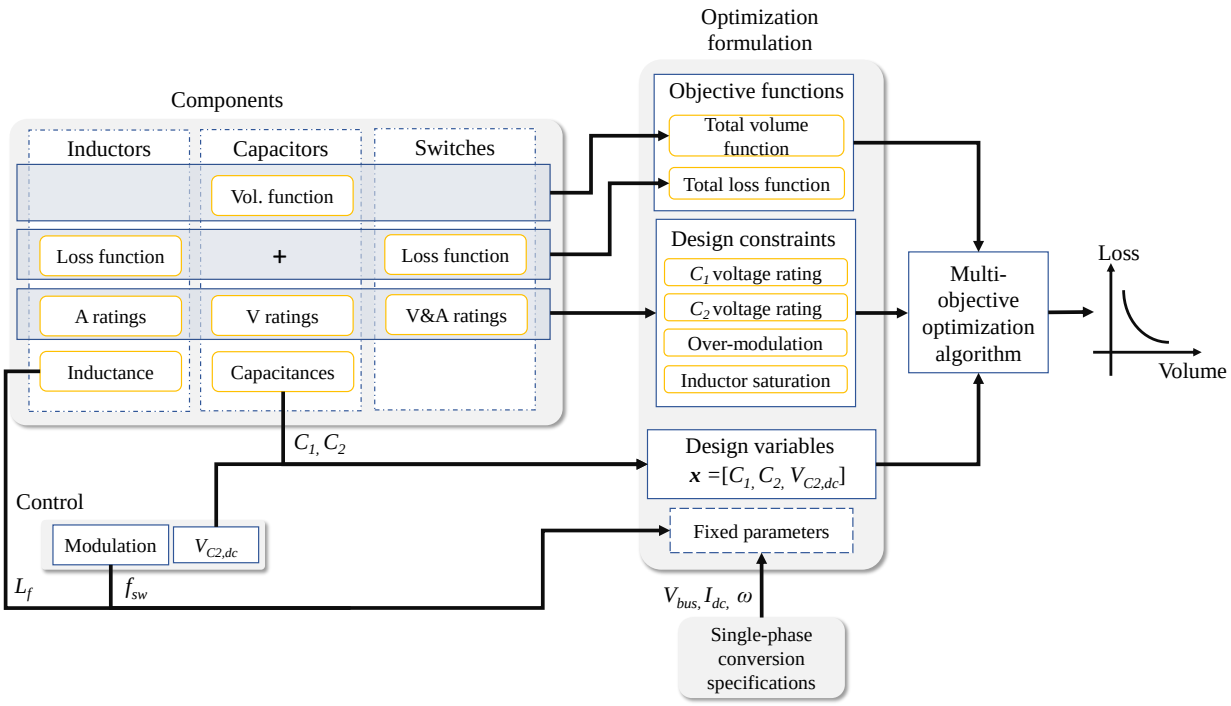

Figure 5.6: Design flow chart for the proposed optimization methodology.

Volume composition

The compositions of the total volume for all design choices on the Pareto front are plotted in Fig. 5.8. As can be seen, the volume of C_1 dominates the total volume for all designs due to lower capacitance density at 400 V. With α starting at zero, C_1 is minimized to the capacitance with the highest voltage ripple allowed by constraint g_1, and C_2 is minimized to the capacitance that corresponds to the highest voltage ripple allowed by either constraint g_2 or g_4. For the specific inductor and switching frequency considered here, the peak voltage on C_2 is constrained by g_2 with the capacitor voltage rating. As α starts to increase from zero, C_1 remains at the minimum capacitance, and C_2 is increased to lower the peak voltage stress in the full-bridge. As α further increases, it becomes more important to lower the loss in the objective function, with subsequent increases of C_1 with α. With $\alpha = 1$, the design is bounded by the upper limits in Table 5.4.

Compared to the previous SSB design in [3], the percentage of C_2's volume in the total volume is much reduced. Fundamentally, the proposed optimization scheme is able to identify the minimal required energy storage on C_2 under the four design constraints to improve the energy utilization ratio, whereas the design in [3] oversized C_2 with conservative design constraints [22]. A detailed comparison to previous work with hardware results is performed in Section V.

Loss composition

The compositions of the losses for all design choices on the Pareto front are plotted in Fig. 5.9. As can be observed, for the single-phase conversion scenario considered and the choices of components in this study, the switching loss and inductor loss are the two major loss mechanisms compared to the conduction loss. Both switching loss and inductor loss are heavily related to the voltage stress in the full-bridge converter, which is decided by $V_{\mathrm{C2,\,dc}}$. The corresponding $V_{\mathrm{C2,\,dc}}$ for each design is plotted with the loss composition. As discussed in the volume composition subsection, the design with the highest loss and lowest volume is bounded by the design constraint g_1 or g_2. Yet, the design with the lowest loss is bounded by the upper limits of design variables in Table. 5.4.

Note that the optimized $V_{\mathrm{C2,\,dc}}$ values in Fig. 5.9 are for the operation at 1.5 kW. To minimize the loss for any load for a given design of C_1 and C_2, $V_{\mathrm{C2,\,dc}}$ should be scaled with the load current, or the magnitude of the voltage ripple on C_1: $\Delta v_{\mathrm{C1,\,max}}$, as shown in the control scheme in Fig. 4.4. The scalar k between $\Delta v_{\mathrm{C1,\,max}}$ and $V_{\mathrm{C2,\,dc}}$ can be determined with the over-modulation design constraint g_3. By rewriting g_3, the constraint for the scalar k is given as

$$k = \frac{V_{\mathrm{C2,\,dc}}}{\Delta v_{\mathrm{C1,\,max}}} \geq \sqrt{\frac{2C_2 + C_1}{2C_2}}. \tag{5.23}$$

As can be seen, the constraint for k is only related to the relation between the capacitance of C_1 and C_2. And to minimize the loss in the converter, k should be set to be as close as possible to the lower bound for lowest voltage stress. Though in previous work [3], $V_{\mathrm{C2,\,dc}}$ was

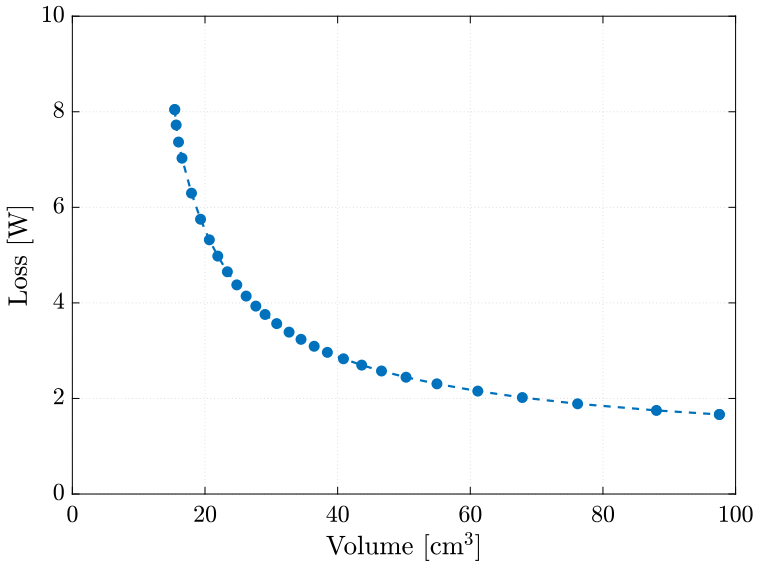

Figure 5.7: Generated Loss-Volume Pareto front curve.

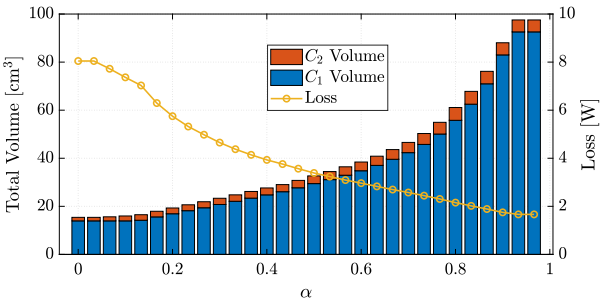

Figure 5.8: Generated optimized volume of C_1 and C_2 for all design choices on the Pareto front, plotted with corresponding total loss for each α increments.

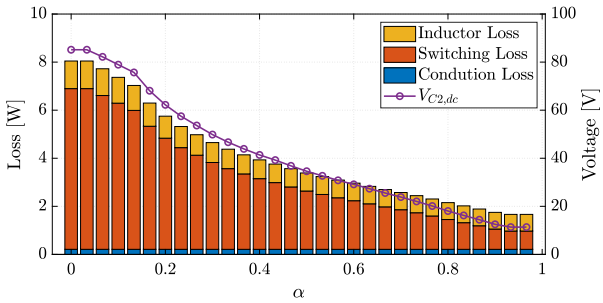

Figure 5.9: Generated loss breakdown for all design choices on the Pareto front, plotted with corresponding $V_{\mathrm{C2,\,dc}}$ for each α increments.

also scaled with the load current, the scaler was empirically determined, which was higher than the quantitative limit in (5.23). As a result, the loss was not optimized in the hardware prototype across the full load range.

Dc-bus voltage ripple analysis

Since the full-bridge converter is lossy, a compensation scheme [3], [16] is needed to regulate v_{C2} by introducing a small voltage ripple $v_{\mathrm{ab,\,comp}}$ across terminal ab. This voltage ripple is in-phase with the buffer current i_{buf} to draw real power into the buffer converter, preventing

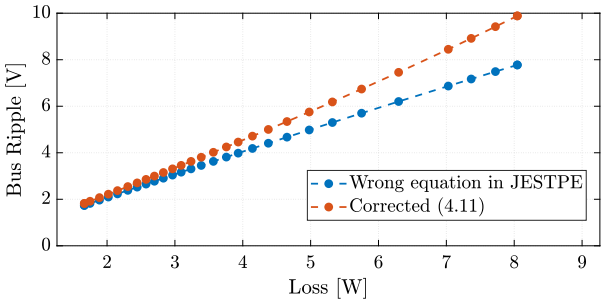

Figure 5.10: Calculated compensation ripple $\Delta v_{\text{bus, pk-pk}}$ vs. loss in the SSB P_{loss}, for all design choices on the Pareto-front. Source resistance $R_s = 10\ \Omega$. Note that the wrong result in [17] is compared with the correct equation (4.11).

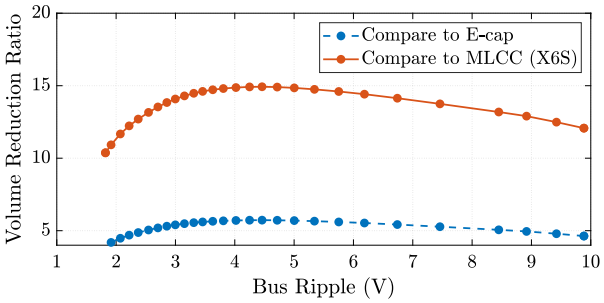

Figure 5.11: Volume reduction ratio of the SSB compared to passive capacitor bank solutions vs. bus ripple.

v_{C2} from decaying. This scheme is noted as *Loss compensation for* C_2 in Fig. 4.4. Since ideally the voltage ripple on C_1 is canceled perfectly, the voltage ripple on the dc-bus is exactly $v_{\text{ab, comp}}$. (4.11) can be used to calculate the peak-to-peak dc-bus voltage ripple as in (5.24).

$$\Delta v_{\text{bus, pk-pk}} = I_{\text{dc}} R_{\text{S}} - \sqrt{(I_{\text{dc}} R_{\text{S}})^2 - 8 P_{\text{loss}} R_{\text{S}}}. \tag{5.24}$$

With an example source resistance $R_{\text{S}} = 10\ \Omega$, the corresponding $\Delta v_{\text{bus, pk-pk}}$ for each design choice on the Pareto front in Fig. 5.7 can be calculated based on their losses, and plotted in Fig. 5.10.

In practical applications, the input current ripple or the dc-bus voltage ripple have to remain below certain limits. For example, the Google Little Box challenge requires the input current ripple ratio to be lower than 20% [1], which corresponds to 1 A ripple current limit. Thus, an upper bound of the loss in the SSB can be calculated from (5.24). Graphically, it is a horizontal line that represents a loss value in Fig. 5.7, and any design points on the Pareto front that are located above this line should not be considered for implementation. Alternatively, the current ripple limit can also be incorporated into the MOO problem as one of the design constraints such that the all calculated optimization results satisfy the ripple requirement.

Equivalent capacitance analysis

To compare the size of the SSB to the conventional electrolytic capacitor bank solution, the equivalent capacitance for an ideal electrolytic capacitor bank (i.e., without ESR) can be computed from $\Delta v_{\text{bus, pk-pk}}$. As the electrolytic capacitor bank buffers the pulsating power

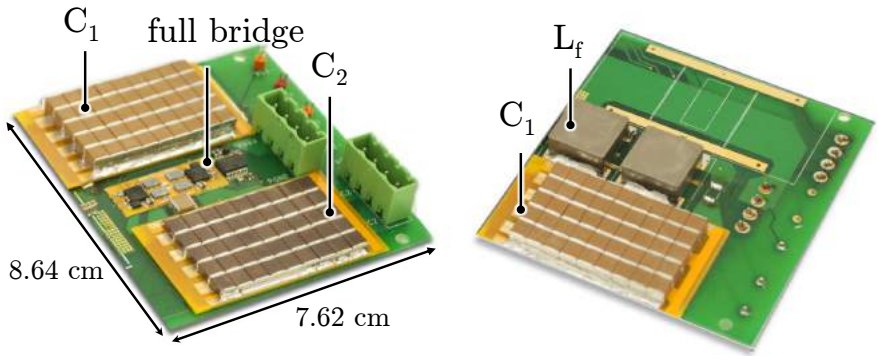

Figure 5.12: Photos (top and bottom) of the 1.5 kW SSB hardware test bed. The capacitors are soldered on the yellow daughter boards for the ease of adjustment during testing.

at twice the line frequency, the relation between the bus ripple $\Delta v_{\text{bus, pk-pk}}$ and the required capacitance is given as

$$C_{\text{buf}} = \frac{I_{\text{dc}}}{\omega_{\text{line}} \Delta v_{\text{bus, pk-pk}}}. \tag{5.25}$$

We benchmark the capacitance density (capacitance per volume) of Nichicon UCP2W121 MHD6 to calculate the corresponding physical volume of the required electrolytic capacitor as

$$\text{Vol}_{\text{E-cap}} = \frac{C_{\text{buf}}}{\rho_{\text{E-cap}}} \tag{5.26}$$

where $\rho_{\text{E-cap}} = 14\ \mu\text{F/cm}^3$ for Nichicon UCP2W121MHD6.

If multi-layer ceramic capacitors (MLCC) are used to construct the passive buffer, the capacitance density of TDK C5750X6S at 400 V ($\rho_{\text{MLCC}} = 5.4\ \mu\text{F/cm}^3$) is used to calculate the physical volume of the total capacitors needed Vol_{MLCC}.

Once the required $\text{Vol}_{\text{E-cap}}$ and Vol_{MLCC} are obtained from corresponding bus voltage ripples, the volume reduction ratio of each SSB design on the Pareto-front compared to passive capacitor bank solutions can be plotted in Fig. 5.11. As can be observed, within the plotted bus ripple range, the SSB can achieve more than five times reduction on capacitor volume compare to conventional electrolytic capacitor bank solutions.

5.6 Hardware Verification

In order to verify the calculated Loss-Volume trade-off, a SSB hardware test bed has been developed as shown in Fig. 5.12. The ceramic capacitors are soldered on separate daughter boards to test combinations of C_1 and C_2 at different locations on the Pareto front. Three hardware prototype with different parameters as listed in Table 5.5 are built and experimentally verified, with all efficiency measurements obtained using Yokogawa WT3000 power

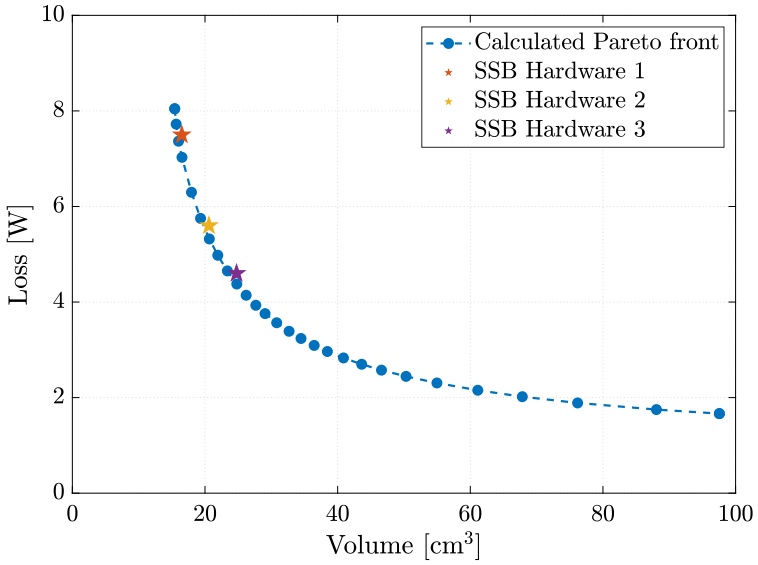

Figure 5.13: Measured loss and component volume of three hardware configurations, plotted with the calculated Loss-Volume Pareto-front curve

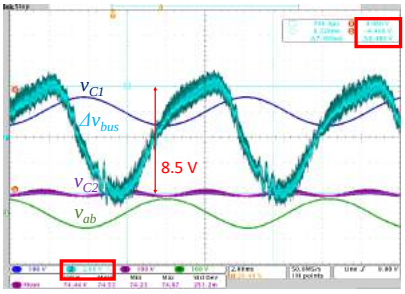

Figure 5.14: 1.5 kW, 400 V dc-bus operation waveform of the SSB hardware prototype 1. Bus voltage is ac-coupled to show the ripple component.

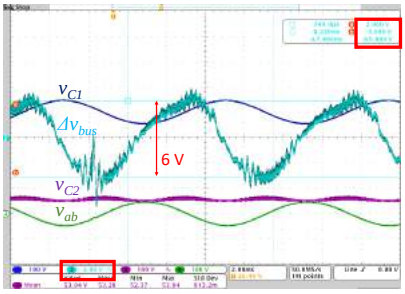

Figure 5.15: 1.5 kW, 400 V dc-bus operation waveform of the SSB hardware prototype 2. Bus voltage is ac-coupled to show the ripple component.

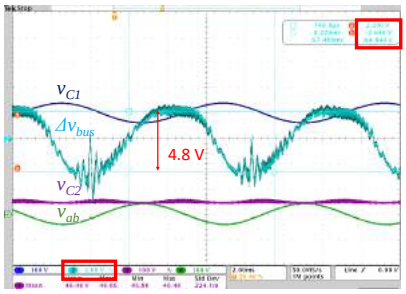

Figure 5.16: 1.5 kW, 400 V dc-bus operation waveform of the SSB hardware prototype 3. Bus voltage is ac-coupled to show the ripple component.

Table 5.5: Design parameters for three tested hardwares in this work

	Hardware 1	Hardware 2	Hardware 3
No. of capacitors for C_1 (volume)	180 (14.36 cm^3)	225 (17.96 cm^3)	270 (21.55 cm^3)
Equivalent large-signal capacitance for C_1 @ 400 V	77.4 μF	96.8 μF	116.1 μF
No. of capacitors for C_2 (volume)	30 (2.14 cm^3)	37 (2.64 cm^3)	45 (3.21 cm^3)
Equivalent large-signal capacitance for C_2 @ $V_{C2,\,dc}$	107.2 μF	217.3 μF	315.4 μF
$V_{C2,\,dc}$ at 1.5 kW	74 V	54 V	46 V
Power density by component volume (C_1,C_2,L_f)	72.8 W/cm^3	60.7 W/cm^3	52.0 W/cm^3
2-port efficiency @ 1.5 kW	99.50%	99.63%	99.69%

Table 5.6: Calculated and measured ripple comparison

Hardware No.	1	2	3
Measured loss at 1.5 kW (W)	7.5	5.6	4.6
Calculated bus ripple from loss (V)	9.1	6.5	5.3
Measured bus ripple (V)	8.5	6.0	4.8
Dc bus voltage ripple ratio	2.1%	1.5%	1.2%
Dc current ripple ratio	22%	16%	13%

Table 5.7: Design parameters of previous hardware demonstration

	Hardware in [3], [11]	Hardware in [4], [14]	Hardware in [29]
Rated dc-side power	2 kW	500 W	750 W
Dc-bus voltage	400 V	200 V	200 V
Line Frequency	60 Hz	50 Hz	60 Hz
C_1 volume (types)	19.1 cm^3 (MLCC X6S)	86.3 cm^3 (Film)	86.3 cm^3 (film)
Equivalent large-signal capacitance for C_1 @ 400 V	100 μF	100 μF	100 μF
C_2 volume (types)	9 cm^3 (MLCC X7S)	9 cm^3 (E-cap)	10.85 cm^3 (E-cap)
Equivalent large-signal capacitance for C_2 @ $V_{C2,\,dc}$	430 μF	470 μF	440 μF
$V_{C2,\,dc}$ at full load	81 V	60 V	60 V
L_f volume (specs)	4.1 cm^3 (94 μH, 8.6 A)	34.3 cm^3 (100 μH, 3 A)	3.3 cm^3 (44 μH, 6.1 A)
Power density by component volume (C_1,C_2,L_f)	62.1 W/cm^3	3.85 W/cm^3	7.47 W/cm^3
2-port efficiency @ full load	99.3%	Not Reported	Not Reported

meters with high precision. The volume and measured power loss at 1.5 kW of each hardware prototype is plotted along with the calculated Pareto front in Fig. 5.13. As can be seen, the measured losses are very close to the calculated values for each design, and demonstrate similar loss-volume trade-off trends as the generated Pareto-front design sets, which verifies the practicability of the developed loss and volume models, as well as the optimization process.

The operation waveforms of the three tested hardware prototypes at 1.5 kW are given in Fig. 5.14, Fig. 5.15, and Fig. 5.16, for hardware 1, 2, and 3 respectively. The dc-bus voltage is ac-coupled on the oscilloscope to measure the peak-to-peak ripple voltage. As expected,

hardware 1 introduced the largest peak-to-peak bus ripple of 8.5 V, with the highest loss. Hardware 2 and 3 introduced bus ripple voltage of 6 V and 4.8 V respectively.Note that the low frequency noise in Fig. 5.14, Fig. 5.15, and Fig. 5.16 were caused by wire parasitic inductance during the zero-crossing of v_{ab}. Extra wires were used to connect different capacitor boards to vary the capacitor counts for 3 hardware prototypes. From (5.24), a corresponding bus ripple voltage can be calculated from the measured loss. However, the calculated ripple from the measured loss and the actual measured bus ripple might have some discrepancies as shown in Table 5.6. This slight deviation can be caused by errors in the ADC and sensing circuits in the controller and/or measurement errors in the power meter. Moreover, the source resistance R_s can also vary with temperatures during testing.

The efficiency of the SSB can be defined in several ways [3], [21]. As the SSB is usually connected at the dc-bus, it is cascaded between the dc source and the inverter (or PFC and the load for ac-dc), the 2-port efficiency is more convenient in terms of calculating efficiencies within a system with multiple stages of converters. In the dc-ac case, the 2-port efficiency is defined as

$$\eta = 1 - \frac{P_{\text{loss}}}{P_{\text{dc}}} \tag{5.27}$$

where P_{dc} is the average dc power ($V_{\text{bus}} I_{\text{dc}}$).

The 2-port efficiencies at 1.5 kW for three hardware prototypes are also listed in Table 5.5. For hardware 1 and 3, the 2-port efficiencies across the full load range are also plotted for comparison in Fig. 5.17. Thanks to the control scheme in Fig. 4.4 to control $V_{\text{C2, dc}}$ to the lowest possible level for every load point, the efficiencies remain very high even at light load conditions for both hardware designs.

To demonstrate that the proposed method has optimized the energy utilization of the capacitors, Table 5.7 lists previous hardware demonstrations for comparison. For hardware in [3], as the exact same types of capacitors for C_1 and C_2 are used in the design, the volume composition can be directly compared. Comparing hardware 1 in this work with the SSB in [3], the percentage of C_2's volume in the total capacitor volume decreases from 32% to only 13%, resulting in 17% increase in power density and slight improvement in efficiency due to more optimized $V_{\text{C2,dc}}$ control. While [4], [21], [29] use different types of capacitors in the design such that the volume cannot be fairly compared, it can be readily observed that the capacitance of C_2 is much larger than C_1 in both hardware demonstrations, which is the result of using conservative operating constraint. A quantitative metric to fairly compare the energy utilization of C_2 is the maximum conversion ratio of the full-bridge in (3.16), which should be close to one to fully utilize C_2's energy. The maximum conversion ratio can be calculated from C_1, C_2 and $V_{\text{C2, dc}}$ values provided in the literatures using (3.16), which is 0.85 for [3], 0.68 for [4], [21], and 0.82 for [29]. Whereas for both the computed Pareto designs and the tested hardware prototype 1, 2 and 3 in this work, the maximum conversion ratios are all approximately one.

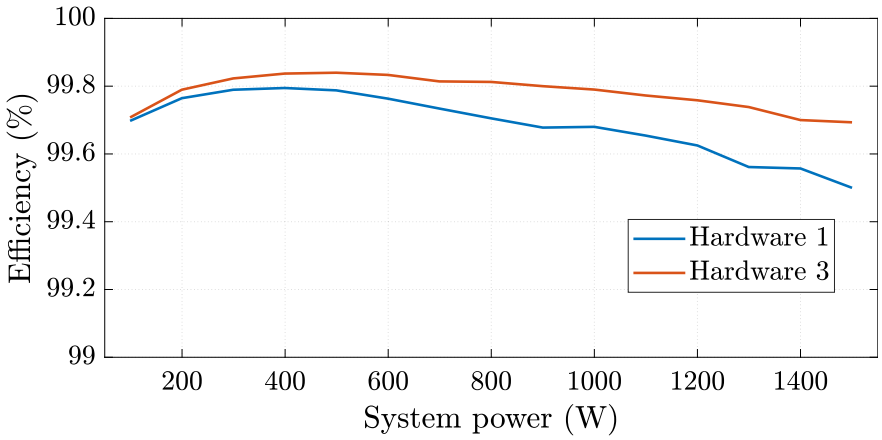

Figure 5.17: Efficiencies of hardware 1 and 3 across the full load range.

Table 5.8: Inductors for comparison

Part No.	Inductance	I_{sat}	DCR	Volume
IHLP6767	47 μH	8.6 A	0.04 Ω	2.06 cm^3
IHLP4040	47 μH	4.5 A	0.17 Ω	0.47 cm^3
IHLP5050	15 μH	14.5 A	0.03 Ω	1.14 cm^3

5.7 Generalized Design Process

So far, the optimization is constrained for a given inductor with fixed-frequency modulation. In this way, the loss and volume tradeoff caused by the relation among C_1, C_2 and $V_{\text{C2, dc}}$ can be studied in detail and independently from other variables. Moreover, the optimization results are directly applied to real hardware designs and verified with experiments. However, the framework of the proposed optimization methodology can also be generalized for more comprehensive optimizations, as shown in Fig. 5.18. Compared to the design process in Fig. 5.6, both f_{sw} and L_{f} are set as design variables instead of fixed parameters. The volumes, losses and V&A ratings of capacitors, inductors and switches are all considered in the model.

It should be noted that volume functions for both capacitors and inductors are preferred to be continuous in this generalized design process to improve the numerical stability for the optimization procedure. For instance, a general capacitance/inductance (per volume) density can be used to estimate the needed volumes[9]. Yet, the results might not be as practical, unless the degree of freedom in the actual capacitor and inductor design and manufacturing is high [30]–[32].

If a large component database is linked to the procedure, to optimize the buffer for specific inductors or capacitors, corresponding capacitance or inductance should be set to

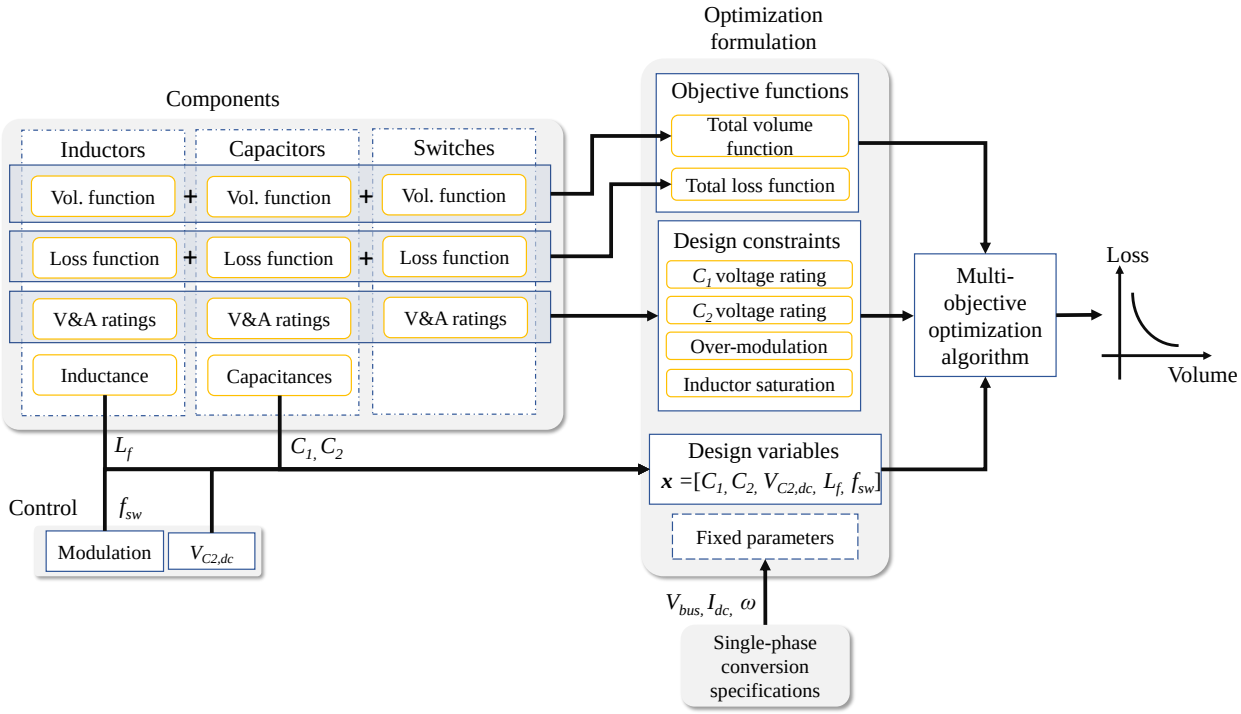

Figure 5.18: Design flow chart with generalized optimization methodology.

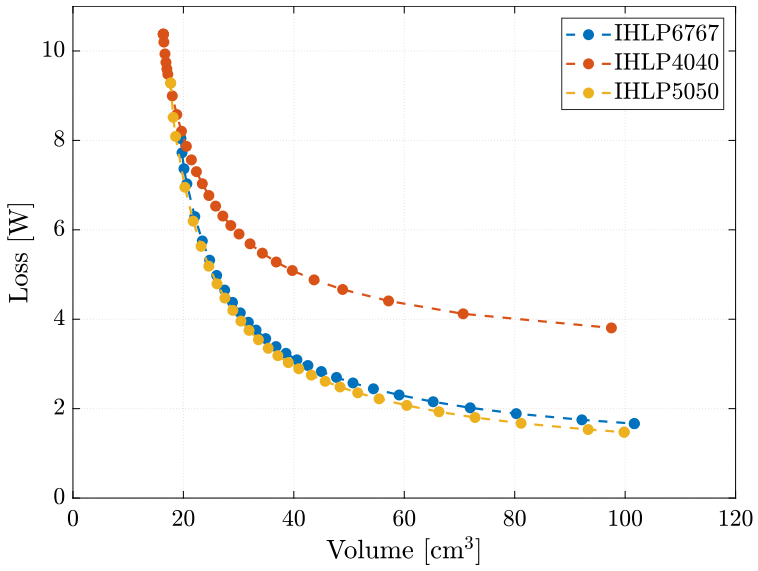

Figure 5.19: Calculated Pareto Front with three different inductors.

fixed parameters, and V&A ratings should also be updated accordingly. The optimization process then has to be repeated for all combinations of components, and multiple loss-volume tradeoff curves will be generated to determine the final Pareto front. For example, two other inductors listed in Table. 5.8 have been selected to compare with the optimization result in Fig. 5.7 obtained with the Vishay IHLP6767 inductor. The volume of the inductors are added to the total volume function. The result of such optimization are shown in Fig. 5.19.

The algorithm to solve the multi-objective optimization (MOO) problem is not limited to Weighted Sums method. Different methods to solve continuous nonlinear MOO problem can be applied, depending on the types of information provided for setting up the problem [28].

To further expand the scopes of the optimization, reliability and cost objective functions [21] can also be adopted in the optimization procedure for cost-effective and reliability-oriented analysis. The volume of the heatsink can be modeled from the loss and switch volume and added to the total volume function to optimize the overall electro-thermal system solution [33].

Behavior during load transient events can also be incorporated. In general, more energy stored in the capacitors will provide higher margin to handle transient events [7]. While the exact voltage and current waveforms also depend on the rest of the system, the total stored energy in C_1 and C_2 can be studied as an objective function to indicate the buffer's ability to handle transient events.

5.8 Conclusion

A methodology to optimize the loss and volume of the SSB is proposed. With updated operating constraint, the energy utilization of the energy buffering capacitors are optimized. The performance of the SSB hardware prototypes designed based on the Pareto front matches the calculated optimal results, which further verifies the effectiveness of the proposed models and optimization process. The Pareto front and the optimized hardware prototypes have identified large space for improvement in both power density and efficiency compared to previous SSB hardware prototypes. Furthermore, the proposed methodology provides a framework to link component properties to the operating constraints and the objective functions, which can be generalized to involve more design variables and objectives for the optimization.

Chapter 6

High Power Density Full Ac-dc System Implementations with the SSB

High efficiency and high power density single-phase ac-dc Power Factor Correction (PFC) converters and dc-ac inverters are desirable in many applications such as data center power delivery and electric vehicle on-board chargers. In conventional boost converter based designs, two of the major limitations to achieve high power density are the size of the filter inductor of the boost converter (or buck in the inverter mode) and the twice-line frequency energy buffering capacitor bank. In this chapter, two high power density single-phase converters with similar architectures of FCML as the PFC/inverter stage and SSB as the energy buffer stage are presented and discussed. The unique challenges in both hardware and digital controller designs to achieve the co-operation of PFC, FCMLs and SSB are addressed, and corresponding solutions are presented in detail.

6.1 Proposed Coupled Control for the SSB in PFC and Inverter Applications

While the SSB control method with a band-pass filter and a differentiator in Fig. 4.4 has been verified with hardware in both this work and [16], the voltage and current relations defined by the impedance model in Fig. 4.2 can be used to design a more efficient control method for using the SSB with PFC or inverter, if critical system information such as phase, frequency and power can be utilized.

Coupling SSB Control with a Boost PFC Controller

In this section, the SSB is connected at the dc output of a boost PFC (Since the proposed control is compatible with conventional 2-level boost and FCML boost converters, the boost

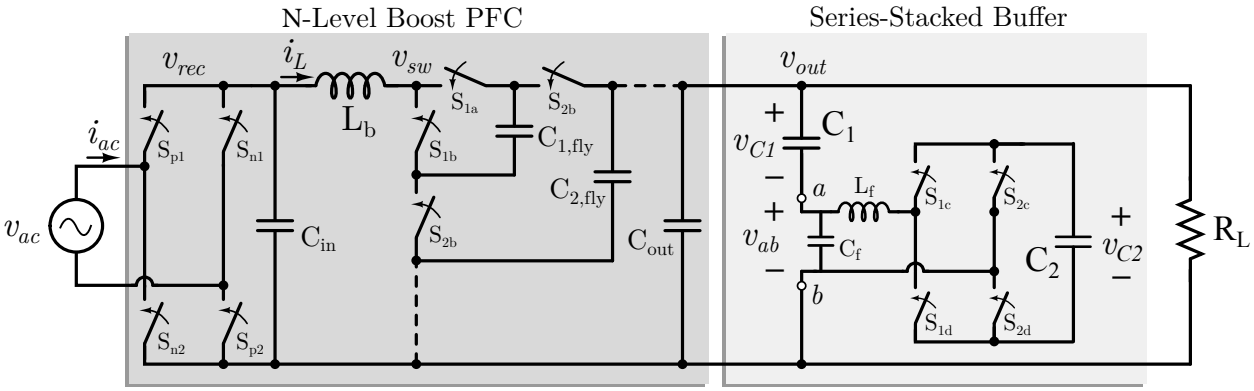

Figure 6.1: Block diagram of the PFC and SSB system.

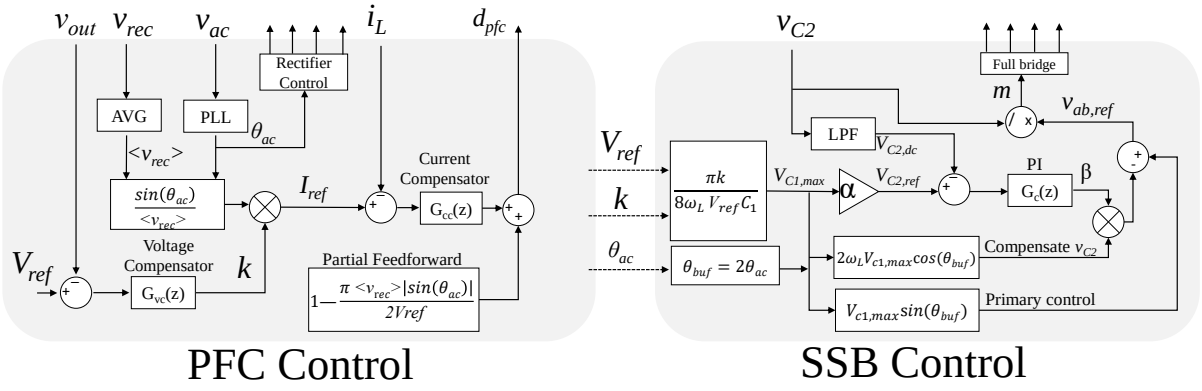

Figure 6.2: Control diagram for the PFC and SSB.

converter stage is generalized as a N-level converter, N = 2,3,4...), as shown in Fig. 6.1. Assuming an ideal control on the PFC side, the ac voltage and current are in phase. As a result, the internal voltage and current relation of the SSB is the same as in the inverter case in Fig. 3.1, yet only the power flow in the system is in the opposite direction.

PFC control

The control block diagram for the boost PFC is shown on the left of Fig. 4.4. A PFC control scheme for boost converter operating in continuous conduction mode (CCM), similar to the classical multi-loop control [34], [35] is analyzed in this example.

An inner current loop regulates the inductor current i_L to follow a desired current reference i_{ref} generated in phase with v_{rec}. To precisely match the phase of the input current to the input voltage and reject disturbance due to measurement noise, a phase-locked loop (PLL) based on a digital notch filter [36] is adopted in this design. For controlling high

power-density FCML converters, due to the small filter inductor in the FCML boost converter, the disturbance from the input voltage on the current is more significant than in conventional two-level boost converters with large filter inductors, which leads to problems such as current phase leading at line frequency. For this reason, a partial voltage feedforward control term is also included to offset such disturbance [37], [38].

The outer voltage loop regulates the output voltage to the desired dc value (i.e., 400 V) by scaling the magnitude of the input current. As shown in Fig. 6.2, the output voltage loop provides a multiplying factor k to the current loop reference. This control loop is usually designed to have very low bandwidth such that the current reference with in one line cycle is not distorted (($\leq$ 30Hz)). From the impedance plot in Fig. 4.5, it should be noted that Z_{C1} is the dominating impedance in low frequency range ($\leq$ 30), which should be used to design the PI compensator.

SSB Control

In ac-dc PFC applications, if the input ac voltage $v_{\mathrm{ac}} = V_{\mathrm{ac}} \sin(\omega_{\mathrm{L}} t)$ and input current $i_{\mathrm{ac}} = I_{\mathrm{ac}} \sin(\omega_{\mathrm{L}} t)$ (where $\omega_{\mathrm{L}} = 2\pi\times$ 60 rad/s, for the US line frequency considered here) are controlled to be in phase by the PFC controller, the instantaneous input ac power is expressed as

$$p_{\mathrm{in}} = v_{\mathrm{ac}} i_{\mathrm{ac}} = \frac{V_{\mathrm{ac}} I_{\mathrm{ac}}}{2}(1 - \cos(2\omega_{\mathrm{L}} t)) = P_0(1 - \cos(2\omega_{\mathrm{L}} t)). \tag{6.1}$$

The instantaneous power processed by the SSB is purely reactive, i.e., $p_{\mathrm{buf}} = -P_0 \cos(2\omega t)$, where P_0 is the rated output power. Assuming negligible ripple on V_{out}, the current flowing into the SSB can be derived as

$$i_{\mathrm{buf}} = \frac{p_{\mathrm{buf}}}{V_{\mathrm{out}}} = \frac{-P_0}{V_{\mathrm{out}}} \cos(2\omega_{\mathrm{L}} t). \tag{6.2}$$

With similar derivation in Chapter 3, the expression for v_{ab} is then

$$v_{\mathrm{ab}} = -\Delta v_{\mathrm{C1}} = \frac{P_0}{2\omega_{\mathrm{L}} V_{\mathrm{out}} C_1} \sin(2\omega_{\mathrm{L}} t). \tag{6.3}$$

As discussed in Chapter 4 and 5, to ensure correct operation, the SSB controller must fulfill two major functions: generating correct voltage to cancel the 120 Hz ripple on C_1 (annotated as "primary control" in Fig. 4.4) and drawing real power into the converter to regulate the dc voltage of v_{C2} (annotated as "compensate v_{C2}" in Fig. 4.4). In Chapter 4, these two functions are realized with a band-pass filter and a differentiator in the controller [3], [16]. However, in the PFC controller, there is already a significant computational burden from the PLL and the dual-loop PFC control. Adding another two digital filters will further lengthen the computation time. Moreover, the differentiator have to be designed with sufficient bandwidth ($\geq$ 120 Hz) so that it can capture the twice-line frequency signal. As a result, it is not able to reject the low frequency ($\approx$10 Hz) disturbance from the voltage

control loop of the PFC. To solve these issues, the proposed control scheme utilizes three terms from the PFC controller – dc output reference voltage V_{ref}, voltage loop multiplying factor k, and angle of the input voltage θ_{ac} from the PFC PLL's output, to minimize the disturbance from the dc bus voltage.

Primary control path

If the input voltage is defined as $v_{\text{ac}} = V_{\text{ac}} \sin(\omega_{\text{L}} t) = V_{\text{ac}} \sin(\theta_{\text{ac}})$, the relation between the angle of v_{ab} (defined as θ_{buf}) and θ_{ac} can be determined from (6.3) as

$$\theta_{\text{buf}} = 2\omega_{\text{L}} t = 2\theta_{\text{ac}}. \tag{6.4}$$

Equation (3.7) also indicates that the magnitude of Δv_{C1} (defined as $\Delta V_{\text{C1, max}}$) varies with the power level P_0, which means that if there is access to any variable that reflects the power level in the PFC controller, the correct buffer voltage can be computed. In the PFC controller, the voltage-loop factor k determines the magnitude of the input current reference I_{ref}, which determines the power in the system. In an universal ac input PFC controller as in Fig. 4.4, the relation between k and I_{ref} is

$$I_{\text{ref}} = \frac{|\sin(\theta_{\text{ac}})|}{< v_{\text{rec}} >} k = I_{\text{ac}} |\sin(\theta_{\text{ac}})| \tag{6.5}$$

where $< v_{\text{rec}} >$ is the 120 Hz cycle average of the rectified input voltage. The relation between the magnitude of the input ac voltage V_{ac} and $< v_{\text{rec}} >$ is

$$< v_{\text{rec}} >= \frac{2V_{\text{ac}}}{\pi}. \tag{6.6}$$

From (6.5) and (6.6), the relation between scaler k and rated output power P_0 can be derived as

$$k = I_{\text{ac}} < v_{\text{rec}} >= I_{\text{ac}} \frac{2V_{\text{ac}}}{\pi} = \frac{4P_0}{\pi} \tag{6.7}$$

which can be used to calculate $\Delta V_{\text{C1, max}}$ as

$$\Delta V_{\text{C1, max}} = \frac{\pi k}{8\omega_{\text{L}} V_{\text{ref}} C_1}. \tag{6.8}$$

Once the relative phase and magnitude of the primary v_{ab} are obtained, a clean 120 Hz voltage reference signal can be generated with the built-in trigonometric *sine* Look-up Table (LUT) functions of the micro-controller (such as Texas Instrument C2000 DSP (digital signal processor)) as

$$v_{\text{ab,pri}} = \frac{\pi k}{8\omega V_{\text{ref}} C_1} \sin(2\omega_{\text{L}} t). \tag{6.9}$$

v_{C2} loss compensation control path

As discussed in previous chapters, to draw real power into the SSB to compensate for the loss in the converter, a voltage term that is in-phase with the buffer current i_{buf} is needed. With the phase relation showing in Fig. 4.3 , the voltage term to maintain V_{C2} can then be implemented with the *cosine* LUT functions in the MCU

$$v_{\text{ab, comp}} = -V_{\text{comp}} \cos(2\omega_{\text{L}} t). \tag{6.10}$$

Comparison to previous voltage control methods

Compared to the band-pass filter in the control schemes in Chapter 4 [3], [4], [14], [16], the use of the LUT guarantees that only the 120 Hz component and no other harmonics is included in the generated v_{ab}. The derivative term for loss compensation does not need to be calculated from a digital differentiator as in [16]. Instead, it is generated with the LUT *cosine* function. The use of LUT for both primary and loss compensation enables faster computation than the digital band-pass filters and differentiator. The buffer waveforms using the coupled control and the band-pass filter based control are shown in Fig. 6.3 and Fig. 6.4. As can be seen, the coupled SSB control generated much cleaner v_{ab} without a low frequency noise profile and regulated v_{C2} much closer to the desired value compared to the old band-pass filter based control

Moreover, the voltage controlled scheme in [4], [14], [16] has to measure v_{ab}, which requires differential measurement with extra amplifiers, voltage divider and passive filter network. The proposed control scheme only needs to measure v_{C2}, which greatly simplifies sensing circuitry and reduces measurement noise. As a result, in practical software implementation in the micro-controller, the proposed control method greatly reduces the execution time of the control subroutine, compared to computing the digital filters and the differentiator in [4], [14], [16], which allows the potential to operate the converter with higher frequency and implement more safety and start-up control functions if desired.

6.2 Design and Implementation of a 1.5 kW Universal Input PFC

This section presents the design and implementation of a 1.5 kW universal ac (95 to 265 V_{ac}) input, 400 V_{dc} output PFC converter for data center power delivery application with a flying capacitor multilevel (FCML) boost front-end and a SSB.

Hardware Prototype

A hardware prototype with the proposed architecture and control is designed and implemented on one main power board, as annotated in Fig. 6.5. The boost PFC stage is a

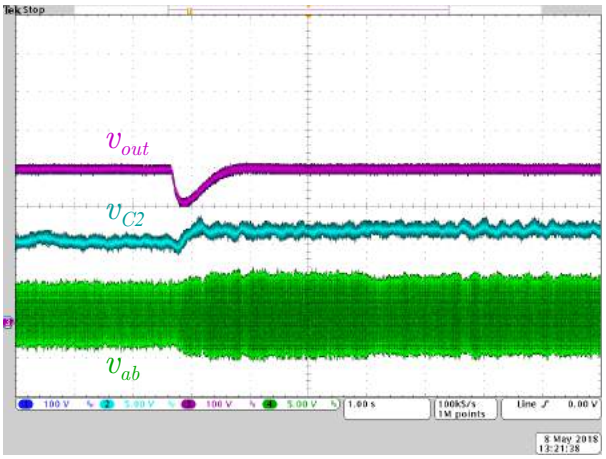

Figure 6.3: Experimental waveforms of PFC dc output voltage, v_{out}, v_{C2}, and buffer converter output voltage, v_{ab} during a slight load step (100 W to 150 W) implementing the band-pass fitler based SSB control methods.

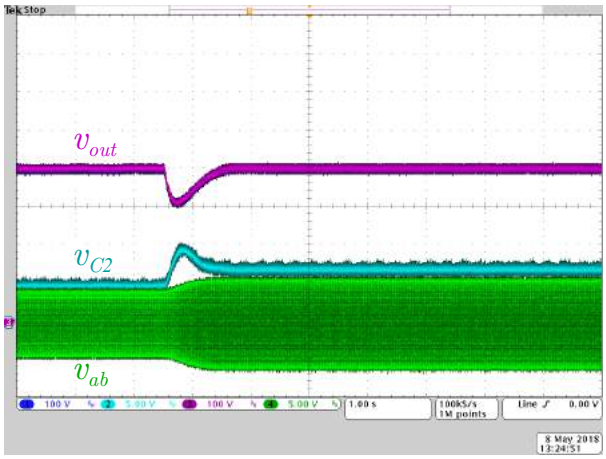

Figure 6.4: Experimental waveforms of PFC dc output voltage, v_{out}, v_{C2}, and buffer converter output voltage, v_{ab} during a slight load step (100 W to 150 W) implementing the coupled SSB control methods.

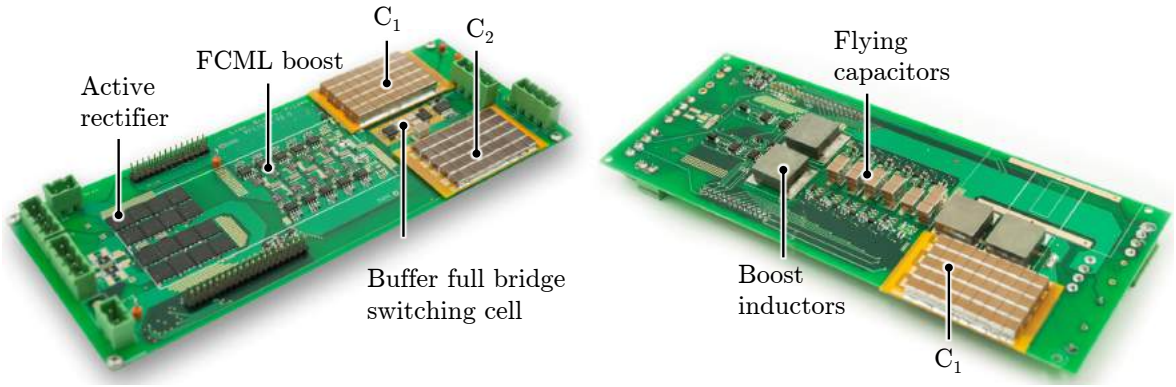

Figure 6.5: Converter photos with key components annotated.

six-level FCML boost. For the 400 V dc-bus considered here, each switch needs to block 80 V ($\frac{V_{\text{out}}}{5}$), so 100 V rated GaN FETs are used. Detailed operation and component sizing of the FCML have been discussed in many literature [9], [11], [39]. Chapter 9 of this thesis will also discuss the operation and modulation of the FCMLs.

The full bridge in the SSB is implemented on a separate PCB switching cell and soldered onto the main power board. Such switching cell design facilitates manufacturing, repairing and debugging process [11]. Moreover, the micro-controller is stacked on top of the power

Table 6.1: Component Listing of the Hardware Prototype

Function block	Component	Mfr. & Part number	Parameters
6-level FCML	GaN FETs	GaN Systems GS61004T	100 V, 15 mΩ
	Single flying capacitor	TDK C5750X6S2W225K250KA × 6	450 V, 2.2 μF
	Inductors (L)	Vishay IHLP6767GZER220M01 × 2	23 A, 22 μH
Series Stacked Buffer	GaN FETs	EPC 2033	150 V, 7 mΩ
	Capacitor C_1	TDK C5750X6S2W225K250KA × 180	450 V, 2.2 μF (0.431 μF @ 400 V)
	Capacitor C_2	TDK CGA9P3X7S2A156M250KB × 45	100 V, 15 μF (3.44 μF @ 80 V)
	Inductor	Vishay IHLP6767GZER470M11 × 2	8.6 A, 47 μH
Active rectifier	MOSFETs	STMicroelectronics STL57N65M5 × 4	650 V, 61 mΩ

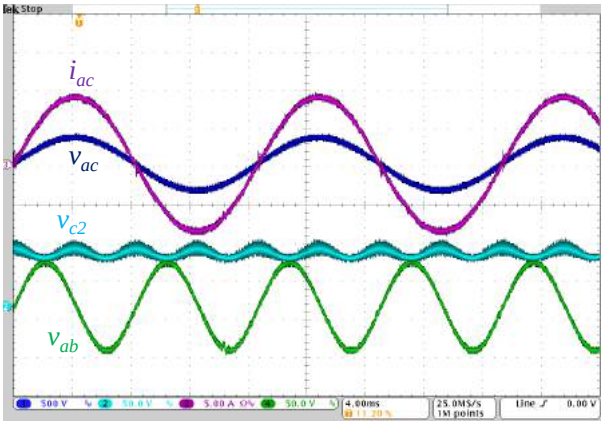

Figure 6.6: Experimental waveforms of input voltage v_{ac}, input current i_{ac}, C_2 voltage v_{c2} and buffer converter output voltage v_{ab}. 240 V_{ac} to 400 V_{dc}, 1.5 kW load.

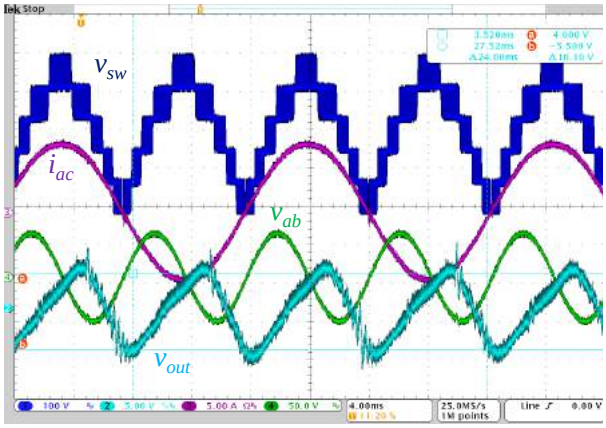

Figure 6.7: Experimental waveforms of output dc voltage v_{out}, input current i_{ac}, switching node voltage v_{sw}, buffer converter output voltage v_{ab}. The output dc bus voltage is ac-coupled to show the ripple component. 240 V_{ac} to 400 V_{dc}, 1.5 kW load.

board. Key components with their parameters are listed in Table. 6.1.

Experimental Verification

The converter was tested with 240 V_{ac} input up to 1.5 kW, and 120 V_{ac} input up to 600 W (due to the current limit of the ac supply). Figure 6.6 and Fig. 6.7 show the operation at 1.5 kW, 240 Vac, and Fig. 6.8 and Fig. 6.9 show the operation at 600 W, 120 Vac. As can be seen in both test conditions, the input voltage and current are well in-phase, and the switching node voltage indicates good balancing among flying capacitors. Specifically, compared to the switch node waveforms of the 7-level FCML at full power in [11], [38], the staircase waveform is much more uniformed without obvious voltage band caused by the

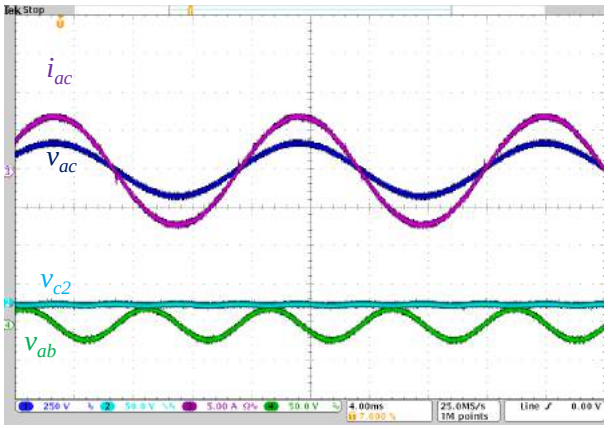

Figure 6.8: Experimental waveforms of input voltage v_{ac}, input current i_{ac}, C_2 voltage v_{c2} and buffer converter output voltage v_{ab}. 120 $\mathrm{V_{ac}}$ to 400 $\mathrm{V_{dc}}$, 600 W load.

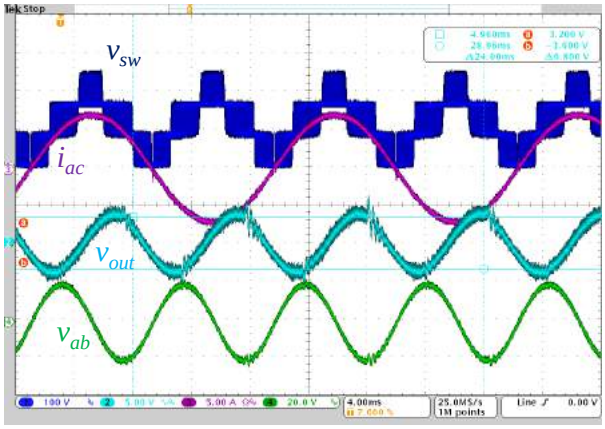

Figure 6.9: Experimental waveforms of output dc voltage v_{out}, input current i_{ac}, switching node voltage v_{sw}, buffer converter output voltage v_{ab}. The output dc bus voltage is ac-coupled to show the ripple component. 120 $\mathrm{V_{ac}}$ to 400 $\mathrm{V_{dc}}$, 600 W load.

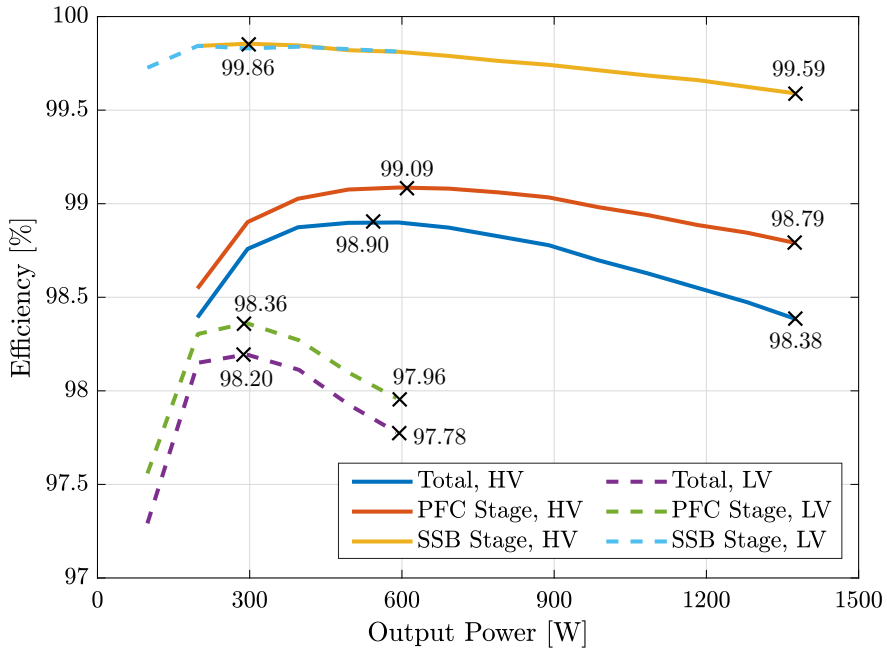

Figure 6.10: Efficiency measurement with 240 $\mathrm{V_{ac}}$ (HV) and 120 $\mathrm{V_{ac}}$ (LV) inputs. Total system efficiency, PFC efficiency and SSB efficiency are plotted.

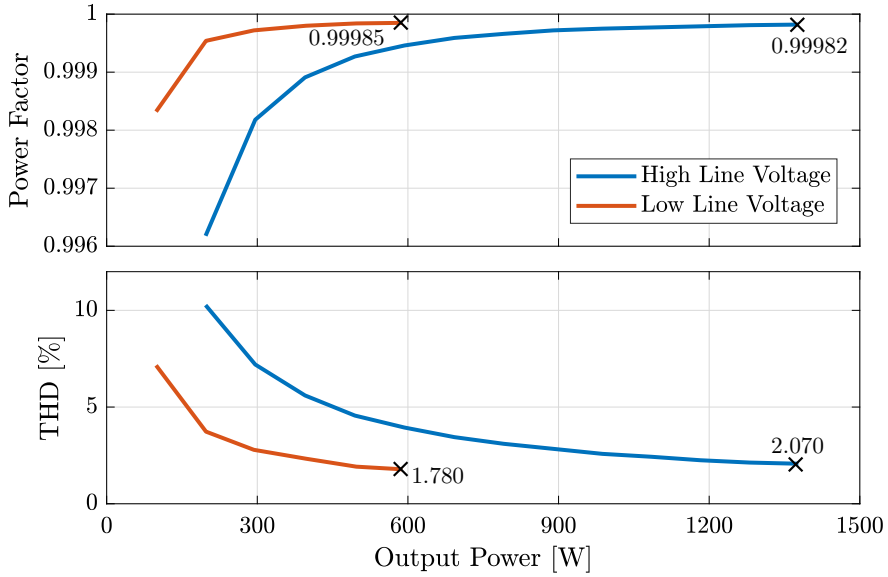

Figure 6.11: Power factor and THD measurement for 240 Vac and 120 Vac input.

imbalance among flying capacitor voltages. For the SSB, v_{C2} is regulated with steady dc levels. Moreover, as the dc output voltage is ac-coupled in Fig. 6.7 and Fig. 6.9 to show the ripple component, it can also be observed that the proposed system control scheme is able to determine the correct phase and magnitude of v_{ab} to cancel the large ripple on C_1. The remaining small bus voltage ripple is introduced by the loss compensation term, as the bus ripple and v_{ab} are 90° out of phase. As shown in Fig. 6.7, at 1.5 kW, the peak-to-peak ripple is 10.1 V, which is 2.5% of the bus voltage.

Loss and power factor data are recorded with digital power analyzers Yokogawa WT3000E. Overall loss and buffer loss are measured, and corresponding loss in the PFC stage can then be calculated. The individual efficiencies of the FCML PFC stage and the SSB are illustrated in Fig. 6.10 for both 240 V_{ac} and 120 V_{ac} input. At 240 V_{ac} input, the PFC stage reaches a peak efficiency of 99.1%, and the SSB alone is able to achieve an efficiency of above 99.5% across the full load range, thanks to the partial power processing characteristic and variable minimal $V_{C2,dc}$ control. Consequently, the peak total system efficiency is 98.9%, and at 1.4 kW, the efficiency is at 98.4%.

The power factor is above 0.996 for all tested loads, owing to the partial feedforward control. The Total Harmonic Distortion (THD) data for both high line and low line is collected with digital power analyzer Keysight PA2201, and they are well below the regulation limits. Power factor and THD for both high and low line are plotted in Fig. 6.11.

Conclusion

The proposed PFC architecture with FCML boost front-end and SSB can greatly reduce the passive component volume compared to conventional solutions. Thanks to the improved design and control techniques implemented in this design, the FCML boost front-end reaches a power density of 490 W/in^3, and the SSB reaches a power density of 567 W/in^3 by box volume. The system is also able to achieve excellent performance in THD, power factor and dc-bus ripple. Moreover, we have also demonstrated that the proposed system control scheme can be implemented in an efficient way with a single DSP micro-controller.

6.3 Design and Implementation of a 6 kW on-board EV Charger

Single-phase on-board electric vehicle (EV) chargers convert grid ac voltage to dc voltage to charge the high-voltage battery pack in the EV. High efficiency and high power density single-phase ac-dc converters are desirable in such applications to reduce the heat loss, volume and weight of these chargers. Moreover, the capability of bidirectional conversion is preferred for potential vehicle-to-grid applications. This section presents the system architecture and embedded digital control implementation of a 7 kW, universal ac (120-240 V_{AC}) to 400 V_{DC} single-phase ac-dc bidirectional converter. The converter features an interleaved 6-level flying capacitor multilevel (FCML) ac-dc stage and a series-stacked buffer for buffering twice-line frequency pulsating power to achieve high efficiency and power density.

System Architecture and Operation

The overall system schematic drawing is shown in Fig. 6.12. From the ac side to the dc side, it consists of an active rectifier, an ac-dc (bi-directional) conversion stage with 2-phase interleaved 6-level FCML converters, and a series-stacked buffer (SSB) across the dc bus. The overall control diagram for both PFC and SSB is shown in Fig. 6.13. Compared to the 1.5 kW PFC in last section, the only difference is the interleaved PFC current control. The inductor current of each phase is regulated independently to ensure equal current sharing between the two phases. Moerover, the control for open-loop inverter mode is shown in Fig. 6.14.

SSB control in the inverter mode

In the inverter mode, the dc load is replaced with a dc-source, and the ac source is replaced with a resistor as shown in Fig. 6.12. For simplicity, the ac load considered in this work is resistive and the FCML inverter runs open-loop voltage control with the rectified sinusoidal duty ratio:

$$d_{\text{inv}} = m|\sin(\omega_L t)|, \tag{6.11}$$

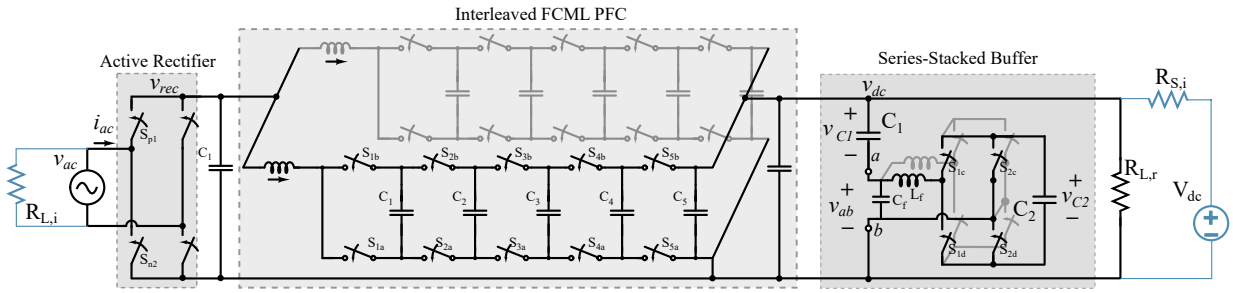

Figure 6.12: Schematic of the overall system with active rectifier (unfolder), interleaved FCML, and series-stacked buffer. The dc source and load are shown in blue.

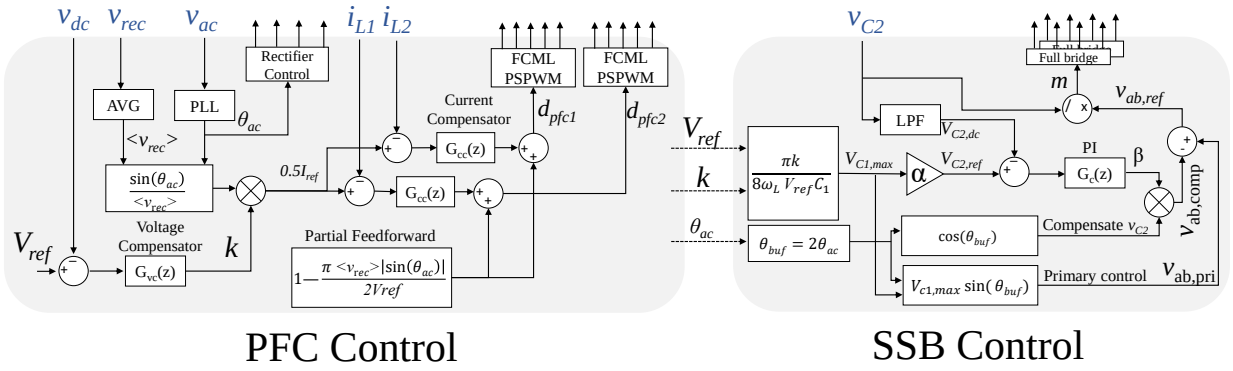

Figure 6.13: Overall control system of the interleaved PFC and SSB in rectifier mode. The sensed parameters are in blue font.

where m is the modulation depth (0 to 1) determining the peak ac voltage $V_{\text{ac}} = mV_{\text{dc}}$. The angle $\theta_{ac} = \omega_L t$ is passed to the rectifier/unfolder control to create a full sine wave.

Instead of sensing the inverter current to generate a current reference for the SSB as in [3], the same inductor current sensors in the PFC mode are used to calculate the system power such that the voltage-based control scheme in [40], [41] can be applied. Note that the inductor current direction is reversed compared to the PFC mode, which means the current sensing circuitry should be able to measure bi-directional current. In the actual hardware implementation, the current amplifier LT1999 with 1.5-V dc bias at zero current is used.

The load ac current of the two FCML phases are measured and averaged with moving-average filter at 120 Hz. If the peak ac current is I_{ac}, the 120 Hz average value is $\frac{2I_{\text{ac}}}{\pi}$. As shown in (6.3), the magnitude of v_{ab} can be calculated with the dc power level. In this case, the averaged ac current is used to calculate the load dc power as

$$P_{\text{dc}} = V_{\text{dc}} I_{\text{dc}} = \frac{V_{\text{ac}} I_{\text{ac}}}{2} = \frac{mV_{\text{dc}} I_{\text{ac, avg}} \pi}{4}. \tag{6.12}$$

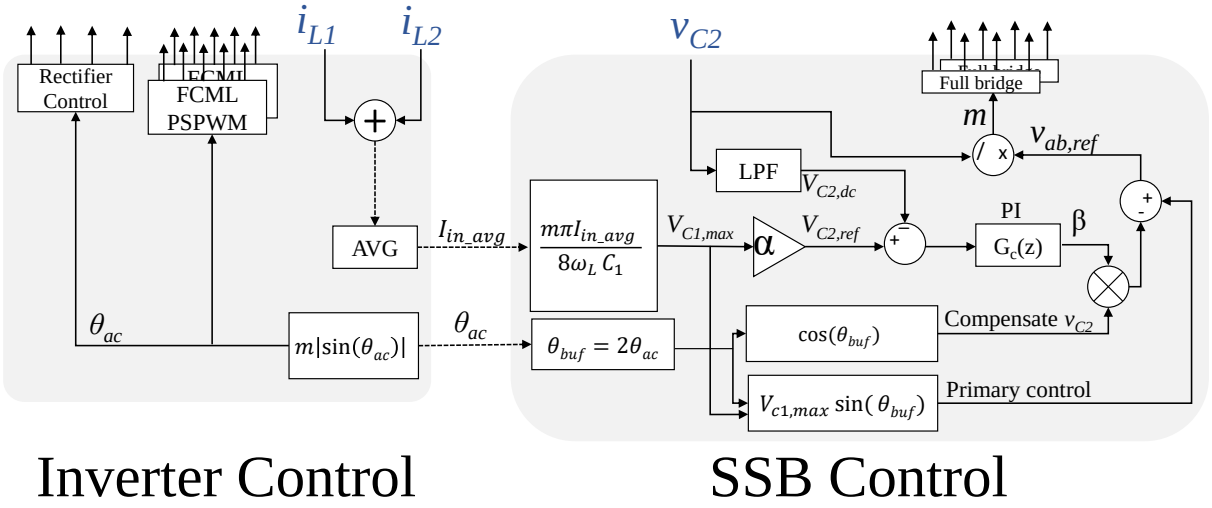

Figure 6.14: Overall control system in open-loop inverter mode.

The new expression for the SSB controller to generate the correct v_{ab} can thus be simplified to:

$$v_{\text{ab, inv}} = \frac{P_{\text{dc}}}{2\omega_L V_{dc} C_1}\sin(2\omega_L t) = \frac{m\pi I_{\text{ac, avg}}}{8\omega_L C_1}\sin(2\omega_L t). \tag{6.13}$$

Once the magnitude of v_{ab} is determined, the remainder of the SSB control is identical to the PFC mode.

Sensing average inductor current in FCML

In both PFC and inverter mode, the average inductor current in the FCMLs needs to be sampled accurately. Moreover, the inductor current of the two FCMLs need to be sampled separately such that they can be regulated independently to prevent unequal current sharing between the two phases.

In [41], [42], the inductor current is sensed with a shunt resistor in the ground return path to lower the common-mode voltage stress for the corresponding current amplifier. or an implementation employing a single FCML, the input inductor current does indeed equal the ground return current so that such placement of the shunt resistor is feasible. However, for two interleaved converters, while the total input inductor current equals the total return current, the individual inductor current of each phase cannot be obtained by sensing the individual ground return current. To sense the inductor current of each phase, the shunt resistors are placed between the source of the lowest switches and return ground, as in Fig. 6.15. In this configuration, the shunt resistors are directly sensing the current of the lowest switches $S_{1,1}$ and $S_{2,1}$, which will be equal to the inductor current only when $S_{1,1}$ and $S_{2,1}$ are on. Moreover, a unity-gain buffer is added between the current amplifier and

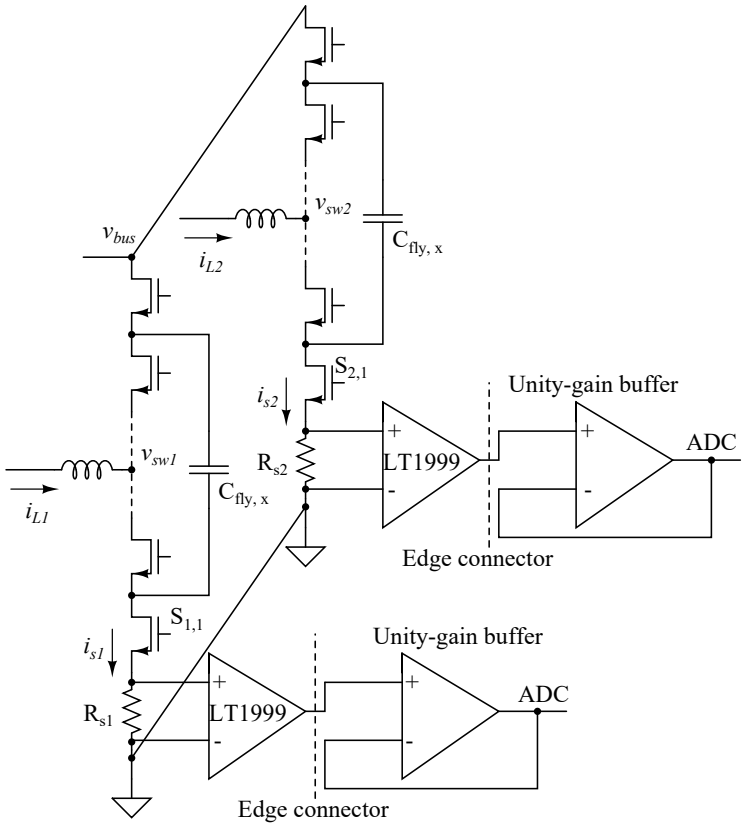

Figure 6.15: Current sensing circuitry for two interleaved FCML phases.

ADC input to increase the driving strength and noise immunity of the signal as it is routed through multiple boards and connectors.

For a conventional 2-level converter, if an up-down count mode carrier counter (i.e., symmetrical triangular wave carrier) is used for digital PWM signal generation, the center of the PWM signal will align with the average inductor current [43], [44]. For the FCML, the same control can be applied to align PWM signals with the average inductor current. As can be seen in Fig. 6.16, the moment when the inductor current reaches the average value is when the carrier counter reaches either zero or peak value.

ADC triggering and windowing

The internal ADC channels and associated control modules in the Texas Instruments C2000 Delfino 28379D DSP are used to implement the required ADC timing.

When the ADC channel is triggered, the sample-and-hold (S/H) switch in the ADC is closed and a capacitor is charged during the programmed time window to sample the input voltage. However, at the moment when the S/H switch is closed, there will be a instantaneous

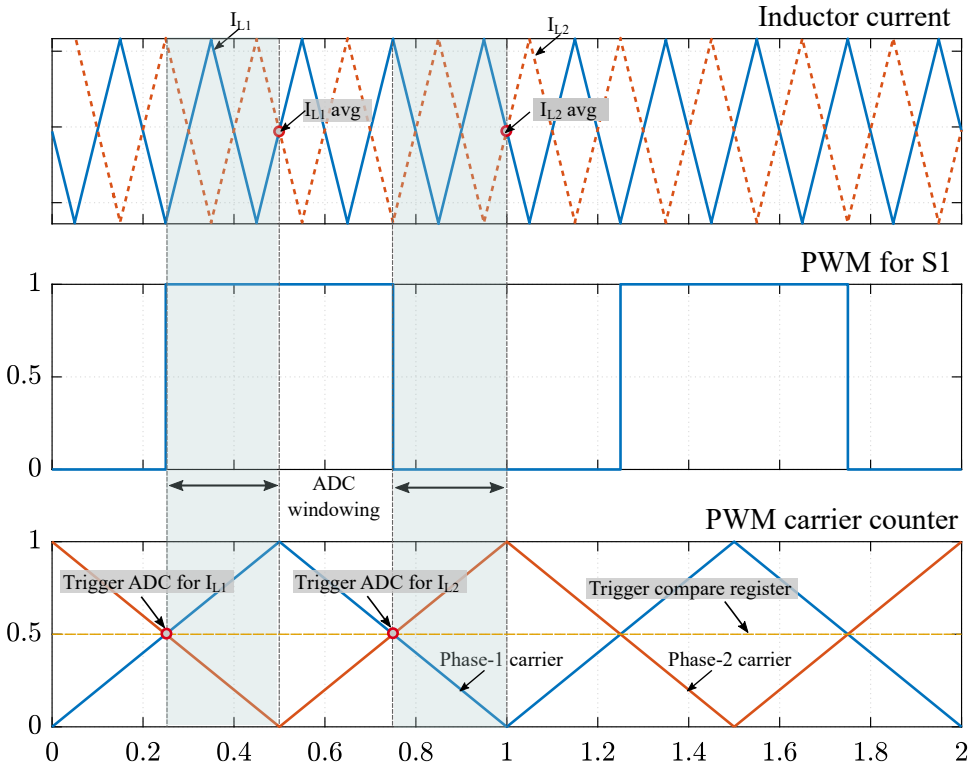

Figure 6.16: Generalized key waveforms demonstrating the timing of ADC triggering to sample the average inductor current of the two phases. Duty ratio is 0.5 for PSPWM. Peak value of the carrier counter and the switching period are normalized.

voltage drop spike on the capacitor, which causes noise in the ADC reading [45]. Thus, the ADCs have to be triggered before the carrier counter reaches zero or peak value to obtain clean readings of the average inductor current.

For the S/H capacitor to obtain the average inductor current, the final reading of the S/H capacitor during the sample window has to be equal to the average inductor current. To ensure this, the ADCs are triggered by using the ePWM module in the TI Delfino DSP when the duty ratio is 0.5, referencing to the PWM carrier counter of $S_{1,1}$. With a duration of a quarter of the switching period, the sensing window ends right at the peak of the carrier counter. For interleaved current sensing, the ADC for i_{L1} is triggered at 0.5 duty ratio during the up-count region, and the ADC for i_{L2} is triggered during the down-count region. A detailed illustration of ADC triggering and windowing is shown in Fig. 6.16. Different ADC timing configurations can also be implemented to adapt to the overall system control as long as it ensures that the final reading of the S/H capacitor is correct. For example, the ADC window can be shortened to leave more headroom for system control computation, yet the end of the window has to be aligned with peak or zero of the carrier counter.

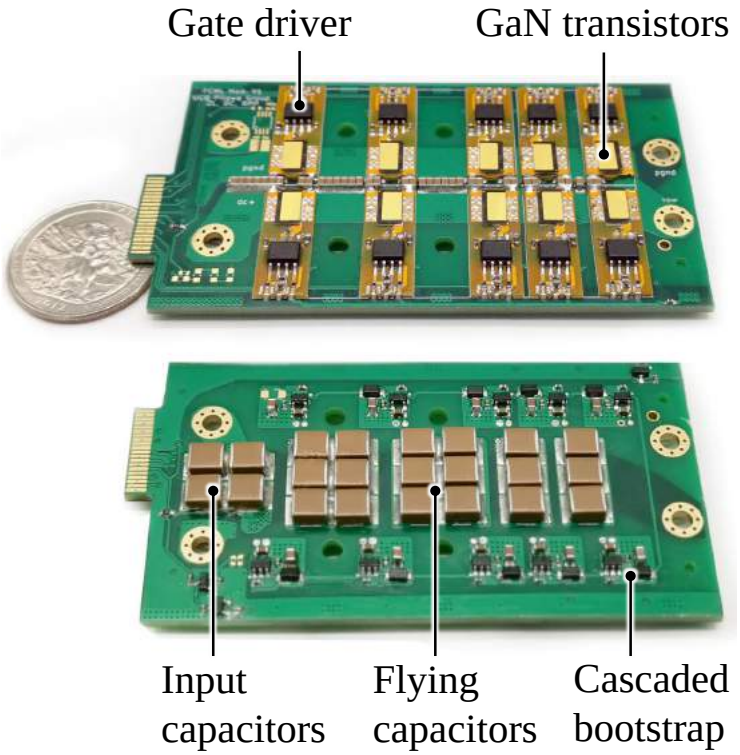

Figure 6.17: First version of the 6-level FCML module with switching cell daughter boards, with a US quarter for size reference.

The detailed block diagram of the firmware setup such as ADCs, interrupts, ePWMs and major PFC/inverter control subroutines using the TI C2000 Delfino DSP is presented in the **Appendix**.

Hardware Design and Assembly

High power density FCML module

A high power density FCML module in Fig. 6.17 is designed with ten 100 V GaN System FETs, isolated gate drivers and cascaded bootstrap method for floating gate driving power [46]. The dimensions of the FCML module are 87 mm × 49 mm × 6.4 mm, which correspond to 27.3 cm^3 of box volume. To test the thermal performance of the FCML module, a thin heatsink is designed for the FCML module as shown in Fig. 6.18. With air flow from a small electrical fan, the FCML module is tested up to 4.3 kW, 400 Vdc to 250 Vdc, with peak heatsink temperature of 70°C. Thermal image and efficiency plot are provided in Fig. 6.19 and Fig. 6.20. In the final EV charger assembly, a simplified switching-cell-less design is used, as shown in Fig. 6.21.

Figure 6.18: FCML module with custom designed low-profile heatsink.

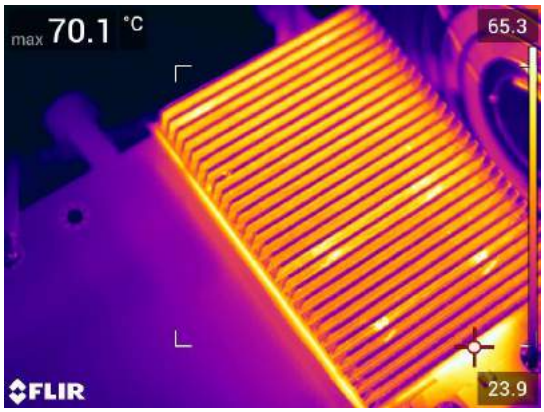

Figure 6.19: Thermal image of the FCML module testing at 4.3 kW, 400 V to 250 V dc-dc.

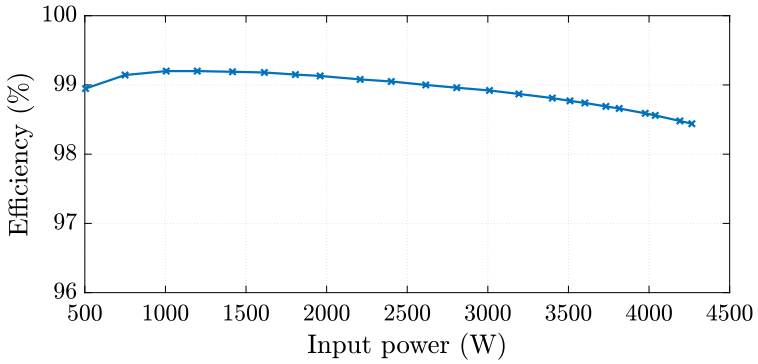

Figure 6.20: Efficiency of the FCML module high power dc-dc thermal testing up to 4.3 kW, 400 Vdc to 250 Vdc with air-cooled heatsink solution.

Full system assembly

A hardware prototype with the proposed architecture and control has been designed and constructed (Fig. 6.22). A render of the an exploded view of the assembly is shown in Fig. 6.23. The hardware prototype consists of an interleaved pair of FCML modules, a series-stacked buffer power stage, an unfolder/rectifier, and capacitors for energy buffering. Signal connectivity to the microcontroller board is provided through a connectors board, and power connectivity between the power stages is provided through bolt and power-tap element connections. The prototype was designed with a philosophy of balancing a combination of electrical, mechanical, and thermal aspects. As such, the electrical design is relaxed from

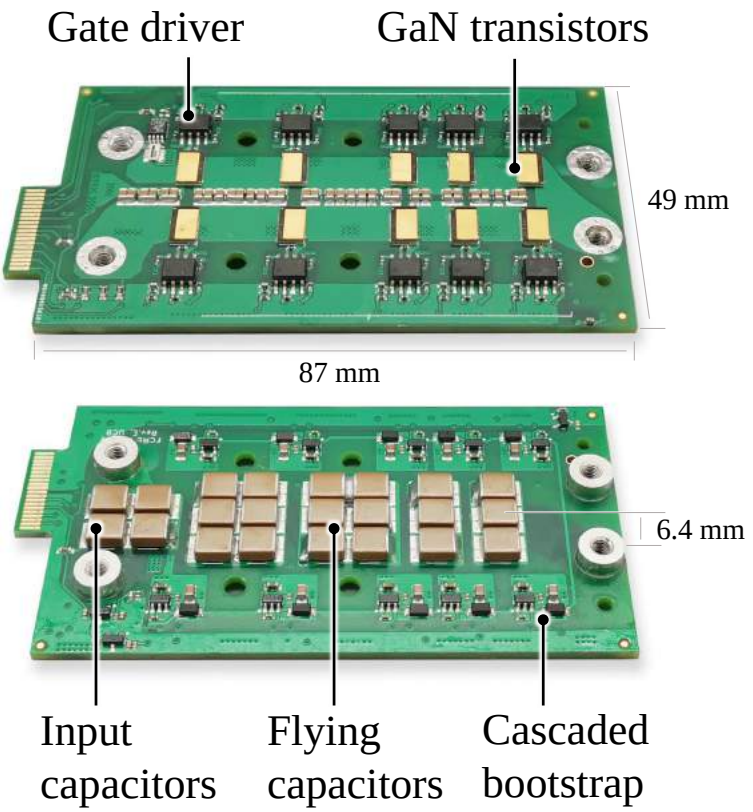

Figure 6.21: 6-level FCML module without switching cell PCBs with dimensions. This module was contract-manufactured.

the absolute optimal layout in favor of mechanical mounting and capability for automated assembly. The mechanical design for the system focuses on a modular approach to assembly, with high utilization of 3D space. The thermal design for the system drove the mechanical and electrical designs such that all of the heat-generating surfaces were placed on a single side, to simplify fluid routing and thermal efficiency for a single-sided liquid- or air-cooling system. Key components used in the charger system and their parameters are listed in Table 6.2.

Experimental Results

Bidirectional PFC and inverter control validation

The converter was tested in the PFC mode with a 120 V_{ac} (low line) and a 240 V_{ac} (high line) input for a 400 V_{dc} output. The converter was also tested in the inverter mode with a 400 V_{dc} input and a 240 V_{ac} output up to 1 kW. The system was tested without a heatsink. Figure 6.24 shows the THD on the ac side of the system running in PFC mode, and Fig 6.25

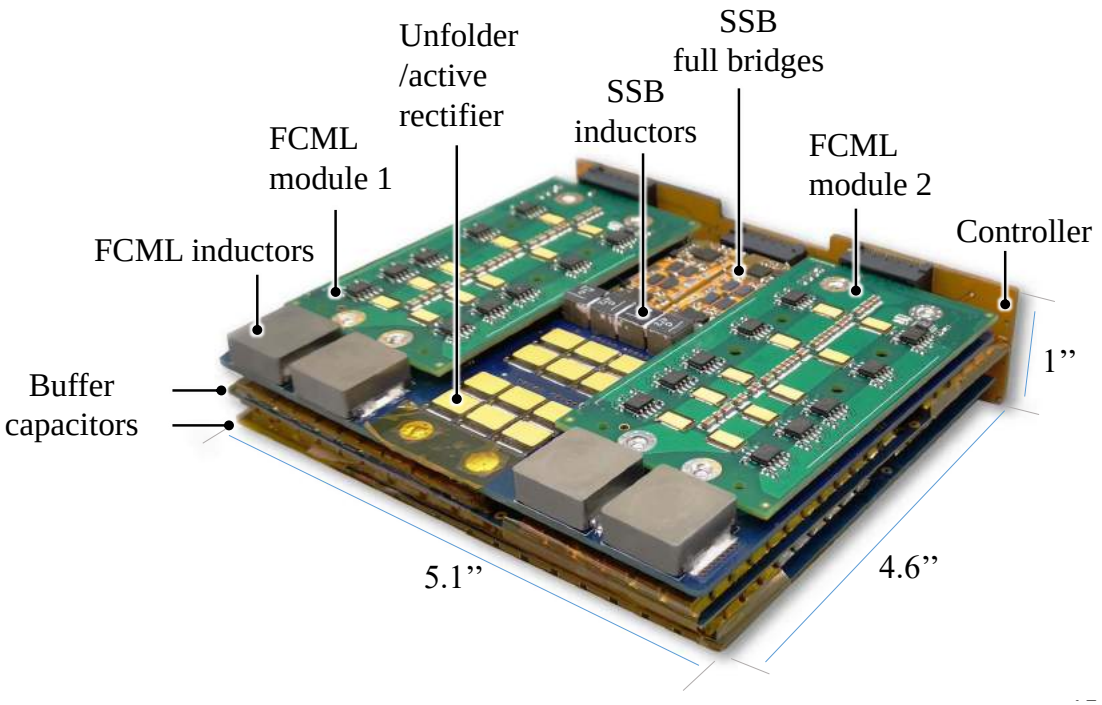

Figure 6.22: The hardware assembly of the EV charger.

shows the measured power factor for 240 V_{ac} to 400 V_{dc}. In all test conditions, the input voltage and current are well in-phase (PF $\geq$ 0.99), and the switching node voltage shows good balancing between the flying capacitor voltages (v_{sw1}, Fig. 6.26) and good current balancing between interleaved FCML modules (i_{L1}, i_{L2}, Fig. 6.27). To validate the control for the SSB, film capacitors of smaller values than the full power specifications were used for C_1 (80 μF) and C_2 (68 μF) to simulate the voltage ripple effects at the full power level (6 kW). The dc bus ripple (Δv_{dc}) is about 10 V (2.5% of 400 V_{dc} – Fig. 6.26) at 1.5 kW, high-line PFC input.

High power inverter mode test

To validate the control architecture and high density implementation, the converter has been operated in the inverter mode at high power. A 400 V_{dc} input dc voltage with 2 Ω source impedance were used to produce a 240 V_{ac} output. The system was tested while connected to the cold plate liquid cooling system set at 25 °C, as shown in Fig. 6.28. Figure 6.29 shows a plot of efficiency for the inverter stage up to 6.1 kW input. It can be seen that the efficiency values are well above 98.5% for most of the range, with a peak above 99%. To capture such high conversion efficiencies, a high precision power analyzer (Keysight PA2201) was used. Table 6.3 lists converter performance specifications, including important efficiency and power density metrics. Operation waveoforms at 6.1 kW are shown in Fig. 6.30.

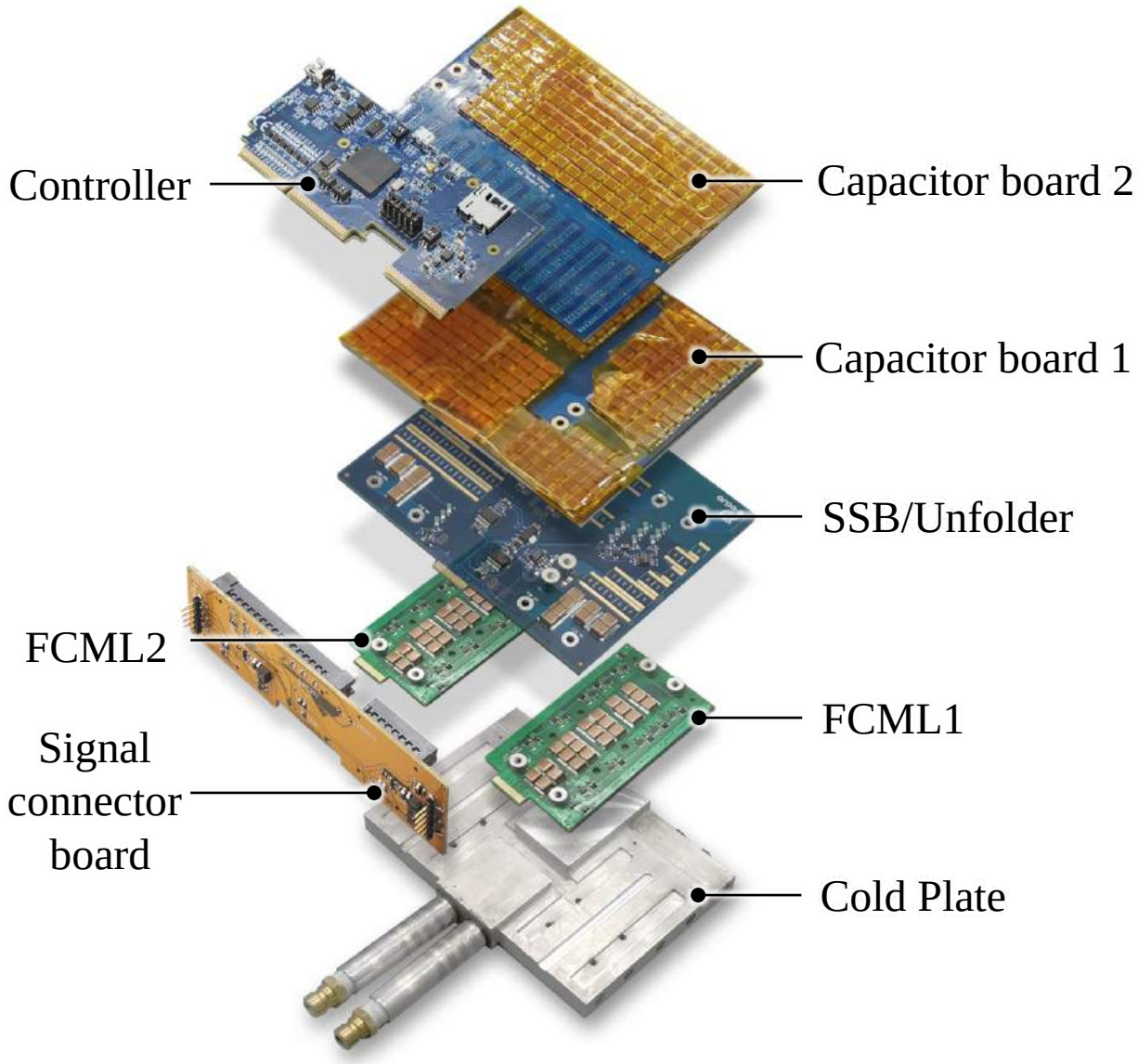

Figure 6.23: Exploded view render of the hardware assembly.

Table 6.2: Component listing

Component	Part No.	Parameters
Interleaved 6-Level FCML (per parallel leg)		
GaN FETs	GaN Systems GS61008T	100 V, 7 $m\Omega$
Isolated Gate Drivers	Si8271GB-IS	Silicon Labs Si827x Series
Flying Capacitors	TDK C5750X6S225K250KA	2.2 μF × 2–5 (parallel, $\sim$ 2.6μF effective)
Inductors	Vishay IHLP6767GZER220M11	22 μH × 2 (series)
Active Rectifier / Unfolder		
GaN FETs	GaN Systems GS66516T	650 V, 25 $m\Omega$× 3 (parallel)
Isolated Gate Drivers	Si8274GB1-IS1	Silicon Labs Si827x Series
Interleaved Series-Stacked Buffer (per parallel leg)		
GaN FETs	EPC 2033	150 V, 7 $m\Omega$
Isolated Gate Drivers	Si8274GB1-IM1	Silicon Labs Si827x Series
Inductors	Coilcraft XAL7070-472	4.7 μH × 2 (series)
Buffer Capacitors		
C_1	TDK C5750X6S225K250KA	0.43 μF × 820 (parallel, $\sim$ 366μF effective at 400 V bias)
C_2	TDK C5750X7S2A156M250KB	3 μF × 200 (parallel, $\sim$ 600μF effective at 100 V bias)
Control		
Microcontroller	TI F28379D controlCARD	C2000 Series Board

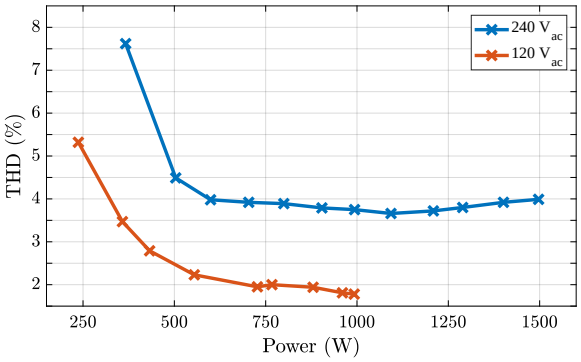

Figure 6.24: The THD of the system, PFC mode from 120 and 240 V_{ac} to 400 V_{dc}.

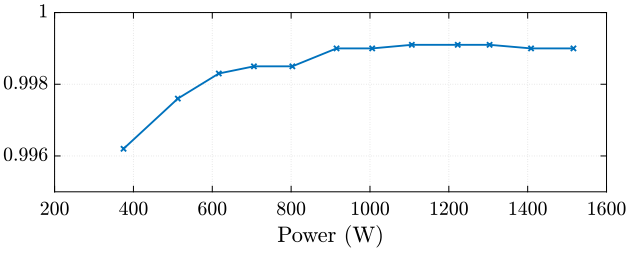

Figure 6.25: The measured power factor of the system, PFC mode 240 V_{ac} to 400 V_{dc}.

Conclusion

The successful experimental demonstration of the 6.1 kW EV charger proves the proposed coupled control of the SSB with the main inverter/PFC stage can be realized with careful hardware design under high current and noise operation conditions.

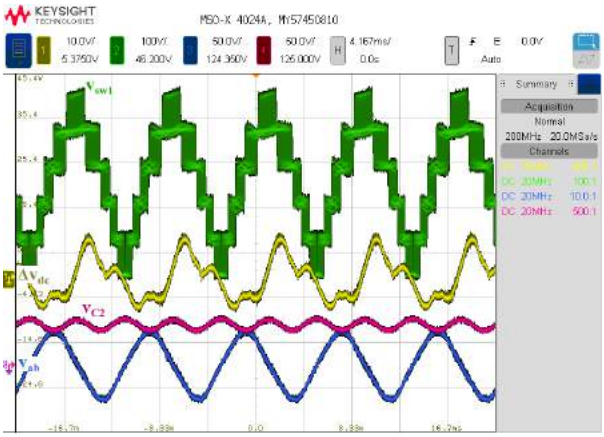

Figure 6.26: Typical SSB voltage waveforms for v_{C2} and v_{ab}, dc bus voltage ripple (ac coupled), and FCML switch-node of the system, PFC mode from 240 V_{ac} to 400 V_{dc}, 1.5 kW.

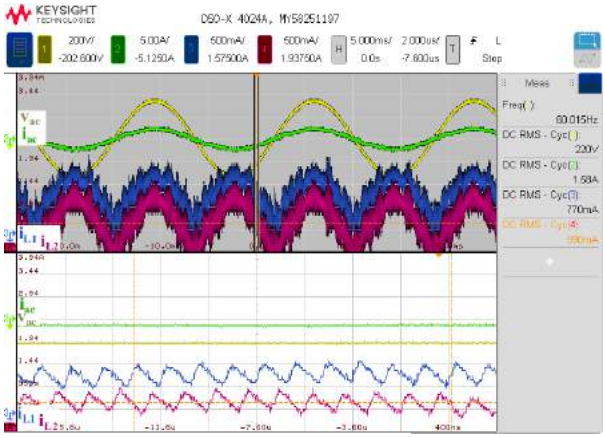

Figure 6.27: Typical current waveforms of the interleaved FCML, PFC mode from 240 V_{ac} to 400 V_{dc}, 375 W.

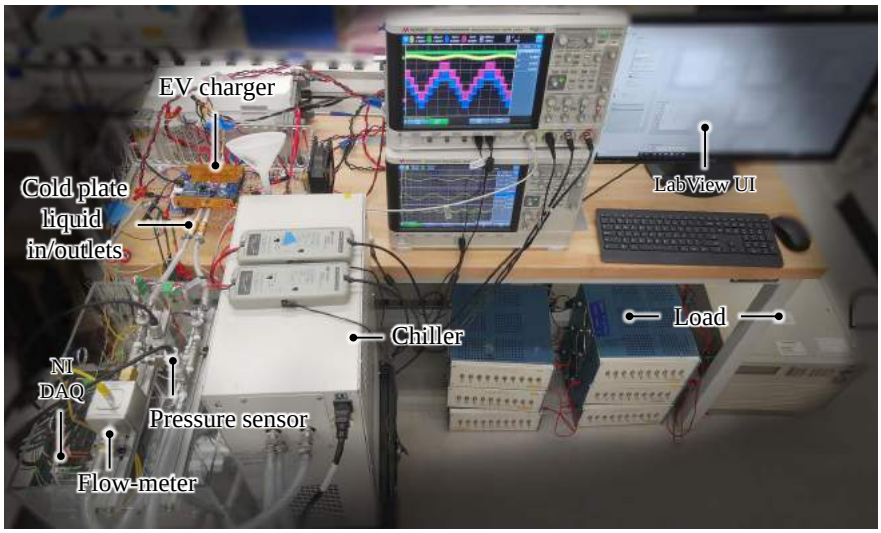

Figure 6.28: Full experimental setup with the liquid cooling loop and temperature data acquisition.

Table 6.3: Key performance specifications for the 6.1 kW inverter test

Parameter	Value
DC Voltage	400 V_{dc}
AC Voltage	240 $V_{ac,\ rms}$
AC Current	25 A
AC Power	6.1 kW
Peak Efficiency	99.01% at 1.1 kW
Full Load Efficiency	97.7% at 6.1 kW
Switching Frequency	150 kHz
Effective Frequency @ v_{sw}	750 kHz
PCBA Rect. Box Dimensions	5.1" × 4.6" × 1.0" (12.95 cm × 11.68 cm × 2.54 cm)
Cold Plate Dimensions	5.1" × 3.6" × 0.375" (12.95 cm × 9.14 cm × 0.95 cm)
Without cold plate	
Weight	0.8 kg
Volume	23.46 in^3 (384.4 cm^3)
Volumetric Power Density (w/o. cold plate)	260 W/in^3 (15.9 W/cm^3)
Gravimetric Power Density	7.6 kW/kg
With cold plate	
Weight	1.1 kg
Volume	30.35 in^3 (497 cm^3)
Volumetric Power Density	201 W/in^3 (12.3 W/cm^3) e
Gravimetric Power Density	5.5 kW/kg

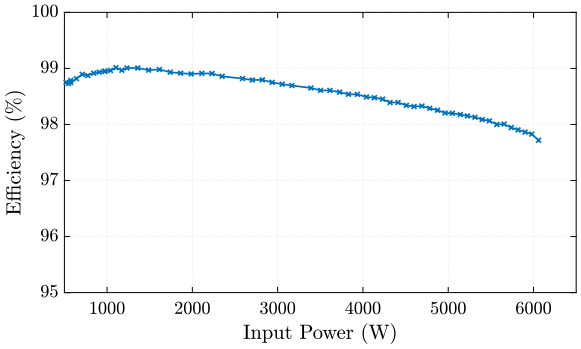

Figure 6.29: The efficiency of the 6.1 kW inverter test, 400 V_{dc} to 240 V_{ac}.

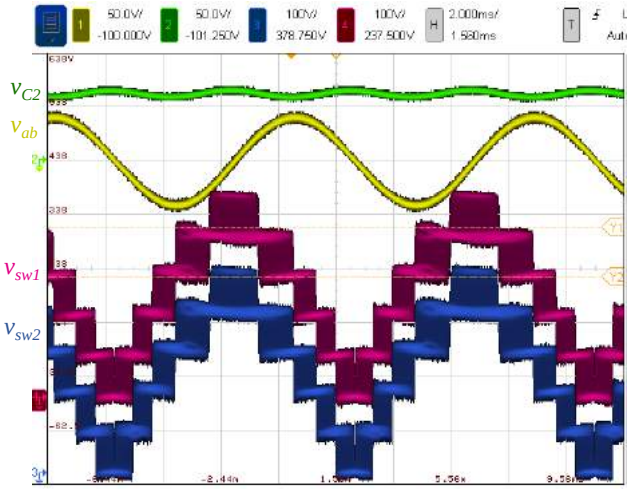

Figure 6.30: Typical SSB voltage waveforms for v_{c2} and v_{ab}, and FCML switching node voltages from 400 V_{dc} to 240 V_{ac}, 6.1 kW.

Chapter 7

Half-Bridge Series-Stacked Buffers for Low-power Flyback Rectifiers

7.1 Introduction

Ac-dc conversion using a flyback converter with no power factor correction (PFC) function is widely used in the universal ac input (90-240 V_{ac}) mobile and laptop chargers. With the high power delivery capability of USB-C, the state-of-the-art mobile chargers can reach a maximum power of 65 W [47], with output voltages from 10 to 20 V. The conventional solution with an input bulk capacitor and a flyback converter is shown in Fig. 7.1. The two main passive components in the chargers are the flyback transformer and the input electrolytic bulk capacitor. To achieve high power density and efficiency, significant research efforts have been dedicated to the flyback converter, such as the active-clamp technique [48] and the use of planar and more advanced transformer structures [49], [50] etc. Yet, fewer ideas to address the reduction of the input capacitor - typically the largest component - have been successfully demonstrated. The input capacitor is needed to maintain the input voltage to the flyback to be above a certain voltage to avoid high peak current saturating the primary side of the flyback transformer [51]. For instance, as shown in Fig. 7.2, in the worst case of 90 $V_{\text{ac, rms}}$, the input bus voltage is maintained to be above 80 V for the flyback to function. Similar to the large dc-bus capacitor in PFC applications [42], this narrow ripple requirement leads to large required size of the capacitor. Active buffers in single-phase ac-dc application with high power factors such as [11], [52], [53] reduce the required capacitance for twice-line frequency power ripple buffering by operating the buffer capacitor with high voltage swings, while maintaining the dc-bus voltage with extra active converters and control. For non-PFC flyback adapters considered in this work, a similar approach can be employed. Here, the key design aspects are low-complexity and reduced cost compared to high-power PFC converters. In this work, the buffer solution in Fig. 7.3 is proposed based on the series-stacked buffer (SSB) in [3], [17], [52]. The required capacitance is reduced by more than half compared to the passive solution. Meanwhile, the proposed buffer solution

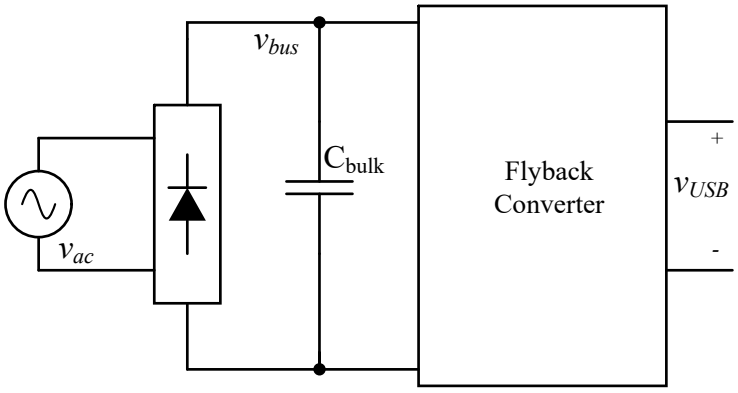

Figure 7.1: Conventional charger solution with diode bridge, input bulk capacitor, and a flyback converter.

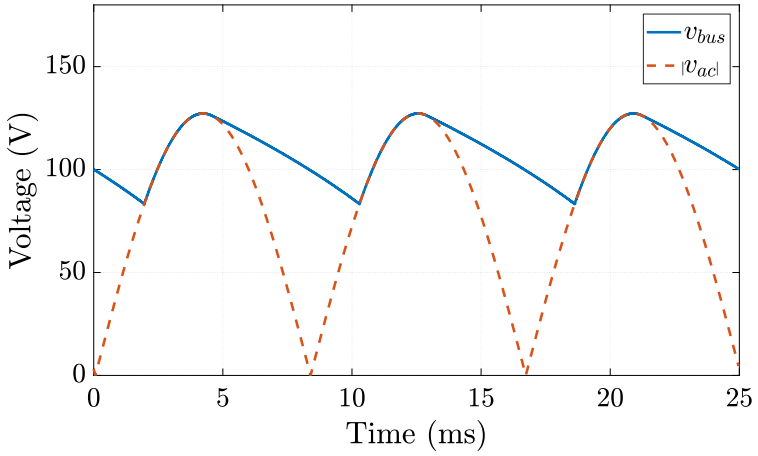

Figure 7.2: Input voltage waveforms with a 80 μF input bulk capacitor, at 90 V_{ac}, 60 Hz, and 65 W.

is easier to implement than existing SSB solutions, as it employs ground-referenced voltage sensing and a low-complexity half-bridge circuit. In this work, detailed operation, control and component sizing of the buffer are discussed, and hardware verification results at various ac voltage and power conditions are provided.

7.2 Principle of Operation of the Half-bridge SSB

As shown in Fig. 7.3, a filter capacitor C_1 is connected in series with a half-bridge circuit. The half-bridge circuit generates a unipolar ac voltage v_{ab} to partially cancel the ripple on

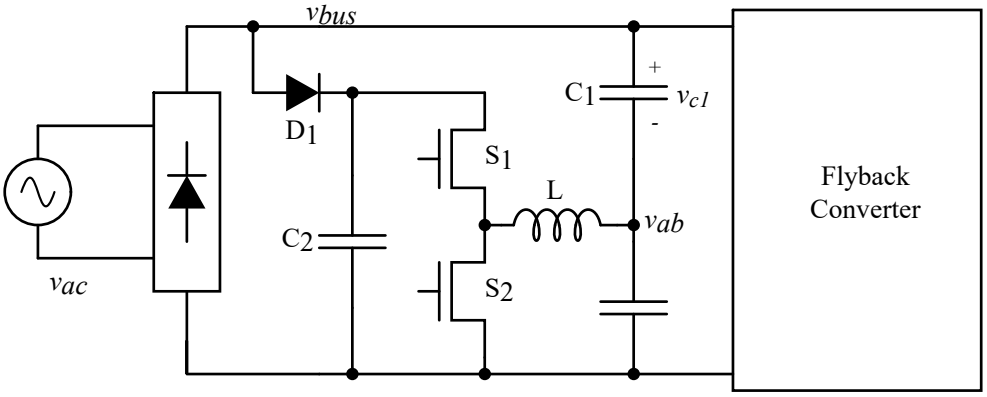

Figure 7.3: Proposed buffer solution and flyback.

C_1 such that the entire buffer structure appears as a larger capacitor across the input of the flyback converter. The dc bias of $v_{\rm ab}$ is calculated from its ripple amplitude such that $v_{\rm ab}$ is not clamped at zero. A support capacitor C_2 provides the needed voltage to generate $v_{\rm ab}$. To maintain $v_{\rm C2}$ to be always above $v_{\rm ab}$, a diode D_1 is connected to the dc-bus.

Figure 7.2 shows the simulated waveform of with a 80 μF input capacitor at 90 $V_{\rm ac}$, 65 W. With the proposed buffer solution, $C_1 = 30$ μF and $C_2 = 10$ μF, the bus voltage can be controlled to be identical to Fig. 7.2, as shown in Fig. 7.4. As can be seen, $v_{\rm C1}$ swings from peak input ac voltage $90\sqrt{2}$ V to 20 V (107 V swing). With $v_{\rm ab}$ partially canceling the ripple portion of $v_{\rm C1}$, the ripple seen on $v_{\rm bus}$ is limited to a range from 83 V to $90\sqrt{2}$ V, which is identical to using a 80 μF input bulk capacitor.

A key benefit of the proposed approach is the ability to greatly reduce the active filter power conversion losses for many practical line voltages and power levels by disabling the half-bridge switching. For higher line voltages, the minimum voltage can still be maintained with only 30 μF across the dc bus, which can be accomplished by operating the half-bridge with a duty cycle of $D = 0$ (i.e., bottom switch S_2 permanently on). Simulation waveforms at 120 Vac, 65 W with this operation mode is shown in Fig 7.5. As can be seen, the minimum voltage is still above 83 V. This mode of operation can also be employed at 90 Vac, if the output power is lower, which would be the case if the USB-C charger is used for smaller loads, as shown in Fig. 7.6, for operation at 90 $V_{\rm ac}$, 25 W with C_1 shorted across the dc-bus.

7.3 Control

The overall control diagram is shown in Fig. 4.4. Three voltages $v_{\rm bus}$, $v_{\rm ab}$ and $v_{\rm C2}$ are sensed. Since they are all ground-referenced voltages, no differential sensing as in [52] is needed. First, the ripple component $\Delta v_{\rm C1}$ is extracted with a high-pass filter (HPF) [53] with a corner frequency at 10 Hz. After that, $\Delta v_{\rm C1}$ is scaled with parameter k (0 to 1).

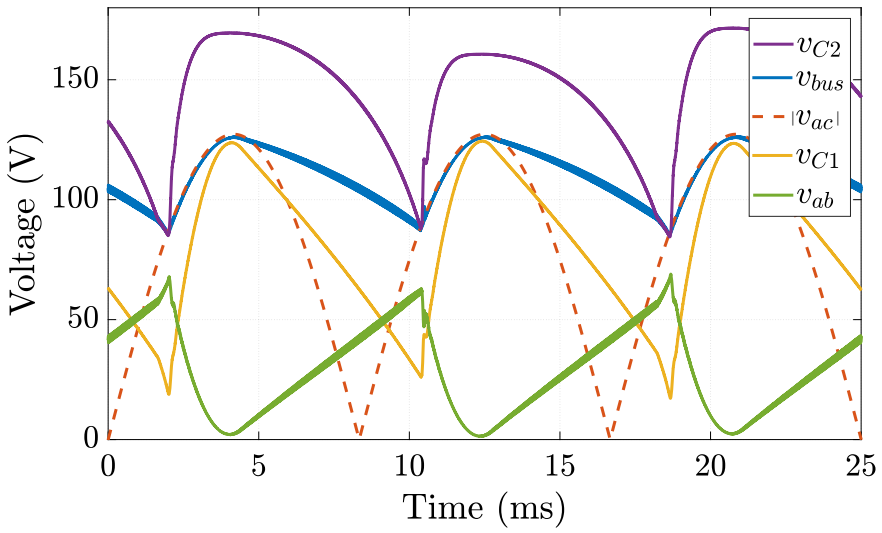

Figure 7.4: Simulated waveforms of the proposed active buffer in PLECS for 90 Vac, 65 W.

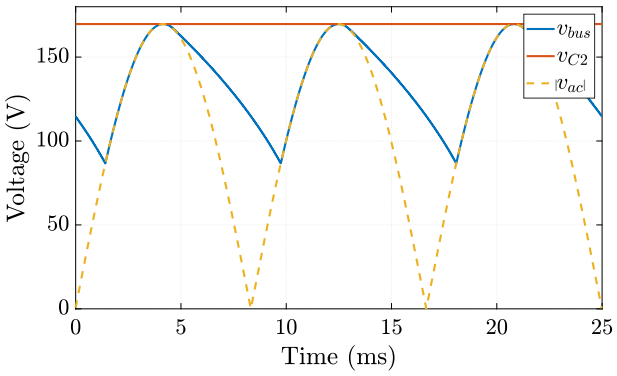

Figure 7.5: Simulated waveforms of the proposed active buffer in PLECS for 120 Vac, 65 W, with S_2 shorted to ground.

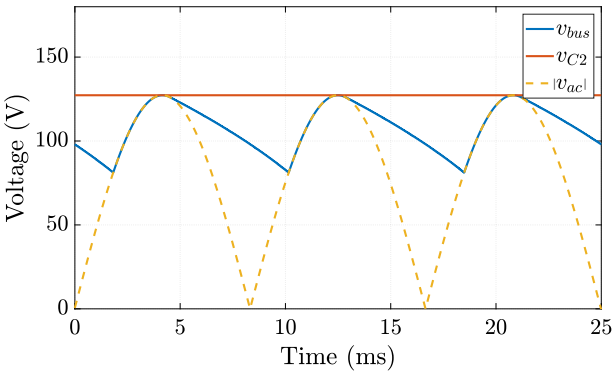

Figure 7.6: Simulated waveforms of the proposed active buffer in PLECS for 90 Vac, 25 W, with S_2 shorted to ground.

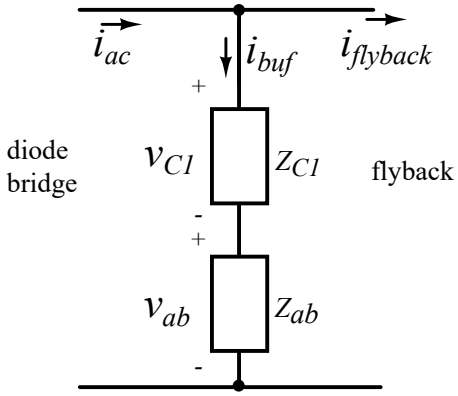

Figure 7.7: Equivalent impedance of the proposed buffer structure.

Consequently, the ripple portion of $v_{\rm ab}$ is $-k\Delta v_{\rm C1}$, which means the ripple on the bus is reduced to $(1-k)\Delta v_{\rm C1}$. Since the half-bridge terminals are connected in series with C_1 across the rectified bus, the equivalent ac impedance of the half-bridge can be analyzed using the simplified schematic drawing in Fig. 7.7. Since the two equivalent impedances are in series, and there should be no net dc current in $i_{\rm buf}$ for capacitive behavior, the relation holds

$$\frac{\Delta v_{\rm ab}}{Z_{\rm ab}} = \frac{\Delta v_{\rm C1}}{Z_{\rm C1}} = i_{\rm buf}. \tag{7.1}$$

As a result, the equivalent impedance of the half bridge is related to C_1 as

$$\frac{Z_{\rm C1}}{Z_{\rm ab}} = \frac{\Delta v_{\rm C1}}{\Delta v_{\rm ab}} = \frac{1}{-k}. \tag{7.2}$$

Thus the relationship of the equivalent impedance $Z_{\rm eq}$ across the dc-bus is

$$Z_{\rm eq} = Z_{\rm C1} + Z_{\rm ab} = (1-k)Z_{\rm C1} \tag{7.3}$$

In other words, the relation between C_1 and the final equivalent capacitance across the dc-bus $C_{\rm eq}$ is determined by k as

$$C_{\rm eq} = C_1/(1-k) \tag{7.4}$$

To operate the half bridge in the buffer, the final $v_{\rm ab,\ ref}$ needs to be unipolar (always above zero). As such, a bias voltage is calculated by detecting the amplitude of $k\Delta v_{\rm C1}$, which is then added to the final $v_{\rm ab,\ ref}$. It should be noted that while the goal of the buffer control for high-power-factor applications [52], [53] is to make the equivalent capacitance of the buffer larger (i.e., to minimize dc-bus voltage ripple as much as possible), it is not the goal of the non-PFC controller implemented here. For conventional non-PFC type flyback application, the larger the input capacitor is, the higher the input current spike will be, as the conduction angle (the portion of time in a line cycle that the ac input voltage charges the input capacitor) [51] of the ac input voltage gets smaller.

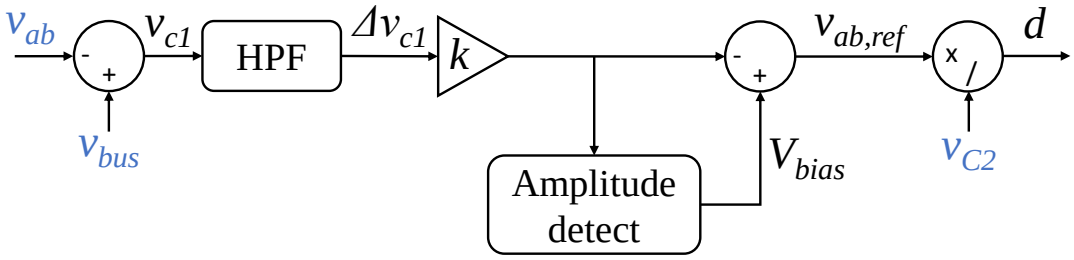

Figure 7.8: Overall control diagram.

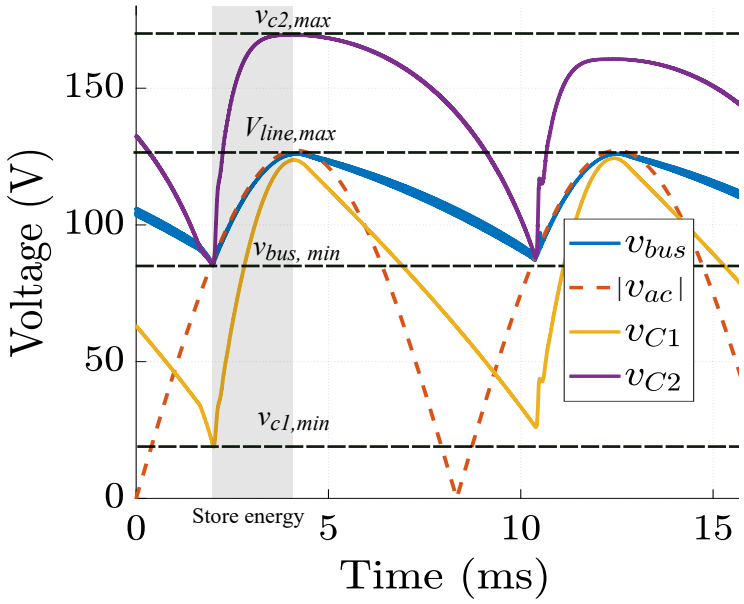

Figure 7.9: Annotated capacitor voltage ripple during energy storage phase for 90 Vac, 65 W.

Component	Part No.	Volume
C_1	(TDK C5750X6S, 450 V) × 27	1.9 cm^3
C_2	(TDK C5750X6S, 450 V) × 16	1.1 cm^3
L	6.8 μH, Vishay IHLP5050	0.58 cm^3
Total volume		3.58cm^3
Switch	Navitas NV6117, 650 V × 2	
Gate driver	Silab 8274	

Table 7.1: Key component list.

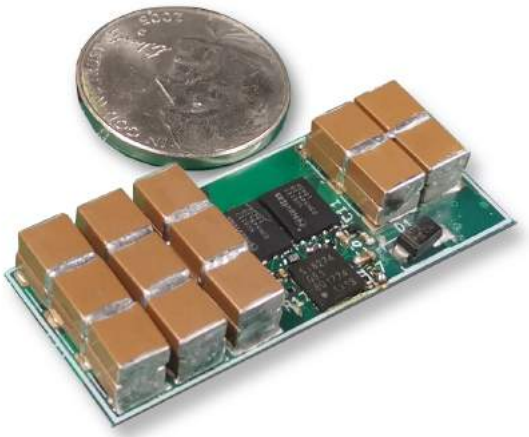

Figure 7.10: Size comparison between the proposed buffer and a US five cent coin.

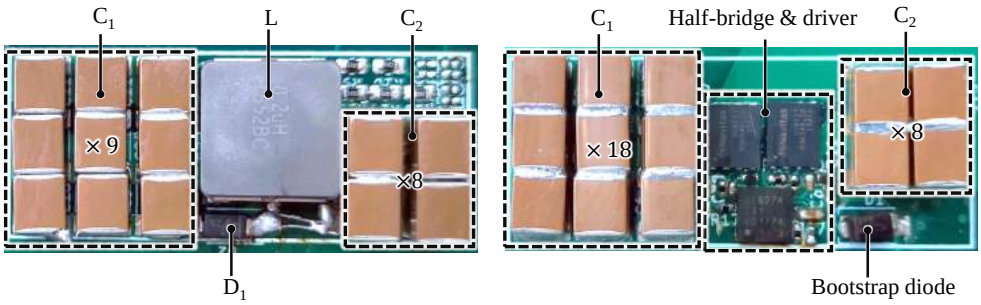

Figure 7.11: Top and bottom of the hardware prototype power stage.

7.4 Capacitor Sizing

The first step to size the capacitors in the proposed active buffer is to decide the final target equivalent capacitance that the buffer is trying to emulate, i.e., the needed input bulk capacitance to maintain required minimum voltage in the worst case scenario. For instance, in the example given above, the needed capacitance across the bus to maintain a minimum voltage of 83 V for 90 Vac input is 80 μF.

With an ideal lossless half-bridge converter, assuming that v_{C2} always stays above the bus voltage, the maximum voltage swing for v_{C1} is from the peak of the line voltage ($90\sqrt{2}$ V) to zero. However, when v_{C1} reaches zero, v_{ab} would be equal to the minimum bus voltage, and the duty ratio of the half-bridge would be one. In the real implementation, v_{bus} will drop further because D_1 turns on to charge C_2. To avoid over-modulation, v_{C1} should swing to a non-zero minimum voltage $v_{C1,\,min}$. The relation between the allowed voltage swing,

capacitor sizing and control scalar k is thus

$$\frac{\Delta v_{\mathrm{C1}}}{\Delta v_{\mathrm{bus}}} = \frac{V_{\mathrm{line,\ max}} - v_{\mathrm{C1,\ min}}}{V_{\mathrm{line,\ max}} - v_{\mathrm{bus,\ min}}} = \frac{C_{\mathrm{eq}}}{C_1} = \frac{1}{1-k}, \tag{7.5}$$

from which C_1 and k can be determined. For instance, if $V_{\mathrm{line,\ max}} = 90\sqrt{2}$ V, $v_{\mathrm{C1,\ min}} = 0$ V, and $v_{\mathrm{bus,\ min}} = 83$ V, the corresponding parameters are $C_1 = 27$ μF and k = 0.65.

In the ideal lossless scenario, C_2 is sized so that the peak capacitor voltage is below the voltage rating of the switches in the half-bridge. When the dc-bus swings from $v_{\mathrm{bus,\ min}}$ to $V_{\mathrm{line,\ max}}$, both v_{C1} and v_{C2} swing from their minimum voltage to maximum. Figure. 7.9 annotates the key voltage levels that relate to the change in energy during energy storage phase (grey area). As the buffer is emulating an equivalent capacitor C_{eq}, the total change in energy in the buffer can be calculated as:

$$\Delta E_{\mathrm{buf}} = \frac{1}{2} C_{\mathrm{eq}} (V^2_{\mathrm{line,\ max}} - v^2_{\mathrm{bus,\ min}}) \tag{7.6}$$

In the same time frame (grey area) in Fig. 7.9, C_1 is charged from $v_{\mathrm{c1,\ min}}$ to $V_{\mathrm{line,\ max}}$, and C_2 is charged from $v_{\mathrm{bus,\ min}}$ to $v_{\mathrm{C2,\ max}}$. Considering the energy flow in the circuit, the relation among the total change in stored energy of the buffer, and the change in energy in C_1 and C_2 can be expressed as,

$$\begin{aligned} \Delta E_{\mathrm{buf}} &= \Delta E_{\mathrm{C1}} + \Delta E_{\mathrm{C2}} \\ \frac{1}{2} C_{\mathrm{eq}} (V^2_{\mathrm{line,\ max}} - v^2_{\mathrm{bus,\ min}}) &= \frac{1}{2} C_1 (V^2_{\mathrm{line,\ max}} - v^2_{\mathrm{C1,\ min}}) \\ &\quad + \frac{1}{2} C_2 (v^2_{\mathrm{C2,\ max}} - v^2_{\mathrm{bus,\ min}}) \end{aligned} \tag{7.7}$$

and the maximum of v_{C2} can be solved as

$$v_{\mathrm{C2,\ max}} = \sqrt{\frac{\Delta E_{\mathrm{bus}} - \Delta E_{\mathrm{C1}}}{C_2} + v^2_{\mathrm{bus,\ min}}}, \tag{7.8}$$

from which the voltage ratings for the actual C_2 capacitors and switches can be determined.

7.5 Hardware and Experimental Results

The proposed buffer is realized in a hardware prototype with TDK X6S ceramic capacitors and a half-bridge circuit implemented with Navitas NV6117, 650 V GaN switches with integrated gate drivers. The buffer prototype is compared with a US five cent coin in Fig. 7.10 for size reference, and the key components are annotated in Fig. 7.11, and listed in Table 7.1. While X6S ceramic capacitors have high energy density, due to the nonlinear-capacitance behavior, the final number of the capacitors in the hardware are determined empirically [10], [23]. In Table 7.1, the total passive component volume is **3.58 cm^3**. Since the equivalent

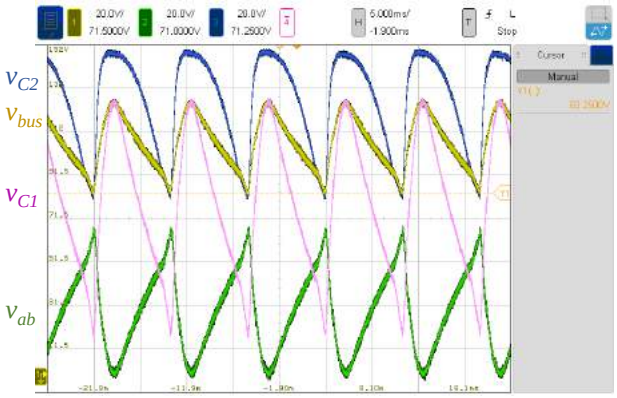

Figure 7.12: Experimental waveforms at 90 V_{ac}, 60 Hz, 65 W.

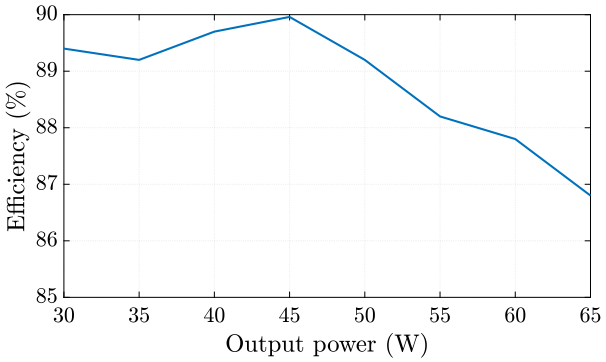

Figure 7.13: Efficiency plot of the proposed buffer.

passive solution is a 450 V, 80 μF capacitor, an exemplar electrolytic capacitor with such specifications, Panasonic ECO-S2WP820BA, is selected for comparison. The Panasonic ECO-S2WP820BA has a diameter of 30 mm and a height of 22 mm, corresponding to a volume of **15.6 cm**^{3}, which is more than four times larger than the total passive volume of the proposed buffer. In the recently proposed $MinE-Cap$ commercial solution [54], where a high voltage electrolytic capacitor (400 V, 39 μF) is connected to the dc-bus all the time, and a lower voltage electrolytic capacitor (160 V, 100 μF) with higher capacitance density only switches into the filter capacitor network during low ac line voltage conditions, the total capacitor volume is **5 cm**^{3}. In the $MinE-Cap$ solution, actual capacitor operating voltages are considered to optimize the capacitance density at different voltage ratings to reduce the overall size of the dc-bus capacitor. A similar approach to select capacitors based on operating voltage can also be applied to the proposed buffer topology in this work to further reduce the needed capacitor size with more comprehensive optimization process [17].

Moreover, in the mobile charger application, the cylindrical shape of the electrolytic capacitors makes them difficult to package in a low-profile fashion, resulting in low filling factor of the usable space in the charger. In comparison, the ceramic capacitors are low-profile and can be distributed with more degree of freedom in the available space inside the charger.

The experimental waveform at 90 V_{ac}, 60 Hz, 65 W, the most critical test condition for maintaining a minimum voltage, is shown in Fig. 7.12. The half-bridge converter switches at 300 kHz and the control is implemented with TI Delfino DSP. It can be seen that the minimum v_{bus} is 83 V as simulated in Fig. 7.4. The voltage v_{C2} is also maintained to generate the correct v_{ab}. In the experimental setup, the flyback converter load is emulated with an electronic load in constant power mode. Since the buffer only needs to turn on above certain power, the efficiency of the buffer is tested from 30 W to 65 W, and plotted in Fig. 7.13. The peak efficiency is 90% at 45 W output power. More design optimization on both component

choices and converter operation parameters can be done to minimize the loss [55].

7.6 Conclusion

The proposed active buffer topology can effectively reduce the required capacitance for non-PFC type flyback rectifiers through more effective utilization of capacitance, comapred to conventional passive filtering. Since the proposed buffer is emulating a larger capacitor at the input of the flyback converter, it can be directly substituted into an existing flyback charger solution without changing the rest of the system, making the proposed solution an attractive option for reducing the size of USB-C chargers.

Chapter 8

Bipolar Multilevel Full Ripple Port Buffer

While the SSB provides benefits such as partial power processing of the buffer converter to achieve high efficiency, there are certain limitations that motivate us to explore other buffer solutions. For instance, while C_1 has relatively high voltage swing, the allowed ripple is limited by the voltage rating of the physical capacitor, which limit the energy utilization of the main energy buffering capacitor. Moreover, with the loss compensation scheme in Chapter 4, the extra ripple induced on the dc-side is also not negligible. In this chapter, we would like to explore a buffer topology that can achieve much higher energy utilization than the SSB, as well as better dc current ripple control.

8.1 Introduction

The bipolar ripple port converter [5] in Fig. 8.1 is a type of active decoupling solutions that applies a line-frequency sinusoidal voltage onto the buffer capacitor with a full-bridge dc-ac inverter to provide the reactive power for active decoupling. Because the buffer capacitor is fully discharged to zero volt at every zero crossing of the sinusoidal voltage, the EUR is 100%. That is, all the energy in the capacitor is used to compensate for the power difference between the dc and ac side in one half 120 Hz cycle. If the buffer capacitor voltage swings with the amplitude up to the full bus voltage, the required capacitance for decoupling is minimized. Moreover, since the power of the buffer capacitor is dependent only on the voltage generated by the buffer converter, the operation is relatively independent from the dc source impedance, and the dc current ripple is very low. However, because of the high voltage stress and high RMS current through the buffer capacitor, implementing the full-bridge converter with a conventional two-level design suffers from large filter inductor size, high voltage stress on the switches, and higher device count compared to half bridge unipolar ripple port. As a result, high loss and large inductor size usually offset the benefit of the small capacitance for the conventional two-level bipolar ripple port.

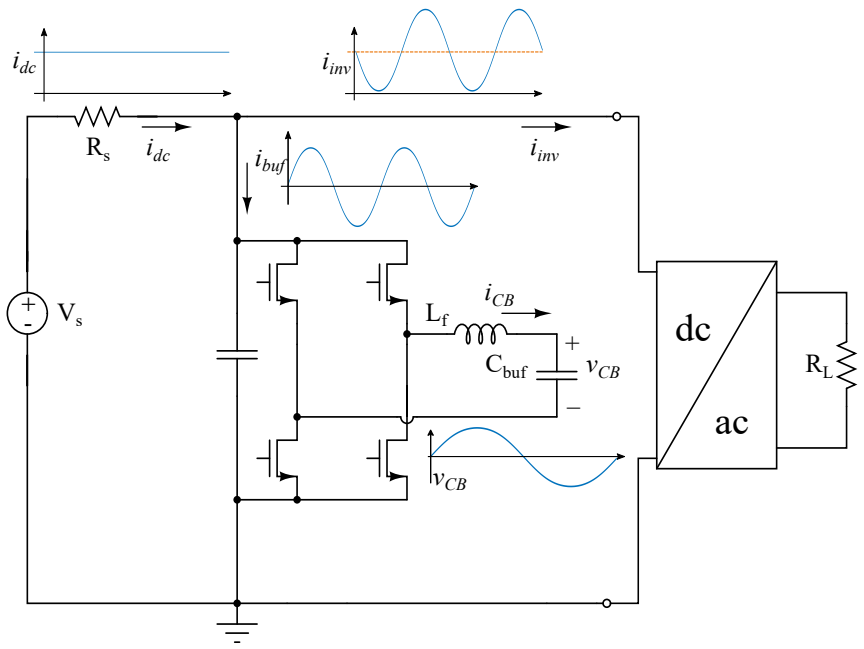

Figure 8.1: Schematic drawing and key waveforms of the bipolar ripple-port active buffer in single-phase inverter applications.

To shrink the converter size and improve efficiency, different active decoupling solutions have been proposed to improve upon the bipolar ripple port converter, which generally incur a trade-off of lower energy utilization ratio of the capacitor. For example, the unipolar half-bridge power pulsating buffer [7], [56] has half the device count of the full-bridge bipolar ripple port. However, if the dc-bias voltage of the capacitor is zero to achieve 100% EUR, the inductor current is not continuous at the voltage zero-crossings. To avoid high current slew rate and high peak current in the actual implementation, the buffer capacitor typically holds high dc bias such that the inductor current is continuous and has lower amplitude, which lowers the EUR and requires higher buffer capacitance as a trade-off.

As briefly mentioned in the beginning of this chapter, while the SSB configuration reduces the power processed by the full-bridge converter to reduce the overall loss by connecting a bulk capacitor in series to block the high dc-bus voltage, the main buffering bulk capacitor is biased with the dc-bus voltage, which means the allowed ripple is limited by the voltage rating of the physical capacitor. As a result, higher total buffer capacitance is also needed. In the practical designs of [3], [7], [56], the energy utilization ratio of the buffer capacitors are all below 50%. To achieve high power density with higher buffer capacitance, instead of using low-energy-density film capacitors, many single high-energy-density multi-layer ceramic capacitors (MLCC) are connected in parallel and packaged as large capacitor blocks. While MLCCs brings benefits such as high energy density and efficiency, they also raise two major

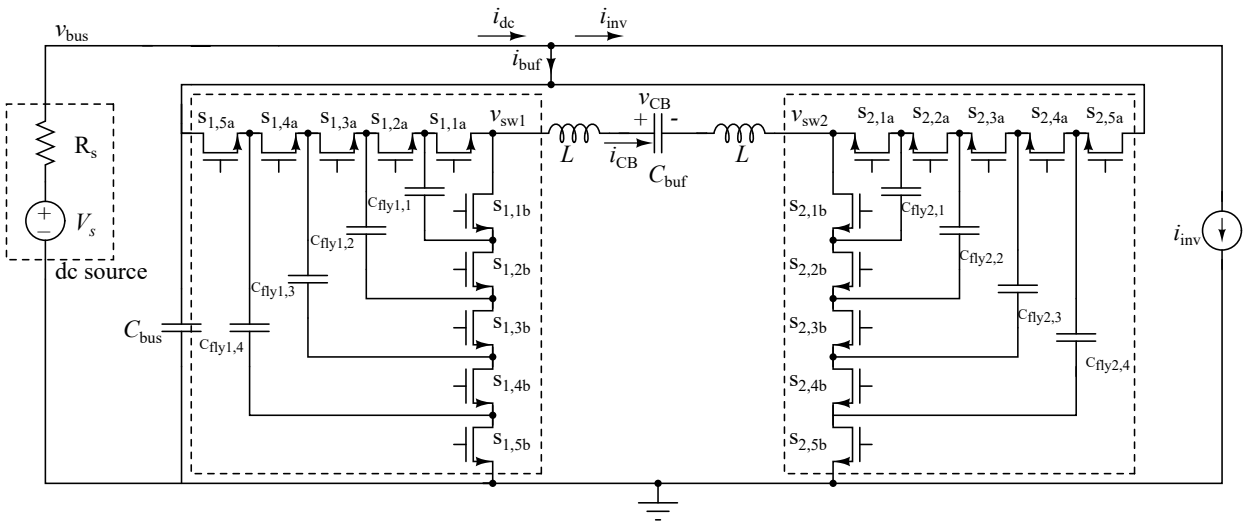

Figure 8.2: Schematic drawing of the bipolar active buffer implemented with two 6-level FCML converters.

concerns:

The first concern is that they are very sensitive to mechanical and thermal shocks, which could cause cracks inside the ceramic layers and lead to various electrical defects or failures [57]. Such properties of MLCC require advanced packaging process to ensure performance and limit the operating conditions and environment of the converter.

Another concern with common X6S, X7S MLCCs is that they do not have a constant capacitance. Instead, the capacitance depends on the voltage bias. As a result, if ideal sinusoidal voltages derived using constant capacitance for normal buffer operations were applied, the capacitor current would be strongly distorted, and so would be the power flowing through the capacitor [10], [58]. Consequently, unwanted harmonics will be present on the dc-side current. This is another reason why buffers implemented with MLCCs in [7] and [3] are operated with limited voltage swings and high dc biases such that the capacitance change within the operating voltage range is negligible and thus does not introduce extra harmonics in the system.

With the work in this chapter, we seek to overcome the limitations of the conventional bipolar ripple port converter by implementing the dc-ac buffer converter with two Flying Capacitor Multilevel (FCML) converters, as shown in Fig. 8.2. With FCML converters, the filter inductor size and the overall passive component volume are much reduced. The high efficiency and high power density characteristics of the FCML in various low to medium voltage applications have recently been demonstrated in [11], [52], [59]. Furthermore, in two-level active buffers, the filter inductors are so large that their reactive power have to be considered at the line frequency [7], [56], which complicates the calculation for ideal capacitor voltage. With much smaller inductors in the FCMLs, as can be demonstrated in this work,

the ideal capacitor voltage can be directly applied without considering the reactive power of the filter inductors.

For the buffer capacitor, different design targets and applications would prefer the use of film capacitor or MLCC over the other. For instance, film capacitors are preferred in more demanding operating conditions such as automotive applications, while MLCCs are more desirable to achieve high power density. As such, the use of both film capacitors and X6S MLCCs are explored and demonstrated with corresponding control techniques. Tradeoffs among different buffer designs such as volume, input current ripple, and loss distribution are discussed in details. The proposed buffer topology, control and modulation schemes are implemented and verified with a compact hardware prototype rated for 2 kW and 400 V dc-bus. The major contributions of this work are as follows:

- The first hardware demonstration of the bipolar ripple port implemented with FCMLs in full-bridge configuration.
- The tested condition of 2 kW at 400 Vdc is higher than any prior work on the bipolar ripple port with film capacitors as the buffer capacitor. A full voltage control scheme with regulation and harmonic compensation is proposed to minimize the harmonics in the capacitor voltage, thus in the dc-side current.
- The first hardware demonstration of using MLCCs as the buffer capacitor in a bipolar ripple port, with a high voltage swing that is close to the full dc-bus voltage. For X6S MLCCs tested in this work, a novel control technique is proposed to eliminate the harmonics in the MLCC's power by actively injecting voltage harmonics in the capacitor voltage, under very high voltage swings. The resulting low harmonic capacitor power is able to maintain a low ripple in the input dc current.
- With the MLCCs, the buffer capacitor volume is 3-4 times smaller than the state-of-the-art solutions designed for the same conversion specifications (Google LittleBox Challenge Specifications [1]: 2 kW, 400 V dc-bus, 20% dc current ripple).

The organization of this chapter is as follows: First, the operating principle of the bipolar full-ripple port is reviewed. Key equations that will be used in the controls are derived. Next, the buffer control and modulation schemes with different types of capacitors are discussed. The unique challenges with the MLCCs are addressed in detail. Finally, hardware design and experimental result of the 2 kW buffer prototype are presented.

8.2 Review of the Full Ripple Port Buffer

Ideal Operation of the bipolar active buffers

The single-phase conversion scenario with the bipolar active buffer is depicted in Fig. 8.1. The dc source is modeled as a voltage source V_s with a source resistance R_s. The single-phase inverter load on the dc-bus is modeled as a current load. For simplicity, the ac side

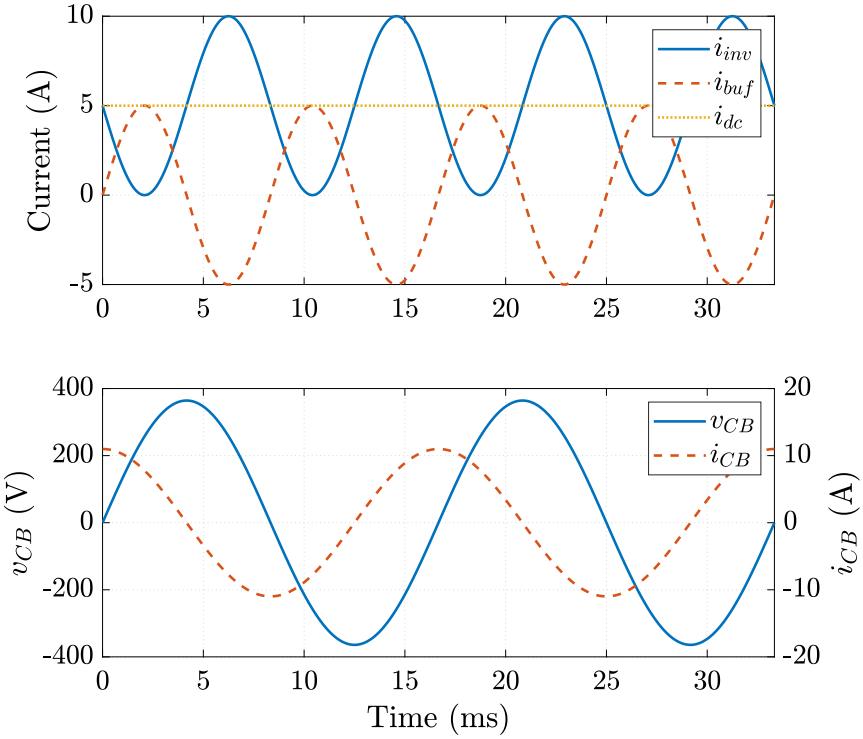

Figure 8.3: Ideal waveforms of the bipolar active buffer $V_{\mathrm{S}} = 450$ V, $i_{\mathrm{dc}} = 5$ A, $R_s = 10\ \omega$, $C_{\mathrm{buf}} = 80\ \mu F$.

of the inverter is considered with unity power factor in this work, but the proposed solution works equally well with non-unity power factor. With unity-power-factor inverter load, the inverter current can be found as

$$i_{\mathrm{inv}} = I_{\mathrm{dc}} - I_{\mathrm{dc}} \sin(2\omega_L t). \tag{8.1}$$

Note that the phase reference for the derivation is set as i_{inv} being $-\sin(2\omega_L t)$, the corresponding inverter ac output is thus in the phase of $\sin(\omega_L t - \frac{\pi}{4})$ or $\sin(-\omega_L t + \frac{\pi}{4})$ [56]. To cancel the twice-line frequency component in the inverter current, the buffer current has to be (8.2) such that $i_{\mathrm{buf}} + i_{\mathrm{inv}}$ is a dc constant.

$$i_{\mathrm{buf}} = I_{\mathrm{dc}} \sin(2\omega_L t). \tag{8.2}$$

For the buffer to draw such current, a line-frequency sinusoidal voltage has to be applied to the buffer capacitor C_{buf}. Using the power balancing relation of the buffer converter, the

differential equation using fundamental capacitor voltage/current relation can be found as

$$V_{\text{bus}} i_{\text{buf}} = v_{\text{CB}} i_{\text{CB}}$$
$$V_{\text{bus}} I_{\text{dc}} \sin(2\omega_L t) = C_{\text{buf}} v_{\text{CB}} \frac{\mathrm{d}v_{\text{CB}}}{\mathrm{d}t}. \tag{8.3}$$

Separating two variables and integrating both sides, we can obtain

$$V_{\text{bus}} I_{\text{dc}} \int \sin(2\omega_L t)\mathrm{d}t = C_{\text{buf}} \int v_{\text{CB}} \mathrm{d}v_{\text{CB}}$$
$$\frac{V_{\text{bus}} I_{\text{dc}}}{2\omega_L}(k - \cos(2\omega_L t)) = \frac{1}{2} C_{\text{buf}} v_{\text{CB}}^2 = E_{\text{Cbuf}}. \tag{8.4}$$

Since the capacitor energy E_{Cbuf} is always greater than zero, the constant k from the indefinite integral cannot be lower than one. If the capacitor voltage is discharged to zero after each twice line cycle, the EUR of the capacitor is 100%. In other words, by setting the initial energy $E_{\text{Cbuf}}(0) = 0$ in (8.4), $k = 1$ for the 100% EUR [56], which is true for the bipolar ripple port considered in this work. Assuming the buffer capacitance C_{buf} is constant, the solution to the differential equation with $k = 1$ is

$$v_{\text{CB}} = V_{\text{CB}} \sin(\omega_L t) = \sqrt{\frac{2V_{\text{bus}} I_{\text{dc}}}{\omega_L C_{\text{buf}}}} \sin(\omega_L t), \tag{8.5}$$

where V_{CB} is the magnitude. The ideal waveforms of i_{inv}, i_{buf}, i_{dc}, v_{CB} and i_{CB} are plotted in Fig. 8.3. From (8.5), we can also derive the minimum capacitance needed by setting $V_{\text{CB}} = V_{\text{bus}}$ as

$$C_{\text{buf, min}} = \frac{2P_0}{\omega_L V_{\text{bus}}^2}, \tag{8.6}$$

where P_0 is the single-phase system power $V_{\text{bus}} I_{\text{dc}}$, V_{bus} is the dc-bus voltage and ω_L is the line angular frequency.

8.3 Buffer Control with Film Capacitors as the Main Buffer Capacitor

If film capacitors were used as the buffer capacitor, the ideal voltage in (8.5) could be directly applied because of the constant capacitance. Thus, the goals for the buffer control scheme should be:

- Generate reference capacitor voltage based on (8.5) with correct frequency, phase, and magnitude to buffer the needed power in the overall dc-ac system.
- Regulate the output voltage of the dc-ac buffer converter (i.e., capacitor voltage v_{CB}) with low harmonics such that no unwanted harmonic contents are induced in the dc-side input current.

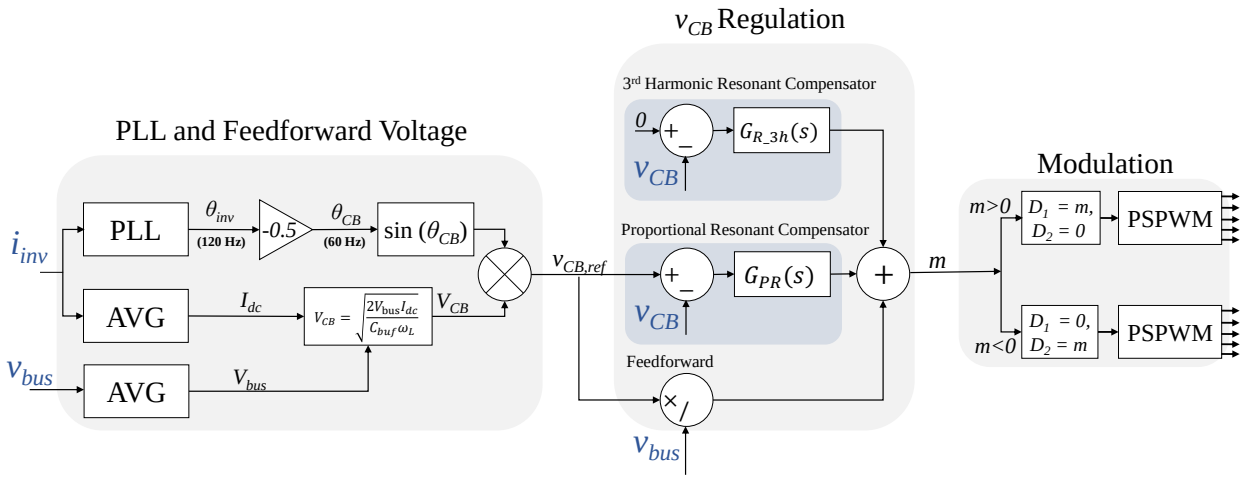

Figure 8.4: Control diagram of the proposed buffer control scheme for film capacitors. The sensed parameters are in blue font.

The full control scheme of the buffer converter with film capacitors is shown in Fig. 8.4. It comprises three main elements: generation of an ideal voltage reference for buffer capacitor voltage v_{CB}, regulation of v_{CB} and modulation, i.e., generation of the appropriate PSPWM signals.

Buffer capacitor voltage v_{CB} reference

To generate a low-harmonic and low-noise reference voltage for the buffer capacitor, a Phase-Locked Loop (PLL) based control is implemented as shown in Fig. 8.4 [60]. From (8.1) and (8.5), the angular relation between the inverter current and buffer voltage can be determined. If the angle of the ac portion of the inverter current is $\theta_{\mathrm{inv}} = -2\omega_L t$, the angle for the buffer capacitor voltage is then $\theta_{\mathrm{CB}} = \omega_L t = -0.5\theta_{\mathrm{inv}}$. In other applications where the buffer control is integrated with the main inverter or PFC control [52], [61], the angle can also be obtained from the main ac voltage.

The inverter current i_{inv} is sensed, and a PLL based on digital notch filters is designed to detect the angle θ_{inv}. Once θ_{CB} is calculated from θ_{inv}, the magnitude V_{CB} can be calculated based on (8.5). To do so, the average dc current I_{dc} is obtained by averaging i_{inv}, and the dc-bus voltage V_{bus} is also sensed and calculated. C_{buf} and ω_L are known parameters to the system. The square-root function in the DSP controller can then be used to calculate V_{CB}.

Regulation of v_{CB}

In the ideal case, v_{CB} can be generated by feed-forwarding the calculated reference using (8.5). However, as the voltage and current swings on the buffer capacitor become larger as

the load increases, the actual $v_{\rm CB}$ will be distorted, which means the capacitor power is also distorted. As can be seen from the power balancing relation in (8.3), any distortion on the capacitor power will result in discrepancy between the actual $i_{\rm buf}$ and the ideal buffer current $I_{\rm dc}\sin(2\omega_L t)$, which means the ripple component in $i_{\rm inv}$ will not be perfectly canceled. As a result, there will be unwanted ripple component in the dc-side current as

$$\begin{aligned} i_{\rm dc} &= i_{\rm inv} + i_{\rm buf} \\ &= I_{\rm dc} - I_{\rm dc}\sin(2\omega_L t) + i_{\rm buf} \\ &= I_{\rm dc} - I_{\rm dc}\sin(2\omega_L t) + \frac{v_{\rm CB} i_{\rm CB}}{V_{\rm bus}} \end{aligned} \tag{8.7}$$

Since the peak-to-peak ripple of the dc-side current is usually restricted to a certain limit (e.g., $\leq 20\%$ of the dc average current) for many practical applications [1], it is necessary to regulate $v_{\rm CB}$. To obtain a low-harmonic $v_{\rm CB}$, a regulation scheme with feedforward, a Proportional-Resonant (PR) compensator $G_{\rm PR}$ at the fundamental 60 Hz frequency, and a resonant compensator at 180 Hz (third harmonic) $G_{\rm R\_3h}$ is implemented [62]. The transfer function for the $G_{\rm PR}$ is

$$G_{\rm PR}(s) = K_P + K_{i1}\frac{s}{s^2+\omega_L^2}, \tag{8.8}$$

and the transfer function for 3rd harmonic resonant compensator is

$$G_{\rm R\_3h}(s) = K_{i3}\frac{s}{s^2+(3\omega_L)^2}, \tag{8.9}$$

where K_P is the proportional gain, and K_{i1} and K_{i3} are the gains for resonant compensators at the fundamental line frequency (60 Hz) and the 3rd harmonic (180 Hz). As will be presented in the experiment results, 3rd harmonic resonant compensator is essential to maintain low harmonics in the dc-side current.

8.4 Challenges of Using Nonlinear Ceramic Capacitors as the Main Buffer Capacitors

To study the voltage and current behavior of non-linear ceramic capacitors, two capacitors with different characterstics, the **TDK C5750X6S** X6S MLCC and **TDK Ceralink FA** PLZT ceramic capacitor are used as design examples. Key parameters of the two tested capacitors are given in Table 8.1 (Note that the Ceralink Flex-Assembly (FA) series are constructed with single ceramic capacitor, and they are only offered with assembly of two (FA2), three (FA3), and ten (FA10)). To fairly compare with X6S capacitors, all the data and parameters in this work for FA series are for the single PLZT ceramic capacitor). The capacitance v.s. bias voltage curves of TDK C5750X6S and Ceralink FA are shown in Fig. 8.5 and Fig. 8.6. As can been seen, the capacitance of TDK C5750X6S decreases with the

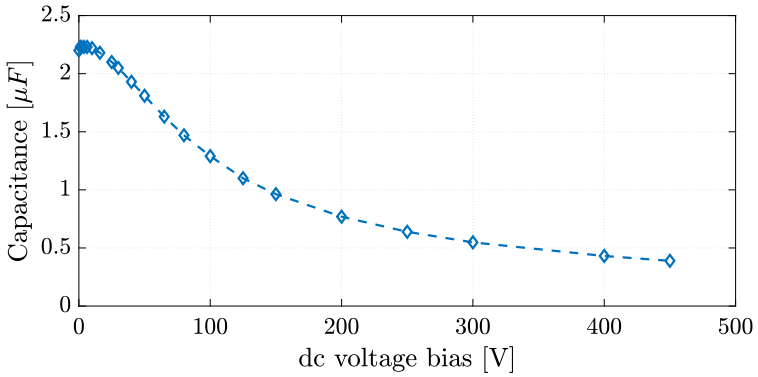

Figure 8.5: Capacitance v.s. voltage bias curve of TDK C5750X6S.

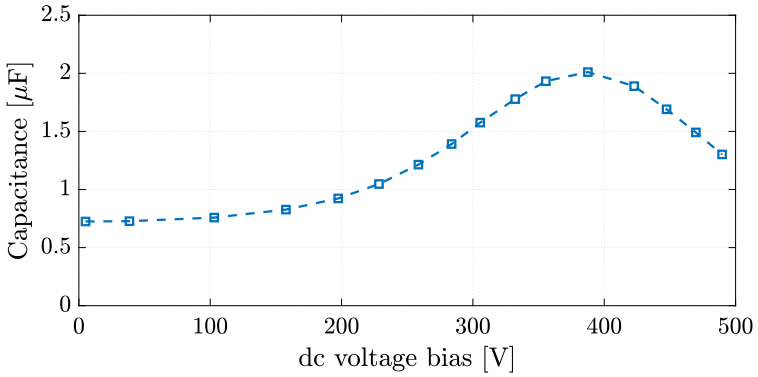

Figure 8.6: Capacitance v.s. voltage bias curve of Ceralink capacitor.

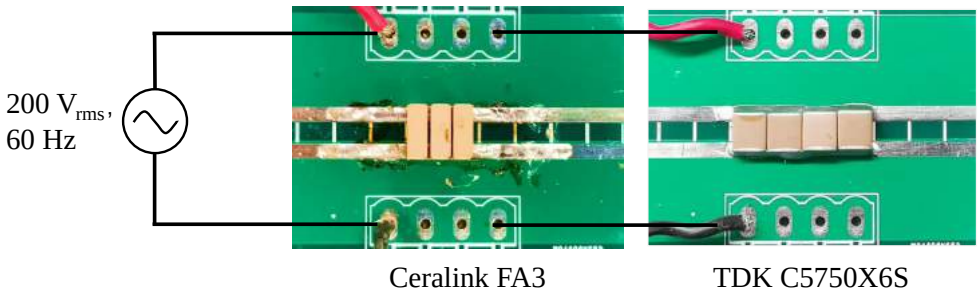

Figure 8.7: Applying ac voltage to test nonlinear behavior of both Ceralink and X6S capacitors.

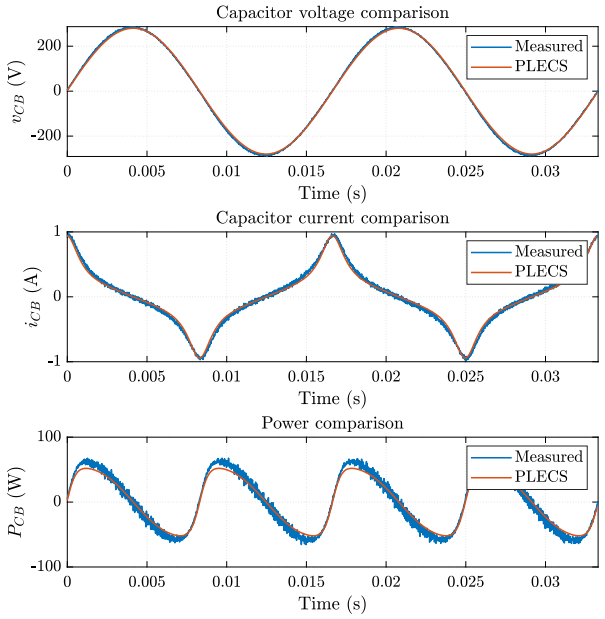

Figure 8.8: Experimental and simulated wavef orms of four **TDK C5750X6S** under $v_{\mathrm{CB}} = 280\sin(\omega_L t)$ V

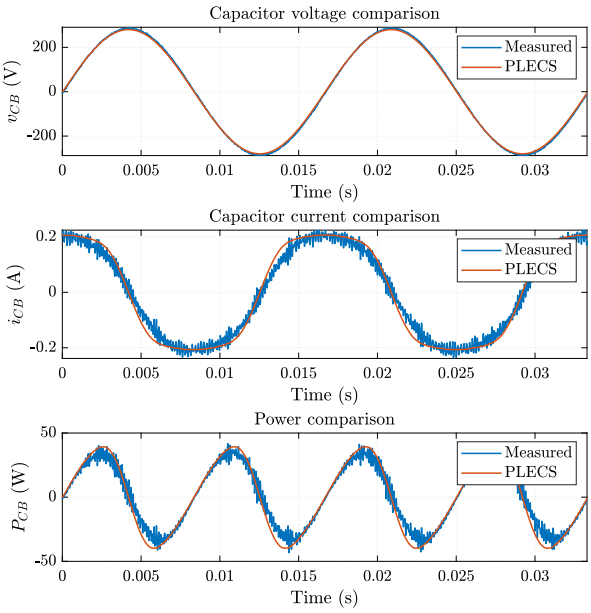

Figure 8.9: Experimental and simulated waveforms of three **Ceralink** capacitors (FA3) under $v_{\mathrm{CB}} = 280\sin(\omega_L t)$ V

Table 8.1: Parameters of tested capacitors

Parameters	TDK C5750X6S	Ceralink FA
Voltage rating	450 V	500 V
Volume	7.1 cm^3	16.8 cm^3
C @ 0 V	2.2 μF	0.6 μF
C @ 400 V	0.47 μF	1.9 μF

voltage bias, while the capacitance of Ceralink FA increases with the voltage bias. To study the capacitor voltage and current relation with varying capacitance, four TDK C5750X6S capacitors in parallel and one Ceralink FA3 (three single capacitors in parallel) are tested with 200 $\mathrm{V_{rms}}$, 60 Hz pure sinusoidal voltage, which has sufficiently high voltage swings to introduce significant capacitance changes, as shown in Fig. 8.7. In order to build appropriate control scheme for buffer application, voltage-dependent variable capacitor models based on $C-V$ curves in Fig. 8.5 and Fig. 8.6 are implemented in the simulation software PLECS. The experimental and simulated results are plotted and compared in Fig. 8.8 for TDK C5750X6S, and Fig. 8.9 for the Ceralink FA3. As can be observed, the simulated capacitor current in

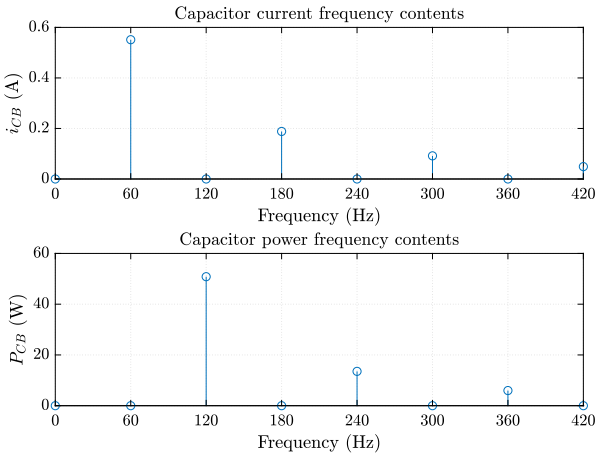

Figure 8.10: Harmonic contents of the **TDK C5750X6S** current and power.

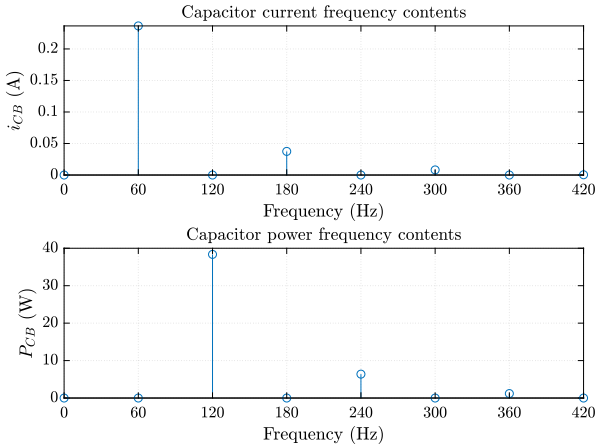

Figure 8.11: Harmonic contents of the **Ceralink** capacitor current and power.

PLECS match the actual capacitor current well. Moreover, the current and power of both capacitors contain significant harmonic distortion.

The harmonic contents of the current and power are plotted in Fig. 8.10 and Fig. 8.11, for TDK C5750X6S and Ceralink FA3 respectively. It can be seen that while the capacitor current waveforms are different for TDK C5750X6S and Ceralink FA3, they both contain only odd harmonics (3rd, 5th...), while the resulting capacitor powers contain even harmonics of 60 Hz (4th, 6th...). By further analyzing the phases of the harmonics using `fft` in Matlab, the major difference between TDK C5750X6S and Ceralink FA3 is the phase of the third harmonic, which is also the strongest harmonic. As can be seen from the `fft` phase results in Fig. 8.12 and Fig. 8.13, the phase of the third harmonic for TDK C5750X6S is zero, while the phase of the third harmonic for Ceralink FA3 is π.

In the bipolar active buffer application of Fig. 8.1, if TDK C5750X6S or Ceralink capacitors are used as the buffer capacitors, the resulting capacitor power will contain even harmonics if the pure sinusoidal voltage in (8.5) is applied. From the buffer power balancing relation in (8.3), the even harmonics in the capacitor power will introduce even harmonics in the buffer current i_{buf}, which will be seen in the dc-side current or the dc-bus voltage. In other applications where the ceramic capacitors are applied with sinusoidal line voltages, such as the ac line voltage filters for three-phase inverters [63], the non-linear behavior will also introduce unwanted harmonic contents in the displacement ac current.

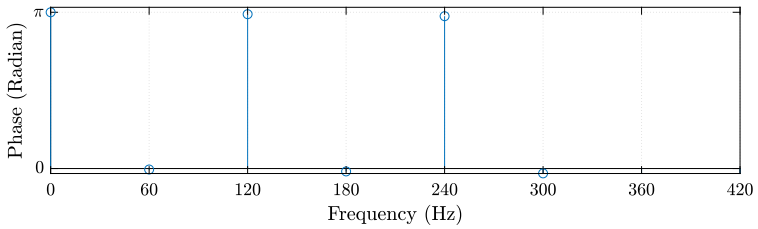

Figure 8.12: The phases of the harmonic contents of the **TDK C5750X6S** capacitor current.

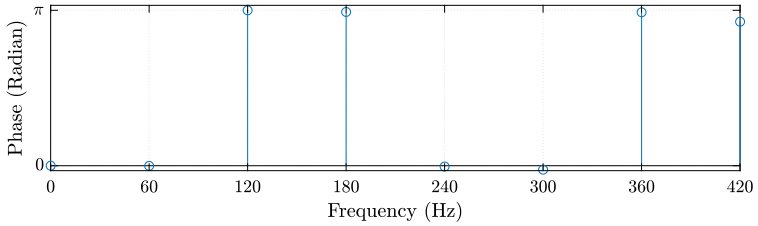

Figure 8.13: The phases of the harmonic contents of the **Ceralink** capacitor current.

8.5 Buffer Control with MLCCs as the Main Buffer Capacitor

The ultimate goal of the control for the buffer is to suppress ripple components in the dc-side current. To do so, the buffer power has to match the ripple portion of the inverter power. As discussed in Section 8.4, non-linear ceramic capacitors cannot be the direct replacement of linear film capacitors with the same control, as they will introduce unwanted power harmonics. Intuitively, if the capacitance of the MLCCs is the function of the voltage bias, by incorporating a voltage-dependent capacitance function $C(V)$ into the differential equation (8.3), an explicit voltage expression in time domain can be solved for MLCCs similar to (8.5). However, this approach first requires a good curve fitting to find an expression for the $C-V$ curve in Fig. 8.5. As the derating curve is non-linear, higher order terms are needed for more accurate modeling, which will make the differential equation (8.3) much more difficult to solve and the final result much more complicated than constant capacitance. Moreover, the fitting parameters will vary for individual MLCCs. As such, it is not realistic nor effective to first derive an ideal buffer voltage expression with voltage-dependent capacitance and to directly apply such voltage in the control. In this work, utilizing the harmonic analysis in Fig. 8.10, instead of trying to solve for the correct capacitor voltage in time domain, a control scheme is proposed such that the buffer capacitor voltage is reconstructed and controlled in frequency domain.

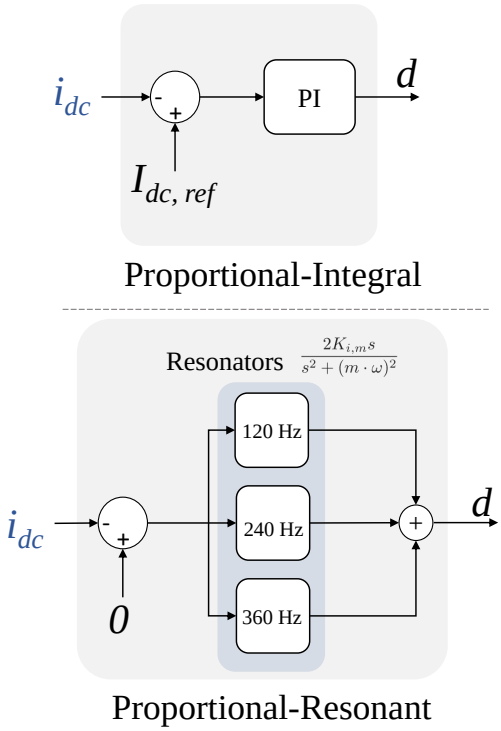

Figure 8.14: Linear PI and PR controller to directly regulate input dc current.

How injecting odd voltage harmonics can eliminate even power harmonics

To eliminate the even harmonics in the power of non-linear capacitors, odd voltage harmonics with proper phase and magnitude need to be injected to the capacitor voltage. To mathematically show this, the current harmonic content is simplified to contain only the third harmonic, as it is the strongest harmonic. Moreover, the voltage and current are normalized for the ease of calculation.

With the original sinusoidal capacitor voltage being normalized to $\sin(\omega_L t)$, the corresponding normalized capacitor current with third harmonic is

$$i_{\text{cap, norm}} = \cos(\omega_L t) + I_{3\text{rd}} \cos(3\omega_L t) \tag{8.10}$$

where $I_{3\text{rd}}$ is positive for TDK C5750, and negative for Ceralink FA as discussed in Section 8.3. The corresponding power is thus

$$\begin{aligned} P_{\text{cap}} &= v_{\text{cap}} i_{\text{cap, norm}} \\ &= \sin(\omega_L t)(\cos(\omega_L t) + I_{3\text{rd}} \cos(3\omega_L t)) \\ &= \frac{1}{2}((1 - I_{3\text{rd}}) \sin(2\omega_L t) + I_{3\text{rd}} \sin(4\omega_L t)) \end{aligned} \tag{8.11}$$

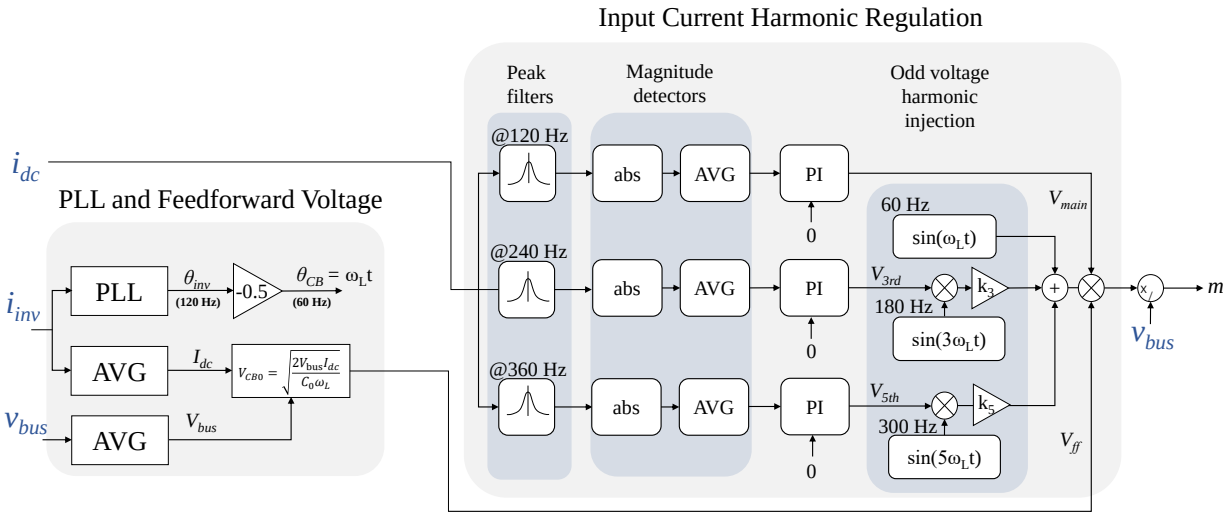

Figure 8.15: Control diagram of the proposed buffer control scheme with harmonic injection.

As expected, the power contains fourth harmonic content. Moreover, the desired twice-line frequency power is also influenced by the current harmonic with $(1 - I_{3\text{rd}})$.

If we inject the third harmonic voltage, the new capacitor voltage is

$$v_{\text{cap, inject}} = \sin(\omega_L t) + V_{3\text{rd}} \sin(3\omega_L t) \tag{8.12}$$

While in reality the newly injected third harmonic voltage will induce higher order harmonics, since its magnitude is far smaller than the fundamental voltage, the impact of higher order harmonics is negligible. Thus, ignoring higer order terms, the updated power can be approximated as:

$$\begin{aligned} P_{\text{cap, inject}} &= v_{\text{cap, inject}} i_{\text{cap, norm}} \\ &= (\sin(\omega_L t) + V_{3\text{rd}} \sin(3\omega_L t)) \times \\ &(\cos(\omega_L t) + I_{3\text{rd}} \cos(3\omega_L t)) \\ &= \frac{1}{2}((1 - I_{3\text{rd}} + V_{3\text{rd}}) \sin(2\omega_L t) + \\ &(I_{3\text{rd}} + V_{3\text{rd}}) \sin(4\omega_L t) + \\ &V_{3\text{rd}} I_{3\text{rd}} \sin(6\omega_L t)) \end{aligned} \tag{8.13}$$

Note that since the voltage and current are both normalized, the parameter $|I_{3\text{rd}}|$ and $|V_{3\text{rd}}|$ are both much smaller than one. As such, the sixth harmonic power can be ignored in the following analysis.

As can be seen in (8.13), the magnitude of the fourth power harmonic is $(I_{3\text{rd}} + V_{3\text{rd}})$. To eliminate this term, the value of the required injected voltage magnitude is straightforward to

obtain:$V_{3\text{rd}} = -I_{3\text{rd}}$, which means that for TDK C5750X6S $V_{3\text{rd}}$ is negative, and for Ceralink FA3 $V_{3\text{rd}}$ is positive.

From a control system point of view, the variable to regulate, the ripple in i_{dc}, and the final control effort $v_{\text{cap, inject}}$ are at different frequencies. Thus, a feedback system to eliminate the ripple components in i_{dc} cannot be realized with only linear compensators such as Proportional-Integral (PI) or Proportional-Resonant (PR) controllers [7], [64] in Fig. 8.14, as they do not change the frequencies between the input and output signals. For instance, since the ripple in i_{dc} and v_{dc} are directly proportional to the capacitor power harmonics, they will only contain even harmonic contents. Moreover, since their references are dc constants, the error terms from sensing i_{dc} or v_{dc} contain only even harmonics as well. As a result, the output d from the linear compensators will also contain only even harmonics. Injecting even-harmonic voltage not only cannot eliminate the even harmonics in the capacitor power, but also introduces harmonics at other frequencies. Assuming a fourth harmonic voltage is added to the capacitor voltage, using similar calculation as (8.13), the power harmonics can be obtained as:

$$\begin{aligned} P_{\text{cap, 4th}} &= v_{\text{cap, inject}} i_{\text{cap, norm}} \\ &= (\sin(\omega_L t) + V_{4\text{th}} \sin(4\omega_L t)) \times \\ &(\cos(\omega_L t) + I_{3\text{rd}} \cos(3\omega_L t)) \\ &= \frac{1}{2}(V_{4\text{th}} I_{3\text{rd}} \sin(\omega_L t) + (1 - I_{3\text{rd}}) \sin(2\omega_L t) \\ &+ V_{4\text{th}} \sin(3\omega_L t) + I_{3\text{rd}} \sin(4\omega_L t) \\ &+ V_{4\text{th}} \sin(5\omega_L t)) + V_{4\text{th}} I_{3\text{rd}} \sin(7\omega_L t)) \end{aligned} \tag{8.14}$$

As can be seen, not only the original fourth harmonic power in (8.11) cannot be cancelled with the injected fourth harmonic voltage, there are newly induced power harmonics at the fundamental, third, fifth and seventh .

Proposed voltage harmonic injection method

To overcome the limitation of linear controllers, the control scheme in Fig. 8.15 is proposed. Parameters i_{inv} and v_{bus} are sensed to generate the phase reference and provide system load information. Parameter i_{dc} is sensed and the ripple harmonics are regulated. First, the harmonic contents at 120 Hz, 240 Hz, and 360 Hz in i_{dc} are obtained with three peak filters at corresponding frequencies shown in Fig. 8.16. Next, the magnitude of each harmonic content is calculated using moving average filters. By separating the harmonic magnitudes, PI controllers with zero reference can be used to regulate each harmonic content to zero. The outputs from PI controllers for 240 Hz and 360 Hz $V_{3\text{rd}}$ and $V_{5\text{th}}$ are multiplied with the sinusoidal reference voltages of the 3rd and 5th voltage harmonics. The output of PI controller for 120 Hz ripple V_{main} scales the overall voltage magnitude to cancel any mismatch in the main twice-line frequency power. To improve the transient performance, a feedforward voltage V_{ff} that scales with the inverter load current is calculated using the capacitance at

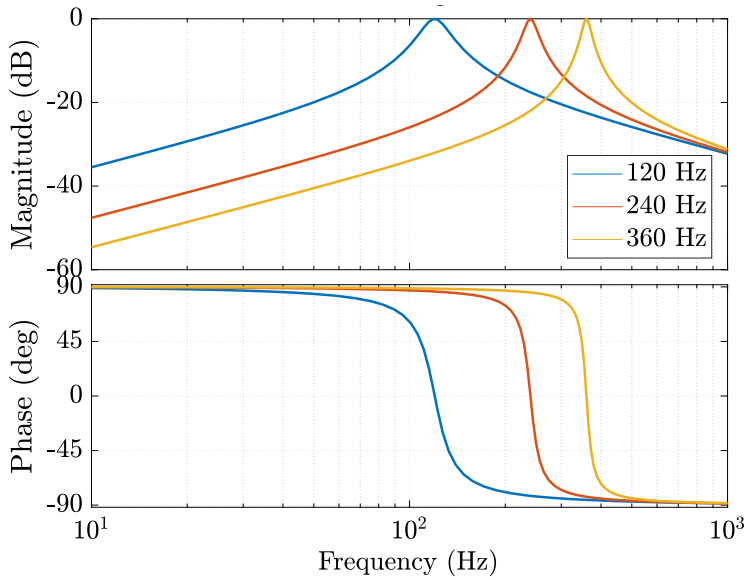

Figure 8.16: Bode plots of three peak filters with center frequencies at 120 Hz, 240 Hz and 360 Hz.

zero voltage bias (the calculation of V_{ff} does not have to be very accurate). Finally, to account for the use of both Ceralink FA and C5750X6S capacitors as the buffer capacitor, the third harmonic voltage is scaled with a constant gain k_3. As shown in (8.13), to cancel the fourth harmonic power ripple, $k_3 = -1$ for C5750X6S, and $k_3 = 1$ for Ceralink FA. k_5 is set to -1 for both capacitors. The final expression for the capacitor voltage is thus

$$v_{\text{CB, X6S}} = V_{\text{ff}} V_{\text{main}} (\sin(\omega_L t) + k_3 V_{\text{3rd}} \sin(3\omega_L t) + k_5 V_{\text{5th}} \sin(5\omega_L t)). \tag{8.15}$$

With the proposed control, the conversion scenario for 400 V dc-bus and 1 kW dc power is simulated in PLECS with both capacitors: with one hundred parallel-connected TDK C5750X6S, and one hundred parallel-connected single Ceralink FA capacitors. The simulated waveforms and frequency contents with TDK C5750X6S are plotted in Fig. 8.17 and Fig. 8.18, and the simulated results with Ceralink FA are plotted in Fig. 8.19 and Fig. 8.20.

As shown in the spectrum plot in Fig. 8.18 and Fig. 8.20, the controller is able to determine the correct magnitude and phase for the odd voltage harmonics to be injected into the capacitor voltage. As a result, with both types of non-linear ceramic capacitors, the capacitor powers have no even harmonic content except for the 120 Hz content for twice-line frequency power buffering.

The transient behavior of the power harmonic elimination control is also simulated in PLECS for a load step from 2 kW to 1 kW system power in Fig. 8.21 for the TDK C5750X6S. And the voltage magnitude commands for the fundamental, 3rd and 5th harmonic contents are shown in Fig 8.22. As can be seen in both figures, the controller is able to adjust the

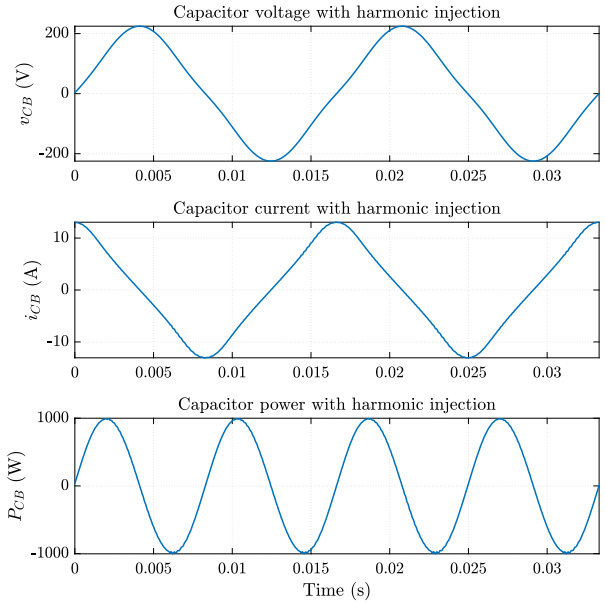

Figure 8.17: Simulated waveform for single-phase buffering scenario with 1 kW system power and 400 V dc-bus using TDK C5750 X6S capacitors as the buffer capacitor.

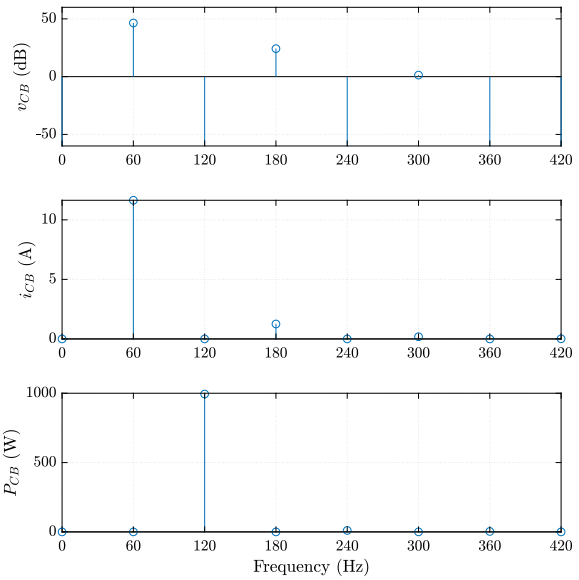

Figure 8.18: Harmonic contents of the capacitor voltage, current and power with the proposed control using TDK C5750 X6S capacitors.

magnitudes of the fundamental and odd harmonic voltages to suppress the ripple term in the dc input current to zero within a few line cycles after the load step. More optimization on the PI parameters can be done to improve the dynamic performance.

8.6 Modulation Scheme for the two FCML Legs

Once the reference of v_{CB} is determined from the active decoupling control in Fig. 8.4 or Fig. 8.15, the two FCML legs have to be modulated with D_1 and D_2 to generate the correct differential conversion ratio m. However, for a given m, there are infinite combinations of $D_1 - D_2$ as well as phase relations that can produce the correct m. Thus, it is necessary to determine the modulation scheme that results in the lowest loss and smallest passive component sizes. In this work, two modulation schemes are evaluated and compared.

Unipolar PSPWM scheme

In a conventional two-level full-bridge inverter, there are two common modulation schemes: bipolar and unipolar modulation. Detailed operations of bipolar and unipolar modulation are given in [65]. While bipolar modulation requires fewer switching signals, unipolar modu-

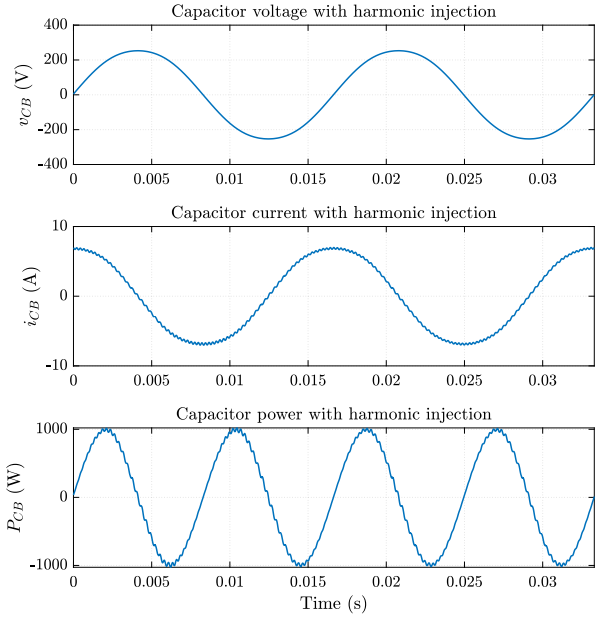

Figure 8.19: Simulated waveform for single-phase buffering scenario with 1 kW system power and 400 V dc-bus using Ceralink capacitors as the buffer capacitor.

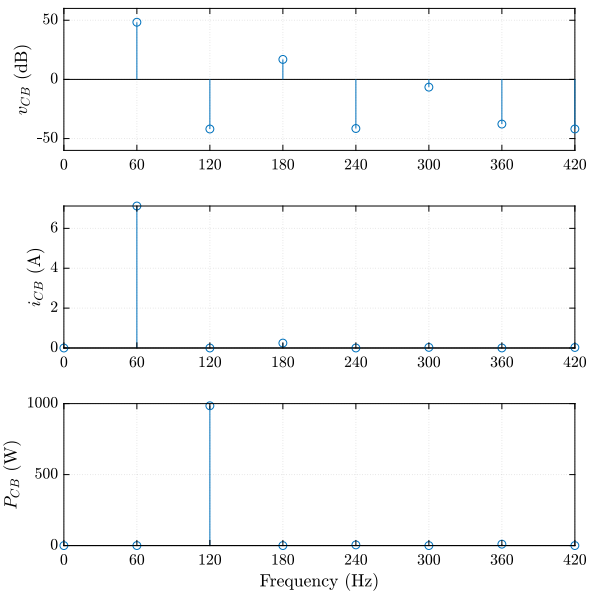

Figure 8.20: Harmonic contents of the capacitor voltage, current and power with the proposed control using Ceralink capacitors.

lation has certain advantages over bipolar such as low inductor ripple current, low dv/dt on switching node, low switch voltage stress etc. [65] Thus, in this work, we investigated the use of unipolar modulation with the two FCML legs. Two half-bridge FCML legs are modulated with duty ratio D and $1-D$ respectively, and differential conversion ratio $m = 2D-1$. The PWM signals for two half-bridge legs are aligned to the symmetrical center of the waveform. Consequently, the frequency of the voltage across the inductor is twice of the switching frequency. Thus, the inductor ripple is reduced and smaller inductor can be used, compared to bipolar modulation. For the two FCML legs considered here, as long as the PWM signals controlling the switches in identical positions ($s_{1,1a}$ and $s_{2,1a}$, $s_{1,2a}$ and $s_{2,2a}$ and so on) in two FCMLs are in the unipolar configuration shown in Fig. 8.23, the frequency of the inductor current ripple is also doubled. In a single FCML, with PSPWM, the frequency of the inductor current ripple is already $(N-1)$ times of the switching frequency. If two FCML legs are modulated with unipolar scheme, the inductor current ripple is $2(N-1)$ times of the switching frequency. As a result, compared to a single FCML, the inductor size can be further reduced given the same switching frequency, or the switching frequency can be halved if the inductance remains the same.

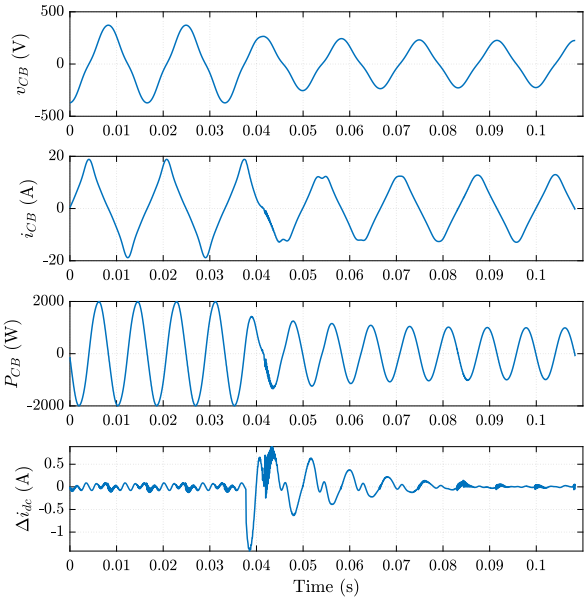

Figure 8.21: MLCC buffer capacitor voltage, current, power and corresponding dc-side current ripple during a load step from 2 kW to 1 kW dc power.

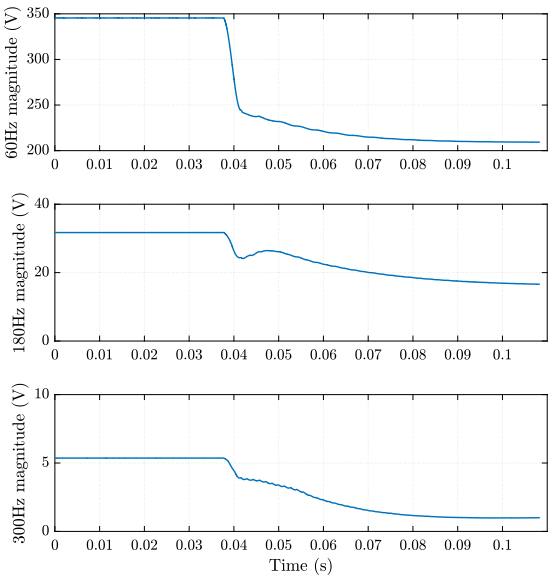

Figure 8.22: Capacitor voltage magnitudes of each frequency contents during a load step from 2 kW to 1 kW dc power.

Leg-alternating scheme

The other modulation strategy evaluated in this work is shown in Fig. 8.24. Essentially, one leg is shorted to ground while the other leg modulates, alternating each half cycle. Since each leg is turned off for half a cycle, the total loss of the buffer converter is almost equivalent to half-bridge configuration (with only additional minor conduction loss of the low-side FETs on the FCML leg shorted to ground). As only one FCML leg is modulating at a time, the inductor current ripple frequency is $(N-1)$ times of the switching frequency.

Comparison of two modulation schemes

The discrepancy in losses between the two modulation strategies can be understood by analyzing the average power processed by one FCML leg within one line cycle.

In the leg-alternating case, the average power processed by one FCML leg is relatively straightforward to calculate. Each FCML is turned on for only one half line cycle. The average processed power of one FCML is simply obtained by dividing the total energy processed

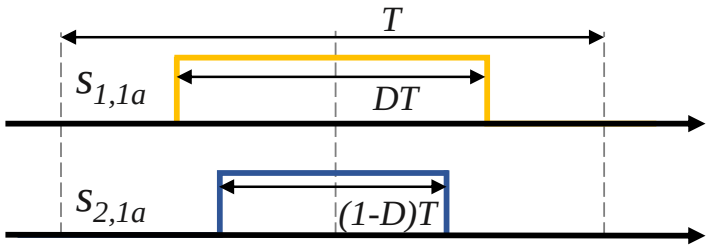

Figure 8.23: Exemplar unipolar PWM signals for $s_{1,1a}$ and $s_{2,a}$, with switching period T. $s_{1,1a}$ operates with duty ratio D, and $s_{2,1a}$ operates with complimentary duty $1-D$. The center of the two signals are aligned.

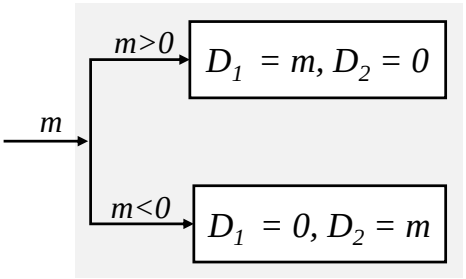

Figure 8.24: Leg-alternating modulation scheme.

in one half line cycle period $T_{\mathrm{L}}/2$ over one line period T_L as

$$\begin{aligned} P_{\mathrm{FCML,\ la}} &= \frac{E_{\mathrm{tot,\ la}}}{T_L} = \frac{\int_0^{T_L/2} |V_{\mathrm{bus}} i_{\mathrm{buf}}|}{T_L} \\ &= \frac{\int_0^{T_L/2} |P_0 \sin(2\omega_L t)|}{T_L} \\ &= \frac{P_0}{\pi} \end{aligned} \tag{8.16}$$

The average power processed by one FCML with the unipolar modulation can be calculated by analyzing the power delivered out from port v_1 in Fig. 8.25. The instantaneous power at terminal v_1 can be calculated as

$$p_{\mathrm{FCML,\ uni}} = v_1 i_{\mathrm{CB}} = D V_{\mathrm{bus}} i_{\mathrm{CB}}. \tag{8.17}$$

Since the differential conversion ratio $m = 2D - 1 = \frac{v_{\mathrm{CB}}}{V_{\mathrm{bus}}}$, (8.17) can be written as

$$\begin{aligned} p_{\mathrm{FCML,\ uni}} &= \frac{1+m}{2} V_{\mathrm{bus}} i_{\mathrm{CB}} \\ &= \frac{V_{\mathrm{bus}} + v_{\mathrm{CB}}}{2} i_{\mathrm{CB}}. \end{aligned} \tag{8.18}$$

since $i_{\text{CB}} = C_{\text{buf}}\frac{dv_{\text{CB}}}{dt}$ and $v_{\text{CB}}i_{\text{CB}} = V_{\text{bus}}i_{\text{buf}} = P_0\sin(2\omega_L t)$, substituting in (8.5), (8.18) can be further derived to be

$$\begin{aligned} p_{\text{FCML, uni}} &= \frac{V_{\text{bus}}i_{\text{CB}}}{2} + \frac{P_0\sin(2\omega_L t)}{2} \\ &= \frac{V_{\text{bus}}C_{\text{buf}}\omega_L V_{\text{CB}}\cos(\omega_L t)}{2} + \frac{P_0\sin(2\omega_L t)}{2} \\ &= \frac{V_{\text{bus}}\sqrt{2P_0\omega_L C_{\text{buf}}}\ \cos(\omega_L t)}{2} + \frac{P_0\sin(2\omega_L t)}{2}. \end{aligned} \tag{8.19}$$

The average power processed in one line cycle can then be calculated

$$\begin{aligned} P_{\text{FCML, uni}} &= \frac{\int_0^{T_L}|p_{\text{FCML, uni}}|}{T_L} \\ &= \frac{V_{\text{bus}}\sqrt{2P_0\omega_L C_{\text{buf}}}}{\pi}. \end{aligned} \tag{8.20}$$

To compare the average processed power of two modulation schemes, the ratio $\frac{P_{\text{FCML, uni}}}{P_{\text{FCML, la}}}$ is derived as

$$\frac{P_{\text{FCML, uni}}}{P_{\text{FCML, la}}} = \frac{V_{\text{bus}}\sqrt{2\omega_L C_{\text{buf}}}}{\sqrt{P_0}}, \tag{8.21}$$

which is plotted against the dc-side current i_{dc} in Fig. 8.26. It can be observed that as the load power increases, the ratio becomes lower. Moreover, the minimum of the ratio can also be derived based on the constraint $m \leq 1$, i.e., $V_{\text{CB}} \leq V_{\text{bus}}$. Deriving from (8.5), the allowed range of P_0 is found as

$$P_0 \leq \frac{\omega_L C_{\text{buf}}V_{\text{bus}}^2}{2}. \tag{8.22}$$

Correspondingly, the minimum of the ratio $\frac{P_{\text{FCML, uni}}}{P_{\text{FCML, la}}}$ is 2. As such, leg-alternating modulation scheme is utilized in the final implementation for its lower processed power.

8.7 Design and Implementation of the Full-Bridge FCML Converter

FCML component sizing

The dc-ac converter in the buffer is implemented with two 6-level FCMLs in a full-bridge configuration. For FCMLs, it is critical for the flying capacitor voltages to maintain close to the ideal balanced voltage levels to avoid high voltage stress on the switches and extra switching harmonics. While active balancing techniques are more robust [66], [67], they require additional sensing and computing capabilities. As such, in this work, the FCMLs

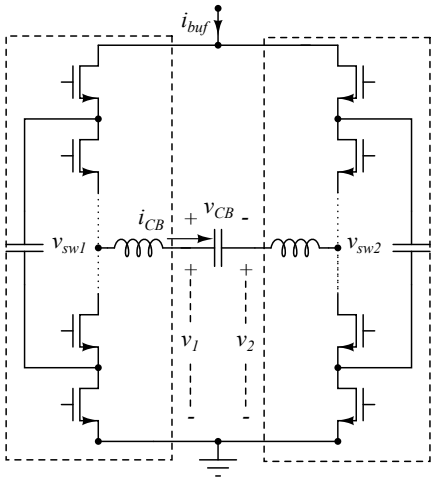

Figure 8.25: Terminal voltage v_1 and v_2 are defined to calculate the power processed by each FCML leg.

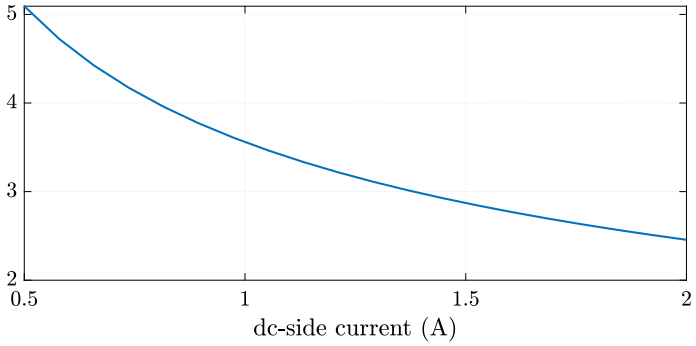

Figure 8.26: Calculated ratio of $\frac{P_{\text{FCML, uni}}}{P_{\text{FCML, la}}}$ vs. dc-side current.

rely on the strong natural balancing strength of the even-level FCMLs to maintain good voltage balancing [68], as will be seen in the experiment results. It should be noted that this work demonstrates strong natural balancing for simplicity, and the proposed control technique is fully compatible with active balancing, should one wish to use such methods. More detailed operation and sizing of passive components for the FCML can be found in [9], [39], [59], [69], [70]. Yet, there are a few specifications that are worth-noting for this particular application.

Unlike the FCML inverters tested in [11], [59], the output voltage and current of the buffer dc-ac converter are 90° out of phase, and contain high-order harmonics with the MLCCs. As such, the inductor current ripple and flying capacitor voltage ripple have to be specifically calculated in one line cycle with the buffer voltage and current to determine the ratings for the inductor, capacitors and switches.

With the equations in [59], [70], the calculated inductor current ripple Δi_{L} and flying capacitor voltage ripple (peak-to-average) Δv_{cfly} with 150 kHz switching frequency and 3 μF flying capacitor, and 13.6 μH inductor are plotted in Fig. 8.27. The voltage stress seen by each switch is

$$v_{\text{sw, rating}} = V_{\text{nom}} + \Delta v_{\text{cfly}}, \tag{8.23}$$

where V_{nom} is the nominal flying capacitor voltage $\frac{V_{\text{bus}}}{5} = 80$ V for the 6-level FCML. Therefore, the peak switch voltage stress is 87 V for this design. The top envelope of the inductor current is

$$i_{\text{L, top}} = i_{\text{CB}} + 0.5\Delta i_{\text{L}}, \tag{8.24}$$

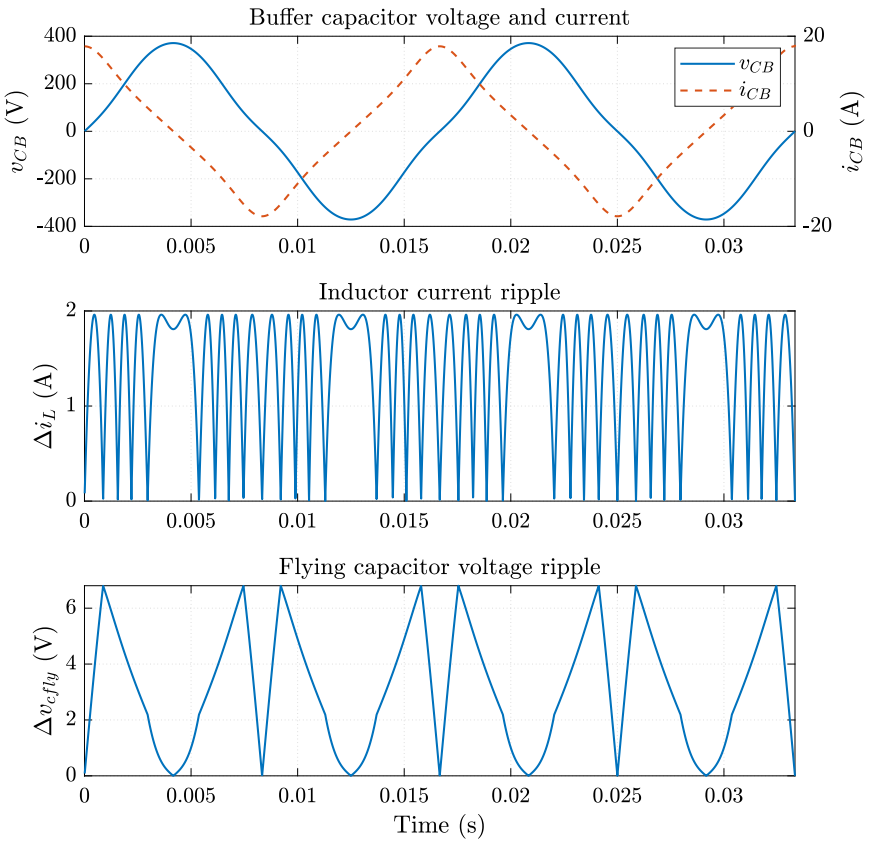

Figure 8.27: Calculated inductor current ripple and flying capacitor voltage ripple in two line cycles with MLCC buffer capacitor for 2 kW, 400 V dc-bus.

whose maximum is the peak inductor current in one line cycle. The saturation limit of the inductor current rating is thus calculated to be 18.4 A.

Hardware Implementation

The dc-ac full-bridge FCML converter in the buffer is implemented with two 6-level FCML modules in Fig. 6.17. The full buffer hardware prototype is constructed with two FCML modules mounted on a control and sensing board as shown in Fig. 8.28. Two LT1999 current amplifiers are to sense i_{dc} and i_{inv} with 5 mΩ shunt resistors The proposed control scheme and all the PWM signals are digitally implemented in the Texas Instruments C2000 Delfino DSP. The output terminals for v_{CB} are connected to the buffer capacitor. For the buffer capacitor, the film capacitors tested in this work are two 450 V, 40 μF TDK B32776G4406K, which result in a maximum voltage V_{CB} of 364 V at 2 kW dc power based on (8.5). In the case with MLCCs, one hundred TDK C5750 capacitors are connected in parallel and constructed as a single block. As simulated in Fig. 8.17, the corresponding peak voltage for 100 TDK

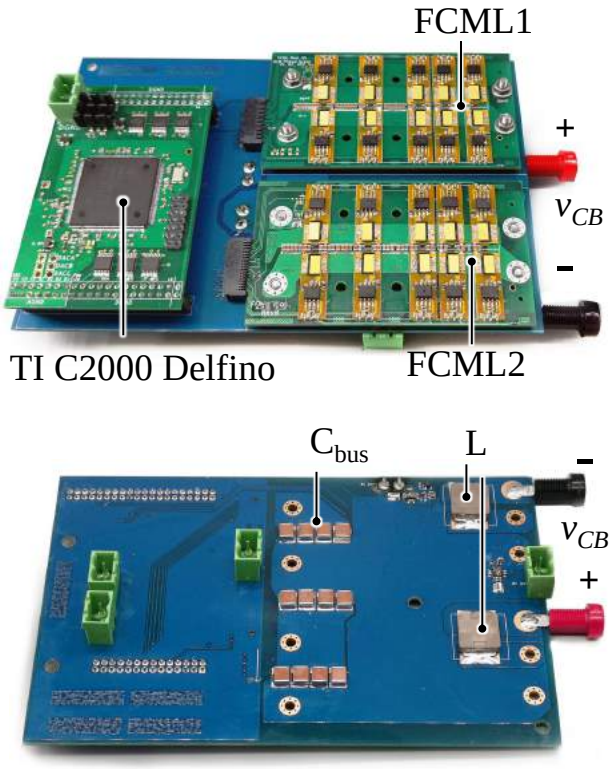

Figure 8.28: Tested buffer hardware. The dc-ac converter is implemented with a full-bridge converter with two FCML legs.

C5750 is 371 V. The two buffer capacitors are shown in Fig. 8.29 for size comparison. The filter inductors and other key components are listed in Table. 8.2. For the 2 kW test, the buffer is tested with no heatsink attached to the FCML modules and only airflow from an electric fan.

Accounting for the volume of all the passive components (C_{bus}, C_{buf}, filter inductors, flying capacitors) in the main power stage, the power density of the hardware by passive component volume is **21.6 W/cm^3 (354 W/in^3)** with film capacitors, and **157.5 W/cm^3 (2581.1 W/in^3)** with MLCCs. The volume breakdown of passive components in the main power stage are listed in Table. 8.3.

8.8 Experimental Verifications

The experimental setup includes a dc voltage source of 450 V, a 10 Ω source resistor, and an electronic load operated in current load mode to emulate an inverter load with unity power factor. The buffer converter is tested up to 2 kW with no heatsink, and the efficiency is measured with Keysight PA2201A power analyzer.

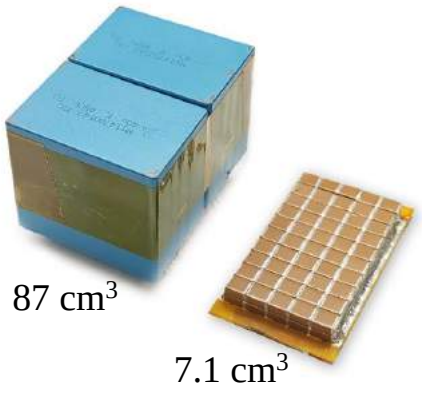

Figure 8.29: Buffer capacitor size comparison between the tested film capacitors (TDK B32776G4406K) and MLCCs (TDK C5750X6S).

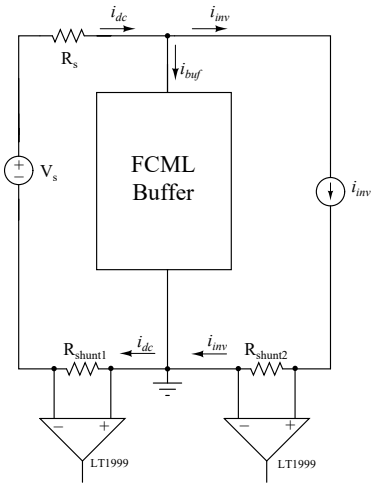

Figure 8.30: Current sensing circuitry with two shunt resistors and current amplifiers.

Results with film capacitors

Figure 8.31 and Fig. 8.32 show the steady-state operation under the condition of 400 V dc-bus, and 2 kW dc powe, using film capacitors as C_{buf}. Dc source current i_{dc}, buffer capacitor voltage v_{CB} and i_{CB} and the differential FCML switching node voltage $v_{\text{sw1}} - v_{\text{sw2}}$ are monitored. As can be seen in Fig. 8.31, with only feedforward and PR compensator at the line frequency, the buffer capacitor's voltage and current are obviously distorted, and the buffer converter is not able to perfectly cancel the twice-line frequency component in i_{inv}, resulting in 850 mA ripple on the dc-side current. With an additional 3rd harmonic resonant compensation term, the buffer capacitor voltage is less distorted, and the resulting

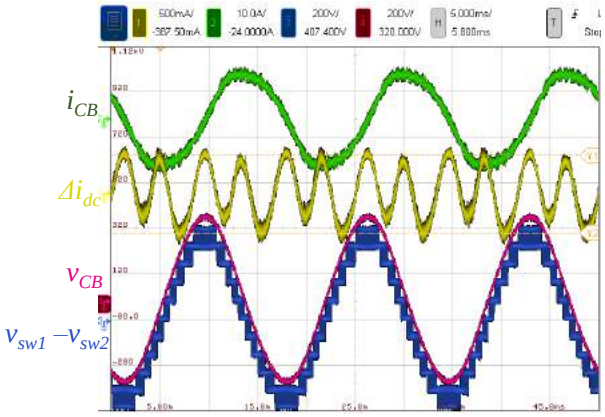

Figure 8.31: Experimental waveforms of the proposed buffer with **film capacitors** controlled with only feedforward and PR compensator. The dc source current i_{dc} is ac-coupled to showcase the ripple component. Without 3rd harmonic compensation, the dc current ripple is 850 mA. Test condition: 400 V dc bus, 2 kW dc power.

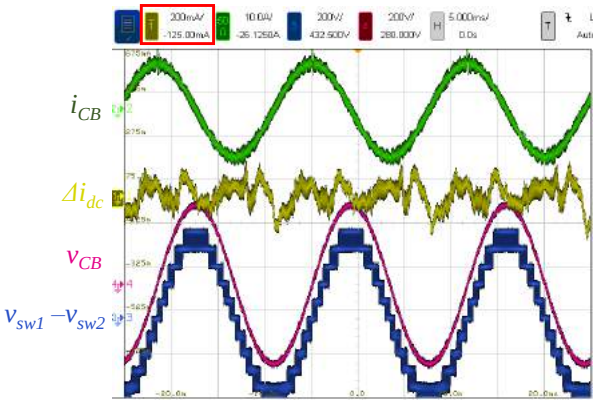

Figure 8.32: Experimental waveforms of the proposed buffer with **film capacitors** controlled with additional 3rd harmonic compensation, along with feedforward and PR compensator. The dc source current i_{dc} is ac-coupled to showcase the ripple component. As shown, the dc-side current has much lower ripple component of only 200 mA with 3rd harmonic compensation. Test condition: 400 V dc bus, 2 kW dc power.

Table 8.2: Key component list of the buffer converter.

Component	Part number	Parameters
GaN transistors	GaN Systems GS1008T	100 V, 7 mΩ
GaN gate driver	Silicon Lab Si8271	
Flying capacitors	TDK C5750X6S × 36	2.2 μF, 450 V
dc-bus capacitors	TDK C5750X6S × 20	2.2 μF, 450 V
Inductors	Vishay IHLW5050 × 2	6.8 μH, 18 A
Buffer capacitors	TDK B32776G4406K (film) × 2	40 μF, 450 V
	TDK C5750X6S (MLCC) × 100	2.2 μF, 450 V

ripple component in the dc-side current is reduced to 200 mA, as shown in Fig. 8.32. The corresponding ripple current ratio is 4%, which is significantly lower than the common limit of 20% [1]. This ripple ratio is equivalent to having a 6.6 mF physical capacitor at the dc-bus, if a passive capacitor bank solution is used. The harmonic can be further suppressed if resonant compensator at higher order of harmonics are included [62].

Fig. 8.33 and Fig. 8.34 show the transient behavior of the buffer during load step up and down respectively. The emulated single-phase inverter power steps from 1 kW to 2 kW in

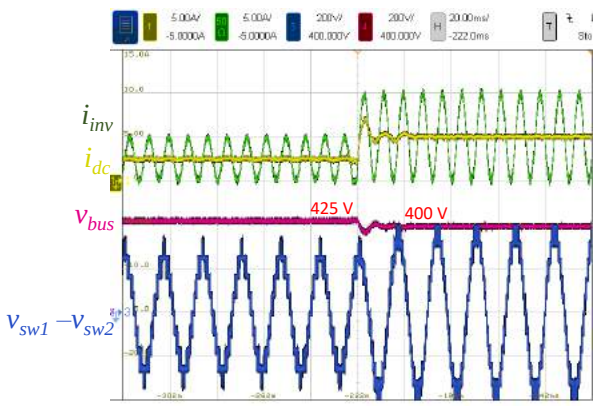

Figure 8.33: Experimental waveforms of the proposed buffer during load step up. The dc side current steps from 2.5 A to 5 A.

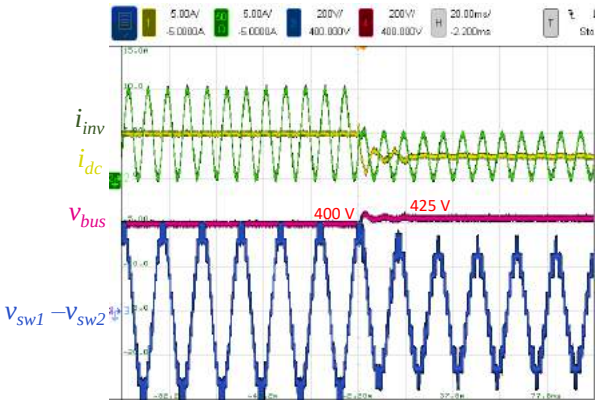

Figure 8.34: Experimental waveforms of the proposed buffer during load step down. The dc side current steps from 5 A to 2.5 A.

Table 8.3: Volumes of passive components

Passive components	Volume (cm^3)
C_{buf} (Film)	87.02
C_{buf} (MLCC)	7.1
C_{fly}	2.87
C_{bus}	1.60
L	1.13

Fig. 8.33 and steps down from 2 kW to 1 kW in Fig. 8.34. In both cases, the control is able to adjust the magnitude of v_{CB} to the new load condition after one line cycle and suppress the harmonic in v_{CB} to minimize the dc current ripple. Note that the dc-bus voltages changes accordingly due to the 10 Ω source resistance.

Results with X6S MLCCs

The steady-state operating waveform with the MLCCs as the buffer capacitor at 2 kW and 400 V dc-bus is shown in Fig. 8.35. It can be seen that with the proposed power harmonic elimination technique, the dc-side current has only 300 mA ripple component, which is 6% of the dc average current. The low ripple indicates that the buffer power contains low harmonic, demonstrating the effectiveness of the proposed control.

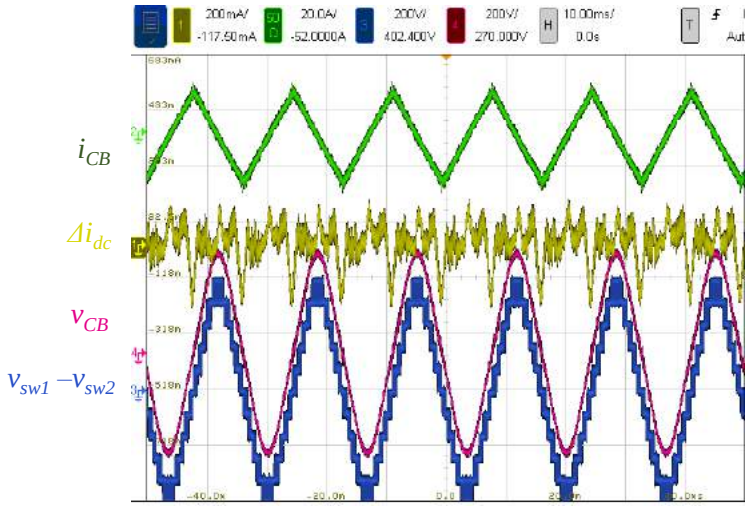

Figure 8.35: Experimental waveforms of the buffer with **MLCCs** controlled with the proposed power harmonic elimination scheme. The dc source current i_{dc} is ac-coupled to showcase the ripple component. As shown, the dc-side current has low ripple component of only 300 mA, resulting from the low-harmonic buffer power. Test condition: 400 V dc bus, 2 kW dc power.

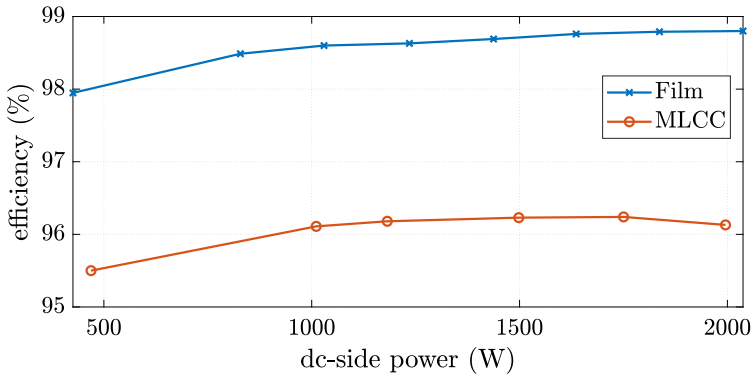

Figure 8.36: Measured buffer efficiencies of using both film capacitor and MLCC as buffer capacitors.

Loss comparison

The tested buffer efficiencies of using both film capacitors and MLCCs are plotted in Fig. 8.36. As can be seen, the buffer with the film capacitors maintains higher efficiency than the MLCCs across the full load range.

While both the peak voltage and current in the FCML converters are slightly higher in the case with the MLCCs, which leads to higher loss in the converters, the major difference

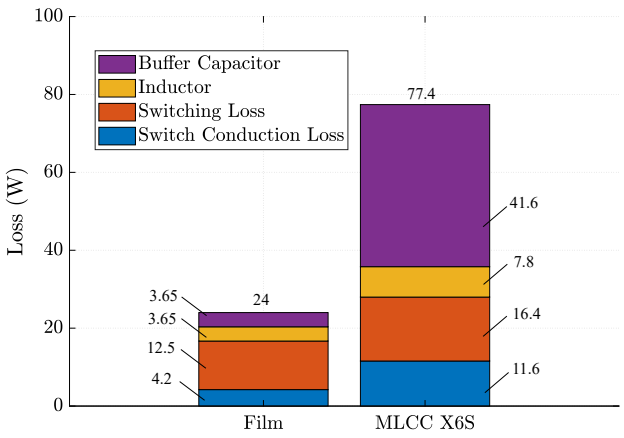

Figure 8.37: Estimated loss composition of the buffer converters with film capacitor and MLCC.

Table 8.4: Comparison to other active buffers

Reference	[7]	[3]	This work (film cap)	This work (X6S MLCC)
Power rating (kVA)	2	2	2	2
Buffer capacitor type	MLCC	MLCC	Film	X6S MLCC
Effective buffer capacitor energy density	0.38 J/cm^3	0.41 J/cm^3	0.06 J/cm^3	0.74 J/cm^3
Total effective buffer capacitance	150 μF (350 V)	100 μF (450 V)+ 430 μF (80 V)	80 μF	77.5 μF (effective with 371 V peak)
Total capacitor volume (cm^3)	**24.6**	**28.1**	**87**	**7.1**
Total passive volume (cm^3)	**31.2**	**32.9**	**92.6**	**12.7**
Energy utilization	49%	46%	100%	100%
Efficiency @ 2 kW	98.65%	99.3%	98.8%	96.12%
Dc-side ripple ratio @ 2 kW	$< 3\%$	15%	4%	6%

in the overall loss is from the MLCC buffer capacitors. The large voltage swing on the MLCCs induces high dielectric hysteresis loss besides the ESR conduction loss. As tested in [58], the loss density of the TDK C5750 under 60 Hz, 400 V peak-to-peak sinusoidal voltage at 60°C is 3 W/cm^3. At 2 kW in the bipolar buffer, the peak-to-peak voltage swing on the buffer capacitor is 742 V, thus a loss density higher than 3 W/cm^3 is expected for the buffer application.

The estimated loss composition at 2 kW of both buffers are provided in Fig. 8.37. The individual contributions from the device switching, device conduction, inductors, and buffer capacitors are also labeled on the sides of the stacked bar diagram. The loss on the buffer capacitors are estimated by subtracting the converter loss from the total loss. The estimated loss density of MLCC is thus $\frac{41.6\text{W}}{7.1\text{cm}^3} = 5.9$ W/cm^3. On the other hand, the loss on the film capacitors is estimated to be 3.65 W, which is consistent with the tested high efficiencies (>99.5%) of film capacitors in [10].

Comparison of key performance metrics with other high power density active buffer solutions are presented in Table. 8.4. The efficiency with the film capacitors are comparable to

Table 8.5: Buffer control parameters for different numbers of X6S

Number of Capacitors	Fundamental (V)	V_{3rd} (%)	V_{5th} (%)
100	345 V	9%	0.9%
120	306 V	9.5%	0.75%
140	272 V	8.7%	0.63%
160	247 V	8.4%	0.65%
180	226 V	8%	0.53%
200	210 V	7.5%	0.45%

other high performance buffer solutions. With the MLCC, the volume of the buffer capacitor is 3-4 times smaller, yet the high dielectric loss led to relatively low overall buffer efficiency.

8.9 Loss-Volume Tradeoff Study

For Series-Stacked Buffer, the Loss-Volume pareto front study in Chapter 5 shows that with more capacitors, the loss will be lower because with higher number of capacitors, the power process by the full-bridge is reduced. However, in the bipolar ripple port, it can be seen from (8.3) that since the power of the buffer capacitor has to be always equal to the full ripple power of $V_{\text{bus}}i_{\text{buf}}$, the actual loss from the converter has to be calculated based on the capacitor current and voltage combination of a particular capacitance value. For instance, in the linear capacitor case, with higher capacitance, the capacitor voltage (8.5) will have a lower magnitude. However, this also means that since the total power magnitude is fixed for a given single-phase conversion scenario, the magnitude of the capacitor current will increase. As a result, the conduction loss in the converter will actually increase with buffer capacitance. Furthermore, with nonlinear ceramic capacitors, the dielectric hysteresis loss that is related to the voltage swing magnitude has to be included in the loss model.

In this section, based on the loss model developed in last section, a simulation-only loss-volume study similar to Chapter 5 is carried out to observe the general trends with X6S nonlinear capacitors. The capacitor number is varied from 100 to 200, with an increment of 20. Since the exact voltage waveforms for different numbers of TDK C5750X6S are determined by the feedback loop in Fig. 8.15, the control parameters for third and fifth harmonics are extracted from PLECS, and put into the loss function. In Table. 8.5, the fundamental component of the buffer capacitor voltage and the corresponding percentage of third and fifth harmonics from PLECS simulation are presented.

To model the hysteresis loss, a simple model that relates such loss with the square of the voltage magnitude is used for estimation as: $P_{\text{hs,mlcc}} \propto V_{\text{CB}}^2$. Nevertheless, more complicated loss modeling of the ceramic capacitors itself is an active area of research [23], [26]. Fig. 8.38 shows the total losses of all the numbers of capacitors, and Fig. 8.39 shows the corresponding loss breakdown. As can be seen, for 100, 120, 140 X6S capacitors, while the overall loss

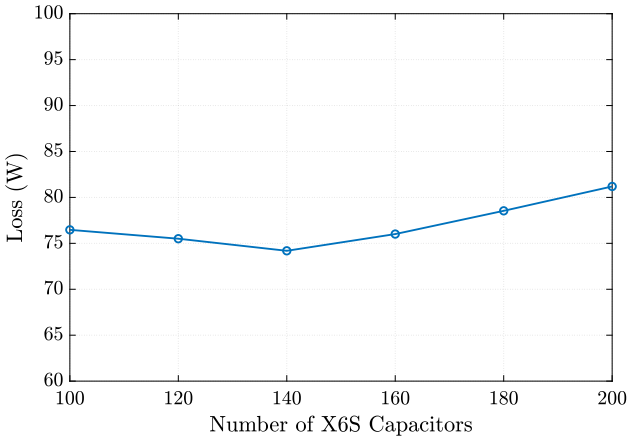

Figure 8.38: Calculated total loss of the buffer converter with simulated voltage and current waveforms for each number of X6S capacitors.

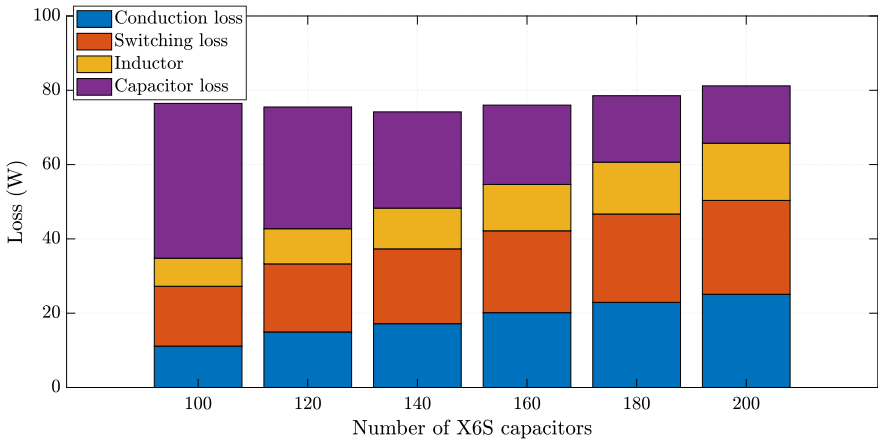

Figure 8.39: Loss breakdown of the buffer converter with simulated voltage and current waveforms for each number of X6S capacitors.

decreases due the reduction of hysteresis loss, the percentage of the reduced loss is not as high as the gain in volume. Moreover, for 160, 180, and 200 capacitors, as the number of capacitor increases, the conduction loss of both switch and inductor start to dominate. From the results, we can see that after a certain number of capacitors, it makes zero sense to further increase the capacitance to lower the loss. In other words, once the buffer capacitance is large enough to maintain the V_{CB} magnitude to be lower than the dc-bus voltage, the motivation to use larger capacitors to improve efficiency is not as strong as for the SSB. Yet, further experimental results are necessary to confirm this observation.

8.10 Conclusion

The proposed multilevel bipolar active power pulsation buffer allows minimum energy storage on the buffer capacitor for single-phase conversion, while shrinking the switching-frequency filtering passive component size with the FCML topology. The proposed active decoupling control schemes are able to regulate dc-side current with low ripple contents for both linear film capacitors and non-linear MLCCs. We have also demonstrated that the proposed control schemes with multiple compensators, digital filters and tens of PWM signals can be implemented with a commercially available DSP controller.

Chapter 9

Control and Modulation of Three-phase Flying Capacitor Multilevel Converters

9.1 Introduction

Multilevel converters have advantages such as low inductor current harmonics and reduced voltage stress on power switches for high performance applications compared to conventional two-level designs. Among many multilevel topologies, the flying capacitor multilevel (FCML) [39] converter has been demonstrated with high power density and efficiency due to the use of high energy density capacitors in dc-dc and single-phase applications [11], [42], [52]. In this chapter, we explore the use of the FCML in three-phase applications. An examplar N-level FCML three-phase inverter and PFC systems are shown in Fig. 9.1 and Fig. 9.2 respectively.

SVPWM is a common modulation strategy for three-phase converters which enables reduced inductor current ripple and increased line voltage [71]. However, SVPWM is complicated to implement in multilevel converters because the number of the voltage vectors scales as N^3, where N is the number of levels of the FCML. Instead of SVPWM, Carrier-Based PWM (CBPWM) with continuous duty-ratio is a well-known modulation method that is easy to implement in multilevel converters with common multilevel modulation techniques such as Phase Decomposition PWM (PDPWM) and Phase-Shifted PWM (PSPWM) [39], [72], [73]. PDPWM with zero sequence injection (ZSI) results in an equivalent frequency on the inductor current ripple that is twice of the carrier frequency, which is equivalent to using SVPWM only in three-level three-phase FCML converters [74]. Nevertheless, PDPWM can not achieve natural balancing of the flying capacitor voltages in the FCML [75] and the effective frequency on the inductor current does not increase with N. On the other hand, PSPWM can achieve natural balancing in the FCML [68], and the equivalent frequency of the inductor current ripple is $N-1$ times of the carrier frequency [39]. However, without any

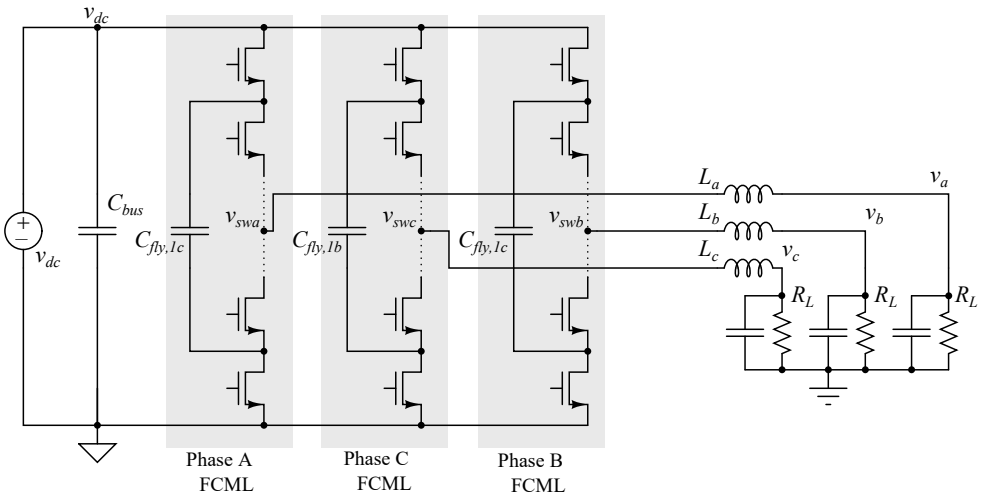

Figure 9.1: Schematic drawing of a three-phase N-level FCML inverter.

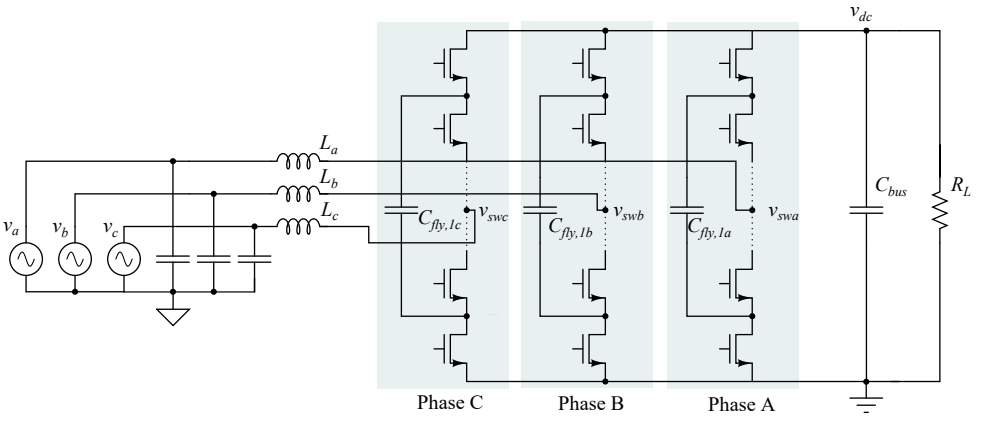

Figure 9.2: Schematic drawing of a three-phase N-level FCML PFC.

carrier phase shift among the three phase legs, PSPWM will result in higher voltage across the inductor because the switching node voltages (v_{swx}) in three FCML converters are not always center-aligned. The phase-shift strategy to make PSPWM equivalent to PDPWM in a single-phase multilevel converter has been discussed in [76]. However, the control strategy is complicated and will result in redundant phase-shift movements. To reduce the the number of phase shift movements and inductor current ripple, a dynamic carrier phase shift strategy is proposed in this work. The proposed modulation scheme can be categorized as a type of CBPWM with continuous duty ratio, and each leg is modulating with PSPWM. The relative switching carrier phases among three phase legs are dynamically adjusted to make sure that all v_{swx} are center-alienged to reduce the voltage stress across the inductor. Moreover, since the effective duty ratio on the switching node voltage is different than the

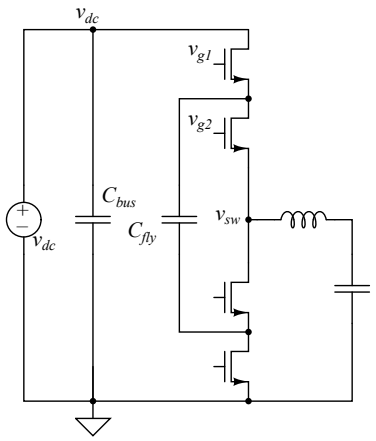

Figure 9.3: Schematic drawing of a single three-level FCML converter.

duty ratio of the PSPWM signals, a control strategy to inject equivalent zero sequence duty ratios to the switching node is implemented so that the voltage across the inductor is as low as SVPWM, and the resultant equivalent frequency on the inductor current ripple is $2(N-1)$ times of the carrier frequency. In short, the advantages of PSPWM and PDPWM are combined together with the proposed modulation.

This chapter first discusses the limitation of different modulation techniques for three phase FCML converters. After that, the detailed operation of the proposed modulation strategy and its relation to SVPWM are discussed. Next, the digital implementation of the proposed control is presented. Lastly, the experimental results of a three-phase six-level FCML converter hardware prototype are provided and analyzed.

9.2 Proposed Modulation Strategy

Phase relation between switching node voltages and PWM signals using PSPWM under different duty ratios

With SVPWM, the center of the switching node voltages in three phase legs are always aligned to minimize the inductor current ripple [71]. However, this is not always the case with PSPWM in three-phase FCML converters. To illustrate the fundamental problem of using PSPWM in three-phase converters, the ideal waveforms of a single three-level dc-dc FCML in Fig. 9.3 operating with PSPWM is shown in Fig. 9.4 and Fig. 9.5, for duty ratio of 0.25 and 0.75 respectively. For duty ratio of 0.25, as marked with the orange dashed line, the center of the switching node voltage (center of the higher voltage level) is aligned with the center of the PSPWM signal. Yet, for duty ratio of 0.75, the center of v_{sw} is shifted by $\frac{1}{4}T_{\text{sw}}$ from the PSPWM signal. To be more specific, in a 3-level FCML, the phase between the switching node voltage and PWM signal is zero when D < 0.5, and $\frac{1}{4}T_{\text{sw}}$ when D $>$

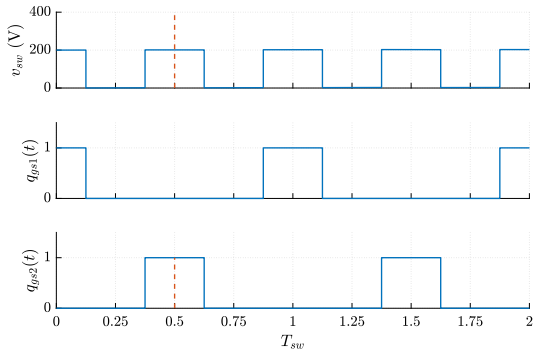

Figure 9.4: Three-level FCML switching waveforms with 0.25 duty ratio. Top: v_{sw}, middle and bottom: two PSPWM signals. The center of the switching node voltage is aligned with the PSPWM.

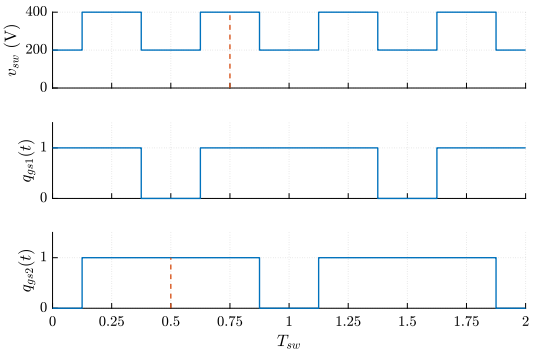

Figure 9.5: Three-level FCML switching waveforms with 0.75 duty ratio. The center of the switching node voltage is not aligned with the high level of PSPWM. Instead, the center of v_{sw} is phase shifted by $\frac{1}{4}T_{\text{sw}}$.

0.5. In fact, in a N-level FCML converter, for a duty ratio of D, if $floor((N-1)D)$ is odd, the center of the switching node voltage will be shifted by $\frac{1}{2(N-1)}T_{\text{sw}}$ compared to when $floor((N-1)D)$ is even.

In the three-phase converter, the duty ratios in three phase legs are different. Therefore, since the relation between the inductor voltage stress and switching node voltages in a three-phase converter (as shown in Fig. 9.1)is

$$v_{\text{Lx}} = v_{\text{swx}} - \frac{v_{\text{swa}} + v_{\text{swb}} + v_{\text{swc}}}{3} - v_{\text{xn}}, \text{x} = a, b, c, \tag{9.1}$$

where v_{xn} are the three phase line-neutral voltages. if the duty ratios in three phase legs do not have the same parity of $floor((N-1)D)$, v_{swx} in each leg will not be center aligned, which leads to larger inductor current ripple than SVPWM or PDPWM with ZSI, as shown in Fig. 9.6 for a three-level FCML three-phase inverter when phase A voltage is at its peak, with $D_a = 0.82$, $D_b = 0.18$, $D_c = 0.18$.

The equivalence of effective duty ratios between PSPWM with ZSI and SVPWM

According to the analysis in previous work [77], with proper zero sequence injection (ZSI) duty D_{z} adding to the ideal duty ratio D_{x}, PDPWM can be equivalent to SVPWM. In this section, the effective duty ratio D_{eff} of the PSPWM with ZSI is shown to be equal to the SVPWM. To avoid complicated calculation of SVPWM in FCML converters with high number of levels, the proof of the equivalence is carried out in a three-level FCML. If the

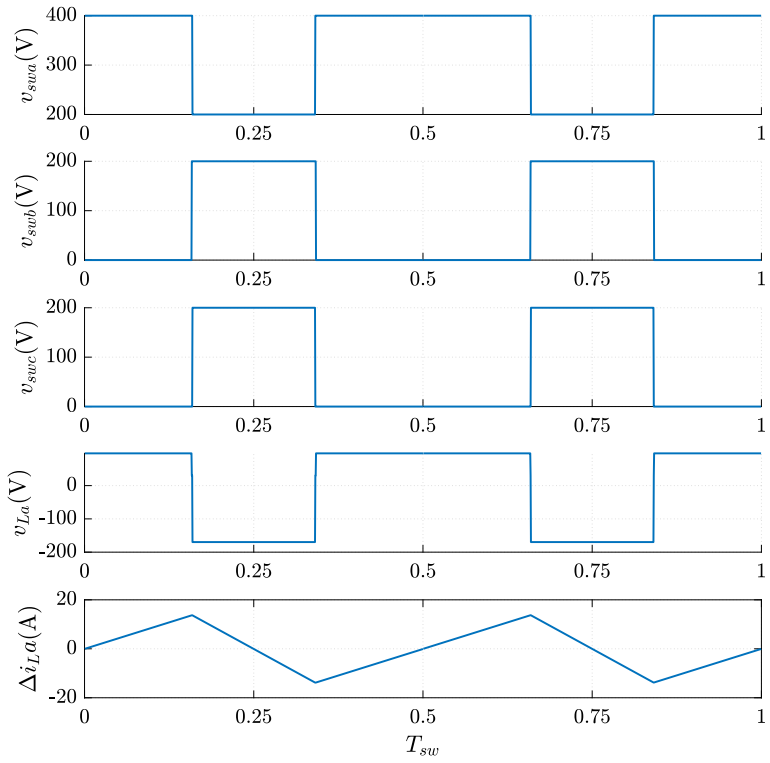

Figure 9.6: Ideal waveforms of the three-phase three-level FCML with PSPWM without any phase shift among three phases. $D_a = 0.82$, $D_b = 0.18$, $D_c = 0.18$.

three line-neutral voltages are defined as

$$\begin{aligned} v_{\mathrm{an}} &= \cos(\omega_L t) \\ v_{\mathrm{bn}} &= \cos(\omega_L t - \frac{2\pi}{3}) \\ v_{\mathrm{cn}} &= \cos(\omega_L t + \frac{2\pi}{3}). \end{aligned} \tag{9.2}$$

The ZSI duty for the two level converters is calculated from the three-phase line-neutral voltage v_{xn} (x = a, b, c) as

$$D_{\mathrm{Z}} = -\frac{\max(D_{1\mathrm{a}}, D_{1\mathrm{b}}, D_{1\mathrm{c}}) + \min(D_{1\mathrm{a}}, D_{1\mathrm{b}}, D_{1\mathrm{c}})}{2}, \tag{9.3}$$

where

$$D_{1\mathrm{x}} = \frac{v_{\mathrm{xn}}}{V_{\mathrm{dc}}}, \mathrm{x} = a, b, c \tag{9.4}$$

and the final duty ratio of the PWM signals for two-level inverters is

$$D_{\mathrm{x,\ 2L}} = D_{1\mathrm{x}} + D_{\mathrm{z}} + 0.5. \tag{9.5}$$

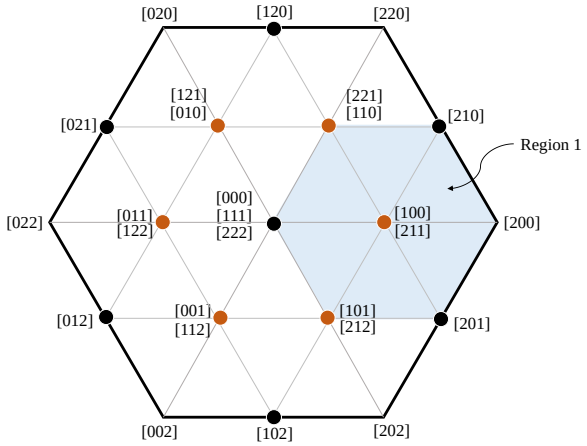

Figure 9.7: The vector distribution of three level SVPWM. The shaded small hexagonal area is the re-centered region that is equivalent to two-level SVPWM.

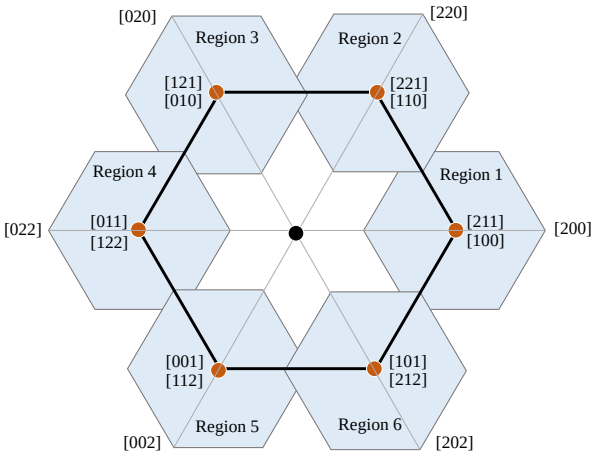

Figure 9.8: All re-centered small hexagonal regions that are equivalent to two-level SVPWMs.

For N-level (N≥3) multilevel converters, the ZSI duty ratio is different from the two-level converters because of the additional vectors in the multilevel converters [78][79]. The ZSI duty for multilevel converters is

$$D_{\mathrm{ZN}} = -\frac{\max(D'_{\mathrm{a,\ 2L}}, D'_{\mathrm{b,\ 2L}}, D'_{\mathrm{c,\ 2L}}) + \min(D'_{\mathrm{a,\ 2L}}, D'_{\mathrm{b,\ 2L}}, D'_{\mathrm{c,\ 2L}})}{2}, \tag{9.6}$$

where

$$D'_{\mathrm{2x}} = D_{\mathrm{x,\ 2L}} \bmod (\frac{1}{N-1}). \tag{9.7}$$

And the final duty ratio for N-level inverter is

$$D_{\mathrm{x,\ NL}} = D_{\mathrm{x,\ 2L}} + D_{\mathrm{ZN}} + \frac{1}{2(N-1)}. \tag{9.8}$$

With PSPWM, the switching node voltage is always modulated between the adjacent voltage levels that is separated by $\frac{V_{\mathrm{dc}}}{N-1}$. Moreover, the two modulating voltage levels and the effective duty ratio of the switching node voltages in FCML change with the PSPWM duty ratio. The modulating high ($v_{\mathrm{swH\_PS}}$) and low voltage ($v_{\mathrm{swL\_PS}}$) levels and the effective duty ratio on the switching node $D_{\mathrm{eff\_PS}}$ need to be calculated using the PSPWM duty ratio in (9.8) to compare with SVPWM as follows:

$$\begin{aligned} v_{\mathrm{swH\_PS}} &= v_{\mathrm{dc}} \frac{ceil((D_{\mathrm{x,\ NL}} \cdot (N-1)) \bmod 1)}{N-1} \\ v_{\mathrm{swL\_PS}} &= v_{\mathrm{dc}} \frac{ceil((D_{\mathrm{x,\ NL}} \cdot (N-1)) \bmod 1) - 1}{N-1}. \end{aligned} \tag{9.9}$$

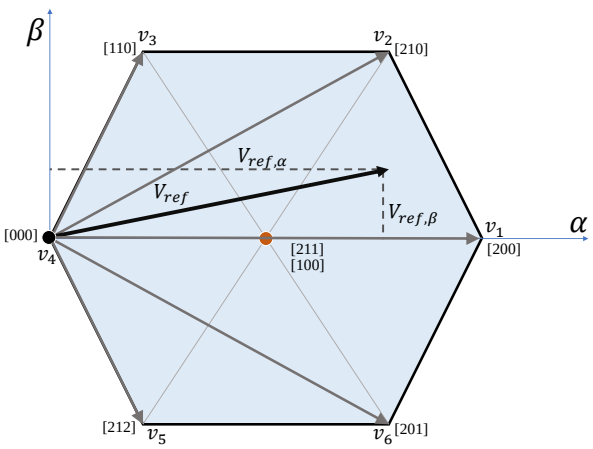

Figure 9.9: Region one of three-level SVPWM with a reference vector.

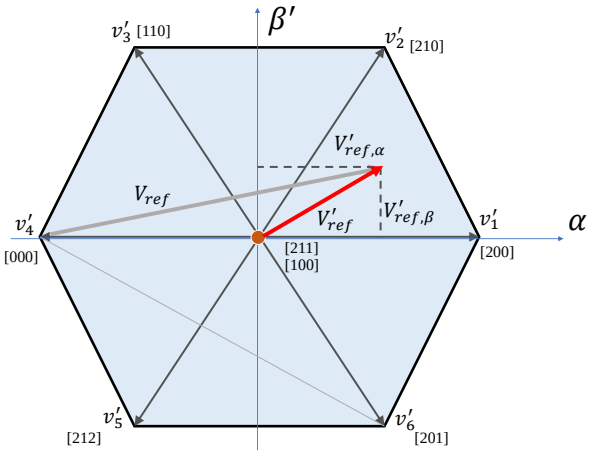

Figure 9.10: Region one of three level SVPWM with the modified reference vector re-centered at [211] ([110]).

$$D_{\text{eff\_PSPWM}} = (D_{\text{x, NL}} \cdot (N-1)) \bmod 1 \tag{9.10}$$

The three-level SVPWM vector diagram shown in Fig. 9.7 has 27 different voltage vectors. Here 2, 1 and 0 coding corresponds to the switching node voltage levels of V_{dc}, $0.5V_{\text{dc}}$, and 0 respectively. To utilize the three voltage levels and modulate equivalently to a two-level converter using SVPWM, the main hexagon can be divided into six small hexagonal regions with the corresponding center vector marked in orange, as shown in Fig. 9.7 and Fig. 9.8 [80]. The voltage levels of switching node voltage (v_{sw}) in different hexagon regions are shown in Table 9.1.

Table 9.1: High and Low Voltage Level of Switching Node in Each Phase at Different Regions of Three-Level SVPWM

region	v_{swaH} / v_{swaL}	v_{swbH} / v_{swbL}	v_{swcH} / v_{swcL}
1	V_{dc} / $0.5V_{\text{dc}}$	$0.5V_{\text{dc}}$ / 0	$0.5V_{\text{dc}}$ / 0
2	V_{dc} / $0.5V_{\text{dc}}$	$0.5V_{\text{dc}}$ / 0	$0.5V_{\text{dc}}$ / 0
3	$0.5V_{\text{dc}}$ / 0	V_{dc} / $0.5V_{\text{dc}}$	$0.5V_{\text{dc}}$ / 0
4	$0.5V_{\text{dc}}$ / 0	V_{dc} / $0.5V_{\text{dc}}$	V_{dc} / $0.5V_{\text{dc}}$
5	$0.5V_{\text{dc}}$ / 0	V_{dc} / $0.5V_{\text{dc}}$	V_{dc} / $0.5V_{\text{dc}}$
6	$0.5V_{\text{dc}}$ / 0	V_{dc} / $0.5V_{\text{dc}}$	V_{dc} / $0.5V_{\text{dc}}$

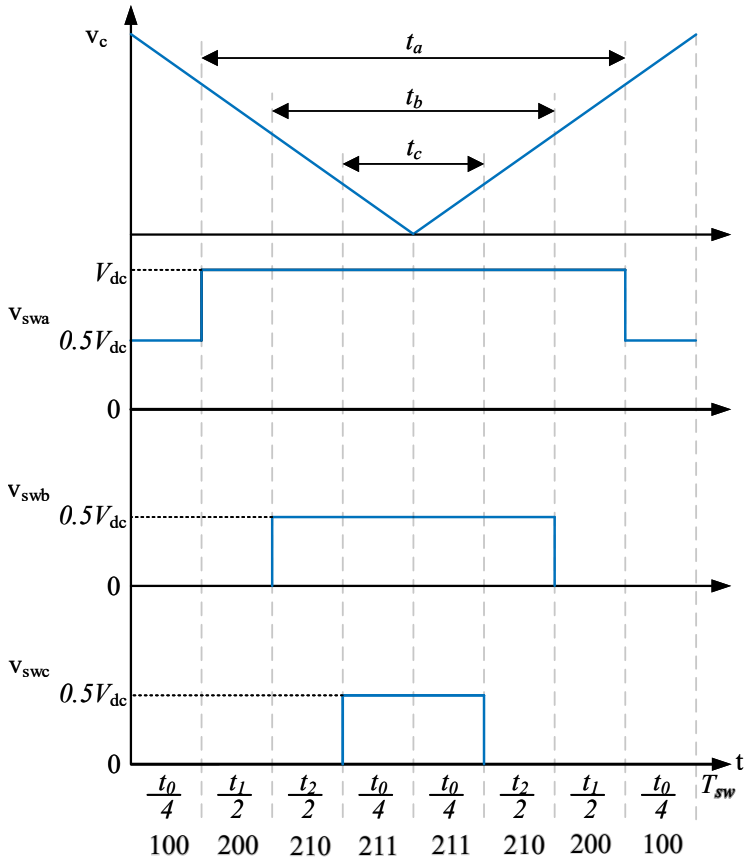

Figure 9.11: The timing diagram of switching node voltages of three-level SVPWM in region one. The vector sequence in a half cycle is [100] - [200] - [210] - [211].

In Fig. 9.9, a reference voltage vector $\boldsymbol{V}_{\text{ref}}$ is shown in the vector diagram, which can be represented with $\alpha - \beta$ coordinates as

$$\begin{bmatrix} v_{\text{ref},\alpha} \\ v_{\text{ref},\beta} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{\text{an}} \\ v_{\text{bn}} \\ v_{\text{cn}} \end{bmatrix} \tag{9.11}$$

However, if the reference voltage vector is originated from the center of the main hexagon [000], modulating from [000] to two adjacent vectors [210] and [200] will result in a transition between V_{dc} and 0 on the switching node. To utilize the intermediate voltage level $0.5V_{\text{dc}}$, the reference vector can be re-centered to [211] as shown in Fig. 9.10, where the updated reference vector $\boldsymbol{V}'_{\text{ref}}$ is drawn in red. Similar to two-level SVPWM, the updated vector $\boldsymbol{V}'_{\text{ref}}$ is the average between the two most adjacent vectors $\boldsymbol{v}'_{\boldsymbol{1}}$[200] and $\boldsymbol{v}'_{\boldsymbol{2}}$[210]. The modulation

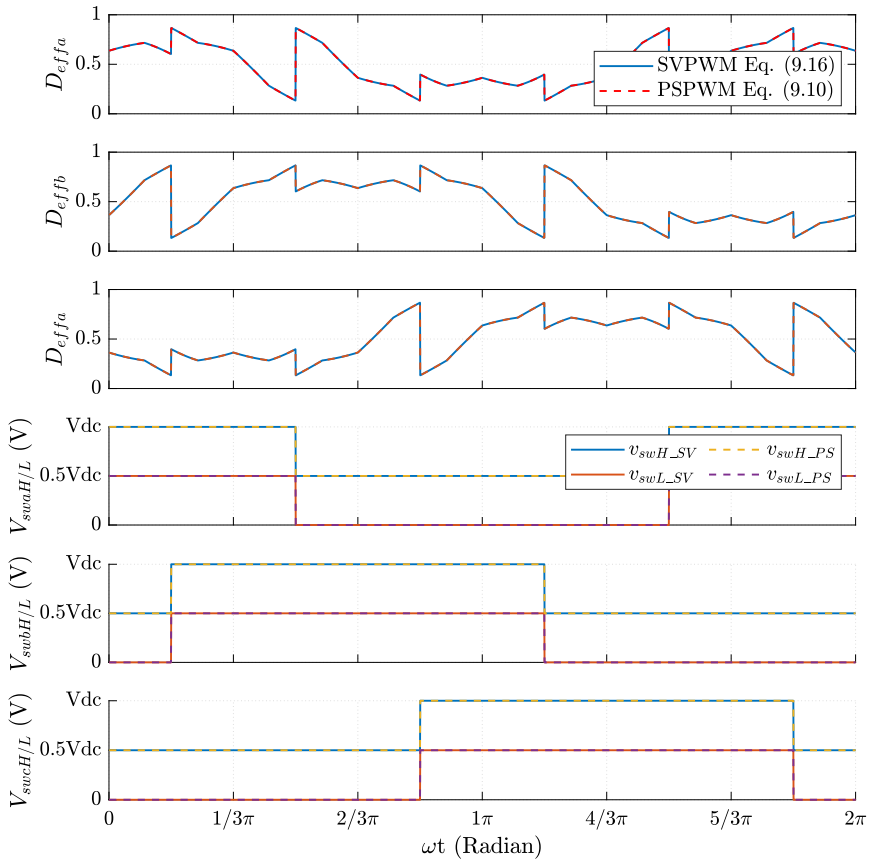

Figure 9.12: The effective duty ratio and the modulating voltage level of PSPWM with ZSI and SVPWM when v_{an}, v_{bn} and v_{cn} are 120 v_{rms} and V_{dc} is 400 V.

vector sequence is thus [100] - [200] - [210] - [211], as in Fig. 9.11. Moreover, $\boldsymbol{V}'_{\text{ref}}$ can be represented with updated $\alpha - \beta$ coordinates as

$$\begin{bmatrix} v'_{\text{ref},\alpha} \\ v'_{\text{ref},\beta} \end{bmatrix} T_{\text{sw}} = \begin{bmatrix} v'_{1,\alpha} \\ v'_{1,\beta} \end{bmatrix} t_1 + \begin{bmatrix} v'_{2,\alpha} \\ v'_{1,\beta} \end{bmatrix} t_2 \tag{9.12}$$

where t_1 and t_2 are the time duration that are spent on $\boldsymbol{v}'_{\boldsymbol{1}}$ [200] and $\boldsymbol{v}'_{\boldsymbol{2}}$ [210] respectively. And the relation between the original $\boldsymbol{v}_{\boldsymbol{1}}$, $\boldsymbol{v}_{\boldsymbol{2}}$ in Fig. 9.9 and the vectors with updated α and β axis $\boldsymbol{v}'_{\boldsymbol{1}}$, $\boldsymbol{v}'_{\boldsymbol{2}}$ is

$$\begin{bmatrix} v'_{\text{y},\alpha} \\ v'_{\text{y},\beta} \end{bmatrix} = \begin{bmatrix} v_{\text{y},\alpha} \\ v_{\text{y},\beta} \end{bmatrix} - \begin{bmatrix} \frac{v_{\text{dc}}}{3} \\ 0 \end{bmatrix}, \text{y} = 1, 2. \tag{9.13}$$

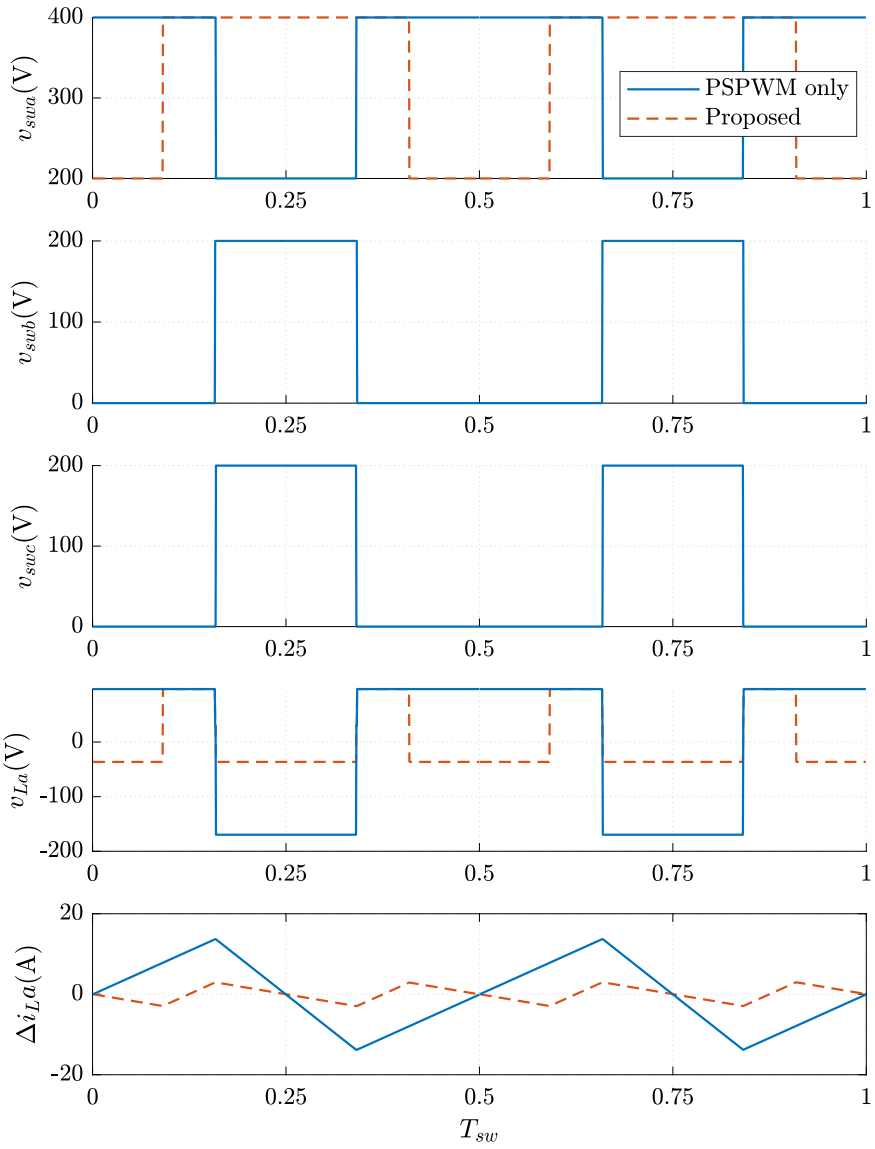

Figure 9.13: Ideal waveforms of the three-phase three-level FCML with PSPWM only and with proposed modulation with ZSI. $D_a = 0.82$, $D_b = 0.18$, $D_c = 0.18$. As can be seen, the proposed control aligns the center of v_{swa} with the other two phases, resulting in reduced voltage and current ripple on the inductor. With ZSI, the effective frequency on the inductor is $2(N-1)f_{\text{sw}}$.

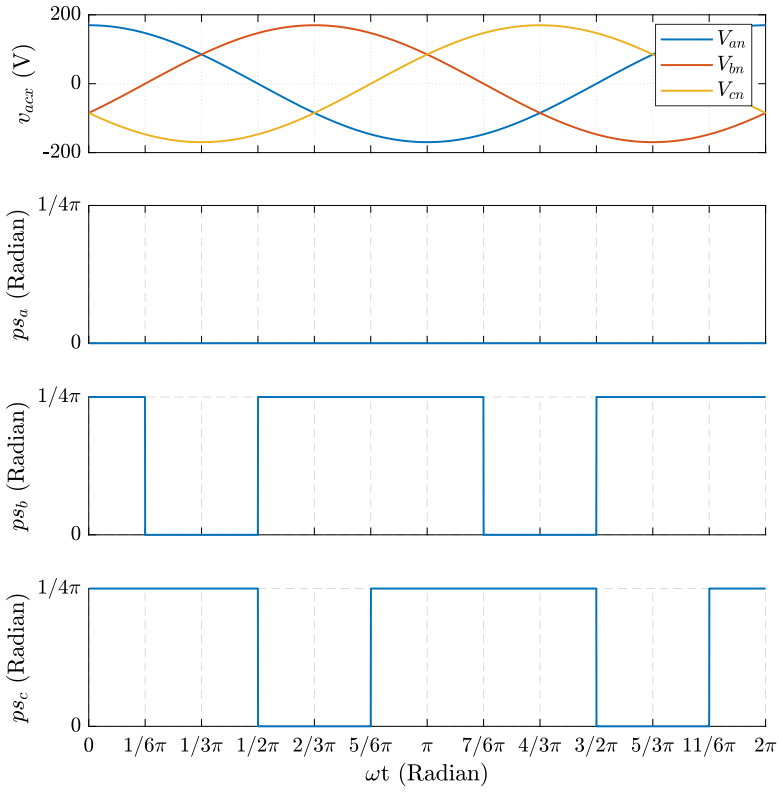

Figure 9.14: The phase shift commands of each phase leg in a three-level FCML inverter with the proposed control in a full line cycle where V_{acx} is 120 V_{rms}, V_{dc} is 400 V_{dc}.

Finally, the time duration of the vectors in region one is calculated as (9.14).

$$\begin{bmatrix} t_1 \\ t_2 \end{bmatrix} T_{sw} = \frac{T_{sw}}{v_{dc}} \begin{bmatrix} 3 \cdot v'_{ref,\alpha} - \sqrt{3} \cdot v'_{ref,\beta} \\ 2\sqrt{3} \cdot v'_{ref,\beta} \end{bmatrix} \tag{9.14}$$

The relationship between the time duration of the vectors and the time duration of high switching node voltage in region one is shown in Fig. 9.11. The effective on-times (voltage at higher levels) of the switching node voltage for each phase are calculated as

$$\begin{aligned} t_a &= (T_{sw} + t_1 + t_2)/2 \\ t_b &= (T_{sw} - t_1 + t_2)/2 \\ t_c &= (T_{sw} - t_1 - t_2)/2 \end{aligned} \tag{9.15}$$

Consequently, the effective duty ratios on the switching node of each phase using three-

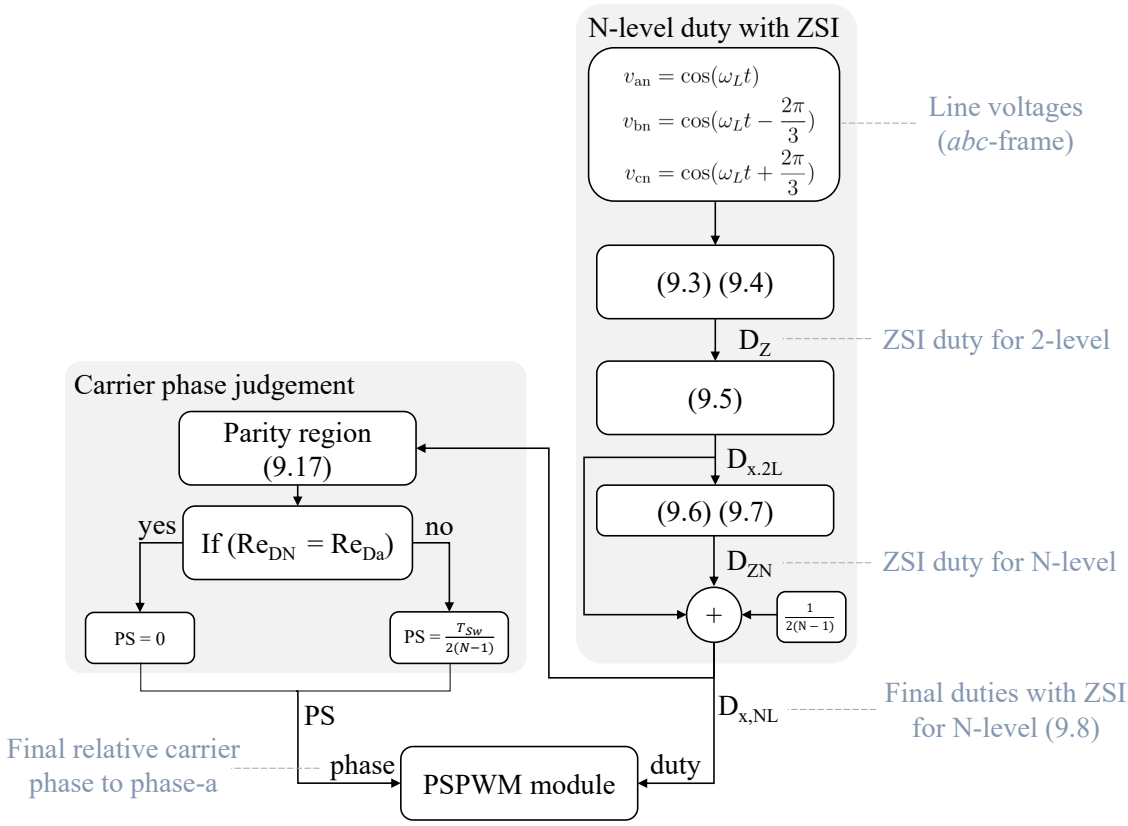

Figure 9.15: Flow chart of the derivation process of the duties and phases for modulation each FCML legs.

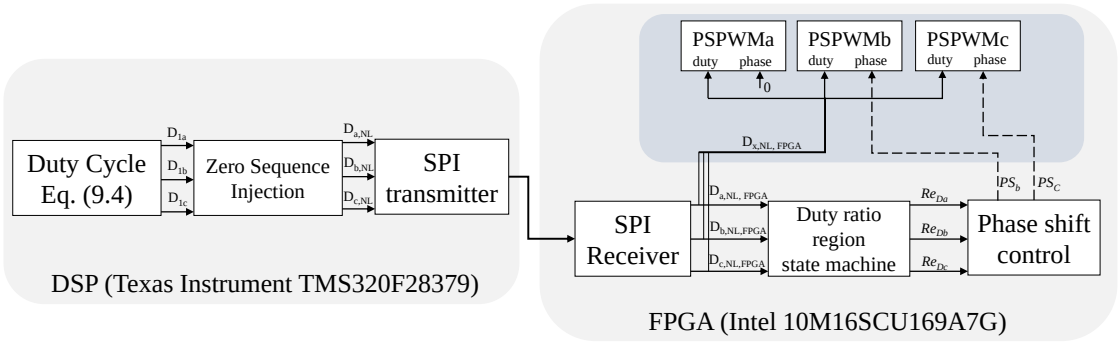

Figure 9.16: Digital implementation of the proposed control for six-level three-phase FCML inverters.

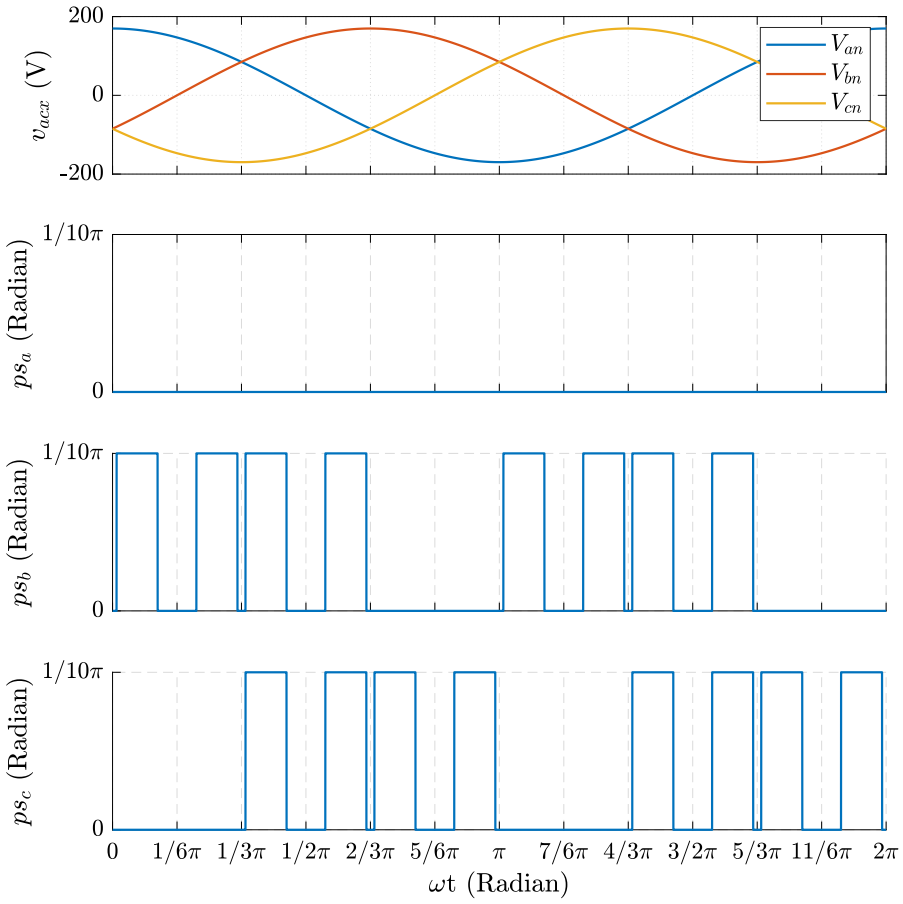

Figure 9.17: The phase shift commands of each phase leg in a six-level FCML inverter with the proposed control in a full line cycle where V_{acx} is 120 V_{rms}, V_{dc} is 400 V_{dc}.

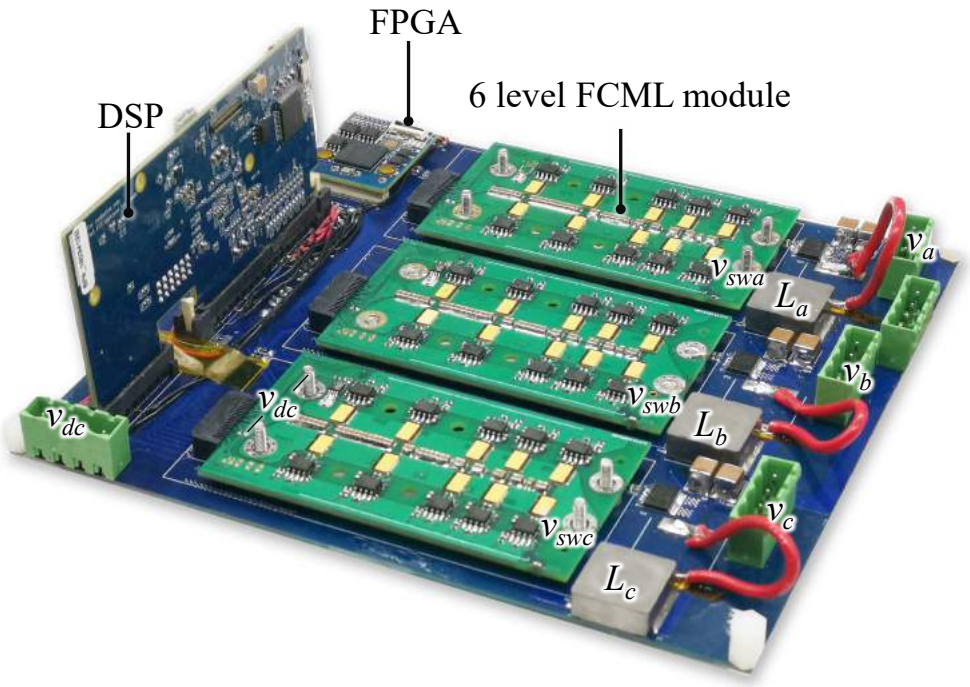

Figure 9.18: The experimental hardware prototype of six-level three-phase FCML inverter. The three six-level FCML modules are mounted onto the main control board with DSP and FPGA.

level SVPWM in region one are determined as

$$D_{\text{effx\_sw}} = \frac{t_{\text{x}}}{T_{\text{sw}}}, \text{x} = a, b, c \tag{9.16}$$

The time duration in other small hexagonal regions of SVPWM have been previously calculated in [80]. The corresponding effective duty ratios can be calculated by substituting t_{a}, t_{b}, and t_{c} into (9.16). In Fig. 9.12, the D_{eff} of PSPWM with ZSI as calculated by (9.8) and (9.10) is equal to the D_{eff} of SVPWM as calculated by (9.16). In addition, the modulating voltage levels on the switching node of PSPWM with ZSI and SVPWM are also identical. In conclusion, the only difference of PSPWM with ZSI and SVPWM is that the switching node voltages of PSPWM are not always center aligned, which can be solved by the proposed dynamic phase-shifting PSPWM.

Proposed dynamic phase shift control

As we have shown that the effective duty ratios and modulating voltage levels of PSPWM with ZSI are identical to that of SVPWM, in order to achieve the same minimum inductor current ripple as SVPWM, a dynamic phase shift control strategy is proposed . As can

be seen in Fig. 9.13, with all three switching node voltages being aligned, the v_{Lx} voltages become smaller compared to PSPWM with no phase shift.

To dynamically shift the carrier PWM phase among three phases, leg A is set as the reference zero phase, and the relative carrier phases in legs B and C to leg A are dynamically changed to ensure that the v_{swx} voltages are always center-aligned across the full line cycle. As shown in Fig. 9.4 and Fig. 9.5, with different duty ratios, the parity regions of three phases have to be evaluated to determine the phase shift as

$$Re_{\mathrm{Dx}} = \mathrm{mod}(floor((N-1)D_{\mathrm{x,\,NL}}), 2). \tag{9.17}$$

If the parity region value of phase B Re_{Db} or phase C Re_{Dc} is the same as phase A, no phase shift is needed, otherwise the corresponding phase shift of the carrier signal is $\frac{1}{2(N-1)}T_{sw}$. The logic to generate phase-shift control signals P_{sx} is described as

$$\begin{aligned} P_{\mathrm{sx}} &= 0, \text{if } Re_{\mathrm{Dx}} = Re_{\mathrm{Da}} \\ P_{\mathrm{sx}} &= 1, \text{if } Re_{\mathrm{Dx}} \neq Re_{\mathrm{Da}} \end{aligned} \tag{9.18}$$

The phase-shift commands for a three-level FCML inverter in one line cycle are plotted in Fig. 9.14.

9.3 Digital Implementation of the Proposed Modulation Strategy

To generate high count of required PWM signals for three-phase FCML converter systems, the proposed modulation is implemented with a digital signal processor (DSP) to calculate the duty ratio of each phase and a field programmable gate array (FPGA) to output the PWM signals. The flow chart of the derivation process for both the duty ratios and phases for each FCML legs in previous sections is illustrated in Fig. 9.15. To realize such computations in real hardware, the digital controller block diagram for the three-phase six-level FCML inverter with proposed modulation is shown in Fig. 9.16. First, duty ratios that are calculated with (9.4) are used to compute the zero sequence injection duty ratios. Second, the updated duty ratios with ZSI are transmitted from the DSP to the FPGA via Serial Peripheral Interface (SPI). On the FPGA side, the parity regions of duty ratios are evaluated with (9.17). If the duty ratio parity region of phase B or phase C is different from phase A, all PWM signals in phase B or phase C need to be phase shifted by $\frac{1}{2(N-1)}T_{\mathrm{sw}}$. The phase shift commands $P_{\mathbf{sx}}$ for phase B and C are implemented with (9.18). The commands of phase shift for the six-level FCMLs in a full line cycle is shown in Fig. 9.17.

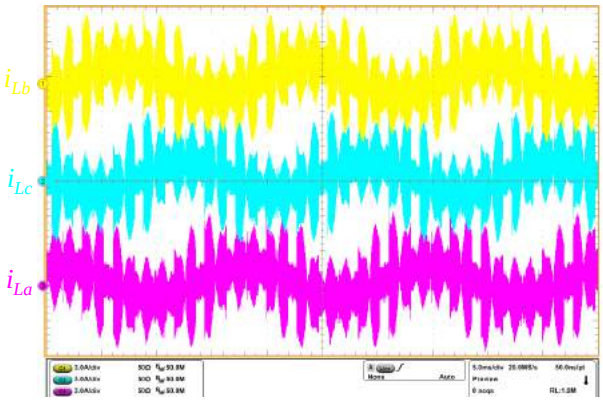

Figure 9.19: Experimental waveforms of the three-phase six-level FCML inverter with PSPWM and ZSI, without any phase shift control. V_{dc} = 400 V, V_{ac} = 120 V_{rms}, 360 W system power.

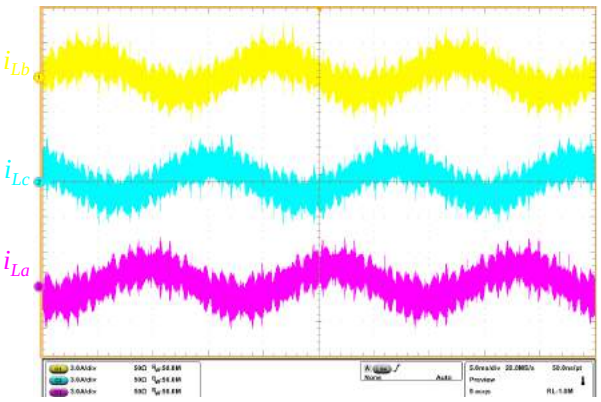

Figure 9.20: Experimental waveforms of the three-phase six-level FCML inverter with the proposed modulation. The inductor current ripple with the proposed control strategy is smaller than PSPWM with ZSI without any phase shift control in Fig. 9.17.

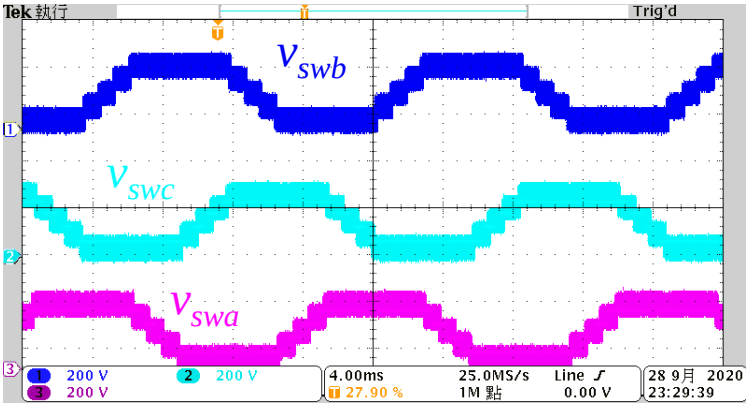

Figure 9.21: The switching node voltages of the three phases at 400 V_{dc}, 360 W, inverter mode, demonstrating good flying capacitor voltage balancing.

9.4 Hardware prototype and Experimental Validations

Verification of the proposed modulation strategy in open-loop inverter

A hardware prototype with the proposed architecture and control is implemented as shown in Fig. 9.18. Three six-level FCML modules in Fig. 6.21 are mounted on the main control board.

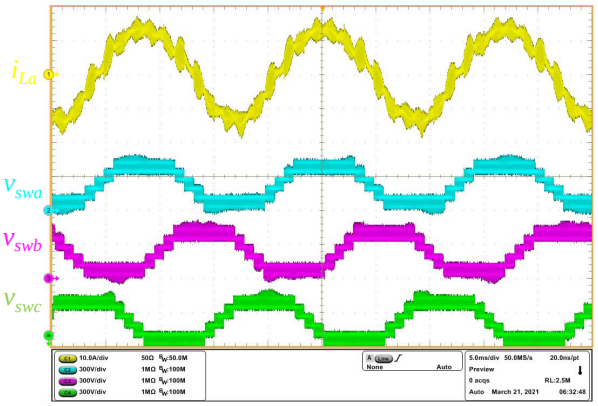

Figure 9.22: Three-phase FCML PFC inductor current and switching node voltages with PSPWM only, with no carrier phase shift control. Test condition: 208 $V_{ac,LL}$ to 400 V_{dc}, 3 kW

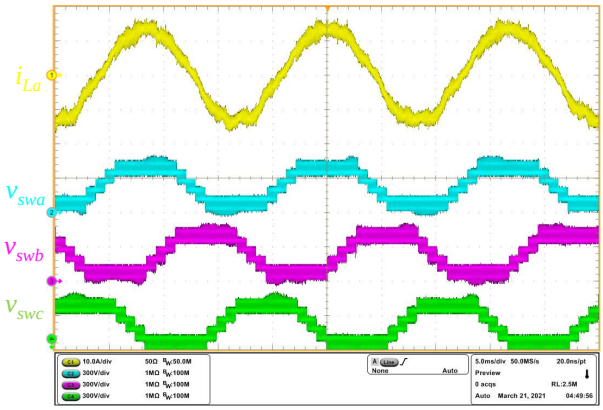

Figure 9.23: Three-phase FCML PFC inductor current and switching node voltages with the proposed dynamic carrier phase shift modulation. Test condition: 208 $V_{ac,LL}$ to 400 V_{dc}, 3 kW

The converter was tested at 400 V_{dc} input, 120 V_{ac}, with 360 W output power. Fig. 9.19 and Fig. 9.20 show the waveforms of three-phase six-level FCML converter with PSPWM only and with the proposed modulation strategy. Compared to the waveforms with PSPWM, the inductor current ripple with the proposed modulation is significantly reduced as predicted by the theoretical analysis. Moreover, the switching node voltages as shown in Fig. 9.21 indicate good balancing among flying capacitor voltages with the proposed modulation.

6 kW three-phase PFC experimental results

The proposed modulation technique is validated with the hardware prototype with a PFC control that is detailed in [81] under the condition: 120 $V_{ac,\ line\text{-}neutral}$ (208 $V_{ac,\ line\text{-}line}$) to 400 V_{dc}, up to 6.1 kW. From Fig. 9.22 and Fig. 9.23, it can be seen that the PFC control system is able to regulate the input current to be in-phase with the input voltage. Compared to the inductor current using only PSPWM wihtout any carrier phase control in Fig. 9.22, the proposed modulation scheme is able to significantly reduce the ripple current in PFC mode as well, as shown in Fig. 9.23. Moreover, zooming into one switching cycle, Figure. 9.24 and Fig. 9.25 experimentally verified the simulated waveforms in Fig. 9.13 that the proposed modulation method aligns the three switching node voltages, resulting in a inductor current ripple frequency that is twice as the effective frequency of the switching node voltage (2(N-1)f_{sw} for N-level FCML converters).

The three-phase PFC converter is tested up to 6.1 kW ac power with the air-cooled heatsink in Fig. 6.18, and the efficiency plot is shown in Fig. 9.26. The peak efficiency is 98.5%. The thermal image at 6.1 kW is shown in Fig. 9.28. Since the airflow from the

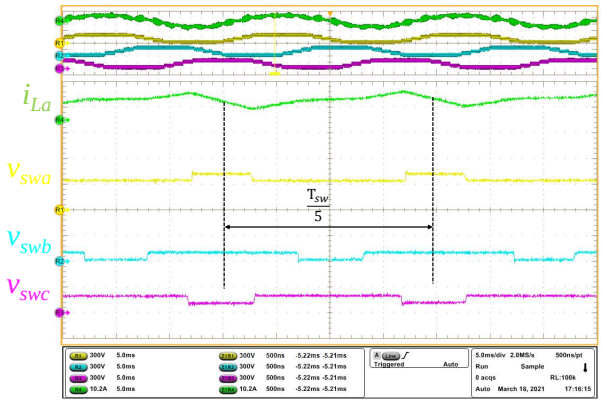

Figure 9.24: Switching node voltages and one phase inductor current of the three-phase PFC using PSPWM only without carrier phase shift control. As can been seen, the switching node voltages are not all center-aligned, and the inductor curren ripple has the same frequency as the switching node voltages.

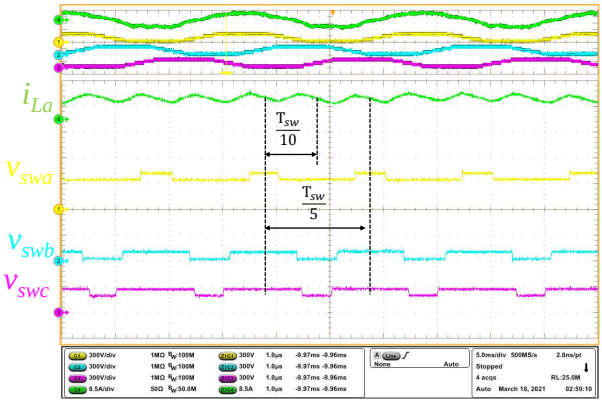

Figure 9.25: Switching node voltages and one phase inductor current of the three-phase PFC using the proposed dynamic carrier phase shift modulation. As can been seen, the switching node voltages are all center-aligned, and the inductor curren ripple has twice the frequency as the switching node voltages.

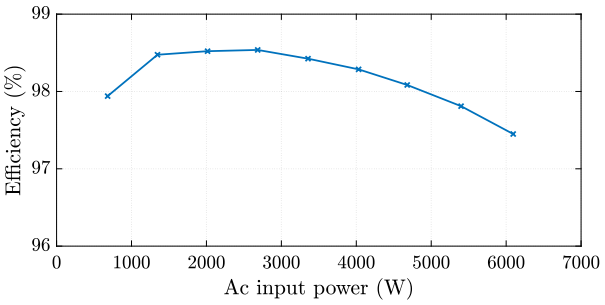

Figure 9.26: Measured efficiency plot up to 6.1 kW input ac power.

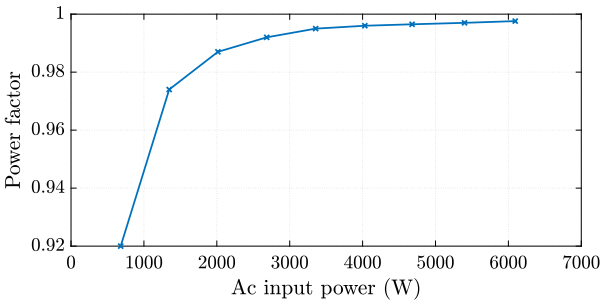

Figure 9.27: Measured power factor up to 6.1 kW input ac power.

electric fans was from the bottom to the top, the hottest module was on the top. Yet, with minimum airflow, the maximum temperature for the top module was reasonably maintained to be 66.8°C. The power factor is also measured and plotted in Fig. 6.11. As can be seen the proposed PFC controller can maintain power factor above 0.98 within most of the test power range. The key specifications and tested results are listed in Table. 9.2.

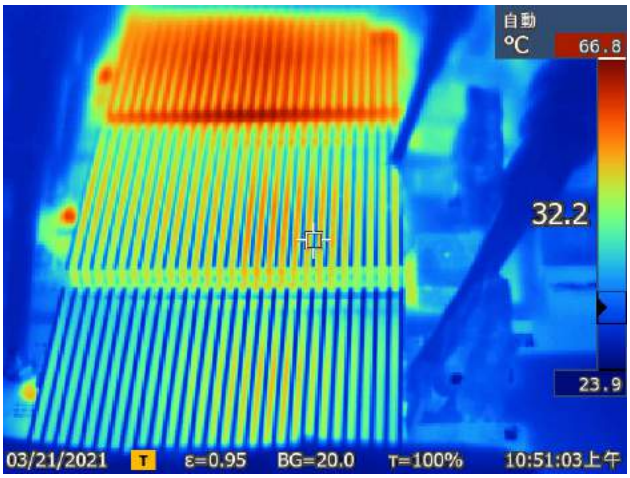

Figure 9.28: Thermal image at 6.1 kW. The airflow from small electric fans was from the bottom to the top.

Parameters	
Switching frequency	100 kHz
Effective frequency on inductor	1 MHz
SPI data clock	5 MHz
Input voltage	208 $V_{ac,LL}$
Output voltage	400 V_{dc}
Peak efficiency	98.5% @ 2.6 kW
Maximum tested power	6.1 kW
Efficiency @ 6.1 kW	97.5%

Table 9.2: Key performance metrics.

9.5 Conclusion

The proposed technique achieved identical inductor current ripple as SVPWM for three-phase FCML inverters, yet it also remains the benefit of PSPWM such as the natural balancing of the flying capacitor voltages. The reduction of current ripple allows the use of smaller inductor, reduces the conduction loss of power devices, and decreases the voltage ripple on the flying capacitors, which reduces the peak voltage stress on the power devices. As a result, power density and efficiency can be improved simultaneously. The benefits of the proposed technique have been verified with a compact hardware, along with a practical and scalable digital control implementation using a DSP and FPGA.

Chapter 10

Conclusions

This dissertation has presented solutions to improve the performance for single-phase and three-phase ac-dc converters. While the investigated circuit topologies, system architectures, and control techniques are specific to certain conversion scenarios, there are common fundamental ideas and practices that are the key enablers for the superior performances:

- **Leveraging high energy density passive components.** This idea is also behind many other efforts in the power electronics community to use high energy density capacitors are the main energy transfer devices rather than inductors. In the SSB, a full-bridge plus a support capacitor replaces the inductor in the passive LC notch filter; In the FCML full ripple port, the energy storage device is capacitor. For the main inverter/PFC stage, FCMLs also greatly improve the overall performance due to the use of high energy density capacitors as the flying capacitors. This is the same reason why hybrid dc-dc converters are achieving record power density and efficiencies [9], [84].

- **Systematic modeling, design trade-off study and optimization.** Power converter design is a multi-variable and multi-objective design problem. To quantitatively study the trade-offs among different design parameters and objective functions becomes important to arrive at designs with desirable features. The first effort is to develop more detailed and accurate models of the converters and components. For instance, the derating curves of the MLCCs are incorporated into the optimization process of the SSBs. Moreover, the nonlinear behavior of the MLCCs are considered for calculating losses for the FCML ripple port buffers. Nevertheless, developing more accurate loss models for MLCCs [23], [63], [85] and GaN switches [86] are active research areas by themselves, which can greatly benefit the design process of high performance converters. The second is that computational tools should be developed for multi-dimensional optimizations. The optimization for SSB in Chapter 5 is relatively simple to compute since we limited the problem to a certain number of variables and objectives of interests. Yet, it still captures the Pareto front trade-off curves and improves power density.

If more variables and objectives are included, more advanced optimization algorithms can be employed.

Besides the general modeling and optimization that are applicable to both single-phase and three-phase converters, different design philosophies of active buffers are also examined in this thesis. Active buffering itself is an active research topic that there are many different buffer topologies. From the two investigated buffers, we can see that while for each specific buffer topology optimizations can be done to improve its own performance, the limitations and tradeoffs within different buffer topologies are vastly different. Understanding the tradeoffs among buffer capacitor EUR, converter processed power and size is important when evaluating new buffer topologies for better performances.

- **Simplifying controls with more fundamental circuit analysis.** To control power converters and systems, it is key to have a good understanding of the desired behaviors of the converters. To control line-frequency behavior of ac-dc systems, abstracting the converters to be equivalent impedances, current and voltage sources can be very effective to identify key control parameters and reduce computation time in the actual controller. For instance, the PFC/SSB controller is developed using the phasor relations from the equivalent circuit analysis, which reduces the redundant parameters in the controller. To control power converters at switching frequencies, it is very important to draw out key switching states and associate waveforms. The proposed modulation technique for three-phase FCMLs is only possible after the phase-shift problem of FCML switching node voltages is identified in Fig. 9.4 and Fig. 9.5.

- **State-of-the-art digital controls.** To control PFC converters, active buffers and multilevel converters with numerous switches, state-of-the-art digital controllers such as DSP and FPGA are used in the hardware demonstrations. Careful design and implementation of the control firmware such as ADC timing and windowing, interrupt triggering, PWM generations, digital filters and feedback compensators, and communication links are essential to manage complicated systems such as the EV charger and the three-phase FCML PFCs. For instance, for controlling interleaved PFC for the EV charger, ADCs have to be triggered and maintained with correct time window to capture the circuit parameters. Yet, the ADC window cannot be too long to run into the computation budgets of the control subroutines for all the feedback and filters. On the other hand, the digital filters and compensators should be implemented efficiently to reduce the computing time. To control systems with multiple FCMLs or other multilevel topologies, using FPGAs to generate the needed high-count PWM signals is more feasible than DSPs [87]. As such, it is crucial to design communication links that are reliable in noisy environment for high power converters. The SPI link in the three-phase FCML converters is carefully designed in both hardware and software to ensure the stable communication between DSP and FPGA.

Chapter 11

Future work

11.1 Series-Stacked Buffers

Alternative ways to control v_{C2}

The ideal impedance of the SSB is to emulate a LC resonant tank at twice line frequency so that it can short all the twice-line frequency current into the buffer branch. Yet, due to the loss in the auxiliary converter, extra voltage ripple has to be induced to draw real power into C_2 with the control in Fig. 4.4. While the existing control does not require extra hardware, the fact that it has to draw real power into an ac port *ab* not only introduces more ripple, but also the stability and available power for loss compensation control are largely related to the source impedance R_s, as discussed in Section 4.3.

Essentially, as long as there is net positive charge injected into C_2 in every line cycle to compensate for the loss in the converter, the voltage can be controlled. To deliver the necessary charge, if extra hardware is used, the charge can be delivered from elsewhere other than port *ab*. Moreover, it can be delivered at other frequencies other than the twice line frequency. A potential solution is shown in Fig. 11.1. If a controlled current source I_{comp} is connected to C_2, the needed charge can be delivered. This current source can be controlled to be low ripple. For example, it can be realized with an inductor and associate switches switching at very high frequency. Because of the small switching ripple, the average of the current source can be regarded as a dc constant. With this method, the main control of v_{ab} and v_{C2} regulation is decoupled, and no more ripple at twice-line frequency will appear on the dc-bus.

The challenges of this method are to design the correct switching circuits to realize the current source behavior, and to design a feedback loop to control the current source based on the dc value of v_{C2}. Moreover, the switching actions from the current source should not interfere with the main full-bridge converter.

Once the control of v_{C2} is independent from the main buffer control, it opens up opportunities to solve many existing limitations of the SSB. Below are some of the potential topics worth investigating.

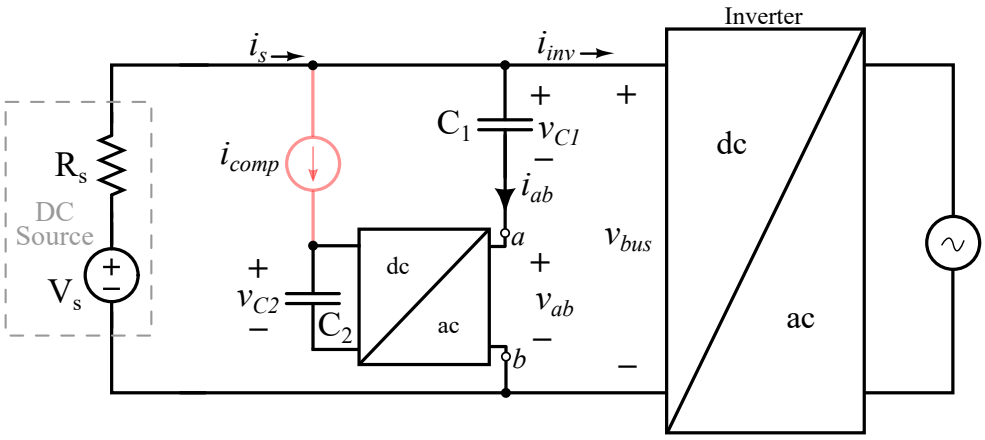

Figure 11.1: Potential charge injection solution to control v_{C2}.

Revisit current control together with new v_{C2} control

In [3], a hysteresis current control instead of voltage control in Chapter 4 was developed for the SSB. Instead of controlling the output voltage v_{ab} to cancel the voltage ripple on v_{C1}, the inductor current of the full bridge is controlled to be equal to the ac portion of the inverter current $i_{inv,ac}$. While such method requires extra current sensing and complicated hysteresis control, it actually enforces the current drawing into the buffer branch. Similar to the equivalent circuit for the power-port buffer in Fig. 2.16, if v_{C2} can be regulated independently from the ab terminals, the buffer current will be a controlled current load, and not related to R_s. As such, with very low R_s on the dc-side, it is worthwhile to explore the possibility of using the charge injection control and current control (hysteresis or average current control) together.

Operation under ac power with strong harmonics

One of the existing concern for SSB operating with strong ac harmonic is to control real power into the ab terminal. With extra harmonics, the real power into ab might also contain strong ripple power that makes v_{C2} hard to control. For instance, in Chapter 6.2, the v_{ab} is forced to be a pure sinusoidal voltage using PLL such that the low frequency disturbance on v_{C2} is much reduced. However, the control does ignore frequency content other than twice-line frequency, which increases the ripple on the dc-bus. If v_{C2} control is separated from v_{ab}, v_{ab} can be controlled to cancel all the harmonic voltages on v_{C1} with much less constraints.

Moreover, as [82] suggested, by injecting controlled current harmonics in the ac-side current for a conventional PFC with passive dc-bus capacitors, the capacitor size can be reduced. As such, it is also possible to reduce the capacitor size in the SSB, as the required energy storage is reduced with controlled harmonics.

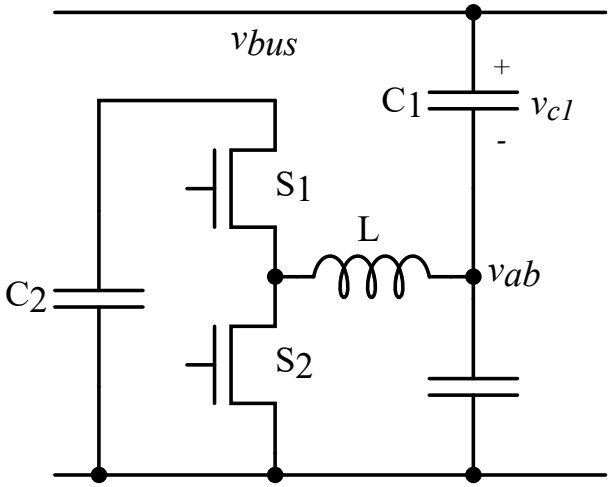

Figure 11.2: General half-bridge SSB schematic.

Improving transient response of PFC + SSB controller

While for PFC applications, the dc-side impedance is usually dominated by the load so that the v_{C2} loss compensation is not as challenging as in the inverter case with low dc-side impedance, the challenge remains in the transient response of the PFC controller. Classic PFC controller with a low-bandwidth voltage loop to scale the reference for the high-bandwidth current loop rely on the large dc-bus capacitor to handle the load transient. However, with SSB, the impedance at other frequency than the twice-line frequency is mostly just C_1. During load transient, a small C_1 will cause much higher voltage overshoot or undershoot than a large capacitor bank. Especially during load step-down, large overshoot could cause over-voltage damage to the PFC converter. The fundamental contradiction is that to minimize buffer size, the energy storage in the buffer should be minimized, yet for transient response, excessive energy storage is usually preferred.

With the existing control of v_{ab} and v_{C2}, the energy flow into the SSB is not able to be adjusted faster than the voltage loop of the PFC. One potential solution with the charge injection control of v_{C2} is that it is possible to charge C_2 to a very high voltage to absorb the excessive energy during transient events. While this method needs a higher voltage rated C_2, a high voltage swing can actually absorb lot of energy, as the change in energy scales with ΔV^2

More exploration on the half-bridge SSB

While the half-bridge SSB is explored in Chapter 7 to replace the filter capacitor in flyback adapter applications, the use of half-bridge in high power factor application in Chapter 3 to 6 has not been explored. With SSB, since the full-bridge output has no dc-bias and only

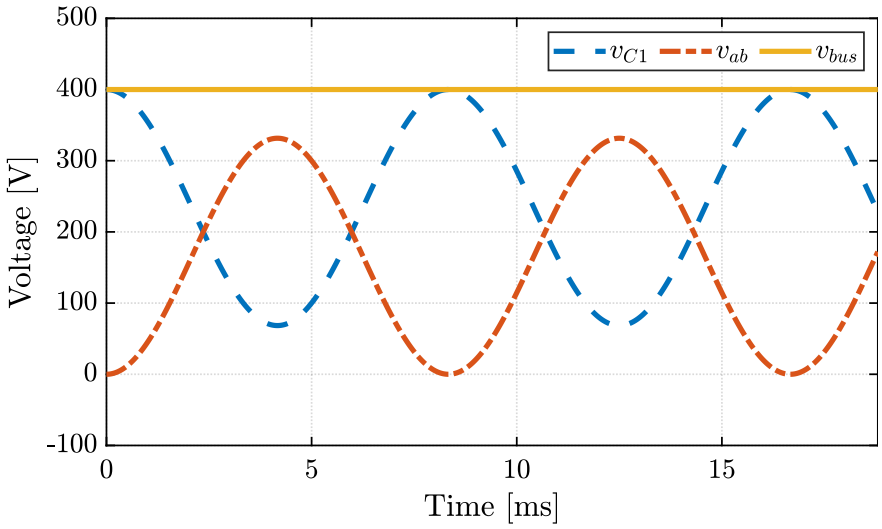

Figure 11.3: Typical waveforms for half-bridge SSB. $C_1 = 30\ \mu$F, 400 V dc-bus and 1.5 kW.

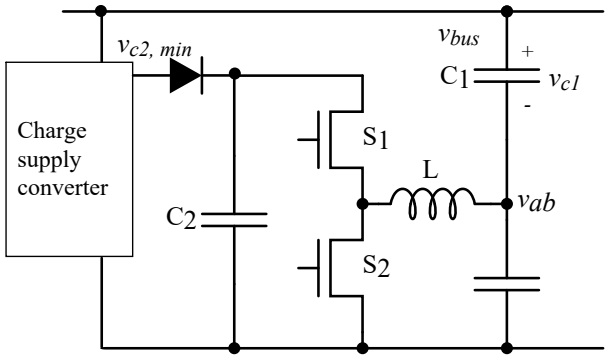

Figure 11.4: Half-bridge SSB with charge supply converter.

cancels the ripple on v_{C1}, the processed power is low so that the efficiency is high. However, since all the dc-bus voltage is biased on C_1, the voltage swing range on v_{C1} is quite limited by the voltage rating of the capacitor. Moreover, the capacitance density of non-linear MLCCs is usually low with high dc-bias. If the buffer converter can share some dc-bias with C_1, there would be an extra degree of freedom to optimize the operating voltage of the capacitor for higher overall power density. For example, for the 400 V_{dc}, 1.5 kW scenario in Chapter 5, C_1 can be just 30 μF using the half-bridge SSB in Fig. 11.2, with corresponding waveforms shown in Fig. 11.3. As can be seen, v_{C1} is allowed to operate with much higher ripple, and v_{ab} is still able to cancel the ripple component. However, as v_{ab} now has a dc-bias, the processed power is much higher compared to full-bridge solution. Thus, tradeoff studies are needed to determine the practical operating parameters. High performance FCMLs can also

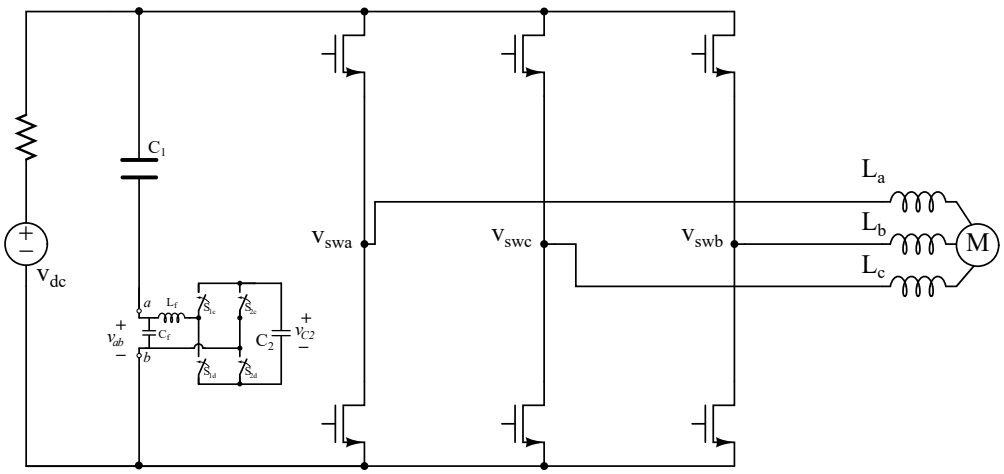

Figure 11.5: Use of the SSB in traction drive inverter applications.

be employed as the half-bridge to offset the efficiency cost due to the higher processed power. In terms of actual hardware implementation, as demonstrated in Chapter 7, the half-bridge design do not need isolated gate driver, isolated gate drive power, and differential sensing as for the full-bridge converter in SSB. The difference between this half-bridge SSB and the split-bus buffer in [83] is that C_2 does not directly connects to the dc-bus. In other words, the reactive power of the half-bridge is not provided from the dc source as in the split-bus buffer.

The simple method of using a diode to maintain the minimum voltage of v_{C2} in Fig. 7.3 is still applicable. If the bus voltage is too high for v_{C2} during operating, a buck converter as the charge supply in Fig. 11.4 can be implemented to provide intermediate voltage levels for $v_{C2,min}$. The converter will be very low-power as it only outputs current when v_{C2} is below its output voltage $v_{C2,min}$. Without the diode, the buck converter can also be actively controlled as a current source, which is essentially identical to the charge injection method in Fig. 11.1.

Using SSB in traction drive inverter dc-bus filtering

In traction motor drives in electrified transportation systems, the three phase inverter is usually operated with a few kilohertz switching frequency. By changing the filter transfer function in the control for the SSB to have high attenuation in kilohertz range, the inverter switching current ripple can be filtered out by the SSB if the full-bridge (or half-bridge) in the SSB are operated at higher frequencies such as hundreds of kilohertz, as shown in Fig. 11.5.

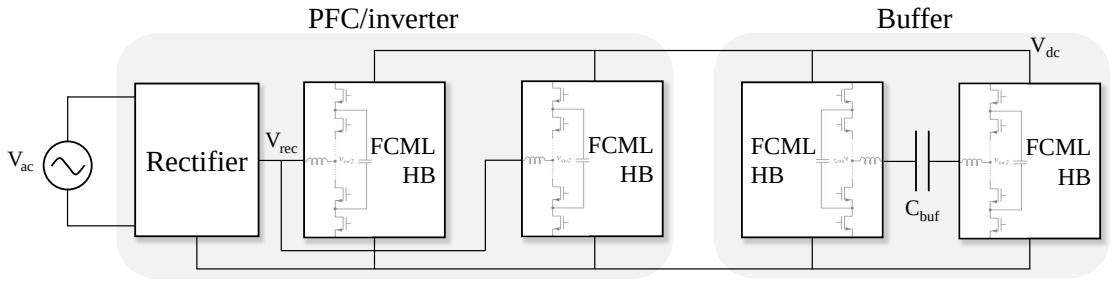

Figure 11.6: Integrated single-phase system with multilevel full ripple port.

11.2 FCML Bipolar Ripple Port

Full single-phase system demonstration

With the FCML modular design in Fig. 6.17, the FCML bipolar ripple port and the FCML inverter stage (or PFC) can be implemented with the digital control architecture for the three-phase FCML converter in Fig. 9.18. Four FCML modules can be utilized to construct a complete single-phase system, as shown in Fig. 11.6. There will be opportunities to couple the main PFC/inverter control with the ripple port buffer control. And it would be interesting to see if the smaller buffer capacitor can achieve high overall system power density.

Operation and control under ac power with strong harmonics

In Chapter 8, the control method to actively inject voltage harmonics into the capacitor is validated for ideal ac power with no higher order harmonics. If the ac power contains strong harmonics, it is possible to inject the correct amount of capacitor voltage harmonics to cancel them. Moreover, the capacitor size can also potentially be reduced if controlled harmonics are injected into the ac-side power on purpose [82].

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Appendix A

Control Software/firmware Implementation in TI C2000 DSP for 6 kW EV Charger

Figure A.1 shows the firmware setup and the main control functions for controlling the EV charger. First, the master PWM counter triggers the Start-of-Conversion (SOC) blocks when it reaches 0.5 duty (for both up and down counting as shown in the figure so that we can sense interleaved inductor current). SOCA/C and SOCB/D blocks in the DSP then trigger the assigned ADC channels to obtain voltages. Note that in C2000 DSP, there are four ADC modules: A,B,C, and D, and each module has a multiplexer selection 1,2,3,4. For the same ADC module, the conversion has to be queued. For instance, for ADC-A1 and ADC-A2, if they are triggered by the same SOC signal, A2 signal is converted after A1's window ends by default. On the other hand, different modules can converter at the same time. That is why in the ADC setup for the EV charger, there is no channel from the same module under each SOC group so that the conversion time can be shortened.

After ADCs are done with the conversion, they can send system interrupt signals for control subroutines. To make sure all the ADC modules have finished conversion, the End-of-Conversion (EOC) signals are sent by the channel with the longest window, which are D1 and D2 in the setup.

In the control subroutines triggered by EOC signals, the main PFC, inverter, and SSB control are implemented. Major computational tasks such as PI controller, moving average, Look-up table, PLL etc are illustrated. After all control computation, duty ratios for FCML1, FCML2, SSB are loaded to the corresponding ePWM registers; GPIOs for unfolder signals are also updated based on the angle information.

Source code repository: `https://github.com/DC37/charger-code`

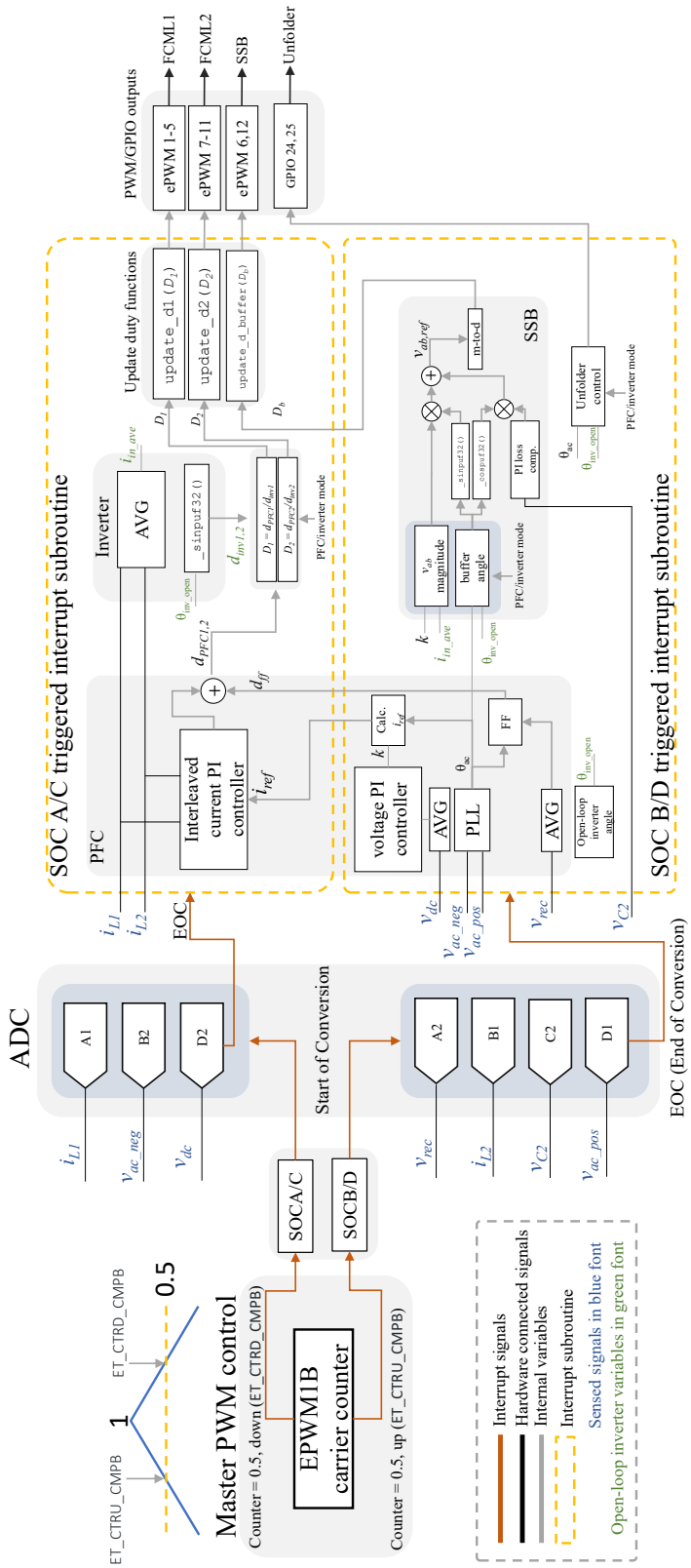

Figure A.1: Block diagram of the firmware setup and major computational tasks for of charger controller implemented in TI C2000 Delfino DSP.

Appendix B

Source code repositories for other projects in the dissertation

Since the control implementation of other projects can be relatively well-understood from the control block diagrams than EV charger, below are the repositories of the source code for:

- **FCML ripple port controlled with film capacitor:** `https://github.com/zliao555/fcml_buffer_film`
- **FCML ripple port controlled with MLCC:** `https://github.com/zliao555/fcml_buffer_MLCC`
- **Half-bridge SSB for flyback:** `https://github.com/zliao555/flyback_SSB`
- **Three phase FCMLs:** `https://github.com/zliao555/three_phase_FCML`