Integrated Hybrid Switched-Capacitor Converters for Point of Load Power Delivery

Pourya Assem
Robert Pilawa-Podgurski, Ed.

Electrical Engineering and Computer Sciences
University of California, Berkeley

Technical Report No. UCB/EECS-2022-243
http://www2.eecs.berkeley.edu/Pubs/TechRpts/2022/EECS-2022-243.html

December 1, 2022

Integrated Hybrid Switched-Capacitor Converters for Point of Load Power Delivery

by

Pourya Assem

A dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Engineering- Electrical Engineeing and Computer Sciences

in the

GRADUATE DIVISION

of the

UNIVERSITY OF CALIFORNIA, BERKELEY

Committee in charge:

Accociate Professor Robert Pilawa-Podgurski, Chair
Professor Seth R. Sanders
Accociate Professor Duncan Callaway

Fall 2020

Integrated Hybrid Switched-Capacitor Converters for Point of Load Power Delivery

by

Pourya Assem

Abstract

Integrated Hybrid Switched-Capacitor Converters for Point of Load Power Delivery

by

Pourya Assem

Doctor of Philosophy in Engineering- Electrical Engineeing and Computer Sciences

University of California, Berkeley

Accociate Professor Robert Pilawa-Podgurski, Chair

The Hybrid Switched-Capacitor (SC) converters have shown potentials for higher efficiency and power-density compared with magnetic and pure SC converters. These advantages have driven new architectures and control schemes suitable for power converters integration in advanced CMOS technology nodes by alleviating the device stress and size. This work focuses on integration of the popular hybrid Dickson SC and cascaded resonant SC converters for high efficiency and power-density DC-DC conversion in datacenter and embedded applications covering few mW to hundreds of W load range.

The first test chip is a hybrid Dickson SC converter for battery powered embedded and mobile applications where the demand focuses on high efficiency and power-density across a large conversion ratio of 3.4 V - 4.2 V for Lithium-ion batteries down to 0.3 V - 0.9 V with load range up to 1.5 A for digital processors and peripherals in advanced CMOS technology nodes. The second test chip is dual-phase time-interleaved extension of the hybrid Dickson SC converter designed with coupled-inductor and multiple outputs for application in multi-core processors with dynamic voltage scaling. The focus of the second test chip is improved efficiency through time-based control and dual-phase operation as well as a higher power-density through compact die-stacked packaging of passive components. The converter is designed for input voltage range of 3.2 V - 3.6 V DC bus conversion down to load voltage of 0.7 V - 1 V with load range up to 1.4 A. The third test chip integrates gate-driver, bootstrap and control peripherals of the cascaded discrete resonant SC converter for higher power conversion from 48 V DC bus down to 6 V intermediate bus. The focus of the third test chip is design of a single-package peripheral for improved efficiency and power-density. In addition, integrating the start-up and shutdown peripherals enables hot swapping in datacenter applications.

Accociate Professor Robert Pilawa-Podgurski
Dissertation Committee Chair

To my parents for all their support.

Contents

List of Figures

List of Tables

Acknowledgements

First and foremost, I like to thank my advisor for his support. It was a pleasure to work and collaborate with my colleagues Wen-Chuen Liu and Yutian Lei on development of the work presented in the Chapter 2 and Zichao Ye on development of the work presented in Chapter 4. I also like to thank Christopher Barth, Shibin Qin, Zitao Liao, Nathan Pallo, Charles Hill, Kelly Fernandez, Samantha Coday, Margaret Blackwell, Rose Abramson, Derek Chou, Nathan Brooks and all the current and past group members for friendship and support and our industry sponsors and collaborators from Texas Instruments.

Chapter 1

Introduction

The power management system for point-of-load power delivery (PoL) from the 48 V bus has gained attention in several large scale applications from which the data centers and telecommunication industry can be pointed out. A typical power management system with growing popularity, as shown in Fig. 1.1, consists of a two-stage topology. The first stage is designed to convert the 48 V DC bus to an intermediate bus voltage feeding a number of the second stage converters for PoL power delivery. The first stage topology should be selected to be highly efficient and achieving high power density, as it performs the bulk of voltage conversion, while the loading transient and regulation can be relaxed by operating in open-loop. Meanwhile, the second stage converters should add a high bandwidth transient handling for line and load regulation with the PoL voltage domain residing in the typical 0.7 V to 3.3 V interval for advanced CMOS processes. The first stage is typically occupying a larger area as the high voltage passive and active components can be bulky. Hence, from a physical design stand point and power-density consideration it is the most optimal to have a single first stage in the system hierarchy design. Thus, the two-stage architecture enables modular and flexible physical design of the PoL power delivery systems by placing the more compact second stage converters throughout the system and close to the load. However, the increased physical distance between the two stages should be treated carefully as the parasitic elements of the long PCB traces delivering large current values can introduce efficiency loss and noise coupling to sensitive signal lines with potential signal integrity issues.

The long PCB traces with undesired resistive and inductive parasitic elements can limit the efficiency and transient performance of the power management systems. A conventional approach to this design challenge is development of the system around a current regime at a intermediate voltage which ensures the efficiency and transient response of the system is not impacted by the physical design constraints as well as meeting the voltage and current stress limits of both stages of the converter in advanced CMOS processes. Hence, it is important to note that the practical selection of intermediate voltage is critical to the application. Selection of a low intermediate voltage leads to distribution of large DC currents from the first stage in order to maintain the rated power delivery. This in turn introduces additional conduction loss because of PCB traces parasitic resistance and decreases the efficiency of power management systems. In addition large steps of DC currents can lead to a significant ESR transient at this unregulated node. Furthermore, the parasitic inductance of long PCB traces can introduce additional undesired ringing transients as

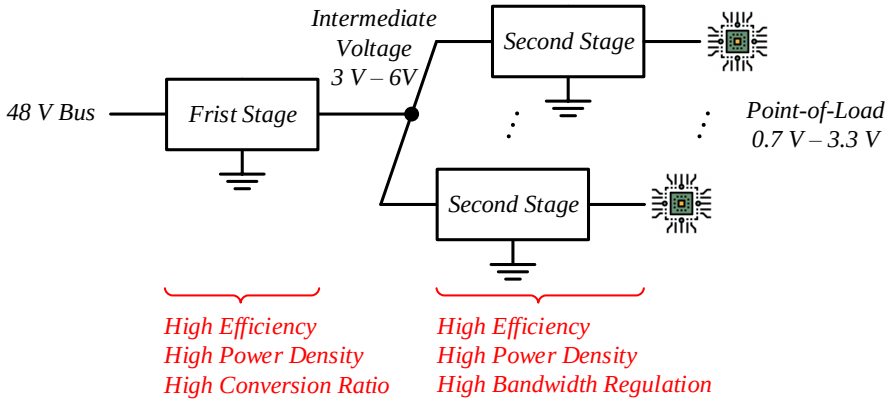


Figure 1.1. The two-stage power management system for 48 V bus to PoL delivery.

the intermediate voltage goes through large DC current load steps. On the other hand, selection of a large mid-point voltage increase the voltage stress on the second stage converter, where it was primarily designed to perform a high-bandwidth regulation. A large voltage stress requires selection of high voltage and bulky devices which reduces the bandwidth of the second stage converters, which are typically designed with either a high-frequency bulk converter, linear regulator or a hybrid of the two. In addition, the second stage converters designed with linear regulator architecture will take a heavy toll on efficiency as the dropout voltage increases. Hence, most systems are designed with intermediate voltage in the 3 V - 6 V range.

This works investigates the advantages of hybrid switched-capacitor (SC) converters in the design of the both converter stages as higher efficiency and power-density can be achieved compared with the conventional magnetic and pure SC converter topologies. These advantages have driven new architectures and control schemes suitable for power converters integration in advanced CMOS technology nodes by alleviating the device stress and size. This work focuses on integration of the popular hybrid Dickson SC and hybrid cascaded resonant SC converters for DC-DC conversion in datacenter and embedded applications covering few mW to hundreds of W load range.

The first CMOS integrated power converter is a hybrid Dickson SC converter for battery powered embedded and mobile application where the demand focuses on high efficiency and power-density across a large conversion ratio of 3.4 V - 4.2 V for Lithium-ion batteries down to 0.3 V - 0.9 V with load range up to 1.5 A for digital processors and peripherals in advanced CMOS technology nodes. A power-density of 330 mW/mm^2 and a peak efficiency of 92.6% with effective switching frequency of 1 MHz. The converter is packaged using flip-chip in 65 nm CMOS technology with passive devices co-packaged through a high-density interposer to minimize the packaging parasitics and volume. A segmented gate-driver is used to enhance the converter efficiency and reliability by maintaining low voltage ringing across the power switches. The converter is integrated with closed-loop output voltage regulation, deadtime control and active capacitor voltage balancing to maximize the active and passive device utilization. The short comings of the first test chip design, such as large RMS current, expensive packaging and a single regulated output is improved and redesigned in a second test chip.

The second CMOS integrated hardware prototype is a dual-phase time-interleaved extension of the hybrid Dickson SC converter designed with coupled-inductor and multiple outputs for application in multi-core processors with dynamic voltage scaling. The focus of the second converter

design is improved efficiency through utilization of coupled-inductor for reduced RMS current and time-based control in a dual-phase operation as well as higher power-density through a compact die-stacked packaging of passive components. The converter is designed for input voltage range of 3.2 V - 3.6 V DC bus conversion down to load voltage of 0.7 V - 1 V for digital processors conversion and load range up to 1.4 A. The two-stage topology of each converter phase is comprised of first-stage hybrid Dickson switched-capacitor 4:1 step-down converter and second-stage ordered power delivery operating at 20MHz with four regulated outputs. The increased switching frequency enables utilization of smaller inductor values as well as improved transient handling of the converter. An all-digital sensor-less current-mode control, replacing sensitive analogs, synchronizes the energy flow between the two stages of each converter phase to maintain the inductor steady-state current. The active flying capacitor balancing peripherals is utilized for reliable operation of the first-stage. The modulator, controller peripherals and the power stage switches are integrated and only external flying capacitors and coupled-inductor are required. The stacked on-die flying capacitors and chip-on-board packaging reduces the converter footprint and improves the power density as well efficiency by reducing parasitic losses. The converter is designed in 65 nm bulk CMOS technology. A peak efficiency of 88.3% and power density of 450mW/mm^2 is measured.

With the first two test chip focusing on the second stage converter, as shown in Fig. 1.1, the third focus of this dissertation is designed to investigate the first stage converter. The third test chip integrates gate-driver and support peripherals of a discrete converter for higher power conversion from 48 V DC bus down to 6 V intermediate bus. The focus of the third test chip is design of a single-package peripheral for the hybrid resonant SC 2:1 switching cell. A quad gate-driver is proposed to improve the power-density and efficiency of the existing architecture. The designed chip integrates the controller, level-shifter, an active bootstrap and gate-driver along with start-up and shutdown peripherals to reduce the parts count. The power stage active and passive components are implemented using discrete components. A three-stage cascaded resonant SC converter with 8:1 conversion ratio from $48V$ DC bus is designed using the custom quad gate-driver chip with pick efficiency of 97.8% and $30A$ load range. The next three chapter of the dissertation focuses on design of each test chip in detail with hardware measurements and comparison to the state-of-the-art prior works.

Chapter 2

Hybrid Dickson SC Converter with Split-Phase Control

2.1 Introduction

Emerging technologies like the internet of things, wearable electronics and embedded biomedical devices can greatly improve quality of life, but the limited capacity of energy sources and power converters remains a challenge. In such applications, digital circuits operate at low voltages, typically below 1 V, in order to reduce the power consumption. In addition, memories [1, 2], near-threshold and subthreshold digital processors [3, 4] operating in the 0.3-0.9 V range have shown a promising figure-of-merit in energy efficient computation in advanced CMOS processes. Capturing this opportunity is challenged by the fact that Lithium-ion battery cells are commercially available in the 3.4-4.2 V voltage range. Recent designs for mobile computing also incorporate dynamic frequency voltage scaling technique [5, 6] for more active and aggressive power saving, which motivates the need for compact power converters capable of large conversion ratios with wide and efficient voltage regulation across the full load range.

Conventional buck converters [7, 8, 9] employ an inductor as intermediate energy storage, which dominates the size and leads to low power density because of the relatively low energy density of inductors compared to capacitors [10]. It is also challenging for conventional buck converters to simultaneously achieve high power density and efficiency at large conversion ratios, due to the large device voltage stress, i.e. full input voltage, relative to the output voltage. This causes poor device utilization, because higher voltage devices with larger on-resistance (R_{DS}) per area are required and may not be available in advanced low voltage bulk CMOS processes. Another option, the SC converters [11, 12, 13] achieve improved device utilization [14]. However, the inherent charge sharing loss within SC converters has limited their achievable power density and efficiency, in particular for large conversation ratios. In [15, 16] high capacitance density processes, e.g., deep trench or ferroelectric capacitors, and high switching frequency are employed in order to reduce charge sharing loss, but these processes are expensive and not commercially available. Moreover, the conventional

SC converters suffer from poor efficiency when operated outside the native fixed ratios, or under output voltage regulation. Although adjustable conversion ratio SC converters [17, 18, 19] enable a wider output voltage range, with somewhat improved efficiencies, they inevitably require more power switches and sacrifice of the power density. Recent hybrid SC converters such as the merged two-stage converter [20], three-level buck converter [21, 22], resonant SC converter (ReSC) [23] and hybrid Dickson converter [24, 25] have eliminated charge sharing loss and increased the capacitor utilization by allowing larger capacitor voltage ripple through soft-charging operation [27, 28], which increases the power density by either increasing the current or reducing the capacitor size. This increase in power density comes at the cost of more challenging capacitor voltage balancing, which may require active balancing techniques, or - in many cases - can be addressed through design choices that enable natural balancing. Compared to the SC converters, hybrid SC converters achieve higher device utilization by taking advantage of the SC converter cascaded topology, while also achieving high efficiency under continuous output voltage regulation. In addition, the hybrid SC converters offer increased power density by reducing the inductor size through increased effective switching frequency and reduced voltage magnitude seen by the inductor compared to the conventional buck converters. This work presents an integrated hybrid SC converter based on the Dickson SC topology with an LC output filter and split-phase control to achieve complete soft-charging operation [24] across a continuously regulated [29] output voltage.

2.2 Hybrid Dickson SC Converter

The Dickson SC converter achieves good device utilization, by reducing the required blocking voltage of power switches to V_{OUT} and $2V_{OUT}$, where $V_{OUT} = V_{IN}/N$ given V_{IN} and N are the input voltage and the native conversion ratio of the Dickson SC converter. This allows the use of lower voltage rating devices with lower R_{DS} per area, and hence the potential to achieve high efficiency and high power density. However, the inherent charge sharing loss in conventional Dickson converters leads to poor capacitor utilization, where the voltage ripple, and subsequent charge transfer to the output from the capacitors must be limited [24]. The hybrid Dickson converter, as shown in Fig. 2.1, eliminates the charge sharing loss by addition of an inductor, L, to the output of the conventional Dickson converter. However, the conventional two-phase control of the hybrid Dickson SC converter still results in a residual charge sharing loss. Therefore, the split-phase control [24] of the hybrid Dickson SC converter is utilized to achieve a complete elimination of the charge sharing loss.

The gate control signals for the conventional two-phase control and the split-phase control are shown in Fig. 2.2(a) and 2.2(b), respectively. All possible switching phases of the hybrid Dickson converter are given in Fig. 2.3, where flying capacitors C_1, C_2 and C_3 are either charged or discharged through the inductive current source load, yielding a smooth current to charge or discharge the capacitors (soft-charging). On the contrary, in conventional operation (hard-charging), the flying capacitors are directly connected to the large output capacitor, C_{OUT}, which acts as a voltage source load. Therefore, a large current transient is expected during the phase switching instances due to the capacitor voltages mismatch in hard-charging operation, which results in significant charge sharing loss [24].

As can be seen from Fig. 2.4(a) simulation results with all equal flying capacitor value of 4 μF and 20 mΩ switch resistance, for the two-phase control soft-charging operation the KVL constraint of $V_{IN} - V_3 = V_2 - V_1$ in phase ϕ_{2A} cannot be satisfied during the transition from phase ϕ_{1A} to

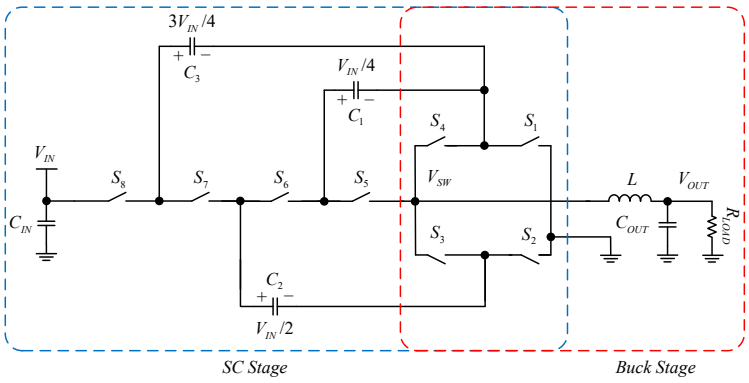


Figure 2.1. The hybrid Dickson SC converter.

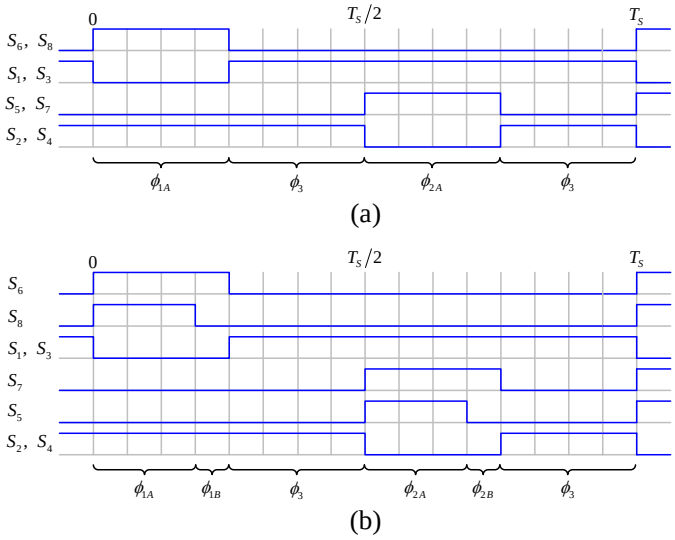


Figure 2.2. Gate control signals for 50% duty-cycle of (a) two-phase control and (b) split-phase control of the hybrid Dickson converter.

phase ϕ_{2A}. This leads to incomplete soft-charging operation with residual charge sharing loss in capacitors, which can be observed from the spiky capacitor current, as shown in Fig. 2.4(c). In the split-phase control operation, buffer phases ϕ_{1B} and ϕ_{2B} are added to reconfigure the capacitor branches of the hybrid Dickson converter to be selectively charged or discharged, so that there is no voltage mismatch during phase transitions and KVL constraint are met, as shown in Fig. 2.4(b). As a result, with the same simulation parameters, smooth capacitor current can be observed, as shown in Fig. 2.4(d). The split-phase control technique achieves complete soft-charging operation by eliminating the charge sharing loss, which is a major source of power loss in the conventional SC converters. The RMS and large peak current stress through the capacitors and power switches are greatly reduced, and hence the converter efficiency, reliability and aging can be improved. The steady-state voltage and current stresses for each power switch are shown in Fig. 2.5. The steady state voltages across C_1, C_2 and C_3 are $V_{IN}/4$, $V_{IN}/2$ and $3V_{IN}/4$ respectively as shown in Fig. 2.1.

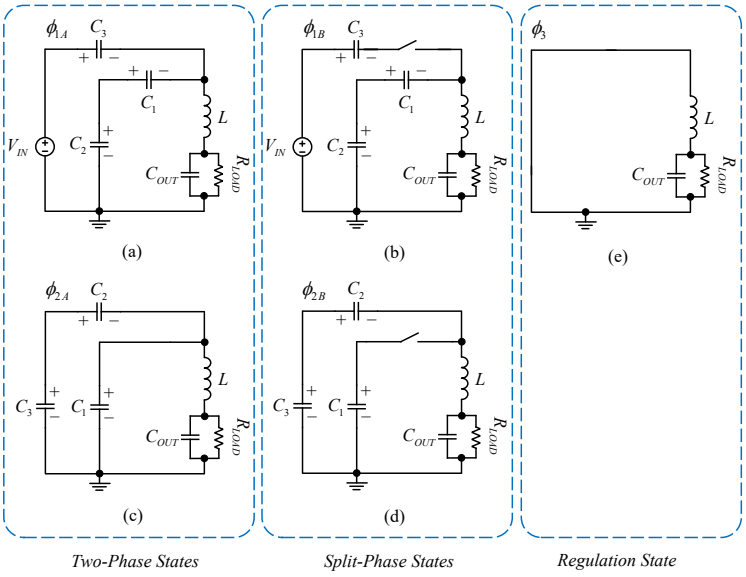


Figure 2.3. Operating phases of the hybrid Dickson converter (a) phase ϕ_{1A}, (b) phase ϕ_{1B}, (c) phase ϕ_{2A}, (d) phase ϕ_{2B} and (e) phase ϕ_3.

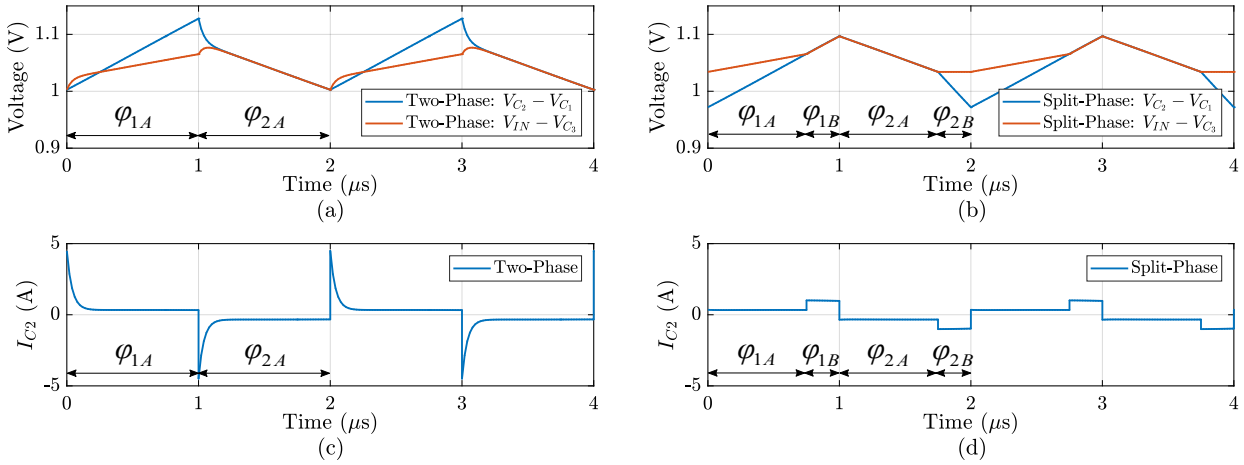


Figure 2.4. Simulated voltage and current waveforms of the hybrid Dickson SC converter in SSL region for 100% duty-cycle. (a) Two-phase control voltages, (b) split-phase control voltages, (c) two-phase control I_{C_2} current and (c) split-phase control I_{C_2} current.

The output referred impedance R_{SC} of a SC converter [14], considering both the capacitor charge sharing loss and the conduction loss, can be modeled by:

$$R_{SC} = \frac{\frac{V_{IN}}{N} - V_{OUT}}{I_{OUT}} \tag{2.1}$$

where N is the conversion ratio and I_{OUT} is the output current. It is important to note that this model does not capture the switching loss of gate drivers and related control peripheral circuits.

Switch \ Phase	ϕ_{1A}	ϕ_{1B}	ϕ_{2A}	ϕ_{2B}	ϕ_3
S_1 & S_3	V_{IN} / 4	V_{IN} / 4	I_{OUT} & I_{OUT} / 2	I_{OUT}	I_{OUT} / 2
S_2 & S_4	I_{OUT} / 2 & I_{OUT}	I_{OUT}	V_{IN} / 4	V_{IN} / 4	I_{OUT} / 2
S_5	V_{IN} / 4	V_{IN} / 4	I_{OUT} / 2	V_{IN} / 4	V_{IN} / 4
S_6	I_{OUT} / 2	I_{OUT}	V_{IN} / 2	V_{IN} / 2	V_{IN} / 2
S_7	V_{IN} / 2	V_{IN} / 2	I_{OUT} / 2	I_{OUT}	V_{IN} / 2
S_8	I_{OUT} / 2	V_{IN} / 4	V_{IN} / 4	V_{IN} / 4	V_{IN} / 4

Figure 2.5. The steady-state voltage and current stresses for each power switch.

It is desirable to minimize R_{SC} to increase the efficiency of the converter. The split-phase control for complete soft-charging operation yields a low R_{SC} independent of the switching frequency, because the frequency dependent charge sharing loss is eliminated [24]. The significant reduction of R_{SC} in the slow switching limit (SSL) compared with the hard-charging operation enables the hybrid Dickson SC converter to operate with a larger capacitor voltage ripple in SSL without compromising the efficiency. Increasing the capacitor utilization can potentially increase the power density by reducing the capacitor size or switching loss in the SSL region.

For the hybrid Dickson SC converter, the output voltage regulation can be achieved by the addition of phase ϕ_3 after ϕ_{1B} and ϕ_{2B} phases. By simultaneously turning on S_1 to S_4 to achieve phase ϕ_3, the switching-node voltage V_{SW} can be momentarily connected to ground to resemble a buck converter operation. The adjustable duty-cycle, D, enables a continuous V_{OUT} range after the LC output filtering, as shown in Fig. 2.6. The output voltage is calculated using the equation below:

$$V_{OUT} = \frac{DV_{IN}}{N} \tag{2.2}$$

where D is calculated from phases $\phi_{1A} + \phi_{1B}$ and phases $\phi_{2A} + \phi_{2B}$ over the T_S period. In Fig. 2.6, it should be noted that the regulation phase ϕ_3 appears twice in each complete switching cycle, effectively doubling the pulse frequency seen by the inductor, without increasing the switching frequency of individual power switches and peripheral circuits. The slight difference between the magnitude of phases $\phi_{1A} + \phi_{1B}$ and $\phi_{2A} + \phi_{2B}$ is a result of active capacitor voltage balancing hysteresis band for full system simulation shown in Fig. 2.6. Details of the hysteresis band and control are provided in Section 2.3.

2.3 Implementation

The hybrid Dickson SC converter was implemented in 65 nm bulk CMOS process, which enables application of the proposed on-chip power management compatible with the most advanced system-on-chip and mixed signal designs to be co-integrated on the same process. The process offers CMOS transistors suitable for the converter operating range. The low density and Q-factor of integrated

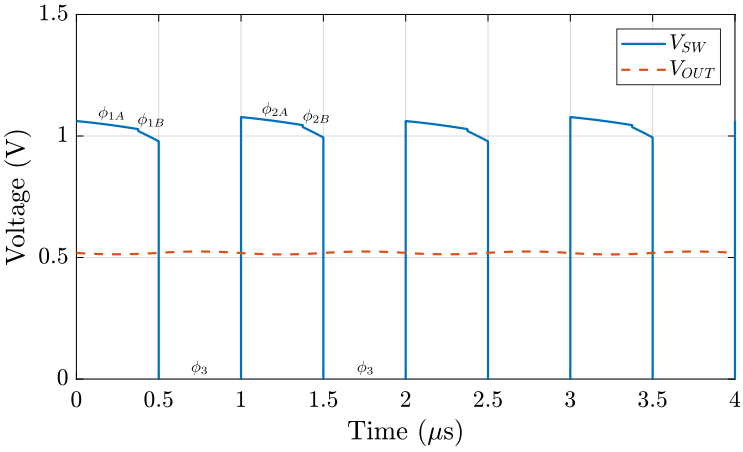


Figure 2.6. Simulated switching node V_{SW} and output voltage V_{OUT} for 50% duty-cycle of split-phase control.

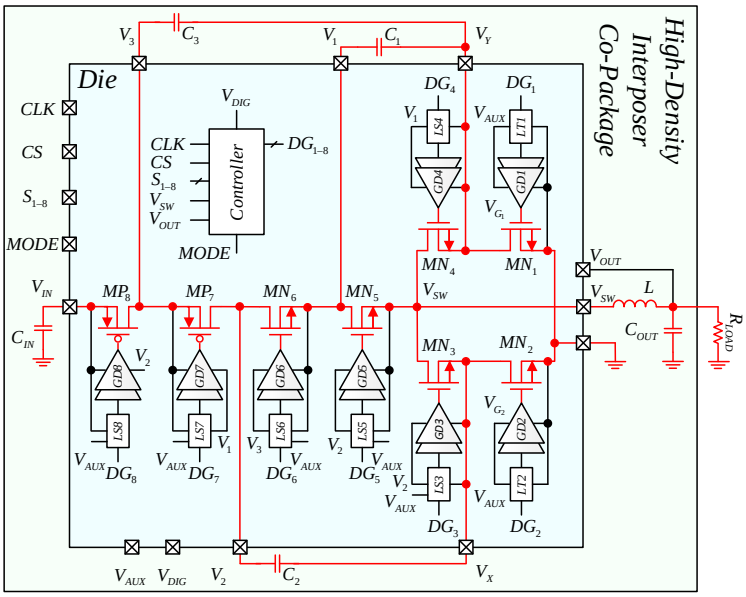


Figure 2.7. Converter top-level implementation and co-packaging of passive components.

passive capacitors and inductors present a challenge for practical implementation of the power converter to achieve high power density and efficiency. Therefore, co-packaging of discrete passive components was employed in this work to meet the performance targets. Figure 2.7 shows the high-level schematic diagram of the hybrid Dickson SC converter with power switches and passive components. A high-level schematic drawing of controller shown in Fig. 2.8. Each sub-block design is discussed in the following subsections. Table 2.1 shows the converter design specifications.

The flying capacitors C_1, C_2 and C_3 as well as input decoupling capacitor C_{IN}, output filter capacitor C_{OUT} and output inductor L are assembled through the high density interposer co-package solution. The power switches MN_1-MP_8 are fully integrated along with the gate-drivers GD_1-GD_8 and level-shifters LS_3-LS_8. The ground referred gate-drivers GD_1-GD_2 use level-translators. The

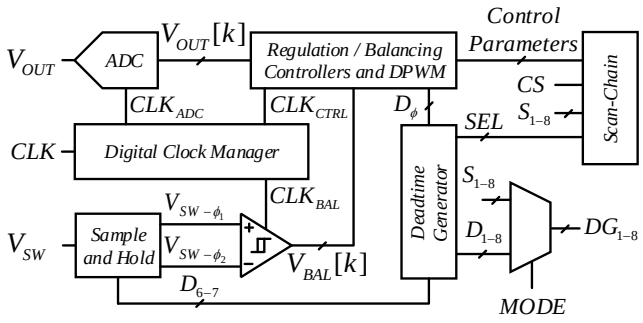


Figure 2.8. Converter controller high-level diagram.

Table 2.1. Converter specifications.

Specification	**Rated**
Input voltage V_{IN}	3.4-4.2 V
Output voltage V_{OUT}	0.3-0.9 V
Output regulation step	20 mV
Output current I_{OUT}	0.1-1.5 A
Power density	330 mW/mm^3
Switching frequency f_{SW}	500 kHz
Output voltage ripple ΔV_{OUT}	$< 4\%$ (10 mV)

converter was implemented with a fully on-chip controller and ADC for closed-loop output voltage regulation as well as deadtime controller and active flying capacitor voltage balancing controller. The digital pulse width modulator (DPWM) is clocked via the CLK pin to generate the control signals D_{1-8} for the power switches. The digital clock manager (DCM) is embedded within the DPWM block and generates the working clocks of controllers, scan-chain and peripheral circuits. Additionally, the converter can be operated using an external controller via the S_{1-8} pins by bypassing the internal controllers. The scan-chain is used for debugging and externally adjusting the converter control parameters. The internal controllers are powered through the digital voltage V_{DIG} provided by an external supply. In addition, V_{AUX} supplies the level-shifters and ground referred gate-drivers. The flying capacitors precharge circuit was implemented externally. Below, the circuit design and implementation of each system block is presented.

2.3.1 Power Switch Sizing and Floorplan

The power switches sizing and floorplan optimization of the converter are constrained by the efficiency and power density, given a fixed active die area for a compact co-packaging solution. In this design, we limited the active die area to the combined footprint areas of the capacitors C_1, C_2, C_3, and C_{IN}. The power switches and flip-chip (FC) pins floorplan are designed to minimize the parasitic inductance and resistance in the current loops, to and from the flying capacitors, as a measure to reduce the ringing overshoots. The normalized power switches charge vector q_{SW} [24] for the split-phase control can be used to determine the relative power switches size for the switches R_{DS} values in order to optimize the loss and area. The switch charge vector q_{SW}, relative power

Table 2.2. The q_{SW} and power switch sizing for split-phase control.

Power Switch	q_{SW}	V_{GS}	V_{DS}	**Relative Size**
MN_1	$\sqrt{3}$	$V_{IN}/2$	$V_{IN}/4$	$\sqrt{3}$
MN_2	1	$V_{IN}/2$	$V_{IN}/4$	1
MN_3	1	$V_{IN}/2$	$V_{IN}/4$	1
MN_4	$\sqrt{3}$	$V_{IN}/4$	$V_{IN}/4$	$2.5 \times \sqrt{3}$
MN_5	1	$V_{IN}/2$	$V_{IN}/4$	1
MN_6	1	$V_{IN}/2$	$V_{IN}/2$	1
MP_7	1	$V_{IN}/2$	$V_{IN}/2$	3
MP_8	1	$V_{IN}/2$	$V_{IN}/4$	3

switch size, gate driving voltage V_{GS} and voltage stress V_{DS} of the power switches are shown in Table 2.2. The power switch sizes are adjusted for the applied V_{GS} under the $V_{IN} = 3.4$ V minimum operating voltage of the Lithium-ion battery cell. To avoid bootstrap circuits for gate driving, the power switches MP_7 and MP_8 are chosen to be the PMOS type devices, which requires $3X$ channel width to match the R_{DS} of the NMOS type devices. This trade-off yet saves significant area when compared with the required area for on-chip or external bootstrap capacitors for gate drivers. In addition, the power switch MN_4 gate-driver is supplied by $V_{GS}/4$, which requires additional $2.5X$ increase in channel width to match the R_{DS} value.

2.3.2 Regulation and Capacitor Voltage Balancing

The output voltage regulation controller consists of a flash ADC and a digital PI compensator. The regulation signal chain and DPWM blocks are co-designed with the active flying capacitor voltage balancing controller which consists of sample and hold circuit, hysteresis comparator and a P/I compensator. The design and circuit implementation of these blocks are discussed below:

ADC

The ADC is designed for 32 linear steps over the range of $V_{min} = 0.28$ V to $V_{max} = 0.92$ V, which covers the required output voltage regulation range of 0.3-0.9 V as specified in Table 2.1. The 5-bit ADC was designed using a flash architecture given the low number of quantization levels as well as providing only a single clock-cycle conversion latency. The circuits and functional block of the designed flash ADC is shown in Fig. 2.9. The 5-bit resolution requires 31 comparators and 32 resistive elements to provide the reference voltage values evenly spaced in the $V_{min} - V_{max}$ range. The resistive voltage reference ladder was compensated with MOS capacitors $C_1 - C_{32}$ in order to provide stable reference voltage values with maximum quiescent current of 15 μA. The inverter-based comparator was designed using the zero-null architecture. The operation of a zero-null comparator is based on biasing the INV_1 inverter at its meta-stability condition, where any offset signal applied to its input triggers INV_1 toward the corresponding stable condition at either high or low states. Hence, the operation of the zero-null comparator is divided into charging and evaluate phases. In the charging phase, the C_{REF} capacitor is charged to the voltage difference between ADC reference voltage of corresponding level, V_{-}, and meta-stability voltage of INV_1. In

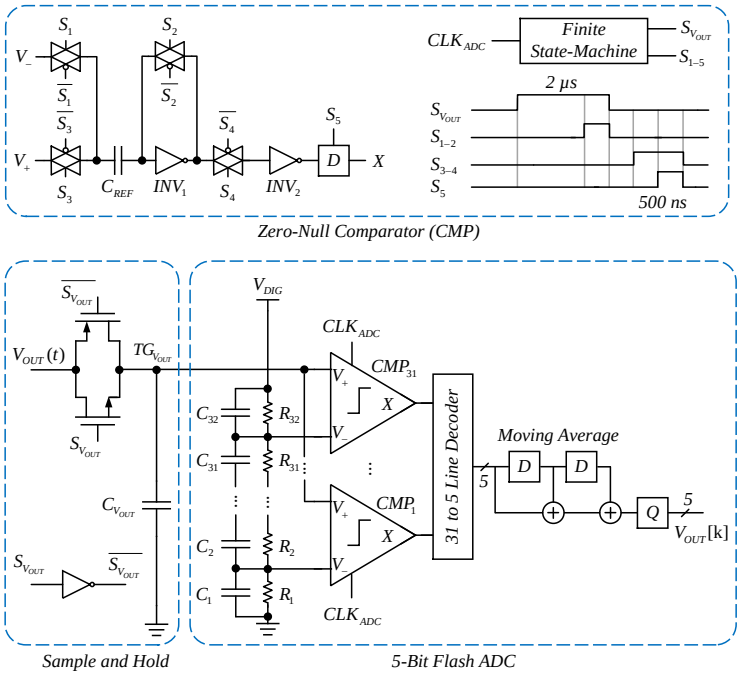


Figure 2.9. The 5-bit flash ADC.

the evaluate phase, the biased INV_1 is triggered into its corresponding stable condition with V_+ applied at input. The S_{1-2} signals are used to initiate the charging phase by shortening input and output of INV_1 through transmission gate S_2 to force meta-stability condition and charging the other plate of C_{REF} to V_- via transmission gate S_1. The S_{3-4} signals are used to initiate the evaluation phase by applying sampled input voltage, V_+, via transmission gate S_3 and driving the register buffer INV_2 via transmission gate S_4. The comparison results are latched at the output register with rising edge of S_5 signal. The long-channel design of INV_1 and short S_{1-2} pulse period minimize power consumption of the comparator cell. The thermal code at the output of the comparator is converted to its binary equivalent using a synthesized 31 to 5 line decoder. A moving average digital filter was used at the output of the flash ADC to improve the sensed voltage integrity. The sample and hold circuit was designed using a transmission gate $TG_{V_{OUT}}$ and sampling capacitor $C_{V_{OUT}}$. The sample and hold control signal $S_{V_{OUT}}$ is timed to activate for a sampling duration of 2 μs with 500 ns setup time before the clock-edges of CLK_{ADC} generated by the DCM rotator block as shown in Fig. 2.9.

Comparator with Sample and Hold Circuit

A hysteresis comparator with sample and hold circuit is used to compare the V_{SW} during phases ϕ_{1A} and ϕ_{2B} at $f_{CLK_{BAL}} = f_{SW}$ rate for active flying capacitor voltage balancing. Figure 2.10 shows the circuit diagram of the hysteresis comparator and its decoder. The hysteresis comparator is supplied by V_{DIG} and implemented using a pre-amplifier in cascade with a dynamic latch [31]. The hysteresis is set through I_{HYST} value. The output of hysteresis comparator is decoded to generate the $V_{BAL}[k]$ values -1 and +1, which are directly passed to the active capacitor voltage balancing PI compensator.

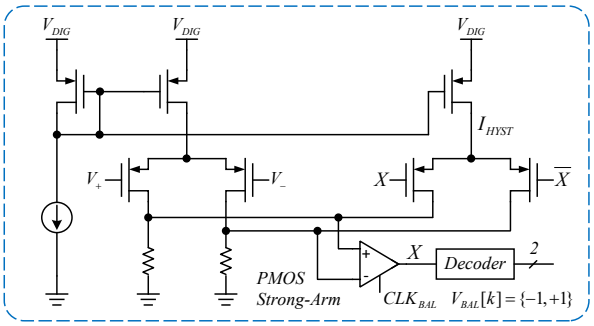


Figure 2.10. Balancing hysteresis comparator and decoder.

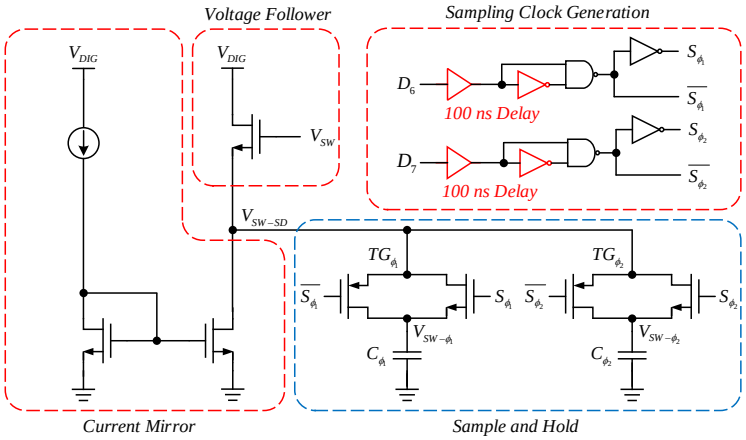


Figure 2.11. Sample and hold circuit for comparator.

The sample and hold circuit is shown in Fig. 2.11. A common drain amplifier is used to track and level shift V_{SW-SD} from V_{SW}. In addition, the common drain amplifier prevents the negative body-diode conduction voltage at V_{SW} from propagating through and discharging the sampling capacitors C_{ϕ_1} and C_{ϕ_2}. The V_{SW-SD} voltage is sampled at the phases ϕ_{1A} and ϕ_{2A} through the transmission gates TG_{ϕ_1} and TG_{ϕ_2}, respectively. The sampling signals S_{ϕ_1} and S_{ϕ_2} are generated by the DCM block with single-shot circuits of 100 ns pulse-width from the 100 ns delayed D5 and D6 signals, respectively. The low-pass RC filter formed by the sampling capacitors and transmission gate resistance damps any ringing artifacts at the V_{SW-SD} node.

Compensator for Balancing and Regulation

Unbalanced flying capacitor voltage levels can lead to a critical voltage stress across the power switches and gate-drivers, which decreases the reliability and can lead to breakdown of the converter. The unbalanced flying capacitor voltage ΔV_{BL} is a direct consequence of unbounded deviations of the V_{C_1} and V_{C_3} from steady-state operation, while $V_{C_2} = V_{IN}/2$ stays constant in this topology. This phenomenon can be shown through the KVL relations in phases ϕ_{1A} and ϕ_{2A}, assuming equal

charge transfer into and from C_2 in phases ϕ_{1B} and ϕ_{2B}, for the split-phase control operation as shown by the equations below:

$$\phi_{1A} : V_{IN} - V_{C_3} = V_{C_2} - V_{C_1} \tag{2.3}$$
$$\phi_{2A} : V_{C_3} - V_{C_2} = V_{C_1} \tag{2.4}$$

where the V_{C_1} and V_{C_3} do not have a unique solution and $V_{C_2} = V_{IN}/2$ is a single solution. Therefore, the initial conditions of $V_{C_1} = V_{IN}/4$ and $V_{C_1} = 3V_{IN}/4$, set through the precharge at start-up, should be preserved via an active voltage balancing technique. This behavior is unique to the soft-charging operation as the flying capacitors are charged and discharged through a current source, whereas in the case of hard-charging the output capacitor provides a single solution of $V_{C_1} = V_{IN}/4$ and $V_{C_1} = 3V_{IN}/4$ for a voltage balanced operation. Hence, any mismatch in the timing and charge transfer between the flying capacitors, through the soft-charging load current source, can lead to a deviation from the V_{C_1} and V_{C_3} initial conditions. This relation is shown by the equations below:

$$\Delta V_{C_3} C_3 = I_{OUT} \Delta t_{C_3} \tag{2.5}$$
$$\Delta V_{C_1} C_1 = I_{OUT} \Delta t_{C_1} \tag{2.6}$$

where the output current I_{OUT} is assumed to be constant as well as $C_1 = C_3$ effective values. In addition, the KVL equations in phases $\phi_{1A} + \phi_{1B}$ and $\phi_{2A} + \phi_{2B}$ imply that any mismatch in the flying capacitor voltages in steady-state operation should converge to the condition $\Delta V_{BL} = \Delta V_{C_1} = \Delta V_{C_3}$. Therefore, any voltage deviation ΔV_{BL} caused by the switching time mismatch, loss, transient load or even I_{OUT}, C_1 and C_3 variations can be corrected through applying a timing correction $\Delta t_{BL} = \Delta t_{C_1} = \Delta t_{C_3}$ to the control phases of $\phi_{1A} + \phi_{1B}$ and $\phi_{2A} + \phi_{2B}$, as shown in Fig. 2.12 to achieve an amp-second balancing operation [32, 33, 34] for the flying capacitors C_1 and C_3. Therefore, the duty-cycle corrections $d_{\phi_{1A}+\phi_{1B}}$ and $d_{\phi_{2A}+\phi_{2B}}$ are applied to the phases of duty-cycle $D_{\phi_{1A}+\phi_{1B}}$ and $D_{\phi_{1A}+\phi_{1B}}$ as shown by the equations below:

$$D_{\phi_{1A}+\phi_{1B}} \pm d_{\phi_{1A}+\phi_{1B}} = \frac{T_{\phi_{1A}} + T_{\phi_{1B}}}{T_s} \pm \frac{\Delta t_{BL}}{T_s} \tag{2.7}$$
$$D_{\phi_{2A}+\phi_{2B}} \mp d_{\phi_{2A}+\phi_{2B}} = \frac{T_{\phi_{2A}} + T_{\phi_{2B}}}{T_s} \mp \frac{\Delta t_{BL}}{T_s} \tag{2.8}$$

where the plus and minus signs are determined based on the voltage deviation ΔV_{BL} sign to decrease or increase the C_1 and C_3 effective charging or discharging times $T_{\phi_{1A}} + T_{\phi_{1B}}$ and $T_{\phi_{2A}} + T_{\phi_{2B}}$ in the control phases $\phi_{1A}+\phi_{1B}$ and $\phi_{2A}+\phi_{2B}$, receptively. The active capacitor voltage balancing extracts the information about voltage deviations ΔV_{C_1} and ΔV_{C_3} through sampling and comparing the switching node voltages $V_{SW-\phi_{1A}} = V_{C_2} - V_{C_1} - V_{TH}$ and $V_{SW-\phi_{2A}} = V_{C_3} - V_{C_2} - V_{TH}$ at phases ϕ_{1A} and ϕ_{2A}, respectively. Therefore, the value of $V_{BAL}[k]$ which is determined by the sign of ΔV_{BL} is calculated by:

$$V_{BAL}[k] = \begin{cases} +1, V_{SW-\phi_{1A}} < V_{SW-\phi_{2A}} \\ -1, V_{SW-\phi_{1A}} > V_{SW-\phi_{2A}} \end{cases} \tag{2.9}$$

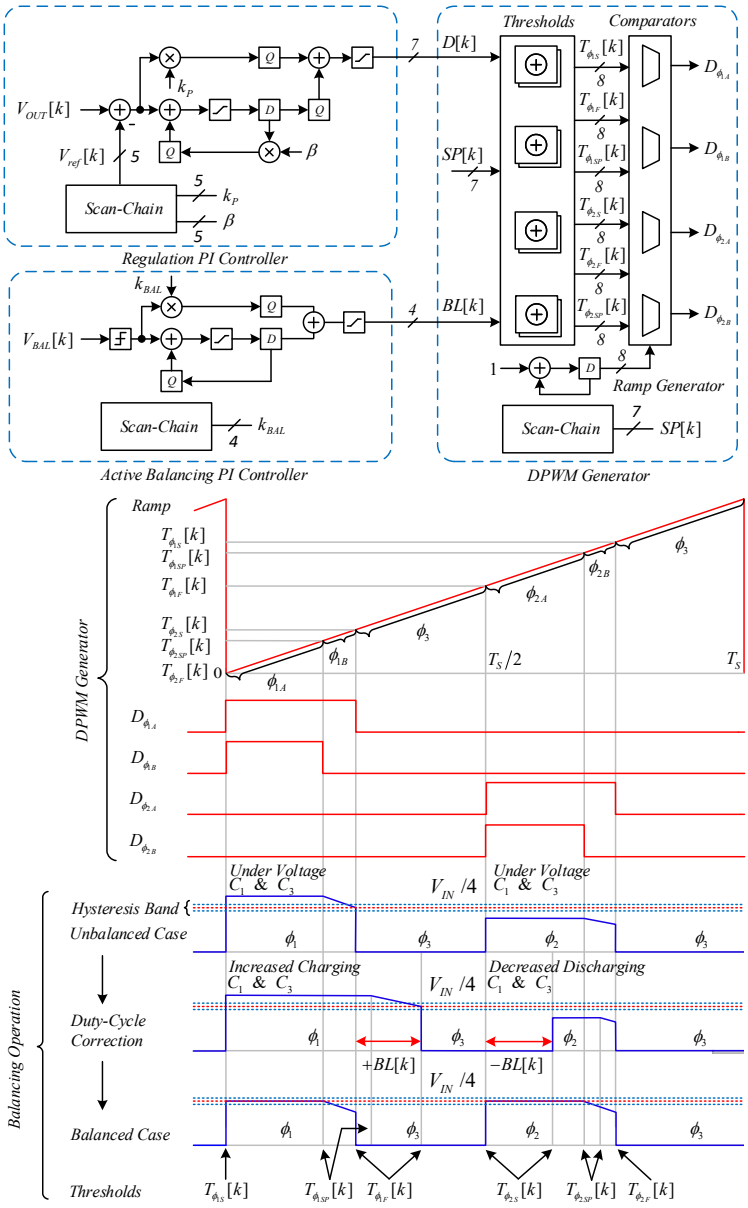


Figure 2.12. Regulation and active flying capacitor voltage balancing PI compensators and DPWM generation.

where $V_{BAL}[k] = +1$ implies that C_1 and C_3 are overcharged and a negative duty-cycle correction is applied to the charging phases $\phi_{1A} + \phi_{1B}$ and a positive duty-cycle correction to the discharge phases $\phi_{2A} + \phi_{2B}$ in order to reduce V_{C_1} and V_{C_3}. Similarly, $V_{BAL}[k] = -1$ implies that C_1 and C_3 are undercharged, and complementary duty-cycle corrections are applied. Therefore, the control law for duty-cycle correction to achieve an amp-second balancing of the flying capacitors can be implemented through a compensator to compute the duty-cycle correction factor $BL[k]$ as shown in Fig. 2.12. The active balancing compensator was implemented to operate in integral mode during the steady-state operation and in proportional mode during the load transients. This design choice prevents the integrator error accumulation during the load transients where the flying

capacitor can take several clock cycles to become balanced. In addition, the proportional mode gain can help to decrease the settling time. The integrator is disabled by clock-gating the integrator feedback register and the proportional mode is enabled by setting a non-zero value assigned to k_{BAL} via scan-chain. The integrator clock-gating is performed in a feed-forward configuration via scan-chain using the external microcontroller to synchronize the load transients with the balancing controller. However, the balancing controller can always be operated in stand-alone configuration with the integrator engaged, which only leads to longer balancing settle time in presence of severe unbalance due to heavy load transients. The $BL[k]$ correction factor is applied to the $\phi_{1A} + \phi_{1B}$ falling edge and $\phi_{2A} + \phi_{2B}$ rising edge to achieve a symmetric duty-cycle. In addition, the BL[k] value is added and subtracted from the overall $\phi_{1A}+\phi_{1B}$ and $\phi_{2A}+\phi_{2B}$ periods in order the to keep the switching period T constant as shown in equations (7) and (8). The ϕ_A and ϕ_B of each phase are then scaled and calculated accordingly based on SP[k] value by including the offset inserted by BL[k] value as shown by equations (10)-(15). It is important to note that the balancing BL[k] introduces minimal adjustments and asymmetry to $\phi_{1A} + \phi_{1B}$ and $\phi_{2A} + \phi_{2B}$ periods and induces minimal effects on the split-phase steady-state operation. Hence a constant SP[k] is used. The only scenario with required large BL[k] offset, and thus inducing significant effect on timing of the split-phase operation, is during the heavy load transients which will take several clock cycle for the flying capacitor to re-enter their balanced steady-state for a minimal BL[k]. Hence minimal efficiency degradation for violation of split-phase timing might occur during the load transients. The DPWM block was designed using a digital counter-based ramp generator, and its threshold computation and comparator blocks of the DPWM are synthesized arithmetic units. The control signal chain and DPWM has a $10mV$ regulation resolution to prevent limit-cycle given the 5-bit ADC linear steps. The threshold values for start and stop of the split and non-split control signals, as shown in Fig. 2.12, are computed using the discrete time equations below:

$$T_{\phi_{1S}}[k] = 0 \tag{2.10}$$
$$T_{\phi_{1SP}}[k] = T_{\phi_{1F}}[k] \times SP[k] \tag{2.11}$$
$$T_{\phi_{1F}}[k] = D[k] - BL[k] \tag{2.12}$$
$$T_{\phi_{2S}}[k] = T_S/2 + BL[k] \tag{2.13}$$
$$T_{\phi_{2SP}}[k] = T_{\phi_{2S}}[k] \times (1 - SP[k]) + T_{\phi_{2F}} \times SP[k] \tag{2.14}$$
$$T_{\phi_{2F}}[k] = T_S/2 + D[k] \tag{2.15}$$

Figures 2.12 also shows the architecture of the PI compensator and DPWM blocks. The proportional coefficient k_P, integrator gain β and regulation voltage reference $V_{ref}[k]$ control parameters as well as the split-phase coefficient $SP[k] \leq 1$ are programmable through the scan-chain. The regulation PI controller transfer function is shown in the equation below:

$$H[z] = \frac{D[z]}{E[z]} = \frac{1}{1 - \beta z^{-1}} + k_P \tag{2.16}$$

where $E[z] = V_{OUT}[z] - V_{ref}[z]$. The $k_P = 3$ and $\beta = 1$ were used for the final measurements. The duty-cycle corrections in steady-state operation are continuously adjusted at each switching cycle based on the comparator's output state. The signal chain design does lead to slight dithering of the output switching node, but its effects are less than the ADC LSB/2 and no limit-cycle

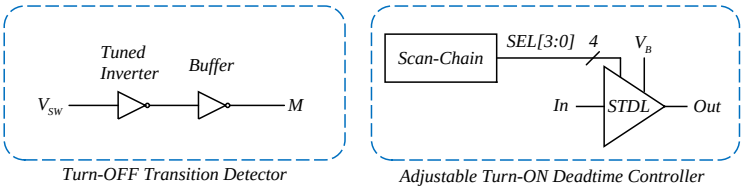


Figure 2.13. Deadtime detector and controller.

behavior is observed. In addition, the regulation controller is running at a slower bandwidth to make the two controllers operation as independent as possible. The $SP[k]$ coefficient was fine tuned in an open loop near the 0.75 theoretical value [24] for both ϕ_1 and ϕ_2 phases to maximize the efficiency across the converter operating range. Anti-wrapping and limiter blocks are used in the implementation of the integrator loops and PI compensator output, respectively.

2.3.3 Deadtime Controller

Minimizing the deadtime can improve the converter efficiency through reduction of body-diode conduction and charge recovery loss, especially at larger conversion ratios where the shorter duty-cycle becomes comparable to the deadtime period. In addition, minimizing the deadtime can improve the flying capacitor balancing at shorter duty-cycle or higher f_{SW} by providing better amp-second matching of the converter operating phases. Therefore, an adjustable deadtime controller was implemented in this work.

The two phase operation of hybrid Dickson SC converter requires independent deadtime controllers at each phase, as different set of gate drive signals are in control of deadtime at each phase. The deadtime controller consists of independent adjustable delay line for turn-ON transition, automated turn-OFF transition detectors and a non-overlap generator. The deadtime controller was designed to minimize the body-diode conduction at both transitions. The turn-OFF transition is detected using a tuned inverter with its input connected to the switching node V_{SW} as shown in Fig. 2.13. The tuned inverter is designed with a 300 mV threshold for a proper deadtime turn-OFF timing. The inverter output is inverted and buffered prior to get connected to the masking signal M of the non-overlap generator as shown in Fig. 2.14. The 20 ns resolution of the DPWM signal is insufficient for deadtime generation of turn-ON transition, as the deadtime can have sub nanosecond periods. Therefore a segmented tapped delay line (STDL) is used to generate the deadtime with 500 ps resolution over a 4-bit control range to cover maximum of 7.5 ns of deadtime for the full load range as shown in Fig. 2.13 and Fig. 2.14. The STDL delay elements are designed using current-starved inverter. The bias current is supplied externally for course tuning and the turn-ON transition deadtime is controlled for fine tuning via the scan-chain at each phase.

2.3.4 Gate-Driver and Voltage Borrowing

The low breakdown voltage of the power switch devices in the available CMOS process places a hard constraint on the maximum allowable power switches voltage stress, including ringing overshoots at the switching transitions. The ringing is a by-product of parasitic inductance in the

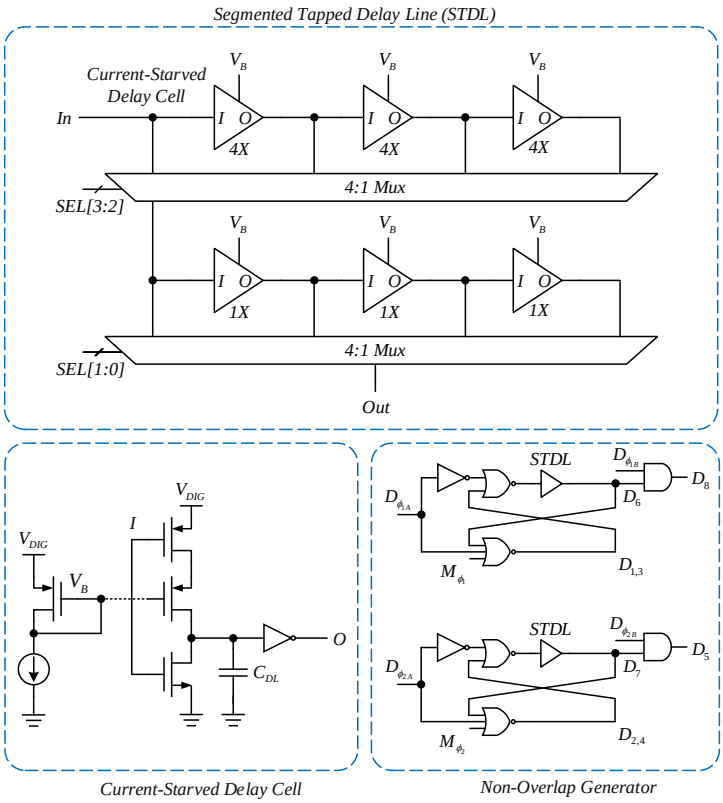


Figure 2.14. Segmented tapped delay line and non-overlap clock generator.

conduction current loop. In order to decrease the ringing amplitude and thus the overall voltage stress across the power switches, it is desired to reduce both the di/dt and the parasitic inductance L. The parasitic inductance can be reduced through careful layout and packaging while di/dt can be reduced using circuit and control techniques. The segmented gate-driver works on the principle of limiting the di/dt through shaping the V_G profile for a slow switching of the MOSFET until most of the current I_{DS} is conducted across the drain-source terminals. When the V_G reaches the plateau voltage and slightly above, the MOSFET is nearly conducting the full I_{DS} current. The reminder of the transition period doesn't involve large di/dt. Therefore, a plateau voltage detector can be used to increase the remaining V_G profile transition rate to reduce the overall transition period and hence the overlap loss. The proposed segmented gate-driver for achieving low ringing and overlap loss is shown in Fig. 2.15 along with the described operation principle in Fig. 2.16. As shown in Fig. 2.16, the turn-ON and turn-OFF transitions of the power switches are divided into two regions. The region boundary is defined by the plateau voltage $V_{Plateau}$ of the switches. As shown in Fig. 2.15 a weak gate-driver is used to turn-ON the power switch device with a slow rising V_G profile up to the plateau voltage to limit di/dt, therefore reducing the ringing overshoot. The $V_{Plateau}$ is then detected through a tuned feedback inverter from V_G to enable the strong driver and increase the V_G profile transition rate, therefore reducing the overall transition period and overlap loss. The tuned inverter is designed with the threshold slightly above the $V_{Plateau}$ of its corresponding power switch. The worst-case equivalent series inductance (ESL) parasitic of 1 nH, obtained through multiphysics simulation of die floorplan and co-packaging solution, is considered in the design of the segmented gate-driver. The ESL parasitic includes series combination of the

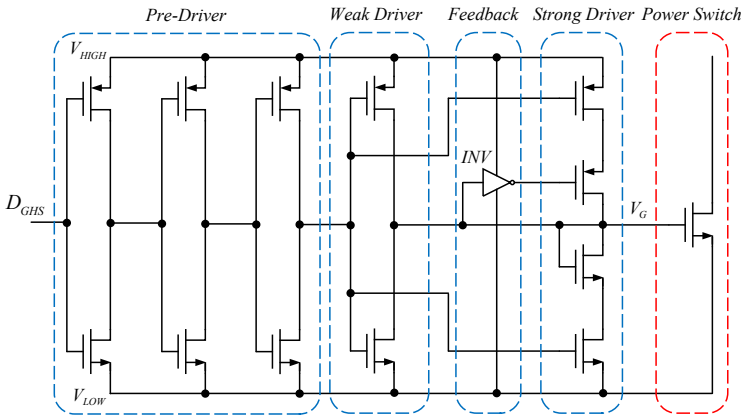


Figure 2.15. Segmented gate-driver design with weak and feedback activated strong driver.

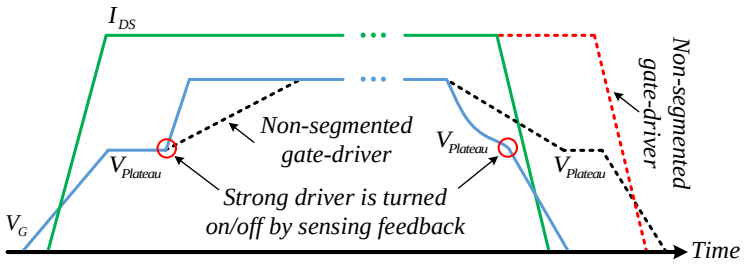


Figure 2.16. Segmented gate-driver vs. non-segmented voltage and current profile.

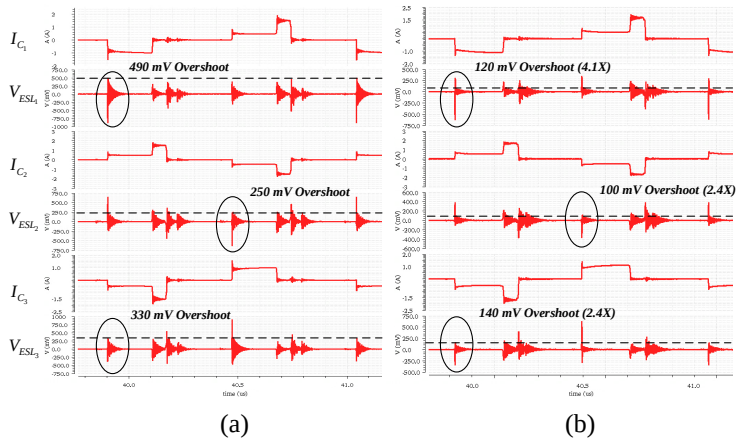


Figure 2.17. The ringing simulation results (a) without segmented gate-driver, (b) with segmented gate-driver.

power switch, layout interconnects, FC and high-density interposer (HDI) package as well as ESL of the flying capacitors in the conduction current loop. Figure 2.17 compares the current through each flying capacitor and the voltage ringing across the ESL parasitic of each conduction current loop with and without employing the segmented gate-driver. The simulation results shown in Fig. 2.17 indicate a minimum of 2.4X ringing reduction with the segmented gate-driver.

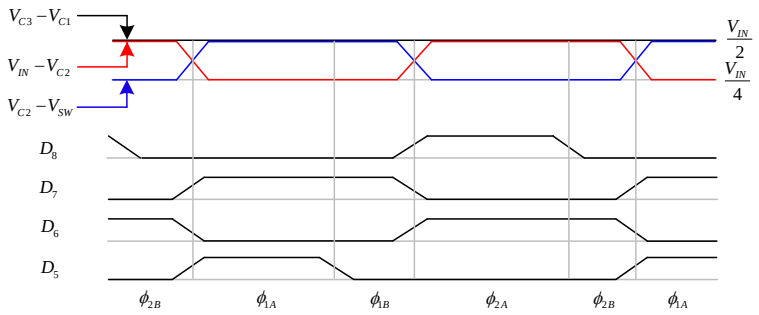


Figure 2.18. Gate-driver voltage borrowing in the time domain and corresponding gate drive signals.

Table 2.3. Gate-driver voltage borrowing technique.

Gate-Driver	**Supply Source**
GD_{1-2}	V_{AUX}
GD_3	V_{C_2}
GD_4	V_{C_1}
GD_5	$V_{C_2} - V_{sw}$
GD_{6-7}	$V_{C_3} - V_{C_1}$
GD_8	$V_{IN} - V_{C_2}$

The gate-driver requires a stable voltage to operate reliably. The traditional way of providing power to a floating gate-driver is by use of bootstrap technique. The bootstrap techniques [35, 36] requires a large capacitor, typically an order of magnitude larger than the gate capacitance to avoid large voltage droop at the switching instances. Given the low capacitor density in 65 nm bulk CMOS process, addition of the bootstrap capacitor on-die can occupy a large area and decrease the power density of the converter significantly. The circuit topology of the Dickson SC converter makes it possible to use the flying capacitors to also serve as the source for gate driving. Therefore, a voltage borrowing technique [38] was adopted to supply the gate-driver by selection of proper voltage nodes in the converter as shown in Fig. 2.7. Table 2.3 provides a listing of the voltage borrowing sources. The time domain borrowed voltages and corresponding gate drive signals are shown in Fig. 2.18, where the required gate drive voltage of $V_{IN}/2$ is available during the active periods of GD_5 and GD_8 as well as a constant voltage of $V_{IN}/2$ for GD_3, GD_6 and GD_7. The voltage borrowing technique imposes a negligible voltage imbalance across the flying capacitors as charges are being asymmetrically redirected for gate-driving. However, the charge recycling due to the embedded connectivity across capacitors and gate-drivers in addition to the active balancing circuit makes the converter operates on a fully balanced state.

2.3.5 Level-Shifter

The higher complexity SC converter with floating power switches and gate-drivers requires control signal level shifting. In addition, the charge flow should be precisely timed for a balanced flying capacitor voltage in steady state operation. Therefore, a reliable level-shifter with minimized delay and transient response is a crucial specification in the design of hybrid SC converters. The

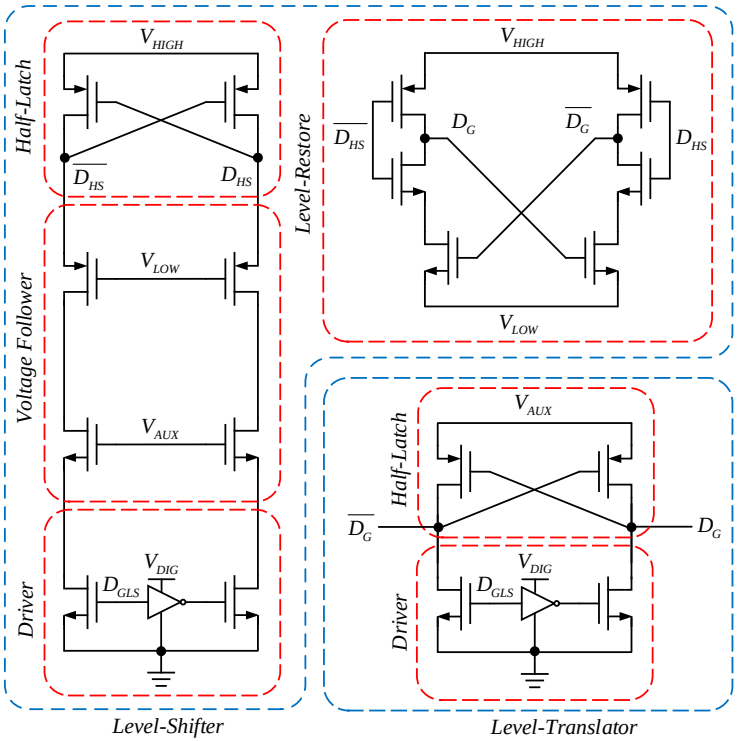


Figure 2.19. Static level-shifter and level-translator circuits with delay compensation.

level-shifter should also have minimum performance variations over the V_{IN} voltage range. The static level-shifter and level translator used in this work are shown in Fig. 2.19. The power switches MN_1 and MN_2 are directly driven from the controller using the level translator. The power switches MN_3 to MP_8 are controlled using level-shifters. The level-shifter consist of the bottom-side driver, the voltage follower, the high-side latch and the level restorer. The bottom side driver and voltage follower should be designed stronger than the high side latch for minimum delay [37]. The propagation delay matching among level-shifter/translator is maintained through equal $V_{HIGH} - V_{LOW}$ and individual device sizing.

2.3.6 Scan-Chain and External Control

The scan-chain was designed for direct access to control signals DG_{1-8} for debugging and external control through pins S_{1-8}, as shown in Fig. 2.7 by bypassing the internal controller. The scan-chain was synthesized and operates at 100 kHz provided by the DCM block. The external controller was also used during the precharge start-up and shut-down sequences. The start-up and shut-down sequences are initiated by disabling the internal controller and activating the MN_1 and MN_2 ground referred power switches. The voltage on the flying capacitors are then ramped-up or ramped-down through an external resistive voltage divider and transmission gates as shown in Fig. 2.20.

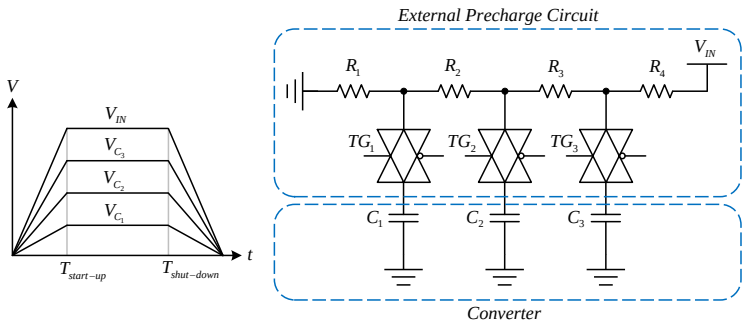


Figure 2.20. External start-up circuit and shut-down circuit.

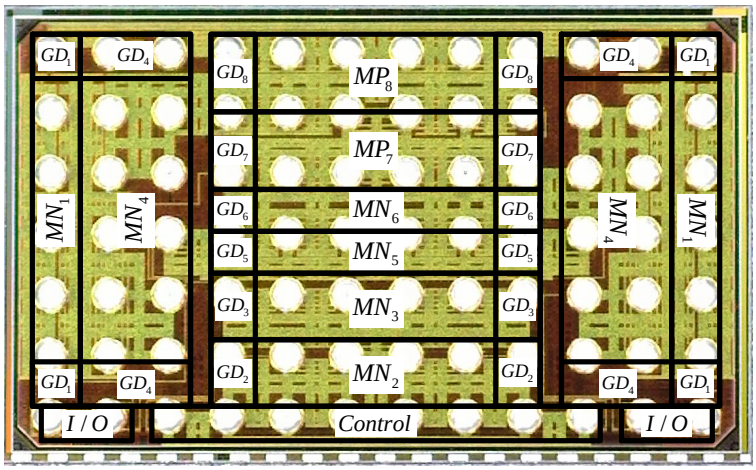


Figure 2.21. Die micrograph and system components.

2.4 Experimental Results and Measurements

A hybrid Dickson converter with the high-level system schematic shown in Fig. 2.7 was implemented using TSMC 65nm bulk CMOS process with a wafer-level FC package. The die micrograph is shown in Fig. 2.21 and has a total die area of 4 mm^2. The die area breakdown is shown in Table 2.4. Careful layout uses 94.5% of total die area for the converter implementation in order to maximize the silicon use. As shown in Fig. 2.22, the passive components including an input capacitor, an output capacitor, three flying capacitors and an inductor are co-packaged with the die using HDI and a PCB cavity to reduce the effective stacked area to that of the die dimension. Owing to the difficulty finding a commercial off-the-shelf inductor with suitable dimensions and design parameters, minor custom modifications to a commercial inductor were performed. The manufacturer inductor footprint of 2 mm × 2 mm was sanded down and modified to 1.8 mm × 1.6 mm to custom fit the die dimension, as shown in the cutaway sideview of Fig. 2.22(b). In a commercial implementation, a custom inductor of suitable dimension would of course be preferred, but in this work the inductor dimension were limited. The HDI useful area is also limited to the die dimension and the excess edges are for PCB connectivity and handling. Table 2.5 shows the volume of the die and passive components packages. This compact package helps reduce parasitic inductance and resistance, which helps achieve high efficiency and power density.

Table 2.4. The die area breakdown.

Die block	**Die Area (%)**
$MN_1 + GD_1$	12.1
$MN_2 + GD_2$	7.3
$MN_3 + GD_3 + LS_3$	7.3
$MN_4 + GD_4 + LS_4$	29.2
$MN_5 + GD_5 + LS_5$	4.2
$MN_6 + GD_6 + LS_6$	4.2
$MP_7 + GD_7 + LS_7$	11.1
$MP_8 + GD_8 + LS_8$	11.1
Controller	5.9
I/O	2.1

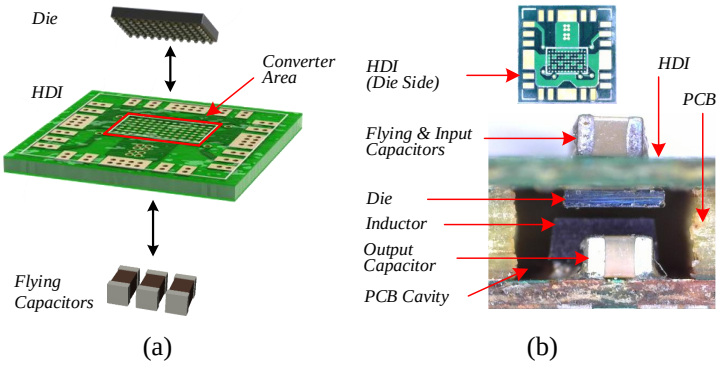


Figure 2.22. The co-packaging of FC die. (a) HDI breakout board and (b) cutaway view of the die assembly.

Table 2.5. Active and passive component footprints.

Component	**Volume (mm^3)**	**Packaging**
Die	1.2	7×12 Ball Grid Flip-Chip
L	2.8	Coilcraft EPL2010 (Modified)
C_{OUT}	0.3	0402 (Imperial)
C_1	0.3	0402 (Imperial)
C_2	0.3	0402 (Imperial)
C_3	0.3	0402 (Imperial)

Given the converter specifications by Table 2.1, the power-train passive components, switching frequency and power switches are designed for soft-charging operation with an optimal power density. The pulse frequency seen by the L and C_{OUT} is twice of the switching frequency. In addition, the voltage swing seen by the inductor is a quarter of the input voltage V_{IN}. This greatly reduces the output voltage ripple compared to conventional buck converters, if the same passives are used. The flying capacitor values are chosen to bound their steady-state voltage ripple within 340 mV at the most extreme case of 1.5 A output current in order to prevent the voltage swing across the power switches to exceed the device ratings. In addition, it is critical to supply the

Table 2.6. Flying Capacitor Matching.

Flying Capacitor	Capacitor	Bias	Derated Capacitance
C_1	4.7μF	0.9 V	4.2μF
C_2	15μF	1.8 V	4μF
C_3	22μF	2.7 V	3.9μF

gate-drivers through voltage borrowing with a large enough voltage to maintain the efficiency, thus a limited flying capacitor voltage swing is desirable. The flying capacitors are matched, given the DC bias derating of the multi-layer ceramic capacitors (MLCC) of the flying capacitors, to effective capacitance range of 3.9 μF to 4.2 μF. Table 2.6 shows the selected flying capacitor values. A 180 nH inductor is used as shown in Table 2.6, however a large value inductor with relatively larger footprint and smaller parasitic can be used to reduce the conduction loss. The output capacitor was selected for the maximum output voltage ripple of 10 mV, which is 5% of the lowest designed output voltage and suitable for sensitive applications.

2.4.1 Voltage Regulation and Balancing

Figure 2.12 shows the system level implementation of the voltage regulation and active balancing controllers. The measured waveforms of V_{SW}, I_L, and V_{OUT} for a step-change in output voltage reference are shown in Fig. 2.23, and illustrates the DPWM operation and corresponding output voltage regulation. The duty-cycle of V_{SW} was adjusted through the closed-loop PI compensator as shown in Fig. 2.12 when the output voltage reference changes from 0.9 V to 0.5 V for an output current of I_{OUT} = 0.5 A. The V_{SW} and inductor current I_L waveforms of Fig. 2.23 illustrates the balanced flying capacitor voltage, as shown though the equal voltage and current amplitudes of the phases ϕ_1 and ϕ_2. In addition, the ringing overshoots are mitigated and the deadtime was minimized.

Figure 2.24 shows the measured equal voltage swing of the flying capacitor to illustrate the effective capacitance matching to overcome the DC bias degradation of MLCC and proper split-phase operation with no to minimal voltage spikes at the phase transitions. Figure 2.25 shows the measurements of voltage nodes V_1, V_2 and V_3 of Fig. 2.7 to compare the effective flying capacitor voltage balancing with the active balancing compensator enabled and disabled. The disabled case shows the capacitors C_1 and C_3 undercharged by approximately $100mV$ from the steady-state values at $V_{IN}/4 = 1V$ and $V_{IN}/4 = 3V$, respectively, while the C_2 voltage stays balanced at $V_{IN}/2 = 2V$. The active balancing enabled case shows near equally spaced voltages at the V_1, V_2 and V_3 nodes presenting a balanced flying capacitor voltage.

The regulated output voltage was measured in a closed-loop across the designed voltage range from 300 mV to 900 mV. Figure 2.26 shows the linear steps corresponding to the programmed $V_{OUT}[k]$ reference via the scan-chain. For this measurement the output resistance was a 600 mΩ resistor. The output voltage regulation was also measured with a load step from 250 mA to 500 mA as shown in Fig. 2.27. The maximum overshoot and undershoot voltage of 24 mV was observed along with 45 μs settling time.

The efficiency across the full output current range of 0.1-1.5 A with V_{IN} = 4.2 V and f_{SW} = 400 kHz was measured for different output voltage settings as shown in Fig. 2.28. The efficiency charac-

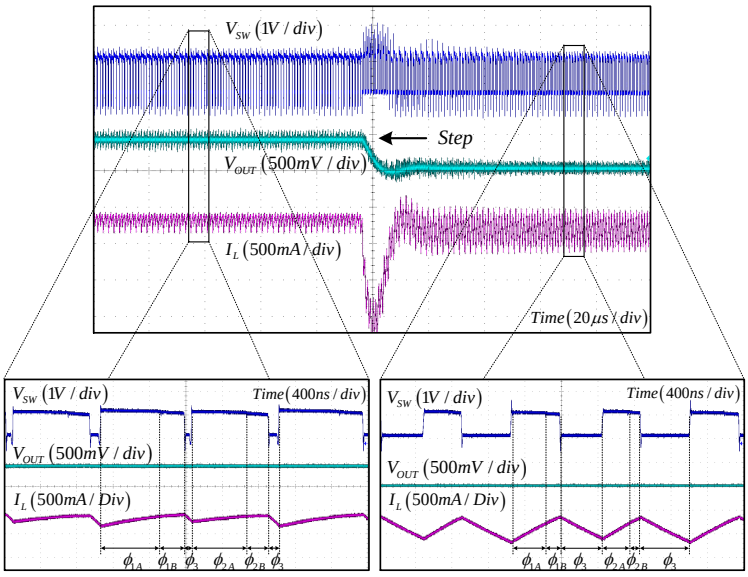


Figure 2.23. Measured transient waveforms of output voltage V_{OUT} regulation for 0.9 V to 0.5 V step.

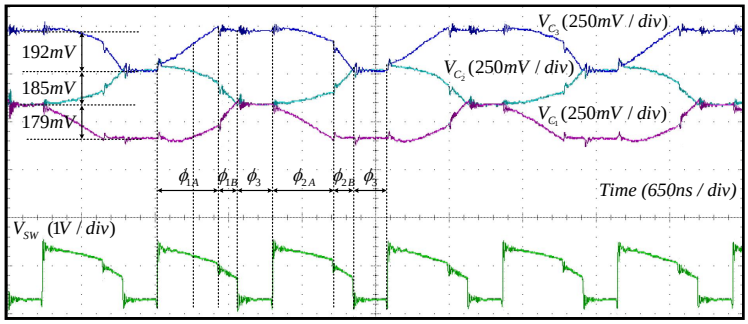


Figure 2.24. Measured flying capacitor voltage swing to show effective capacitance matching.

teristics are quite similar to that of conventional buck converters, where switching and conduction loss dominate at lower and higher current, respectively. However, the hybrid Dickson converter has lower $L \times f_{SW}$ requirement than conventional bulk converter [30] and thus smaller inductor and/or lower f_{SW} trade-off can be used.

2.4.2 Efficiency versus Variable V_{IN}

Figure 2.29 shows the measured efficiency across the full output current range at various V_{IN} values, covering the charged to discharged voltage states of the Lithium-ion battery cell for regulated $V_{OUT} = 0.6$ V. This shows the designed level-shifters and developed voltage borrowing technique are able to operate over wide V_{IN} and I_{OUT} ranges. Higher efficiency occurs at lower input voltage because of lower switching overlap loss, even though switch resistances increase moderately from lower supply voltages to the gate-drivers.

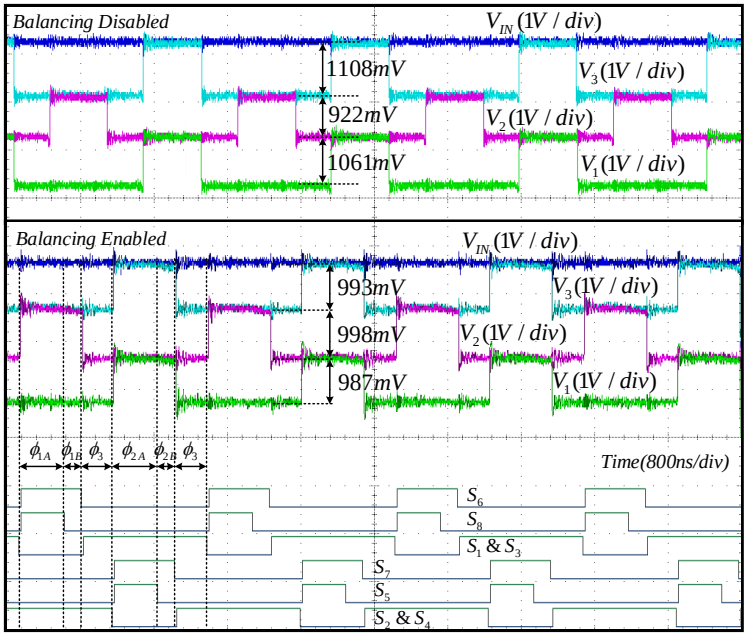


Figure 2.25. Measured V_1 to V_3 nodes to show effective flying capacitor voltage balancing.

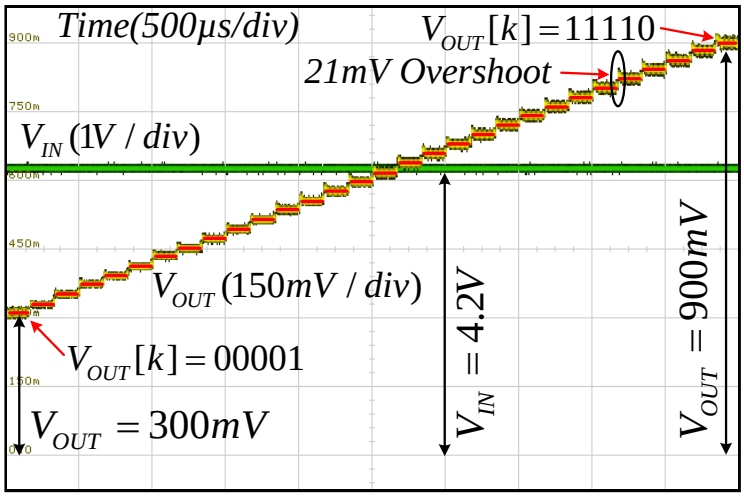


Figure 2.26. Measured regulated output voltage in closed-loop across the designed voltage range.

2.4.3 Efficiency versus Variable f_{SW}

Figure 2.30 shows the effectiveness of increasing f_{SW} from 300 kHz to 500 kHz in achieving higher efficiency by lowering the RMS current ripple. Measurements are taken across the full output current range with $V_{IN} = 4.2$ V and regulated $V_{OUT} = 0.6$ V. The results illustrate that for these parameters, conduction loss dominates over switching loss. The major conduction loss components can be broken down into the metal interconnect and the inductor DC resistance (DCR) losses. For the inductor employed in this work, AC losses were relatively low. The f_{SW} higher than 500 kHz has marginal effect in reduction of the conduction loss, while the switching loss increases, specially

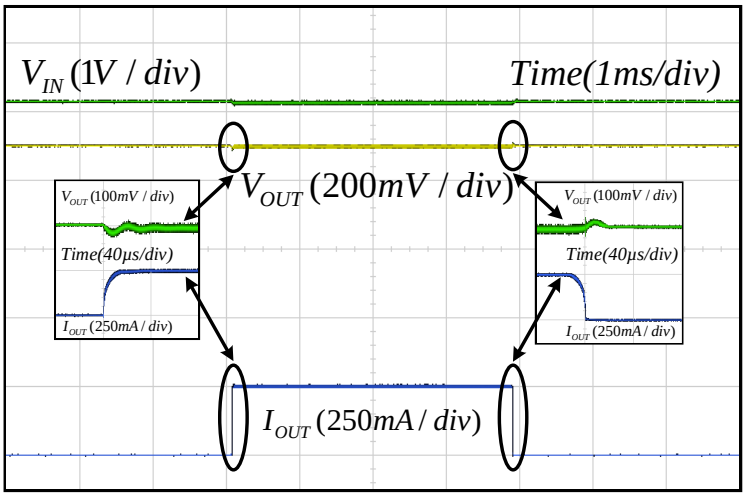


Figure 2.27. Measured regulated output voltage in closed-loop under load step.

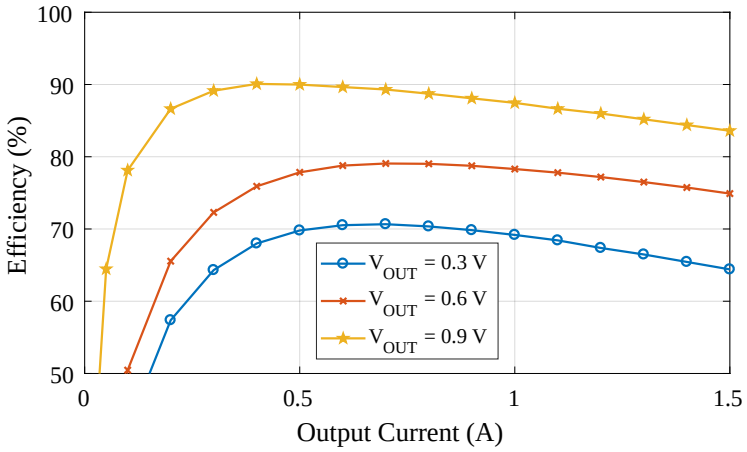


Figure 2.28. Measured efficiency for full output current range at $V_{IN} = 4.2$ V and $f_{SW} = 400$ kHz for various V_{OUT} values.

in the light load regime. Hence, a maximum f_{SW} of 500 kHz was chosen to the characterize the converter.

2.4.4 Efficiency versus Two-Phase and Split-Phase Controls

The converter efficiency was measured at $SP[k] = 1$ and $SP[k] = 0.78$ to implement the two-phase and split-phase controls, respectively, with the $V_{IN} = 4.2$ V, $V_{OUT} = 0.9$ V and $f_{SW} = 400$ kHz operating point across the full load range. As shown in Fig. 2.31, up to a 2.2 percentage points improvement in efficiency at light load was demonstrated, with corresponding heavy load improvement being 0.6. This corresponds to a 9.1% and 4.3% reduction in power losses at light and heavy loads, respectively. It should be noted that the smaller relative improvement at heavy load is due to the fact that the majority of the losses at this operating point are conduction losses.

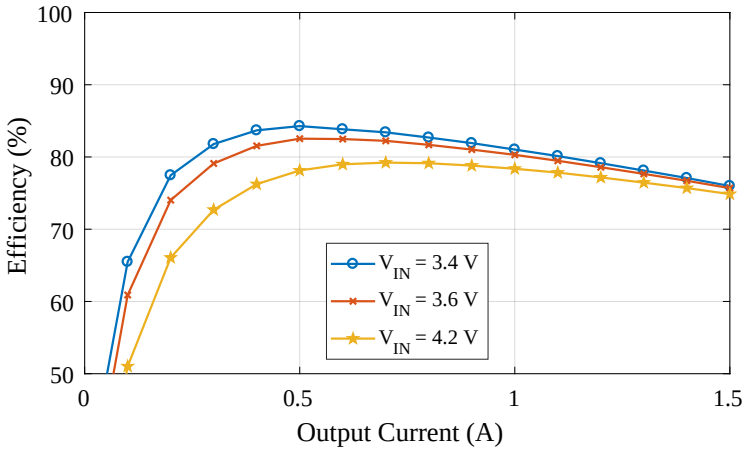


Figure 2.29. Measured efficiency for full output current range at $V_{OUT} = 0.6$ V and $f_{SW} = 400$ kHz for various V_{IN} values.

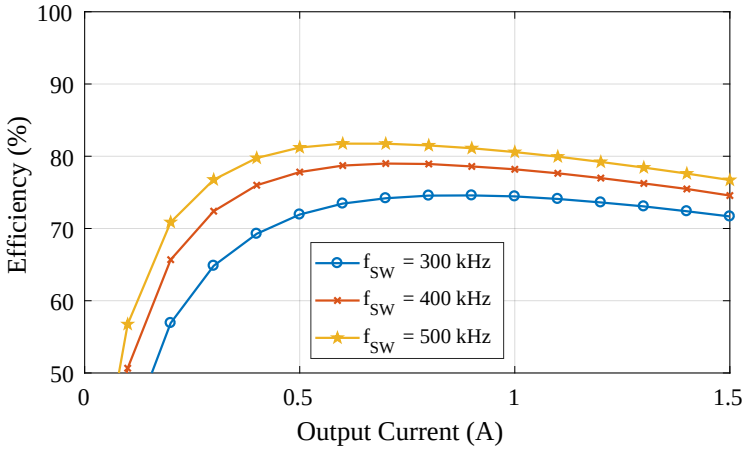


Figure 2.30. Measured efficiency for full output current range at $V_{IN} = 4.2$ V and $V_{OUT} = 0.6$ V for various f_{SW} values.

During the split-phase operation, there is only one current conduction path, whereas the original two-phase operation always has current flowing through two parallel paths as shown in the drawing of Fig. 2.3 phases.

2.4.5 Converter Performance Characterization

All the efficiency measurements are taken considering the control and external supplies losses. The Keithley sourcemeters are used at the power and auxiliary inputs and output of device under test for efficiency measurements. The converter performance was characterized at 500 kHz, with effective inductor frequency of 1 MHz, and the Lithium-ion battery nominal voltage of 4.2 V for the highest step-down ratio and use of split-phase control. Figure 2.32 shows the converter performance for the full voltage and current load range specified by Table 2.1 using the 180 nH inductor with DCR of 24 $m\Omega$ and derated $C_{OUT} = 19$ μF at maximum 900 mV DC-bias value.

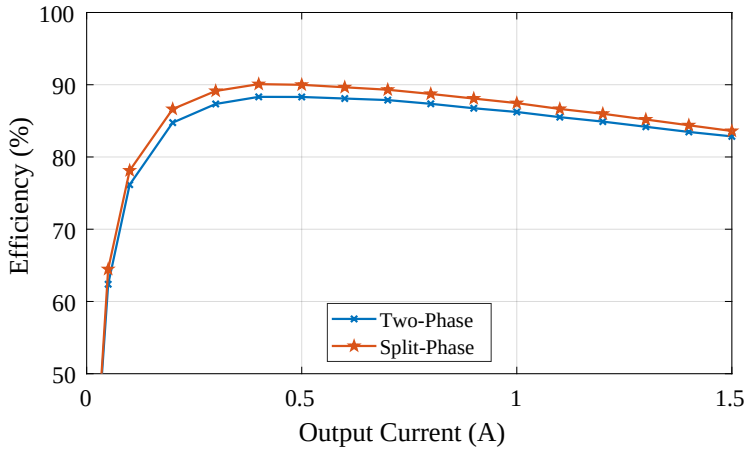


Figure 2.31. Measured efficiency for full output current range at $V_{IN} = 4.2$ V, $V_{OUT} = 0.9$ V and $f_{SW} = 400$ kHz for two-phase and split-phase controls.

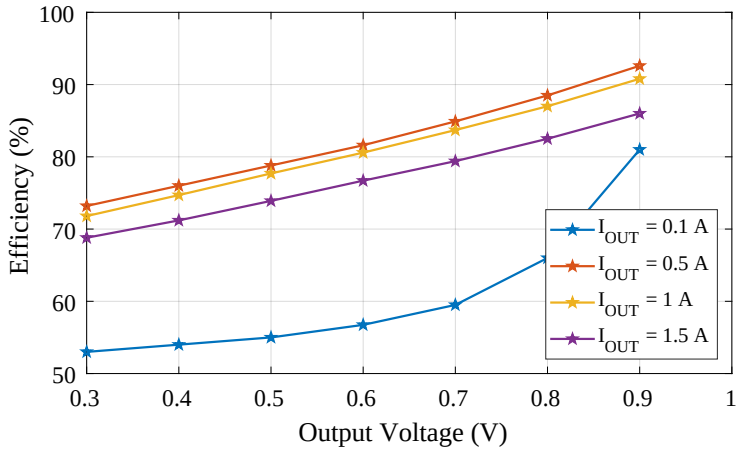


Figure 2.32. Measured efficiency for the regulated V_{OUT} continuous range at $V_{IN} = 4.2$ V and $f_{SW} = 500$ kHz.

Table 2.7. Comparison with prior state-of-the-art work.

Converter Specification	**This Work**	**JSSC19 [26]**	**JSSC17 [12]**	**JSSC15 [23]**	**JSSC15 [8]**	**TI TPS8268090**
Topology	Hybrid SC	Hybrid SC	SC	ReSC	Buck	Buck
Technology	65 nm Bulk	180 nm Bulk	130 nm Bulk	180 nm Bulk	65 nm Bulk	NR
Active Area (mm^2)	4	5.5	1.12	9.88	5	6.67
Inductor (nH)	180	220	N/A	5.5	220	NR
Input Voltage (V)	3.4-4.2	3-5	1.6-3.3	3.7-6	1.8	2.5-5
Output Voltage (V)	0.3-0.9	0.3-1.2	0.5-3	1.2-3	0.6-1.5	0.9
Peak Output Current (A)	1.5	2.5	0.12	1.64	0.6	1.6
η_{MAX} @ Conversion Ratio	92.6% @ 4.7	90% @ 3.8	91% @ 2.0	91% @ 2.0	96% @ 1.3	81% @ 2.8

The prototype converter test board is shown in Fig. 2.33. Table 2.7, Fig. 2.34 and Fig. 2.35 compares this work with relevant prior state-of-the-art converters implemented on common bulk CMOS process. The converter estimated power loss breakdown for regulated $V_{OUT} = 0.9$ V and $I_{OUT} = 0.5$ A is shown in Table 2.8, including all control and auxiliary supplies losses.

Table 2.8. Estimated power loss breakdown.

Breakdown	**Loss (%)**
Control Loss	2%
Inductor DCR Loss	16%
Inductor AC Loss	5%
Switching Loss	29%
Conduction Loss	48%

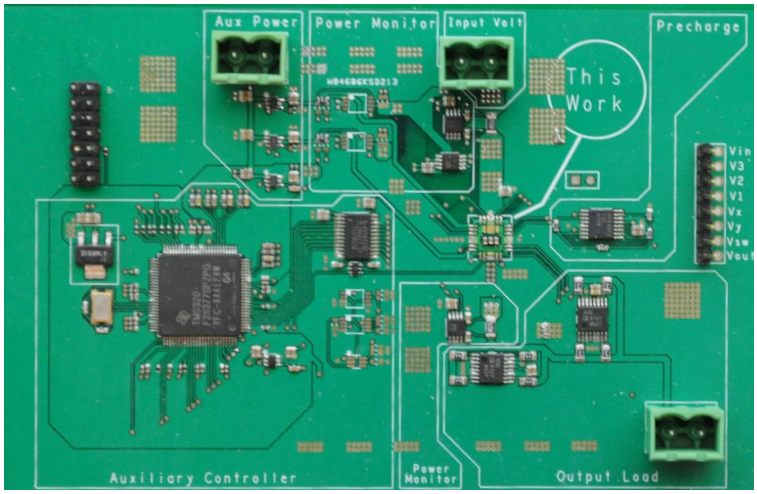


Figure 2.33. Prototype converter test board.

Figure 2.35 compares the converter efficiencies at their corresponding peak power density data points of Fig. 2.34, computed based on the die area. However, this metric alone does not provide a fair comparison. For instance, the adjustable ratio SC converters [18, 19, 12] utilize large die area to achieve high efficiency across the designed conversion ratios, but at much lower output current or lower current density. By using both Fig. 2.35 and Fig. 2.34, the primary performance indexes including efficiency, conversion ratio and power density are considered, where the target of this work is to push toward the upper-right corners in both comparison figures. Conventional buck converters [8] achieve very high efficiency, but at much lower conversion ratios (up to 3:1). SC converters [11, 12] demonstrate high efficiencies. However, most SC converters have drastic reduction in efficiency when non-native conversion ratios are covered. The higher power density data point provided in [23] is mainly because of the higher output voltage range at $2.5V$, and both higher output current and voltage in the work presented in [26] as marked in the Fig. 2.34. The lower efficiencies at the peak power density in [26] compared to the presented work is likely due to charge redistribution loss of [26], which is a partial hard-charging topology.

2.5 Conclusion

The hybrid Dickson SC converter demonstrated a high efficiency and power density at large conversion ratios through soft-charging with the split-phase control at lower effective switching

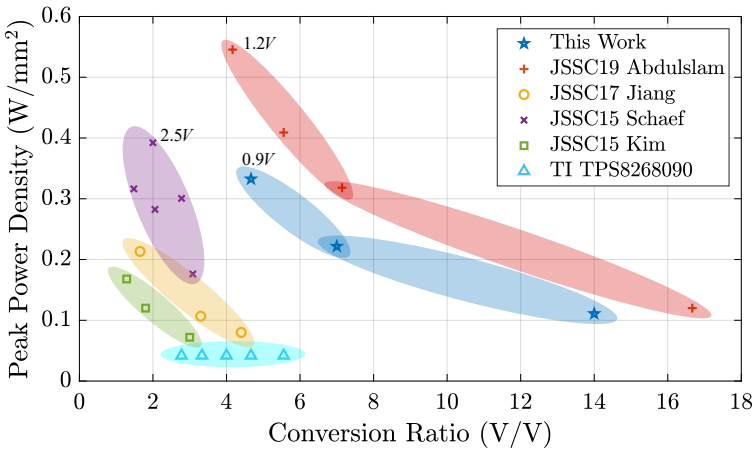


Figure 2.34. Peak power density at conversion ratio comparison from die area.

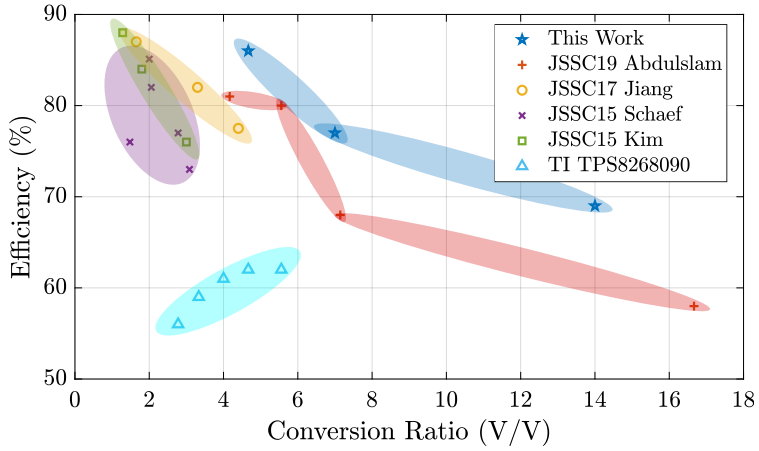


Figure 2.35. Efficiency comparison corresponding to Fig. 2.34 data points.

frequency of 1 MHz. The output voltage regulation, deadtime control and active flying capacitor voltage balancing enables reliable and wide continuous conversion ratio at maximum power density of 330 mW/mm^2 and a peak efficiency of 92.6%. The segmented gate-driver design mitigated the ringing while maintaining the efficiency. Finally, the balancing technique demonstrated in this work can be adopted for larger native conversion ratios and other SC topologies.

Chapter 3

Dual-Phase Hybrid Asymmetric Dickson SC Converter with Multiple Outputs and Coupled-Inductor

3.1 Introduction

The need for integration of high power-density and efficient DC-DC converters with single input and multiple-output (SIMO) topologies [39, 40, 41, 42, 43, 44] provides an opportunity for utilization of the hybrid switched-capacitor (SC) converter with potentials to improve the figure of merit in SIMO class converters. The SIMO typologies typically consists of a first-stage step-down conversion prior to a second-stage ordered power delivery (OPD) as the energy sources often reside at a distanced voltage level from the load. The Dickson SC topology provides high utilization of switches and capacitors and additionally a hybrid Dickson SC [45] with an output inductor to provide soft-charging operation, is a promising replacement for the first-stage conventional buck conversion in a SIMO architecture. Moreover, the output inductor can serve as the storage element in OPD redistributive control, thus decreasing overall volume as a single passive element serves both functions. However, the immediate challenge in the design of two-stage converters with an indirect intermediate energy storage element – inductor – is a uniform control of energy flow between the two stages, as a mismatch in the input and output energy flow of the inductor can accumulate and result in converter failure or loss of regulation. The conventional controllers monitor and regulate the current or directly the energy of the inductor [39, 40, 42, 43]. However, the low current ratings of target application in this work and low R_{DS-ON} of the converter switches in advanced CMOS process make the design of sensitive analog current-sense amplifiers and the control peripherals, with large area and power consumption, in high-noise substrate of switching converters a challenge. Thus, the sensor-less approach in this work is proposed to alleviate the design complexity and increase the system reliability.

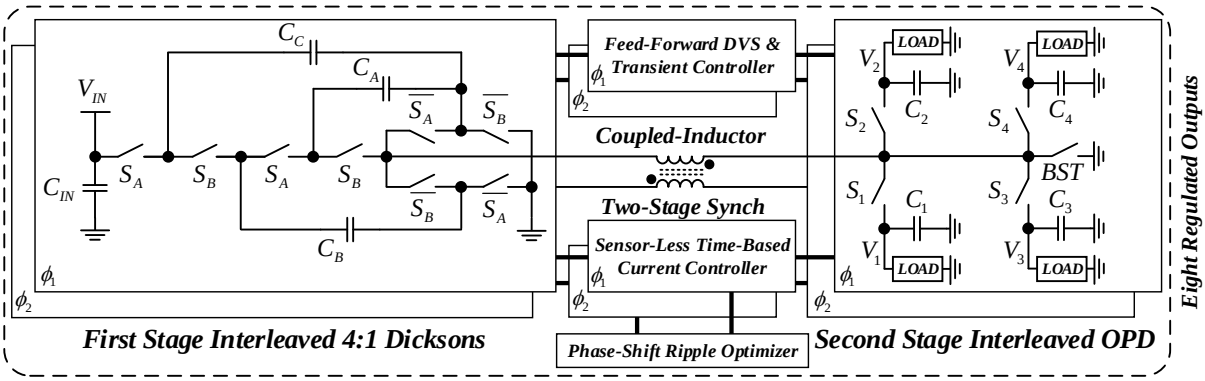


Figure 3.1. The dual-phase time-interleaved SIMO converter with coupled-inductor and sensor-less time-based control.

The two key design concerns in this converter class are the cross-regulation mitigation during load transients and DVS events as well as output voltage ripple reduction. The conventional OPD redistributive control suffers from cross-regulation and voltage ripple as the outputs are refreshed only once per conversion cycle, which degrades the transient response. Use of energy aware or hybrid designs through augmented linear regulator [39, 43] can alleviate the problem at the expense of extra area, power loss and sensitive analog circuitry. The cross-regulation can be eliminated by use of overhead current buffering of the inductor and reordering of output regulation sequence during the transient periods [42] at the expense of a complex and sensitive current sensor design. In addition, use of high-voltage switches for fast transients and DVS cross-regulation compensation [40] is at odds with the desire to utilize high frequency and low voltage switches to achieve high power-density conversion. Similarly, use of pure SC converter [41] improves the transient characteristics, but can lead to poor efficiencies for load regulation at non-native conversion ratios and DVS operation. Furthermore, the conduction loss of integrated hybrid converters due to poor metallization of most CMOS process and current ripple is the bottleneck in achieving high efficiency designs of magnetic based SIMO converters. Hence, utilization of the coupled-inductor and dual-phase time-interleaved operation can reduce the RMS current ripple and the consequent conduction losses in addition to reduction of the output voltage ripple and the filter capacitor size to improve both the transients handling and physical packaging of the converter.

The proposed dual-phase time-interleaved coupled-inductor hybrid Dickson SC converter, as shown in Fig. 3.1, is designed to provide high power-density and efficiency step-down conversion followed by two independent OPD stages providing a total of eight independently regulated output voltages. In the conventional coupled-inductor converters [46], the secondary load sides of the coupled-inductors are connected together. However, as the coupled-inductor utilization in this application is for the purpose of current ripple reduction in each converter, therefore it is not necessary to tie the secondaries together. By disjointing the secondaries [47], it is possible to run each converter at the different steady-state operating point. In addition, each second-stage will see only the current of its own first-stage instead of sum of the two. Hence, this reduced current is beneficial in lowering the current rating of switches and in-turn reducing the consequent conduction losses. However, having the first-stages running at different duty-cycles results in partial flux cancellation of the coupled-inductor in reducing the current ripple with the SIMO converters

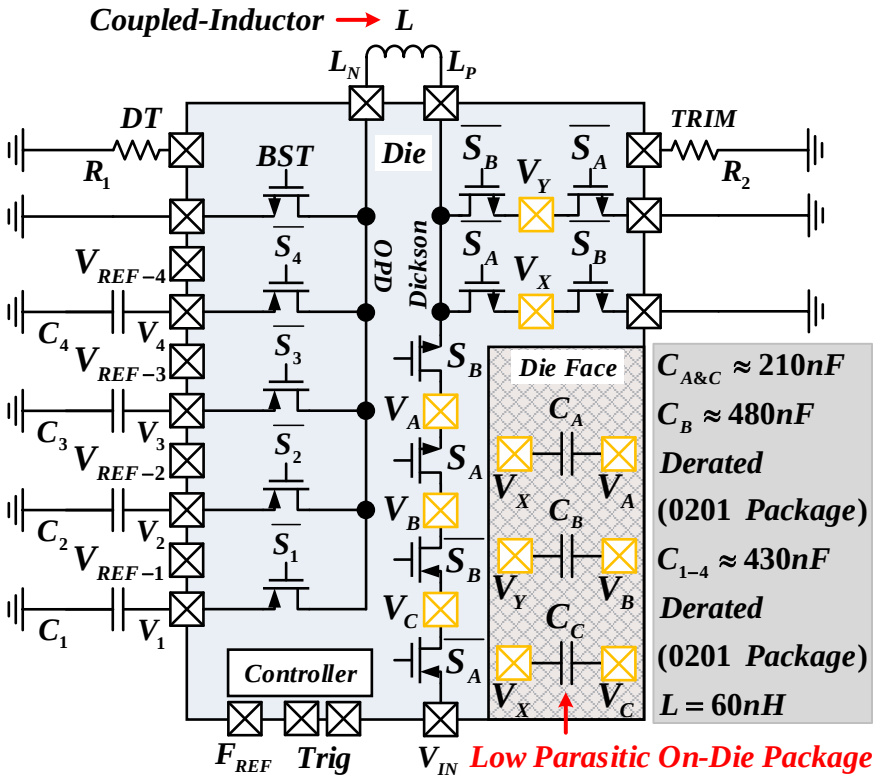


Figure 3.2. The two-stage converter top-level.

running in 180^o phase respect to each other. Hence, an optimal phase-shift correction between the two interleaved phases should be applied to partially regain the benefit of coupled-inductor current ripple reduction. The proposed design is most optimal when the average output voltages of each converter phase are equal. In addition, the two-phase operation of Dickson SC converter doubles the effective switching frequency of the inductor, compared with the buck converter, and reduces the current ripple of inductor. Hence, the OPD switching period is designed to refresh the outputs once per Dickson SC operating phase at 20MHz.

The low-complexity all-digital sensor-less current-mode controller, first-stage flying capacitor balancing as well as the first-stage and second-stage power switches are integrated as shown in Fig. 3.2. A low-profile external capacitor stacking on the die-face and chip-on-board packaging, as discussed in the packaging section, are utilized to reduce the parasitic and improve converters performance.

3.2 Operation Principle

The two main challenges in the design of multi-stage OPD in the area of SIMO converter are the uniform energy flow management of the storage element and the proper handling of cross-regulation during the transient events. The approach proposed in this work address the two challenges through a combined solution by utilization of a time-based control.

Starting with the energy flow management of the storage element, as shown by the inductor of Fig. 3.1, the current-mode control schemes are conventionally employed to directly monitor and regulate the inductor current by modulation of the first-stage converter. However, the Dickson SC converter used in this work is not as robust as a buck converter as the flying capacitor voltage balancing with the current-mode control can become a more complex challenge. Therefore, a digital pulse width modulator (DPWM) for voltage mode control is used in this work to control the Dickson SC converter and an independent flying capacitor voltage balancing controller is designed in parallel [45]. Hence, an indirect method is devised to monitor the inductor current through monitoring the charging rate of the OPD output capacitors C_{1-4} as shown in Fig. 3.1. The charging rate of OPD output capacitor depend on the ratio of available current of the inductor I_L to the sum of OPD output currents given by equation (3.1) below:

$$\alpha_I = \frac{I_L}{\sum_{i=1}^{4} I_i} \tag{3.1}$$

Given the $\alpha_I = 1$ ratio, the OPD output capacitors are regulated within one period of the OPD switching cycle T. A $\alpha_I > 1$ ratio, increases the charging rate of the OPD output capacitor to be regulated in a time-frame lower than one period of the OPD switching cycle. Opposite criteria holds for $\alpha_I < 1$ ratio, where the decreased charging rate of OPD output capacitor leads to loss of regulation. Hence by tracking the regulation time of the OPD output capacitors within one period of the OPD switching cycle, sufficient information about the inductor current can be collected as described. For the steady state operation to maintain the OPD output regulation and prevent the inductor current accumulation a $\alpha_I = 1$ should be maintained as the conventional current-mode controllers achieve. Hence, for indirect monitoring of α_I, the output OPD capacitor regulation period can be compared with the OPD period. By augmenting a freewheel period to the OPD period, a controller can be implemented to measure the deviation of the output OPD capacitor regulation period. Any excess time of the OPD output regulation crossing to the freewheel period is indication of $\alpha_I < 1$ and vice-versa for $\alpha_I > 1$. Hence, the controller can be used to modulate the inductor current in order to maintain the OPD output regulation period at the boundary of the freewheel period to achieve the $\alpha_I = 1$ in steady-state.

The $\alpha_I = 1$ directly translates to maintaining an average zero voltage across the inductor during the steady-state operation. A positive average voltage leads to increase in the current flow and the negative average voltage leads to a decrease in the current flow. The increase in the current flow can saturate the magnetic component as well as damaging the on-die power switches. A decrease in the current flow can cause a loss of regulation on the SIMO output as enough energy is not stored to feed and regulate the output loads. The voltage monitoring of the inductor requires additional analog sense blocks, which can occupy a large area and increased power consumption as oppose to the proposed time-based approach. However, in order to provide a background information for digestion of following sections, the average voltage across the inductor for the proposed time-based approach is analyzed here.

The average voltage at the inductor positive terminal L_P, as shown in Fig. 3.1, which is also the output of the first-stage Dickson SC converter is calculated by equation (3.2) below:

$$\overline{V_{L_P}} = \frac{V_{IN} D}{N} \tag{3.2}$$

where V_{IN} is the input voltage to the SIMO converter, N is the native step-down ratio of the first-stage Dickson SC converter and D is the first-stage duty-cycle. With the design specification of V_{IN} ranging in 3.2V - 3.6V domain and the output voltage of OPD terminals ranging in 700mV - 1V domain, a first-stage with 3:1 Dickson SC topology is well-suited as the OPD is only required to operate in the buck mode. However, a 4:1 Dickson SC topology requires the OPD to operate in both buck and boost mode. In addition, the 3:1 Dickson SC topology requires one less flying capacitor, which improved power-density of the SIMO converter. This design trade-off comes at the price of increased inductor current ripple which can severely degrade the converter efficiency given the poor metalization of available CMOS process. Hence, a 4:1 Dickson SC topology is chosen for this work despite its lower power-density and more complex controller design for OPD operation in both buck and boost modes. The design choice of 4:1 SC converter provides the advantage of operating the buck and boost modes at the boundry of their duty-cycle limits, which lowers the current ripple in the inductor small and thus reducing the consequent conduction losses. The proposed sensor-less time-based control is applicable to both buck and boost modes, as shown in Fig. 3.5 and Fig. 3.4 respectively and explained in detail in the following sections.

The controllers are designed to achieve a zero average voltage across the inductor in order to regulate the energy flow and prevent accumulation or loss of energy in the inductive storage element. In order to calculate the average voltage across the inductor, the average voltage at the L_N node, which is the input to the OPD, is first calculated as shown in by the equation (3.3) below:

$$\overline{V_{L_N}} = \frac{V_{BST}T_{BST} + \sum_{i=1}^{4} V_i T_i + V_{L_P}T_{FW}}{T_{BST} + \sum_{i=1}^{4} T_i + T_{FW}} \tag{3.3}$$

where V_{BST} and T_{BST} are the voltage and time duration of L_N node during the boost period and the V_{FW} and T_{FW} are the voltage and time duration of L_N node during the freewheel period as shown in Fig. 3.5 and Fig. 3.4. Given the L_P node is grounded during the T_{BST} and T_{FW} periods and $V_{FW} = V_{BST} = 0$, the average voltage at L_N node is reduced to equation (3.4) below:

$$\overline{V_{L_N}} = \frac{\sum_{i=1}^{4} V_i T_i}{T_{BST} + \sum_{i=1}^{4} T_i + T_{FW}} \tag{3.4}$$

In the other hand, the freewheel operation is performed by grounding both terminals of the inductor through the BST switch and the Dickson SC bottom four bridge switches as shown in Fig. 3.3. Hence, the freewheel operation circulates the inductor current through the ground loop. However, a lossless loop assumption can be challenged as the inductor direct-current resistance (DCR) and poor process metalization can have severe effects on the inductor circulating current for long periods. Hence, T_{FW} is kept short as discussed in the following description of buck and boost mode operation sections.

The current overhead buffer added to the inductor current as a result of the T_{FW} period is indicated by ΔI_{BUF}. The overall current of inductor can calculated by equation (3.5) below:

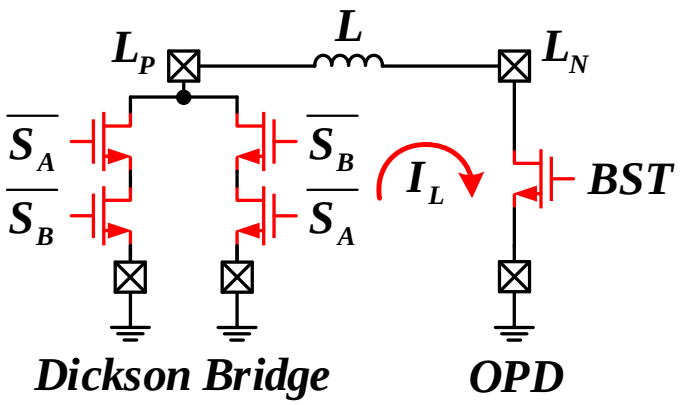


Figure 3.3. The freewheel operation of inductor through ground loop.

$$I_{MIN} = I_{REQ} + \Delta I_{BUF} \tag{3.5}$$

where I_{REQ} is sum of the OPD output currents and I_{MIN} is the minimum current of the inductor current required to maintain the 2% freewheel period. Given, the $\alpha_I > 1$ for the addition of ΔI_{BUF}, yet the steady-state current of inductor is maintained as the over head current buffer circulates in the freewheel current loop and does not transfer to the OPD output capacitors. Therefore, the effective $\alpha_I = 1$ is achieved. Addition of a overhead current buffer is also beneficial to handle the unexpected small step-up DVS and current transients without loss of regulation. Similarly, the overhead current buffering can be temporarily increased in a feed-forward approach before the step-up DVS and transient events to handle the cross-regulation as enough energy is stored in the inductor to source the OPD outputs. The detail of transient handling operation is discussed in the following sections.

3.2.1 Boost Mode

The boost mode operation is shown in Fig. 3.4. The boost mode is engaged if the average voltage at the OPD output is higher than the maximum allowable regulated output voltage of the first-stage Dickson SC converter. The duty-cycle of the Dickson SC converter is fixed at 96% while the freewheel period is maintained at 2% through regulating the boost period at the beginning of the OPD period. In addition, it is important to maintain the freewheel period within the 4% to ensure a false boost period is not activated between the L_P and L_N nodes during the off-time of L_P period. This safeguarding is performed through masking the last OPD output activation signal with the DPWM signal of the Dickson SC converter. Given the 1% duty-cycle resolution of the generation core and the 2% regulation bins of the freewheel sensing, it is guaranteed to achieve a limit-cycle free regulation of the freewheel period.

In the boost mode, the freewheel duty-cycle less than 2% is an indication of overhead current buffering of the inductor storage element, as the low current increases the charging time of C_{1-4}

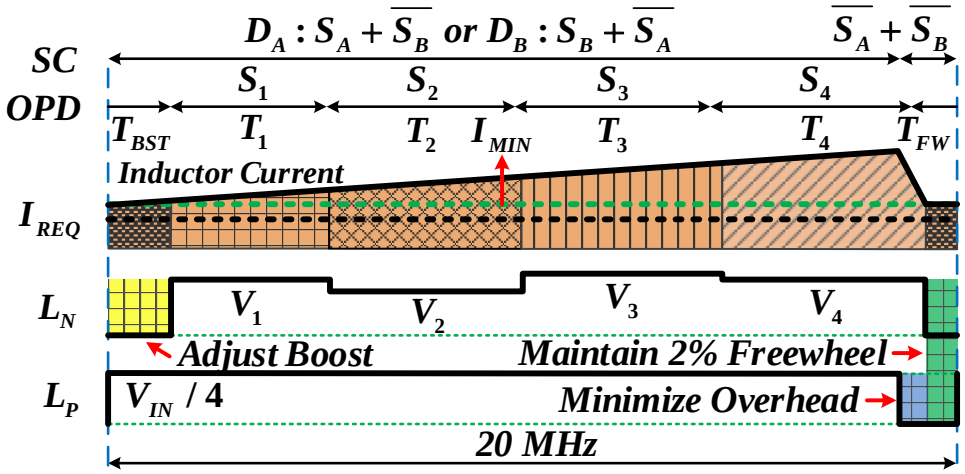


Figure 3.4. The boost mode operation principle.

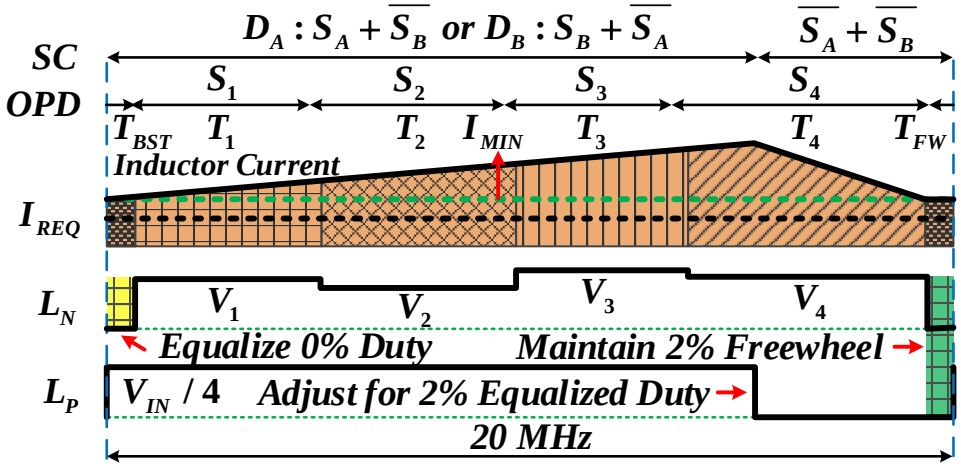


Figure 3.5. The buck mode operation principle.

output capacitors. The freewheel duty-cycle of greater than 2% is an indication of high overhead current buffering of the inductor storage element, as the high current decreases the charging time of C_{1-4} output capacitors. A low current can be compensated by increasing the DC current of the inductor through the increase of the boost period T_{BST} at the beginning of the OPD period. Similarly, a high current can be compensated by decreasing the DC current of the inductor through decreasing the boost period T_{BST} at the beginning of the OPD period.

3.2.2 Buck Mode

The buck mode operation is shown in Fig. 3.5. The buck mode is engaged if the average voltage at the OPD output is lower than the maximum allowable regulated output voltage of the first-stage Dickson SC converter. This condition is flagged if the Dickson SC converter duty-cycle is lower

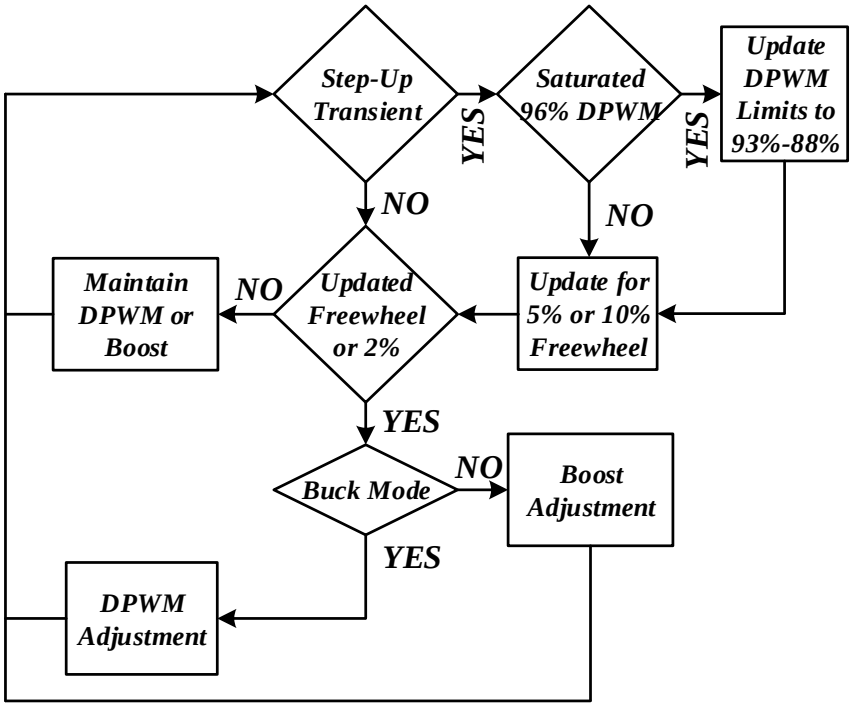


Figure 3.6. The flow chart for transients handling of buck and boost modes.

than the 96% designed threshold value. It is critical to perform a seamless transition between the buck and boost mode, in order to maintain the proper energy overhead in the inductor storage element for uninterrupted regulation of OPD outputs. Therefore, this transition is automatically triggered when the threshold duty-cycle of the Dickson SC converter is sensed.

With the buck mode controller engaged, the boost duty-cycle at the start of the OPD period is disabled. Hence, the freewheel current buffering period is now maintained through duty-cycle adjustment of the Dickson SC converter. Given the 1% duty-cycle resolution of the DPWM generation core and the 2% regulation bins of the freewheel sensing, it is guaranteed to achieve a limit-cycle free regulation of the freewheel period.

3.2.3 Transient Handling

The flow chart of Fig. 3.6 shows the feed-forward controller for transient handling of the converter. As shown by the flow chart, the converter increases the freewheel period and corresponding DPWM limits, thus the overhead current buffer, to handle the step-up DVS or load transients. The freewheel period can be increased to 5% and 10% depending on the transient load level. The converter is rolled-back to 2% freewheel period after the transient to lower the overhead current buffer in order to minimize any conduction loss as result of increases inductor current. The selection between buck and boost mode operation is also shown by the flow chart.

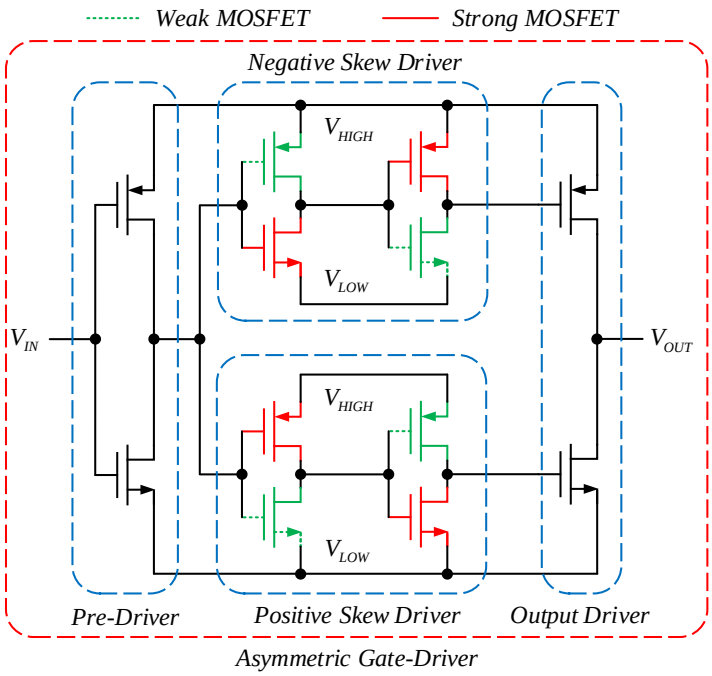


Figure 3.7. The asymmetric gate-driver.

3.3 Implementation

The SIMO converter presented in this work is implemented in 65nm bulk CMOS process. The two power stages as well as the controller are integrated on-die. The power switches of OPD are selected from 1 V core devices which have a significantly lower R_{DS-ON} per area compared with the I/O devices. The power switches of Dickson SC are selected from the 1.8 V I/O devices as the voltage borrowing technique used for powering the floating gate drivers are operating at $V_{IN}/2$, which exceeds the gate voltage limit of the core devices. The complete soft-charging operation of Dickson SC can be achieved through split-phase control [50, 51, 45]. However, the split-phase controller complexity adds area and energy consumption overhead in the implementation of a compact SIMO converter. Hence, a lower complexity two-phase Dickson SC controller with asymmetric flying capacitors [51] can be employed to achieve complete soft-charging, where the asymmetric Dickson SC requires the flying capacitor C_B to be significantly larger than C_A and C_C. The converter is implemented with C_B at 2.5X larger than the remaining flying capacitor to minimize the charge redistribution loss. An active voltage balancing [45] is also employed to guarantee the power switches safe operation. In addition, a well balanced Dickson SC converter has symmetrical voltage on its output node during the two phases of operation, which provides a symmetrical current ripple [45]. A symmetrical current ripple is required as the OPD switching period is within each operating phase of the Dickson SC. Thus, the controller operation relies on a uniform current ripple across the two phases of the Dickson SC. The peripherals and controller designs are discussed in the following sections.

3.3.1 Asymmetric Gate-Driver

The high frequency operation of design converter calls for switching loss reduction in all circuit blocks. Specially as the floating gate-drivers are supplied by the fly capacitors and increased power consumption of the gate-drivers can lead to flying capacitor balancing issues. Therefore, an asymmetric gate-driver [64, 48] is utilized to reduce the current short-through of the gate-driver last inverter stage. The asymmetric gate-driver, as shown in Fig. 3.7, introduces feed-forward deadtime with the pull-up and pull-down devices of the last stage inverter to avoid simultaneous activation at the switching instances. The simulation results show a 12% reduction in the gate-driver power consumption using this technique. It is also important to note that the gate-driver layout area is increased only by 7%. Hence, the favorable trade-off between the area and power consumption justifies the utilization of this technique to improve the converter performance metrics.

3.3.2 Fast Level-Shifter

The level-shifter design plays a critical role in maintaining the balanced state of the flying capacitor, as slight mismatches in the switching timing of the Dickson SC operating phases can accumulate charge and lead to an imbalanced voltage on the flying capacitors. In addition, the timing mismatch in the operating phases of Dickson SC converter can lead to instability of the OPD controller as the tight 2% regulation of the freewheel period and symmetric inductor current are hard constraints. The fast level-shifter design used in this work minimized the switching timing mismatch [49**?**] to alleviate the imbalanced charge accumulation on the flying capacitor. The application of latch-based decoder, as shown in Fig. 3.8 provides a symmetrical low-to-high and high-to-low transitions on the level-shifter output in reference with the input signal.

3.3.3 Dickson Controller

Given the asymmetric Dickson SC converter, the two-phase controller is designed in this work with utilization of the proposed hybrid low-power DPWM generation as oppose to the more complex split-phase controller [45]. The Dickson SC controller schematic diagram is shown in Fig. 3.9.

In the counter-based DPWM generation of Dickson SC converter [45], where a high frequency base clock is required for high resolution DPWM, a large power consumption is expected. However, the counter-based approach can be synthesized and occupy a small area. An alternative approach is utilization of tapped delay-line at a larger area and complexity trade-off, however the energy consumption is significantly reduced. In the other hand, the linearity of tapped delay-line, can be considerably degraded from the PVT variations and layout mismatched geometry, can become a bottleneck for the case of sensitive applications. Reducing the layout area and utilization of less sensitive delay-cells with better matching can significantly increase the linearity of the DPWM generation. In addition, the complexity introduced by the delay mismatch in the relatively large multiplexer design of the tapped delay-line can severely undermine the linearity as well. Therefore, more advanced techniques such as segmented tapped delay-line or hybrid counter-based / tapped delay-line architectures [52, 53, 54] are focused to reduce the delay mismatch to improved the linearity by reduction of the multiplexer geometric size as well as improved delay-cell designs. Furthermore, the DPWM generation should be fitted for the application space and use of a generic DPWM generator with a wide duty-cycle range can lead to a design overhead. The proposed hybrid

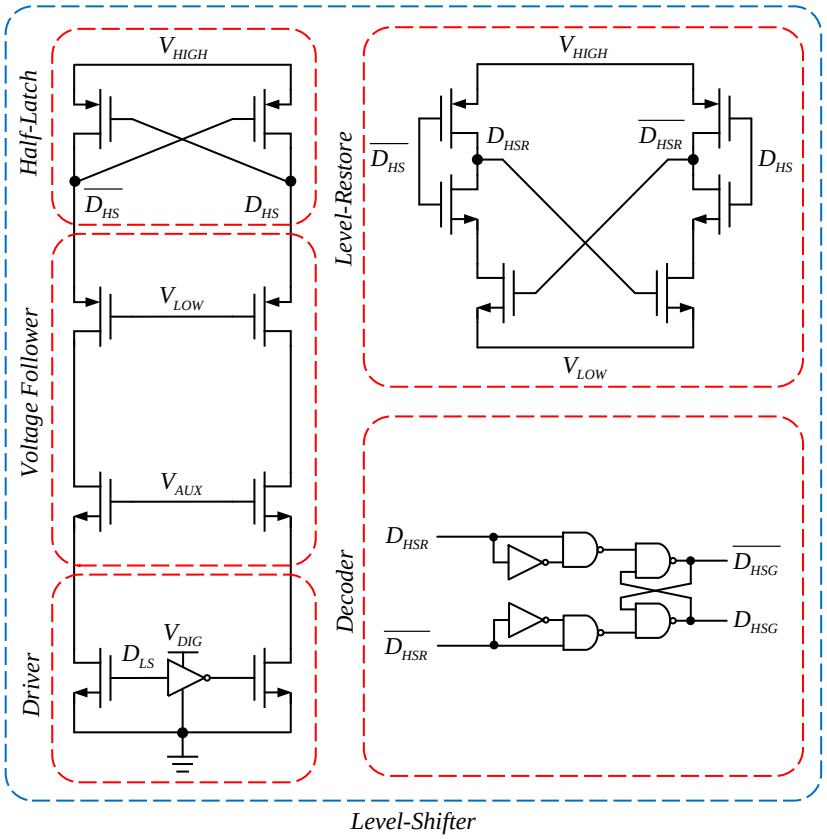


Figure 3.8. The fast level-shifter.

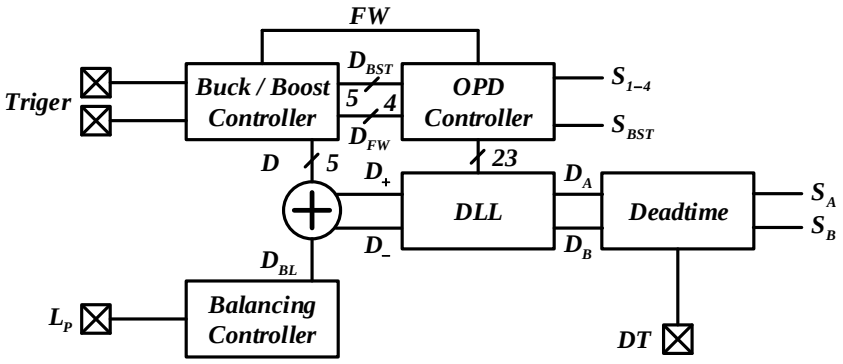


Figure 3.9. The SIMO controller top level diagram.

counter-based / tapped delay-line with a folded architecture, as shown in Fig. 3.10, is capable of generating asymmetrical duty-cycle for the two operating phases of Dickson SC converter. In addition, the DPWM duty-cycle is limited between the 75% to 96% range as the regulated output voltage does not require a wide range. The proposed folded architecture provides a small layout area and linearity as the length of the tapped delay-line and multiplexer are significantly reduced, while a lower power consumption is achieved.

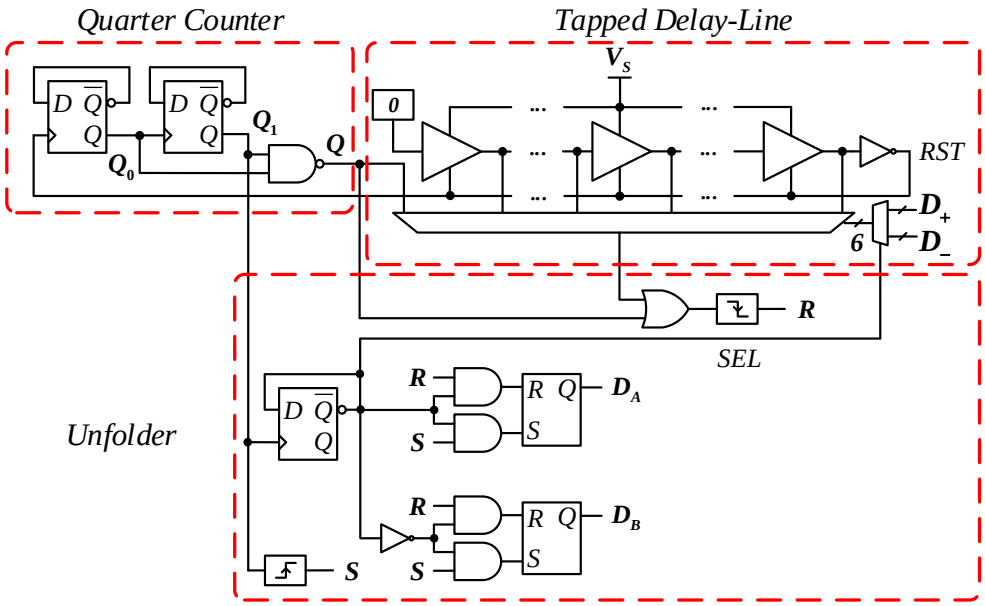


Figure 3.10. The hybrid DPWM generator for first-stage Dickson SC.

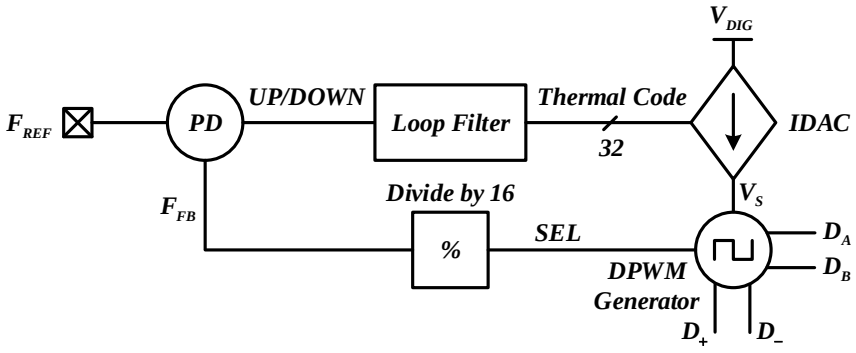


Figure 3.11. The DLL controller of DPWM generator.

Figure 3.11 shows the high-level system diagram, where a digital delay-locked loop (DLL) architecture [55] is adopted. A low frequency external reference clock F_{REF} is fed externally and a digitally assisted oscillator forms the core of this design. The digitally assisted oscillator consists of the hybrid counter-based / tapped delay-line and the unfolder to generated the asymmetric DPWM signals as shown in Fig. 3.13. The hybrid counter-based / tapped delay-line itself breaks down to the 2-bit counter serving as the quarter counter and tapped delay-line serving as the oscillator. The tapped-delay line is essentially a current-starved ring oscillator with the basic delay-cell shown in Fig. 3.12. A tie-low signal at the input of the first delay-cell initiates the signal propagation through the tapped-delay line until it reaches the output of last delay-cell and activates the reset signal RST. The RST signal discharges the delay cap C_{DLY} of delay-cell to reinitialize the tie-low signal propagation through the tapped delay-line. Therefore, a continuous current-controlled oscillation via the V_S of IDAC, as shown in Fig. 3.12, is achieved. The quarter counter consists of a 2-bit D flip-flop counter and a NAND gate decoder to make the multiplexer output transparent

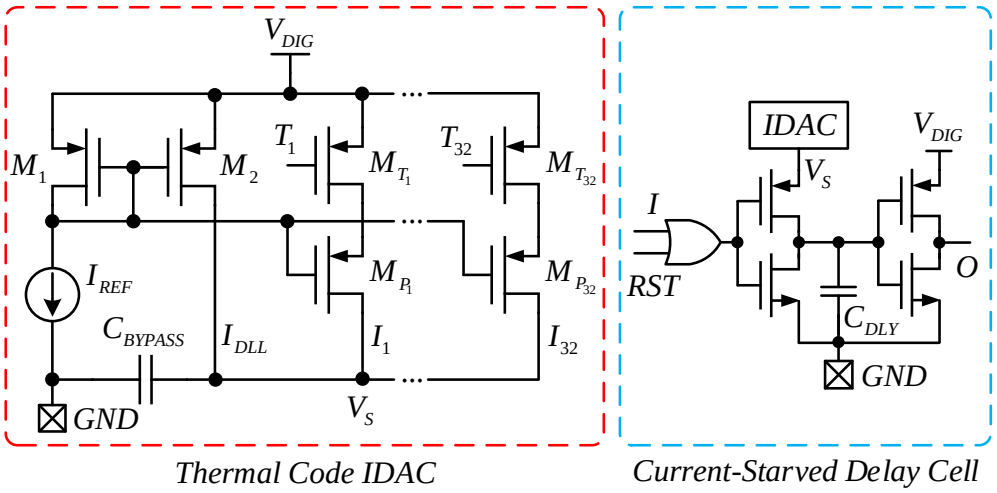


Figure 3.12. The IDAC and current-starved delay cell of DPWM generator.

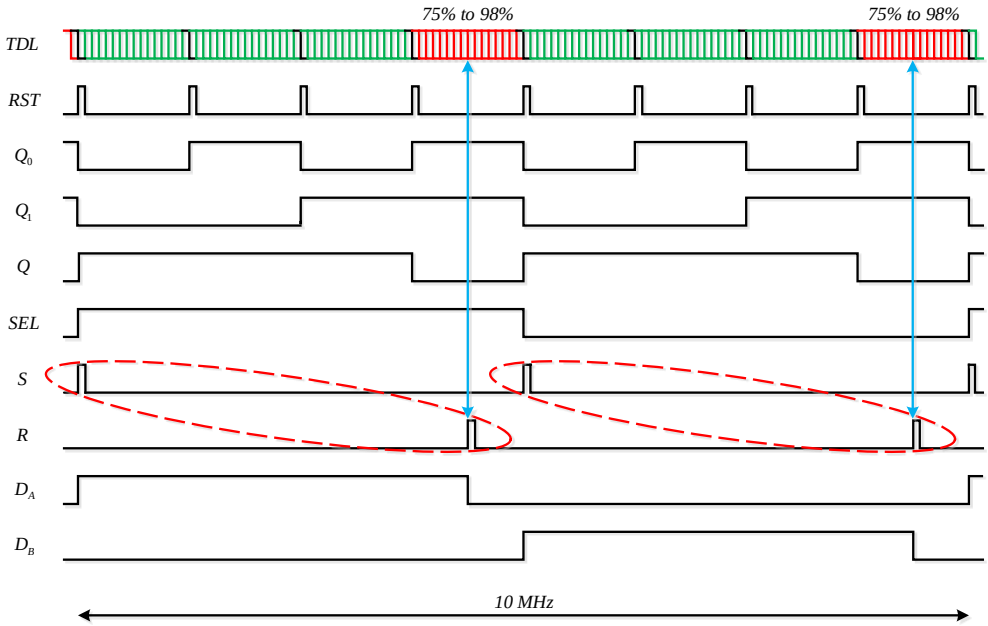


Figure 3.13. The hybrid DPWM generator operation.

to the unfolder only during the last $2'b11$ count and disabled for $2'b00$ to $2'b10$ periods as shown in the timing diagram of Fig. 3.13. Therefore, the reset signal R to the unfolder is only allowed to have a falling edge during the 75% to 96% of the DPWM period. The D flip-flop of the unfolder is clocked by the MSB of the quarter counter to toggle the SEL signal feeding the duty-cycle of each phases of the Dickson SC converter to the tapped delay-line multiplexer. At the same time, the SEL signal makes the set signal S and reset signal R to the SR-latches of D_A and D_B DPWM signals transparent. This mechanism unfolds the S and R signals to of each phase of the DPWM in order to share the tapped delay-line, which can save considerable area and power consumption. In addition, a shared tapped delay-line makes the timing of the both phases DPWM matched.

The tapped delay-line consists of 21 delay-cell in order to achieve a 1% duty-cycle resolution for control of the Dickson SC converter in 75% to 96% range. Dithering the DPWM generated signals D_A and D_B to increase the resolution is not viable as the sensor-less control of energy flow in the inductor storage element is on per OPD switching cycle basis. Another advantage of the proposed techniques is the largely synthesized portion of the design to a compact layout and a shorter design cycle. The DLL signal SEL is operating at 10 MHz where the 4-bit frequency divider generates F_{FB} fed to the phase detector. The loop filter of the DLL is a 5-bit thermal code up/down counter controlling the IDAC of tapped delay-line. The deadtime controller [45] is used to produce the non-overlap signal $S_A/\overline{S_A}$ and $S_B/\overline{S_B}$ from the DLL output signals D_A and D_B respectively. The deadtime duration is controller via external resistor R_{DT} as shown in Fig. 3.2.

3.3.4 OPD Controller

The SIMO outputs of the converter are designed with 1 V PMOS switch devices. The output voltage range of 700 mV to 1 V is selected so the PMOS switches can be operated with ground referred gate-drivers in order to avoid the utilization of complex floating gate-driver for a NMOS switch device, which require additional bootstrapped capacitors. The second stage controller is shown in Fig. 3.14, which consists of the output voltage comparators and a finite-state-machine in connection with the first-stage DLL controller. The FSM controls the sequential operation of output switches as well as the boost switch S_{BST} as in the buck and boost operations of Fig. 3.5 and Fig. 3.4 respectively.

The boost switch S_{BST} duty-cycle is adjusted in 1% increments from 0% to 22% through the first-stage controller DLL as shown in Fig. 3.14. The TDL and quarter counter are used to create generate the control signal via a secondary multiplexer. Note the freewheel and boost periods are adjacent to each other at the transition of the OPD switching cycles. Therefore, the S_{BST} can server as both boost and freewheel switch to conserve area. Hence, the boost and freewheel signals are generated through a single controller in the FSM as shown in Fig. 3.14. The last OPD output regulated, the FSM activates S_{BST} to enter the freewheel period, while a counter is set to measure the freewheel period until the end of OPD switching cycle. Then the S_{BST} duty-cycle at the beginning of a new switching cycle-adjusted based on the flow chart of Fig. 3.6. If the converter is in the boost mode, the S_{BST} duty-cycle in the new switching cycle is adjusted to maintain a 2% freewheel duty-cycle. And if, the converter is in the buck mode, the S_{BST} duty-cycle in the new switching cycle is equalized to 0% duty-cycle and the first-stage duty-cycle is adjusted to maintain a 2% freewheel duty-cycle.

The high frequency operation and tight load regulation specification of the SIMO outputs, requires a high gain and low latency comparator. In addition, the device mismatch and PVT variations can cause severe performance degradation of the SIMO load regulation. Conventional full-swing differential comparator can be biased to reduce the latency and increase the slew-rate, yet the consecutive number of stages in design of such comparators makes the area, latency and power consumption trade-off unfavorable. The strong-arm comparator with low area, latency and power consumption can be a good candid, but the clocked operation of this comparator makes it unsuitable for the application as the SIMO output requires continuous monitoring. Therefore, an inverter-based comparator [45] with low area and latency but slightly higher power consumption is utilized in this work. In addition, the topology of the inverter-based comparator mitigates the mismatch and PVT variations. The inverter-based comparator is shown in Fig. 3.15. The inverter-

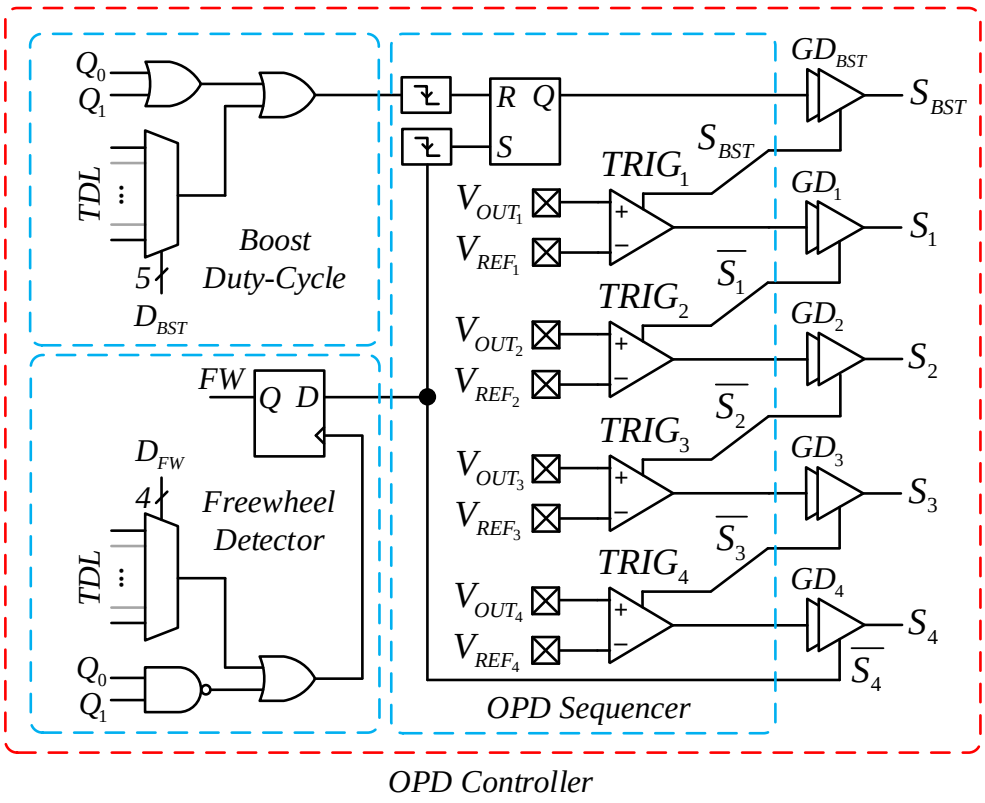


Figure 3.14. The OPD output controller.

based comparator have two operating phases of pre-charge and evaluate, which are initiate by the OPD controller at the beginning of each OPD switching period. During the precharge phase, the input and output of inverter are shorted to V_M of inverter. A nulling capacitor is then charged between the the V_M and the output reference voltage. The nulling capacitor mitigates the mismatch and PVT variations of the inverter by charging to the appropriate voltage that sets the inverter at it's mono-stable V_M point. The evaluate phase is then activated by connecting the capacitor to the respective output during its charging phase.

3.3.5 Packaging

In order to reduces the parasitic inductance and resistance of flying capacitor loops, a die-stacked capacitor approach is utilized [56], where the flying capacitors are directly soldered on top of the die via gold studs. The floor-planing of the die is designed with the optimal placement of the flying capacitor mounting pads as shown in Fig. 3.16. Each mounting pad consist of an array of six pads with $50\mu \times 50\mu m$ wirebond pads which totals to a $300\mu m$ length of a 0402 (imperial) MLCC pad width. The wirebond pads are bonded with the gold ball stud and wirebond removed to provide a lifted surface from the die surface for the flying capacitors to land. It also provides the cavity for the solder paste to penetrate and form the connection between the gold ball studs and the MLCC pads. With the capacitors soldered in place, the chip is bonded on the daughter card PCB and covered with globe-top to package the converter. The two time-interleaved SIMO

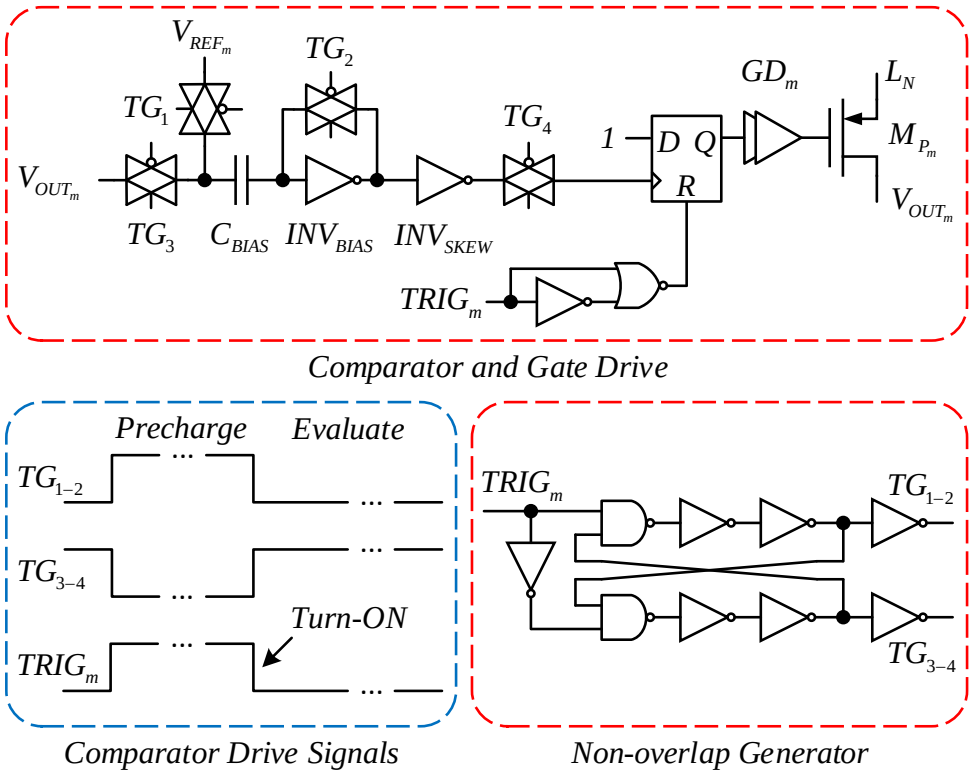


Figure 3.15. The OPD inverter-based comparator.

converters are packaged on the same daughter card PCB with the shared coupled-inductor placed between them. The output capacitors are soldered on the back side of the daughter card PCB. A total area of $22.1mm^2$ is used in the packaging of the converters as shown in Fig. 3.16.

3.4 Measurements

The SIMO converter measurements where conducted to characterize first-stage and second-stage performance independently. The Dickson SC converter can be isolated from the second-stage by connecting the output of the coupled inductor directly to the output filter capacitor and load. The dual time-interleaved Dickson SC converters connected through the coupled-inductor are then measured for efficiency as shown in Fig. 3.17 and Fig. 3.18 for 700 mV and 820 mV outputs for both converters respectively. The measurements where taken by applying symmetrical phase shift for optimal flux cancellation in the coupled-inductor case. In the next step, the same measurements are conducted with each of the Dickson SC converter using a 60nH inductors, which is equivalent to the magnetizing inductance seen through the coupled-inductor. The DCR values of the are also closely matched to minimize the test setup discrepancy in the efficiency measurements. The efficiency measurements are conducted with $V_{IN} = 3.6$ V as shown in Fig. 3.17 and Fig. 3.18 below.

As seen in the Fig. 3.17 and Fig. 3.18 the coupled-inductor achieves an overall higher efficiency

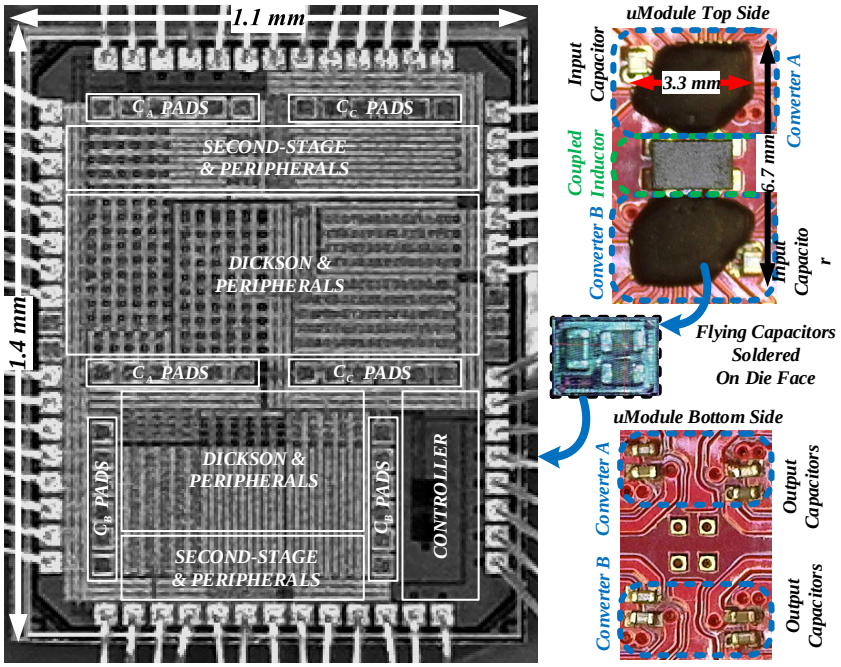


Figure 3.16. The SIMO converter die and the stacked capacitor packaging.

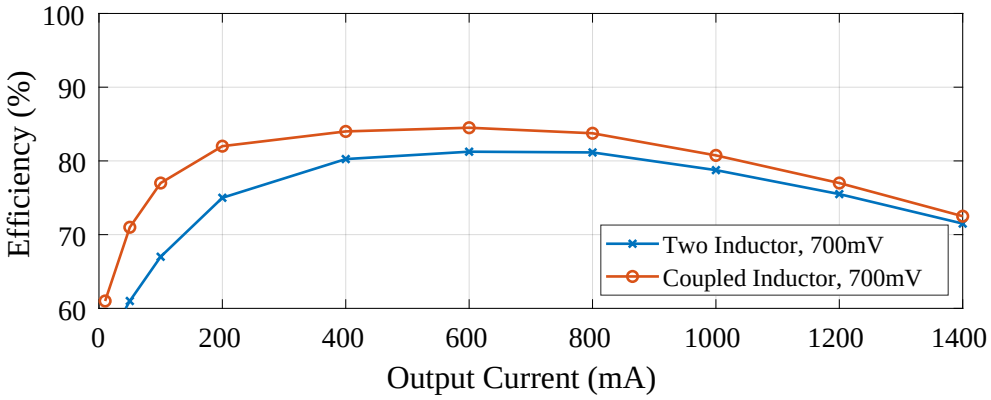


Figure 3.17. The efficiency measurement of Dickson SC converter with and without coupled-inductor at 700mV output.

compared with the discrete inductors. The efficiency improvements are more pronounced in the light load regime as the conduction losses are reduced as a result of lower inductor RMS current. In addition, the efficiency improvements in the 700 mV case are larger than the 820mV measurements, as the coupled inductor achieves a higher RMS current reduction factor [46].

In the next step, the second-stage is connected to the first-stage via the coupled-inductor and the dual time-interleaved SIMO converters are measured for efficiency. The SIMO converters are supplied with the V_{IN} = 3.6 V and configured to operate in both buck and boost modes. With the converter A in the boost mode, the output voltages of 700 mV, 800 mV, 900 mV and 1 V are regulated at outputs V_{1-4} respectively. With the converter B in the buck mode, the output

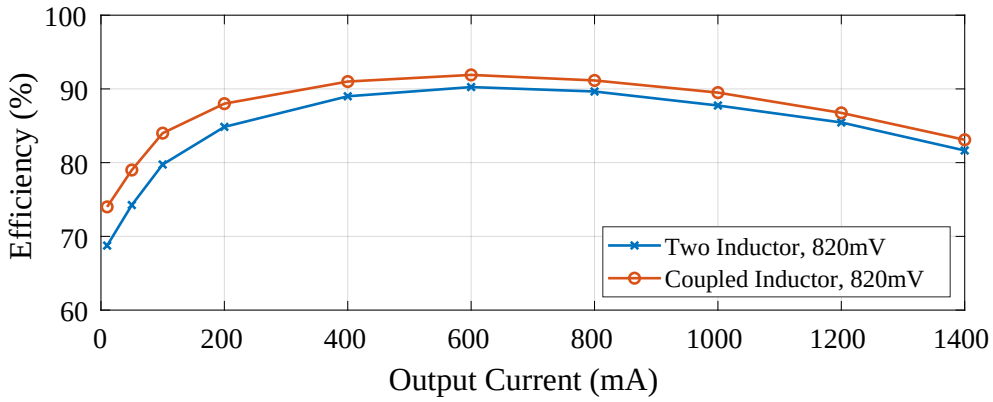


Figure 3.18. The efficiency measurement of Dickson SC converter with and without coupled-inductor at 820mV output.

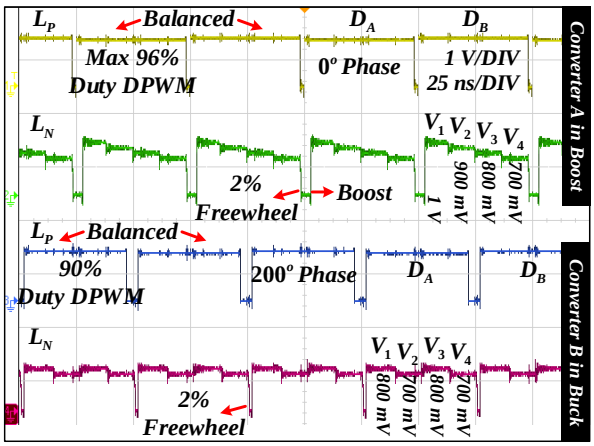


Figure 3.19. The first-stage and second-stage controller measurements for converter A running in boost mode and converter B running in buck mode.

voltages of 800 mV, 700 mV, 800 mV and 700 mV are regulated at outputs V_{5-8} respectively. The switching waveforms at the input of the coupled-inductor L_P and output of the coupled-inductor L_N are shown in Fig. 3.19 below.

The L_P node shows the output of the first-stage Dickson SC converters. The L_P measurements validate the balanced flying capacitor voltages as the marked D_A and D_B operating phases of each Dickson SC converter have equal voltage amplitudes. The duty-cycle of Dickson SC in the converter A is also set at the maximum 96% as it is operating in the boost mode. The L_N node measurements of converter A shows the 700 mV, 800 mV, 900 mV and 1 V are regulated at outputs V_{1-4} respectively, along with the freewheel and boost periods. Similarly, the L_N node measurements of converter A shows the 800 mV, 700 mV, 800 mV and 700 mV are regulated at outputs V_{5-8} respectively, along with the freewheel period. The duty-cycle of Dickson SC in the converter B runs at a value less than the maximum 96% as it is operating in the buck mode.

The transient measurements are taken to validate the cross-regulation elimination capability of the proposed time-based technique. The SIMO converter B is set to regulate 1 V on all its outputs

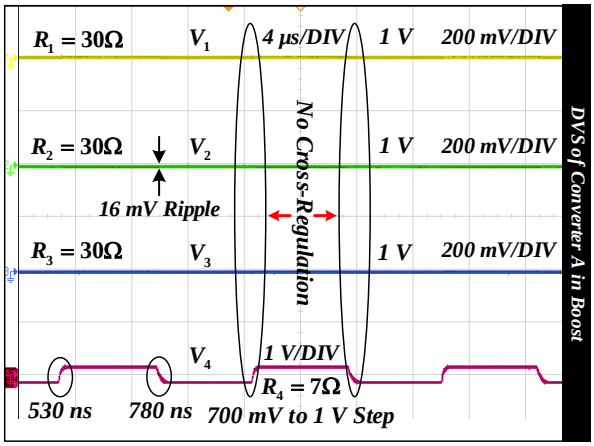


Figure 3.20. The single output channel DVS step loading with cross-regulation elimination at 10% freewheel.

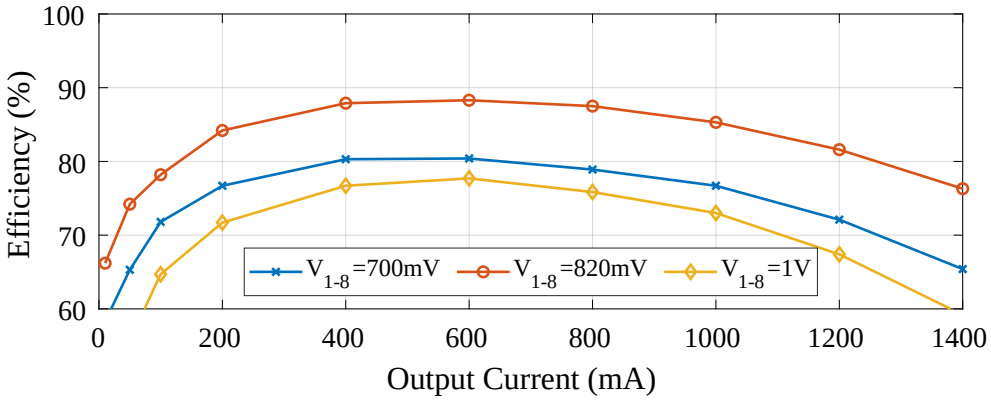


Figure 3.21. The SIMO converter efficiency.

V_5 to V_8 while the converter A is set to regulate 1V on outputs V_1 to V_3. The output V_4 of converter A is periodically toggled to regulate at voltage levels 700 mV and 1 V. With a resistor load of 30 Ω is connected to all outputs and input voltage of V_{IN} = 3.6V the cross-regulation transient is measured as shown in Fig. 3.20 with 10% freewheel period to provide the overhead energy stored in the inductor. As shown in Fig. 3.20 no observable cross-regulation are present on the other output terminals at the transient instances.

With the controller loops operational, the SIMO converter efficiency is measured as shown in Fig. 3.21. The light load efficiency reflects the improvement gain by the coupled inductor as shown in Fig. 3.17 and Fig. 3.18 of the first-stage Dickson SC converter. Optimal phase-shifts are applied for each voltage trend in the efficiency measurements.

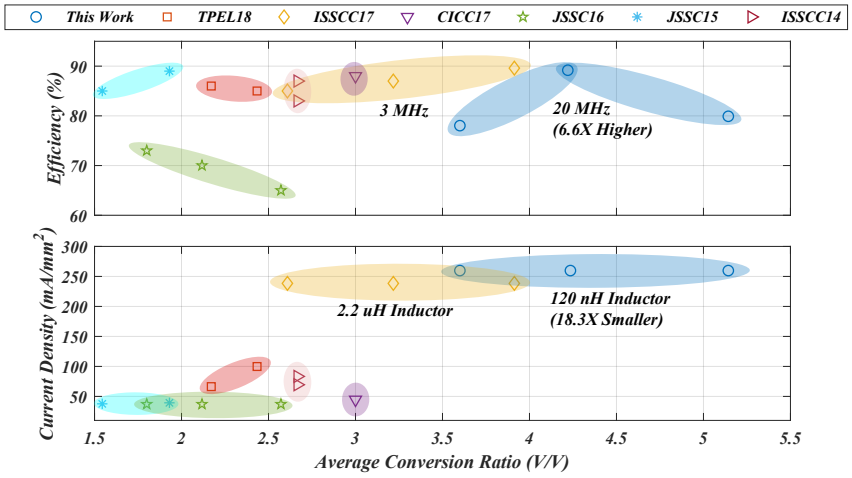


Figure 3.22. The SIMO converter efficiency and current-density comparison with prior works.

Table 3.1. Comparison with prior state-of-the-art work.

Converter Specification	**This Work**	**ISSCC14 [44]**	**JSSC15 [43]**	**CICC17 [41]**	**TPEL18 [39]**	**ISSCC17 [40]**	**JSSC16 [42]**
Technology	65 nm CMOS	350 nm CMOS	350 nm CMOS	130 nm CMOS	180 nm CMOS	28 nm CMOS	65 nm CMOS
First Stage	Dual Hybrid SC	Buck	Buck	Dual SC	Buck	3-Level Buck	Dual Buck
Control Method	Time-Based	RBAOT	Error-Based	Gate-Drive Modulation	OVACC	SRC & AFC	Current-Mode
V_{IN} (V)	3.2 - 3.6	2.7 - 5	5	2.4 - 4.2	3.3 - 4	3 - 4.5	1.6 - 2
V_{OUT} (V)	0.7 - 1	0.6 - 1.8	1.8 - 3.3	0.8 - 1.6	0.9 - 2.2	0.8 - 1.45	0.6 - 1.2
f_{SW} (MHz)	20	1	0.7	1	1	3	20 & 100
C_{OUT} (μF)	0.43	10	10	2.2	10	2	0.01
L (μH)	2 x 0.06	4.7	4.7	Not Applicable	4.7	2.2	2 x 0.2
Cross Regulation (mV/mA)	None Observed	0.04	0.1	0.01	None Observed	0.032	None Observed
Ripple (mV)	40	30	40	20	25	5	40
η_{MAX} (%)	88.3	87	88.7	87.6	86	89.6	74
Area (mm^2)	3.08	5.4	11.75	14.57	5.52	2.5	3.6
Power Density (mW/mm^2)	450	400	130	100	410	460	100

3.5 Comparison with State-of-the-Art

The presented sensor-less current-mode control of the two-stage SIMO DC-DC converters eliminates the cross-regulation and need for sensitive analog peripherals. The dual-phase coupled-inductor design along with the first-stage Dickson SC and low-parasitic packaging of the converter improved the efficiency and current density compared to the prior state-of-the-art designs.

The converter is tested in the dual-phase operation. The L_P and L_N nodes of both converters in the buck and boost modes at steady-state and the optimal phase are shown in Fig. 3.19 with the loads regulated at 33 mA per channel and 16 mV ripple. The transient measurements of converter A, with converter B in steady-state, under a 300 mV DVS steps at the fourth channel with no cross-regulation observed at other channels are shown in Fig. 3.20. The comparison with the prior works and efficiency measurements are shown in Table 3.1 and Fig. 3.22. The coupled-inductor improves the light load efficiency and alleviates the need for extreme switching frequencies [42] to lower the ripple loss. The proposed design utilizes significantly smaller magnetics compared to the buck architectures [39, 43, 44] as well as higher current-density and efficiency at larger conversion ratios compared with the multilevel design [40]. In addition, the current-density are much greater than the hard-charging SC design [41].

Chapter 4

A Quad Gate-Driver for Cascaded Resonant Converter

4.1 Introduction

Datacenter and telecommunication applications place stringent requirements on the efficiency and power density of step-down DC-DC converters. High efficiency yields lower operating costs and less challenging thermal management, while high power density frees up valuable real estate for computing and communication components. Recently, hybrid switched-capacitor (SC) converters [57, 58, 59, 60] have demonstrated high performance in research prototypes for the emerging 48 V DC bus standard in datacenter, owing to the increased energy density of multi-layer ceramic capacitors (MLCCs) compared to power inductors. Moreover, hybrid SC solutions achieve their high performance through the advantageous property that each switch in steady-state is only exposed to a fraction of the input voltage, enabling the use of low-voltage semiconductor switches with low on-state resistance and reduced parasitic capacitance. However, the increased number of semiconductor switches, as well as attendant gate driving, level-shifting, and high-side gate drive power requirement pose practical implementation challenges that must be overcome. Furthermore, the use of low-voltage switches requires careful attention to start-up and shutdown conditions, where the switch rating may be inadvertently exceeded. In this work, we present a fully integrated controller and gate-driver for the cascaded resonant converter [1] and demonstrate its performance in a 48 V to 6 V DC-DC step-down converter, delivering 30 A to the output. The converter is intended as an intermediate bus converter (IBC), and thus does not require regulation, which is handled by a final point-of-load (PoL) converter. While conventional IBCs for datacenters typically provide 48 V to 12 V (4:1) step-down followed by a 12:1 PoL converter, the presented prototype addresses – thanks to the increased level of integration - the more challenging 8:1 step-down ratio. The resulting decreased input voltage and step-down requirement of the PoL converter – often the largest and least efficient converter in the power delivery chain – yields significant system-level benefits. In addition, the lower output voltage of IBCs enables application of more advanced CMOS processes

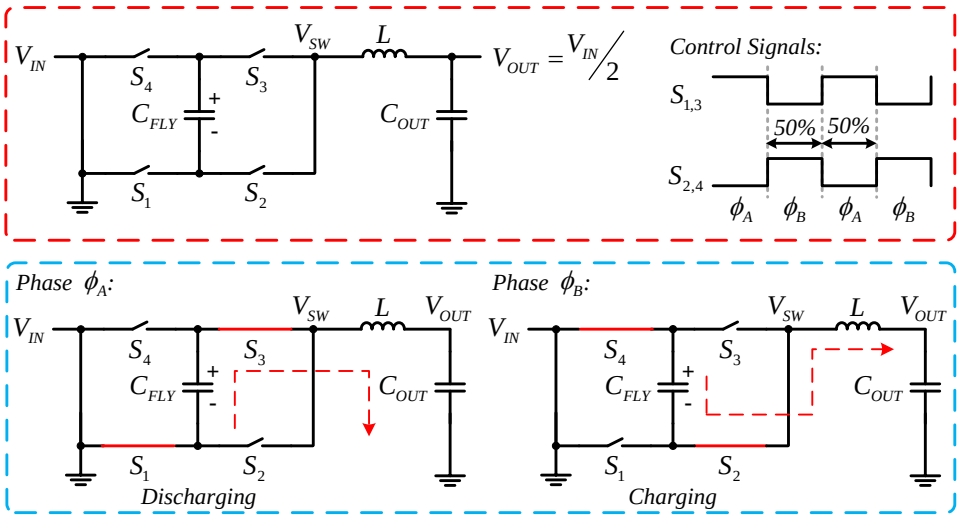


Figure 4.1. The 2:1 SC converter cell.

in the design of the final PoL converter for a high-bandwidth regulation at the PoL. However, a lower bound should be considered in the selection of IBCs output voltage based on their respective application as the increasing current can have a significant efficiency drawback given the parasitic resistance of the long PCB traces between the IBC and the final PoL converter. In addition, the parasitic inductance of the PCB traces can introduce severe ringing during the load step changes. The physical distance of the IBC and the final PoL converter is yet a remaining challenge in the floorplan design of larger systems, where a 3 V to 6 V voltage domain is gaining popularity across the datacenter applications for its desirable trade-offs.

4.2 Resonant 2:1 SC Converter

The 2:1 SC converter is the simplest SC series-parallel topology and a building block of more complex architectures. The 2:1 SC converter cell, used in the design of cascaded resonant converter, is shown in Fig .4.1. Given the symmetrical two-phase operation of a 2:1 SC converter cell in resonant mode at 50% duty-cycle per phase, the controller design is simplified and the need for complex and energy consuming variable pulse-width modulators is omitted. In addition, the symmetrical two-phase operation opens the opportunity for a more advanced bootstrap technique presented in this work to eliminate the lossy bootstrap diode used in the conventional bootstrap method, which is shown in Fig. 4.2. The drawback of bootstrap diode is the accumulated voltage drop as the number of chained bootstrap stages increases, which in-turn requires a higher voltage at the auxiliary input V_{AUX} to compensate for the voltage drop. With increasing number of the bootstrap stages, the growing V_{AUX} pushes the stress limits on the integrated peripheral devices to a point where more complex cascoded configuration or drain-extended devices should be used. In addition, the need for the auxiliary low dropout linear regulator (LDO) to provide a uniform voltage across the gate-drivers increases the system complexity and power consumption. Hence,

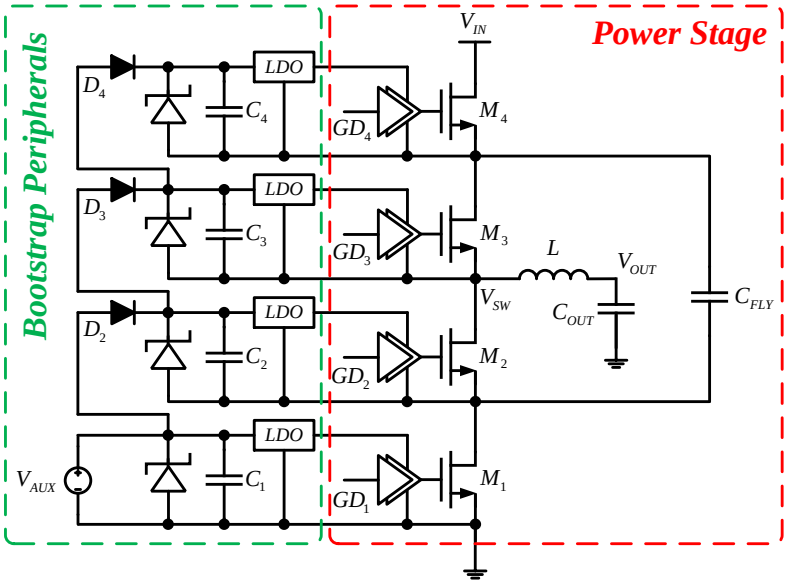


Figure 4.2. The conventional diode-based bootstrap method used for 2:1 SC resonant converter cell.

the active bootstrap method proposed in this work has the potential to improvement the system design by replacing the bootstrap diode with an active switch to eliminate the voltage drop and its consequent design overheads and deficiencies. A top level system schematic diagram is shown in Fig. 4.3. In addition, the start-up and shutdown procedures have been challenging in SC converters as the voltage stress across the power switches should be maintained and bounded for reliability during the start-up and shutdown periods. This work extends on the prior design [57] to include the start-up and shutdown features through an assist switch M_{ST}, as shown in Fig. 4.3, for a stand-alone operation and providing a hot-swapping capability.

The 2:1 SC converter cell is operated in the resonance mode to achieve zero current switching (ZCS) as investigate in the prior design [57]. The resonance mode provides an advantages in the power-density as the filter inductor and flying capacitor can be downsized significantly. However, the increased RMS current ripple through the resonating components increases the conduction loss and degrades the efficiency, especially at the light load regime. This bottleneck in efficiency can be partially relieved through zero voltage switching (ZVS) as shown in [57]. In addition, by increasing the switching frequency to lower the RMS current, at the cost of operating in partial ZCS mode and increased switching loss, a balanced point between the conduction and switching loss can lead to achieve a maximum available efficiency. The resonance frequency of converter is determined by the following equation:

$$f_R = \frac{1}{2\pi\sqrt{C_{FLY}L}} \tag{4.1}$$

where the C_{FLY} is assumed to be much smaller than the C_{OUT}. Given the relatively large C_{FLY} value in μF range compared with the parasitic capacitance of the system, it is also safe to assume the equivalent resonance capacitance of C_{FLY} is sufficient to compute the resonance frequency.

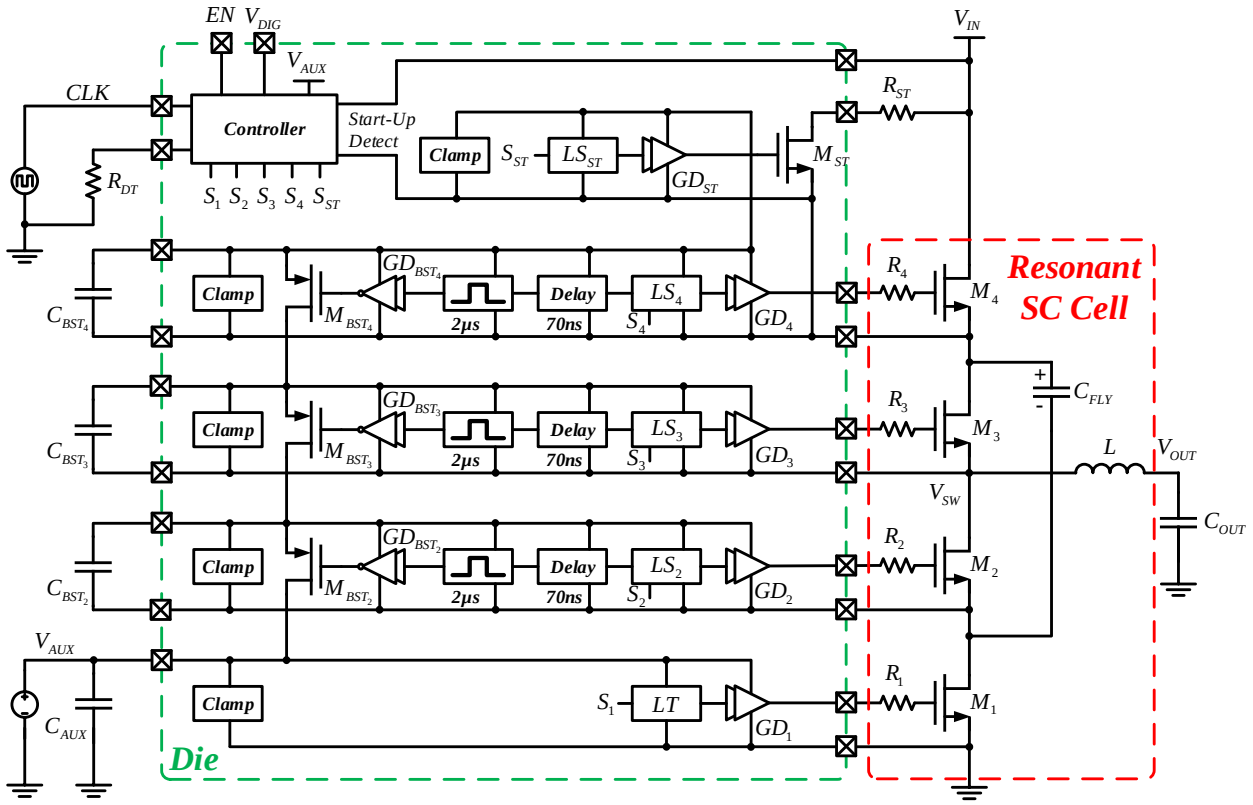


Figure 4.3. The quad gate-driver IC top level system schematic diagram.

In addition, slight mismatches raised from the computation error and the MLCC derating due to the DC-bias, AC amplitude and the operating temperature can be disregarded as the output characteristic impedance R_{SC} of the 2:1 SC resonant converter has low sensitivity to the switching frequency f_{SW} deviation as shown in the Fig. 4.4 and computed by equation below:

$$R_{SC} = \frac{\frac{V_{IN}}{2} - V_{OUT}}{I_{OUT}} \tag{4.2}$$

It is also worthy to note that the sensitivity and variations of the 2:1 SC resonant converter R_{SC} to f_{SW} is highly a function of the inductor placement. The R_{SC} versus f_{SW} is plotted in Fig. 4.5 for the inductor placement on the output [57] in comparison to the inductor in series with the C_{FLY} [72]. The working principle, design and measurements of the peripheral building blocks of the quad gate-driver IC, as shown in the Fig. 4.3 top level schematic diagram, are discussed in detail in the following sections.

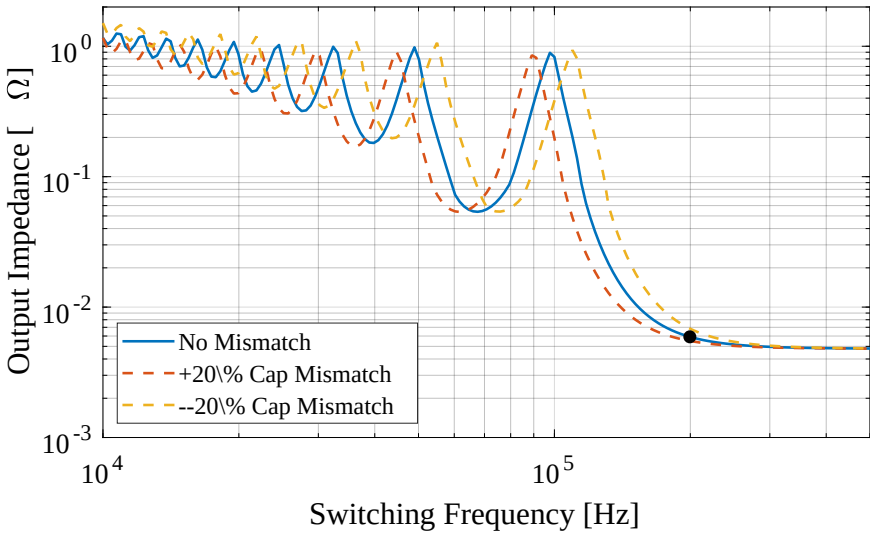


Figure 4.4. The C_{FLY} mismatch effect on the output impedance with $f_R = 200kHz$, $C_{FLY} = 12.7\mu$F and $L = 50nH$.

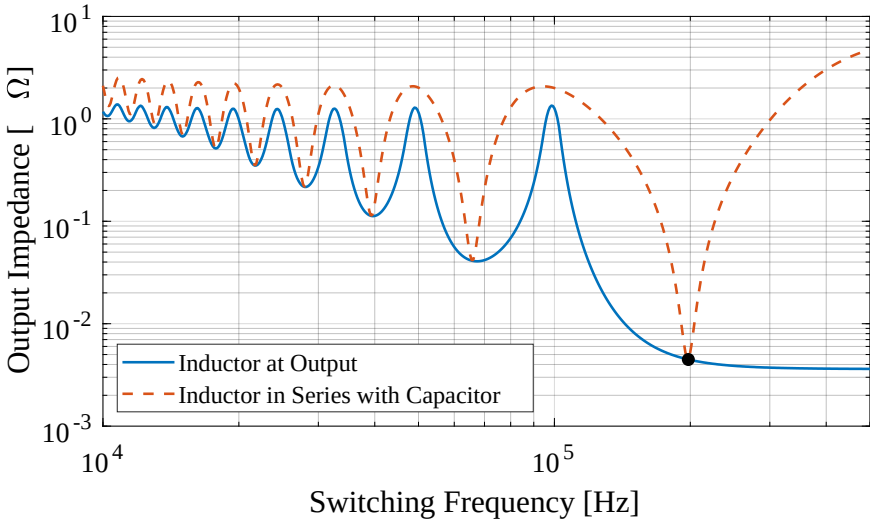


Figure 4.5. The inductor placement effect on the output impedance with $f_R = 200kHz$, $C_{FLY} = 12.7\mu$F and $L = 50nH$.

4.3 Implementation

A hardware prototype demonstrating these concepts was developed in the 180nm BCD process. This section is focused on the working principle and the circuit design of the peripheral building blocks necessary for a stand-alone operation of the 2:1 SC resonant converter.

4.3.1 Active Bootstrap

The active bootstrap is the key circuit level contribution of this work. The power delivery to gate-drivers is the most challenging part of the conventional switched-capacitor converters as majority of the power switches and their corresponding gate-driver are not ground referred and floating across multiple voltage domains. It is also important to note that the floating gate-driver and their power delivery techniques should be prone to fast slew rates of the floating wells as the SC converters voltage domains can switch as fast as 50 V/ns [57]. Among the several power delivery methods to the floating gate-driver, the isolated coupled-coil technology from Analog Devices [62], isolated RF-Link technology of Silicon Labs [63] and the non-isolated conventional bootstrap methods [57, 61] are popular among the designers. The isolated coupled-coil and RF-Link technology requires special CMOS process which might not be at the disposal of the designer. Another disadvantage of the coupled coil-technology is the low power delivery efficiency topped at 30% with the current generation, which can produce substantial heat on the PCB and unnecessary loading of the converter's thermal management system. Hence, the non-isolated conventional techniques is more popular if isolation is not critical to the application. Another disadvantage of diode-based bootstrap architectures [57, 65] is the unsymmetrical voltage delivery to the gate-drivers, which has the potential to lead to efficiency degradation and flying capacitor voltage imbalance in the steady-state operation of the converter [68, 69]. The active bootstrap technique presented in this work is an extension of the approach introduced in the earlier designs [57, 70].

The equal timing of each operating phase provides an advantage to utilize the proposed active bootstrap technique to charge the bootstrap capacitors with relaxed timing constraints. The switching phases of the converter along with the active bootstrap states are shown in Fig. 4.6. The active control of bootstrap switches should be synchronized to the converter switching phases ϕ_A and ϕ_B. During phase ϕ_A with power switch M1 being activated, the bootstrap capacitor C_{BST_2} is connected in parallel with the auxiliary input voltage capacitor C_{AUX} and is charged to V_{AUX} through the bootstrap switch M_{BST_2}. Similarly, with the M_3 switch activated, the bootstrap capacitors C_{BST_4} is connected in parallel with the bootstrap capacitor C_{BST_3} and is charged through the bootstrap switch M_{BST_4}. During phase ϕ_B with the M_2 switch activated, the bootstrap capacitors C_{BST_3} is connected in parallel with the bootstrap capacitor C_{BST_2} and is charged through the bootstrap switch M_{BST_3}. The bootstrap switches are controlled via pulsed drivers GD_{BST_n}. The pulsed drivers GD_{BST_n} are activated after 70 ns to compensate for deadtime period and prevent shorting during the deadtime period. The pulse period of 2μs is then utilized to charge the bootstrap capacitors as shown in Fig. 4.6. As bootstrap circuits of Fig. 4.6 suggest, a natural selection of bootstrap switches is a PMOS device with its gate controlled through an auxiliary gate-driver GD_{BST_n} on the same voltage domain as its respective gate-driver GD_n is powered by the bootstrap capacitor C_{BST_n}. In addition, the PMOS devices assist with the start-up and pre-charge procedure as discussed in the next subsection.

The bootstrap driver circuit is shown in Fig. 4.7, where the primary deadtime delay buffering and the bootstrap timer buffer pulse are generated using RC delay circuits as oppose to the design and implementation of more precise process, voltage and temperature (PVT) compensated current-starved delay cell in floating wells. The current-starved delay cell requires the area overhead for a more complex current source design and proper noise isolation as the floating wells can have slew rates as high as 50 V/ns respect to substrate at ground. Given the large margins and relaxed constraints eased by the equal timing of the operating phases and a relatively stable supply voltage provided to the bootstrap driver, the RC value can be selected with proper margins to ensure a safe operation of the active bootstrap circuit, while preserving the die area and less components

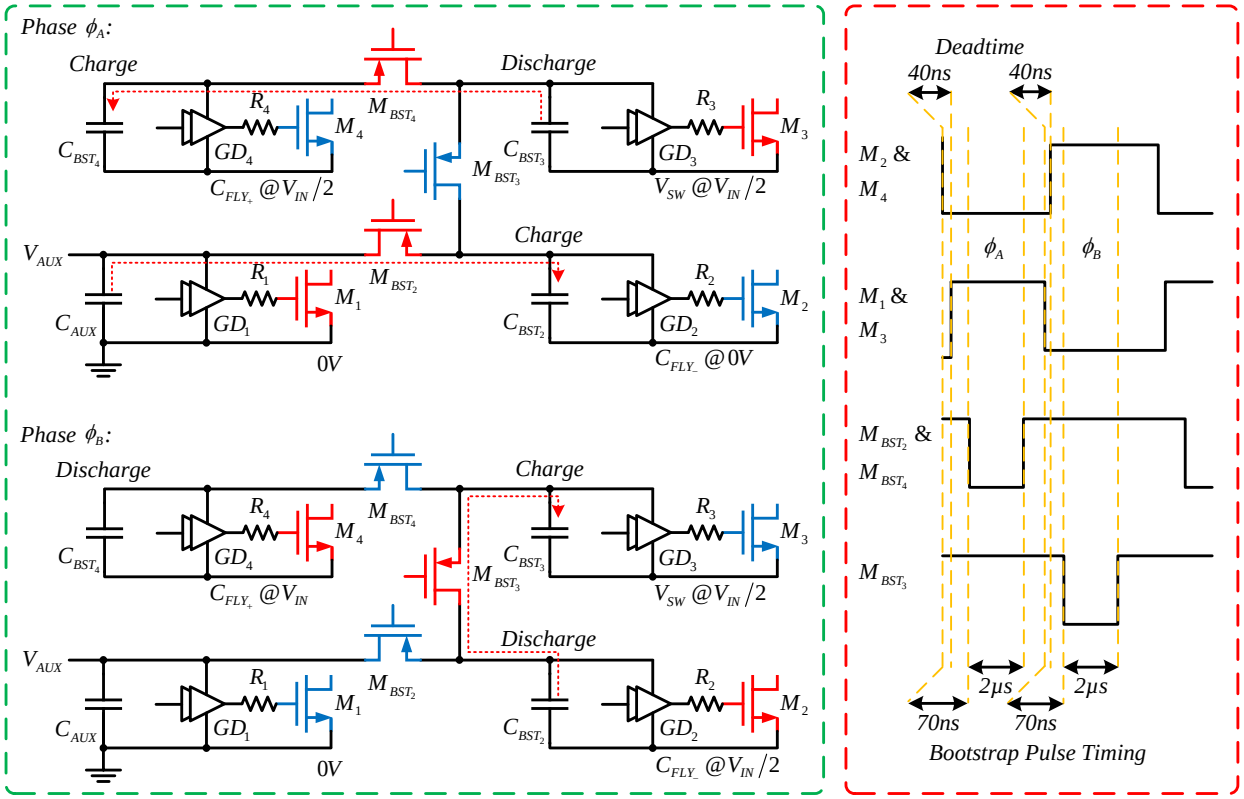


Figure 4.6. The active bootstrap working principle and control signals.

counts for circuit reliability. The deadtime delay buffering of t_{BST-DT} is controlled via selection of RC values R_{DT} and C_{DT}. Similarly, the bootstrap timer buffer pulse of $t_{BST-ACTIVE}$ is controlled via selection of RC values R_{BST} and C_{BST}. A design margin of 25% is considered in design of both t_{BST-DT} and $t_{BST-ACTIVE}$ based on PVT simulation results.

4.3.2 Asymmetric Gate-Driver

In order to minimize the bootstrap capacitors C_{BST} and the bootstrap active switches M_{BST} size, it is critical to reduce the switching losses occurring in the operation of the gate-driver and its peripheral circuits powered by the floating C_{BST}. Equivalently, a lower loss reduces the RC charge time of the C_{BST} to V_{AUX} and effectively increasing the limit on maximum allowable f_{SW}. Given the dominant parasitic dynamic energy loss in a conventional inverter-chain gate-driver is dominated by the shot-through current of the last and largest inverter stage, a feed-forward mechanism [64, 48] for non-overlap activation of the last stage pull-up and pull-down devices is utilized to minimize this loss. In addition, any switching parasitic loss reduction can lead to a higher converter efficiency given the high switching frequency. This feed-forward non-overlap signaling mechanism is designed into the gate-driver architecture through separation of the signal paths leading to the last stage inverter's pull-up and pull-down devices. Each path consist of a inverter chain with asymmetric

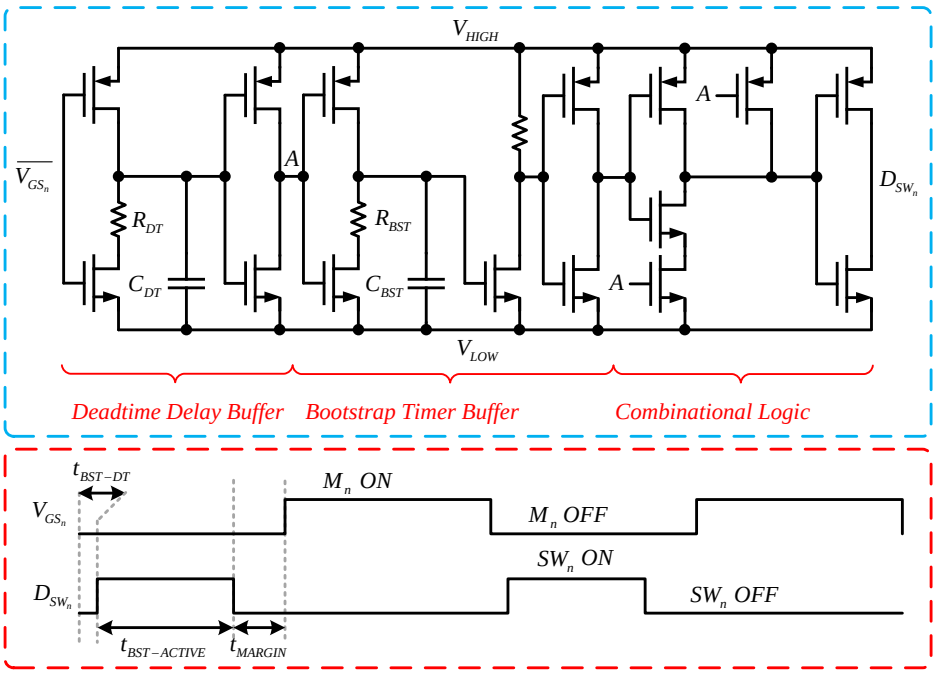


Figure 4.7. The active bootstrap driver circuit and control signals.

delays through alternating adjustments of its devices' sizing as shown in Fig. 4.8. The simulation suggests a maximum 15% energy loss reduction is achieved through applying a 31% asymmetry factor across the process corners and PVT variations. It is important to note that the overall W x D of the asymmetric gate-driver inverter-chain is kept constant in reference with its conventional invert-chain design. Thus, area overhead of 8%is consumed for the extra required metalization and guardring designs. A tappering factor of 14 is used in the design of the gate-driver. A similar approach is taken in the design of the bootstrap PMOS device gate-driver GD_{BST} as shown in Fig. 4.3.

4.3.3 Fast Level-Shifter

The conventional desired parameters used in the design of power converter level-shifters are the signal isolation, delay matching and minimization across a wide range of voltage domains while providing proper signal integrity. The signal isolation requirement is merely a function of the application. The static level-shifters are by far the most simple and popular designs, however they do not provide isolation as some newer and complex topologies such as coupled-coil or RF-Link techniques are benefiting from. The work presented here doesn't require signal isolation, thus the simpler static level-shifter is utilized. The delay matching and minimization as well as common-mode rejection should be approached at both circuit and layout levels to provide the optimal solution on the given CMOS process. The level-shifter architecture used in this work is a modified SR-latch based design [49**?**] to provide symmetrical low-to-high t_{LH} and high-to-low t_{HL} delays

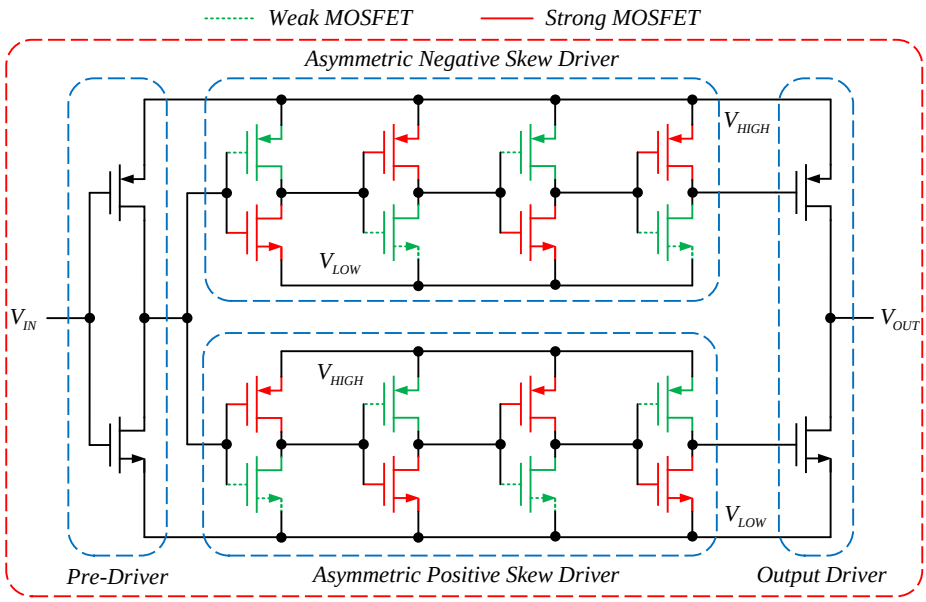


Figure 4.8. The asymmetric gate-driver architecture.

across PVT variations and device corners at the switching transitions as shown in Fig. 4.9. In addition, the level-shifter design for high-power switched-capacitor converter introduce a challenge to compensate for the signal integrity issues raised as the floating gate-driver N-well switches across voltage domains with slew-rates as highs as 50 V/ns. The N-well parasitic capacitance coupled to the substrate and level-shifter devices can induce significant number of glitches to the signal lines. Therefore, circuit and layout techniques should be devised to minimize the cross-talk between the parasitic elements coupled to the floating N-well.

The high-side latch and voltage followers devices layout geometry are designed carefully for matching to consider a high common-mode rejection for protection of the gate terminals from over-voltage stress and reliability issues. In addition, the devices are minimum sized to reduce the parasitic capacitance for a fast transient response. In the other hand, the low-side current-steering switches and the respective inverter are designed for minimum delay across the differential output nodes for a high common-mode rejection consideration. The level-restore logic is also designed with minimum sized devices. With all the design consideration to maximize the common mode rejection, the high slew-rates as high as 50 V/ns across the floating wells to ground and the pico-second delay range between the differential signals of the static level-shifter can lead to small glitches at the transient and switching events. Hence, a secondary protection measure is taken by employing zener diodes across the high-side latch gate terminal as shown in Fig. 4.9. Moreover, small glitches can propagate through the level-restore logic and causes false triggering of the decoder latch. Hence, a Schmitt trigger inverter is inserted at the output of the level-restore logic to provide a hysteresis band for filtering of the small glitches. The decoder latch is designed with pull-up and pull-down resistive devices as shown in Fig. 4.9 to lock the latch in the reset mode during the start-up of the converter. The ground referred gate-driver GD_1 is controlled via the level-translator as shown in Fig. 4.10 in chain with a decoder.

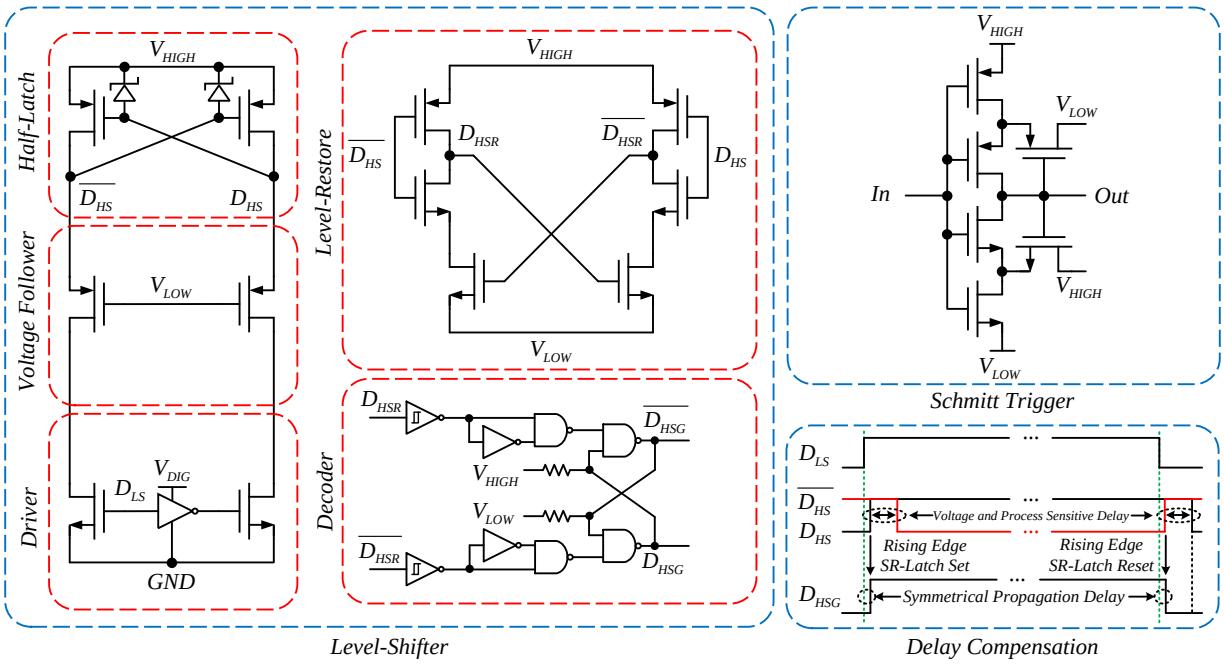


Figure 4.9. The level-shifter used for the floating gate-driver GD_{2-4}.

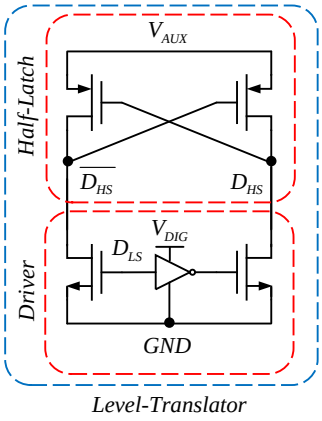


Figure 4.10. The level-translator used for the ground refereed gate-driver GD_1.

4.3.4 Start-Up and Shutdown

The start-up procedure of the converter consists of the bootstrap circuit C_{BST} pre-charge and the power stage C_{FLY} pre-charge phases. Similarly, the shutdown procedure is a reversed start-up operation. The start-up and shutdown features place the design ahead of the conventional approach [57], where the input voltage is ramped-up and ramped-down to cycle through the start-

up and shutdown phases. In addition, the added features enable the converter for hot-swapping application. The three-stage converter start-up and shutdown procedures are operated under no load conditions. However a hybrid design can be devices to provide an auxiliary power supply, such as linear a regulator, to the output during the start-up and shutdown procedure to support any rated loads. The following subsections focus on the start-up and shutdown phases of the converter.

Bootstrap Pre-Chrage

The bootstrap pre-charge is the first phase in the start-up procedure of the converter. It is necessary to have control over the power stage switches as the converter goes through the start-up phase. Hence, the bootstrap capacitors should be charged to power the level-shifter and gate-driver circuits. Equally important, the level-shifter design has an embedded reset function to ensure the power switches are kept off as the V_{HIGH} and V_{LOW} voltages rise to establish the differential voltage of V_{AUX} during the start-up phase. The bootstrap pre-charge phase is initiated by activating the power switch M_1 through the ground refereed GD_1 as shown in Fig. 4.3 and Fig. 4.11. With the drain of power switch M_2 grounded, the bootstrap capacitor C_{BST_2} is charged to $V_{AUX} - V_D$ at time-step T_{STEP_1}, where V_D is the body-diode voltage drop of the bootstrap PMOS device M_{BST_2}. With the C_{BST_2} powered, the level-shifter and respective gate-driver of power switch M_2 becomes operational. Hence, by activating M_2, the C_{BST_2} charges up to $V_{AUX} - 2V_D$ at time-step T_{STEP_2}. Similarly, the C_{BST_3} is charged to $V_{AUX} - 3V_D$ at time-step T_{STEP_3}. With the bootstrap capacitors partially charged, the converter is cycled through a clock period at time-step T_{STEP_4} with the power stage switch M_4 still deactivated in order to charge the bootstrap capacitors C_{BST_2} and C_{BST_3} through their respective bootstrap switches M_{BST_2} and M_{BST_3}. Therefore, at time-step T_{STEP_5} the bootstrap capacitors C_{BST_2} and C_{BST_3} are sequentially charged to approximately V_{AUX} and bootstrap capacitor C_{BST_4} through the M_{BST_4} body-diode to $V_{AUX} - V_D$. With the bootstrap capacitors nearly charged to their steady-state operation voltage level, it is guaranteed that the level-shifters and gate-drivers have the power stage switches under control and the flying capacitor pre-charge phase can be initiated. In addition, the nearly charged bootstrap capacitors protects the converter during longer flying capacitor pre-charge phase against accidental control loss as the bootstrap capacitor loose charge through leakage over time. This pre-charge sequence is shown in Fig. 4.11.

Start-Up Procedures

The second phase of the start-up begins by pre-charging the flying capacitor C_{FLY} to $V_{In}/2$. With the full control of the power stage switches after the bootstrap capacitors pre-charge phase, the C_{FLY} is charged to $V_{In}/2$ through R_{ST} current limiting resistor and M_{ST} pre-charge assist switch as shown in Fig. 4.3. A three-stage converter start-up phase is shown in Fig. 4.12, where the first-stage serves as the ramp generation circuit by blocking the high-voltage input and the following stages operate in the steady-state switching mode to synchronously charge and discharge their flying and output capacitors during the start-up and shutdown respectively.

The first-stage power switch M_4 is rated for the full input voltage and provide blocking functionality to protect downstream transistors before all flying capacitors are fully charged. The dedicated pre-charge resistor R_{ST} provide a selectable and controlled charging current of capacitor C_{FLY} with its negative terminal grounded through M_1, while the output capacitor is simultaneously be-

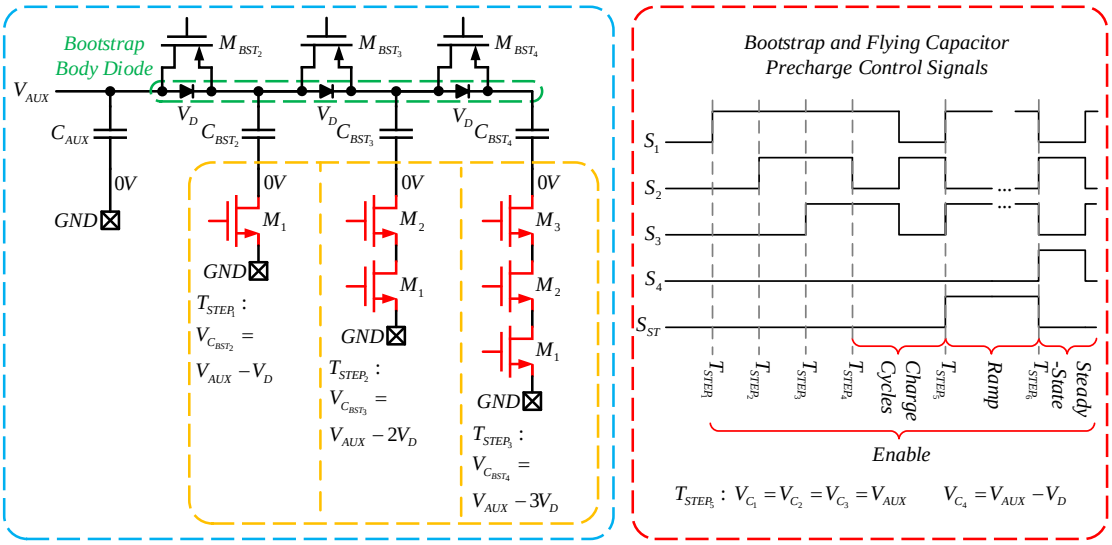
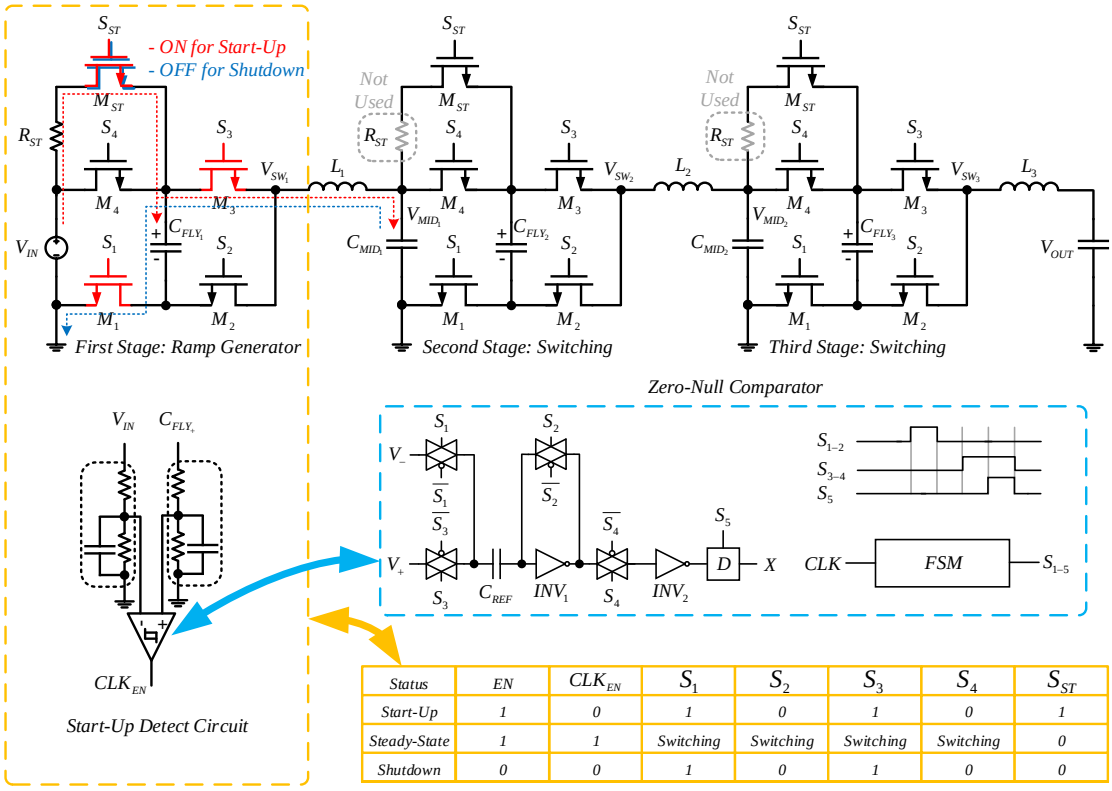


Figure 4.11. The bootstrap pre-charge diagram during the start-up phase.



Status	EN	CLK_{EN}	S_1	S_2	S_3	S_4	S_{ST}
Start-Up	1	0	1	0	1	0	1
Steady-State	1	1	Switching	Switching	Switching	Switching	0
Shutdown	0	0	1	0	1	0	0

Figure 4.12. The pre-charge of three-stage converter.

ing charge through the inductor and M_3. A voltage comparator tracks the charging of C_{FLY} to $V_{In}/2$ and deactivate M_{ST} to transition the converter into steady-state operation as shown in Fig.

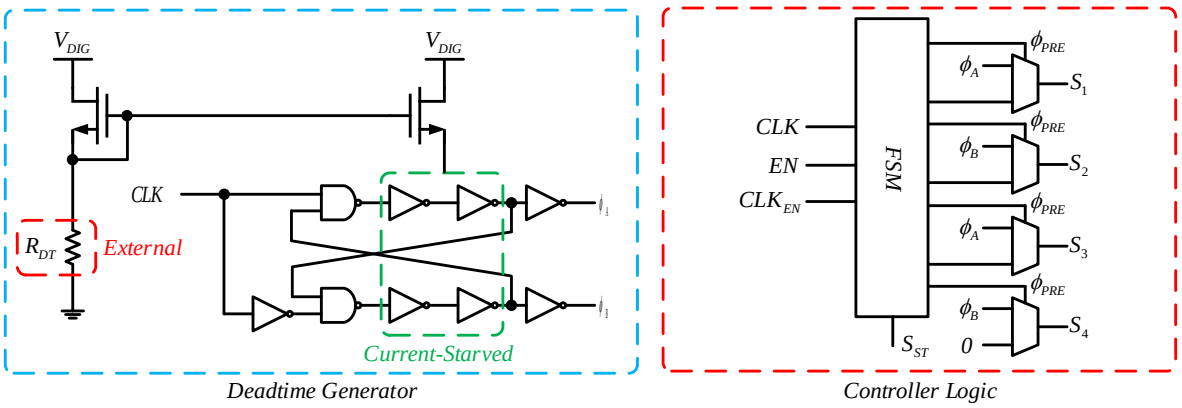


Figure 4.13. The controller and deadtime non-overlap clock generator.

4.12. The voltage comparator is designed with the zero-null architecture [45] and connected to the input voltage and output flying capacitor top-plate through a resistive network as shown in Fig. 4.12. The voltage comparator is disables after the start-up phase to eliminated accidental deactivation of the converter.

Shutdown Procedure

During shutdown operation, power switch M_1 permanently grounds the negative terminal of C_{FLY_1} in the first-stage and disconnects the converter from the input supply by disabling power switch M_4 and start-up assist switch M_{ST}. With the power switch M_3 kept on, the flying capacitor C_{FLY_1} acts as the input supply to the second-stage and third-stage converters. Hence, the switching second-stage and third-stage converters deplete the C_{FLY_1} charge and the converter ramps-down to shutdown as shown in Fig. 4.12.

4.3.5 Controller

The converter is designed with an embedded controller which handles the start-up and shutdown procedure as well as the steady-state operation. The controller is powered by the V_{DIG} and fed by an external reference clock as shown in Fig. 4.3. The controller consists of a FSM and a non-overlap generator as shown in Fig. 4.13. The non-overlap deadtime generator delay is controlled via a the external resistor R_{ST} and the current-starved inverters as shown in Fig. 4.13. The deadtime delay is controllable within 5 ns to 40 ns range. The controller logic consists of a FSM and output multiplexers. The pre-charge multiplexer signal ϕ_{PRE} is controlled as the table in Fig. 4.12 summarizes to produce the S_{1-4} and S_{ST} signals as shown in the precharge phases of the start-up in Fig. 4.11.

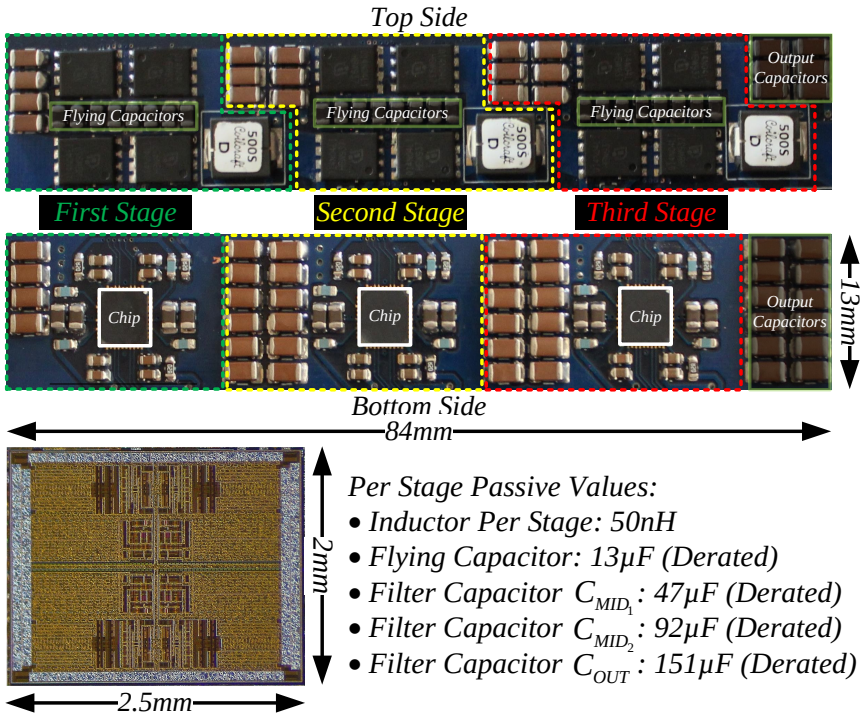


Figure 4.14. The three-stage converter with quad gate-driver in 40 lead QFN package and the die micrograph.

4.3.6 ESD & and High-Voltage Latch-Up Protection

All the converter input signal pads are protected through ESD clamps and input resistors. The ESD power clamp is also used across the V_{AUX} and V_{DIG} to GND in order to protect the control peripheral circuits. The floating deep N-Well of gate-drivers are protected through 55 V ESD diodes of each respective V_{DD} pads. In addition, the high-side 5 V switch devices of levels-shifter, gate-driver and bootstrap peripherals inside the deep N-Well are protected through the body-diode of large gate-driver inverter chain devices across the floating V_{SS} and V_{DD} pads as recommended by the manufacturer. The high-voltage and low-voltage wells are protected against latch-up through strong substrate ground connection and isolation spacing recommended by the manufacturer for the rated wells' voltage.

4.3.7 Packaging and Three-Stage Converter

The converter is implemented in 180 nm BCD process and packaged with 40 lead QFN package as shown in Fig. 4.14. The die area of 5 mm^2 is used in the design of quad gate-driver chip. The chip micrograph of Fig. 4.14 highlights the compact overall size of the quad gate-drive, which contains full driving functionality, control, and start-up for four power MOSFETs. The PCB has a total area of 1092 mm^2 and thickness of 4.1 mm, which places the power density at maximum value of 660 W/in^3.

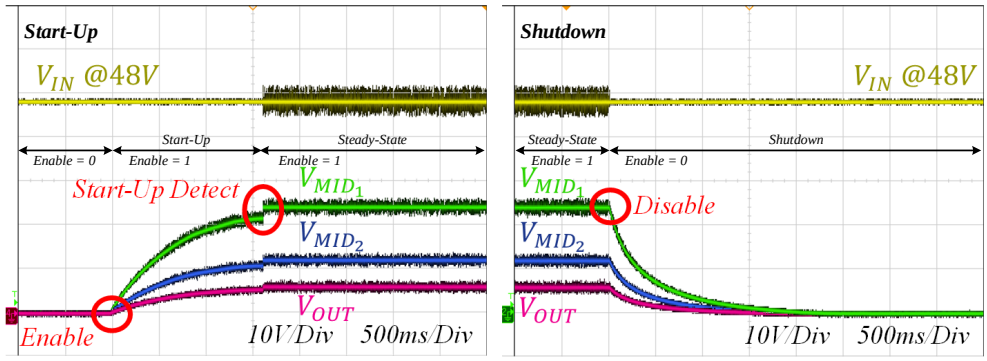


Figure 4.15. The three-stage output voltage measurement at start-up phase.

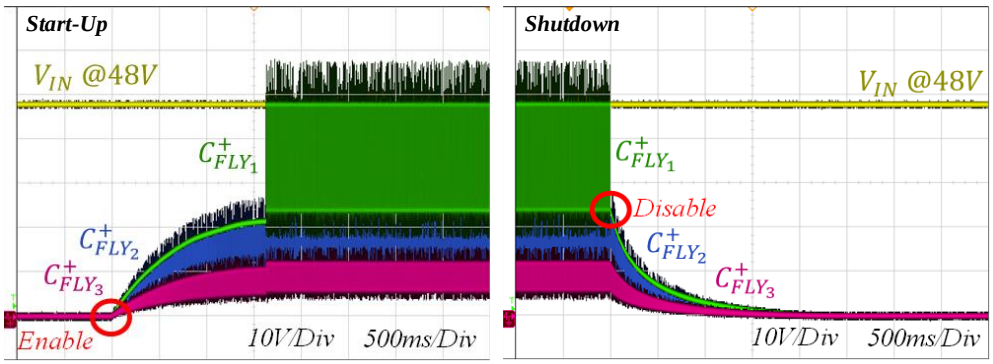


Figure 4.16. The three-stage flying capacitor voltage measurement at start-up phase.

4.4 Three-Stage Cascaded SC Resonance Converter

4.4.1 Start-Up and Shutdown Measurements

The three-stage converter at start-up phase is measured and shown in Fig. 4.15 and Fig. 4.16. With the enable signal inserted, the flying capacitor C_{FLY_1} starts to charge through the R_{ST} and ramps-up as the C_{FLY_2} and C_{FLY_3} of the second-stage and third-stage converters charge through steady-stage switching. As the flying capacitor C_{FLY_1} voltage reaches $V_{In}/2$, the start-up detect comparator triggers and shifts the first-stage converter into steady-state switching as shown in 4.16. In parallel, the output voltage plot of Fig. 4.15 shows the voltage tracking of the second-stage and third-stage as the first-stage flying capacitor C_{FLY_1} ramps-up through R_{ST}. Similarly, the plot of Fig. 4.16 shows the shutdown procedure as the first-stage converter exits the steady-state switching and disabling power switch M_4 and start-up assist switch M_{ST} while enabling the ground referred power switch M_1 as well as M_3. The flying capacitor C_{FLY_1} acts as the input source to the second-stage and third-stage, while the converter is isolated from V_{In} by the high-voltage block power switch M_1 of the first-stage. The continuously switching second-stage and third-stage deplete the flying capacitor C_{FLY_1} to shutdown as shown by the Fig. 4.15 showing the output voltages and Fig. 4.16 showing the flying capacitor voltages.

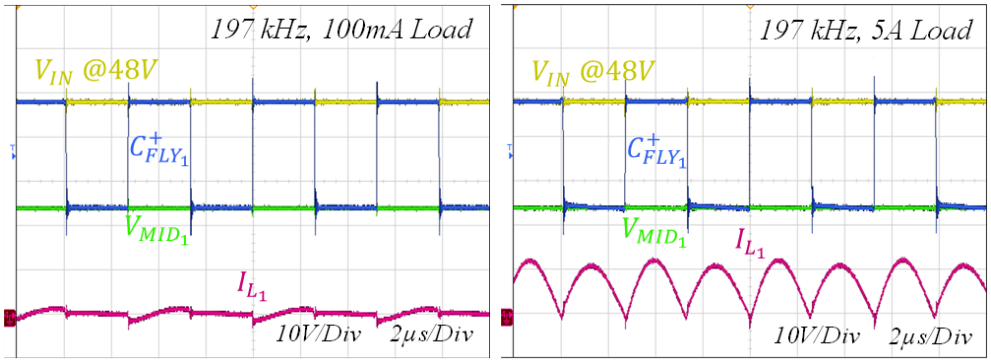


Figure 4.17. The resonance operation at steady-state.

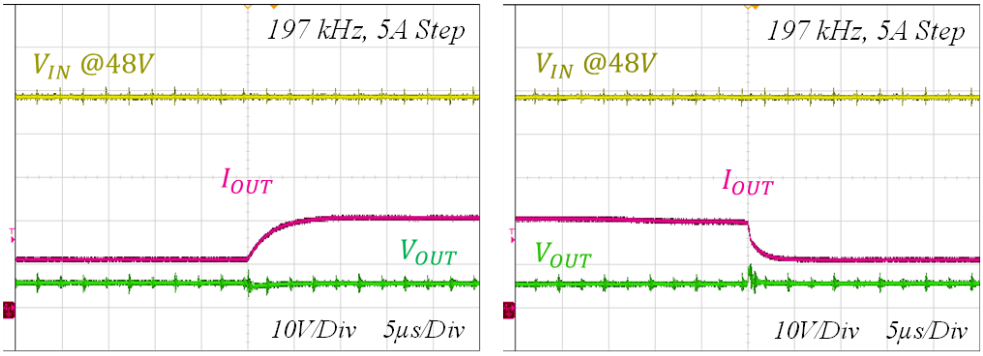


Figure 4.18. The three-stage output voltage measurement at start-up phase.

4.4.2 Steady-State Resonance Measurements

The converter is measured for resonance steady-state operation at the wide load range. The plots of Fig. 4.17 shows the input / output, the switching node and the inductor current of the first-stage converter for 100 mA and 5 A loads. The resonance frequency of 197 kHz is measured with 50 nH inductor and derated C_{FLY_1} of 13 μF. The second-stage and third-stage are also tuned by adjusting the flying capacitors C_{FLY_2} and C_{FLY_3} to resonate at a similar frequency.

4.4.3 Transient Measurements

The converter is measured for resonance steady-state operation at the wide load range. The plots of Fig. 4.18 shows the input / output voltages as well the output current during a load-step transient of 5 A. The step-up and step-down load transients shown in Fig .4.18 suggest a overshoot and undershoot respectively.

Table 4.1. Comparison with prior state-of-the-art work.

Converter Specification	This Work	ISSCC20 [66]	ISSCC20 [65]	LTC7821 [61]	TPEL20 [57]
Topology	Non-Isolated Cascaded Resonant	Non-Isolated Buck	Isolated 3-Level Buck + Current Doubler	Non-Isolated 3-Level Buck	Non-Isolated Dual Interleaved Cascaded Resonant
Technology	0.18 μm CMOS BCD	0.5 μm 120V CMOS	0.18 μm CMOS BCD	Not Reported	Discrete Design
Switching Method	Resonance ZCS	HS / AZVT	HS	CCM / DCM / Burst	Resonance ZCS / ZVS
V_{IN} (V)	32 - 56	48 - 80	48 - 60	10 - 72	36 - 60
V_{OUT} (V)	4 - 7	12	0.5 - 1	2 - 34	9 - 15
I_{MAX} (A)	30	5	60	25	60
P_{MAX} @ 48 V V_{IN} (W)	180	60	60	125	720
f_{SW} (kHz)	200	2000	333	200 - 1500	100
L	3 x 50 nH	1 x 1.5 μH + 1 x 0.82 μH	1 x 1.5 μH + 4:1 Transformer	1 x 2 μH	2 x 50 nH + 2 x 180 nH
Total Derated C (μF)	329	18.8	Not Reported	480	467
η_{max} (%) @ Conversion Ratio	97.9 @ 8	93.6 @ 6.66	92.8 @ 48	97.8 @ 3	99 @ 4
Full Load η_{max} (%) @ Conversion Ratio	97.6 @ 8	92.5 @ 4	85 @ 48	94 @ 9.6	97.23 @ 4

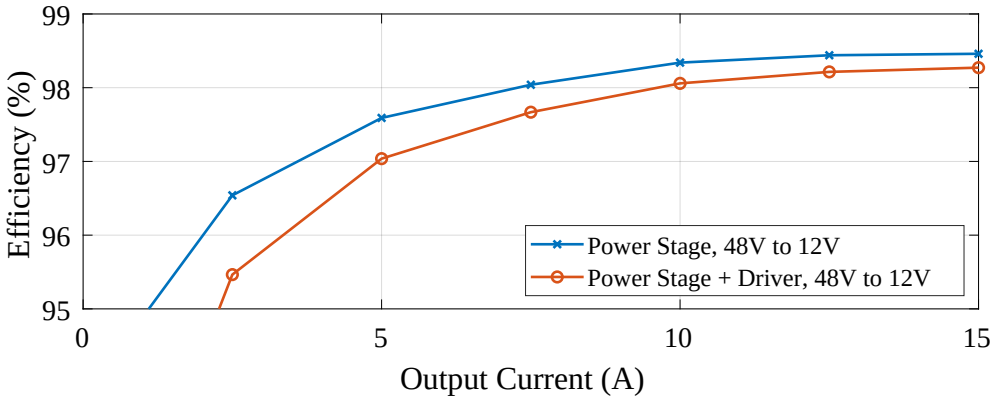


Figure 4.19. The two-stage efficiency measurements.

4.4.4 Efficiency Measurements

The measurements are taken for the two-stage and three-stage converters with no auxiliary helper circuits during the steady-state operation. The power to the quad gate-driver chips and the power-train stages are measured separately to provide an intuition in characterization of the converter power loss breakdown. Figures 4.19 and 4.20 show the efficiency measurements across the designed load range of 15 A and 30 A respectively. It is critical to note that the middle bypass capacitors should be sized significantly larger than the flying capacitor to provide a low ripple input voltage bus to the proceeding stages. Other methods such as interleaved architecture [57] can be utilized to alleviate the middle bypass capacitor requirements and extend the load range.

During very light-load, ZCS operation is not maintained, as the converter is designed to primarily achieve ZCS during medium to heavy load, to minimize transistor overlap losses. The three-stage converter achieves a peak efficiency of 97.8% at approximately 20 A, with an efficiency above 97% maintained up to full load.

4.5 Comparison and Conclusion

The designed converter has shown promising results in comparison with the prior state-of-the-art works of similar class. The design of quad gate-driver helped in miniaturization and power optimization of the control and auxiliary peripherals required to operate the power-train of 2:1 switched-capacitor cell, effectively reducing the converter footprint and overall energy density. The converter is benchmarked against other state-of-the-art prior works in Table 4.1. Compared to

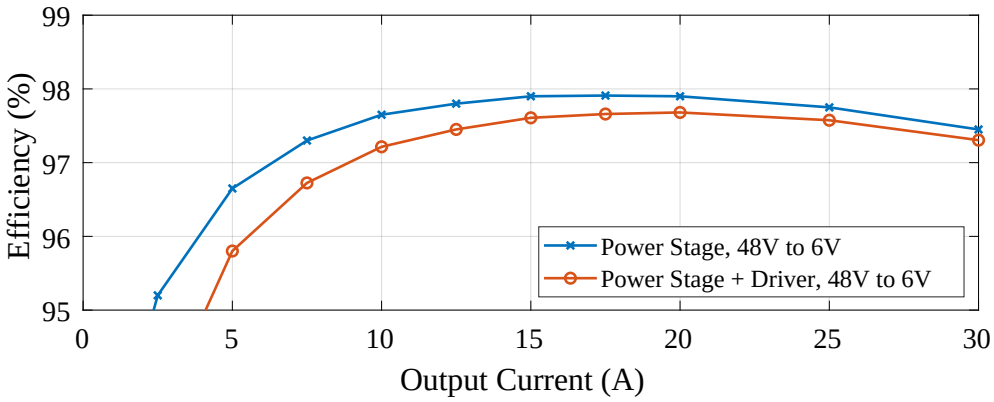


Figure 4.20. The three-stage efficiency measurements.

prior work this work demonstrates the highest efficiency of any CMOS integrated controller, as well as significantly reduced inductor sizes and increased power output compared to past work. Moreover, as shown in the annotated photograph of the PCB hardware prototype of Fig. 4.14, the compact integrated quad gate-drive enables an ultra-compact hardware design with greatly reduced component count compared to conventional, discrete solutions.

The quad gate-driver chip presented in this work demonstrates a step forward in integration of peripherals needed for operation of the 2:1 SC converter resonant cell. This work is the first prototype and most design efforts was directed at correct and robust functionality of the essential blocks. Further follow-up designs can improve on the shortcomings of the current solution, such as a programmable bootstrap timing. Further improvements can be achieved through addition of on-die auxiliary supply to power the control peripherals. Furthermore, the QFN packaging is a bottleneck in further reduction of the chip and consequently the converter. A flipchip packaging can help with the miniaturization and improving the power density of the converter by multiple folds to compete with the industrial solutions [71].

Bibliography

[1] S. Miyano et al., "Highly Energy-Efficient SRAM With Hierarchical Bit Line Charge-Sharing Method Using Non-Selected Bit Line Charges," in IEEE Journal of Solid-State Circuits, vol. 48, no. 4, pp. 924-931, April 2013.

[2] J. Chen, L. T. Clark and T. H. Chen, "An Ultra-Low-Power Memory With a Subthreshold Power Supply Voltage," in IEEE Journal of Solid-State Circuits, vol. 41, no. 10, pp. 2344-2353, Oct. 2006.

[3] S. Jain et al., "A 280mV-to-1.2V wide-operating-range IA-32 processor in 32nm CMOS," 2012 IEEE International Solid-State Circuits Conference, San Francisco, CA, 2012, pp. 66-68.

[4] K. Craig, Y. Shakhsheer, S. Arrabi, S. Khanna, J. Lach and B. H. Calhoun, "A 32 b 90 nm Processor Implementing Panoptic DVS Achieving Energy Efficient Operation From Sub-Threshold to High Performance," in IEEE Journal of Solid-State Circuits, vol. 49, no. 2, pp. 545-552, Feb. 2014.

[5] Y. H. Lee et al., "A Near-Optimum Dynamic Voltage Scaling (DVS) in 65-nm Energy-Efficient Power Management With Frequency-Based Control (FBC) for SoC System," in IEEE Journal of Solid-State Circuits, vol. 47, no. 11, pp. 2563-2575, Nov. 2012.

[6] M. E. Sinangil, N. Verma and A. P. Chandrakasan, "A Reconfigurable 8T Ultra-Dynamic Voltage Scalable (U-DVS) SRAM in 65 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 44, no. 11, pp. 3163-3173, Nov. 2009.

[7] S. H. Lee et al., "12.1 A 0.518mm^2 quasi-current-mode hysteretic buck DC-DC converter with 3μs load transient response in 0.35μm BCDMOS," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, San Francisco, CA, 2015, pp. 1-3.

[8] S. J. Kim et al., "High Frequency Buck Converter Design Using Time-Based Control Techniques," in IEEE Journal of Solid-State Circuits, vol. 50, no. 4, pp. 990-1001, April 2015.

[9] S. J. Kim, R. K. Nandwana, Q. Khan, R. C. N. Pilawa-Podgurski and P. K. Hanumolu, "A 4-Phase 30–70 MHz Switching Frequency Buck Converter Using a Time-Based Compensator," in IEEE Journal of Solid-State Circuits, vol. 50, no. 12, pp. 2814-2824, Dec. 2015.

[10] Y. Lei, W. C. Liu and R. C. N. Pilawa-Podgurski, "An analytical method to evaluate flying capacitor multilevel converters and hybrid switched-capacitor converters for large voltage conversion ratios," 2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL), Vancouver, BC, 2015, pp. 1-7.

[11] J. Jiang, Y. Lu, C. Huang, W. H. Ki and P. K. T. Mok, "20.5 A 2-/3-phase fully integrated switched-capacitor DC-DC converter in bulk CMOS for energy-efficient digital circuits with 14% efficiency improvement," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, San Francisco, CA, 2015, pp. 1-3.

[12] J. Jiang, W. Ki and Y. Lu, "Digital 2-/3-Phase Switched-Capacitor Converter With Ripple Reduction and Efficiency Improvement," in IEEE Journal of Solid-State Circuits, vol. 52, no. 7, pp. 1836-1848, July 2017.

[13] N. Butzen and M. Steyaert, "12.2 A 94.6%-efficiency fully integrated switched-capacitor DC-DC converter in baseline 40nm CMOS using scalable parasitic charge redistribution," 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2016, pp. 220-221.

[14] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters," 2006 IEEE Workshops on Computers in Power Electronics, Troy, NY, 2006, pp. 216-224.

[15] T. M. Andersen et al., "A 10 W On-Chip Switched Capacitor Voltage Regulator With Feedforward Regulation Capability for Granular Microprocessor Power Delivery," in IEEE Transactions on Power Electronics, vol. 32, no. 1, pp. 378-393, Jan. 2017.

[16] D. El-Damak, S. Bandyopadhyay and A. P. Chandrakasan, "A 93% efficiency reconfigurable switched-capacitor DC-DC converter using on-chip ferroelectric capacitors," 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, San Francisco, CA, 2013, pp. 374-375.

[17] Y. K. Ramadass, A. A. Fayed and A. P. Chandrakasan, "A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 45, no. 12, pp. 2557-2565, Dec. 2010.

[18] L. G. Salem and P. P. Mercier, "A Recursive Switched-Capacitor DC-DC Converter Achieving 2ˆN-1 Ratios With High Efficiency Over a Wide Output Voltage Range," in IEEE Journal of Solid-State Circuits, vol. 49, no. 12, pp. 2773-2787, Dec. 2014.

[19] S. Bang, D. Blaauw and D. Sylvester, "A Successive-Approximation Switched-Capacitor DC–DC Converter With Resolution of V˙textIN/2ˆN for a Wide Range of Input and Output Voltages," in IEEE Journal of Solid-State Circuits, vol. 51, no. 2, pp. 543-556, Feb. 2016.

[20] R. C. N. Pilawa-Podgurski and D. J. Perreault, "Merged Two-Stage Power Converter With Soft Charging Switched-Capacitor Stage in 180 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 47, no. 7, pp. 1557-1567, July 2012.

[21] W. Kim, D. Brooks and G. Y. Wei, "A Fully-Integrated 3-Level DC-DC Converter for Nanosecond-Scale DVFS," in IEEE Journal of Solid-State Circuits, vol. 47, no. 1, pp. 206-219, Jan. 2012.

[22] J. Xue and H. Lee, "12.5 A 2MHz 12-to-100V 90%-efficiency self-balancing ZVS three-level DC-DC regulator with constant-frequency AOT V2 control and 5ns ZVS turn-on delay," 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2016, pp. 226-227.

[23] C. Schaef and J. T. Stauth, "A 3-Phase Resonant Switched Capacitor Converter Delivering 7.7 W at 85% Efficiency Using 1.1 nH PCB Trace Inductors," in IEEE Journal of Solid-State Circuits, vol. 50, no. 12, pp. 2861-2869, Dec. 2015.

[24] Y. Lei, R. May and R. Pilawa-Podgurski, "Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter," in IEEE Transactions on Power Electronics, vol. 31, no. 1, pp. 770-782, Jan. 2016.

[25] W. C. Liu, P. Assem, Y. Lei, P. K. Hanumolu and R. Pilawa-Podgurski, "10.3 A 94.2%-peak-efficiency 1.53A direct-battery-hook-up hybrid Dickson switched-capacitor DC-DC converter with wide continuous conversion ratio in 65nm CMOS," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2017, pp. 182-183.

[26] A. Abdulslam and P. P. Mercier, "A Symmetric Modified Multilevel Ladder PMIC for Battery-Connected Applications," in IEEE Journal of Solid-State Circuits, vol. 55, no. 3, pp. 767-780, March 2020, doi: 10.1109/JSSC.2019.2957658.

[27] R. C. N. Pilawa-Podgurski, D. M. Giuliano and D. J. Perreault, "Merged two-stage power converterarchitecture with softcharging switched-capacitor energy transfer," 2008 IEEE Power Electronics Specialists Conference, Rhodes, 2008, pp. 4008-4015.

[28] Pilawa-Podgurski, R. (2012). Architectures and Circuits for Low-Voltage Energy Conversion and Applications in Renewable Energy and Power Management. PhD Dissertation. Massachusetts Institute of Technology.

[29] Y. Lei, Z. Ye and R. C. N. Pilawa-Podgurski, "A GaN-based 97% efficient hybrid switched-capacitor converter with lossless regulation capability," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 4264-4270.

[30] Y. Lei; W. C. Liu; R. C. N. Pilawa-Podgurski, "An Analytical Method to Evaluate and Design Hybrid Switched-Capacitor and Multilevel Converters," in IEEE Transactions on Power Electronics , vol.PP, no.99, pp.1-1.

[31] B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," in IEEE Solid-State Circuits Magazine, vol. 7, no. 2, pp. 12-17, Spring 2015.

[32] S. Thielemans, A. Ruderman, B. Reznikov and J. Melkebeek, "Improved Natural Balancing With Modified Phase-Shifted PWM for Single-Leg Five-Level Flying-Capacitor Converters," in IEEE Transactions on Power Electronics, vol. 27, no. 4, pp. 1658-1667, April 2012.

[33] C. Feng, J. Liang and V. G. Agelidis, "Modified Phase-Shifted PWM Control for Flying Capacitor Multilevel Converters," in IEEE Transactions on Power Electronics, vol. 22, no. 1, pp. 178-185, Jan. 2007.

[34] A. M. Y. M. Ghias, J. Pou, M. Ciobotaru and V. G. Agelidis, "Voltage-Balancing Method Using Phase-Shifted PWM for the Flying Capacitor Multilevel Converter," in IEEE Transactions on Power Electronics, vol. 29, no. 9, pp. 4521-4531, Sept. 2014.

[35] A. Sarafianos and M. Steyaert, "Fully Integrated Wide Input Voltage Range Capacitive DC-DC Converters: The Folding Dickson Converter," in IEEE Journal of Solid-State Circuits, vol. 50, no. 7, pp. 1560-1570, July 2015.

[36] Z. Ye, Y. Lei, W. c. Liu, P. S. Shenoy and R. C. N. Pilawa-Podgurski, "Design and implementation of a low-cost and compact floating gate drive power circuit for GaN-based flying capacitor multi-level converters," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017, pp. 2925-2931.

[37] Y. Moghe, T. Lehmann and T. Piessens, "Nanosecond Delay Floating High Voltage Level Shifters in a 0.35 mum HV-CMOS Technology," in IEEE Journal of Solid-State Circuits, vol. 46, no. 2, pp. 485-497, Feb. 2011.

[38] V. W.-S. Ng and S. R. Sanders, "Switched capacitor DC-DC converter: Superior where the buck converter has dominated," Ph.D. dissertation, Dept. Elect. Eng. Comput. Sci., Univ. California, Berkeley, CA, USA, 2011.

[39] N. Pham, T. Yoo, T. T. Kim, C. Lee and K. Baek, "A 0.016 mV/mA Cross-Regulation 5-Output SIMO DC–DC Buck Converter Using Output-Voltage-Aware Charge Control Scheme," in IEEE Transactions on Power Electronics, vol. 33, no. 11, pp. 9619-9630, Nov. 2018.

[40] L. Chu et al., "10.5 A three-level single-inductor triple-output converter with an adjustable flying-capacitor technique for low output ripple and fast transient response," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 186-187.

[41] Z. Hua and H. Lee, "A 1.2A auto-configurable dual-output switched-capacitor DC-DC regulator with continuous gate-drive modulation achieving ¡0.01mV/mA cross regulation," 2017 IEEE Custom Integrated Circuits Conference (CICC), Austin, TX, 2017, pp. 1-4.

[42] Y. Jiang and A. Fayed, "A 1 A, Dual-Inductor 4-Output Buck Converter With 20 MHz/100 MHz Dual-Frequency Switching and Integrated Output Filters in 65 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 51, no. 10, pp. 2485-2500, Oct. 2016.

[43] M. Jung, S. Park, J. Bang and G. Cho, "An Error-Based Controlled Single-Inductor 10-Output DC-DC Buck Converter With High Efficiency Under Light Load Using Adaptive Pulse Modulation," in IEEE Journal of Solid-State Circuits, vol. 50, no. 12, pp. 2825-2838, Dec. 2015.

[44] D. Lu, Y. Qian and Z. Hong, "4.3 An 87%-peak-efficiency DVS-capable single-inductor 4-output DC-DC buck converter with ripple-based adaptive off-time control," 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, 2014, pp. 82-83.

[45] P. Assem, W. Liu, Y. Lei, P. K. Hanumolu and R. C. N. Pilawa-Podgurski, "Hybrid Dickson Switched-Capacitor Converter With Wide Conversion Ratio in 65-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 55, no. 9, pp. 2513-2528, Sept. 2020.

[46] J. Lee, Honnyong Cha, D. Shin, Kyoung-Jun Lee, D. Yoo, & J. Yoo (2013). JPE 13-3-2 Analysis and Design of Coupled Inductors for Two-Phase Interleaved DC-DC Converters.

[47] A. Ikriannikov and T. Schmid, "Magnetically coupled buck converters," 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, 2013, pp. 4948-4954.

[48] F. Hamzaoglu and M. R. Stan, "Split-path skewed (SPS) CMOS buffer for high performance and low power applications," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 48, no. 10, pp. 998-1002, Oct. 2001.

[49] Y. Moghe, T. Lehmann and T. Piessens, "Nanosecond Delay Floating High Voltage Level Shifters in a 0.35 μm HV-CMOS Technology," in IEEE Journal of Solid-State Circuits, vol. 46, no. 2, pp. 485-497, Feb. 2011.

[50] Y. Lei, W. C. Liu and R. C. N. Pilawa-Podgurski, "An analytical method to evaluate flying capacitor multilevel converters and hybrid switched-capacitor converters for large voltage conversion ratios," 2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL), Vancouver, BC, 2015, pp. 1-7.

[51] Y. Lei, R. May and R. Pilawa-Podgurski, "Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter," in IEEE Transactions on Power Electronics, vol. 31, no. 1, pp. 770-782, Jan. 2016.

[52] A. Sun, M. T. Tan and L. Siek, "Segmented Hybrid DPWM and tunable PID controller for digital DC-DC converters," 2010 International Symposium on Next Generation Electronics, Kaohsiung, 2010, pp. 154-157.

[53] N. Rahman, A. Parayandeh, Kun Wang and A. Prodic, "Multimode digital SMPS controller IC for low-power management," 2006 IEEE International Symposium on Circuits and Systems, Island of Kos, 2006, pp. 4 pp.-.

[54] B. J. Patella, A. Prodic, A. Zirger and D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters," in IEEE Transactions on Power Electronics, vol. 18, no. 1, pp. 438-446, Jan. 2003.

[55] S. Yuwono, S. Han, G. Yoon, H. Cho and S. Lee, "Development of low-complexity all-digital frequency locked loop as 500 MHz reference clock generator for field-programmable gate array," in IET Circuits, Devices & Systems, vol. 8, no. 2, pp. 73-81, March 2014.

[56] C. Schaef, E. Din and J. T. Stauth, "A Hybrid Switched-Capacitor Battery Management IC With Embedded Diagnostics for Series-Stacked Li–Ion Arrays," in IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3142-3154, Dec. 2017.

[57] Z. Ye, Y. Lei and R. C. N. Pilawa-Podgurski, "The Cascaded Resonant Converter: A Hybrid Switched-Capacitor Topology With High Power Density and Efficiency," in IEEE Transactions on Power Electronics, vol. 35, no. 5, pp. 4946-4958, May 2020.

[58] Y. Lei, W. Liu and R. C. N. Pilawa-Podgurski, "An Analytical Method to Evaluate and Design Hybrid Switched-Capacitor and Multilevel Converters," in IEEE Transactions on Power Electronics, vol. 33, no. 3, pp. 2227-2240, March 2018.

[59] Z. Ye, S. R. Sanders and R. C. N. Pilawa-Podgurski, "Modeling and Comparison of Passive Component Volume of Hybrid Resonant Switched-Capacitor Converters," 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), Toronto, ON, Canada, 2019, pp.

[60] Z. Ye, R. A. Abramson, Y. -L. Syu and R. C. N. Pilawa-Podgurski, "MLB-PoL: A High Performance Hybrid Converter for Direct 48 V to Point-of-Load Applications," 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL), Aalborg, Denmark, 2020, pp.

[61] Analog Devices, "Hybrid Step-Down Synchronous Controller" LTC7821 datasheet, April. 2018.

[62] Analog Devices, “Low Emission, Isolated DC-to-DC Converters” ADuM5028 datasheet, June. 2018.

[63] Silicon Labs, “4 Amp ISOdriver with High Transient (dV/dt) Immunity” Si8271 datasheet, September. 2020.

[64] J. Wittmann, A. Barner, T. Rosahl and B. Wicht, ”An 18 V Input 10 MHz Buck Converter With 125 ps Mixed-Signal Dead Time Control,” in IEEE Journal of Solid-State Circuits, vol. 51, no. 7, pp. 1705-1715, July. 2016.

[65] M. Choi and D. Jeong, ”18.6 A 92.8%-Peak-Efficiency 60A 48V-to-1V 3-Level Half-Bridge DC-DC Converter with Balanced Voltage on a Flying Capacitor,” 2020 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 296-298.

[66] Q. Cheng, L. Cong and H. Lee, ”11.4 A 48-to-80V Input 2MHz Adaptive ZVT-Assisted GaN-Based Bus Converter Achieving 14% Light-Load Efficiency Improvement,” 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 196-198.

[67] J. Xue, M. K. Song, X. Ke, M. Chen and L. Shtargot, ”8.7 A 2MHz 4-to-60VIN Buck-Boost Converter for Automotive Use Achieving 95% Efficiency and CISPR 25 Class 5 Standard,” 2019 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019, pp. 158-160.

[68] Z. Ye, Y. Lei, Z. Liao and R. C. N. Pilawa-Podgurski, ”Investigation of capacitor voltage balancing in practical implementations of flying capacitor multilevel converters,” 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL), Stanford, CA, 2017, pp. 1-7.

[69] Z. Ye, Y. Lei, W. Liu, P. S. Shenoy and R. . Pilawa-Podgurski, ”Improved Bootstrap Methods for Powering Floating Gate Drivers of Flying Capacitor Multilevel Converters and Hybrid Switched-Capacitor Converters,” in IEEE Transactions on Power Electronics, vol. 35, no. 6, pp. 5965-5977, June 2020.

[70] EPC, “Enhancement-Mode GaN Power Transistor Half-Bridge with Integrated Synchronous Bootstrap” EPC2108 datasheet, August. 2018.

[71] Texas Instruments, “5A, 100V Half-Bridge Gate Driver for Enhancement Mode GaN FETs” LM5113 datasheet, April. 2013.

[72] Y. Li, X. Lyu, D. Cao, S. Jiang and C. Nan, ”A 98.55% Efficiency Switched-Tank Converter for Data Center Application,” in IEEE Transactions on Industry Applications, vol. 54, no. 6, pp. 6205-6222, Nov.-Dec. 2018.