# Modeling EOL Degradation for NBTI Reliability of Low EOT Negative Capacitance p-SOI MOSFETs

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Acknowledgement

I would like to thank my family and friends for giving me the mental and emotional support to make my time in the Fifth Year M.S. Program productive and enjoyable. I want to thank Professor Sayeef Salahuddin for giving me the opportunity to do work on truly promising negative capacitance MOSFETs. Finally, I thank Nirmaan Shanker and Chirag Garg, PhD students from Professor Salahuddin's group, for giving me direction and technical guidance throughout the process of creating my thesis.

# Modeling EOL Degradation for NBTI Reliability of Low EOT Negative Capacitance p-SOI MOSFETs

Neeraj Avinash Shenoy

**Research Project**

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

Approval for the Report and Comprehensive Examination:

**Committee**

Professor Sayeef Salahuddin
Research Advisor

5.12.2023

(Date)

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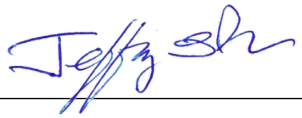

Professor Jeffrey Bokor
Second Reader

May 12, 2023

(Date)

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by

Neeraj Avinash Shenoy

A thesis submitted in partial satisfaction of the

requirements for the degree of

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in

Electrical Engineering and Computer Sciences

in the

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of the

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Committee in charge:

Professor Sayeef Salahuddin, Chair
Professor Jeffrey Bokor

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Modeling EOL Degradation for NBTI Reliability of Low EOT Negative Capacitance p-SOI MOSFETs

Abstract

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University of California, Berkeley

Professor Sayeef Salahuddin, Chair

Bias temperature instability (BTI) has become an increasingly pressing degradation mechanism due to its impact on the reliability of metal-oxide-semiconductor field-effect transistors (MOSFETs). BTI results in a gradual shift of MOSFET characteristics, such as threshold voltage ($V_T$), over time. We are interested in the reliability of p-type silicon-on-insulator (SOI) MOSFETs ($L_g = 90$ nm) incorporating a 1.8 nm $HfO_2$-$ZrO_2$ superlattice (HZH) gate stack. This gate stack exhibits an effective oxide thickness of 7.5 Å due to negative capacitance (NC) effects. In this paper, we estimate the end-of-life (EOL) degradation of threshold voltage ($\Delta V_T$) of low EOT NC p-SOI MOSFETs using a negative bias temperature instability (NBTI) physical model. The model is created based on experimental data of stress time ($t_{STR}$) and $\Delta V_T$ of p-SOI MOSFETs under constant temperature ($T = 85°C$) and varying overdrive voltage ($V_{OV}$) conditions. We find $\Delta V_{IT}$, the interface trap contribution, is the major contributor to the overall $\Delta V_T$, while $\Delta V_{HT}$ and $\Delta V_{OT}$, the hole trapping and bulk trap generation contributions, are negligible. So, we extrapolate the $\Delta V_{IT}$ physical model out to $t_{STR} = 10$ years $\approx 3 * 10^8$ seconds and find estimates for degradation of $\Delta V_T$ at EOL. We now have a better sense of the reliability of NC p-SOI MOSFETs under constant $T$ and varying $V_{OV}$ conditions.

To everyone who can believe in themselves and trust the process.

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## Acknowledgments

I would like to thank my family and friends for giving me the mental and emotional support to make my time in the Fifth Year M.S. Program productive and enjoyable. I want to thank Professor Sayeef Salahuddin for giving me the opportunity to do work on truly promising negative capacitance MOSFETs. Finally, I thank Nirmaan Shanker and Chirag Garg, PhD students from Professor Salahuddin's group, for giving me direction and technical guidance throughout the process of creating my thesis.

# Chapter 1

# Introduction

## 1.1 Background

As integrated circuits (ICs) become smaller and more complex, the reliability of these devices becomes increasingly important. Bias temperature instability (BTI) is a degradation mechanism that has gained attention in recent years due to its potential impact on the reliability of MOSFETs.

BTI results in a gradual shift in MOSFET characteristics, such as threshold voltage ($V_T$), transconductance ($g_m$), subthreshold slope ($S$), linear and saturation drain current ($I_{DLIN}$ and $I_{DSAT}$), etc., over time. Hence, this degrades the performance of digital, memory, and analog CMOS circuits [4].

Positive bias temperature instability (PBTI) occurs when the MOSFET is subjected to a positive bias voltage and elevated temperatures. PBTI degradation can lead to an increase in the threshold voltage of the MOSFET over time, negatively affecting the device's performance and reliability. This reliability issue is typically analyzed in n-type MOSFETs.

Negative bias temperature instability (NBTI) occurs in MOSFETs when the transistor is subjected to a negative bias voltage and elevated temperatures, reducing the threshold voltage of the MOSFET over time. This reliability issue is typically analyzed in p-type MOSFETs. This shift in operating characteristics, much like PBTI, can result in increased power consumption, reduced performance, and ultimately, device failure. The shift towards smaller process nodes in IC manufacturing has led to the use of thinner gate oxides in MOSFETs, which are more susceptible to NBTI [5].

## 1.2 Motivation

The importance of NBTI and PBTI reliability has increased due to several factors. These include the shift towards smaller process nodes, increased power consumption, and the growing demand for reliable ICs in critical applications such as automotive, aerospace, and medical

devices. Accurate lifetime predictions for both NBTI and PBTI are necessary to ensure the devices meet the required reliability standards.

End-of-life (EOL) projections, particularly threshold voltage shift ($\Delta V_T$) versus stress time ($t_{STR}$) projections, have become crucial in assessing the reliability of MOSFETs. Accurate lifetime predictions are necessary for ensuring the performance and safety of MOSFETs in a wide range of applications, including automotive, aerospace, and medical devices.

In summary, NBTI and PBTI reliability are becoming increasingly important due to the shift towards smaller process nodes, increased power consumption, and the demand for reliable ICs in critical applications. Accurate EOL predictions for NBTI and PBTI are necessary to ensure the devices meet the required reliability standards. In this thesis, we will create physical models for $\Delta V_T$ of negative capacitance (NC) MOSFETs.

## 1.3 Thesis Organization

This thesis is organized into Introduction, Theory, Methodology, Results, and Conclusion sections. The Introduction is meant to provide a background into key reliability concerns of MOSFETs and underscore the need to model EOL degradation. The Theory will explain the device structure, key terms, and models. The Methodology is meant to explain how the modeling is conducted. The Results will show the outcomes of the models. Finally, the Conclusion will provide key takeaways, the importance of the outcomes, and a discussion on future work.

# Chapter 2

# Theory

## 2.1 Device Structure

We seek to create EOL models for $L_g = 90$ nm p-SOI MOSFETs incorporating a ferroelectric-antiferroelectric (FE-AFE) 1.8 nm $HfO_2$-$ZrO_2$ superlattice (HZH) gate stack (**Figure 2.1**). The integrated gate oxides show an effective oxide thickness (EOT) of 7.5 Å on p-SOI MOSFETs due to the NC effect [8].

## 2.2 Key Terms

In this section, we define some key terms.

$$|V_{OV}| = |V_G| - |V_T| \tag{2.1}$$

We denote the overdrive voltage as $V_{OV}$. In **Equation 2.1**, notice absolute value signs are used, as $V_G$ and $V_T$ are both negative values for p-type MOSFETs.

The stress time $t_{STR}$ indicates the period of time under which the device is being stressed. During the stress period, the gate of the device is subjected to a stress voltage $V_{GSTR}$. These terms will become relevant when discussing the measurement scheme for the experimental data in the Methodology section.

The voltage acceleration factor ($\Gamma$) and activation energy ($E_A$) are, for the sake of our discussion, parameters we will be extracting from our models. Variations of $\Gamma$ will be extracted based on the type of physical model being created.

$$\Delta V_T = \Delta V_{IT} + \Delta V_{HT} + \Delta V_{OT} \tag{2.2}$$

There are three uncorrelated subcomponents to the overall $\Delta V_T$ that are recognized [6]. These include the interface trap contribution ($\Delta V_{IT}$), hole trapping contribution ($\Delta V_{HT}$), and bulk trap generation contribution ($\Delta V_{OT}$) (**Equation 2.2**). The interface trap contribution is thought to contribute most to the overall $\Delta V_T$, while the hole trapping contribution is

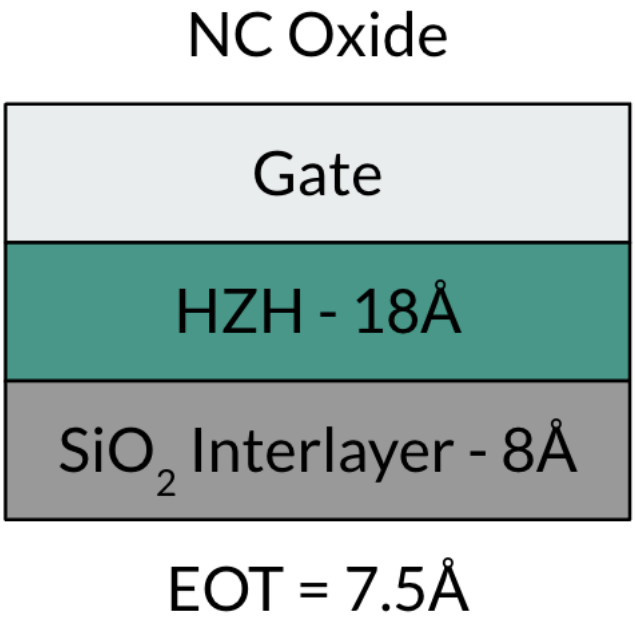


Figure 2.1: Cross Section of Negative Capacitance MOSFET

minimal. The bulk trap generation contribution should be negligible due to the low capture cross-section of bulk traps in low EOT devices [5].

## 2.3 Models

We will create an empirical model for $\Delta V_T$ and physical models for $\Delta V_{IT}$, $\Delta V_{HT}$, $\Delta V_{OT}$. If we can show through the model fits that $\Delta V_{IT}$ is the dominant contributor to the overall $\Delta V_T$, and $\Delta V_{HT} + \Delta V_{OT}$ is negligible, then we can extrapolate the $\Delta V_{IT}$ physical model to EOL ($t_{STR} = 10$ years). We can show $\Delta V_{IT}$ is the dominant contributor by calculating averaged ratios $\frac{\Delta V_{IT}}{\Delta V_T}$ across $V_{OV}$ based on the respective threshold voltage shift values. It should be noted we cannot extrapolate the overall $\Delta V_T$ model to EOL, as it is empirical in nature and thus is not valid for stress times outside the experimental data range.

# Chapter 3

# Methodology

This chapter outlines the methodology to create the physical models and how we can extrapolate EOL information.

## 3.1 Experimental Data

Preliminary experimental data on NC p-SOI MOSFETs has been gathered [8] under constant temperature ($T = 85°C$) and varying overdrive voltage ($V_{OV}$) conditions.

An ultrafast measure-stress-measure scheme has been used to gather this data [9], as displayed in **Figure 3.1**. A stress voltage $V_{GSTR}$ is applied to the gate of the MOSFET for a stress time $t_{STR}$. Then, the measurement of $\Delta V_T$ is performed in the period immediately following each stress period.

## 3.2 $\Delta V_T$ Empirical Model

The empirical model for $\Delta V_T$ [5] is shown in **Figure 3.2**.

$A$, $\Gamma_V$, $E_A$, $n$ are variable parameters across devices.

## 3.3 $\Delta V_{IT}$ Physical Model

The physical model for $\Delta V_{IT}$ [2] is shown in **Figure 3.3**.

$A$, $\Gamma_{IT}$ are variable parameters across devices.

## 3.4 $\Delta V_{HT}$ Physical Model

The physical model for $\Delta V_{HT}$ [2] is shown in **Figure 3.4**.

$B$, $\Gamma_{HT}$ are variable parameters across devices.

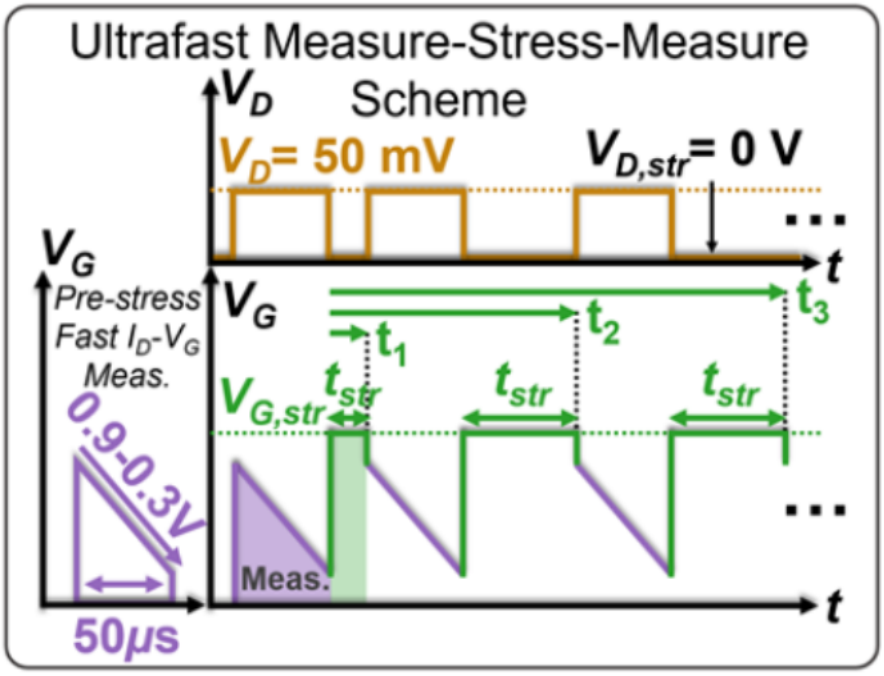


Figure 3.1: Ultrafast Measure-Stress-Measure Scheme for Experimental Data

$$\Delta V_T = A * e^{\Gamma_V * V_{GSTR}} * e^{-\left(E_A/kT\right)} * t^n$$

Figure 3.2: Empirical Model

$$\Delta V_{IT} = \frac{q}{C_{ox}}(A(V_{ov} - \Delta V_T)^{\Gamma_{IT}} e^{\frac{-E_{AIT}}{kT}} t^{\frac{1}{6}})$$

$$where\ E_{AIT} = (\frac{2}{3}(E_{Akf} - E_{Akr}) + \frac{E_{ADH2}}{6})$$

Figure 3.3: Interface Trap Model

$$\Delta V_{HT} = \frac{q}{C_{ox}}(B(V_{ov} - \Delta V_T)^{\Gamma_{HT}} e^{\frac{-E_{AHT}}{kT}})$$

Figure 3.4: Hole Trapping Model

## 3.5 $\Delta V_{OT}$ Physical Model

The physical model for $\Delta V_{OT}$ [2] is shown in **Figure 3.5**.

$C$ is a variable parameter across devices.

$$\Delta V_{HT} = \frac{q}{C_{ox}}(C(1 - e^{(-(\frac{t}{n})^{\beta_{OT}})}))$$

$$where\ n = \eta(V_{ov} - \Delta V_T)^{-\frac{\Gamma_{OT}}{\beta_{OT}}} e^{\frac{E_{AOT}}{kT\beta_{OT}}}$$

Figure 3.5: Bulk Trap Generation Model

## 3.6 Fixed Parameters for Physical Models

A table of fixed parameter values has been provided. This table is valid for the three aforementioned physical models for the subcomponents of $\Delta V_T$.

| **Fixed Parameters (constant across devices)** | | |
|---|---|---|
| $E_{Akf}$ = 0.175eV | $E_{Akr}$ = 0.2eV | $E_{ADH2}$ = 0.6eV |
| $E_{AHT}$ = 0.03eV | $E_{AOT}$ = 0.15eV | $\beta_{OT}$=0.36eV |
| $\Gamma_{OT}$ = 9 | $\eta$ = 5x$10^{12}$ | |

Figure 3.6: Fixed Parameters for Subcomponents of $\Delta V_T$

# Chapter 4

# Results

## 4.1 $\Delta V_T$ Empirical Model

The empirical model for $\Delta V_T$ fits the experimental data very well with a normalized root mean square error (RMSE) of $\sim 10^{-4}$.

A plot of the extracted time exponent parameter $n$ (**Figure 4.1**) from the power law portion of the empirical model shows an average value of around $n = .152 \approx 1/6$. Thus, our extracted time parameter is close to the ideal value, as mentioned in the literature [3].

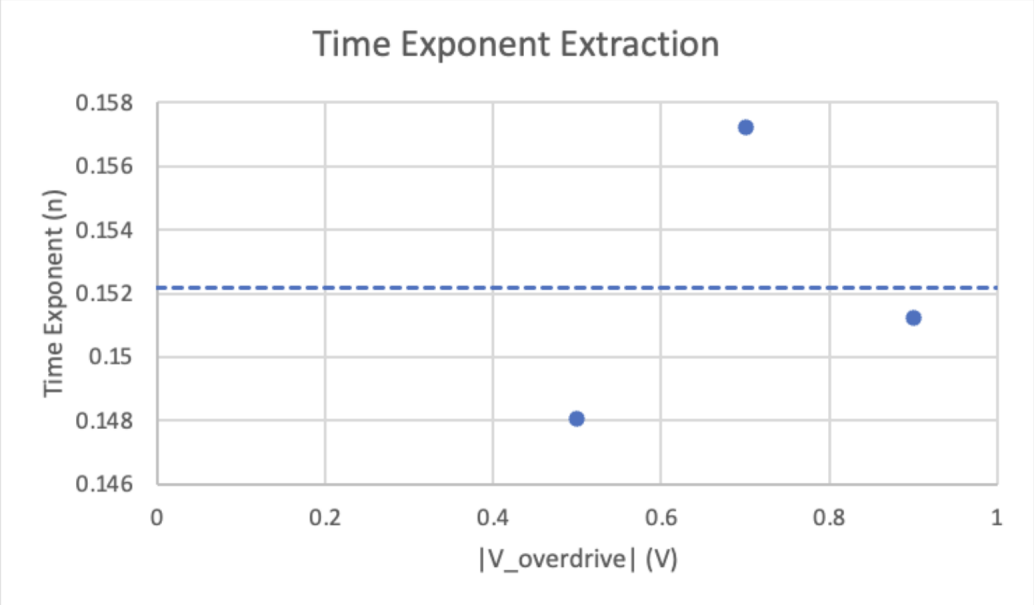


Figure 4.1: Time Exponent Extraction from Empirical Model

The following three plots (**Figures 4.2, 4.3, 4.4**) show the fit of the empirical model

alongside the experimental data. To reiterate, this model cannot be extrapolated to high $t_{STR}$ due to its empirical nature.

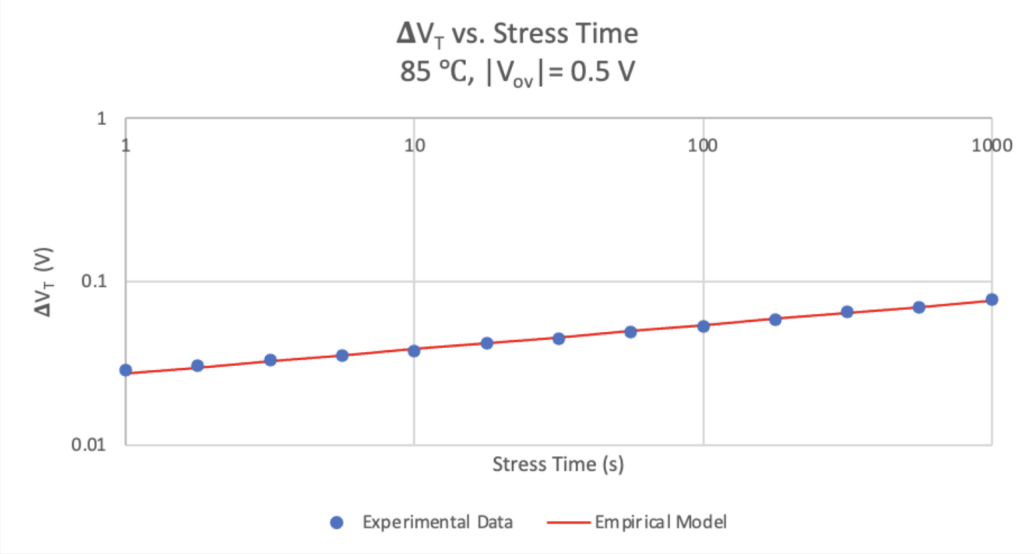


Figure 4.2: Empirical Model Fit for $T = 85°C$, $|V_{OV}| = 0.5$ V

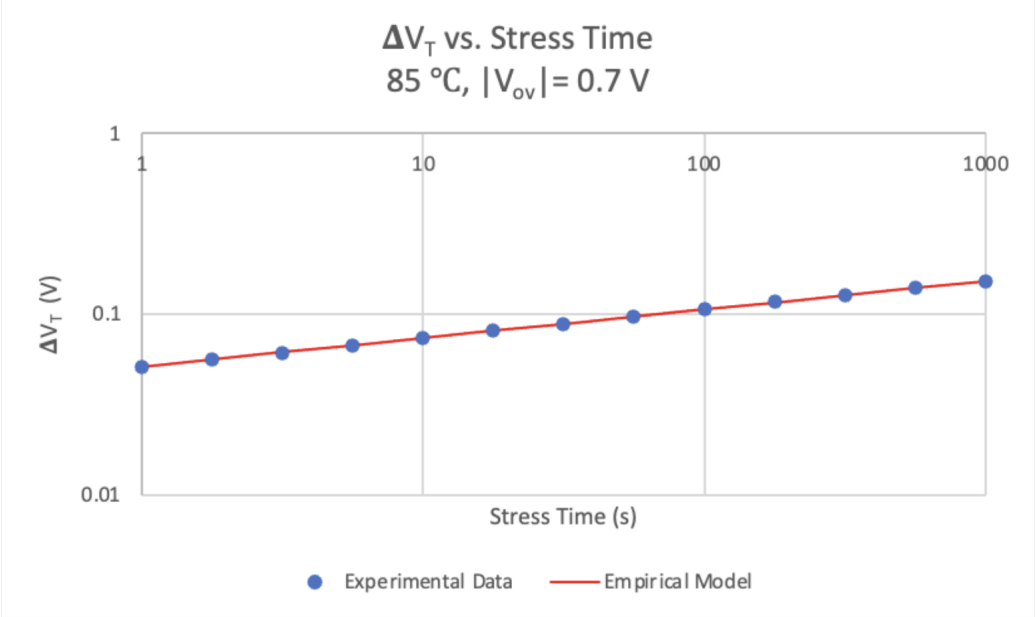


Figure 4.3: Empirical Model Fit for $T = 85°C$, $|V_{OV}| = 0.7$ V

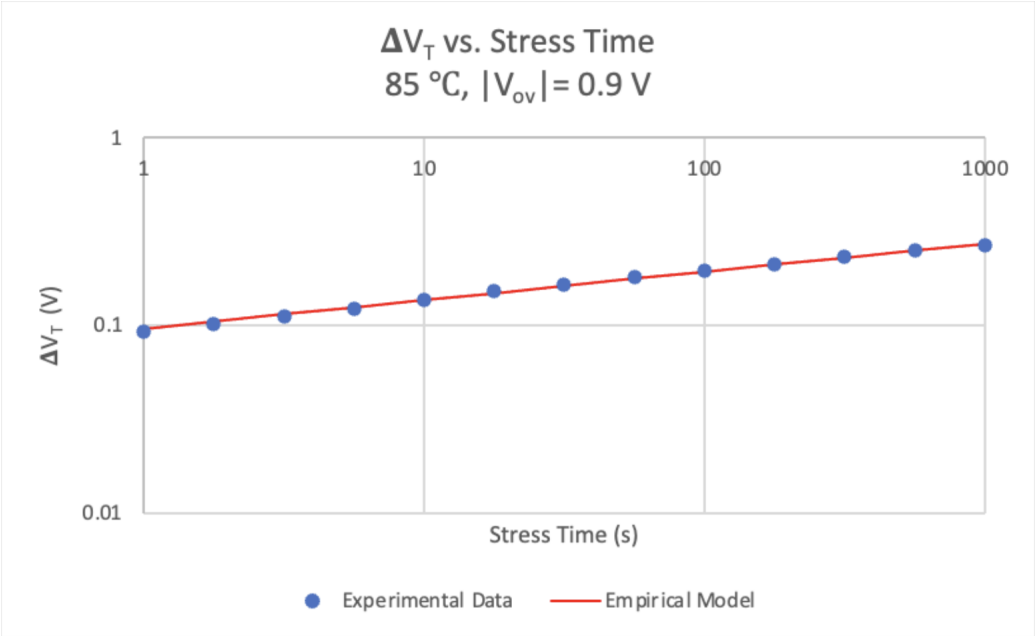


Figure 4.4: Empirical Model Fit for $T = 85°C$, $|V_{OV}| = 0.9$ V

## 4.2 $\Delta V_{IT}$ Physical Model

The physical model for $\Delta V_{IT}$ fits the experimental data very well with a normalized root mean square error (RMSE) of $\sim 10^{-4}$.

Plots of the interface trap model fit are shown (**Figures 4.5, 4.6, 4.7**).

**Table 4.1** shows the averaged values for $\frac{\Delta V_{IT}}{\Delta V_T}$ across $V_{OV}$. Based on these ratio values, $\Delta V_{IT}$ seems to be a dominant contribution to the overall $\Delta V_T$, comprising more than 99% of the overall threshold voltage shift across all $V_{OV}$.

| | $T = 85°C$, $\lvert V_{OV}\rvert = 0.5$ V | $T = 85°C$, $\lvert V_{OV}\rvert = 0.7$ V | $T = 85°C$, $\lvert V_{OV}\rvert = 0.9$ V |
|---|---|---|---|
| Average $\frac{\Delta V_{IT}}{\Delta V_T}$ | 0.995867685 | 0.999541055 | 1.000114274 |

Table 4.1: Average $\frac{\Delta V_{IT}}{\Delta V_T}$ Values for Varying $V_{OV}$

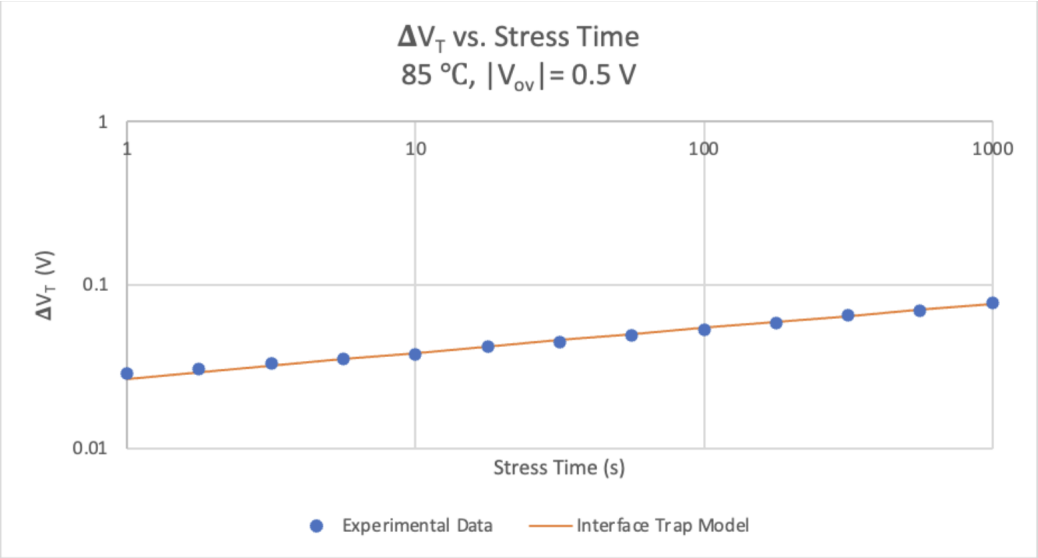


Figure 4.5: Interface Trap Model Fit for $T = 85°C$, $|V_{OV}| = 0.5$ V

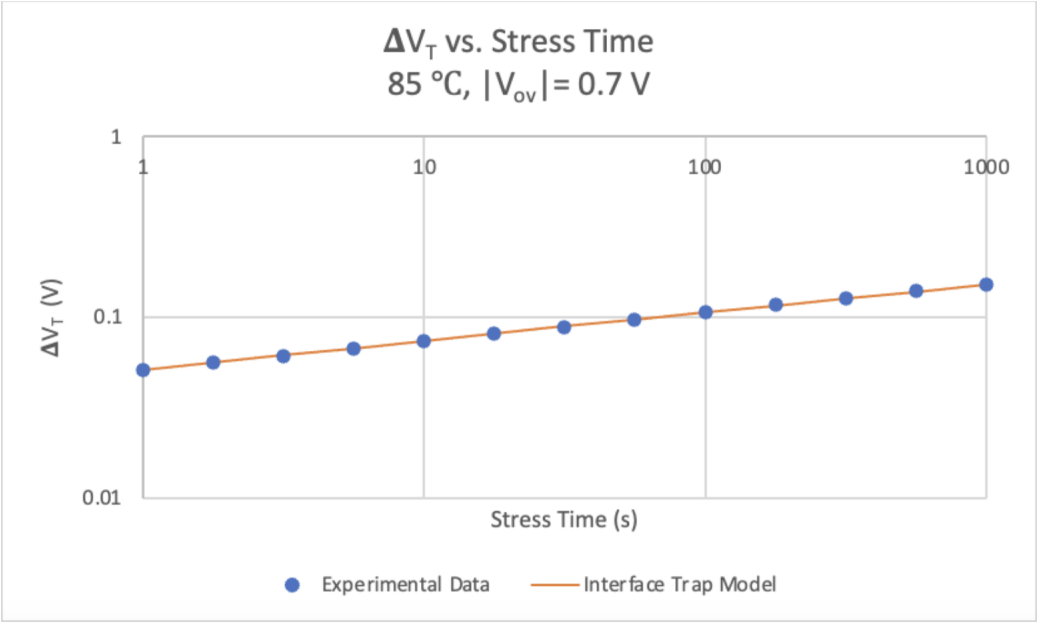


Figure 4.6: Interface Trap Model Fit for $T = 85°C$, $|V_{OV}| = 0.7$ V

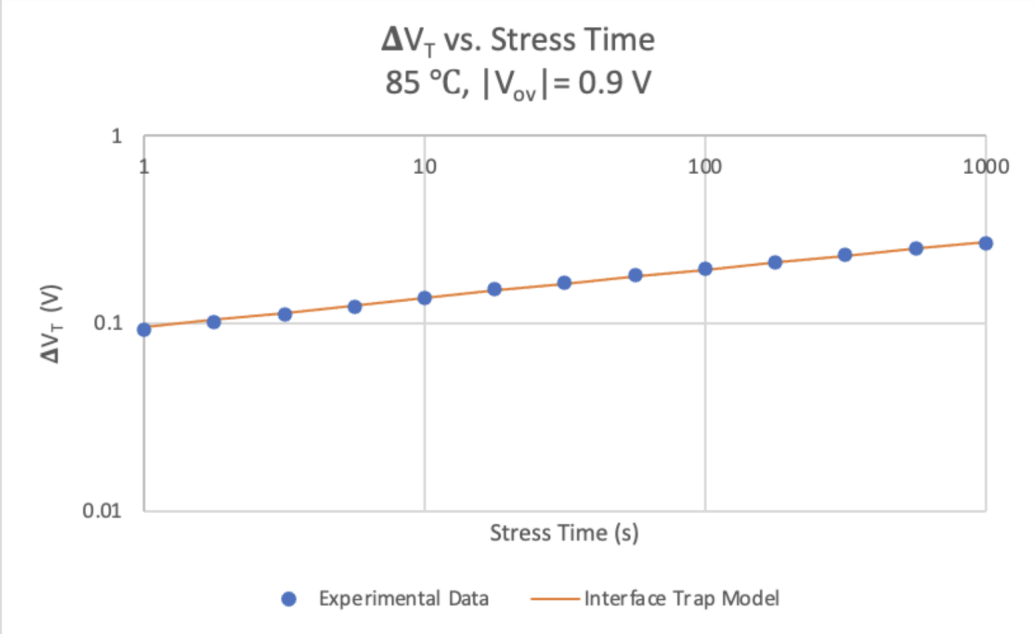


Figure 4.7: Interface Trap Model Fit for $T = 85°C$, $|V_{OV}| = 0.9$ V

## 4.3 $\Delta V_{HT} + \Delta V_{OT}$ Physical Models

The physical model for $\Delta V_{HT}$ fits the experimental data moderately well with a normalized root mean square error (RMSE) of $\sim 10^{-3}$, and the physical model for $\Delta V_{OT}$ fits the experimental data poorly with a normalized root mean square error (RMSE) of $\sim 10^{-1}$.

All $\Delta V_{OT}$ values from its physical model are essentially equal to zero. Additionally, all $\Delta V_{HT}$ values from its physical model are far less than those from the $\Delta V_{IT}$ physical model. For these reasons, plots for the model fit of the hole trapping and bulk trap generation models have not been included, as $\Delta V_{HT} + \Delta V_{OT}$ is a negligible contribution to $\Delta V_T$.

## 4.4 Extrapolation of $\Delta V_{IT}$ Physical Model to EOL

After showing $\Delta V_{IT}$ is a dominant contribution to the overall $\Delta V_T$, and $\Delta V_{HT} + \Delta V_{OT}$ is a negligible contribution to $\Delta V_T$, we can now extrapolate the physical model for interface trap out to EOL (**Figures 4.8, 4.9, 4.10**). We extend the model to $t_{STR} = 10$ years $\approx 3 * 10^8$ seconds and record the resultant $\Delta V_T$ values (**Table 4.2**). These values represent the EOL degradation of p-SOI MOSFETs at constant $T = 85°C$ and varying $V_{OV}$.

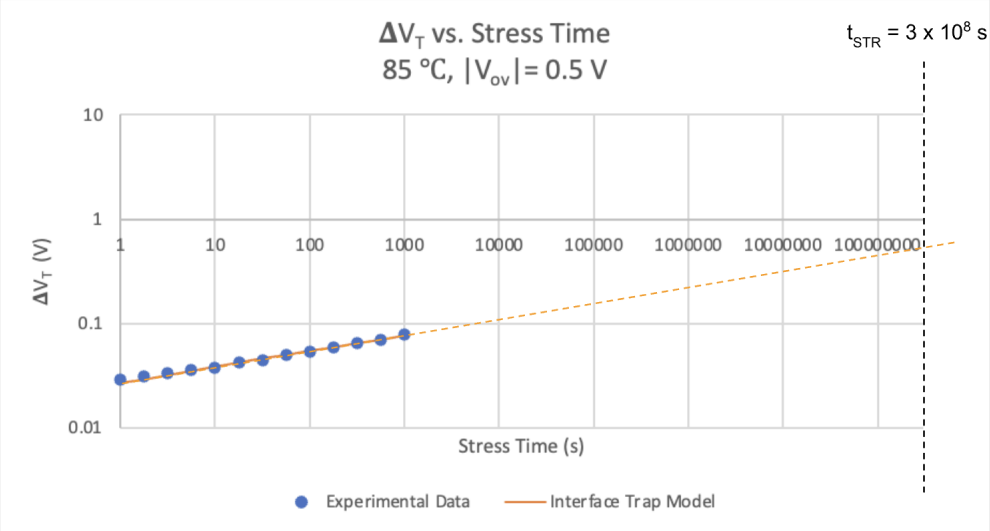


Figure 4.8: EOL Estimation for $T = 85°C$, $|V_{OV}| = 0.5$ V

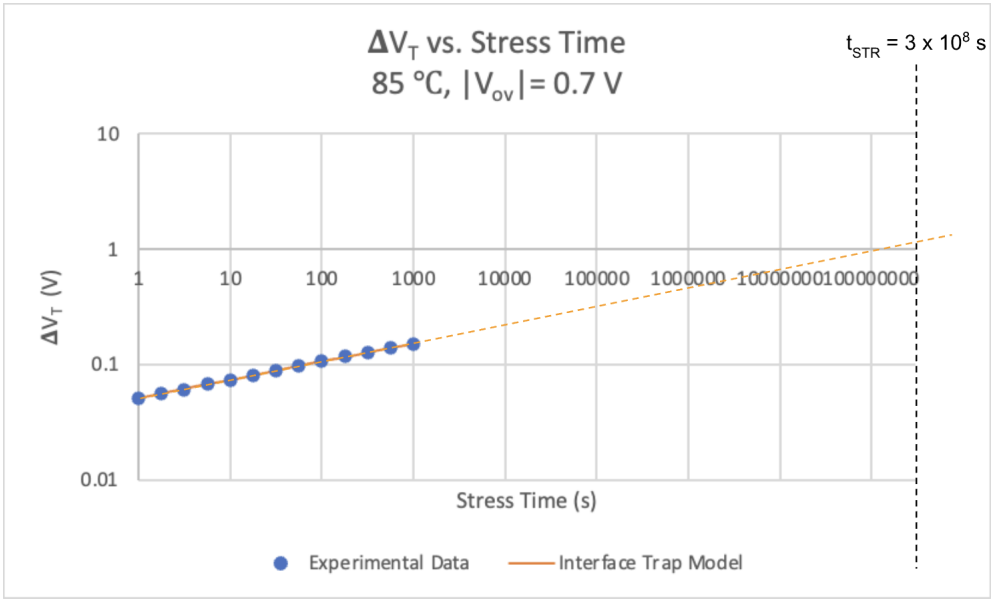


Figure 4.9: EOL Estimation for $T = 85°C$, $|V_{OV}| = 0.7$ V

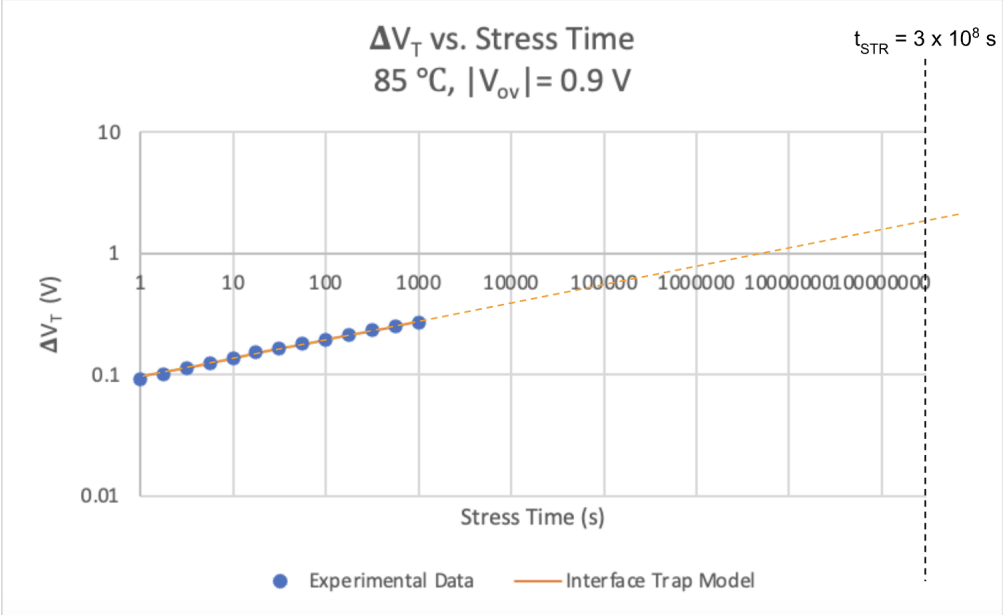


Figure 4.10: EOL Estimation for $T = 85°C$, $|V_{OV}| = 0.9$ V

| | $T = 85°C$, $\|V_{OV}\| = 0.5$ V | $T = 85°C$, $\|V_{OV}\| = 0.7$ V | $T = 85°C$, $\|V_{OV}\| = 0.9$ V |
|---|---|---|---|
| $\Delta V_T$ (V) at EOL | 0.494380291 | 1.107428888 | 1.843464689 |

Table 4.2: $\Delta V_T$ (V) at $t_{STR} = 10$ years

# Chapter 5

# Conclusion

## 5.1 Main Takeaways

Regarding the model fits, the empirical model for $\Delta V_T$ fits very well with the experimental data. The physical model for $\Delta V_{IT}$ has a similarly great fit. The physical model fits for $\Delta V_{HT}$ and $\Delta V_{OT}$ are noticeably lesser, most likely reflecting how each of these contributors is very minor to the overall $\Delta V_T$.

$\Delta V_T$ is almost entirely accounted for by $\Delta V_{IT}$, whereas $\Delta V_{HT}$ and $\Delta V_{OT}$ are very minor contributors. So, $\Delta V_T$ at high $t_{STR}$ is able to be approximated by an extrapolation of the physical model for the interface trap contribution.

Extrapolating the physical model for $\Delta V_{IT}$ out to $t_{STR} = 10$ years, we find estimates for the EOL degradation at constant temperature ($T = 85$°C) and varying $|V_{OV}| = \{0.5, 0.7, 0.9\}$ V.

## 5.2 Importance

This work is important since we now know the EOL degradation of $\Delta V_T$ of NC p-SOI MOSFETs at constant temperature ($T = 85$°C), varying $V_{OV}$ for $t_{STR} = 10$ years, which is a standard benchmark for EOL [1]. So, we now have a better sense of the reliability of these NC p-SOI MOSFETs.

## 5.3 Future Work

Comphy models, or "compact-physics" models, for NBTI seem promising for creating physical models for constant $V_{OV}$, varying temperature conditions. Models can be created for cryogenic temperatures, accounting for quantum mechanical effects, as well as for temperatures of up to at least 170°C [7].

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