Analog Generators for SerDes Clock Generation and Distribution

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by

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Abstract

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The ever-increasing demand for ultra-high-speed interconnects has driven the development of wireline transceivers operating at $> 100Gbps$ per lane. As a major contribution of data random jitter, clock-dependant distortion of transmitters and receivers, the clock generation and distribution circuits in SerDes becomes increasingly complex and time-consuming with stringent specifications, especially considering the fast development of technology nodes of the FinFET processes. This thesis focuses on the design of energy-efficient clock generation and distribution network with generator-based design methodology using Berkeley Analog Generator, which speeds up the design procedure, while satisfying the performance requirements.

A bang-bang phase-locked loop generator for $28/32Gbps$ SerDes that encapsulates this design methodologies for its circuit blocks and the complete PLL system is first reported. The generator is fully automated and parameterized, producing the layout and schematic based on process characterization and top-level specifications. Three 14GHz PLLs are instantiated in TSMC 16nm, GF 14nm and Intel 22nm technologies, demonstrating the process portability. The rapid generation time of less than four days enables fast PLL design and technology porting. The PLL design fabricated in TSMC 16nm shows RMS jitter of $565.4fs$ and power of $6.64mW$ from a $0.9V$ supply.

Furthermore, a flexible clock distribution network for a $200Gbps$ pulse amplitude modulation four-level transmitter is designed using the layout generators in 28nm CMOS technology. The proposed TX achieves an eye opening with $> 52.9mV$ eye height, $0.36UI$ eye width, 98% RLM and $4.63pJ/b$ at $200Gbps$ PAM-4 signaling under $> 6dB$ channel loss at $50GHz$, demonstrating the highest data rate achieved using a planar process.

To complete the whole TX design, a layout generator for sub-100fs sub-sampling PLL is proposed. With a type-I loop and tri-state integral path, the voltage ripples of the hybrid

loop is eliminated and the PLL reaches a RMS jitter of $44fs$ at $28GHz$ output, a spur of $-56.6dB$, which results in the FOM value $-254.8dB$. Finally, the PLL is merged with the transmitter data path, achieving 4.69 pJ/bit efficiency, $54mV$ eye height, $0.27UI$ eye width, and 97% RLM under $6dB$ channel loss at $50GHz$, showing the capability of the generator-based design methodology.

To Yajuan and my family

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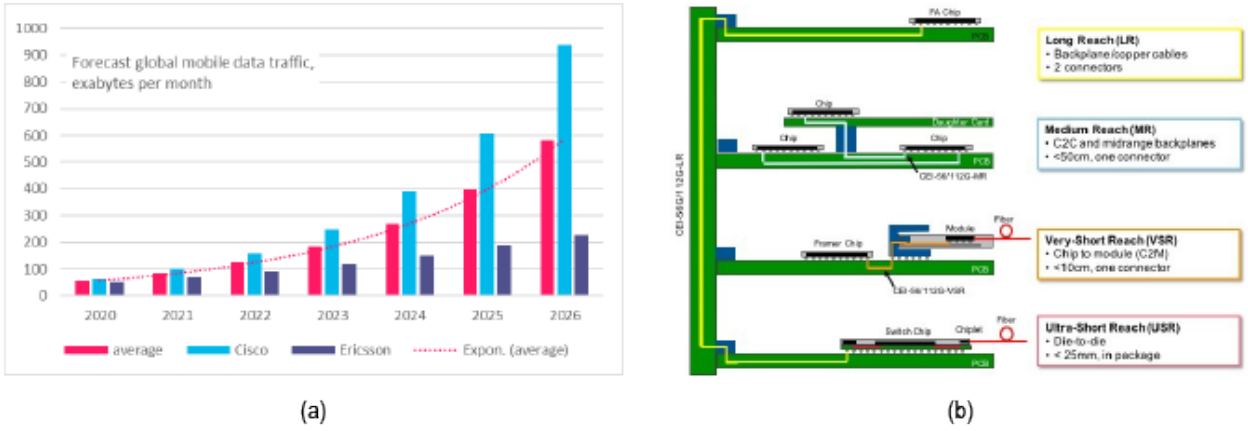
Chapter 1

Introduction

1.1 Motivation

The continue global increase mobile data usage [1] requires the data system to communicate faster and more efficiently (Figure 1.1(a)). SerDes and wireline communication form the critical backbone of modern communications systems. For example, in data centers, the serial interfaces between chips and systems require communication of various forms [2], within packages or backplanes, from the backplane to the top of the rack router, from rack to rack, and long-haul out of the datacenter across the country or the world (Figure 1.1(b))..



(a) (b)

Figure 1.1: (a) Comparison of global mobile data traffic forecasts [1] and (b) different forms of serial interfaces in data centers [2].

So far, the data rate of the ultra-high-speed wireline IOs doubles every 3-4 years and the development of wireline transceiver exceeding $> 200Gb/s$ [1], [2] has become the next goal [5], [6], [7],[8],[9],[10],[11],[12]. For example, PCIe data rates (Fig. 1.2(a)) have doubled every 3 years, and the 2022 PCIe standard is aiming to achieve 128Gb/s per pin and >256

Gb/s total bandwidth [3]. Fig. 1.2(b) also shows that per-lane Ethernet data rates [4] have doubled every 3.9 years, with standards targeting 200 Gb/s in 2026.

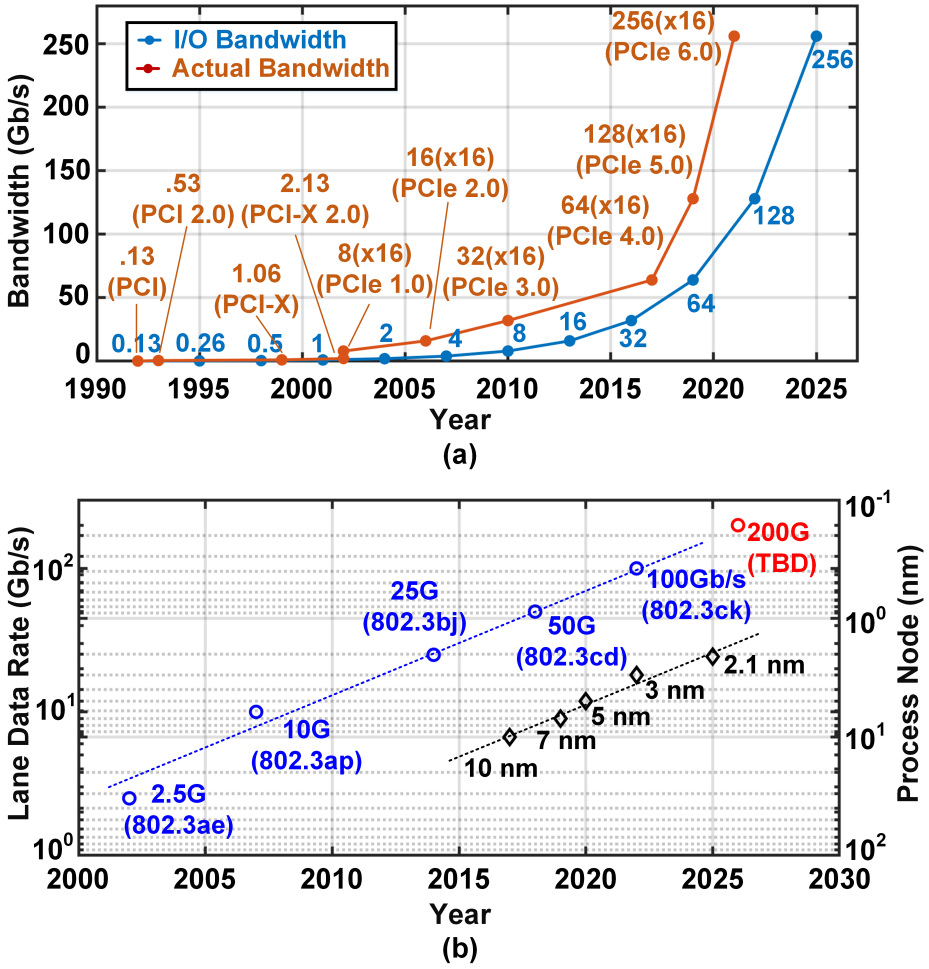


Figure 1.2: (a) I/O bandwidth (data rate per lane) and actual bandwidth (data rate of link) of the PCIe standard versus year [3] and (b) a summary forecast from the Ethernet Bandwidth Assessment [4].

In a wireline transceiver, the clock generation and distribution circuit plays a crucial role. As the clock non-ideality is a major contribution of data random jitter, transmitter duty cycle distortion, quadrature error. The jitter transfer, jitter generation and jitter tolerance specifications of the receiver also closely related to the clock and data recovery circuit. As the clock and data recovery shares very similar analysis/design method with PLL, this thesis will focus on phase locked loop and clock distribution at the transmitter side. Table 1.1 shows the performance of clock generation and distribution of the papers in recent years. We can get that 1) the RMS Jitter from PLL and clock distribution is around 0.01UIp-p of

the data rate, and 2) the percentage of its power is around $30-50\%$ of total transmitter power, which is also the guidelines of the designs in this thesis.

Table 1.1: Performance exploration of clock generation and distribution in SerDes TXs.

Paper	Technology	Data Rate	Modulation	Clock Jitter	Clock Power	% of Clk Power
JSSC'18 [13]	45nm	$80Gb/s$	PAM-4	$228fs$	$18.3mW$	41.5%
VLSI'18 [14]	16nm	$112Gb/s$	PAM-4	$130fs$	N/A	N/A
ISSCC'20 [12]	40nm	$100Gb/s$	PAM-4	External	$162.0mW$ (w/o PLL)	26.2%
JSSC'19 [5]	14nm	$128Gb/s$	PAM-4	External	$57.3mW$ (w/o PLL)	33.7%
JSSC'19 [6]	10nm	$112Gb/s$	PAM-4	$154fs$	$97.9mW$	50.8%
JSSC'16 [15]	16nm	$64Gb/s$	PAM-4	$150fs$	$115.0mW$	51.0%

As shown in Fig. 1.2(b) FinFET technologies below 16 nm have been widely used in high-speed links, since the transceivers used for System-on-Chip (SoC) interfaces follow process technology scaling necessitated by "digital-first" architectures. Fortunately, the FinFET process is superior in providing a higher cut-off frequency and intrinsic gain compared to planar processes. This enables the SerDes circuits to meet the demands of ultra-high-speed interconnects.

However, as new process technologies are applied, the SerDes circuit design becomes increasingly complex and time-consuming. The design rule explosion at advanced technology nodes and increased sensitivity to routing parasitics with smaller feature sizes require repetitive design iterations. Additionally, reliability issues such as electromigration and dynamic voltage drop further lengthen the circuit design cycle.

To address these concerns, the Berkeley Analog Generator (BAG) 2.0 framework [16] was introduced, to enable fast circuit designs using executable generators. The generators, built within a Python-based framework, can produce DRC- and LVS-clean schematics and layouts alongside verification test benches with parameterized specification files. In addition, the framework allows designers to codify their design procedure into design scripts, which enables schematic and layout generation, extraction, simulation, and resizing procedures into automatic design iteration loops, drastically reducing the design and validation time.

Figure 1.3 shows BAG structure [16] split into three levels. In core scripts, the generator framework provides interfaces between Python and commercial CAD tools (Virtuoso, Calibre, EMX, etc.). It also provides various functions to draw or modify layouts and schematics and utilizes a routing grid system with a track manager to set wire widths and spacing. With process-specific primitives and technology parameters, various layout templates are designed to generate DRC-clean analog CMOS, digital CMOS, resistor, MOM capacitor and inductor layouts.

By using generator templates and the track system, circuit designers develop process-independent schematic and layout generators and create DRC- and LVS-clean instances with parameters and sizes specific to a particular technology. At the top level, designers

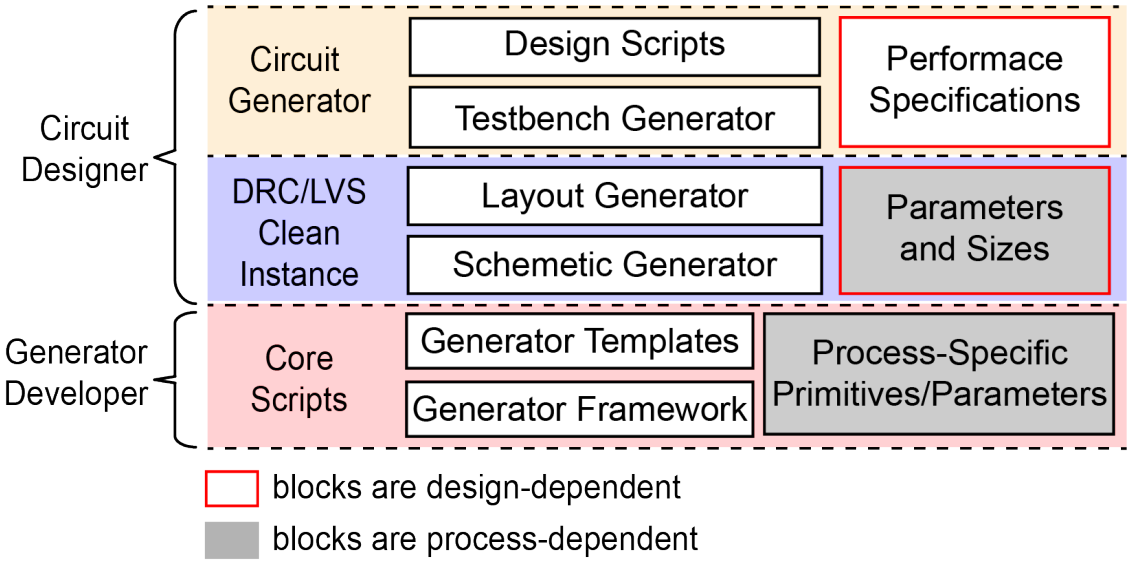


Figure 1.3: The hierarchy of Berkeley Analog Generator.

codify their design procedure into scripts that can generate test benches and alter design parameters to meet the target performance specifications. With the framework, designers can easily implement circuits and systems in a different technology merely by updating the process-specific primitives and parameters.

With the BAG framework, [17] and [18] demonstrate circuit design methodologies based on machine learning by converging circuit parameters to particular design specifications in a large design space using hundreds to thousands of simulations. While this procedure works effectively, the long convergence time limits both the size of the circuit and the number of design parameters. For this reason, the state-of-art ML-based design methodologies mainly focus on small-scale circuits, such as an operational amplifier and a simplified wireline receiver frontend. In designing large AMS circuits or systems, a traditional top-down or bottom-up design methodology is still preferred. By leveraging the experience of circuit designers, the number of iterations and the run time of the design script are drastically reduced.

In this thesis, we explore three topics to show the circuit designs with generator concept: 1) a bang-bang phase-locked loop (BBPLL) generator for 28/32Gbps SerDes, 2) a clock distribution circuit for 200Gbps PAM-4 transmitter, and 3) a 25GHz sub-100 fs sub-sampling PLL for 200Gbps transmitter and the whole 200Gbps transmitter with the PLL.

1.2 Thesis Organization

In Chapter 2, a phase-locked loop (PLL) generator is proposed based on BAG using top-down and bottom-up approaches. The proposed PLL generator automatically produces a top-level

schematic and layout of a PLL whose circuit parameters satisfy a target performance specification. The proposed generator is process-portable and proven in three different technology nodes from three different foundries. The total generation time took less than four days, showing that the proposed PLL generator enables fast PLL circuit design and technology portability. The simulated and measured performance of the generated PLL is comparable to one that is manually designed.

Chapter 3 discussed the clock distribution network for 200Gbps SerDes transmitter, with flexible timing control maximizes the timing margin between clock domains. The 200 *Gbps* transmitter is tested to verify the performance of the clock distribution circuit. In Chapter 4, the sub-100fs hybrid PLL for 200Gbps PAM-4 SerDes transmitter is discussed. This chaper begin with the PLL requirements and specifications, and then proceeds to the architecture of the tri-state type-I sub-sampling PLL. The circuits design and system simulation of the PLL are included as well. Chapter 5 shows the measurement setup and test results of the sub-100fs PLL.

In Chapter 6, the whole 200Gbps PAM-4 SerDes TX with PLL is presented. We discussed the system considerations ans structure of the transmitter, and then the layout and test bench setup. After that, the measurements results of the 200Gbps TX is presented.

Chapter 7 concludes this work and and future research directions, and Appendix A presents the detailed optimization problems for the VCO generator in Chapter 2

Chapter 2

An Automated and Process-Portable Generator for Phase-Locked Loops

In this chapter, we propose a phase-locked loop (PLL) generator developed based on BAG using top-down and bottom-up approaches. The PLL generator automatically produces a top-level schematic and layout of a PLL whose circuit parameters satisfy a target performance specification. The proposed generator is process-portable and proven in three different technology nodes from three different foundries. The total generation time took less than four days, showing that the proposed PLL generator enables fast PLL circuit design and technology portability. The simulated and measured performance of the generated PLL is comparable to one that is manually designed.

2.1 Background

Analog Circuit Generation Flow

Figure 2.1 shows the proposed analog circuit generator flow with the traditional top-down and bottom-up design methodology using BAG. First, in the system design, the circuit architecture is chosen based on the system specifications, and the specifications of each block can be derived with system models, calculations and simulations. The interfaces between blocks and loading effects are considered in the block specifications, so the blocks can be merged in schamatic and layout directly.

Then, at the bottom of the hierarchy, the devices are produced with the device-level generators. These devices including transistors, capacitors, inductors, varactors, etc., are the basic elements of analog circuits, similar to different kinds of bricks in Lego, with which houses, trees, castles can be assembled. Starting from the layout and schematic generators, a large number of devices with different parameters and sizes are characterized with simulation scripts to get the target performance specifications, and a look-up table is built on these

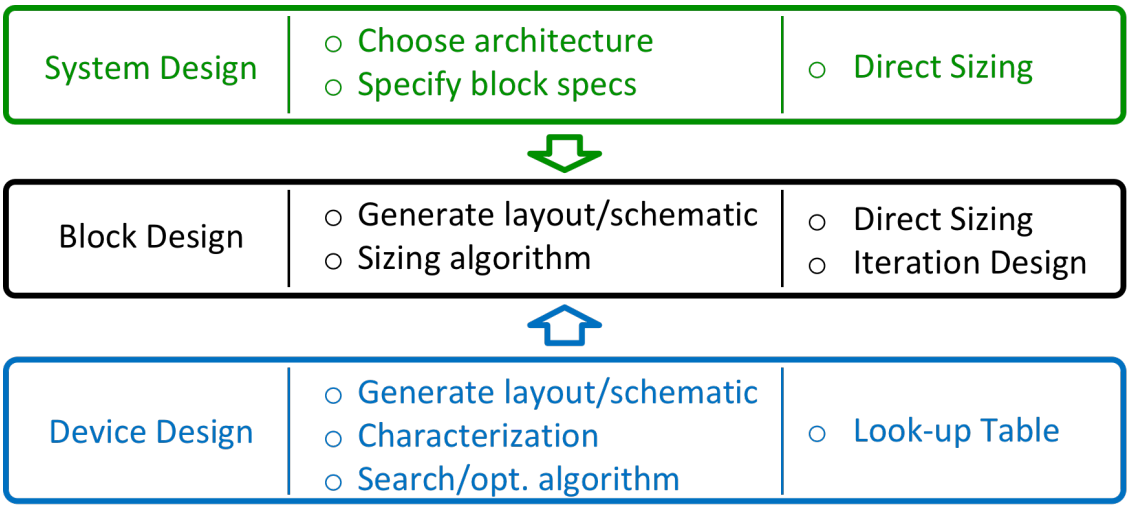


Figure 2.1: Analog circuit generation flow using BAG.

simulation results. Based on the look-up table, we can perform search or optimization algorithms to get the optimal device for a target specification.

Finally, at the middle level, the blocks are designed with the specifications from the system and the devices from the device generators. We can adopt direct sizing approach from simple block, such as the digital circuit designed manually, and use an automatic iteration loop to size a complex design and satisfy the system requirements.

Bang-Bang PLL

Bang-bang loops are widely used in wireline communication system components such as clock and data recovery (CDR) circuits [19], [20] and PLLs [21], [22]. The phase detector (PD) translates the input phase difference into a binary output, which simplifies integration with a digital or hybrid loop filter (LF). Compared to an analog filter, the required areas scale with technology node without performance degradation. A time-to-digital converter (TDC) can be also used for PDs in the digital domain, increasing the complexity of the circuit implementation. Since it is widely used in low-jitter applications, a bang-bang PLL is selected for this evaluation.

Figure 2.2 shows the proposed bang-bang PLL architecture, which is based on a hybrid loop architecture containing a digital frequency loop and an analog phase loop. The digital frequency loop includes a frequency detector (FD), a bang-bang PD and an integrator as digital frequency loop filter. The FD detects the frequency error by comparing the number of counted clock cycles from the reference clock to the divider ratio. The bang-bang PD is a single flip-flop (FF), which generates phase early and late information by sampling the reference clock by the divider output. The FD and PD outputs are combined with

programmable gain to drive the digital loop filter to generate control signals for frequency locking. The digital blocks are developed with Chisel [23] and elaborated to Verilog for digital synthesis.

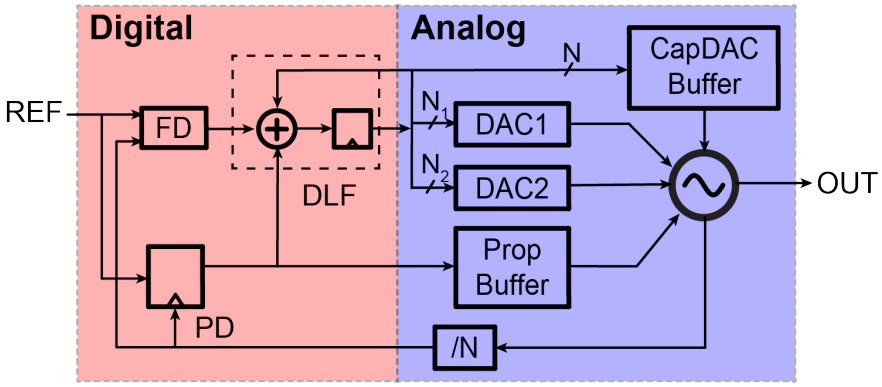


Figure 2.2: Bang-bang PLL architecture.

The analog block contains a clock divider and an LC voltage-controlled oscillator (VCO), as well as peripherals such as a capacitor digital-to-analog converter (DAC) driver, voltage DACs, and a proportional path buffer driving different frequency knobs of the VCO. Figure 2.3 shows a schematic diagram of the VCO, which includes a current mirror, NMOS/PMOS cross-coupled pairs, a capacitor DAC (CapDAC) and three varactors. One of the varactors is driven by a proportional buffer for phase control, with programmable gain K_p to tune the PLL loop bandwidth. The frequency control includes an N-bit CapDAC and two other varactors driven by N_1-bit and N_2-bit DACs. For the CapDAC and varactors, the capacitor and corresponding frequency changes are labeled in Figure 2.3. The analog blocks are implemented with BAG, to create process-portable PLL instances.

2.2 PLL Generator and Design Methodologies

To generate the PLL, the parameterized schematic and layout generators are initially implemented to create subblock instances from bottom to top. Then, the block-level design scripts create block instances to meet block-level specifications from system models. Finally, the generated block instances are combined to produce a top-level instance that satisfies all PLL specifications.

The design methodologies for the PLL generator are classified into three types (Figure 2.4). The direct-sizing method adjusts the block size simply from fanout analysis or pre-defined interfaces. This method is suitable for top-level and non-critical blocks, including CapDAC buffer, divider, proportional path buffer and voltage DAC of the PLL. The design method based on look-up tables is used for single devices or low-level circuits such as cross-coupled pairs, inductors, MOM capacitors, and CapDAC switches. The iteration

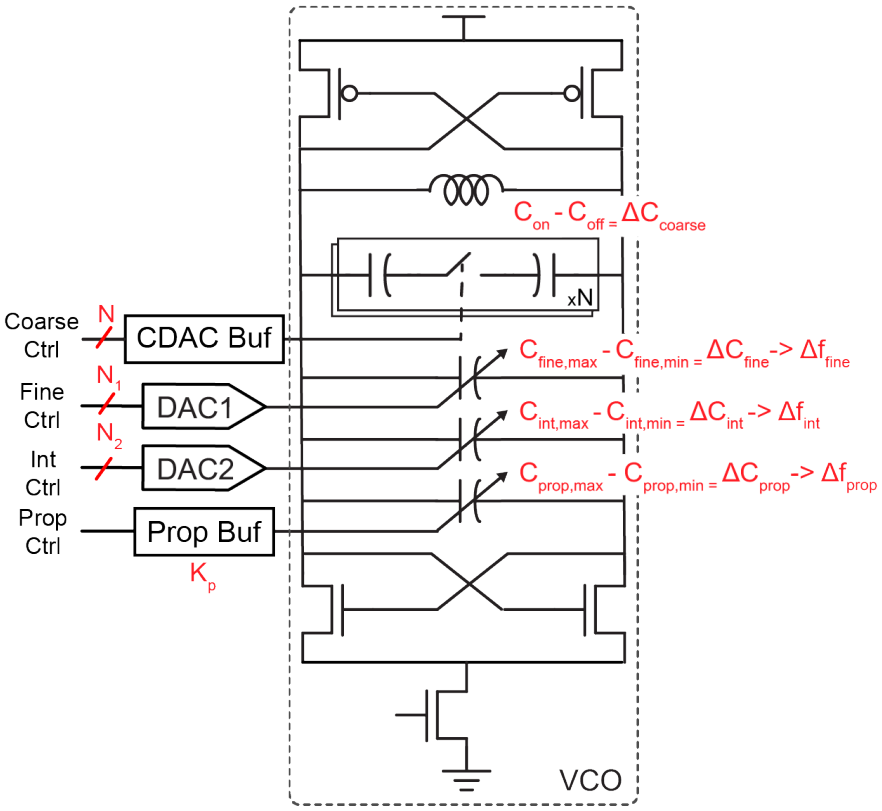


Figure 2.3: Voltage-controlled oscillator schematic.

loop method is used for critical blocks, which are power-consuming and determine the performance of the whole PLL system.

Design Methodology	Direct Sizing	Look-up Table	Iteration Design
Circuit Level	Non-critical blocks or top-level design	Single device, low-level circuits	Critical blocks
Examples	Serializer, Deserializer, PD logics, Clock divider	Inductor, MOM Cap, Varactor, CapDAC Switch, transistors	VCO, VCO buffer, CML driver

Figure 2.4: Three types of design methodologies for different levels of the PLL.

Schematic and Layout Generation

The process-portable circuit generator requires that the design instances, produced from the schematic and layout generators, are DRC- and LVS-clean in different technologies. Figure 2.5 shows the hierarchy of the PLL design using the XBase layout engine, including *TemplateBase*, *AnalogBase*, *DigitalBase*, *ResBase*, *CapBase* and *InductorBase*. It is notable that all layout generators are inherited from *TemplateBase* and merged within.

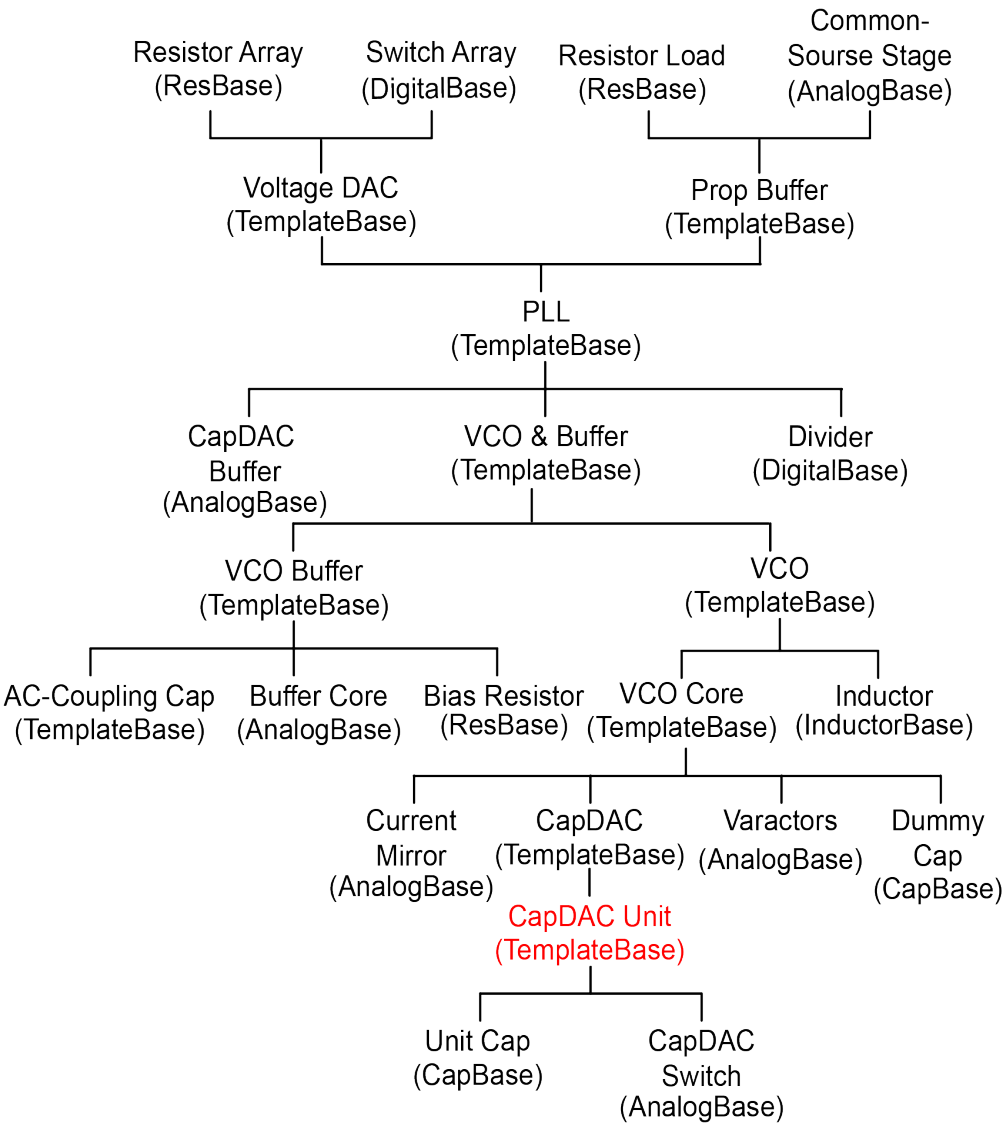


Figure 2.5: The hierarchy of the PLL design.

As shown in Figure 2.6, the layout generator first retrieves the layout parameters, and sizes the design to generate the layout for each block in Figure 2.5, where the *new_template()* function creates a lower-level instance in the Cadence library and the *add_instance()* function instantiates the instance in current layout. The schematic generator gets the schematic parameters from the layout generator and sizes the schematic template with *design()* functions to generate the schematic instance. LVS and extraction are run on the views of the instance to generate the extracted netlist for post-layout simulation. Figure 2.7 shows two VCO layouts with the 4-bit CapDAC, 1-turn inductor with radius of $20\mu m$ and the 3-bit CapDAC, 2-turn inductor with radius of $40\mu m$, respectively, demonstrating the flexibility

and effectiveness of the layout generator. Finally, Table 2.1 summarizes the hierarchy and the corresponding number of lines for each levels in VCO. The whole VCO is implemented with about 7000 lines of code, and the inductor accounts for 43% of them.

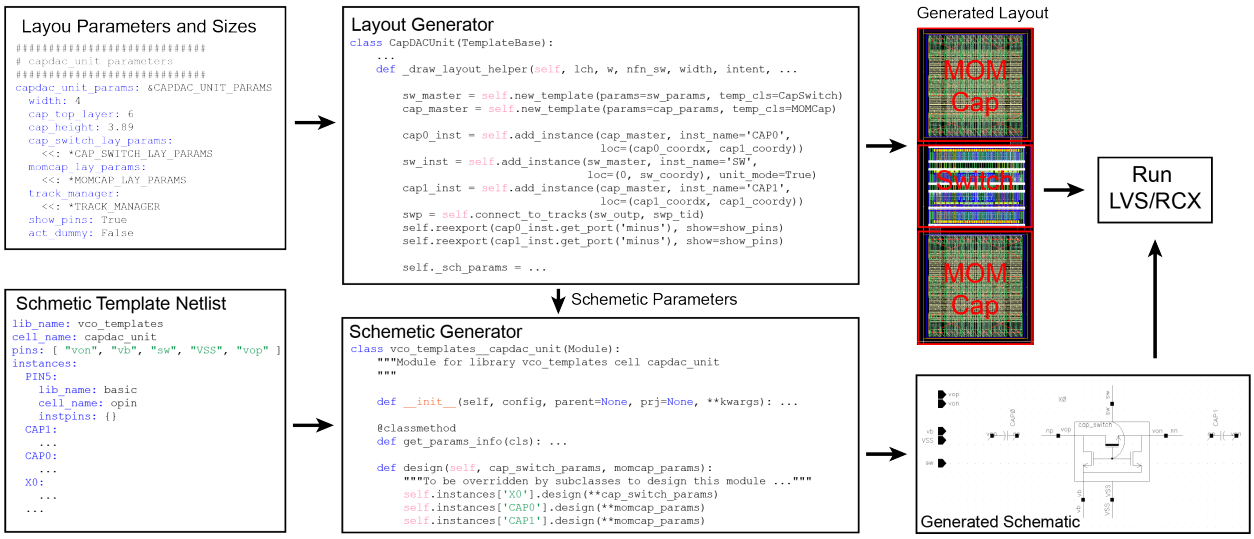


Figure 2.6: Schematic and layout generation flow example with the analog generator.

Table 2.1: Layout generator summary for VCO.

Lv. 1	Lv. 2	Lv. 3	Lv. 4	Lv. 5	Lines of code
VCO					217 (layout) + 1392 (generator)
	Inductor				3032 (layout) + 365 (generator)
	VCO Core				1584
		CapDAC			515
			CapDAC Unit		216
				Cap Switch	289 (layout) + 114 (generator)
				MOM Cap	398 (layout) + 233 (generator)
		Varactor			269 (layout) + 264 (generator)
		Cross-Coupled Pair			193
		Current Mirror			347
		Decouple Cap			--

PLL Top-Level Analysis

The block generators get block-level specifications from the system-level model. In this design, the VCO generator within the PLL generator requires the phase noise and frequency tuning range of the CapDAC and the fine, integral and proportional varactors. Figure 2.8 shows the PLL model, where K_{pd} is the PD gain, K_p is the proportional path gain, K_I is

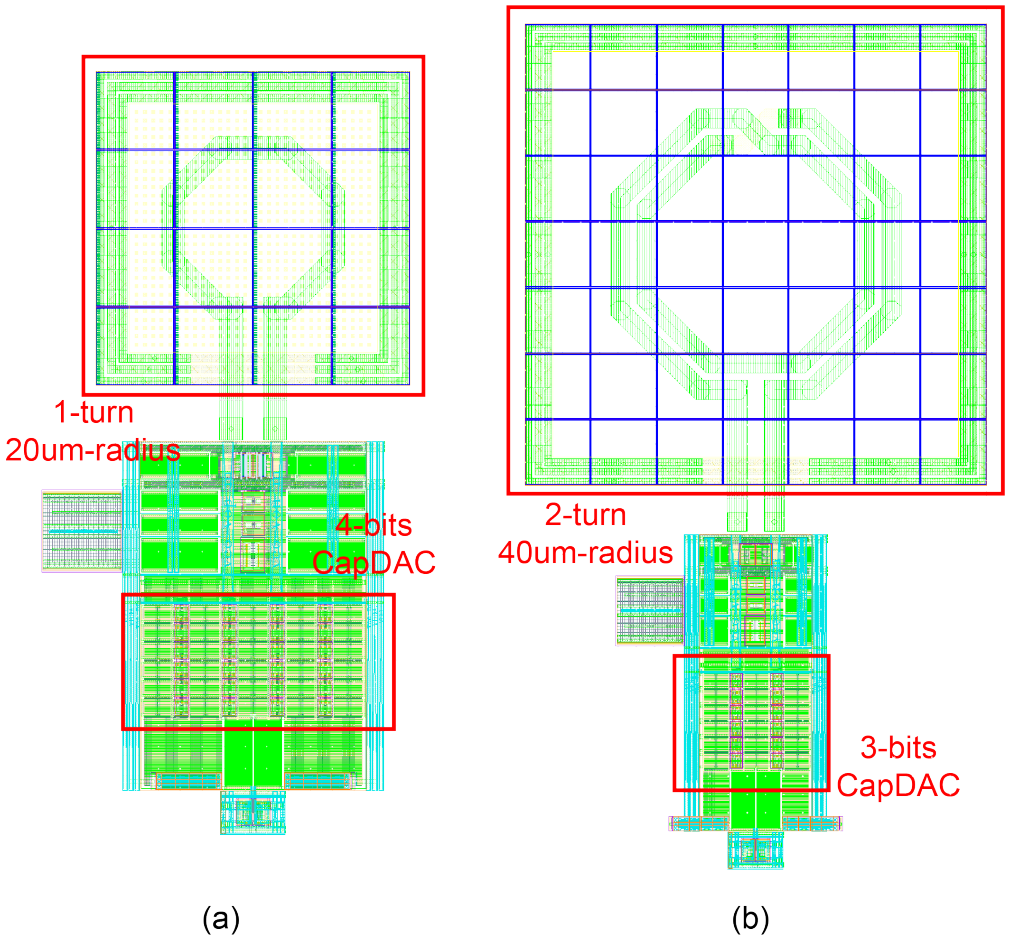


Figure 2.7: VCO layout with (a) 4-bit CapDAC, 1-turn inductor with radius of $20\mu m$ and (b) 3-bit CapDAC, 2-turn inductor with radius of $40\mu m$.

the integral path gain, Δf_{prop} is the proportional frequency step, K_{vco} ($\approx \Delta f_{prop}/V_{DD}$) is the VCO sensitivity to control voltage, and N is the divider ratio.

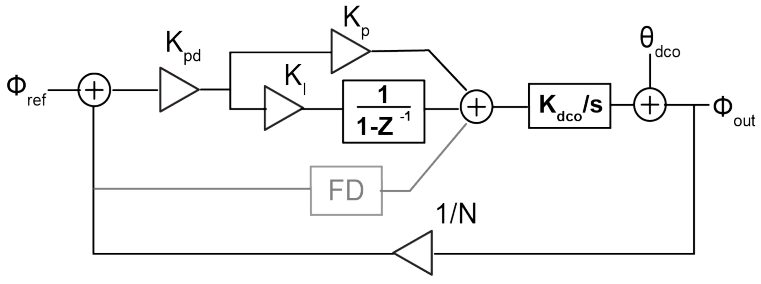


Figure 2.8: PLL model.

The phase noise is dominated by the limit cycle jitter and VCO phase noise. The limit cycle jitter is caused by the latency of the loop, which is related to the update time T_{update} ($= 1/f_{ref}$), proportional and integral gain Kp and K_I, proportional frequency step $K_{BB} = K_p \Delta f_{prop}$, and output frequency f_o.

$$\begin{aligned} J_{lc,pk-pk} &= T_{update}(K_p + K_I)\Delta f_{prop}/f_o && (2.1)\\ &\approx T_{update} K_p \Delta f_{prop}/f_o && (2.2)\\ &= T_{update} K_{BB}/f_o && (2.3) \end{aligned}$$

The VCO phase noise is high-pass filtered by the loop filter with the transfer function

$$H_{vco}(s) = \frac{j\omega}{j\omega + K_{pd}K_p K_{vco}/N} \tag{2.4}$$

where, the open loop gain $G(s)$ is $1 + K_{pd}K_pK_{vco}/j\omega N$, and the loop bandwidth ω_u is $K_{pd}K_pK_{vco}/N$. Consider the phase noise of a VCO with flicker noise is assumed as

$$L(f) = \frac{1}{f^2}(K_w + \frac{K_f}{f}) \tag{2.5}$$

the VCO phase noise and its transfer function are illustrated in Figure 2.9. By integrating the phase noise from low frequeny f_x to infinity, the integrated RMS jitter of the VCO is

$$\begin{aligned} \sigma_{vco}^2 &= 2\int_{f_x}^{\infty} \frac{L(f)}{|1+G(f)|^2}\, dx \\ &= \frac{K_w}{f_u}\frac{\pi}{2}\left[1 + \frac{2}{\pi}\frac{K_f/K_w}{f_u}\ln\left(\frac{f_u}{f_x}\right)\right] \end{aligned} \tag{2.6}$$

$$J_{vco,rms} = \sigma_{vco}/f_o \tag{2.7}$$

So the total RMS jitter is

$$J_{total,rms} = \sqrt{J_{vco,rms}^2 + J_{lc,rms}^2} \tag{2.8}$$

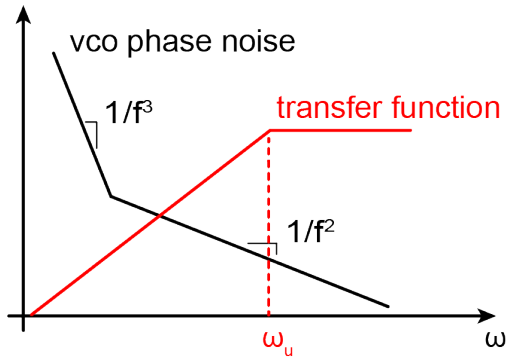


Figure 2.9: VCO phase noise and its transfer function of the BBPLL.

where $J_{lm,rms} = J_{lm,pk-pk}/2\sqrt{3}$[1]. Therefore, VCO phase noise decreases with a higher loop bandwidth (proportional to K_{BB}), and the limit cycle jitter increases when K_{BB} rises. Similar to the analysis in [21] and [22], the optimal K_{BB} can be found, which determines Δf_{prop} if K_p is assumed. Furthermore, for the proper operation of a PLL, the loop bandwidth has to be smaller than the by the 1/10 of reference frequency, and K_{BB} is limited to a maximum value [24].

Figure 2.10 shows the pll phase noise optimization with different proportional frequency step $K_{BB} = K_p \Delta f_{prop}$. As the proportional frequency step cannot be larger than 7.4MHz with the reference frequency limitation mentioned above, we chose the operation point just at the limited frequency and found the design solution which consumes the minimum power.

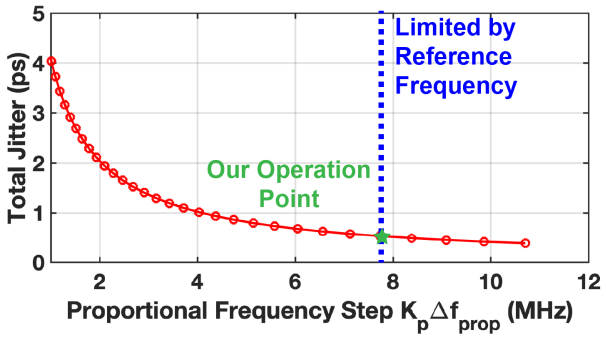


Figure 2.10: Phase noise optimization of the BBPLL in this design.

The VCO is also required to cover the frequency range under process, voltage and temperature (PVT) variations. The maximum and minimum frequency are restricted by $f_{max} - f_{min} = \alpha f_0$, where α is the frequency range ratio and f_0 is the center frequency. The frequency overlaps between CapDAC and fine varactor settings, as well as fine varactor and

[1]For uniform distribution, the ratio between the interval length and the standard deviation is $2\sqrt{3}$

integral varactor settings, guarantee continuous frequency tuning. Finally, to avoid jitter contribution from the frequency control loop, the frequency resolution of the integral varactor is required to be much higher than that of the proportional varactor. These conditions are listed as constraints in the optimizations of the VCO design.

Inductor Generator

When running block-level generators, device-level generators are required to provide the optimal devices for given specifications. For example, the device-level generators for the MOS transistors, inductors, MOM capacitors, and CapDAC switches in the VCO are based on the look-up table design method. These device generators follow a similar optimization approach except for their input parameters and performance specifications. In the following, the generator of inductors, MOM capacitors and CapDAC switches are used as examples to show the development of a device-level generator.

One particular issue in inductor generation is the potential for DRC errors in inductor layouts with certain parameters. For instance, when the radius of an inductor with multiple turns is too small, the layout is unfeasible because of some of the required paths are too short to meet DRC rules. To address this problem, a feasibility function is defined

$$Feasibility(n, r, w, s) = \begin{cases} 1 & \text{if } DRC\ clean \\ 0 & \text{if } DRC\ dirty \end{cases} \tag{2.9}$$

where n is number of turns, r is radius, w is metal width and s is metal spacing. This function supports computations such as interpolation of the four variables and optimization for quality factor (Q) or area. When this function value is smaller than 1, the inductor is considered infeasible (Figure 2.11).

As shown in Figure 2.12, the inductor generator includes three parts. The first part is sweeping inductors of different sizes. Starting from the inductor schematic and layout generator, four parameters including radius, number of turns, metal width and space are swept. The generated layouts are sent to EMX for electromagnetic (EM) simulation and the inductance and Q are calculated based on the S-parameter results. The feasibility value is also included by checking the inductor layout.

In the second step, inductor query, an interpolation method is performed across the whole look-up table, to produce the inductor, Q and feasibility functions. With these functions, the inductance and Q are estimated to within an error of 1%, as shown in Table 2.2. Finally, with the query functions, a search algorithm is implemented based on the look-up table for maximum Q or minimum size. The search result is used as a initial value for the openMDAO [25] optimization algorithm to further optimize the result. After an optimized inductor is generated, the S-parameter and model files are extracted by EM simulation for higher-level circuit simulations.

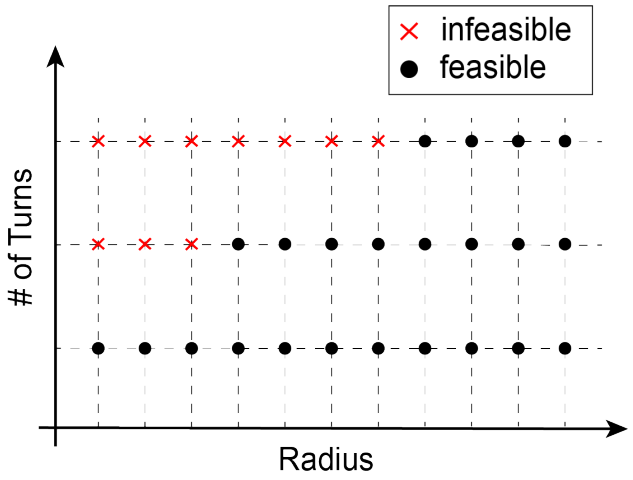


Figure 2.11: Inductor feasibility check example (for given width and space).

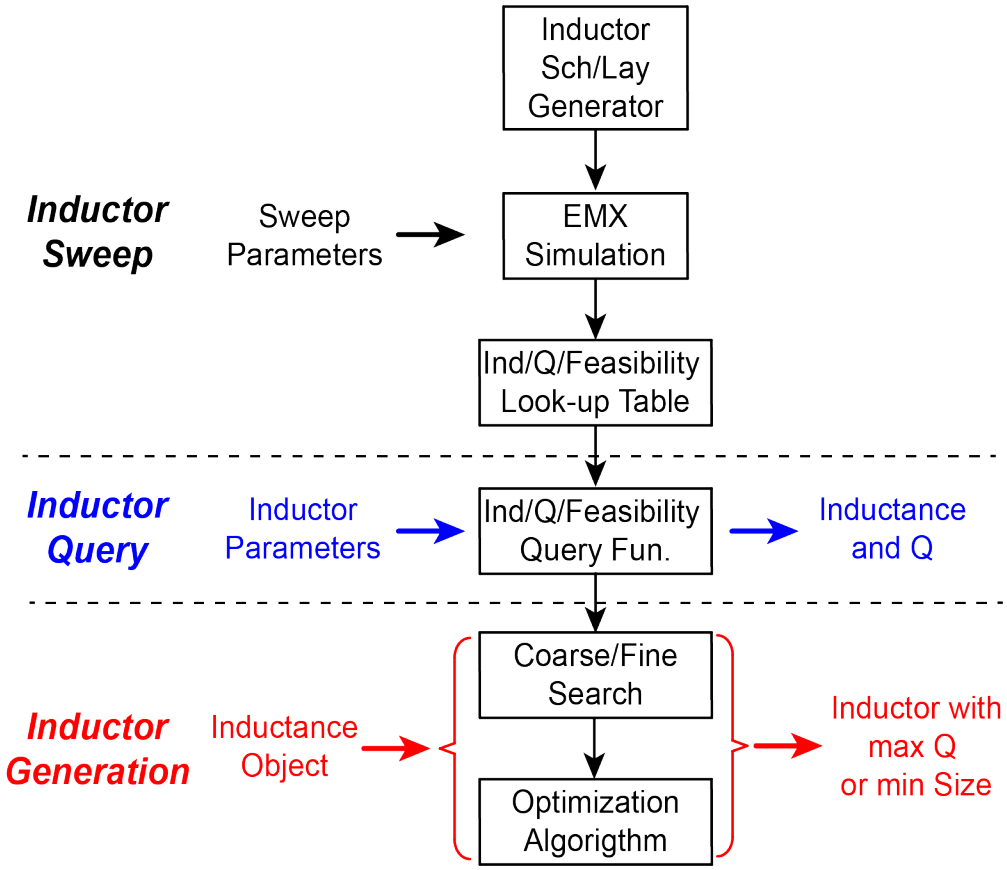


Figure 2.12: Inductor generation flow.

Table 2.2: Inductance and Q-factor comparison from inductor query function and EM simulation at 14GHz

#	turn	radius (µm)	width (µm)	space (µm)	EM Sim		Calculation		Relative Error	
					Inductance (nH)	Q	Inductance (nH)	Q	Inductance	Q
1	2	62	4.5	2.5	0.894	11.56	0.891	11.60	0.34%	0.34%
2	1	62	4.5	2.5	0.324	9.27	0.322	9.28	0.62%	0.11%
3	3	62	4.2	2.5	1.78	10.76	1.77	10.70	0.56%	0.56%
4	2	75	7	3.3	1.02	12.62	1.02	12.64	0%	0.16%

Varactor Generator

As it is difficult to change inductance of the tank on chip, the frequency of the VCO is usually modified by changing capacitance in the LC-tank, and the corresponding device to realize the function is varactor. There are two kinds of varactors in a CMOS technology [26], which are inversion-mode MOS (I-MOS) capacitor and accumulation-mode MOS (A-MOS) capacitor.

The inversion-mode varactor is based on a MOS transistor, with gate is one terminal, and drain, source, and base are connected together as the other terminal. As the name suggests, this type of varactor is in inversion mode. On the other hand, for the varactor in accumulation mode, the D–S diffusions (p-doped) from the PMOS device are replaced with n-doped diffusions. Though A-MOS varactors offers more linear transfer function between control voltage and capacitance, and higher Q, which results in better VCO phase noise performance. However, we use I-MOS varactors in this design due to its simplicity and compatibility with BAG.

For the varactor, the design parameters are the transistor channel length, number of fingers, and device threshold, which affects the average capacitance ($C_{var-avg}$), capacitance range ($C_{var-range}$) and quality factor (Q_{var}) of the varactors. Consider a LC-tank with CapDAC, and a varactor, the Q of total capacitors are

$$\frac{1}{Q_{total}} = \frac{C_{var-avg}}{C_{total}}\frac{1}{Q_{var}} + \frac{C_{CapDAC}}{C_{total}}\frac{1}{Q_{CapDAC}} \tag{2.10}$$

where Q_{total} is the Q of total capacitors, C_{total} is the total capacitance, C_{CapDAC} is the capacitance of the CapDAC, and Q_{CapDAC} is the Q of the CapDAC. Therefore, to improve the Q of the total capacitors, for given capacitance tuning range of the varactor, we need the ratio between the Q and the average capacitance of the varactor ($Q_{var}/C_{var-avg}$) being as large as possible. As the tuning range is also critical for a varactor, the figure-of-merit (FOM_{var}) for a varactor is defined as

$$FOM_{var} = \frac{Q_{var}C_{var-range}}{C_{var-avg}} \tag{2.11}$$

Figure 2.13 shows the capacitance tuning range, capacitance ratio between tuning range an average capacitance, Q and FOM versus different number of fingers and channel lengths for ulvt varactors. As the figures suggest, the longer channel length provides large ratio between varactor capacitance range and average capacitance, while the channel lengths in the middle provides the best Q. This can be explained by the gate resistance and channel resistance. When the channel length is small, the gate resistance is dominant, and reversely, the channel resistance is dominant. Hence, in total, the channel lengths 36 nm and 72 nm provide the optimal FOM values, and channel lengths 76 nm, 80 nm, 84 nm, 88 nm and 90 nm also offer reasonable FOM values.

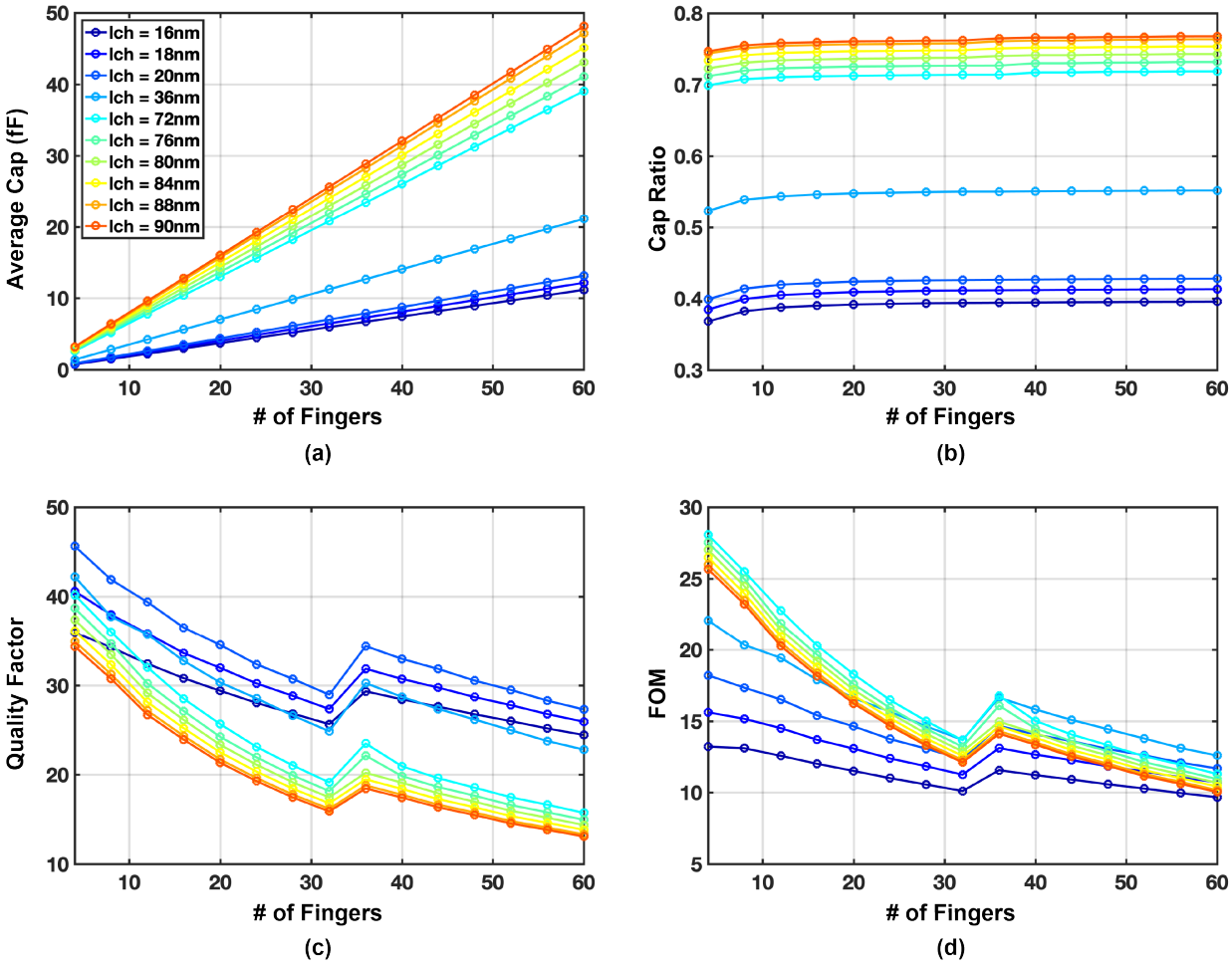


Figure 2.13: (a) Capacitance tuning range, (b) capacitance ratio between tuning range an average capacitance, (c) Q and (d) FOM versus different number of fingers and channel lengths for ulvt varactors.

Hence, similar to the generation procedure of inductor, the varactors with optimal FOM

are chosen to make the look-up table for the searching algorithms. Figure 2.14 shows the average capacitance, number of fingers, channel length and transistor threshold versus capacitance tuning range of these optimal varactors. As expected, the average capacitance and number of fingers increases with the rising of capacitance tuning range. The optimal channel lengths vary from 36 nm to 90 nm, and most of the optimal device are svt devices.

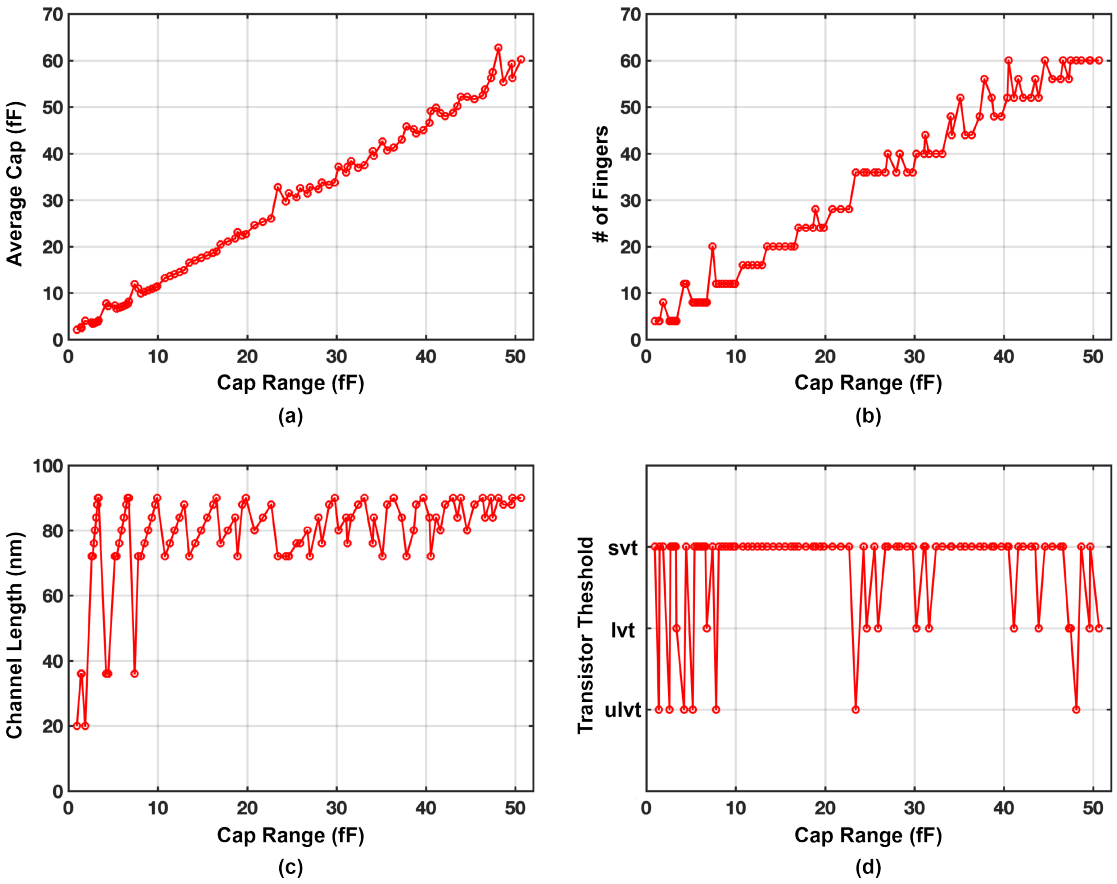


Figure 2.14: (a) average capacitance, (b) number of fingers, (c) channel length and (d) transistor threshold versus capacitance tuning range of optimal varactors.

MOM Capacitor Generator

The MOM capacitors are made up of inter-digitated fingers on multiple stacked metal layers, and a replacement of MIM capacitor for their compatibility with standard CMOS technology, which shows high density with the process scaling. In MOM capacitors, the main parameters are width, height and layers of the stack-up metal. The metal layers used by the MOM capacitors affects its capacitance, parasitic capacitance of one terminal and Q. Table 2.3

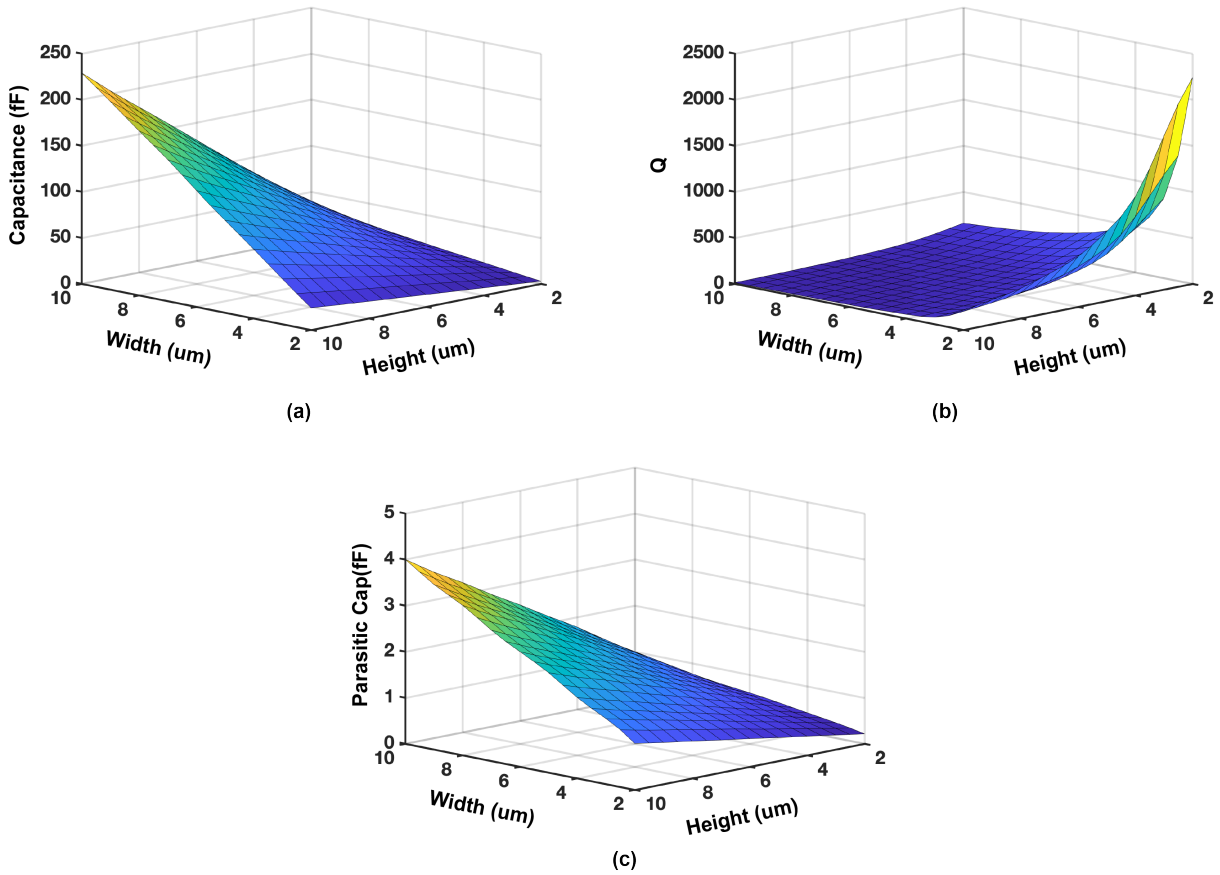


Figure 2.15: (a) Capacitance, (b) Q and (c) parasitic capacitance of MOM capacitors using M5 and M6 with different width and height.

compares $10 \times 10um^2$ capacitors using different metal layers with the top layer fixed to M6 in TSMC 16nm.

Table 2.3: Comparison of MOM capacitor with different layers.

layer	Capacitance	Parasitic Cap	Percentage	Q value
M1-M6	485.88 fF	9.25 fF	1.90%	6.08
M2-M6	403.05 fF	6.33 fF	1.58%	6.89
M3-M6	325.61 fF	5.15 fF	1.58%	7.98
M4-M6	243.92 fF	3.72 fF	1.52%	34.65
M5-M6	165.70 fF	3.06 fF	1.85%	432.66

In this particular process, for the applications of MOM capacitors, where the Q are critical (capacitors in the LC tank or AC-coupling capacitors), we would like to use MOM

capacitors with layers from M5 to M6. For the DC coupling capacitors, M1 to M6 are the optimal stack-up layers for their high capacitance density. Otherwise, for other applications, to reduce the bottom-plate capacitance ratio, the MOM capacitors with layers from M4 to M6 are preferable. Figure 2.15 shows the capacitance, Q and parasitic capacitance of MOM capacitors using M5 and M6 with different width and height, which are stored as the look-up table. Based on the loop-up tables, Figure 2.16 shows the height and parasitic capacitance interpolation functions for 4 um wide MOM capacitors using M5 and M6 with different capacitances. These functions can be used to find the dimensions and estimate the parasitic capacitance for capacitors with given capacitance.

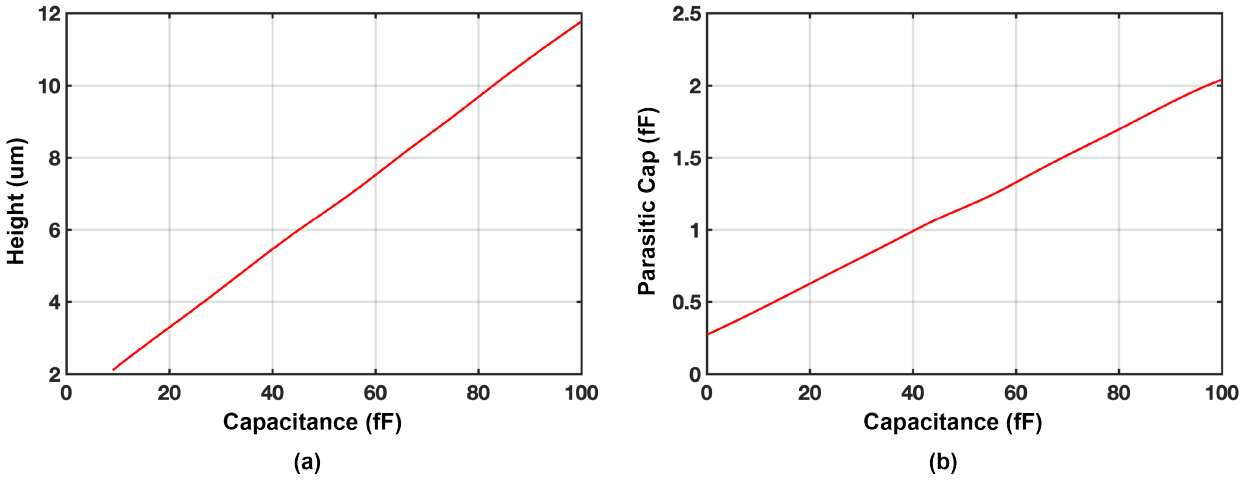


Figure 2.16: (a) Height and (b) parasitic capacitance of one terminal for 4 um wide MOM capacitors using M5 and M6 with different capacitances.

CapDAC Switch Generator

In the LC VCO, the coarse resonate frequency is modified by turning on or off the switches in a CapDAC, as the capacitance represented to the LC tank changes. However, the switch resistance and parasitic capacitance will affect the tank Q and the VCO design.

Figure 2.17 shows the circuit diagram of capacitor switch used in the CapDAC. While transistor M0 is the differential switch that controls the on and off of two capacitors, transistor M1 and M2 provide bias to the M1 drain and source. In real designs, transistor M0 is sized to reduce the turn-on resistance, and transistor M1 and M2 use minimum sizes to avoid extra parasitic capacitance.

Figure 2.18 plots the resistance and parasitic capacitance, by sweeping the number of fingers of transistor M0 with transistors of different thresholds. As expected, the ulvt devices provides the minimum resistance, while almost same parasitic capacitance. The results are saved into a look-up table for high-level circuit generation.

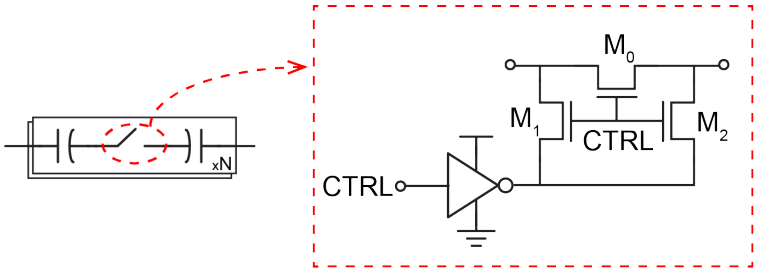


Figure 2.17: Capacitance switch circuit diagram.

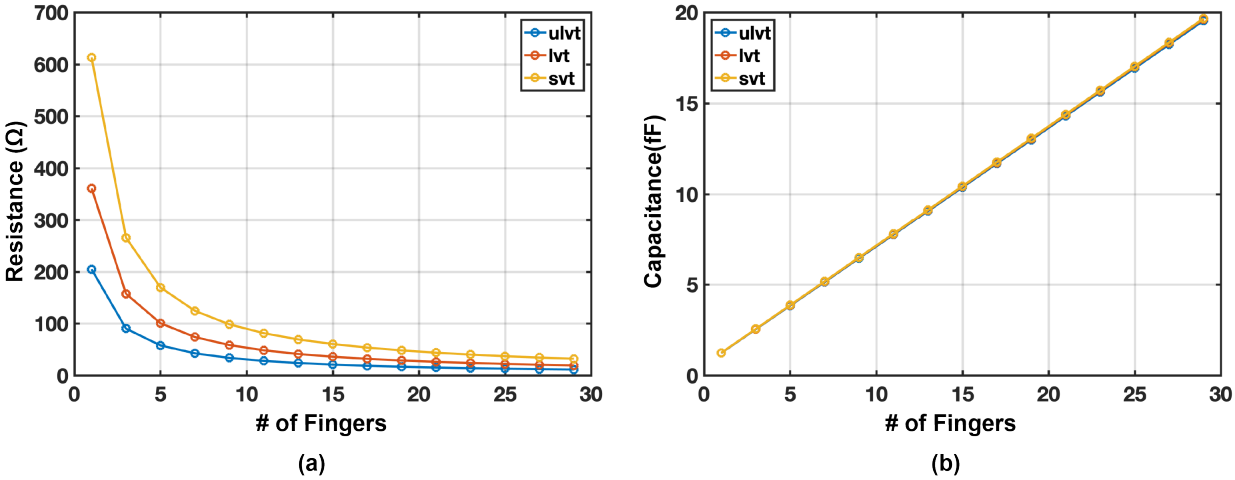


Figure 2.18: Capacitance switch simulation results.

VCO Design Procedure

The LC VCO is designed with a iteration loop, due to the crucial role that influences the power, phase noise and frequency range of the PLL. The aim for the VCO design is to satisfy given phase noise, frequency range, and frequency resolution specifications with minimized power. Before looking into the design procedure, the design considerations of phase noise and frequency planing are discussed as follows.

First, the phase noise of a LC VCO is defined by Leeson's equation [27]

$$\mathcal{L}(\omega_m) = (1 + NF) \cdot \frac{1}{V_o^2} \cdot \frac{kT}{C} \cdot \frac{\omega_o}{Q} \cdot \frac{1}{\omega_m^2} \tag{2.12}$$

where, ω_m is the offset frequency, NF is the noise factor, V_o^2 is the output amplitude, kT is Boltzmann's constant times the temperature of observation, C is the tank capacitance, ω_o is the oscillating frequency, Q is the tank quality factor. Interestingly, the inductance L is not

shown in Equation 2.12, but embedded in the oscillating frequency. The output amplitude of the VCO is related to the bias current I_b and tank parallel resistance R_p, and can be calculated as

$$V_o = \frac{2}{\pi} I_b R_p = \frac{2}{\pi} \omega I_b Q L \tag{2.13}$$

The right side of Equation 2.13 is due to the property of a parallel LC tank, where $Q = R_p/\omega L$. Figure 2.19 (a) shows VCO output amplitude versus bias current [28]. When the current increases from a small value, the output amplitude follows Equation 2.13 initially, and then becomes saturated by the supply rails. When in saturation, the MOS transistors stay in triode region limited the supply rails, and the reduce its output impedance causes the tank parallel resistance R_p decreases. Therefore, the two regions are called current-limited (I-limited) and voltage-limited (V-limited) regions. In the I-limited region, the phase noise improves with the increase of output amplitude V_o. However, in V-limited region, the phase noise becomes worse due to the extra current noise injection from the current mirror and cross-coupled pair transistors, but nearly constant output amplitude V_{max}. Considering the phase noise, power consumption and efficiency, the current value between the I-limited region and V-limited region is the optimal bias point. This operation point determines the size of the transistors, if the overdrive voltages $V*$ of transistors of the current mirror and cross-coupled pair are assumed.

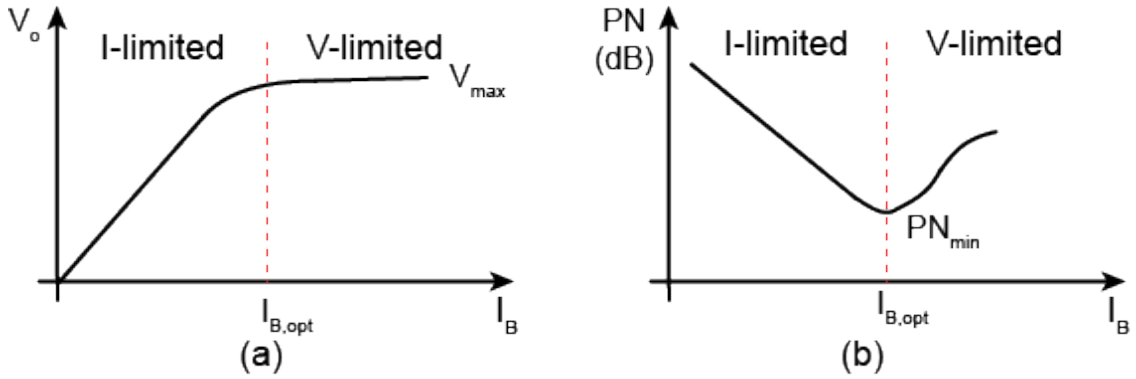


Figure 2.19: VCO (a) output amplitude and (b) phase noise versus bias current.

Then, for the tank capacitance C and quality factor Q, consider that the tank inductance reduces, the tank capacitance has to increase to maintain the oscillating frequency. This is done by sizing up all the components in the VCO except the inductor, including the CapDAC, varactors, cross-coupled pair and current mirror transistors, so the ratio between variable capacitance and total capacitance stays constant, and hence the same goes for the frequency tuning range and resolution. Similarly, the current are sized up by the same ratio to keep identical voltage biases of the transistors. Assume that the Q of the tank does not vary

too much, with the increase of tank capacitance, the phase noise becomes better, showing a trade-off between power and phase noise (Figure 2.20).

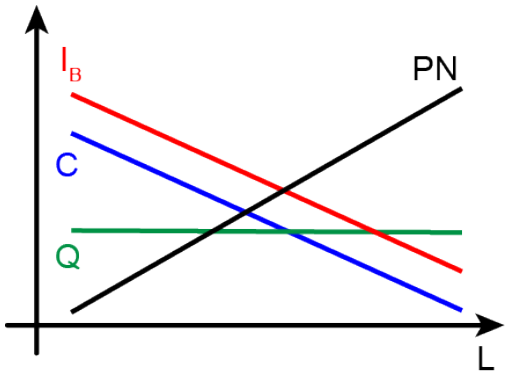


Figure 2.20: VCO Bias current, tank capacitance, Q and phase noise versus tank inductance, for the same frequency range and resolution.

Finally, to minimize the noise factor, the flicker noise from the tail current source are suppressed by increasing its transistor lengths, and use reasonable current mirror ratio. The AM-PM noise conversion are considered by choosing reasonable varactor sizes and CapDAC bit, which is four in this design.

As shown in Figure 2.3 of the VCO, the phase control is through a varactor, and the frequency control includes an N-bit CapDAC and two varactors. The CapDAC and the fine varactor aims to cover enough frequency tuning range, and the fine varactor provides tiny capacitance variation for frequency resolution.

Figure 2.21 depicts a single-ended model of the VCO tank, where the frequency range and resolution are affected by the inductor L, capacitor DAC, fine-tuning varactor C_{fine}, routing parasitic capacitor C_{par}, load capacitance C_L, explicit capacitor C_{exp}, integral-tuning varactor C_{int} and proportional path varactor C_{prop}. R_L, R_{fine}, R_{int} and R_{prop} are the parasitic resistances of the inductor and the fine, integral, and proportional varactors, which determine the tank Q. R_{sw}, C_{sw} and C_p are the resistance of the unit switch the capacitance and bottom plate capacitance of the unit MOM capacitor in the CapDAC, respectively. The Capacitor DAC is split into N units with a capacitor and switch of N_{sw} fingers. Based on the model, two optimization problems (A.5 and A.10 in Appendix A) are derived to meet the frequency range and resolution specification.

Figure 2.22 shows the VCO design flow as three steps. The design flow starts by generating an inductor with the maximum Q factor for a given initial inductance value estimated from an initial phase noise factor.

In step one, C_{prop}, C_{int} and C_{exp} are modeled as a fixed capacitor C'_{exp}. Based on the initial inductance, the VCO generator decides the fine tuning varactor capacitance, the CapDAC unit capacitance C and the capacitor switch N_{sw} (Figure 2.21) by maximizing

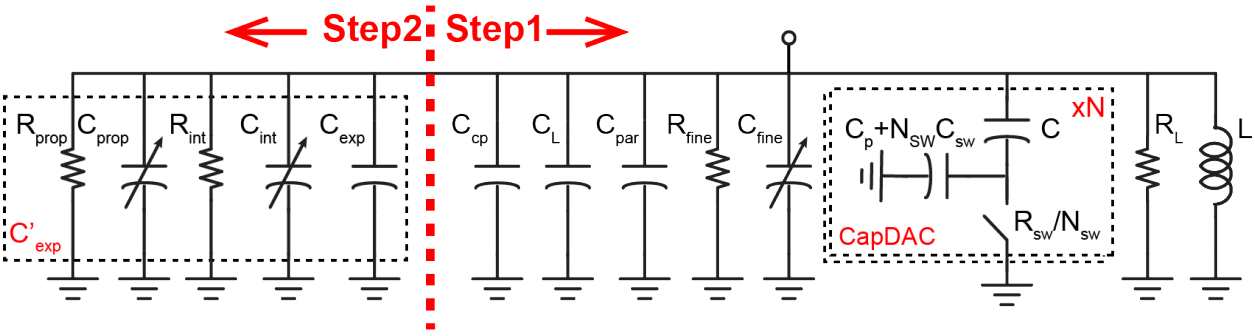


Figure 2.21: VCO tank model.

the resonant tank Q factor with frequency range constraints, as shown in Equations 1 of Figure 2.22. However, the size of the cross-coupled pair and its parasitic capacitance are still undetermined when running the searching algorithm, and the frequency drops after taking it into consideration. To address this problem, when the cross-coupled pair is sized, its parasitic capacitance is returned to the searching algorithm until the size of the cross-coupled pair converges to a stable value.

Similarly, the routing parasitics were initially neglected, causing a frequency gap between calculation and simulation. This parasitic capacitance is included in C_{par} and updated by equation (2.14) after each simulation and sent back to the search algorithm until the frequency converges to the design specifications.

$$C_{par,new} = C_{par,old} + \frac{1}{4\pi^2 L}\left(\frac{1}{f_{sim}^2} - \frac{1}{f_{cal}^2}\right) \tag{2.14}$$

Another search algorithm designs the integral and proportional varactors, by maximizing tank Q with frequency overlap and resolution constraints, as shown in Equations 2 of Figure 2.22. From Equations 3 of Figure 2.22, once output amplitude V_0 and center frequency f_0 are determined, the reduction in inductance L causes a increase of total capacitance C and bias current I_b, as well as an improvement in phase noise. Therefore, after checking the phase noise result from post-layout simulation, the loop iterates with decreasing inductance until the phase noise specification is satisfied.

2.3 Simulation and Measurement Results

The PLL generator is tested in three CMOS FinFET technologies, TSMC 16nm, GF 14nm and Intel 22nm. The design time to generate a full layout is less than four days, including less than 20 minutes for schematic and layout generation, 12-37 hours for VCO generation and one day for adding dummy fill and I/O pads with electrostatic discharge (ESD) protection. The time differences of VCO generation are mainly caused by the extraction and

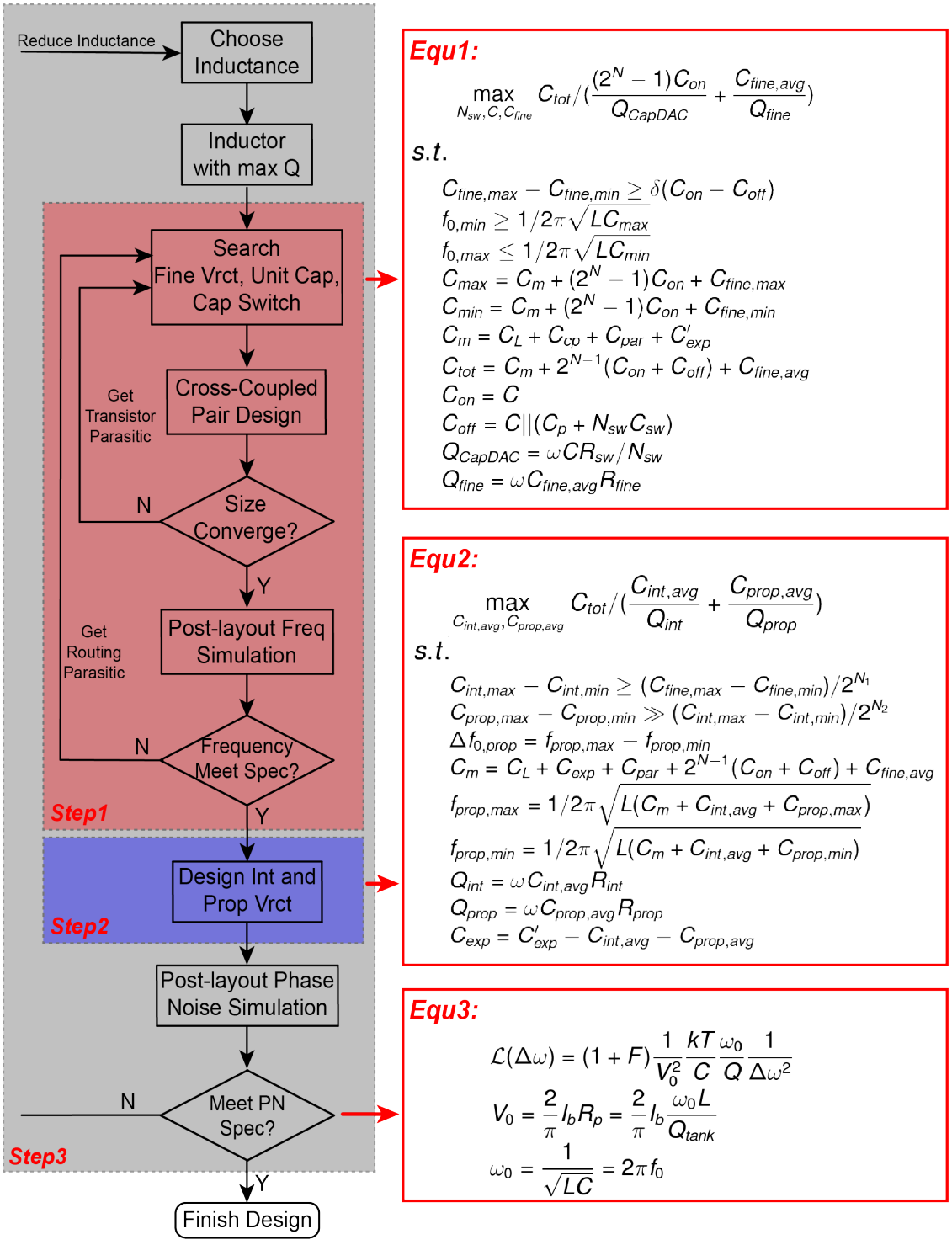


Figure 2.22: Automatic VCO design flow.

Table 2.4: Top-level specifications for PLL generator

Center frequency f_0	14 GHz
Total RMS Jitter J_{tot}	600 fs
Frequency range ratio α	20%
Overlap ratio δ	20%
CapDAC bits	4
Fine DAC bits	8
Integral DAC bits	7
Proportional gain K_p	0.15
Proportional frequency step Δf_{prop}	33 MHz

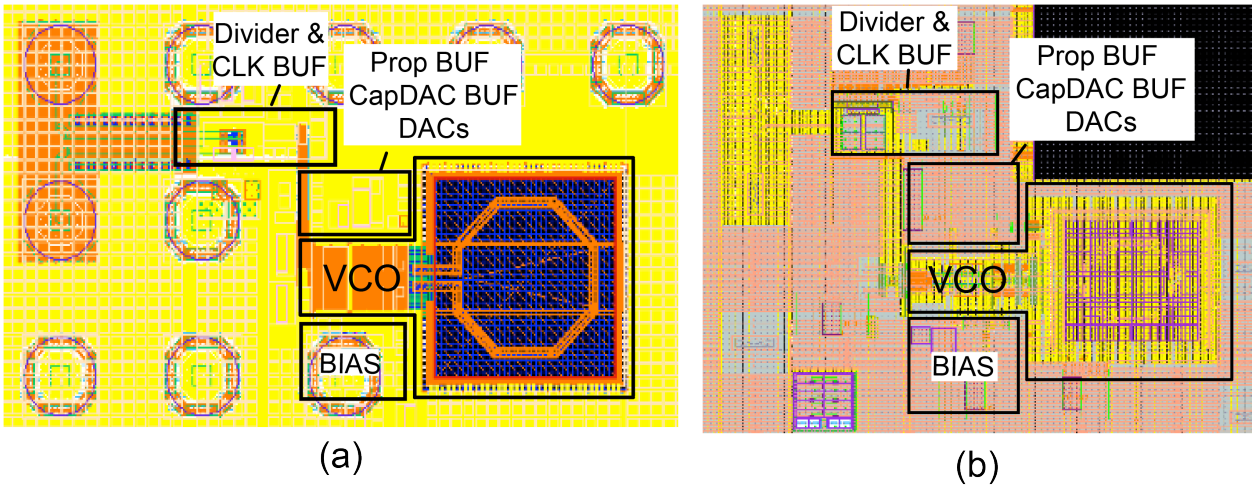


Figure 2.23: Generated PLL layouts at (a) GF 14nm and (b) Intel 22nm technologies.

simulation procedures in different technologies. The specifications and parameters are shown in Table 2.4. Figure 2.23 shows the PLL layouts in GF 14nm and Intel 22nm technologies. The core areas of the two layouts are $0.043mm^2$ and $0.048mm^2$. Figure 2.24 shows the PLL micrograph located in a $28Gbps/32Gbps$ SerDes of TSMC16nm process, with the core area being $0.042mm^2$. Figure 2.25 shows the measured phase noise of PLL; the integrated jitter is $565.4fs$ in the $1KHz$ to $100MHz$ frequency range with a power of $6.64mW$ from a $0.9V$ supply.

Figure 2.26 shows the simulated phase noise and frequencies with different CapDAC settings of the generated VCO in three different processes under specifications of -100dBc/Hz phase noise at 1MHz offset and 20% range of the 14GHz center frequency. From the results, the three designs meet the target design specifications, validating the effectiveness of the VCO design scripts and demonstrating their process portability.

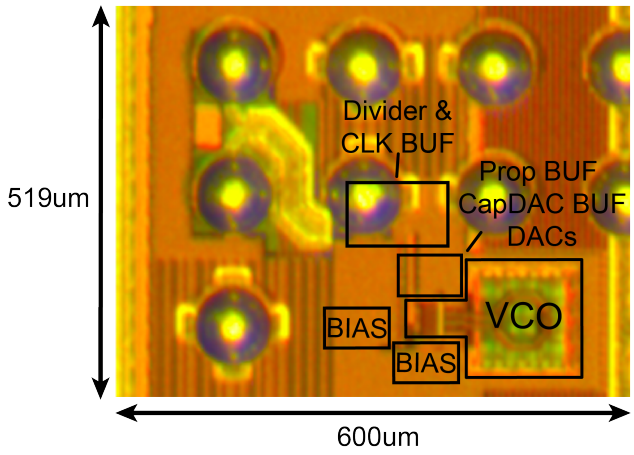


Figure 2.24: Chip micrograph of the PLL in TSMC 16nm.

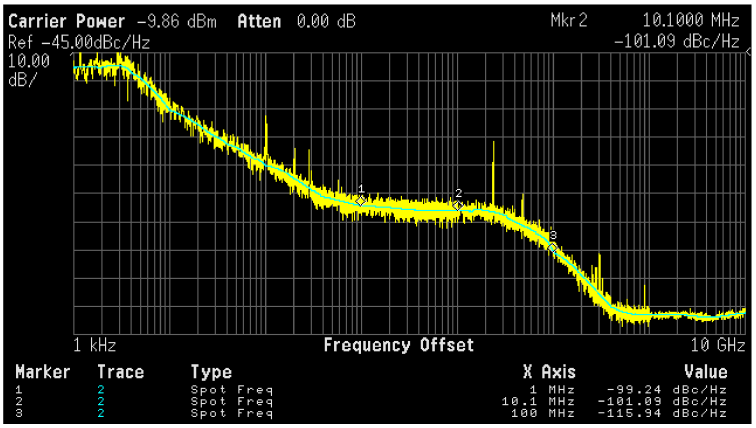


Figure 2.25: Measured PLL phase noise at 14GHz in TSMC 16nm.

Table 2.5 compares this design with state-of-the-art PLLs working around 14GHz [29],[30],[31],[32], where get a reasonable figure-of-merit (FOM) compared with other custom designs, demonstrating the capability of our design methodology and PLL generator.

2.4 Summary

In this chapter, a complete process-portable LC PLL generator is developed and with instances generated in multiple technology nodes. The layout and schematics instances are DRC- and LVS-clean. Three different kinds of design methodologies are introduced and used to generate the PLL instance meeting design specs automatically. The measurement results of the fabricated 16nm chip demonstrate the performance is comparable to a manually designed circuit, meeting the specifications for high-speed wireline links.

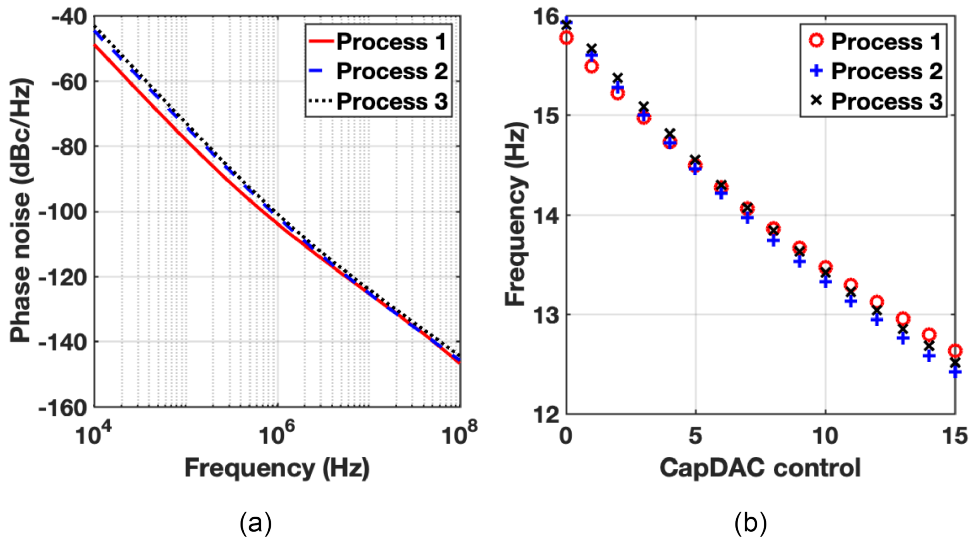


Figure 2.26: Simulated VCO performance in three different technologies: (a) Phase noise and (b) frequency range with CapDAC control.

Table 2.5: PLL performance comparison.

	ISSCC'14 [29]	JSSC'16 [30]	VLSI'17 [31]	ISSCC'09[32]	This work
Frequency	15GHz	10GHz	18GHz	11GHz	14GHz
Architecture	Injection-locked + Ring VCO	PFD + Ring	Sampling + LC VCO	Bang-Bang + LC DCO	Bang-Bang + LC VCO
Ref. Clk	1.875GHz	625MHz	450Mhz	245MHz	875MHz
Power(mW)	46.2	7.6	25.2	20.4	6.64
Technology	20nm	65nm	16nm	65nm	16nm
Supply(V)	1.25/1.0	1.2	0.9/1.8	1.1/1.2	0.9
Area(mm^2)	0.044	0.009	0.39	0.088	0.042
RMS Jitter	268fs	414fs	164fs	345fs	565.4fs
$FOM_J(dB)^*$	-234.8	-238.8	-241.7	-236.1	-236.7

$^*FOM_J = 10log(\frac{\sigma_{rms}}{1s} \cdot \frac{Power}{1mW})$

Chapter 3

Clock Distribution for 200Gb/s PAM-4 SerDes TX

For ultra-high-speed wireline IOs, the development of wireline TX exceeding $200Gb/s$ has become the next goal. This chapter provides a flexible clock distribution network for a $200Gbps$ pulse amplitude modulation four-level transmitter using the layout generators in 28nm CMOS technology [33],[34].

3.1 200Gb/s TX architecture and Clock Distribution Requirements

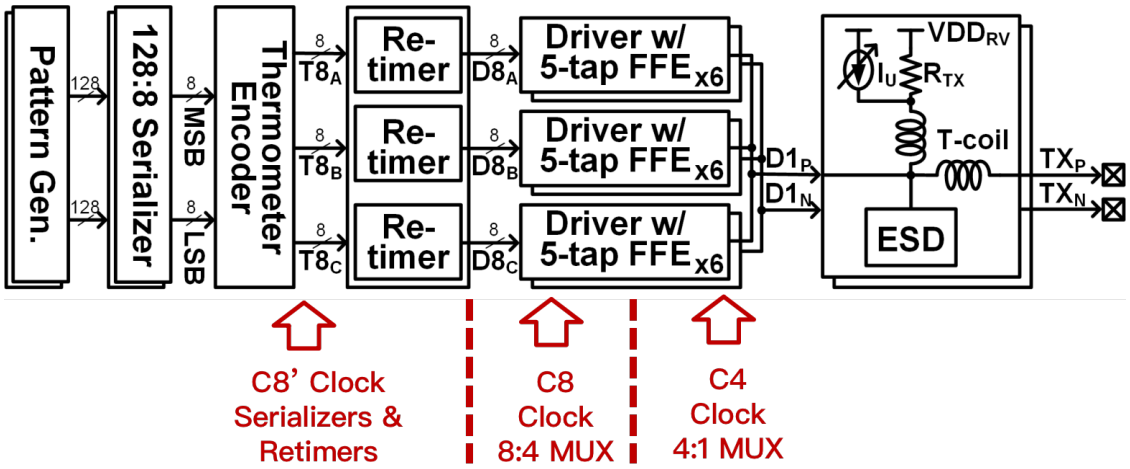


Figure 3.1: TX data path diagram and its requirements for clock distribution.

Figure 3.1 shows the structure of the data path, which consists of pattern generators, 128:8 serializers, a thermometer encoder, retimers, and three FFE driver bundles which are

equally weighted. In PAM-4 mode, the three retimers receive three thermometer-encoded signals ($T8_{A/B/C}$), while in NRZ mode, they receive three identical signals from thermometer encoder. The retimer outputs ($D8_{A/B/C}$) are sent to the three driver bundles, each composed of six segments connected in parallel. The output currents from the segments are summed in a customized termination network with 90 Ω resistors, pull-up current sources and electrostatic discharge (ESD) protection diodes. The T-coils inserted between the termination network and pads [7], [15], [35] are designed to minimize the worst-case ISI pattern.

From the diagram of Figure 3.1, the data path received three clocks with stringent timing constraints, which are 25 GHz C4 clock for 4:1 MUX, 12.5 GHz C8 clock for 8:4 MUX and 12.5 GHz C8' clock for Serializers and retimers. For example, the setup time and hold time of the 4:1 MUX are $< 10\,ps$. Considering the delay variation of the 8:4 MUX, C8 clock distribution and C4 clock distribution, it is extremely hard to satisfy the timing requirements at different PVT corners. Furthermore, due to the segmented data path architeture, the capacitive load from eighteen driver and FFE segments for the clock distribution is large. For C4 clock of highest frequency, the capacitive load is about 290 fF. Finally, The 4:1 MUX requires a clock distribution network to correct duty-cycle error and quadrature error for a output eye diagram without distortions.

Therefore, the clock distribution network (3.2) includes three blocks with programmable delay. C4 clock distribution corrects the duty-cycle error and quadrature distortion and drive the large load from 4:1 MUX. C8 and C8' clock distribution offers delay variation to meet the time margin between clock domains.

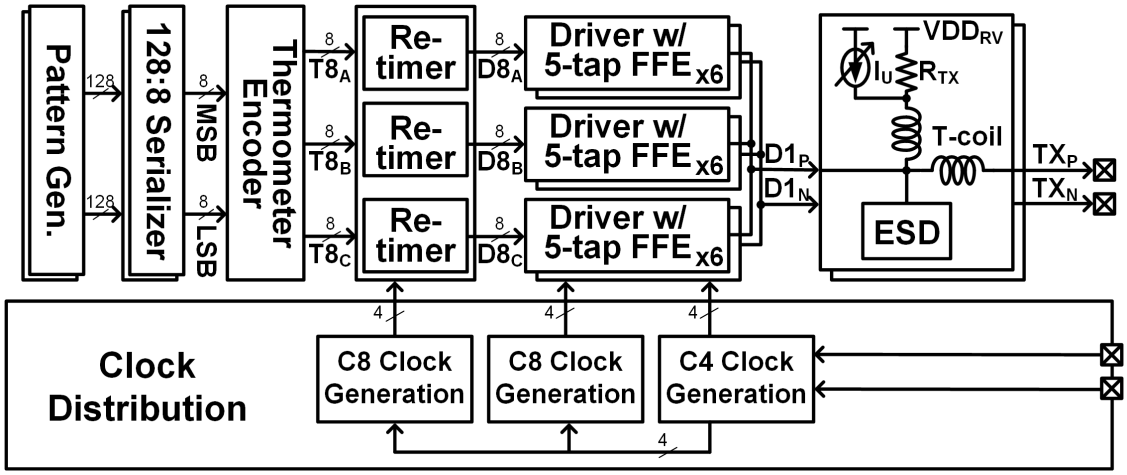


Figure 3.2: TX data path diagram and its requirements for clock distribution.

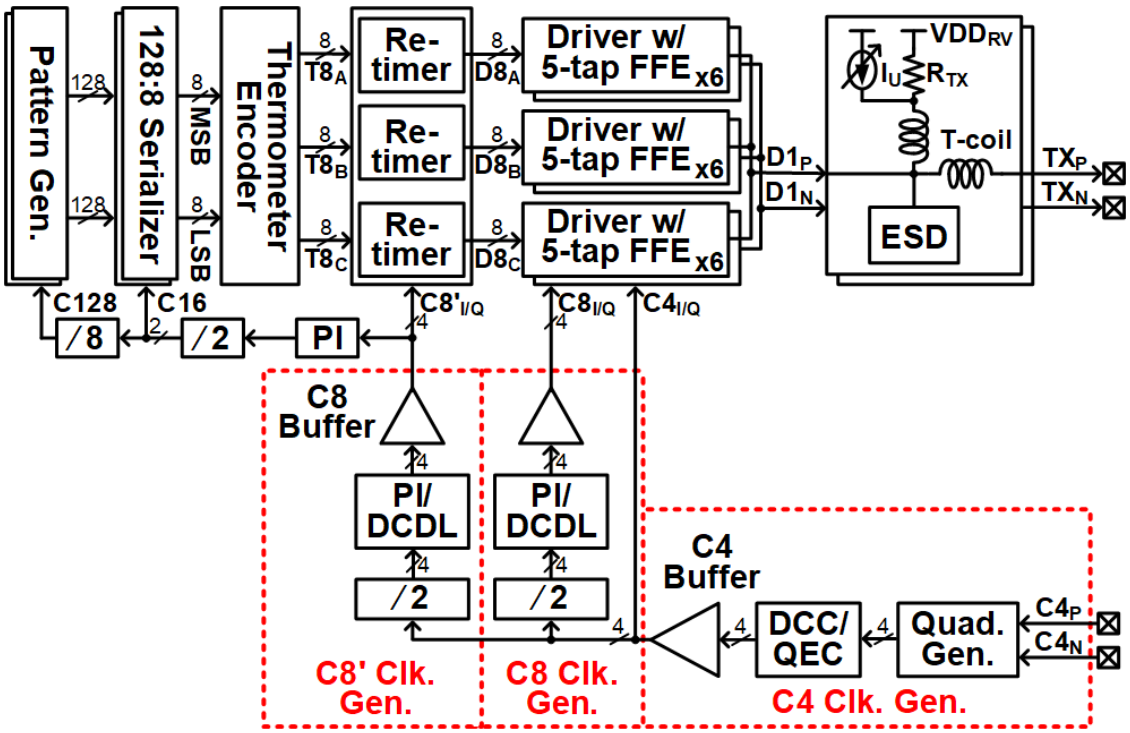


Figure 3.3: Block diagram of the C4 clock path and circuit details.

3.2 Implementation of Clock Distribution Network

Figure 3.3 shows the C4 clock generation, which receives a differential 25 GHz clocks followed by an injection-locked (IL) quadrature clock generator. The dedicated duty-cycle correction (DCC) and quadrature error correction (QEC) circuits are used to compensate duty-cycle distortion and quadrature errors. The data path receives the four-phase 25 GHz clocks ($C4_{I/Q}$) through a resonant clock buffer.

The C8 clock generation divides the outputs of the C4 clock generation and produce two pairs of four-phase 12.5 GHz clocks. Each pair of C8 clocks is distributed to the data path by C8 clock buffers through a phase interpolator (PI) and a digitally controlled delay line (DCDL), which serve as coarse/fine skew control to suppress the C8 quadrature errors and maximize the timing margins between clock domains.

Clock Path: C4 Clock Distribution

Fig. 3.4 shows the C4 clock distribution circuit. Firstly, the external differential clock is received through a TIA-based clock RX to match the 50 Ω transmission line impedance and determine the output common-mode voltage. The quadrature clock is generated with an open-loop injection-locked quadrature clock generator, which consists of 4 stages of cas-

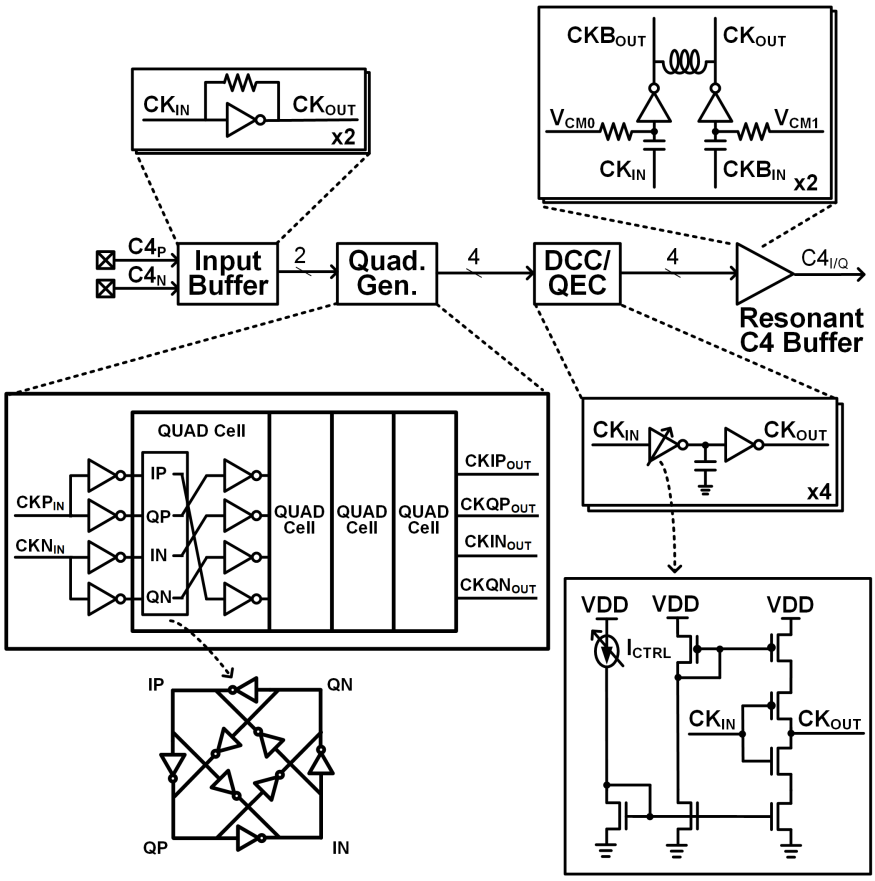


Figure 3.4: Block diagram of the C4 clock path and circuit details.

caded I/Q clock correlators [36]. The I/Q error is <0.91% at 30.37 mW. The phase noise is approximately -134.18 dBc/Hz at 1MHz offset. The residual I/Q phase errors of the quadrature clock are corrected by a current-controlled delay line [37] driven by a 7-bit current DAC. From post-layout simulation, we observe that the delay line provides a 1.4 ps tuning range at a maximum step size of 53 fs. This is enough to minimize the deterministic jitter at the 4:1 MUX introduced from clock distribution. Finally, two resonant clock buffers are adopted to drive the load capacitance of the 4:1 MUX along the datapath. Inductors with $L = 142$ pH resonate with the total load capacitance, consisting of the input capacitance of the 4:1 MUX and routing parasitics at 25 GHz, to lower power consumption. The buffers in the final stage are ac-coupled, so the duty cycle errors of the output clock can be compensated by adjusting the input dc voltage. In post-layout simulations, the resonant buffer consumes 49.14 mW, which is approximately 60% of the buffer power when inductors are not used. Fig. 3.5 shows the 25 GHz duty cycle of the output clock versus input bias voltage under different corners and temperatures in post-layout simulation.

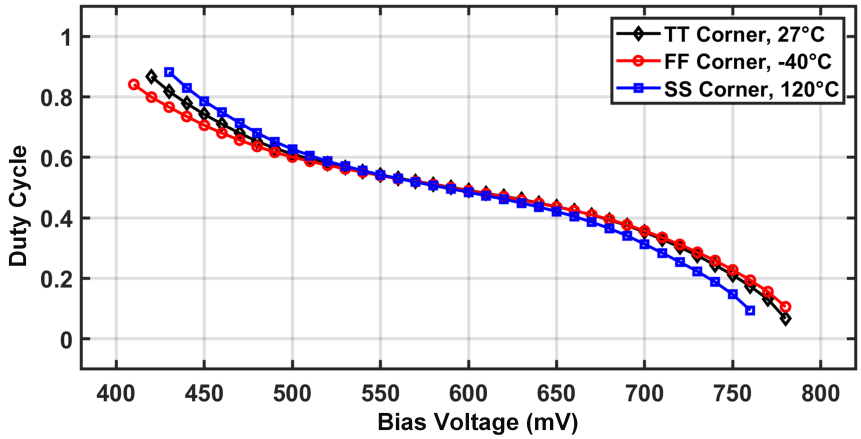


Figure 3.5: Simulated C4 clock duty cycle versus input bias voltage under different corners and temperatures.

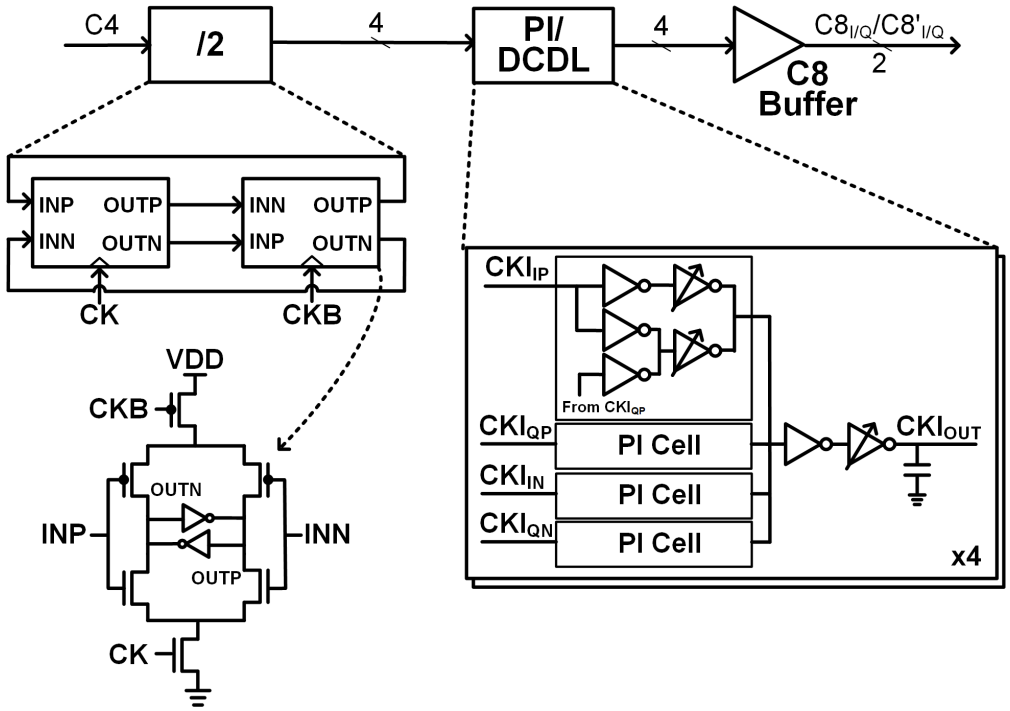


Figure 3.6: Block diagram of the C8 clock path and circuit details.

Clock Path: C8 Clock Distribution

To accommodate the delay across the 8:4 MUX, the 4:1 MUX, and the local clock buffer in the TX segments across PVT corners and to leave sufficient margin for the final 4:1

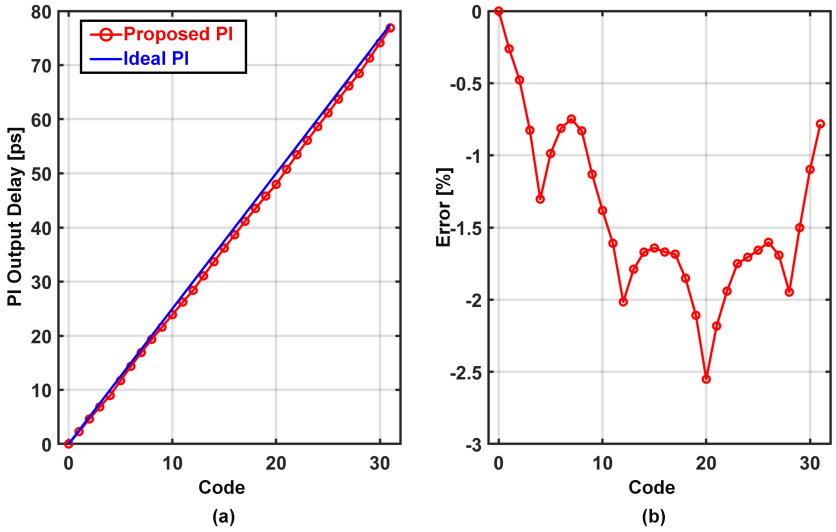


Figure 3.7: (a) PI output delay versus ideal and (b) their percentage errors.

MUX, the C8 and C8' clock paths are designed with flexible delays. First, the C4 clocks go through a C^2MOS frequency divider, which can operate at 25 GHz across PVT corners and provide a large output swing to avoid the use of an extra CML-to-CMOS circuit. The divider consumes 8.93 mW of power in post-layout simulation. The divided clocks are then applied to an 5-bit inverter-based PI [38]. To improve the linearity, in the first stage, the 8-phase clocks are generated from the I/Q clocks, and the interpolated clocks are subsequently generated in the second stage. As shown in Fig. 3.7, the two-stage PI increases linearity, with a maximum error of ∼2.5% observed in post-layout simulation. To achieve a finer resolution and remove quadrature error, the current-controlled delay line, which has a resolution of 175 fs and a 4.6 ps tuning range, is used. Ac-coupled buffers, similar to the ones used in the C4 clock distribution but excluding resonant inductors, are applied to drive the data path. Additionally, the duty cycle error can be adjusted via the input dc voltage, as in the case of the C4 buffer.

3.3 Circuit Generation

The proposed TX is primarily designed using BAG. Only top-level integration and the design of a handful of blocks, including ESD diodes and clock distribution wires, is done manually. First, Python-based layout generation scripts are written to describe circuit instance placement, routing, and/or power grid filling. These scripts extend the *XBase* layout engine [16] using different layout templates such as *TemplateBase*, *AnalogBase*, *DigitalBase*, etc. The schematic generators are implemented with programmable device sizes. Utilizing process-specific input parameters associated with the grid, routing tracks, and device sizes, the layout

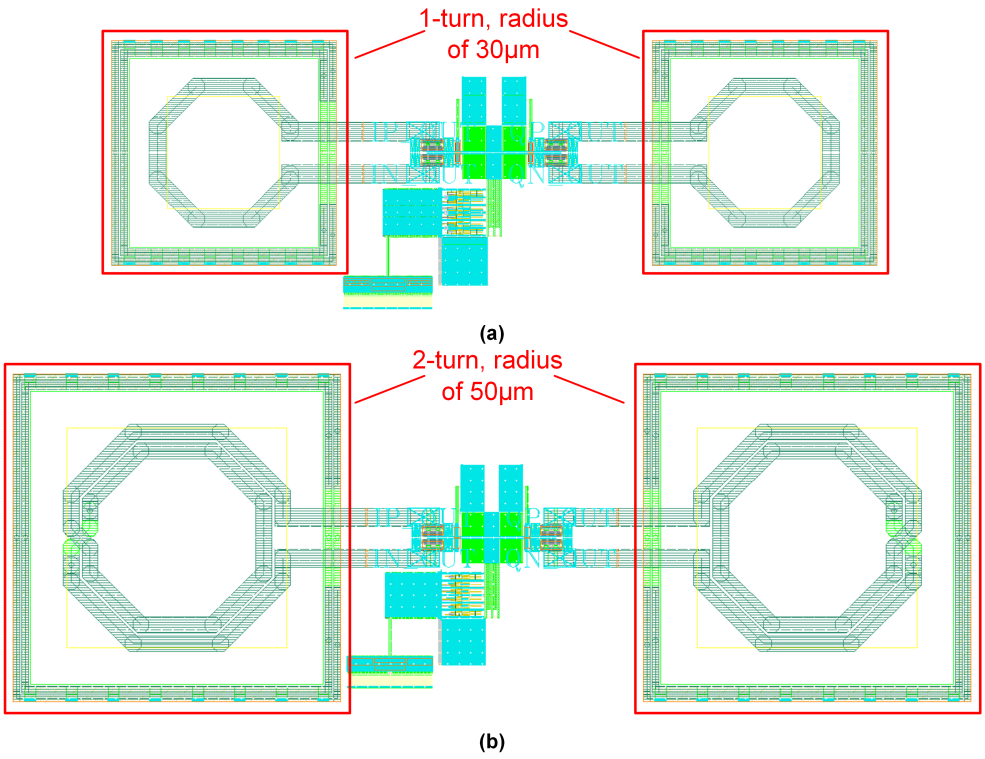


Figure 3.8: C4 clock distribution layouts using (a) 1-turn inductor of radius 30-μm and (b) 2-turn inductor of radius 50-μm.

and schematic generators produce DRC- and LVS-clean layouts.

In the generator design flow, the specifications and initial input parameters of the blocks and sub-blocks are derived from top to bottom. Then, the block-level designs are generated with BAG and extracted and verified manually to check whether specifications are satisfied. Iterations involving input parameter resizing, schematic and layout regeneration, and post-layout design simulation are performed until the design specifications are met. Finally, the generated block instances are combined to produce a top-level instance that satisfies all specifications. Because the time to regenerate a layout and schematic with modified sizes is less than 5 minutes, design iterations using this flow are only limited by simulation time. Fig. 3.8(a) and (b) show two C4 clock distribution layouts with a 1-turn inductor of radius 30-μm and 2-turn inductor of radius 50-μm, respectively, demonstrating the flexibility and effectiveness of the layout generator.

Fig. 3.9 shows the hierarchy and flow of the TX design using the *XBase* layout engine. The schematic and layout generators fetch the design parameters and sizes to generate the schematic and layout for each block. For example, the schematic and layout of C8 clock generator are generated and extracted by running the BAG script. Post-layout simulations

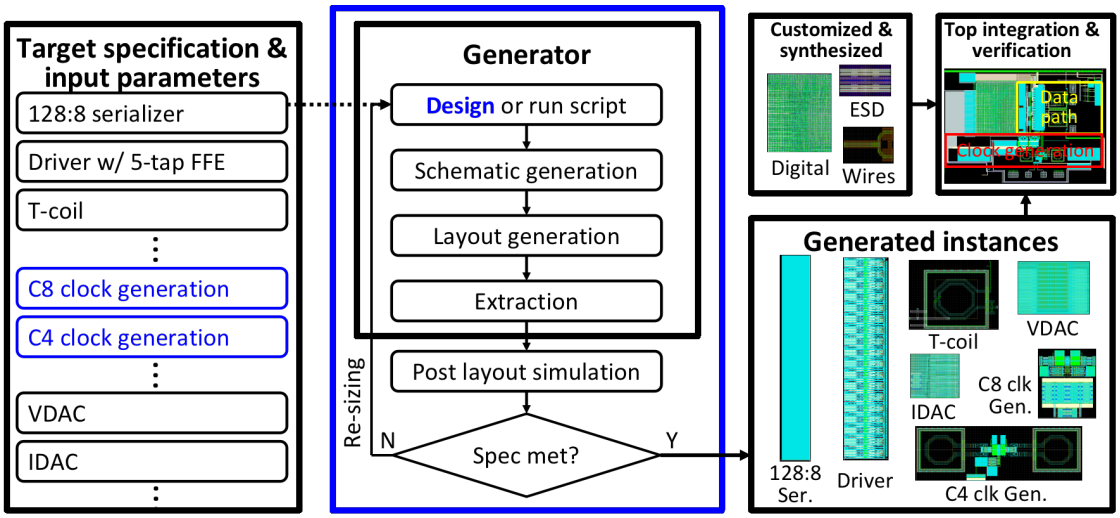
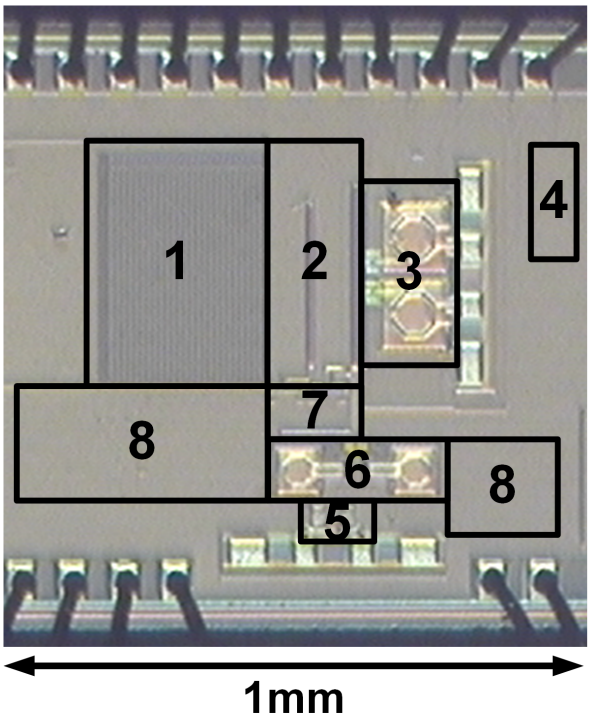


Figure 3.9: Design flow of the proposed TX with BAG.

Table 3.1: Layout generator summary for C8 clock generator.

Lv. 1	Lv. 2	Lv. 3	Lv. 4	Lv. 5	Lines of code
VCO					217 (layout) + 1392 (generator)
	Inductor				3032 (layout) + 365 (generator)
	VCO Core				1584
		CapDAC			515
			CapDAC Unit		216
				Cap Switch	289 (layout) + 114 (generator)
				MOM Cap	398 (layout) + 233 (generator)
		Varactor			269 (layout) + 264 (generator)
		Cross-Coupled Pair			193
		Current Mirror			347
		Decouple Cap			--

are performed, and the input parameters are adjusted until the bandwidth and rise/fall times meet requirements. Using a similar procedure, the high-level blocks are generated, such as the 128:8 serializer, 4:1 MUX and driver, T-coil, C4 and C8 clock distributions, current DAC, and voltage DAC. Finally, the customized blocks, digital design, and generated layouts are merged manually to produce the proposed top-level TX. Table 3.1 uses a C8 clock generator as a example to summarize the hierarchy and the number of lines for each levels.



	Block	Layout
1	Pattern Gen+ Digital	Synthesized
2	TX Data Path	BAG
3	Output Network	BAG
4	FFE Bias Circuit	Custom + BAG
5	Clock Receiver	BAG
6	C4 Clock Dis.	BAG
7	C8 Clock Dis.	BAG
8	VDACs + IDACs	BAG
	Top	Custom

Figure 3.10: Die photo and layout details.

3.4 Measurement Results

The two prototype TXs (with and without ESD protection diodes) were fabricated in a 28nm planar CMOS technology. The TX occupies an active area of 0.4323 mm^2 (Fig. 3.10). Fig. 3.11 shows the measurement setup. The output of the Keysight E8257D clock signal source is connected to a balun to generate the differential clock. This clock is fed to the chip via test probes. The chip's output data, also retrieved using test probes, is fed to the headers of the Keysight 86118A module through a dc block. The total channel loss through the probes, cables, dc blocks and limited bandwidth of the sampling scope header is approximately 6 dB.

Fig. 3.12 compares the 25GHz clock from signal generator and 50GHz clock pattern from the TX output, showing merely 8fs extra measured jitter from the clock distribution circuit.

Fig. 3.13 shows the data eye diagrams when applying PRBS7 patterns without and with ESD protection. Without ESD protection, the TX achieves a data rate up to 100 Gb/s using an NRZ pattern (Fig. 3.13(a)) and 200 Gb/s using a PAM-4 pattern (Fig. 3.13(c)). Due to the ESD capacitance, the TX with ESD protection achieves a data rate up to 180 Gb/s using a PAM-4 pattern (Fig. 3.13(d)). We also show that the data rate is 90 Gb/s when using the NRZ pattern (Fig. 3.13 (b)). The coarse and fine FFE coefficients for different scenarios are

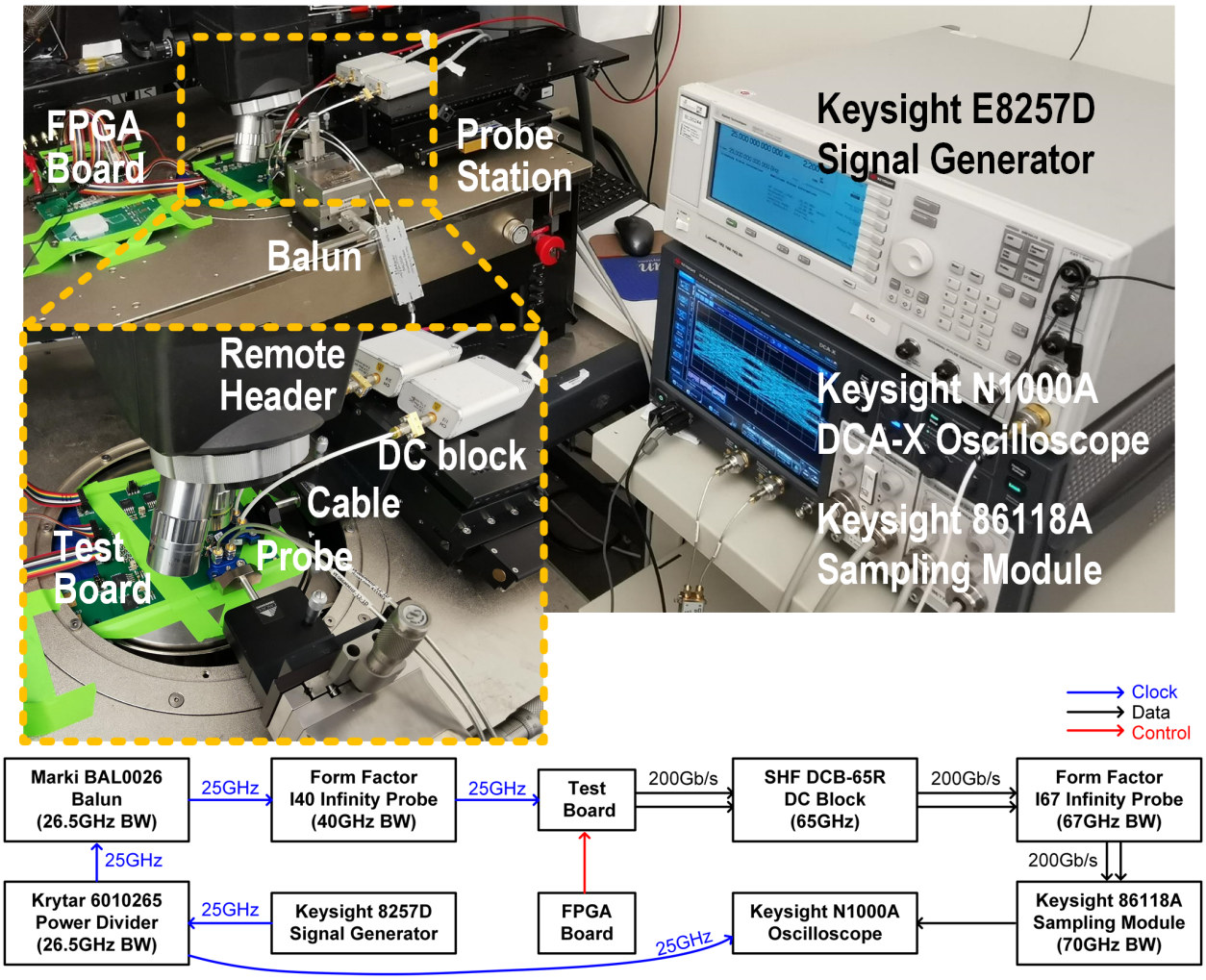


Figure 3.11: Measurement setup.

also indicated under the eye diagrams. The level mismatch ratios (RLM) of the PAM-4 eye diagrams are 98.4% and 98.2% respectively, meeting the requirement of >95% specified by relevant standards [39], [40]. As shown in the FFE coefficients of Fig. 3.13, under different scenarios, the re-configurable FFE provides flexibility to change the FFE from having one main-tap with one pre-tap and one post-tap to having one main-tap and two post-taps. This allows the FFE to accommodate different channels and data patterns, while maintaining the best performance.

Fig. 3.14 shows the power breakdown of the chip based on post-layout simulation, in which the FFE segments, C8 clock distribution, and C4 clock distribution consume approximately 46.4%, 22.9%, and 18.5% of the total power, respectively. Finally, Table 3.2 compares this article with the recently reported PAM-4 TXs operating above 100 Gb/s. With a planar

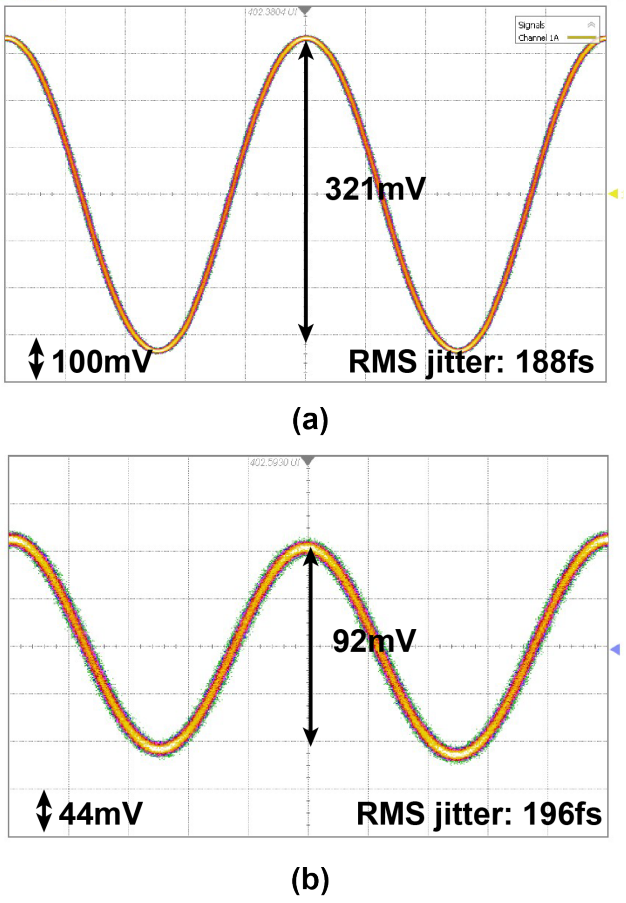


Figure 3.12: Comparison of (a) the 25 GHz clock from signal generator and (b) 50 GHz clock pattern from TX output.

CMOS technology, the proposed TX achieves the highest data rate with reasonable energy efficiency.

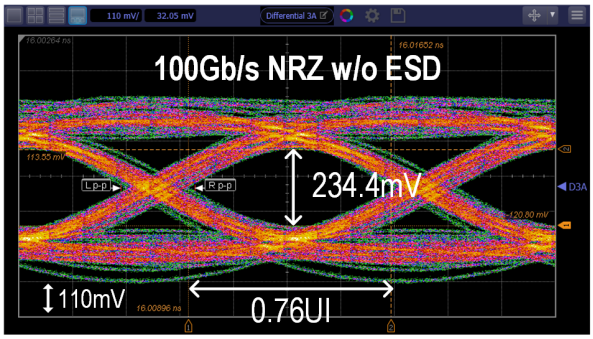
3.5 Summary

A flexible clock distribution network for a 200$Gbps$ pulse amplitude modulation four-level transmitter is designed using the layout generators in 28nm CMOS technology. The proposed TX achieves an eye opening with $> 52.9mV$ eye height, $0.36UI$ eye width, 98% RLM and $4.63pJ/b$ at 200$Gbps$ PAM-4 signaling under $> 6dB$ channel loss at $50GHz$, demonstrating the effectiveness of the clock distribution circuit.

Table 3.2: TX performance comparison

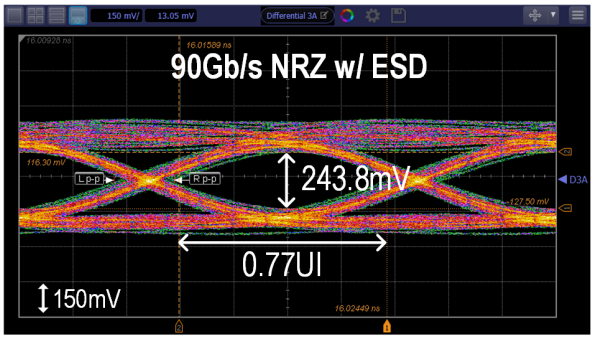
	JSSC'19 [5]		JSSC'19 [6]		ISSCC'18 [7]		ISSCC'21 [8]	ISSCC'20 [12]	ISSCC'21 [41]	This Work			
Technology	14nm		10nm		14nm		7nm	40nm	10nm	28nm			
Architecture	Quarter-rate		Quarter-rate		Quarter-rate		Quarter-rate	Quarter-rate	Quarter-rate	Quarter-rate			
Clock Source	External		On-chip		External		External	External	On-chip	External			
Output Swing w/o FFE (V_{ppd})	1		0.75		0.92		N/A	0.56	1.0	0.8			
FFE	3-tap		3-tap		8-tap		8-tap	8-tap	8-tap	5-tap			
ESD Protection	Yes		Yes		Yes		Yes	No	Yes	No		Yes	
Signaling	PAM-4	NRZ	PAM-4	NRZ	PAM-4	NRZ	PAM-4	NRZ	PAM-4	PAM-4	NRZ	PAM-4	NRZ
Data Rate (Gb/s)	128	64	112	56	112	56	112	100	224	200	100	180	90
Efficiency (pJ/bit)*	1.3	2.7	1.72	3.44	2.6	5.2	1.40	6.19	2.11	4.63	9.26	4.59	9.18
Eye Height (mV)	100**	240**	30	260	90**	170**	59	73	90	53	234	43	244
RLM	98.6%	N/A	98.5%	N/A	N/A	N/A	96.5%	N/A	99%	98.4%	N/A	98.2%	N/A
Active Area (mm^2)	0.048		0.0302		0.095		0.032	0.504	0.088	0.432			

*Excluding PLL and including DSP
**Estimated from eye-diagram



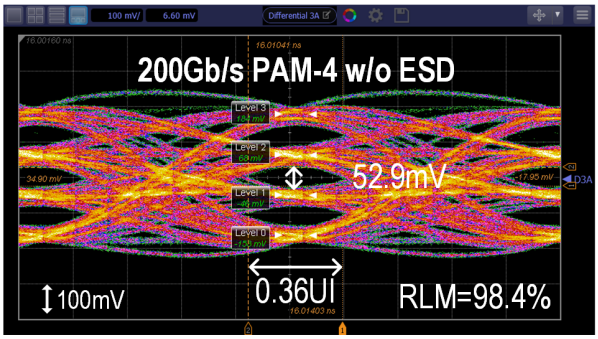
Coarse FFE (Segments): [3/18, 9/18, 6/18]
Fine FFE (DAC code): [48, 127, 38]
Polarity: [-1, +1, -1]

(a)



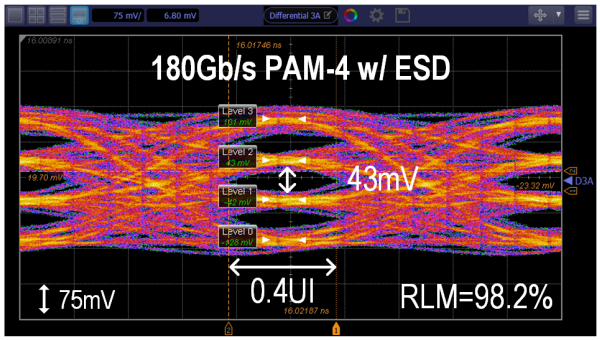
Coarse FFE (Segments): [13/18, 4/18, 1/18]
Fine FFE (DAC code): [117,127, 117]
Polarity: [+1, -1, -1]

(b)



Coarse FFE (Segments): [3/18, 9/18, 6/18]
Fine FFE (DAC code): [58, 127, 48]
Polarity: [-1, +1, -1]

(c)



Coarse FFE (Segments): [3/18, 9/18, 6/18]
Fine FFE (DAC code): [58, 127, 63]
Polarity: [-1, +1, -1]

(d)

Figure 3.13: Measured NRZ and PAM-4 eye diagrams w/o and w/ ESD.

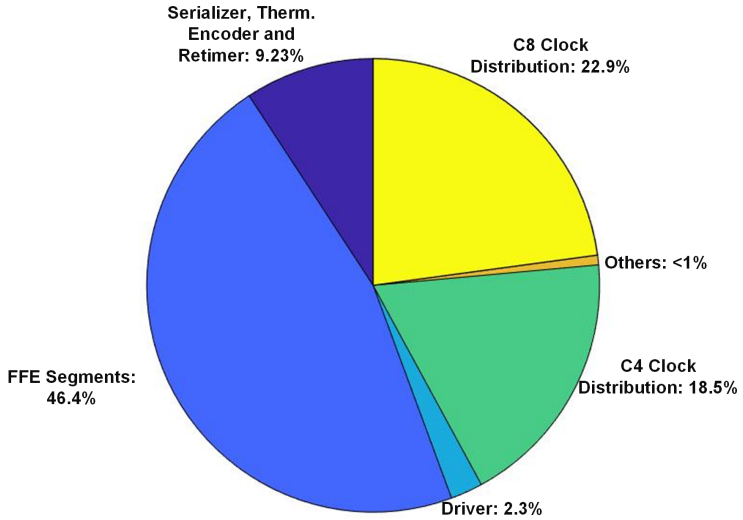


Figure 3.14: Power breakdown based on post-layout extracted simulations.

Chapter 4

Sub-100fs PLL Design for 200Gb/s PAM-4 SerDes Transmitter

4.1 PLL Specification for High-Speed SerDes TX

With the increase of data rate, if the modulation scheme (NRZ, PAM-4, and PAM-8, etc) is fixed, the most significant difference lies in the reduction of 1-UI time width. When the data rate of each generation doubles, the time width decreases by two times. For example, 1-UI of the $50GBaud/s$ data rate is $20ps$, however, when the data rate becomes $100GBaud/s$, the 1-UI is only $10ps$, which cause extremely requirement to jitter of clock generation (PLL) and distribution, and ISI of data path.

To discuss the phase noise transfer function of a CDR from data input to data output, Figure. 4.1 shows a example of a VCO-based CDR and its model [42],[43]. The clock output of the CDR is at the VCO output, while the data output of the CDR rests in the PD, where the input data is sampled by the output clock. So the jitter transfer from the data input DIN to data output $DOUT$, called output jitter transfer fuction (OJTF) or jitter tracking, which is

$$\begin{aligned} OJTF &= \frac{\phi_{dout}}{\phi_{din}} = \frac{1}{1+LG(s)} \\ &= \frac{s^2 \cdot \frac{C}{K_{PD}I_{CP}K_{VCO}}}{1+sRC+s^2 \cdot \frac{C}{K_{PD}I_{CP}K_{VCO}}} \end{aligned} \tag{4.1}$$

which is a high-pass filter with corner frequency of $\sim K_{PD}I_{CP}K_{KVCO}R$, where K_{PD} is the gain of PD, I_{CP} is the current of the charge pump, K_{VCO} is the sensitivity of the VCO, R and C are the resistance and capacitance of the resistor and capacitor in the loop filter and $LG(s)$ is the loop gain of the CDR loop.

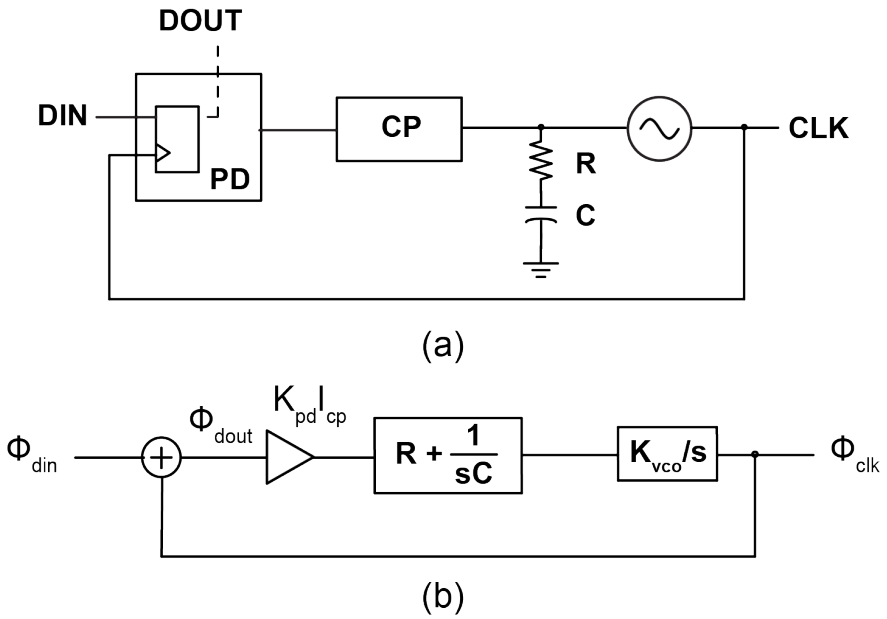


Figure 4.1: (a) CDR example and (b) model.

Then, for a SerDes transceiver system (Figure. 4.2) with TX PLL, RX PLL and RX CDR, where the loop bandwidths of TX and RX PLL are $f_{PLL,TX,3dB}$ and $f_{PLL,RX,3dB}$, and the loop bandwidth of RX CDR is $f_{CDR,RX,3dB}$. As the generated phase noise in a PLL is low-pass, the whole transfer function from PLL to CDR is a band-pass characteristic.

From the interpolation of CEI-56 [44] and IEEE802.3bs [45] specifications, the jitter requirement of TX is that the randomn jitter (RJ) has to be less than $0.01UI_{pp}$ or $100fs$ for $100GBaud/s$ signaling, after a $10MHz$ clock and data recovry (CDR) filter. Considering other jitter contributions on clock distribtution path, such as clock buffer, quadrature generation, quadrature error correction, and duty cycle correction, we set the jitter target of the PLL at TX being $< 100fs$ integrated from $1KHz$ to $100MHz$.

4.2 High Performance PLL Overview

Different PLL architectures have been proposed for different kinds of purposes. The bang-bang PLL in Chapter 2 offers excellent power efficiency due to its simplicity, however, the in-band limited-cycle jitter or quantization noise from the bang-band PD or 1-bit TDC limits the phase noise performance. In the traditional PFD based PLL [24] (Figure. 4.4(a)), the PFD provides a linear transfer function and large frequency locking range, making it suitable for an analog PLL. However, the CP noise dominates the in-band phase noise, and the capacitor in the loop filter consumes large area.

The CP noise contribution can be reduced by increasing the PD gain, which is used in

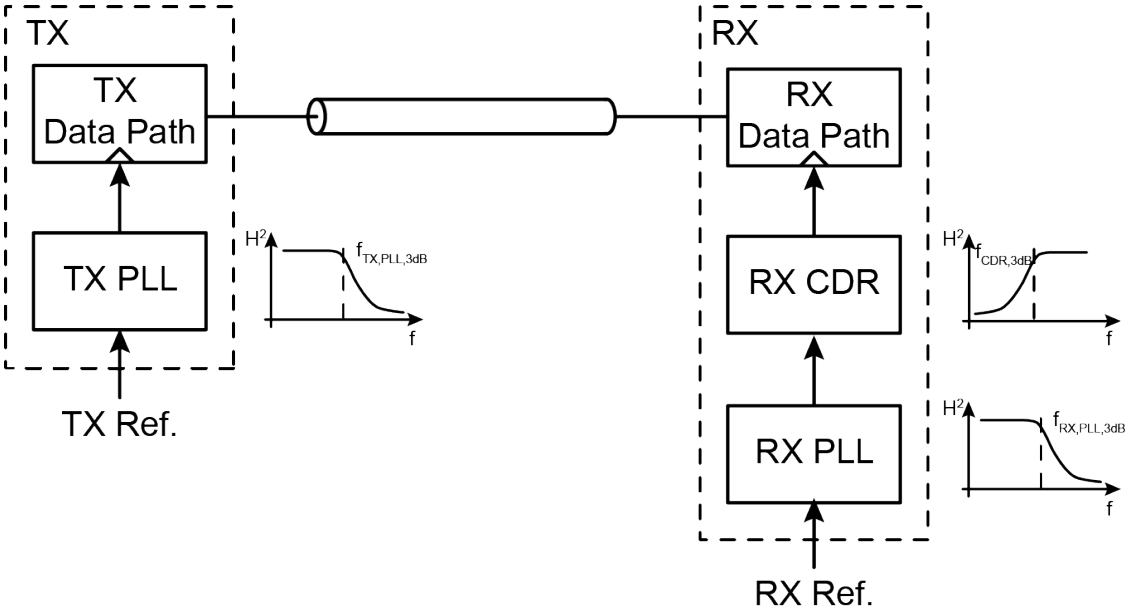


Figure 4.2: Transceiver system with TX PLL, RX PLL and RX CDR.

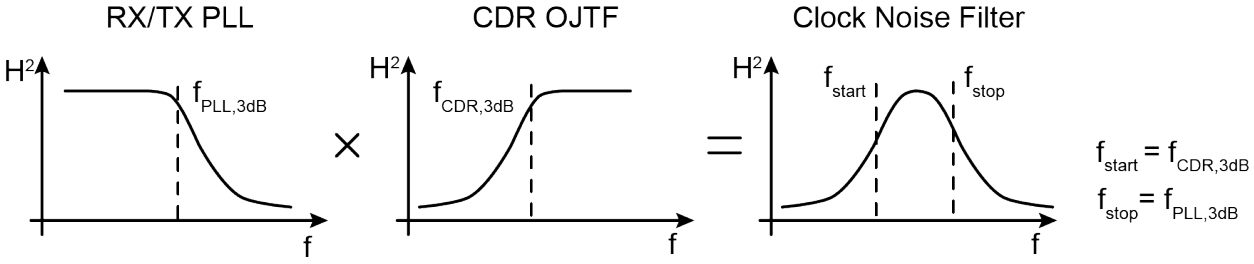


Figure 4.3: Clock phase noise filter with PLL and CDR.

the sub-sampling PLL (SSPLL) [46], [47], sampling PLL (SPLL) [48]. With the same loop as Figure. 4.4(b), the transfer function of CP is

$$\begin{aligned} H_{cp}(s) &= \frac{\phi_{dout}}{\phi_{din}} = \frac{G_{cp}(s)}{1+LG(s)} \\ &= \frac{LG(s)}{1+LG(s)}\frac{N}{K_{pd}I_{cp}} \end{aligned} \tag{4.2}$$

From 4.2, when increasing K_{pd} by M times, the CP noise gain will decrease by M^2. This helps to reduce the total CP phase noise contribution, even with the loop bandwidth increasing. For the sub-sampling PLL, the performance is even better by removing the clock divider,

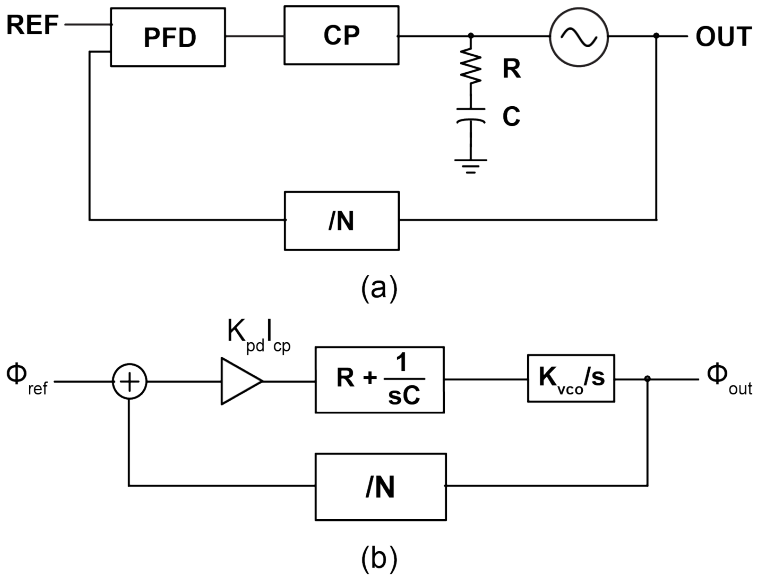


Figure 4.4: (a) PFD based PLL and (b) model.

making N in 4.2 being 1. However, the reference feedthrough at the sampling PD will affect the VCO and increase the spur of the PLL output [46], [47], which requires careful design, such as clock buffer between VCO and SSPD.

Another potential architecture is injection-locked PLL (ILPLL) [49] or injection-locked frequency multiplier (ILFM). The ILPLL relies on injection-locking VCO which is locked to the reference clock. However, as the frequency division ratio is large, the frequency locking range is small, which requires a extra frequency locking loop to pull the VCO frequency near enough. Due to the injection locking nature, the ILPLL also suffers from spur coming from the reference coupling.

The digital time-to-digital (TDC) based PLL [50] offers flexibility to apply digital signal processing (DSP) in LF, which eliminates the large capacitor and scales with the advanced technology. However, the trade-off between quantization noise of the TDC and resolution, which is related to power and area, requires careful TDC design and optimization.

In summary, we can find that in all the PLL architectures, the VCO dominates the out-band phase noise, while the other components such as reference clock, PD, CP, clock divider dominates the in-band phase noise, in spite of the phase locking scheme is base on phase detection or injection-locking. In the PLL design, the loop bandwidth is the critical parameter to leverage the VCO phase noise contribution against the contribution of other components.

Due to the jitter requirements and design complexity, in this 200Gb/s PAM-4 SerDes TX, we adopt SSPLL to generated clock with RMS jitter $< 100fs$. A hybrid loop is applied to

eliminate the integral capacitor of the LF to save area and increase flexibility, and a tri-state integral path is used to relax the demand of a high-resolution DAC and ensure the low-jitter performance.

4.3 SSPLL and Hybrid SSPLL

Figure. 4.5(a) shows the the diagram of the SSPD [46], where the reference clock sample the VCO clock directly with two cascading switches. Figure. 4.5(b) shows the transfer function between the input phase difference of the two clocks ϕ_{in} $(= \phi_{vco} - \phi_{ref})$ and the output voltage. As shown in Figure. 4.5(c), at the locking state, the switch samples the center of the VCO, which generates a voltage equal to V_{DC}. However, if the reference clock is early, the sampling point is ahead of the locking point, and the output voltage is lower than V_{DC}. Otherwise, the output voltage is higher than V_{DC}. Therefore the SSPD output is approximately a scaled replica of the VCO clock waveform, if we sweep the reference clock phase while fixing the VCO clock phase.

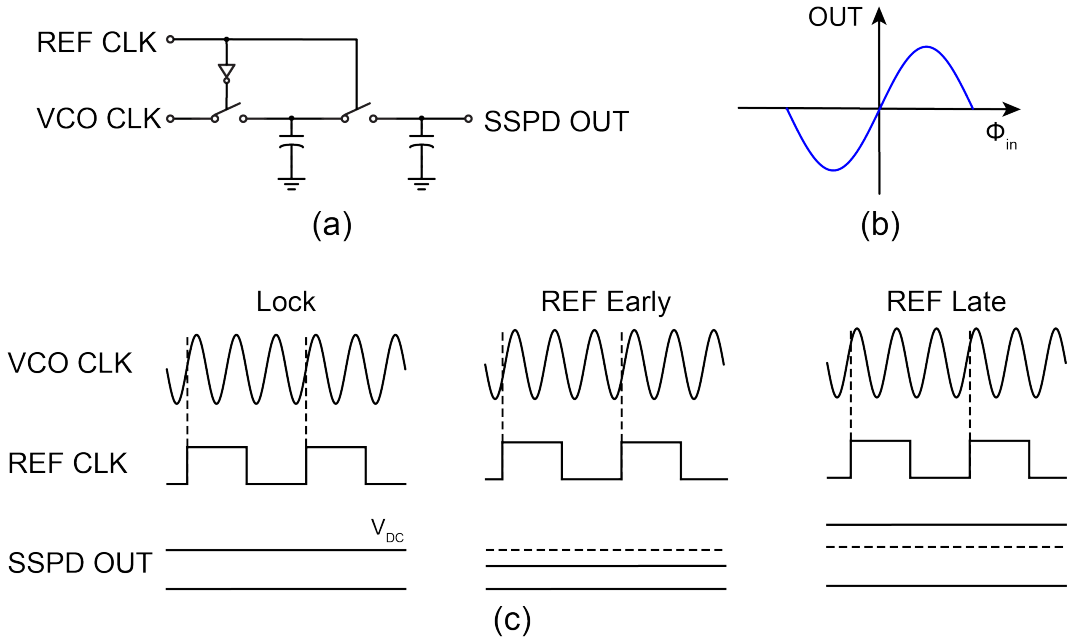


Figure 4.5: SSPD (a), its transfer function (b) and timing diagrams (c).

As the SSPD output voltage is just DC voltages, the corresponding sub-sampling charge pump (SSCP) can be just a open-loop operational transconductance amplifier (OTA), which transfer input voltage to output current. This structure makes the SSPLL immune to SSPD and SSCP mismatches and offsets, as the fixed offsets voltage will map to a fixed phase difference between the reference clock and the VCO clock. As long as the phase difference and gain deviation is small, the PLL loop characteristic is unaffected.

One problem embedded in the SSPD is that, the PD behaves exactly same way with any VCO clock whose frequency is a multiple of reference clock frequency. For example, the diagram in Figure 4.5 shows the VCO clock frequency is three times of the reference frequency. If we change the multiplier to two, the lock state, the reference early state and the reference late state would be identical.

The problem can be addressed with a traditional PFD with dead-zone. As shown in Figure 4.6, two FFs sample the outputs of the PFD (UP_{LIN} and DN_{LIN}) and get UP_{DZ} and DN_{DZ}. Figure 4.7(a) shows two cases of phase locking. When the time difference T_d between CLK_{REF} and CLK_{DIV} is larger than the half of the clock period T, the sampling results is high. Otherwise the sampling result is low. So there is a dead zone between $-\frac{T}{2}$ and $-\frac{T}{2}$ the transfer function between input phase (ϕ_{in}) and output voltage ($UP_{DZ} - DN_{DZ}$), as shown in figure 4.7(b).

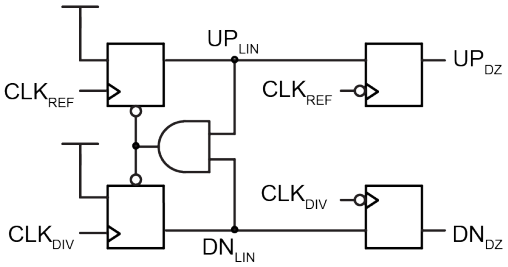


Figure 4.6: (a) Dead-zone PD and (b) timing diagrams.

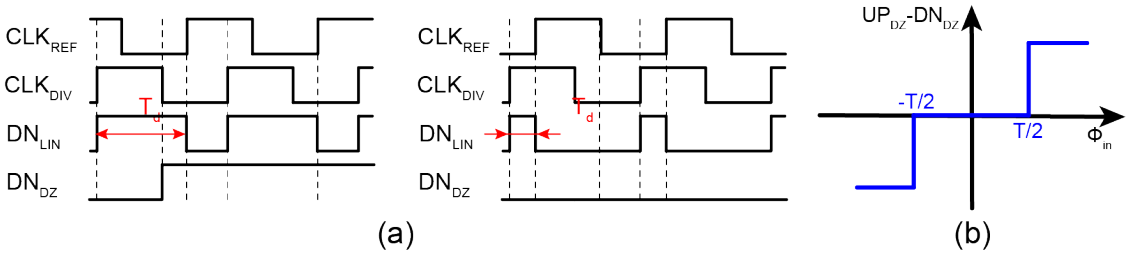


Figure 4.7: Phase locking (a) time diagrams and (b) transfer function.

However, by integrating the frequency difference, the phase difference can be large enough to change the output, as shown in the frequency locking diagram (Figure 4.8 (a)). Figure 4.8(b) presents a bang-bang or binary frequency-locking characteristic between input frequency (f_{in}) and output voltage ($UP_{DZ} - DN_{DZ}$). Therefore, this DZPD can be used to help the SSPD for frequency locking, without affecting the phase locking process.

Combining the SSPD and the DZPD with the SSCP and the traditional CP, the SSPLL looks like Figure 4.9, where the two charge pump currents sum together to driver the LF and control the frequency of the VCO, forming a type-II PLL. The output of the VCO is

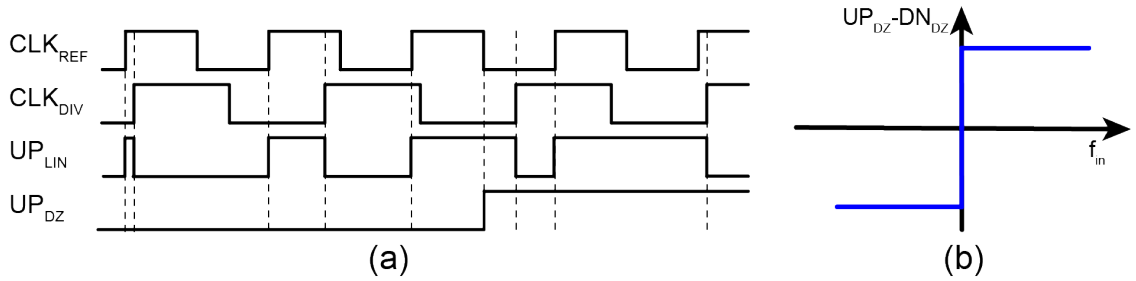


Figure 4.8: Frequency locking (a) time diagram and (b) transfer function.

followed by a clock buffer and goes through two paths. One path is constructed by the clock buffer directly connected to the SSPD, and in the other path, the buffer output is divided by the divider chain and then compared with the reference clock with the DZPD. During the normal operation, the loop is frequency locked and the DZPD and CP is ineffective, so the CP does not affect phase noise of the SSPLL output.

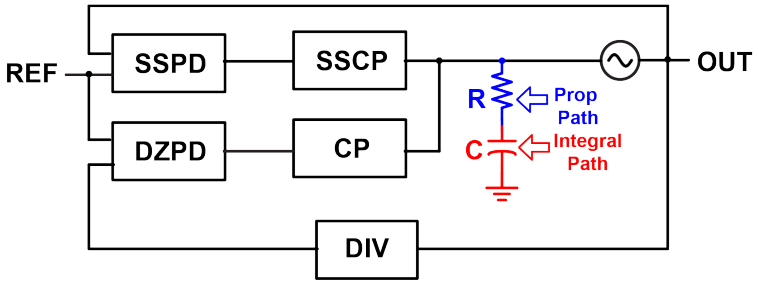


Figure 4.9: SSPLL with SSPD, DZPD, SSCP and traditional CP.

In the analog SSPLL above, the capacitor usually take fairly large area to set the loop bandwidth and guarantee the loop stability. However, the LF in Figure 4.9 can be split into two parts, where the resistor is the proportional path for the phase locking, and the capacitor is the integral path for the frequency locking. Therefore, the capacitor can be moved into digital domain to save the area, which also benefits from the technology scaling. Figure 4.10 shows the diagram of the hybrid SSPLL, where the SSPD and DZPD are connected to a comparator and FF, respectively. The digital outputs are summed together and filtered by the digital filter, which is followed by a voltage DAC to control the frequency of the VCO. Finally, the digital integral loop also offers flexibility to configure the PLL.

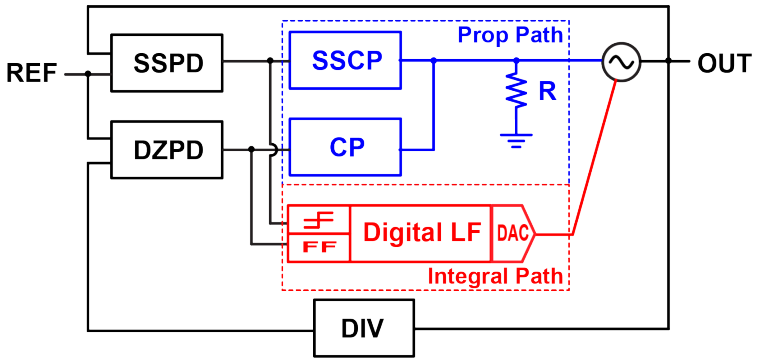


Figure 4.10: Hybrid SSPLL.

4.4 The Architecture of Hybrid Type-I SSPLL with Tri-State Integral Path

Due to the area limitation and layout generator written in BAG, the resolution of the DAC is less than or equal to 9. When simulating the hybrid SSPLL with the 9-bits DAC, there are ripples on the proportional control voltage and the integral control voltage of the VCO, as shown in Figure 4.11. The reason is that the 9-bits DAC is too coarse to control the VCO to get the exact frequency. So the integral DAC control have to jump between several frequency control near the target frequency continuously to reach the exact frequency on average. These ripples on the control and the proportional control create in-band spur on phase noise and spectrum, and increase the integrated RMS jitter. For example, in the transient simulation, the ripple voltages on proportional control and integral control are $41mV$ and $10mV$ respectively. This is also reflected on the SSPD output with a ripple of 54mV.

In a type-II loop, the difference of SSPD positive output and negative output will be integrated and reflect on the integral path. To make the integral output being stable, the difference should be 0. This is identical with the waveforms shown in Figure 4.11. When the PLL loop locks, the average voltage of proportional control is $\frac{VDD}{2}$ and the average voltage of SSPD differential output is zero.

To eliminate the ripple on the control voltages, we can rely on the proportional path to generate a offset voltage compared to $\frac{VDD}{2}$, which is corresponding to the offset voltage of SSPD differential output. As this offset voltage is analog, it can reach the exactly control voltage and frequency. In real implementation, the SSPD integral gain can be set to zero, or the SSPD integral path can be removed, which turns the PLL loop into a pure type-I loop (Figure 4.12).

Figure 4.13 shows the simulation results of the type-I SSPLL. By making the integral gain of the sub-sampling path being zero, the integral control converges to a constant value.

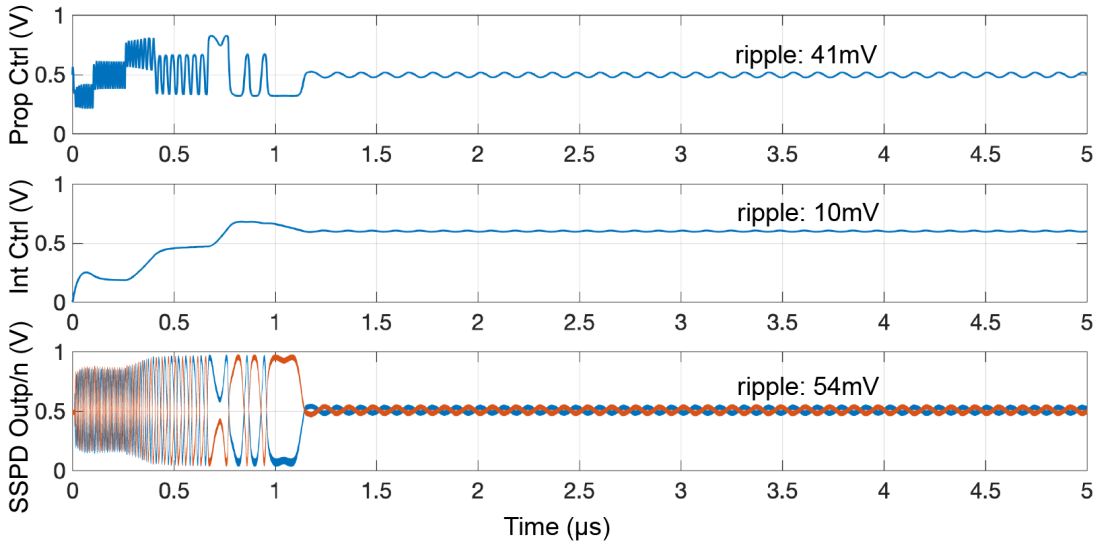


Figure 4.11: Simulation results of proportional control, integral control and CP inputs for the Hybrid SSPLL.

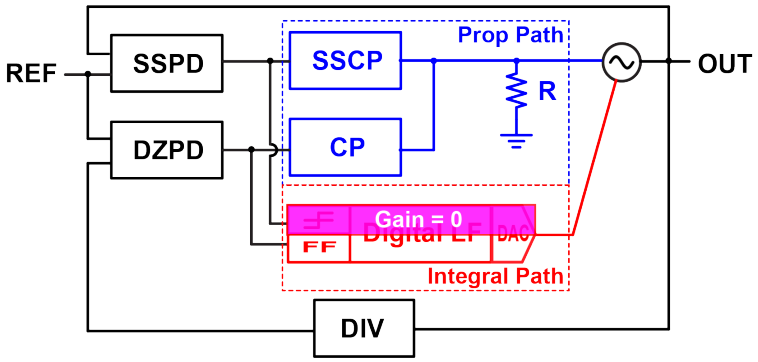


Figure 4.12: Type-I SSPLL.

However, there are situations that the frequency offset is too large, where the proportional ctrl and SSPD differential outputs saturate. Therefore, the SSPD and SSCP gain, and the loop characteristic are largely changed, causing the PLL loop out of lock. In this simulation, we can see the ripple on the proportional control and SSPD ouput are $350mV$ and $837mV$, respectively, which is larger than the type-II PLL.

To summarize so far, the type-II PLL have ripples on proportional control and integral control, due to the coarse DAC resolution of integral path. However, the situations that the proportional offset voltage is too large exist type-I PLL, causing the PLL out of lock. Therefore, we can combine the two cases, by creating a tri-state integral path, where in the middle region, the the loop is type-I, and out of this region, the loop is type-II. The type-II

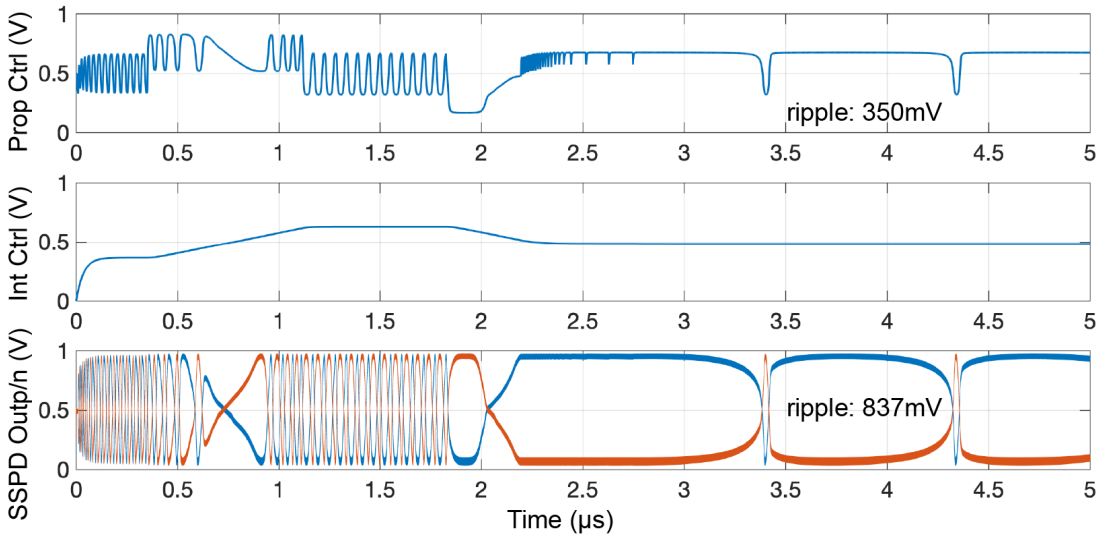


Figure 4.13: Simulation results of proportional control, integral control and CP inputs for the Type-I SSPLL.

state is to draw the frequency close enough with the integral path, so in the type-I state the proportional offset voltage is small enough and does not affect the loop characteristic.

We propose the architecture as Figure 4.14, where the SSPD connects to two comparators instead of one. While one comparator have positive offset V_{op}, the other comparator have negative offset $-V_{on}$. Therefore, if we label SSPD differential output with $SSPD_{out,diff}$, the outputs of the two comparators ($\{CMP0, CMP1\}$) are

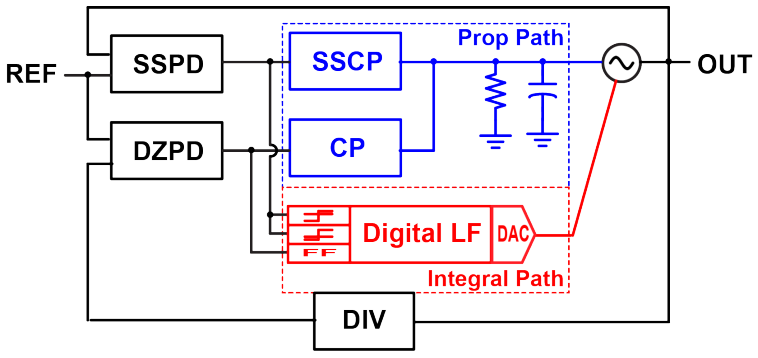


Figure 4.14: Type-I SSPLL with tri-state integral path.

$$\{CMP0, CMP1\} = \begin{cases} 00, & \text{if } SSPD_{out,diff} < -V_{on}; \\ 01, & \text{if } -V_{on} \leq SSPD_{out,diff} \leq V_{op}; \\ 11, & \text{if } SSPD_{out,diff} > V_{op}. \end{cases} \tag{4.3}$$

And the gain of the integral path in the three regions are

$$Gain_{int} = \begin{cases} -G, & \text{if } \{CMP0, CMP1\} = 00; \\ 0, & \text{if } \{CMP0, CMP1\} = 01; \\ G, & \text{if } \{CMP0, CMP1\} = 11. \end{cases} \tag{4.4}$$

which is a tri-state function for the integral path, with a zero-gain region or type-I loop in between, and type-II loop beyond the region. Figure 4.15 shows the simulation results with the SSPLL above. Before $2.4\mu s$, the type-II loop works to control the DAC control code and draw the frequency close enough. After that, the type-I loop starts to function, and the offset voltages of proportional control and SSPD differential voltage converges to $61mV$ and $148mV$ to make up the residual frequency. Due analog nature of the proportional loop, there is no frequency error and ripple on the control signals when the PLL is locked.

In this structure, we can note that the offsets of the comparators changes V_{on} and V_{op}, and affects the zero-gain region of the integral path. Generally, the offsets are small compared with V_{on} and V_{op}. For example, in this case V_{on} and V_{op} are around $150mV$, which provides enough margin for the offsets of the comparators. Furthermore, V_{on} and V_{op} are adjustable manually in the design.

Besides the type-I SSPLL with tri-state integral path, the other remedy is delta-sigma ($\Delta\Sigma$) modulator. Figure 4.16 shows the architecture of the type-II SSPLL with $\Delta\Sigma$ modulator. The $\Delta\Sigma$ modulator and the 9-bits make up a higher-resolution $\Delta\Sigma$ DAC, by pushing the quantization noise to higher band of the oversampled frequency, which is then filtered by a low-pass filter.

With a high-resulution DAC, the frequency error is largely reduced, and the ripples caused by the frequency error become smaller. Figure 4.17 shows the simulation results. The ripple on proportional control, integral control and SSPD outputs are $13mV$, $3mV$ and $20mV$, which is about three-times smaller than the type-II SSPLL.

4.5 Design and Implementation of the Reconfigurable Hybrid SSPLL

Figure 4.18 shows the design of a hybrid SSPLL, with reconfigurable integral path of type-II mode, type-I mode, type-I mode with tri-state integral path and type-II mode with $\Delta\Sigma$

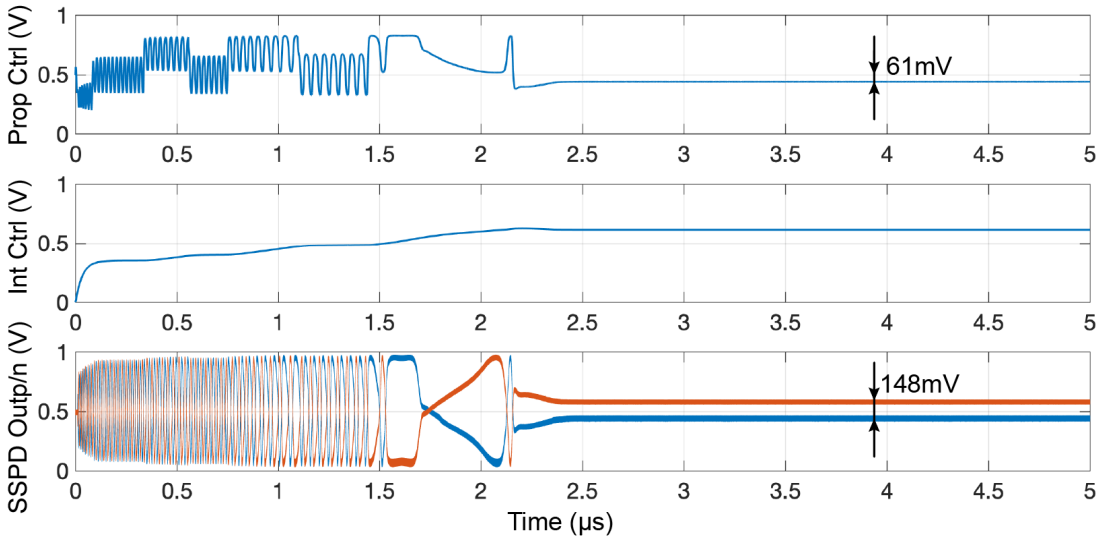


Figure 4.15: Simulation results of proportional control, integral control and CP inputs for the Type-I SSPLL with tri-state integral path.

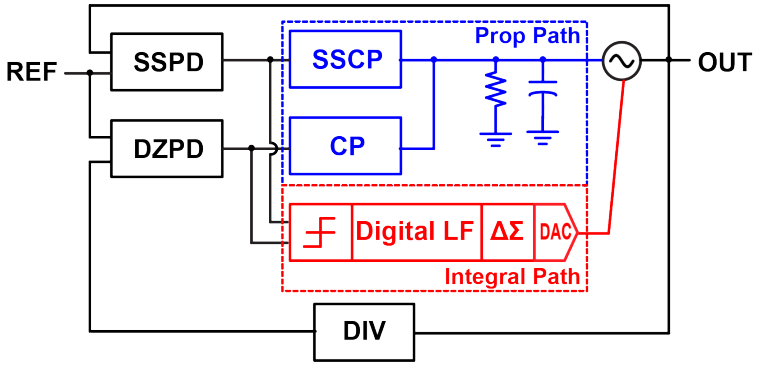


Figure 4.16: Type-II SSPLL with ΔΣ modulator.

modulator. In the PLL, the VCO drives a SSPD and connects to a C^2MOS divider, which is followed by static flip-flop (FF) based divider chain. The SSPD compares the phases of the reference clock and the VCO output phase directly, and drives a SSCP and a buffer to avoid the kick-back noise and clock coupling of the followed two comparators with independent offsets. The DZPD gets the difference of the referece clock and the divider chain output, and then drives a CP and a FF for synchronization. Besides the DZPD, a traditional PFD is also added for performance comparison. In the proportional path, the SSCP and the CP drive the analog loop filter include R_1 to provide a proportional gain, and R_2 and C to reduce the high-frequency ripple of the control line. In the reconfigurable integral path, the two comparators and the FF adds up with programmable gains, which is then filtered by digital

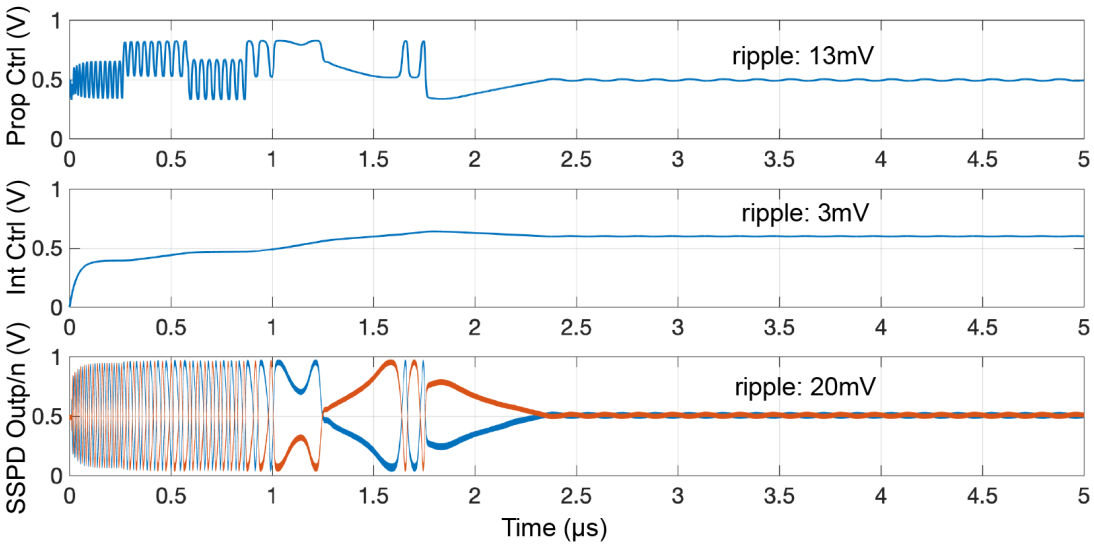


Figure 4.17: Simulation results of proportional control, integral control and CP inputs of Type-II SSPLL with ΔΣ modulator.

LF. The mode MUX chooses the output of the digital LF or the output of the ΔΣ modulator, and controls the VCO through a 9-bits DAC. The VCO is supplied by a low drop regulator (LDO) for performance comparison, which can be disabled and get the supply from external directly.

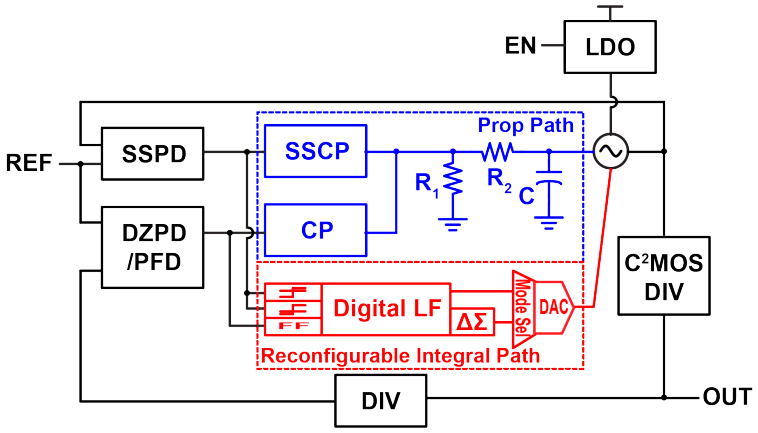


Figure 4.18: Reconfigurable Hybrid SSPLL.

Table 4.1 shows the PLL settings for different modes for performance comparison. When the SSPLL is in type-II mode, the offsets of the two comparators are 0 and the integral gain is non-zero, with the ΔΣ modulator being turned off. When the PLL is in Type-I mode, the gain of the integral path is set to 0. When the PLL is in type-I mode with tri-state integral

path, the two comparator offsets are set to $-V_{on}$ and V_{op} and the gain of the integral path is > 0. Finally, in the type-II mode with $\Delta\Sigma$ modulator, the settings are identical with type-II, except the $\Delta\Sigma$ modulator is turned on.

Table 4.1: SSPLL system settings.

Mode	Offset of Comparator 0	Offset of Comparator 1	Integral Gain	$\Delta\Sigma$ Modulator	Remark
Type-II	0	0	> 0	OFF	In-band spur
Type-I	0	0	$= 0$	OFF	Out of lock
Type-I with Tri-State Integral Path	$-V_{on}$	$-V_{op}$	> 0	OFF	No ripple and spur
Type-II with $\Delta\Sigma$ Modulator	0	0	> 0	ON	Noise of $\Delta\Sigma$ Modulator

VCO and Clock Buffer

Figure 4.19 shows the circuit diagram of the VCO and clock buffer. We applied a class-C architecture [51], [52] to reduce the conduction angle of the cross-coupled pair than conventional VCOs, by a higher efficiency of coverting current into fundermental harmonic. From a theoretical analysis, the class-C VCO will improve the phase noise by 3.9dB with the same current or reduce the current by 39% for the same phase noise level [53]. To further lower the second-harmonic noise from the tail current source, a inductor is added between the current source and the tail node of the cross-coupled pair, which resonates with the parasitic of sources of the two transistors and generate a high-impedance at the second harmonic [54]. Figure 4.20 shows the phase noise comparison results for the VCO without and with tail inductor. At frequency of $13.70GHz$, the tail inductor reduce the phase noise by $6.2dB$ at $1MHz$ offset.

To cover enough frequency range for PVT corner, a 4-bits Capactive DAC (CapDAC) is adopted in this design. In simulation, the CapDAC can tune the VCO frequency from $23.44GHz$ to $27.40GHz$. Then, a fine varactor is added after the CapDAC to cover the frequency band of the coarse tuning and provide enough frequency resoluton with a 9-bits DAC control, whose frequency tuning range is about $247MHz$. The proportional VCO-gain (K_{VCO}) is control by the proportional varactor, which affects the SSPD output voltage range. In this design, the K_{VCO} of the proportional path is around $55MHz/V$. Figure 4.21 shows the layout of the VCO and buffer, in which the inductors, CapDAC, varactors, cross-coupled pair, current mirror and buffer are labeled.

As the DC voltage of the VCO output is the supply voltage, the ac-coupling capacitor and self-biased buffer or trans-impedance amplifier (TIA) are used to shift the DC voltage to half VDD. The transistors in the TIA are sized based on the capacitive load after.

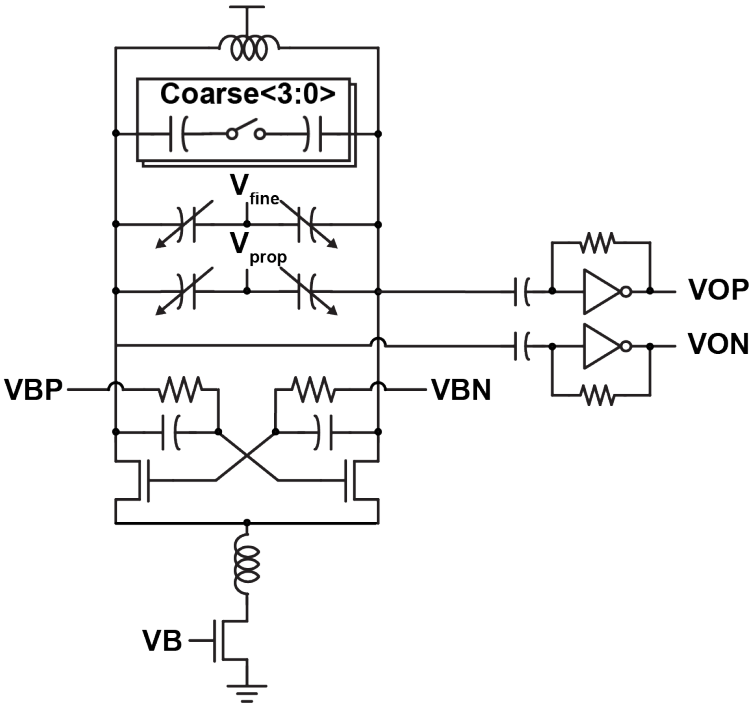


Figure 4.19: VCO and clock buffer.

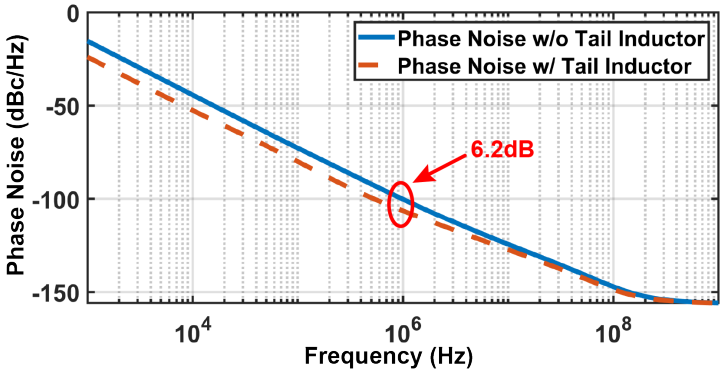


Figure 4.20: Phase noise comparison for VCO without and with tail inductor.

Sub-sampling Phase Detector and Charge Pump

Figure 4.22 shows the SSPD used in this design, with two CMOS switches cascade to sample the VCO buffer outputs with reference clock rising edge and falling edge and remove the reference ripples to get stable DC voltages. Two MUXs with transmission gates are attached to swap the two outputs and perform the inversion function. The simulated transfer function of the SSPD is plotted in Figure 4.23 (a), with the PD gain is $117.57GV/s$ or $4.70V/UI$ at

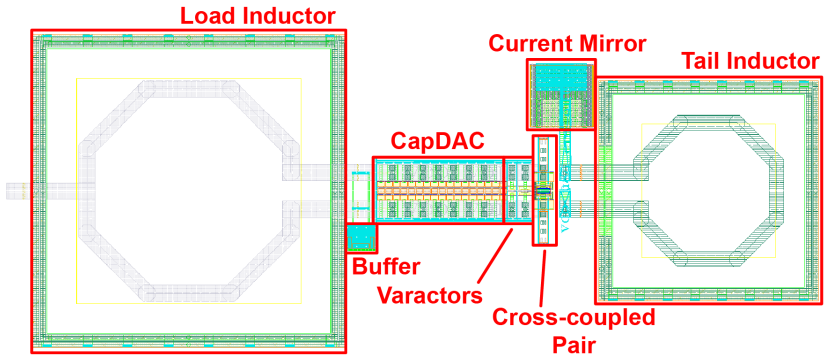


Figure 4.21: VCO and buffer layout.

25GHz.

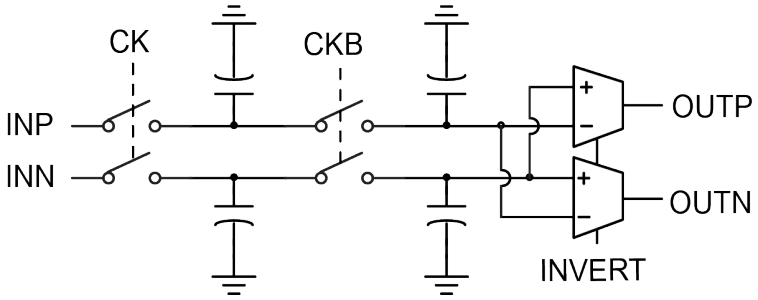


Figure 4.22: SSPD.

From the SSPLL diagram in Figure 4.18, the SSPD is followed by two comparators with double-tail configuration [55]. When setting the offset voltages of the comparators being both $0mV$, the digital SSPD transfer function in 4.23 (b) shows as a bang-bang or binary characteristic. However, When offsets voltages are set to $-300mV$ and $300mV$, the digital SSPD transfer function is tri-state, with a zero gain region from $-1.7ps$ to $2ps$. The asymmetric time region is mainly from the offset of the comparator and the layout mismatch of wires between the SSPD and the two comparators.

Figure 4.24 (a) shows the SSCP for the SSPD [46]. The input differential pair transform the input voltages to currents, which are mirrored to the final stage. There are two knobs to adjust the gain and average current of the SSCP, which include the I_{REF} to adjust the g_m of the input transistors and pulse controls PUL and $\overline{PUL}$ to adjust the turn-on time of the output current. Figure 4.24 (b) shows the pulse generation circuit, with a delay circuit. By turning on the inverting function, the duty-cycle of the pulse output is programmed from 0% to 100%.

Figure 4.25 (a) shows the SSCP transfer function, when the I_{ref} is set to $100\mu A$ and

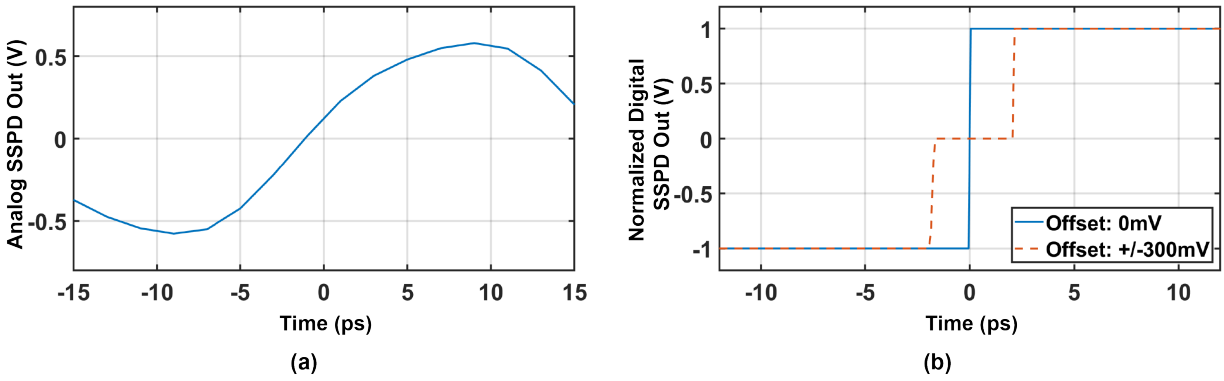


Figure 4.23: Simulated SSPD digital transfer function.

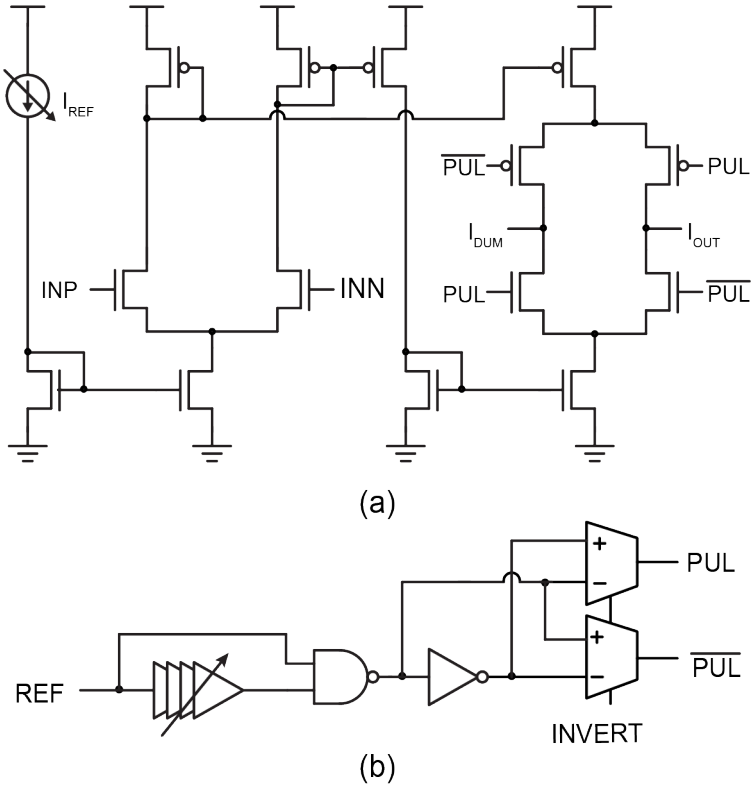


Figure 4.24: (a) SSCP and (b) pulse generation.

$50\mu A$ when the pulse duty cycle is 100%, or $100\mu A$, when the pulse duty cycle is 50%. In the three cases, the gains are $412.1\mu A/V$, $364.4\mu A/V$ and $206.9\mu A/V$. Figure 4.25 (b) shows the SSPD and SSCP transfer function, when the I_{ref} is set to $100\mu A$ and $50\mu A$ when the pulse duty cycle is 100%, or $100\mu A$, when the pulse duty cycle is 50%. From the plot, the

gains are $26.98MA/s$, $19.59MA/s$ and $20.52MA/s$, respectively.

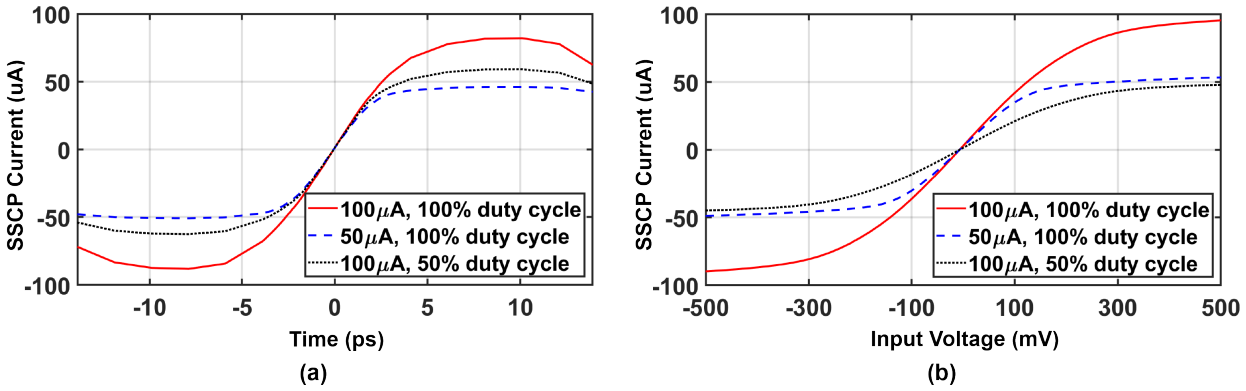


Figure 4.25: SSCP transfer function.

Dead-Zone Phase Detector/Traditional PFD and Charge Pump

Figure 4.26 shows the design of the DZPD and PFD. An inversion function is first added to the DZPD (Figure 4.6), which is then sampled by two FFs for synchronization. In the other path, the traditional PFD is attached by two SR latches to map the up and down pulses (UP/DN_{LIN}) with variable pulse widths to fixed high and low levels (UP/DN_{BB}) for digital filter. As shown in Figure 4.27, by this modification, the PFD can be used in a hybrid loop. Finally, a MUX is added after the ZDPD and PFD to choose the operation mode.

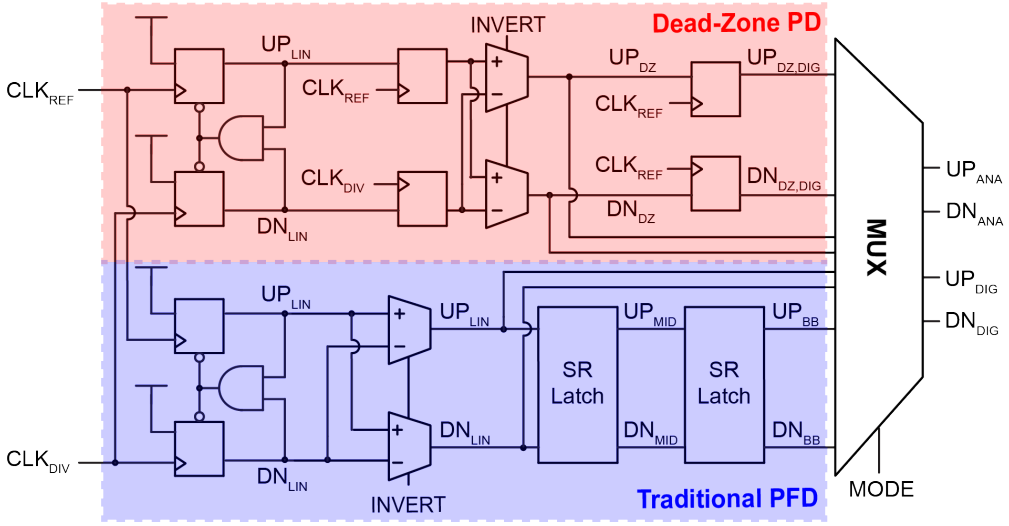


Figure 4.26: Dead-zone PD and traditional PFD.

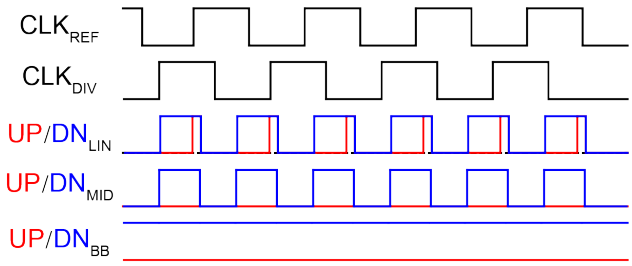


Figure 4.27: Dead-zone PD and traditional PFD.

Figure 4.28 (a) shows the PFD transfer function, with analog output and normalized digital output. From the plots, the analog transfer function presents a linear response between the input time difference and the analog output voltage. However, the digital transfer function offers a bang-bang response between input time difference and output.

Figure 4.28 (b) shows the simulated DZPD transfer function, with analog output and normalized digital output. The two transfer functions match together and the time dead-zone of the DZPD is from $-140ps$ to $140ps$.

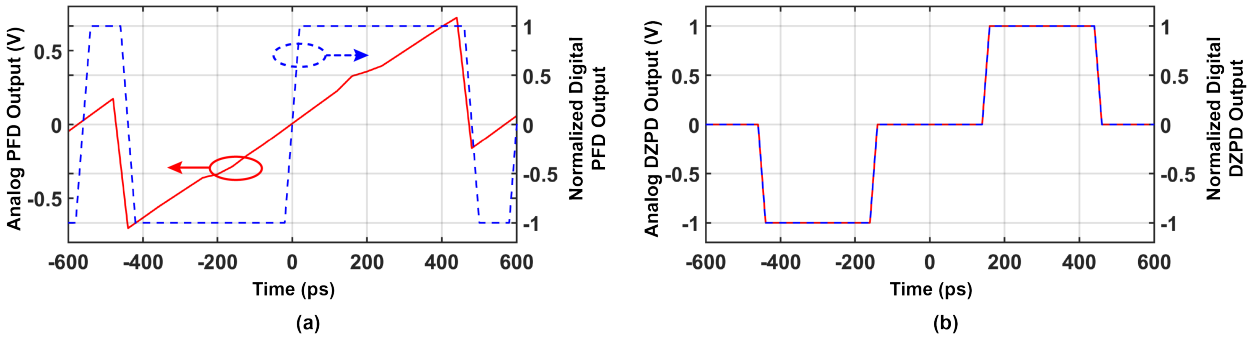


Figure 4.28: PFD/DZPD phase transfer function.

Figure 4.29 shows the design of a regular charge pump for the DZPD and PFD. As the DZPD and PFD are only for frequency locking of SSPD loop and perfromance comparison respectively, the matching requirement is relaxed. Figure 4.30 shows the transfer function of the DZPD/PFD and CP between PD input to charge pump output, with the charge pump current of $100uA$. As expected, the transfer functions of the PFD and CP offers a linear response, while the DZPD and CP presents a dead-zone region similar as the DZPD.

Figure 4.31 shows the frequency transfer function of the PFD and DZPD. The PFD shows a non-linear transfer function between input frequency and outputs, with a zero gain at $1.5625GHz$. Similarly, the DZPD shows a non-linear frequency transfer function, though offering a dead-zone for phase detection. Finally, Figure 4.32 shows the transfer function of the PFD/ DZPD and CP, between input frequency and output current.

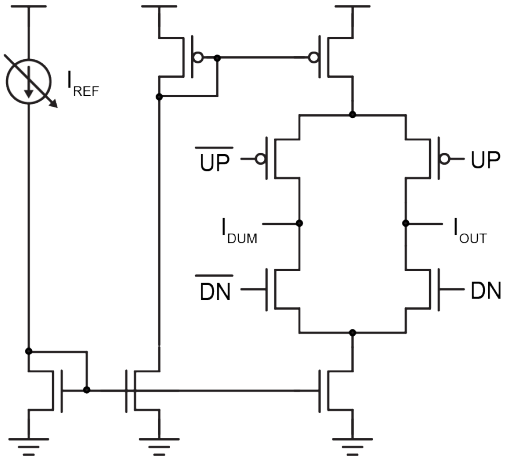


Figure 4.29: Charge pump.

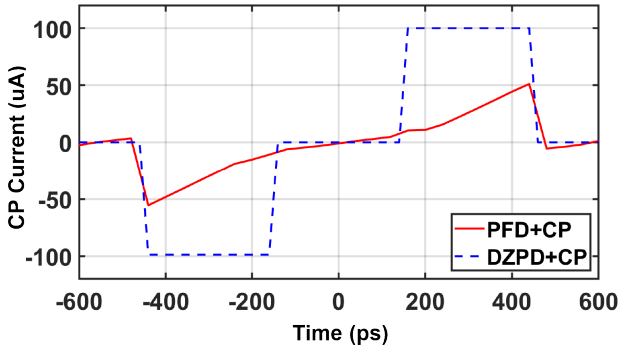


Figure 4.30: PFD/DZPD and charge pump transfer function.

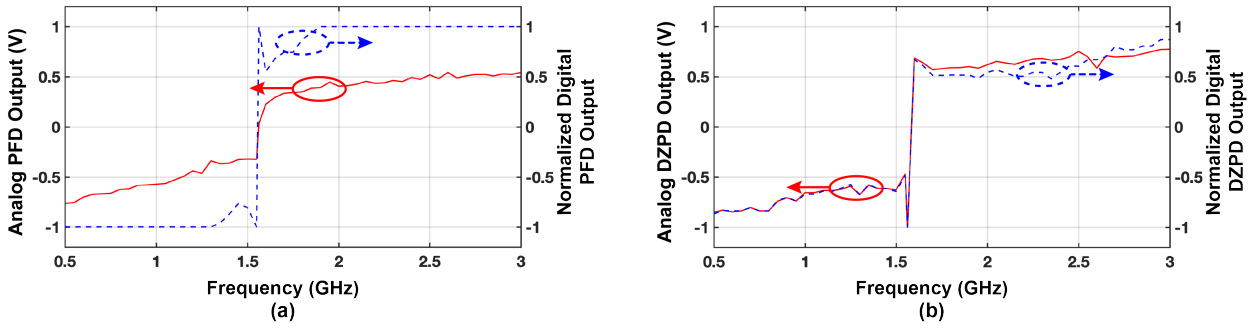


Figure 4.31: PFD/DZPD frequency transfer functions.

Low-Dropout Regulator

In a typical System on Chip (SoC) system, the supply scheme can be complicate. The main reasons are that different blocks requires different supply voltages and isolation to avoid

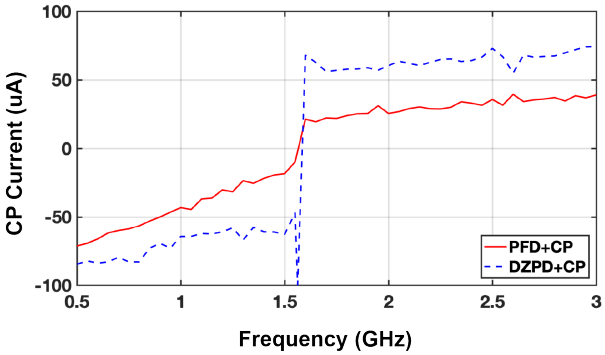


Figure 4.32: PFD/DZPD and charge pump frequency transfer function.

noise coupling, even the supply voltages are same. Figure 4.33 [56] presents a example of the SoC power scheme. Due to the high efficiency,the DC-DC converters shift the 2.7-4.0V battery supply to 1.8/1.2V and 0.6V in the first stage. The LDOs after converts the various intermediate supplies and isolate circuits from noisy part of the system, such as digital circuits and mixed-signal circuits.

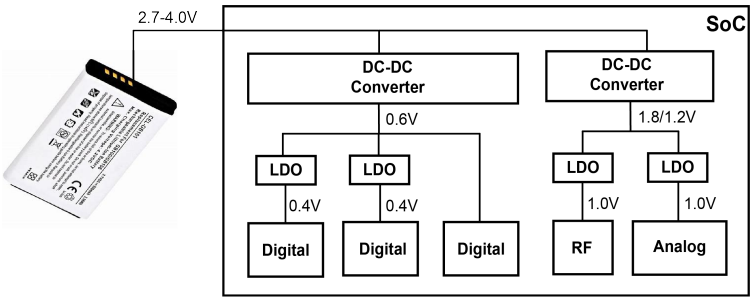


Figure 4.33: SoC power scheme.

In SerDes system, the data path usually consumes large current and transfers random data, causing a large supply fluctuation. However, the VCO in the PLL is a sensitive block that requires a clean supply for phase noise performance, which can even be affected by blocks in the PLL such as PD and digital loop. Therefore, a LDO is usually added on the VCO and CP to decouple their supplies from other blocks, and provide them a clean supply in the noisy SerDes system. Though we split the supply domains and provides a independent supply to the VCO, we added a LDO to assess the its effect to the VCO and PLL include noise and reliability.

Figure 4.34 shows the schematic of the LDO, which is based on a PMOS pass device. The PMOS LDO provides provides larger loop gain and lower voltage drop from supply to output. However, the large impedance at output node creating another low-frequency pole, may cause reliability issue. In the LDO, the main pole is located at the output of the

LDO and the second pole is set at the output of the amplifier. By adding a large decouple capacitor and extra capacitor on board, the phase margin of the LDO is 78.35°, with a DC loop gain of 26.72dB (Figure 4.35).

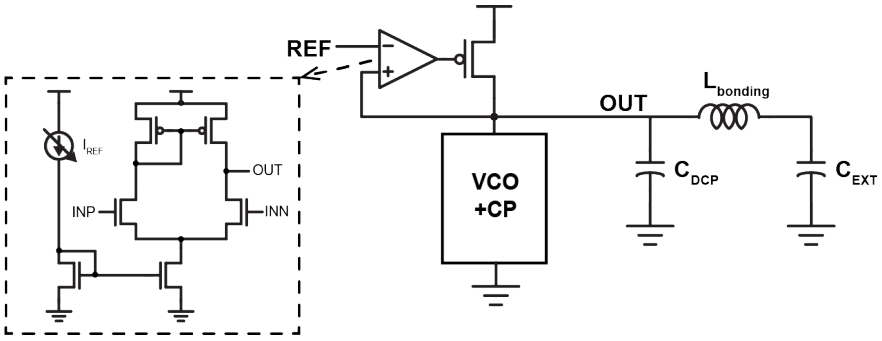


Figure 4.34: LDO schematic diagram.

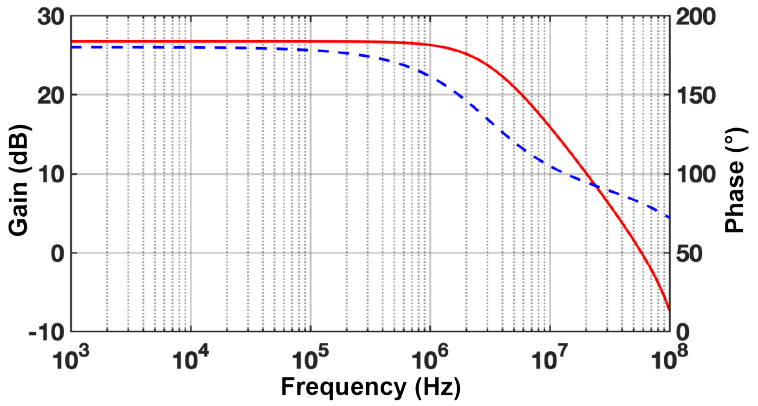


Figure 4.35: LDO loop gain and phase.

Figure 4.36 shows the simulated PSRR of the LDO, as the dominate pole is at the output, the worse PSRR is at DC, which is around $-12.93dB$. Above the frequency, the decouple capacitor comes to play a more important role and improve the PSRR. As shown in Figure 4.37, the output voltage follows the reference voltage until $1.25V$, where the gain of the error amplifier drops.

$\Delta\Sigma$ Modulator

To make a high-resolution $\Delta\Sigma$ DAC [57] with a 9-bits DAC, a $\Delta\Sigma$ modulator is applied. Figure 4.38 shows the principle of the $\Delta\Sigma$ modulator. From Figure 4.38 (a) and (b), by over-sampling the siganl with high frequency clock, the same quantization noise power distributes over a larger frequency range (from f_{s1} to f_{s2}), with a low noise density. Furthermore, the $\Delta\Sigma$

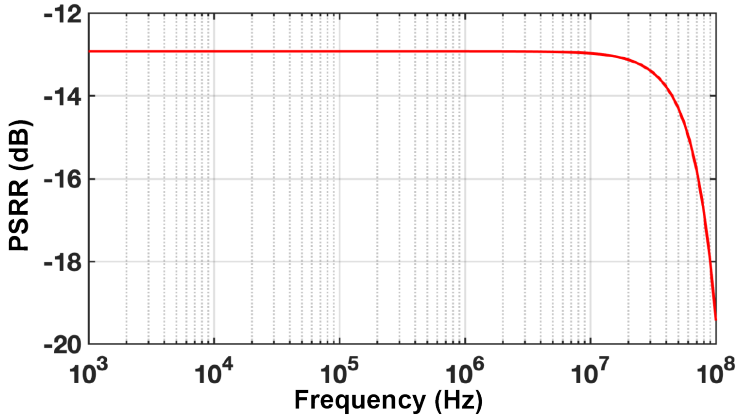


Figure 4.36: LDO PSRR.

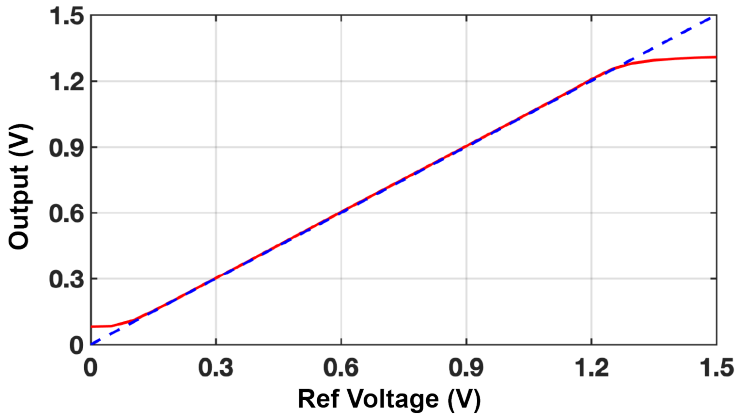


Figure 4.37: LDO output voltage when sweeping the input references.

modulator redistribute the quantization noise power by pushing the noise power to higher frequency, so a low-pass filter can get rid of most of the high-frequency components. Hence, the signal-to-noise power and the resolution of the DAC is improved.

Figure 4.39 shows the architecture of the $\Delta\Sigma$ modulator. Considering the trade-off between complexity, reliability and performance. We adopt a second-order modulator, using a feed-forward structure with extra input feed-in [58]. The signal transfer function (STF) and the noise transfer function (NTF) of the structure are

$$STF(z) = 1 \tag{4.5}$$

$$NTF(z) = (1 - z^{-1})^2 \tag{4.6}$$

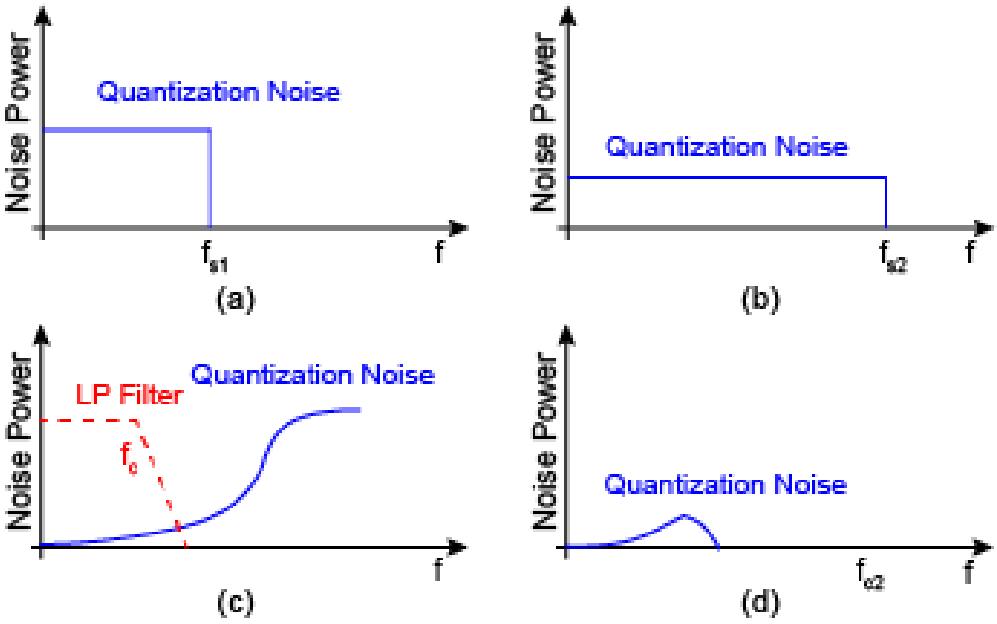


Figure 4.38: DZPD/PFD and charge pump transfer function.

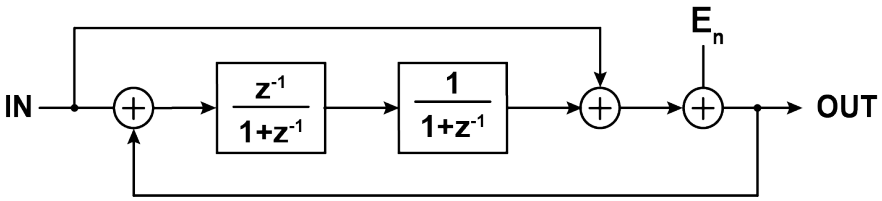


Figure 4.39: DZPD/PFD and charge pump transfer function.

As shown in Figure 4.16 and equation 4.5, the main advantage of this architecture is that there is no DC component at the outputs of the two integrators, which reduces their dynamic range requirements. Moreover, as the STF is purely constant, providing a flat response, without increasing the risk of instability.

The design is simulated using Simulink with a 1MHz input and a clock frequency of $1.5625GHz$. As shown in Figure 4.40, the quantization noise power are aligned in Simulink simulation and calculation. By setting the LF filter frequency corner to about $10MHz$ or oversampling ratio of 156, a 22-bits DAC is implemented with a 9-bits DAC physically.

4.6 System Optimization

Fig. 4.41 shows the model of the PLL. The DZPD, CP and integral path are excluded in the model, as they are ineffective when the loop is locked. The SSPD and SSCP are modeled

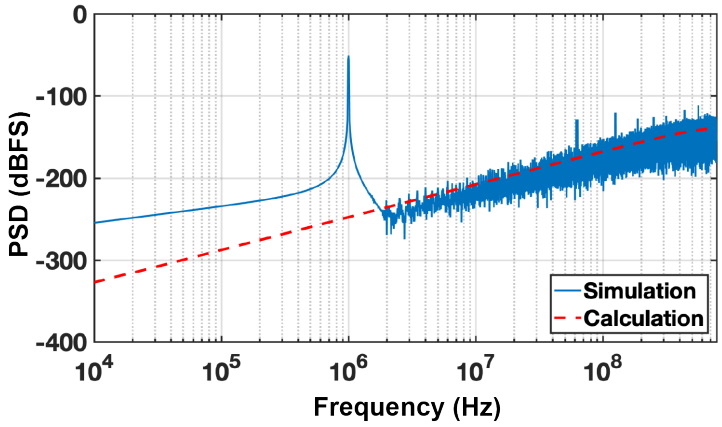


Figure 4.40: $\Delta\Sigma$ modulator calculation and simulation results.

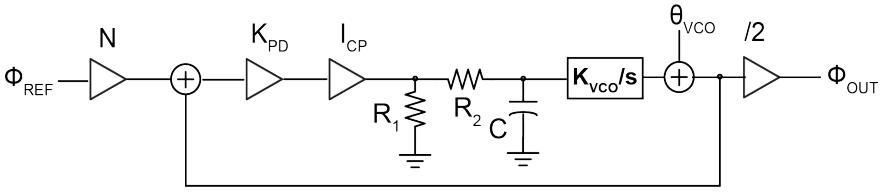


Figure 4.41: PLL model.

by K_{SSPD} and I_{SSPD} The VCO is modeled by the gain blocks of K_{vco}/s to describe the proportional gain, with the VCO phase noise modeled by a noise block θ_{vco}.

In the SSPLL, the noise contribution of the CP is negligible, and the dominating noise sources are the reference clock and ring oscillator, and their noise transfer functions are

$$\frac{\phi_{out}}{\phi_{ref}} = \frac{K_{pd} N I_{cp} R_1 K_{vco}}{s + K_{pd} I_{cp} R_1 K_{vco1}} \tag{4.7}$$

$$\frac{\phi_{out}}{\phi_{vco}} = \frac{1}{s + K_{pd} I_{cp} R_1 K_{vco}} \tag{4.8}$$

The oscillator phase noise is dominant when the loop bandwidth is small, otherwise the reference noise dominates the PLL phase noise. To determine the VCO phase noise requirement, Fig. 4.42 shows the PLL jitter integrated from $1KHz$ to $100MHz$ with different loop bandwidth under different VCO phase noise specifications. The phase noises of the VCO are assumed to be dominated by the thermal noise, with $-80dBc/Hz$, $-90dBc/Hz$,

$-100dBc/Hz$ and $-110dBc/Hz$ at $1MHz$ offset. As shown, when the VCO phase noise decreases, the optimal loop bandwidth drops to equalize the jitter contribution from the VCO and reference. Furthermore, the VCO phase noise are required to be around $-100dBc/Hz$ at $1MHz$ offset, when the integrated jitter target is below $100fs$.

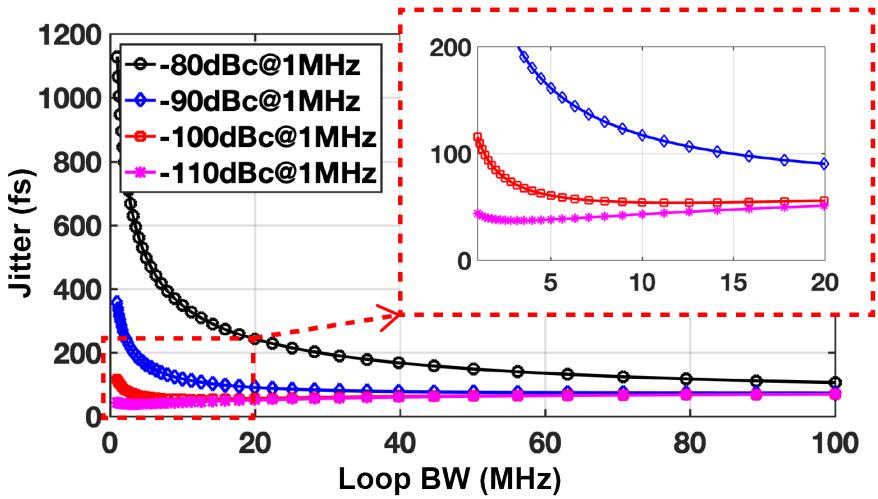


Figure 4.42: PLL RMS jitter versus different VCO phase noise at $1MHz$ offset.

Fig. 4.43 shows the PLL jitter when changing the loop bandwidth, with measured reference phase noise at $1.5625GHz$ and VCO phase noise of $-100dBc/Hz$ at 1MHz offset. With the optimal loop bandwidth being around $11MHz$, and the integrated jitter is about $54fs$.

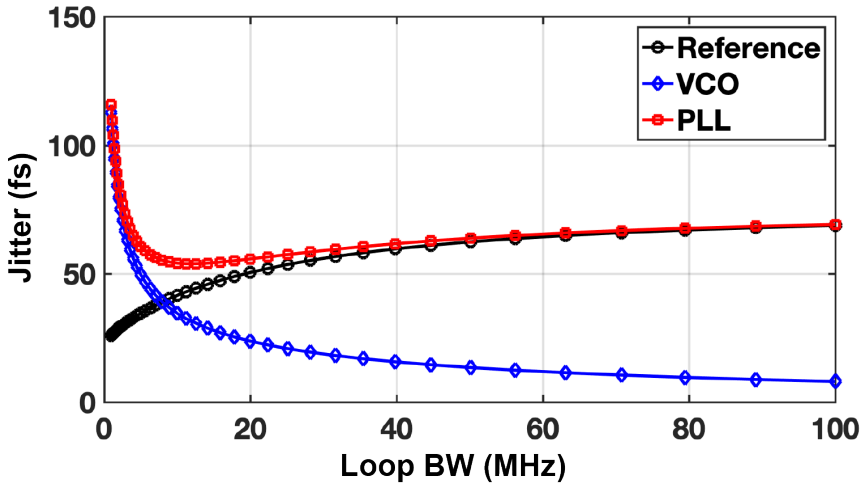


Figure 4.43: PLL RMS jitter breakdown versus loop bandwidth.

4.7 Summary

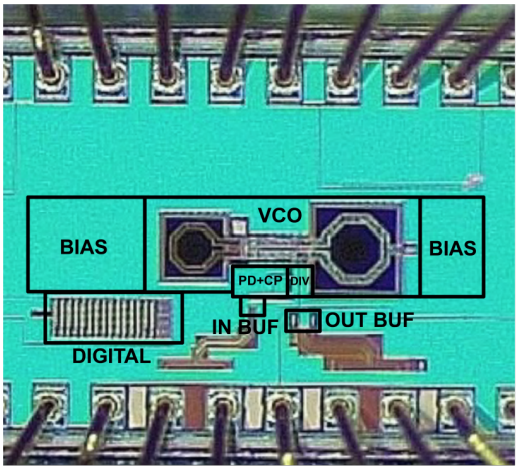
A hybrid type-I sub-100fs SSPLL with tri-state integral path for 200Gbps PAM-4 SerDes transmitter is proposed. First, the chapter discuss the requirement of the SSPLL. The SSPLL with tri-state integral path is derived from the simulation of the type-II and type-I architecture. After that, the blocks of the SSPLL are discussed and their simulation results are presented. Finally, this chapter show the analysis and optimization of the PLL system.

Chapter 5

Sub-100fs Sub-Sampling PLL Measurement Results

5.1 Testbench Setup

The SSPLL with tri-state integral path from Chapter 4 is implemented with 28nm planar process. All the layout of the blocks are generated using BAG or with digital flow, and the top-level layout is merged manually. Figure 5.1 shows the layout of the PLL, with a total area of $0.1343mm^2$.



	Block	Layout	Area (mm^2)
1	Digital	Synthesized	0.0084
2	VCO	BAG	0.0684
3	PD+CP	BAG	0.0043
4	DIV	BAG	0.0015
5	Input Buffer	BAG	0.0015
6	Output Buffer	BAG	0.0024
7	Bias	BAG	0.0478
	Top	Manual	0.1343

Figure 5.1: PLL layout.

Figure 5.2 shows the test bench setup for the PLL. The PC controls the FPGA to program the scan chain on the PLL chip, which also acquires current and voltage biases from the bias board. The signal generator E8257D generates the reference clock, based on the divider ratio is set to 16 or 32. The clock is transformed to a differential clock with a balun 5310A,

which is connected to the PLL with K-connectors and transmission lines on PCB board. The divided-by-2 differential clocks pass through the transmission lines and K-connectors are converted to single-ended clock though the hybrid SH1455A. Finally, the signal analyzer N9030A measures the spectrum and phase noise of the PLL output.

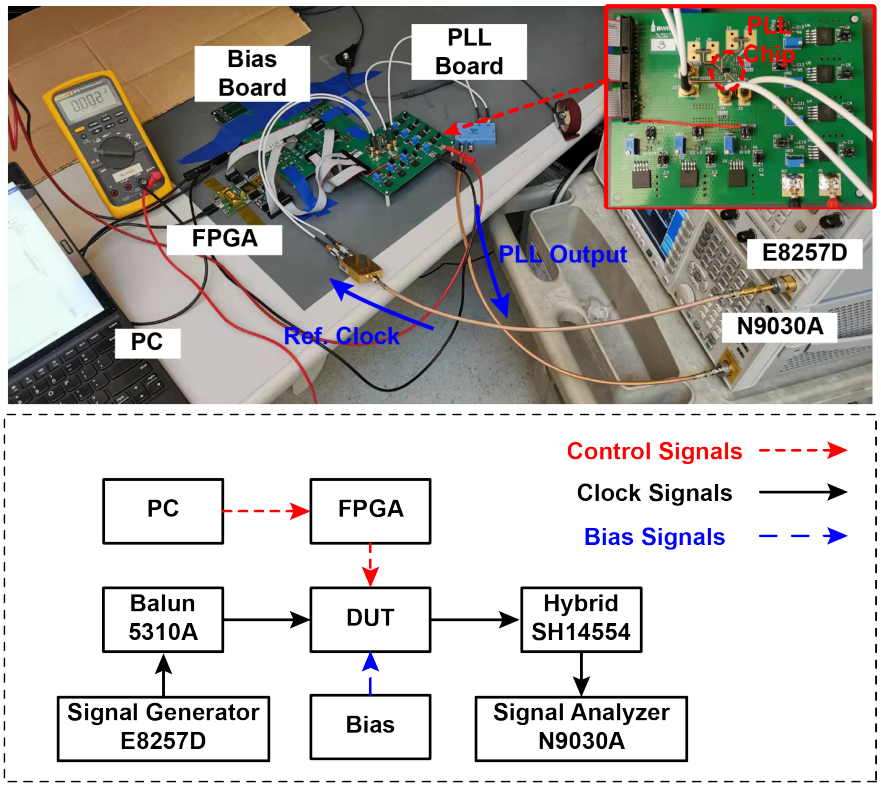


Figure 5.2: PLL layout.

The bandwidth of the balun and hybrid are 6.5GHz an 18GHz, which are large enough to avoid the loss attenuating the clock amplitudes. The loss of the channel is assessed with a channel on PLL bias PCB, as shown in Figure 5.3 (a). At $14GHz$, the 3.3-inches channel shows a loss of $-11.53dB$ (Figure 5.4). While the channel length of the PLL PCB (Figure 5.3) is 0.6 inches, the loss is $-2.10dB$.

5.2 VCO Measurement Results

The VCO is tested with the open-loop PLL. By fixing the fine control and proportional control voltages, the frequency with different CapDAC code is from $24.6GHz$ to $29.2GHz$, as demonstrated in Figure 5.5.

Figure 5.6 shows the phase noise of the divided VCO output at oscillating frequency of $12.07GHz$ and $14.07GHz$. The phase noise at $1MHz$ offset are $-104.27dBc/Hz$ and

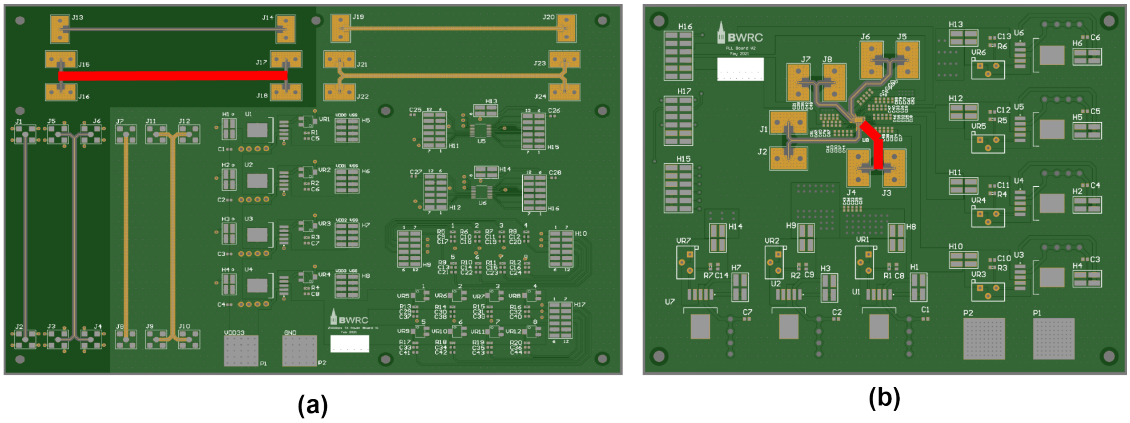


Figure 5.3: (a) PLL bias PCB, and (b) PLL PCB.

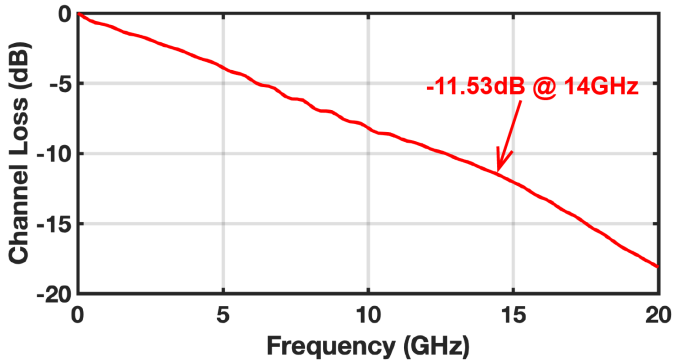


Figure 5.4: Loss of power PCB channel.

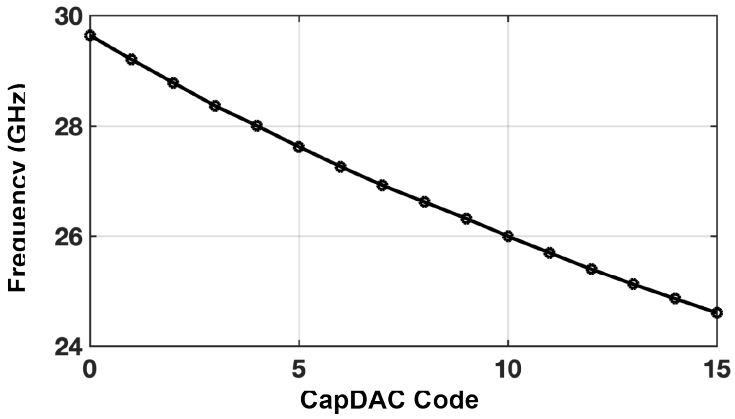


Figure 5.5: VCO frequency versus CapDAC codes.

$-100.10dBc/Hz$, respectively, meeting the phase noise requirements in Section 4.6.

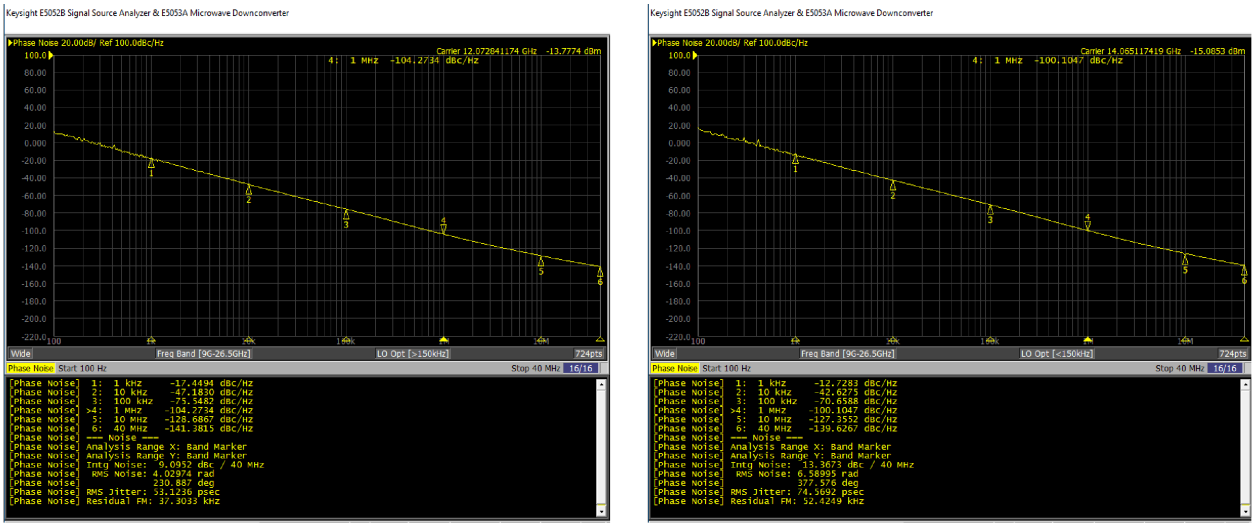


Figure 5.6: VCO phase noise at $12.07GHz$ and $14.07GHz$.

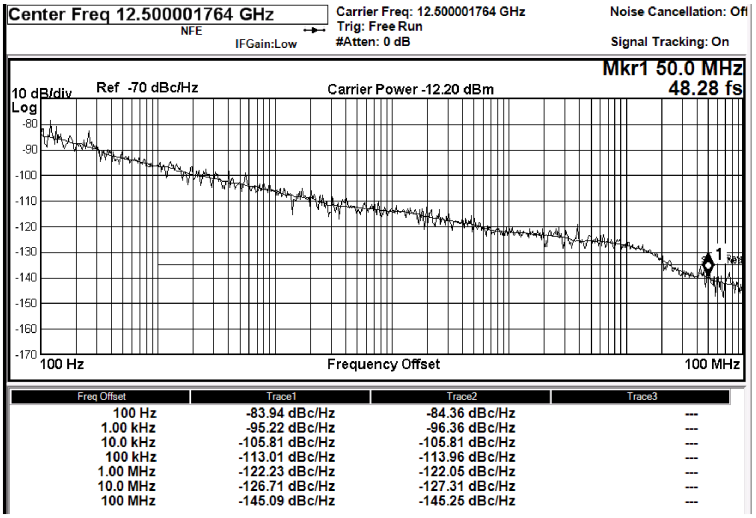
5.3 PLL Measurement Results

Test Results of SSPLL with Tri-State Integral Path

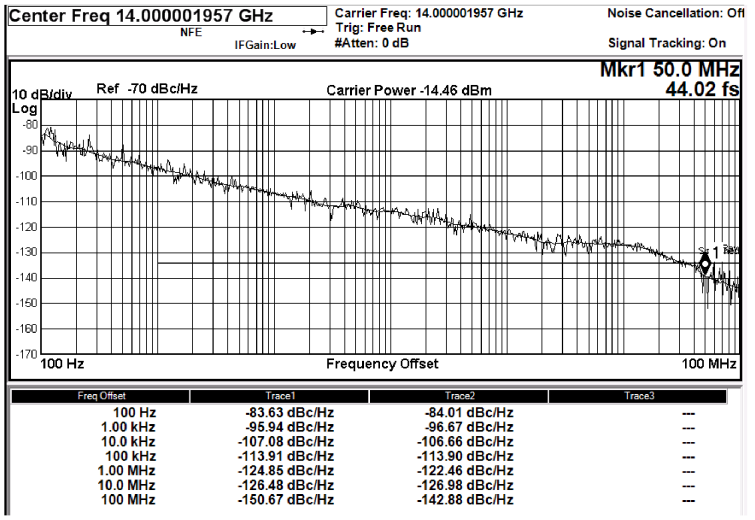
Figure 5.7 shows the phase noise measurement results, when the PLL is operating at $25GHz$ and $28GHz$ PLL. As the clock output is connected to the C^2MOS divider, the frequency shown in the test results are $12.5GHz$ and $14GHz$. From these figures, the phase noises at $1MHz$ offset are $-120.7dBc/Hz$ and $-124.85dBc/Hz$, and the integrated RMS jitter from $1KHz$ to $100MHz$ are $49.22fs$ and $44.02fs$, respectively. Considering the analysis in Section 4.1, they meets the specification of the $200Gb/s$ SerDes TX, or even SerDes TX of higher speed.

Figure 5.7 shows the spectrum of the $25GHz$ and $28GHz$ PLL outputs. After the signal path outside the chip, including the wire-bondings, PCB T-lines, K-connectors, hybrid and cables, the output clock power is about $-14dBm$, Due to the clock feed-through and charge injection of sub-sampling PD., the spur of the reference clock at the divider outputs are $-65.6dB$ and $-56.6dB$ lower than the clock power, satisfying the specifications for the SerDes TX application.

To check the in-band spur from the loop dynamics, Figure 5.9 shows the spectrum of the $12.5GHz$ and $14GHz$ PLL outputs with span of $100MHz$. By eliminating the ripples on the VCO control lines, the spectrum is clean near the clock tone.



(a)



(b)

Figure 5.7: Phase noise of PLL output clocks at 12.5GHz and 14GHz.

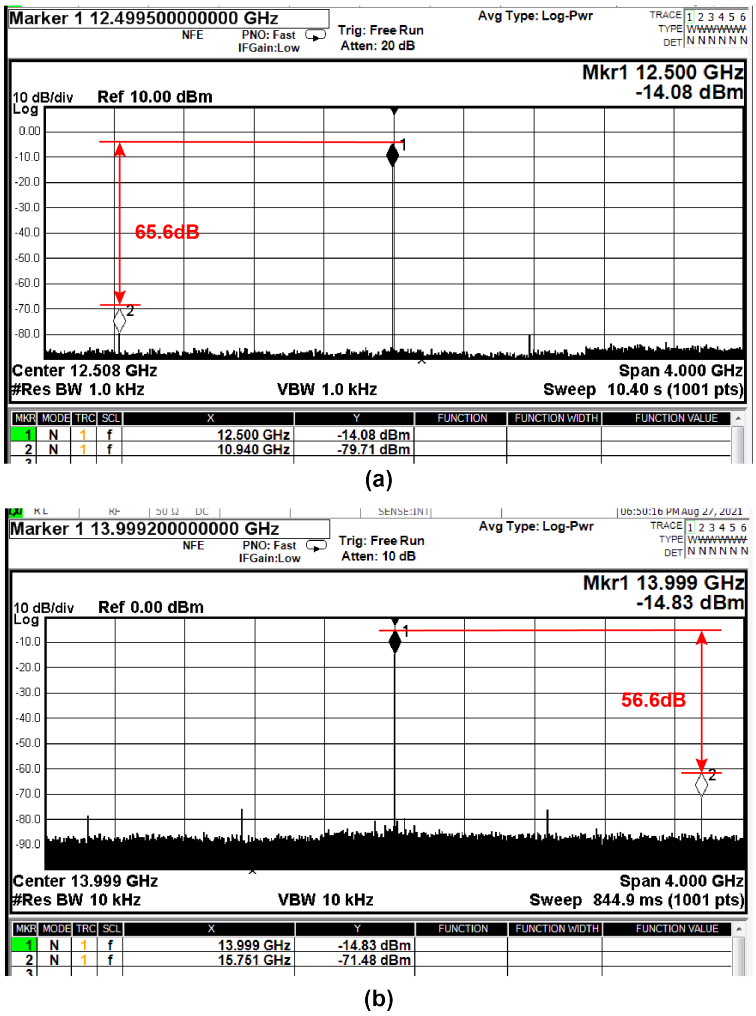


Figure 5.8: Spectrum of PLL output clocks at 12.5GHz and 14GHz with span of 4GHz.

Test Results of SSPLL in type-II Mode

Figure 5.10 shows the phase noise results of the PLL output in type-II mode. Due to the coarse DAC resolution and the ripples on the VCO control lines, there are spurs around 10MHz in phase noise plots. Therefore, the integrated RMS jitter of the two clocks are 137.7fs and 99.13fs respectively, which are about 50fs larger than the type-I mode with tri-state integral path.

Figure 5.11 shows the spectrum of the 25GHz and 28GHz PLL outputs with span of 100MHz in type-II mode. Due to the control line ripples, the in-band spur are clearly shown in the spectrum plots, which are about 15dB higher than the phase noise floor.

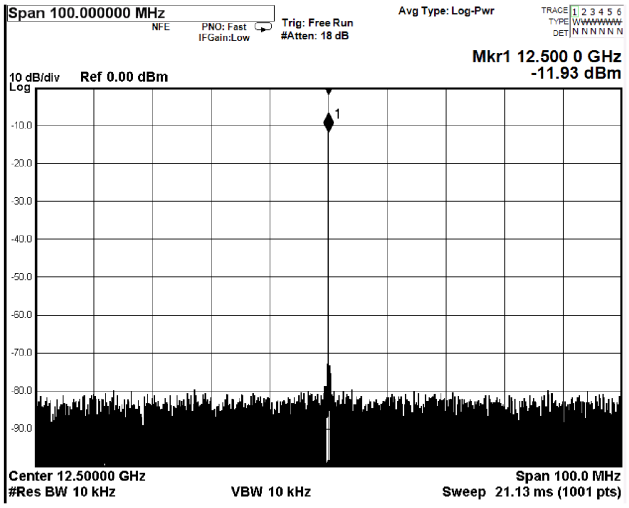
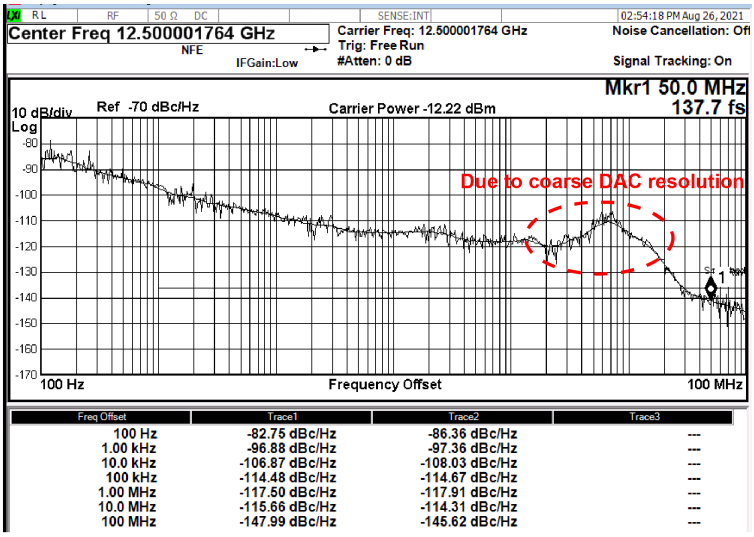
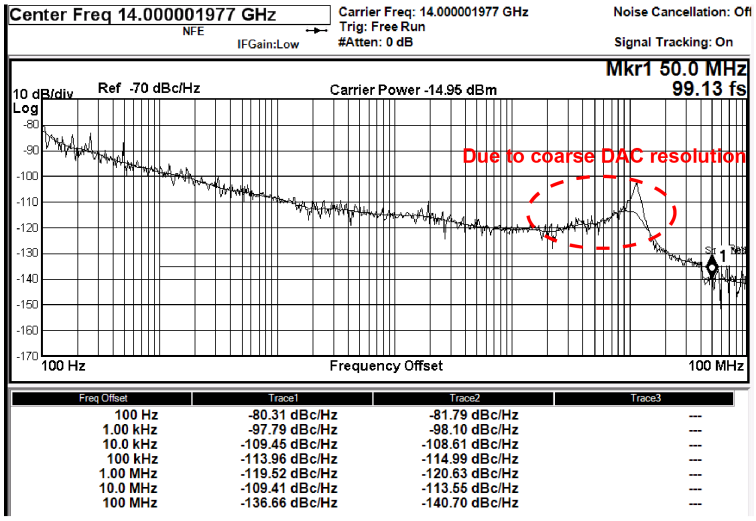


Figure 5.9: Spectrum of PLL output clocks at $12.5GHz$ and $14GHz$ with span of $100MHz$.



(a)



(b)

Figure 5.10: Phase noise of PLL output clocks at $12.5GHz$ and $14GHz$ in type-II mode.

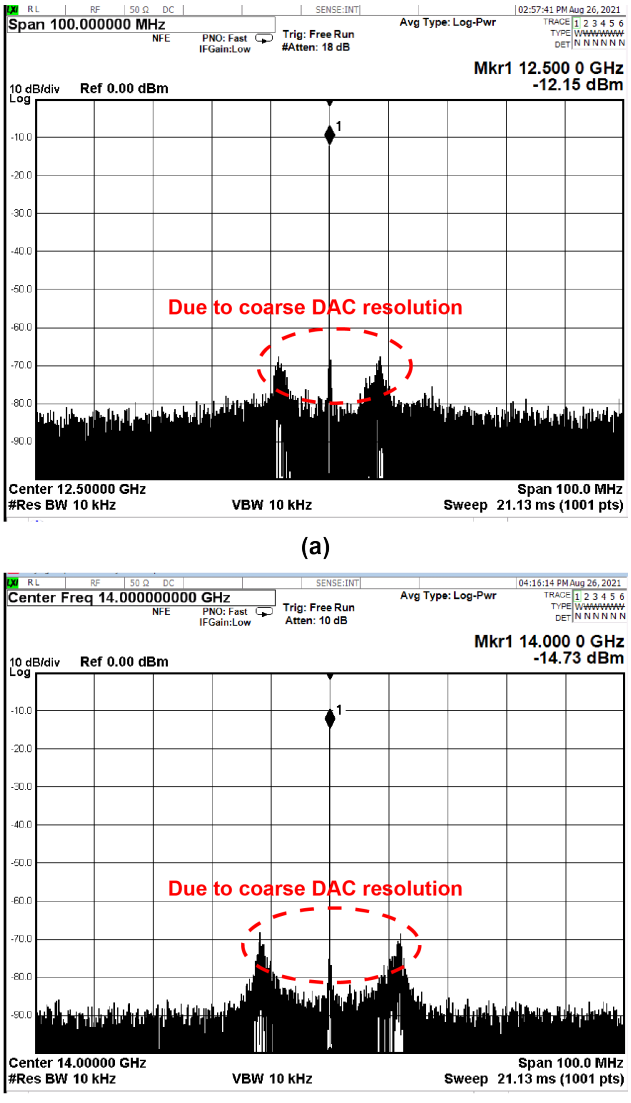
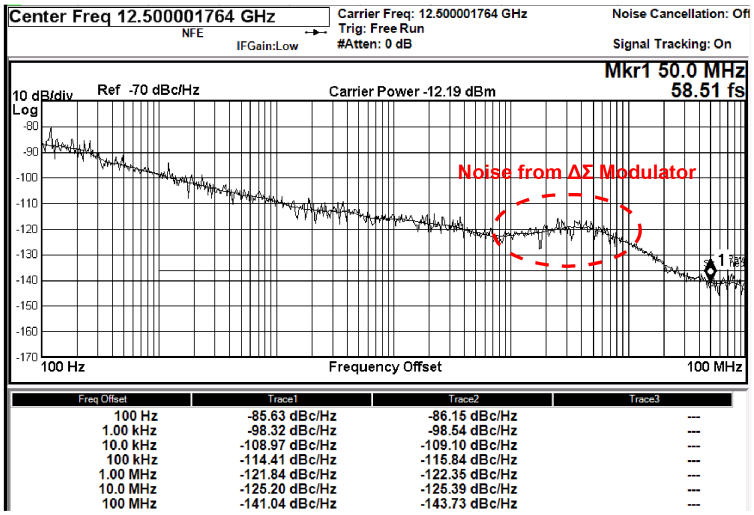


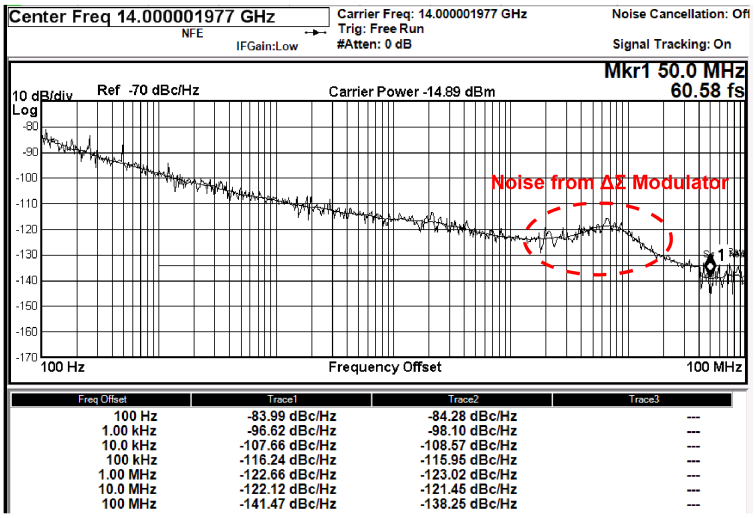
Figure 5.11: Spectrum of PLL output clocks at $12.5GHz$ and $14GHz$ in type-II mode.

Test Results of SSPLL in ΔΣ Mode

Figure 5.10 shows the phase noise results of the PLL output in ΔΣ mode. The phase noise presents bumps between $1MHz$ and $10MHz$, caused by the noise of the ΔΣ modulator. The bump increases the integrated jitter by around $10fs$, leading to the RMS values of $58.51fs$ and $60.58fs$.



(a)



(b)

Figure 5.12: Phase noise of PLL output clocks at $12.5GHz$ and $14GHz$ in ΔΣ mode.

Figure 5.9 shows the spectrum of PLL outputs with span of $100\,MHz$ in ΔΣ mode. Due to the ΔΣ modulator, the frequency error of the integral path is much smaller than the type-II mode, producing a clean clock tone. However, in the $14GHz$ spectrum, we can still

notice some spur near the tone coming from the $\Delta\Sigma$ noise, which is about $7dB$ higher than the phase noise floor.

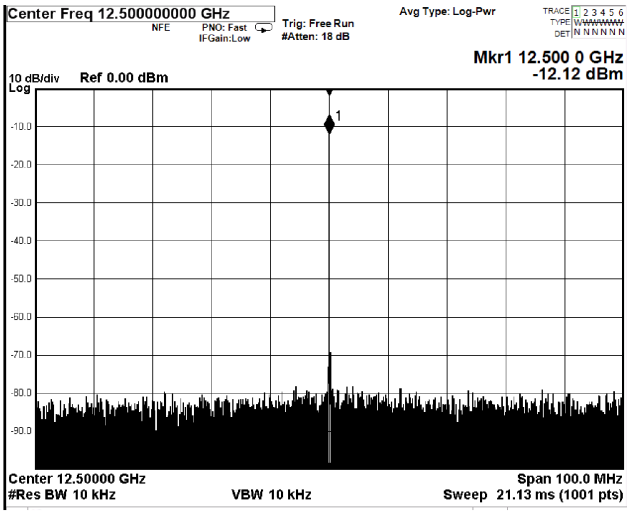


Figure 5.13: Spectrum of PLL output clocks at $12.5GHz$ and $14GHz$ in $\Delta\Sigma$ mode.

Test Results of SSPLL in type-I Mode

Figure 5.14 shows the phase noise results of the PLL output in type-I mode. As the PLL is out-of-lock, the clock phase noise almost follows the VCO, leading to a huge integrated RMS jitter of $8.519ps$ and $8.643ps$.

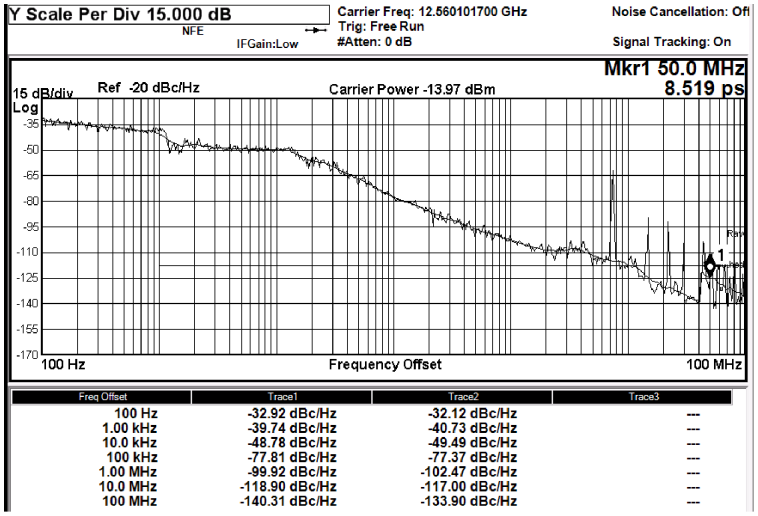


Figure 5.14: Phase noise of PLL output clocks at (a) $12.5GHz$ and (b) $14GHz$ in type-I mode.

Figure 5.9 shows the spectrum of the PLL outputs in type-I mode, which is full of noise and spur with un-locked loop.

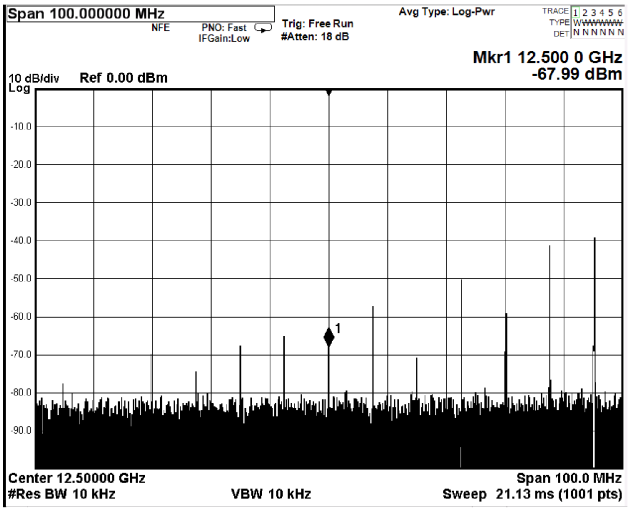


Figure 5.15: Spectrum of PLL output clocks at (a) 12.5GHz and (b) 14GHz in type-I mode.

5.4 LDO effects on Phase Noise

As discussed in Section 4.5 of Chapter 4, the LDO in SerDes systems may affect the VCO and PLL phase noise. Therefore the phase noise of the PLL with LDO is tested to assess its effect. As expected, the phase noise in Figure 5.16 is inferior because of the LDO, however, the difference of the integrated RMS jitter is 10fs, so the phase noise degradation is small.

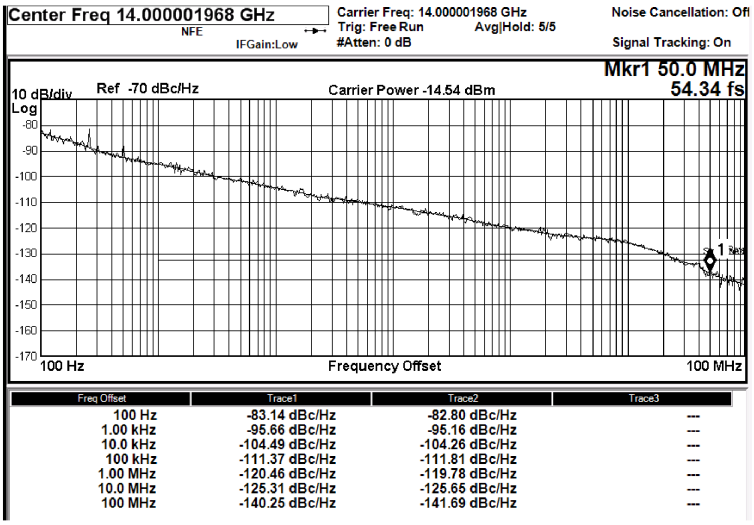


Figure 5.16: Phase noise of PLL output clocks at $14GHz$ with LDO.

5.5 Phase Noise Breakdown

Figure 5.17 shows the phase noise with the blocks in the PLL, including the VCO, the reference and its buffer, CP, PD and LF, when the output frequencies are $12.5GHz$ and $14GHz$. As expected, the VCO and the reference are the main sources of phase noise, and the phase noise is optimized when the loop bandwidth are $12MHz$ and $14MHz$.

Figure 5.18 compares the PLL phase noise and the noise from the $\Delta\Sigma$ modulator, showing that the $\Delta\Sigma$ noise causes the phase noise bump between $1MHz$ and $10MHz$.

5.6 Summary and Comparison Table

The total power of the PLL is $17mW$, where the referece buffer, PD and divider chain, digital loop and scan chain, and VCO, CP and C^2MOS divider accounts for 25%, 3% and 72%, respectively (Figure 5.19). From the measured integrated RMS jitter and the power consumption, the figure-of-merit (FoM_J) can be calculated as

$$FOM_J = 10log(\frac{\sigma_{rms}}{1s} \cdot \frac{Power}{1mW}) \tag{5.1}$$

where σ_{rms} and $Power$ are the integrated rms jitter and the power consumption, respectively. The resulting FoM_J of the PLL is $-254.8dB$. Furthermore, the figure-of-merit (FoM_T) considering freqency range can be calculated as

$$FOM_T = 10log(\frac{\sigma_{rms}}{1s} \cdot \frac{Power}{1mW} \cdot \frac{1}{TR}) \tag{5.2}$$

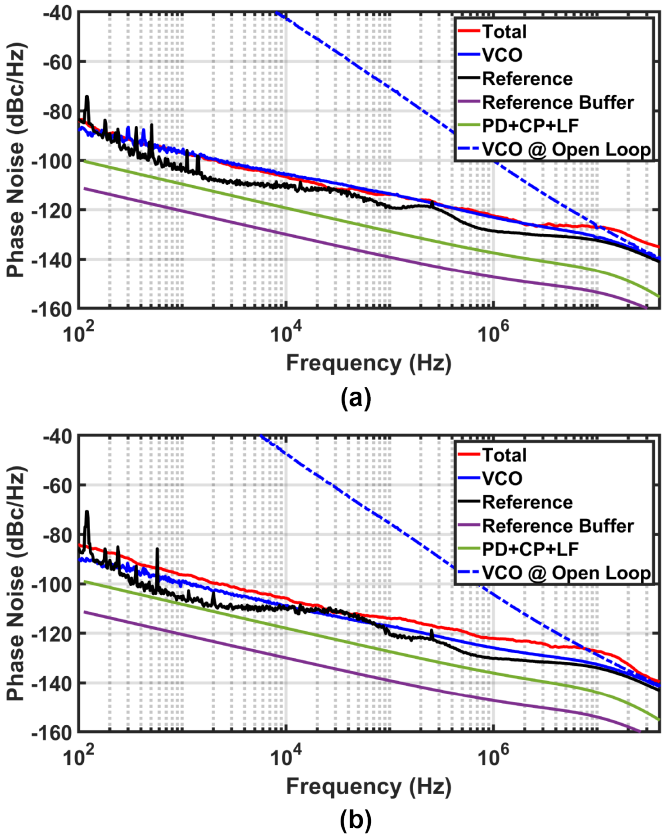


Figure 5.17: Phase noise break down of (a) $12.5GHz$ and (b) $14GHz$ clocks.

where, $TR = f_{max} - f_{min}/f_{mid}$ f_{max} is the maximum frequency, f_{min} is the minimum frequency and f_{mid} is the average frequency. Considering PLL output frequency range is $24.6 - 29.6GHz$, the FOM_T is $-247.3dB$.

Table 5.1 compares this design with state-of-the-art PLLs operating beween $20 - 30GHz$. Using the layout generated with BAG, we are still reaching the best FOM values compared with other designs, showing the effective of the design methodology and PLL architecture.

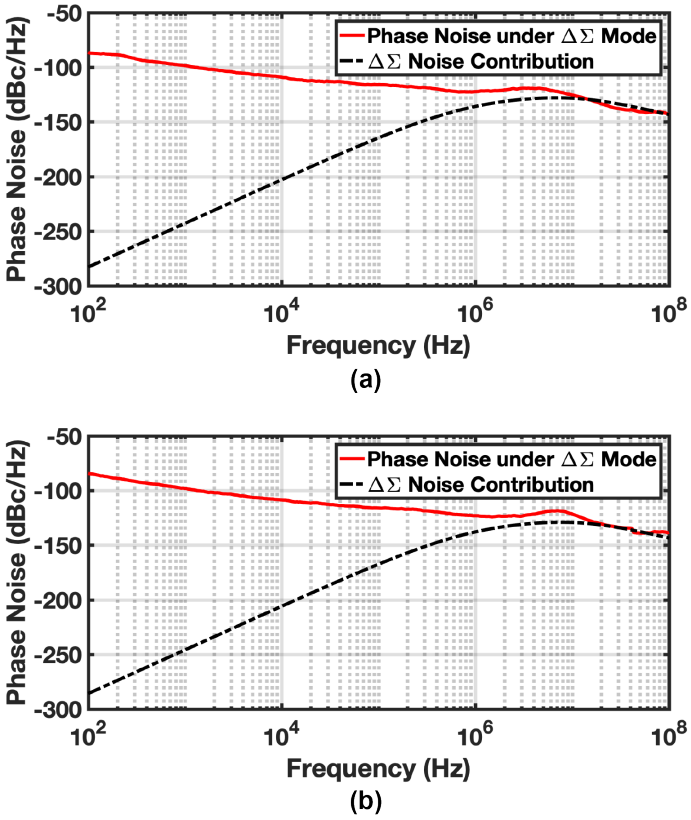


Figure 5.18: Phase noise break down of (a) $12.5GHz$ and (b) $14GHz$ clocks in $\Delta\Sigma$ mode.

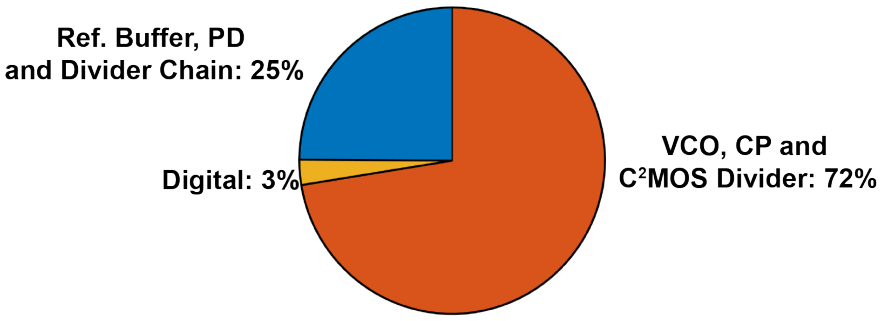


Figure 5.19: PLL power breakdown.

Table 5.1: PLL performance comparison.

	JSSC'14 [59]	TCS-I'19 [49]	JSSC'18 [60]	ISSCC'19 [61]	JSSC'18 [62]	This Work
Topology	BB PLL	IL PLL	IL PLL	SS PLL	PFD PLL	SS PLL
Technology	32nm SOI	65nm CMOS	65nm CMOS	65nm CMOS	28nm CMOS	28nm CMOS
Supply (V)	1.0	1.2/0.95	1.2	1.2/0.55	1.2	1.0/0.9
Frequency (GHz)	23.8-30.2	18.0-2	27.4-30.8	25.4-29.5	23.3-30.2	24.6-29.6
Ref. Clk (GHz)	0.1944	1.125-1.438	2.0-2.4	0.103	0.4915	1.53-1.85
RMS Jitter (Integration BW)	199.0 fs (1M-1G)	57.4 fs (1k-100M)	86.0 fs (1K-100M)	71.0 fs (1K-100M)	114.0 fs (10K-40M)	44.0 fs (1K-100M)
Ref. Spur (dB)	N/A	-45.3	-32.62	-63	-65	-56.6
PN @ 1MHz (dBc/Hz)	-86 (28GHz)	-121 (20GHz)	-115.6 (29.25GHz)	-112.8 (26.368G)	-104 (25.95GHz)	-124.86 (14GHz)*
FOM_J** (dB)	-239.10	-253.5	-247.5	-252.9	-243.9	-254.8
FOM_T*** (dB)	-232.86	-247.3	-238.1	-244.6	-238.1	-247.5
Power (mW)	31	13.7	24.3	10.2	31	17.0
Area (mm^2)	0.022	0.462	0.11	0.24	0.11	0.134

*Measured from divide-by-2 divider

**$FOM_J = 10log(\frac{\sigma_{rms}}{1s} \cdot \frac{Power}{1mW})$

***$FOM_T = 10log(\frac{\sigma_{rms}}{1s} \cdot \frac{Power}{1mW} \cdot \frac{1}{TR})$, $TR = \frac{f_{max}-f_{min}}{f_{mid}}$

Chapter 6

200Gbps PAM-4 Transmitter with Hybrid Sub-Sampling PLL

By merging the datapath, clock distribution and SSPLL from Chapter 4, this chapter presents a complete 200Gbps PAM-4 TX in 28nm CMOS technology with layout generators, which includes a low-jitter type-I hybrid sub-sampling PLL with tri-state integral path, a clock distribution network with flexible timing control, and a high-bandwidth data path with 5-tap FFE and T-coil for bandwidth extension.

6.1 Structure and Clock Design Considerations of the 200Gb/s PAM-4 Transmitter

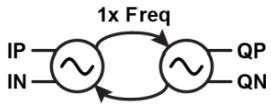
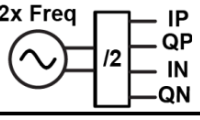
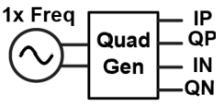
	Quad LC VCO	Diff. LC VCO + Divider	Diff. LC VCO + Quad Gen
Diagram			
Comparison	Good Jitter Small Power Large Area High Complexity	Better Jitter Large Power Large Area High Complexity	Good Jitter Small Power Small Area Low Complexity

Figure 6.1: VCO and quadrature clock generation options.

For 200Gb/s PAM-4 transmitter, one of the main considerations of the clock generation and distribution is the choice of voltage-controlled oscillator and quadrature clock generation

options. Figure 6.1 shows the three potential options, whose quadrature errors are small enough to meet requirements and within reasonable adjustment range. First, a quadrature VCO can be used to generate the 4-phase clocks directly. While this architecture provides good jitter and small power, it needs large layout area and design effort due to two LC VCOs coupled with each other.

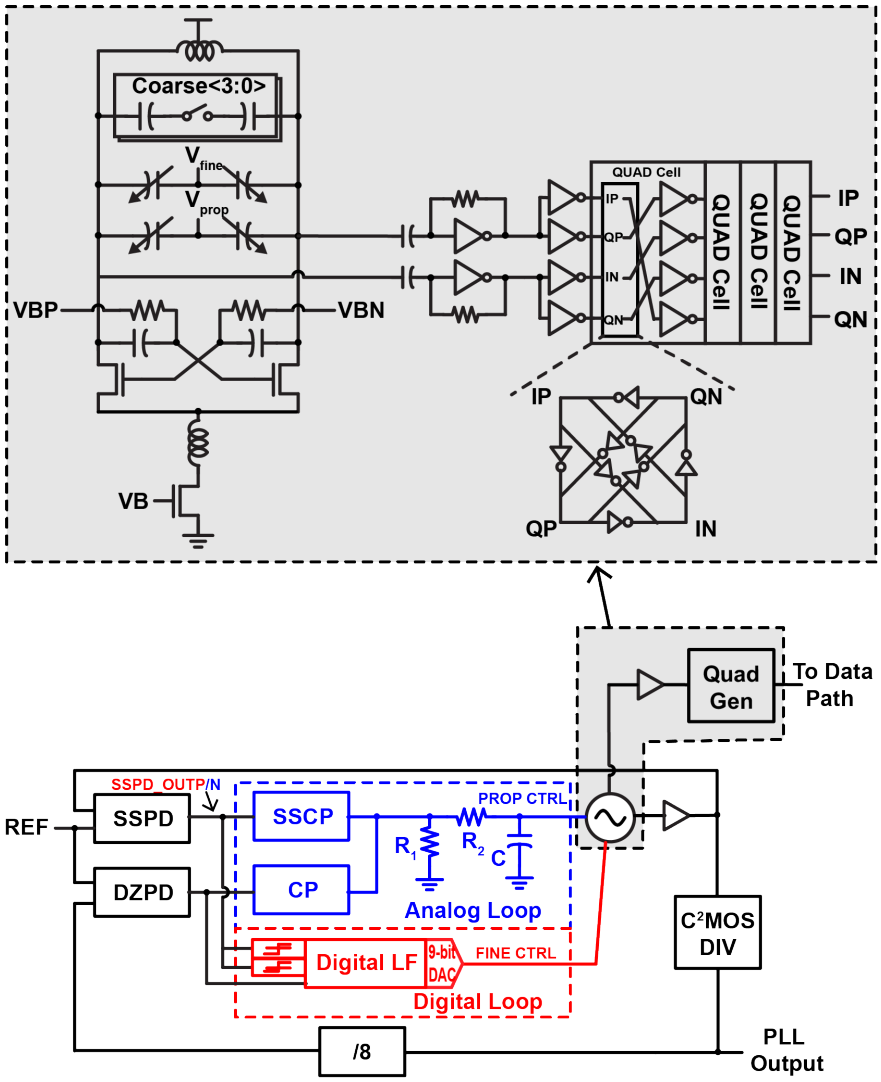


Figure 6.2: VCO and quadrature clock generation options.

The second option is the VCO operating at doubled frequency followed by a frequency divider. This architecture usually provides better jitter performance with less interference and noise existing at the VCO frequency. However, as the VCO works at doubled frequency, it requires more power due to the lower tank quality factor. The design of frequency divider also increases the area and complexity if a resonant tank or CML-to-CMOS circuit is applied.

Finally, a differential LC VCO at quarter rate ($25GHz$ in this desgin) and quadrature clock generation circuit is employed, which has small power, small area, and low complexity. The class-C VCO with tail inductor connects to a ac-coupled trans-impedance-amplifier-based clock buffer to adjust the DC voltage and correct duty-cycle of the clock, and an injection- locked quadrature generator is attached to generate the 4-phase $25GHz$ clocks.

Figure 6.3 shows the overall TX architecture. The type-I hybrid SSPLL with tri-state integral path from 4 and quadrature clock generator from 3 produce the low-jitter 4- phase 25GHz clocks, while the remaining duty cycle errors and quadrature errors are corrected by the variable delays and ac-coupling resonant buffer, which drives the 4-to-1 multiplexers (MUXs) in the data path and the C2MOS clock dividers in the clock distribution network. The phases of divided clocks are adjusted by the phase interpolator and digital- controlled delay line to maximize the time margin between the retimers, 8-to-4 MUXs and 4-to-1 MUXs across different PVT corners.

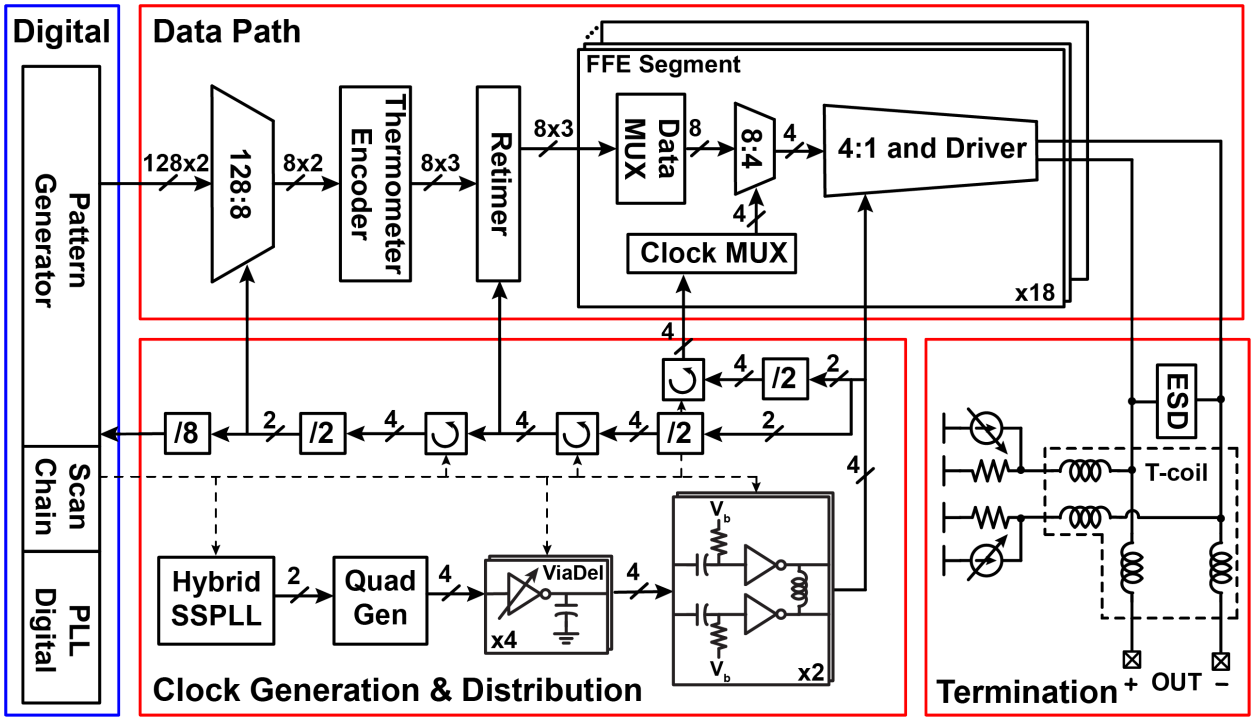


Figure 6.3: Architecture of the 200Gb/s PAM-4 TX.

The data path consists of pattern generators, 128:8 serializers, a thermometer encoder, and retimers, followed by 18 FFE driver segments, which can be programmed to support PAM-4 and NRZ data pattern. To extend the data path bandwidth, T-coils are added at the output node to isolate the capacitive loading from MUX/driver cells, ESD diodes (supporting >1-KV HBM and 250-V CDM levels), resistors, pull-up current sources and

PADs. The flexible 5-tap coarse-fine FFE is tuned to cancel the pre- and post- inter-symbol interference (ISI).

Figure 6.4 shows the circuit diagram of the coarse and fine FFE scheme. For coarse FFE, to avoid implementing 1-UI delay at full data rate, the 1-UI delay is implemented in quarter rate, by multiplexing proper data ($D8\langle 0:7\rangle$) and clock ($C8\langle 0:3\rangle$) into the 8-to-4 MUX. It also increases the time margin for the MUX and enables the implementation of the 5-tap FFE at a lower data rate. The fine FFE is adjusted in the final 4-to-1 MUX/driver stage, by tuning the gate voltage of the cascode MOS transistor (M2), controlling the tap weights with 0.6mVppd resolution by a 7-bit DAC. Figure 4 also compares the pulse response without FFE and with FFE. By properly setting the 1-tap and 2-tap post cursor FFE, the inter-symbol interference (ISI) is eliminated. From the channel loss, the FFE improves the loss by 4.5dB at baud-rate frequency.

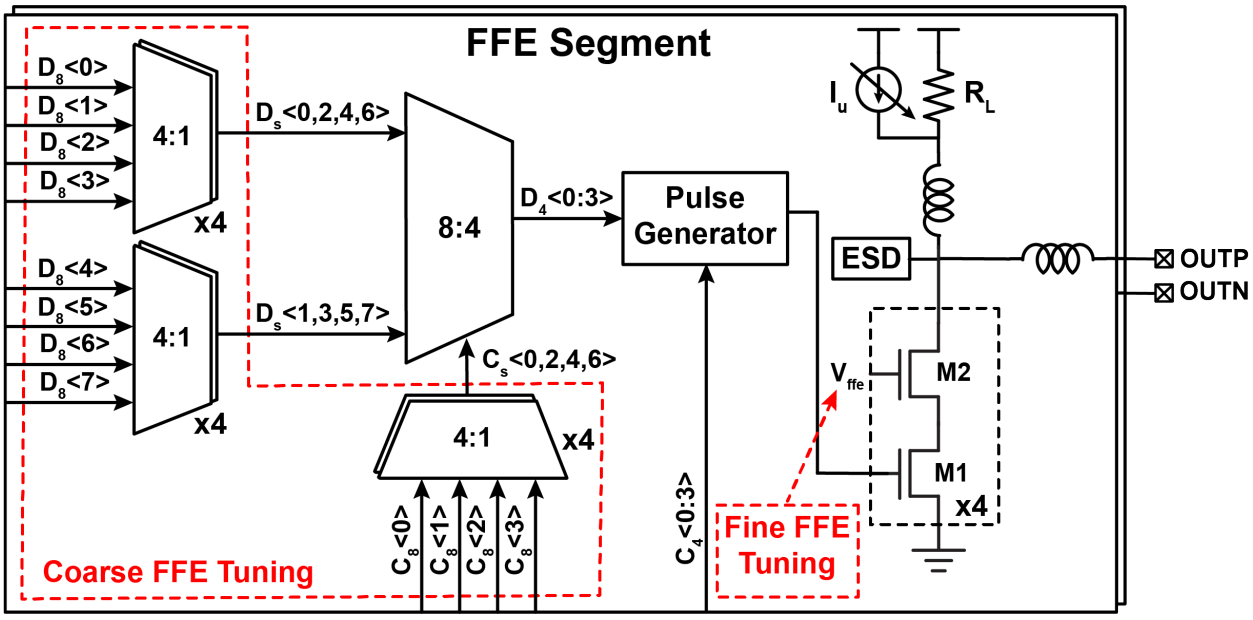
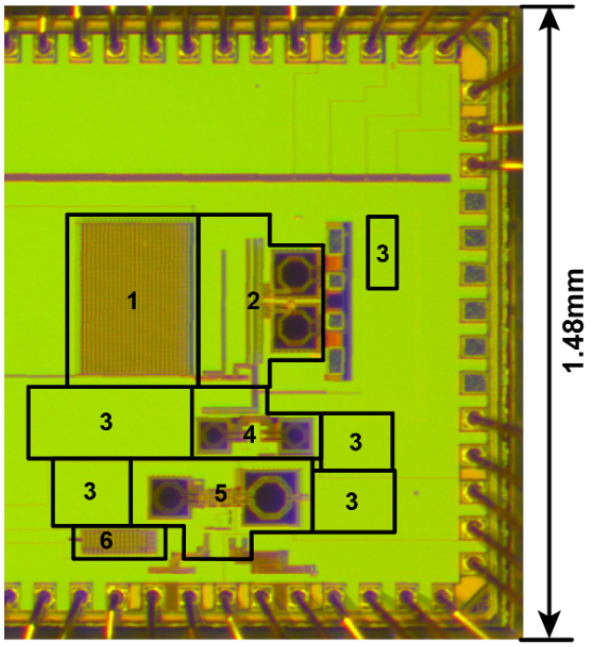


Figure 6.4: Circuit diagram of the coarse and fine FFE scheme.

6.2 Layout and Testbench Setup

The proposed TX was designed, fabricated in a 28nm planar CMOS technology (Figure 6.5). The active area of the TX is $0.5617mm^2$, in which the blocks are either generated with BAG or synthesized with digital flow and the top-level is merged manually.

Figure 6.6 shows the test bench setup for the 200Gb/s SerDes TX with SSPLL. The Keysight N8257D signal generator produces the reference clock, which is converted to differential after the Marki BAL0006 balun and connected to the test board. The chip receives the



	Block	Layout	Area (mm^2)
1	Patten Gen.	Synthesized	0.1357
2	Data Path	Generated	0.1292
3	Bias Circuit	Generated	0.1646
4	Clock Dis.	Generated	0.0472
5	PLL	Generated	0.0766
6	PLL Digital	Generated	0.0084
	Top	Manual	0.5617

Figure 6.5: Architecture of the 200Gb/s PAM-4 TX.

differential reference clocks through the K-connectors and FR4 microstrip transmission line, and generates $12.5GHz$ differential clocks. These clocks are converted to single-ended clock after the Mini-Circuits BLK-18-S+ DC block, and Marki BAL0026 balun. The Keysight N5052B signal analyzer receives one of the clocks from the HP 11667B power divider to plot its spectrum and phase noise.

The data path of chip uses clocks generated from the SSPLL clocks and the clock distribution network to produce the $100Gb/s$ NRZ and $200Gb/s$ PAM-4 PRBS-7 pattern. The high-speed data stream is probed with FormFactor I67 Infinity probe, and connects to Keysight 1046A sampling module through SHF DCB-65R DC block and Centric RF C8184 adaptor. Finally, the Keysight N1000A sampling scope gets the data, which is triggered by the amplified PLL clock with Mini-Circuits ZX60-183-S+, to plot the eye-diagram. The total channel loss of is 6dB at baud-rate frequency, due to bandwidth of probes, cables, DC blocks, adaptors and scope headers.

6.3 Measurement Results

SSPLL Test Results

In the SerDes transmitter, the same PLL with different buffer size in Chapter 4 is used, which is tested to verify its performance. Figure 6.7 shows the phase noise of the 12.5GHz

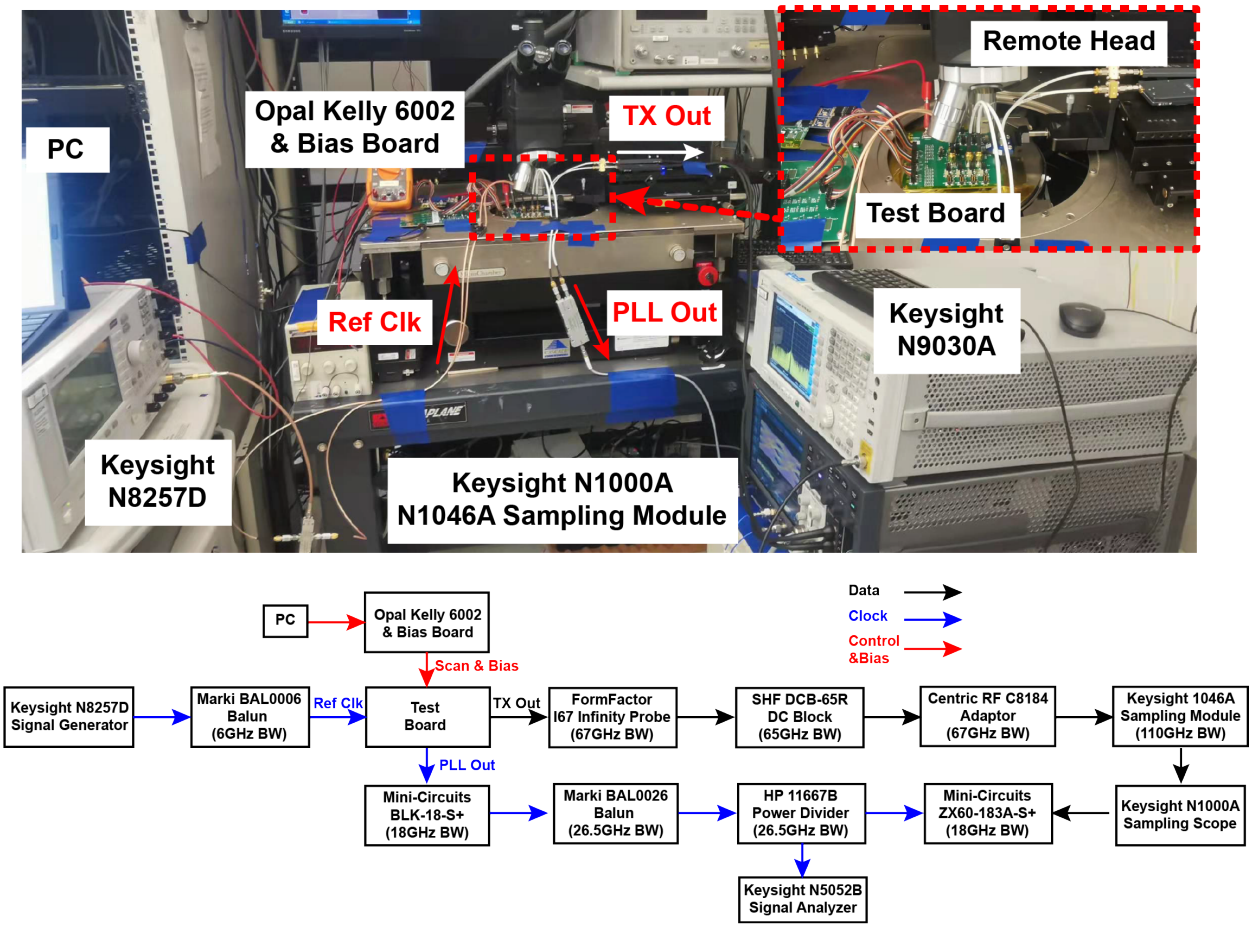


Figure 6.6: Architecture of the 200Gb/s PAM-4 TX.

PLL outputs. The phase noise at $1MHz$ offset is $-121.71dBc/Hz$, with the RMS jitter integrated from $1KHz$ to $100MHz$ being $46.49fs$.

Figure 6.8 shows the spectrum of the PLL outputs with a frequency range of $4GHz$. The power of the spur coupled from the reference is $-62.33dB$ less than the clock power. These results are almost same with the SSPLL standalone, and meet the specifications of the $200Gb/s$ SerDes TX.

Test Results of Serdes TX

Similar as Chapter 3, there are two versions for the SerDes TX design, TX with ESD and without ESD, and the test results of both of them are presented.

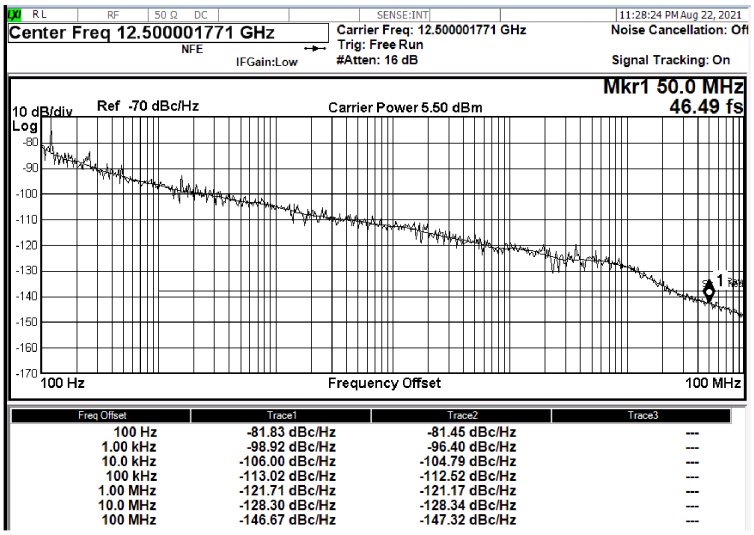


Figure 6.7: SSPLL phase noise.

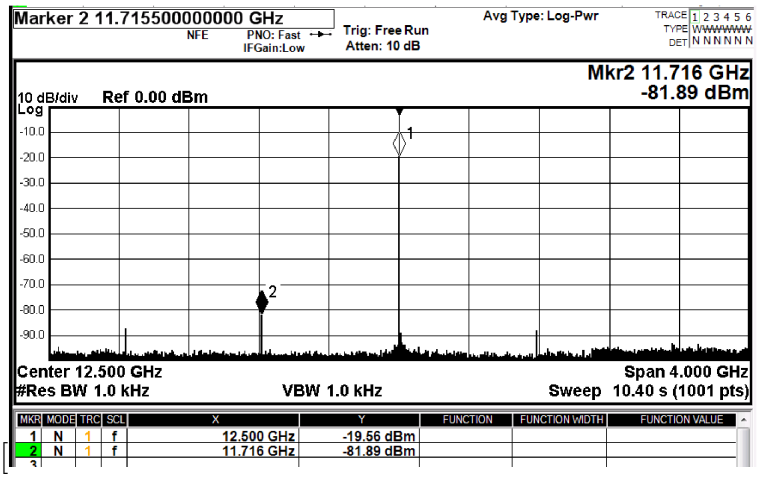


Figure 6.8: SSPLL spectrum.

Eye Diagram of Clock Pattern

Figure 6.9 shows the eye diagram of the $50GHz$ clock pattern for TX without and with ESD. For the TX without ESD, the eye amplitude is $301mV$ and the RMS jitter is $139fs$. On the other hand, for the TX with ESD, the eye amplitude is $203mV$ and the RMS jitter is $197fs$.

Eye Diagram of NRZ Pattern

Figure 6.10 shows the eye diagram of the $100Gb/s$ PRBS-7 NRZ pattern for TX with ESD, when the FFE is off. The vertical eye opening is $107mV$, and the horizontal eye opening is

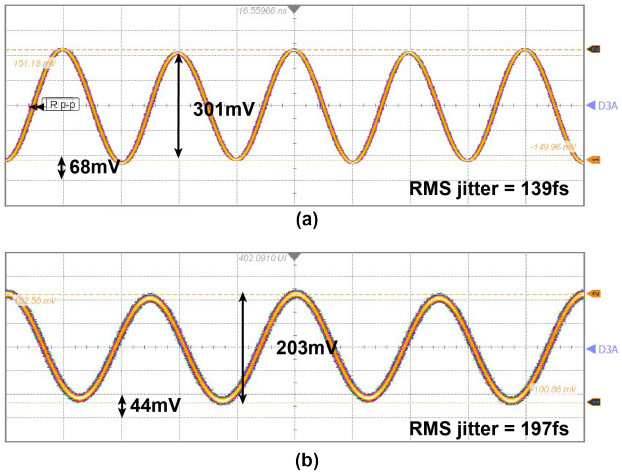


Figure 6.9: Eye diagram of $50GHz$ clock pattern for TX (a) without and (b) with ESD.

$0.57UI$.

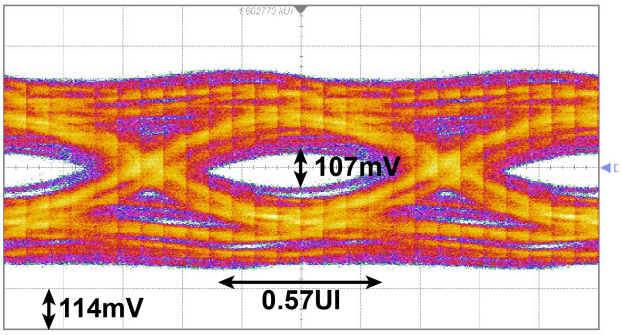


Figure 6.10: Eye diagram of $100Gb/s$ PRBS-7 NRZ pattern for TX with ESD, when the FFE is off.

Figure 6.11 shows the eye diagram of the $100Gb/s$ PRBS-7 NRZ pattern for TX without and with ESD, when the FFE is on. For the TX without ESD, the vertical eye opening is $214mV$ and the horizontal eye opening is $0.76UI$. On the other hand, for the TX with ESD, the vertical eye opening is $270mV$ and the horizontal eye opening is $0.76UI$[1].

Eye Diagram of PAM-4 Pattern

Figure 6.12 shows the eye diagram of the $100Gb/s$ PRBS-7 PAM-4 pattern for TX with ESD, when the FFE is off, the PAM-4 eye is totally closed. From the eye diagram, the output swing is about $750mV$.

[1]Generally, the TX without ESD is better than with ESD. The inconsistency of is an open mystery.

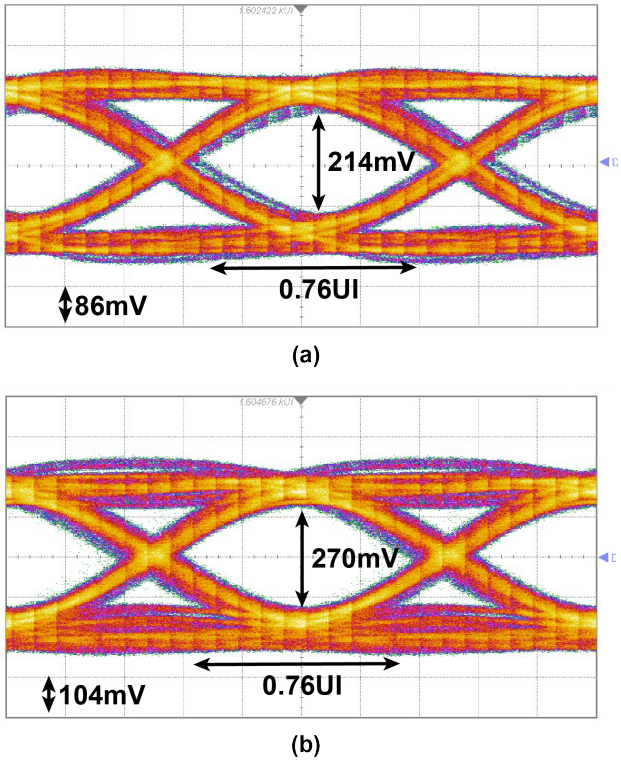


Figure 6.11: Eye diagram of $100Gb/s$ PRBS-7 NRZ pattern for TX (a) without and (b) with ESD.

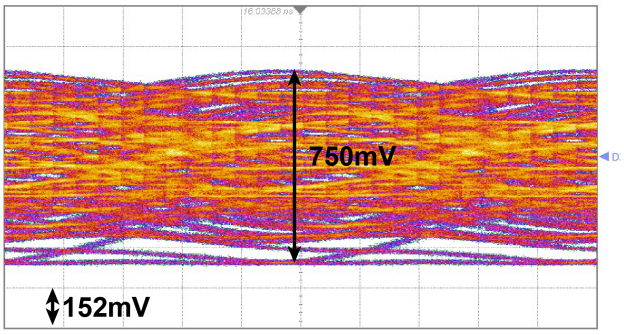


Figure 6.12: Eye diagram of $100Gb/s$ PRBS-7 PAM-4 pattern for TX with ESD, when the FFE is off.

Figure 6.13 shows the eye diagram of the $200Gb/s$ PAM-4 pattern for TX without and with ESD, when the FFE is on. For the TX without ESD, the vertical eye openings are $41mV$, $39mV$ and $35mV$, respectively, the horizontal eye openings are $0.37UI$, $0.29UI$ and $0.29UI$, respectively. For the TX with ESD, the vertical eye opening is $62mV$, $54mV$ and $60mV$

respectively, and the horizontal eye opening are $0.35UI$, $0.27UI$ and $0.33UI$ respectively.[2]. The Ratio of Level Mismatch (RLM) are 95.6% and 96.7%, meeting the requirement of $> 95\%$ from standards [39], [40].

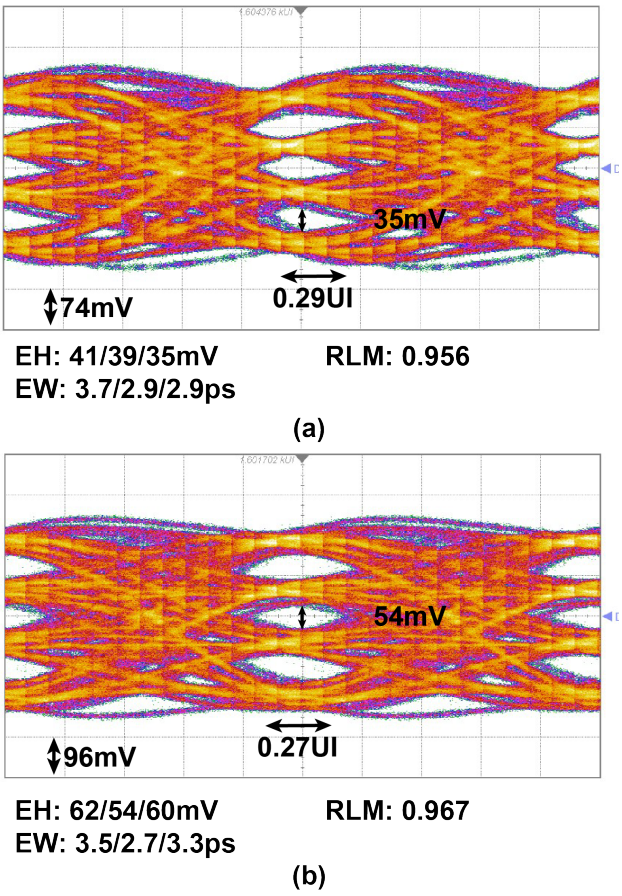


Figure 6.13: Eye diagram of $100Gb/s$ PRBS-7 NRZ pattern for TX (a) without and (b) with ESD.

Pulse Response and Channel Loss

Figure 6.14 shows the pulse responses and the channel losses of the TX with ESD. By properly setting the 1-tap and 2-tap post cursor FFE as labeled below Figure 6.14 (a), the inter-symbol interference (ISI) is eliminated, including the first post-cursor ISI with ratio 0.34 of the main cursor.

The channel loss of the whole signal path, including the driver, probe, DC-block, cable, adaptor and scope remote head is calculated by the inverse Fourier transform. When the

[2]Similar to the NRZ case, the inconsistency of eye-diagram is an open mystery.

FFE is off, the normalized loss at baud-rate frequency is $-11.7dB$, and the FFE improves it by about $4.5dB$.

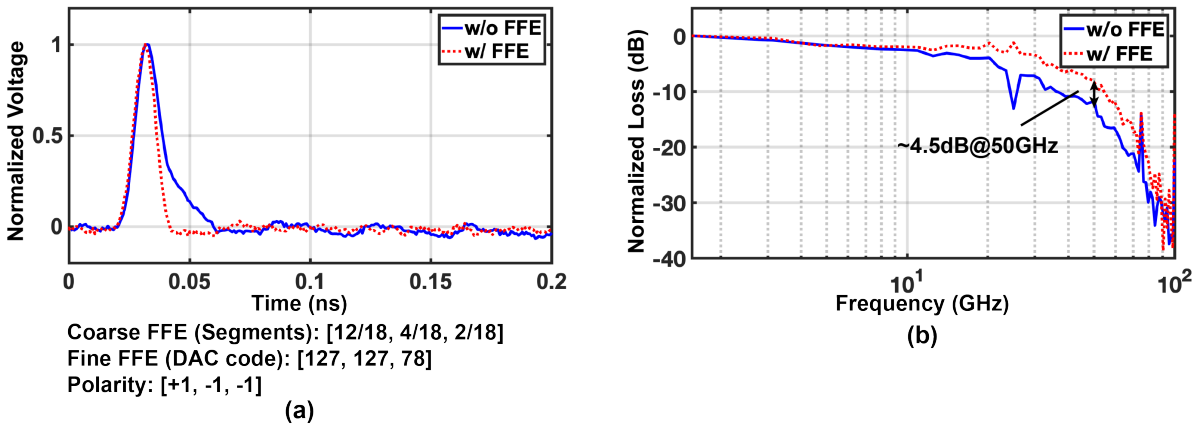


Figure 6.14: TX (a) pulse response and (b) channel loss from inverse Fourier transform.

6.4 Summary and Comparison Table

The whole TX consumes 937mW, with 17mW in SSPLL, 348mW in clock distribution and 566mW in data path (Figure 6.15). For $200Gb/s$ PAM-4 data, the efficiency is $4.69pJ/bit$, while the efficiency is $9.37pJ/bit$ with $100Gb/s$ NRZ data.

Figure 6.1 compares the TX performance with other state-of-the-art designs, showing the highest data-rate with an on-chip PLL at good power efficiency for a design in a standard planar CMOS process using generator-based design flow.

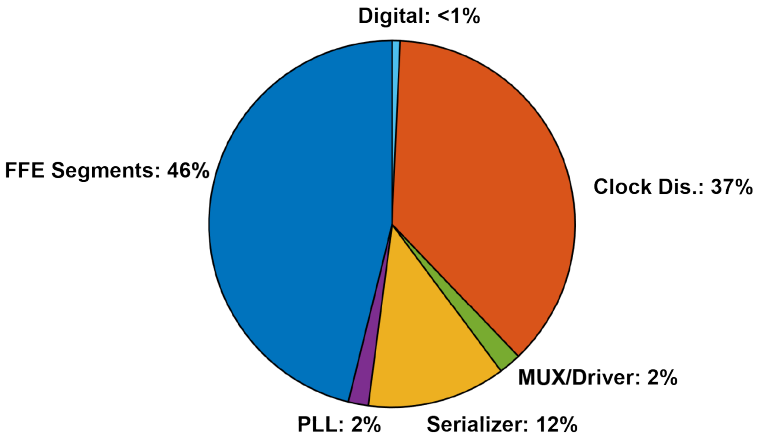


Figure 6.15: TX power breakdown.

Table 6.1: TX performance comparison.

	ISSCC'21 [41]	ISSCC'21 [34]		ISSCC'18 [5]		ISSCC'20 [12]	ISSCC'21 [63]	ISSCC'21 [64]	This Work	
Architecture	Quarter-rate	Quarter-rate		Quarter-rate		Quarter-rate	Quarter-rate	Quarter-rate	Quarter-rate	
Clock Source	On-chip	External		On-chip		External	External	External	On-chip	
Output Swing w/o FFE	$1.0V_{ppd}$	$0.8V_{ppd}$		$0.75V_{ppd}$		$0.56V_{ppd}$	-	-	$0.75V_{ppd}$	
FFE	8-tap	5-tap		3-tap		8-tap	8-tap	5-tap	5-tap	
ESD	Yes	Yes		No		Yes	Yes	Yes	Yes	
RJ(fs_{rms})	65 (4MHz CDR)	204		150		-	-	-	134	
Signaling	PAM-4	PAM-4	NRZ	PAM-4	NRZ	NRZ-4	PAM-4	PAM-4	PAM-4	NRZ
Data Rate (Gb/s)	224	180	90	112	56	100	112	112	200	100
Efficiency (pJ/bit)	2.25	4.59*	9.18*	1.72	3.44	6.19*	1.40*	1.71	4.69	9.37
Eye Height (mV)	90	53	234	30	260	73	59	46	51	270
Active Area (mm^2)	0.088	0.432		0.0302		0.504	0.032	0.228	0.541	

*Excluding PLL

Chapter 7

Conclusions

7.1 Thesis Summary

In ultra-high-speed wireline transceivers, the design of clock generation and distribution circuits has becomes increasingly complex and time-consuming. while the development and usage of new FinFET processes make the situation even worse. In this thesis, we focus on the design of energy-efficient clock generation and distribution network for a 28/32$Gbps$ SerDes and 200$Gbps$ PAM-4 transmitter with generator-based design methodology using BAG, which accelerates the design procedure, while satisfying the performance requirements.

The BBPLL generator for 28/32$Gbps$ SerDes that using top-down and bottom-up design methodology is reported. The design methodologies for the PLL generator are classified into three types: the direct-sizing method, look-up table method and iteration loop method. After the system-level analysis, the generator for the inductor, varactor, MOM capacitor, CapDAC switch and VCO are proposed using these methodologies. Three 14GHz PLLs are instantiated in TSMC 16nm, GF 14nm and Intel 22nm technologies, demonstrating the process portability. The generation time each design is less than four days, which enables fast PLL design and technology porting. The PLL design in TSMC 16nm shows RMS jitter of 565.4fs, power of 6.64mW and a FOM value of -236.7.

Furthermore, a flexible clock distribution network for a 200$Gbps$ PAM-4 transmitter is designed using the BAG layout generators in 28nm CMOS technology. The C8 clock distribution circuit with delay variable satisfies the timing constrains of different data path stages at all PVT corners, and the C4 clock distribution circuit with duty-cycle and quadrature error correction eliminates the clock-related distortion of the eye-diagram. With an eye opening with $> 52.9mV$ eye height, 0.36UI eye width, 98% RLM and 4.63pJ/b at 200$Gbps$ PAM-4 signaling under $> 6dB$ channel loss at 50GHz, the proposed TX demonstrates the highest data rate achieved using a planar process.

Finally, a sub-100fs sub-sampling PLL is generated with BAG, and merged with the data path and clock distribution circuit. The hybrid architecture is used to remove the capacitor

in the LF, and the type-I loop with tri-state integral path eliminates the voltage ripples of the hybrid loop. In the measurement, the PLL offers a RMS jitter of $44fs$ at $28GHz$ output, and a spur of $-56.6dB$, which results in the FOM value $-254.8dB$. The transmitter data path, achieving 4.69 pJ/bit efficiency, $54mV$ eye height, $0.27UI$ eye width, and 97% RLM, showing the fastest TX system using a planar process.

7.2 Future Directions

With the $200Gbps$ TX layout generator proposed in this thesis, it becomes possible to investigate more design directions. First, just like the BBPLL generator, it will be interesting to build a circuit generator of the data path, clock distribution network and PLL, which can design the system automatically meeting the data rate and jitter requirements.

Based on the low-level layout generators, more circuits such as the 200Gbps CDR, or even receiver can be designed. The fractional-N PLL based on the type-I hybrid SSPLL with tri-state path is also a direction to explore, as between $20-30GHz$ the designs with jitter performance below $50fs$ are rare.

Taking a step forward, with further requirement of the data roaming and information explosion, the data rate of $400Gbps$ will be the aim the next generation SerDes. The PAM8 modulation scheme or even faster PAM4 architectures are potential options. The generator-based design methodologies can play a significant role in these designs.

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Appendix A

VCO Frequency Optimization

In Chapter 2, the object of frequency range and frequency resolution for VCO design is decideing the sizes of CapDAC, fine varactor,integral varactor and proportional varactor, while maximizing the tank quality factor. This is done with a two-steps design strategy. First, the CapDAC and varactor are sized, with C_{exp}, C_{int} and C_{prop} labeled as a fixed capacitor C'_{exp}. Then the quality factor of the tank is

$$Q_{tot,1} = C_{tot}/(\frac{(2^N-1)C_{on}}{Q_{CapDAC}} + \frac{C_{fine,avg}}{Q_{fine}}) \tag{A.1}$$

where C_{tot} is the total capacitance, Q_{CapDAC} is the quality factor of the CapDAC, i.e. $\omega C R_{sw}/N_{sw}$, Q_{fine} is the quality factor of the fine varactor, and C_{fine_avg} is the average capacitance of the fine varactor. Then the maximum frequency f_{max} and minimum frequency f_{min} are

$$f_{max} = \frac{1}{2\pi\sqrt{L(C_m + (2^N-1)C_{off} + C_{fine,min})}} \tag{A.2}$$

$$f_{min} = \frac{1}{2\pi\sqrt{L(C_m + (2^N-1)C_{on} + C_{fine,max})}} \tag{A.3}$$

where C_m is $C_L + C_{cp} + C_{par} + C'_{exp}$, including the capacitance of the load, cross-coupled pair, routing parasitic and C'_{exp}, C_{on} is C, C_{off} is $C||(C_p + N_{sw}C_{sw})$, and $C_{fine,max}$ and $C_{fine,min}$ are the maximum and minimum capacitance of the fine varactor. To guarantee enough coverage between the frequency band, the tuning range of the varactor should be larger than the CapDAC tuning step.

$$C_{fine,max} - C_{fine,min} \geq \delta(C_{on} - C_{off}) \tag{A.4}$$

where coverage ratio δ is a ratio factor larger than one. Therefore, the optimization problem is the A.5, where $f_{0,max}$ and $f_{0,min}$ are the target maximum and minimum frequencies, and the variables are the CapDAC switch size N_{sw}, unit capacitance C, and fine tuning varactor C_{fine_avg}.

$$\begin{aligned}
&\max_{N_{sw},C,C_{fine}} C_{tot}/(\frac{(2^N-1)C_{on}}{Q_{CapDAC}}+\frac{C_{fine,avg}}{Q_{fine}}) \\
s.t.& \\
C_{fine,max}-C_{fine,min} &\geq \delta(C_{on}-C_{off}) \\
f_{0,min} &\geq 1/2\pi\sqrt{LC_{max}} \\
f_{0,max} &\leq 1/2\pi\sqrt{LC_{min}} \\
C_{max} &= C_m+(2^N-1)C_{on}+C_{fine,max} \\
C_{min} &= C_m+(2^N-1)C_{on}+C_{fine,min} \\
C_m &= C_L+C_{cp}+C_{par}+C'_{exp} \\
C_{tot} &= C_m+2^{N-1}(C_{on}+C_{off})+C_{fine,avg} \\
C_{on} &= C \\
C_{off} &= C||(C_p+N_{sw}C_{sw}) \\
Q_{CapDAC} &= \omega C R_{sw}/N_{sw} \\
Q_{fine} &= \omega C_{fine,avg} R_{fine}
\end{aligned} \tag{A.5}$$

Similarly, the quality factor of the integral varactor and proportional varactor is

$$Q_{tot,2}=C_{tot}/(\frac{C_{int,avg}}{Q_{int}}+\frac{C_{prop,avg}}{Q_{prop}}) \tag{A.6}$$

where C_{tot} is the total capacitance, $C_{int,avg}$ is the average capacitance of the integral varactor, Q_{int} is the quality factor of the integral varactor, $C_{prop,avg}$ is the average capacitance of the integral varactor, Q_{prop} is the quality factor of the integral varactor. The size of the fine tuning varactor should be large enough to meet frequency overlapping specification, and small enough that the capacitance variation is tiny compared with proportional control to avoid the limit cycle jitter contribution. The equations A.7 and A.8 are derived

$$C_{int,max}-C_{int,min} \geq (C_{fine,max}-C_{fine,min})/2^{N_1} \tag{A.7}$$

$$C_{prop,max}-C_{prop,min} \gg (C_{int,max}-C_{int,min})/2^{N_2} \tag{A.8}$$

where $C_{int,max}$ is the maximum capacitance of integral varactor, $C_{int,max}$ is the minimum capacitance of integral varactor, $C_{prop,max}$ is the maximum capacitance of proportional varactor, and $C_{prop,max}$ is the minimum capacitance of proportional varactor. The proportional frequency tuning range is determined with system analysis

$$\Delta f_{0,prop} = f_{prop,max} - f_{prop,min} \tag{A.9}$$

$f_{0,prop}$ is the proportional frequency step specification, and $f_{prop,max}$ and $f_{prop,max}$ is the maximum and minimum frequency when changing the proportional varactor. Therefore, the optimization problem is shown in Equation A.10, where the variables are integral varactor $C_{int,avg}$, and proportional tuning varactor $C_{prop,avg}$.

$$\begin{aligned}
&\max_{C_{int,avg},C_{prop,avg}} C_{tot}/(\frac{C_{int,avg}}{Q_{int}} + \frac{C_{prop,avg}}{Q_{prop}}) \\
&s.t. \\
C_{int,max} - C_{int,min} &\geq (C_{fine,max} - C_{fine,min})/2^{N_1} \\
C_{prop,max} - C_{prop,min} &\gg (C_{int,max} - C_{int,min})/2^{N_2} \\
\Delta f_{0,prop} &= f_{prop,max} - f_{prop,min} \\
C_m &= C_L + C_{exp} + C_{par} + 2^{N-1}(C_{on} + C_{off}) + C_{fine,avg} \\
f_{prop,max} &= 1/2\pi\sqrt{L(C_m + C_{int,avg} + C_{prop,max})} \\
f_{prop,min} &= 1/2\pi\sqrt{L(C_m + C_{int,avg} + C_{prop,min})} \\
Q_{int} &= \omega C_{int,avg} R_{int} \\
Q_{prop} &= \omega C_{prop,avg} R_{prop} \\
C_{exp} &= C'_{exp} - C_{int,avg} - C_{prop,avg}
\end{aligned} \tag{A.10}$$

From A.5 and A.10, the sizes of CapDAC, fine varactor,integral varactor and proportional varactor are decided from frequency range and frequency resolution for VCO design with a searching algorithm in Chapter 2.