An Ultra-Low Loss Radio Frequency Beamforming Technique for Power-Constrainted Phased Array Applications

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An Ultra-Low Loss Radio Frequency Beamforming Technique for Power-Constrainted Phased Array Applications

by

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Abstract

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Phased arrays have become increasingly important as wireless networks and sensors move to higher frequencies in an effort to alleviate overcrowding, increase bandwidth and improve spatial resolution. These arrays provide significant benefits by allowing the nodes within a wireless network to quickly steer their high-gain beams, i.e. beamforming, to maximize signal strength and reduce overall interference.

However, current methods of beamforming require significant power, making them impractical for power-constrained applications. This is, in part, because the passive radio frequency (RF) structures used for phased shifting and summation in these beamformers are quite lossy and require compensation with power-hungry amplifiers. The additional power-intensive RF amplification, along with the large number of antenna elements, means modern phased arrays often consume significant amounts of power and produce large amounts of heat. Both the power consumption and thermal load create challenges for mobile and low-power applications.

To address these challenges, this work presents a fully-passive method of beamforming with better than state-of-the-art passive loss. This technique utilizes: (1) balanced impedance phase shifters, which take advantage of array symmetry to reduce the number of lossy passive components, and (2) transmission-line transformers built into the high-Q PCB antenna feed traces to enable low-loss combining and impedance transformation. The theoretical operation of the proposed fully-passive beamformer is detailed in this dissertation, with special emphasis on estimation of key performance metrics using circuit theory. To validate the theory, we present the design and test results from a prototype 4-channel, 12 GHz, RF beamforming integrated circuit (IC) utilizing the proposed technique.

To A Better Future

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Chapter 1

Introduction

1.1 Phased Array Overview

Today, phased arrays [1]–[3] or electrically steerable antennas (ESAs), are a key enabling technology for many modern wireless networks and sensors. Fig. 1.1 shows some of the many applications of phased arrays: (a) They are used in high-performance radars for planes, cars, and drones to provide single degree spatial resolution imaging [4]. (b) They enable highly focused transmit power for satellites and 5G base stations to increase range and energy efficiency [5], [6]. (c) They allow for near instantaneous digital steering of wireless beams to track fast moving objects, like planes and trains. (d) They are even being researched for Internet-of-Things applications to provide low-power spatially selective tags [7].

Phased arrays are composed of multiple antenna elements (sometimes thousands) ar-

Figure 1.1: Examples of applications using phased arrays

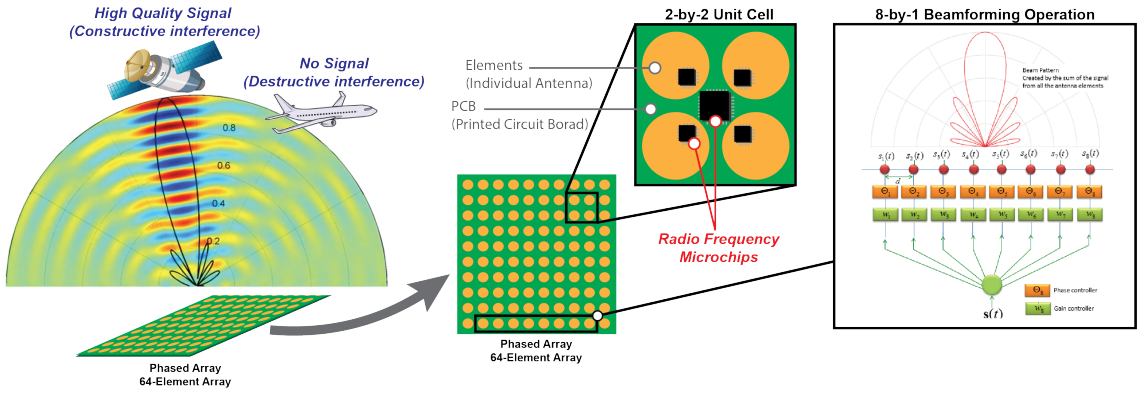


Figure 1.2: Overview of phased array function and operation showing possible realization

Table 1.1: Qualitative summary of the pros and cons associated with phased arrays

Pros	Cons
Means to linearly improve receive performance by increasing number of receive elements	Large power/component overhead for beamformer, signal distribution and processing
Greater range or higher data rate for given transmit power	Large area requirements for antenna elements
Greater spacial selectivity for interference mitigation and high-resolution imaging	Requirement for channel estimation to know where to point the beam

ranged in regular patterns. These individual antenna elements work together to receive or transmit signals with a fixed phase relationship, creating radiation patterns with regions of constructive (high gain) and destructive (low gain) interference. In this way, they are able to form narrow, high-gain wireless beams that can be programmed electronically to track objects as they move or hone in on small signals in noisy environments, as shown in Fig. 1.2. This operation of precise phase shifting and summation to form the wireless beams is called beamforming. The more antenna elements that are beamformed for the array, the higher the gain and the narrower the beam, which translate to greater range and spatial selectivity.

The theoretical operation of these beamforming arrays has been well understood for many decades [8] and they have historically been utilized in government settings for radar and astronomy [5], [9]. However, advances in in silicon radio frequency (RF) performance, integration and digital signal processing over the last decade or so have made it possible to deploy phased array antenna in a host of new applications [10].

With all that said, there are pressing power challenges to implementing phase arrays in

modern wireless networks [11]–[13]. These systems require many antenna elements, each with their own power-hungry RF signal chains and signal processing. The result being, a significant increase in RF power consumption for phased array beamforming systems when compared to omni-directional wireless systems at lower frequencies. The fact that these phase array systems usually operate at significantly higher frequencies, where silicon transistors are less efficient and per-antenna apertures are smaller, only makes the power problem worse. Even in modestly sized arrays, this added power consumption can be problematic for both battery-life and thermal management.

For broader context, Table 1.1 summarizes the high-level system benefits and drawbacks associated with phased arrays, based on current literature [1]–[3]. The high power consumption required for beamforming will be explored in detail in the following sections.

Phased Array Architectures

There are many different phased array architectures [14], each named based on where in the signal chain the associated beamforming (i.e. phase shifting and summation) takes place:

- **RF Beamforming Arrays** utilize phase shifters and power combiners in the high-frequency RF-domain [1] [6], [15]–[18].
- **Baseband Beamforming Arrays** utilize phase shifters and summation techniques at analog baseband, between the mixers and the analog-to-digital converters [2] [19], [20].
- **Digital Beamforming Arrays** implement phase shifters and summation in the digital-domain, relying on digital signal processing to construct the required beams [21], [22].

These three common phased array architectures are pictured in Fig. 1.3. Moving from digital to analog-baseband to analog-RF beamforming, the signal frequency on which the beamformer is operating goes up. This in turn increases the losses and area associated with the beamformer. Inversely, moving from analog-RF to analog-baseband to digital beamforming, the number of mixers, data converters, and amplifiers required goes up, which drives up power consumption and area. This contention between beamformer loss/area and the number of duplicated signal chain components makes it difficult to adopt a one-size-fits-all approach to phased array design. It is often necessary to consider the system requirements in detail to select the optimum array architecture for performance critical applications[3].

There has been extensive research on the trade-offs associated with each array architecture based on desired system performance - like energy efficiency, spectral efficiency, size,

[1] **LO-Beamforming Arrays** also use phase shifters and combiners in the RF-domain. In this case, the phase shifters are in the path of the local oscillator (LO).

[2] **IF-Beamforming Arrays** uses phase shifters and combiners at an intermediate frequency (IF), higher than baseband but lower than RF.

[3] The optimal system may be a hybrid of two of the architectures, a hybrid-beamforming architecture.

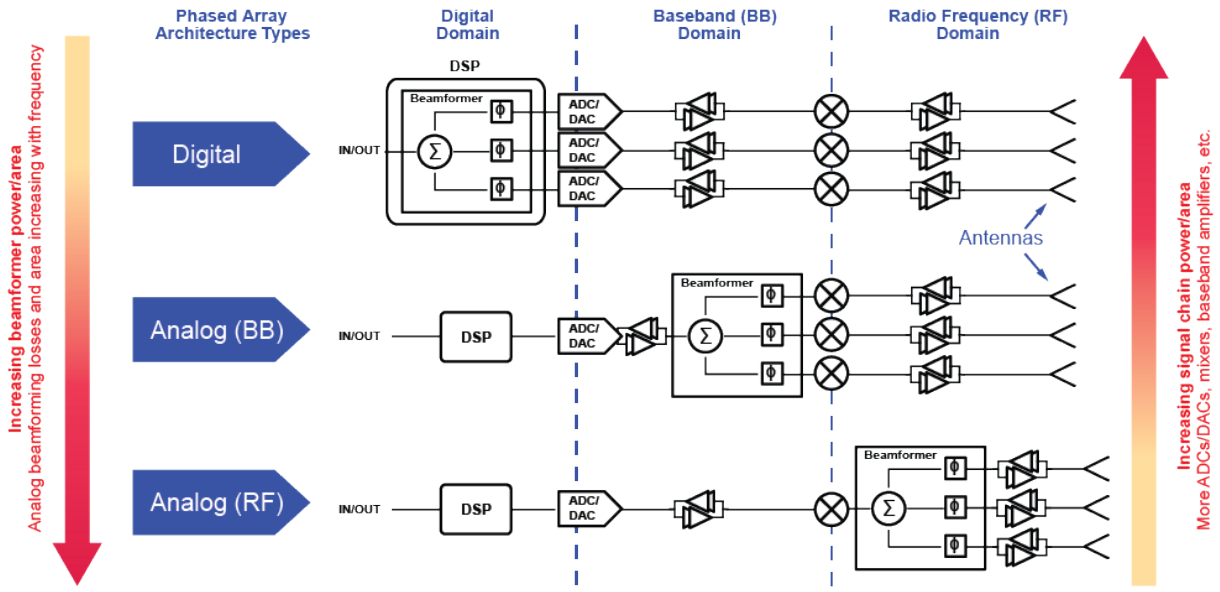


Figure 1.3: Common phased array architectures using digital, baseband and RF beamforming

and system layout [12], [13]. Detailed analysis of these trade-offs are beyond the scope of this work, however, there are a few key trends worth highlighting. First, there is growing evidence in the volume of literature and commercial deployments [6], [15]–[18] that RF beamforming architectures yield the lowest power phased arrays in situations where only one or two beams are required (e.g. in channels with limited multi-path). Savings in signal chain power due to a reduction in components (e.g. mixers, baseband amplifiers, and data converters) generally outweighs the high beamformer power consumption in RF beamforming arrays for a single-beam. Second, in spite of the high power consumption, digital, IF, and baseband beamforming architectures continue to generate notable research interest because of their significant benefits in system flexibility and multi-beam support [21]. With advances in technology nodes making digital conversion and processing less energy intensive and new techniques for reducing data converter resolution requirements in massive arrays [21], [23], interest in digital beamforming architectures is likely to grow.

RF Beamforming and Power Consumption

Given the background presented, the focus of this manuscript will be on RF beamforming techniques. They appear to hold the most promise for delivering ultra-low power phased arrays that can address the needs of applications with limited power and thermal budgets.

A more detailed block diagram of an RF beamforming phased array is shown in Fig. 1.4. Using this illustration, we can derive an equation that describes the total array power, P_{TOT}, as a function of the number of antenna elements in the array, N, and other blocks in the

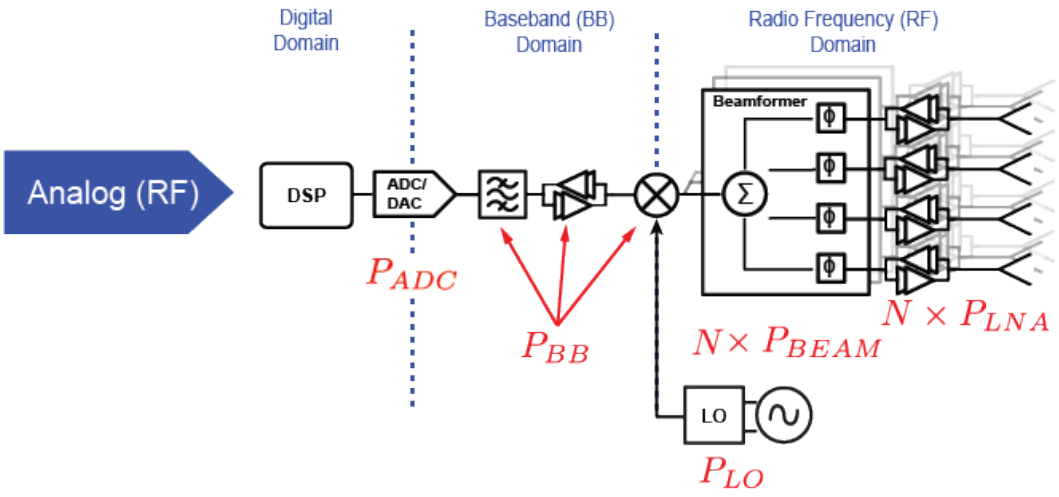


Figure 1.4: RF beamforming phased array architecture highlighting main power consumers

Table 1.2: Estimated power budget for 16- and 64-element RF beamforming phased array

Component Name	$N = 16$		$N = 64$	
	Power Consumption	Percent of Total	Power Consumption	Percent of Total
Amplifiers and Beamformers	560mW	84%	2,240mW	95%
Baseband and LO	41mW	6%	41mW	2%
ADCs	64mW	10%	64mW	3%
Total	665mW	-	2,345mW	-

signal chain. See Eq. 1.1, where P_{LNA}, P_{BEAM}, P_{LO}, P_{BB}, and P_{ADC} are the RF low noise amplifier (LNA), beamformer, local oscillator (LO), baseband, and digital converter per channel power consumption, respectively. This allows us to approximate the power budget for an RF combining array with various numbers of antenna elements.

$$P_{TOT} = NP_{LNA} + NP_{BEAM} + P_{LO} + P_{BB} + P_{ADC} \tag{1.1}$$

Substituting power consumption estimates for state of the art circuits from research literature and commercial offerings, we estimate the power budget for an RF beamforming receive phased array in Table. 1.2. Note, this assumes power per LNA (P_{LNA}) is 10mW [24], beamformer power per channel (P_{BEAM}) is 25mW [17], power for the baseband and LO ($P_{LO} + P_{BB}$) is 40.8mW [13], and power per ADC ($P_{ADC} = cB2^b$) is 32mW for a 1 GHz bandwidth (B), 6 bits (b), 494fJ/sample/step (c) data converter [13].

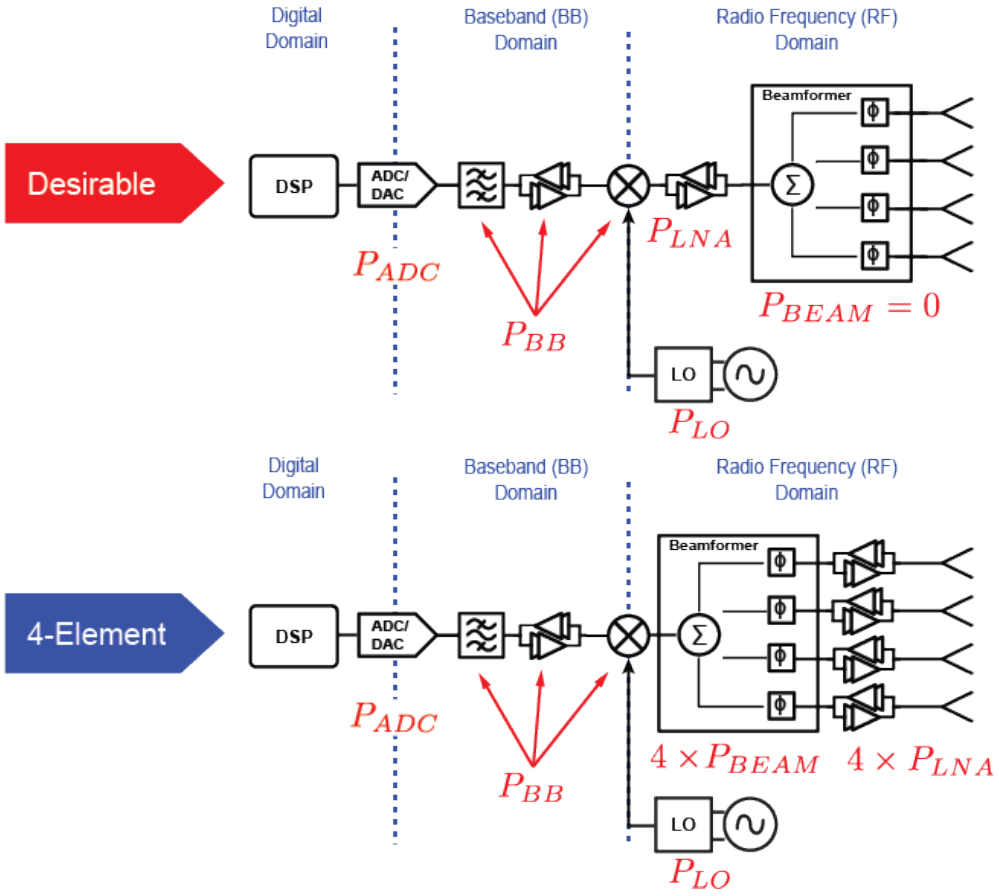


Figure 1.5: RF beamformer on the antenna node versus conventional beamformer placement

Beyond 64-elements, phased array power consumption is almost entirely dominated by the RF amplifiers and beamformers. Even for relatively small arrays with only 16 elements, RF amplifiers and beamformer still make up over 80% of the power budget. This makes solutions that address the power consumption of the RF blocks incredibly important and valuable.

For this reason, it is desirable to place a passive beamformer on the antenna node, in between the antenna and the RF amplifiers, i.e. to use a front end beamformer. This architecture, shown in Fig. 1.5 for a 4-channel beamformer, significantly reduces the number of power-hungry RF amplifiers that are required and so proportionally decreases power consumption. But it is only viable if the insertion loss (IL) of the passive beamformer is low and the linearity is high. Losses on the antenna node reduce receiver sensitivity and transmitter efficiency, while good linearity is required to support high transmit output powers.

The output power per element for most low power CMOS phased array transmitters range from 0 to 15 dBm. This means a front end beamformer with low compression and

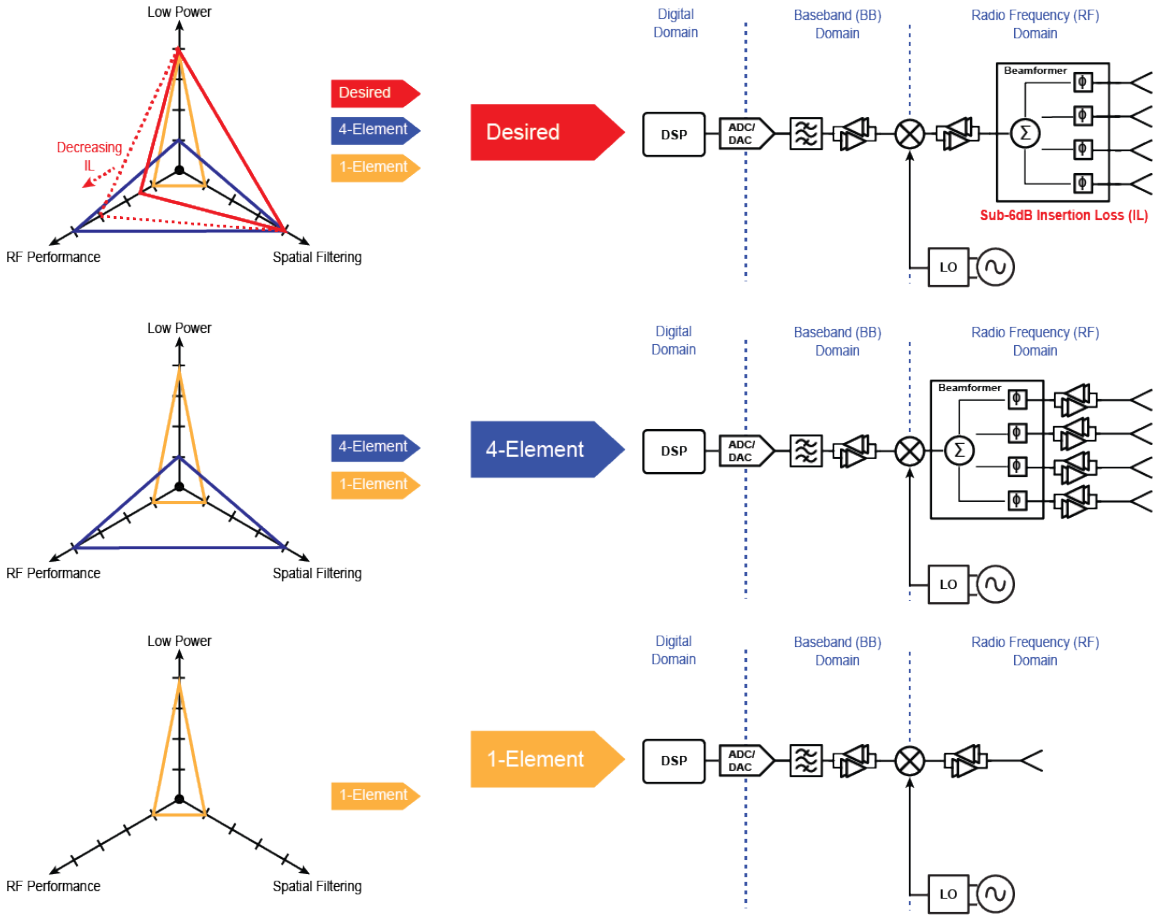


Figure 1.6: System level performance for phased array versus beamformer placement

distortion at 15 dBm or higher. For the IL, lower is always better. However, ensuring that the IL is less than the combiner gain is an important benchmark for a passive beamforming system, e.g. less than 6 dB loss for a 4-element passive RF beamformer. Adding a 4-element passive RF beamformer with IL = -6 dB to the antenna node increases spacial selectivity by four at the expense of a four fold increase in antenna count, without compromising RF performance or power consumption. As the beamformer IL decreases, the RF performance of the system with the added beamformer improves and this trade off becomes more favorable, as illustrated in Fig. 1.6.

Designing a fully passive RF beamformer with low IL (below the combiner gain benchmark), high linearity, and reasonable resolution to enable ultra-low power beamforming phased arrays is the key motivation for this work.

1.2 Modern RF Beamforming Techniques

Section 1.1 introduced briefly the benefits and applications of phased arrays, discussed the more popular architectures with a special emphasis on RF beamforming arrays because of their low power potential, and motivated through numerical example the need for a fully passive RF beamformer with low IL and high linearity to enable ultra-low power beamforming phased arrays. This section will review state-of-the-art RF beamforming techniques and explore why they historically have been so power-intensive and or lossy.

Most state of the art K/Ka-band [6], [16], [17], [25]–[30] and X/Ku-band [18], [31]–[34] RF beamformers use a combination of Wilkinson combiners [35] for power combining and vector modulators or switch-type passive phase shifters for phase shifting [36]. Unfortunately, RF beamformers realized in this way require RF amplifiers to compensate for lossy passive phase shifters and combiners, or use active RF vector modulators with built-in gain. In both cases, the active RF components consume significant amounts of power to generate low-noise, low-distortion gain at these high frequencies.

Wilkinson Combiners

Wilkinson combiners [35] are a common choice for RF power combining because of their simple design, requiring only a couple quarter–wavelength transmission lines and a shunt resistor for isolation, see Fig. 1.7. The transmission lines are realized using lumped components or controlled impedance traces to optimize area and losses for the given application frequency. Since, the length of the quarter–wavelength transmission lines are inversely proportional to the RF frequency while per-unit length conductor losses are roughly proportional to RF frequency, the Wilkinson combiner has a relatively flat loss as a function of frequency. On-chip Ku/K/Ka-band, 2-to-1 Wilkinson combiner implementations from modern literature show a roughly 1 dB IL [29], [30].

Due to the difficulty of routing high frequency connections for the isolation resistors when there are more than two input ports, high order combiners are typically implemented by cascading multiple to 2-to-1 Wilkinson combiners. Therefore, a 4-to-1 combiner typically exhibits 2 dB of IL [26], [28], [33]. This value of 2 dB IL will serve as a reference when comparing phase shifter losses in the literature, which do not include a power combiner, to this work and other beamformer publications, which do include combiner losses.

Active Phase Shifters

Active phase shifters use RF amplifiers to implement the required phase shift. The most common circuit in this category is the vector modulator (VM) [26], [28], [31], [32], shown in Fig. 1.8. VMs decompose an RF signal into two orthogonal phase components (I and Q), then use a weighted sum to impart a phase shift. Because these techniques require active devices operating at very high frequencies, they consume significant power to preserve

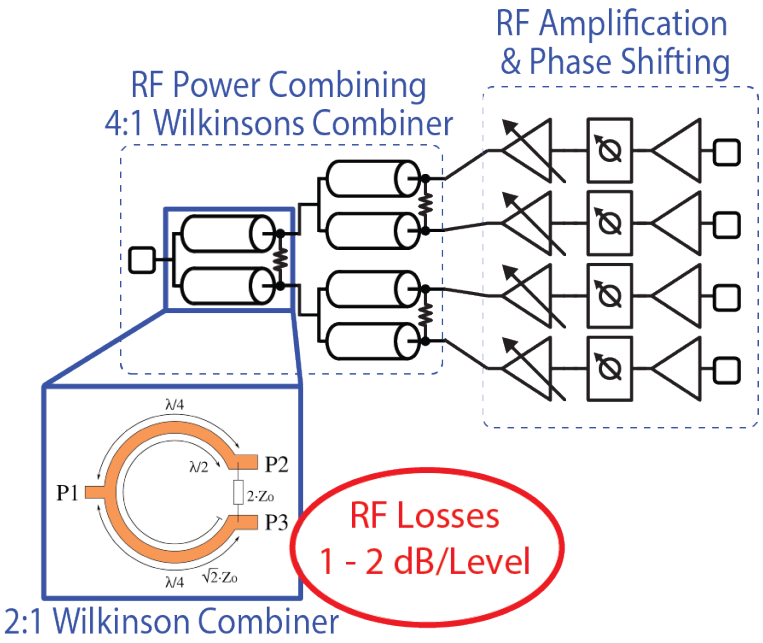


Figure 1.7: Example Wilkinson combiner

linearity and minimize added noise. VM power consumption in recent literature ranges from 28mW [26] to over a 100mW [28].

Although they consume a lot of power, VMs can provide high resolution phase and gain control which is beneficial for certain high-performance applications where precise beam steering and tapering are required. Such power-intensive active phase shifting techniques are not desirable for ultra low power applications which are the focus of this work.

Switch-Type Passive Phase Shifters

Generally, passive phase shifters rely on switches to change the circuit characteristics so as to alter the phase of the RF signal, see Fig. 1.8. These phase shifters are often implemented in unit cells, each capable of creating some fixed delay, which are then cascaded to improve the tuning range and resolution (i.e. the number of bits) . The cascade of passive phase shifting unit cells results in high insertion losses due to the cumulative on-state resistance and off-state parasitics of the switching elements, in addition to passive component losses.

Passive phase shifters have been realized in silicon CMOS [27], [29], [33], [34], [37]–[39], GaAs MMIC [40]–[45], and MEMs [46]–[52] processes, among others. The IL versus frequency for recent work from 10 to 40 GHz and 4-to-6 bits in this area is listed in Table 1.2 and plotted Fig. 1.9. The IL for both silicon CMOS and GaAs MMIC phase shifters in this frequency and resolution range is roughly 6 dB or worse.

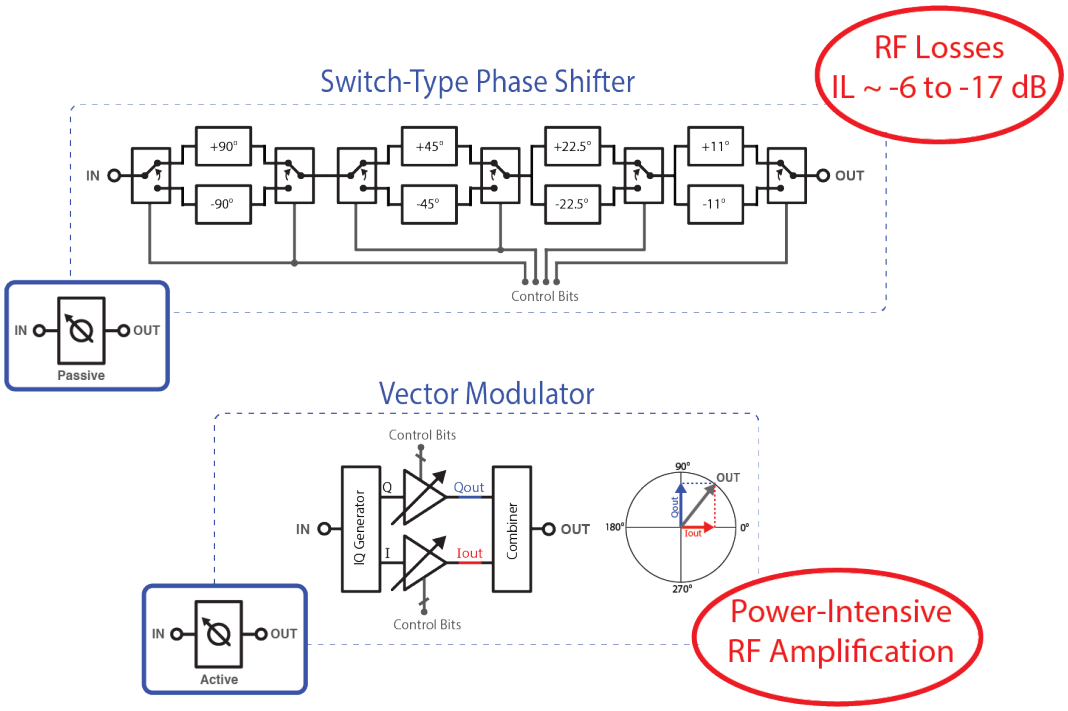


Figure 1.8: Example vector modulator (VM) and passive switch-type phase shifter

When we factor in another 2 dB of loss from an on-chip 4-to-1 Wilkinson combiner, modern RF beamformers realized using these passive switch-type phase shifters exhibit large passive IL in excess of 8 dB for 4-to-1 combiners [16], [17], [27], [29], [30], [33], [34]. See Table 1.4. Ultimately, passive phase shifter implementations currently available in silicon CMOS or GaAs are too lossy to be used on the antenna node.

While MEMs processes can realize significantly lower phase shifter IL, as low as 1.3 dB, they are much harder to integrate into a modern phased array system. MEMs devices typically require very large control voltages (>10V), special vacuum sealed packaging to ensure reliability, extensive footprints because of their large minimum feature size, and expensive manufacturing processes that don't integrate well with silicon CMOS. The desired phase shifter would have IL comparable to MEMs but offer the integration flexibility of silicon CMOS, see Fig. 1.10.

Fully Passive RF Beamformers

Less common passive beamforming architectures, like frequency scanned arrays [53], [54], Rotman lenses [55], Butler matrix [56], and Van Atta arrays [7], [57], would also meet the power requirements for mobile phased array applications. But in practice they have not been an attractive option because of their size, high RF losses and limited scan range.

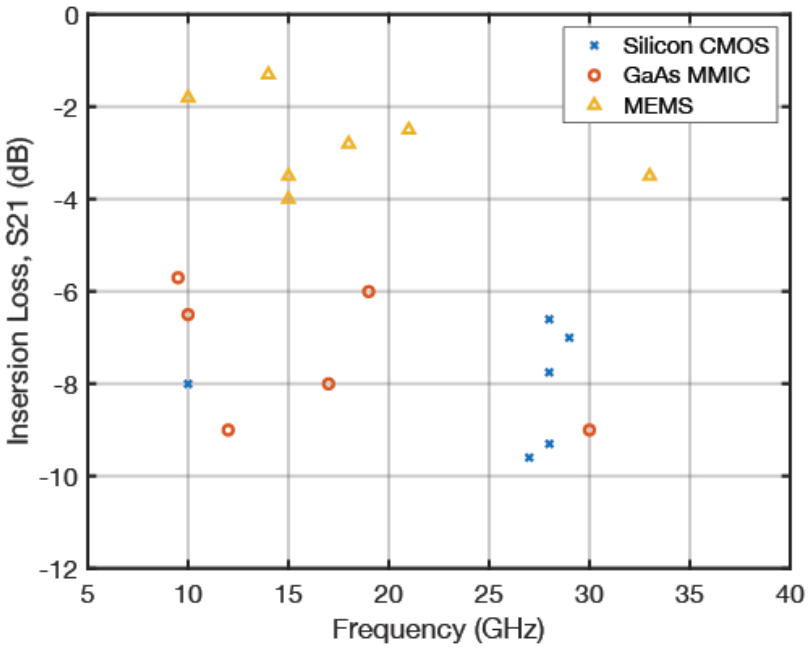


Figure 1.9: Survey of 4-to-6 bit phase shifter IL operating between 10 and 40 GHz

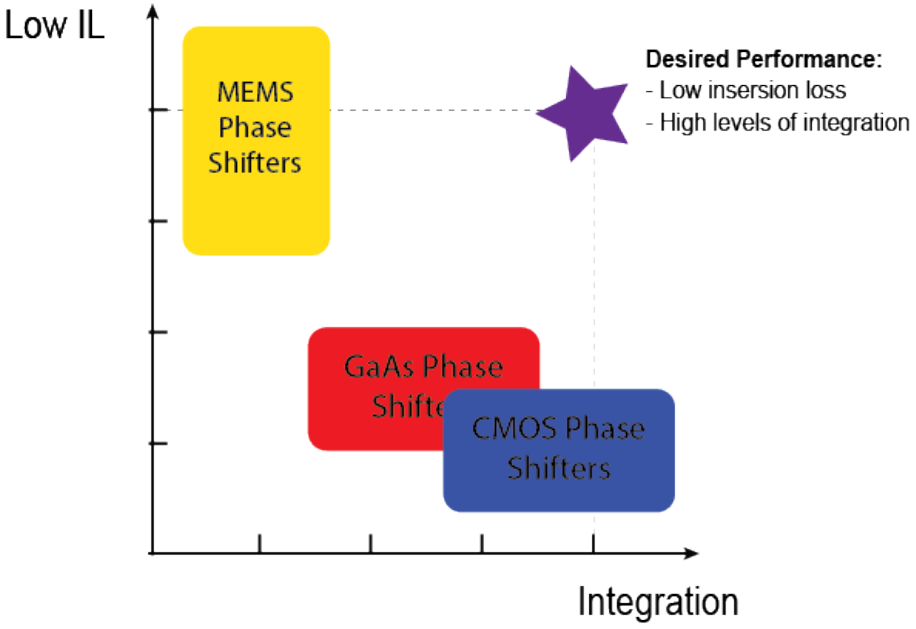


Figure 1.10: Desired passive phase shifter performance and integration

Table 1.3: Modern 4-to-6 bit switched passive phase shifters IL performance

Source	**Freq**	**IL**	**Bits**	**Type**	**Category**
RFIC 2016 [37]	28GHz	-17dB	6	TLine	Si CMOS (SiGe)
RFIC 2016 [27]	27GHz	-9.6dB	5	HP-LP	Si CMOS (45nm SOI)
TMTT 2011 [33]	10GHz	-8dB	5	HP-LP	Si CMOS (0.13μm)
AMPC 2018 [34]	18GHz	-17dB	5	HP-LP	Si CMOS (0.18μm)
MWCL 2016 [38]	28GHz	-7.6dB	4	HP-LP	Si CMOS (65nm Bulk)
RFIC 2017 [29]	29GHz	-7dB	6	HP-LP	Si CMOS (45nm SOI)
TMTT 2017 [39]	28GHz	-8dB	5	Reflection	Si CMOS (65nm Bulk)
ICCC 2017 [40]	10GHz	-6.5dB	6	HP-LP	GaAs MMIC (0.25μm)
TMTT 2000 [41]	19GHz	-6dB	5	HP-LP	GaAs MMIC (0.25μm)
IMS 1982 [42]	9.5GHz	-5.7dB	4	Loaded Line	GaAs MMIC (1000μm)
Qorvo 2019 [43]	12GHz	-9dB	6	HP-LP	GaAs MMIC (0.15μm)
Qorvo 2019 [44]	17GHz	-8dB	6	HP-LP	GaAs MMIC (0.15μm)
Qorvo 2021 [45]	30GHz	-7dB	5	HP-LP	GaAs MMIC (0.25μm)
TMTT 2015 [46]	15GHz	-3.5dB	5	TLine	MEMS (635μm Alumina)
CSICS 2008 [47]	18GHz	-2.8dB	6	TLine	MEMS (250μm Alumina)
IMS 2012 [48]	21GHz	-2.5dB	4	Loaded Line	MEMS (Alumina)
TMTT 2013 [49]	15GHz	-4dB	4	Loaded Line	MEMS (500μm Quartz)
MGWL 1999 [50]	33GHz	-3.5dB	4	TLine	MEMS (Hi-Res Silicon)
TMTT 2006 [51]	14GHz	-1.3dB	4	TLine	MEMS (LCP)
TMTT 2003 [52]	10GHz	-1.8dB	4	TLine	MEMS (200μm GaAs)

Table 1.4: Passive IL for select modern X/Ku/K/Ka-Band RF beamformers

FOM	2018 ISSCC [17]	2017 RFIC [29]	2018 JSSCC [30]	2011 TMTT [33]
Technology	28nm CMOS	45nm CMOS	28nm CMOS	0.13μm CMOS
Freq (GHz)	28	25-33	25-28	9-10
# of Channels	24	2	8	4
# of RX/TX	24 / 24	2 / 2	8 / 8	4 / 0
Phase Shifter Type	Passive	HP-LP	HP-LP	HP-LP
Combiner Type	Wilkinson	Wilkinson	Wilkinson	Wilkinson
Phase Shifter IL (dB)	-7	-7	-9	-8
Combiner IL* (dB)	-2	-2	-2	-2.1
Total Passive IL (dB)	**-9**	**-9**	**-11**	**-10.1**

* Based on stated values or estimated -2 dB value for 4-to-1 Wilkinson combiner

Newer approaches such as [58], which reduce the number of lossy passives needed for phase shifting and use high-Q PCB traces for power combining, have the potential to overcome some of these challenges, but have not been demonstrated at high enough frequencies or with sufficient antenna elements and integration to be considered for most phased array systems.

1.3 Proposed Passive RF Beamformer

To address the high loss and power consumption of state-of-the-art beamformers, a technique for performing RF phase shifting and summation with very low loss and zero active power consumption is presented here. The proposed beamformer uses transmission-line transformers (TLTs) [59] incorporated into the feed lines and balanced passive impedance tuning to construct an RF beamforming phased array [58]. Utilizing the feed structure for signal combining eliminates the need for additional lossy RF combining structures and the use of balanced passive impedance tuning reduces the complexity associated with phase shifting. Altogether this allows for the realization of a simple, low power and low loss RF beamformer at a broad range of frequencies.

The proposed beamformer further improves upon previous designs [58] by incorporating a differential crossover switch into the phase shifters, extending their range of operations to the full $\pm 180°$, making it possible to realize phased arrays with more elements and wider scan angles [60]. Additionally, to address issues of integration and demonstrate the technique at a more relevant frequency for phased array applications, the proposed beamformer was designed to operate at 12 GHz and integrated into a CMOS RF integrated circuit (RFIC).

The resulting work is a completely integrated, passive, 4-channel, beamforming RFIC at 12 GHz with very low loss. The RFIC beamformer uses balanced impedance phase shifters (BIPS), which take advantage of array symmetry to reduce the number of lossy passive components, and transmission-line transformers built into the high-Q PCB antenna feed traces to enable low-loss combining and impedance transformation. Using this new architecture, the measured passive loss is only 5.4 dB, significantly less than state-of-the-art for comparable beamformers and phase shifters, while supporting all possible beam angles and greater than 5-bits of phase shifter resolution.

The high-level structure and operational principle of the beamformer with the balanced impedance tuning (BIT) algorithm are shown in Fig. 1.11. Antenna elements are connected in series at the chip input with the load impedance fed by the beamformer (R_L) designed to be four times the radiation resistance of the antenna elements in the array to ensure optimal power transfer. The RF feed lines connecting the antennas to the IC are designed to also function as transmission-line transformers (TLTs), transforming the effective common-mode impedance seen at the input of the IC to a large real value in order to facilitate low-loss and wide bandwidth series combining without affecting the differential-mode impedance. A balanced impedance phase shifting technique is utilized to enable low-loss phase shifting and beamforming. The receiver configuration is described here. Via reciprocity, the transmit configuration would work in an identical way.

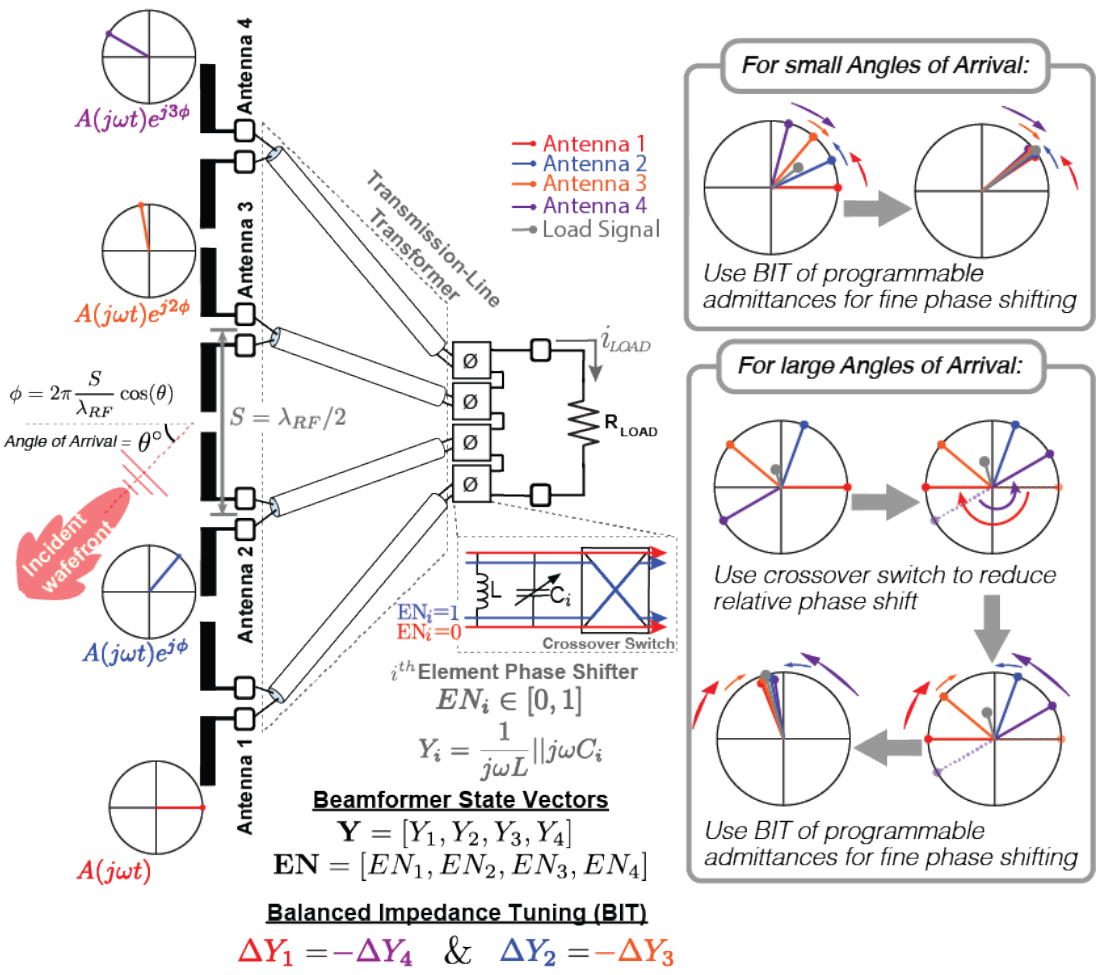


Figure 1.11: Proposed four-element series connected array with low-loss passive beamformer

1.4 Thesis Organization

The theory and conceptual workings of the proposed low-loss passive beamformer are described in Chapter 2. This includes a description of power-combining using TLTs and the phase shifters using balanced impedance tuning with crossover switches for extended scan angle. In Chapter 3, the design of the prototype RFIC and antenna array are detailed. The realization of the high-impedance PCB TLTs and antenna elements as well as key on-chip components, like the phase shifters and input matching network, are highlighted. Chapter 4 reports the experimental setup, simulation environment, and measurement results obtained using the prototype array and custom RFIC. Finally, Chapter 5 concludes this work with a brief summary and comments about possible directions for future research.

Chapter 2

Theory

There are two major components which enable the proposed fully-passive RF beamforming introduced in Section 1.3. The first is transmission-line transformers (TLTs) built into the RF feed lines, which serve to condition the signals from each antenna element for simple low-loss series combining in the RF-domain. TLT-base power combining is described in Section 2.1 and 2.2. The second is balanced impedance tuning of passives for phase shifting, which utilize array symmetry to reduce component counts and realize a basic low-loss phase shifter. The balanced impedance phase shifter (BIPS) is described in Section 2.3 and 2.4. Both of these techniques work together to reduce the number of lossy components and traces in the RF path and provide a beneficial impedance transformation, resulting in a potentially lower-loss RF beamformer, as shown in Fig. 2.1. Note, the analysis that follows is for the receive configuration but holds for transmit as well, since the structures are passive and reciprocal.

2.1 Power-Combining with Transmission-Line Transformers (TLTs)

Transmission-line transformers (TLTs) [59] have been used for impedance transformation for many years. More recently, series voltage combining using TLTs has been proposed in the design of high power output RF power amplifiers [61], [62]. They can also be used to transform the effective common-mode impedance of differential antenna in an array to a large magnitude value, enabling simple series connections for power combining. Since physically separated RF antennas require transmission (or feed) lines to route signals to a centralized location for processing, with minimal modification, these feed lines can also implement a TLT that can be used for low-loss signal combining in the RF domain. To our knowledge, the use of a TLT to combine signals from multiple antennas in a phased array was first demonstrated in [58], [60].

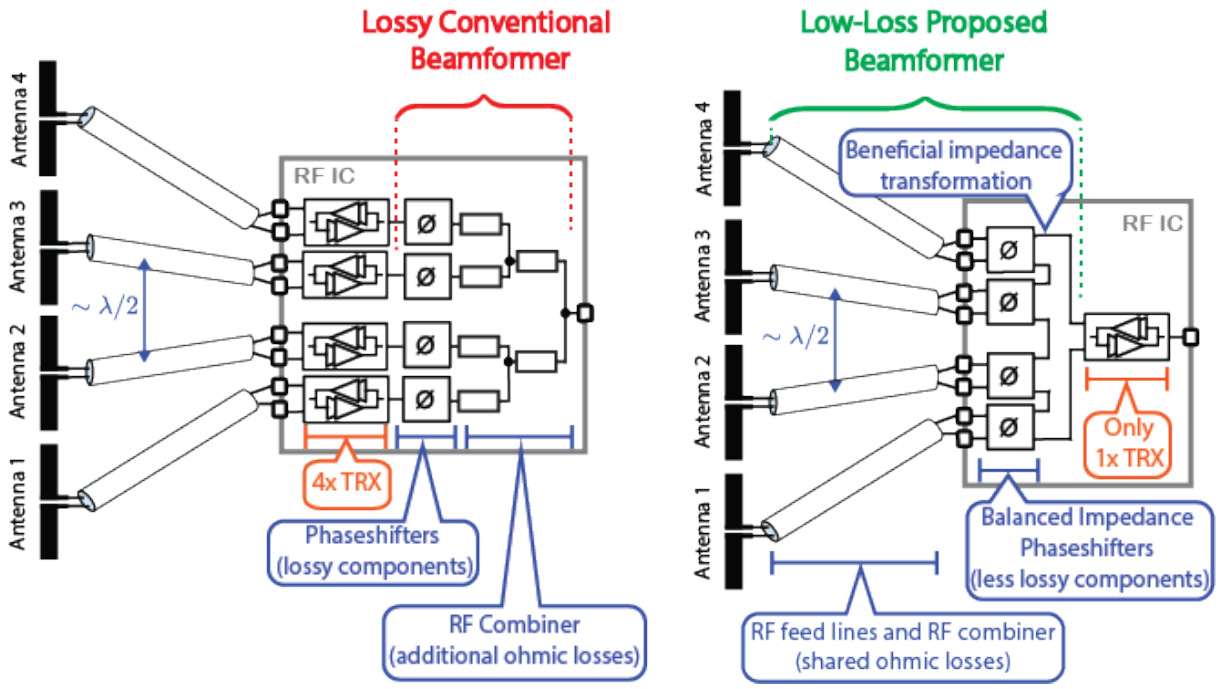


Figure 2.1: Comparison of conventional and proposed beamformer RFIC implementations

Infinite Common-Mode Impedances, $Z'_{CM} = \infty$

An N-element phased array configured as a receiver can be modelled with differential sources (Source 1, 2, ... N) representing the antennas, a load (R_L) for the receiver, and differentially coupled transmission lines for the feed-lines, as shown in Fig. 2.2a. Using the transmission-line equation, the circuit in Fig. 2.2a can be transformed into the circuit in Fig. 2.2b. Assuming that the transmission lines have a differential characteristic impedance ($Z_{o(DM)}$) that is equal to the antenna's differential source resistance (R_S), the antenna's differential source resistance is unchanged by this transformation. But the antenna's common-mode impedance (Z_{CM}) is transformed to an effective value (Z'_{CM}) via Eq. 2.1. Note Z'_{CM}'s dependence on the transmission lines characteristic common-mode impedance ($Z_{o(CM)}$) and electrical length (ℓ_{TL}/λ_{RF}).

$$Z'_{CM} = Z_{o(CM)} \frac{Z_{CM} + jZ_{o(CM)} \tan\left(2\pi \frac{\ell_{TL}}{\lambda_{RF}}\right)}{Z_{o(CM)} + jZ_{CM} \tan\left(2\pi \frac{\ell_{TL}}{\lambda_{RF}}\right)} \tag{2.1}$$

From the circuit in Fig. 2.2b, we can show in the case of broadside incident waves (in-phase sources), the series connected antennas in this array optimally transfer all their available power (P_{AVS}) to the load ($P_L = NP_{AVS}$), provided their effective common-mode impedance at the series summing nodes (Z'_{CM}) is infinite.

This can be shown by first noting the following key relationships.

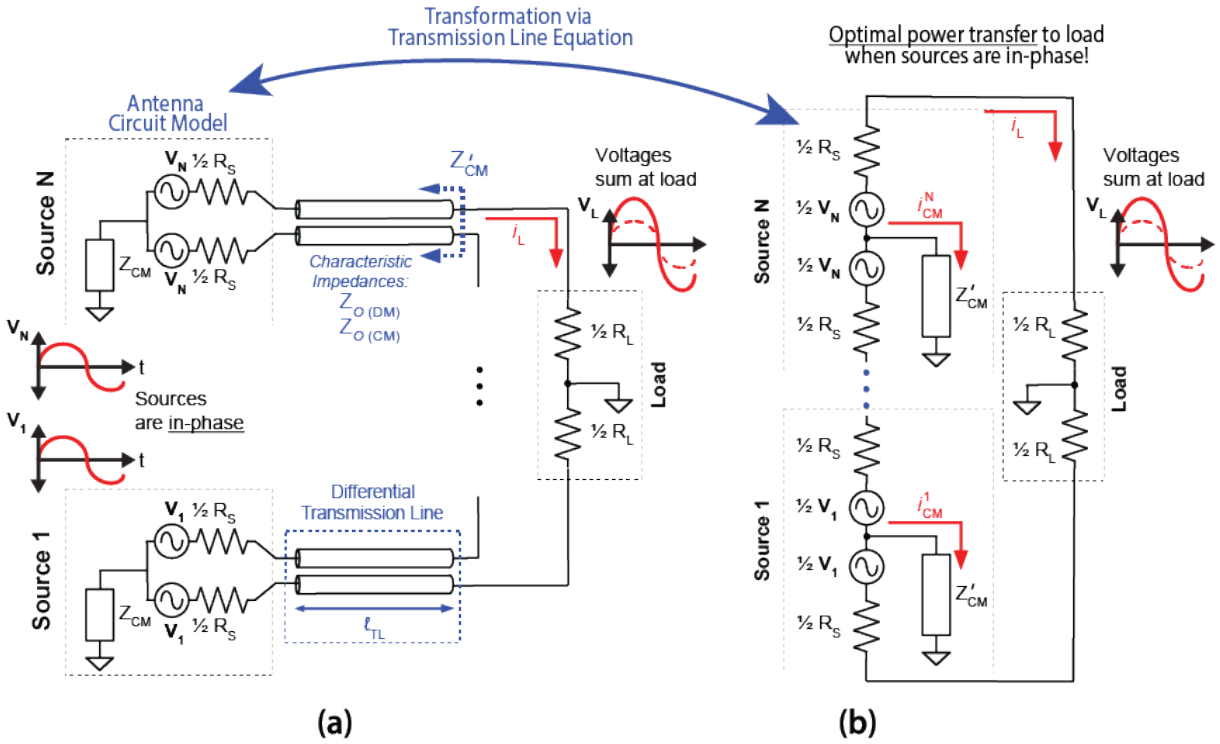


Figure 2.2: Series-connected phased array circuit with TLT for optimal power combining

$$R_L = NR_S \tag{2.2}$$

$$V_1 = V_2 = ... = V_N = V_S \tag{2.3}$$

$$P_{AVS} = \frac{V_S^2}{8R_S} \tag{2.4}$$

Then, solving for the power delivered to the load.

$$P_L = \frac{1}{2}(V_L)^2 \frac{1}{R_L} = \frac{1}{2}\left(NV_S \frac{NR_S}{2NR_S}\right)^2 \frac{1}{NR_S} = N\frac{V_S^2}{8R_S} = NP_{AVS} \tag{2.5}$$

Finite Common-Mode Impedances, $Z'_{CM} < \infty$

When Z'_{CM} is finite, some amount of current ends up flowing through the common-mode paths (i^1_{CM} through i^N_{CM}) and results in loss. The power dissipated by Z'_{CM} in this case is related to the common-mode voltages across each antenna in the series stack. Assuming that Z'_{CM} is optimally designed to be a large real resistance, we see that:

$$P^k_{CM} = \frac{1}{2} \cdot \frac{(v^k_{CM})^2}{|Z'_{CM}|} \tag{2.6}$$

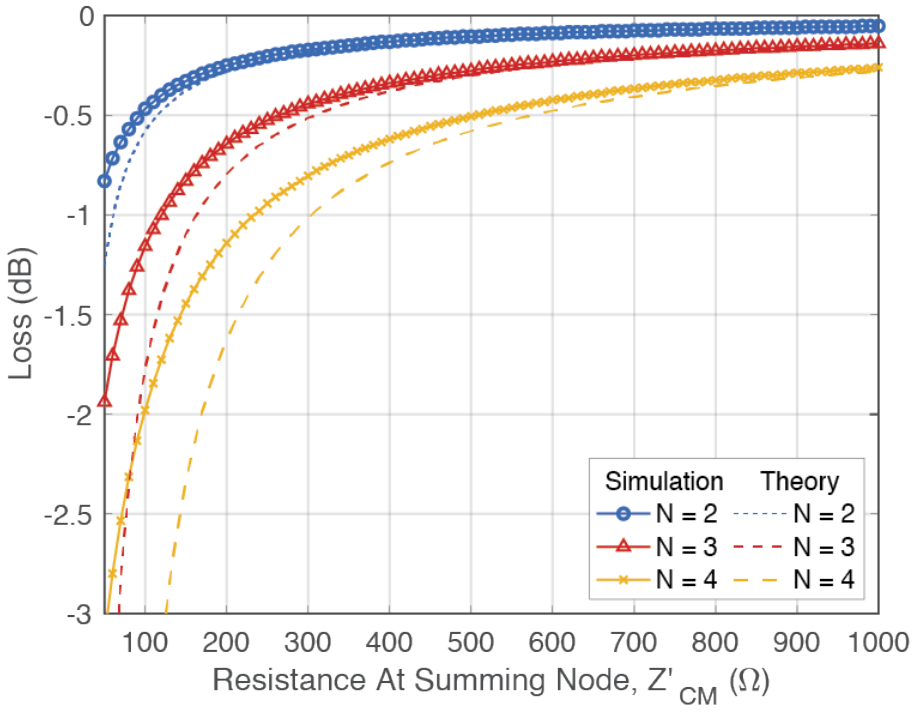


Figure 2.3: TLT combining loss as function of summing node common-mode resistance

$$P_{CM} = \sum_{k=1}^{N} \frac{1}{2} \cdot \frac{(v_{CM}^k)^2}{|Z'_{CM}|} \tag{2.7}$$

where P_{CM}^k is the power dissipated in the common-mode impedance of the k^{th} antenna, v_{CM}^k is the common-mode voltages across the k^{th} antenna, and P_{CM} is the total common-mode power dissipated in the array.

If Eq. 2.8 holds and the sum total of the common-mode currents (i_{CM}) are small relative to the load current (i_L), shown in Fig. 2.2b, then the common-mode voltages across Z'_{CM} will not deviate appreciably from the ideal case where Z'_{CM} is infinite.

$$i_{CM} = \sum_{k=1}^{N} i_{CM}^k \ll i_L \tag{2.8}$$

This allows us to define a function $f(k, N)$, independent of Z'_{CM}, that describes how v_{CM}^k scales with it's position, k, in the N element array and the available voltage from the source, v_{AVS}.

$$v_{CM}^k \approx f(k, N) \cdot v_{AVS} \tag{2.9}$$

Table 2.1: Scaling function for common-mode voltage across antenna's in N element array.

N	$f(k,N)$	α
2	$-1/2, 1/2$	0.25
3	$1, 0, 1$	0.67
4	$-3/2, -1/2, 1/2, 3/2$	1.25

Substituting Eq. 2.9 into Eq. 2.7 we get

$$P_{CM} \approx \frac{1}{2} \cdot \frac{(v_{AVS})^2}{|Z'_{CM}|} \sum_{k=1}^{N} f(k,N)^2 \tag{2.10}$$

Meanwhile, the total power delivered to the load, P_L:

$$P_L \approx \sum_{k=1}^{N} \frac{1}{2} \cdot \frac{(v_{AVS})^2}{|R_S|} = N\frac{1}{2} \cdot \frac{(v_{AVS})^2}{|R_S|} \tag{2.11}$$

Therefore, the fractional loss, L_{CM}, due to currents flowing through Z'_{CM} is the ratio of P_{CM} to P_L.

$$L_{CM} = \frac{P_{CM}}{P_L} \approx \frac{R_S}{|Z'_{CM}|} \cdot \frac{1}{N} \sum_{k=1}^{N} f(k,N)^2 \tag{2.12}$$

Defining a term Q_{TLT}, to represent the Q of the combination of transmission line and antenna, as $|Z'_{CM}|/R_S$; and α scaling factor, corresponding to the ratio of common-mode to differential-mode excitation in the network as $\frac{1}{N}\sum_{k=1}^{N} f(k,N)^2$; we find L_{CM} takes on a form shown in Eq. 2.13.

$$L_{CM} \approx \frac{1}{Q_{TLT}} \cdot \alpha \tag{2.13}$$

The values of $f(k,N)$ can be computed by inspection for different k and N then used to derive α, see Table. 2.1. This allows us to estimate L_{CM} for a 2, 3, and 4-element array utilizing TLT-based power combining, as shown in Eq. 2.14

$$\begin{aligned} L_{CM} &\approx 0.25 \times \frac{R_S}{|Z'_{CM}|}, \quad N = 2 \\ L_{CM} &\approx 0.67 \times \frac{R_S}{|Z'_{CM}|}, \quad N = 3 \\ L_{CM} &\approx 1.25 \times \frac{R_S}{|Z'_{CM}|}, \quad N = 4 \end{aligned} \tag{2.14}$$

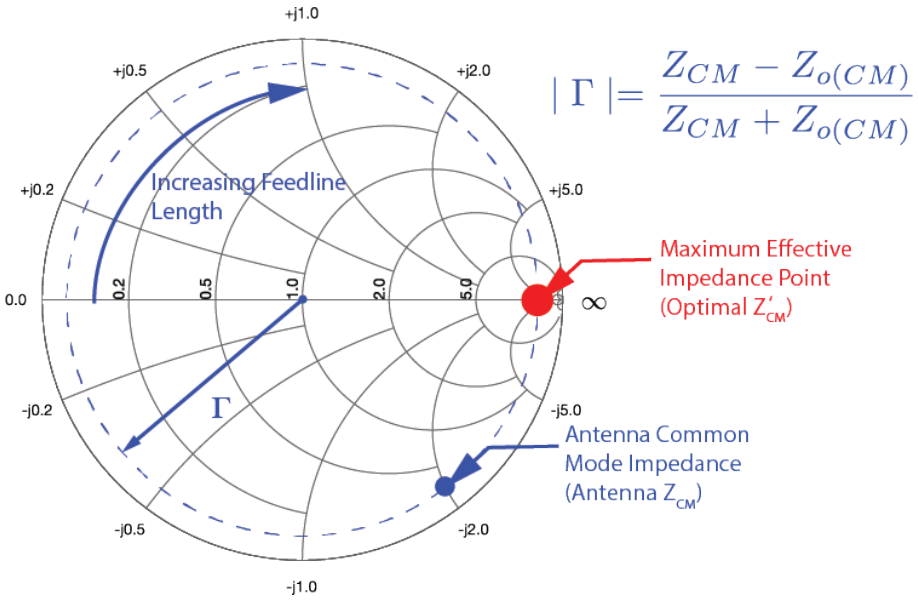


Figure 2.4: Smith Chart transformation from Z_{CM} to Z'_{CM} due to the transmission-line

These theoretical results are compared to simulation from Keysight's Advanced Design Systems (ADS) circuit simulator in Fig. 2.3. We see good agreement between the theoretical and simulated results, especially for low losses where our assumption that the currents flowing through the common-mode paths (i^1_{CM} through i^N_{CM}) are much less than the load current (i_L) hold.

Notice, α increases more than linearly with increasing N, driving up losses for larger arrays. This makes it important to maximize Z'_{CM} through the appropriate design of $Z_{o(CM)}$ and ℓ_{TL}. Maximizing Z'_{CM} becomes critical for larger arrays and the upper limit on N for TLT-based power combining is primarily set by this loss mechanism.

Maximizing Common-Mode Impedances, Z'_{CM}

From the trajectory of Z'_{CM} shown in Fig. 2.4, we can see that changes in ℓ_{TL} results in rotation around the Smith Chart, with the optimal ℓ_{TL} resulting in a large real value for Z'_{CM} and therefore low TLT losses. This behavior is periodic so there are multiple optimal values for ℓ_{TL}, separated by approximately $\lambda_{RF}/2$. For a lossy transmission line, optimal Z'_{CM} values become smaller every rotation around the Smith Chart, making shorter lines more ideal.

Using a 2D heat map in Fig. 2.5, we can visualize the impact of $Z_{o(CM)}$ as well as ℓ_{TL} on the realized Z'_{CM} and therefore TLT summation losses. Higher $Z_{o(CM)}$ values decrease the required ℓ_{TL} for optimal Z'_{CM}. They also increase the magnitude of the optimal Z'_{CM} and

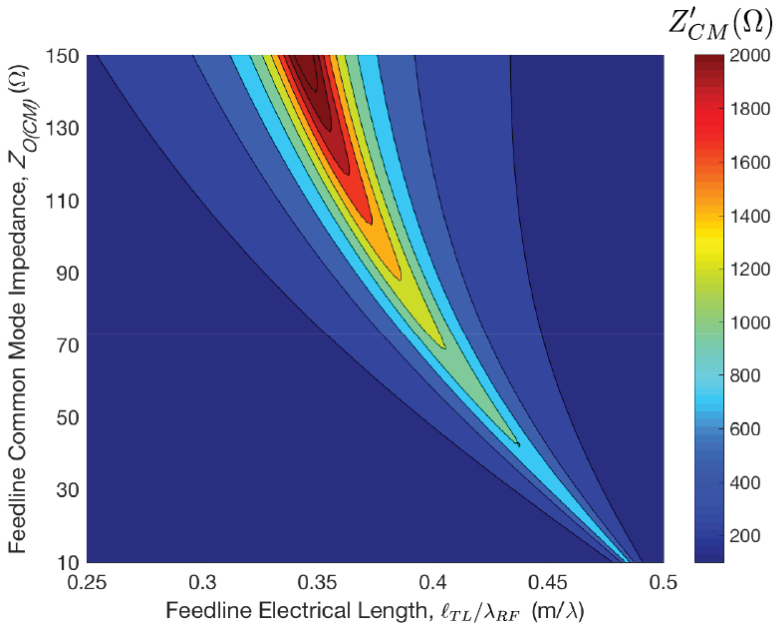


Figure 2.5: 2D Heat map of Z'_{CM} over ℓ_{TL} and $Z_{o(CM)}$ for $Z_{CM} = 12.5\Omega - j100\Omega$

the range of lengths (and therefore also frequencies) over which Z'_{CM} is large. This results in low TLT losses and a wider effective bandwidth (BW) for the array.

2.2 Comparing TLT-Based Combining to Conventional RF Combining Techniques

To compare the theoretical performance of a TLT-based combiner with other RF power combiners, we can examine the S-parameters and power delivered to the load over frequency for each circuit. The Wilkinson combiner and 3dB combiner (Wilkinson combiner without the added isolation resistor) are two of the most common RF power combiners in today's literature, so they were chosen for this comparison. All combiners were designed to operate optimally at an RF frequency (f_{RF}) of 2 GHz and were simulated in ADS.

S-parameters for the TLT-based combiner, 3dB combiner, and Wilkinson combiner are shown in Fig. 2.6, Fig. 2.7, and Fig. 2.8, respectively. The normalized power delivered to a load at port 1 with in-phase excitation on ports 2 and 3 for the TLT-based and 3dB combiners is shown in Fig. 2.9. The 3dB combiner and Wilkinson have identical performance in this regard so the Wilkinson data was not included in Fig. 2.9. A summary of this comparison for low-power beamforming is discussed in the following paragraphs, and shown in Table 2.2 at the end of this chapter.

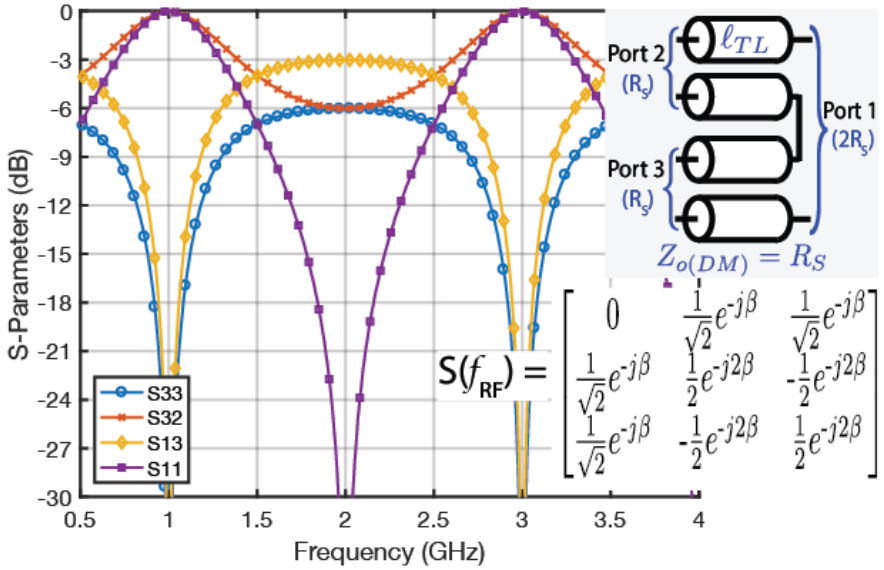


Figure 2.6: S-parameters across frequency for TLT-based combiner, with $\beta = 2\pi\ell_{TL}/\lambda_{RF}$

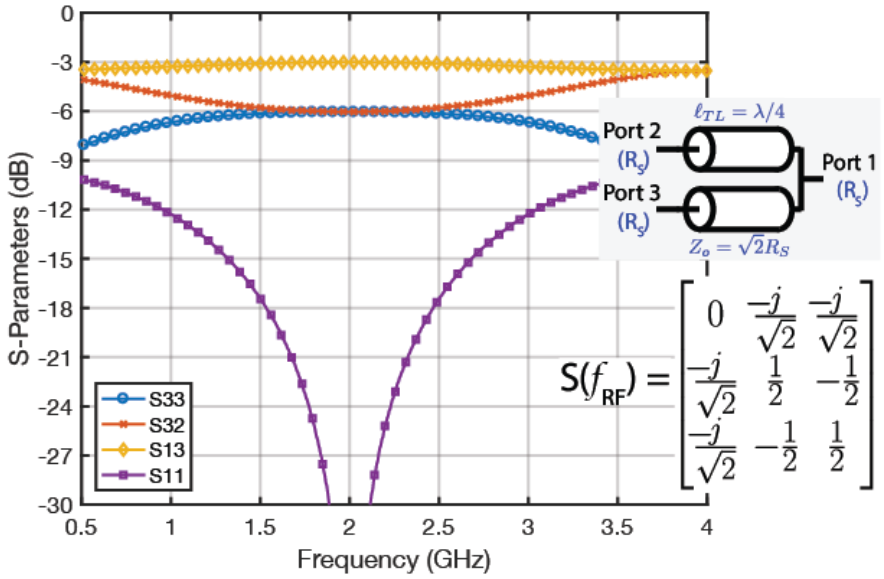


Figure 2.7: S-parameters across frequency for 3dB combiner

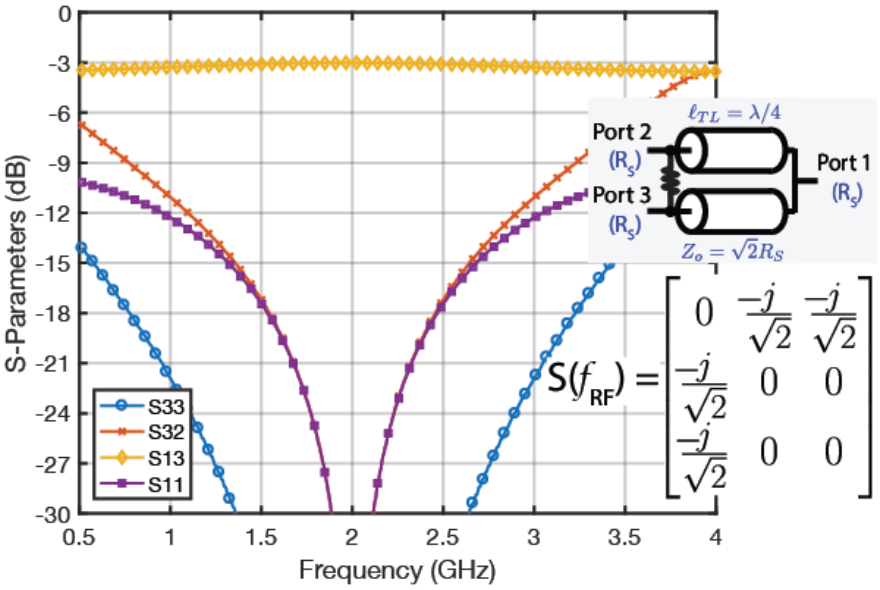


Figure 2.8: S-parameters across frequency for Wilkinson combiner

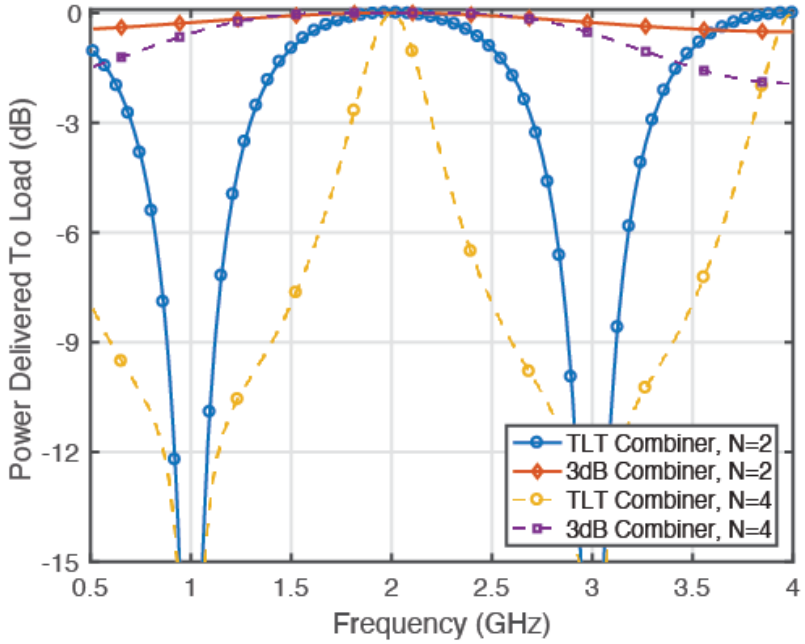


Figure 2.9: Power delivered to the load across frequency for TLT-based and 3dB combiner

Insertion Loss: The loss in a Wilkinson is primarily due to resistive and dielectric losses in the transmission lines, which scale with the number of levels of combining required. Normally, $\log_2(N)$ levels are required, so a 4-element array would have a 2 level Wilkinson combiner and double the loss of a 2-element array[1]. In contrast, it is straight forward to directly combine more than 2-elements using a TLT, which avoids cascading of combiner losses. Also, because the TLT architecture allows it to be used upstream of phase shifters, it can be integrated into the RF feed lines, sharing ohmic losses, as shown in Fig. 2.1. This avoids the need for additional large lossy on-chip RF traces. The TLT-based combiner does experience losses from common-mode currents, but these can be mitigated by careful design to maximize Z'_{CM} at the summing nodes and generally do not outweigh the reduction in ohmic losses for reasonable values of Q_{TLT}.

Output Impedance: The TLT-based combiner output port impedance is a series combination of the input port resistance (i.e. 100Ω for $N = 2$ and 200Ω for $N = 4$ with 50Ω input ports). While the output port impedance for the Wilkinson combiner and 3dB combiner is the same as the input port (i.e. 50Ω for $N = 2$ and $N = 4$ with 50Ω input ports)[2]. The larger output port impedance in the TLT-based combiner can be beneficial for certain low-power systems. In receivers with common-gate low noise amplifiers (LNAs), a larger port impedance means a smaller g_m to achieve power match and therefore less power consumption. Similarly, in mixer-first receivers, larger port impedance means smaller mixer switches and less LO power [63]. In low output power transmitters, a larger port impedance would make it easier to match the power amplifier (PA) to the optimal output load resistance, reducing the matching network Q and associated losses.

Fractional Bandwidth: The Wilkinson combiner and 3dB combiner are broad-band, while the TLT-based combiner is narrow-band. As mentioned earlier, bandwidth for the TLT-based combiner is a function of the transmission line $Z_{o(CM)}$ used to implement it. Higher $Z_{o(CM)}$ values result in larger bandwidths. Per Fig. 2.9, a TLT-based combiner implemented with $Z_{o(CM)} = 12.5\Omega$ transmission lines[3], has a fractional 3 dB bandwidth of roughly 70% when $N = 2$ and 20% when $N = 4$. Note, fractional bandwidths of 20% or more are usually not limiting in RF systems [64] so this may be an attractive trade-off for low-power applications, considering the other benefits.

Port Isolation: At f_{RF}, both the TLT-based combiner and 3dB combiner have identical S-parameters and provide the same amount of isolation between input ports. The magnitude of the S-parameters as a function of frequency are captured in Fig. 2.6, Fig. 2.7, and Fig. 2.8. At f_{RF}, the Wilkinson combiner is the only solution of the three that provides full isolation between ports 2 and 3. However, in the proposed architecture, isolation is less pressing. For

[1] N-way Wilkinson combiners are generally impractical to route on planar substrates since they require an isolation resistor connecting every port to every other port.

[2] The output impedance for the Wilkinson and 3dB combiner is determined by the impedance of the quarter wave transmission-lines used, so it is to some extent a design variable. However, by convention the transmission-line impedance is chosen so that the output port's impedance is 50Ω.

[3] A differential microstrip transmission line with 50Ω differential impedance will have a minimum common-mode impedance of 12.5Ω, so this is a conservative value on which to make comparisons.

receivers, since the RF combining happens before the LNA, signals that might leak from one port to the next due to imperfect isolation are very small. While for transmitters, there is only a single driver and the TLT is acting as a RF splitter, so power re-entering the antenna ports is limited to power reflected due to port mismatch and antenna-to-antenna interactions.

2.3 Phase Shifting with Balanced Impedance Tuning

Balanced Impedance Tuning Phase Shifters

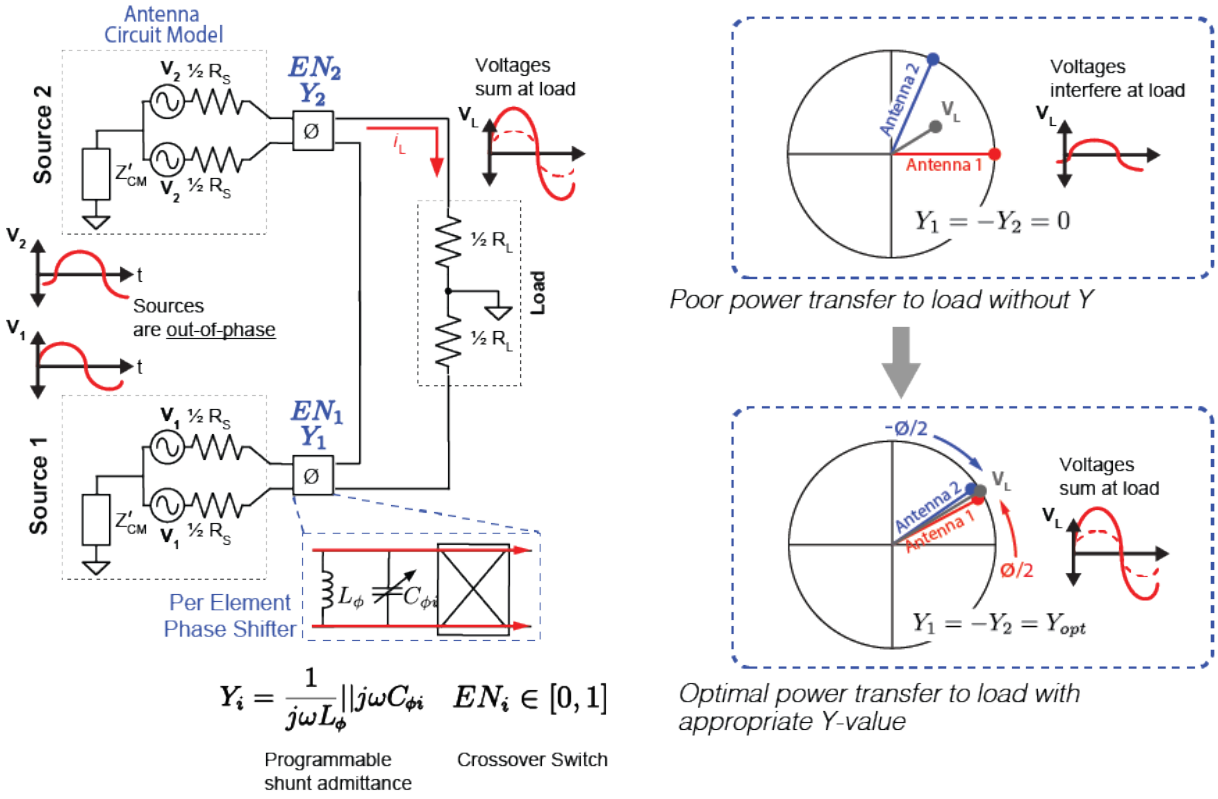
When using a TLT power combiner as described in Section 2.1, if the relative phase relationship between the antenna signals (ϕ) is non-zero, the power transfer is not optimal and is proportional to $\cos^2(\phi/2)$. In effect, the TLT combiner creates a directive array and a means to steer the beam is needed. Conventional phase shifters discussed in Section 1.2 can be used to address this issue by adding the appropriate phase shift to the differential signals before they are combined. However, these phase shifters are generally either passive and quite lossy [29], [30], [37] or power-intensive [6].

In contrast, by adding a reactance in shunt across each source, as shown in Fig. 2.10, and tuning the values in a balanced way (i.e. an increase in reactance across one source is matched by decreases in reactance across another source), we can achieve near optimum power transfer over a broad range of ϕ with minimal loss and no active devices. This allows us to realize a $\pm 90°$ phase shift with much fewer lossy components than a standard switch-type phase shifter.

This method of phase shifting, utilizing balanced impedance tuning (BIT), differs significantly from high/low pass and switched transmission line techniques for passive phase shifting [58]. By taking advantage of the symmetry inherent in a linear phased array, i.e. the desired phase shift on one antenna element is the negative of the desired phase shift on another, we are able to reduce the number of switchable or tunable passive components required from three or four per antenna to one, while still maintaining a good match to the load. This is because the reactance added in shunt across Source 1 is cancelled by the negative reactance added in shunt across Source 2. Reducing the number of switched or tuned elements is very important for minimizing phase shifter loss.

Extended-Range Balanced Impedance Tuning Phase Shifters

It was shown in [60] that the losses due to the balanced impedance tuning approach rise rapidly beyond a $|\phi|$ of 90°. To extend this range further, and to make these techniques practical for larger linear arrays, we can use a crossover switch. The crossover switch, which can be implemented using four MOSFET switches in a passive mixer configuration, creates a 0° phase shift when disabled and a 180° phase shift when enabled. By enabling the crossover across antenna 2, as shown in Fig. 2.11, the normalized power delivered to the load now has



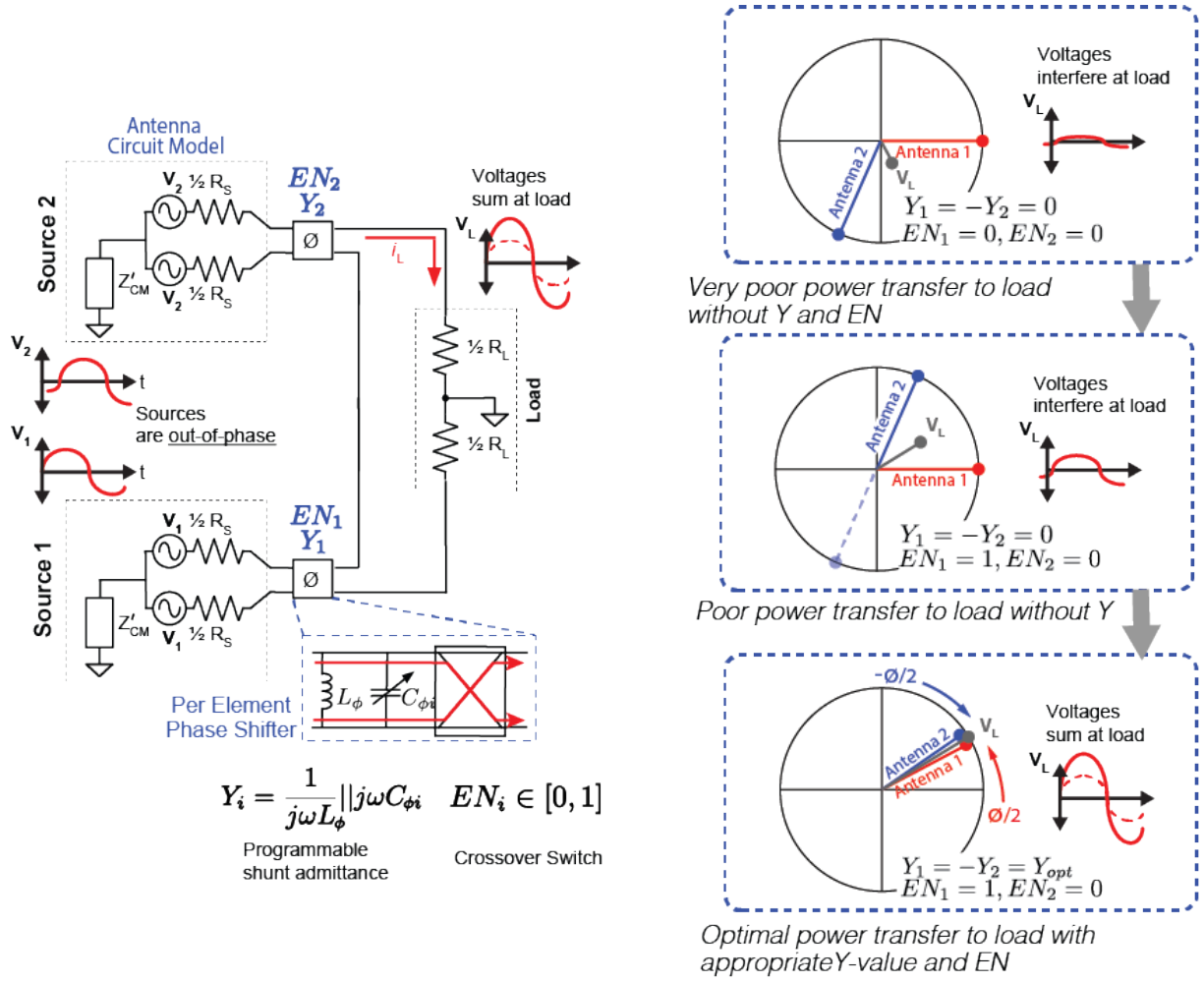
$$Y_i = \frac{1}{j\omega L_\phi} || j\omega C_{\phi i} \qquad EN_i \in [0,1]$$

Figure 2.10: Series-connected array with low-loss balanced-impedance-tuning phase shifter.

low loss for $|\phi| > 90°$ and high loss for $|\phi| < 90°$. We can switch back and forth between the two states in Fig. 2.10 and Fig. 2.11 to create a control strategy that provides sub-1 dB theoretical loss across all ϕ values, and therefore all possible beam angles, for a linear array. We will refer to such a circuit that incorporates balanced impedance tuning of shunt impedances and crossover switches across series connected antenna as a balanced impedance phase shifter (BIPS, for convenience).

The state of the BIPS across the i^{th} antenna element can be described by a binary enable variable which indicates if the crossover switch is enabled ($EN_i = 1$) or not ($EN_i = 0$), and an admittance variable (Y_i), which indicates the shunt programmable admittance. Therefore, the total beamformer state can be described by an enable vector ($\mathbf{EN} = [EN_1, EN_2, ..., EN_N]$) and admittance vector ($\mathbf{Y} = [Y_1, Y_2, ..., Y_N]$) with length equal to the number of antennas in the array, N. For convenience, we also define a change in the admittance variable relative to an initial reference state, usually zero, as ΔY_i.

The extended-range BIT algorithm has the following key features: First, the crossover switches are configured to reduce the maximum phase delay between all ports. Second, the change in admittance across the BIPS unit cell for port 1, ΔY_1, is set to be equal to the



$$Y_i = \frac{1}{j\omega L_\phi} || j\omega C_{\phi i} \quad EN_i \in [0,1]$$

Figure 2.11: Extended range balanced-impedance-tuning phase shifter.

negative of the change in admittance across the BIPS unit cell for port 4, $-\Delta Y_4$. Third, the change in admittance across the BIPS unit cell for port 2, ΔY_2, is set to be equal to the negative of the change in admittance across the BIPS unit cell for port 3, $-\Delta Y_3$. Again, these features emerge from the symmetry inherent in a 1-dimensional linear phased array. Forth, the value of ΔY_1 and ΔY_2 are swept to maximize the power delivered to the load for a given angle of arrival, θ. This last step may take into account practical considerations like finite quantization steps in the programmable Y values, relative phase delays in the ports due to differing feed lengths, and limits in the absolute range of Y. The algorithm also works for transmit, where power is flowing from a source to the beamformed ports with varying phase delays to maximize the power delivered for a given θ. The procedure is visualized in Fig. 2.12.

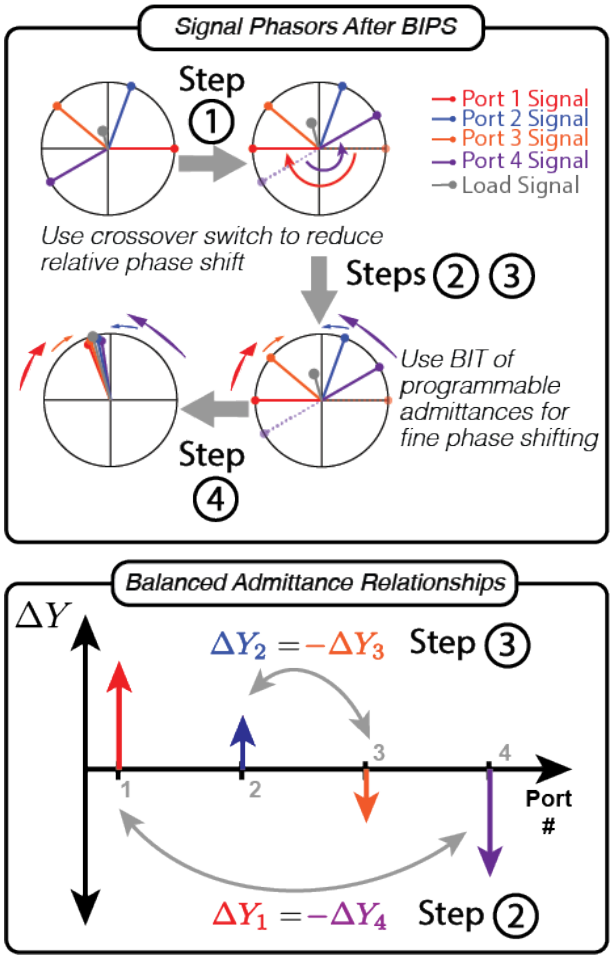


Figure 2.12: Vizualization of the BIT algorithm which levearges symmetry in linear 1-dimensional phased arrays to facilitate low-loss beamforming with BIPS.

Deriving P_L Under BIPS: 2-Element Array

For a 2-element array we can represent the circuit as shown in Fig. 2.13. To make the math more tractable, we replace the sources with their Norton equivalent and assume infinite Z'_{CM}. The exact equation for the power delivered to the load (P_L) as a function of the power available from each source (P_{AVS}), the phase difference (ϕ) and the reactance across each source (Z_ϕ, where $Z_\phi = 1/Y_\phi$) is derived below.

Defining $\boldsymbol{i_L^1}$ as the load current, $\boldsymbol{i_L}$, when only $\boldsymbol{i_S^1}$ is connected and $\boldsymbol{i_L^2}$ as $\boldsymbol{i_L}$ when only $\boldsymbol{i_S^2}$ is connected. We can express $\boldsymbol{i_L^1}$ and $\boldsymbol{i_L^2}$ as a function of the known elements in the circuit and define $\boldsymbol{i_L}$ as the sum of $\boldsymbol{i_L^1}$ and $\boldsymbol{i_L^2}$ via superposition. (Note, $R_L = 2R_S$. Also note, these simplifications assume a purely reactive Z_ϕ.)

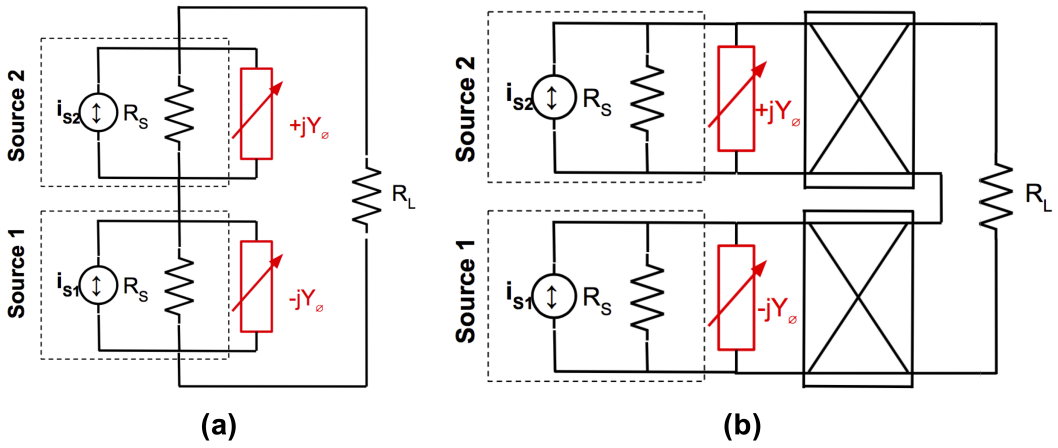


Figure 2.13: Norton equivalent for series-connected array (a) without and (b) with crossover

$$\boldsymbol{i_L^1} = \boldsymbol{i_S^1}\frac{R_S||-Z_\phi}{(R_S||-Z_\phi)+(R_S||+Z_\phi)+2R_S} \tag{2.15}$$

$$\boldsymbol{i_L^2} = \boldsymbol{i_S^2}\frac{R_S||+Z_\phi}{(R_S||+Z_\phi)+(R_S||-Z_\phi)+2R_S} \tag{2.16}$$

$$\frac{R_S||\pm Z_\phi}{(R_S||+Z_\phi)+(R_S||-Z_\phi)+2R_S} = \frac{|Z_\phi|^2 \pm jR_S|Z_\phi|}{4|Z_\phi|^2+2R_S^2} \tag{2.17}$$

We can also express $\boldsymbol{i_{S1}}$ and $\boldsymbol{i_{S2}}$ in complex form as a function of P_{AVS}, R_S and ϕ.

$$\boldsymbol{i_S^1} = 2\sqrt{\frac{2P_{AVS}}{R_s}}\left[\cos(\frac{\phi}{2})+j\sin(\frac{\phi}{2})\right] \tag{2.18}$$

$$\boldsymbol{i_S^2} = 2\sqrt{\frac{2P_{AVS}}{R_s}}\left[\cos(\frac{\phi}{2})-j\sin(\frac{\phi}{2})\right] \tag{2.19}$$

Putting these together we find an expression for i_L and therefore P_L for the $EN = [0,0]$ state, $P_L[0,0]$, Eq. 2.23. Note, that enabling the crossover switch across either antenna 1 or 2, effectively shifts ϕ by 180° and moves the system from the $EN = [0,0]$ state to the $EN = [0,1]$ state.[4] Therefore, the power delivered to the load in the $EN = [0,1]$ state,

[4]The binary state vector that describes the state of the array's crossover switches is unaffected by mirror transformations or inversion. For example, the state [0,0,1] is equivalent to the state [1,0,0], mirror transformation, and the state [1,0,1] is equivalent to the state [0,1,0], inversion. This drastically reduces the number of unique states to consider. For $N = 2$ there are only two unique states. For $N = 3$ there are only 3 unique states. For $N = 4$ there are only six unique states.

$P_L[0,1]$, can be evaluated as a function of ϕ and Y_ϕ by replacing ϕ with $\phi + 180°$, as shown in Eq. 2.24.

$$i_L = 4\sqrt{\frac{2P_{AVS}}{R_s}}\left[\frac{|Z_\phi|^2\cos(\frac{\phi}{2}) + |Z_\phi|R_S\sin(\frac{\phi}{2})}{4|Z_\phi|^2 + 2R_S^2}\right] \tag{2.20}$$

$$P_L = \frac{1}{2}|i_L|^2 R_L, R_L = 2R_S \tag{2.21}$$

$$P_L = 2P_{AVS}\left[\frac{|Z_\phi|^2\cos(\frac{\phi}{2}) + |Z_\phi|R_S\sin(\frac{\phi}{2})}{|Z_\phi|^2 + \frac{1}{2}R_S^2}\right]^2 \tag{2.22}$$

$$P_L[0,0] = 2P_{AVS}\left[\frac{\cos(\frac{\phi}{2}) + |\frac{Y_\phi}{Y_S}|\sin(\frac{\phi}{2})}{1 + \frac{1}{2}|\frac{Y_\phi}{Y_S}|^2}\right]^2 \tag{2.23}$$

$$P_L[0,1] = 2P_{AVS}\left[\frac{\cos(\frac{\phi+\pi}{2}) + |\frac{Y_\phi}{Y_S}|\sin(\frac{\phi+\pi}{2})}{1 + \frac{1}{2}|\frac{Y_\phi}{Y_S}|^2}\right]^2 \tag{2.24}$$

Using Eq. 2.23 and Eq. 2.24, P_L can be plotted for different shunt admittance values (Y_ϕ) and EN states in a 2-element array, as shown in Fig. 2.14. In this arrangement, we can switch back and forth between the two EN states, $EN = [0,0]$ and $EN = [0,1]$ to create a control strategy that provides sub $0.3dB$ loss across all ϕ values and, therefore, all possible beam angles.

Deriving P_L Under BIPS: 3-Element Array

For a 3-element array the math is very similar to the 2-element array, except that we now need to define a ϕ value for the signal from each antenna element since the relative phase shifts are no longer necessarily all equal. We will let ϕ^1, ϕ^2, and ϕ^3 represent the phase shift from some arbitrary reference to antenna signals 1, 2, and 3, respectively. We also need to define Z_ϕ^1, Z_ϕ^2, Z_ϕ^3 to represent the shunt impedances across antenna 1, 2, and 3, respectively. Following the same procedure as before, we can express $\boldsymbol{i_L}$, and therefore P_L, as a function of the known elements in the circuit. (Note, $R_L = 3R_S$.)

$$\boldsymbol{i_L} = \boldsymbol{i_L^1} + \boldsymbol{i_L^2} + \boldsymbol{i_L^3} \tag{2.25}$$

$$\boldsymbol{i_L^1} = \boldsymbol{i_S^1}\frac{(R_S||Z_\phi^1)}{(R_S||Z_\phi^1)+(R_S||Z_\phi^2)+(R_S||Z_\phi^3)+3R_S} \tag{2.26}$$

$$\boldsymbol{i_L^2} = \boldsymbol{i_S^2}\frac{(R_S||Z_\phi^2)}{(R_S||Z_\phi^1)+(R_S||Z_\phi^2)+(R_S||Z_\phi^3)+3R_S} \tag{2.27}$$

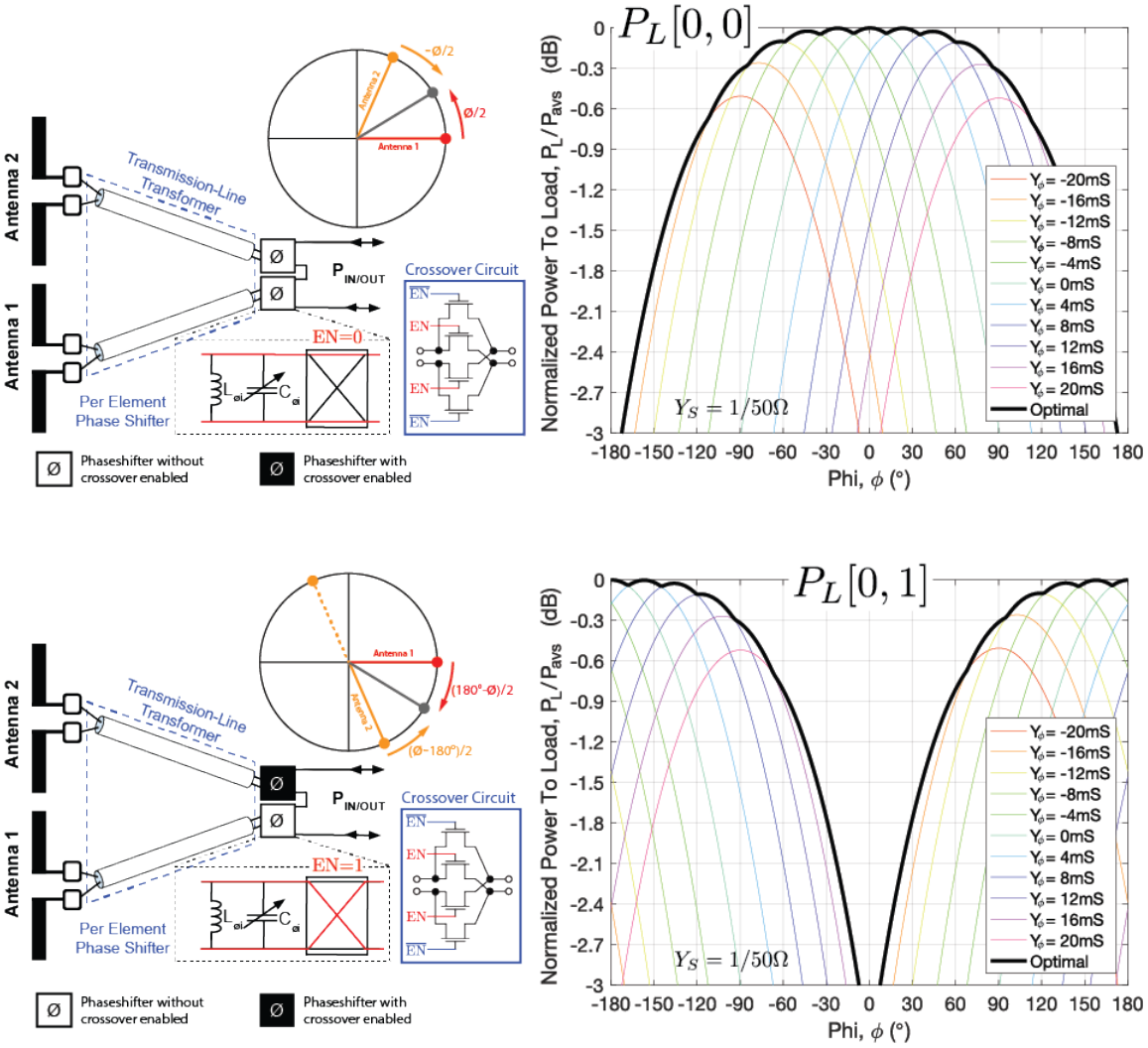


Figure 2.14: Normalized P_L delivered from 2-element array with different Y_ϕ and EN

$$\boldsymbol{i_L^3} = \boldsymbol{i_S^3}\frac{(R_S||Z_\phi^3)}{(R_S||Z_\phi^1)+(R_S||Z_\phi^2)+(R_S||Z_\phi^3)+3R_S} \tag{2.28}$$

We can express source current from the k^{th} source, $\boldsymbol{i_S^k}$, in complex form as a function of P_{AVS}, R_S and relative phase delay of that source, ϕ^k. See Eq. 2.29. Note, that enabling the crossover switch across the k^{th} antenna, effectively shifts ϕ^k by 180°, to $\phi^k + 180°$. Moving us from one configuration to another, e.g. state [0, 0, 0] to the state [0, 0, 1].

$$\boldsymbol{i_S^k} = 2\sqrt{\frac{2P_{AVS}}{R_s}}\left[\cos(\phi_k) + j\sin(\phi_k)\right] \tag{2.29}$$

Putting these together we find an expression for i_L and therefore P_L, as shown in Eq. 2.30. This is the most general solution and can be used to find P_L in all possible configurations.

$$P_L = \frac{1}{2}|i_L|^2 R_L, R_L = 3R_S \tag{2.30}$$

However, in the state [0, 0, 0] and [1, 0, 1] configurations illustrated in the 3-element circuit from Fig. 2.15, the phase shifts are balanced. That is $(\phi^1 + \phi^3)/2 = \phi^2$, regardless of the selected reference phase. Under these conditions, the optimal P_L occurs when $Z_\phi^1 = -Z_\phi^3 = Z_\phi$ and $Z_\phi^2 = \infty$. Choosing the reference phase such that $\phi^2 = 0$ is convenient here because it allows us to further reduce the number of variables as $\phi^1 = -\phi^3 = \phi$. With these simplifications, it follows that the load current is:

$$\boldsymbol{i_L} = \boldsymbol{i_L^1} + \boldsymbol{i_L^2} + \boldsymbol{i_L^3} \tag{2.31}$$

$$\boldsymbol{i_L^1} = \boldsymbol{i_S^1}\frac{R_S||-Z_\phi}{(R_S||-Z_\phi) + (R_S||+Z_\phi) + 4R_S} \tag{2.32}$$

$$\boldsymbol{i_L^2} = \boldsymbol{i_S^2}\frac{R_S}{(R_S||-Z_\phi) + (R_S||+Z_\phi) + 4R_S} \tag{2.33}$$

$$\boldsymbol{i_L^3} = \boldsymbol{i_S^3}\frac{R_S||+Z_\phi}{(R_S||-Z_\phi) + (R_S||+Z_\phi) + 4R_S} \tag{2.34}$$

Where

$$\frac{R_S||\pm Z_\phi}{(R_S||+Z_\phi)+(R_S||-Z_\phi)+4R_S} = \frac{|Z_\phi|^2 \pm jR_S|Z_\phi|}{6|Z_\phi|^2 + 4R_S^2} \tag{2.35}$$

$$\frac{R_S}{(R_S||+Z_\phi) + (R_S||-Z_\phi) + 4R_S} = \frac{|Z_\phi|^2 + R_S^2}{6|Z_\phi|^2 + 4R_S^2} \tag{2.36}$$

Therefore

$$\boldsymbol{i_L^1} = 2\sqrt{\frac{2P_{AVS}}{R_s}}\left[\cos(\phi) + j\sin(\phi)\right]\frac{|Z_\phi|^2 - jR_S|Z_\phi|}{6|Z_\phi|^2 + 4R_S^2} \tag{2.37}$$

$$\boldsymbol{i_L^2} = 2\sqrt{\frac{2P_{AVS}}{R_s}}\frac{|Z_\phi|^2 + R_S^2}{6|Z_\phi|^2 + 4R_S^2} \tag{2.38}$$

$$\boldsymbol{i_L^3} = 2\sqrt{\frac{2P_{AVS}}{R_s}}\left[\cos(\phi) - j\sin(\phi)\right]\frac{|Z_\phi|^2 + jR_S|Z_\phi|}{6|Z_\phi|^2 + 4R_S^2} \tag{2.39}$$

Based on these equations we find an expression for the P_L in the state [0, 0, 0], Eq. 2.41. Note, similar to the 2-element array, the P_L in the state [1, 0, 1] configuration can be found by substituting ϕ with $\phi \pm 180°$ in Eq. 2.42.

$$P_L = \frac{1}{2}|i_L|^2 R_L, R_L = 3R_S \tag{2.40}$$

$$P_L[0,0,0] = 3P_{AVS} \times \left[\frac{1+|\frac{Y_\phi}{Y_S}|^2+2(\cos(\phi)+|\frac{Y_\phi}{Y_S}|\sin(\phi))}{3+2|\frac{Y_\phi}{Y_S}|^2}\right]^2 \tag{2.41}$$

$$P_L[1,0,1] = 3P_{AVS} \times \left[\frac{1+|\frac{Y_\phi}{Y_S}|^2+2(\cos(\phi+\pi)+|\frac{Y_\phi}{Y_S}|\sin(\phi+\pi))}{3+2|\frac{Y_\phi}{Y_S}|^2}\right]^2 \tag{2.42}$$

The final state to consider in the 3 element array is the state [0, 0, 1] configuration. This configuration is not balanced so we cannot easily reduce the number of variables and must rely on the more general solution in Eq. 2.40.

Deriving P_L Under BIPS: N-Element Array

In the most general case, we consider an N-element array, where $N > 1$. We will let ϕ^k represent the phase shift from some arbitrary reference to the signal from the k^{th} antenna. We also define Z_ϕ^k to represent the shunt impedances across the k^{th} antenna. Following the same procedure as before, we can express $\boldsymbol{i_L}$, and therefore P_L, as a function of the known elements in the circuit. Defining $\boldsymbol{i_L^k}$ as the load current, $\boldsymbol{i_L}$, when only $\boldsymbol{i_S^k}$ is connected, we can compute $\boldsymbol{i_L}$ by summing all $\boldsymbol{i_L^k}$ via superposition.

$$\boldsymbol{i_L} = \sum_{k=1}^{N} \boldsymbol{i_L^k} \tag{2.43}$$

$$\boldsymbol{i_L^k} = \boldsymbol{i_S^k}\frac{(R_S||Z_\phi^k)}{\sum_{k=1}^{N}(R_S||Z_\phi^k)+NR_S} \tag{2.44}$$

$$\boldsymbol{i_S^k} = 2\sqrt{\frac{2P_{AVS}}{R_s}}\left[\cos(\phi^k) + j\sin(\phi^k)\right] \tag{2.45}$$

Here, $\boldsymbol{i_S^k}$ is the complex source current from the k^{th} source as a function of P_{AVS}, R_S and the relative phase delay of that source, ϕ^k. Again, enabling the k^{th} crossover switch, effectively shifts ϕ^k by 180°, to $\phi^k + 180°$. Moving us from one configuration to another, e.g. state [0, 0, 0] to the state [0, 0, 1].

Putting these together we find an expression for $\boldsymbol{i_L}$ and therefore P_L, as shown in Eq. 2.46. This is the most general solution and can be used to find P_L in all possible configurations for an N-element array, where $N > 1$.

$$P_L = \frac{1}{2}|\boldsymbol{i_L}|^2 R_L, R_L = NR_S \tag{2.46}$$

With the equations for 2 (Eq. 2.23 and 2.24), 3 (Eq. 2.40, 2.41 and 2.42) and 4-element arrays (Eq. 2.46), we can plot the normalized power delivered to the load across ϕ assuming ideal selection of **Y** and **EN**. See Fig. 2.15. From these plots we see the minimum theoretical loss for 2, 3 and 4-element arrays using BIPS, is 0.3 dB 0.48 dB and 0.52 dB, respectively.

Furthermore, we can visualize the predicted array factor for a 4-element array using an RF beamformer with ideal BIPS. The beamformer array factor is the power delivered to the load, normalized by the power received from a single antenna, so for the 4-element array the ideal array factor is 6 dB. Fig. 2.16 plots this array factor versus angle of arrival, θ, for the key **EN** states and select **Y** values. Each of the faint dashed lines represent the resulting array gain for a specific **Y** value and **EN** state, i.e a beam pattern. While the bold solid curves are the optimal array factor achievable over all **Y** values in the select **EN** state. The global optimum in Fig. 2.16 shows a only a 0.52 dB drop in array factor over all θ.

Effect Of Finite Component Q on BIPS Performance

Deriving a meaningful mathematical expression for the phaseshifter component loss, L_{BIPS}, over all possible beam angles is not very practical. Given the number of variables, such calculations may be better suited for numerical solvers. However, it is relatively straight forward to derive the phaseshifter component loss for $\phi = 0$ or boresight excitation. The component loss at other angles, $\phi \neq 0$, will likely increase slightly relative to the $\phi = 0$ value. But the component loss estimates at $\phi = 0$ still form a good baseline for design.

When $\phi = 0$ the programmable admittance for each antenna element is set to zero, $Y_\phi^k = 0$ for all k. Under these conditions, the circuit in Fig. 2.17a reduces to Fig. 2.17b as the inductances and programmable capacitors (used to implement the per element phaseshifter) resonate with one another leaving only their lossy shunt resistances.

The value of this lossy shunt resistance, R_{BIPS}, is equal to $(Q_{cap}|Z_C|)||(Q_{ind}|Z_L|)$ where Z_C and Z_L are the capacitance and inductance impedances, respectively. Since, for $Y_\phi^k = 0$ $|Z_C| = |Z_L|$, then $R_{BIPS} = (Q_{cap}||Q_{ind})|Z_L|$. Noting that the range of Y_ϕ^k necessary for full range of beam angles is approximately $\pm 1/R_S$, we can state that $|Z_L| \approx R_S$. Substituting R_S in for Z_L, we have that $R_{BIPS} \approx (Q_{cap}||Q_{ind})R_S$. For convenience, we will use Q to refer to $Q_{cap}||Q_{ind}$, going forward.

$$R_{BIPS} \approx QR_S \tag{2.47}$$

Having motivated the circuit representation in Fig. 2.17b, we can derive the power delivered to the load, P_L, and compare it to the power dissipated in the in the phaseshifter, P_{BIPS}, to define the system's fractional loss due to the phaseshifter components, L_{BIPS}.

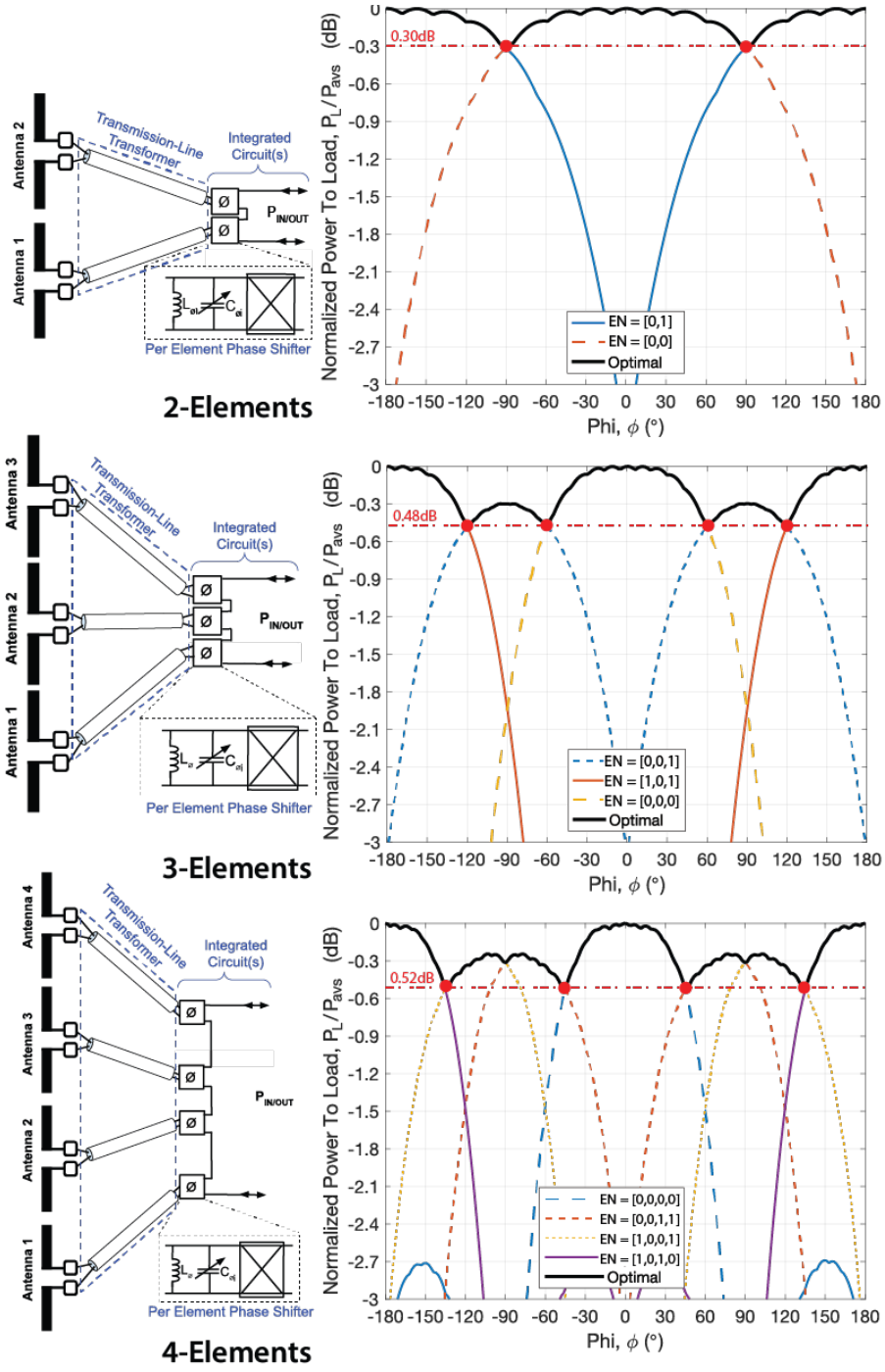


Figure 2.15: Normalized P_L delivered from 2, 3, and 4-element array with optimal BIPS

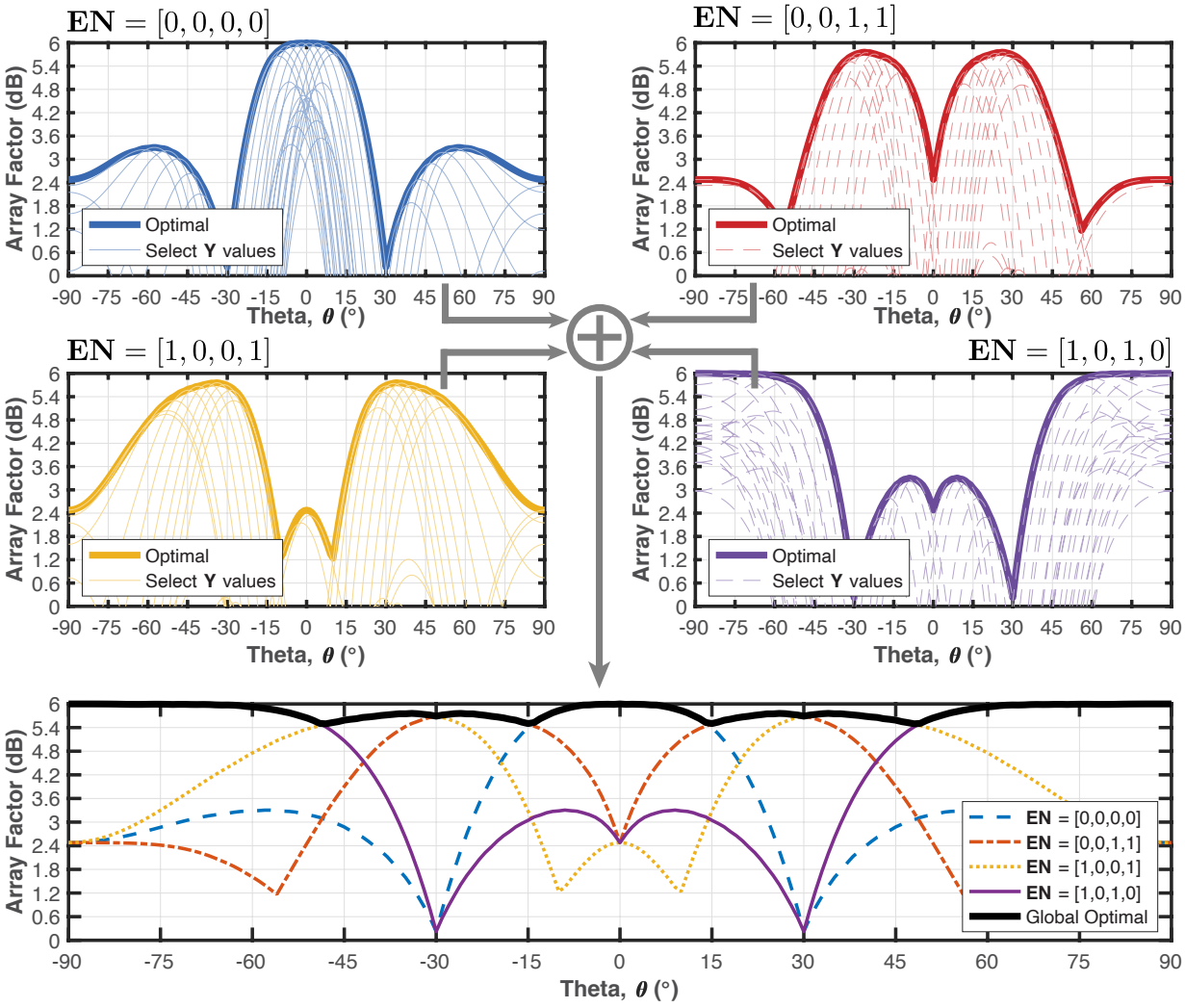


Figure 2.16: Simulated array factor for proposed 4-element beamformer with optimal BIPS.

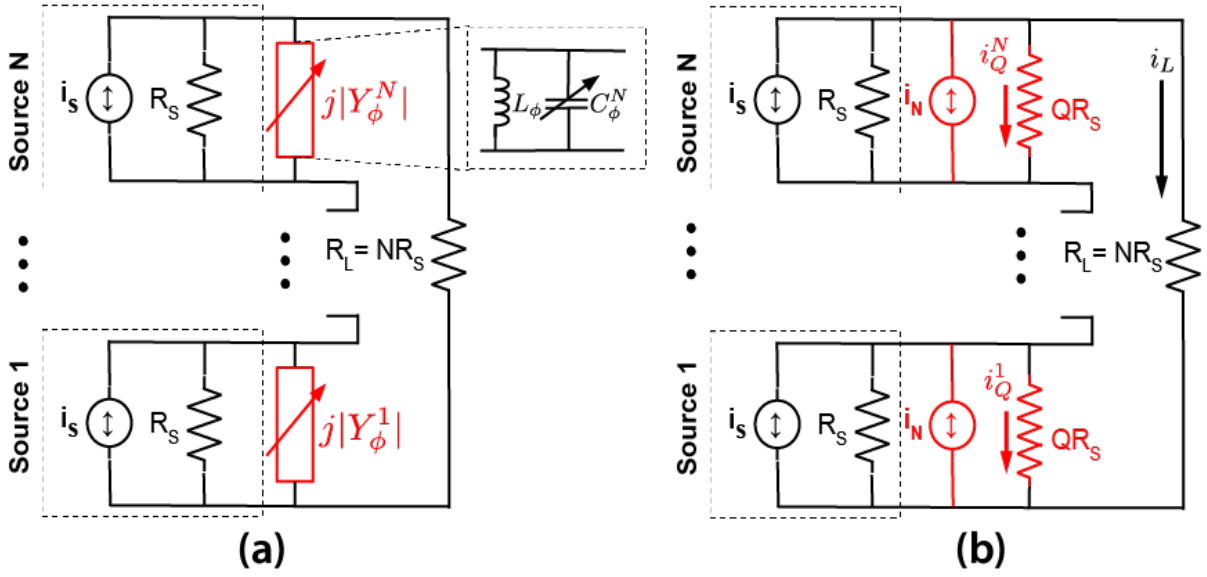


Figure 2.17: Norton model for series-connected array showing lossy resistive elements

$$L_{BIPS} = \frac{P_{BIPS}}{P_L} = \frac{\sum_{k=1}^{N} P_{BIPS}^k}{P_L} = \frac{\sum_{k=1}^{N} \frac{1}{2}(i_Q^k)^2 QR_S}{\frac{1}{2} i_L^2 NR_S} \tag{2.48}$$

$$L_{BIPS} = \frac{QR_S}{NR_S} \frac{\sum_{k=1}^{N}(i_Q^k)^2}{i_L^2} = \frac{Q}{N} \frac{N(i_Q^k)^2}{(\sum_{k=1}^{N} i_L^k)^2} = \frac{Q}{1} \frac{(i_Q^k)^2}{(N i_L^k)^2} \tag{2.49}$$

$$L_{BIPS} = \frac{Q}{N^2} \left(\frac{i_Q^k}{i_L^k} \right)^2 \tag{2.50}$$

Where i_Q^k is the current flowing through the lossy phaseshifter components connected in shunt across the k^{th} source and P_{BIPS}^k is the power this current dissipates. While i_L is the total current flowing through the load and i_L^k is the current flowing through the load when only k^{th} source is connected.

We can then express i_L^k and i_Q^k as a function of circuit components using $Z_{TOT} = R_S||QR_S||(R_L + (N-1)(R_S||QR_S))$ to simplify the expressions.

$$i_L^k = i_S^k \frac{Z_{TOT}}{R_L + (N-1)(R_S||QR_S)} \tag{2.51}$$

$$i_L^k = i_S^k Z_{TOT} \frac{Q+1}{(2N-1)Q + N} \tag{2.52}$$

$$i_Q^k = i_S^k \frac{Z_{TOT}}{QR_S} - i_L^k (N-1) \frac{R_S}{R_S + QR_S} \tag{2.53}$$

Putting these together we find an expression for i_Q^k / i_L^k and L_{BIPS}, as shown in Eq. 2.54 and Eq. 2.55, respectively.

$$\frac{i_Q^k}{i_L^k} = \frac{i_S^k}{i_L^k} \frac{Z_{TOT}}{QR_S} - (N-1) \frac{R_S}{R_S + QR_S} = \frac{N}{Q} \tag{2.54}$$

$$L_{BIPS} = \frac{Q}{N^2} \left(\frac{i_Q^k}{i_L^k} \right)^2 = \frac{1}{Q} \tag{2.55}$$

We convert L_{BIPS} into an insertion loss in Eq. 2.56. Note, the losses due to component Q in the phase shifter described by L_{BIPS} here are in addition to conduction losses in the transistors that implement the crossover switches.

$$IL_{BIPS} = \frac{1}{1 + L_{BIPS}} = \frac{1}{1 + 1/Q} \tag{2.56}$$

Then finally, since this network is passive, the array noise factor, F_{BIPS}, is the inverse of the insertion loss, IL_{BIPS}, under matched conditions.

$$F_{BIPS} = 1 + \frac{|i_N(QR_S)|^2}{|i_N(R_S)|^2} = 1 + \frac{1}{Q} \tag{2.57}$$

In practical circuit realizations, $|Z_L|$ may vary significantly from R_S. We can relax the assumption that $|Z_L| \approx R_S$ to account for these situations and instead substitute $(|Z_L|/R_S)R_S$ in for $|Z_L|$. We now find that $R_{BIPS} \approx QR_S(|Z_L|/R_S)$. As a result, L_{BIPS}, IL_{BIPS} and F_{BIPS} are:

$$L_{BIPS} = \frac{1}{Q} \frac{R_S}{|Z_L|} \tag{2.58}$$

$$IL_{BIPS} = \frac{1}{1 + L_{BIPS}} = \frac{1}{1 + (1/Q)(R_S/|Z_L|)} \tag{2.59}$$

$$F_{BIPS} = 1 + \frac{1}{Q} \frac{R_S}{|Z_L|} \tag{2.60}$$

2.4 Comparing BIPS to Conventional RF Phase Shifting Techniques

There are many types of passive RF phase shifters (e.g. reflective type [39], switched high-pass low-pass [29], and distributed [37]) and many metrics on which to judge their performance. This makes general comparison difficult [36]. However, one of the most important

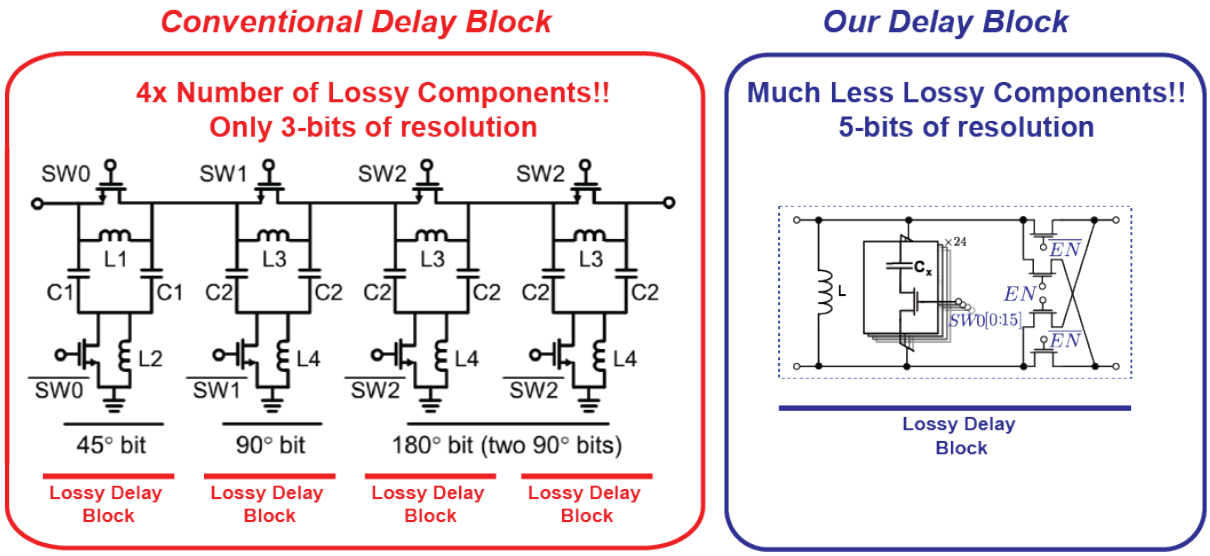


Figure 2.18: Comparison of loss sources in switched type phase shifter versus BIPS

metrics is the phase shifter loss, especially when the phase shifter is being used before any RF amplification stages because it directly impacts receiver noise figure and transmitter efficiency. These losses are primarily due to finite component Q, transmission line losses and series transistor on-resistance [37], [41].

The BIPS has an unique structural advantage because the number of series transistors and the number of passive components is not directly tied to the range or resolution of the phase shift. In the conduction path, a BIPS implemented as described here, has a pair of series transistors in the crossover switch along with one fixed inductor and programmable capacitor per antenna element. While a switched low-pass (LP) high-pass (HP) phase shifter [41], for example, requires a series transistor along with multiple fixed passives per bit of resolution per antenna element. This means for a 3 or 4-bits of phase shift, a switched LP HP phase shifter would incur two times the series transistor losses and require four or more times as many inductors when compared to BIPS, as shown in Fig. 2.18. Detailed analysis of the losses due to finite component Q in BIPS is shown in Section 2.3.

Because BIPS combine the RF signals directly, they cannot be easily used with per element amplitude control schemes, like those used in complex beamformers which use amplitude and phase control. This can be addressed by using conventional beamforming techniques at the sub-array level and the proposed technique at the individual-element level. In such a system, amplitude control would be possible at the sub-array level. This could provide reasonable beam shaping, while allowing for the performance benefits we have proposed.

A summary of the comparison between a passive switched-type phase shifter and BIPS for low-power beamforming is shown in Table. 2.3.

Table 2.2: Comparison of TLT-based and Wilkinson combiner for low-power beamforming

	Wilkinson Combiner	**TLT**
Insertion Loss	Low loss, approximately 1 to 2 dB/level. So for N=4, total loss would range from 2 to 4 dB	Can be very low loss depending on achieved Z'_{CM}. For $Z'_{CM} = 100\Omega$, simulated loss ranges from 0.5 to 2.0 dB for N=2 and N=4, respectively
Output Impedance	Normally, equal to input port impedance (50Ω)	Equal to $N \times$ input port impedance (200 Ohms for 4x50Ω antenna)
Bandwidth	Very wide bandwidth	Narrow band (70% for 2 port, 20% for 4 port) but, generally, not limiting
Isolation	Very high isolation (>20dB)	Low isolation (-6dB for 2 port, -12 dB for 4 port)
Phase Shifting	Does **not** support Balanced Impedance Phase Shifters (BIPS)	Does support Balanced Impedance Phase Shifters (BIPS)

Table 2.3: Comparison of passive switch-type PS and BIPS for low-power beamforming

	Passive Switched Phase Shifter	**BIPS**
Lossy Components	1 to 2 transistor switches, 2 to 3 fixed value inductors and caps	2 transistor switches, 1 fixed value inductor and 1 programmable caps
Resolution/Loss	Adding 1 bit of resolution, adds 1-3 dB of losses (Q_{COMP}, R_{ON})	Adding bits of resolution doesn't directly drive losses
Range	360°	360°
Amplitude Control	Easy to integrate amplitude control for each antenna element	Not possible to integrate amplitude control for each antenna element. However, amplitude control can be incorporated at the full-array level.

Chapter 3

Array and ASIC System Design

To evaluate the beamformer proposed in Section 1.3 and described in Chapter 2, a prototype beamforming RFIC was designed and fabricated using a bulk 28 nm CMOS process. The fully integrated, passive, 4-channel, RF beamforming IC was designed to operate at 12 GHz (Ku-band) with greater than 5-bits of phase shifter resolution. A printed circuit board (PCB) array was also fabricated with four antennas and a TLT-based power combiner on a Megtron dielectric material. These elements were combined to realize a 4 x 1 linear phased array with a fully passive RF beamformer that could be tested over the air, as shown in Figure. 3.1 and described in detail in the following sections.

The antenna array design is discussed in Section 3.1, the TLTs in Section 3.2, the IC

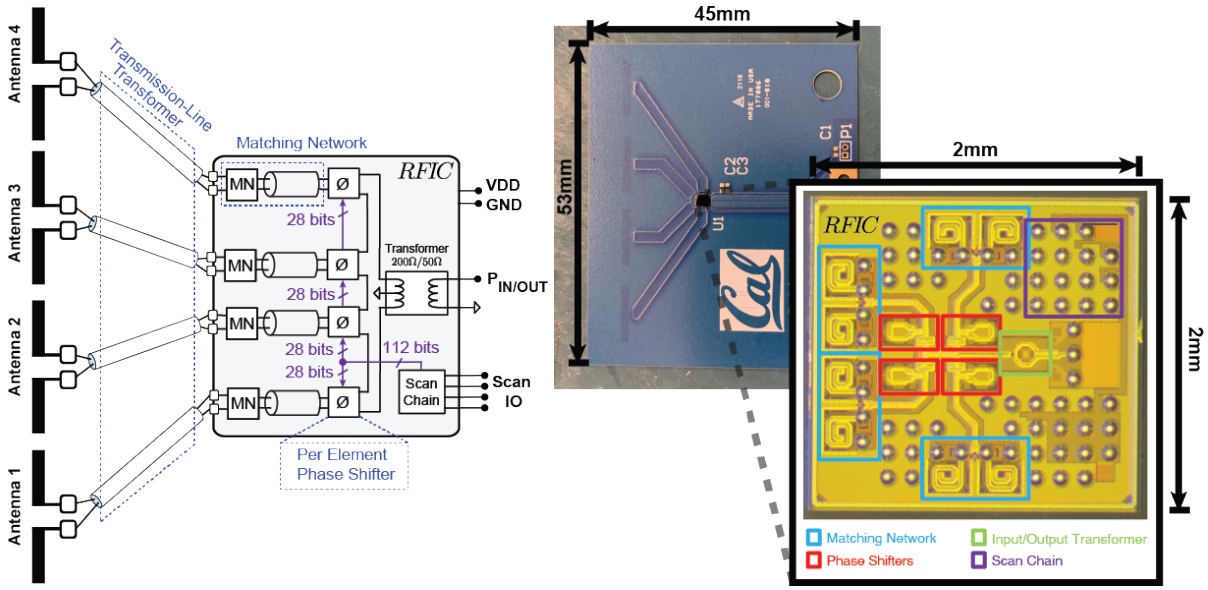


Figure 3.1: Implementation of proposed array showing schematic of custom RFIC

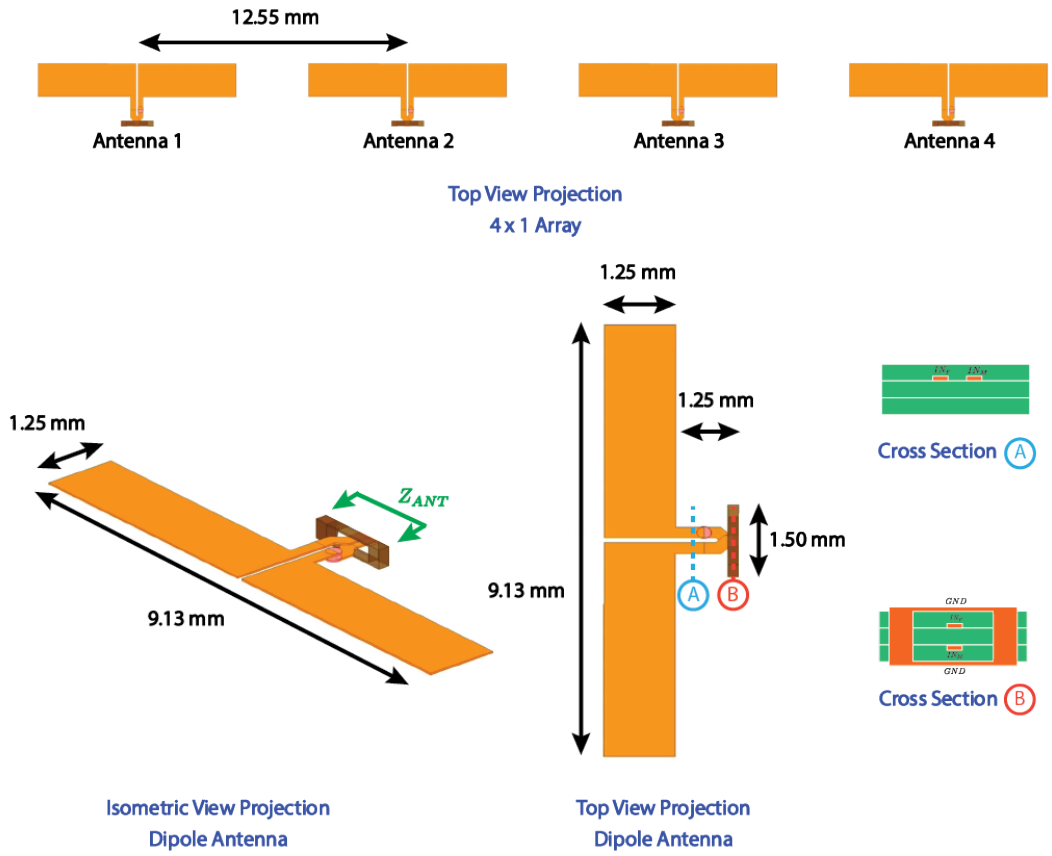


Figure 3.2: Dimensioned detail of dipole antenna and 4 x 1 array

interface and matching network in Section 3.3, and the BIPS in Section 3.4.

3.1 Antenna Array

A four-element linear antenna array was designed for use with the proposed beamformer. It consisted of four 12-GHz half-wavelength dipoles, with 12.55 mm (or approximately half-wavelength) spacing, arranged to maximize broadside radiation and minimize antenna interaction. The array was designed on commercial PCB technology with Panasonics' Megtron 6 dielectric material which has a relative dielectric constant of roughly 3.6 at 12 GHz. The PCB had four copper layers and a finished thickness of 0.41 mm. This resulted in 50 Ω dipoles of length 9.13 mm and width 1.25 mm when routed on layer 2 with 1 oz copper. Dipoles were chosen for their simplicity and because they have a balanced output which makes interface with the TLTs straightforward. The 4 x 1 array and a dimensioned detail of the dipole antenna is shown in Fig. 3.2.

A minimum-sized micro via was used to transition the co-planar feed network shown in cross section A of Fig. 3.2 to the vertical feed network shown in cross-section B. The via had a drill diameter of 152 μm and annular ring of 254 μm. The vertical feed was then enclosed in a ground cage to provide well-defined ground reference for the antenna. The ground cage had an inner width 1 mm and the outer with 1.5 mm. The vertical feed and ground cage allowed for easy direct connection to the broadside-coupled RF lines. The rationale for using broadside-coupled RF lines and their design is described in Section 3.2.

The design was optimized and verified using Finite Element Method (FEM) simulations in ANSYS HFSS. The resulting 12-GHz dipole had a differential, $Z_{ANT(DM)}$, and common-mode impedance, $Z_{ANT(CM)}$, seen at cross-section B of $46 + j4\ \Omega$ and $1 + j53\ \Omega$, respectively. Simulated antenna broadside gain was -0.34 dB and 0.85 dB for the inner and outer dipoles, respectively. The overall simulated broadside gain for the array was 6.15 dB.

3.2 Broad-Side Coupled RF Feedlines for TLT Combining

The RF feed lines which connect the antennas in the array to the custom RFIC double as TLTs to enable low loss series combining on-chip. As described in Section 2.1, for low loss and high bandwidth combining the TLTs should have a differential characteristic impedance of 50 Ω and a common-mode characteristic impedance that is as large as possible.

Differential Microstrip Transmission Lines

Differential microstrip transmission lines would be the natural choice for an RF feedline connecting a differential antenna to an RFIC. These transmission lines generally offer a well-controlled characteristic impedance and strong coupling to the ground plane which reduces electromagnetic interference. Additionally, since both microstrip signal traces are on the top layer, it is easy to interface such transmission lines with surface mount type (SMT) components like RFICs which also reside on the top layer. The structure, relevant dimensions, and parasitic reactances associated with a differential microstrip transmission line are shown in Fig. 3.3.

From Fig. 3.3, we can observe the key relationships between microstrip geometry and per-unit-length parasitic reactances which ultimately define transmission line characteristic impedance, Z_o. First, the per-unit-length inductance under differential excitation (L_d) is proportional to S, where S is the separation between the positive and negative signal traces in the differential pair. Second, the per-unit-length inductance under common–mode excitation (L_c) is proportional to H, where H is the height of the dielectric separating the signal traces from the ground plane. Third, the per-unit-length capacitance under differential excitation (C_d) is proportional to t/S, where t is the trace thickness set by the copper weight. Forth, the per-unit-length capacitance under common–mode excitation (C_c) is proportional to W/H, where W is the signal trace width.

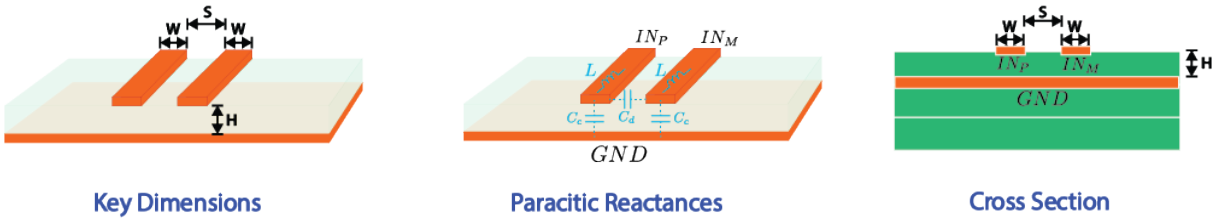


Figure 3.3: Key features for differential microstrip transmission line

$$L_d \propto S \tag{3.1}$$

$$L_c \propto H \tag{3.2}$$

$$C_d \propto t/S \tag{3.3}$$

$$C_c \propto W/H \tag{3.4}$$

Since Z_o is equal to the square root of per-unit-length inductance over capacitance, as shown in Eq. 3.5, we can use the relationships from Eq. 3.1, 3.2, 3.3, and 3.4 to define Z_o under differential and common–mode excitation.

$$Z_{o(x)} = \sqrt{L_x/C_x} \tag{3.5}$$

The resulting relationships between microstrip geometry and Z_o under: common-mode excitation, differential excitation with a near-field ground plane[1], and differential excitation with a far-field ground plane [2] are shown in Eq. 3.6, 3.7, and 3.8, respectively.

$$Z_{o(CM)} = \sqrt{\frac{L_c}{2C_c}} \propto \sqrt{\frac{H}{W/H}} = \frac{H}{\sqrt{W}} \tag{3.6}$$

$$Z_{o(DM)}[nf] = \sqrt{\frac{2L_c}{C_c/2}} \propto \sqrt{\frac{H}{W/H}} = \frac{H}{\sqrt{W}} \tag{3.7}$$

$$Z_{o(DM)}[ff] = \sqrt{\frac{L_d}{C_d}} \propto \sqrt{\frac{S}{t/S}} = \frac{S}{\sqrt{t}} \tag{3.8}$$

[1]Near-field ground plane is defined such that the coupling between the signal traces and ground is significantly higher than the coupling between the signal traces themselves or L_c much smaller than L_d and C_c much greater than C_d. Under these conditions L_c and C_c dominate the expression for $Z_{o(DM)}$.

[2]Far-field ground plane is the opposite of a near-field ground plane. Under these conditions L_d and C_d dominate the expression for $Z_{o(DM)}$.

From Eq. 3.6 and 3.7 with a near-field ground plane (nf), we find that $Z_{o(DM)}$ and $Z_{o(CM)}$ depend on the same dimensions so it is impossible to simultaneously set $Z_{o(DM)}$ to 50 Ω and maximize $Z_{o(CM)}$. From Eq. 3.6 and 3.8 with a far-field ground plane (ff), we see $Z_{o(DM)}$ and $Z_{o(CM)}$ are now independent, allowing us to maximize $Z_{o(CM)}$. However, in this case the practical limitations in PCB minimum spacing between traces and copper weight make it impractical to achieve $Z_{o(DM)}$ of 50 Ω.

Similar results can be visualized using HFSS simulation over a wide range of H and W without making approximations about the ground plane. The minimum S available from our PCB manufacturer was 65 μm and the maximum copper weight was 1oz, which corresponds to a t of 35 μm. Fig. 3.4 and 3.5 show the relevant contour plots of $Z_{o(DM)}$ and $Z_{o(CM)}$, respectively, versus H and W. The design regions of interest are shaded. Under these conditions, the simulation results show that there was no combination of H and W dimensions that allow for $Z_{o(DM)} \approx 50$ Ω and $Z_{o(CM)} > 100$ Ω.

This makes differential microstrip transmission lines a less ideal choice for implementing a TLT for a 4-element series-connected array. They may still function well for 2–element series-connected arrays [58], since arrays with smaller numbers of elements are less sensitive to TLT $Z_{o(CM)}$, per Section 2.1.

Broadside-Coupled Transmission Lines

Broadside coupled transmission lines do not rely on coplanar signal traces. Instead the signal traces are routed on top of one another with the PCB dielectric sandwiched in the middle, increasing the coupling area and reducing the effective electrical separation. This allows for more control of $Z_{o(DM)}$ without relying on coupling to the ground plane. The structure, relevant dimensions, and parasitic reactances associated with a differential microstrip transmission line are shown in Fig. 3.6.

Much like we did for the microstrip, from Fig. 3.6, we can observe the key relationships between broadside coupled transmission line geometry and per-unit-length parasitic reactances which define Z_o. First, the per-unit-length inductance under differential excitation (L_d) is proportional to S, where S is the height of the dielectric separating the positive and negative signal traces in the differential pair. Second, the per-unit-length inductance under common–mode excitation (L_c) is proportional to H, where H is the separation between the signal traces from the ground plane. Third, the per-unit-length capacitance under differential excitation (C_d) is proportional to W/S, where W is the signal trace width. Forth, the per-unit-length capacitance under common–mode excitation (C_c) is proportional to t/H, where t is the trace thickness set by the copper weight.

$$L_d \propto S \tag{3.9}$$

$$L_c \propto H \tag{3.10}$$

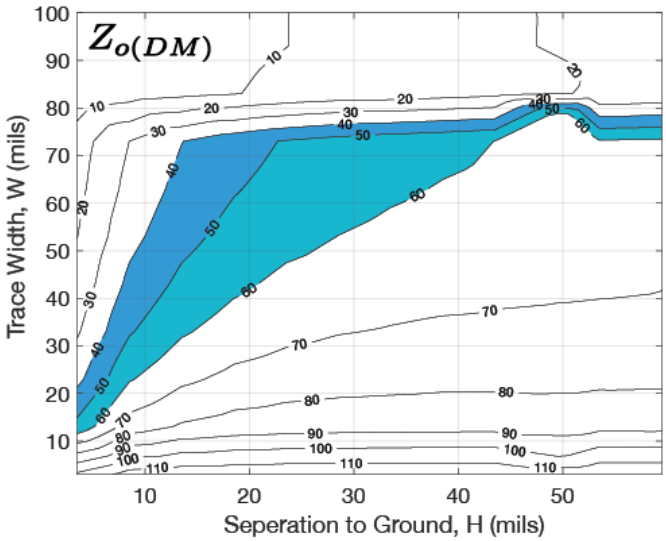


Figure 3.4: Contour of simulated $Z_{o(DM)}$ versus H and W for microstrip coupled transmission line with $Z_{o(DM)} \approx 50\ \Omega$ region shaded.

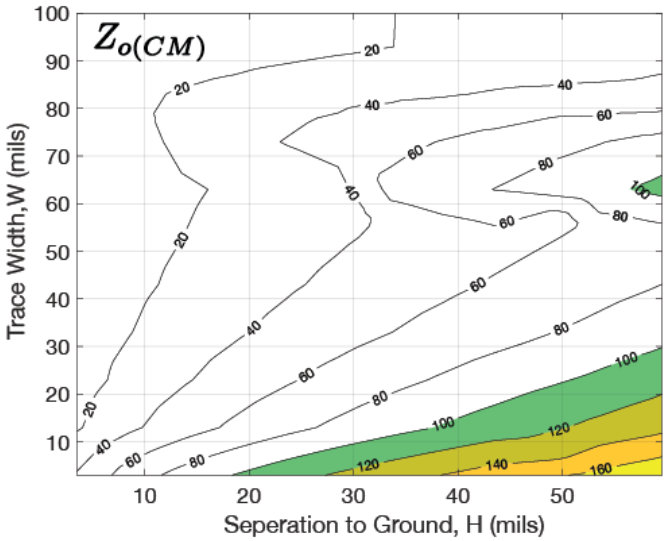


Figure 3.5: Contour of simulated $Z_{o(CM)}$ versus H and W for microstrip coupled transmission line with $Z_{o(CM)} > 100\ \Omega$ region shaded.

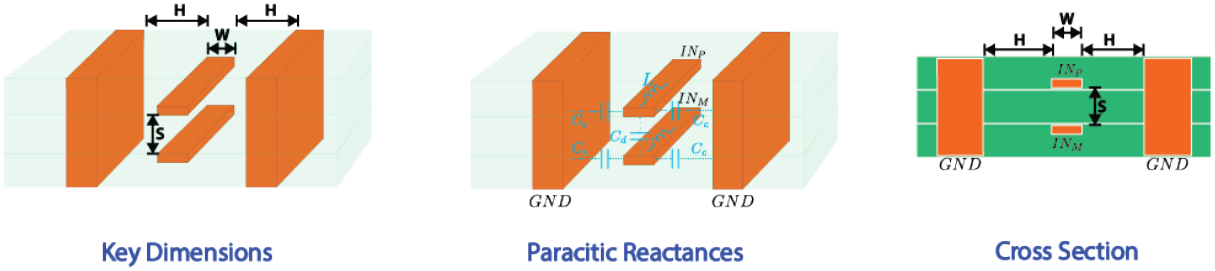


Figure 3.6: Key features for broadside-coupled microstrip transmission line

$$C_d \propto W/S \tag{3.11}$$

$$C_c \propto t/H \tag{3.12}$$

Using Eq. 3.5 again, we can exploit relationships from Eq. 3.9, 3.10, 3.11, and 3.12 to define Z_o under differential and common–mode excitation for broadside coupled transmission lines. The resulting relationships between broadside geometry and Z_o under common-mode and differential excitation are shown in Eq. 3.13 and 3.14, respectively.

$$Z_{o(CM)} = \sqrt{\frac{L_c/2}{4C_c}} \propto \sqrt{\frac{H}{t/H}} = \frac{H}{\sqrt{t}} \tag{3.13}$$

$$Z_{o(DM)} = \sqrt{\frac{L_d}{C_d}} \propto \sqrt{\frac{S}{W/S}} = \frac{S}{\sqrt{W}} \tag{3.14}$$

Eq. 3.13 and 3.14 show that $Z_{o(DM)}$ and $Z_{o(CM)}$ are now independent. Therefore, it is possible to simultaneously set $Z_{o(DM)}$ to 50 Ω and maximize $Z_{o(CM)}$, even when considering the practical limitations in PCB minimum spacing between traces and copper weight. This makes broadside coupled transmission lines a more ideal choice for implementing a TLT for a 4-element series-connected array.

TLT Design Procedure

Given the choice of a broadside-coupled transmission line, it was necessary to design a TLT network for our specific antenna array. The design procedure that was used to realize the TLT incorporated in the RF feed lines for the prototype system is outlined below. All steps were guided by FEM electro-magnetic simulation using HFSS.

First, the broadside coupled transmission line $Z_{o(DM)}$ was set to 50 Ω by adjusting W and S. Larger S values result in larger W for the same $Z_{o(DM)}$, per Eq. 3.14, which can reduce resistive losses. However, large S values require larger diameter vias, due to limitations in

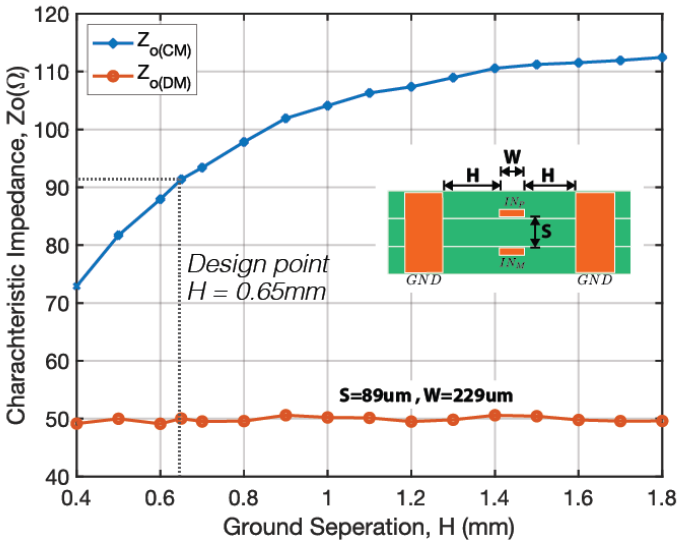


Figure 3.7: Simulated Z_o as a function of H for broadside coupled transmission line.

PCB manufacturing drill aspect ratio. Larger vias have greater parasitic inductances and make it challenging to route in tight spaces. For this reason, a S value of 89 μm was chosen to allow us to maximize W while using the minimum-diameter laser-drilled micro vias available from our PCB manufacturer, 152 μm. This resulted in a W of 229 μm, which is roughly equivalent to the W required for a differential microstrip using the same PCB stack up.

Second, H is swept while W and S are kept constant to find a value of H that provides sufficiently high $Z_{o(CM)}$ without requiring too much board area. The resulting $Z_{o(DM)}$ and $Z_{o(CM)}$ values versus H are simulated and plotted in Fig. 3.7. Note, $Z_{o(DM)}$ remains constant as H is swept, as expected from Eq. 3.14. An H value of 650 μm was chosen as a compromise between high $Z_{o(CM)}$ and small transmission line cross-sectional area. This resulted in a $Z_{o(CM)}$ of 92 Ω and a $Z_{o(DM)}$ of 50 Ω.

Third, the length of the transmission lines are adjusted to present a large real effective common-mode impedance at the RFIC interface, using the principles outlined in Section 2.1. We will refer to the effective common-mode impedance seen at the RFIC interface as $Z_{INT(CM)}$. Based on antenna common-mode impedance, $Z_{ANT(CM)}$, the optimal transmission line lengths, ℓ, to produce a large real $Z_{INT(CM)}$ were found to be 12 mm and 21 mm. Since $Z_{o(DM)} \approx Z_{ANT} \approx 50\ \Omega$, note that $Z_{INT(DM)} \approx 50\ \Omega$ and is relatively unchanged by ℓ. However, the different ℓ values translated to a 250° delay in the signal from the outer to the inner elements that must be accounted form in the predicted beamformer states.

Finally, the transmission lines are routed from the antennas in the linear array to the RFIC as shown in Fig. 3.8. The longer transmission line length, $\ell_1 = 21\ mm$, was used to route the outer antennas, and the shorter transmission line length, $\ell_2 = 12\ mm$, was used

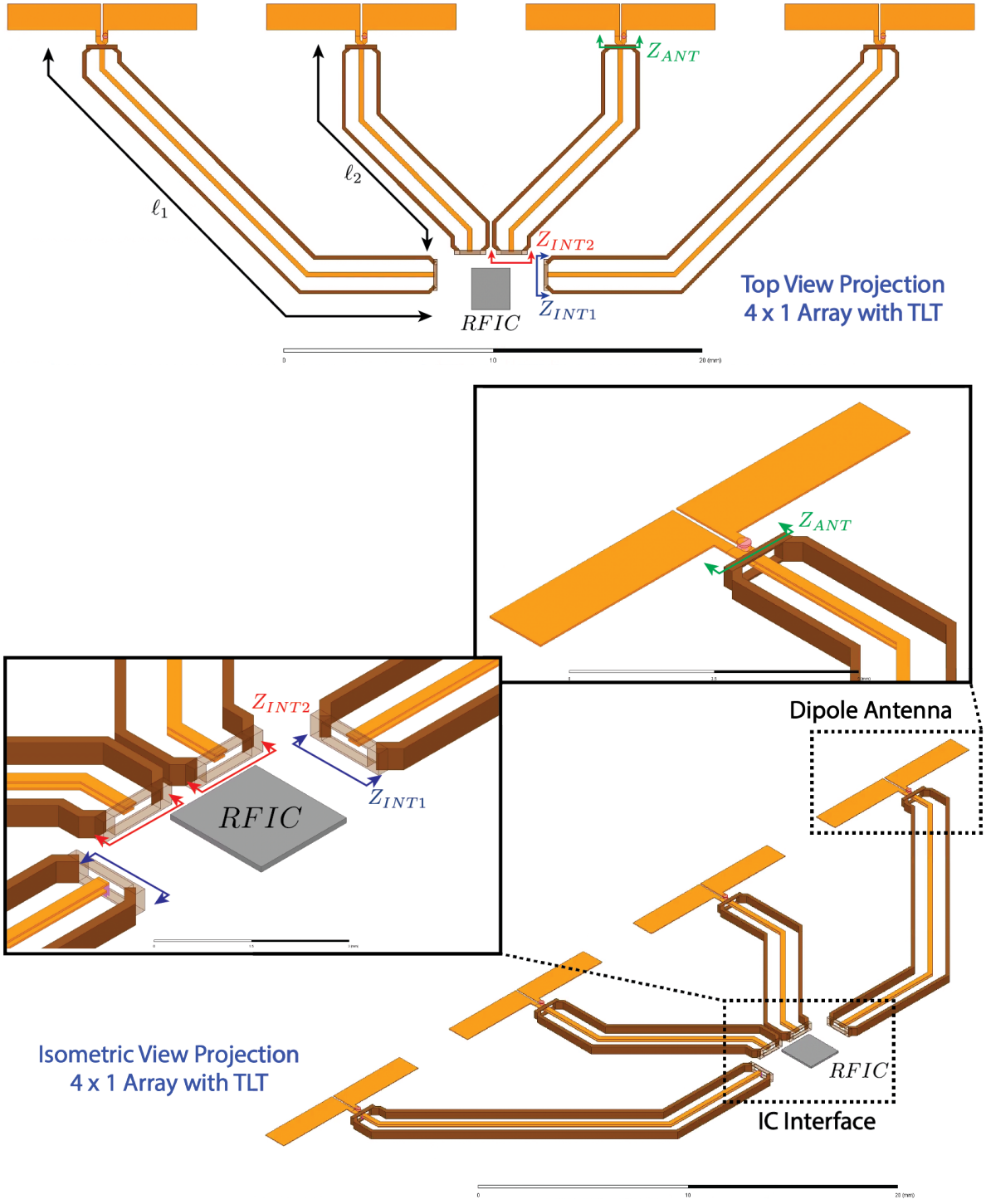


Figure 3.8: TLT routing from antenna array to RFIC

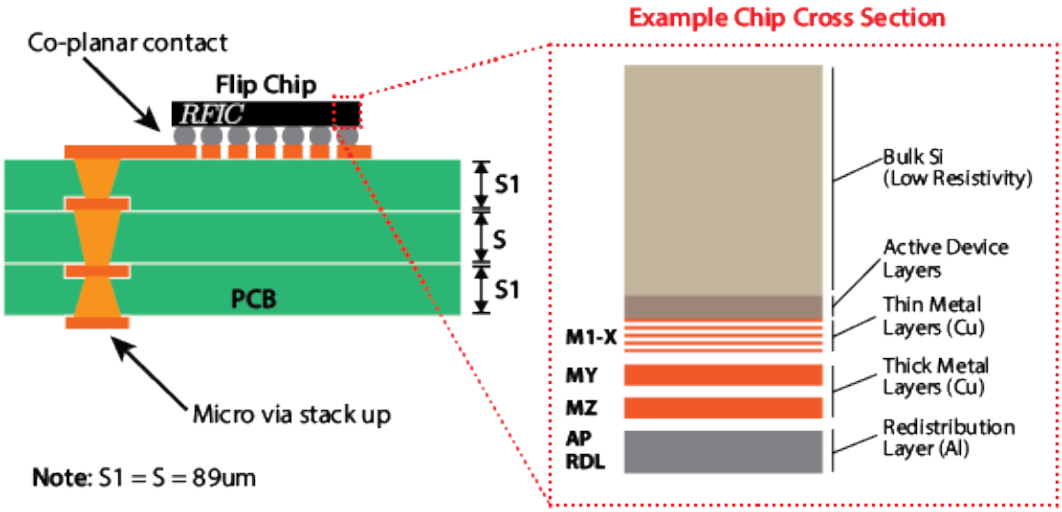


Figure 3.9: Cross section of PCB and flip chip RFIC

to route the inner antennas. This results in a $Z_{INT1(CM)}$ of $633 + j105\ \Omega$ and $Z_{INT2(CM)}$ of $368 + j128\ \Omega$ for the inner and outer transmission lines, respectively. A ground cage, identical to one described in the antenna subsection, was placed at the end of the transmission lines to provide a well-defined ground reference for the interface to the RFIC.

3.3 IC Interface and On-Chip Matching Networks

It was not possible to maintain a broadside-coupled transmission line from the PCB to the RFIC since the solder balls connecting the RFIC to the PCB require coplanar contact on the top layer. Furthermore, once on chip, broadside-coupled lines are more lossy because they allow the signal traces to couple to the resistive bulk substrate only a few microns away, as shown in Fig. 3.9. These features meant that the routing from the TLTs to the IC solder balls and from the solder balls to the central summing node introduce unwanted parasitics. These parasitics are managed with an on-chip matching network designed to compensate for the routing associated with the IC interface and on-chip transmission lines. The IC interface and on-chip matching networks are discussed below.

IC Interface

The transition between the RFIC and the PCB featured a traditional ground signal signal ground (GSSG) pad layout with bump spacing of $S_{bump} = 150\ \mu m$. GSSG layouts provide good signal to signal coupling and shield the diff pair on both sides with a ground metal during the transition. A column of stacked microvias was used to transition the broadside-

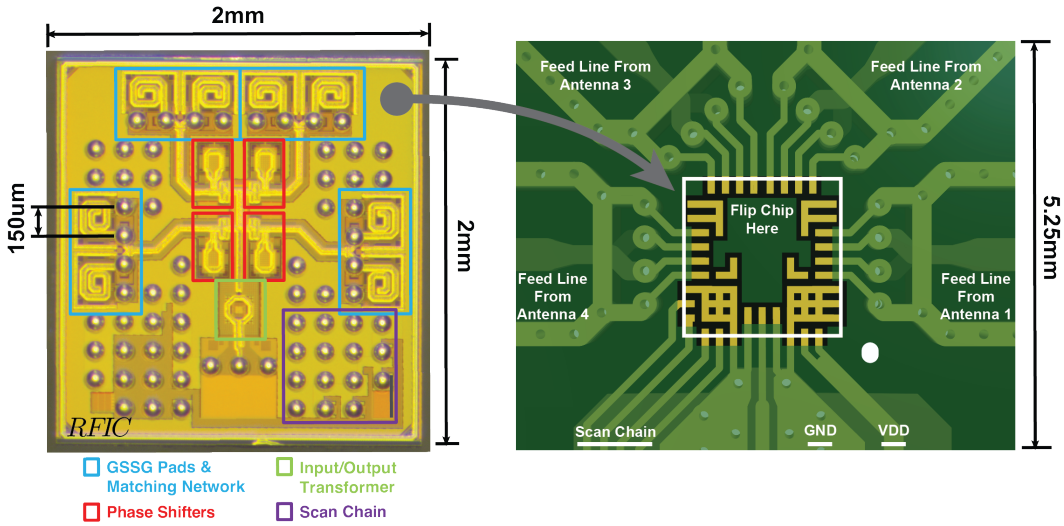


Figure 3.10: Interface between TLT feed lines and flip chip RFIC

coupled TLT signal traces from layers two and three up to the top layer. Then traces with minimum width and spacing were used to connect from the vias to the RFIC GSSG pads. Minimum width and spacing was defined by our PCB vendor as $W_{min} = 75\ \mu m$ and $S_{min} = 75\ \mu m$, respectively. This resulted in the IC interface shown in Fig. 3.10.

On-Chip Matching Networks

An on-chip differential microstrip line of length $\ell_{TL} = 500\ \mu m$ was used to route the signals from the GSSG pads to the summing node at the center of the IC. The microstrip line was routed on the thickest metal layers to reduce losses, with the signals on the aluminum redistribution layer (AP RDL) and the ground on the furthest available thick copper layer (MY). Transmission signal spacing and width were chosen such that the line had a $Z_{O(DM)}$ of 50 Ω to minimize unintended differential impedance transformations. This resulted in a microstip with signal width of 10 μm, spacing of 5 μm, and a $Z_{O(CM)}$ of 20 Ω. The parasitic effects of this on-chip transmission line and IC interface were modeled in HFSS to provide a baseline for matching network design, as shown in Fig. 3.11.

The matching network shown in Fig. 3.12 was used to compensate for the parasitic effects of the IC interface and on-chip transmission line. The network consisted of two shunt inductors (L_{sh}) which also provided ESD protection, a differential capacitor (C_{sh}), and a pair of series capacitors (C_{ser}). This schematic can be decomposed into an equivalent differential-mode and common-mode matching network which allowed us to achieve simultaneous matching for both modes through careful design of L_{sh}, C_{sh} and C_{ser}. The parasitic capacitance on the signal pads, $C_{pad} = 60\ fF$, was also modeled in the network for accuracy.

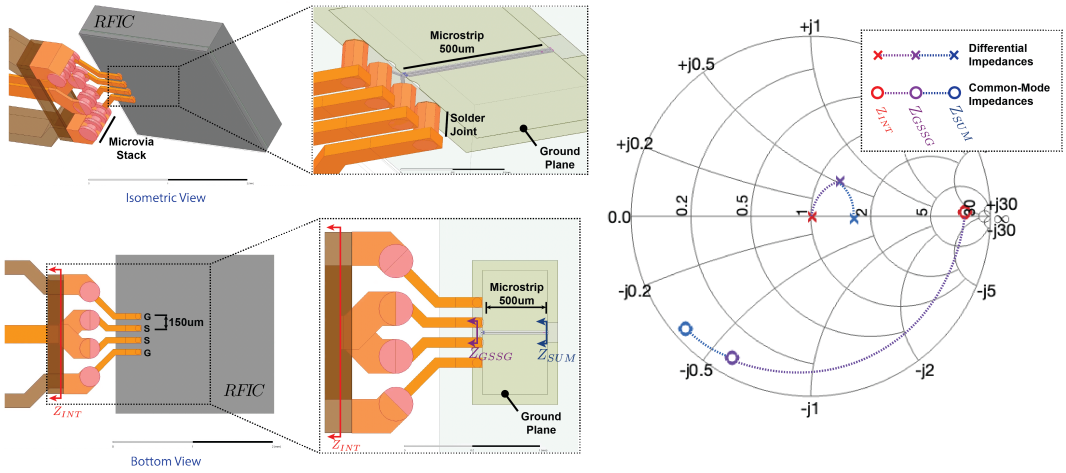


Figure 3.11: HFSS model for on-chip transmission line and IC interface

The design procedure for the on-chip matching network proceeded as follows: First, we assume that $Z_{sh(DM)} = 2L_{sh}||C_{sh}||C_{pad}/2$ is selected correctly to place $Z_{GSSG(DM)}$ on the unit circle. The values for L_{sh} and C_{sh} are under constrained at this point and were finalized later in the design procedure. Second, the value of C_{ser} is set to move $Z_{MN(DM)}$ to 50 Ω. Since the on-chip microstrip line has a $Z_{o(DM)}$ of 50 Ω, setting $Z_{MN(DM)}$ to 50 Ω, effectively sets $Z_{SUM(DM)}$ to 50 Ω for any ℓ_{TL}. Third, the value of L_{sh} was set to maximize the real component of $Z_{SUM(CM)}$, given the derived C_{ser}. Fourth, having set L_{sh} in the previous step, the value for C_{sh} was determined based on the requirements for $Z_{sh(DM)}$ in step one. Finally, local optimization was performed to finalize values of L_{sh}, C_{sh} and C_{ser} using realistic estimates of component Q.

This procedure resulted in a matching network with $L_{sh} = 0.418\ nH$, $C_{sh} = 50\ fF$ and $C_{ser} = 1.21\ pF$. The inductors were implemented on the thick metal AP RDL and MZ layer with a spiral configuration to maximize inductance per unit area and Q. An inductor Q of 15 at 12 GHz was predicted, based on high-frequency electromagnetic EMX simulation. Metal-over-metal (MOM) capacitors routed on the high density thin metal layers from M2 to M6 were used for C_{par} and C_{ser}. The capacitor terminals were connected with vias to the AP layer. A capacitor Q of 140 for C_{sh} and 14 for C_{ser} at the AP layer was predicted using EMX simulation.

The impact of the matching network on the summing node impedance is shown in Fig. 3.13. The simulated summing node impedance at 12GHz after the antenna, TLT, IC interface, on-chip matching network, and microstrip line was $Z_{SUM(DM)} = 48.7 + j0.2\ \Omega$ and $Z_{SUM(CM)} = 245.8 - j76.5\ \Omega$. Based on the theory discussed in Section 2.1 and plotted in Fig. 2.3, a common-mode impedance of 245 Ω at the summing node is expected to contribute roughly 1 dB of combining losses. Additionally, simulations of the 500 μm of microstrip transmission line indicate it adds roughly 0.6 dB of resistive losses.

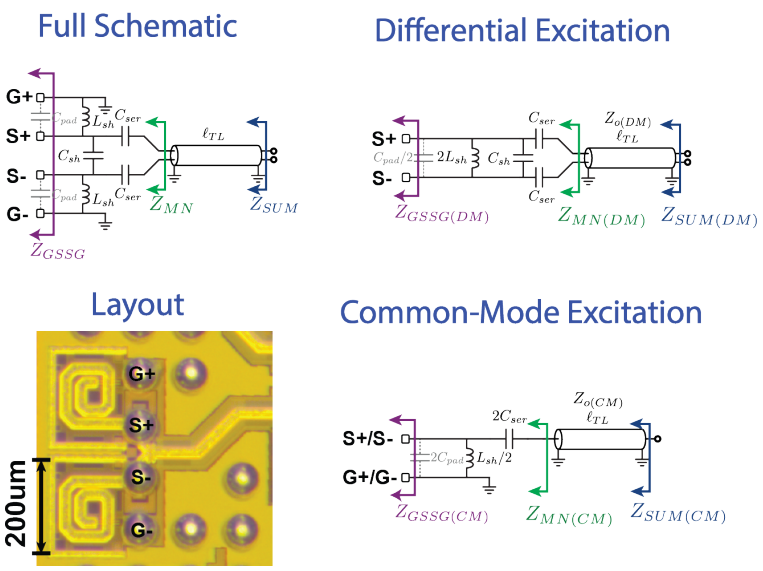


Figure 3.12: On-chip matching network schematic and layout

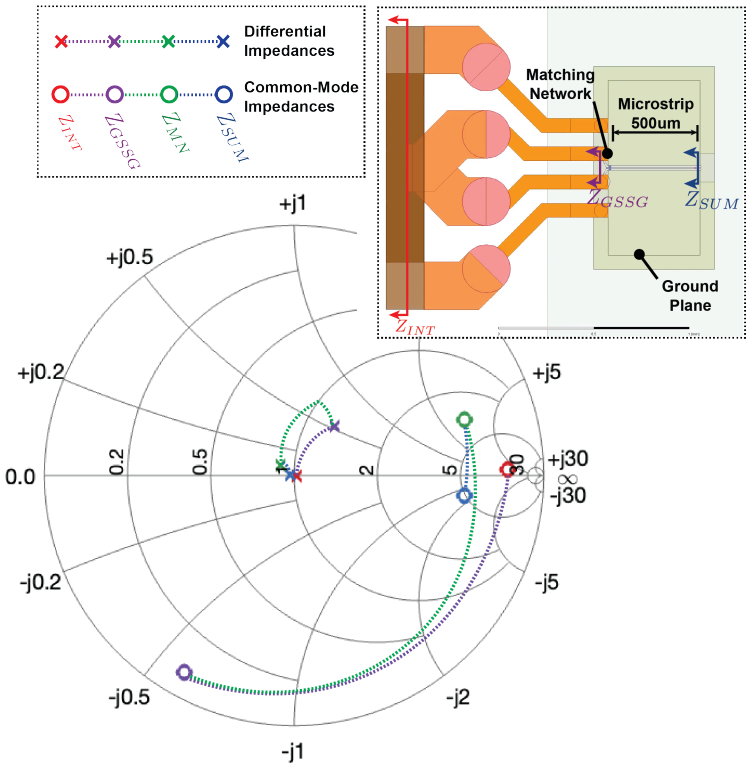


Figure 3.13: Smith chart of simultaneous differential-mode and common-mode matching

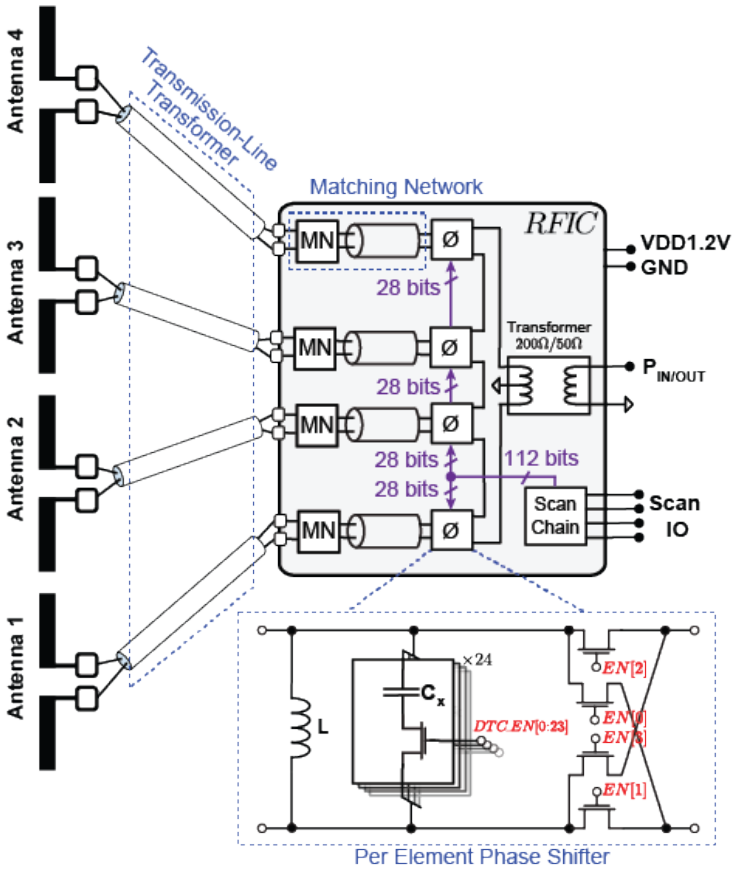


Figure 3.14: Integration BIPS with crossover switch into system

3.4 Balanced Impedance Phase Shifters with Crossover Switch

The on-chip balanced impedance phase shifters (BIPS) are connected in shunt across each antenna element just before the series connections, as shown in Fig. 3.14. They consist of a crossover switch to implement ±180° phase shifts and a programmable admittance for smaller phase shifts, realized using a fixed inductor and digitally tunable capacitor. The control strategy used by the BIPS relies on balanced impedance tuning, such that any positive susceptance added in shunt across one antenna element is cancelled by the negative susceptances added in shunt across the other elements, resulting in coherent summation of antenna signals with minimal impedance variation at the load. This strategy significantly reduces the number of RF switches and passives needed for the phase shifter, resulting in a much lower-loss solution. The optimal state values for a given angle of arrival are predicted by solving Kirchhoff's equations using the BIT algorithm in Section 2.3 to determine which

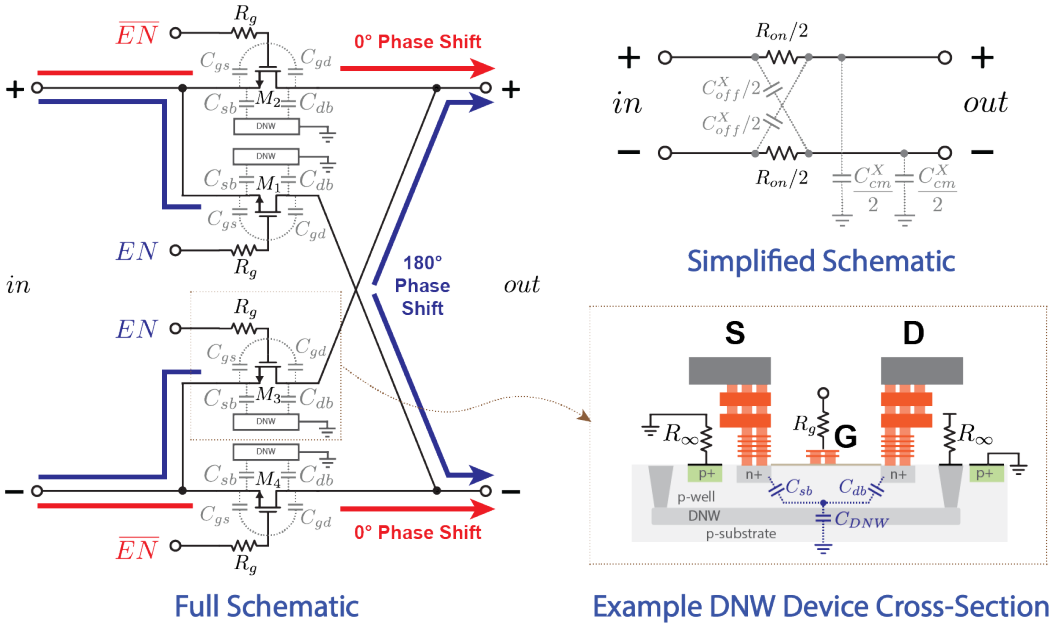


Figure 3.15: Detailed crossover switch schematic showing DNW NMOS transistors

combination of **EN** and **Y** maximize the power delivered to the load. The crossover switch, programmable admittance elements, and their overall integration are discussed below.

Crossover Switch

The phaseshifter crossover switch was designed using four 1V NMOS transistors in a passive triode configuration as shown in Fig. 3.15. Each transistor had a W/L of 22μm/30nm and had their source and drains connected up to the AP RDL, while the gate was routed on the thin metal layer (M2). The resulting crossover switch had a fully routed on-resistance of approximately $R_{on} = 5.5\ \Omega$ when driven with a 1V gate drive. From Eq. 3.15, the on-state conduction losses given R_{on}, IL_{on}, was expected to be -0.5dB.

$$IL_{on} = 20\log_{10}\left(\frac{2Z_o}{2Z_o + R_{on}}\right) \tag{3.15}$$

Ultimately, the size of the devices and therefore the minimum R_{on} we could achieve was limited by the devices parasitic off-state capacitance and associated routing capacitance, C_{off}. Both C_{off} and the off-state capacitance from the programmable capacitor limit the maximum inductor value that can be used to realize the phaseshifter, which in turn limits Z_L and increases L_{BIPS}, per Eq. 2.58 in Section 2.3.

The NMOS devices were placed inside a deep N well (DNW) to reduce parasitic capacitance to the substrate, C^X_{cm} [65]. Smaller C^X_{cm} values reduce common-mode currents and

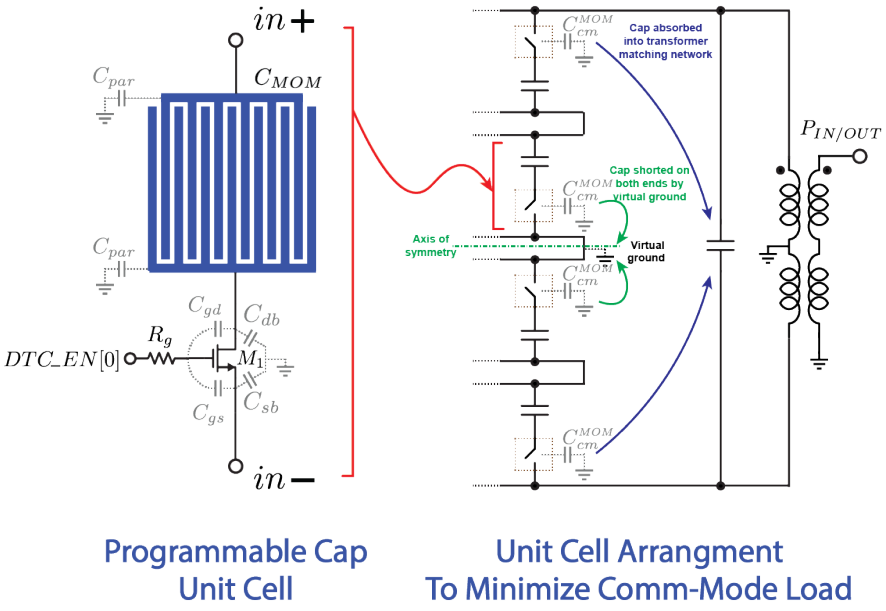


Figure 3.16: Capacitor unit cell with asymmetry to minimize common-mode loading

common-mode losses, per Eq. 2.14 in Section 2.1. In addition, an explicit 10 kΩ gate resistor was added to prevent common-mode currents from flowing through C_{gs} and C_{gd} into the supply rails. Approximate expressions for C_{off}^{X} and C_{cm}^{X} in terms of known device parameters are shown in Eq. 3.16 and Eq. 3.17. Fully extracted EMX simulation of the crossover switch predicted $C_{off}^{X} = 226fF$ and $C_{cm}^{X} = 181fF$.

$$C_{off}^{X}/2 = (1/C_{gs} + 1/C_{gd})^{-1} + (1/C_{sb} + 1/C_{db})^{-1} \tag{3.16}$$

$$C_{cm}^{X}/2 = 2[(1/(C_{db} + C_{sb}) + 1/C_{DNW})^{-1}] \tag{3.17}$$

The transistor gates were driven by a scan chain with a unique register for each NMOS transistor. This allowed for normal 1-bit operation, $EN = 0 \rightarrow 0°$ phase shift and $EN = 1 \rightarrow 180°$ phase shift, but it also allowed us to disable individual transistors during debug.

Digitally Tunable Capacitor

A digitally tunable capacitor (DTC) was designed using a bank of switchable capacitor unit cells for use in the phase shifter. The capacitor unit cells consisted of a fixed MOM capacitor and a 1V NMOS transistor switch, as shown in Fig. 3.16. Each cell had a C_{on}^{MOM} of 22 fF and a C_{off}^{MOM} of 6 fF, with a typical Q of 25 when on and 73 when off at 12 GHz.

There is an inherent asymmetry in the unit cell's parasitic capacitance to the substrate ground since the transistor is connected directly to the negative terminal. We leverage this

asymmetry to reduce the common-mode loading effects, per Fig. 3.16. Unit cells on the outer elements are arranged such that their parasitic capacitance to ground can be absorbed by the differential matching capacitor on the input/output transformer (200 Ω/50 Ω). Unit cells on the inner elements are arranged such that their parasitic capacitance to ground is shorted by the virtual ground along the circuits axis of symmetry. Like the crossover switch, the transistors in the capacitor unit cells also included an explicit 10 kΩ gate resistor to prevent common-mode currents from flowing through C_{gs} and C_{gd} into the supply rails.

Overall Phaseshifter

The phaseshifter's programmable admittance was implemented using a fixed 200pH inductor in parallel with a DTC, consisting of a bank of twenty-four switchable MOM capacitor unit cells. When considering transistor parasitics in the crossover switch and the C_{on}-to-C_{off} ratio of the capacitor unit cells, this combination was found to produce the desired susceptances needed for the full range of phase shift while exceeding the required quantization for 5-bit performance (4^+ bits from the programmable admittance with 24 possible states and 1-bit from the crossover switch). The simulated admittance values across scan configuration are shown in Fig. 3.17. A phaseshifter Q of roughly 2, was expected based on the extracted simulation results. Based on Eq. 2.56, this would contribute roughly 1.8 dB of loss.

Using the simulated phaseshifter admittance values and the algorithm for maximizing power with BIPS from Section 2.3, we can predict the optimal beamformer states for any given angle of arrival (θ). It is important to take into consideration the relative phase shift from the inner to the outer antenna elements due to differences in feed line length for this calculation. The predicted optimal beamformer states for select θ are shown in Table 3.1.

The state of the beamformer is described by three vectors: A binary **EN** vector which details the state of the 180° crossover switches across each element, A **Y** vector which details the ideal admittance across each element in mS, and a **DTC_EN** vector which maps the desired **Y** values to the DTC state to realize that approximate admittance across each element. The values for DTC_EN_i range from 0 to 24 and represent the number of capacitor unit cells enabled in the DTC. The relationship between **Y** and **DTC_EN** is described in Eq. 3.18, where C_{on}^{MOM} and C_{off}^{MOM} are MOM cap unit cells on and off-capacitance, respectively. Each vector contains four values with subscripts indicating the element for which they are associated, see Eq. 3.19, 3.20, and 3.21.

$$\mathbf{Y} = j\omega(C_{on}^{MOM} \cdot \mathbf{DTC\_EN} + C_{off}^{MOM} \cdot [24 - \mathbf{DTC\_EN}]) - j\frac{1}{\omega L} \tag{3.18}$$

$$\mathbf{Y} = [Y_1,\ Y_2,\ Y_3,\ Y_4] \tag{3.19}$$

$$\mathbf{DTC\_EN} = [DTC\_EN_1,\ DTC\_EN_2,\ DTC\_EN_3,\ DTC\_EN_4] \tag{3.20}$$

$$\mathbf{EN} = [EN_1,\ EN_2,\ EN_3,\ EN_4] \tag{3.21}$$

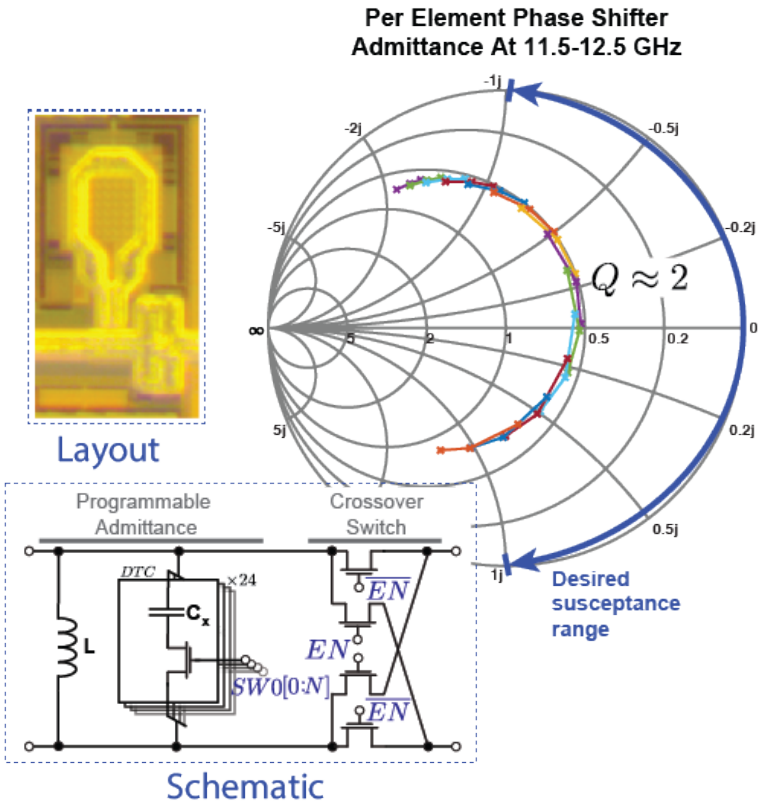


Figure 3.17: BIPS schematic, layout, and simulated admittance values

Table 3.1: Optimal beamformer states for select angle of arrival (θ)

θ (°)	**Y** (mS)				**DTC_EN**				**EN**			
-90	-13.33	10.00	10.00	-13.33	10	20	20	10	0	0	1	1
-85	-13.33	10.00	10.00	-13.33	10	20	20	10	0	0	1	1
-80	-13.33	10.00	13.33	-10.00	10	20	21	11	0	0	1	1
-75	-13.33	10.00	13.33	-6.67	9	20	21	12	0	0	1	1
-70	-16.67	10.00	13.33	-6.67	9	20	21	13	0	0	1	1
-65	-20.00	10.00	13.33	-3.33	7	19	21	14	0	0	1	1
-60	20.00	-6.67	0.00	-13.33	24	12	15	9	0	1	0	0
-55	16.67	-10.00	3.33	-10.00	22	11	16	11	0	1	0	0
-50	13.33	-10.00	3.33	-6.67	21	11	17	13	0	1	0	0
-45	6.67	-13.33	6.67	0.00	19	11	18	16	0	1	0	0
-40	3.33	-13.33	10.00	6.67	16	10	19	18	0	1	0	0
-35	-3.33	-16.67	10.00	13.33	14	9	20	21	0	1	0	0
-30	16.67	10.00	-20.00	-13.33	23	20	8	11	0	1	1	1
-25	13.33	10.00	-13.33	-3.33	21	20	9	14	0	1	1	1
-20	3.33	6.67	-13.33	3.33	18	19	10	17	0	1	1	1
-15	-3.33	3.33	-10.00	10.00	14	17	11	20	0	1	1	1
-10	-13.33	0.00	-10.00	16.67	11	16	12	23	0	1	1	1
-5	-3.33	13.33	10.00	-20.00	14	21	19	7	0	1	1	0
0	-13.33	10.00	10.00	-13.33	10	20	20	10	0	1	1	0
5	-20.00	10.00	13.33	-3.33	7	19	21	14	0	1	1	0
10	16.67	-10.00	0.00	-13.33	23	12	16	11	0	0	0	1
15	10.00	-10.00	3.33	-3.33	20	11	17	14	0	0	0	1
20	3.33	-13.33	6.67	3.33	17	10	19	18	0	0	0	1
25	-3.33	-13.33	10.00	13.33	14	9	20	21	0	0	0	1
30	-13.33	-20.00	10.00	16.67	11	8	20	23	0	0	0	1
35	13.33	10.00	-16.67	-3.33	21	20	9	14	0	0	1	0
40	6.67	10.00	-13.33	3.33	18	19	10	16	0	0	1	0
45	0.00	6.67	-13.33	6.67	16	18	11	19	0	0	1	0
50	-6.67	3.33	-10.00	13.33	13	17	11	21	0	0	1	0
55	-10.00	3.33	-10.00	16.67	11	16	11	22	0	0	1	0
60	-13.33	0.00	-6.67	20.00	9	15	12	24	0	0	1	0
65	-3.33	13.33	10.00	-20.00	14	21	19	7	0	0	1	1
70	-6.67	13.33	10.00	-16.67	13	21	20	9	0	0	1	1
75	-6.67	13.33	10.00	-13.33	12	21	20	9	0	0	1	1
80	-10.00	13.33	10.00	-13.33	11	21	20	10	0	0	1	1
85	-13.33	10.00	10.00	-13.33	10	20	20	10	0	0	1	1
90	-13.33	10.00	10.00	-13.33	10	20	20	10	0	0	1	1

Chapter 4

Measurement Results

4.1 Experimental Setup

The array described in Chapter 3 was evaluated using the over-the-air (OTA) measurement setup shown in Fig. 4.1. It consisted of an anechoic environment (built using foam RF-absorbers), a 4-port network analyzer (Agilent N5242A, PNA X, 26.5 GHz), two precision rotating platforms, and a USB-to-SPI adapter for digital control of the RFIC. Control of the precision rotating platforms and PNA measurement acquisition were automated to ensure repeatability. This setup allowed us to measure the S-parameters and derive the far-field gain for the proposed array (or antenna under test, AUT). The measurement procedure is outlined below.

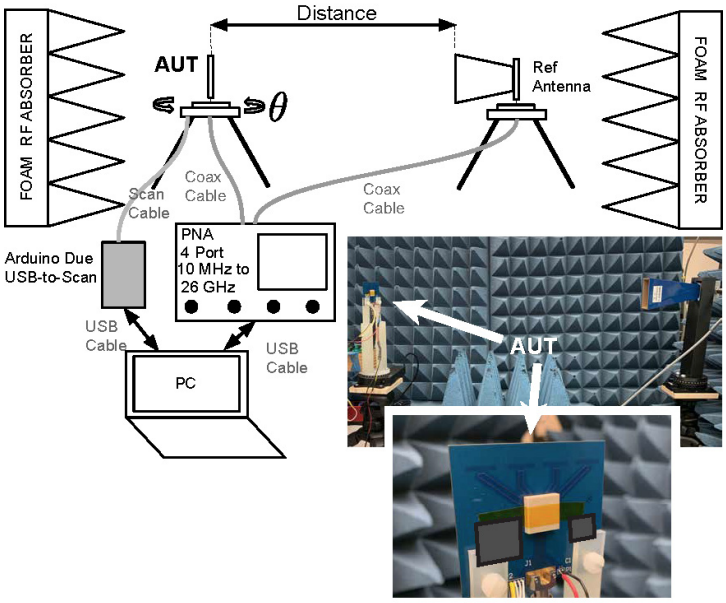


Figure 4.1: Far-field OTA measurement setup for proposed RF beamformer

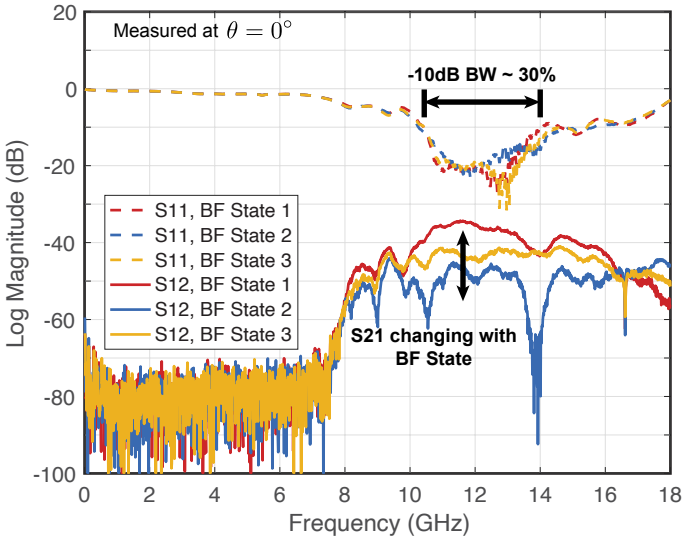


Figure 4.2: Measured beamformer, BF, S-parameters for three different BF states

First, the measurement distance was set to 0.546 m to ensure that only the far-field radiation patterns were captured. This distance was based on the estimated far-field distance [66] for the array being greater than $2D^2/\lambda$. Second, the gain for the reference (Ref) antenna, G_{REF}, was characterized using measured S-parameters and the three-antenna method [67], [68] at 12 GHz. Third, using the same Ref antenna, the S-parameters for the proposed array was measured over a $\pm 90°$ range in azimuth angle, θ. Finally, the radiation patterns for the proposed array ($G_{AUT}(\theta)$) were calculated from the $S21(\theta)$ data using Eq. 4.1. The Friis free space path loss, L, is 48.7 dB at 12 GHz at a distance of 0.546 m. Experimental results obtained from this procedure are described in Section 4.2.

$$G_{AUT}(\theta) = 20\log_{10}(|\boldsymbol{S21(\theta)}|) + L - G_{REF} \tag{4.1}$$

4.2 Results

Measured beamformer, BF, S-parameters for three different beamformer states are shown in Fig. 4.2. As the BF state changes from State 1 to 3, steering the beam away from 0°, the peak S21 value drops, as expected. However, S11 is largely unchanged with BF state, indicating there is minimal impedance variation with beam angle.

The resulting uncalibrated beam patterns, shown in Fig. 4.3, demonstrate strong agreement with theoretical results from Table 3.1, having a beam angle RMS error of 3.35° between +40° and -40° and a 3 dB scan angle of ±55°. The system has a half power beam width (HPBW) of 27° and a sidelobe level of -10 dB, at a beam angle of 0°, which agrees well

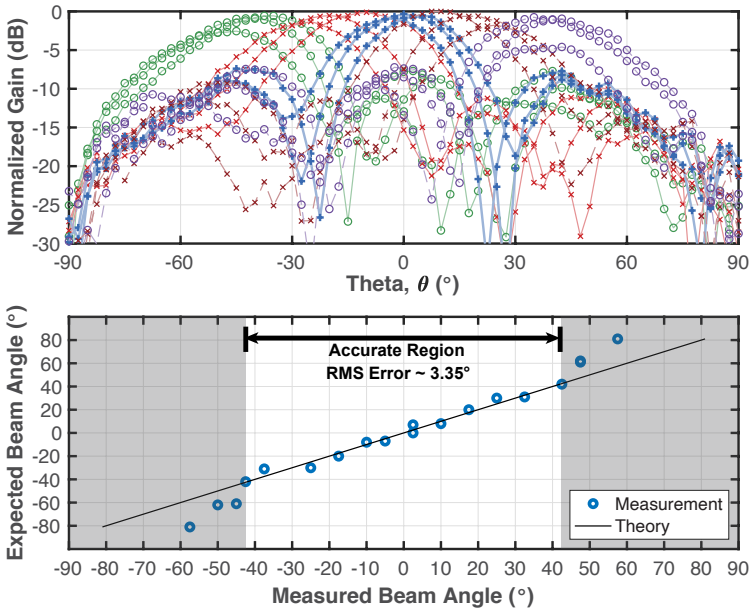


Figure 4.3: Measured beam patterns and comparison of measured beam angles to predicted beam angles, without calibration.

with the expected performance for a 4-element linear phased array. The beam angle RMS error and sidelobe level can both be improved with calibration, which is quite common in state-of-the-art beamformers.

The beamformer loss is derived by examining the difference in the expected system gain from detailed antenna-only HFSS simulation and the measured beamformer gain after de-embedding 1.03 dB of loss for the on-chip transformer. This procedure is illustrated in Fig. 4.4. The simulated array gain at broadside (0°) is 6.11 dBi, while the measured array gain after the beamformer is 0.73 dBi. From the difference in these two, we obtain an estimated beamformer loss of 5.4 dB. This compares reasonably well with the simulated loss of 4.53 dB and theoretical loss of 4.22 dB.

Also shown in Fig. 4.4 is the minimum achievable beam angle for uniform phase shift given our phase shifters LSB step size. Here we observe a beam angle resolution of between 1° and 2°, which agrees well with the expected step size based on the slightly-greater-than 5-bit phase shifter resolution.

To measure the input referred P1dB point, the BF input power was swept from -10 dBm to 16 dBm, the upper limit for the PNA, while recording the S21. A 0.1 dB drop is observed in the device S21 at +16 dBm input power, indicating that the IP1dB point is well in excess of +16 dBm. The extrapolated IP1dB is estimated to be +26 dBm based on calculated distortion coefficients at the 0.1 dB compression point. The P1dB sweep measurement is shown in Fig. 4.5.

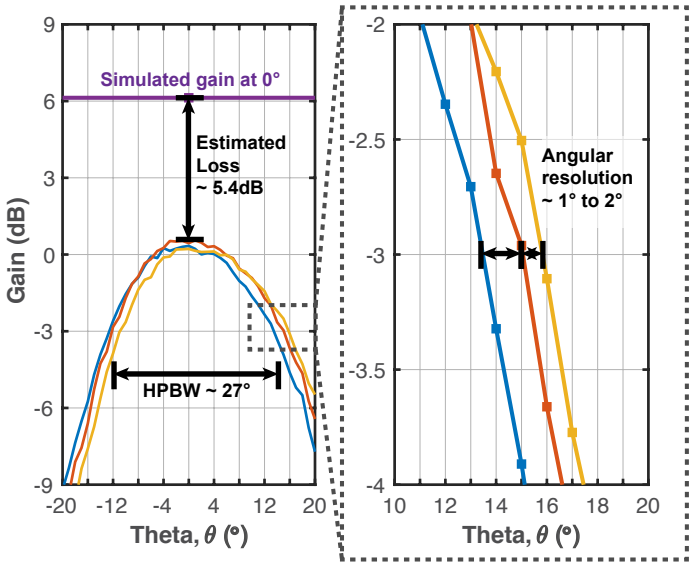


Figure 4.4: Measured beam patterns showing estimated system loss, HPBW, and minimum beam angle resolution for uniform phase shift.

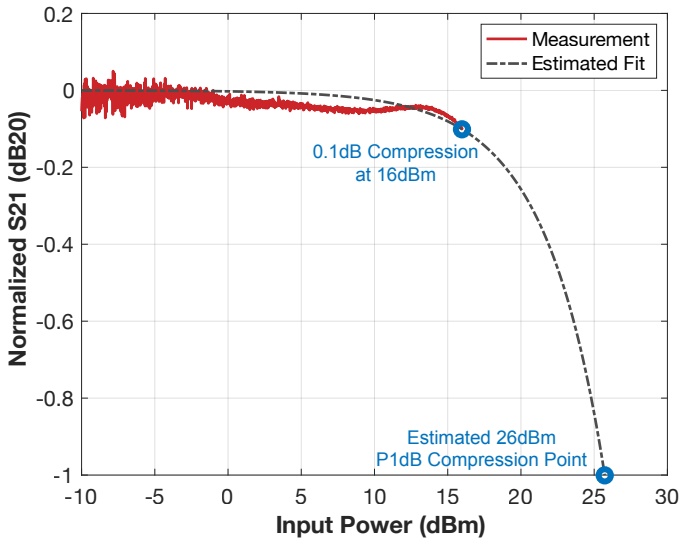


Figure 4.5: Input referred P1dB measurement sweep from -10 dBm to 16 dBm, the upper limit for the PNA.

Chapter 5

Conclusion

5.1 Summary

We have presented the first fully-integrated 4-element passive RF beamformer utilizing balanced impedance phase shifters (BIPS) and transmission-line transformers (TLTs) for the Ku-Band. Previous implementations utilizing these relatively new techniques operated well below 4GHz, did not accommodate more than two elements, and were not fully integrated. By leveraging these techniques, we were able to demonstrate a beamforming RFIC with 5.4dB of passive IL, which is more than 3dB better than relevant state-of-the-art RF beamformers. The IC also achieves 5-bits of phase shifter resolution, very high linearity with extrapolated IP1dB of +26dBm (tested up to +16dBm), and a reasonable 30% fractional bandwidth. Detailed comparison between this work and state-of-the art RF beamformers [17], [29], [33] and phaseshifters [40], [41] operating between X and Ka-Bands with the lowest reported passive IL is presented in Table. 5.1.

The proposed beamformer IL of 5.4dB is also 2.4dB better than what could be achieved using state-of-the-art Si or GaAs phaseshifters, when considering combiner losses, as shown in Fig. 5.1. RF beamformers [16], [17], [27], [29], [30], [33], [34] and phaseshifters [27], [29], [33], [34], [37]–[52] operating between 10 and 30GHz, with full 360° phase control and greater than 3 bits of resolution were included in this figure. The proposed CMOS beamformer IL is competitive with MEMs phaseshifters without the requirements for high control voltages, specialized vacuum sealed packaging, or complex integration strategies. This satisfies the desired goals outlined in Section 1.2.

Crucially, this fully passive 4-element beamformer has sub-6dB of passive loss. Meaning the beamforming gain exceeds its losses so it can be used without pre-amplication. This enables greater system performance (better spatial filtering, larger array gains) without affecting system power, at the expense of array area. Taken together, the low loss, high linearity and fully passive nature of this solution make it an attractive front-end beamformer for power and thermally-constrained applications.

Table 5.1: Comparison to state-of-the-art passive RF beamformers and passive phaseshifters

	This Work	RF Beamformers			RF Phase Shifters	
		[17] ISSCC 2018	[29] RFIC 2017	[33] TMTT 2011	[41] TMTT 2000	[40] ICCC 2017
Operating Frequency	10-14 GHz (X/Ku-Band)	24-32GHz (Ka-Band)	25-33GHz (Ka-Band)	9-10GHz (X-Band)	17-21GHz (K-Band)	8-12GHz (X-Band)
Technology	28nm Bulk CMOS	28nm Bulk BiCMOS	45nm SOI CMOS	0.13um CMOS	0.25um GaAs pHEMT	0.25um GaAs
# of Elements	4	24	2	4		
Integrated (RX/ TX)	No	Yes (24/24)	Yes (2/2)	Yes (4/0)		
Combiner (i.e. Comb) Type	TLT	Wilkinson	Wilkinson	Wilkinson		
Phase Shifter (i.e. PS) Type	Balanced Impedance	Switch Type	Switch Type	Switch Type	Switch Type	Switch Type
Phase Shifter Bits	5-bits	3-bits	5-bits	5-bits	5-bits	6-bits
Passive Phase Shifter IL	NA	7 dB ✢	7 dB ✢	8 dB ✢	6 dB	6.5 dB
Passive Power Combiner IL	NA	1.6 dB ✢	2 dB ✢	2.1 dB ✢	2 dB**	2 dB**
Estimated Passive BF IL	**5.4 dB ◊**	**8.6 dB ✢**	**9 dB ✢**	**10.1dB ✢**	**8 dB****	**8.5 dB****
RX Linearity, IP1dB	**> 16 dBm (Est. 26 dBm)**	**NS**	**5 dBm**	**-12.5 dBm**	**NS**	**29 dBm**
Power Per Channel RX/TX	**0 mW / 0 mW**	**42 mW / 162 mW**	**0 mW / 0 mW**	**36 mW / NA**	**0 mW / 0 mW**	**0 mW / 0 mW**
Max Gain RX/TX	-5.4 dB	34 dB / 44 dB	-10 dB / -10 dB	10.1 dB / NA dB		
Noise Figure	5.4 dB ♦	3.8 dB	-10 dB / -10 dB	3.4 dB		

NA: Not Applicable
NS: Not Stated
◊ : Estimate includes both PS and Comb losses (both)
PS: Phase Shifter
Comb: Power Combiner
✢ : Based on simulated results
♦ : Estimate for NF of passive circuit is equal to its loss
** : Based on stated values or estimated -2 dB value for 4-to-1 Comb

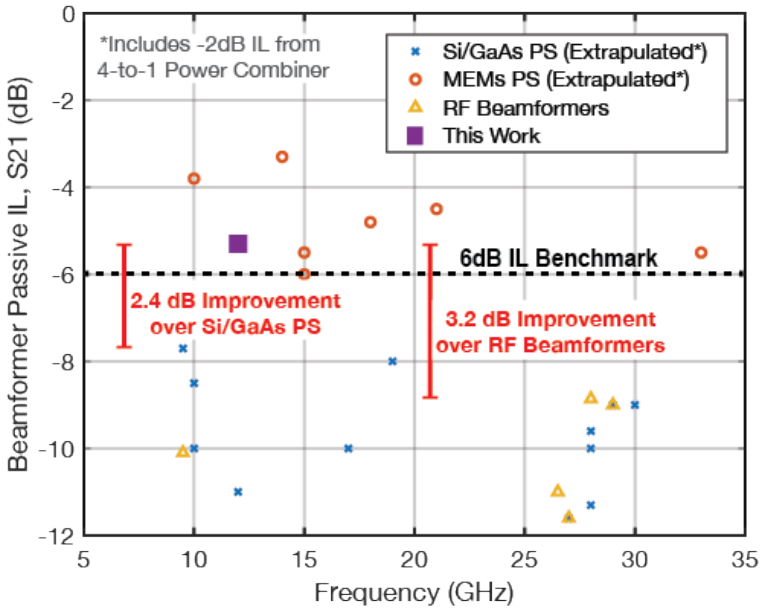


Figure 5.1: Achievable beamformer IL for proposed beamformer compared with state-of-the-art passive RF beamformers and phaseshifters (PS).

5.2 Future Research

Meaningful work can be done to improve the performance of this relatively new RF beamforming technique and demonstrate higher levels of integration. Below are a few suggested directions for future research.

The most important metric for a front end beamformer is its loss. Although the RFIC presented represents a significant improvement over state-of-the-art and crosses the 6dB IL benchmark, there is still room for improvement. Minimizing beamformer IL through the optimization of the TLT feedlines, on-chip matching networks, and BIPS will likely be fruitful avenues for future research.

Additionally, practical phased array systems require several features above and beyond low-loss performance. Improving the proposed beamformer so it can: work with single ended antennas which are more popular, steer a beam in more than one dimension, and scale up to accommodate arrays with much more than four elements, requires further innovation and will go a long way to advancing this technology.

Finally, demonstration of this beamformer technology in a specific application, such as 5G, satellite communication, IoT, or radar are crucial. Such academic demonstrations are necessary to ensure that the proposed beamformer can meet the complex constellation of requirements for modern RF wireless and sensing applications.

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