Dynamical Modeling and Control of the Flying Capacitor Multilevel Converter

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By

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Abstract

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High-performance power conversion is increasingly critical for innovation in almost every modern technology. In anticipation of future applications, the datacenter and electric transportation sectors both continue to demand power converters that are more efficient and compact, but simultaneously capable of supporting far greater power consumption. In recent works, solutions from the family of hybrid-switched-capacitor converters have been shown to meet the efficiency and power-density requirements of next-generation systems. Among these, the Flying Capacitor Multilevel (FCML) converter is promising for electric drives and dc-dc converters alike, as it incorporates smaller filter magnetics, uses high-figure-of-merit low-voltage switches, and is capable of faster dynamic response. The widespread adoption of this converter and related topologies, however, has been limited due to uncertainty about the behavior of the flying capacitor voltages under transient conditions.

This thesis studies the dynamic behavior of the capacitor voltages and presents solutions for regulating the capacitor voltages through "active balancing" control. Standard averaging methods are shown to be inadequate in accurately capturing the capacitor voltage dynamics under certain operating conditions, motivating new converter models developed from higher-order averaging techniques. The refined models obtained are capable of accurately describing the capacitor voltage behavior, and predict small-signal instabilities in standard active balancing control approaches. Subsequently, new modeling techniques and active balancing controllers that do not exhibit small-signal instabilities are developed, and future directions for incorporating these controllers in physical systems are highlighted.

To Amma and Appa

Contents

Contents **ii**

List of Figures **iv**

List of Tables **xiv**

1 Introduction **1**
1.1 Improving Power Converter Performance 1
1.2 The Case for Multilevel Converters 3
1.3 Naturally Balanced FCML Converter Operation 16
1.4 Research Outline 20

2 Active Balancing Based on the Standard Averaged Model **22**
2.1 A Review of Standard Averaged Modeling of Power Converters 23
2.2 Averaged Plant Model for the FCML Converter 26
2.3 Parallel Controller Structure 32
2.4 Experimental Verification of Active Balancing Controller 41
2.5 Characterization of Small-Signal Instability 51
2.6 Survey of Active Balancing Literature Based on Averaged Models 54

3 Generalized Averaged Modeling **60**
3.1 A Review of Generalized Averaged Modeling of Power Converters 61
3.2 Application of Generalized Averaging to the FCML Converter 63
3.3 Model Reduction and Analysis of Minimum Harmonics Required 70
3.4 Analysis of Closed-Loop Active Balancing Dynamics 84
3.5 Experimental Results 86
3.6 Summary of Generalized Averaged Modeling of FCML Converters 94

4 Charge Models for Averaging Effects of Ripple **97**
4.1 Introduction to Charge Modeling for the FCML Converter 97
4.2 Simulation Verification of Plant Model 110
4.3 Design of a State-Feedback Balancing Controller 113
4.4 Experimental Verification of Active Balancing Controller 115

4.5 Justification of the Averaging Method Via Perturbation Theory 122

5 Conclusions and Directions for Future Study **128**
5.1 Summary of Contributions and Conclusions 128
5.2 Future Studies of Generalized Averaged Modeling 129
5.3 Future Studies of Charge Models for Capacitor Dynamics 130

Bibliography **134**

A Application of Singular Perturbation Theory for Model Order Reduction **147**

B Linearization of Generalized Averaged Model **150**

C Incorporating Integrators, Filters, and Delays in the State-Space Model **153**

List of Figures

1.1 Two multilevels converters ((a) Flying Capacitor Multilevel (FCML) Converter; (b) Cascaded H-Bridge (CHB) Converter) exhibiting the properties studied in this introductory section. 3
1.2 Carriers w_k and switching signals s_k ($k \in \{1, 2, \ldots, N-1\}$) corresponding to symmetric Phase-Shifted Pulse Width Modulation (PS-PWM). 4
1.3 Steady-state switching node voltage v_{sw} and inductor current waveform i_L for (a) standard two-level buck converter; (b) N-level multilevel converter. 6
1.4 Parameter α given by (1.8) plotted as a function of conversion ratio M for different level counts $N = 2, \ldots, 6$. 7
1.5 Normalized current ripple given by (1.9) plotted as a function of conversion ratio M for different level counts $N = 3, \ldots, 6$. 7
1.6 (a) Canonical vertical power semiconductor model used in [34, 35] to derive the voltage scaling characteristic of (1.14); (b) Equivalent circuit model of power semiconductor device, modeling parasitic per-unit-area on-state resistance $\hat{R}_{\text{on}}$ and per-unit-area drain-to-source capacitance $\hat{C}_{\text{ds}}$. 9
1.7 Normalized volt-seconds $\hat{\Lambda}$ given by (1.11) and normalized semiconductor loss $\hat{P}$ given by (1.17) plotted as a function of the normalized switching frequency $\hat{f}_{\text{s}}$ defined in (1.18). An N-level converter performs better than a two-level converter in the range $\frac{1}{(N-1)^2} < \hat{f}_{\text{s}} < 1$. 10
1.8 Illustration of the inductor current i_L, output capacitor current $i_{C_{\text{o}}}$ and output voltage v_{o} during a transient in the inductor current reference i_{ref}. This scenario corresponds to the minimum output voltage deviation Δv_{o} during the load step-up transient. 12
1.9 Digital PWM sampling and update modes for a two-level converter implementing average current control, considering a one-step computation delay: (a) single-sampling single-update at carrier valley; (b) double-sampling double-update at carrier peaks and valleys. 14
1.10 Digital PWM sampling and update modes for an N-level converter implementing average current control, considering a one-step computation delay: (a) single-sampling single-update at carrier w_1 valley; (b) multi-sampling, multi-update at peaks, valleys, and intersections of all carriers [52]. For multilevel converters, double-update schemes are also possible, but are not shown in this figure for clarity. 14

1.11 Switching signals under PS-PWM for a 4-level FCML converter, highlighting the circuit states in two switching phases. In each switching phase, a maximum of two flying capacitors are connected in series with the inductor. 16
1.12 Measured voltage response in a 5-level FCML converter for a step in the input voltage v_{in} from 7 V to 30 V. The converter is configured with $C = 8.8\,\mu\text{F}$, $L = 10\,\mu\text{H}$, $f_{\text{s}} = 75\,\text{kHz}$, and $R = 8\,\Omega$. Over a timescale of approximately 30 ms, the capacitor voltages balance to their respective nominal fractions of the input voltage. 18
1.13 (a) Measured waveforms of Fig. 1.12, showing the underdamped capacitor voltage behavior in a timescale of 4 ms after the input voltage step; (b) Off-state switch drain-source voltages v_{ds}, highlighting the excessive voltage observed across switch pair s_4. 19

2.1 (a) General representation of feedback control and the pulse width modulator in a two-level converter; (b) Frequency domain representation of the open-loop small-signal system response to the pulse width modulated switching signal with modulation frequency $f_{\text{m}} << f_{\text{s}}$. Assuming the plant has a low-pass characteristic, the dominant components of the plant output $v(t)$ occur at dc and the modulation frequency f_{m}. 23
2.2 Magnitude response of averaging operator (2.4). Assuming the modulation frequency is significantly lower than the switching frequency ($f_{\text{m}} << f_{\text{s}}$) the averaging operator captures the baseband content shown in Fig. 2.1. 24
2.3 Schematic drawing of an N-level FCML converter with $n_c = N-1$ complementary switch pairs and $M = N - 2$ flying capacitors. 26
2.4 Block diagram of the small-signal averaged plant given in (2.21), highlighting the parallel inductor and capacitor sub-plants. 29
2.5 Parallel control structure and an equivalent model of the controller. The flying capacitor plant naturally rejects the common duty ratio term d_{curr} applied to all switches, as shown in the equivalent model. 33
2.6 Block diagram representation of the balancing controller given in (2.42). 35
2.7 Example imbalanced capacitor voltages, shown in a timescale of one switching period. The reference capacitor voltages are respective nominal fractions of the input voltage, $\frac{k}{n_c}V_{\text{in}}$, shown as red lines. The signed errors associated with imbalanced voltages are indicated by arrows. 36
2.8 Example duty ratios applied to each switch resulting from simultaneous current control and active balancing actions. The balancing actions appear as difference duty ratios Δd_k, applied recursively to each switch beginning with $d_1 = d_{\text{curr}}$. The pulse width corresponding to the common-mode duty ratio d_{curr} is shown via dashed lines. 36

2.9 Equivalent closed-loop system after feedback linearization of the current dynamics. To ensure the balancing disturbance is rejected in practice, the current controller bandwidth should be chosen to be significantly higher than the balancing control bandwidth. 38
2.10 12-Level FCML converter prototype with $L = 10\,\mu$H, $C_k = 8.8\,\mu$F, $f_s = 100\,$kHz. The parallel controller is implemented on a Texas Instruments TMS320F28379D DSP. The hardware is reconfigured as a 6-level FCML converter by shorting input-side switch pairs. 40
2.11 (a) Measured capacitor voltage and inductor current response of a current-controlled converter relying on natural balancing when supply voltage is changed from 50 V to 90 V. The capacitor voltages exhibit underdamped dynamics, resulting in unequal switch voltage stress. (b) Measured response of a converter implementing the proposed parallel active balancing controller. The capacitor voltages track the reference values with negligible error compared to the natural balancing case. In both cases, the current control bandwidth is set to 10 kHz, and the current reference $i_{L,\text{ref}} = 3\,$A. The active balancing control bandwidth is set to 600 Hz for each flying capacitor. 42
2.12 (a) Measured response of a current-controlled converter relying on natural balancing when a 50 Hz, $10\,V_{\text{RMS}}$ ac perturbation is applied to the supply voltage. The capacitor voltages do not track their respective reference values as the natural balancing dynamics are not sufficiently fast. (b) Measured response of a converter implementing the proposed parallel active balancing controller. The capacitor voltage tracking is significantly improved and the disturbance to the inductor current is reduced. In both cases, the current control bandwidth is set to 10 kHz, and the current reference $i_{L,\text{ref}} = 2\,$A. The active balancing control bandwidth is set to 300 Hz for each flying capacitor. 44
2.13 Maximum normalized device voltage stress V_{ds} given by (2.53), plotted against the supply perturbation frequency for a current-controlled converter relying on natural versus active balancing. A $10\,V_{\text{RMS}}$ perturbation is applied on top of a nominal 50 V dc supply voltage. The current control bandwidth is set to 5 kHz and two different active balancing control bandwidths are studied, 300 Hz and 500 Hz. The device voltage stress is consistently lower under active balancing. . 46
2.14 Measured current distortion given by (2.54), plotted against the supply perturbation for a current-controlled converter relying on natural versus active balancing. A $10\,V_{\text{RMS}}$ perturbation is applied on top of a nominal 50 V dc supply voltage. The current control bandwidth is set to 5 kHz. Under active balancing, the current distortion is consistently lower, indicating better decoupling of the capacitor voltages and inductor current with active balancing. 47

2.15 Measured capacitor voltage and current response during a step change in the current reference i_{ref} from 7 A to 10 A at $v_{\text{in}} = 250$ V. The current control bandwidth is set to 10 kHz. The flying capacitor voltages are undisturbed during the load current transient, verifying that the capacitor voltages naturally reject the common-mode duty ratio used to control current. 49
2.16 (a) Measured capacitor voltage response in the current-controlled converter relying on natural balancing during a large step change in the current reference from i_{ref} from 2 A to 15 A. (b) Measured capacitor voltage response in the current-controlled converter implementing the proposed active balancing controller. In both cases, the load transient is tested with $v_{\text{in}} = 40$ V and $L = 4.7\,\mu$H. 50
2.17 (a) Measured closed-loop stability boundary with 10 μH filter inductance, 100 kHz switching frequency, 5 kHz designed current control bandwidth, and 80 V dc supply voltage. The maximum designed balancing bandwidth resulting in a stable system is plotted in blue as a function of the load current. Two points shown in green and red indicate examples of stable and unstable designs respectively. (b) Time domain responses corresponding to the stable and unstable designs indicated in Fig. 2.17a. 52
2.18 (a) Measured closed-loop stability boundary with 3.3 μH filter inductance, 100 kHz switching frequency, 5 kHz designed current control bandwidth, and 80 V dc supply voltage. The maximum designed balancing bandwidth resulting in a stable system is plotted in blue as a function of the load current. Two points shown in green and red indicate examples of stable and unstable designs respectively. (b) Time domain responses corresponding to the stable and unstable designs indicated in Fig. 2.18a. 53
2.19 Representation of averaged dynamics used as the plant model in this chapter and faster unmodeled dynamics. The unmodeled ripple contribution is insignificant at moderate to heavy loads, but becomes more relevant at light loads, contributing to closed-loop instability depending on the choice of active balancing controller gains. 54
2.20 Structure of the active balancing controller proposed in [108, 111–113]. As shown in (2.56), this balancing controller results in coupled capacitor voltage dynamics and forces low-bandwidth operation in practice. 55
2.21 (a) Block diagram representation of the small-signal system in (2.21) in cascade form. (b) System resulting from the state feedback decoupling control law derived following the principles of [114]. This control law is identical to that presented in Section 2.3, but does not explicitly show the parallel control structure. 57

3.1 Block diagram representation of averaged plant model, showing the unmodeled impacts of the inductor current ripple. 60
3.2 Schematic drawing of an N-level FCML converter, explicitly modeling a parasitic resistance R_{s}. 63

3.3 Block diagram of the full generalized averaged model given in (3.26). Contributions of the generalized averaged model compared to the standard averaged model are highlighted and appear as feedback dynamics. 67
3.4 Simulated and modeled capacitor voltage responses for a 6-level FCML converter operating at $D = 0.35$, varying the total numbers of harmonics modeled n. The model with $n = 2$ accurately captures the step-transient response. In the circuit simulation and model, $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R = 3.5\,\Omega$, $R_s = 0.3\,\Omega$, and $f_s = 100\,\text{kHz}$. The line voltage is stepped from 100 V to 125 V. 68
3.5 Simulated and modeled capacitor voltage responses for a 6-level FCML converter operating at $D = 0.50$. At this conversion ratio, $n = 3$ is required to predict the correct steady-state behavior. A small error of 5.8 Hz is observed between the predicted and observed dominant oscillation frequency. In the circuit simulation and model, $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R = 5\,\Omega$, $R_s = 0.3\,\Omega$, and $f_s = 100\,\text{kHz}$. The line voltage is stepped from 100 V to 125 V. 69
3.6 Block diagram representation of reduced-order model, showing the decoupled capacitor voltage and output filter dynamics. 72
3.7 Eigenvalues characterizing the natural balancing dynamics of a 4-level FCML converter operating at $D = 0.5$ as predicted by the full generalized averaged model (3.26) and the reduced-order model of (3.48). The reduced-order model accurately captures the dominant eigenvalues which participate entirely in the capacitor voltage dynamics. In the full and reduced-order model, $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R = 8\,\Omega$, $R_s = 0.3\,\Omega$, $V_{\text{in}} = 80\,\text{V}$, and $f_s = 100\,\text{kHz}$. 74
3.8 Plots of $A_{c,klm}$ as given by (3.51) normalized to $-\frac{\omega_0}{m\Omega_s}$ for a 4-level converter. The curves depict the contribution of different inductor current harmonics to the capacitor dynamics. For a small range of duty ratios centered at $D = 0.5$, the contributions of the second and third harmonics are negligible. 75
3.9 Block-diagram representation of the capacitor voltage dynamics after model-order reduction. The feedback elements model the coupling between capacitors due to each inductor current harmonic as given by (3.53). 76
3.10 Flowchart depicting the procedure proposed in this section to determine the minimum number of inductor current harmonics required to capture the capacitor voltage dynamics. 78
3.11 A Selective Modal Analysis (SMA) [123, 124, 126, 127] perspective on the n-term approximation of the generalized averaged model. The contribution of harmonics of order $n+1, n+2, \ldots, \infty$ to the p dominant modes studied are assumed to be zero. 79
3.12 Minimum number of inductor current harmonics required to model capacitor voltage dynamics in a 4-level converter, determined from the procedure outlined in Section 3.3. For the 4-level converter, the results obtained from the procedure confirms the qualitative conclusions obtained by visual examination of Fig. 3.8. The converter parameters used in this example are $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R_s = 0.3\,\Omega$, $V_{\text{in}} = 80\,\text{V}$, $I_{\text{out}} = 5\,\text{A}$, $R = V_{\text{in}}D/I_{\text{out}}$, and $f_s = 100\,\text{kHz}$. 80

3.13 Simulated and modeled capacitor voltage responses for a 4-level FCML converter operating at $D = 0.25$, varying the total numbers of harmonics modeled n. The model with $n = 2$ accurately captures the step-transient response. In the circuit simulation and model, $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R = 2.5\,\Omega$, $R_s = 0.3\,\Omega$, and $f_s = 100\,\text{kHz}$. The line voltage is stepped from 100 V to 125 V. 81
3.14 Simulated and modeled capacitor voltage responses for a 4-level FCML converter operating at $D = 0.50$, varying the total numbers of harmonics modeled n. The model with $n = 1$ accurately captures the step-transient response. In the circuit simulation and model, $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R = 5\,\Omega$, $R_s = 0.3\,\Omega$, and $f_s = 100\,\text{kHz}$. The line voltage is stepped from 100 V to 125 V. 82
3.15 Minimum number of inductor current harmonics required to model capacitor voltage dynamics in a 6-level converter, determined from the procedure outlined in Section 3.3. The converter parameters used in this example are $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R_s = 0.3\,\Omega$, $V_{\text{in}} = 80\,\text{V}$, $I_{\text{out}} = 5\,\text{A}$, $R = V_{\text{in}}D/I_{\text{out}}$, and $f_s = 100\,\text{kHz}$. 83
3.16 Parallel active balancing control structure detailed in Chapter 2. 84
3.17 Block diagram representation of the closed-loop small-signal system. The additional plant dynamics captured in the generalized averaged model are highlighted and can destabilize active-balanced systems designed around the standard averaged model in light-load conditions. 85
3.18 Simulated capacitor voltages for a 6-level FCML converter implementing the parallel active balancing controller of [96] at two different average load current conditions. The closed-loop system is destabilized at light-loads by the contribution of the current ripple. In this experiment, $v_{\text{in}} = 250\,\text{V}$, $D = 0.25$, $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R_s = 0.3\,\Omega$, and $f_s = 100\,\text{kHz}$. 86
3.19 Eigenloci of the closed-loop small-signal model derived from generalized averaging as the average load current is varied. The model predicts the same instability observed in the simulation result of Fig. 3.18, with a relative error of 8% in the predicted oscillation frequency. The model is evaluated with $v_{\text{in}} = 250\,\text{V}$, $D = 0.25$, $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R_s = 0.3\,\Omega$, and $f_s = 100\,\text{kHz}$. 87
3.20 Measured response of capacitor voltages in a 4-level FCML converter operating at $D = 0.5$ to a step in the input voltage from 7 V to 30 V. The measured responses are curve-fit to the general form of an exponential response to determine the time constant τ_{d} and oscillation frequency f_{d} of the dominant mode. The converter tested has $L = 4.7\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $f_s = 100\,\text{kHz}$. 88
3.21 Comparison of measured and modeled time constant τ_{d} and oscillation frequency f_{d} of the dominant mode characterizing a 4-level FCML converter. The parameters of the dominant mode are extracted from step-response measurements such as those shown in Fig. 3.20, and match the generalized averaged model with $n = 2$. The converter tested has $L = 4.7\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R = 8.5\,\Omega$, $f_s = 100\,\text{kHz}$. The generalized averaged model uses $R_s = 0.3\,\Omega$ considering experimental inductor characterizations in [77]. 89

3.22 Comparison of measured and modeled time constant τ_{d} and oscillation frequency f_{d} of the dominant modes characterizing a 5-level FCML converter. The generalized averaged model predicts f_{d} well, but conservatively estimates that the converter will not balance at the "nominal" conversion ratio of $D = 0.5$ as $\tau_{\mathrm{d}} \to \infty$. Unmodeled parasitic elements present in the hardware such as switch drain-source capacitances re-introduce a finite balancing time constant at this conversion ratio [80]. The converter tested has $L = 4.7\,\mu\mathrm{H}$, $C = 8.8\,\mu\mathrm{F}$, $R = 8.5\,\Omega$, $f_s = 100\,\mathrm{kHz}$. The generalized averaged model uses $R_s = 0.3\,\Omega$ considering experimental inductor characterizations in [77]. 90

3.23 Measured capacitor voltage responses in a 6-level FCML converter implementing the active balancing controller of [96] for two different designed balancing loop bandwidths ω_{bal}. The balancing control is enabled at time $t = 0$. For the design with $\omega_{\mathrm{bal}} = 2\pi \cdot 3255\,\mathrm{rad/s}$, the capacitor voltages exhibit small-signal instability. The converter is designed with $L = 10\,\mu\mathrm{H}$, $C = 8.8\,\mu\mathrm{F}$, $R = 6.9\,\Omega$, and $f_s = 100\,\mathrm{kHz}$, and operated with $v_{\mathrm{in}} = 80\,\mathrm{V}$ and $D = 0.25$. 91

3.24 Eigenloci of the closed-loop small-signal generalized averaged model for a 6-level converter as the designed balancing loop bandwidth ω_{bal} is varied. The model is derived with $n = 5$ for the same design and operating conditions as the experimental measurement of Fig. 3.23, and verifies that $\omega_{\mathrm{bal}} = 2\pi \cdot 3255\,\mathrm{rad/s}$ corresponds to an unstable design. 92

3.25 Measured and modeled stability boundaries as a function of the average load current for a 6-level FCML converter designed with $L = 10\,\mu\mathrm{H}$, $C = 8.8\,\mu\mathrm{F}$, and $f_s = 100\,\mathrm{kHz}$, and operated with $v_{\mathrm{in}} = 80\,\mathrm{V}$ and $D = 0.25$. The stability boundary indicates the maximum balancing designed balancing control bandwidth ω_{bal} that yields a stable closed-loop response. The generalized averaged model accurately predicts instabilities arising from the impact of the current ripple on the capacitor voltage dynamics. 93

3.26 Rank of the controllability matrix $\mathcal{C}$ associated with the small-signal system of (3.58) as a function of the quiescent duty ratio D for a 3-level, 4-level, 5-level, and 6-level converter. 95

4.1 Switching signals s_k and switching node voltage v_{sw} for a 4-level FCML converter resulting from phase-shifted pulse-width modulation (PS-PWM) with duty ratio D for (a) Mode 1, $0 < D < 1/3$, (b) Mode 2, $1/3 < D < 2/3$, (c) Mode 3, $2/3 < D < 1$. In all three operating modes, the average value of the switching node voltage and the output voltage are equal to $D\,v_{\mathrm{in}}$. 98

4.2 Switching signals s_k, switching node voltage v_{sw}, and inductor current i_L for a 4-level FCML converter operating in mode 2. The switching phases occurring in each sub-period and the value of the inductor current at the end of each switching phase are annotated with roman numerals. 99

4.3 Simulated capacitor voltage responses to a step in the supply voltage from 48 V to 54 V for a 4-level FCML converter operating in mode 2. Results are shown for a controller regulating the average output voltage to 24 V and not implementing any active balancing feature. The underdamped capacitor voltage dynamics induce excessive blocking voltage stresses on the converter's switches. The converter is simulated with $L = 10\,\mu$H, $C = 8.8\,\mu$F, $f_s = 100\,$kHz. 101
4.4 Converter waveforms illustrating the small-signal capacitor current response in operating mode 2 to a perturbation in the switching node voltage pulse position in sub-period 2. The differences in the quantity of charge flowing into each flying capacitor as a result of the perturbation are shown as shaded areas, and impact the capacitor voltages via the relations given in (4.8). The small-signal impact of all perturbations is summarized in (4.19). 103
4.5 Normalized characteristic oscillation frequency $\hat{\omega}_{\text{osc}}$ defined in (4.32) as a function of the conversion ratio M. 105
4.6 Converter waveforms illustrating the small-signal capacitor current response in operating mode 1 to a perturbation in the switching node voltage pulse position in sub-period 2. The small-signal impact of all perturbations is summarized in (4.23). 106
4.7 Converter waveforms illustrating the small-signal capacitor current response in operating mode 3 to a perturbation in the switching node voltage pulse position in sub-period 2. The small-signal impact of all perturbations is summarized in (4.26). 107
4.8 Carriers, modulating waveforms, and key converter waveforms for a 4-level FCML converter operating in mode 1 with a perturbation applied in sub-period 2. In the proposed implementation, two modulating waveforms $m_{k,a}$ and $m_{k,b}$ are associated with each triangular carrier w_k, and are used for up-count and down-count comparisons respectively. 108
4.9 Simulated capacitor voltage responses for a 4-level FCML converter when applying a 1 kHz perturbation in control input ΔT_1. The converter is operated with $v_{\text{in}} = 48\,$V, $f_s = 100\,$kHz, $L = 10\,\mu$H, and $C = 8.8\,\mu$F. The capacitor voltage responses are post-processed via Fast Fourier Transforms (FFTs) to determine the magnitude and phase response at the perturbation frequency. 110
4.10 Comparison of simulated frequency response of capacitor voltage $v_{c,1}$ to perturbations in ΔT_1 to the theoretical response $\boldsymbol{H}_{\boldsymbol{k},11}$ obtained from (4.34). The simulation results agree with the theoretical frequency response in all operating modes up to a tested bandwidth of 5 kHz. 112
4.11 Comparison of simulated frequency response of capacitor voltage $v_{c,2}$ to perturbations in ΔT_1 to the theoretical response $\boldsymbol{H}_{\boldsymbol{k},21}$ obtained from (4.34). The simulation results agree with the theoretical frequency response in all operating modes up to a tested bandwidth of 5 kHz. 112

4.12 Block-diagram representation of the small-signal active balancing control loop. The controller $\boldsymbol{K}$ is designed in this work to damp the natural capacitor voltage oscillations. 113
4.13 Block diagram representation of a single-sampled digital control architecture where the state-feedback balancing controller is implemented in parallel with a dual-loop output voltage controller. 115
4.14 Oscilloscope waveform capture showing an example perturbation in ΔT_1 and measured capacitor voltages for the 4-level FCML converter prototype operating in mode 2. The data is post-processed using FFTs in MATLAB to determine the plant magnitude and phase response. 116
4.15 Comparison of measured frequency response of capacitor voltage $v_{c,1}$ to perturbations in ΔT_1 to the theoretical response $\boldsymbol{H}_{\boldsymbol{k},11}$ obtained from (4.34). The experimental measurements confirm the theoretical plant behavior in all operating modes, and exhibit nonzero damping arising from unmodeled parasitic elements in the converter. 117
4.16 Comparison of measured frequency response of capacitor voltage $v_{c,2}$ to perturbations in ΔT_1 to the theoretical response $\boldsymbol{H}_{\boldsymbol{k},21}$ obtained from (4.34). The experimental measurements confirm the theoretical plant behavior, and exhibit nonzero damping arising from unmodeled parasitic elements in the converter. . . 117
4.17 Comparison of measured frequency response in operating mode 2 of capacitor voltage $v_{c,1}$ to perturbations in $v_{c,1_{\text{ref}}}$ to the theoretical response $\boldsymbol{H}_{\boldsymbol{CL},11}$ obtained from (4.47). 119
4.18 Measured responses of the capacitor voltages and inductor current in the 4-level FCML converter to a step in the supply voltage from 45 V to 50 V when (a) the output voltage controller is active but the balancing controller is not enabled, and (b) both the output voltage and active balancing controllers are enabled. The converter operates with an average load current of 5 A and an output voltage set-point of 24 V. The proposed active balancing controller damps the natural capacitor voltage oscillations, enabling improved capacitor voltage tracking during the line transient. 120
4.19 Measured responses of the capacitor voltages and inductor current in the 4-level FCML converter to a step in the supply voltage from 45 V to 50 V when (a) the output voltage controller is active but the balancing controller is not enabled, and (b) both the output voltage and active balancing controllers are enabled. In this experiment, the converter operates at a light-load condition corresponding to 0.25 A average load current. The proposed active balancing controller damps the natural capacitor voltage oscillations, and does not exhibit the small-signal instability inherent to controller derived from averaged models such as [96, 107, 108]. 121

5.1 Converter waveforms illustrating the small-signal capacitor current response when $M = 1/3$ to a perturbation in the switching signal edges occurring in sub-period 2.131

A.1 Block diagram representation of the feedback dynamics corresponding to the m^{th} harmonic coefficient of the inductor current. 148
A.2 Block diagram depiction of equivalent system when the feedback dynamic blocks in the full generalized averaged model represented in Fig. 3.3 are substituted with their dc gains. This structure is identical to the parallel feedback form shown in Fig. 3.9. 149

List of Tables

2.1 Component Details 40

4.1 Modulating Waveform Generation 109

Acknowledgments

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Chapter 1

Introduction

Power electronic systems play an increasingly critical role in modern technology. As a result, advancements in the performance of power electronics directly enable innovations in almost every technology sector. In consumer electronics, improvements in power conversion have enabled efficient power delivery in increasingly small form factors and at low costs. Developments in this space that have received widespread attention in industry include integrated dc-dc converters [1–7] and methods for wireless power transfer [8, 9]. In data centers, rapid increases in processor power consumption have motivated recent investigation of power distribution and converter architectures that can deliver greater currents with improved dynamic performance [10–17]. In the broader industry of grid-scale systems, efficient and cost-effective power semiconductor devices and advances in digital control have enabled the adoption of high voltage dc (HVDC) transmission architectures [18–20] and increased integration of renewable energy systems [21, 22].

1.1 Improving Power Converter Performance

Engineers assess power converter performance via different criteria depending on the end-application requirements. Common metrics such as power conversion efficiency and volumetric power density are practical for quantitatively comparing the nominal steady-state performance of converters or systems. Other metrics such as settling time, overshoot, and bandwidth can be used for comparing the dynamic characteristics of converters and their accompanying controllers under application-defined transient conditions.

Innovations in power conversion technology to improve performance along one or more of these metrics occurs at different levels of the design. Component-level innovation, driven by advancements in materials and packaging, enables power electronics designers to select from higher performance switches, inductors, capacitors, and transformers comprising switching power converters. At this scale, research and development often seeks the reduction of parasitic resistances, inductances, and capacitances which contribute to losses in the converter and limit the speeds at which converters can be switched. Advancements in integrated cir-

cuits used in power converters such as gate drivers, isolation devices, and microprocessors facilitate smaller converter footprints, more efficient designs, and advanced control techniques. Despite improvements in components, the performance of a given power converter can be fundamentally limited by the circuit configurations that it can form during operation. For example, the inductor voltages and capacitor currents that appear in each switching state determine the volume of the passive components in the converter. These currents and voltages can also limit the maximum rate at which the converter can respond to line and load transients. In response to limitations at the topology level, engineers seek alternative power conversion circuits that meet the application demands while offering improved performance compared to conventional solutions. Innovations in circuit topology typically comprise reductions in the volume of passive components, reductions in cost through the use of fewer components or more widely available products, improvements in efficiency through the use of higher-performance devices, or improvements in transient performance. For widely used and newly introduced topologies alike, innovation can also occur in the domain of converter control. The scope of control in power electronics is broad—it may be at a low level, for example to position switching signals to achieve efficient soft-switching operation, or at a higher level to achieve application-specific functions such as power factor correction in grid-connected converters or dynamic voltage scaling in CPUs and GPUs. In certain applications, engineers explore innovations at a higher architecture level. For example, the number of power conversion stages in the system and the operating voltages and currents of these stages may be re-evaluated to address bottlenecks limiting efficiency, miniaturization, or lifetime.

The categories of innovation that have just been described are typically not considered in isolation. Power converter designers often target improved performance all of these areas. In many cases, innovations at one level enable cascaded improvements at higher levels of the design. As an example, the commercialization of wide-bandgap semiconductor devices has enabled practical demonstrations of power converters in medium-voltage applications replacing conventional transformer solutions. At the same time, demonstrations of new converter topologies and system architectures are enabled by advancements in the capabilities of commercially available microcontrollers and custom digital controllers.

This dissertation focuses on the interaction between control and circuit topology. The following chapters develop methods of digital control to enable high-performance demonstrations of one particularly promising topology: the Flying Capacitor Multilevel (FCML) converter. This introductory chapter first presents fundamental scaling laws and commercial trends motivating the broader class of multilevel converters. After highlighting the advantages of the FCML converter and the operating principles characterizing state-of-the-art demonstrations, the penultimate section of this chapter introduces the key challenges limiting widespread adoption of the topology and motivates the topics of research presented in the subsequent chapters.

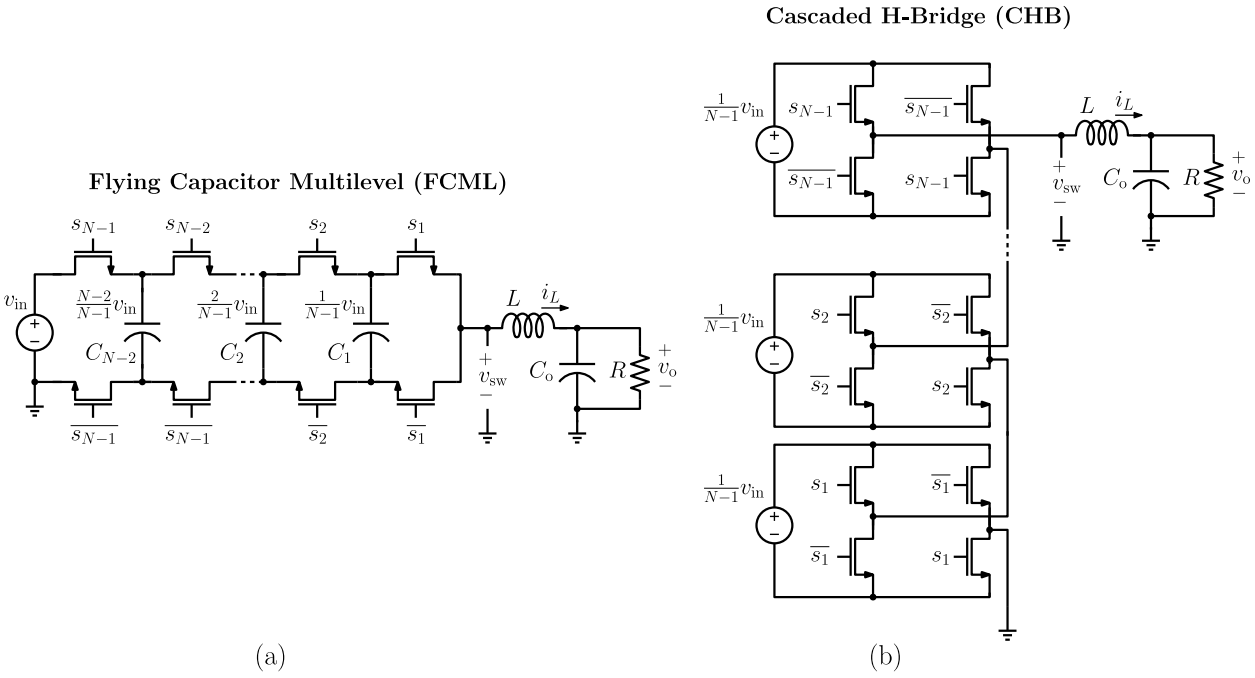


Figure 1.1: Two multilevels converters ((a) Flying Capacitor Multilevel (FCML) Converter; (b) Cascaded H-Bridge (CHB) Converter) exhibiting the properties studied in this introductory section.

1.2 The Case for Multilevel Converters

The investigation of "multilevel" switching converters spanning the past four decades has broadly been motivated by two fundamental goals: a reduction in the filtering burden of magnetic elements connected to the switching node of the converter, and a reduction in the blocking voltage burden of power semiconductor devices comprising the switching network. These two goals, combined with the proliferation of applications demanding high-performance power conversion, have inspired research and development of numerous multilevel topologies [23–32]. This introductory section considers the subset of topologies featuring the following favorable properties:

- Equal blocking voltages across all power semiconductor devices, to allow for the use of common parts, simplifying device cost, layout, and thermal design
- Equal switching activity for all power semiconductor devices, to simplify the control signals provided to the converter and facilitate selection of power devices
- Evenly separated switching node voltage levels between 0 V and v_{in}, to reduce the instantaneous voltage applied to filter magnetics while simplifying analysis of switching ripple

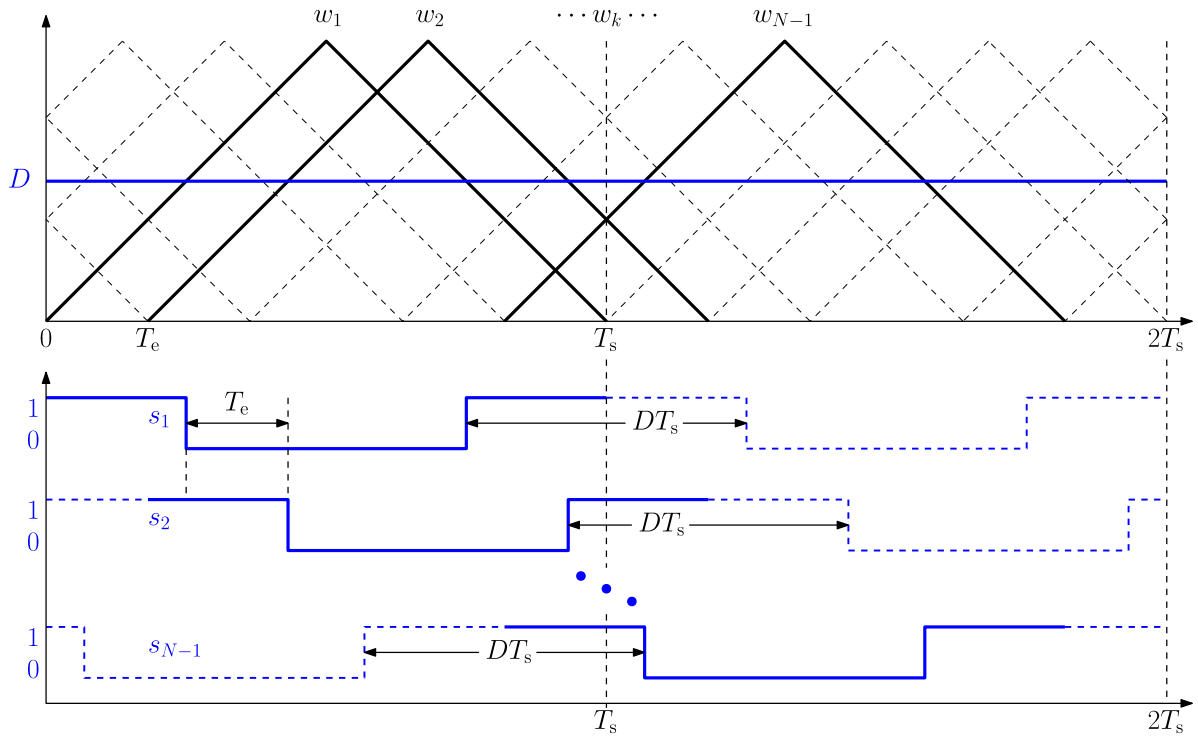


Figure 1.2: Carriers w_k and switching signals s_k ($k \in \{1, 2, \ldots, N-1\}$) corresponding to symmetric Phase-Shifted Pulse Width Modulation (PS-PWM).

- A higher effective frequency of the switching node voltage waveform compared to the switching frequency, to enable further reduction in magnetics size via reduction of the applied volt-seconds

In practice, multilevel converters do not need to satisfy all of these requirements. The superset of multilevel converters satisfying only some of these properties contains converters exhibiting various tradeoffs in switching device count, passive component volume, losses, and layout challenges. A comprehensive review of all topologies is outside the scope of this work due to the large variation in application requirements and motivations behind each topology. Furthermore, fair comparison of the broader class of multilevel converters is difficult as the advantages and disadvantages of a given topology may only be apparent under certain operating conditions. Nevertheless, the aforementioned constraints assist in motivating the topology studied in this work by providing a foundation for discussing the scaling laws enabling several performance improvements.

Fig. 1.1 shows two converters that exhibit all of the required characteristics: the Flying Capacitor Multilevel (FCML) [25] and Cascaded H-Bridge (CHB) [27] converters. For switching frequency $f_s = 1/T_s$, both converters are able to generate a switching node voltage waveform with a fundamental frequency $f_e = 1/T_e = (N-1)\, f_s$ when operated

with Phase-Shifted Pulse Width Modulation (PS-PWM) [33]. Carrier waveforms w_k , $k \in \{1, 2, \ldots, N-1\}$ and switching signals s_k resulting from a constant modulating waveform with value D for an N-level converter are shown in Fig. 1.2. The generated switching signals are circularly separated in phase by $2\pi/(N-1)$ radians through a set of $N-1$ equally phase shifted carriers. In nominal operation, the modulating waveforms compared against each phase-shifted carrier are identical, yielding circularly symmetric switching signals.

The analysis that follows assumes dc modulation for a dc-dc conversion application, however the scaling laws presented are equally applicable to the case of dc-ac converters with appropriate modifications to the definitions of modulating waveforms and the location of the circuit ground node. Multilevel converters featuring the properties highlighted above are shown to: increase system power density by reducing the volume of the filter inductor, increase converter efficiency through the use of high-figure-of-merit low-voltage switches, and enable faster dynamic response through a higher slew rate of the inductor current and higher effective frequency of the inductor current ripple.

Filter Inductor Size

The generated switching node voltage and inductor current waveforms for the multilevel converters under dc modulation are compared in Fig. 1.3 to the equivalent waveforms in a standard step-down ("buck") converter. Assuming a constant supply voltage v_{in} and load voltage $v_{\text{o}} = M v_{\text{in}}$, where $M \in [0, 1]$ is the conversion ratio, the steady-state behavior of the standard buck converter is illustrated in Fig. 1.3a. The fundamental frequency $f_{\text{e}} = 1/T_{\text{e}}$ of the switching node voltage waveform is equal to the switching frequency $f_{\text{s}} = 1/T_{\text{s}}$ at which the devices in the converter are operated. Similarly, the effective duty ratio D_{e} of the switching node voltage waveform, defined as the proportion of the total switching period for which $v_{\text{sw}} = v_{\text{in}}$, is equal to the duty ratio D of the steady-state switching signal applied to the converter. Therefore, the peak-to-peak inductor current ripple in steady-state operation can be expressed as

$$\Delta i_{L,\text{pp,2L}} = \frac{v_{\text{in}} - v_{\text{out}}}{L f_{\text{e}}} D_{\text{e}} = \frac{v_{\text{in}}}{L f_{\text{s}}} M\ (1 - M) \tag{1.1}$$

It is also instructive to calculate the net volt-seconds applied to the inductor in each sub-interval of the switching period, which defines the peak magnetic flux in the inductor and constrains its core area. The net volt-second product for the buck converter is given by

$$\Lambda_{\text{2L}} = L\, \Delta i_{L,\text{pp,2L}} = \frac{v_{\text{in}}}{f_{\text{s}}} M\ (1 - M) \tag{1.2}$$

Inspecting the switching node voltage waveform in Fig. 1.3a, the buck converter can be categorized as a "two-level" converter, as the switching node voltage only takes one of two instantaneous values: 0 V or v_{in}. By contrast, multilevel topologies generate intermediate voltages between 0 V and v_{in} at the switching node. In this work, a multilevel converter that generates N total voltages at its switching node is referred to as an N-level converter. The converters differ in the mechanisms by which the multilevel switching node voltage is

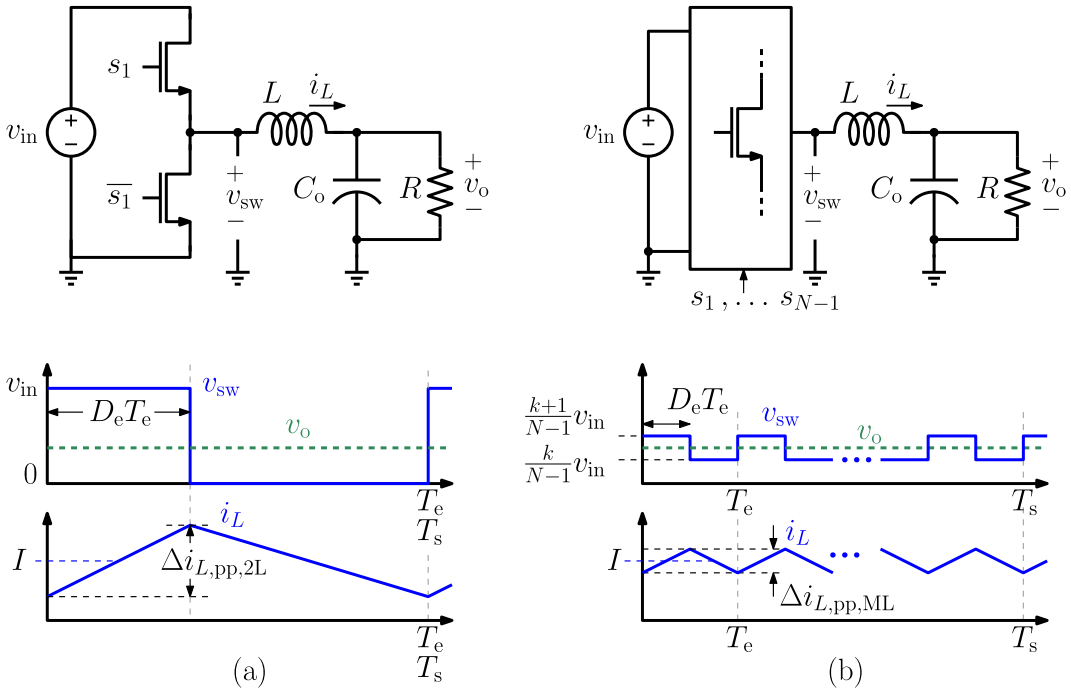


Figure 1.3: Steady-state switching node voltage v_{sw} and inductor current waveform i_L for (a) standard two-level buck converter; (b) N-level multilevel converter.

generated, but can generally be represented by the circuit abstracting the switching network shown in Fig. 1.3b.

In the case of multilevel converters, the switching node voltage alternates between two fractions of the input voltage, k/v_{in} and $(k+1)/v_{in}$, where k is given by a floor function as

$$k = \lfloor (N-1)\, M \rfloor \ , \ k \in \{0, 1, 2, \ldots, N-2\} \tag{1.3}$$

The effective frequency f_e of the switching node voltage waveform is $N-1$ times greater than the frequency f_s at which the devices in the converter are operated. As a consequence, the peak-to-peak inductor current ripple in steady-state operation for the multilevel converter is given by

$$\Delta i_{L,pp,ML} = \frac{\frac{k+1}{N-1}V_{in} - MV_{in}}{Lf_e} D_e = \frac{V_{in}}{Lf_s} \frac{D_e\,(1-D_e)}{(N-1)^2} \tag{1.4}$$

and the volt-second product for the multilevel converter is given by

$$\Lambda_{ML} = \frac{V_{in}}{f_s} \frac{D_e\,(1-D_e)}{(N-1)^2} \tag{1.5}$$

Here, the effective duty ratio in the multilevel case is given by

$$D_e = M\,(N-1) - k \tag{1.6}$$

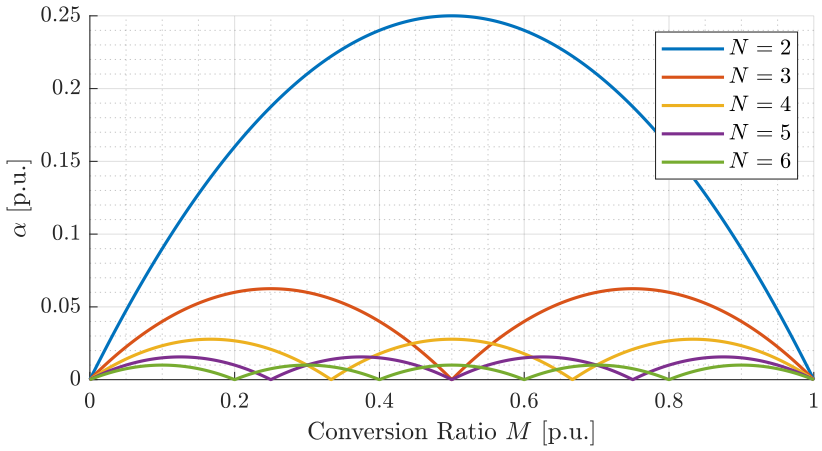


Figure 1.4: Parameter α given by (1.8) plotted as a function of conversion ratio M for different level counts $N = 2, \ldots, 6$.

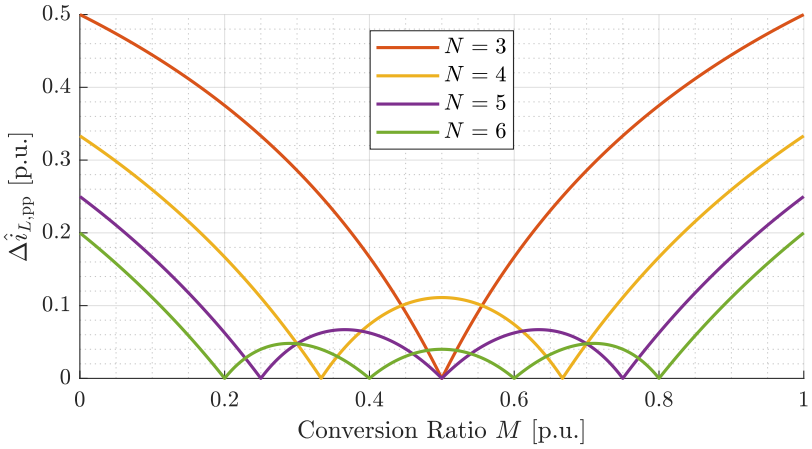


Figure 1.5: Normalized current ripple given by (1.9) plotted as a function of conversion ratio M for different level counts $N = 3, \ldots, 6$.

where k is given in (1.3). The expression in (1.5) can be compactly expressed as

$$\Lambda_{\mathrm{ML}} = \frac{V_{\mathrm{in}}}{f_{\mathrm{s}}}\,\alpha \tag{1.7}$$

$$\alpha := \frac{D_{\mathrm{e}}\,(1 - D_{\mathrm{e}})}{(N-1)^2} \tag{1.8}$$

where α is a unitless parameter incorporating the level count and effective duty ratio of the multilevel converter. Figure 1.4 depicts parameter α as a function of the conversion ratio M. The maximum value of α occurs when $D_{\mathrm{e}} = 0.5$, and for a given D_{e}, α scales inversely

with level count as $\frac{1}{(N-1)^2}$. Maintaining a constant inductance and switching frequency, the current ripple in the multilevel converter for any conversion ratio is smaller than that of a two-level converter. To emphasize this reduction, Fig. 1.5 plots the normalized current ripple defined as

$$\Delta\hat{i}_{L,\mathrm{pp}} := \frac{\Delta i_{L,\mathrm{pp,ML}}}{\Delta i_{L,\mathrm{pp,2L}}} = \frac{D_\mathrm{e}\left(1-D_\mathrm{e}\right)}{\left(N-1\right)^2\left(M\left(1-M\right)\right)} \tag{1.9}$$

as a function of the conversion ratio M. Alternatively, for a fixed current ripple specification and switching frequency, multilevel converters can always be designed with a smaller inductance L compared to a two-level converter.

In the general case, converters may be expected to operate over a range of conversion ratios due to variations in the supply voltage or, in the case of inverters, variations in the load voltage. Given an identical specification for the average inductor current and expected conversion ratio range $M_\mathrm{min} \leq M \leq M_\mathrm{max}$, the normalized volt-seconds

$$\hat{\Lambda} := \frac{\max_{M_\mathrm{min}\leq M\leq M_\mathrm{max}}\left\{\Lambda_\mathrm{ML}\right\}}{\max_{M_\mathrm{min}\leq M\leq M_\mathrm{max}}\left\{\Lambda_\mathrm{2L}\right\}} \tag{1.10}$$

can be used to compare the advantage of using an N-level converter compared to a two-level converter from the perspective of reduction in the inductor volume [34]. For converters operating over wide conversion ratio ranges where $(M_\mathrm{max} - M_\mathrm{min}) > \frac{1}{(N-1)}$, the normalized volt-seconds are given by

$$\hat{\Lambda} = \frac{1}{\left(N-1\right)^2}\cdot\frac{f_\mathrm{s,2L}}{f_\mathrm{s,ML}} \tag{1.11}$$

where $f_\mathrm{s,2L}$ is the switching frequency of the two-level converter and $f_\mathrm{s,ML}$ is the switching frequency of the multilevel converter. The expression in (1.11) suggests that the switching frequency in a multilevel design can be reduced while still maintaining lower normalized volt-seconds and consequently smaller magnetics. The benefits of this property will be highlighted in the following section.

Switching Devices

In medium- and high-voltage applications, often only a limited selection of commercially available power semiconductor devices rated for the converter port voltage is available. Power converter designers in these applications frequently seek system architectures and power converter topologies that allow for the use of switches rated only for a fraction of the full port voltage. However, even in applications where devices rated for the full voltage are widely available, low-voltage devices can be compelling as they enable the design to be more efficient. The advantages of using power semiconductor devices rated for lower blocking voltages are highlighted by studying the losses in the device, following the analysis of [34, 35].

Consider the simplified vertical device structure in Fig. 1.6a [34, 35] and its equivalent electrical circuit in the context of the switching converter as shown in Fig. 1.6b. Assuming

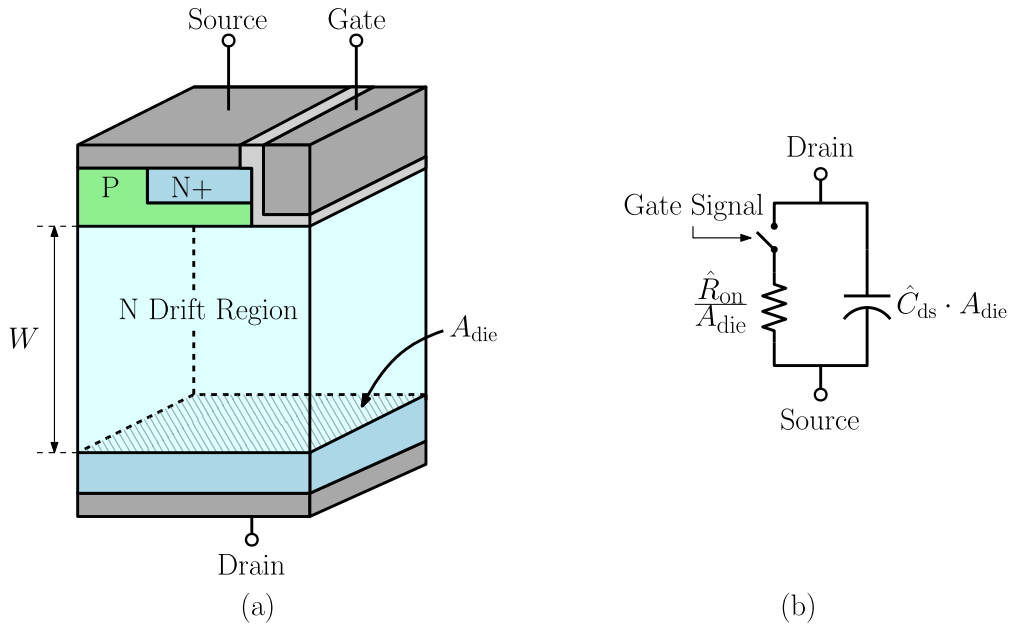


Figure 1.6: (a) Canonical vertical power semiconductor model used in [34, 35] to derive the voltage scaling characteristic of (1.14); (b) Equivalent circuit model of power semiconductor device, modeling parasitic per-unit-area on-state resistance $\hat{R}_{\text{on}}$ and per-unit-area drain-to-source capacitance $\hat{C}_{\text{ds}}$.

the device blocks a voltage v_{in} and is rated for a blocking voltage $V_{\text{B}} \geq v_{\text{in}}$, the total hard-switching loss in the device (ignoring overlap losses for simplicity) is the sum of the conduction and switching losses P_{cond} and P_{sw}, and is given by

$$P_{\text{loss}} = P_{\text{cond}} + P_{\text{sw}} = I_{\text{RMS}}^2 \cdot \frac{\hat{R}_{\text{on}}\left(V_{\text{B}}\right)}{A_{\text{die}}} + \hat{C}_{\text{ds}}\left(V_{\text{B}}\right) \cdot A_{\text{die}} \cdot v_{\text{in}}^2 \cdot f_{\text{s}} \tag{1.12}$$

where I_{RMS} is the root-mean-square (RMS) current through the switch; $\hat{R}_{\text{on}}\left(V_{\text{B}}\right)$ and $\hat{C}_{\text{ds}}\left(V_{\text{B}}\right)$ are the per-unit-area parasitic on-state resistance and drain-to-source capacitance respectively, parameterized in terms of the blocking voltage V_{B}; and f_{s} is the switching frequency. The loss mechanisms scale inversely as the switch die area A_{die} shown in Fig. 1.6a is modified—the conduction losses decrease with increasing area, whereas the switching losses increase with increasing area. Therefore, to evaluate losses across devices rated for different blocking voltages, it is useful to compare the best device possible for a given blocking voltage. The loss expression in (1.12) can be bounded using the mean inequality of [36] as

$$P_{\text{loss}} \geq 2 I_{\text{RMS}} v_{\text{in}} \sqrt{f_{\text{s}}} \cdot \sqrt{\hat{R}_{\text{on}}\left(V_{\text{B}}\right) \cdot \hat{C}_{\text{ds}}\left(V_{\text{B}}\right)} \tag{1.13}$$

Therefore, for an application specifying the RMS switch current, switch blocking voltage, and switching frequency, the quantity $\sqrt{\hat{R}_{\text{on}}\left(V_{\text{B}}\right) \cdot \hat{C}_{\text{ds}}\left(V_{\text{B}}\right)}$ dictates the optimal loss in a

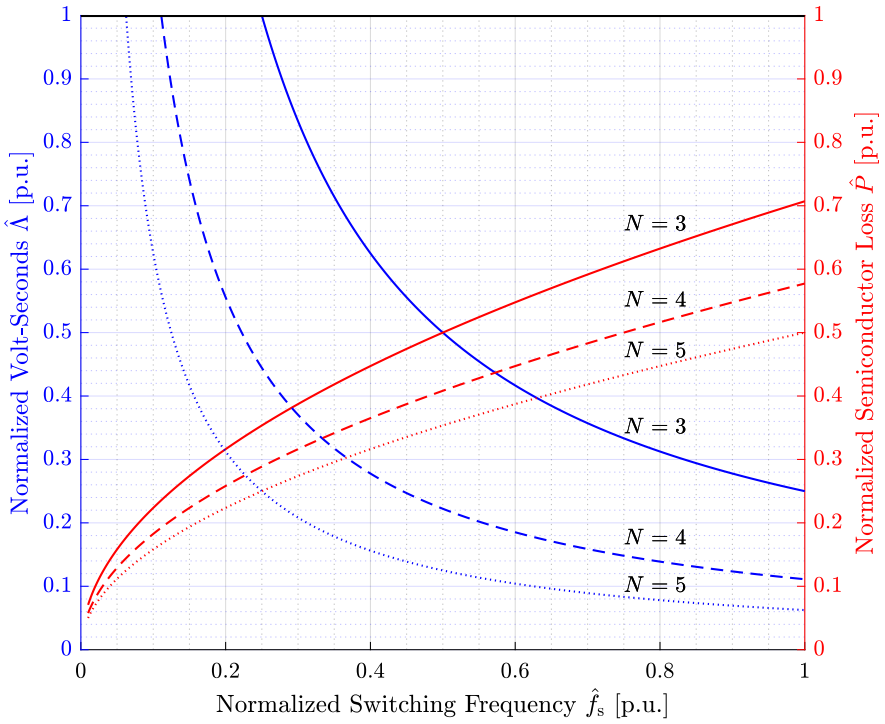


Figure 1.7: Normalized volt-seconds $\hat{\Lambda}$ given by (1.11) and normalized semiconductor loss $\hat{P}$ given by (1.17) plotted as a function of the normalized switching frequency $\hat{f}_s$ defined in (1.18). An N-level converter performs better than a two-level converter in the range $\frac{1}{(N-1)^2} < \hat{f}_s < 1$.

switch rated for blocking voltage V_B, and can be used to compare devices with different blocking voltages. Following the standard analysis of the structure in Fig. 1.6 given in [34, 35] for silicon devices, the quantity $\sqrt{\hat{R}_{on}(V_B) \cdot \hat{C}_{ds}(V_B)}$ can be approximated as

$$\sqrt{\hat{R}_{on}(V_B) \cdot \hat{C}_{ds}(V_B)} \approx \sqrt{k_R k_C} \cdot \sqrt{V_B} \tag{1.14}$$

where k_R and k_C are material parameters. This analysis highlights that the losses in the power semiconductor device increase as its rated blocking voltage is increased. Therefore, the minimum possible semiconductor loss for a hard-switching device in a two-level converter is achieved when the device is rated for blocking voltage $V_B = V_{in}$, and is given by

$$P_{min,2L} = 2 I_{RMS} v_{in}^{\frac{3}{2}} \sqrt{f_s} \sqrt{k_R k_C} \tag{1.15}$$

Suppose the multilevel converter replaces the single power device with $N-1$ series-connected devices, as is the case in the FCML converter shown in Fig. 1.1a. As each device must only

be rated to block $\frac{V_{\text{in}}}{(N-1)}$ in its off-state, the minimum total hard-switching loss in the $N-1$ devices is

$$P_{\text{min,N}-1} = \frac{1}{\sqrt{N-1}} \cdot 2 I_{\text{RMS}} v_{\text{in}}^{\frac{3}{2}} \sqrt{f_{\text{s}}} \sqrt{k_{\text{R}} k_{\text{C}}} \tag{1.16}$$

For identical switching frequency, the total loss in the $N-1$ lower voltage devices is reduced by a factor of $\sqrt{N-1}$ compared to the total loss in the single device rated for V_{in}. Observing from (1.11) that the multilevel converter retains favorable volt-second characteristics at lower switching frequencies, it is not necessary to switch both the multilevel design and the two-level design at the same frequency. Allowing the switching frequency to be different, a normalized semiconductor loss term comparing the minimum hard switching losses in both converters can be defined as

$$\hat{P} := \frac{P_{\text{min,ML}}}{P_{\text{min,2L}}} = \frac{1}{\sqrt{N-1}} \cdot \sqrt{\frac{f_{\text{s,ML}}}{f_{\text{s,2L}}}} \tag{1.17}$$

Fig. 1.7 plots both the normalized volt-seconds $\hat{\Lambda}$ given in (1.11) and the normalized semiconductor loss $\hat{P}$ given in (1.17) on common axes as a function of the normalized switching frequency

$$\hat{f}_{\text{s}} := \frac{f_{\text{s,ML}}}{f_{\text{s,2L}}} \tag{1.18}$$

For each level count N, the normalized volt-seconds and the normalized semiconductor loss are both simultaneously lower than unity when the two-level and multilevel converter are operated with the same switching frequency ($\hat{f}_{\text{s}} = 1$). As the switching frequency is reduced, the multilevel converter can perform better than the two-level converter with respect to both power density and efficiency in the range $\frac{1}{(N-1)^2} < \hat{f}_{\text{s}} < 1$. The simultaneous improvement of volt-seconds and semiconductor losses is only possible due to the higher effective frequency of the switching node voltage, motivating the study of multilevel converters such as those shown in Fig. 1.1 compared to others that do not exhibit this property.

A few nuances of the discussion above are worth highlighting before concluding this section. First, the approximation given in (1.14) is only valid for the simple vertical device structure studied. The characterization of commercially available silicon-carbide and gallium-nitride devices in [34] reveals that the quantity $\sqrt{\hat{R}_{\text{on}}(V_{\text{B}}) \cdot \hat{C}_{\text{ds}}(V_{\text{B}})}$ generally scales as

$$\sqrt{\hat{R}_{\text{on}}(V_{\text{B}}) \cdot \hat{C}_{\text{ds}}(V_{\text{B}})} = \sqrt{k_{\text{R}} k_{\text{C}}} \cdot V_{\text{B}}^{\alpha} \quad , \quad 0 < \alpha < 0.5 \tag{1.19}$$

This variation changes the relationship between normalized switching frequency and normalized semiconductor loss visualized in Fig. 1.7, but does not affect the principle of exchanging semiconductor losses and inductor volt-seconds by modifying the switching frequency. Second, the analysis has assumed that power semiconductor devices are available with arbitrarily granular blocking voltage ratings. In practice, economies of scale in semiconductor manufacturing result in device availability only at a few discrete blocking voltages (eg: 100 V, 200 V,

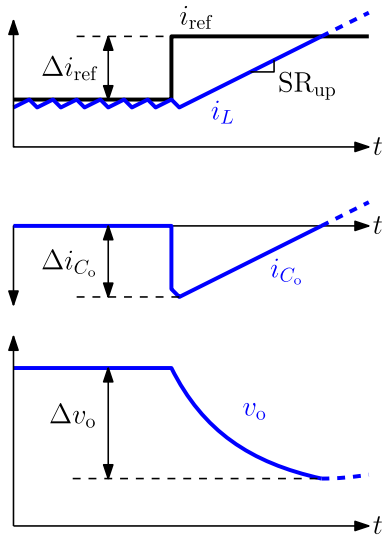


Figure 1.8: Illustration of the inductor current i_L, output capacitor current i_{C_o} and output voltage v_o during a transient in the inductor current reference i_{ref}. This scenario corresponds to the minimum output voltage deviation Δv_o during the load step-up transient.

650 V, 1.2 kV) for a given technology. Thus, higher figure-of-merit devices rated for lower blocking voltages may not necessarily be available for higher level-count designs. Finally, the analysis of converter performance has conspicuously neglected practical considerations such as overlap losses in the semiconductor devices, losses in the inductor, and the volume of the semiconductor devices and associated gate drive hardware. For more complete analysis of scaling laws relevant to the design of multilevel converters, the reader is referred to the examples in [37–41].

Dynamic Response

The reduced inductance requirement and higher effective frequency of the inductor current ripple in multilevel converters have favorable implications for the converter dynamics from several perspectives. The improved load-transient response of multilevel converters has received recent attention for dc-dc applications in [5, 42–51]. For dc-ac applications, recent work in [52, 53] has highlighted opportunities for multi-sampled control at the effective switching frequency, reducing modulator delays and enabling higher-bandwidth current control loops.

The reduced inductance in the output filter of multilevel converters corresponds to a higher maximum slew rate of the inductor current in response to load transients. For step-down converters with a filter inductor at the load side, the theoretical maximum inductor current slew-up and slew-down rates corresponding to application of v_{in} or 0 V at the switch-

ing node respectively are given by

$$\mathrm{SR_{up}} = \frac{v_{\mathrm{in}}}{L}\,(1-M) \tag{1.20}$$

$$\mathrm{SR_{down}} = \frac{v_{\mathrm{in}}}{L}\,(-M) \tag{1.21}$$

Fig. 1.8 illustrates the inductor current and output voltage waveforms corresponding to minimum output voltage deviation in a peak current-controlled step-down converter. The inductor current reference i_{ref} is stepped by a value of Δi_{ref} in response to a load transient. Assuming negligible parasitic resistance in the output capacitor and that the peak-to-peak inductor current ripple is negligible relative to its average value, the minimum possible output voltage deviation Δv_{o} is approximated by

$$\Delta v_{\mathrm{o}} \approx \frac{1}{C}\cdot\frac{\left(\Delta i_{\mathrm{ref}}\right)^2}{2\,\mathrm{SR_{up}}} \tag{1.22}$$

for the step-up load transient and

$$\Delta v_{\mathrm{o}} \approx \frac{1}{C}\cdot\frac{\left(\Delta i_{\mathrm{ref}}\right)^2}{2\,\left|\mathrm{SR_{down}}\right|} \tag{1.23}$$

for the step-down load transient. For two-level converters, several works have investigated techniques to regulate the inductor current and output voltage in the converter to achieve near-minimum output voltage deviation or time-optimal recovery of the converter output voltage under load transients [54–60]. As the inductance required to meet a fixed current ripple specification is $(N-1)^2$ times lower in the multilevel converter, the magnitudes of $\mathrm{SR_{up}}$ and $\mathrm{SR_{down}}$ are $(N-1)^2$ times greater, implying $(N-1)^2$ times smaller output voltage deviation for the same output capacitance. Alternatively, multilevel converters achieve identical deviation in the output voltage with a smaller output capacitance compared to a two-level converter, though practical considerations such as the effects of parasitic resistances in the output capacitor may limit this reduction.

In applications incorporating average current control loops, the higher effective frequency of the inductor current waveform in multilevel converters allows for higher sampling rates for a given switching frequency, corresponding to shorter controller and modulator delays. To control the average current, the digital controller must sample the inductor current waveform without introducing artifacts of the current ripple into the measurements. This is typically accomplished by restricting the sampling frequency to a maximum of two times the fundamental frequency of the current ripple, which intentionally aliases the ripple content to dc and prevents it from appearing in the sampled data [61–64]. In multilevel converters, the higher effective fundamental frequency of the inductor current ripple allows for the digital controller to sample the average inductor current up to $2\,(N-1)$ times per switching period. Consequently, *multi-sampled* average current control loops for multilevel converters can also achieve higher bandwidths compared to their two level counterparts, assuming the current controller can appropriately compensate the small-signal characteristics of the multi-sampled modulator [52].

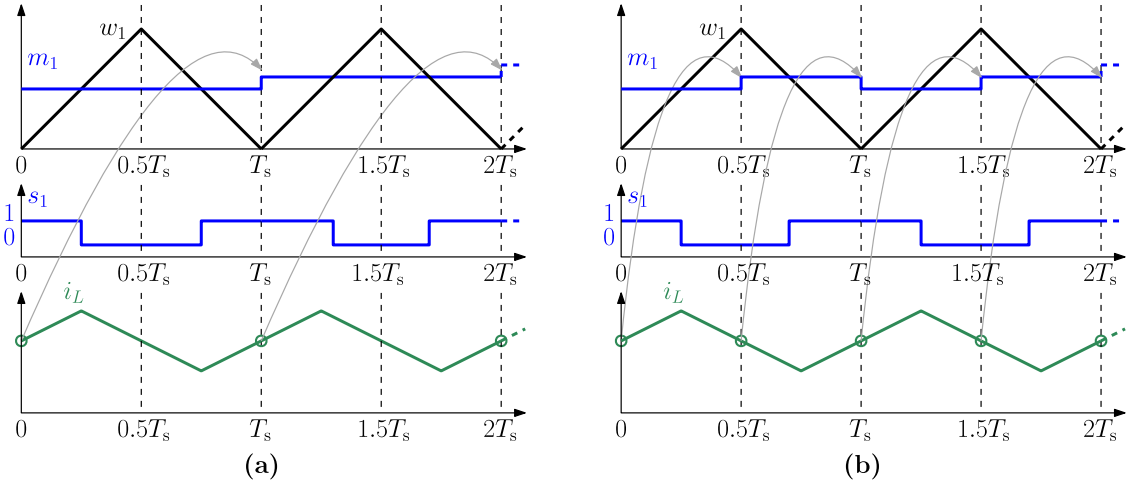


Figure 1.9: Digital PWM sampling and update modes for a two-level converter implementing average current control, considering a one-step computation delay: (a) single-sampling single-update at carrier valley; (b) double-sampling double-update at carrier peaks and valleys.

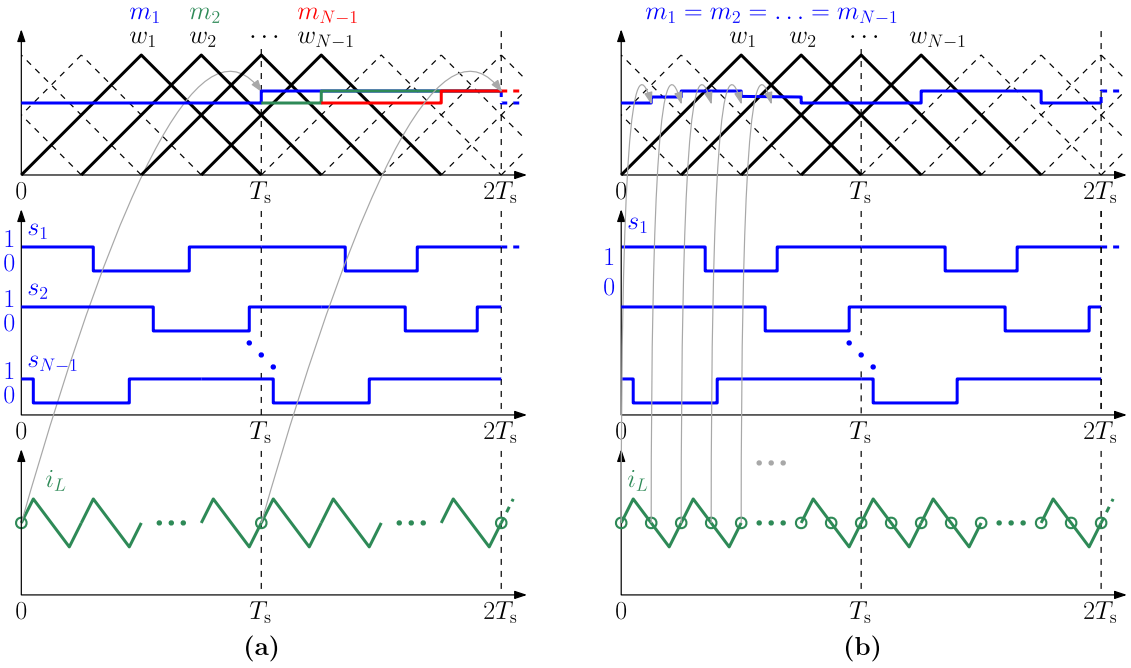


Figure 1.10: Digital PWM sampling and update modes for an N-level converter implementing average current control, considering a one-step computation delay: (a) single-sampling single-update at carrier w_1 valley; (b) multi-sampling, multi-update at peaks, valleys, and intersections of all carriers [52]. For multilevel converters, double-update schemes are also possible, but are not shown in this figure for clarity.

Typically average current control is implemented by synchronizing the sampling instants with either or both of the carrier peaks and valleys [62]. Fig. 1.9 illustrates the possible sampling synchronization schemes for a two-level converter. Sampling the inductor current once or twice per period as shown in Fig. 1.9a and Fig. 1.9b respectively corresponds to the standard single- and double-sampled implementations of regularly sampled PWM [52]. Like two-level converter, multilevel converters can be controlled through single-sampled schemes as shown in Fig. 1.10a, but can also incorporate multi-sampled schemes where the inductor current is sampled at the peaks, valleys, and intersections of carriers as shown in Fig. 1.10b. This is of particular interest in grid-tied converters, where the modulator delays can impact the stability characteristics of the converter and connected system [52, 64]. A detailed discussion of multi-sampling and its application to multilevel converters operated with PS-PWM can be found in [52, 53].

Several recent works [42, 46–48, 50, 51, 65] have investigated controllers for multilevel converters to make effective use of the faster slew rates and opportunities for multi-sampling. The works of [42, 47] investigate peak and valley current control for 3-level Flying Capacitor Multilevel (FCML) converters in point-of-load voltage regulator applications. The voltage-mode controller presented in [46] aims for minimum deviation of the output voltage under load transients. The work of [65] develops a controller that can respond to load transients in optimal time. The predictive digital controllers presented in [50] for peak, valley, and average current control aim for dead-beat (single-cycle) control of the inductor current. The work in [50] also investigates multi-sampled predictive control where the predictive control law is evaluated at the effective frequency of the inductor current ripple as opposed to the switching frequency. The analysis in [52] develops analytical models for the modulator delay in single- and multi-sampled digital PS-PWM implementations. The works highlighted above study different methods for control of the inductor current and output voltage in multilevel converters. The controllers presented are generally more complex than those developed for two-level converters, however, as they are required to implement additional functions to maintain nominal "balanced" operation. In implementation, the need for balancing can prevent multilevel converters from achieving the true optimal response shown in Fig. 1.8. The nature of this issue is described in greater detail at the end of this chapter and motivates the research presented in the remainder of this work.

Summary

Multilevel converters featuring reduced voltages across power semiconductor devices and a higher fundamental frequency of the voltage applied across filter magnetic components enable simultaneous improvements in passive component volume and power semiconductor losses compared to standard two-level solutions. For the class of converters studied, the reduced filter inductance required to meet a current ripple specification and the higher fundamental frequency of the inductor current ripple also enable improved dynamic response through higher inductor current slew rates and compatibility with multi-sampled control. Among the class of converters that demonstrate the properties highlighted in the beginning of this

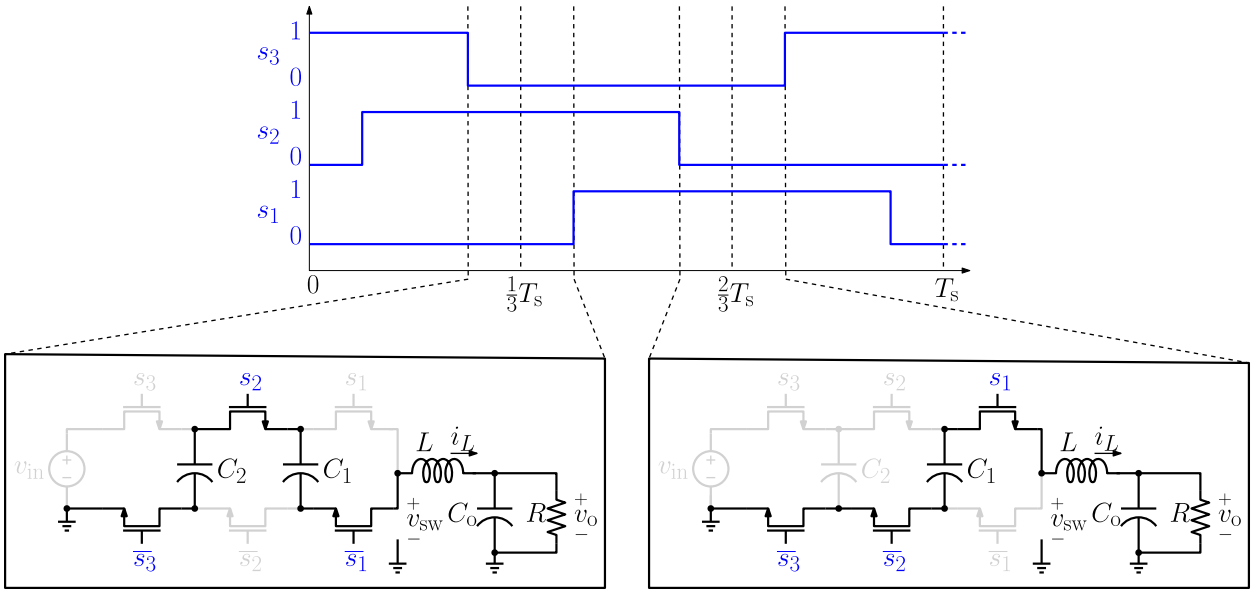


Figure 1.11: Switching signals under PS-PWM for a 4-level FCML converter, highlighting the circuit states in two switching phases. In each switching phase, a maximum of two flying capacitors are connected in series with the inductor.

chapter, the Flying Capacitor Multilevel (FCML) converter is particularly attractive as it is also practical for dc modulation and can therefore be used in dc-dc conversion applications [25, 32, 66]. By contrast, the Cascaded H-Bridge (CHB) converter shown in Fig. 1.1 requires multiple isolated voltage domains for nonzero average power delivery in dc-dc applications, which can have a significant impact on the system's volume and efficiency. Furthermore, the FCML converter features a lower number of power semiconductor devices for a given level count compared to the CHB converter. The following section provides an overview of the principles and challenges of standard "naturally balanced" operation of the FCML converter.

1.3 Naturally Balanced FCML Converter Operation

The discussion so far has implicitly assumed that the capacitor voltages $v_{c,k}$ with $k \in \{1, 2, \ldots, M\}$ follow the nominal "balanced" distribution shown in Fig. 1.1, expressed as

$$v_{c,k} = \frac{k}{N-1} v_{\text{in}} \quad , \; k \in \{1, 2, \ldots, M\} \tag{1.24}$$

A few additional characteristics of typical designs enable the linear-ripple inductor current characteristic described in Section 1.2 where the effective fundamental frequency of the current ripple is $f_e = (N-1)\, f_s$ under balanced conditions. First, the input and output voltage ripples and flying capacitor voltage ripples are assumed negligible such that the inductor

current ripple is only a function of the dc input voltage and dc flying capacitor voltages. Second, the output capacitor $C_{\rm o}$ is assumed to be significantly larger in value than the flying capacitors such that in each switching phase, the inductor current and flying capacitor voltages are well-approximated by a second-order LC response corresponding to only the series connection of the inductor and flying capacitors. Third, the effective frequency $f_{\rm e}$ is assumed to be much greater than the LC-resonant frequency of this equivalent circuit. When the converter is operated with PS-PWM, the switching phases occurring within a switching period consist of either zero, one, or two capacitors connected in series with the inductor. To illustrate this property, Fig. 1.11 highlights two switching phases occurring under PS-PWM for a 4-level converter. In the first switching phase shown, the flying capacitors are both connected in series with the inductor; in the second switching phase shown, only capacitor C_1 is connected. If the values of all flying capacitors are assumed to be identical ($C_1 = C_2 = \cdots = C_M = C$) the switching frequency requirement given above can be summarized as

$$f_{\rm e} >> \frac{1}{2\pi\sqrt{LC}} \tag{1.25}$$

A fourth standard assumption which allows for straightforward computation of the flying capacitor voltage ripples is that the peak-to-peak inductor current ripple is negligible compared to its average value, however this assumption is not strictly necessary for sizing the flying capacitors.

Under the assumptions of small voltage ripples and sufficiently high switching frequency described above, the output states of the converter—the inductor current and output voltage—can be controlled via the typical techniques developed for two-level converters. Treating the flying capacitor voltages as balanced, the works in [67–70] design control loops for the converter output based on its averaged model [71] given by

$$\dot{\overline{v_{c,k}}} = 0 \tag{1.26}$$

$$\dot{\overline{i_L}} = \frac{1}{L}\left(\overline{v_{\rm in}} \cdot D - \overline{v_{\rm o}}\right) \tag{1.27}$$

$$\dot{\overline{v_{\rm o}}} = \frac{1}{C_{\rm o}}\left(\overline{i_L} - \frac{\overline{v_{\rm o}}}{R}\right) \tag{1.28}$$

where the overline notation $\bar{x}$ indicates the quantity x averaged over one switching period $T_{\rm s}$. The averaged model is derived in detail in subsequent chapters, however an immediate observation from (1.26) is that the standard averaging methods of [71] predict zero dynamics for the capacitor voltages. This motivates a critical underlying question—are the capacitor voltages truly static as the averaged model suggests, or is there some other balancing mechanism not captured by averaging?

The issue of whether and under what conditions the capacitor voltages are maintained at the nominal values given in (1.24) is of great practical significance. If the capacitor voltages are not balanced, the fundamental frequency $f_{\rm e}$ of the switching node voltage $v_{\rm sw}$ is not $N-1$ times greater than the switching frequency $f_{\rm s}$, and the RMS current in the

filter inductor is greater, resulting in increased losses in the switching devices, inductor, and output capacitor. In addition, a deviation of the capacitor voltages away from the balanced distribution subjects some of the switching devices to off-state voltages exceeding the nominal value of $\frac{v_{\text{in}}}{(N-1)}$, which can be catastrophic in high-voltage applications using low-voltage semiconductor devices.

Following the initial presentation of the FCML conveter in [25], the works of [72–78] have investigated the dynamic behavior of the capacitor voltages under operation with symmetric PS-PWM. These works reveal mechanisms through which the capacitor voltages reach their nominal balanced values—collectively referred to as the "natural balancing" property—that are not described by the standard averaged model of the converter in (1.26). Fig. 1.12 shows this natural balancing property in measured capacitor voltages from a 5-level FCML converter prototype. The converter is subjected to a step in the input voltage from 7 V to 30 V, and the capacitor voltages settle to the new balanced distribution after approximately 30 ms. The models presented in [72–74, 78] primarily find that the natural balancing of capacitor voltages arises from the coupling between the capacitor voltages and the inductor current ripple, which will be studied in greater detail in subsequent chapters. Parasitic elements such as the drain-source capacitances of the switching devices have also been demonstrated to contribute to natural balancing in [76, 77, 79, 80]. The steady-state capacitor voltages may differ from the values given in (1.24) due to phenomena present in physical converters that are typically omitted in standard converter models. In particular, the analysis in [81]

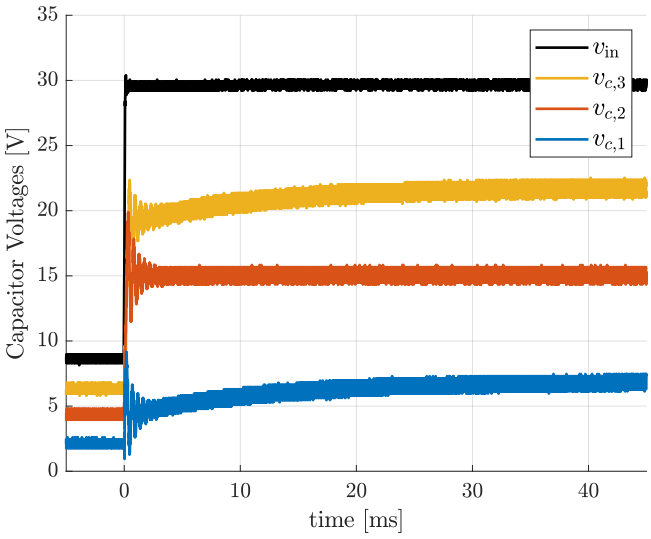
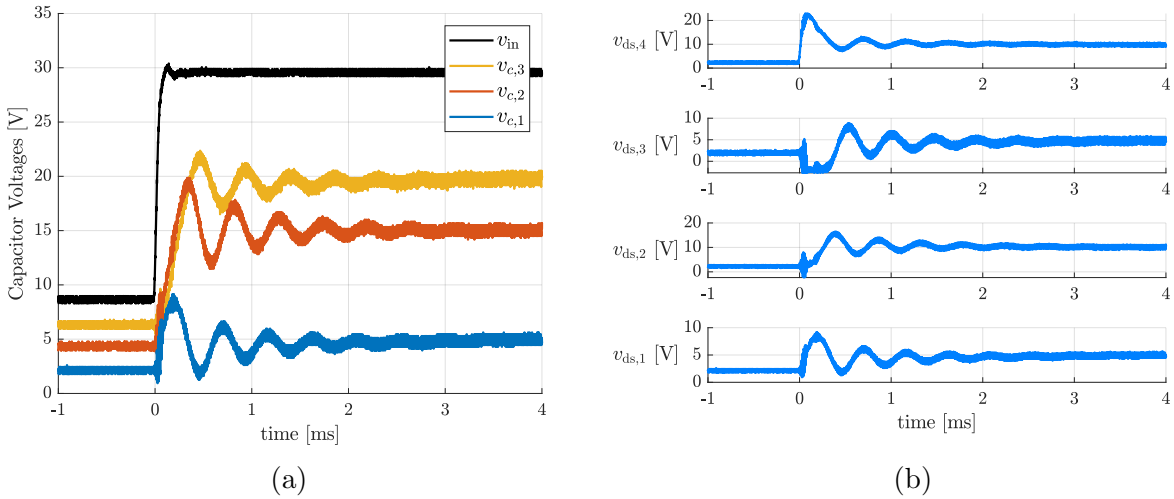


Figure 1.12: Measured voltage response in a 5-level FCML converter for a step in the input voltage v_{in} from 7 V to 30 V. The converter is configured with $C = 8.8\,\mu\text{F}$, $L = 10\,\mu\text{H}$, $f_{\text{s}} = 75\,\text{kHz}$, and $R = 8\,\Omega$. Over a timescale of approximately 30 ms, the capacitor voltages balance to their respective nominal fractions of the input voltage.



(a) (b)

Figure 1.13: (a) Measured waveforms of Fig. 1.12, showing the underdamped capacitor voltage behavior in a timescale of 4 ms after the input voltage step; (b) Off-state switch drain-source voltages v_{ds}, highlighting the excessive voltage observed across switch pair s_4.

finds that switching frequency ripple present at the input of the converter and variations in the duty ratios and phase shifts of switching signals arising from asymmetric propagation delays in gate drive circuitry contribute to steady-state capacitor voltage imbalance. As these nonidealities typically only result in small steady-state deviations of capacitor voltages on the order of 5% of the nominal values [81], they are neglected in this work in favor of studying the far greater imbalance that occurs during the natural balancing transient.

The instantaneous imbalance that occurs as capacitor voltages settle to their balanced values can be significant, and is a practical consideration limiting broader adoption of FCML converters. Natural balancing under PS-PWM is typically characterized by underdamped dynamics. The waveforms shown in Fig. 1.13a for the 5-level converter in a timescale of 4 ms after the input voltage step highlight that the capacitor voltage responses can be highly oscillatory immediately after the line transient has occurred. These oscillations result in excessive voltages across the switching devices. Fig. 1.13b highlights the off-state switch drain-source voltages during the balancing transient shown in Fig. 1.13a. A peak stress of 20 V volts is observed across switch s_4, corresponding to 267% of the nominal value or 7.5 V. Several techniques have been proposed in the literature to achieve faster natural dynamics. The works of [72, 73, 82–85] propose the addition of a resonant "balance booster" circuit between the switching node and ground to improve the natural balancing speed. In [72, 73] the speed of the natural balancing response is found to be inversely related to the amplitude of ripple in the inductor current, motivating slower switching frequencies for improved flying capacitor voltage dynamics. While enabling some improvements in the natural balancing response, these techniques also present practical challenges. The addition of balance booster circuits

negatively impacts the converter volume through the large passive components added to the output filter network. Reductions in switching frequency to improve balancing response result in increased inductor current ripple, which can have a detrimental impact on converter efficiency and output current quality. Furthermore, the techniques proposed in [72, 73, 82–85] often still yield capacitor voltage dynamics that are too slow to track fast line voltage variations such as those associated with converter start-up and shut-down scenarios. As a consequence, to ensure that the flying capacitor voltages remain approximately balanced, most practical demonstrations of FCML converters assume that the converter input voltage is only ramped slowly during start-up and shut-down through pre-charge circuits [86, 87]. Alternatively, designs such as [88] replace the low-voltage high-figure-of-merit power semiconductor devices in the converter with devices that can tolerate the full supply voltage, to enable faster start-up and guarantee robust converter operation at the cost of increased losses in the switches. These techniques have undesirable consequences for system power density and efficiency, and introduce additional thermal management challenges that may ultimately make the FCML converter an unattractive alternative to conventional solutions.

1.4 Research Outline

This work presents solutions for regulating the flying capacitor voltages through closed-loop "active balancing" control. Compared to the natural balancing dynamics under converter operation with PS-PWM, the closed-loop design aims for faster capacitor voltage response to line transients. A key feature of active balancing control, as will be highlighted in subsequent chapters, is the ability to specify the closed-loop dynamics as part of the controller design process. In contrast to the natural balancing mechanism, where the capacitor voltage behavior is complex function of the converter design and operating point, this quality of active balancing control is highly valuable.

The remainder of this thesis is organized as follows:

Chapter 2: Active Balancing Based on the Standard Averaged Model

An active balancing controller is derived using the standard averaging procedure of [71]. First, the principles of standard averaged modeling are reviewed. Next, an averaged plant model for the FCML converter is derived, and its linearization is shown to have a parallel structure. A "parallel controller" is designed to regulate flying capacitor voltages and the inductor current simultaneously. The parallel controller is shown to enable significantly improved capacitor voltage balancing during line transients, and the performance improvements obtained through active balancing control are quantified through frequency response characterizations. Small-signal instabilities are shown to arise in light-load conditions and are experimentally characterized. Finally, the proposed active balancing controller derived

from the averaged model of the converter is compared to state-of-the-art techniques in the literature.

Chapter 3: Generalized Averaged Modeling

The dynamics of the FCML converter are studied more rigorously through the procedure of generalized averaged modeling [89] to analyze the impact of the inductor current ripple on the average capacitor voltages. First, the method of generalized averaged modeling is reviewed. Next, a model for the FCML converter is derived without making a small-ripple approximation for the inductor current. The inductor current ripple is characterized through the inclusion of its harmonic content at multiples of the switching frequency. A reduced-order model for the generalized averaged system is obtained through the application of singular perturbation theory [90–92], where it is shown that the switching period is a small parameter characterizing the separation of timescales between the dynamics of the inductor current ripple and those of the average capacitor voltages. The reduced-order model is employed to study the minimum number of harmonics modeling the inductor current ripple that are required to accurately capture the capacitor voltage dynamics. The reduced-order model is subsequently linearized to study the closed-loop dynamics with active balancing control, and is shown to accurately capture small-signal instabilities at light-load conditions. The model is verified through experimental characterization of a hardware prototype in natural balancing and active balancing scenarios.

Chapter 4: Charge Models for Averaging Effects of Ripple

The contribution of the inductor current ripple to the dynamics of the average capacitor voltages is characterized by studying the net change in charge stored on the flying capacitors over a switching period. First, an expression for the charge flow into and out of the flying capacitors in a 4-level FCML converter is obtained by approximating the inductor current ripple as piecewise-linear in each switching phase. The small-signal impacts of perturbations in the switching node voltage pulse position on the capacitor voltages are studied to obtain a plant model for active balancing controller design. The plant model is verified against small-signal analysis of circuit simulation. Next, a state-feedback controller is designed to damp the oscillatory capacitor voltage dynamics. The small-signal plant model and closed-loop system with active balancing control are experimentally verified on a hardware prototype. In particular, the proposed controller is shown to be stable at light loads as it incorporates the impacts of the inductor current ripple. Finally, the charge model is shown to be equivalent the order-1 averaged model resulting from application of KBM averaging theory [93–95].

Chapter 5: Conclusions and Directions for Future Study

The main contributions of this thesis are summarized, and relevant areas for continued research in dynamical modeling and control of the FCML converter are highlighted.

Chapter 2

Active Balancing Based on the Standard Averaged Model

Portions of this chapter are adapted in whole or in part from [96].

Under symmetric PS-PWM, where the duty ratios of all switching signals are equal and neighboring switching signals are equally phase-shifted, the averaged converter model predicts zero capacitor voltage dynamics. However, when the duty ratios are allowed to vary independently, the averaged converter model predicts that differences in the duty ratios of neighboring switching signals yield nonzero average current into the flying capacitors. Treating perturbations in duty ratios away from the nominal value under symmetric PS-PWM as control inputs, the averaged converter dynamics can serve as a plant model for active balancing control. An implicit assumption is that the capacitor voltage dynamics predicted by the averaged model dominate over the natural balancing dynamics not captured by averaging. This section first details the design of an active balancing controller that can be implemented in parallel with controllers regulating the converter output current. The proposed controller is shown to enable significant improvements in capacitor voltage balancing compared to natural balancing demonstrations under the same operating conditions. The controller is also shown to achieve higher-bandwidth closed-loop performance compared to prior work, as it maintains decoupled closed-loop flying capacitor voltage dynamics and compensates interactions between the active balancing and current controllers. Subsequently, the validity of the averaged model is studied as a function of the converter operating point, and small-signal instabilities are shown to arise in conditions where the small-ripple approximation of the inductor current inherent to averaged modeling is not valid.

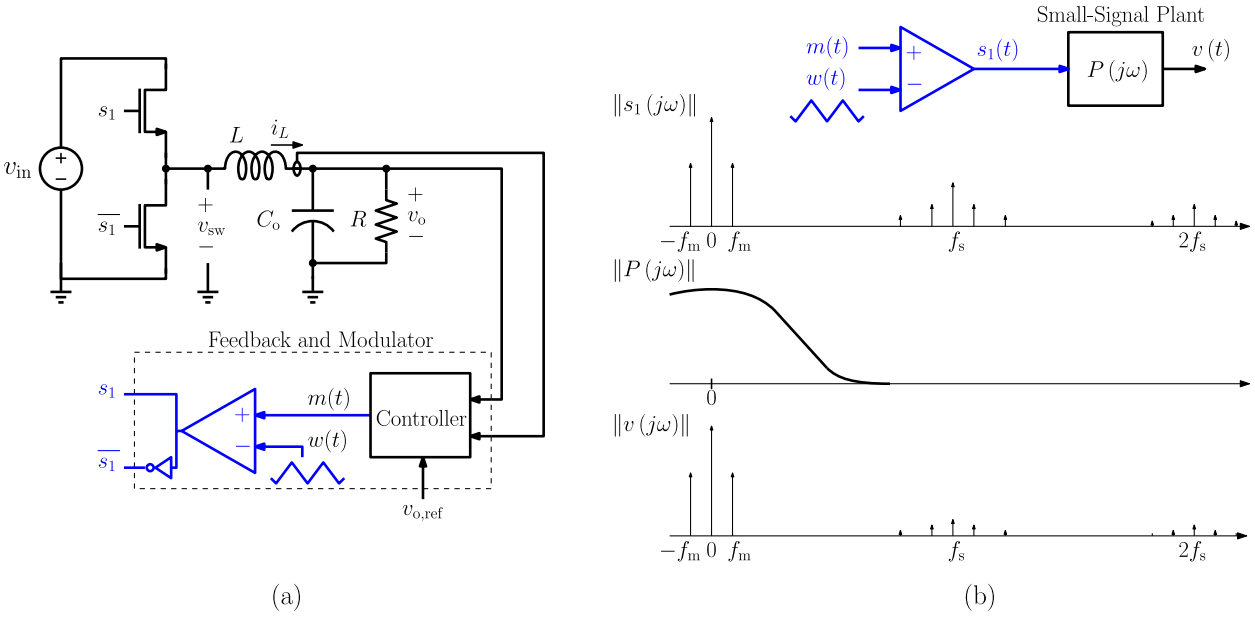


Figure 2.1: (a) General representation of feedback control and the pulse width modulator in a two-level converter; (b) Frequency domain representation of the open-loop small-signal system response to the pulse width modulated switching signal with modulation frequency $f_{\text{m}} << f_{\text{s}}$. Assuming the plant has a low-pass characteristic, the dominant components of the plant output $v(t)$ occur at dc and the modulation frequency f_{m}.

2.1 A Review of Standard Averaged Modeling of Power Converters

In the most general sense, averaging seeks to approximate an original system consisting of time-periodic dynamics with a time-invariant system that can be studied and controlled in a more straightforward manner. In the study of switching circuits, averaging finds application when the goal of modeling is to capture the "local average" behavior of voltages and currents while neglecting or simplifying the impacts of ripple in the state variables. Averaged models take various forms depending on how the ripple in state variables is treated. In many pulse-width-modulated converters operating in the continuous conduction mode (CCM), ripples in inductor currents and capacitor voltages are small by design and their impact on the local average converter behavior can be ignored with negligible impact on the accuracy of the resulting model. This is the standard notion of averaging in power electronics, presented in [71, 94, 97, 98] and studied in detail in [99, 100]. In some topologies such as resonant converters, the ripple in state variables has significant impact on the average behavior of the converter output voltage. For these topologies, refined methods of averaging are required. These averaging methods will be detailed in the following chapters in the context of developing more accurate models for the FCML converter.

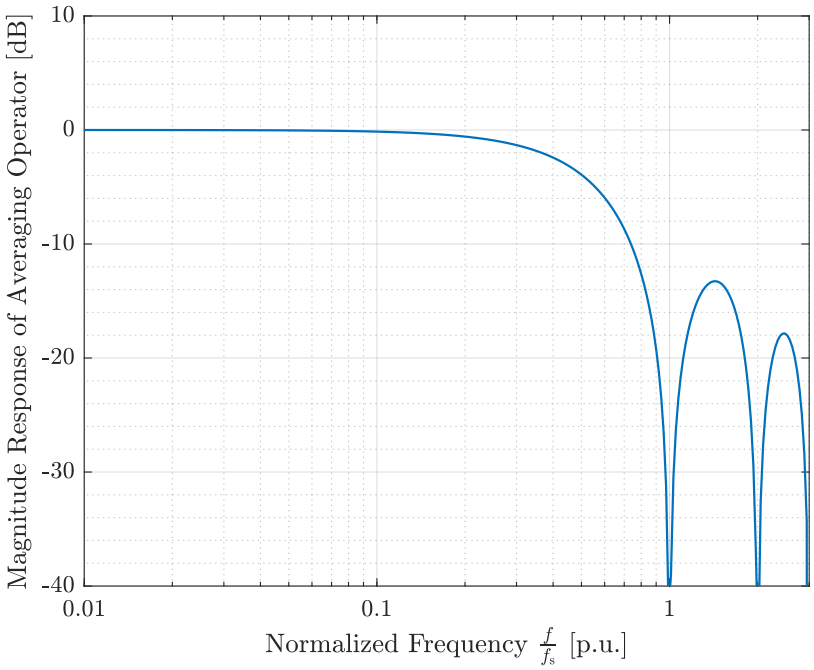


Figure 2.2: Magnitude response of averaging operator (2.4). Assuming the modulation frequency is significantly lower than the switching frequency ($f_{\mathrm{m}} << f_{\mathrm{s}}$) the averaging operator captures the baseband content shown in Fig. 2.1.

The standard theory of averaging [71, 94] considers N-dimensional systems with state vector $\boldsymbol{x} \in \mathbb{R}^N$ and exogenous inputs $\boldsymbol{w} \in \mathbb{R}^{N_{\mathrm{u}}}$ described via T_{s}-periodic dynamics

$$\dot{\boldsymbol{x}} = \boldsymbol{f}\left(\boldsymbol{x}, \boldsymbol{w}, t\right) \tag{2.1}$$

$$\boldsymbol{f}\left(\,\cdot\,,\,\cdot\,, t + kT_{\mathrm{s}}\right) = \boldsymbol{f}\left(\,\cdot\,,\,\cdot\,, t\right)\ ,\ k \in \mathbb{Z} \tag{2.2}$$

The state variables consist of capacitor voltages and inductor currents in the converter, and the exogenous inputs consist of independent voltage and current sources connected to the converter ports. The averaging procedure approximates the system in (2.1) by a time-invariant (but generally nonlinear) system given by

$$\dot{\overline{\boldsymbol{x}}} = \boldsymbol{f}_{\mathbf{avg}}\left(\overline{\boldsymbol{x}}, \overline{\boldsymbol{w}}, \boldsymbol{d}\right) \tag{2.3}$$

where

$$\boldsymbol{f}_{\mathbf{avg}}\left(\cdot\right) = \frac{1}{T_{\mathrm{s}}} \int_0^{T_{\mathrm{s}}} \boldsymbol{f}\left(\cdot, \tau\right) d\tau \tag{2.4}$$

and $\boldsymbol{d}$ is a vector containing the average values of the switching signals applied to the converter (in other words, the duty ratios of the switching signals). The new state and

exogenous input vectors $\overline{\boldsymbol{x}}$ and $\overline{\boldsymbol{w}}$ approximate the local average quantities

$$\overline{\boldsymbol{x}} = \frac{1}{T_{\mathrm{s}}} \int_{t-T_{\mathrm{s}}}^{t} \boldsymbol{x}\left(\tau\right) d\tau \tag{2.5}$$

$$\overline{\boldsymbol{w}} = \frac{1}{T_{\mathrm{s}}} \int_{t-T_{\mathrm{s}}}^{t} \boldsymbol{w}\left(\tau\right) d\tau \tag{2.6}$$

under the conditions that: (a) the ripple in the state variables is small and has negligible impact on the behavior of the local average quantities; and (b) the local averages of switching signals and state variables vary sufficiently slowly with respect to the averaging interval T_{s}. For standard converters operating in CCM in particular, the local average values of state variables are much larger than the peak-to-peak ripples, and the first of these conditions is easily justified. The second condition is justified by the structure of the control loop in pulse-width modulated systems, namely the modulator that generates switching signals for the converter based on the controller output. Figure 2.1 illustrates the canonical structure of a PWM control loop with feedback of converter currents and voltages to a generic controller. The controller output is the modulating waveform $m(t)$ that is compared against carrier waveform $w(t)$ to produce the pulse-width modulated switching signal $s_1(t)$. The characteristics of the pulse-width modulator have been characterized in several works [33, 62, 63]. General small-signal characteristics of the pulse-width modulator are illustrated in Fig. 2.1 and summarized as follows: application of a small-signal perturbation at modulation frequency f_{m} to a dc modulating waveform results in a modulator output consisting of content at the modulation frequency and side-bands of the switching frequency f_{s}. If the modulation frequency is sufficiently low relative to the switching frequency, the frequency contents of the state variables are dominantly represented by baseband components as shown in Fig. 2.1. These baseband components are accurately captured by the averaging operator of (2.4) which has the frequency response characteristic shown in Fig. 2.2 [99].

Averaged modeling generally yields a nonlinear structure for $\boldsymbol{f}_{\mathbf{avg}}$. A final step of linearization is typically performed to obtain an equivalent model that approximates the converter behavior in a small-signal sense. Such analysis simplifies controller design through the use of well-established techniques developed for linear systems, and is valuable for evaluating controller performance, as it yields analytical expressions for closed-loop transient responses. Finally, linearization is an important tool used to evaluate the stability of the equilibrium operating point of the closed-loop system, particularly as a function of the controller design and converter operating point. The linearized model is obtained by evaluating the Jacobian matrices of $\boldsymbol{f}_{\mathbf{avg}}$ with respect to small-signal variations in the state variables and control inputs (duty ratios) at a quiescent state vector $\overline{\boldsymbol{x}_{\mathrm{e}}}$ and input vector $\boldsymbol{d}_{\mathrm{e}}$. It can be represented generally as

$$\dot{\tilde{\boldsymbol{x}}} = \boldsymbol{F} \cdot \tilde{\boldsymbol{x}} + \boldsymbol{G} \cdot \tilde{\boldsymbol{d}} \tag{2.7}$$

$$\boldsymbol{F} = \nabla_{\overline{\boldsymbol{x}}} \boldsymbol{f}_{\mathbf{avg}}|_{\overline{\boldsymbol{x}}=\overline{\boldsymbol{x}_{\mathrm{e}}}\,,\,\boldsymbol{d}=\boldsymbol{d}_{\mathrm{e}}} \tag{2.8}$$

$$\boldsymbol{G} = \nabla_{\boldsymbol{d}} \boldsymbol{f}_{\mathbf{avg}}|_{\overline{\boldsymbol{x}}=\overline{\boldsymbol{x}_{\mathrm{e}}}\,,\,\boldsymbol{d}=\boldsymbol{d}_{\mathrm{e}}} \tag{2.9}$$

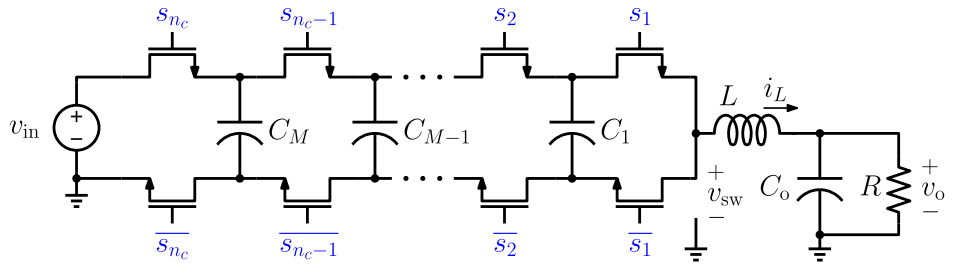


Figure 2.3: Schematic drawing of an N-level FCML converter with $n_c = N-1$ complementary switch pairs and $M = N-2$ flying capacitors.

where the notation $\nabla_{\bar{\boldsymbol{x}}} \boldsymbol{f}_{\mathbf{avg}}$ represents the Jacobian matrix of $\boldsymbol{f}_{\mathbf{avg}}$ evaluated with respect to vector $\bar{\boldsymbol{x}}$. In the following section, the principles of averaged modeling highlighted in this section will be applied to characterize an average plant model for active balancing control.

2.2 Averaged Plant Model for the FCML Converter

In the remainder of this work, for brevity of notation, an N-level FCML converter will be defined to have $n_c = N-1$ complementary switch pairs and $M = N-2$ flying capacitors as shown in Fig. 2.3. An N-level FCML converter with state variables labeled as shown in Fig. 2.3 is represented by the following dynamical equations

$$C_k \dot{v}_{c,k} = i_L \cdot (s_{k+1} - s_k) \qquad k \in 1, \ldots, M \tag{2.10}$$

$$L\dot{i}_L = v_{\text{in}} s_{n_c} - v_{\text{o}} + \sum_{k=1}^{M} v_{c,k} \cdot (s_k - s_{k+1}) \tag{2.11}$$

$$C_{\text{o}} \dot{v}_{\text{o}} = i_L - \frac{v_{\text{o}}}{R} \tag{2.12}$$

The impact of switching on the state dynamics is captured by switching functions $s_1, \ldots, s_{n_c}$ which will be treated as control inputs to the system. The capacitor voltages $v_{c,1}$,...,$v_{c,M}$, inductor current i_L, and output voltage v_{o} are the N state variables to be controlled. This section derives an averaged model for the FCML converter that can be used for active balancing control.

Applying the averaging operator of (2.4) to the dynamical equations in (2.10)–(2.12) describing the N-level FCML converter yields the system

$$C_k \dot{\overline{v_{c,k}}} = \overline{i_L} \cdot (d_{k+1} - d_k) \qquad k \in 1, \ldots, M \tag{2.13}$$

$$L\dot{\overline{i_L}} = \overline{v_{\text{in}}} \cdot d_{n_c} - \overline{v_o} + \sum_{k=1}^{M} \overline{v_{c,k}} \cdot (d_k - d_{k+1}) \tag{2.14}$$

$$C_o \dot{\overline{v_{\text{o}}}} = \overline{i_L} - \frac{\overline{v_o}}{R} \tag{2.15}$$

Note that as the expressions in (2.10)–(2.12) are bilinear with respect to the state variables and switching functions, the averaged model only captures the impact of the duty ratios d_k of the switching signals. As a consequence, active balancing controllers based on the averaged model can only act on the switch duty ratios. The averaged equation given in (2.13) predicts that when $d_{k+1} = d_k$ for all $k \in \{1, 2, \ldots, n_c\}$, the average current into every flying capacitor $v_{c,k}$ is zero. Recalling that this condition corresponds to symmetric PS-PWM, the averaged model does not predict the natural balancing behavior highlighted in Section 1.3 and detailed in [72–78]. However, when duty ratios are allowed to vary independently (i.e., $d_{k+1} \neq d_k$) the averaged model of (2.13) predicts nonzero average current into the capacitor. This motivates the investigation of active balancing controllers that adjust duty ratios independently depending on a negative feedback principle. To achieve the steady-state inductor current ripple characteristics described in Section 1.2, the balancing controller should generate equal duty ratios when capacitor voltages are balanced. When a capacitor voltage deviates from its nominal balanced value, the balancing controller should adjust duty ratios such that the average current into the capacitor corrects the error. The aforementioned assumptions underlie the subsequent analysis—state variables are assumed to have small ripple with respect to their average values and averaged quantities are assumed to vary slowly with respect to the averaging interval $T_\mathrm{s} = \frac{1}{f_\mathrm{s}}$.

The model of (2.13)-(2.15) fits the general form of (2.3) with the state vector defined as

$$\overline{\boldsymbol{x}} := \begin{bmatrix} \overline{v_{c,1}} & \overline{v_{c,2}} & \cdots & \overline{v_{c,M}} & \overline{i_L} & \overline{v_\mathrm{o}} \end{bmatrix}^\mathrm{T} \in \mathbb{R}^N \tag{2.16}$$

and the vector of duty ratios defined as

$$\boldsymbol{d} := \begin{bmatrix} d_1 & d_2 & \cdots & d_{n_c} \end{bmatrix}^\mathrm{T} \in \mathbb{R}^{n_c} \tag{2.17}$$

where $[\,\cdot\,]^\mathrm{T}$ denotes the matrix transpose. As a starting point for controller design, the nonlinear model in (2.13)–(2.15) is linearized at a quiescent dc operating point to study the small-signal dynamics of the averaged system. The quiescent state is vectorized as

$$\overline{\boldsymbol{x}_\mathbf{e}} := \begin{bmatrix} V_{c,1} & V_{c,2} & \cdots & V_{c,M} & I_L & V_\mathrm{o} \end{bmatrix}^\mathrm{T} \in \mathbb{R}^N \tag{2.18}$$

where

$$V_{c,k} := \frac{k}{n_c}\,\overline{v_\mathrm{in}} \tag{2.19}$$

and I_L and V_o represent the quiescent inductor current and output voltage respectively. The quiescent input consists of equal duty ratios D and is expressed as

$$\boldsymbol{d}_\mathbf{e} := \begin{bmatrix} D & D & \cdots & D \end{bmatrix}^\mathrm{T} \in \mathbb{R}^{n_c} \tag{2.20}$$

This choice of $\overline{\boldsymbol{x}_\mathbf{e}}$ and $\boldsymbol{d}_\mathbf{e}$ corresponds to the desired steady-state operating condition under symmetric PS-PWM with balanced capacitor voltages. The small-signal dynamics are given by

$$\dot{\tilde{\boldsymbol{x}}} = \boldsymbol{F} \cdot \tilde{\boldsymbol{x}} + \boldsymbol{G} \cdot \tilde{\boldsymbol{d}} \tag{2.21}$$

where

$$\boldsymbol{F} = \left[\begin{array}{ccc|cc} 0 & \cdots & 0 & 0 & 0 \\ 0 & \cdots & 0 & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & 0 & 0 \\ \hline 0 & \cdots & 0 & 0 & -\frac{1}{L} \\ 0 & \cdots & 0 & \frac{1}{C_\mathrm{o}} & -\frac{1}{RC_\mathrm{o}} \end{array}\right] \in \mathbb{R}^{N\times N} \tag{2.22}$$

$$\boldsymbol{G} = \left[\begin{array}{cccccc} \frac{-I_L}{C_1} & \frac{I_L}{C_1} & 0 & \cdots & 0 & 0 \\ 0 & \frac{-I_L}{C_2} & \frac{I_L}{C_2} & \cdots & 0 & 0 \\ \vdots & \ddots & \ddots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{-I_L}{C_M} & \frac{I_L}{C_M} \\ \frac{V_{c,1}}{L} & \frac{V_{c,2}-V_{c,1}}{L} & \frac{V_{c,3}-V_{c,2}}{L} & \cdots & \cdots & \frac{\overline{v_\mathrm{in}}-V_{c,M}}{L} \\ 0 & 0 & 0 & \cdots & \cdots & 0 \end{array}\right] \in \mathbb{R}^{N\times n_c} \tag{2.23}$$

The structure of the small-signal model reveals properties of the plant that may be used to derive the controller structure. From (2.22) it follows that the small-signal capacitor voltages, vectorized as $\tilde{\boldsymbol{v}}_{\boldsymbol{c}} := [\,\tilde{v}_{c,1} \;\; \cdots \;\; \tilde{v}_{c,M}\,]^\mathrm{T}$, and the small-signal inductor current $\tilde{i}_L$ are naturally decoupled, as the cross-coupling elements in $\boldsymbol{F}$ are zero. Thus $\tilde{\boldsymbol{v}}_{\boldsymbol{c}}$ and $\tilde{i}_L$ can be realized as the outputs of two separate sub-plants modeled as decoupled integrators, as shown in Fig. 2.4. Furthermore, the small-signal capacitor voltages are decoupled from each other, as the terms in the top-left block of $\boldsymbol{F}$ are all zero. Thus, the capacitor sub-plant can also be modeled internally as a system of decoupled integrators, shown in the expanded view in Fig. 2.4. It is emphasized that the block diagram in Fig. 2.4 is only valid in the averaged sense—the averaged analysis assumes that the ripple content of state variables do not significantly affect the dynamics of the averaged components. Section 2.5 examines the extent to which this assumption is true, and consequently, presents the limitations of active balancing controllers designed from averaged models.

Linear manipulation of (2.21) reveals the capacitor sub-plant is modeled by the dynamical matrix equation

$$\dot{\tilde{\boldsymbol{v}}}_{\boldsymbol{c}} = \boldsymbol{G}_{\boldsymbol{p},\boldsymbol{v_c}} \cdot \boldsymbol{\Delta}\tilde{\boldsymbol{d}} \tag{2.24}$$

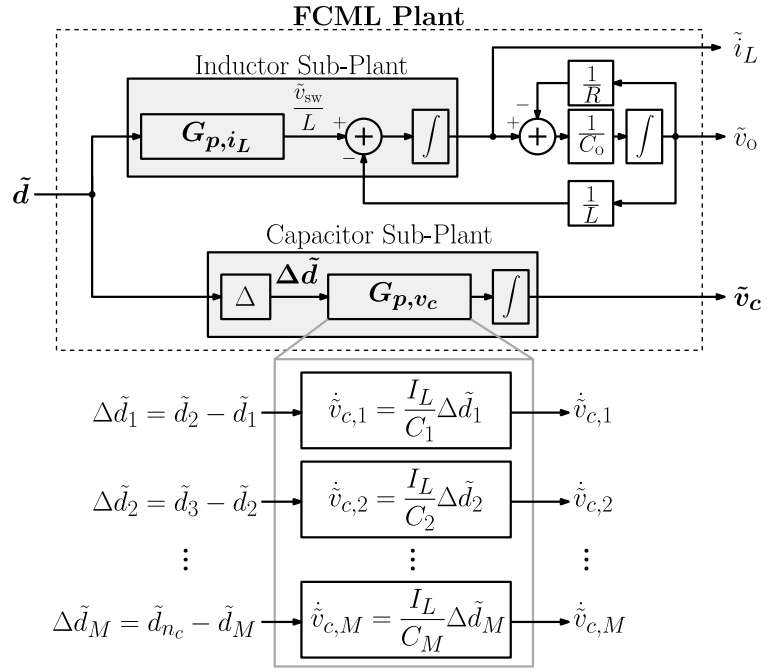


Figure 2.4: Block diagram of the small-signal averaged plant given in (2.21), highlighting the parallel inductor and capacitor sub-plants.

where

$$\boldsymbol{G_{p,v_c}} = \begin{bmatrix} \frac{I_L}{C_1} & 0 & \cdots & 0 \\ 0 & \frac{I_L}{C_2} & \ddots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{I_L}{C_M} \end{bmatrix} \in \mathbb{R}^{M\times M} \tag{2.25}$$

and $\boldsymbol{\Delta\tilde{d}}$ denotes a vector of difference variables Δd_k defined as

$$\boldsymbol{\Delta\tilde{d}} = \begin{bmatrix} \Delta\tilde{d}_1 \\ \Delta\tilde{d}_2 \\ \vdots \\ \Delta\tilde{d}_M \end{bmatrix} := \begin{bmatrix} \tilde{d}_2 - \tilde{d}_1 \\ \tilde{d}_3 - \tilde{d}_2 \\ \vdots \\ \tilde{d}_{n_c} - \tilde{d}_M \end{bmatrix} \in \mathbb{R}^M \tag{2.26}$$

The inductor sub-plant is modeled by

$$\dot{\tilde{i}}_L = \boldsymbol{G_{p,i_L}} \cdot \tilde{\boldsymbol{d}} - \frac{\tilde{v}_o}{L} \tag{2.27}$$

where

$$\boldsymbol{G_{p,i_L}} = \begin{bmatrix} \frac{V_{c,1}}{L} & \frac{V_{c,2}-V_{c,1}}{L} & \cdots & \frac{\overline{v_{in}}-V_{c,M}}{L} \end{bmatrix} \tag{2.28}$$

Each sub-plant responds to a different characteristic of the system inputs. The flying capacitor voltage dynamics are dependent on the differences of neighboring duty ratios Δd_k, shown in Fig. 2.4 as the output of a difference operator Δ. The inductor current responds to a weighted sum of duty ratios.

A key observation motivates the controller presented in this work: a common offset applied to all duty ratios does not affect the capacitor voltage dynamics. This common offset—henceforth referred to as the *common mode* duty ratio—is always rejected by the capacitor sub-plant, as it is eliminated by the differences of duty ratios in (2.24). The following decomposition illustrates this point. Let

$$\begin{aligned} \tilde{d}_1 &= \tilde{d}_{\mathrm{CM}} + \tilde{d}_{\mathrm{DM},1} \\ \tilde{d}_2 &= \tilde{d}_{\mathrm{CM}} + \tilde{d}_{\mathrm{DM},2} \\ &\vdots \\ \tilde{d}_{n_c} &= \tilde{d}_{\mathrm{CM}} + \tilde{d}_{\mathrm{DM},n_c} \end{aligned} \tag{2.29}$$

where d_{CM} is the common mode (offset) variable, and $d_{\mathrm{DM},k}$ indicates a *differential mode* variation added to it. Clearly,

$$\begin{aligned} \Delta\tilde{d}_1 &= \tilde{d}_2 - \tilde{d}_1 = \tilde{d}_{\mathrm{DM},2} - \tilde{d}_{\mathrm{DM},1} \\ \Delta\tilde{d}_2 &= \tilde{d}_3 - \tilde{d}_2 = \tilde{d}_{\mathrm{DM},3} - \tilde{d}_{\mathrm{DM},2} \\ &\vdots \\ \Delta\tilde{d}_M &= \tilde{d}_{n_c} - \tilde{d}_{n_c-1} = \tilde{d}_{\mathrm{DM},n_c} - \tilde{d}_{\mathrm{DM},n_c-1} \end{aligned} \tag{2.30}$$

Thus the controller in this work uses the common mode duty ratio to control current and the differential mode duty ratios to regulate the capacitor voltages. The common mode duty ratio is a sensible choice for controlling the inductor current as it does not affect the capacitor voltages. At the same time, the balancing controller determines the differences of duty ratios Δd_k that should be applied to steer capacitor voltages. The differential mode duty ratios can be constructed from these difference variables recursively, as will be discussed in Section 2.3. In this approach, both the capacitor balancing and output regulation objectives can be achieved independently.

One aspect of the control structure demands further study—from the perspective of the current controller, the difference variables set by the balancing controller add to the current control action as a disturbance. This disturbance will be studied and compensated in the design of the current controller.

Controllability of the Small-Signal System

The preceding discussion presents an intuitive argument that the parallel internal structure of the small-signal plant derived from the averaged model allows for simultaneous control of

both the capacitor voltages $\tilde{\boldsymbol{v}}_{\boldsymbol{c}}$ and the converter output states ($\tilde{i}_L$ and $\tilde{v}_{\mathrm{o}}$). The ability to completely specify the closed-loop dynamics of the N state variables using the $n_c = N-1$ duty ratio inputs can be shown more rigorously by evaluating the controllability of the small-signal system (2.21) using the techniques described in [101–103]. To demonstrate that (2.21) is completely controllable, consider an invertible transformation of the input vector given by

$$\tilde{\boldsymbol{\delta}} = \begin{bmatrix} \tilde{d}_2 - \tilde{d}_1 \\ \tilde{d}_3 - \tilde{d}_2 \\ \vdots \\ \tilde{d}_{n_c} - \tilde{d}_M \\ \tilde{d}_{n_c} \end{bmatrix} = \boldsymbol{T} \cdot \tilde{\boldsymbol{d}} \tag{2.31}$$

where

$$\boldsymbol{T} := \begin{bmatrix} -1 & 1 & 0 & \cdots & 0 & 0 \\ 0 & -1 & 1 & \ddots & \vdots & \vdots \\ \vdots & \ddots & \ddots & \ddots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & -1 & 1 \\ 0 & 0 & 0 & \cdots & 0 & 1 \end{bmatrix} \tag{2.32}$$

The small-signal system (2.21) expressed with respect to the new vector $\tilde{\boldsymbol{\delta}}$ is

$$\dot{\tilde{\boldsymbol{x}}} = \boldsymbol{F} \cdot \tilde{\boldsymbol{x}} + \hat{\boldsymbol{G}} \cdot \tilde{\boldsymbol{\delta}} \tag{2.33}$$

where

$$\hat{\boldsymbol{G}} = \boldsymbol{T}^{-1} \cdot \boldsymbol{G} \tag{2.34}$$

The system (2.33) and consequently (2.21) are completely controllable if the accompanying *controllability matrix* $\mathcal{C}$, given by

$$\mathcal{C} := \begin{bmatrix} \hat{\boldsymbol{G}} & \boldsymbol{F} \cdot \hat{\boldsymbol{G}} & \boldsymbol{F}^2 \cdot \hat{\boldsymbol{G}} & \cdots & \boldsymbol{F}^{N-1} \cdot \hat{\boldsymbol{G}} \end{bmatrix} \tag{2.35}$$

has rank N. From (2.23), $\hat{\boldsymbol{G}}$ is given by

$$\hat{\boldsymbol{G}} = \begin{bmatrix} \frac{I_L}{C_1} & 0 & 0 & \cdots & 0 & 0 \\ 0 & \frac{I_L}{C_2} & 0 & \cdots & 0 & 0 \\ \vdots & \ddots & \ddots & \ddots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{I_L}{C_M} & 0 \\ \frac{-V_{c,1}}{L} & \frac{-V_{c,2}}{L} & \frac{-V_{c,3}}{L} & \dots & \frac{-V_{c,M}}{L} & \frac{\overline{v_{\mathrm{in}}}}{L} \\ 0 & 0 & 0 & \cdots & 0 & 0 \end{bmatrix} \tag{2.36}$$

and has $n_c = N - 1$ linearly independent rows. Matrix $\boldsymbol{F} \cdot \hat{\boldsymbol{G}}$ is

$$\boldsymbol{F} \cdot \hat{\boldsymbol{G}} = \begin{bmatrix} 0 & 0 & 0 & \cdots & 0 & 0 \\ 0 & 0 & 0 & \cdots & 0 & 0 \\ \vdots & \ddots & \ddots & \ddots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 0 & 0 \\ 0 & 0 & 0 & \cdots & 0 & 0 \\ -\frac{V_{c,1}}{LC_\mathrm{o}} & -\frac{V_{c,2}}{LC_\mathrm{o}} & -\frac{V_{c,3}}{LC_\mathrm{o}} & \cdots & -\frac{V_{c,M}}{LC_\mathrm{o}} & \frac{\overline{v_\mathrm{in}}}{LC_\mathrm{o}} \end{bmatrix} \tag{2.37}$$

From (2.36) and (2.37) it is clear that $\mathcal{C}$ has rank N, therefore the small-signal system is completely controllable. An immediate result of complete controllability is that averaged capacitor voltage dynamics, which are predicted by the open-loop model to be zero, can be specified by the design of the closed-loop controller. The following section outlines a controller structure that allows for the independent specification of the closed-loop behavior of the capacitor voltages and output states. In particular, it will be shown that the capacitor voltages can be decoupled from the inductor current through the appropriate controller structure.

2.3 Parallel Controller Structure

The following section introduces a control structure where a separate balancing and current controller operate in parallel and their outputs are summed. The balancing controller comprises an internal model controller (IMC) that sets differences of duty ratios Δd_k to balance each flying capacitor voltage with a designed closed-loop bandwidth while decoupling the capacitor voltage dynamics. Differences of neighboring duty ratios are summed to obtain a vector of the balancing contributions to each duty ratio, $\boldsymbol{d}_{\mathbf{bal}} = [d_{\mathrm{bal},1} \ \cdots \ d_{\mathrm{bal},n_c}]^\mathrm{T}$. The current controller sets a scalar value d_curr applied equally to every duty ratio. Thus, the current controller computes the common mode duty ratio $d_\mathrm{CM} = d_\mathrm{curr}$ and the balancing controller computes the differential mode duty ratios $\boldsymbol{d}_{\mathbf{bal}} = [d_{\mathrm{DM},1} \ \cdots \ d_{\mathrm{DM},n_c}] = \boldsymbol{d}_{\mathbf{DM}}$. Using the notation $\mathbf{1} = [1 \ \cdots \ 1]^\mathrm{T}$, the net control action is expressed as

$$\begin{aligned} \boldsymbol{d} &= \boldsymbol{d}_{\mathbf{bal}} + d_\mathrm{curr} \cdot \mathbf{1} \\ &= \begin{bmatrix} d_{\mathrm{bal},1} + d_\mathrm{curr} \\ d_{\mathrm{bal},2} + d_\mathrm{curr} \\ \vdots \\ d_{\mathrm{bal},n_c} + d_\mathrm{curr} \end{bmatrix} \end{aligned} \tag{2.38}$$

The proposed *parallel controller* is shown in Fig. 2.5. The Σ block in the balancing controller and the Δ block in the capacitor voltage path of the plant represent sum and

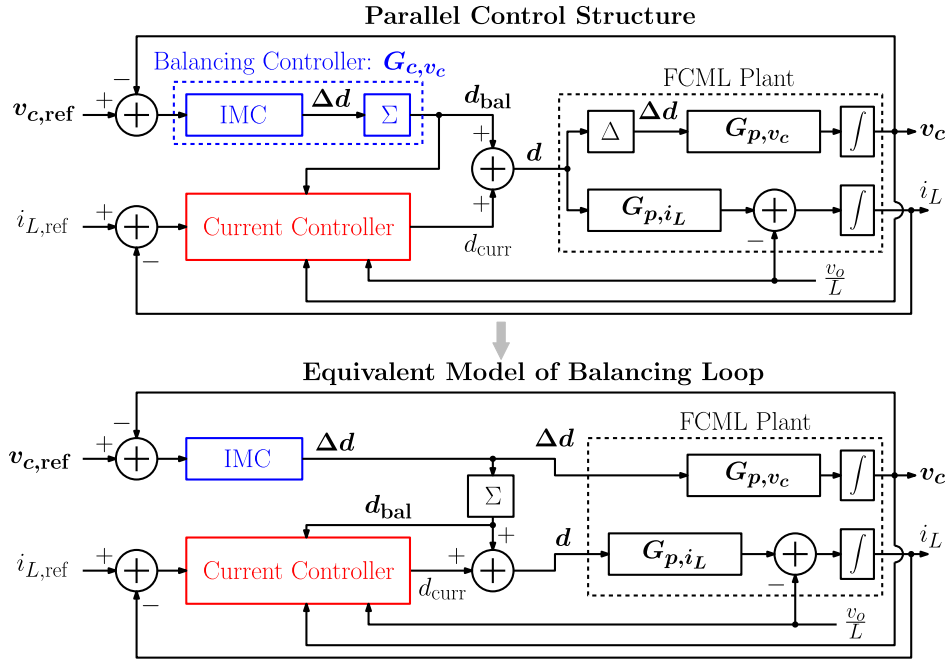


Figure 2.5: Parallel control structure and an equivalent model of the controller. The flying capacitor plant naturally rejects the common duty ratio term d_{curr} applied to all switches, as shown in the equivalent model.

difference operations on neighboring duty ratios respectively, and will be detailed in the following analysis. The common mode duty ratio computed for current control, $d_{\text{CM}} = d_{\text{curr}}$, is rejected by the capacitor sub-plant, so the closed-loop system can be represented by an equivalent model, also shown in Fig. 2.5. By contrast, the differential mode duty ratios computed for balancing, $\boldsymbol{d}_{\mathbf{DM}} = \boldsymbol{d}_{\mathbf{bal}}$, are not rejected by the inductor sub-plant, so the current controller must be designed to reject disturbances injected by the balancing controller.

Balancing Controller

Recalling that the small-signal capacitor sub-plant is a MIMO system that is already represented by decoupled integrators, the balancing controller should be designed such that the capacitor dynamics remain decoupled in the closed-loop system. This ensures that the control action taken to steer one flying capacitor voltage does not disturb the others. The principle of internal model control [104] is used to ensure this decoupling.

In general, if the matrix input-output description of a linear system is square and invertible, an internal model controller (IMC) is designed by multiplying the inverse of the plant model by a diagonal system consisting of integrators. As the matrix $\boldsymbol{G}_{\boldsymbol{p},\boldsymbol{v_c}}$ in (2.25) is diagonal, the capacitor sub-plant in (2.24) can be expressed through the Laplace transform

as

$$\boldsymbol{v_c}(s) = \frac{1}{s} \cdot \boldsymbol{G_{p,v_c}} \cdot \boldsymbol{\Delta d}(s) \tag{2.39}$$

The IMC design procedure detailed in [104] aims to design a controller matrix for this system such that the loop transfer matrix of the system is diagonal and consists of integrator elements. In this sense, internal model control seeks to decouple the closed-loop responses of capacitor voltages. Such an approach is particularly interesting in the system studied as the plant model of (2.39) already consists of decoupled capacitor voltages. Thus, application of the IMC design procedure to the capacitor sub-plant in (2.39) results in a diagonal-matrix proportional controller where the bandwidths of the channels can be set independently via each channel's proportional gain. This controller is given by

$$\boldsymbol{G_{\mathbf{IMC}}} = \begin{bmatrix} \omega_1 \frac{C_1}{I_L} & 0 & \cdots & 0 \\ 0 & \omega_2 \frac{C_2}{I_L} & \ddots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \omega_M \frac{C_M}{I_L} \end{bmatrix} \tag{2.40}$$

where ω_k is the designed bandwidth for capacitor k. The corresponding loop transfer matrix, obtained via the Laplace transform, is diagonal with integrator elements and given by

$$\boldsymbol{L_{v_c}} = \begin{bmatrix} \frac{\omega_1}{s} & 0 & \cdots & 0 \\ 0 & \frac{\omega_2}{s} & \ddots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{\omega_M}{s} \end{bmatrix} \tag{2.41}$$

The difference variables $\boldsymbol{\Delta d}$ computed by the IMC must somehow be applied to the n_c differential mode duty ratios $\boldsymbol{d_{\mathbf{DM}}}$ such that the balancing actions for flying capacitors do not interfere with each other. Since there is one more control variable compared to the number of capacitors (i.e., $M = n_c - 1$), $d_{\text{bal},1} = 0$ is chosen, as it does not disturb the current control action. With the value for $d_{\text{bal},1}$ fixed, the balancing controller action $\boldsymbol{d_{\mathbf{bal}}}$ may be computed via back-substitution, which is computationally efficient and readily implemented in digital signal processors (DSPs). The small-signal balancing controller $\boldsymbol{G_{c,v_c}}$ in Fig. 2.5 is given by

$$\begin{bmatrix} \tilde{d}_{\text{bal},1} \\ \tilde{d}_{\text{bal},2} \\ \vdots \\ \tilde{d}_{\text{bal},n_c-1} \\ \tilde{d}_{\text{bal},n_c} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \cdots & 0 \\ \frac{\omega_1 C_1}{I_L} & 0 & 0 & \cdots & 0 \\ \frac{\omega_1 C_1}{I_L} & \frac{\omega_2 C_2}{I_L} & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ \frac{\omega_1 C_1}{I_L} & \frac{\omega_2 C_2}{I_L} & \frac{\omega_3 C_3}{I_L} & \cdots & \frac{\omega_M C_M}{I_L} \end{bmatrix} \cdot \begin{bmatrix} \tilde{e}_{v_{c,1}} \\ \tilde{e}_{v_{c,2}} \\ \vdots \\ \vdots \\ \tilde{e}_{v_{c,M}} \end{bmatrix} \tag{2.42}$$

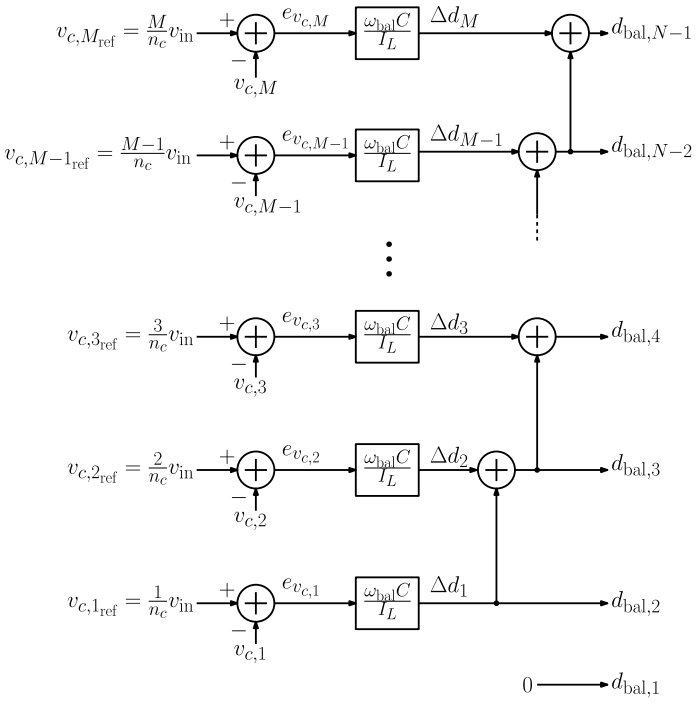


Figure 2.6: Block diagram representation of the balancing controller given in (2.42).

where the small-signal feedback error for capacitor voltages is vectorized as

$$\tilde{\boldsymbol{e}}_{\boldsymbol{v_c}} := \begin{bmatrix} \tilde{e}_{v_{c,1}} \\ \tilde{e}_{v_{c,2}} \\ \vdots \\ \tilde{e}_{v_{c,M}} \end{bmatrix} = \begin{bmatrix} \tilde{v}_{c,1_{\text{ref}}} - \tilde{v}_{c,1} \\ \tilde{v}_{c,2_{\text{ref}}} - \tilde{v}_{c,2} \\ \vdots \\ \tilde{v}_{c,M_{\text{ref}}} - \tilde{v}_{c,M} \end{bmatrix} \tag{2.43}$$

The balancing controller of (2.42) is visualized as a block diagram in Fig. 2.6. The propagation from Δd_k to $d_{\text{bal},1}$ is straightforward to implement as a recursive computation in a modern digital controller. To illustrate the active balancing control action as time-domain waveforms, a scenario with imbalanced capacitor voltages is shown in Fig. 2.7 over the timescale of a switching period T_{s}. Note the underlying assumptions in this work: the average flying capacitor voltages vary slowly relative to the switching period, and the capacitor voltage ripples are small with respect to their average values. The errors associated with each flying capacitor voltage are indicated by arrows, where the reference values are the nominal fractions of the supply voltage $\overline{v_{\text{in}}}$, indicated by the red lines. Figure 2.8 shows the corresponding control action to steer these example capacitor voltage errors to zero. The difference variables Δd_k are applied recursively to each switching signal beginning with $d_1 = d_{\text{curr}}$.

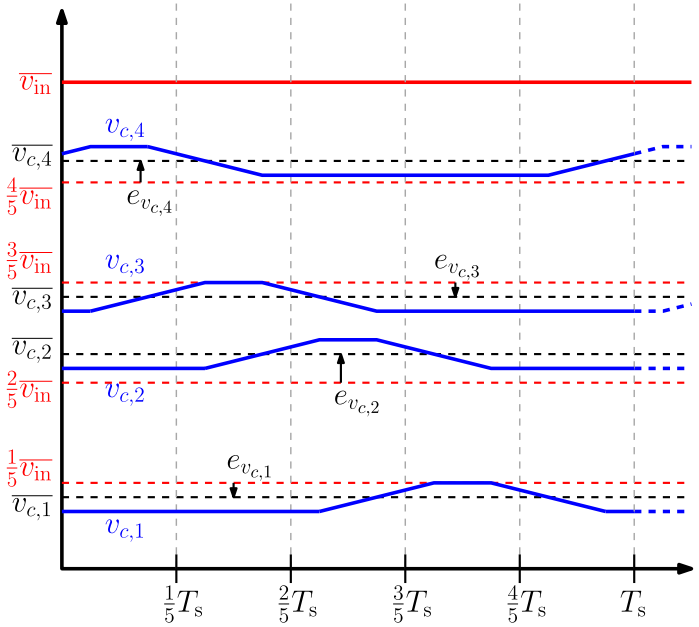


Figure 2.7: Example imbalanced capacitor voltages, shown in a timescale of one switching period. The reference capacitor voltages are respective nominal fractions of the input voltage, $\frac{k}{n_c}V_{\text{in}}$, shown as red lines. The signed errors associated with imbalanced voltages are indicated by arrows.

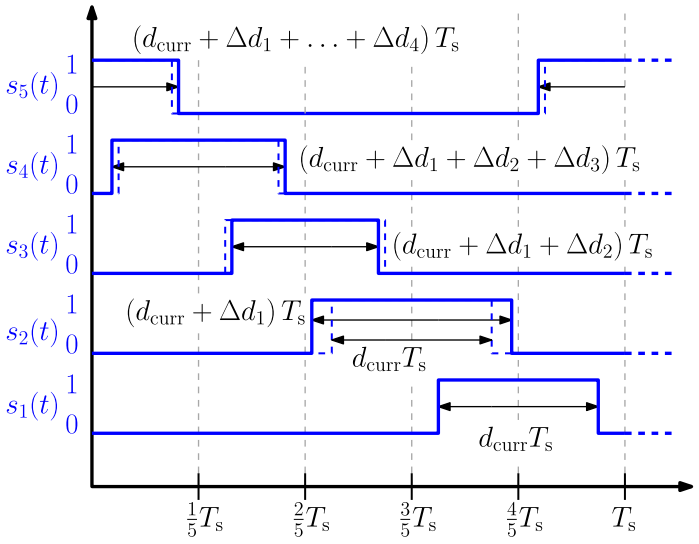


Figure 2.8: Example duty ratios applied to each switch resulting from simultaneous current control and active balancing actions. The balancing actions appear as difference duty ratios Δd_k, applied recursively to each switch beginning with $d_1 = d_{\text{curr}}$. The pulse width corresponding to the common-mode duty ratio d_{curr} is shown via dashed lines.

In implementation, the balancing controller in (2.42) may be adapted to remove the quiescent-point dependence on I_L. In the prototype implemented in this work and demonstrated in Section 2.4, the denominator terms I_L are replaced with the current reference $i_{L,\text{ref}}$ to eliminate the dependence of the active balancing closed-loop bandwidth on the load current. Further adaptive measures may be considered to remove the controller's dependence on converter parameters. For example, in converters incorporating Class II dielectrics for the flying capacitors, the capacitance values will change dramatically as a nonlinear function of the supply voltage. If the supply voltage is expected to have large-signal variations, the capacitance terms in (2.42) may be updated dynamically with a modeled voltage-controlled capacitance characteristic.

Current Controller

From inspection of (2.27), the inductor current clearly responds to a linear combination of the duty ratios. Using the control input decomposition of (2.38), the dynamics in (2.27) can be re-expressed as

$$\dot{\tilde{i}}_L = \boldsymbol{G_{p,i_L}} \cdot \left(\tilde{\boldsymbol{d}}_{\mathbf{bal}} + \tilde{d}_{\text{curr}} \cdot \mathbf{1} \right) - \frac{\tilde{v}_{\text{o}}}{L} \tag{2.44}$$

Recalling that the small-signal model is derived with respect to the equilibrium point (2.18) consisting of balanced capacitor voltages, (2.44) can be simplified as

$$\dot{\tilde{i}}_L = \frac{1}{L} \left(\overline{v_{\text{in}}} \cdot \tilde{d}_{\text{curr}} - \tilde{v}_{\text{o}} + \frac{\overline{v_{\text{in}}}}{n_c} \cdot \mathbf{1}^{\text{T}} \cdot \tilde{\boldsymbol{d}}_{\mathbf{bal}} \right) \tag{2.45}$$

The first two terms in small-signal dynamics (2.45) are identical to the small-signal current dynamics in the standard two-level buck converter. The final term arises from the balancing controller action $\boldsymbol{d}_{\mathbf{bal}}$ and acts as a disturbance to the current control loop. This disturbance term, however, is not exogenous to the system—it arises from the balancing controller implemented in parallel with the current controller. Assuming that the current controller can measure the balancing control action $\boldsymbol{d}_{\mathbf{bal}}$ (a reasonable assumption if both controllers are implemented on the same processor) the current control action can compensate the balancing control disturbance. The linear control law

$$\tilde{d}_{\text{curr}} = \frac{1}{\overline{v_{\text{in}}}} \left(\tilde{u} + \tilde{v}_{\text{o}} - \frac{\overline{v_{\text{in}}}}{n_c} \mathbf{1}^{\text{T}} \cdot \tilde{\boldsymbol{d}}_{\mathbf{bal}} \right) \tag{2.46}$$

compensates the balancing control disturbance, the disturbance impact of the small-signal output voltage, and the contribution of the input voltage, yielding the net small-signal dynamics

$$\dot{\tilde{i}}_L = \frac{1}{L} \tilde{u} \tag{2.47}$$

Note that with the control law of (2.46), the equivalent small-signal plant for current controls is a first-order system with respect to a new input $\tilde{u}$. Standard linear control techniques

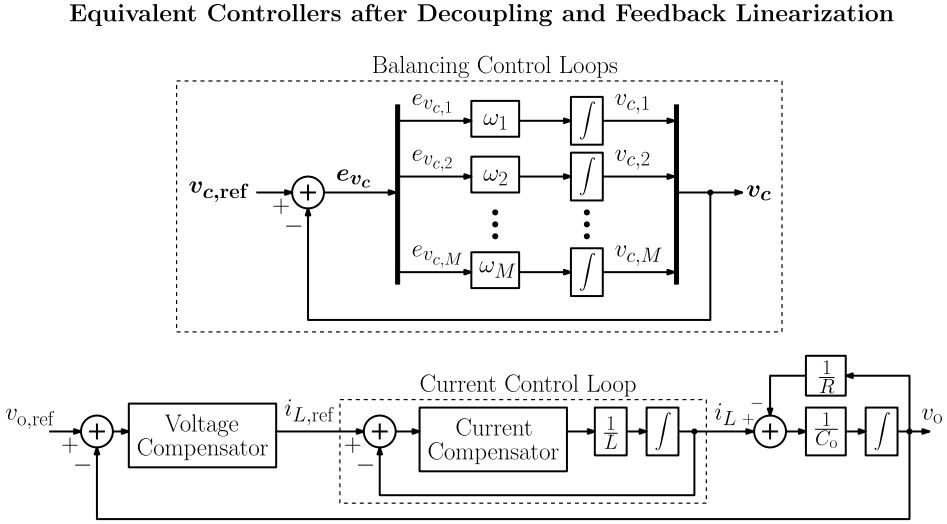


Figure 2.9: Equivalent closed-loop system after feedback linearization of the current dynamics. To ensure the balancing disturbance is rejected in practice, the current controller bandwidth should be chosen to be significantly higher than the balancing control bandwidth.

can be employed to compensate this new plant, which now remains fixed as the converter operating point varies. A typical choice in average current control is to employ a proportional-integral (PI) compensator [62] for the current controller, yielding the final linear control law

$$u = K_p e_{i_L} + K_i \int_{-\infty}^{t} e_{i_L} d\tau \tag{2.48}$$

$$e_{i_L} = i_{L,\mathrm{ref}} - i_L \tag{2.49}$$

The procedure outlined above to compensate the disturbance impact of the balancing control action on the average inductor current dynamics follows the principles of *feedback linearization* as outlined in [97, 105, 106]. From the perspective of the inductor current dynamics, the disturbance impacts of other state variables are easy to negate assuming those states are sensed. The current control law can also be obtained via direct application of the feedback linearization concept to the nonlinear average current dynamics in (2.14). Compared to a controller derived from the small-signal model, the resulting nonlinear current controller can compensate the balancing disturbance effectively for large-signal variations in the capacitor voltages.

With the substitution $d_k = d_{\mathrm{bal},k} + d_{\mathrm{curr}}$, the dynamical system given by (2.14) can be re-expressed as

$$L\dot{\overline{i_L}} = \overline{v_\mathrm{in}} d_{\mathrm{curr}} + \alpha - \overline{v_\mathrm{o}} \tag{2.50}$$

where

$$\alpha = \overline{v_{c,1}} d_{\mathrm{bal},1} + \left(\overline{v_{c,2}} - \overline{v_{c,1}}\right) d_{\mathrm{bal},2} + \cdots + \left(\overline{v_\mathrm{in}} - \overline{v_{c,M}}\right) d_{\mathrm{bal},n_c} \tag{2.51}$$

The corresponding state feedback control law

$$d_{\text{curr}} = \frac{1}{\overline{v_{\text{in}}}} u - \frac{\alpha - \overline{v_{\text{o}}}}{\overline{v_{\text{in}}}} \tag{2.52}$$

linearizes the response of $\overline{i_L}$ with respect to a new input u. This input can then set by a feedback control law such as (2.49).

To ensure that the disturbance impacts of the balancing actions on the inductor current are rejected effectively in practice considering delays and errors in sampling the capacitor voltages, the closed-loop bandwidth of the current controller should be greater than that of the balancing controller. In this section, a PI compensator is used to eliminate steady-state error for dc load current references, but other structures for the current loop feedback compensator can also be considered. Depending on the converter application and the expected forms of current references, the feedback compensator can easily be replaced by other designs that offer improved performance.

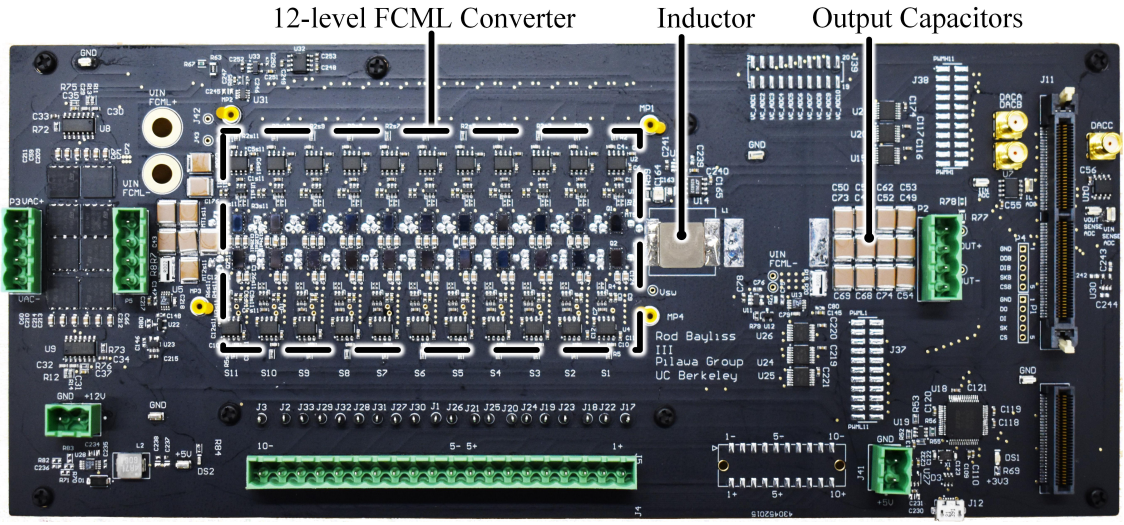


Figure 2.10: 12-Level FCML converter prototype with $L = 10\,\mu$H, $C_k = 8.8\,\mu$F, $f_s = 100\,$kHz. The parallel controller is implemented on a Texas Instruments TMS320F28379D DSP. The hardware is reconfigured as a 6-level FCML converter by shorting input-side switch pairs.

Table 2.1: Component Details

Component	Description	Part Name
S_{1-5A}, S_{1-5B}	100 V, 1.8 mΩ GaN-FET	EPC2302
C_{1-4}	$4 \times 2.2\,\mu$F, X6S, 450V	C5750X6S2W225K250KA
C_o	$20 \times 2.2\,\mu$F, X6S, 450V	C5750X6S2W225K250KA
L	$10\,\mu$H	IHLP5050CEER100M01
Gate Driver	5 V, 7.6 A / 1.3 A	LM5114
Isolator	Power and Signal	ADUM5240
Cap. Voltage Sensor	Instrumentation Amplifier	AD8429ARZ-R7
Current Sensor	Current Sense Amplifier	LT1999IMS8-20

2.4 Experimental Verification of Active Balancing Controller

A 12-level FCML converter hardware prototype, shown in Fig. 2.10 is constructed to verify the proposed parallel controller. Key component details and part numbers are given in Table 2.1. The hardware is configured as a 6-level FCML converter by bypassing switch pairs on the input side. The flying capacitor voltages are measured directly using M on-board differential voltage sensors, however a capacitor voltage estimator such as the one presented in [64] could be considered to simplify the hardware design and reduce cost. The inductor current is measured through a shunt resistor and amplifier circuit. To validate its practical utility, the parallel controller is implemented on a Texas Instruments TMS320F28379D DSP. The proposed implementation is similar in cost and complexity to the work of [107], which relies on direct capacitor voltage sensing and TMS320x DSP implementation. The work in [108] presents an implementation with a single sensor reducing component count, but the controller is implemented on expensive DSPACE FPGA hardware and its structure does not offer a decoupled response. The method presented in [50] is only developed for 3-level converters, and is not cost-effective for DSP implementation as it requires high-speed computation and positioning of switching edges. The controller proposed in this chapter is implemented on a single core of the DSP with single-sampled single-update PS-PWM [52]. The control law calculation for both the current controller and active balancing controller is timed in experiments and runs in approximately 7.5 μs. Thus, the proposed parallel controller can be executed once per switching period with $f_\mathrm{s} = 100\,\mathrm{kHz}$.

Three experiments—a supply transient measurement, a measurement of the converter response to periodic perturbation of the supply voltage, and a load transient measurement—are conducted to compare the performance of an FCML converter relying on natural balancing to one implementing the proposed parallel controller. The experiments verify that capacitor voltage tracking is significantly improved with active balancing for fast variations in the line voltage. A stiff output voltage generated by a large bulk output capacitance is used to simplify the current controller design, as the output voltage dynamics are not of interest. This setup is representative of an FCML converter feeding a stiff bus, as in the case of a rectifier in an electric vehicle onboard charger or first-stage dc-dc converter in a datacenter setting.

Supply Voltage Transient Response

The first experiment compares balancing responses for a damped-step transient in the supply voltage. The desired capacitor voltages—corresponding to nominal fractions of the input voltage—are overlaid as reference values alongside the measured results. A current controller designed for 10 kHz control bandwidth regulates the output current to 3 A during an input voltage transient from 50 V to 90 V. As seen in Fig. 2.11a, when the controller relies on natural balancing, the flying capacitor voltages exhibit oscillations which introduce unequal voltage stress across the switches in the converter. Capacitor voltage oscillations also couple

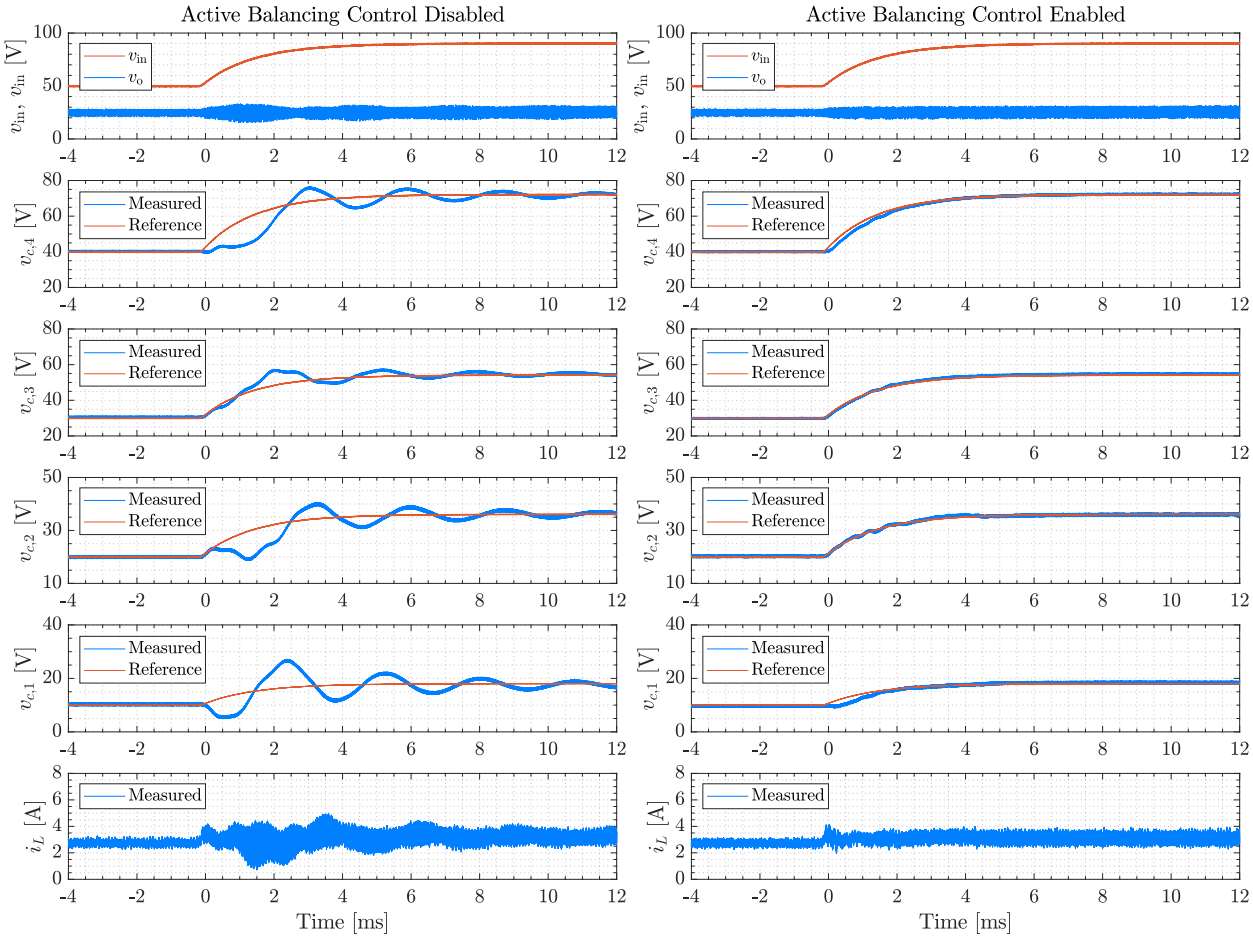


Figure 2.11: (a) Measured capacitor voltage and inductor current response of a current-controlled converter relying on natural balancing when supply voltage is changed from 50 V to 90 V. The capacitor voltages exhibit underdamped dynamics, resulting in unequal switch voltage stress. (b) Measured response of a converter implementing the proposed parallel active balancing controller. The capacitor voltages track the reference values with negligible error compared to the natural balancing case. In both cases, the current control bandwidth is set to 10 kHz, and the current reference $i_{L,\text{ref}} = 3$ A. The active balancing control bandwidth is set to 600 Hz for each flying capacitor.

into the current response in the form of increased harmonic content and peak-to-peak ripple. In contrast, active balancing designed for 600 Hz control bandwidth significantly improves voltage tracking, as seen in Fig. 2.11b, and the inductor current is significantly less disturbed, exhibiting approximately 50% lower peak deviation during the balancing transient.

Periodic Supply Voltage Perturbation

The second experiment shows the improved voltage tracking with active balancing when the converter is subjected to large-signal periodic input voltage perturbations similar to the twice-line-frequency variations present in converters fed by a rectified single-phase ac supply [109]. A current controller with 10 kHz control bandwidth regulates the output current to 2 A during the periodic perturbation. Figure 2.12a illustrates that the capacitor voltage tracking is poor when the system relies entirely on natural balancing, as the natural dynamics are too slow for capacitor voltages to track fast variations in the input voltage. This finding is consistent with open-loop audiosusceptibility characterizations in [77]. Active balancing once again significantly improves voltage tracking, shown in Fig. 2.12b. Here the specified balancing bandwidth is 300 Hz for all capacitors.

With active balancing, the maximum observed device voltage stress V_{ds} over the perturbation period decreases as a consequence of better capacitor voltage tracking. The maximum stress observed in the natural and active balancing cases is measured and characterized in Fig. 2.13 as a function of the supply perturbation frequency. The maximum measured voltage stress is normalized to the maximum stress expected at the peaks of the input perturbations to obtain a normalized stress metric defined as

$$\max V_{\mathrm{ds,norm}} := \frac{\max V_{\mathrm{ds}}}{\max \frac{v_{\mathrm{in}}}{n_c}} \tag{2.53}$$

Actively balanced systems featuring two different designed balancing bandwidths are studied and compared to the natural balancing case. For both active balancing designs, with perturbation frequencies within the controller bandwidths, the maximum observed device voltage stress is consistently smaller compared to the design relying on natural balancing. In the frequency ranges studied, the higher bandwidth active balancing design enables higher fidelity tracking of capacitor voltages, yielding the lowest normalized stress. The lower normalized stress with active balancing control indicates that in general, switching devices in FCML converters employing active balancing do not need to be significantly over-rated relative to the nominal blocking voltage stress. The proposed active balancing strategy therefore ensures safe operation of FCML converters designed with low-voltage switches.

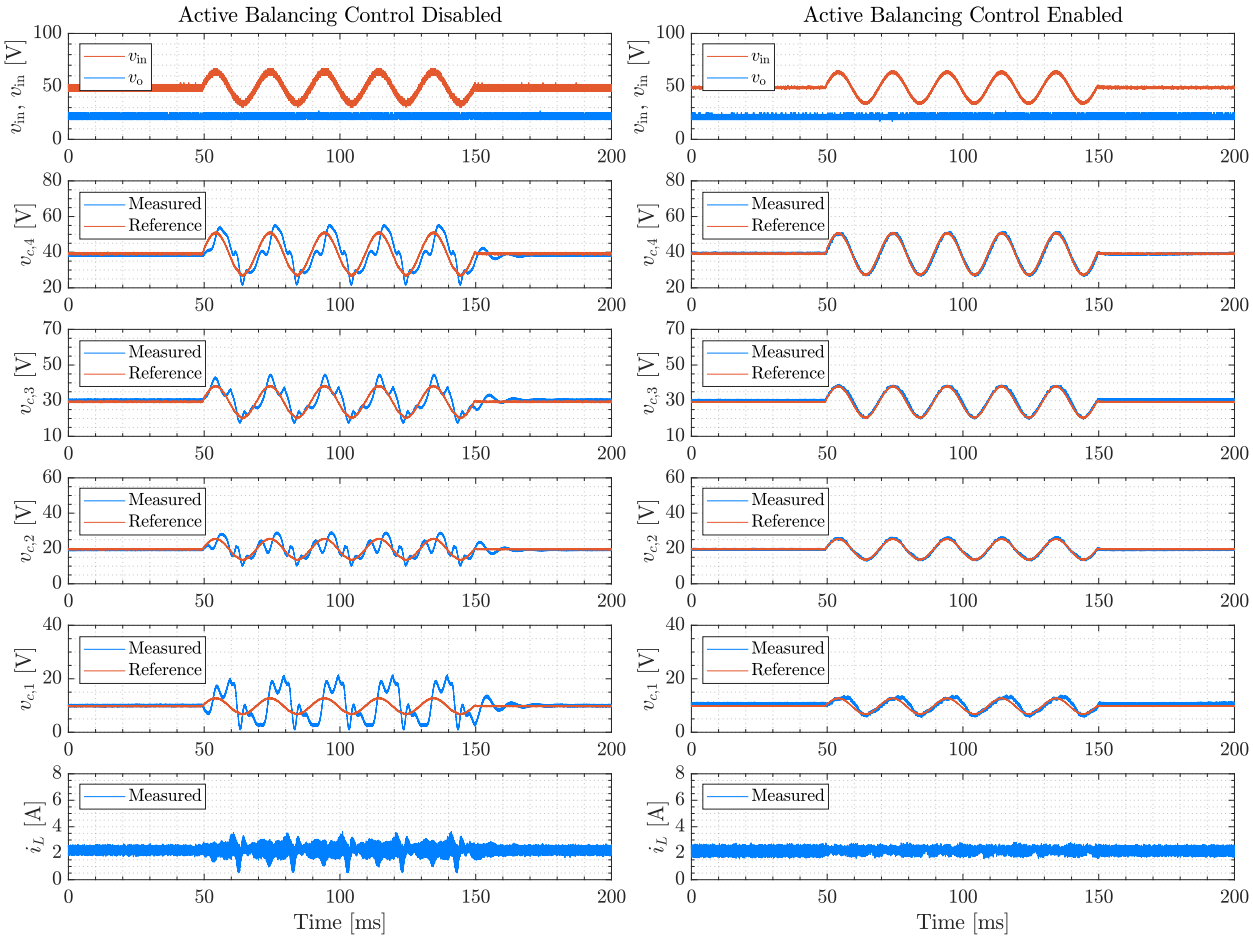


Figure 2.12: (a) Measured response of a current-controlled converter relying on natural balancing when a 50 Hz, 10 V_{RMS} ac perturbation is applied to the supply voltage. The capacitor voltages do not track their respective reference values as the natural balancing dynamics are not sufficiently fast. (b) Measured response of a converter implementing the proposed parallel active balancing controller. The capacitor voltage tracking is significantly improved and the disturbance to the inductor current is reduced. In both cases, the current control bandwidth is set to 10 kHz, and the current reference $i_{L,\text{ref}} = 2$ A. The active balancing control bandwidth is set to 300 Hz for each flying capacitor.

Comparing the time-domain responses in Fig. 2.12a and 2.12b, the inductor current response also improves with active balancing, as the input perturbation and capacitor voltage variations are noticeably decoupled from the current ripple. The coupling between the line voltage variation and the inductor current waveform can be analyzed via a harmonic distortion metric defined as

$$k_{\text{dist}} := \frac{\text{RMS}\left(i_L - I_{L,\text{ref}}\right)}{I_{L,\text{DC}}} \tag{2.54}$$

This metric quantifies the power of the disturbed inductor current waveform relative to its dc value. This current distortion number is plotted in Fig. 2.14 as a function of the supply perturbation frequency. As the perturbation frequencies increase, the capacitor voltage tracking degrades, and the harmonic content in the inductor current generally increases due to nonidealities in the implemented feedback linearized current controller. In general, the current distortion is lower with the proposed active balancing controller compared to the current-controlled converter relying on natural balancing, indicating better decoupling in the actively balanced system compared to the naturally balanced one. For converters interfaced to dc buses with low-frequency voltage ripple such as those in single-phase inverter or rectifier systems, lower value of the distortion metric k_{dist} enables more efficient converter operation owing to lower RMS inductor current and consequently lower conduction loss. In ac applications, the reduced harmonic distortion in the inductor current improves power quality compared to the converter relying on natural balancing. This motivates active balancing control even when capacitor voltage deviations do not cause excessive switch voltages.

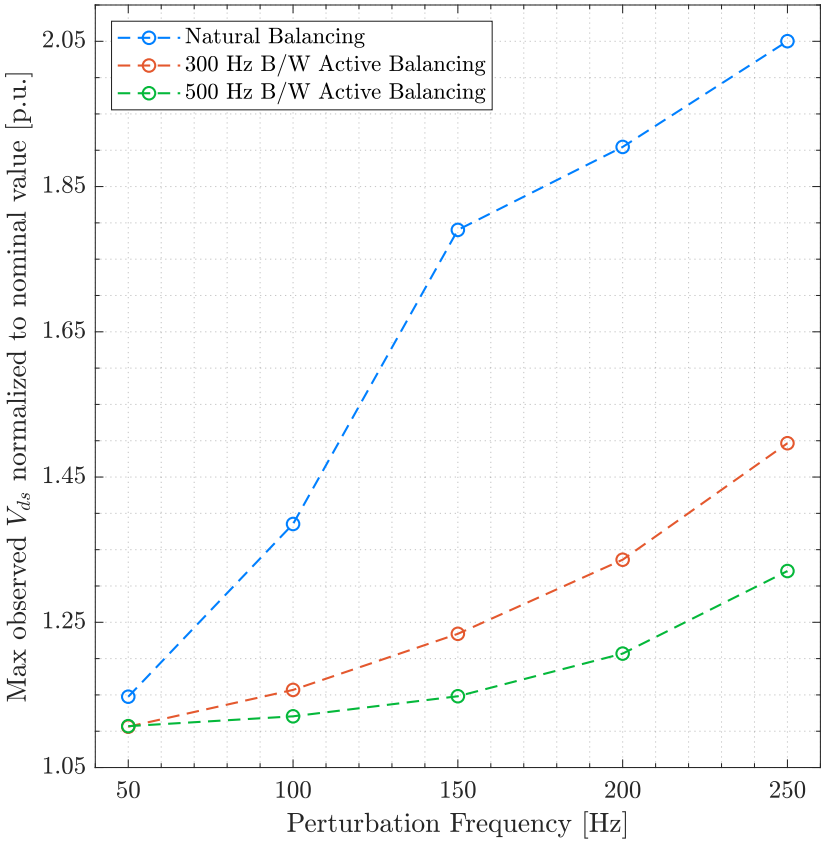


Figure 2.13: Maximum normalized device voltage stress V_{ds} given by (2.53), plotted against the supply perturbation frequency for a current-controlled converter relying on natural versus active balancing. A $10\,\mathrm{V_{RMS}}$ perturbation is applied on top of a nominal 50 V dc supply voltage. The current control bandwidth is set to 5 kHz and two different active balancing control bandwidths are studied, 300 Hz and 500 Hz. The device voltage stress is consistently lower under active balancing.

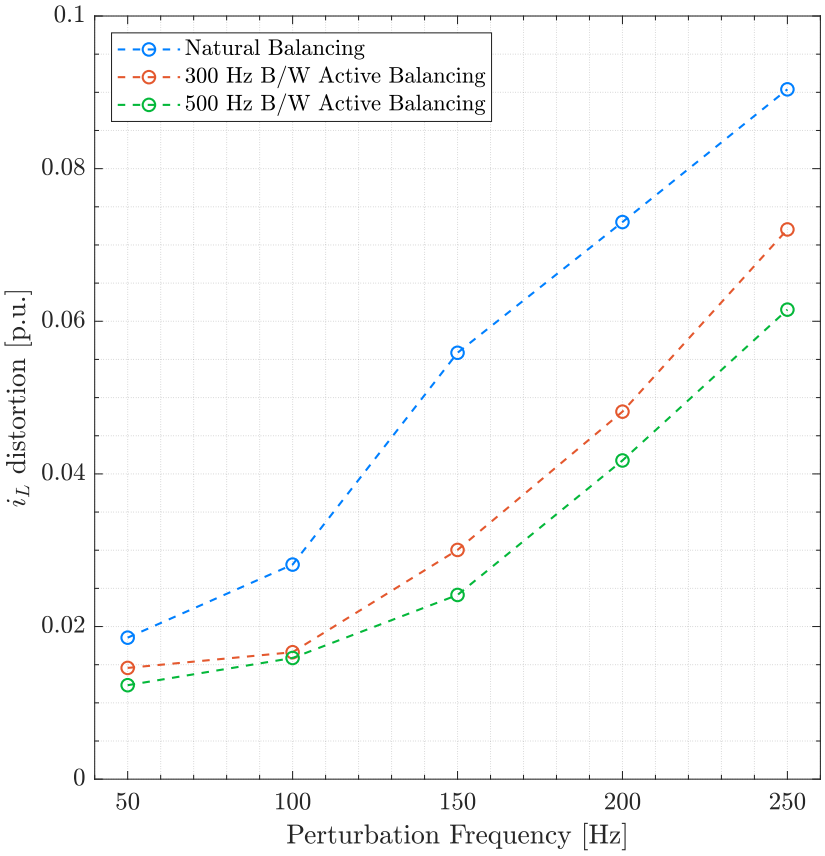


Figure 2.14: Measured current distortion given by (2.54), plotted against the supply perturbation for a current-controlled converter relying on natural versus active balancing. A $10\,V_{RMS}$ perturbation is applied on top of a nominal 50 V dc supply voltage. The current control bandwidth is set to 5 kHz. Under active balancing, the current distortion is consistently lower, indicating better decoupling of the capacitor voltages and inductor current with active balancing.

Load Transient Response

The third experiment investigates the load disturbance rejection of the proposed active balancing controller. Figure 2.15 illustrates results corresponding to 1 kW peak power operation at 250 V input, with a current control bandwidth of 10 kHz. The common-mode duty ratio varies in response to the changing current reference, but does not visibly disturb the flying capacitor voltages. This experiment illustrates an operating point where the ripple in both the capacitor voltages and inductor current are low relative to their average values. Under these conditions, the averaged model given in (2.13)-(2.15) accurately predicts that variations in the common-mode duty ratio do not affect the capacitor voltages. This yields a similar load-transient response under natural balancing.

Experimentally measured converter responses to a large step in the current reference from 2 A to 15 A are shown in Fig. 2.16a and Fig. 2.16b for the converter relying on natural balancing and active balancing respectively. In the high-current operating condition where the small-ripple approximation of capacitor voltages used to derive the averaged model is less accurate, the load transient disturbs the capacitor voltages due to nonlinear coupling between the capacitor voltage ripples and the average load current. Large-signal nonlinearities that are not captured by averaging such as clamping between neighboring capacitor voltages are also observed. The load transient response is improved with the active balancing controller as demonstrated in Fig. 2.16b, however the average capacitor voltages are still disturbed due to coupling between the capacitor voltage ripples and the average load current. Additionally, measurement errors arise from sampling the peaks and valleys of capacitor voltage ripples, which are significant relative to the average capacitor voltages. This measurement error also disturbs capacitor voltage regulation during the transient, further confirming that the accuracy of the proposed averaged converter model decreases as capacitor voltage ripples increase. The limitations of the averaged model are further studied in the following section, where the impact of current ripple on the closed-loop dynamics is experimentally characterized.

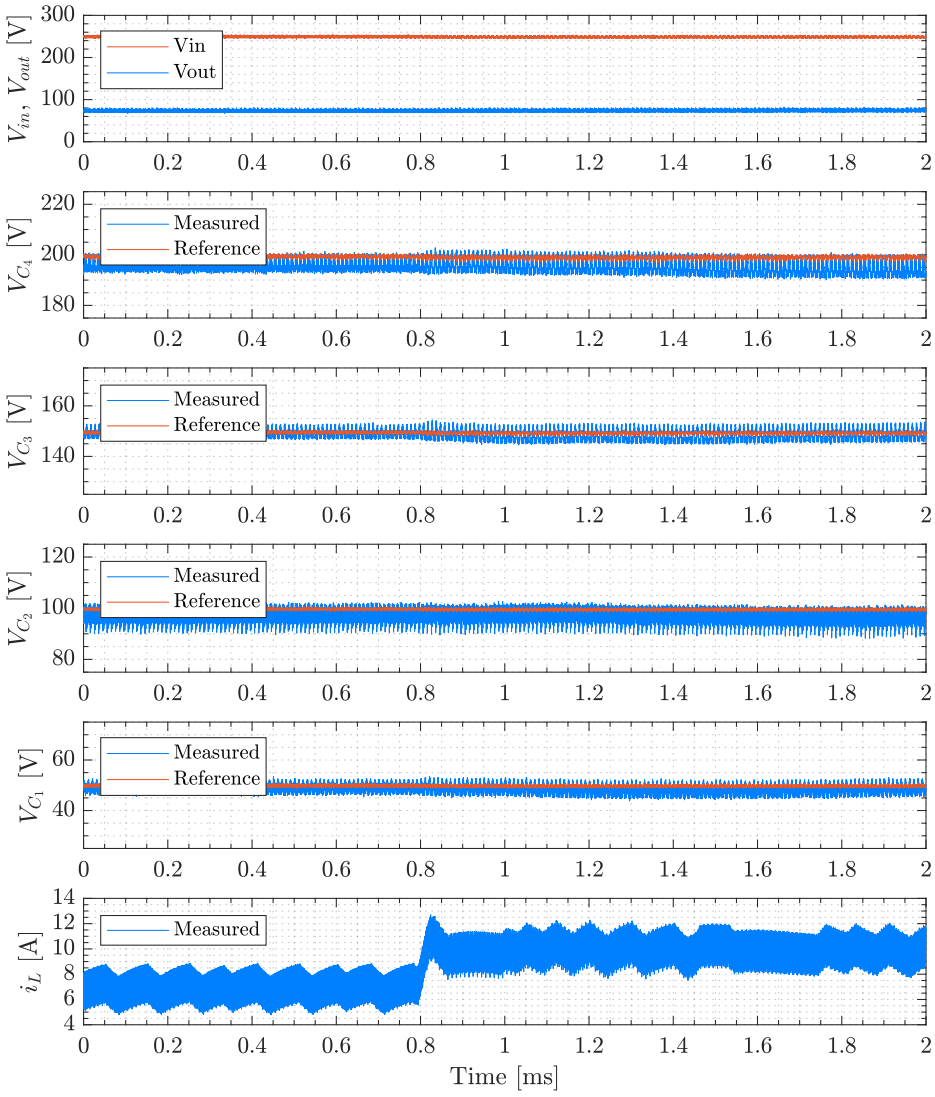
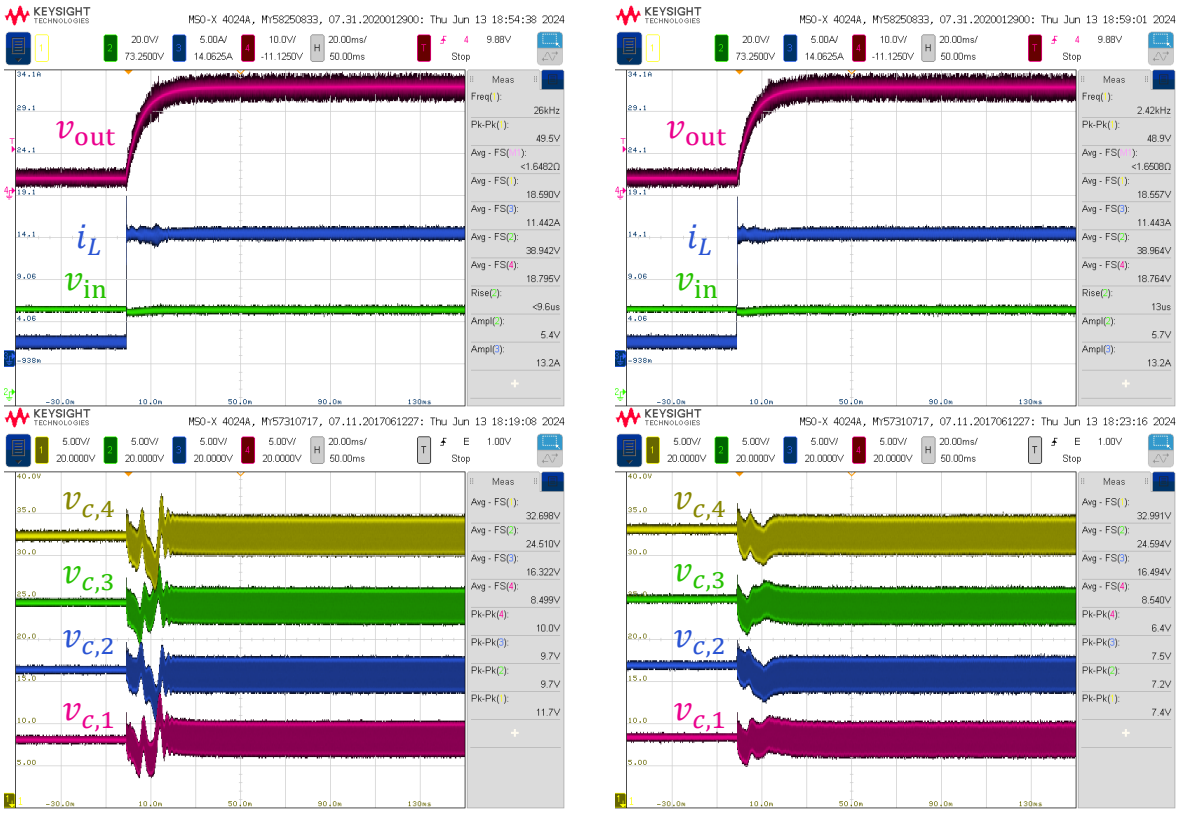


Figure 2.15: Measured capacitor voltage and current response during a step change in the current reference i_{ref} from 7 A to 10 A at $v_{\text{in}} = 250$ V. The current control bandwidth is set to 10 kHz. The flying capacitor voltages are undisturbed during the load current transient, verifying that the capacitor voltages naturally reject the common-mode duty ratio used to control current.



(a) (b)

Figure 2.16: (a) Measured capacitor voltage response in the current-controlled converter relying on natural balancing during a large step change in the current reference from i_{ref} from 2 A to 15 A. (b) Measured capacitor voltage response in the current-controlled converter implementing the proposed active balancing controller. In both cases, the load transient is tested with $v_{\text{in}} = 40\,\text{V}$ and $L = 4.7\,\mu\text{H}$.

2.5 Characterization of Small-Signal Instability

As shown in the experimental results in Section 2.4, the proposed controller enables improved capacitor voltage balancing in current-controlled FCML converters subjected to large-signal variation in the supply voltage. In the averaged sense (considering the model presented in Section 2.3), the proposed control structure ideally realizes a stable decoupled system for arbitrary selections of capacitor balancing bandwidths and inductor current control bandwidth. However, in practice, delays in the control loop and the ripple content of the inductor current have significant impact on the small-signal stability of the closed-loop system. Furthermore, these practical considerations result in residual coupling between the balancing control action and the inductor current due to imperfect cancellation by the feedback linearizing control law. This section presents experimental results characterizing the closed-loop small-signal stability with the proposed controller as a function of the converter design and operating point. In subsequent chapters, refined models are derived and shown to agree with the findings presented in this section.

The performance limits of the active balancing controller may be characterized by the maximum designed balancing bandwidth ω_{bal} that can be chosen before the closed-loop system becomes unstable in the small-signal sense. In the following discussion, small-signal instability corresponds to the deviation of capacitor voltages away from dc reference values once the balancing controller is enabled. For small-signal-unstable designs, nonlinearities in the closed-loop system eventually result in the capacitor voltages exhibiting steady-state limit cycle oscillations or saturating to either the supply voltage or 0 V. The exact nature of the steady-state capacitor voltage behavior depends on the operating point and controller parameters and is not the focus of study in this section. For the purposes of evaluating the closed-loop performance of the active balancing controller, any of these large-signal behaviors are regarded as unstable, since large deviations of capacitor voltages away from the nominal balanced values result in excessive switch voltage stress.

Figure 2.17a shows the experimentally measured maximum stable balancing bandwidth as a function of the load current for the 6-level converter with 10 μH filter inductance. For each load current condition, the balancing bandwidth is incremented in 100 Hz steps until the capacitor response becomes unstable. The stability boundary, indicated by the blue markers in Fig. 2.17a, is defined as the designed balancing bandwidth for which measured oscillation amplitudes of any capacitor voltage grow to greater than one fourth the nominal switch blocking voltage $\frac{V_{\text{in}}}{n_c}$. The error bars in Fig. 2.17a indicate the 100 Hz resolution of the stability boundary characterization arising from the fixed step size. Note that the curve shown characterizes the system stability boundary and should not be interpreted as a reference design.

At low currents, the maximum stable balancing bandwidth is significantly reduced compared to its value at greater loads. This suggests that a fixed balancing bandwidth that yields stable closed-loop operation at a given load current may not necessarily do so at lighter loads. Figure 2.17b illustrates light-load measurements of the capacitor voltages over time for stable and unstable designs indicated by the green and red plots respectively. The

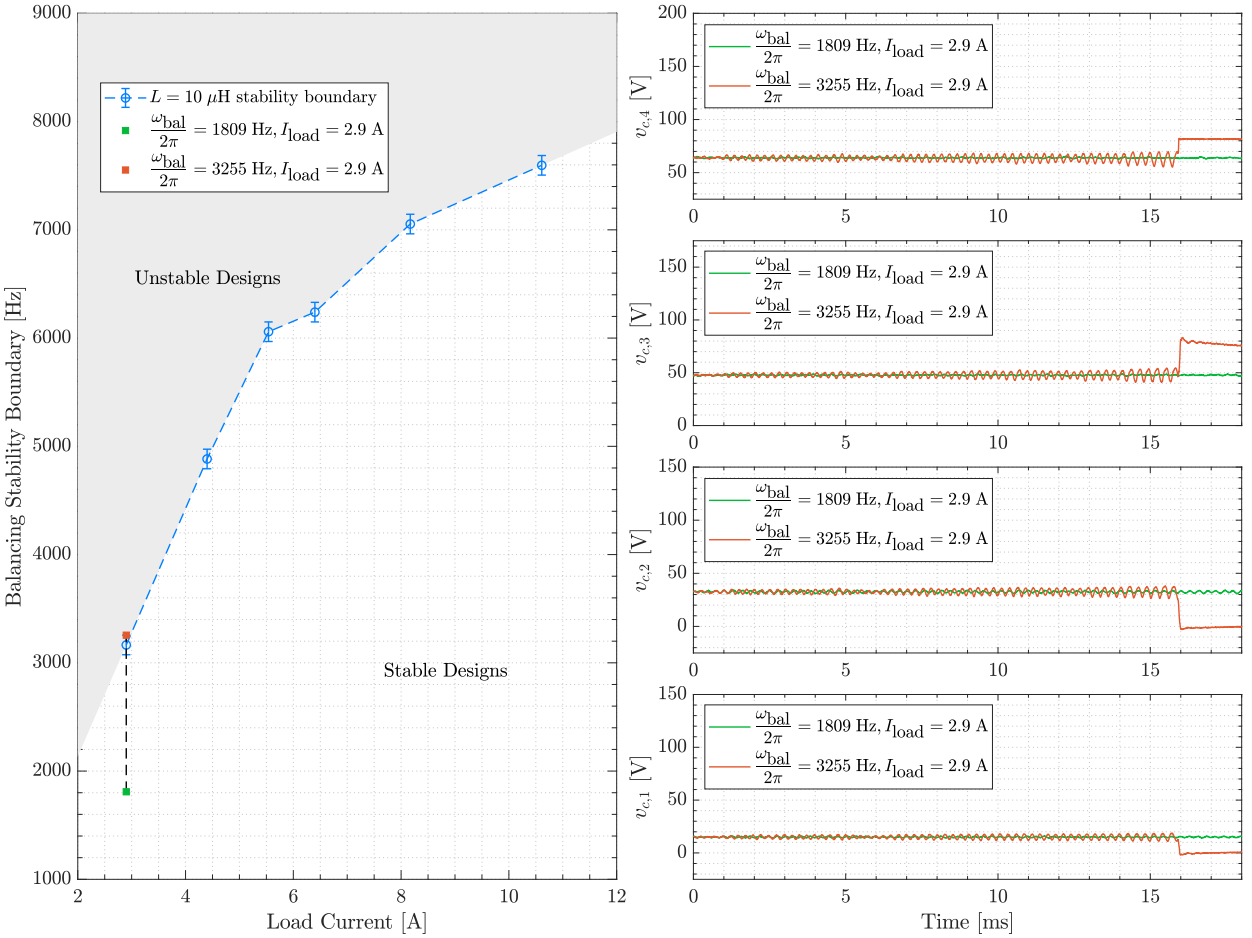


Figure 2.17: (a) Measured closed-loop stability boundary with 10 μH filter inductance, 100 kHz switching frequency, 5 kHz designed current control bandwidth, and 80 V dc supply voltage. The maximum designed balancing bandwidth resulting in a stable system is plotted in blue as a function of the load current. Two points shown in green and red indicate examples of stable and unstable designs respectively. (b) Time domain responses corresponding to the stable and unstable designs indicated in Fig. 2.17a.

time-axis is adjusted such that time $t = 0$ corresponds to the instant when the active balancing controller is enabled. For balancing bandwidths above the stability boundary, capacitor voltages are characterized by an oscillatory response with a growing amplitude that eventually saturate due to limits on the duty cycle applied and body-diode-induced clamping between neighboring capacitor voltages.

The load-dependence of the stability of the closed-loop system is not predicted by the averaged models used in this work. It is the result of the dynamics not modeled by the

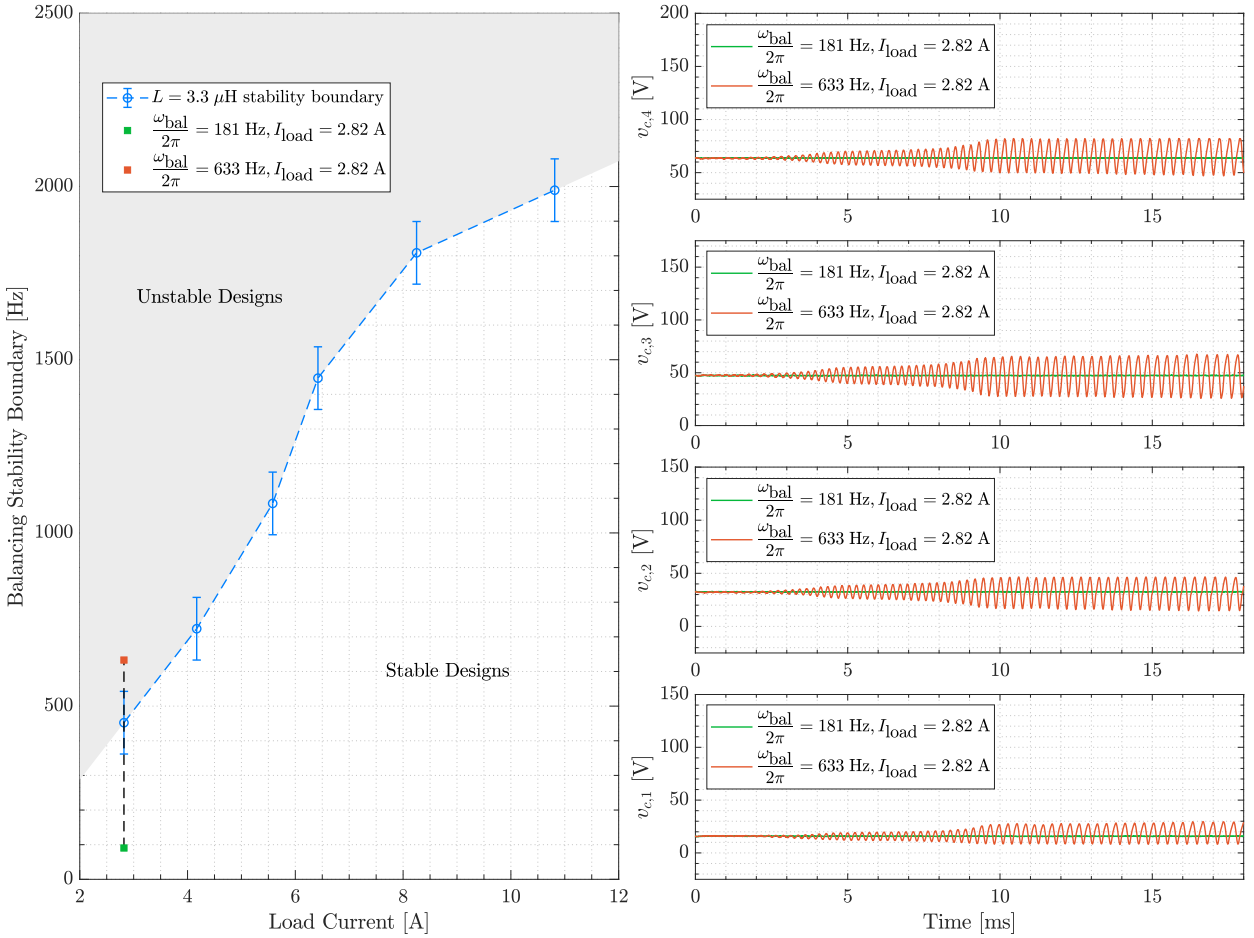


Figure 2.18: (a) Measured closed-loop stability boundary with 3.3 μH filter inductance, 100 kHz switching frequency, 5 kHz designed current control bandwidth, and 80 V dc supply voltage. The maximum designed balancing bandwidth resulting in a stable system is plotted in blue as a function of the load current. Two points shown in green and red indicate examples of stable and unstable designs respectively. (b) Time domain responses corresponding to the stable and unstable designs indicated in Fig. 2.18a.

averaging procedure, namely the ripple content of the state variables [72, 73, 89, 94, 110]. To verify that the inductor current ripple is a primary contributor to the stability of the system for a designed balancing bandwidth, the stability boundary is re-characterized for a 6-level converter with a smaller inductance and consequently larger current ripple. Figure 2.18a shows this maximum stable bandwidth as a function of the load current for the 6-level converter with 3.3 μH filter inductance, and Fig. 2.18b shows corresponding time domain measurements at light load. For a converter designed to have higher current ripple, the

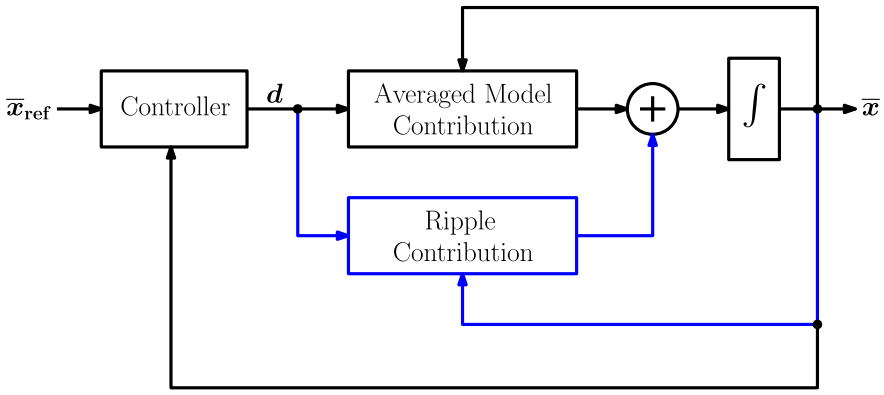


Figure 2.19: Representation of averaged dynamics used as the plant model in this chapter and faster unmodeled dynamics. The unmodeled ripple contribution is insignificant at moderate to heavy loads, but becomes more relevant at light loads, contributing to closed-loop instability depending on the choice of active balancing controller gains.

maximum stable balancing bandwidth for a given load current is consistently lower. This verifies that the inductor current ripple, unmodeled in the design process for the controller proposed in this chapter, impacts the stability of the closed-loop system.

The block diagram in Fig. 2.19 depicts how the plant modeling error generally affects the plant dynamics. Noting the high performance of the active balancing controller compared to the naturally balanced approach in the experimental results of Section 2.4, it is evident the unmodeled dynamics can be disregarded at heavy-load conditions, but are non-negligible at lighter loads. According to the natural balancing studies in [72],[73], and [74], the ripple content in the inductor current has significant impact on the natural balancing dynamics. Since the ripple is purposefully ignored in the averaged modeling approach, its impact is captured in Fig. 2.19 as a part of the unmodeled dynamics. The small-signal instabilities studied in this section motivate the refined models of Chapter 3 that explain the impacts of the inductor current ripple on the closed-loop stability of the capacitor voltages. Light-load instabilities of active balancing controllers based on averaged models also motivate the design of controllers that predict and complement the natural balancing action, as presented in Chapter 4.

2.6 Survey of Active Balancing Literature Based on Averaged Models

Several published works have investigated active balancing controller design based on the averaged model of the FCML converter operating with PS-PWM, however the presented closed-loop systems exhibit limitations arising from their structure and implementation.

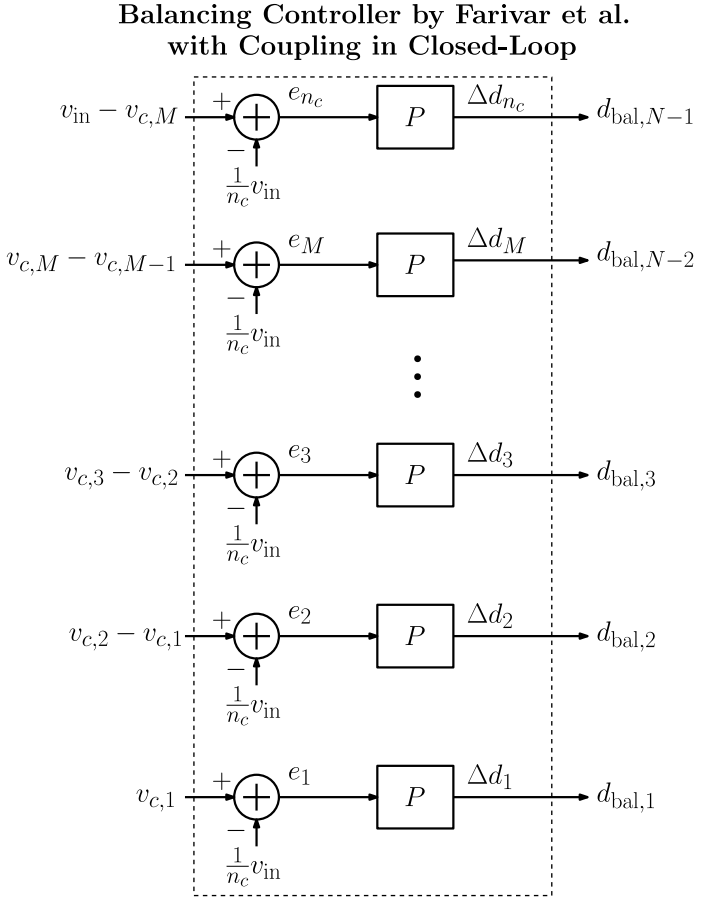


Figure 2.20: Structure of the active balancing controller proposed in [108, 111–113]. As shown in (2.56), this balancing controller results in coupled capacitor voltage dynamics and forces low-bandwidth operation in practice.

This section summarizes a few approaches in the literature and highlights key challenges in each that are addressed in the balancing controller presented in this chapter.

The works in [108, 111–113] present balancing controllers which act on switch duty ratios to regulate the average flying capacitor currents. However, the controllers in these works follow from qualitative arguments about charging and discharging flying capacitors in response to measured imbalance rather than analysis of the plant model. As a consequence, the resulting closed-loop systems exhibit coupling between different flying capacitors. Due to this coupling and uncompensated interactions between the balancing control actions and the inductor current, these works only verify closed-loop performance through low-bandwidth demonstrations. While such designs ensure steady-state balancing, they are not suitable for responding to line transients such as those studied in Section 2.4. Furthermore, as the closed-loop capacitor voltage dynamics are not extensively characterized, it is not clear how

the balancing performance of these systems compares to the natural balancing response.

The structure of the controllers proposed in [108, 111–113] is shown in Fig. 2.20. The controller output variables $d_{\mathrm{bal},k}$ represent the contributions of the balancing controller to the duty ratios, which are subsequently summed with the current control action d_{curr}. Note that the quantity regulated in this scheme is the "cell voltage", defined as the difference of neighboring capacitor voltages. In the structure shown in Fig. 2.20, the balancing controller outputs are given by

$$d_{\mathrm{bal},k} = \Delta d_k = P \cdot \left(e_{v_{c,k-1}} - e_{v_{c,k}}\right) \tag{2.55}$$

where P is a parameter representing the controller gain. The corresponding capacitor voltage dynamics, obtained from (2.13) are given by

$$\dot{v}_{c,k} = \frac{i_L}{C} \cdot P \cdot \left(2e_{v_{c,k}} - e_{v_{c,k+1}} - e_{v_{c,k-1}}\right) \tag{2.56}$$

Each capacitor voltage in this control scheme is clearly coupled to the neighboring capacitor voltages. This coupling and its impact on the inductor current dynamics are not addressed in [108, 111–113], and it is not immediately clear how to choose P to get a stable and satisfactory closed-loop design. By comparison, in the decoupled closed-loop system designed in Section 2.3 (shown in Fig. 2.9) the closed-loop bandwidth of each capacitor voltage control loop is precisely the balancing gain ω_k.

The works in [107, 114] both present controllers for active balancing derived from the principle of "inverting" the dynamics of the averaged model. In both approaches, state-feedback control laws are derived to obtain a linear plant that has decoupled input-output behavior with respect to a new set of inputs. In [114], the transformation is calculated on the small-signal plant model of an FCML converter without an output capacitor C_{o} (i.e., a converter with a purely inductive output filter). The approach is easily applied to the converter with an output capacitor shown in Fig. 2.3 by representing the small-signal dynamics of (2.21) in a cascade form

$$\tilde{\boldsymbol{z}} := \begin{bmatrix} \tilde{v}_{c,1} & \cdots & \tilde{v}_{c,M} & \tilde{i}_L \end{bmatrix}^{\mathrm{T}} \in \mathbb{R}^{n_c} \tag{2.57}$$

$$\dot{\tilde{\boldsymbol{z}}} = \hat{\boldsymbol{F}} \cdot \tilde{\boldsymbol{z}} + \boldsymbol{W} \cdot \tilde{v}_{\mathrm{o}} + \hat{\boldsymbol{G}} \cdot \tilde{\boldsymbol{\delta}} \tag{2.58}$$

$$\dot{\tilde{v}}_{\mathrm{o}} = \frac{1}{C_{\mathrm{o}}} \left(i_L - \frac{v_{\mathrm{o}}}{R}\right) \tag{2.59}$$

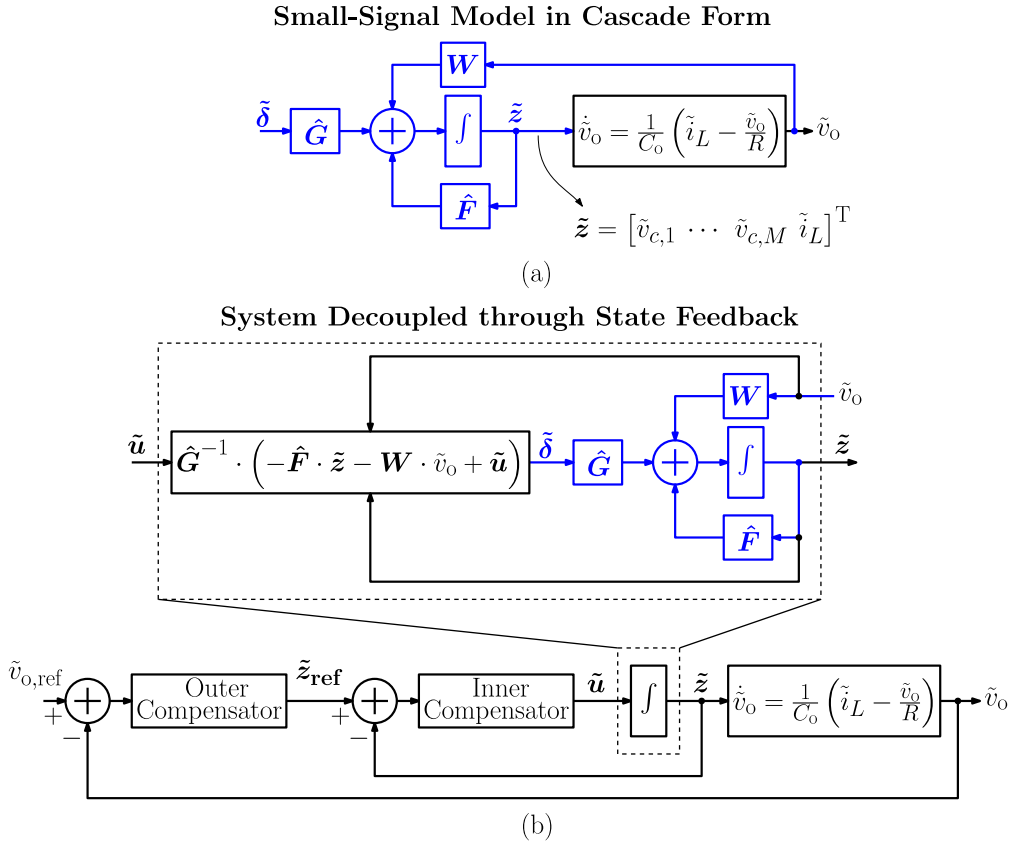


Figure 2.21: (a) Block diagram representation of the small-signal system in (2.21) in cascade form. (b) System resulting from the state feedback decoupling control law derived following the principles of [114]. This control law is identical to that presented in Section 2.3, but does not explicitly show the parallel control structure.

where $\tilde{\boldsymbol{\delta}}$ is given in (2.31), and

$$\hat{\boldsymbol{F}} = \mathbf{0}_{\boldsymbol{n_c}\times\boldsymbol{n_c}} \tag{2.60}$$

$$\hat{\boldsymbol{G}} = \begin{bmatrix} \frac{I_L}{C_1} & 0 & 0 & \cdots & 0 & 0 \\ 0 & \frac{I_L}{C_2} & 0 & \cdots & 0 & 0 \\ \vdots & \ddots & \ddots & \ddots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{I_L}{C_M} & 0 \\ -\frac{V_{c,1}}{L} & -\frac{V_{c,2}}{L} & -\frac{V_{c,3}}{L} & \cdots & -\frac{V_{c,M}}{L} & \frac{\overline{v_{in}}}{L} \end{bmatrix} \in \mathbb{R}^{n_c \times n_c} \tag{2.61}$$

$$\boldsymbol{W} = \begin{bmatrix} 0 & \cdots & 0 & -\frac{1}{L} \end{bmatrix}^T \in \mathbb{R}^{n_c} \tag{2.62}$$

(2.63)

Fig. 2.21a shows a block diagram representation of the small-signal system in cascade form. Application of the state feedback control law $\tilde{\boldsymbol{\delta}} = \hat{\boldsymbol{G}}^{-1} \cdot \left(-\hat{\boldsymbol{F}} \cdot \tilde{\boldsymbol{z}} - \boldsymbol{W} \cdot \tilde{v}_{\mathrm{o}} + \tilde{\boldsymbol{u}} \right)$ yields a new plant consisting of decoupled integrators connecting each of the new inputs $\tilde{u}_k$ to each of the states $\tilde{z}_k$. Given (2.60), the net decoupling control law is $\tilde{\boldsymbol{\delta}} = \hat{\boldsymbol{G}}^{-1} \cdot (-\boldsymbol{W} \cdot \tilde{v}_{\mathrm{o}} + \tilde{\boldsymbol{u}})$, where

$$\hat{\boldsymbol{G}}^{-1} = \begin{bmatrix} \frac{C_1}{I_L} & 0 & 0 & \cdots & 0 & 0 \\ 0 & \frac{C_1}{I_L} & 0 & \cdots & 0 & 0 \\ \vdots & \ddots & \ddots & \ddots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{C_M}{I_L} & 0 \\ \frac{V_{c,1}}{\overline{v_{\mathrm{in}}}} \cdot \frac{C_1}{I_L} & \frac{V_{c,2}}{\overline{v_{\mathrm{in}}}} \cdot \frac{C_2}{I_L} & \frac{V_{c,3}}{\overline{v_{\mathrm{in}}}} \cdot \frac{C_3}{I_L} & \cdots & \frac{V_{c,M}}{\overline{v_{\mathrm{in}}}} \cdot \frac{C_M}{I_L} & \frac{L}{\overline{v_{\mathrm{in}}}} \end{bmatrix} \tag{2.64}$$

As shown in Fig. 2.21b, the new decoupled system can be controlled via linear state feedback to control the capacitor voltages and inductor current. Similar to the representation in Fig. 2.9, $\tilde{v}_{\mathrm{o}}$ can be controlled through an outer regulation loop setting the current reference for the inner loop as shown in Fig. 2.21b. It can be shown that the control law of (2.64) expresses exactly the same actions to decouple the balancing and current control loops as the control laws presented in Section 2.3. This confirms that the parallel controller derived in this chapter achieves the same performance as a controller derived directly from the matrix description of the small-signal system. Details of how to convert the transformed input vector $\tilde{\boldsymbol{\delta}}$ back into the vector of duty ratios $\tilde{\boldsymbol{d}}_{\mathbf{bal}}$ are missing from the discussion in [114]. By contrast, the control law analysis in Section 2.3 highlights how to calculate the balancing contributes to the duty ratios $d_{\mathrm{bal},k}$ from the duty ratio differences Δd_k. The structure of the parallel controller demonstrates that active balancing control does not require significant computational effort, as the balancing control actions and the compensation actions in the current controller to reject the balancing disturbances can be recursively computed.

In [107], the inversion approach is applied directly the nonlinear averaged model of (2.13)–(2.15). The final controller structure is similar to that presented in Section 2.3 and [114]—differences of duty ratios are adjusted based on measured capacitor voltage error and are appropriately propagated to eliminate coupling between capacitor voltages in closed-loop. A benefit of applying inversion principles on the nonlinear averaged model is that the controller achieves model inversion even when the state variables deviate significantly from the quiescent point. This difference is illustrated in the experimental results of [107]. Section 2.3 highlights how the balancing controller gains and decoupling terms in the current control law can be updated using measured state information to achieve similar closed-loop behavior. Similar to [114], the work of [107] presents the decoupling control law as a matrix controller. Direct evaluation of the matrix rows to determine the controller outputs can be difficult to implement in digital controllers with constrained computational resources. However, the

triangular structure of the control law is compatible with substitution algorithms such as that presented for the balancing controller in Section 2.3. One drawback of the approach in [107] is that the resulting closed-loop system does not offer a means to directly control the inductor current, a consequence of the system having N state variables but only $N-1$ control inputs. In [107], the outputs of the transformed plant are defined to be only the $N-2$ flying capacitors $v_{c,k}$ and output voltage v_{o} to decouple the input-output behavior without uncontrolled dynamics. The lack of direct control of the inductor current limits the practical utility of this approach, as control of the inductor current can be highly desirable in applications such as motor drives and power factor correction (PFC) converters.

Importantly, the works of [107, 114] do not characterize the choice of controller gains and achievable closed-loop active balancing bandwidths, and imply that the dynamics of capacitor voltages can be assigned arbitrarily (with standard limitations of digital control such as controller and modulator delays). The stability characterization in Section 2.5 illustrates a fundamental limitation of balancing controllers based on averaging that is not discussed in [107, 114]: the inductor current ripple is not considered in the model of the capacitor voltage dynamics. This modeling error can be considered negligible for designs and operating points where the contribution of the inductor current ripple to the average capacitor voltage dynamics is small compared to the contribution of the average inductor current. At light loads, small-signal instability arises from the modeling error and can only be suppressed through significant de-rating of the balancing controller gains. The following chapter develops refined averaged models that capture the coupling between the current ripple and the average capacitor voltage dynamics. The models are subsequently used to verify the experimental findings in this chapter.

Chapter 3

Generalized Averaged Modeling

Portions of this chapter are adapted in whole or in part from [115].

Experimental characterization in the previous chapter highlighted that active balancing controllers derived from the averaged converter model are generally only useful in operating conditions where the small-ripple approximation of the inductor current is valid. In light-load conditions where the current ripple is comparable to the average current, the standard averaged model does not accurately capture the capacitor voltage dynamics. This modeling error results in unstable operation without significant de-rating of the balancing controller gains to the point where the balancing action may no longer be effective. Moreover, at zero-load operation, the balancing controllers derived from averaging assume there is no balancing mechanism in the converter. These findings motivate the investigation of converter models that capture the coupling between the inductor current ripple and the capacitor voltages.

The notion of coupling between the ripple content of some state variables and the average dynamics of others is familiar in the field of power converter modeling. In resonant converters, for example, tank inductor currents are assumed to be nominally sinusoidal at the tank resonant frequency with zero average value, but result in nonzero average current into the

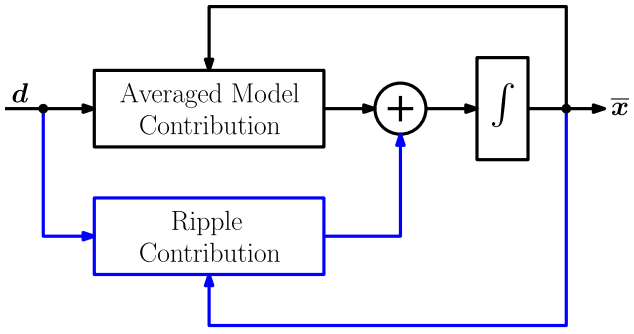


Figure 3.1: Block diagram representation of averaged plant model, showing the unmodeled impacts of the inductor current ripple.

load network. For FCML converters, investigations of the natural balancing of capacitor voltages under PS-PWM in [72–78] have highlighted that the contribution of inductor current ripple to the average capacitor currents is the reason for capacitor voltage balancing. As shown in Section 1.3 and from the averaged model in (2.13), the average inductor current does not act to balance the flying capacitors in symmetric PS-PWM, as all the duty ratios are equal. This chapter aims to study the exact nature of the coupling between the inductor current ripple and average capacitor voltage dynamics. A model for the contribution of the inductor current ripple, shown generally in Fig. 3.1, is derived through the method of generalized averaging [89] yielding a refined plant description. The new plant model incorporating the impact of the current ripple is shown to accurately capture the small-signal instabilities that arise in actively balanced systems.

Before proceeding, the averaging nomenclature appearing in the literature must be clarified to avoid misinterpretation of the methods. Historically, two techniques of "higher-order averaging" have been applied to study the dynamic impacts of ripple in power converters. In both approaches, the contributions of the ripple to the average dynamics appear as terms added to the standard averaged model. The standard averaged model is always recovered as an "order-0" approximation of the higher-order averaged model. The first method of higher-order averaging, presented in [89] as "generalized averaging", is based on a Fourier decomposition approach. Ripples in state variables are decomposed into sinusoidal components at different harmonics of the switching frequency, and their contributions to the averaged dynamics are considered in a per-harmonic manner. This is the method that will be investigated in this chapter due to its simplicity and connection to previously developed models of the FCML converter. The second method, proposed in [94], is based on formulating the averaged model as the solution to a perturbation problem, and will be discussed in the next chapter.

3.1 A Review of Generalized Averaged Modeling of Power Converters

The method of generalized averaging presented in [89] represents the time-domain behavior of state variables over a sliding window of length $T_\mathrm{s} = 1/f_\mathrm{s}$ with the complex exponential Fourier series representation given by

$$x(t - T_\mathrm{s} + s) = \sum_{m=-\infty}^{\infty} \langle x \rangle_m(t)\, e^{jm\omega_s(t-T_\mathrm{s}+s)} \tag{3.1}$$

where $\omega_s = 2\pi f_\mathrm{s}$ and s is a variable indexing time in the interval $[t - T_\mathrm{s}, t)$. The integral definition for the complex-valued Fourier series coefficients $\langle x \rangle_m$,

$$\langle x \rangle_m(t) = \frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} x(t - T_\mathrm{s} + s)\, e^{-jm\omega_s(t-T_\mathrm{s}+s)}\, \mathrm{d}s \tag{3.2}$$

is referred to as the "generalized averaging operator." As in the case of standard averaging, applying the generalized averaging operator to the state variables and inputs of the time-varying system yields a new time-invariant system representing the averaged behavior. In the generalized averaged model, the the Fourier coefficients $\langle x\rangle_m(t)$ are the new (complex) state variables. The index-0 states $\langle x\rangle_0(t)$ describe the time-averaged components of state variables. The key contribution of the generalized averaging procedure over standard averaging is its description of the coupling between the zero- and nonzero-index coefficients. These nonzero-index coefficients correspond to the m^{th}-harmonic content of ripple in state variables, inputs, and switching signals. As the Fourier coefficients $\langle x\rangle_m(t)$ are paired in (3.1) with vectors in the complex plane rotating at angular frequency $m\omega_s$, generalized averaged models have also been referred to as "dynamic phasor" models in the literature [116, 117].

Two mathematical properties reported in [89] are useful when applying generalized averaging in the context of the FCML converter. For generic signals $x(t)$ and $y(t)$,

$$\langle xy\rangle_m = \sum_{w=-\infty}^{\infty} \langle x\rangle_{m-w}\langle y\rangle_w \tag{3.3}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\langle x\rangle_m = \left\langle \frac{\mathrm{d}}{\mathrm{d}t}x \right\rangle_m - jm\omega_\mathrm{s}\langle x\rangle_m \tag{3.4}$$

Both properties can be derived from the definition of the generalized averaging operator in (3.2). Additionally, because the signals $x(t)$ and $y(t)$ are real-valued in power converter analysis, the positive- and negative-index coefficients can be related as

$$\langle x\rangle_{-m} = \langle x\rangle_m^* \tag{3.5}$$

$$\langle x\rangle_m\langle y\rangle_{-m} + \langle x\rangle_{-m}\langle y\rangle_m = 2\mathrm{Re}\left\{\langle x\rangle_m\langle y\rangle_m^*\right\} \tag{3.6}$$

where $\langle x\rangle_m^*$ indicates the complex conjugate of $\langle x\rangle_m$.

A methodical procedure is now highlighted to derive the generalized averaged model from the switched differential equations describing the converter dynamics. Consider the general representation of the switched system in (2.1), repeated as

$$\dot{\boldsymbol{x}} = \boldsymbol{f}\left(\boldsymbol{x}, \boldsymbol{w}, t\right) \tag{3.7}$$

Assuming the state vector is represented as $\boldsymbol{x} = \begin{bmatrix} x_1 & \cdots & x_N \end{bmatrix}^\mathrm{T}$, (3.7) can be expanded as

$$\begin{bmatrix} \dot{x}_1 \\ \vdots \\ \dot{x}_N \end{bmatrix} = \begin{bmatrix} f_1\left(\boldsymbol{x}, \boldsymbol{w}, t\right) \\ \vdots \\ f_N\left(\boldsymbol{x}, \boldsymbol{w}, t\right) \end{bmatrix} \tag{3.8}$$

First, each state variable x_k is decomposed into into the positive and negative coefficients corresponding to n_k harmonics. In other words,

$$x_k\left(t - T_\mathrm{s} + s\right) = \sum_{m=-n_k}^{n_k} \langle x_k\rangle_m\left(t\right) e^{jm\omega_\mathrm{s}(t-T_\mathrm{s}+s)} \tag{3.9}$$

Note that as the dimension of the extended state-space resulting from generalized averaging is $\sum_{k=1}^{N} 2n_k$, care should be taken to not include more harmonics for each state variable than necessary. For many state variables, a small-ripple approximation is valid and the effects of ripple can be neglected with small error. For these variables, $n_k = 0$ is sufficient. The question of how many harmonics to model for state variables is central to the discussion in subsequent sections of this chapter.

Next, for each coefficient $\langle x_k \rangle_m$, where $m \in \{0, \ldots, n_k\}$, the m^{th} harmonic of the right-hand side in (3.8) is evaluated, i.e.

$$\langle f_k(\boldsymbol{x}, \boldsymbol{w}, t) \rangle_m \tag{3.10}$$

In evaluating these expressions, the convolution property of (3.3) is typically employed, as will be demonstrated in the next section.

Finally, the dynamics of the m^{th}-harmonic coefficient of the k^{th} state variable is given by

$$\frac{\mathrm{d}}{\mathrm{d}t}\langle x_k \rangle_m = \langle f_k(\boldsymbol{x}, \boldsymbol{w}, t) \rangle_m - jm\omega_{\text{s}}\langle x_k \rangle_m \tag{3.11}$$

The process is repeated for all state variables to obtain the complete generalized averaged model.

3.2 Application of Generalized Averaging to the FCML Converter

The generalized averaging procedure is described with respect to the N-level converter schematic shown in Fig. 3.2. In this schematic, a parasitic resistance R_{s} is explicitly modeled in series with the inductor to capture losses in the converter. This resistor represents the lumped effects of losses in the switches, inductor, and capacitors, and will be shown in the subsequent analysis to contribute to the damping of the flying capacitor voltage dynamics. This damping is observed in experimental measurements, and has been reported in prior literature modeling the FCML converter [72–77].

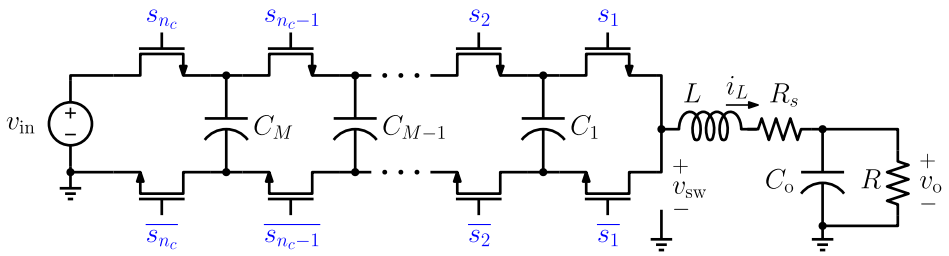


Figure 3.2: Schematic drawing of an N-level FCML converter, explicitly modeling a parasitic resistance R_{s}.

Application of the generalized averaging procedure to the dynamics of the FCML converter results in an extended state space with a greater number of dimensions than the original system. In applying the generalized averaging operator to the FCML converter dynamics, a few assumptions are useful for restricting the dimensions and complexity of the resultant model. The following analysis assumes that the ripple content of the capacitor voltages $v_{c,k}$, supply voltage v_{in}, and load voltage v_{o} are negligible, yielding the approximations

$$v_{c,k}(t) \approx \langle v_{c,k} \rangle_0(t) \tag{3.12}$$

$$v_{\text{in}}(t) \approx \langle v_{\text{in}} \rangle_0(t) \tag{3.13}$$

$$v_{\text{o}}(t) \approx \langle v_{\text{o}} \rangle_0(t) \tag{3.14}$$

These approximations are consistent with those reported in the models of [72–76, 78, 118], and are physically justified for practical FCML converter designs. In particular, this work assumes that the flying capacitances are sufficiently large such that the capacitor voltage ripple can be neglected at all load conditions.

A small-ripple approximation is *not* made for the inductor current. Considering n harmonics, the inductor current can be expanded as

$$i_L(t - T_s + s) \approx \sum_{m=-n}^{n} \langle i_L \rangle_m(t)\, e^{jm\omega_s(t-T_s+s)} \tag{3.15}$$

Following the notation of [89], $\langle i_L \rangle_m$ denotes the complex state variable corresponding to the m^{th} harmonic of the inductor current, and is decomposed as $\langle i_L \rangle_m = \langle i_L \rangle_m^{\mathbb{R}} + j\langle i_L \rangle_m^{\mathbb{I}}$.

The dc components of the switching signals s_k are given by $\langle s_k \rangle_0 = d_k$. For phase shift ϕ_k (in radians) associated with switching signal s_k, the m^{th}-harmonic of the switching signals is a complex variable $\langle s_k \rangle_m = \langle s_k \rangle_m^{\mathbb{R}} + j\langle s_k \rangle_m^{\mathbb{I}}$ defined as

$$\langle s_k \rangle_m = \frac{\sin(m\pi d_k)}{m\pi} e^{jm\phi_k} \quad , m \in \mathbb{N} \tag{3.16}$$

In this definition, s_k is centered at $t = 0$ when $\phi_k = 0$. Without loss of generality, this work assumes a "leading" arrangement of $\phi_k = 2\pi\,(k-1)\,/n_c$.

The switched equations in (2.10)–(2.12) all contain difference terms $s_{k+1} - s_k$. To simplify notation, a switching function difference variable is defined as $\Delta s_k := s_{k+1} - s_k$. Note that because the generalized averaging operator (3.2) is linear, the following holds true for the switching function difference variable

$$\langle \Delta s_k \rangle_m = \langle s_{k+1} \rangle_m - \langle s_k \rangle_m \tag{3.17}$$

where $\langle \Delta s_k \rangle_m$ is a complex state variable decomposed as $\langle \Delta s_k \rangle_m = \langle \Delta s_k \rangle_m^{\mathbb{R}} + j\langle \Delta s_k \rangle_m^{\mathbb{I}}$.

The converter model resulting from generalized averaging is given by

$$\begin{aligned}\dot{\langle v_{c,k}\rangle_0} &= \frac{1}{C_k}\langle \Delta s_k i_L\rangle_0 = \frac{1}{C_k}\sum_{m=-n}^{n}\langle \Delta s_k\rangle_{-m}\langle i_L\rangle_m \\ &= \frac{1}{C_k}\left(\langle \Delta s_k\rangle_0\langle i_L\rangle_0 + \ 2\mathrm{Re}\left\{\sum_{m=1}^{n}\langle \Delta s_k\rangle_m^*\langle i_L\rangle_m\right\}\right) \qquad (3.18)\\ \dot{\langle i_L\rangle_0} &= \frac{1}{L}\left(\langle v_{\mathrm{sw}}\rangle_0 - \langle v_{\mathrm{o}}\rangle_0 - R_s\langle i_L\rangle_0\right) \qquad (3.19)\\ \dot{\langle i_L\rangle_m} &= \left(-jm\omega_s - \frac{R_s}{L}\right)\langle i_L\rangle_m + \frac{1}{L}\langle v_{\mathrm{sw}}\rangle_m \qquad (3.20)\\ \dot{\langle v_o\rangle_0} &= \frac{1}{C_{\mathrm{o}}}\left(\langle i_L\rangle_0 - \frac{\langle v_{\mathrm{o}}\rangle_0}{R}\right) \qquad (3.21)\end{aligned}$$

where

$$v_{\mathrm{sw}} = v_{\mathrm{in}}s_{n_c} - \sum_{k=1}^{M} v_{c,k}\cdot\Delta s_k \qquad (3.22)$$

$$\langle v_{\mathrm{sw}}\rangle_0 = \langle v_{\mathrm{in}}\rangle_0\langle s_{n_c}\rangle_0 - \sum_{k=1}^{M}\langle v_{c,k}\rangle_0\langle \Delta s_k\rangle_0 \qquad (3.23)$$

$$\langle v_{\mathrm{sw}}\rangle_m = \langle v_{\mathrm{in}}\rangle_0\langle s_{n_c}\rangle_m - \sum_{k=1}^{M}\langle v_{c,k}\rangle_0\langle \Delta s_k\rangle_m \qquad (3.24)$$

The extended state space of the generalized averaged system is represented by the state vector

$$\boldsymbol{x} := \left[\begin{array}{c} \langle v_{c,1}\rangle_0 \\ \vdots \\ \langle v_{c,M}\rangle_0 \\ \langle i_L\rangle_0 \\ \langle v_{\mathrm{o}}\rangle_0 \\ \hline \langle i_L\rangle_1^{\mathbb{R}} \\ \langle i_L\rangle_1^{\mathbb{I}} \\ \hline \vdots \\ \hline \langle i_L\rangle_n^{\mathbb{R}} \\ \langle i_L\rangle_n^{\mathbb{I}} \end{array}\right] \in \mathbb{R}^{N+2n} \qquad (3.25)$$

If the duty ratios and phase shifts of switching signals are considered constants, the balancing dynamics obtained from (3.18)–(3.20) can be compactly represented in matrix form

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\cdot\boldsymbol{x} + \boldsymbol{B}\cdot\langle v_{\mathrm{in}}\rangle_0 \qquad (3.26)$$

where

$$\boldsymbol{A} = \left[\begin{array}{c|c|c|c} \boldsymbol{A_{00}} & \boldsymbol{A_{01}} & \cdots & \boldsymbol{A_{0n}} \\ \hline \boldsymbol{A_{10}} & \boldsymbol{A_{11}} & \boldsymbol{0} & \boldsymbol{0} \\ \hline \vdots & \boldsymbol{0} & \ddots & \boldsymbol{0} \\ \hline \boldsymbol{A_{n0}} & \boldsymbol{0} & \boldsymbol{0} & \boldsymbol{A_{nn}} \end{array}\right] \tag{3.27}$$

$$\boldsymbol{B} = \left[\begin{array}{c|c|c|c} \boldsymbol{B_0^{\mathrm{T}}} & \boldsymbol{B_1^{\mathrm{T}}} & \cdots & \boldsymbol{B_n^{\mathrm{T}}} \end{array}\right]^{\mathrm{T}} \tag{3.28}$$

with

$$\boldsymbol{A_{00}} = \begin{bmatrix} 0 & \cdots & 0 & \frac{\langle \Delta s_1 \rangle_0}{C_1} & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & \frac{\langle \Delta s_M \rangle_0}{C_M} & 0 \\ -\frac{\langle \Delta s_1 \rangle_0}{L} & \cdots & -\frac{\langle \Delta s_M \rangle_0}{L} & -\frac{R_s}{L} & -\frac{1}{L} \\ 0 & \cdots & 0 & \frac{1}{C_o} & -\frac{1}{RC_o} \end{bmatrix} \tag{3.29}$$

$$\boldsymbol{A_{0m}} = \begin{bmatrix} \frac{2\langle \Delta s_1 \rangle_m^{\mathbb{R}}}{C_1} & \frac{2\langle \Delta s_1 \rangle_m^{\mathbb{I}}}{C_1} \\ \vdots & \vdots \\ \frac{2\langle \Delta s_M \rangle_m^{\mathbb{R}}}{C_M} & \frac{2\langle \Delta s_M \rangle_m^{\mathbb{I}}}{C_M} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{3.30}$$

$$\boldsymbol{A_{m0}} = \begin{bmatrix} -\frac{\langle \Delta s_1 \rangle_m^{\mathbb{R}}}{L} & \cdots & -\frac{\langle \Delta s_M \rangle_m^{\mathbb{R}}}{L} & 0 & 0 \\ -\frac{\langle \Delta s_1 \rangle_m^{\mathbb{I}}}{L} & \cdots & -\frac{\langle \Delta s_M \rangle_m^{\mathbb{I}}}{L} & 0 & 0 \end{bmatrix} \tag{3.31}$$

$$\boldsymbol{A_{mm}} = \begin{bmatrix} -\frac{R_s}{L} & m\omega_s \\ -m\omega_s & -\frac{R_s}{L} \end{bmatrix} \tag{3.32}$$

$$\boldsymbol{B_0^{\mathrm{T}}} = \begin{bmatrix} 0 & \cdots & 0 & \frac{\langle s_{n_c} \rangle_0}{L} & 0 \end{bmatrix} \tag{3.33}$$

$$\boldsymbol{B_m^{\mathrm{T}}} = \begin{bmatrix} \frac{\langle s_{n_c} \rangle_m^{\mathbb{R}}}{L} & \frac{\langle s_{n_c} \rangle_m^{\mathbb{I}}}{L} \end{bmatrix} \tag{3.34}$$

Fig. 3.3 shows a block diagram representation of the model of (3.26), highlighting the additional dynamics captured compared to the standard averaged model. In particular, the block diagram reveals the feedback structure of the natural balancing mechanism. The average capacitor voltages influence the inductor current ripple, decomposed in the generalized averaged model into different harmonic terms. Each inductor current harmonic may subsequently drive average current into or out of the capacitor.

The natural balancing dynamics predicted by the generalized averaged model are examined in a case study of a 6-level FCML converter operated with $D = 0.35$. Fig. 3.4 demonstrates the capacitor voltage responses when a step-transient in the supply voltage is applied. The result of a circuit simulation is compared to the generalized averaged model of

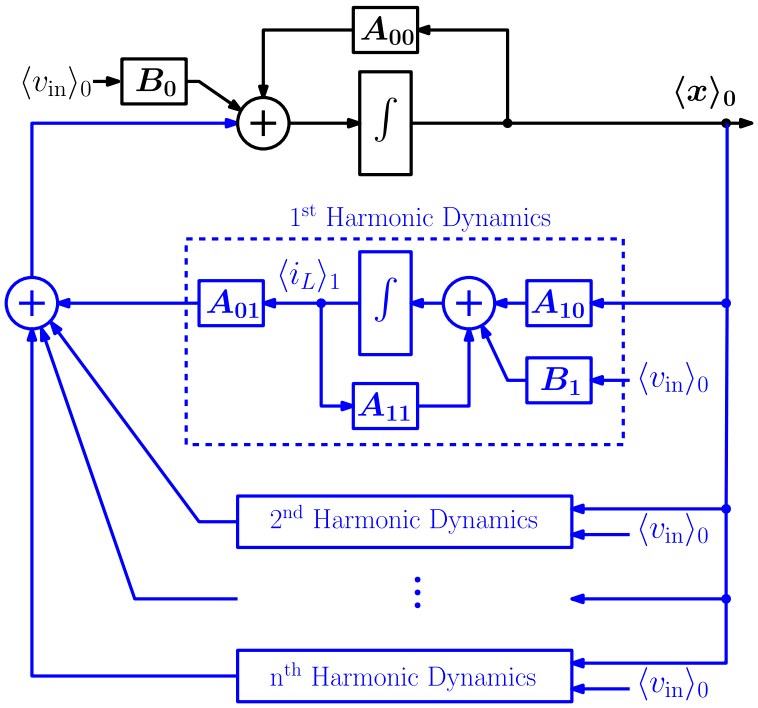


Figure 3.3: Block diagram of the full generalized averaged model given in (3.26). Contributions of the generalized averaged model compared to the standard averaged model are highlighted and appear as feedback dynamics.

(3.26) evaluated for different numbers of modeled inductor current harmonics n. For $n = 0$, where no harmonics are modeled, the model predicts that the capacitors have no dynamics. When the first harmonic is included, the model predicts nonzero but incorrect dynamics for the capacitor voltages. Including the second harmonic yields a model that predicts the dominant oscillatory modes and damping of the capacitor dynamics accurately as evidenced by the excellent agreement between the transient responses. The model with $n = 2$ captures the dominant second order response with a relative error of 21% for the damping time constant and 3% for the oscillation frequency, corresponding to a (vector) relative error of 3% in the dominant pole location. Including additional harmonics has minor impact on the transient response.

In Fig. 3.5, the verification is performed with the duty ratio modified to $D = 0.5$. Notably at this operating point, the second harmonic of the inductor current does not contribute to the capacitor voltage dynamics, and $n = 3$ is required to capture the correct steady-state solution. The fourth, fifth, and sixth harmonics also do not contribute to the capacitor voltage dynamics, and $n = 7$ is required to obtain a similar result as the circuit simulation with a relative error of 1.4% in the dominant pole location.

The waveforms of Fig. 3.4 and Fig. 3.5 highlight two important characteristics of generalized averaged models of FCML converters. First, the single-frequency describing function

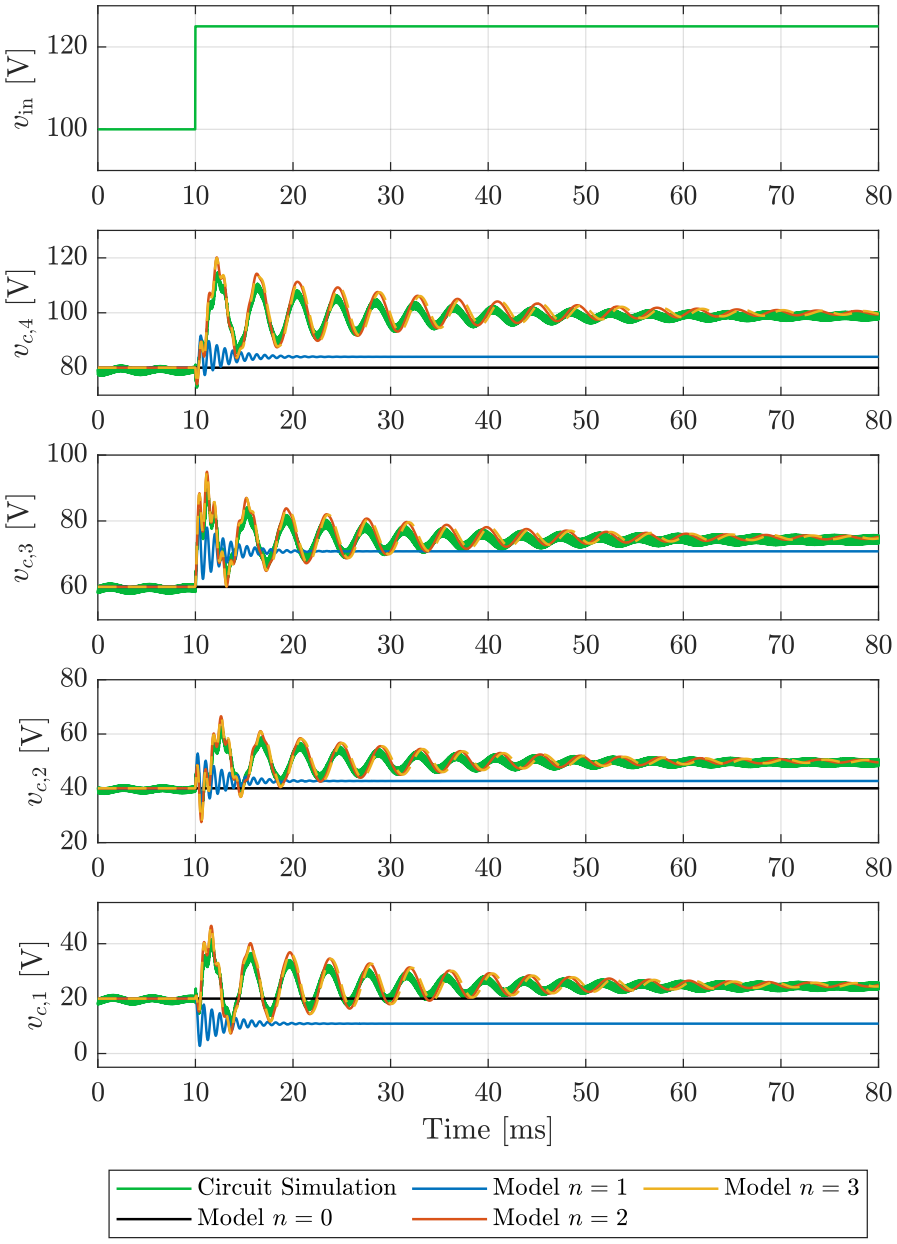


Figure 3.4: Simulated and modeled capacitor voltage responses for a 6-level FCML converter operating at $D = 0.35$, varying the total numbers of harmonics modeled n. The model with $n = 2$ accurately captures the step-transient response. In the circuit simulation and model, $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R = 3.5\,\Omega$, $R_s = 0.3\,\Omega$, and $f_s = 100\,\text{kHz}$. The line voltage is stepped from 100 V to 125 V.

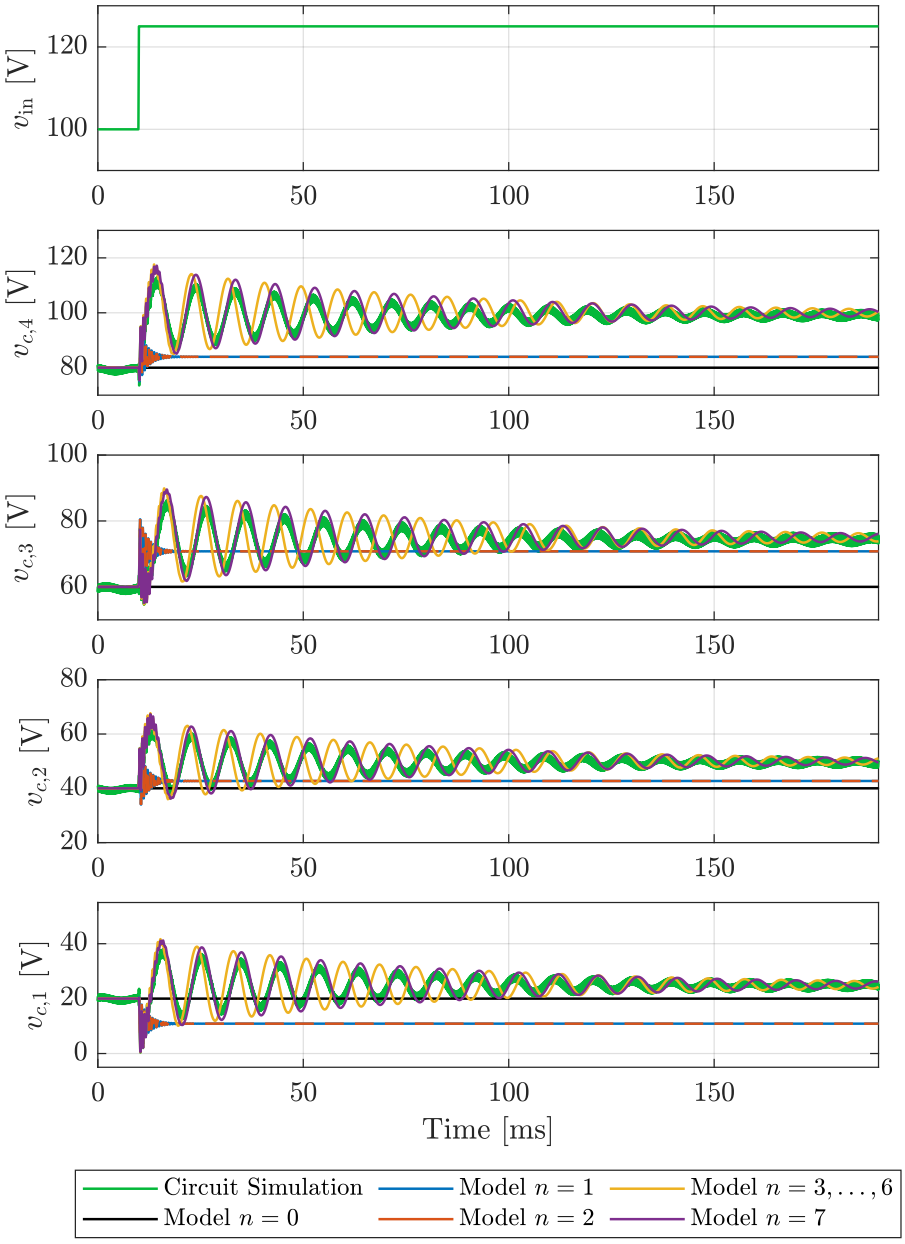


Figure 3.5: Simulated and modeled capacitor voltage responses for a 6-level FCML converter operating at $D = 0.50$. At this conversion ratio, $n = 3$ is required to predict the correct steady-state behavior. A small error of 5.8 Hz is observed between the predicted and observed dominant oscillation frequency. In the circuit simulation and model, $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R = 5\,\Omega$, $R_s = 0.3\,\Omega$, and $f_s = 100\,\text{kHz}$. The line voltage is stepped from 100 V to 125 V.

approach typical of resonant converter analysis [89, 119–122] where only the first harmonic component of state variables is modeled, is not generally applicable. In the 6-level converter example, the model considering only the first harmonic does not capture the dominant capacitor voltage dynamics. Second, the total number of harmonics required to model a given converter appears to depend on the operating point. This raises a natural question of how many inductor current harmonics one must include before the generalized averaged model converges to some predicted behavior. The following section studies this topic, first by presenting a simplified model and subsequently by examining its dependence on the number of harmonics considered.

3.3 Model Reduction and Analysis of Minimum Harmonics Required

This section studies the contribution of the different inductor current harmonics to the natural balancing dynamics under PS-PWM, where all duty ratios are equal to a common value D and the phase shift in radians between neighboring switching signals is $2\pi/n_c$. The following substitutions are made

$$\langle \Delta s_k \rangle_0 = 0 \tag{3.35}$$

$$\langle \Delta s_k \rangle_m = \frac{\sin(m\pi D)}{m\pi} \exp(jm\phi_k) \left[\exp\left(\frac{jm2\pi}{n_c} \right) - 1 \right] \tag{3.36}$$

The average capacitor voltage dynamics typically vary slowly relative to the switching period [72–74, 76, 78], motivating the investigation of techniques that reduce the model dimensions while preserving the slow behavior. This work presents a technique for model order reduction based on the theory of singular perturbations [90–92].

Model Order Reduction

The equation of (3.20) can be re-expressed as

$$\frac{1}{jm\omega_s} \dot{\langle i_L \rangle}_m = \frac{jm\omega_s L + R_s}{jm\omega_s L} \left(-\langle i_L \rangle_m + \frac{\langle v_{\text{sw}} \rangle_m}{jm\omega_s L + R_s} \right) \tag{3.37}$$

For typical switching frequencies, $\omega_s \gg 1$, so the coefficient on the left-hand side of (3.37) can be approximated as $1/\omega_s \approx 0$. Using this approximation, (3.37) becomes an algebraic expression in $\langle i_L \rangle_m$ and $\langle v_{\text{sw}} \rangle_m$ that can be simplified to

$$\langle i_L \rangle_m \approx \frac{\langle v_{\text{sw}} \rangle_m}{jm\omega_s L + R_s} =: \frac{\langle v_{\text{sw}} \rangle_m}{Z_m} \tag{3.38}$$

The approximation of (3.37) by (3.38) is characteristic of a singular perturbation approach [90–92]. A small parameter (in this case, the switching period) quantifies a separation of

time-scales. As a result, the state vector resulting from generalized averaging is recognized to consist of slow state variables (the 0^{th} order coefficients in (3.25) corresponding to the average component of the state variables) and fast state variables (the higher order coefficients in (3.25) modeling the inductor current ripple). The approximation of (3.38) yields a reduced-order model of dimension N that approximates the behavior of the full-order generalized averaged model. Note that the approach for model order reduction does not simply ignore the *contributions* of the nonzero-order coefficients to the averaged dynamics. Instead, the procedure ignores the *dynamics* of these coefficients, treating the inductor current ripple as a quasi-static quantity that can be calculated from the average capacitor voltages and switching functions. Appendix A provides mathematical background justifying the singular perturbation approach in this context.

Applying (3.38), each of the capacitor voltage dynamics can be expressed as

$$\langle \dot{v_{c,k}} \rangle_0 = \frac{1}{C_k} \left(2\text{Re} \left\{ \sum_{m=1}^{n} \langle \Delta s_k \rangle_m^* \frac{\langle v_{\text{sw}} \rangle_m}{Z_m} \right\} \right) \tag{3.39}$$

Using (3.24), the right-hand side of (3.39) is expanded as

$$\begin{aligned} &2\text{Re} \left\{ \begin{bmatrix} \frac{-\langle \Delta s_k \rangle_1^*}{C_k} \\ \vdots \\ \frac{-\langle \Delta s_k \rangle_n^*}{C_k} \end{bmatrix}^{\text{T}} \begin{bmatrix} \frac{\langle \Delta s_1 \rangle_1}{Z_1} & \cdots & \frac{\langle \Delta s_M \rangle_1}{Z_1} \\ \vdots & \ddots & \vdots \\ \frac{\langle \Delta s_1 \rangle_n}{Z_n} & \cdots & \frac{\langle \Delta s_M \rangle_M}{Z_n} \end{bmatrix} \right\} \begin{bmatrix} \langle v_{c,1} \rangle_0 \\ \vdots \\ \langle v_{c,M} \rangle_0 \end{bmatrix} \\ &+ 2\text{Re} \left\{ \begin{bmatrix} \frac{\langle \Delta s_k \rangle_1^*}{C_k} \\ \vdots \\ \frac{\langle \Delta s_k \rangle_n^*}{C_k} \end{bmatrix}^{\text{T}} \begin{bmatrix} \frac{\langle s_{n_c} \rangle_1}{Z_1} \\ \vdots \\ \frac{\langle s_{n_c} \rangle_n}{Z_n} \end{bmatrix} \right\} \langle v_{\text{in}} \rangle_0 \end{aligned} \tag{3.40}$$

Recalling that (3.40) yields a scalar value of $\langle \dot{v_{c,k}} \rangle_0$, the reduced-order dynamics for all flying capacitors C_k can be expressed as a vector concatenation of (3.40) for each capacitor C_k. The reduced-order model describing the capacitor voltage dynamics is given by

$$\begin{bmatrix} \langle \dot{v_{c,1}} \rangle_0 \\ \vdots \\ \langle \dot{v_{c,M}} \rangle_0 \end{bmatrix} = \boldsymbol{A_c} \cdot \begin{bmatrix} \langle v_{c,1} \rangle_0 \\ \vdots \\ \langle v_{c,M} \rangle_0 \end{bmatrix} + \boldsymbol{B_c} \cdot \langle v_{\text{in}} \rangle_0 \tag{3.41}$$

where the matrix $\boldsymbol{A_c}$ can be expressed as the product of two component matrices $\boldsymbol{A_{c,\alpha}}$ and $\boldsymbol{A_{c,\beta}}$ as

$$\boldsymbol{A_c} = 2\text{Re} \left\{ \boldsymbol{A_{c,\alpha}} \cdot \boldsymbol{A_{c,\beta}} \right\} \tag{3.42}$$

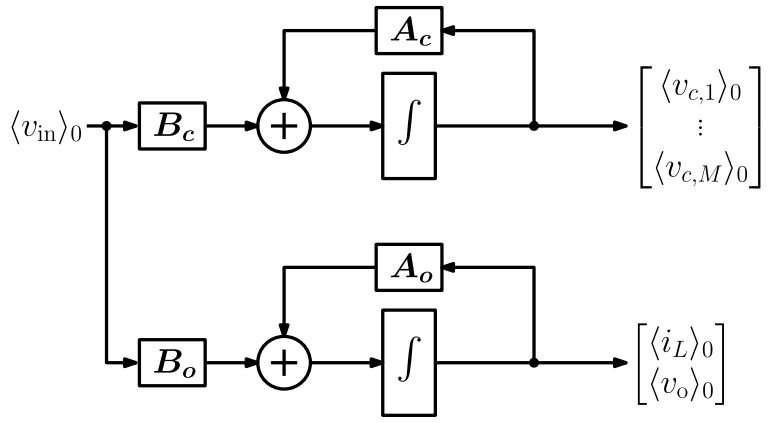


Figure 3.6: Block diagram representation of reduced-order model, showing the decoupled capacitor voltage and output filter dynamics.

with

$$\boldsymbol{A_{c,\alpha}} = \begin{bmatrix} \frac{\langle \Delta s_1\rangle_1^*}{C_1} & \cdots & \frac{\langle \Delta s_1\rangle_n^*}{C_1} \\ \vdots & \ddots & \vdots \\ \frac{\langle \Delta s_M\rangle_1^*}{C_M} & \cdots & \frac{\langle \Delta s_M\rangle_n^*}{C_M} \end{bmatrix} \tag{3.43}$$

$$\boldsymbol{A_{c,\beta}} = \begin{bmatrix} \frac{-\langle \Delta s_1\rangle_1}{Z_1} & \cdots & \frac{-\langle \Delta s_M\rangle_1}{Z_1} \\ \vdots & \ddots & \vdots \\ \frac{-\langle \Delta s_1\rangle_n}{Z_n} & \cdots & \frac{-\langle \Delta s_M\rangle_n}{Z_n} \end{bmatrix} \tag{3.44}$$

The matrix $\boldsymbol{B_c}$ is similarly decomposed as

$$\boldsymbol{B_c} = 2\mathrm{Re}\left\{\boldsymbol{B_{c,\alpha}}\cdot\boldsymbol{B_{c,\beta}}\right\} \tag{3.45}$$

$$\boldsymbol{B_{c,\alpha}} = \begin{bmatrix} \frac{\langle \Delta s_1\rangle_1^*}{C_1} & \cdots & \frac{\langle \Delta s_1\rangle_n^*}{C_1} \\ \vdots & \ddots & \vdots \\ \frac{\langle \Delta s_M\rangle_1^*}{C_M} & \cdots & \frac{\langle \Delta s_M\rangle_n^*}{C_M} \end{bmatrix} \tag{3.46}$$

$$\boldsymbol{B_{c,\beta}} = \begin{bmatrix} \frac{\langle s_{n_c}\rangle_1}{Z_1} & \cdots & \frac{\langle s_{n_c}\rangle_n}{Z_n} \end{bmatrix}^{\mathrm{T}} \tag{3.47}$$

From (3.19) and (3.21), the average capacitor voltages do not couple into the average inductor current and output voltage dynamics under the assumption that $\langle \Delta s_k\rangle_0 = 0$. The complete reduced-order model including the averaged inductor current and output voltage

dynamics is therefore

$$\begin{bmatrix} \dot{\langle v_{c,1}\rangle_0} \\ \vdots \\ \dot{\langle v_{c,M}\rangle_0} \\ \hline \dot{\langle i_L\rangle_0} \\ \dot{\langle v_o\rangle_0} \end{bmatrix} = \hat{\boldsymbol{A}} \cdot \begin{bmatrix} \langle v_{c,1}\rangle_0 \\ \vdots \\ \langle v_{c,M}\rangle_0 \\ \hline \langle i_L\rangle_0 \\ \langle v_o\rangle_0 \end{bmatrix} + \hat{\boldsymbol{B}} \cdot \langle v_{\text{in}}\rangle_0 \tag{3.48}$$

where

$$\hat{\boldsymbol{A}} = \left[\begin{array}{c|c} \boldsymbol{A_c} & \boldsymbol{0} \\ \hline \boldsymbol{0} & \boldsymbol{A_o} \end{array}\right], \qquad \hat{\boldsymbol{B}} = \left[\begin{array}{c} \boldsymbol{B_c} \\ \hline \boldsymbol{B_o} \end{array}\right] \tag{3.49}$$

In the reduced-order system, the sub-matrices $\boldsymbol{A_c}$ and $\boldsymbol{B_c}$ are given by (3.42) and (3.45) respectively. Fig. 3.6 illustrates the reduced-order system as a block diagram, showing the decoupling between the average capacitor voltage dynamics and the dynamics of the inductor current and output voltage. Sub-matrices $\boldsymbol{A_o}$ and $\boldsymbol{B_o}$ describe the dynamics of these output filter states with

$$\boldsymbol{A_o} = \begin{bmatrix} -\frac{R_s}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & -\frac{1}{RC_o} \end{bmatrix}, \qquad \boldsymbol{B_o} = \begin{bmatrix} \langle s_{n_c}\rangle_0 \\ 0 \end{bmatrix} \tag{3.50}$$

The reduced-order model in this work recovers the quasi-steady-state harmonic model obtained in [72], where the assumption of time-scale separation between the capacitor voltage and inductor current ripple dynamics is made without rigorous justification. By comparison, this work identifies the switching frequency as the converter design parameter that quantifies this separation.

To illustrate the validity of the reduced-order model, Fig. 3.7 compares the eigenvalues of the matrices $\boldsymbol{A}$ (corresponding to the full generalized averaged model) and $\hat{\boldsymbol{A}}$ (corresponding to the reduced-order model) for a 4-level FCML converter operating at $D = 0.5$ with three inductor current harmonics modeled ($n = 3$). The reduced-order model captures the slowest eigenvalues accurately, and predicts the dominant complex-conjugate pole pair with a relative error of 2%. Using the theory of eigenvalue participations [123, 124], it can be shown that this pair of eigenvalues participates solely in the capacitor voltages. The reduced-order model also captures both real eigenvalues participating in the output filter states. Observing Fig. 3.7, the full generalized averaged model only additionally models the three eigenvalue pairs participating in the inductor current harmonics. These decay quickly relative to the dominant eigenvalue participating in the capacitor voltages, justifying the singular perturbation approach.

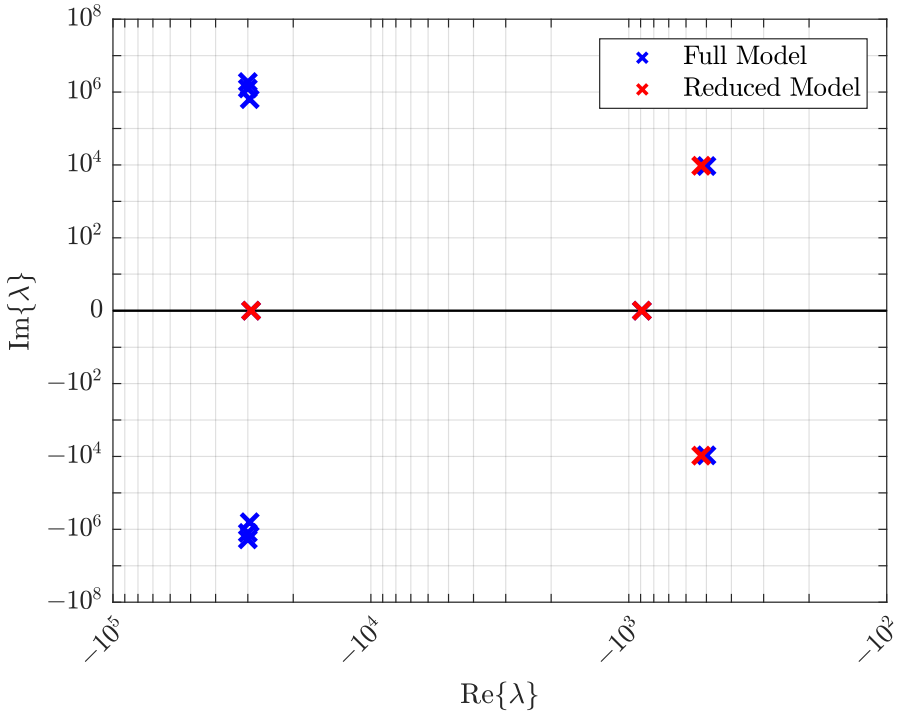


Figure 3.7: Eigenvalues characterizing the natural balancing dynamics of a 4-level FCML converter operating at $D = 0.5$ as predicted by the full generalized averaged model (3.26) and the reduced-order model of (3.48). The reduced-order model accurately captures the dominant eigenvalues which participate entirely in the capacitor voltage dynamics. In the full and reduced-order model, $L = 10\,\mu\mathrm{H}$, $C = 8.8\,\mu\mathrm{F}$, $R = 8\,\Omega$, $R_s = 0.3\,\Omega$, $V_{\mathrm{in}} = 80\,\mathrm{V}$, and $f_s = 100\,\mathrm{kHz}$.

The coupling between the k^{th} and l^{th} capacitor voltages via the m^{th} harmonic of the inductor current is given by

$$A_{c,klm} = -\frac{\omega_0}{m\Omega_s}\frac{\sin^2(m\pi D)}{(m\pi)^2}\cdot 2\sin\left(\frac{m\pi}{n_c}\right)\cdot\cos\left(\frac{m\,(l-k)}{2\pi}\right) \tag{3.51}$$

where ω_0 and Ω_s are defined as

$$\omega_0 = \frac{1}{\sqrt{LC}}\,, \qquad \Omega_s = \frac{\omega_s}{\omega_0} \tag{3.52}$$

The expression of (3.51) represents the m^{th} harmonic contribution to the corresponding element of $\boldsymbol{A_c}$ in (3.42). For the 4-level FCML converter, the expression in (3.51) normalized to $-\frac{\omega_0}{m\Omega_s}$ is plotted in Fig. 3.8 for different values of m, and gives insight into the contributions

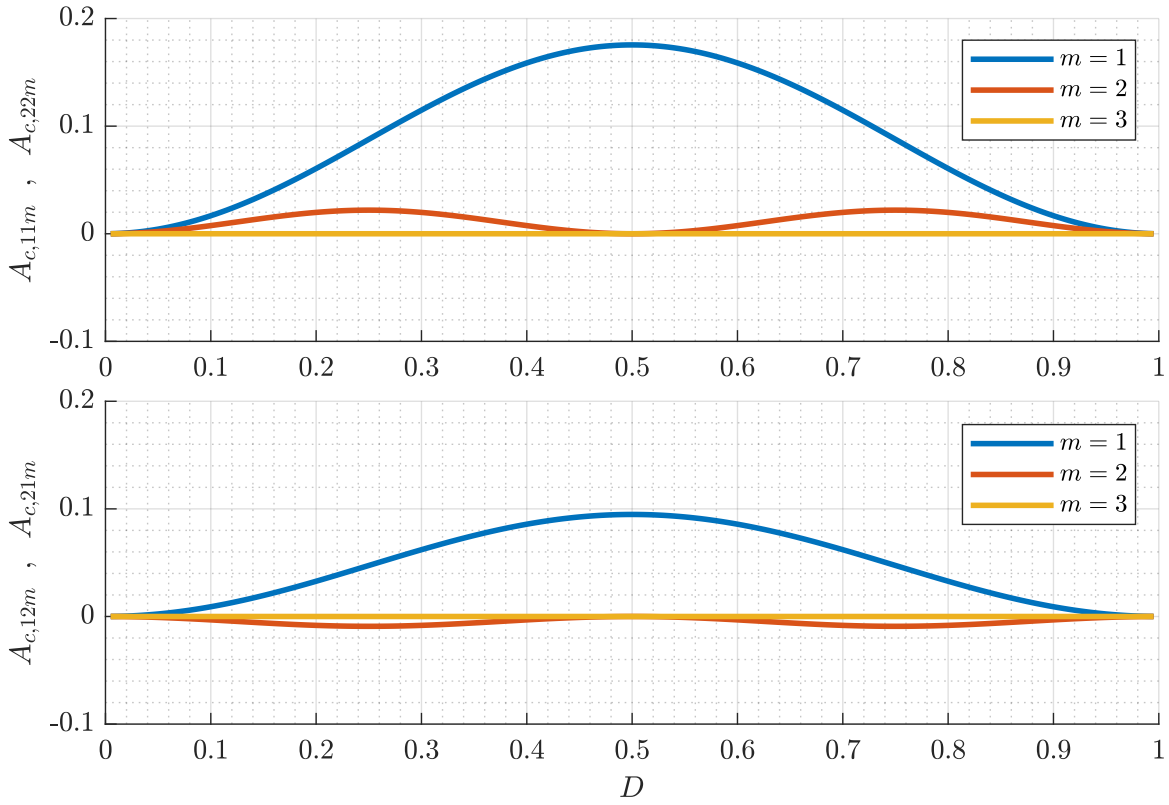


Figure 3.8: Plots of $A_{c,klm}$ as given by (3.51) normalized to $-\frac{\omega_0}{m\Omega_s}$ for a 4-level converter. The curves depict the contribution of different inductor current harmonics to the capacitor dynamics. For a small range of duty ratios centered at $D = 0.5$, the contributions of the second and third harmonics are negligible.

of different inductor current harmonics for a given design. First, it is clear from the term $\sin(m\pi/n_c)$ in (3.51) that for an N-level converter, inductor current harmonics that are multiples of $n_c = N - 1$ (i.e., $m = kn_c,\ k \in \mathbb{N}$) never contribute to the capacitor voltage dynamics. Second, from the term $\sin^2(m\pi D)$, the m^{th} harmonic of the inductor current does not contribute to the capacitor voltage dynamics when the duty ratio satisfies $mD \in \mathbb{N}$. These findings answer why the second, fourth, fifth, and sixth harmonics of the inductor current have no impact on the capacitor dynamics for the 6-level converter operating at $D = 0.5$, as shown in Fig. 3.5. For the 4-level converters, Fig. 3.8 can be used to qualitatively identify ranges of duty ratios where the contributions of particular harmonics may be ignored. For a small range of duty ratios centered at $D = 0.5$, the contributions to $\boldsymbol{A_c}$ from the second and third harmonics are minor compared to that of the first harmonic.

Direct inspection of the elements of $\boldsymbol{A_c}$ given by (3.51) can only reliably yield conservative estimates of which harmonics can be ignored, because the contributions of different harmonics

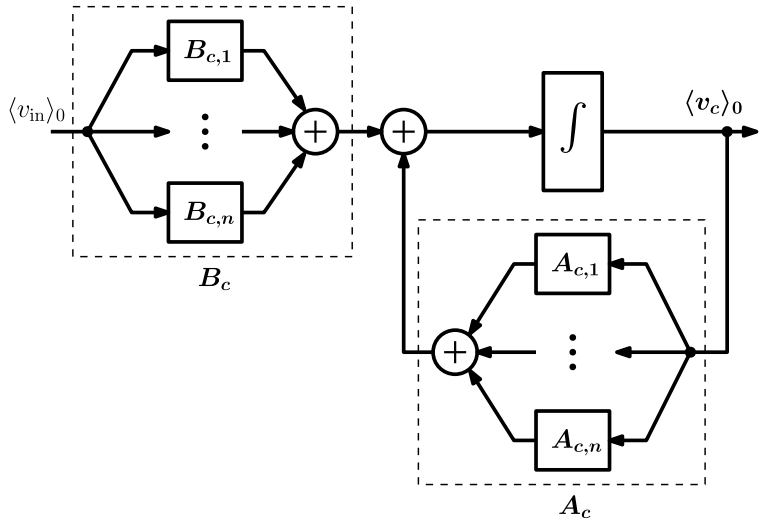


Figure 3.9: Block-diagram representation of the capacitor voltage dynamics after model-order reduction. The feedback elements model the coupling between capacitors due to each inductor current harmonic as given by (3.53).

occur via a parallel form shown in Fig. 3.9. This structure is revealed by re-expressing the matrix $\boldsymbol{A_c}$ as

$$\boldsymbol{A_c} = \sum_{m=1}^{n} \boldsymbol{A_{c,m}} =: \sum_{m=1}^{n} 2\text{Re}\left\{ \begin{bmatrix} \frac{\langle \Delta s_1 \rangle_m^*}{C_1} \\ \vdots \\ \frac{\langle \Delta s_M \rangle_m^*}{C_M} \end{bmatrix} \begin{bmatrix} \frac{-\langle \Delta s_1 \rangle_m}{Z_m} & \cdots & \frac{-\langle \Delta s_M \rangle_m}{Z_m} \end{bmatrix} \right\} \tag{3.53}$$

In this representation, the different inductor current harmonics contribute to the average capacitor voltage dynamics via constituent matrices $\boldsymbol{A_{c,m}}$ that are summed. The poles associated with the capacitor voltages are not directly predicted by the relative magnitudes of elements of these constituent matrices, but additionally depend on the effect of the summation on the characteristic polynomial of $\boldsymbol{A_c}$, a more complex matter.

The following section presents a mathematical framework for quantitatively evaluating the contributions of different inductor current harmonics to the poles associated with capacitor voltages. This framework is subsequently used to identify the number of harmonics that must be modeled in several case studies where the converter design and operating point are varied.

Impact of Number of Harmonic Terms Included in Model

The contributions of different inductor current harmonics to the matrix $\boldsymbol{A_c}$ can be studied from a modal perspective—i.e., how the dominant eigenvalues participating in the capacitor voltage dynamics change as the number of modeled harmonics increases. The minimum model complexity is the harmonic order past which the change in the predicted eigenvalues converges to within a predefined tolerance (defined here as 5% relative error).

As the matrix $\hat{\boldsymbol{A}}$ characterizing the reduced-order system in (3.48) is block-diagonal, its eigenvalues are the collective eigenvalues of its individual blocks. Each eigenvalue of $\hat{\boldsymbol{A}}$ only participates in the state variables associated with its corresponding block. Thus, in the reduced-order model for an N-level FCML converter, there are $M = N - 2$ eigenvalues that participate only in the capacitor voltage states. Of these eigenvalues, the dominant (or slowest) eigenvalues are of the greatest interest as they quantify the speed of the natural capacitor voltage balancing. These are also the eigenvalues that closed-loop controllers such as those discussed in Section 3.4 seek to move to achieve a desired time-domain balancing characteristic. Thus, considering that all eigenvalues of the open-loop system have negative real parts [125], one can optionally study a subset of the $p \leq M$ eigenvalues with real parts of smallest magnitude. Generally, for FCML converters with $N \geq 4$, capacitor voltages exhibit a dominant second-order characteristic [77] and $p = 2$ suffices. In special cases, the system may be better characterized by a dominant third-order characteristic, such as in the 5-level converter case studied in [77]. As an *ansatz*, the case studies appearing in this section consider $p = 2$ for even-level converters and $p = 3$ for odd-level converters.

To start the analysis, the matrix $\boldsymbol{A_c}$ corresponding to the 0^{th}-order generalized averaged model ($n = 0$) is studied. Notated as $\boldsymbol{A_{c,0}}$, this matrix is given simply as $\boldsymbol{A_{c,0}} = \boldsymbol{0_{M\times M}}$, because the standard averaged model predicts zero capacitor voltage dynamics. As a next step, the eigenvalues of $\boldsymbol{A_{c,1}}$ (the capacitor voltage dynamics when one inductor current harmonic is modeled) can be studied. Generally, there are no longer M eigenvalues at the origin, and some eigenvalues near the imaginary axis have nonzero participation in one or more capacitor states. Ordering the eigenvalues from 1 to M by increasing magnitude of their real parts, the first p eigenvalues are collected as a vector

$$\boldsymbol{\Lambda_1} := \begin{bmatrix} \lambda_1(\boldsymbol{A_{c,1}}) & \cdots & \lambda_p(\boldsymbol{A_{c,1}}) \end{bmatrix}^{\mathrm{T}} \tag{3.54}$$

Likewise the p dominant eigenvalues of $\boldsymbol{A_{c,2}}$ (the model including the second harmonic) can be collected as

$$\boldsymbol{\Lambda_2} := \begin{bmatrix} \lambda_1(\boldsymbol{A_{c,2}}) & \cdots & \lambda_p(\boldsymbol{A_{c,2}}) \end{bmatrix}^{\mathrm{T}} \tag{3.55}$$

The maximum relative error in the prediction of the dominant p eigenvalues between $\boldsymbol{A_{c,2}}$ and $\boldsymbol{A_{c,1}}$ can be expressed via the ℓ^∞-norm as

$$e_1 = \left\| (\boldsymbol{\Lambda_2} - \boldsymbol{\Lambda_1}) \oslash \boldsymbol{\Lambda_1} \right\|_\infty \tag{3.56}$$

where $\oslash$ denotes element-wise division. Note that if $\boldsymbol{A_{c,1}}$ has any eigenvalues at the origin, $e_1 = \infty$.

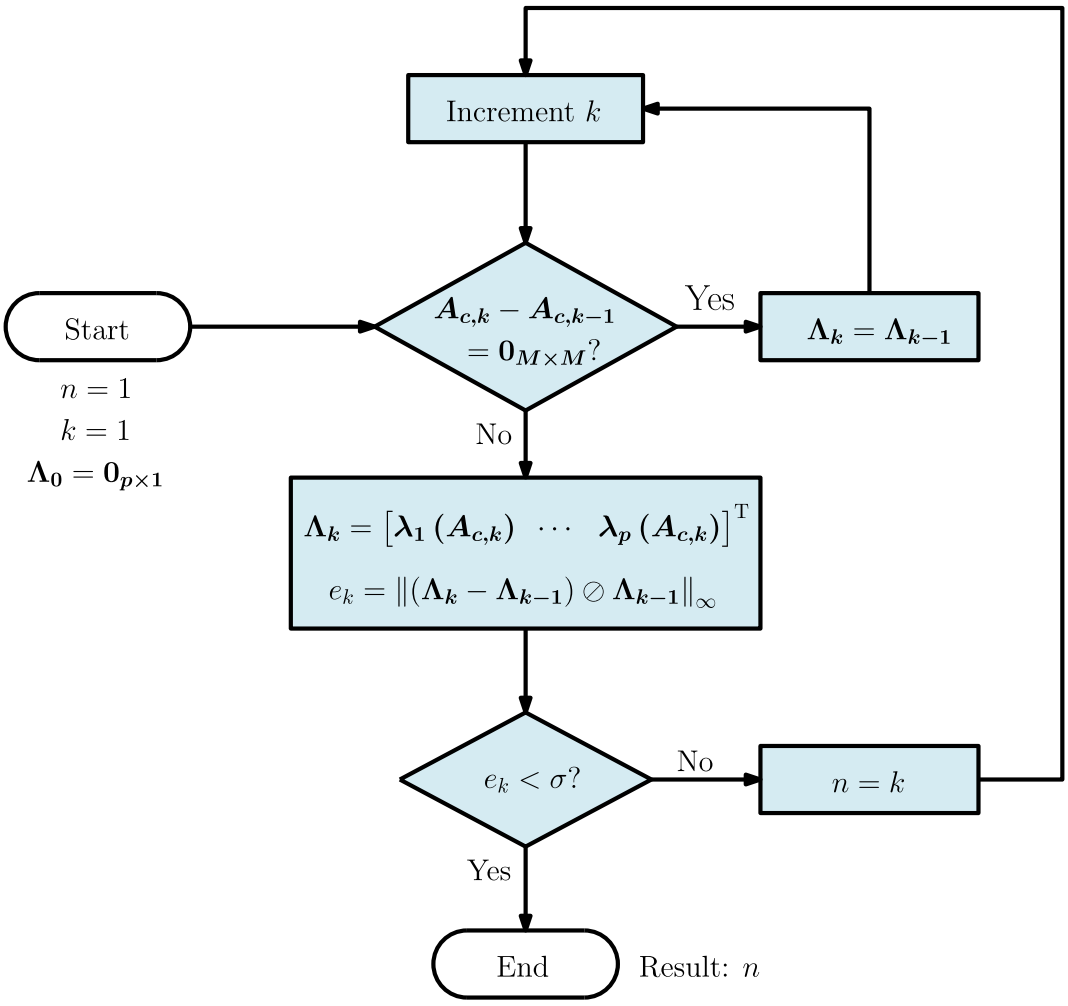


Figure 3.10: Flowchart depicting the procedure proposed in this section to determine the minimum number of inductor current harmonics required to capture the capacitor voltage dynamics.

The steps outlined above can be repeated for $\boldsymbol{A_{c,3}}$, $\boldsymbol{A_{c,4}}$, and so on. In each step, if $\boldsymbol{A_{c,k}} - \boldsymbol{A_{c,k-1}} \neq \mathbf{0}_{M\times M}$, the relative error is evaluated as

$$e_k = \|(\mathbf{\Lambda_k} - \mathbf{\Lambda_{k-1}}) \oslash \mathbf{\Lambda_{k-1}}\|_\infty \tag{3.57}$$

or set to $e_k = \infty$ if $\boldsymbol{A_{c,k-1}}$ has any eigenvalues at the origin. Otherwise, if $\boldsymbol{A_{c,k}} - \boldsymbol{A_{c,k-1}} = \mathbf{0}_{M\times M}$, the procedure assigns $\mathbf{\Lambda_k} = \mathbf{\Lambda_{k-1}}$. In this manner, the procedure also does not evaluate relative error for inductor current harmonics that do not contribute to the capacitor voltage dynamics as discussed in Section 3.3. The iterative procedure is continued until the relative error e_k falls within a predefined tolerance σ (defined here as $\sigma = 5\%$). At this

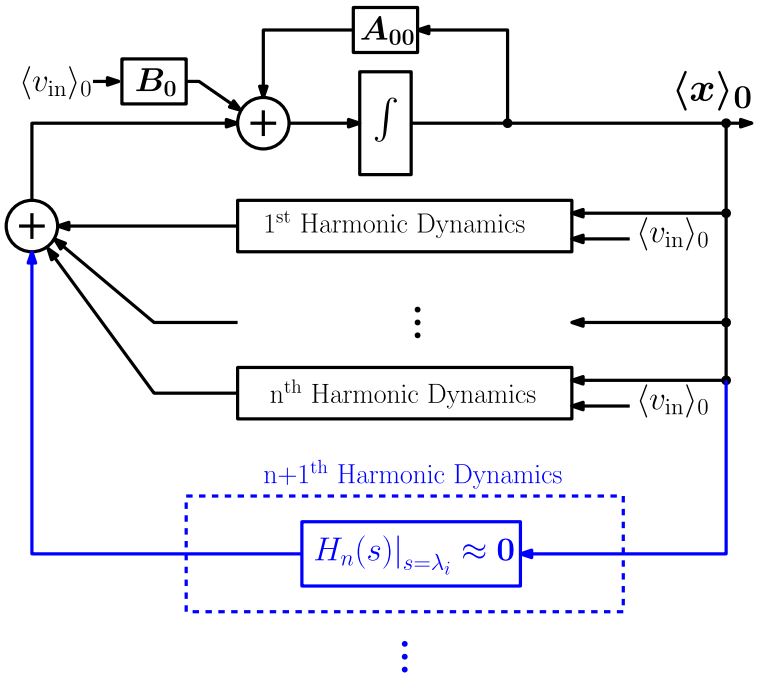


Figure 3.11: A Selective Modal Analysis (SMA) [123, 124, 126, 127] perspective on the n-term approximation of the generalized averaged model. The contribution of harmonics of order $n+1, n+2, \ldots, \infty$ to the p dominant modes studied are assumed to be zero.

point, the minimum number of required harmonics n is the previous value of k for which $\boldsymbol{A_{c,k}} \neq \boldsymbol{0_{M \times M}}$.

The procedure described thus far to determine the minimum number of required harmonic terms is summarized in Fig. 3.10. This section presents one possible method for analyzing the incremental behavior of the eigenvalues as the number of harmonics terms is increased, using the same relative eigenvalue error metric as [126]. Modifications of the proposed procedure, such as weighting the changes in different eigenvalues depending on their locations or using a different norm in (3.57), can be easily incorporated in future studies.

The approach described above can be examined from the perspective of selective modal analysis [123, 124, 126, 127] by showing the n-term approximation of the reduced-order model in the context of the full generalized averaged model. As illustrated in Fig. 3.11, by assuming that the eigenvalues of model converge within n harmonics, the procedure described above claims that the harmonics of order $n+1, n+2, \ldots, \infty$ do not have any impact on the p dominant modes being analyzed. The extent to which this claim is true depends on the behavior of the feedback dynamics corresponding to these higher order harmonics at the frequencies $\lambda_1, \ldots, \lambda_p$. In the framework of selective modal analysis, the procedure described in this section claims that the neglected feedback elements have approximately zero gain at the frequencies of interest and can therefore be regarded as decoupled from the

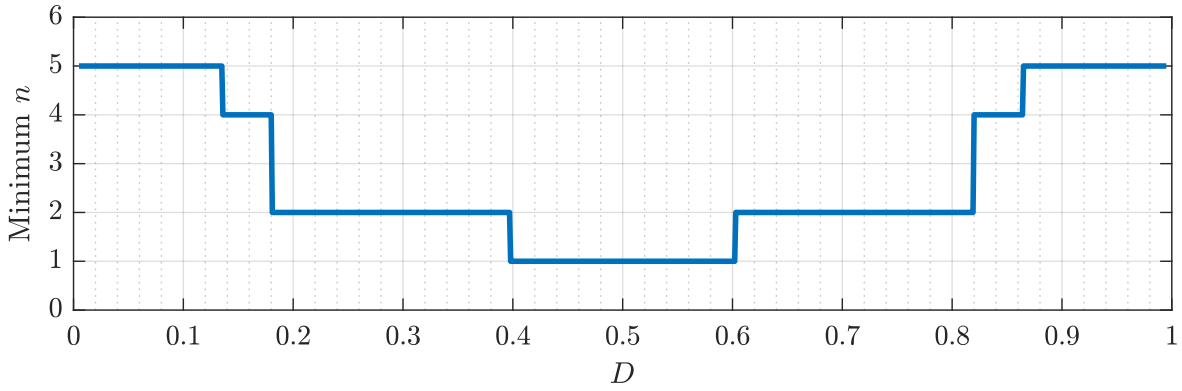


Figure 3.12: Minimum number of inductor current harmonics required to model capacitor voltage dynamics in a 4-level converter, determined from the procedure outlined in Section 3.3. For the 4-level converter, the results obtained from the procedure confirms the qualitative conclusions obtained by visual examination of Fig. 3.8. The converter parameters used in this example are $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R_s = 0.3\,\Omega$, $V_{\text{in}} = 80\,\text{V}$, $I_{\text{out}} = 5\,\text{A}$, $R = V_{\text{in}}D/I_{\text{out}}$, and $f_s = 100\,\text{kHz}$.

capacitor voltage dynamics at these frequencies. In reality, the remaining harmonics do have some small impact on the capacitor voltage dynamics as the neglected feedback dynamics do not truly have zero gains as assumed. In particular, the eigenvectors corresponding to the dominant modes being studied may continue to vary as additional harmonics are included. As will be demonstrated next, the results of the procedure described in this section can be verified through comparison to circuit simulation and experimental hardware. Therefore, further analysis of the impacts of ignoring the higher-order harmonics is deferred for future work.

The obtained minimum number of harmonics required to model a 4-level FCML converter as a function of the duty ratio is shown in Fig. 3.12. The results obtained from the quantitative procedure match the qualitative conclusions obtained by visual examination of Fig. 3.8. As predicted, the second harmonic of the inductor current has negligible contribution to the capacitor dynamics at duty ratios between $D = 0.4$ and $D = 0.6$. Outside this range, the second harmonic cannot be ignored. Step-response simulations for the converter operating at $D = 0.25$ in Fig. 3.13 and $D = 0.50$ in Fig. 3.14 confirm the conclusions of the study. For the converter operating at $D = 0.25$, including the second harmonic allows the model to match the result of circuit simulation with 0.3% relative error in the dominant pole location. By comparison, for operation at $D = 0.50$, the dominant pole location is predicted with 0.5% relative error using only the first harmonic, as shown in Fig. 3.14.

Fig. 3.15 plots the minimum number of harmonics required to model the 6-level FCML converter as a function of the converter duty ratio. The analysis confirms the time domain verifications of Fig. 3.4 and Fig. 3.5, where $n = 2$ and $n = 7$ are required to accurately

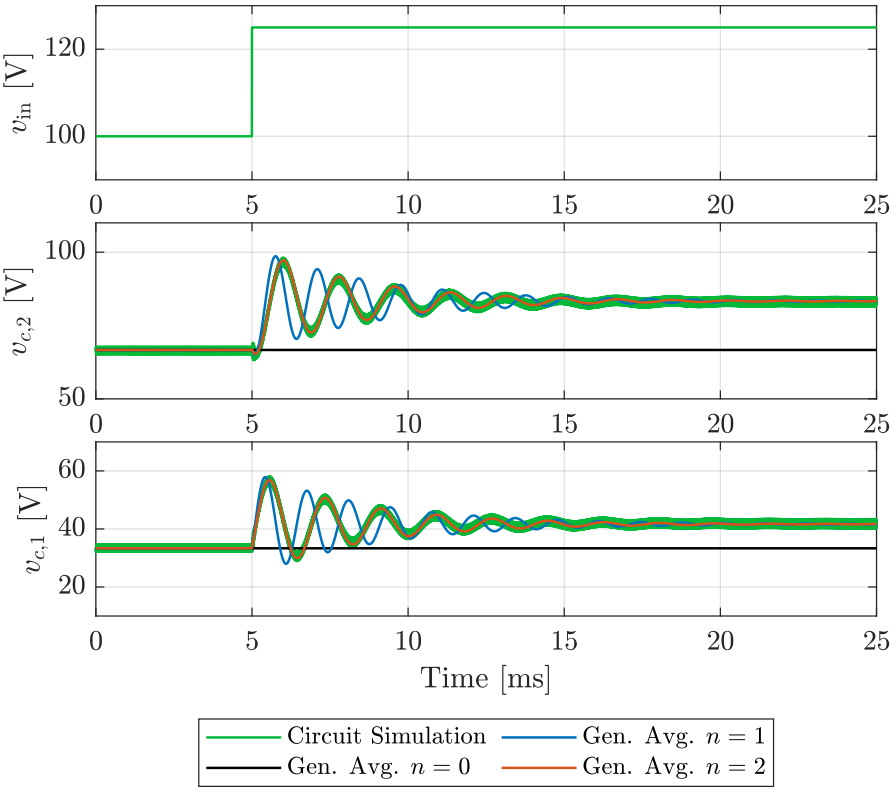


Figure 3.13: Simulated and modeled capacitor voltage responses for a 4-level FCML converter operating at $D = 0.25$, varying the total numbers of harmonics modeled n. The model with $n = 2$ accurately captures the step-transient response. In the circuit simulation and model, $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R = 2.5\,\Omega$, $R_s = 0.3\,\Omega$, and $f_s = 100\,\text{kHz}$. The line voltage is stepped from 100 V to 125 V.

capture the dominant capacitor voltage behavior for $D = 0.35$ and $D = 0.5$ respectively.

When the duty ratio approaches $D = 0$ and $D = 1$, the minimum required n increases, as the contributions of all harmonics become smaller and of comparable magnitude. To restrict the total number of harmonics modeled to finite values and avoid distortion of the vertical axis in plots such as Fig. 3.12 and Fig. 3.15, n is restricted in this section to a maximum value of $n = 2(N - 1)$. In the sense of this restriction, plots such as Fig. 3.12 and Fig. 3.15 are only meaningful in the range of $D \in (0.1, 0.9)$.

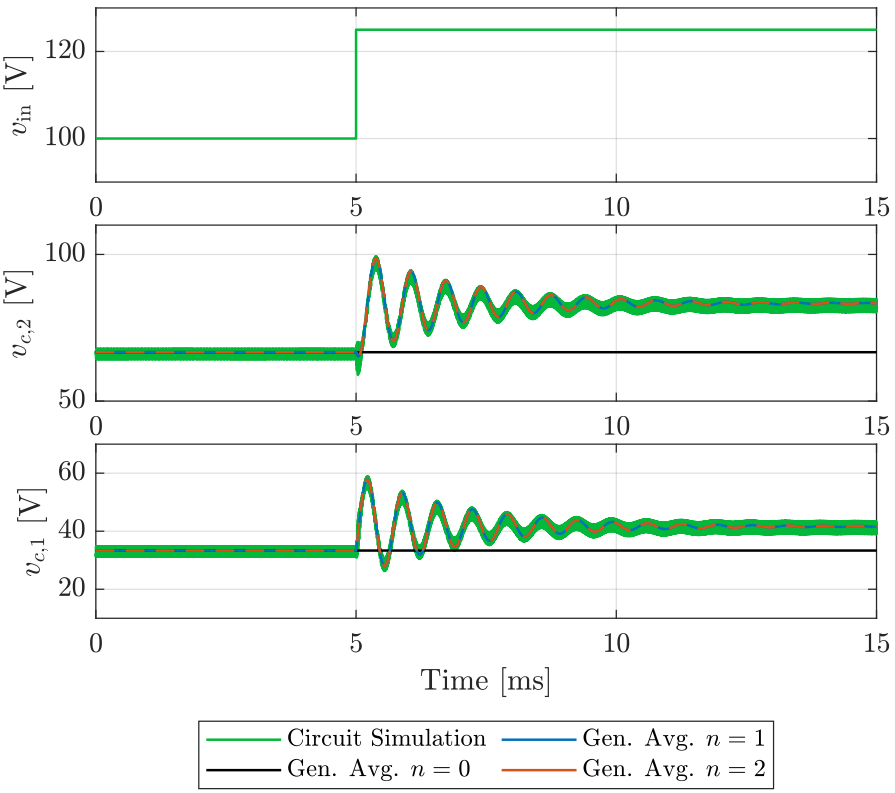


Figure 3.14: Simulated and modeled capacitor voltage responses for a 4-level FCML converter operating at $D = 0.50$, varying the total numbers of harmonics modeled n. The model with $n = 1$ accurately captures the step-transient response. In the circuit simulation and model, $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R = 5\,\Omega$, $R_s = 0.3\,\Omega$, and $f_s = 100\,\text{kHz}$. The line voltage is stepped from 100 V to 125 V.

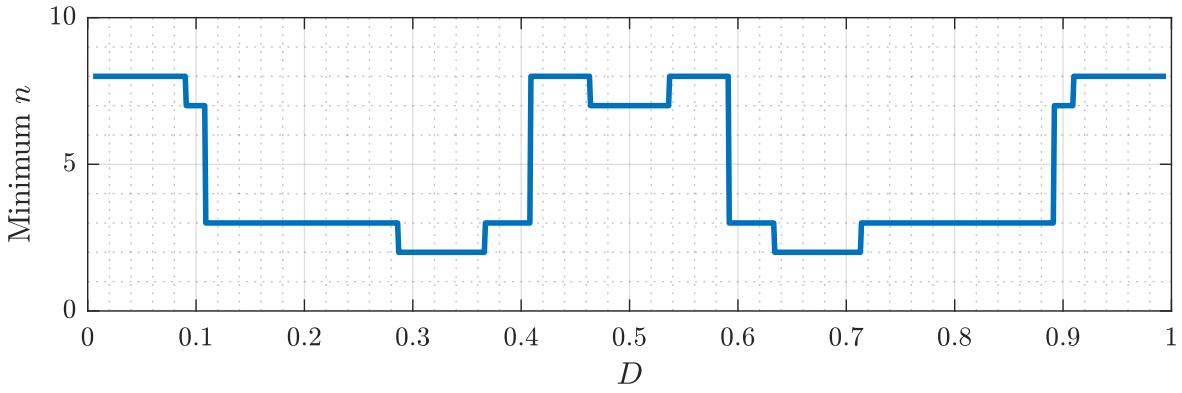


Figure 3.15: Minimum number of inductor current harmonics required to model capacitor voltage dynamics in a 6-level converter, determined from the procedure outlined in Section 3.3. The converter parameters used in this example are $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R_s = 0.3\,\Omega$, $V_{\text{in}} = 80\,\text{V}$, $I_{\text{out}} = 5\,\text{A}$, $R = V_{\text{in}}D/I_{\text{out}}$, and $f_s = 100\,\text{kHz}$.

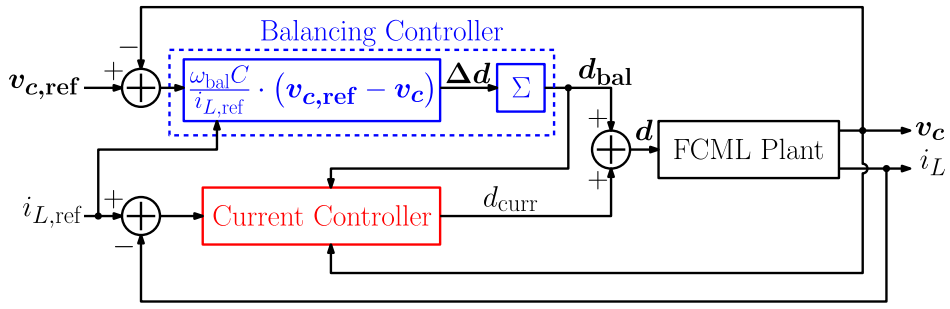


Figure 3.16: Parallel active balancing control structure detailed in Chapter 2.

3.4 Analysis of Closed-Loop Active Balancing Dynamics

The original motivation for studying the generalized averaged converter model was to characterize the conditions under which small-signal instabilities occur in actively balanced systems. The parallel controller introduced in Section 2.3 is redrawn in Fig. 3.16, assuming the designed closed-loop balancing bandwidth for all flying capacitor voltages is ω_{bal}.

A small-signal model derived from the generalized averaged converter model can be used to predict the impact of ω_{bal} and the converter operating point on the stability of the control loop. The model is derived by linearizing the model in (3.26) about the steady-state operating point of symmetric PS-PWM with balanced capacitor voltages. The state vector is decomposed as $\langle \boldsymbol{x} \rangle_{\mathbf{0}} = \overline{\langle \boldsymbol{x} \rangle}_{\mathbf{0}} + \langle \tilde{\boldsymbol{x}} \rangle_{\mathbf{0}}$ where the notation $\overline{\langle \boldsymbol{x} \rangle}_{\mathbf{0}}$ represents the quiescent operating point and the notation $\langle \tilde{\boldsymbol{x}} \rangle_{0}$ represents the small-signal variation.

The small-signal model, derived in detail in Appendix B, is given generally as

$$\langle \dot{\tilde{\boldsymbol{x}}} \rangle_{\mathbf{0}} = \boldsymbol{F} \cdot \langle \tilde{\boldsymbol{x}} \rangle_{\mathbf{0}} + \boldsymbol{G} \cdot \tilde{\boldsymbol{d}} \tag{3.58}$$

$$= (\boldsymbol{F_0} + \boldsymbol{F_1} + \cdots + \boldsymbol{F_n}) \cdot \langle \tilde{\boldsymbol{x}} \rangle_{\mathbf{0}} + (\boldsymbol{G_0} + \boldsymbol{G_1} + \cdots + \boldsymbol{G_n}) \cdot \tilde{\boldsymbol{d}} \tag{3.59}$$

$$=: \left(\boldsymbol{F_0} \cdot \langle \tilde{\boldsymbol{x}} \rangle_{\mathbf{0}} + \boldsymbol{G_0} \cdot \tilde{\boldsymbol{d}} \right) + \left(\boldsymbol{F_r} \cdot \langle \tilde{\boldsymbol{x}} \rangle_{\mathbf{0}} + \boldsymbol{G_r} \cdot \tilde{\boldsymbol{d}} \right) \tag{3.60}$$

where $\boldsymbol{d}$ indicates a vector of switch duty ratios. The matrix indices of (3.59) denote the individual contributions of the different current harmonics. As shown in (3.60), the small-signal dynamics can be grouped into two terms. The first term is the 0^{th}-order small-signal contribution which is identical to the model derived from standard averaging in [96, 114]. The second term is the net ripple contribution from the n modeled inductor current harmonics. In a closed-loop system designed around the standard averaged model, the contribution of the inductor current ripple appears as a plant disturbance. Fig. 3.17 depicts this disturbance within the closed-loop system, where $\boldsymbol{K}$ denotes the small-signal equivalent model of the controller. Note that as the ripple contribution appears as matrix addition in (3.60), its role on the eigenvalues of the closed-loop system is non-trivial. Therefore, in the remainder of

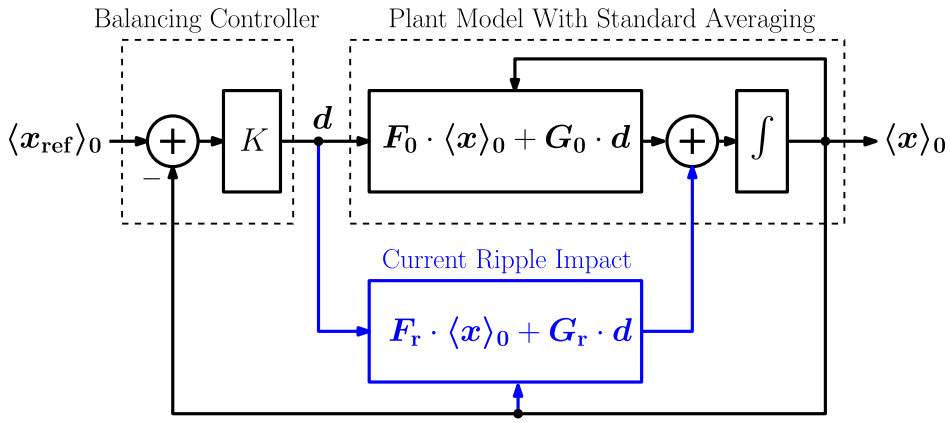


Figure 3.17: Block diagram representation of the closed-loop small-signal system. The additional plant dynamics captured in the generalized averaged model are highlighted and can destabilize active-balanced systems designed around the standard averaged model in light-load conditions.

this chapter, the stability of the closed-loop system is characterized via eigenloci methods, where a single parameter is swept and the trajectories of the closed-loop system's eigenvalues are observed.

In addition to the plant disturbance, computation and modulator delays in the digital control loop and filters in the measurement path can further degrade the stability margins of the closed-loop system. To incorporate these impacts, the state-space depicted in Fig. 3.17 is extended following standard realization methods described in [62, 128] and summarized in Appendix C.

Fig. 3.18 shows simulated capacitor voltages for a 6-level FCML converter implementing the active balancing controller of Chapter 2 with a designed active balancing loop bandwidth of 600 Hz under two different average load current conditions. The converter switching frequency is 100 kHz and capacitor voltage measurements are filtered with a 5 kHz-bandwidth first-order IIR filter. Time $t = 0$ corresponds to the instant at which the closed-loop active balancing control is enabled. For the converter operating at the 3 A load condition, the capacitor voltages exhibit small-signal instability with a characteristic oscillation frequency of 1.92 kHz. At the 5 A load condition, the capacitor voltages are small-signal stable. The stability dependence on the average load current can be verified by studying the eigenloci of the closed-loop system derived from the generalized averaged model. Fig. 3.19 shows the eigenloci of the closed-loop system as the average current is swept from 3 A to 5 A. For the 6-level converter, the modeled closed-loop system has 15 total eigenvalues. Nine eigenvalues occurring in the left half-plane with $\text{Re}\{\lambda\} < -10^4$ are introduced by the integrator in the PI current controller, digital filters associated with capacitor voltages, and controller delays. The right-most complex-conjugate pair of eigenvalues participates in the capacitor voltages, and moves towards the right half-plane as the load current is decreased. The operating point

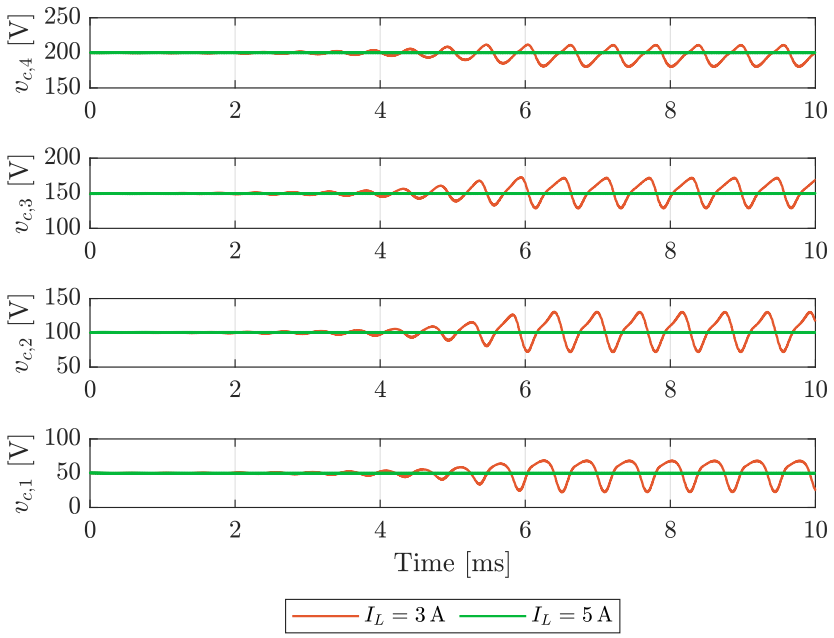


Figure 3.18: Simulated capacitor voltages for a 6-level FCML converter implementing the parallel active balancing controller of [96] at two different average load current conditions. The closed-loop system is destabilized at light-loads by the contribution of the current ripple. In this experiment, $v_{\text{in}} = 250\,\text{V}$, $D = 0.25$, $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R_s = 0.3\,\Omega$, and $f_s = 100\,\text{kHz}$.

corresponding to 3 A average current is verified as unstable, confirming the results in Fig. 3.18.

3.5 Experimental Results

The models presented in this chapter are verified against experimental characterization of the same 12-level FCML converter prototype shown in Fig. 2.10. The hardware is reconfigured in different experiments for lower level counts by bypassing an appropriate number of consecutive switch pairs starting at the input side. Table 2.1 lists the key components comprising the hardware prototype.

Characterization of Natural Balancing Dynamics

To verify the reduced-order model derived in Section 3.3, the dominant modes associated with natural capacitor voltage balancing in a 4-level FCML converter are compared against

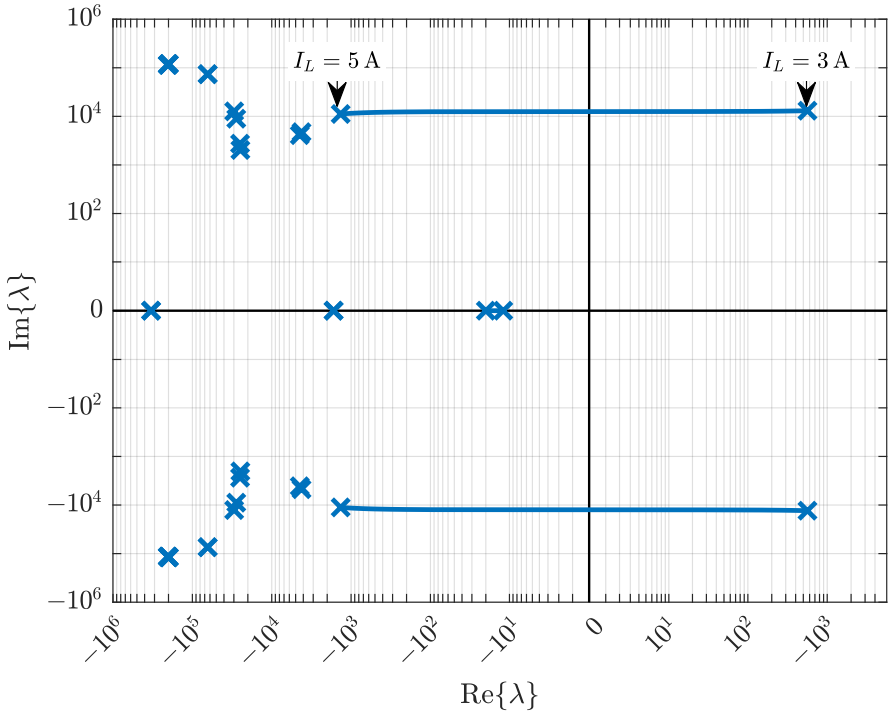


Figure 3.19: Eigenloci of the closed-loop small-signal model derived from generalized averaging as the average load current is varied. The model predicts the same instability observed in the simulation result of Fig. 3.18, with a relative error of 8% in the predicted oscillation frequency. The model is evaluated with $v_{\mathrm{in}} = 250\,\mathrm{V}$, $D = 0.25$, $L = 10\,\mu\mathrm{H}$, $C = 8.8\,\mu\mathrm{F}$, $R_s = 0.3\,\Omega$, and $f_s = 100\,\mathrm{kHz}$.

experimental measurement. The converter is configured with $L = 4.7\,\mu\mathrm{H}$, $C = 8.8\,\mu\mathrm{F}$, $R = 8\,\Omega$, and $f_s = 100\,\mathrm{kHz}$, and the dominant modes are measured from the response to a step-transient in the input voltage as shown in Fig. 3.20. For each duty ratio, the measured data for $v_{c,1}$ after the time instant where the step occurs is fit to the general second-order form

$$x(t) = a_1 e^{-\frac{t}{\tau_\mathrm{d}}} \cos\left(2\pi f_\mathrm{d} t + a_2\right) + a_3 \tag{3.61}$$

using MATLAB's `fmincon` nonlinear optimization solver. The parameters τ_d and f_d represent the time constant and oscillation frequency of the dominant mode respectively. The time constant and oscillation frequency obtained from the measured data are compared in Fig. 3.21 to the results from the reduced-order model with $n = 2$. The model accurately predicts both quantities over the range of duty ratios examined, confirming its application in modeling the natural capacitor voltage dynamics.

The dominant modes associated with natural balancing in a 5-level FCML converter with $L = 10\,\mu\mathrm{H}$, $C = 8.8\,\mu\mathrm{F}$, and $f_s = 75\,\mathrm{kHz}$ are characterized in Fig. 3.22. The dominant time

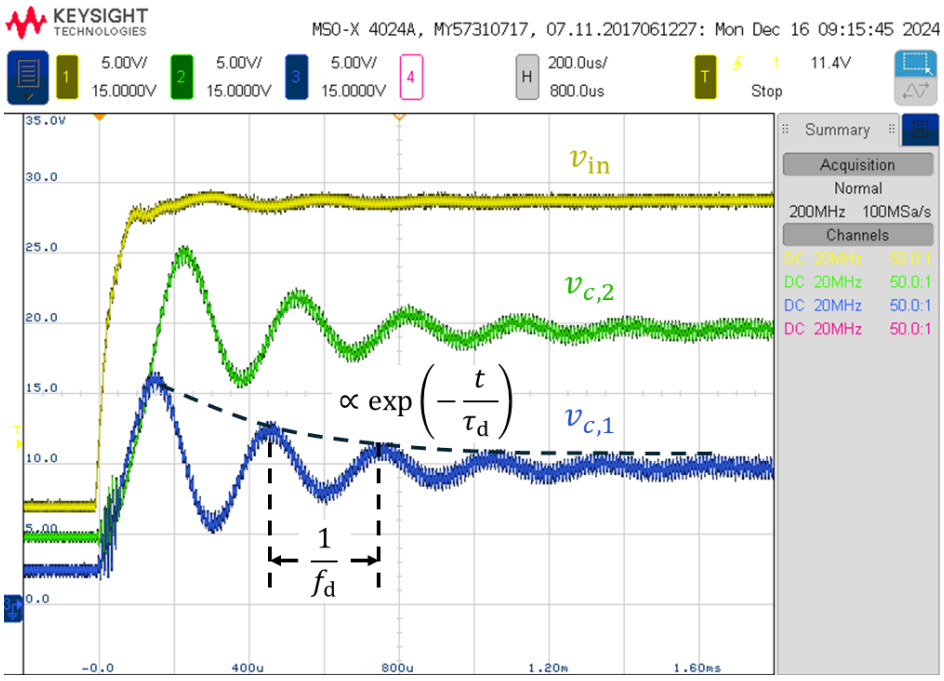


Figure 3.20: Measured response of capacitor voltages in a 4-level FCML converter operating at $D = 0.5$ to a step in the input voltage from 7 V to 30 V. The measured responses are curve-fit to the general form of an exponential response to determine the time constant τ_d and oscillation frequency f_d of the dominant mode. The converter tested has $L = 4.7\,\mu$H, $C = 8.8\,\mu$F, $f_s = 100\,$kHz.

constants predicted by the model match the experimental results for $D < 0.4$ and $D > 0.6$. For converter operation at $D = 0.5$, the generalized averaged model predicts that the dominant time constant approaches infinity, as one of the dominant eigenvalues approaches the origin. This prediction matches the claims of [72, 73, 129, 130] that $D = 0.5$ in the 5-level FCML converter corresponds to a "nominal conversion ratio" where the capacitor voltages exhibit steady-state imbalance. In practice, as observed in the measured data, the balancing time constant remains finite as it additionally depends on unmodeled parasitic converter elements such as the switch drain-source capacitances [80]. In this sense, the conclusions of the generalized averaged model and the models of [72, 73, 129] give conservative predictions of the natural balancing dynamics. For high-performance designs featuring switching devices with reduced parasitic capacitances, these models reveal operating points where the natural balancing dynamics are expected to be too slow for practical use.

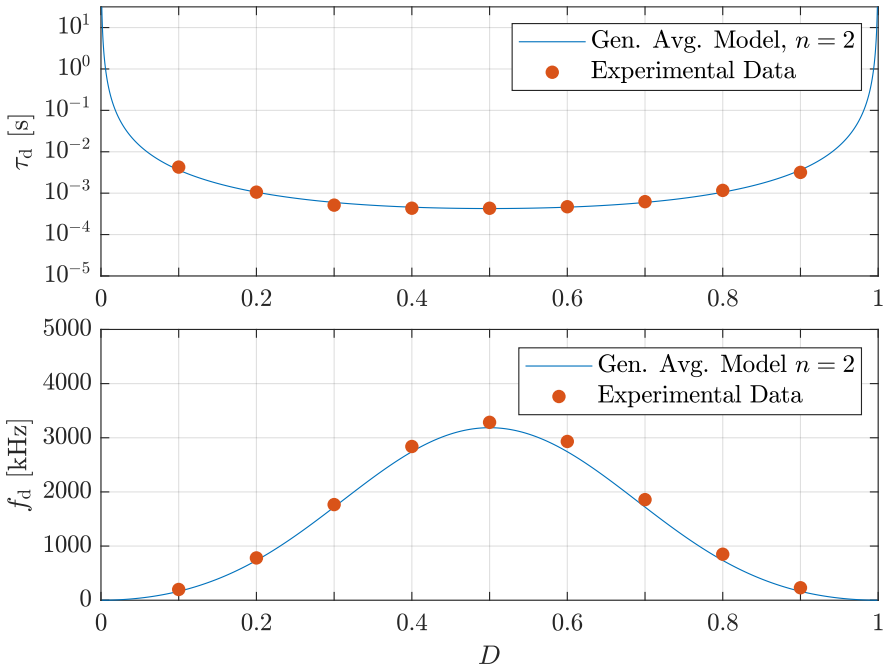


Figure 3.21: Comparison of measured and modeled time constant τ_d and oscillation frequency f_d of the dominant mode characterizing a 4-level FCML converter. The parameters of the dominant mode are extracted from step-response measurements such as those shown in Fig. 3.20, and match the generalized averaged model with $n = 2$. The converter tested has $L = 4.7\,\mu$H, $C = 8.8\,\mu$F, $R = 8.5\,\Omega$, $f_s = 100\,$kHz. The generalized averaged model uses $R_s = 0.3\,\Omega$ considering experimental inductor characterizations in [77].

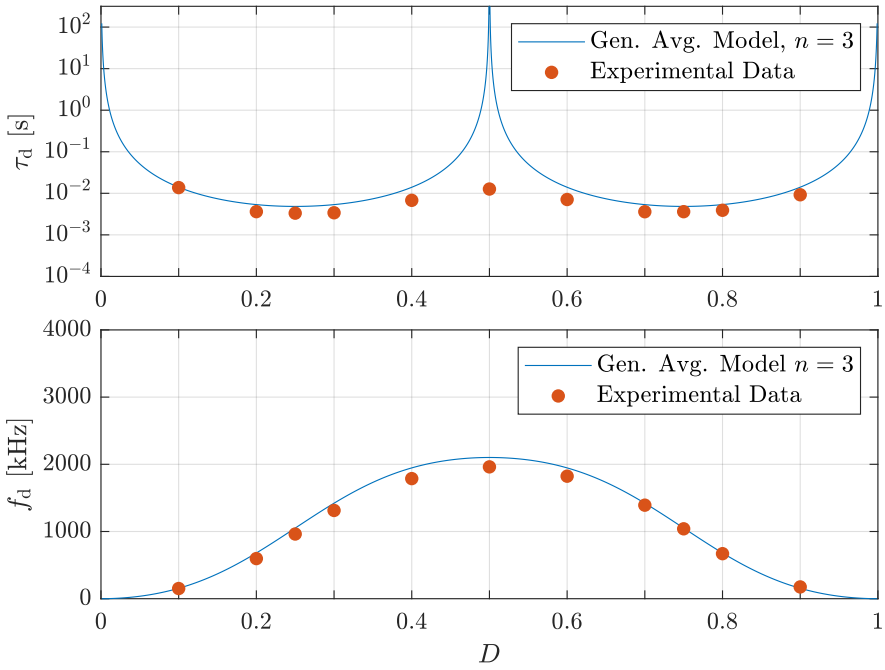


Figure 3.22: Comparison of measured and modeled time constant τ_d and oscillation frequency f_d of the dominant modes characterizing a 5-level FCML converter. The generalized averaged model predicts f_d well, but conservatively estimates that the converter will not balance at the "nominal" conversion ratio of $D = 0.5$ as $\tau_d \to \infty$. Unmodeled parasitic elements present in the hardware such as switch drain-source capacitances re-introduce a finite balancing time constant at this conversion ratio [80]. The converter tested has $L = 4.7\,\mu$H, $C = 8.8\,\mu$F, $R = 8.5\,\Omega$, $f_s = 100\,$kHz. The generalized averaged model uses $R_s = 0.3\,\Omega$ considering experimental inductor characterizations in [77].

Characterization of Active Balancing Systems

Predictions of small-signal instability in closed-loop active balancing systems using the model derived in Section 3.4 are compared to experimental characterization of a 6-level FCML converter with $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, and $f_s = 100\,\text{kHz}$. Fig. 3.23 shows measured small-signal instability in the hardware prototype when the designed active balancing bandwidth is $\omega_{\text{bal}} = 2\pi \cdot 3255\,\text{rad/s}$. By comparison, when $\omega_{\text{bal}} = 2\pi \cdot 1809\,\text{rad/s}$, the closed-loop system is small-signal stable. Fig. 3.24 shows the closed-loop eigenloci predicted by the small-signal model as the active balancing parameter ω_{bal} is swept over the same range under the same operating conditions. The dominant eigenvalue participating in the capacitor voltages moves towards the imaginary axis as the parameter ω_{bal} is increased, and lies in the right half-plane for $\omega_{\text{bal}} = 2\pi \cdot 3255\,\text{rad/s}$.

The block diagram of the closed-loop system shown in Fig. 3.17 and the experimental measurement of small-signal instability motivate a study investigating the limits of active balancing controller design as the load is varied. At light-load conditions, the relative contri-

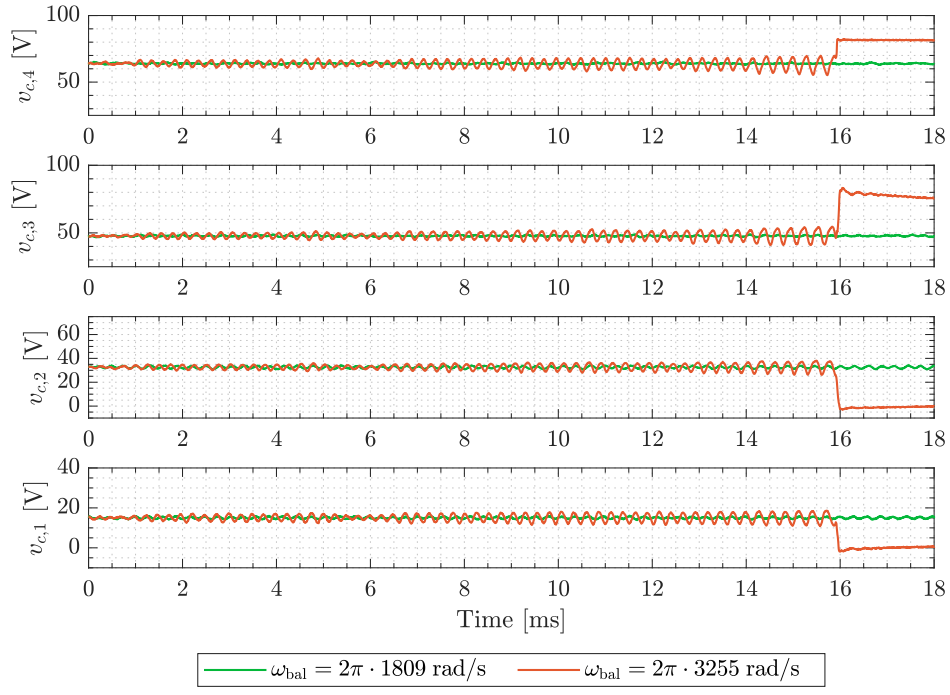


Figure 3.23: Measured capacitor voltage responses in a 6-level FCML converter implementing the active balancing controller of [96] for two different designed balancing loop bandwidths ω_{bal}. The balancing control is enabled at time $t = 0$. For the design with $\omega_{\text{bal}} = 2\pi \cdot 3255\,\text{rad/s}$, the capacitor voltages exhibit small-signal instability. The converter is designed with $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $R = 6.9\,\Omega$, and $f_s = 100\,\text{kHz}$, and operated with $v_{\text{in}} = 80\,\text{V}$ and $D = 0.25$.

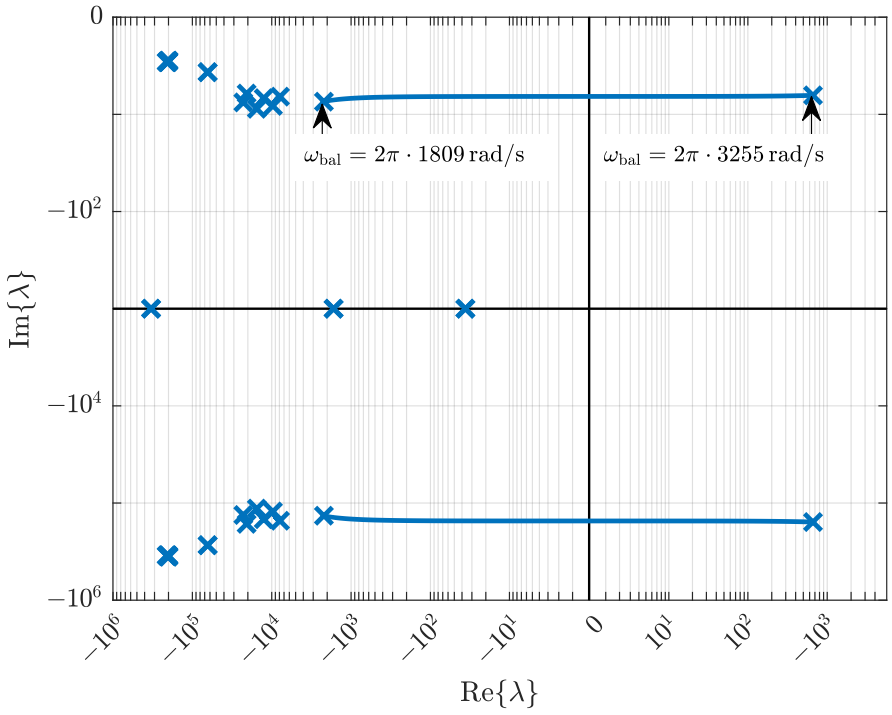


Figure 3.24: Eigenloci of the closed-loop small-signal generalized averaged model for a 6-level converter as the designed balancing loop bandwidth ω_{bal} is varied. The model is derived with $n = 5$ for the same design and operating conditions as the experimental measurement of Fig. 3.23, and verifies that $\omega_{\text{bal}} = 2\pi \cdot 3255\,\text{rad/s}$ corresponds to an unstable design.

bution of the inductor current ripple increases compared to the contribution of the average current, and the system is expected to exhibit small-signal instability at lower values ω_{bal}. To confirm this claim quantitatively, the eigenloci of the small-signal model varying ω_{bal} are evaluated for different values of the average load current. The balancing stability boundary is defined as the maximum value of ω_{bal} that can be designed for a given load current before the system exhibits small-signal instability [96]. Fig. 3.25 shows the theoretical stability boundary determined from the eigenloci of the closed-loop small-signal model and the stability boundary characterized experimentally in [96]. The trend of the predicted stability boundary with respect to the average load current follows the experimental results with a maximum relative error of 20% at 5 A and a minimum relative error of 3% at 10.5 A. Errors in the experimental characterization of the stability boundary in [96] can be attributed to the visual inspection procedure used to identify small-stability, and contribute to the discrepancy observed in Fig. 3.25. The agreement between the trends of the experimental and theoretical stability boundaries confirms that the generalized averaged model predicts the dominant modes that introduce instability as ω_{bal} is varied. Furthermore, for a fixed design

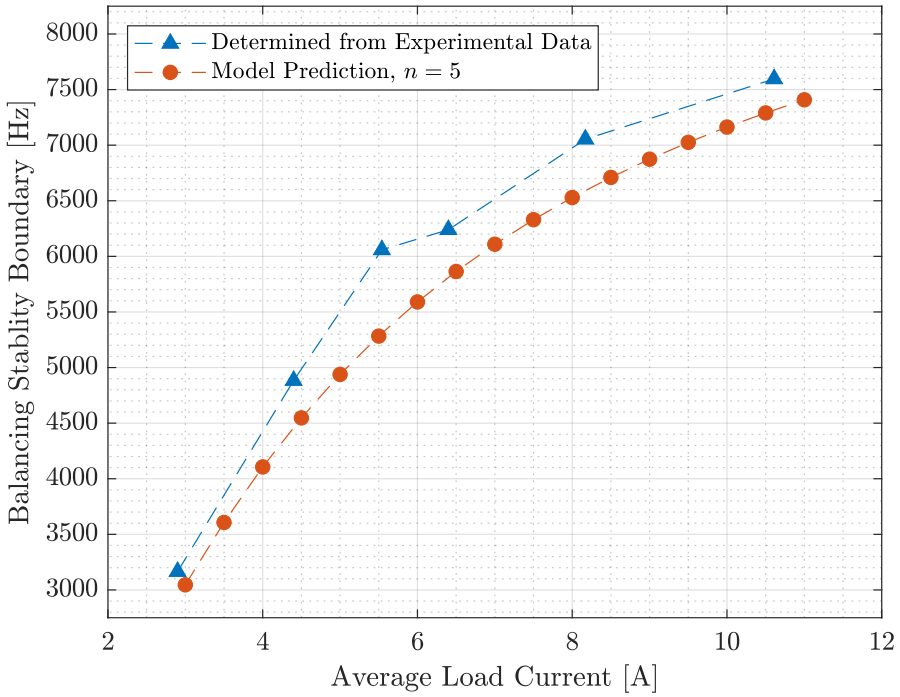


Figure 3.25: Measured and modeled stability boundaries as a function of the average load current for a 6-level FCML converter designed with $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, and $f_s = 100\,\text{kHz}$, and operated with $v_{\text{in}} = 80\,\text{V}$ and $D = 0.25$. The stability boundary indicates the maximum balancing designed balancing control bandwidth ω_{bal} that yields a stable closed-loop response. The generalized averaged model accurately predicts instabilities arising from the impact of the current ripple on the capacitor voltage dynamics.

of ω_{bal}, the modeled stability boundary defines the minimum load current required for stable operation. This confirms that active balancing controllers designed from averaging cannot maintain balancing bandwidths to arbitrarily light loads [96].

3.6 Summary of Generalized Averaged Modeling of FCML Converters

This chapter has illustrated how generalized averaged modeling clearly captures the interactions between the inductor current ripple and the dynamics of the average capacitor voltages. Due to the simplifying assumption that the capacitor voltages have negligible ripple, the approach proves to be practical for modeling the FCML converter, as this interaction is decomposed into the interaction between different harmonic components of the inductor current ripple and the average capacitor voltages. A key area of focus in the analysis in Section 3.3 was the further simplification of these interactions into a reduced-order form to enable analysis in the dimensions of the original state space. When applied to study the natural balancing dynamics with symmetric PS-PWM, the reduced-order model has the same structure as prior frequency domain models of the FCML converter. Subsequently, the reduced-order models are shown to be useful in characterizing designs and operating conditions where small-signal instabilities arise in actively balanced designs.

A key benefit of the generalized averaging approach compared to the alternative method of higher-order averaging studied in the next chapter is its compatibility with a large range of ripple waveforms. In the generalized averaging procedure, no assumption is made about the shape of the inductor current ripple, and non-sinusoidal ripple shapes are accommodated by including a greater number of harmonics in modeling the ripple. This makes generalized averaging a natural choice for systems where two state variables resonate with each other—the resulting model captures the interactions between the average components of the state variables and between the ripple components. A natural extension of the analysis presented in this chapter is to study FCML converter designs where the capacitor voltages also have significant ripple. In such converters, the inductor current ripple shape is piecewise-parabolic [131] as the harmonic components of both the capacitor voltage and inductor current ripple interact.

In Section 3.4, the generalized averaged model was employed to characterize the closed-loop behavior of an active balancing controller designed from the standard averaged model. Naturally, one is interested in how the additional plant information contributed by the generalized averaged model can be used to design the active balancing controller. It is immediately clear inspecting the reduced-order models derived in this chapter that the averaged converter dynamics are highly nonlinear. The structure of the small-signal plant derived from generalized averaging varies as a function of the conversion ratio D at which the linearization is evaluated. Therefore, it is cannot be expected in general that a controller designed from the small-signal plant model evaluated at one operating point would be stable or achieve similar performance when the operating point is varied.

The methods for active balancing controller design presented in Chapter 2 emphasize two properties of the closed-loop dynamics. First, the active balancing controller aims for improved tracking of the capacitor voltages compared to the naturally balanced behavior. This is straightforward to accomplish when the controller is designed from the small-signal aver-

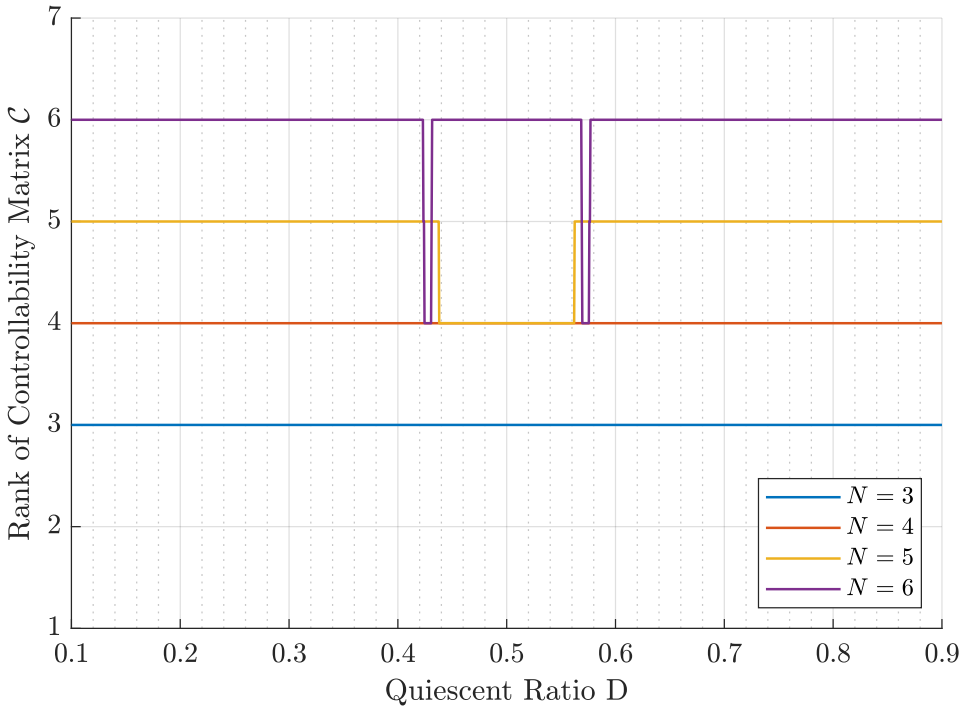


Figure 3.26: Rank of the controllability matrix $\mathcal{C}$ associated with the small-signal system of (3.58) as a function of the quiescent duty ratio D for a 3-level, 4-level, 5-level, and 6-level converter.

aged plant model, as the capacitor voltages appear to be internally decoupled and respond to different control inputs (the differences of neighboring duty ratios). From the structure of the small-signal dynamics of the generalized averaged model given in (3.58) and detailed in (B.13), the capacitor voltages are internally coupled (via nonzero entries in $\boldsymbol{F_{c,m}}$) and respond to weighted sums of the duty ratios due to the inductor current ripple (via nonzero entries in $\boldsymbol{G_{c,m}}$). Therefore, it is unclear how the structure of the active balancing control law based on the averaged model should be modified to compensate the impact of the inductor current ripple. Second, the active balancing controller aims to decouple the dynamics of the capacitor voltages and the inductor current. Studying the small-signal dynamics of (3.58), this once again proves difficult, as both the capacitor voltages and inductor current respond to weighted sums of the duty ratios. State-feedback methods such as those discussed in Section 2.6 may yield control laws for converters expected to operate over a narrow range of conversion ratios. However, considering effects of computation delays, modulator delays, and saturations on the controller outputs, it is unclear if these controllers will yield satisfactory closed-loop performance in general.

Finally, the small-signal converter model in (3.58) reveals that the active balancing plant

obtained by treating duty ratios as control inputs is not always completely controllable. Fig. 3.26 illustrates the rank of the controllability matrix $\mathcal{C}$ associated with the small-signal system of (3.58) for a 3-level, 4-level, 5-level, and 6-level converter as a function of the duty ratio. In all cases, the small-signal model is evaluated with $C = 8.8\,\mu\text{F}$, $L = 10\,\mu\text{H}$, $R_\text{s} = 0.3\,\Omega$, $f_\text{s} = 100\,\text{kHz}$, and $n = 10 \cdot (N-1)$ harmonics of the inductor current, where N is the converter level count. The 5-level converter exhibits a rank deficiency of 1 in the range $0.44 < D < 0.56$. The 6-level converter exhibits a rank deficiency of 1 in the approximate ranges $0.4235 < D < 0.424$ and $0.576 < D < 0.5765$ and a rank deficiency of 2 in the approximate ranges $0.424 < D < 0.43$ and $0.57 < D < 0.576$. The presence of uncontrollable modes of the system may be acceptable if these modes are stable, however uncontrollable modes are generally undesirable for active balancing control as the balancing performance for all flying capacitors cannot be completely specified in the controller design. The presence of uncontrollable modes for higher level-count converters and the aforementioned uncertainties about closed-loop performance in the presence of practical non-idealities motivates the study of other control inputs to to balance the capacitor voltages.

To summarize, generalized averaged modeling captures the natural converter dynamics and small-signal converter behavior accurately, but results in plant dynamics that are difficult to employ for controller design. The following chapter presents an alternative to generalized averaged modeling that yields less accurate descriptions of the coupling between capacitor voltages, but is simpler and can be used to design more robust active balancing controllers.

Chapter 4

Charge Models for Averaging Effects of Ripple

Portions of this chapter are adapted in whole or in part from [132].

In the FCML converter designs studied throughout this work, the current ripple shape is piecewise-linear, and the steady-state inductor current waveform has a triangular shape. Neglecting the effects of parasitic elements in the converter, the inductor current values at the start and end of each switching phase within the switching period can be related through simple linear expressions. Thus, instead of capturing the current ripple through a Fourier series decomposition, a refined averaged model could track the trajectory of the inductor current over a switching period and average its impacts on the capacitor voltages. It will be shown for the FCML converter that this approach yields simple expressions for the capacitor voltage dynamics. The resulting model approximates the capacitor voltage dynamics less accurately than the generalized averaged model, but can act as an accurate plant for the design of active balancing controllers.

4.1 Introduction to Charge Modeling for the FCML Converter

This section introduces methods of modeling flying capacitor voltage dynamics by analyzing changes in charge over a switching period. The method, first studied in [78], characterizes the inductor current waveform over a switching period and subsequently determines its net impact on the charge stored on the flying capacitors.

Before proceeding, some terminology characterizing the converter operation is introduced. For an N-level FCML converter, the converter can be said to operate in one of $N-1$ *operating modes*. Given the conversion ratio $M = v_{\mathrm{o}}/v_{\mathrm{in}}$, the index m_{op} used to identify the operating

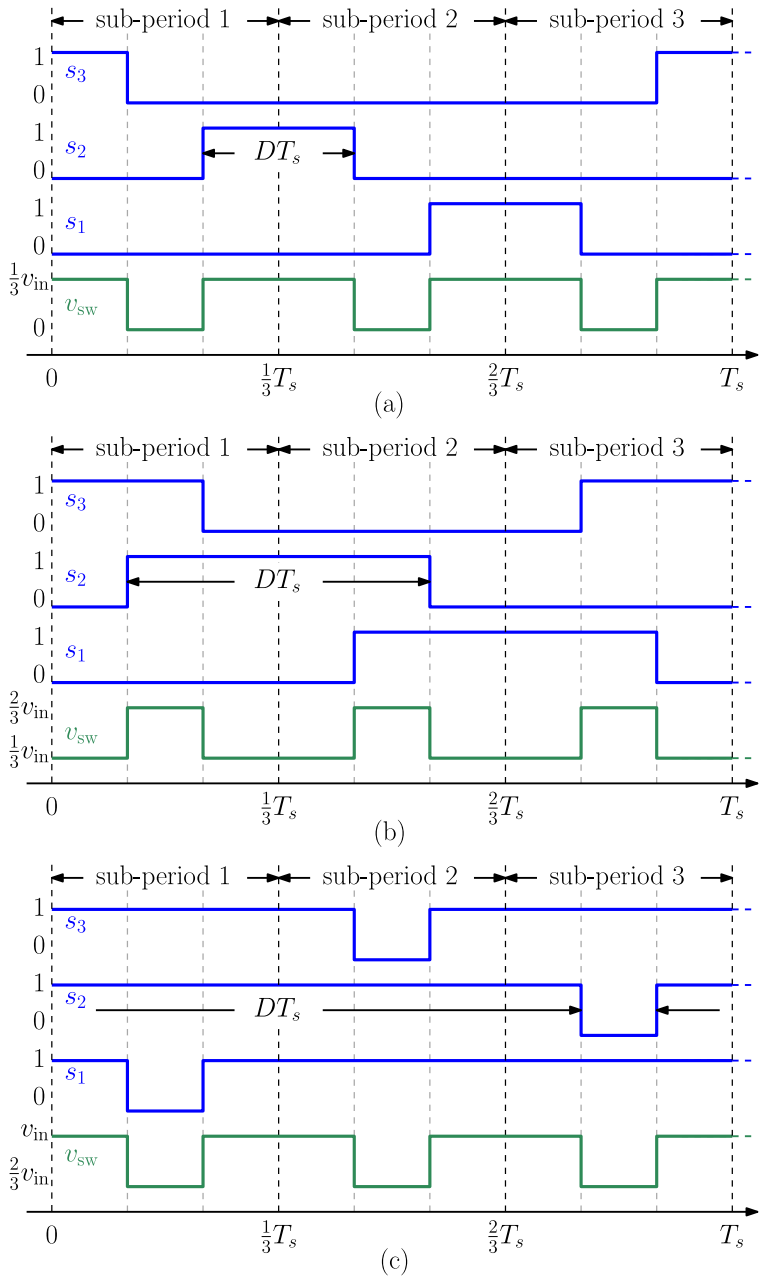


Figure 4.1: Switching signals s_k and switching node voltage v_{sw} for a 4-level FCML converter resulting from phase-shifted pulse-width modulation (PS-PWM) with duty ratio D for (a) Mode 1, $0 < D < 1/3$, (b) Mode 2, $1/3 < D < 2/3$, (c) Mode 3, $2/3 < D < 1$. In all three operating modes, the average value of the switching node voltage and the output voltage are equal to $D\,v_{\text{in}}$.

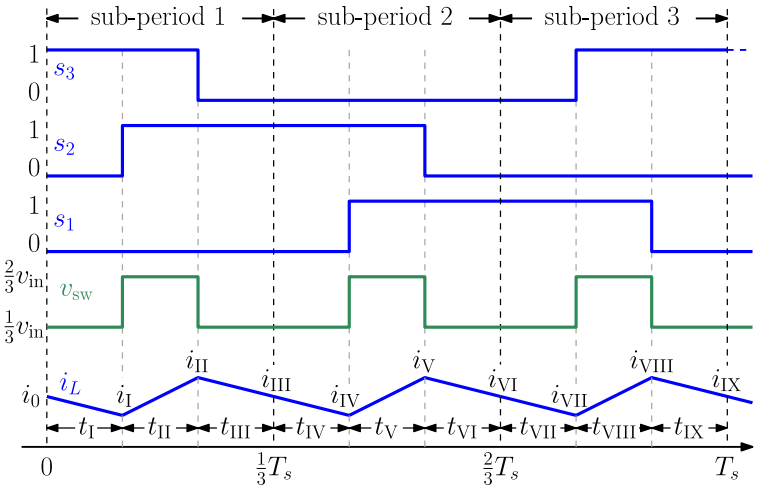


Figure 4.2: Switching signals s_k, switching node voltage v_{sw}, and inductor current i_L for a 4-level FCML converter operating in mode 2. The switching phases occurring in each sub-period and the value of the inductor current at the end of each switching phase are annotated with roman numerals.

mode is defined as

$$m_{\text{op}} := \begin{cases} 1 & , \ 0 \leq M < \frac{1}{N-1} \\ 2 & , \ \frac{1}{N-1} \leq M < \frac{2}{N-1} \\ \vdots & \\ N-1, & \frac{N-2}{N-1} \leq M < 1 \end{cases} \tag{4.1}$$

Under operation with symmetric PS-PWM, the operating mode determines the extent of overlap between the switching signals. For a given m_{op}, the switching node voltage alternates between a low level of $\frac{m_{\text{op}}-1}{N-1} \cdot v_{\text{in}}$ and a high level of $\frac{m_{\text{op}}}{N-1} \cdot v_{\text{in}}$. For an N-level FCML converter, the switching period can be divided into $N-1$ sub-period of length $T_{\text{e}} = \frac{T_{\text{s}}}{N-1}$. These sub-periods correspond to the fundamental period of the steady-state inductor current ripple. The following analysis assumes that all flying capacitors are identical (i.e. $C_1 = C_2 = C$), and that the flying capacitance is sufficiently large to approximate the average flying capacitor voltages as constant over a time window of length T_{s}. Furthermore, the output capacitance C_{o} is assumed sufficiently large to approximate the output voltage $v_{\text{o}} = M v_{\text{in}}$ as constant. Section 4.5 justifies the separation of timescales between the inductor current ripple and the capacitor voltage dynamics by showing that the charge model can be obtained from a standard perturbation approach for averaging.

Consider the waveforms for operating mode 2 highlighted in Fig. 4.2. Assuming that the average capacitor voltages and output voltage are approximately constant over the switching period, the inductor current in the time window of length T_{s} is piecewise-linear and can be

expressed generally as

$$i_L(t) = i_0 + \frac{1}{L}\int_0^t s_3 v_{\text{in}} + (s_2 - s_3)\, v_{c,2} + (s_1 - s_2)\, v_{c,1} - v_{\text{o}}\, d\tau \tag{4.2}$$

where i_0 denotes the steady-state average current. The impact of the different switch states over the switching period is captured via the switching function terms $s_k\,, k \in \{1, 2, 3\}$ appearing inside the integral in (4.2).

From (4.2), the value of the inductor current at the end of each switching phase can be defined recursively as

$$\begin{aligned} i_{\text{I}} &:= i_0 + \frac{v_{\text{in}} - v_{c,2} - v_{\text{o}}}{L} t_{\text{I}} \\ i_{\text{II}} &:= i_{\text{I}} + \frac{v_{\text{in}} - v_{c,1} - v_{\text{o}}}{L} t_{\text{II}} \\ i_{\text{III}} &:= i_{\text{II}} + \frac{v_{c,2} - v_{c,1} - v_{\text{o}}}{L} t_{\text{III}} \\ &\vdots \end{aligned} \tag{4.3}$$

The switching phase durations for operation in mode 2 are given by

$$t_k = \begin{cases} \left(M - \frac{1}{3}\right) T_s, & \text{if } k \in \{\text{II}, \text{V}, \text{VIII}\} \\ \frac{1}{2}\left(\frac{2}{3} - M\right) T_s, & \text{otherwise} \end{cases} \tag{4.4}$$

The net charge flowing into the flying capacitors can be subsequently expressed as an integral of the inductor current. Once again, the impact of the switch states on the capacitor current is captured via switching function terms s_k.

$$\begin{aligned} \Delta Q_1 &= \int_0^{T_s} (s_2 - s_1)\; i_L(t)\, dt \\ \Delta Q_2 &= \int_0^{T_s} (s_3 - s_2)\; i_L(t)\, dt \end{aligned} \tag{4.5}$$

For operation in mode 2, the expressions of (4.5) are expanded as

$$\Delta Q_1 = \frac{i_{\text{I}} + i_{\text{II}}}{2} t_{\text{II}} + \frac{i_{\text{II}} + i_{\text{III}}}{2} t_{\text{III}} + \frac{i_{\text{III}} + i_{\text{IV}}}{2} t_{\text{IV}} - \frac{i_{\text{V}} + i_{\text{VI}}}{2} t_{\text{VI}} - \frac{i_{\text{VI}} + i_{\text{VII}}}{2} t_{\text{VII}} - \frac{i_{\text{VII}} + i_{\text{VIII}}}{2} t_{\text{VIII}} \tag{4.6}$$

$$\Delta Q_2 = \frac{i_0 + i_{\text{I}}}{2} t_{\text{I}} + \frac{i_{\text{VII}} + i_{\text{VIII}}}{2} t_{\text{VIII}} + \frac{i_{\text{VIII}} + i_{\text{IX}}}{2} t_{\text{IX}} - \frac{i_{\text{II}} + i_{\text{III}}}{2} t_{\text{III}} - \frac{i_{\text{III}} + i_{\text{IV}}}{2} t_{\text{IV}} - \frac{i_{\text{IV}} + i_{\text{V}}}{2} t_{\text{V}} \tag{4.7}$$

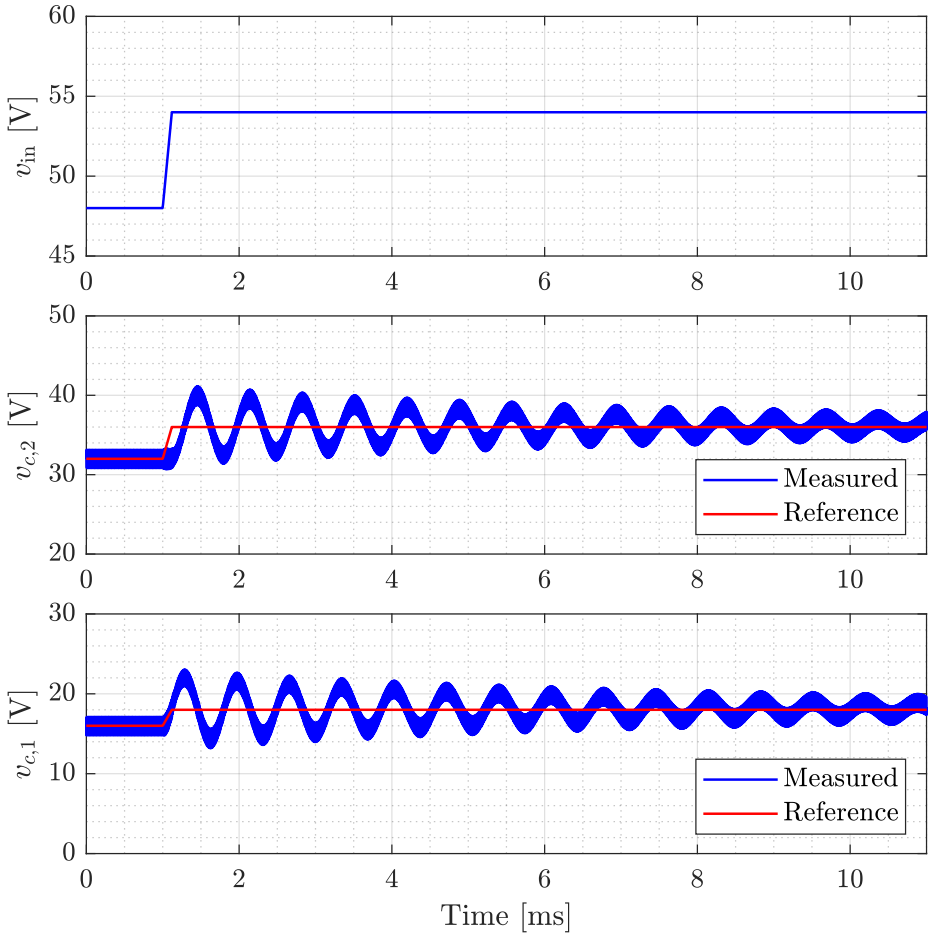


Figure 4.3: Simulated capacitor voltage responses to a step in the supply voltage from 48 V to 54 V for a 4-level FCML converter operating in mode 2. Results are shown for a controller regulating the average output voltage to 24 V and not implementing any active balancing feature. The underdamped capacitor voltage dynamics induce excessive blocking voltage stresses on the converter's switches. The converter is simulated with $L = 10\,\mu\text{H}$, $C = 8.8\,\mu\text{F}$, $f_s = 100\,\text{kHz}$.

Following the method presented in [78], the average capacitor voltage dynamics are obtained from the capacitor charge flow in (4.5) via an average current relation given by

$$\begin{aligned} \dot{v}_{c,1} &\approx \frac{\Delta Q_1}{C T_s} \\ \dot{v}_{c,2} &\approx \frac{\Delta Q_2}{C T_s} \end{aligned} \tag{4.8}$$

Collecting the two state variables into a state vector $\boldsymbol{v_c} := [v_{c,1}\ v_{c,2}]^{\text{T}}$, where T denotes the transpose operator, (4.8) yields linear time-invariant capacitor voltage dynamics for open-

loop operation without active balancing control, summarized as

$$\dot{\boldsymbol{v}}_{\boldsymbol{c}} = \begin{bmatrix} 0 & \frac{\left(1-6M+6M^2\right)T_s}{6LC} \\ -\frac{\left(1-6M+6M^2\right)T_s}{6LC} & 0 \end{bmatrix} \left(\boldsymbol{v}_{\boldsymbol{c}} - \overline{\boldsymbol{v}}_{\boldsymbol{c}}\right) \tag{4.9}$$

where

$$\overline{\boldsymbol{v}}_{\boldsymbol{c}} = \begin{bmatrix} \frac{1}{3}v_{\text{in}} & \frac{2}{3}v_{\text{in}} \end{bmatrix}^{\text{T}} \tag{4.10}$$

The small-signal impact of imbalance in the capacitor voltages is characterized by linearizing the expression of (4.8) with respect to variations in $v_{c,1}$ and $v_{c,2}$. The small-signal characteristics are obtained at the quiescent point corresponding to balanced capacitor voltages and a constant output voltage $v_{\text{o}} = Mv_{\text{in}}$. Collecting the two state variables into a state vector $\boldsymbol{v}_{\boldsymbol{c}} := \begin{bmatrix} v_{c,1} & v_{c,2} \end{bmatrix}^{\text{T}}$, the linearization of (4.8) is expressed concisely as

$$\dot{\tilde{\boldsymbol{v}}}_{\boldsymbol{c}} := \frac{1}{CT_s} \nabla_{\boldsymbol{v}_{\boldsymbol{c}}} \begin{bmatrix} \Delta Q_1 \\ \Delta Q_2 \end{bmatrix}_{\boldsymbol{v}_{\boldsymbol{c}} = \overline{\boldsymbol{v}}_{\boldsymbol{c}}} \tilde{\boldsymbol{v}}_{\boldsymbol{c}} \tag{4.11}$$

$$= \begin{bmatrix} 0 & \frac{\left(1-6M+6M^2\right)T_s}{6LC} \\ -\frac{\left(1-6M+6M^2\right)T_s}{6LC} & 0 \end{bmatrix} \tilde{\boldsymbol{v}}_{\boldsymbol{c}} \tag{4.12}$$

where $\tilde{\boldsymbol{v}}_{\boldsymbol{c}}$ represents the small-signal state variation and $\nabla_{\boldsymbol{v}_{\boldsymbol{c}}}$ indicates the Jacobian matrix evaluated with respect to the vector $\boldsymbol{v}_{\boldsymbol{c}}$.

As the model of (4.8) is linear in the capacitor voltages, the small-signal model presented in (4.12) is identical to the result given in [78] characterizing the natural capacitor voltage balancing dynamics under PS-PWM. For the ideal converter with zero parasitic elements and a stiff output voltage, the model of (4.12) predicts that the open-loop capacitor voltages under symmetric PS-PWM are characterized by a persistent oscillation. The simulation result in Fig. 4.3 confirms the presence of this oscillatory mode. Modest parasitic resistances in the circuit in the form of switch channel resistances and inductor equivalent series resistance act to damp the oscillation. In the simulation, these effects are lumped as a $100\,\text{m}\Omega$ resistor in series with the inductor. Therefore, the ideal model developed in this section corresponds to a worst-case plant that can be used for controller design.

To control the capacitor voltages, the switching node voltage pulse position is modulated as a control input. Fig. 4.4 illustrates the inductor current and capacitor current responses to a perturbation within sub-period 2 for a converter operating in mode 2. The position of the switching node voltage pulse is advanced by a time increment ΔT_2 by shifting the rising edge of s_1 and the falling edge of s_2. Note that this control action is different from modulating the duty ratios or phase shifts of switching signals as proposed in previous works. The small-signal impact of the perturbation ΔT_2 is identified by linearizing the expression of (4.5) with respect to variations in ΔT_2. The linearization is performed at the quiescent point of balanced capacitor voltages, a constant output voltage given by $v_{\text{o}} = Mv_{\text{in}}$, and a

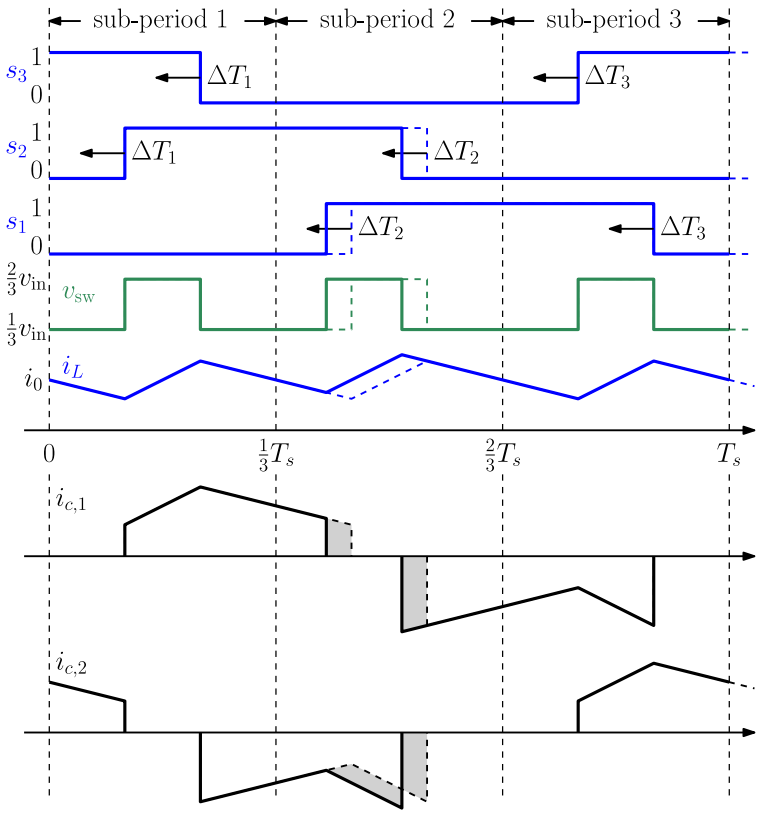


Figure 4.4: Converter waveforms illustrating the small-signal capacitor current response in operating mode 2 to a perturbation in the switching node voltage pulse position in sub-period 2. The differences in the quantity of charge flowing into each flying capacitor as a result of the perturbation are shown as shaded areas, and impact the capacitor voltages via the relations given in (4.8). The small-signal impact of all perturbations is summarized in (4.19).

quiescent value of $\overline{\Delta T_2} = 0$. The small-signal response to perturbations in ΔT_2 is summarized as

$$\begin{bmatrix} \Delta\tilde{Q}_{1,2} \\ \Delta\tilde{Q}_{2,2} \end{bmatrix} = \begin{bmatrix} -2i_0 \\ i_0 + \frac{(1-3M)M}{6} \cdot \frac{v_{\text{in}}}{Lf_s} \end{bmatrix} \Delta\tilde{T}_2 \tag{4.13}$$

Similarly, the small-signal response to a perturbation ΔT_1 in sub-period 1 is given by

$$\begin{bmatrix} \Delta\tilde{Q}_{1,1} \\ \Delta\tilde{Q}_{2,1} \end{bmatrix} = \begin{bmatrix} i_0 - \frac{(1-3M)M}{6} \cdot \frac{v_{\text{in}}}{Lf_s} \\ -2i_0 \end{bmatrix} \Delta\tilde{T}_1 \tag{4.14}$$

and the response to perturbation ΔT_3 in sub-period 3 is given by

$$\begin{bmatrix} \Delta\tilde{Q}_{1,3} \\ \Delta\tilde{Q}_{2,3} \end{bmatrix} = \begin{bmatrix} i_0 + \frac{(1-3M)M}{6} \cdot \frac{v_{\text{in}}}{Lf_s} \\ i_0 - \frac{(1-3M)M}{6} \cdot \frac{v_{\text{in}}}{Lf_s} \end{bmatrix} \Delta\tilde{T}_3 \tag{4.15}$$

Defining a normalized control input

$$\tilde{\boldsymbol{u}} := \frac{1}{T_s}\begin{bmatrix}\tilde{\Delta T_1} & \tilde{\Delta T_2} & \tilde{\Delta T_3}\end{bmatrix}^{\mathrm{T}} \tag{4.16}$$

and considering the natural coupling between flying capacitor voltages given in (4.12), the complete small-signal plant model for the 4-level converter operating in mode 2 is given by

$$\dot{\tilde{\boldsymbol{v}}}_{\boldsymbol{c}} = \boldsymbol{A_2}\cdot\tilde{\boldsymbol{v}}_{\boldsymbol{c}} + \boldsymbol{B_2}\cdot\tilde{\boldsymbol{u}} \tag{4.17}$$

where

$$\boldsymbol{A_2} := \begin{bmatrix} 0 & \frac{\left(1-6M+6M^2\right)T_s}{6LC} \\ -\frac{\left(1-6M+6M^2\right)T_s}{6LC} & 0 \end{bmatrix} \tag{4.18}$$

$$\boldsymbol{B_2} := \frac{1}{C}\begin{bmatrix} i_0-\alpha_2 & -2i_0 & i_0+\alpha_2 \\ -2i_0 & i_0+\alpha_2 & i_0-\alpha_2 \end{bmatrix} \tag{4.19}$$

$$\alpha_2 := \frac{(1-3M)\,M}{6}\cdot\frac{v_{\mathrm{in}}}{Lf_s} \tag{4.20}$$

Note that as the capacitor charge flow derived in (4.2)–(4.8) considers the inductor current ripple, the small-signal plant model in (4.17) depends on the inductor current ripple via the term α_2 given in (4.20). Thus, compared to the averaged plant models used in [96, 107, 108], the plant representation obtained in (4.17) is valid even at operating points where the inductor current ripple is not negligible. Section 4.3 will show how this plant model can be used to design a balancing control loop that is stable across all load conditions.

Operating Modes 1 and 3

The small-signal characteristics for the other two operating modes can be derived following a similar methodology as that presented above for operating mode 2. Switching node voltage perturbations for the converter operating in modes 1 and 3 are shown in Fig. 4.6 and Fig. 4.7 respectively. For both operating modes, the inductor current and capacitor charge flow can be derived from (4.2) and (4.5), and the small-signal capacitor voltage dynamics can be obtained from a linearization of (4.8). In all three operating modes, the small-signal dynamics are given by the general system representation

$$\dot{\tilde{\boldsymbol{v}}}_{\boldsymbol{c}} = \boldsymbol{A_k}\cdot\tilde{\boldsymbol{v}}_{\boldsymbol{c}} + \boldsymbol{B_k}\cdot\tilde{\boldsymbol{u}}\ ,\ k\in\{1,2,3\} \tag{4.21}$$

For operating mode 1, the plant model consists of

$$\boldsymbol{A_1} := \begin{bmatrix} 0 & \frac{-M^2T_s}{2LC} \\ \frac{M^2T_s}{2LC} & 0 \end{bmatrix} \tag{4.22}$$

$$\boldsymbol{B_1} := \frac{1}{C}\begin{bmatrix} i_0-\alpha_1 & -2i_0 & i_0+\alpha_1 \\ -2i_0 & i_0+\alpha_1 & i_0-\alpha_1 \end{bmatrix} \tag{4.23}$$

$$\alpha_1 := \frac{(1-3M)\,M}{6}\cdot\frac{v_{\mathrm{in}}}{Lf_s} \tag{4.24}$$

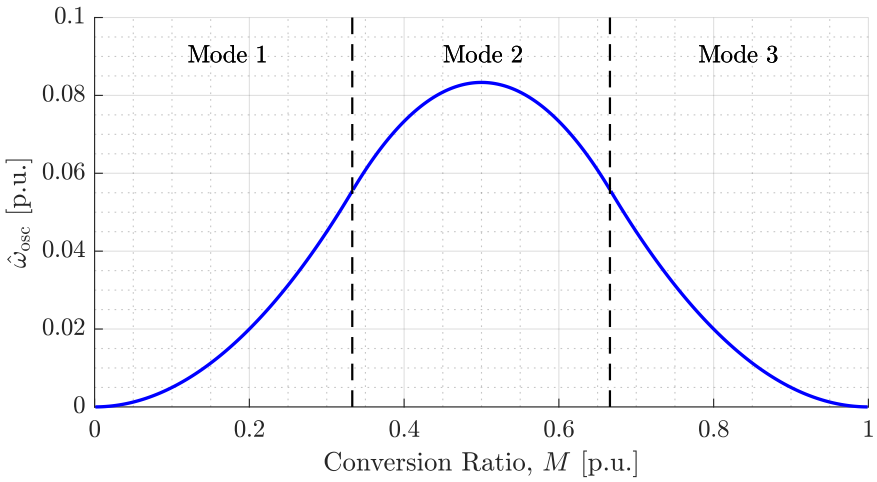


Figure 4.5: Normalized characteristic oscillation frequency $\hat{\omega}_{\text{osc}}$ defined in (4.32) as a function of the conversion ratio M.

The model for operating mode 3 is given by

$$\boldsymbol{A_3} := \begin{bmatrix} 0 & \frac{-(M-1)^2 T_s}{2LC} \\ \frac{(M-1)^2 T_s}{2LC} & 0 \end{bmatrix} \tag{4.25}$$

$$\boldsymbol{B_3} := \frac{1}{C} \begin{bmatrix} -\alpha_3 & 0 & \alpha_3 \\ 0 & \alpha_3 & -\alpha_3 \end{bmatrix} \tag{4.26}$$

$$\alpha_3 := (M-1)^2 \cdot \frac{v_{\text{in}}}{L f_s} \tag{4.27}$$

For the 4-level converter, the matrix $\boldsymbol{A_k}$ is anti-diagonal in all three operating modes, indicating that the open-loop small-signal dynamics in the absence of control inputs is always purely oscillatory. The characteristic oscillation frequency is given by the off-diagonal entries of $\boldsymbol{A_k}$, and is summarized as

$$\boldsymbol{A_k} = \begin{bmatrix} 0 & -\omega_{\text{osc}} \\ \omega_{\text{osc}} & 0 \end{bmatrix} \tag{4.28}$$

$$\omega_{\text{osc}} = 2\pi \frac{\omega_0}{\Omega_{\text{s}}} \cdot \begin{cases} \frac{M^2}{2}, & 0 < M < \frac{1}{3} \\ \frac{-1+6M-6M^2}{6}, & \frac{1}{3} < M < \frac{2}{3} \\ \frac{(M-1)^2}{2}, & \frac{2}{3} < M < 1 \end{cases} \tag{4.29}$$

where

$$\omega_0 := \frac{1}{\sqrt{LC}} \tag{4.30}$$

$$\Omega_{\text{s}} := \frac{2\pi f_s}{\omega_0} \tag{4.31}$$

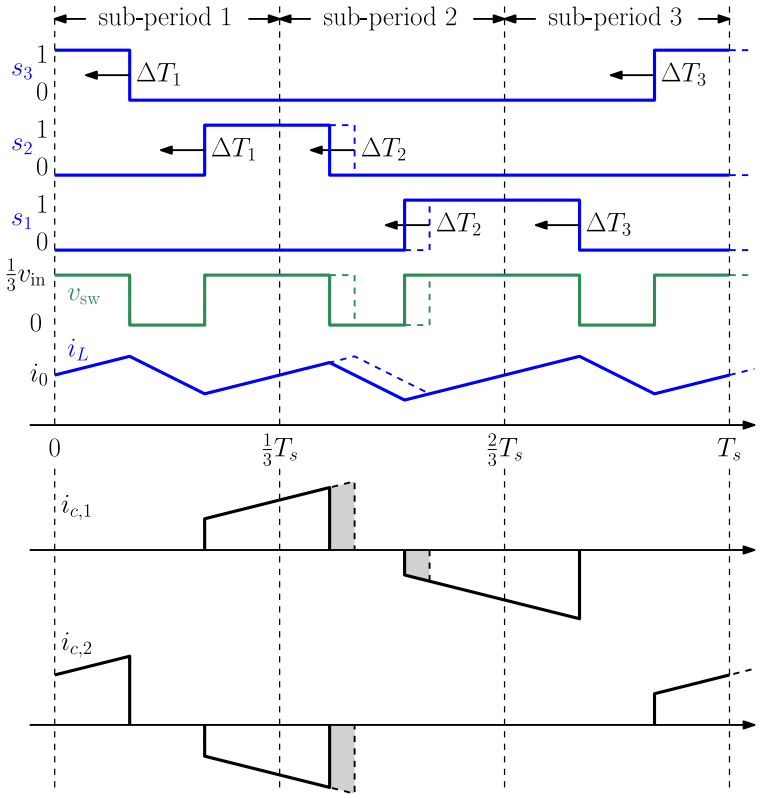


Figure 4.6: Converter waveforms illustrating the small-signal capacitor current response in operating mode 1 to a perturbation in the switching node voltage pulse position in sub-period 2. The small-signal impact of all perturbations is summarized in (4.23).

The current ripple model adapted from [78] and employed in (4.2), (4.5), and (4.8) enables analytical expressions in (4.29) for the oscillatory open-loop capacitor voltage dynamics. By comparison, prior work in [72, 73, 76] has only been able to characterize the dependence of the natural oscillatory behavior on the converter design and operating point via parametric sweeps. Fig. 4.5 plots a normalized characteristic oscillation frequency $\hat{\omega}_{\text{osc}}$ defined as

$$\hat{\omega}_{\text{osc}} := \frac{\omega_{\text{osc}}}{\left(2\pi \frac{\omega_0}{\Omega_s}\right)} \tag{4.32}$$

versus the conversion ratio M. It can be shown from (4.29) that the expression for ω_{osc} continuous and differentiable across the boundaries between modes, highlighting that the open-loop poles of the small-signal plant derived for the different operating modes move smoothly on the imaginary axis of the complex plane as a function of the conversion ratio M.

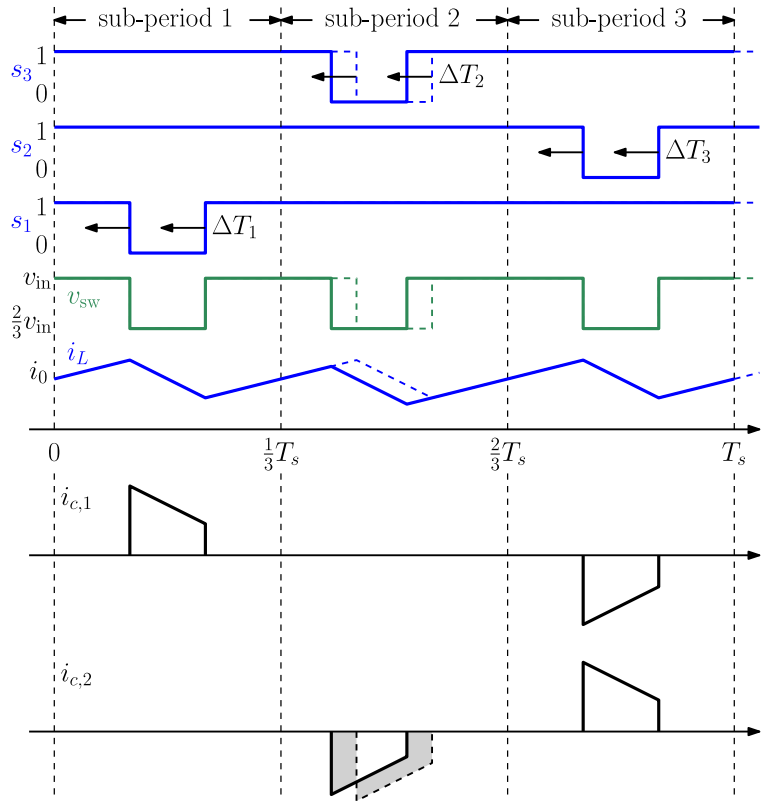


Figure 4.7: Converter waveforms illustrating the small-signal capacitor current response in operating mode 3 to a perturbation in the switching node voltage pulse position in sub-period 2. The small-signal impact of all perturbations is summarized in (4.26).

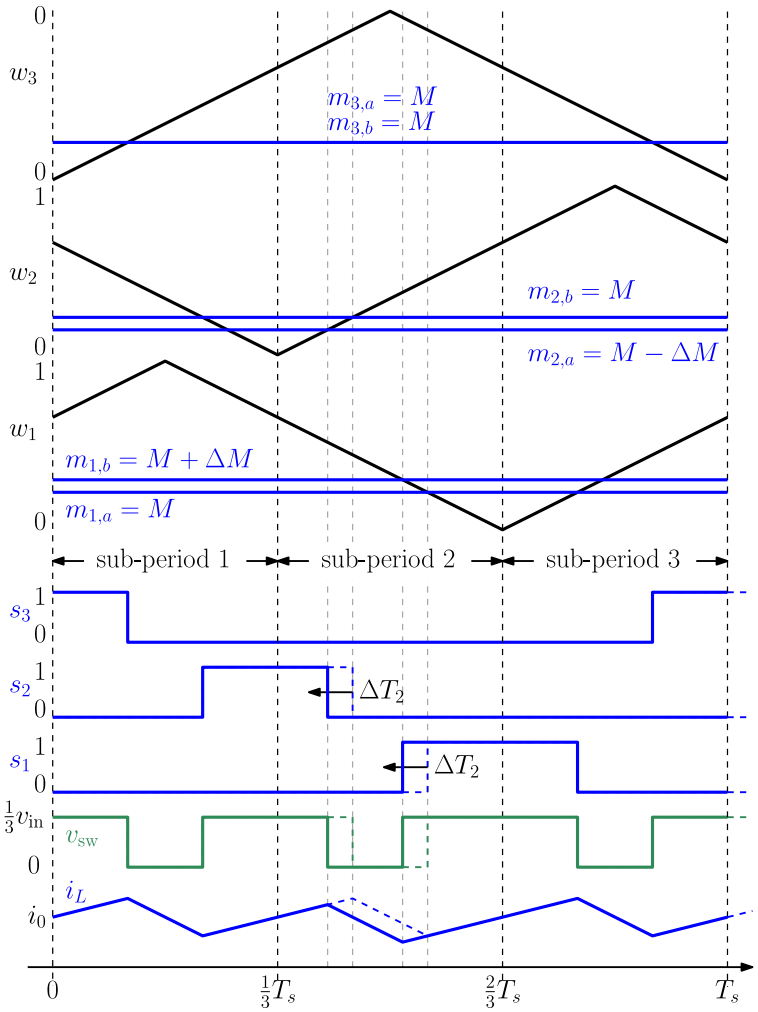


Figure 4.8: Carriers, modulating waveforms, and key converter waveforms for a 4-level FCML converter operating in mode 1 with a perturbation applied in sub-period 2. In the proposed implementation, two modulating waveforms $m_{k,a}$ and $m_{k,b}$ are associated with each triangular carrier w_k, and are used for up-count and down-count comparisons respectively.

The switching edge perturbations acting as balancing control inputs can be implemented in a single-sampled digital PWM system by using phase-shifted triangular carriers with two modulating waveforms. In this scheme, switching signal s_k is generated through a comparison of a carrier waveform w_k against two different modulating waveforms $m_{k,a}$ and $m_{k,b}$ as

$$s_k = \begin{cases} 1, & (w_k > m_{k,a}) \text{ and } w_k \text{ counting up} \\ 1, & (w_k > m_{k,b}) \text{ and } w_k \text{ counting down} \\ 0, & \text{otherwise} \end{cases} \tag{4.33}$$

Table 4.1: Modulating Waveform Generation

	Mode 1	Mode 2	Mode 3
$m_{3,a} =$	$M - \frac{\Delta T_1}{T_s}$	$M - \frac{\Delta T_1}{T_s}$	$M - \frac{\Delta T_2}{T_s}$
$m_{3,b} =$	$M + \frac{\Delta T_3}{T_s}$	$M + \frac{\Delta T_3}{T_s}$	$M + \frac{\Delta T_2}{T_s}$
$m_{2,a} =$	$M - \frac{\Delta T_2}{T_s}$	$M - \frac{\Delta T_2}{T_s}$	$M - \frac{\Delta T_3}{T_s}$
$m_{2,b} =$	$M + \frac{\Delta T_1}{T_s}$	$M + \frac{\Delta T_1}{T_s}$	$M + \frac{\Delta T_3}{T_s}$
$m_{1,a} =$	$M - \frac{\Delta T_3}{T_s}$	$M - \frac{\Delta T_3}{T_s}$	$M - \frac{\Delta T_1}{T_s}$
$m_{1,b} =$	$M + \frac{\Delta T_2}{T_s}$	$M + \frac{\Delta T_2}{T_s}$	$M + \frac{\Delta T_1}{T_s}$

Thus, modulating waveform $m_{k,a}$ controls the falling edge of switching signal s_k and modulating waveform $m_{k,b}$ controls the rising edge. Fig. 4.8 illustrates carriers, modulating waveforms, and relevant converter waveforms for a 4-level FCML converter operating in mode 1 with a perturbation applied in sub-period 2. The nominal values of the modulating waveforms is indicated as M and corresponds to the value applied to all $m_{k,a}$ and $m_{k,b}$ to obtain symmetric phase-shifted switching signals. To achieve a perturbation in sub-period 2, modulating waveforms $m_{2,a}$ and $m_{1,b}$ are offset by $\Delta M = \Delta T_2/T_s$. The proposed implementation is compatible with digital single-update PWM implementation on microcontrollers that offer digital PWM modules with two modulating waveforms such as those in the Texas Instruments C28x family [133]. Based on the desired control action, the offsets ΔM can be applied once per period (for example, at the valley of carrier w_3). For each operating mode, the values of all modulating waveforms can be defined with respect to a nominal value M and the offsets resulting from switching edge perturbations ΔT_k. The values assigned to modulating waveforms in each operating mode are summarized in Table 4.1.

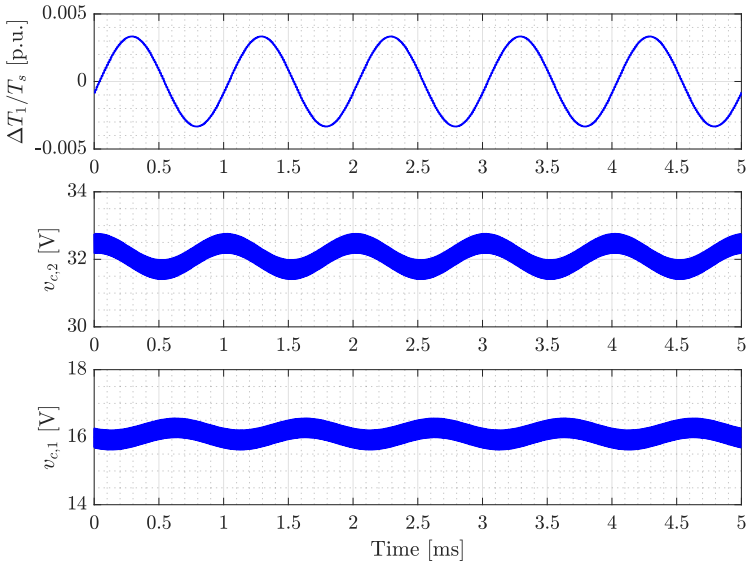


Figure 4.9: Simulated capacitor voltage responses for a 4-level FCML converter when applying a 1 kHz perturbation in control input ΔT_1. The converter is operated with $v_{\text{in}} = 48\,\text{V}$, $f_s = 100\,\text{kHz}$, $L = 10\,\mu\text{H}$, and $C = 8.8\,\mu\text{F}$. The capacitor voltage responses are post-processed via Fast Fourier Transforms (FFTs) to determine the magnitude and phase response at the perturbation frequency.

4.2 Simulation Verification of Plant Model

For each operating mode $k \in \{1, 2, 3\}$, a control-to-output transfer matrix $\boldsymbol{H_k}(s)$ is obtained from a Laplace transform of (4.21) by evaluating

$$\boldsymbol{H_k}(s) = (s\boldsymbol{I_{2\times 2}} - \boldsymbol{A_k})^{-1}\,\boldsymbol{B_k} \tag{4.34}$$

where s is the complex frequency variable and $\boldsymbol{I_{2\times 2}}$ denotes the 2-dimensional identity matrix. The elements of $\boldsymbol{H_k}(s)$ represent transfer functions from individual normalized control inputs to each of the flying capacitor voltages. From the structure of $\boldsymbol{A_k}$ in (4.28), (4.34) can be simplified to

$$\boldsymbol{H_k}(s) = \frac{1}{s^2 + \omega_{\text{osc}}^2}\begin{bmatrix} s & \omega_{\text{osc}} \\ -\omega_{\text{osc}} & s \end{bmatrix}\boldsymbol{B_k} \tag{4.35}$$

It is evident that all plant transfer functions consist of a purely imaginary pole pair at frequency ω_{osc}. The zeros of the individual transfer functions are determined by the columns of matrix $\boldsymbol{B_k}$.

To verify the transfer functions obtained from evaluation of (4.34) for each operating mode, a circuit simulation of a 4-level FCML converter implementing the modulation scheme defined in (4.33) is constructed. As the models presented in this section assume an ideal

lossless converter, the simulation does not include parasitic elements and is configured with $L = 10\,\mu\text{H}$ and $C = 8.8\,\mu\text{F}$, $v_{\text{in}} = 48\,\text{V}$, and $f_s = 100\,\text{kHz}$. To establish a quiescent point for small-signal analysis, the simulation regulates the average converter output voltage through a feedback loop adjusting the nominal value M of the modulating waveforms as described in Fig. 4.8 and Table 4.1. Sinusoidal perturbations are applied to the control inputs ΔT_k, and the responses of $v_{c,1}$ and $v_{c,2}$ are measured and post-processed using Fast Fourier Transforms (FFTs) to determine the magnitude and phase response at the perturbation frequency. An example of a 1 kHz perturbation in control input ΔT_1 and corresponding capacitor voltage responses is shown in Fig. 4.9. The frequency response characterization is repeated for a sweep in frequencies within a 5 kHz bandwidth. There are six total transfer functions for the 4-level converter from each of three control inputs to each of two capacitor voltages—for brevity, only the frequency responses from normalized perturbations in ΔT_1 to $v_{c,1}$ and $v_{c,2}$ (i.e. $\boldsymbol{H}_{\boldsymbol{k},11}(j\omega)$ and $\boldsymbol{H}_{\boldsymbol{k},21}(j\omega)$) are presented in this section. Fig. 4.10 and Fig. 4.11 show frequency response characterizations of $\boldsymbol{H}_{\boldsymbol{k},11}(j\omega)$ and $\boldsymbol{H}_{\boldsymbol{k},21}(j\omega)$ respectively for operating modes 1, 2, and 3. For operating mode 1, the frequency response is evaluated at $M = 1/6$; for operating mode 2, $M = 3/6$; for operating mode 3, $M = 5/6$. In each case, the frequency response characterized in simulation shows strong agreement with the transfer functions obtained in (4.34). The undamped pole pair is evident in all three transfer functions, and its location varies as a function of the conversion ratio M. Due to the symmetry of the expression for ω_{osc} in (4.29) about the point $M = 0.5$, the pole location for the transfer functions corresponding to $M = 1/6$ and $M = 5/6$ are identical.

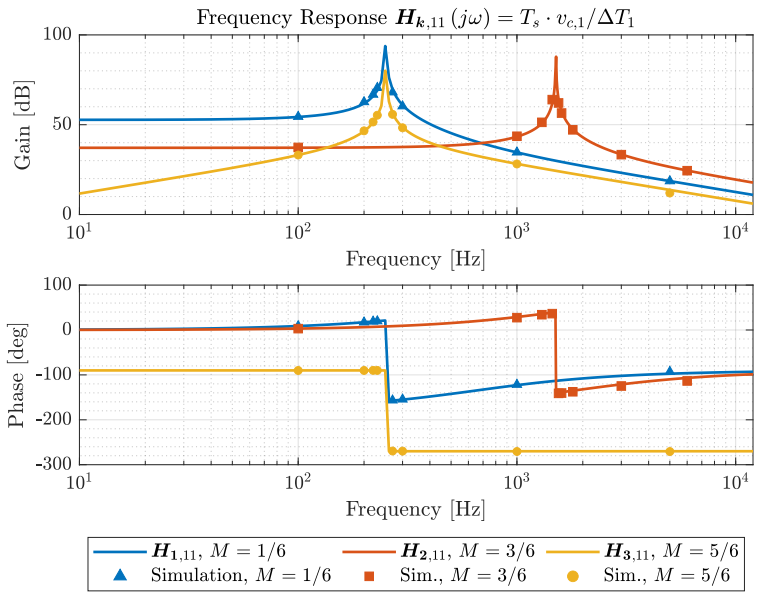


Figure 4.10: Comparison of simulated frequency response of capacitor voltage $v_{c,1}$ to perturbations in ΔT_1 to the theoretical response $\boldsymbol{H}_{\boldsymbol{k},11}$ obtained from (4.34). The simulation results agree with the theoretical frequency response in all operating modes up to a tested bandwidth of 5 kHz.

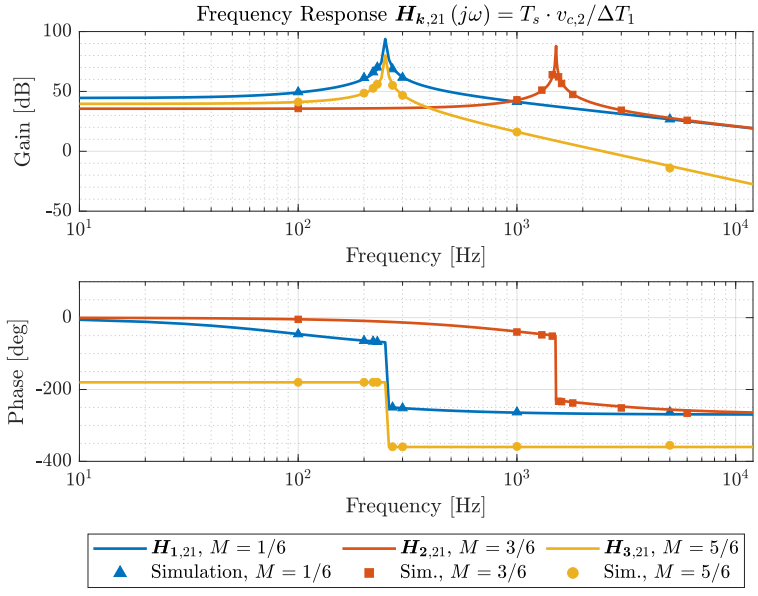


Figure 4.11: Comparison of simulated frequency response of capacitor voltage $v_{c,2}$ to perturbations in ΔT_1 to the theoretical response $\boldsymbol{H}_{\boldsymbol{k},21}$ obtained from (4.34). The simulation results agree with the theoretical frequency response in all operating modes up to a tested bandwidth of 5 kHz.

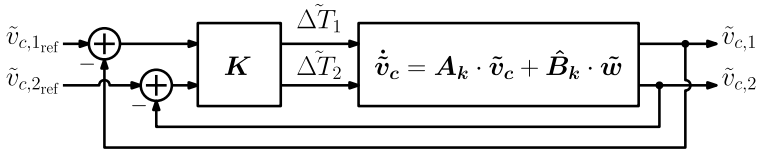


Figure 4.12: Block-diagram representation of the small-signal active balancing control loop. The controller $\boldsymbol{K}$ is designed in this work to damp the natural capacitor voltage oscillations.

4.3 Design of a State-Feedback Balancing Controller

For the 4-level FCML converter, the rank of matrices $\boldsymbol{B_1}$, $\boldsymbol{B_2}$, and $\boldsymbol{B_3}$ in (4.23), (4.19), and (4.26) respectively is always 2 (i.e., matrix $\boldsymbol{B_k}$ always has full row rank). Thus, the rank of the controllability matrix [101–103]

$$\mathcal{C} = \begin{bmatrix} \boldsymbol{B_k} & \boldsymbol{A_k} \cdot \boldsymbol{B_k} & \boldsymbol{A_k^2} \cdot \boldsymbol{B_k} \end{bmatrix} \tag{4.36}$$

is always 2, indicating that the small-signal plant in every operating mode is always completely controllable. This finding is significant as it implies that perturbations in the switching node voltage pulse position can be used to stabilize the marginally stable plant identified for all operating modes in Section 4.1. Depending on the design criteria specifying the locations of the closed-loop poles, different state-feedback controller structures can be considered. This section considers one possible approach which specifies the decay time constant associated with the capacitor voltage oscillations.

As the matrix $\boldsymbol{B_k}$ has three columns but only two rows, one of the control inputs must be redundant. In all three operating modes, the first two columns of $\boldsymbol{B_k}$ are linearly independent. Therefore, the balancing controller can always set $\Delta T_3 = 0$ and completely control the capacitor voltages with ΔT_1 and ΔT_2. Alternative choices for which control input is set to zero may be considered without impact to the design procedure highlighted in this section.

With the choice of $\Delta T_3 = 0$, an equivalent small-signal system can be derived with respect to the remaining two inputs ΔT_1 and ΔT_2, and is summarized as

$$\dot{\tilde{\boldsymbol{v}}}_{\boldsymbol{c}} = \boldsymbol{A_k} \cdot \tilde{\boldsymbol{v}}_{\boldsymbol{c}} + \hat{\boldsymbol{B}}_{\boldsymbol{k}} \cdot \tilde{\boldsymbol{w}} \ , \ k \in \{1, 2, 3\} \tag{4.37}$$

$$\tilde{\boldsymbol{w}} := \frac{1}{T_s} \begin{bmatrix} \Delta\tilde{T}_1 & \Delta\tilde{T}_2 \end{bmatrix}^{\mathrm{T}} \tag{4.38}$$

Here, matrix $\hat{\boldsymbol{B}}_{\boldsymbol{k}}$ is the square matrix consisting of the first two columns of $\boldsymbol{B_k}$. With the system representation of (4.37), a full-state-feedback control law represented by square matrix $\boldsymbol{K} \in \mathbb{R}^{2\times 2}$ can be designed. Fig. 4.12 shows the structure of the small-signal closed-loop system with the state-feedback control law. As the small-signal plant model is derived with respect to an equilibrium consisting of balanced capacitor voltages, the small-signal reference inputs are always 0, i.e.

$$\tilde{v}_{c,1_{\text{ref}}} \equiv 0 \tag{4.39}$$

$$\tilde{v}_{c,1_{\text{ref}}} \equiv 0 \tag{4.40}$$

For the control loop shown in Fig. 4.12, the closed-loop capacitor voltage dynamics are given by

$$\dot{\tilde{\boldsymbol{v}}}_{\boldsymbol{c}} = \left(\boldsymbol{A}_{\boldsymbol{k}} - \hat{\boldsymbol{B}}_{\boldsymbol{k}} \cdot \boldsymbol{K}\right) \cdot \tilde{\boldsymbol{v}}_{\boldsymbol{c}} =: \boldsymbol{A}_{\mathbf{CL}} \cdot \tilde{\boldsymbol{v}}_{\boldsymbol{c}} \tag{4.41}$$

Given the structure of $\boldsymbol{A}_{\boldsymbol{k}}$ in (4.28), this work considers a damping strategy that designs $\boldsymbol{K}$ such that

$$\boldsymbol{A}_{\mathbf{CL}} = \begin{bmatrix} -\sigma & -\omega_{\text{osc}} \\ \omega_{\text{osc}} & -\sigma \end{bmatrix} \tag{4.42}$$

In this approach, the controller design consists of specifying the damping time constant $\tau_d = 1/\sigma$. With the closed-loop dynamics specified, the controller matrix $\boldsymbol{K}$ is given by

$$\boldsymbol{K} = -\hat{\boldsymbol{B}}_{\boldsymbol{k}}^{-1} \left(\boldsymbol{A}_{\mathbf{CL}} - \boldsymbol{A}_{\boldsymbol{k}}\right) = \sigma \cdot \hat{\boldsymbol{B}}_{\boldsymbol{k}}^{-1} \tag{4.43}$$

Following from the complete controllability of the system, other designs for the state-feedback controller may be considered depending on the closed-loop regulation objectives. For example, one may design the matrix $\boldsymbol{K}$ such that it fully decouples the capacitor voltage dynamics, yielding a diagonal structure for the closed-loop dynamics $\boldsymbol{A}_{\mathbf{CL}}$. Alternatively, the damping design may be specified in terms of the quality factor or damping ratio instead of the damping time constant, resulting in an oscillation frequency for the closed-loop system that is different from that of the open-loop system.

Evaluating (4.43) in operating mode 1, the damping controller is given by

$$\boldsymbol{K} = C \cdot \frac{\sigma}{3i_0^2 + \alpha_1^2} \cdot \begin{bmatrix} -i_0 - \alpha_1 & -2i_0 \\ -2i_0 & \alpha_1 - i_0 \end{bmatrix} \tag{4.44}$$

For operating mode 2, the controller is

$$\boldsymbol{K} = C \cdot \frac{\sigma}{3i_0^2 + \alpha_2^2} \cdot \begin{bmatrix} -i_0 - \alpha_2 & -2i_0 \\ -2i_0 & \alpha_2 - i_0 \end{bmatrix} \tag{4.45}$$

Finally, for operating mode 3, the controller is

$$\boldsymbol{K} = C \cdot \sigma \cdot \begin{bmatrix} -\frac{1}{\alpha_3} & 0 \\ 0 & \frac{1}{\alpha_3} \end{bmatrix} \tag{4.46}$$

Note that in the case of operating modes 1 and 2, the average inductor current i_0 appears in the controller gains. In systems employing an average current control loop for regulating the load voltage, the reference inductor current can be substituted for i_0 in (4.44), (4.45), and (4.46).

In the small-signal sense, the switching edge perturbations applied to balance capacitor voltages do not disturb the average inductor current and output voltage dynamics. Therefore, the active balancing controller can be implemented in parallel with other control loops regulating the output voltage and inductor current. Fig. 4.13 illustrates a complete digital control system where the balancing control is implemented in parallel with a standard

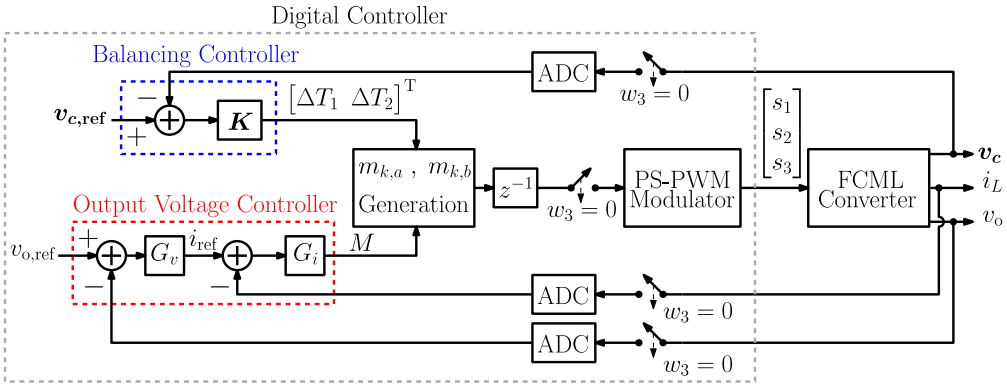


Figure 4.13: Block diagram representation of a single-sampled digital control architecture where the state-feedback balancing controller is implemented in parallel with a dual-loop output voltage controller.

dual-loop output voltage controller. The diagram presents a single-sampled implementation, where the capacitor voltages, inductor current, and output voltage are sampled once per switching period at the valley of carrier w_3. The average inductor current and output voltage are regulated by controlling the nominal value of the modulating waveforms, M. The balancing controller computes the time shifts ΔT_1 and ΔT_2, and the modulating waveforms are subsequently calculated using the update equations in Table 4.1 depending on the operating mode.

4.4 Experimental Verification of Active Balancing Controller

The models presented in this chapter are verified against experimental characterization of the same 12-level FCML converter prototype shown in Fig. 2.10. The hardware is reconfigured as a 4-level converter by bypassing eight consecutive switch pairs starting at the input side. Table 2.1 lists the key components comprising the hardware prototype. The parallel control architecture highlighted in Fig. 4.13 is implemented on a single core of a Texas Instruments TMS320F28379D microcontroller. Each PWM module in the microcontroller is configured to generate switching signals following the scheme presented in Table 4.1. The active balancing and output voltage controllers are run in an interrupt service routine triggered at the valley of carrier w_3 as shown in Fig. 4.13.

Characterization of Plant Model

To verify the plant models derived for all operating modes in the experimental hardware, the plant frequency response is measured through the same characterization procedure detailed

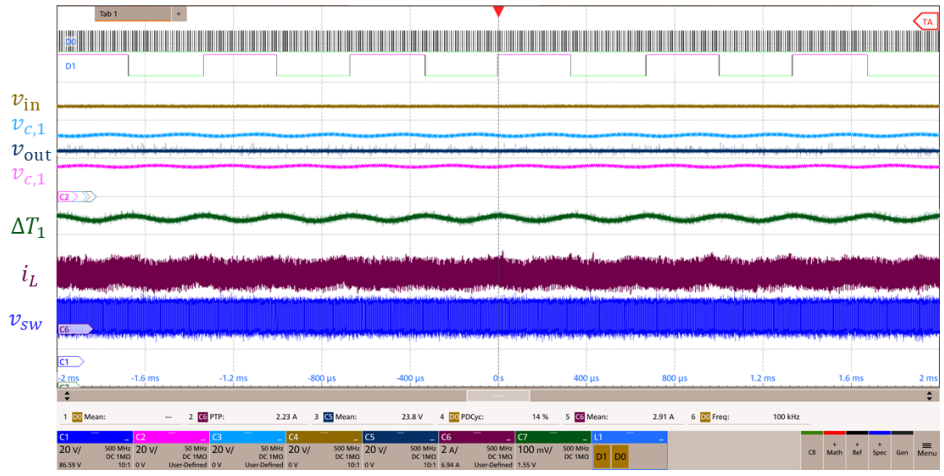


Figure 4.14: Oscilloscope waveform capture showing an example perturbation in ΔT_1 and measured capacitor voltages for the 4-level FCML converter prototype operating in mode 2. The data is post-processed using FFTs in MATLAB to determine the plant magnitude and phase response.

in Section 4.2. In all experiments, the converter is operated with an input voltage of 48 V. In each experiment, the quiescent point is first established by configuring the output voltage control loop to regulate the converter output at a predetermined set-point (8 V, 24 V, and 40 V for operating modes 1, 2, and 3 respectively). The microcontroller applies a small-signal sinusoidal perturbation to one of the control inputs ΔT_1 or ΔT_2, and the capacitor voltage responses are measured using an oscilloscope. A scaled version of the perturbation signal is also output to the oscilloscope using the digital-to-analog converter avaiable in the TMS320F28379D microcontroller. Fig. 4.14 shows an example of a 3 kHz perturbation in ΔT_1 for the prototype operating in mode 2, and the corresponding capacitor voltage measurements alongside other converter waveforms. The measured raw data is subsequently saved and post-processed through FFTs in MATLAB to obtain the magnitudes and relative phase shifts of the perturbation signal and capacitor voltages. The experiment is repeated at several different perturbation frequencies within a 5 kHz bandwidth.

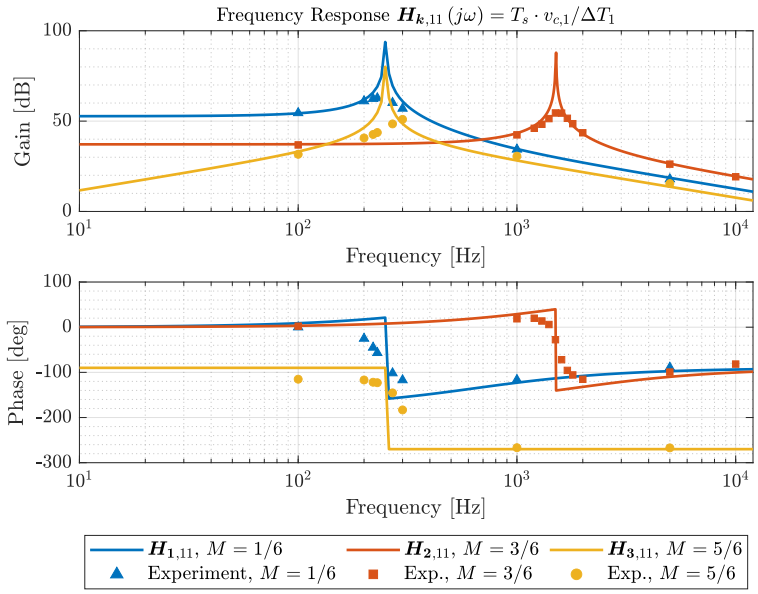


Figure 4.15: Comparison of measured frequency response of capacitor voltage $v_{c,1}$ to perturbations in ΔT_1 to the theoretical response $\boldsymbol{H}_{\boldsymbol{k},11}$ obtained from (4.34). The experimental measurements confirm the theoretical plant behavior in all operating modes, and exhibit nonzero damping arising from unmodeled parasitic elements in the converter.

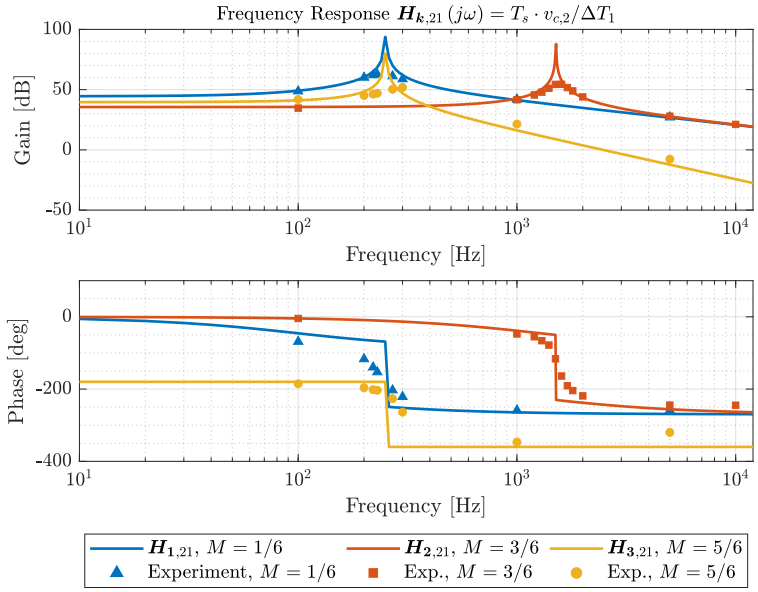


Figure 4.16: Comparison of measured frequency response of capacitor voltage $v_{c,2}$ to perturbations in ΔT_1 to the theoretical response $\boldsymbol{H}_{\boldsymbol{k},21}$ obtained from (4.34). The experimental measurements confirm the theoretical plant behavior, and exhibit nonzero damping arising from unmodeled parasitic elements in the converter.

Measured responses of $v_{c,1}$ to normalized perturbations in ΔT_1 are given in Fig. 4.15 for all three operating modes. Similarly, measured responses of $v_{c,2}$ to normalized perturbations in ΔT_1 are given in Fig. 4.16 for all operating modes. Analytical frequency responses obtained from (4.34) are shown as solid lines. The low- and high-frequency asymptotes and the resonant pole location predicted by the analytical frequency response functions are confirmed by the measured frequency response data. As discussed in Section 4.2, the measured data shows additional damping of the resonant poles arising from the unmodeled impacts of parasitic elements in the hardware prototype. These include parasitic series resistances and switch drain-source capacitances, which have been shown in [72] and [80] to affect the natural flying capacitor voltage balancing dynamics.

Characterization of Closed-Loop Dynamics

To compare the closed-loop capacitor voltage dynamics to the intended behavior specified in the design of the control law $\boldsymbol{K}$, the closed-loop frequency response is experimentally characterized. A small-signal perturbation is applied at each of the capacitor voltage reference inputs, and the capacitor voltage responses at the same frequency are measured. The analytical response between the applied perturbation and the measured capacitor voltages is given by the the transfer matrix

$$\boldsymbol{H_{CL}}(s) = \left[s\boldsymbol{I_{2\times 2}} - \left(\boldsymbol{A_k} - \hat{\boldsymbol{B}}_{\boldsymbol{k}} \cdot \boldsymbol{K}\right)\right]^{-1} \cdot \hat{\boldsymbol{B}}_{\boldsymbol{k}} \cdot \boldsymbol{K} \tag{4.47}$$

Fig. 4.17 compares the analytical frequency response in operating mode 2 of $\boldsymbol{H_{CL},11}$, the closed-loop transfer function from perturbations in $v_{c,1_{\text{ref}}}$ to $v_{c,1}$, to measured data for three different designs of the damping term σ. For each design, the equivalent Q of the closed-loop poles resulting from the damping design is also shown. The measured frequency response data confirms that the digital implementation of the active balancing controller achieves the intended closed-loop performance within the 5 kHz bandwidth measured. The proposed controller provides a parameter σ that can tuned by the designer depending on the application requirements. The transfer functions of (4.47) are not physically meaningful beyond their application in characterizing the closed-loop dynamics. As described in Section 4.3, the plant model in this work is derived with respect to an equilibrium point consisting of balanced capacitor voltages. Therefore the small-signal capacitor voltage references must always be identically 0.

To illustrate the improvement in capacitor voltage dynamics through a time-domain example, the 4-level converter prototype operating in mode 2 is subjected to a step-transient in the supply voltage. Fig. 4.18a shows the measured capacitor voltage, inductor current, and output voltage responses to a step in the supply voltage from 45 V to 50 V when the output voltage controller is active but the balancing controller is not enabled. The converter operates with an average load current of 5 A and the output voltage set-point is 24 V. The nominal values of the capacitor voltages under perfectly balanced operation are shown as reference traces. The capacitor voltages exhibit an underdamped transient response with a

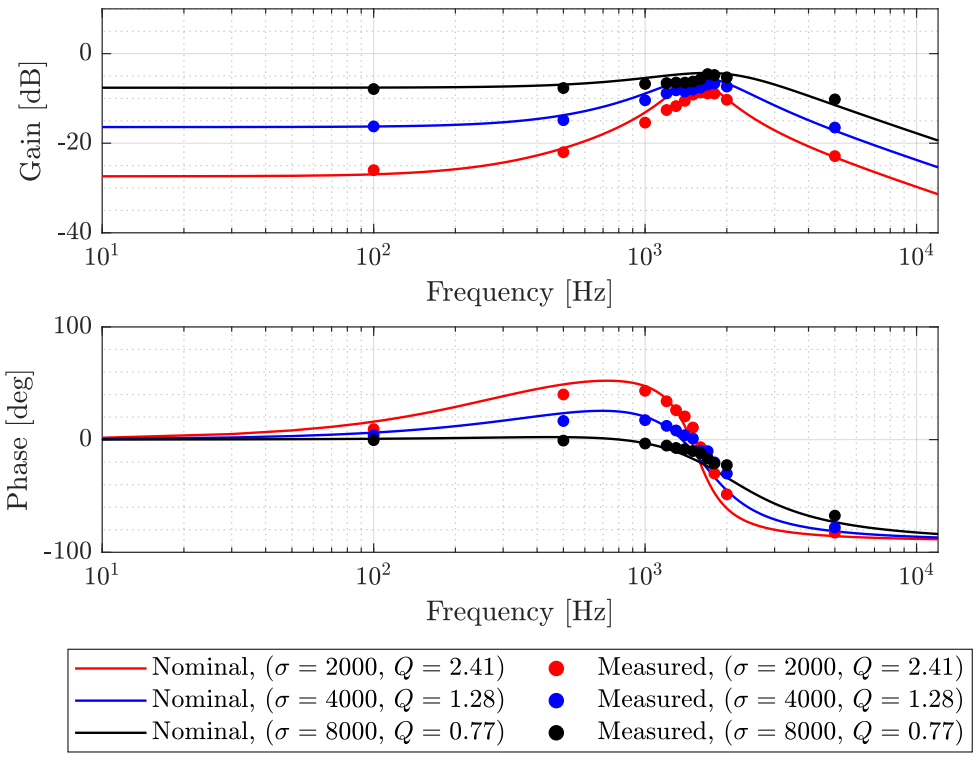


Figure 4.17: Comparison of measured frequency response in operating mode 2 of capacitor voltage $v_{c,1}$ to perturbations in $v_{c,1_{\text{ref}}}$ to the theoretical response $\boldsymbol{H_{CL},_{11}}$ obtained from (4.47).

12 % overshoot in capacitor voltage $v_{c,2}$ and a ± 5 % settling time of approximately 1.5 ms. By comparison, Fig. 4.18b shows the measured responses when the active balancing controller designed for $\sigma = 4000$ is enabled. The overshoot in capacitor voltage $v_{c,2}$ is reduced to 6 %, and the settling time is approximately 0.5 ms, representing a 50% and 66% improvement respectively. The plant models developed in this work contain information about the impact of the inductor current ripple on the capacitor voltage dynamics. Consequently, unlike balancing controllers derived from averaged models of the converter such as [96, 107, 108], the controller derived in this work is stable at light-load and zero-load conditions. Fig. 4.19a illustrates the capacitor voltage responses for the converter operating in mode 2 without active balancing control and subjected to the same input voltage transient when the load is reduced to an average value of 0.25 A. At this operating point, a small-ripple approximation for the inductor current is no longer valid. Without active balancing control, the capacitor voltage responses are once again oscillatory. Fig. 4.19b shows the improved capacitor voltage responses measured once the active balancing controller is enabled. Notably, the small-signal instability of [96] is not observed at this light-load condition.

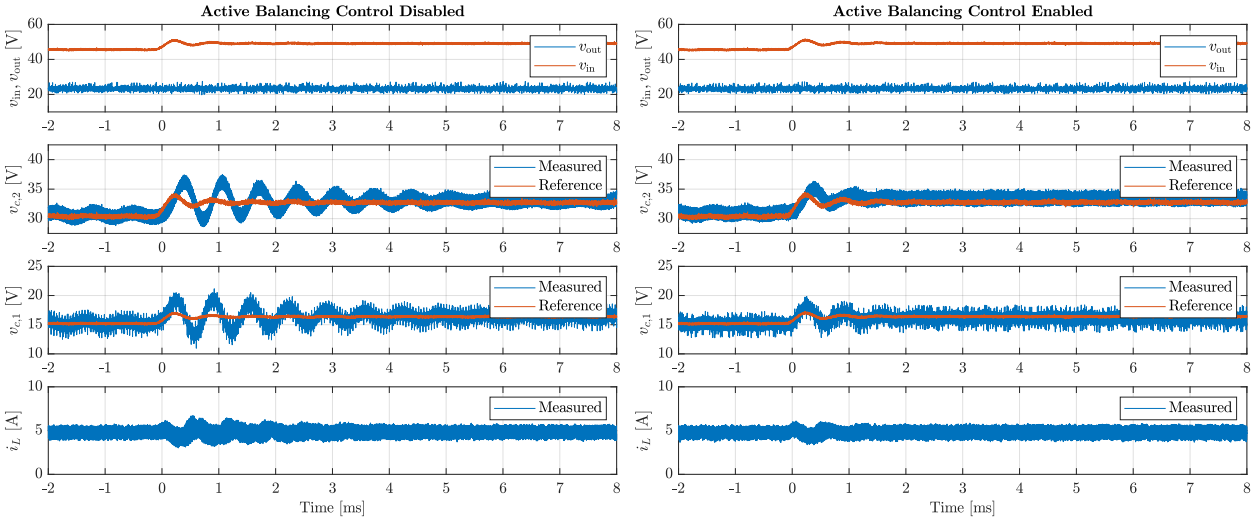


Figure 4.18: Measured responses of the capacitor voltages and inductor current in the 4-level FCML converter to a step in the supply voltage from 45 V to 50 V when (a) the output voltage controller is active but the balancing controller is not enabled, and (b) both the output voltage and active balancing controllers are enabled. The converter operates with an average load current of 5 A and an output voltage set-point of 24 V. The proposed active balancing controller damps the natural capacitor voltage oscillations, enabling improved capacitor voltage tracking during the line transient.

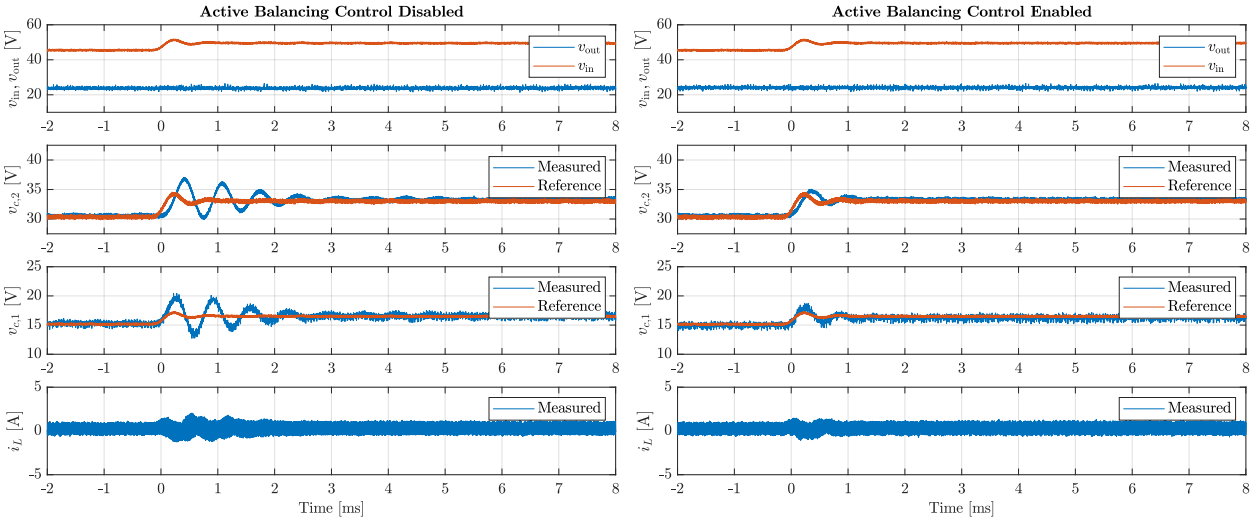


Figure 4.19: Measured responses of the capacitor voltages and inductor current in the 4-level FCML converter to a step in the supply voltage from 45 V to 50 V when (a) the output voltage controller is active but the balancing controller is not enabled, and (b) both the output voltage and active balancing controllers are enabled. In this experiment, the converter operates at a light-load condition corresponding to 0.25 A average load current. The proposed active balancing controller damps the natural capacitor voltage oscillations, and does not exhibit the small-signal instability inherent to controller derived from averaged models such as [96, 107, 108].

4.5 Justification of the Averaging Method Via Perturbation Theory

In the preceding sections of this chapter, the capacitor voltage dynamics were characterized by analyzing the average change in the charge stored on the flying capacitors. The models derived have been verified through open-loop and closed-loop studies in circuit simulations and in measurements of a hardware prototype. This section mathematically justifies the charge modeling approach by using the well-established KBM averaging method [93–95, 134]. In particular, it is shown that analyzing the charge flow in the flying capacitors is equivalent to studying the order-1 KBM averaged model.

Review of Krylov-Bogoliubov-Mitropolsky (KBM) Averaging

Consider a general description of a time-varying periodic dynamical system given by

$$\dot{\boldsymbol{x}} = \epsilon \boldsymbol{F}(\boldsymbol{x}, t) \tag{4.48}$$

The KBM averaging approach [93–95, 134] approximates the solution of this system with the solution to a time-invariant system

$$\dot{\boldsymbol{y}} = \epsilon \boldsymbol{G_1}(\boldsymbol{y}) + \epsilon^2 \boldsymbol{G_2}(\boldsymbol{y}) + \epsilon^3 \boldsymbol{G_3}(\boldsymbol{y}) + \dots \tag{4.49}$$

The dynamics $\boldsymbol{G_k}$ represent the average behavior of the system refined with the k^{th}-order approximation of the ripple and are obtained recursively through the methods described in [94, 95] and reviewed in this section. The key insight of the KBM approach is the decomposition

$$\boldsymbol{x} = \boldsymbol{y} + \epsilon \boldsymbol{\Psi_1}(\boldsymbol{y}, t) + \epsilon^2 \boldsymbol{\Psi_2}(\boldsymbol{y}, t) + \dots \tag{4.50}$$

where $\boldsymbol{\Psi_k}$ are defined to be zero-average functions of time, i.e.

$$\frac{1}{T_\text{s}} \int_{t-T_\text{s}}^{t} \boldsymbol{x}(\tau)\, \mathrm{d}\tau = \frac{1}{T_\text{s}} \int_{t-T_\text{s}}^{t} \boldsymbol{y}(\tau)\, \mathrm{d}\tau \tag{4.51}$$

The dynamics of $\boldsymbol{x}$ and $\boldsymbol{y}$ can be equated as

$$\dot{\boldsymbol{x}} = \dot{\boldsymbol{y}} + \epsilon \left(\frac{\partial \boldsymbol{\Psi_1}}{\partial \boldsymbol{y}} \dot{\boldsymbol{y}} + \frac{\partial \boldsymbol{\Psi_1}}{\partial t} \right) + \epsilon^2 \left(\frac{\partial \boldsymbol{\Psi_2}}{\partial \boldsymbol{y}} \dot{\boldsymbol{y}} + \frac{\partial \boldsymbol{\Psi_2}}{\partial t} \right) + \dots \tag{4.52}$$

The dynamics $\dot{\boldsymbol{y}}$ can be re-expressed as

$$\dot{\boldsymbol{y}} = \epsilon \boldsymbol{f}\left(\boldsymbol{y} + \epsilon \boldsymbol{\Psi_1}(\boldsymbol{y}, t) + \epsilon^2 \boldsymbol{\Psi_2}(\boldsymbol{y}, t) + \dots, t\right) - \tag{4.53}$$

$$\left[\epsilon \left(\frac{\partial \boldsymbol{\Psi_1}}{\partial \boldsymbol{y}} \dot{\boldsymbol{y}} + \frac{\partial \boldsymbol{\Psi_1}}{\partial t} \right) + \epsilon^2 \left(\frac{\partial \boldsymbol{\Psi_2}}{\partial \boldsymbol{y}} \dot{\boldsymbol{y}} + \frac{\partial \boldsymbol{\Psi_2}}{\partial t} \right) + \dots \right] \tag{4.54}$$

In many power converters, including the FCML converter, $\boldsymbol{f}$ takes the form

$$\boldsymbol{F}(\boldsymbol{x},t) = \boldsymbol{F_1}(t)\cdot\boldsymbol{x} + \boldsymbol{F_2}(t)\cdot\boldsymbol{u} \tag{4.55}$$

where $\boldsymbol{u}$ is a constant consisting of voltage and current sources connected to the converter. Therefore (4.54) can be rewritten as

$$\dot{\boldsymbol{y}} = \epsilon\left[\boldsymbol{F_1}(t)\cdot\left(\boldsymbol{y}+\epsilon\boldsymbol{\Psi_1}(\boldsymbol{y},t)+\epsilon^2\boldsymbol{\Psi_2}(\boldsymbol{y},t)+\dots\right)+\boldsymbol{F_2}(t)\cdot\boldsymbol{u}\right]- \tag{4.56}$$

$$\left[\epsilon\left(\frac{\partial\boldsymbol{\Psi_1}}{\partial\boldsymbol{y}}\dot{\boldsymbol{y}}+\frac{\partial\boldsymbol{\Psi_1}}{\partial t}\right)+\epsilon^2\left(\frac{\partial\boldsymbol{\Psi_2}}{\partial\boldsymbol{y}}\dot{\boldsymbol{y}}+\frac{\partial\boldsymbol{\Psi_2}}{\partial t}\right)+\dots\right] \tag{4.57}$$

Grouping the terms on the right-side of (4.57) by powers of ϵ,

$$\epsilon^1 : \boldsymbol{F_1}(t)\cdot\boldsymbol{y}+\boldsymbol{F_2}(t)\cdot\boldsymbol{u}-\frac{\partial\boldsymbol{\Psi_1}}{\partial t} =: \boldsymbol{G_1} \tag{4.58}$$

$$\epsilon^2 : \boldsymbol{F_1}(t)\cdot\boldsymbol{\Psi_1}(\boldsymbol{y},t)-\left[\frac{\partial\boldsymbol{\Psi_1}}{\partial\boldsymbol{y}}\boldsymbol{G_1}+\frac{\partial\boldsymbol{\Psi_2}}{\partial t}\right] =: \boldsymbol{G_2} \tag{4.59}$$

$$\epsilon^3 : \boldsymbol{F_1}(t)\cdot\boldsymbol{\Psi_2}(\boldsymbol{y},t)-\left[\frac{\partial\boldsymbol{\Psi_1}}{\partial\boldsymbol{y}}\boldsymbol{G_2}+\frac{\partial\boldsymbol{\Psi_2}}{\partial\boldsymbol{y}}\boldsymbol{G_1}+\frac{\partial\boldsymbol{\Psi_3}}{\partial t}\right] =: \boldsymbol{G_3} \tag{4.60}$$

$$\vdots$$

Recalling that $\boldsymbol{\Psi_k}$ are zero-average functions, defining

$$\boldsymbol{G_1} = \frac{1}{T_\mathrm{s}}\int_{t-T_\mathrm{s}}^{t}\left(\boldsymbol{F_1}(\tau)\cdot\boldsymbol{y}+\boldsymbol{F_2}(\tau)\cdot\boldsymbol{u}\right)\mathrm{d}\tau \tag{4.61}$$

$$\frac{\partial\boldsymbol{\Psi_1}}{\partial t} = \boldsymbol{F_1}(t)\cdot\boldsymbol{y}+\boldsymbol{F_2}(t)\cdot\boldsymbol{u}-\boldsymbol{G_1} \tag{4.62}$$

$$\boldsymbol{G_2} = \frac{1}{T_\mathrm{s}}\int_{t-T_\mathrm{s}}^{t}\left(\boldsymbol{F_1}(\tau)\cdot\boldsymbol{\Psi_1}(\boldsymbol{y},\tau)-\frac{\partial\boldsymbol{\Psi_1}}{\partial\boldsymbol{y}}\boldsymbol{G_1}\right)\mathrm{d}\tau \tag{4.63}$$

$$\frac{\partial\boldsymbol{\Psi_2}}{\partial t} = \boldsymbol{F_1}(t)\cdot\boldsymbol{\Psi_1}(\boldsymbol{y},t)-\frac{\partial\boldsymbol{\Psi_1}}{\partial\boldsymbol{y}}\boldsymbol{G_1}-\boldsymbol{G_2} \tag{4.64}$$

$$\vdots$$

results in the time-invariant averaged dynamics $\dot{\boldsymbol{y}}$ given by (4.49). The terms $\boldsymbol{G_k}$ in the averaged model represent the contribution of ripple function $\boldsymbol{\Psi_{k-1}}$ to the averaged model. From the procedure highlighted above, the contributions $\boldsymbol{G_k}$ can be calculated recursively to obtain improved approximations of the averaged dynamics. In most converters, calculating the contribution of $\boldsymbol{\Psi_1}$ is sufficient to accurately describe the averaged dynamics. The following analysis shows that the charge model described in this chapter is equivalent to this order-1 evaluation of the KBM-averaged model.

Application of KBM Averaging to the FCML Converter

Consider the original switched dynamics of the FCML converter, given as

$$\dot{v}_{c,k} = \frac{1}{C}\left(s_{k+1} - s_k\right) i_L \tag{4.65}$$

$$\dot{i}_L = \frac{1}{L}\left[v_{\text{in}} s_{n_c} - v_{\text{o}} + \sum_{k=1}^{M}\left(s_k - s_{k+1}\right) v_{c,k}\right] \tag{4.66}$$

$$\dot{v}_{\text{o}} = \frac{1}{C_{\text{o}}}\left(i_L - \frac{v_{\text{o}}}{R}\right) \tag{4.67}$$

Defining the state vector as $\boldsymbol{x} := \begin{bmatrix} v_{c,1} & \cdots & v_{c,M} & i_L & v_{\text{o}} \end{bmatrix}^{\text{T}}$, the vector fields representing the switched dynamics can be compactly represented as

$$\dot{v}_{c,k} = f_{v_{c,k}}\left(\boldsymbol{x}, t\right) \tag{4.68}$$

$$\dot{i}_L = f_{i_L}\left(\boldsymbol{x}, t\right) \tag{4.69}$$

$$\dot{v}_{\text{o}} = f_{v_{\text{o}}}\left(\boldsymbol{x}, t\right) \tag{4.70}$$

The switched dynamics can be put into the standard form of (4.48) by considering the timescale change

$$t' := \frac{t}{T_{\text{s}}} \tag{4.71}$$

yielding

$$\frac{\text{d}}{\text{d}t'} v_{c,k} = T_{\text{s}} \cdot f_{v_{c,k}}\left(\boldsymbol{x}, T_{\text{s}} \cdot t'\right) \tag{4.72}$$

$$\frac{\text{d}}{\text{d}t'} i_L = T_{\text{s}} \cdot f_{i_L}\left(\boldsymbol{x}, T_{\text{s}} \cdot t'\right) \tag{4.73}$$

$$\frac{\text{d}}{\text{d}t'} v_{\text{o}} = T_{\text{s}} \cdot f_{v_{\text{o}}}\left(\boldsymbol{x}, T_{\text{s}} \cdot t'\right) \tag{4.74}$$

given in matrix form as

$$\frac{\text{d}}{\text{d}t'} \boldsymbol{x} = T_{\text{s}} \cdot \boldsymbol{F}\left(\boldsymbol{x}, T_{\text{s}} \cdot t'\right) \tag{4.75}$$

$$\boldsymbol{F}\left(\boldsymbol{x}, T_{\text{s}} \cdot t'\right) := \begin{bmatrix} f_{v_{c,1}}\left(\boldsymbol{x}, T_{\text{s}} \cdot t'\right) \\ \vdots \\ f_{v_{c,M}}\left(\boldsymbol{x}, T_{\text{s}} \cdot t'\right) \\ f_{i_L}\left(\boldsymbol{x}, T_{\text{s}} \cdot t'\right) \\ f_{v_{\text{o}}}\left(\boldsymbol{x}, T_{\text{s}} \cdot t'\right) \end{bmatrix} \tag{4.76}$$

Under the timescale change, the vector fields on the right side of (4.72)–(4.74) are periodic in $t' = 1$. The average of a vector field $f(\cdot, T_\mathrm{s} \cdot t')$ is represented as a new field $g(\cdot)$ given by

$$g(\cdot) := \int_{\frac{t}{T_\mathrm{s}}-1}^{\frac{t}{T_\mathrm{s}}} f(\cdot, s)\,\mathrm{d}s \tag{4.77}$$

$$= \frac{1}{T_\mathrm{s}} \int_{t-T_\mathrm{s}}^{t} f(\cdot, \tau)\,\mathrm{d}\tau \tag{4.78}$$

The order-0 model obtained by averaging (4.75) is the standard averaged model given by

$$\frac{\mathrm{d}}{\mathrm{d}t'}\bar{v}_{c,k} = T_\mathrm{s} \cdot g_{1,v_{c,k}}(\boldsymbol{y}) = 0 \tag{4.79}$$

$$\frac{\mathrm{d}}{\mathrm{d}t'}\bar{i}_L = T_\mathrm{s} \cdot g_{1,i_L}(\boldsymbol{y}) \;= T_\mathrm{s} \cdot \frac{1}{L}\left(v_\mathrm{in} D - \bar{v}_\mathrm{o}\right) \tag{4.80}$$

$$\frac{\mathrm{d}}{\mathrm{d}t'}\bar{v}_\mathrm{o} = T_\mathrm{s} \cdot g_{1,v_\mathrm{o}}(\boldsymbol{y}) \;= T_\mathrm{s} \cdot \frac{1}{C_\mathrm{o}}\left(\bar{i}_L - \frac{\bar{v}_\mathrm{o}}{R}\right) \tag{4.81}$$

where

$$\boldsymbol{y} := \begin{bmatrix} \bar{v}_{c,1} & \cdots & \bar{v}_{c,M} & \bar{i}_L & \bar{v}_\mathrm{o} \end{bmatrix}^\mathrm{T} \tag{4.82}$$

The order-0 averaged model is represented in matrix form in timescale t' as

$$\frac{\mathrm{d}}{\mathrm{d}t'}\boldsymbol{y} = T_\mathrm{s} \cdot \boldsymbol{G_1}(\boldsymbol{y}) \tag{4.83}$$

$$\boldsymbol{G_1}(\boldsymbol{y}) := \begin{bmatrix} g_{1,v_{c,1}}(\boldsymbol{y}) \\ \vdots \\ g_{1,v_{c,M}}(\boldsymbol{y}) \\ g_{1,i_L}(\boldsymbol{y}) \\ g_{1,v_\mathrm{o}}(\boldsymbol{y}) \end{bmatrix} \tag{4.84}$$

Next, a first-order estimate of the ripple is computed by integrating the difference between the switched and averaged dynamics as defined in (4.62). For the capacitor voltages, the ripple $\Psi_{1,v_{c,k}}$ is obtained as

$$\Psi_{1,v_{c,k}}(t' - 1 + s) = \frac{1}{C}\int_{t'-1}^{t'-1+s} \left[s_{k+1}(\tau) - s_k(\tau)\right]\bar{i}_L \mathrm{d}\tau \tag{4.85}$$

where $s \in [0, 1)$. For the inductor current, the ripple Ψ_{1,i_L} is obtained as

$$\Psi_{1,i_L}(t' - 1 + s) = \frac{1}{L}\int_{t'-1}^{t'-1+s} \left(v_\mathrm{in} s_{n_c}(\tau) - \bar{v}_\mathrm{o} + \sum_{k=1}^{M}\left[s_k(\tau) - s_{k+1}(\tau)\right]\bar{v}_{c,k}\right)\mathrm{d}\tau$$
$$- \frac{1}{L}\left(v_\mathrm{in} D - \bar{v}_\mathrm{o}\right) \tag{4.86}$$

For the output voltage, the ripple Ψ_{1,v_o} is given by

$$\Psi_{1,v_\mathrm{o}} = 0 \tag{4.87}$$

as the output voltage dynamics do not contain any time-dependent terms. The order-1 ripple estimate can be vectorized into the form of (4.62) as

$$\boldsymbol{\Psi_1} = \begin{bmatrix} \Psi_{1,v_{c,1}} & \cdots & \Psi_{1,v_{c,M}} & \Psi_{1,i_L} & \Psi_{1,v_\mathrm{o}} \end{bmatrix}^\mathrm{T} \tag{4.88}$$

For the capacitor voltages, the quantity $\frac{\partial \Psi_{1,v_{c,k}}}{\partial i_L}$ can be shown to satisfy

$$\int_{t'-1}^{t'} \frac{\partial \Psi_{1,v_{c,k}}}{\partial i_L} \cdot g_{1,i_L}(\boldsymbol{y})\,\mathrm{d}\tau = 0 \tag{4.89}$$

for operation with symmetric PS-PWM. Therefore, the order-1 contribution to the average capacitor voltage dynamics is obtained from (4.63) as

$$g_{2,v_{c,k}}(\boldsymbol{y}) = \frac{1}{C}\int_{t'-1}^{t'} \left[s_{k+1}(\tau) - s_k(\tau)\right] \Psi_{1,i_L}(\tau)\,\mathrm{d}\tau \tag{4.90}$$

Thus the order-1 KBM averaged capacitor voltage dynamics are expressed as

$$\frac{\mathrm{d}}{\mathrm{d}t'}\bar{v}_{c,k} = T_\mathrm{s}^2 \cdot g_{2,v_{c,k}}(\boldsymbol{y}) \tag{4.91}$$

$$= T_\mathrm{s}^2 \cdot \frac{1}{C}\int_{t'-1}^{t'} \left[s_{k+1}(\tau) - s_k(\tau)\right] \Psi_{1,i_L}(\tau)\,\mathrm{d}\tau \tag{4.92}$$

Substituting (4.86) and applying the change of variables $t = t' \cdot T_\mathrm{s}$ to the right-hand side yields

$$\frac{\mathrm{d}}{\mathrm{d}t'}\bar{v}_{c,k} = \frac{1}{C}\int_{t-T_\mathrm{s}}^{t} \left[s_{k+1}(\sigma) - s_k(\sigma)\right] \Psi_{1,i_L}(\sigma)\,\mathrm{d}\sigma \tag{4.93}$$

In the original timescale, the capacitor voltage dynamics are given by

$$\frac{\mathrm{d}}{\mathrm{d}t}\bar{v}_{c,k} = \frac{1}{CT_\mathrm{s}}\int_{t-T_\mathrm{s}}^{t} \left[s_{k+1}(\sigma) - s_k(\sigma)\right] \Psi_{1,i_L}(\sigma)\,\mathrm{d}\sigma \tag{4.94}$$

This expression is identical to (4.5), confirming the charge modeling approach studied in this chapter.

Through the KBM approach, higher-order coupling between the ripple and averaged dynamics can be studied by continuing the recursive procedure highlighted in (4.61)–(4.64) for $\boldsymbol{G_3}$, $\boldsymbol{\Psi_3}$, and so on. For most pulse width-modulated converters this is unnecessary, as the first-order calculation of ripple (where the ripple is modeled as piecewise-linear) captures the real trajectories of state variables accurately. In the FCML converter, higher-order

descriptions of the ripple can prove useful for designs and operating conditions where the trajectories of the capacitor voltages and inductor current are piecewise-sinusoidal. In particular, converter operation near "nominal" conversion ratios results in inductor currents with very small ripple amplitudes that are not accurately described by piecewise-linear expressions [131]. These cases are not studied in this thesis, but represent opportunities for including second-order (piecewise-parabolic) inductor current models.

Chapter 5

Conclusions and Directions for Future Study

5.1 Summary of Contributions and Conclusions

This dissertation represents the state of the art in dynamical modeling of the FCML converter for active balancing control. An active balancing controller is first developed from standard averaging methods used in power converter analysis. The resulting closed-loop system is shown to enable better capacitor voltage tracking during line transients compared to naturally balanced operation, but exhibits instabilities at light loads due to the unmodeled impact of the inductor current ripple on the capacitor voltage dynamics. A refined model of the converter is subsequently developed from the theory of generalized averaging, and shown to accurately capture both the natural balancing dynamics and the instabilities that arise in closed-loop operation with controllers developed from averaging. Finally, a modeling technique based on charge flow analysis is presented, and is shown to yield simple approximate expressions for the converter dynamics that are compatible with straightforward implementation of state-feedback controllers. The resulting closed-loop systems are stable at light loads as the impact of inductor current ripple on the capacitor voltages is considered.

The research presented in this work is relevant for applications where FCML converters represent an attractive alternative to conventional solutions, but have not been adopted due to concerns about robustness and reliability, especially under transient conditions. These include converters for medium- and high-voltage grid-connected applications, front-end dc/ac and dc-dc systems in next-generation datacenters, and on-chip integrated converters. The presented methods for active balancing control enable accurate capacitor voltage tracking and closed-loop dynamics that can be defined through selection of controller gains. More importantly, the control techniques do not sacrifice the dynamic capability of the converter output and can be implemented in parallel with typical control loops for regulating the inductor current and output voltage. All controllers presented are compatible with low-cost industry-standard microcontroller hardware, and enable improved balancing without

the addition of large passive components or the use of high-voltage power semiconductor devices.

The following sections survey areas for continued research in modeling and control for FCML converters. Extensions of the methods proposed in Chapters 3 and 4 and areas for more detailed study are summarized.

5.2 Future Studies of Generalized Averaged Modeling

Switching Signal Phase Shifts as Control Inputs

The reduced-order model obtained in Section 3.3 is expressed generally as

$$\langle \dot{\boldsymbol{x}} \rangle_0 = \hat{\boldsymbol{A}}\left(\boldsymbol{d}, \boldsymbol{\phi}\right) \cdot \langle \boldsymbol{x} \rangle_0 + \hat{\boldsymbol{B}}\left(\boldsymbol{d}, \boldsymbol{\phi}\right) \cdot \langle v_{\text{in}} \rangle_0 \tag{5.1}$$

Here, the component matrices $\hat{\boldsymbol{A}}$ and $\hat{\boldsymbol{B}}$ are parameterized with $\boldsymbol{d}$, a vector collecting the duty ratios of the n_c switching signals as

$$\boldsymbol{d} := \begin{bmatrix} d_1 & d_2 & \cdots & d_{n_c} \end{bmatrix}^{\text{T}} \tag{5.2}$$

and $\boldsymbol{\phi}$, a vector collecting the phase shifts of the n_c switching signals as

$$\boldsymbol{\phi} := \begin{bmatrix} \phi_1 & \phi_2 & \cdots & \phi_{n_c} \end{bmatrix}^{\text{T}} \tag{5.3}$$

Linearizing (5.1) yields

$$\dot{\tilde{\langle \boldsymbol{x} \rangle}}_{\boldsymbol{0}} = \boldsymbol{F} \cdot \tilde{\langle \boldsymbol{x} \rangle}_{\boldsymbol{0}} + \boldsymbol{G_1} \cdot \tilde{\boldsymbol{d}} + \boldsymbol{G_2} \cdot \tilde{\boldsymbol{\phi}} \tag{5.4}$$

where

$$\boldsymbol{F} = \hat{\boldsymbol{A}}\left(\overline{\boldsymbol{d}}, \overline{\boldsymbol{\phi}}\right) \tag{5.5}$$

$$\boldsymbol{G_1} = \left(\nabla_{\boldsymbol{d}} \left[\hat{\boldsymbol{A}}\left(\boldsymbol{d}, \boldsymbol{\phi}\right) \cdot \overline{\langle \boldsymbol{x} \rangle}_{\boldsymbol{0}} \right] + \nabla_{\boldsymbol{d}} \left[\hat{\boldsymbol{B}}\left(\boldsymbol{d}, \boldsymbol{\phi}\right) \cdot \overline{\langle v_{\text{in}} \rangle}_0 \right] \right)_{\overline{\langle \boldsymbol{x} \rangle}_{\boldsymbol{0}}, \, \overline{\boldsymbol{d}}, \, \overline{\boldsymbol{\phi}}} \tag{5.6}$$

$$\boldsymbol{G_2} = \left(\nabla_{\boldsymbol{\phi}} \left[\hat{\boldsymbol{A}}\left(\boldsymbol{d}, \boldsymbol{\phi}\right) \cdot \overline{\langle \boldsymbol{x} \rangle}_{\boldsymbol{0}} \right] + \nabla_{\boldsymbol{\phi}} \left[\hat{\boldsymbol{B}}\left(\boldsymbol{d}, \boldsymbol{\phi}\right) \cdot \overline{\langle v_{\text{in}} \rangle}_0 \right] \right)_{\overline{\langle \boldsymbol{x} \rangle}_{\boldsymbol{0}}, \, \overline{\boldsymbol{d}}, \, \overline{\boldsymbol{\phi}}} \tag{5.7}$$

$$\tag{5.8}$$

Here, the notation $\nabla_{\boldsymbol{d}}$ indicates the Jacobian with respect to the vector of duty ratios $\boldsymbol{d}$ and $\nabla_{\boldsymbol{\phi}}$ indicates the Jacobian with respect to the vector of phase shifts $\boldsymbol{\phi}$. Allowing the phase shifts to vary independently offers a new degree of freedom for controlling the capacitor voltages. Future work can identify whether the new control input vector $\boldsymbol{\phi}$ allows for simpler balancing control laws compared to control with only the duty ratios. Additionally, future studies can investigate whether allowing the phase shifts to vary independently yields controllable small-signal dynamics at all conversion ratios and operating points.

Extension of Methods to Other Hybrid Switched-Capacitor Converter Topologies

As highlighted in Section 3.6, a key advantage of generalized averaged modeling is its compatibility with a wide range of operating waveforms. Once the vector fields corresponding to the switched converter dynamics are expressed as nonlinear expressions of the state variables and switching signals, the methods of [89] highlighted in Chapter 3 can be methodically applied to analyze the averaged converter dynamics. As a straightforward extension of the analysis in this work, the generalized averaging procedure could be applied to study the capacitor voltage dynamics in resonant or quasi-resonant operation of the FCML converter, which offer improved efficiencies in applications where only a narrow range of conversion ratios is expected [135–138]. A key difference between resonant operation of the FCML converter and the pulse width modulated operation studied in the previous chapters is the shape of the inductor current waveform. In resonant operation, particularly when the converter is controlled to achieve zero current switching (ZCS) such as the demonstration in [139], the inductor current takes a rectified sinusoidal shape at the resonant frequency. The capacitor voltage resonates with the inductor and exhibits non-negligble ripple at the fundamental component of the switching frequency. The generalized averaging method can be applied to characterize the capacitor voltage dynamics during line and load transients and can inform design practices for robust operation. Following from the discussion in Chapter 3, the question of how many inductor current harmonics one must model to accurately capture the capacitor voltage dynamics is also relevant for resonant operation of the converter.

A less straightforward, but valuable extension of the generalized averaged modeling in this work is its application to analysis of the broader class of regulating hybrid switched-capacitor topologies such as those presented in [15, 140–143]. In these converters, the sequence of switching states and the connections formed between flying capacitors and inductors differ from the FCML converter, however the capacitor voltage dynamics are coupled to inductor current ripples and standard averaging methods cannot accurately model the capacitor voltage behavior. The method of generalized averaging can be applied to accurately study the capacitor voltage dynamics in these converters during line and load transients, and can also offer insight into control loop design for high-bandwidth regulation of the output voltage.

5.3 Future Studies of Charge Models for Capacitor Dynamics

Balancing at Nominal Conversion Ratios and Operating Mode Transitions

Chapter 4 presents methods for studying the capacitor voltage dynamics in a 4-level FCML converter through the perspective of net charge flow. Plant models are derived for all three operating modes of the converter. Future work can extend the models to ensure capacitor

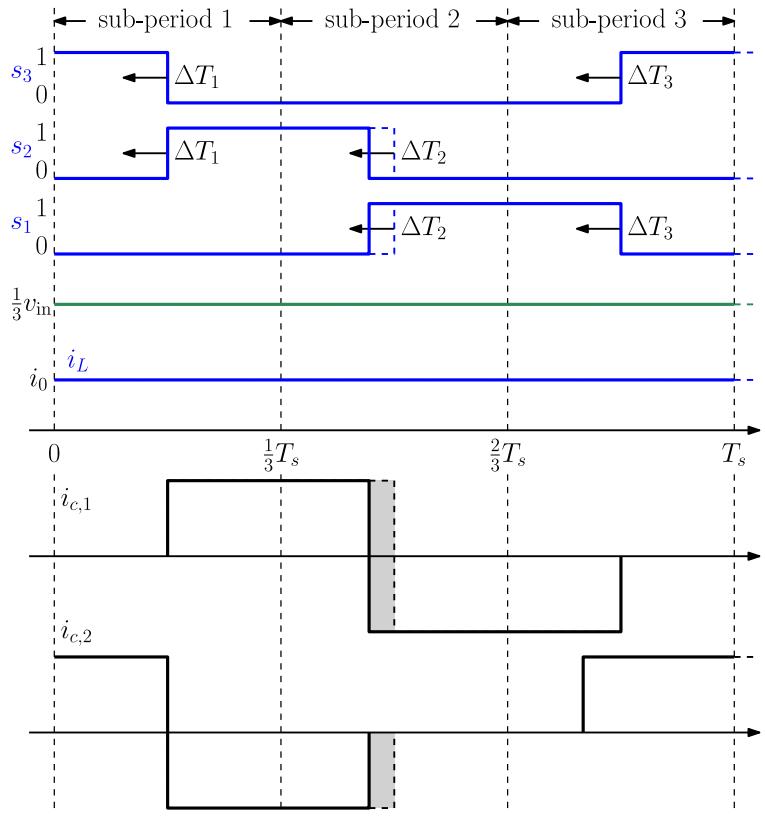


Figure 5.1: Converter waveforms illustrating the small-signal capacitor current response when $M = 1/3$ to a perturbation in the switching signal edges occurring in sub-period 2.

voltage balancing at the nominal conversion ratios $M = 1/3$ and $M = 2/3$ representing the boundaries between the operating modes. At nominal conversion ratios, a total number of 3 switching states occur over the interval of a switching period. Approximating the inductor current ripple as linear yields a nominally constant inductor current over the entire switching period. Fig. 5.1 illustrates the impact of perturbing the edges of switching signals s_2 and s_1 occurring in sub-period 2.

Following the methods of Chapter 4 the small-signal impact of perturbations in the switching edges on the capacitor voltages can be studied by quantifying the net change in capacitor charge. One aspect of nominal conversion ratio operation that demands further study is that the linear ripple approximation of the inductor current is inaccurate when the switching frequency is not significantly greater than the LC resonant frequency corresponding to the series connection of flying capacitors and the inductor. While this is also true for operation at other conversion ratios, higher-order effects influencing the capacitor voltage balancing such as the impacts of the capacitor voltage ripple can have pronounced impacts at nominal conversion ratios [131]. As discussed in Section 4.5, one possible method to mitigate the modeling error is to consider a higher-order KBM averaged model, such as one

that considers piecewise-parabolic inductor current ripple.

The transition between operating modes is a detail of controller implementation that remains to be addressed. In Chapter 4, three different control laws are presented, as the open-loop poles and the impacts of switching edge perturbations vary between the operating modes. Smooth transitions between operating modes are necessary when the input voltage is subjected to large-signal transients, such as those typical of start-up and shut-down scenarios. As the state-feedback control laws shown in Chapter 4 are straightforward to implement in standard microcontroller hardware, the control laws for all three operating modes can be pre-programmed as sub-routines called by the primary control loop interrupt that runs once per switching period. This primary interrupt can decide to transition between the control laws based on measurements of the input and output voltages and calculations of the conversion ratio $M = v_{\mathrm{o}}/v_{\mathrm{in}}$. Some implementation details that need to be considered include appropriate filtering of the input and output voltage and de-rating of the balancing controller gains to prevent the control loop from cycling between control laws for different operating modes when the conversion ratio is near an operating mode boundary.

Generalization for the N-Level Case

An obvious extension of the work in Chapter 4 is the study of the N-level case. To systematically treat charge flow in higher-level converters, a general description of the charge flow for each operating mode m_{op} of an N-level converter must be developed. Subsequently, the impact of perturbations in the switching node voltage pulse position in each sub-period must be analyzed. The *capacitor connection matrix*, a key contribution in the works of [76, 144], can assist in this methodical treatment. The capacitor connection matrix identifies the sequence and polarity in which capacitors are connected to the inductor in each switching phase of the converter. A general expression for the integrated inductor current in each switching phase can first be derived representing the slopes of the inductor current symbolically with independent variables. Using the capacitor connection matrix, these expressions can be aggregated into components of net charge flow into the flying capacitors. Naturally, the treatment of higher-level converters requires more careful study of the controllability of capacitor voltages as the conversion ratio is varied, particularly at nominal conversion ratios.

Other Topics in Modeling and Control of FCML Converters

A large body of current research topics in modeling and control of FCML converters can be developed and re-examined using the charge models presented in Chapter 4. First, the natural balancing dynamics considering the effects of the resistor R_{s} can be examined by modifying the charge model using the KBM averaging theory highlighted in Section 4.5. The parasitic resistor typically introduces a weak damping action that acts to naturally balance the capacitor voltages. Modeling the effects of this damping element can provide an estimate of the minimum damping action that the active balancing controller must provide to balance the capacitor voltages faster than the natural balancing case.

The KBM averaging approach of Section 4.5, which generalizes the charge modeling approach presented for operation with PS-PWM, can be applied to study the capacitor voltage behavior in alternative modulation schemes. Current programmed modulation (CPM), where the switching actions are determined by the comparison of the inductor current to a reference waveform, has been applied to FCML converters in [42, 47, 49], as it promises faster inductor current dynamics and faster natural balancing capability compared to the natural dynamics under symmetric PS-PWM. As highlighted in [47], however, instabilities arise for some CPM schemes depending on the conversion ratio and design parameters such as the peak-to-peak steady-state inductor current ripple. Averaged models using charge models obtained from KBM averaging can provide analytical insight into the balancing capabilities under CPM, operating conditions resulting in unstable capacitor voltages, and possible active balancing techniques for stabilizing capacitor voltages under CPM.

A final area of interest is the observation of capacitor voltages using a reduced number of sensors. The active balancing demonstrations highlighted in this work measure capacitor voltages directly using differential sensing circuits for each flying capacitor. In practice, these circuits can be costly and detract from the system power density. In [129] and [144], estimation schemes are proposed to calculate the capacitor voltages from single-ended measurements of the switching node voltage v_{sw}. The experimental results in [144] illustrate that this single-sensor approach is capable of reconstructing the capacitor voltages over a wide operating range. In particular, [144] focuses on real-time implementation compatible with active balancing controllers—continued research in this area such as the work of [145] aims to improve the robustness of this single-sensor approach and integrate it with active balancing controllers. One drawback of the estimation approaches of [129, 144] is sensitivity to noise on the switching node voltage measurement, and the propagation of this noise into all of the calculated flying capacitor voltages. While advanced filtering methods such as those proposed in [146] can mitigate the impacts of this noise, their implementation is limited by the computation capability of the digital controller. State observers, which internally incorporate a dynamic model of the plant to calculate the system state variables, can offer improved performance in this context. The charge models of Chapter 4 yield simple expressions for the plant behavior that are straightforward to incorporate in standard microcontroller hardware. In one possible approach, a single capacitor voltage can be measured differentially and the remaining can be computed as the output of the observer. Naturally, research in this area must address the required separation between the observer and active balancing controller dynamics to obtain satisfactory closed-loop performance.

All of the topics listed in this final section are addressed to differing extents in the literature, but can benefit from simple models of the capacitor voltage dynamics. The latter two are of particular interest as they can enable lower-cost FCML converter implementations including fully integrated solutions. Continued studies in all of these areas can enable robust and high-performance implementations of FCML converters in the broader industry.

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Appendix A

Application of Singular Perturbation Theory for Model Order Reduction

The singular perturbation approach [90–92] seeks to simplify dynamical systems consisting of variables that evolve at different characteristic time-scales. The original system is approximated with a new one of lower dimension that captures the relevant "slow" behavior. The theory typically assumes that systems are partitioned into the standard form

$$\begin{aligned} \dot{\boldsymbol{x}} &= \boldsymbol{f}\left(\boldsymbol{x}, \boldsymbol{z}, \epsilon\right) \\ \epsilon\dot{\boldsymbol{z}} &= \boldsymbol{g}\left(\boldsymbol{x}, \boldsymbol{z}, \epsilon\right) \end{aligned} \tag{A.1}$$

where $\boldsymbol{x}$ is a vector containing all of the "slow" state variables, and $\boldsymbol{z}$ is a vector containing all of the "fast" state variables. In the case of the FCML converter, the time-scale separation of interest is that between the slow flying capacitor voltage dynamics and the fast dynamics of the inductor current ripple. The scalar parameter ϵ quantifies the extent to which the dynamics of $\boldsymbol{x}$ are slow with respect to those of z. In this work ϵ is $1/\omega_{\mathrm{s}}$.

The standard form of (A.1) can be expressed in a fast time-scale $t' = t/\epsilon$ as

$$\begin{aligned} \frac{\mathrm{d}}{\mathrm{d}t'}x &= \epsilon f(x, z, \epsilon) \\ \frac{\mathrm{d}}{\mathrm{d}t'}z &= g(x, z, \epsilon) \end{aligned} \tag{A.2}$$

The approximation of the original system in (A.1) obtained by setting $\epsilon \to 0$ is premised on the existence of a stable equilibrium manifold $z = h(x)$ obtained from (A.2) with $\epsilon \to 0$ satisfying

$$g(x, h(x), 0) = 0 \tag{A.3}$$

The fast time-scale dynamics of the inductor current harmonics in (3.37) are equivalently

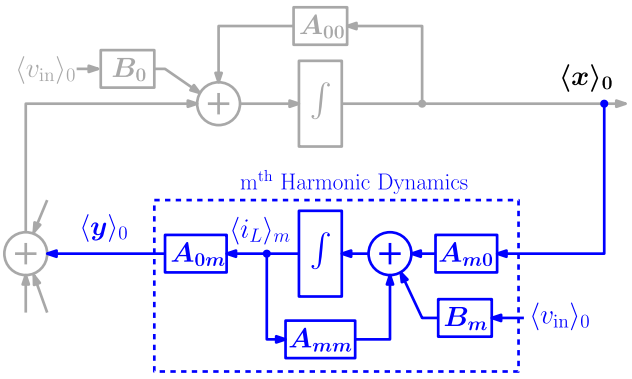

Figure A.1: Block diagram representation of the feedback dynamics corresponding to the m^{th} harmonic coefficient of the inductor current.

expressed via the error dynamics

$$\frac{\mathrm{d}}{\mathrm{d}t'}\eta = -jm\left(\frac{jm\omega_s L + R_s}{jm\omega_s L}\right)\eta \tag{A.4}$$

$$\eta = \left(\langle i_L\rangle_m - \frac{\langle v_{\text{sw}}\rangle_m}{R_s + jm\omega_s L}\right) \tag{A.5}$$

The characteristic decay rate of the error η in the fast time-scale is

$$\alpha_{t'} = \text{Re}\left\{-jm\left(\frac{jm\omega_s L + R_s}{jm\omega_s L}\right)\right\} = -\frac{R_s}{\omega_s L} \tag{A.6}$$

Since $\alpha_{t'} < 0$ always holds for nonzero R_s, the equilibrium manifold is attractive. In the slow time-scale, this characteristic rate corresponds to a time constant $\tau = L/R_s$ associated with convergence of the inductor current harmonics to the manifold. For singular perturbation theory to be valid in this work, τ must be significantly smaller than the time constants of all modes participating in the capacitor voltage dynamics.

This claim also follows from the feedback representation of the fast and slow subsystems depicted in the block diagram of the full generalized averaged model in Fig. 3.3. Fig. A.1 highlights the dynamics of the m^{th} harmonic coefficient of the inductor current. Its contribution to the 0^{th} order state variables (i.e. the output of the feedback dynamics) is denoted $\langle \boldsymbol{y}\rangle_0$. The dynamics of $\langle \boldsymbol{y}\rangle_0$ is given in the Laplace domain as

$$s\langle i_L\rangle_m = \boldsymbol{A_{mm}}\cdot\langle i_L\rangle_m + \boldsymbol{A_{m0}}\cdot\langle \boldsymbol{x}\rangle_0 + \boldsymbol{B_m}\cdot\langle v_{\text{in}}\rangle_0 \tag{A.7}$$

$$\langle \boldsymbol{y}\rangle_0 = \boldsymbol{A_{0m}}\cdot\langle i_L\rangle_m \tag{A.8}$$

If the inductor current harmonics settle to the equilibrium manifold quickly, the $\langle i_L\rangle_m$ quickly settles to a steady-state values that only depends on the inputs (the slow state variables). Thus, with the assumption that τ is small relative to the timescales of interest for the slow

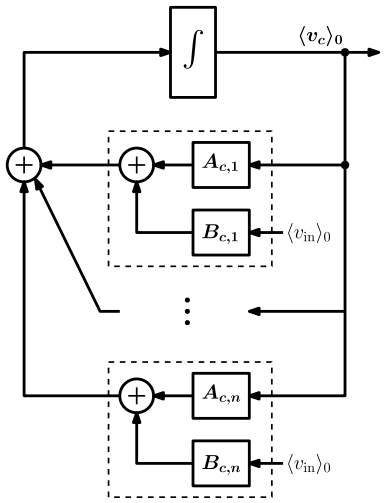

Figure A.2: Block diagram depiction of equivalent system when the feedback dynamic blocks in the full generalized averaged model represented in Fig. 3.3 are substituted with their dc gains. This structure is identical to the parallel feedback form shown in Fig. 3.9.

dynamics, $\langle \boldsymbol{y} \rangle_0$ can be approximated as the result of $\langle \boldsymbol{x} \rangle_0$ multiplied by the dc gain of the feedback dynamics obtained by setting $s \to 0$

$$\langle \boldsymbol{y} \rangle_0 = \lim_{s \to 0} \left[\boldsymbol{A_{0m}} \cdot (s\boldsymbol{I_{2\times 2}} - \boldsymbol{A_{mm}})^{-1} \cdot (\boldsymbol{A_{m0}} \cdot \langle \boldsymbol{x} \rangle_0 + \boldsymbol{B_m} \cdot \langle v_{\text{in}} \rangle_0) \right] \tag{A.9}$$

Noting that $\boldsymbol{A_{mm}}$ is invertible, the approximated feedback dynamics are given by

$$\langle \boldsymbol{y} \rangle_0 = \boldsymbol{A_{c,m}} \cdot \langle \boldsymbol{x} \rangle_0 + \boldsymbol{B_{c,m}} \cdot \langle v_{\text{in}} \rangle_0 \tag{A.10}$$

$$\boldsymbol{A_{c,m}} = \boldsymbol{A_{0m}} \cdot \boldsymbol{A_{mm}^{-1}} \cdot \boldsymbol{A_{m0}} \tag{A.11}$$

$$\boldsymbol{B_{c,m}} = \boldsymbol{A_{0m}} \cdot \boldsymbol{A_{mm}^{-1}} \cdot \boldsymbol{B_m} \tag{A.12}$$

The singular perturbation approach obtains the reduced model by replacing each of the feedback dynamics shown in Fig. 3.3 with its dc-equivalent gain resulting in the model shown in Fig. A.2 [124, 127]. This model can be further simplified into the parallel feedback form presented in Fig. 3.9.

Appendix B

Linearization of Generalized Averaged Model

Following the procedure described in Section 3.3, the reduced-order model is expressed generally as

$$\langle \dot{\boldsymbol{x}} \rangle_0 = \hat{\boldsymbol{A}}\left(\boldsymbol{d}\right) \cdot \langle \boldsymbol{x} \rangle_0 + \hat{\boldsymbol{B}}\left(\boldsymbol{d}\right) \cdot \langle v_{\text{in}} \rangle_0 \tag{B.1}$$

For clarity, matrices $\hat{\boldsymbol{A}}$ and $\hat{\boldsymbol{B}}$ are parameterized with $\boldsymbol{d}$, a vector collecting the duty ratios of the n_c switching signals defined as

$$\boldsymbol{d} := \begin{bmatrix} d_1 & d_2 & \cdots & d_{n_c} \end{bmatrix}^{\mathrm{T}} \tag{B.2}$$

Using the summation representation of $\boldsymbol{A_c}$ in (3.53), the expression of (B.1) can be expanded as

$$\langle \dot{\boldsymbol{x}} \rangle_0 = \left(\boldsymbol{A_0}\left(\boldsymbol{d}\right) + \cdots + \boldsymbol{A_n}\left(\boldsymbol{d}\right)\right) \cdot \langle \boldsymbol{x} \rangle_{\boldsymbol{0}} + \left(\boldsymbol{B_0}\left(\boldsymbol{d}\right) + \cdots + \boldsymbol{B_n}\left(\boldsymbol{d}\right)\right) \cdot \langle v_{\text{in}} \rangle_0 \tag{B.3}$$

where

$$\boldsymbol{A_0}\left(\boldsymbol{d}\right) = \left[\begin{array}{ccc|cc} 0 & \cdots & 0 & \frac{d_2-d_1}{C} & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & \frac{d_{n_c}-d_M}{C} & 0 \\ \hline \frac{d_1-d_2}{L} & \cdots & \frac{d_M-d_{n_c}}{L} & -\frac{R_s}{L} & -\frac{1}{L} \\ 0 & \cdots & 0 & \frac{1}{C_o} & -\frac{1}{RC_o} \end{array}\right] \tag{B.4}$$

$$\boldsymbol{A_m}\left(\boldsymbol{d}\right) = \left[\begin{array}{c|c} \boldsymbol{A_{c,m}} & \boldsymbol{0} \\ \hline \boldsymbol{0} & \boldsymbol{0} \end{array}\right] \tag{B.5}$$

$$\boldsymbol{B_0}\left(\boldsymbol{d}\right) = \left[\begin{array}{ccc|cc} 0 & \cdots & 0 & d_{n_c} & 0 \end{array}\right]^{\mathrm{T}} \tag{B.6}$$

$$\boldsymbol{B_m}\left(\boldsymbol{d}\right) = \left[\begin{array}{c|cc} \boldsymbol{B}_{\boldsymbol{c,m}}^{\mathrm{T}} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{B.7}$$

Here $\boldsymbol{B}_{\boldsymbol{c},\boldsymbol{m}}^{\mathrm{T}}$ indicates the m^{th} column of $\boldsymbol{B}_{\boldsymbol{c}}$ in (3.45).

Note that as the duty ratios are allowed to vary independently in active balancing scenarios, $\boldsymbol{A_0}$ is first expressed generally without the assumption $d_k = d_{k+1}$. The small-signal model is obtained via Jacobian linearization of matrices $\hat{\boldsymbol{A}}$ and $\hat{\boldsymbol{B}}$ at the quiescent point of symmetric PS-PWM characterized by

$$\overline{\boldsymbol{d}} = \begin{bmatrix} D & D & \cdots & D \end{bmatrix}^{\mathrm{T}} \tag{B.8}$$

$$\overline{\langle \boldsymbol{x} \rangle}_{\boldsymbol{0}} = \begin{bmatrix} \frac{\overline{\langle v_{\mathrm{in}} \rangle}_0}{n_c} & \frac{2\overline{\langle v_{\mathrm{in}} \rangle}_0}{n_c} & \cdots & \frac{M\overline{\langle v_{\mathrm{in}} \rangle}_0}{n_c} & \overline{\langle i_L \rangle}_0 & \overline{\langle v_o \rangle}_0 \end{bmatrix}^{\mathrm{T}} \tag{B.9}$$

For compact representation, the evaluation of switching functions (3.16) at the quiescent point is expressed as

$$\overline{\langle s_k \rangle}_m := \langle s_k \rangle_m \Big|_{\boldsymbol{d}=\overline{\boldsymbol{d}}} \tag{B.10}$$

The model takes the general form of (3.58) with

$$\boldsymbol{F} = \hat{\boldsymbol{A}}\left(\overline{\boldsymbol{d}}\right) \tag{B.11}$$

$$\boldsymbol{G} = \left(\nabla_{\boldsymbol{d}} \left[\hat{\boldsymbol{A}}\left(\boldsymbol{d}\right) \cdot \overline{\langle \boldsymbol{x} \rangle}_{\boldsymbol{0}} \right] + \nabla_{\boldsymbol{d}} \left[\hat{\boldsymbol{B}}\left(\boldsymbol{d}\right) \cdot \overline{\langle v_{\mathrm{in}} \rangle}_0 \right] \right)_{\overline{\langle \boldsymbol{x} \rangle}_{\boldsymbol{0}},\, \overline{\boldsymbol{d}}} \tag{B.12}$$

Here, the notation $\nabla_{\boldsymbol{d}}$ indicates the Jacobian with respect to the vector of control inputs $\boldsymbol{d}$. Evaluating (B.12) on (B.3) allows for an expanded representation of (3.58) given by

$$\dot{\tilde{\boldsymbol{x}}} = \left(\boldsymbol{F_0} + \boldsymbol{F_1} + \cdots + \boldsymbol{F_n}\right) \cdot \tilde{\boldsymbol{x}} + \left(\boldsymbol{G_0} + \boldsymbol{G_1} + \cdots + \boldsymbol{G_n}\right) \cdot \tilde{\boldsymbol{d}} \tag{B.13}$$

where the matrices $\boldsymbol{F_0}$ and $\boldsymbol{F_m}$ are given by

$$\boldsymbol{F_0} = \left[\begin{array}{ccc|cc} 0 & \cdots & 0 & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & 0 & 0 \\ \hline 0 & \cdots & 0 & -\frac{R_s}{L} & -\frac{1}{L} \\ 0 & \cdots & 0 & \frac{1}{C_o} & -\frac{1}{RC_o} \end{array}\right] \tag{B.14}$$

$$\boldsymbol{F_m} = \left[\begin{array}{c|c} \boldsymbol{F_{c,m}} & \boldsymbol{0} \\ \hline \boldsymbol{0} & \boldsymbol{0} \end{array}\right] \tag{B.15}$$

$$\boldsymbol{F_{c,m}} = 2\mathrm{Re}\left\{ \frac{1}{Z_m} \begin{bmatrix} \frac{-\overline{\langle \Delta s_1 \rangle}_m^* \overline{\langle \Delta s_1 \rangle}_m}{C_1} & \cdots & \frac{-\overline{\langle \Delta s_1 \rangle}_m^* \overline{\langle \Delta s_M \rangle}_m}{C_1} \\ \vdots & \ddots & \vdots \\ \frac{-\overline{\langle \Delta s_M \rangle}_m^* \overline{\langle \Delta s_1 \rangle}_m}{C_M} & \cdots & \frac{-\overline{\langle \Delta s_M \rangle}_m^* \overline{\langle \Delta s_M \rangle}_m}{C_M} \end{bmatrix} \right\} \tag{B.16}$$

and the matrices $\boldsymbol{G_0}$ and $\boldsymbol{G_m}$ are given by

$$\boldsymbol{G_0} = \begin{bmatrix} \frac{-\overline{\langle i_L\rangle}_0}{C_1} & \frac{\overline{\langle i_L\rangle}_0}{C_1} & 0 & \cdots & 0 & 0 \\ 0 & \frac{-\overline{\langle i_L\rangle}_0}{C_2} & \frac{\overline{\langle i_L\rangle}_0}{C_2} & \ddots & 0 & 0 \\ \vdots & \ddots & \ddots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{-\overline{\langle i_L\rangle}_0}{C_M} & \frac{\overline{\langle i_L\rangle}_0}{C_M} \\ \frac{\overline{\langle v_{\text{in}}\rangle}_0}{n_c L} & \frac{\overline{\langle v_{\text{in}}\rangle}_0}{n_c L} & \frac{\overline{\langle v_{\text{in}}\rangle}_0}{n_c L} & \cdots & \frac{\overline{\langle v_{\text{in}}\rangle}_0}{n_c L} & \frac{\overline{\langle v_{\text{in}}\rangle}_0}{n_c L} \\ 0 & 0 & 0 & \cdots & 0 & 0 \end{bmatrix} \tag{B.17}$$

$$\boldsymbol{G_m} = \left[\begin{array}{c|cc} \boldsymbol{G}_{\boldsymbol{c,m}}^{\mathrm{T}} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{B.18}$$

$$\boldsymbol{G_{c,m}} = 2\mathrm{Re}\left\{ \overline{\langle i_L\rangle}_m \begin{bmatrix} \frac{-\zeta_1^*}{C_1} & \frac{\zeta_2^*}{C_1} & 0 & \cdots & 0 & 0 \\ 0 & \frac{-\zeta_2^*}{C_2} & \frac{\zeta_3^*}{C_2} & \ddots & 0 & 0 \\ \vdots & \ddots & \ddots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{-\zeta_M^*}{C_M} & \frac{\zeta_{n_c}^*}{C_M} \end{bmatrix} + \frac{\overline{\langle v_{\text{in}}\rangle}_0}{n_c Z_m} \begin{bmatrix} \frac{\overline{\langle \Delta s_1\rangle}_0^* \zeta_1}{C_1} & \cdots & \frac{\overline{\langle \Delta s_1\rangle}_0^* \zeta_{n_c}}{C_1} \\ \vdots & \ddots & \vdots \\ \frac{\overline{\langle \Delta s_M\rangle}_0^* \zeta_1}{C_M} & \cdots & \frac{\overline{\langle \Delta s_M\rangle}_0^* \zeta_{n_c}}{C_M} \end{bmatrix} \right\} \tag{B.19}$$

$$\overline{\langle i_L\rangle}_m := \frac{1}{Z_m}\left(\overline{\langle v_{\text{in}}\rangle}_0 \overline{\langle s_{n_c}\rangle}_m + \sum_{k=1}^{M} \frac{\overline{\langle v_{\text{in}}\rangle}_0}{n_c} \overline{\langle -\Delta s_k\rangle}_m \right) \tag{B.20}$$

$$\zeta_k := \frac{\partial}{\partial d_k}\langle s_k\rangle_m \Big|_{d_k = D} = \cos(m\pi D)\, e^{jm\phi_k} \tag{B.21}$$

The small-signal model of [96, 114] obtained from standard averaging is recovered in (B.13) via the 0^{th}-order terms $\boldsymbol{F_0}$ and $\boldsymbol{G_0}$. In (B.19), the model additionally captures the small-signal coupling between duty ratio variations and capacitor voltages via the inductor current harmonics.

Appendix C

Incorporating Integrators, Filters, and Delays in the State-Space Model

This section studies the state-space description of the closed-loop system incorporating the effects of integrators in the controller, measurement filters, and actuator delays. The dynamics of (3.58) are represented as

$$\dot{\boldsymbol{x}} = \boldsymbol{F} \cdot \boldsymbol{x} + \boldsymbol{G} \cdot \boldsymbol{d} \tag{C.1}$$

where

$$\boldsymbol{x} := \begin{bmatrix} v_{c,1} & \cdots & v_{c,M} & i_L & v_\mathrm{o} \end{bmatrix}^\mathrm{T} \tag{C.2}$$

is the small-signal state vector and

$$\boldsymbol{d} := \begin{bmatrix} d_1 & \cdots & d_{n_c} \end{bmatrix}^\mathrm{T} \tag{C.3}$$

is the small-signal vector of control inputs. Tildes and angle brackets are dropped for ease of notation but small-signal analysis of index-0 state variables is implied.

Integrators

The integrator in the PI current controller introduces an additional state to the system. The resulting extended state space is given by

$$\begin{bmatrix} \dot{v}_{c,1} \\ \vdots \\ \dot{v}_{c,M} \\ \dot{i}_L \\ \dot{v}_\mathrm{o} \\ \dot{z} \end{bmatrix} = \boldsymbol{F}_{\mathbf{aug}} \cdot \begin{bmatrix} v_{c,1} \\ \vdots \\ v_{c,M} \\ i_L \\ v_\mathrm{o} \\ z \end{bmatrix} + \boldsymbol{G}_{\mathbf{aug}} \cdot \begin{bmatrix} d_1 \\ \vdots \\ d_{n_c} \end{bmatrix} \tag{C.4}$$

where

$$\boldsymbol{F}_{\mathbf{aug}} = \begin{bmatrix} & & & & & 0 \\ & & \boldsymbol{F} & & & \vdots \\ & & & & & 0 \\ & & & & & 0 \\ & & & & & 0 \\ 0 & \cdots & 0 & 1 & 0 & 0 \end{bmatrix} \tag{C.5}$$

$$\boldsymbol{G}_{\mathbf{aug}} = \begin{bmatrix} \boldsymbol{G} \\ 0 \end{bmatrix} \tag{C.6}$$

Here the appended state variable z is taken to be

$$z = \int_{-\infty}^{t} i_L(\tau)\,\mathrm{d}\tau \tag{C.7}$$

Measurement Filters

Consider a single state in the system, x_k. A first-order filtered version of x_k can be represented as a new state variable y_k with dynamics given by

$$\dot{y}_k = -\omega_{\text{filt}} y_k + \omega_{\text{filt}} x_k \tag{C.8}$$

The transfer function representing this first-order filter can be verified by taking the Laplace transform of both sides of this differential equation, yielding

$$Y_k(s) = \frac{\omega_{\text{filt}}}{s + \omega_{\text{filt}}} X_k(s) \tag{C.9}$$

Incorporating a first order filter for measurement of each flying capacitor voltage results in a new extended state-space representation

$$\begin{bmatrix} \dot{v}_{c,1} \\ \vdots \\ \dot{v}_{c,M} \\ \dot{i}_L \\ \dot{v}_{\text{o}} \\ \dot{z} \\ \dot{v}_{c,1,\text{filt}} \\ \vdots \\ \dot{v}_{c,M,\text{filt}} \end{bmatrix} = \boldsymbol{F}_{\mathbf{filt}} \cdot \begin{bmatrix} v_{c,1} \\ \vdots \\ v_{c,M} \\ i_L \\ v_{\text{o}} \\ z \\ v_{c,1,\text{filt}} \\ \vdots \\ v_{c,M,\text{filt}} \end{bmatrix} + \boldsymbol{G}_{\mathbf{filt}} \cdot \begin{bmatrix} d_1 \\ \vdots \\ d_{n_c} \end{bmatrix} \tag{C.10}$$

where

$$\boldsymbol{F}_{\mathbf{filt}} = \begin{bmatrix} \boldsymbol{F}_{\mathbf{aug}} & \mathbf{0}_{(\boldsymbol{N+1})\times \boldsymbol{M}} \\ \\ \omega_{\text{filt}} \cdot \boldsymbol{I}_{\boldsymbol{M}\times\boldsymbol{M}} & -\omega_{\text{filt}} \cdot \boldsymbol{I}_{\boldsymbol{M}\times\boldsymbol{M}} \end{bmatrix} \tag{C.11}$$

$$\boldsymbol{G}_{\mathbf{filt}} = \begin{bmatrix} \boldsymbol{G}_{\mathbf{aug}} \\ \mathbf{0}_{\boldsymbol{M}\times\mathbf{1}} \end{bmatrix} \tag{C.12}$$

Delays

To model a delay in the feedback loop due to the control action, an input delay is introduced to the state-space system. First, the Pade approximation for the delay is considered. The second-order Pade approximant for e^x (also referred to as [2/2] approximant) is given by

$$e^x \approx \frac{x^2 + 6x + 12}{x^2 - 6x + 12} \tag{C.13}$$

Thus the second-order Pade approximant for a time delay of t_d is given by

$$e^{-st_d} \approx \frac{s^2 - \frac{6}{t_d}s + \frac{12}{t_d^2}}{s^2 + \frac{6}{t_d}s + \frac{12}{t_d^2}} \tag{C.14}$$

The Pade approximation of the delay is realized as a state-space system via the "direct programming technique" [128] which creates a system in controller canonical form. In the realization theory, a general SISO transfer function of the form

$$H(s) = \frac{Y(s)}{U(s)} = \frac{b_n s^n + b_{n-1}s^{n-1} + \cdots + b_0}{s^n + a_{n-1}s^{n-1} + \cdots + a_0} \tag{C.15}$$

is converted in to state-space equivalent

$$\dot{\boldsymbol{w}} = \boldsymbol{A} \cdot \boldsymbol{w} + \boldsymbol{B} \cdot u \tag{C.16}$$

$$y = \boldsymbol{C} \cdot \boldsymbol{w} + \boldsymbol{D} \cdot u \tag{C.17}$$

where

$$\boldsymbol{A} = \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \ddots & \ddots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \\ -a_0 & -a_1 & -a_2 & \cdots & -a_{n-1} \end{bmatrix} \quad \boldsymbol{B} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 1 \end{bmatrix} \tag{C.18}$$

(C.19)

$$\boldsymbol{C} = \begin{bmatrix} b_0 - a_0 b_n & b_1 - a_1 b_n & \cdots & b_{n-1} - a_{n-1} b_n \end{bmatrix} \quad \boldsymbol{D} = b_n \tag{C.20}$$

For the second-order delay applied to the k^{th} plant input, the corresponding state-space model is

$$\dot{\boldsymbol{w}}_{\boldsymbol{k}} = \boldsymbol{A}_{\mathbf{delay},\boldsymbol{k}} \cdot \boldsymbol{w}_{\boldsymbol{k}} + \boldsymbol{B}_{\mathbf{delay},\boldsymbol{k}} \cdot u_k \tag{C.21}$$

$$u_{\text{delay},k} = \boldsymbol{C}_{\mathbf{delay},\boldsymbol{k}} \cdot \boldsymbol{w}_{\boldsymbol{k}} + \boldsymbol{D}_{\mathbf{delay},\boldsymbol{k}} \cdot u_k \tag{C.22}$$

where

$$\boldsymbol{A}_{\mathbf{delay}} = \begin{bmatrix} 0 & 1 \\ -\frac{12}{t_d^2} & -\frac{6}{t_d} \end{bmatrix} \quad \boldsymbol{B}_{\mathbf{delay}} = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \tag{C.23}$$

$$\boldsymbol{C}_{\mathbf{delay}} = \begin{bmatrix} 0 & -\frac{12}{t_d} \end{bmatrix} \quad \boldsymbol{D}_{\mathbf{delay}} = 1 \tag{C.24}$$

Since there are n_c inputs to the plant, the delayed realization corresponds to an addition of $2n_c$ states to the system to represent the delays. Adding delays to the model of (C.10) results in the extended state space

$$\begin{bmatrix} \dot{v}_{c,1} \\ \vdots \\ \dot{v}_{c,M} \\ \dot{i}_L \\ \dot{v}_{\text{o}} \\ \dot{z} \\ \dot{v}_{c,1,\text{filt}} \\ \vdots \\ \dot{v}_{c,M,\text{filt}} \\ \dot{w}_{1,1} \\ \dot{w}_{1,2} \\ \vdots \\ \dot{w}_{n_c,1} \\ \dot{w}_{n_c,2} \end{bmatrix} = \boldsymbol{F}_{\mathbf{delay}} \cdot \begin{bmatrix} v_{c,1} \\ \vdots \\ v_{c,M} \\ i_L \\ v_{\text{o}} \\ z \\ v_{c,1,\text{filt}} \\ \vdots \\ v_{c,M,\text{filt}} \\ w_{1,1} \\ w_{1,2} \\ \vdots \\ w_{n_c,1} \\ w_{n_c,2} \end{bmatrix} + \boldsymbol{G}_{\mathbf{delay}} \begin{bmatrix} d_1 \\ d_2 \\ \vdots \\ d_{n_c} \end{bmatrix} \tag{C.25}$$

where

$$\boldsymbol{F}_{\mathbf{delay}} = \begin{bmatrix} \boldsymbol{F}_{\mathbf{filt}} & \boldsymbol{G}_{\mathbf{filt}} \cdot \boldsymbol{C}_{\mathbf{delay}} \\ \boldsymbol{0}_{\boldsymbol{2n_c}\times(\boldsymbol{N+1+2M})} & \boldsymbol{A}_{\mathbf{delay}} \end{bmatrix} \tag{C.26}$$

$$\boldsymbol{G}_{\mathbf{delay}} = \begin{bmatrix} \boldsymbol{G}_{\mathbf{filt}} \cdot \boldsymbol{D}_{\mathbf{delay}} \\ \boldsymbol{B}_{\mathbf{delay}} \end{bmatrix} \tag{C.27}$$

$$\boldsymbol{A}_{\mathbf{delay}} = \text{diag}\left(\boldsymbol{A}_{\mathbf{delay,1}}, \ldots, \boldsymbol{A}_{\mathbf{delay},\boldsymbol{n_c}}\right) \tag{C.28}$$

$$\boldsymbol{B}_{\mathbf{delay}} = \text{diag}\left(\boldsymbol{B}_{\mathbf{delay,1}}, \ldots, \boldsymbol{B}_{\mathbf{delay},\boldsymbol{n_c}}\right) \tag{C.29}$$

$$\boldsymbol{C}_{\mathbf{delay}} = \text{diag}\left(\boldsymbol{C}_{\mathbf{delay,1}}, \ldots, \boldsymbol{C}_{\mathbf{delay},\boldsymbol{n_c}}\right) \tag{C.30}$$

$$\boldsymbol{D}_{\mathbf{delay}} = \text{diag}\left(\boldsymbol{D}_{\mathbf{delay,1}}, \ldots, \boldsymbol{D}_{\mathbf{delay},\boldsymbol{n_c}}\right) \tag{C.31}$$