High-Performance Bio-sensing ICs

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Acknowledgement

Writing this dissertation, I wholeheartedly believe that getting a PhD is a journey that comprises of many steps and is about going outside of one's comfort zone, making critical but well-informed decisions on the routes to take, communicating with people inside and outside the circle of peers, dedicating the time, potentially pulling all-nighters, and failing, and failing and failing, to finally succeed. Navigating through this journey was impossible without the help of a guide, so I'd like to thank Rikky for all the support throughout this time.

I'd like to thank many of my colleagues and group-mates who genuinely made it easier for me to survive and succeed.

And of course above all, I wouldn't be here today if it was not for the support of my dear Goli and my family. Thank you!

High-Performance Bio-sensing ICs

by

Sina Faraji Alamouti

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University of California, Berkeley

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Abstract

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Recording of bio-signals from the human body has undergone significant improvements in terms of power, speed, and form factor in the past decade due to the help of low-cost compact IC-based solutions. Recent development of these devices focus on integrating multiple sensor inputs in a single IC, enhancing the robustness of the sensor in the face of challenges in ambulatory settings, as well as including some level of smartness in the sensor operation to improve its performance. In this dissertation, a couple of novel examples of the above ICs are presented that achieve state-of-the-art performance while delivering the target functionality. In the first chapter, a heart-rate and oxygen saturation monitoring IC is proposed that leverages a sparse sampling algorithm to significantly lower the sensor power consumption and increase battery life. Then in chapter 3 a sensor IC is discussed that utilizes body-sensor impedance information to help combat the impact of users' motion artifact in biopotential recordings. Lastly, an ultra-low noise current sensor IC is covered in chapter 4 that enables multi-channel sensing of very small electrical currents in biomedical applications. The performance of the above sensor ICs are compared against prior arts and future directions of these projects are discussed at the end of each chapter.

To that whose company eases the troubles.

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Table of Acronyms

Acronym	Description	Acronym	Description
ADC	Analog to Digital Converter	LUT	Look-Up Table
AMB	Ambient Effect	MA	Motion Artifact
CMRR	Common Mode Rejection Ratio	MRI	Magnetic Resonance Imaging
CTDSM	Continuous Time DSM	NS	Noise Shaping
DAC	Digital to Analog Converter	OCT	Optical Coherence Tomography
DAQ	Data Acquisition Unit	OTA	Operational Transconductance Amplifier
DBE	Digital Back-End	PAV	Peaks and Valleys
DNL	Differential Non-Linearity	PCB	Printed Circuit Board
DR	Dynamic Range	PD	Photodetector (or Photodiode)
DSM	Delta-Sigma Modulator	PM	Phase Margin
ECG	Electrocardiography	PPG	Photoplethysmography
EEG	Electroencephalography	PSD	Power Spectral Density
ESI	Electrode Skin Interface	RMS	Root-Mean-Square
FoM	Figure of Merit	RST	Reset
GEVI	Genetically Encoded Voltage Indicator	RZ	Return-to-Zero
HR	Heart Rate	SAR	Successive Approximation Register
INL	Integral Non-Linearity	SFDR	Spurious Free Dynamic Range
IR	Infra-Red	SNDR	Signal to Noise and Distortion Ratio
IRN	Input Referred Noise	SNR	Signal to Noise Ratio
LED	Light Emitting Diode	TFE	Transimpedance Frontend
LFP	Local Field Potentials	THD	Total Harmonic Distortion
LSB	Least Significant Bit	TIA	Transimpedance Amplifier

Acknowledgments

Writing this dissertation, I now wholeheartedly believe that studying a PhD is a journey that comprises of many steps and elements and is about going outside of one's comfort zone, spending a lot of time reading and learning about things that may or may not be helpful in getting to the final destination of a project, making critical but well-informed decisions on the routes to take, communicating with people inside and outside the circle of peers, dedicating the time, potentially pulling all-nighters, and failing, and failing and failing, to finally succeed. Undoubtedly, navigating through such a journey is impossible without the help of a guide, so I'd like to thank Rikky for all the support throughout this time.

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Chapter 1

Biosensors, Goals and Challenges

1.1 History of Biosensing

The recorded history of sensing signals from the body dates back to 2600 BC where Gilgamesh first described and recognized the death of his dear friend by not being able to feel his heart beat, "I touch his heart but it does not beat at all" he said [14]. But as it appears, it took human beings millennia to improve on the methods and add to the signals and information recorded from the body. In 1625 when Santorio of Venice and Galileo published their body thermometer, it was one of the first attempts to try to use an apparatus for recording of a vital sign [56]. After about 80 years, Floyer's report on measuring the timing of pulses using a pendulum was published in 1707 [71]. This trend continued until in 1903 when the first EKG machines were introduced [7]. Later on in 1950s, electrical activity of single neurons in brain of mammals was measured using wires [67]. Later, the advent of patch-clamp electrophysiology in 1970s provided a lot of insight into the synaptic transmission of neurons [60]. In the 1980s to 1990s, silicon microelectrode arrays became the main tool in investigating the communication of neuron groups [16] and even today they still form the standard method in recording of neural activity.

Recording of such signals has always been aimed to provide information about how certain systems and organs in the body operate, assist diagnosis of many physiological and neurological diseases, enhance the prognosis of various medications and treatments, as well as to develop a more thorough understanding of the underlying mechanisms for various illnesses.

1.2 Biosensor Interfaces

Any apparatus used to acquire a biosignal needs to interface with one or multiple parts of the body. Depending on the signal of interest, the recording site, and the signal quality, the type of interface can change. There is a wide spectrum of ways for a device to interact with the human body. From mechanical contact to the body such as in sensing of ECG using piezoelectric materials [23], electrical connection such as in EKG machines, optical

Figure 1.1: Dry snap electrodes fabricated by Florida Research Instruments and generic wet electrodes useful for biopotential measurements.

interfaces as in pulse-oximeters, magnetic and radio-frequency readout such as MRI, high-intensity particles penetrating the body as in X-ray imaging, to the biochemical analysis of body gas or fluids such as human exhales [15]. The focus of this dissertation is however only on electrical and optical interfaces and the following sections review these two interfaces more thoroughly.

Electrical Interfaces

Recording of biopotentials such as Electrocardiogram (ECG), Electroencephalogram (EEG), Electromyogram (EMG), and neural signals such as local field potentials (LFP) and spikes requires electrical contact between the sensor and the recording site. This electrical connection occurs via conductive electrodes contacting the skin, tissue, or nerve endpoints. The advantage of electrical contact is that it provides the most direct access to the recording target and as a result it generally achieves a higher signal quality. Fig. 1.1 shows two sets of dry and wet electrodes useful for biopotential recording. On the other hand, there are a few challenges in making electrical contact to the targets. For one, such a contact requires physical access to the target point and if the target resides within the human body, surgical procedures followed by maintaining an open incision is required. Moreover, the foreign body response generally degrades the recorded signal quality over time and necessitates re-implantation. To address this, wirelessly operating implants have been proposed in the literature to minimize tissue scarring and extend the sensor lifetime in the body [20, 3]. However, this challenge by itself is enough to restrict electrical readout to only applications where the information is otherwise inaccessible such as recording of deep brain neural signals. Another challenge in using electrodes for connection is to achieve a low-impedance contact

Figure 1.2: Apple Watch heart rate and blood oxygen sensors on its back consisting of four LEDs and four photodiodes.

especially when contacting a dry surface such as skin. This will cause a degradation in the signal quality, higher susceptibility to common mode noise and interference, as well as an elevated interface noise level. Chapter 3 focuses on an ambulatory ear-EEG recording device that directly deals with this problem and discusses a potential solution to this challenge.

Optical Interfaces

One other approach in collecting biosignals is the use of light propagation, attenuation, or phase shift when passing through the biological medium. Optical approaches have recently found a lot of interest due to their potential in providing access to information within relatively deeper anatomical areas without the need for incisions or tissue displacement. Fig. 1.2 shows Apple Watch series 7 optical sensors that capture user's heart rate and blood oxygenation level using a circular array of four LEDs and four photodiodes. One of the most commonly used optical methods in retrieving biological signals is the measurement of pulse by recording the time domain changes in the venous tissue volume in response to the pulsatile blood flow. The technique, known as photoplethysmography or PPG in short, detects a pulsatile component in the transmitted or reflected light from the tissue whose periodicity corresponds to the cardiac cycle. A major benefit of this technique is that it provides one of the least invasive methods of acquiring the pulse. The topic of PPG and its sensors will be discussed in greater detail in chapter 2. There are plenty of other optical applications that extract information from the body. Optical coherence tomography (OCT) for example provides micrometer resolution 3D scans of the human tissue with detail information about every layer using a low coherence light. This technique has been used for reconstruction of

3D scans of retinal cells [68]. Another application has to do with monitoring of neural activities using optical methods, a field known as optogenetics [82]. Many individually selected neurons are simultaneously excited using a spatial light modulator and the response can be recorded using high sensitivity imagers. Chapter 4 focuses on a recording device that can serve as an implantable imager to capture fluorescent activity of neurons.

One of the challenges of optical methods however is that since the light needs to propagate back and forth into the tissue, it generally requires a higher power level at the source when providing the desired signal with sufficient levels of SNR. This is why many of the optical biosignal recording systems are constrained by either the sensor battery life or the maximum light intensity allowed to penetrate the tissue without exceeding the standard tissue heating limits. Chapter 2 further discusses this bottleneck and proposes an algorithmic solution in the case of pulse-oximeters.

1.3 Biosensing ICs

The development of microfabrication techniques and compact integrated circuits began making an impact on the world of biomedical devices in its early years [61]. From data acquisition and telemetry in implantable devices to transcutaneous devices such as X-ray and ultrasonic imagers, defibrillators, etc. all benefited from compact chips performing analog amplification or digital operations. But the first distinct IC published in ISSCC dates back to 1969 where a reading aid device was proposed consisting of an integrated photo-transistor array reading the image and a switch matrix that interacted with piezoelectric transducers creating mechanical feedback to the blind to perform direct image translation [47]. Ever since that date, ISSCC has witnessed an ever increasing number of articles focused on biomedical applications. Fig. 1.3 shows the number of papers published in ISSCC from 2006 to 2023 relating to a biomedical application. As seen, on average the number of these papers have increased by more than 4× since 2008 highlighting the significance of the biomedical applications in the field of IC design. This increase in the number of publications stems from opportunities enabled by IC design techniques to improve the existing sensors and devices from many aspects.

With a brief review of the published articles on biomedical applications, a number of noticeable trends can be observed among the majority of these papers. Many of these articles aim to exploit the IC form factor to integrate multiple sensor and actuator modalities on a single die, or increase the number of readout and stimulation channels in the chip. Another group of these works employ novel circuit and architectural ideas to improve the signal to noise ratio and the overall quality of sensor output data or to significantly lower the power consumption of the sensor especially in the case of wearable health monitoring devices and medical implants. Lastly in some cases, new sensing or actuation modalities have been introduced enabling completely new applications.

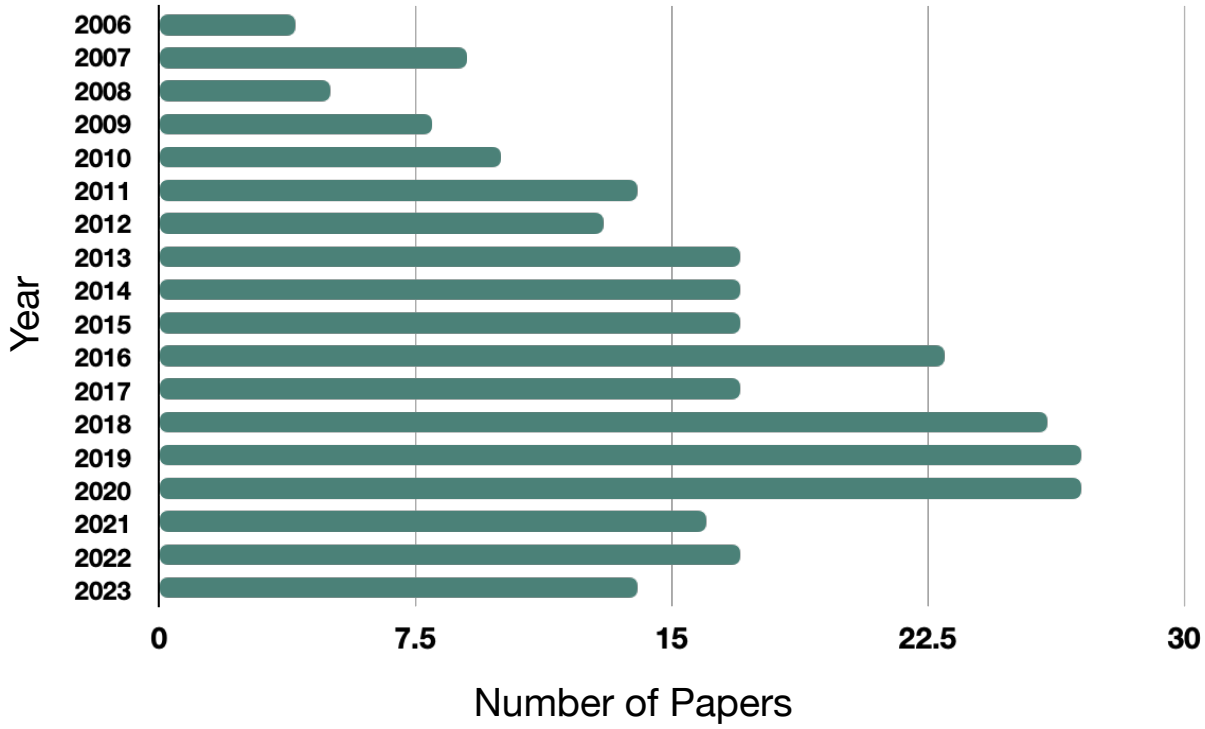


Figure 1.3: Number of papers published in ISSCC with a focus on biomedical applications from 2006 to 2023.

Chapter 2

Low Power HR & S_pO_2 Sensing

2.1 Motivation

Timely diagnosis of many chronic cardiovascular and respiratory systems diseases can be enabled through continuous monitoring of vital signs such as heart rate (HR), blood oxygenation level (SpO_2), respiration rate, blood pressure etc. [4, 5, 72, 49, 17, 70]. A comfortable, wearable device can track these vital signs autonomously, unobtrusively, and without the user's intervention, allowing changes to be immediately detected and reported to medical staff, preventing disease progression. Similarly in patients with a history of heart failure, remote monitoring of vital signals has proven essential in early recognition of potential congestions [5, 70]. Moreover, in the setting of COVID-19, remote monitoring provides the healthcare workforce with real-time biodata without needing any physical contact, reducing the spread of infection [72]. As a result, the interest and market for biosensors in at home care continue to grow. A similar trend is observed for health monitoring wearable devices including smart-watches, rings, and health patches [49]. These devices aim to record a user's vital signs without their intervention. The biodata is recorded, stored, and presented to the user via application interfaces and can be used to warn users of an abnormal condition. Traditionally, electrocardiography (ECG) has been used to accurately measure HR and cardiac waveforms; since it requires access to multiple sites across the body, the subject has to trigger these measurements and thus, it cannot be performed continuously. Photoplethysmography (PPG) is an attractive method to acquire biodata such as HR due to its fully optical, non-invasive nature where the sensors do not even need to contact the subject skin. In addition, using light from two distinct wavelengths, typically red and infra-red (IR), the SpO_2 of the subject can be extracted, a technique known as pulse oximetry. Figure 1 shows the operation of a pulse oximeter where light sources, typically LEDs, are driven sequentially and the reflected light is received by a photodiode (PD), inducing a photocurrent that contains the PPG signal. A current sensing IC, shown in figure 1, then samples and digitizes the photocurrent to output the information.

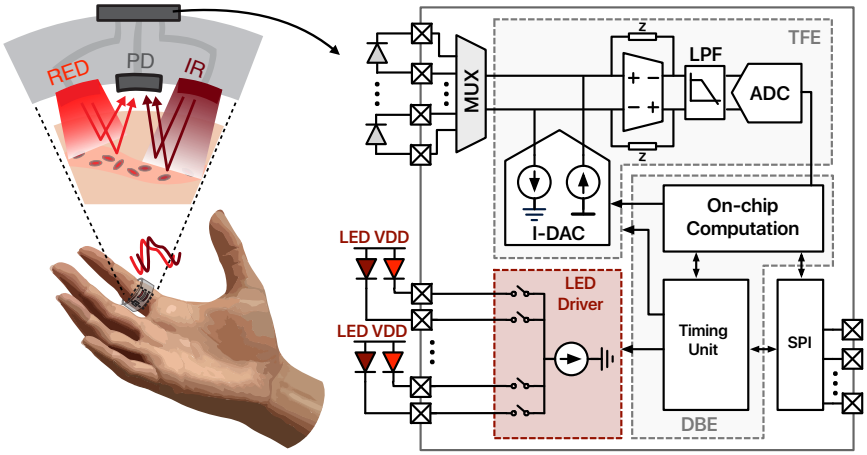


Figure 2.1: Reflectance mode pulse oximetry and typical SpO_2 sensing IC block diagram.

2.2 Devices, Methods, and Prior Arts

Silicon PDs and LEDs are commonly used in today's SpO_2 sensors. Despite great responsivity and mm-scale sizes, they are rigid devices that eventually impact the dimensions and conformality of the sensor. Organic optical devices however are lightweight, mechanically flexible, and shock resistant, and thus offer a more conformal solution, improving user comfort [44, 39, 31]. Flexible vital sign monitoring patches can therefore be built to seamlessly integrate into clothing and be comfortably worn over long durations [31, 11]. In addition, these devices can be printed using low-cost fabrication processes, reducing the overall cost of the health monitoring patches [84, 26].

Commercial SpO_2 sensors operate with mWs of power to drive the LEDs posing strict limits on the sensor battery life. Use of OLEDs further restricts the battery life as these devices generally require higher drive voltages, up to 8 V [31]. Duty cycling has been used in prior arts [10, 63] to lower the power consumption of the overall system at the cost of increased noise bandwidth, impacting signal-to-noise ratio (SNR). The parasitic capacitance of the PD (C_{Par}) impacts the input referred noise of the transimpedance amplifier (TIA) by attenuating the feedback factor as the frequency increases [13]. C_{Par} in silicon PDs ranges from sub-pF to 100s of pF depending on the size of their active area. OPDs however exhibit a much larger C_{Par} up to 10 nF which can exceed the maximum capacitance handled by many of the prior arts. It is thus critical that a sensor IC aimed for a wearable can operate with a wide variety of devices and a wide range C_{Par}. On-chip photodetectors were employed to significantly lower the detector and the interface parasitic capacitance and as a result compensate the SNR penalties at extremely low duty cycle ratios [10, 27]. However, on-chip photodiodes generally offer inferior responsivities compared to their off-the-shelf counterparts, reducing

the power saving benefits of this approach. In addition, there are fundamental limitations on how fast the LEDs can operate as well as the response bandwidth of the PDs, restricting the lower bound of the duty cycle. Moreover, this technique cannot be extended to using organic devices as they are usually fabricated on plastic substrates. [2] tried to balance the tradeoff between SNR and the LEDs and readout power by setting the front-end bias current. The technique significantly reduced the readout power, but the LEDs still dominated the sensor power consumption. Compressive sampling was first introduced in [54] to exploit the sparse nature of the PPG signal and thus save power by reducing the number of sample points. Despite excellent results for HR estimation from the compressively sampled data, SpO_2 measurements required full reconstruction of the PPG waveform out of randomly selected samples, demanding up to 10 mW of processing power [54]. [38] presented the heart-beat-locked-loop technique to make the sensor lock to the PPG signal period and selectively sample the PPG peaks to report HR data. A comparator-based design was used that only detected the input peaks, outputting a digital clock that was synchronized to the input period. This lowered the LED power by a factor of $\sim$6.5$\times$, but since the PPG waveform was not digitized, no SpO_2 measurements were performed.

This work presents an SpO_2 and HR monitoring IC utilizing a reconstruction-free sparse sampling algorithm to reduce the overall system power consumption by about 70%. The remainder of this chapter is strcutured as follows. Section 2.3 outlines the system requirements and the overall architecture of the sensor. In section 2.4, the proposed sparse sampling algorithm is discussed. Section 2.5 describes the circuit-level details of the implemented IC. Bench-top electrical and *in vivo* measurement results are presented in section V followed by the conclusions and comparison against selected prior arts in section VI.

2.3 System Overview

System requirements

As discussed in [48], the PD photocurrent contains multiple components including the detector dark current, the ambient photocurrent, and the reflected light's baseline (I_{DC}) and pulsatile (I_{AC}) components. The overall input baseline component is commonly 40-60 dB stronger than the pulsatile signal. Thus, without any subtraction, the readout chain will need a very large dynamic range, greater than 100 dB [62], which can pose challenges in realizing a low power readout.

The PPG I_{AC} is a low frequency signal with most of its power residing between 0.5 to 5 Hz, which according to the Nyquist theorem can be sampled with frequencies as low as 10 Hz. However, as explained in [38], the timing resolution of the PPG samples can impact the accurate detection of pulsatile peaks, which in turn affects the reported HR error of the sensor. Therefore, a sampling frequency of a few 10s to 100s of Hz is typically selected. In this work, to achieve an average HR error of less than 1 bpm, a sampling rate of 100 S/s is used. Furthermore, to extract SpO_2 with a 2% error, the sensor requires nearly 40 dB of SNR

[21], which determines the noise level of the readout. The amplitude of I_{AC} depends on many biological factors such as the structure, thickness, and color of Epidermis and Dermis, optical factors such as wavelength of light and devices' responsivities, and mechanical factors such as distance between the sensor and tissue as well as the angle of emission. These factors cause the I_{AC} to vary over a wide range from a few nAs to up to 100s of nAs. Thus, to maintain the required SNR for low amplitude inputs, the readout input referred noise density needs to be approximately 1-10 pA/rtHz.

Sensor architecture

The block diagram of a typical SpO_2 sensing IC is shown in Fig. 2.1. LEDs are driven sequentially using on-chip current sources, emitting light at red (660 nm) or green (530nm) as well as IR (880 nm) wavelengths to the tissue. The received photocurrent with a baseline component as large as a few μAs is digitized by the readout. To relax the dynamic range requirements of the chain, the large input DC component is subtracted using differential current DACs (I-DACs). The remaining AC component is then amplified, filtered, and digitized through the readout chain. On-chip digital back-end computes the required code for the DACs, closing the servo-loop. The digitized data is transmitted to an FPGA or a PC via a serial programming interface.

Large values of C_{Par} are an obstacle in achieving low input referred noise in current sensing frontends. Furthermore, C_{Par} poses a constraint on the achievable transimpedance gain and bandwidth in the TIA. As a result, handling very large values of C_{Par} as in OPDs necessitates careful design of the TIA and readout chain. Prior arts have used both capacitive and resistive feedback types in the TIA architecture.

Traditionally, TIAs with capacitive feedback (CTIA) are deployed to achieve the lowest input referred current noise [13]. However, most CTIA designs only handle a few pFs of parasitic capacitance at the TIA input. In order to acquire the current signal out of OPDs with up to 10 nF of C_{Par}, such topologies would require very large values of feedback and load capacitors (100s of pF) to deliver the required noise performance while realizing a reasonable gain. This can result in very large area occupation and demand larger transconductances, increasing the overall power consumption of the TIA. In resistive-capacitive TIAs (ZTIA), the feedback resistor enhances the feedback factor at lower frequencies. This causes the output noise spectrum to only increase at high frequencies, a phenomenon known as "noise peaking". The output noise PSD of the ZTIA can be written in a simplified form as follows:

$$S_{N_{out}}(f) \approx 4kT\left(\frac{1}{g_m}+R_F\right) \times \left(\frac{4\pi^2\frac{R_F}{g_m}C_{Par}^2 f^2+1}{16\pi^4 C_F^2 C_{Par}^2 \frac{R_F^2}{g_m^2} f^4 + 4\pi^2\left(\frac{C_{Par}^2}{g_m^2}+R_F^2 C_F^2\right) f^2 + 1}\right) \quad (2.1)$$

with g_m, R_F, and C_F representing the effective transconductance of the OTA, the feedback resistance and capacitance. Only the OTA thermal noise as well as the feedback resistor's Johnson noise is considered in this analysis. The bandwidth of this noise peaking can be

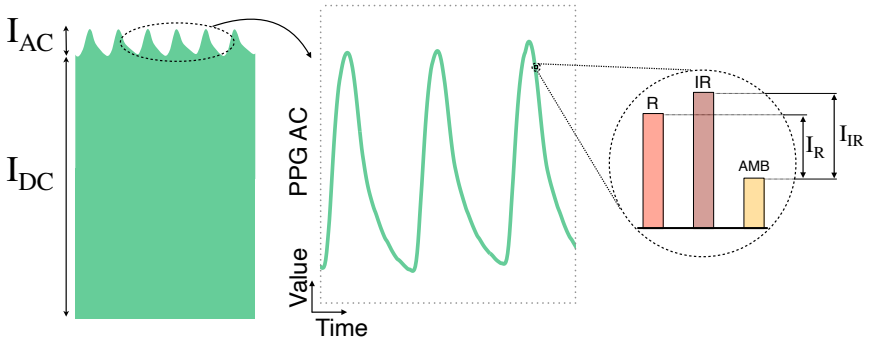


Figure 2.2: PPG signal AC and DC components. Red and IR signals are computed after subtracting the AMB sample, performing system level CDS.

greater than the system's observation bandwidth. It is therefore possible to attenuate the TIA's high frequency noise by means of sufficient filtering through the subsequent blocks. The appendix section covers the derivation of (1) as well as the comparison between CTIA and ZTIA topologies in greater detail. As a result, a ZTIA readout chain can potentially deliver a lower input referred noise compared to CTIA based architectures when C_{Par} is very large and is hence chosen in this design.

2.4 Sparse Sampling of PPG Signal

HR and SpO_2 extraction

Fig. 2.2 shows a typical PPG waveform containing both AC and DC components. The period (T) of the AC component represents a heart-beat cycle and can be used to compute HR. Thus, PPG using a single LED is sufficient to provide HR information. Prior arts have routinely used the average value of the period over 2 or 8 second windows. In this paper, an 8 second window is selected to report HR. (Eq. 2.2)

$$HR = \frac{60}{\overline{T}} \tag{2.2}$$

SpO_2, however, depends on relative concentration of oxygenated versus de-oxygenated hemoglobin, and hence, needs information at two different light wavelengths. As light passes through the tissue, it is attenuated by different elements and this attenuation is described by the extinction coefficient. Light at red and IR wavelengths have been used traditionally [79] since they offer the largest difference in extinction coefficients when passing through oxygenated and de-oxygenated hemoglobin. The value of SpO_2 is computed based on the ratio of AC component over the DC component of red and IR PPG waveforms (Eq. 2.3 &

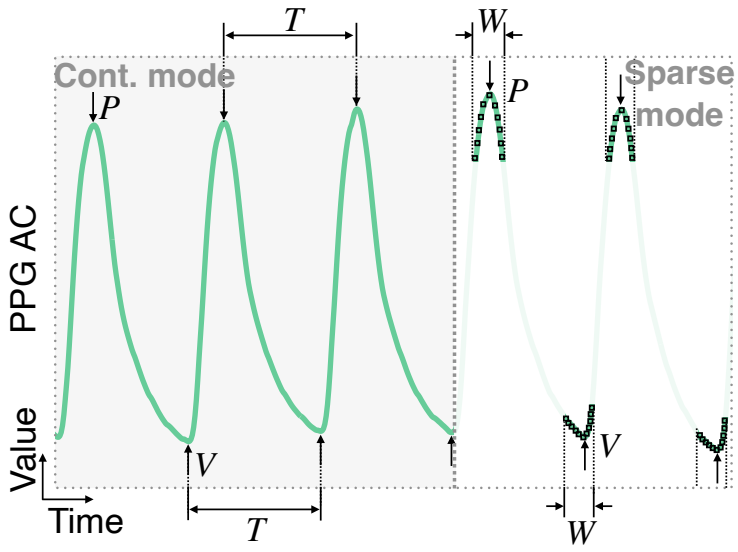


Figure 2.3: Sparse sampling algorithm. The sensor transitions to sparse mode after learning T over multiple cycles where it predicts next PAVs.

2.4). [31]

$$R_{OS} = \frac{I_{AC_{Red}}}{I_{DC_{Red}}} / \frac{I_{AC_{IR}}}{I_{DC_{IR}}} \tag{2.3}$$

$$SpO_2 = \frac{\varepsilon_{Hb_{Red}} - \varepsilon_{Hb_{IR}} \cdot R_{OS}}{\varepsilon_{Hb_{Red}} - \varepsilon_{HbO2_{Red}} + [\varepsilon_{Hb_{IR}} - \varepsilon_{HbO2_{IR}}] \cdot R_{OS}} \tag{2.4}$$

where ε is the extinction coefficient of light at red or IR wavelength through oxygenated or de-oxygenated hemoglobin. To compute SpO_2, only the peak and valley (PAV) values of the PPG signals are needed in the two wavelengths. It is therefore possible to only sample the signal PAVs and as a result save power.

Sparse sampling algorithm

The idea of the proposed sparse sampling algorithm is shown in Fig. 2.3 where the sensor has two modes of operation. The flowchart of this sparse sampling algorithm is also shown in Fig. 2.4. The sensor starts by uniformly sampling the PPG signal at 100 Hz (continuous mode). The period of the AC component (T) is learned over multiple cycles. Once a stable value is realized, the sensor enters the sparse mode where it predicts the upcoming PAVs and takes a few samples centered around them. A window size (W) of $\lceil T/8 \rceil$ is initially selected which can then be reduced upon successful detection of PAVs. A smaller W means that fewer samples are taken and as a result the overall power is decreased. However, larger W allows the backend to accurately detect PAVs in the presence of high heart rate variability.

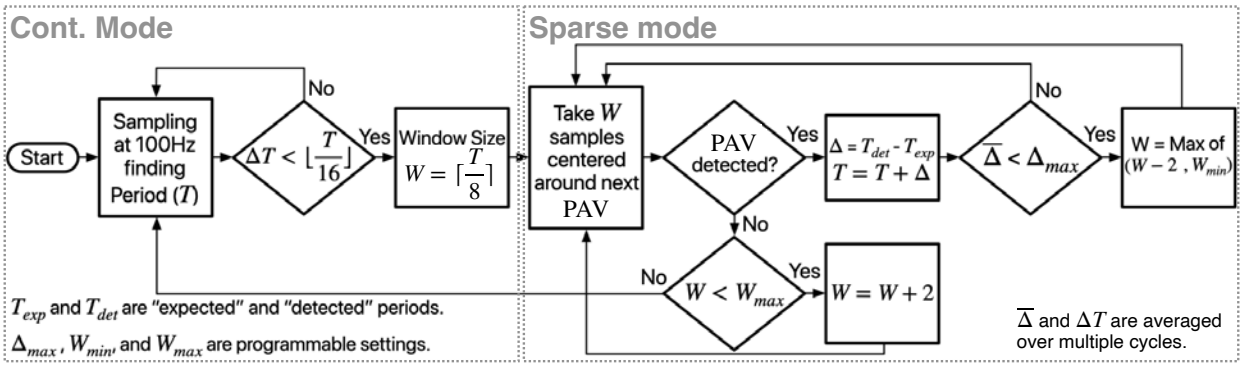


Figure 2.4: Sparse sampling algorithm flow-chart. The system begins with continuous mode sampling at $f_s = 100$ Hz and then transitions to sparse mode upon learning the period, T.

Therefore, cycle-to-cycle updates are made to the estimated value of T to adjust for any period drift. If PAVs are repeatedly missed due to rapid drifts or large motion artifacts, the sensor expands its observation window by increasing W until a programmable maximum, W_{Max}. Without new PAVs detected, the sensor can revert to the continuous mode to re-learn T. The computed T, together with samples taken from signal's PAVs are adequate to provide both HR and SpO_2 information.

Proper detection of PAVs by the backend depends on the SNR of the sparse samples as well as how fast the input is changing. To evaluate the performance of the proposed algorithm at different SNR levels and a range of HR values, a set of MATLAB simulations are run that quantify the reported HR error. The results of such simulations provide information about the required SNR levels at different heart rates to achieve the desired 1 bpm accuracy. These simulations were run with a sine wave input at frequencies ranging from 0.5 to 3 Hz, corresponding to HRs of 30 to 180 bpm, and at amplitudes corresponding to SNRs from 28 to 56 dB. In each run, sparse sampling is performed on the sine wave input and the estimated periods are recorded, averaged over 8 second windows. A total of 12,800 simulations were conducted to capture the mean and variance of the reported HR errors. The results are shown in Fig. 2.5, where the solid lines show the mean error, and the green shades represent the $\pm 3\sigma$ of the computed HR errors. The results confirm that the proposed algorithm provides a robust operation under a wide range of SNR and heart rates. Furthermore, the results demonstrate that a minimum SNR of $\sim$30 dB is sufficient in achieving sub-1 bpm HR error for HRs up to 180 bpm. A similar test is performed in measurements to quantify the performance of the sensor and the results will be discussed in section V.

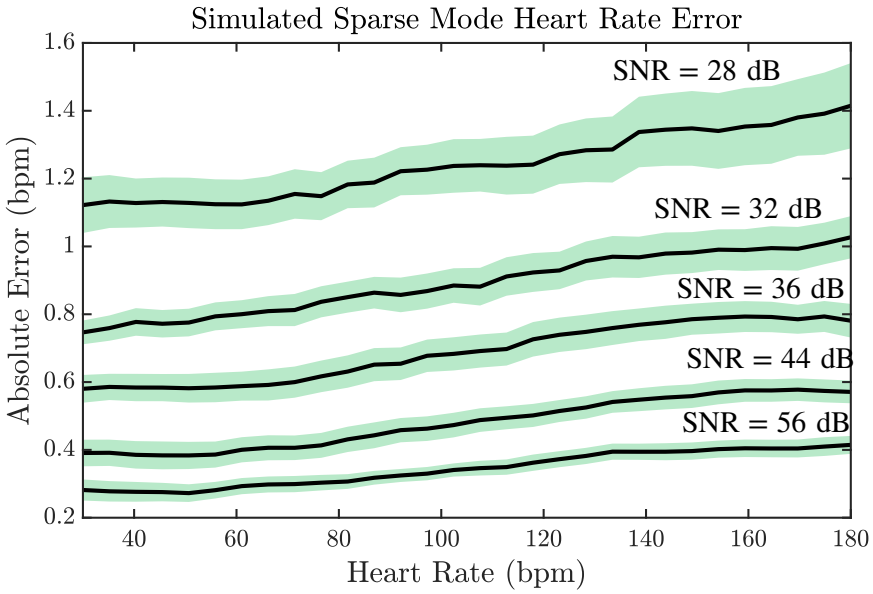


Figure 2.5: Simulated sparse mode HR error for input sine waves at different frequencies and SNRs. Green shades show the $\pm 3\sigma$ range of the error.

2.5 Circuit Implementation

Frontend architecture

Fig. 2.6 shows the detailed block diagram of the transimpedance frontend (TFE) as well as the on-chip digital backend (DBE). The PD is connected and read out differentially at the channel input. The differential readout eliminates the need for a separate low noise bias voltage on the other end of the photodiode. The 0 V bias across the detector also minimizes the PD dark current [25]. 8-bit (5-bit thermometer/3-bit binary coded) differential I-DACs (P and N-DACs) subtract the DC current at the input up to 15 μA. Since the PD current is always in the same direction (cathode to anode), the P and N-DACs at the input are connected considering this polarity. The I-DAC LSB reference current is tunable from 20 to 60 nA to provide a wider range and granularity for the subtraction. N and P I-DAC codes are computed separately to adjust for any mismatch and gain error between them. This calibration only occurs once and the resulting coefficients are programmed into the backend. The DC DAC code for each phase is computed, stored, and updated separately for fastest operation. I-DAC codes are also re-timed prior to entering the DACs to enhance synchronicity and prevent race related glitches. The output current of the I-DACs settles to its expected value in less than 5 μs to not reduce the effective signal duration. The bandwidth of the servo-loop is set via a programmable digital attenuation in the feedback path to have a high-pass corner of $\sim$0.1 Hz. The remaining AC component of the signal is

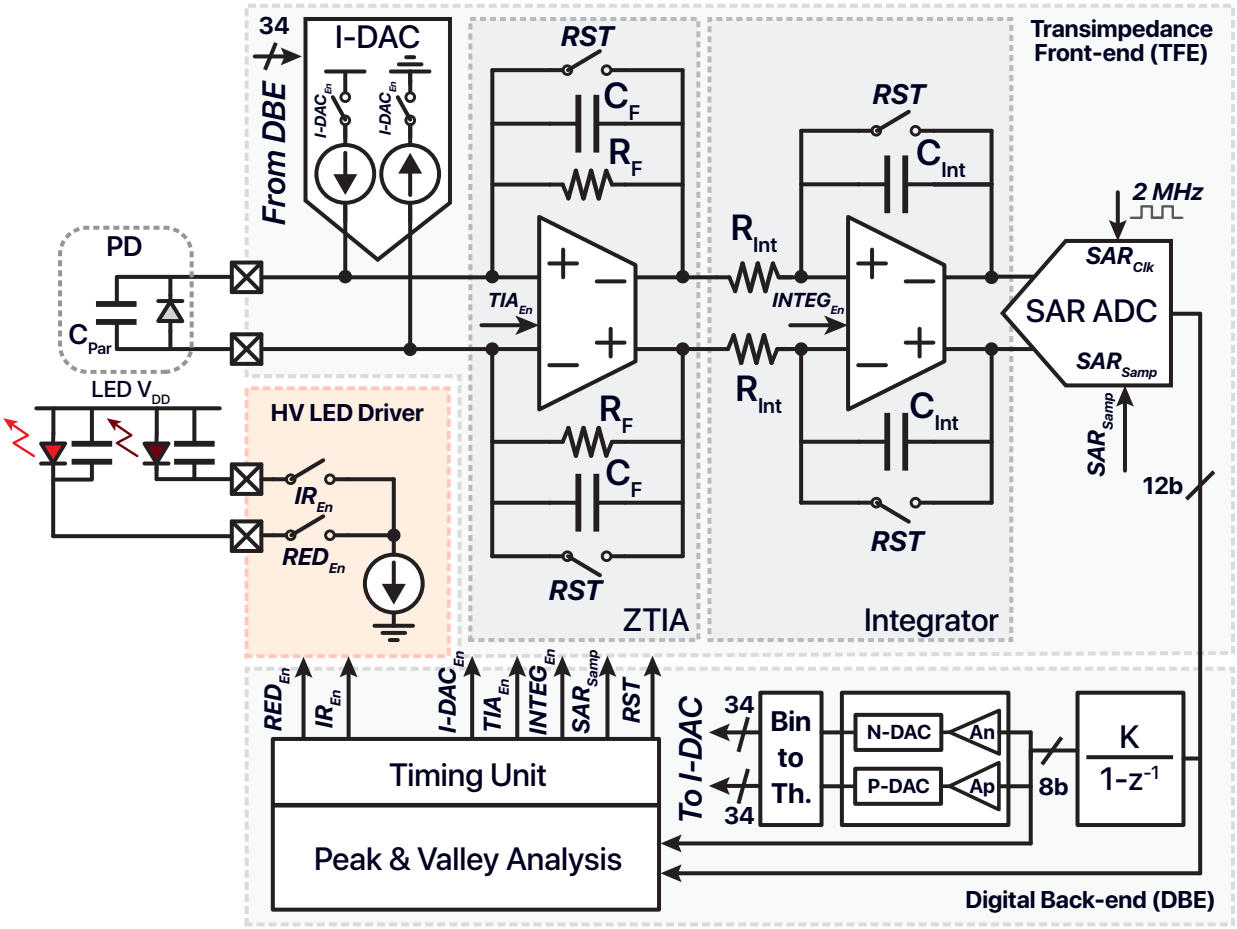


Figure 2.6: Detailed channel block diagram of the chip. The LED driver module is highlighted to indicate the use of HV devices that support up to 8 V of supply.

then amplified via a differential ZTIA followed by a reset integrator that provides additional gain and boxcar averaging, obviating the need for an explicit anti-aliasing filter. A 12-bit synchronous SAR ADC samples the integrator output and delivers the digital code to the DBE.

The timing of TFE operation is diagrammed in Fig. 2.7. Every sample consists of three back-to-back phases. Red and IR signals are acquired followed by an ambient (AMB) phase where no LED is on and the photocurrent due to the ambient light as well as the PD dark current are sampled. AMB must be sampled with each red/IR sample since there can exist time-varying changes in the ambient lighting as well as reflected pulsatile components during this phase. AMB subtraction also serves as a system level correlated double sampling (CDS) that helps remove any offset and flicker noise [63]. T_{RST} and T_{Int} are programmable settings

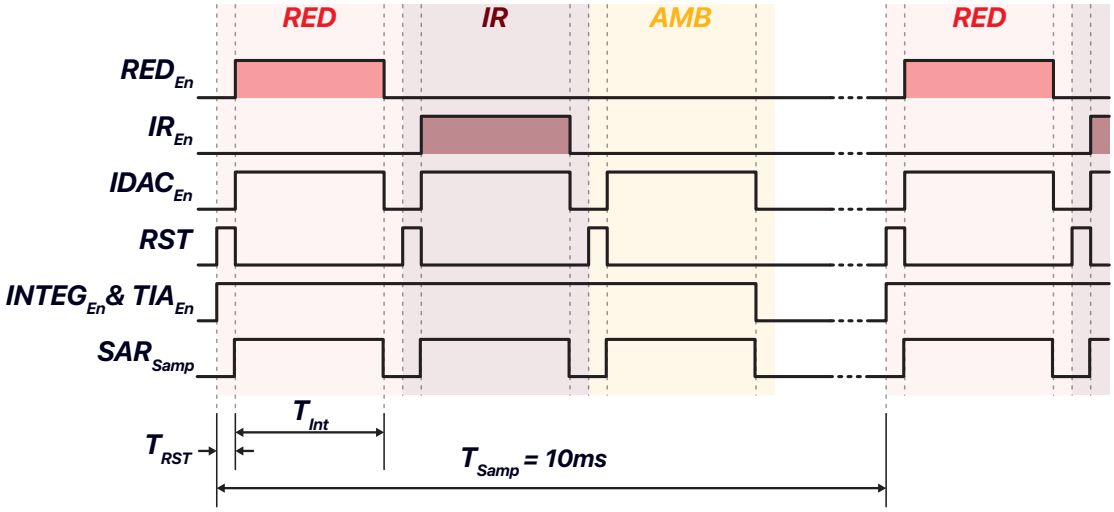


Figure 2.7: Detailed timing diagram of the operation of the sensor. Every set of samples consists of three phases, red, IR, and ambient.

that set the reset and integration durations for TFE. In most measurements, T_{Int} is set from 25 μs to 100 μs with T_{RST} as short as 5 to 10 μs. An on-chip timing unit provides all timing signals to the TFE and LED driver sub-blocks to maintain synchronicity. A peak and valley analysis block within the DBE performs algorithm computations and triggers counters that determine the upcoming sampling windows.

ZTIA design

As previously discussed, a ZTIA topology is utilized to accommodate a wide range of photodiode capacitance (C_{Par}) while maintaining a high SNR. The use of a resistor in the feedback eliminates the reset noise (kT/C) and the need for a separate CDS phase. Fig. 2.8 shows the schematic of the 3-stage current reuse core OTA. The current reuse topology enhances the performance by doubling the effective current efficiency factor (g_m/I_D) of each stage. The fully differential architecture also provides better immunity against supply and common mode noise sources, as well as improved linearity. Fig. 2.9 plots the closed-loop bandwidth and phase margin (PM) of the TIA for C_{Par} ranging from 1 pF to 10 nF. As shown, larger values of C_{Par} reduce the overall bandwidth and as a result increase the PM. The loop maintains a minimum PM of 62° across the entire C_{Par} range. Local and global common mode feedback networks are included to provide common mode bias and improve common mode rejection. Reset switches connect the inputs and outputs of the TIA during the RST phases to quickly bring the outputs to the mid-rail bias point. Values of R_F and C_F are tunable to provide a gain of 1 to 5 MΩ and an adjustable bandwidth. The entire OTA is power

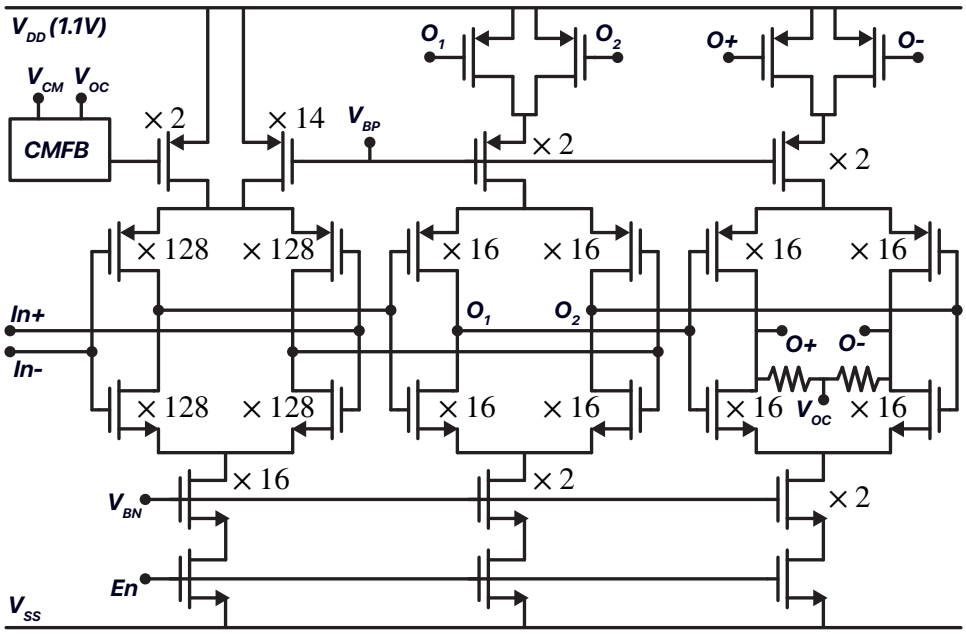


Figure 2.8: Schematic of the ZTIA core OTA. Current reuse topology enhances current efficiency and reduces power. Nested common-mode feedback networks stabilize the OTA in common mode, enhancing CMRR.

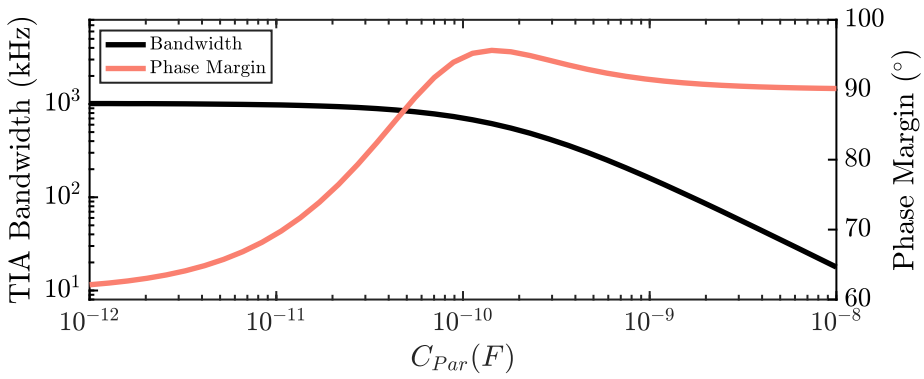


Figure 2.9: Post-extraction simulated TIA bandwidth and phase margin vs. C_{Par}. The OTA shows a minimum of 62° of phase margin over the entire C_{Par} range.

gated using low resistance NMOS transistors to save power outside of sampling windows. The power gating is implemented using switches at the source terminals of the tail current sources to minimize the switching glitch.

Reset integrator and SAR ADC

The RC integrator captures the TIA output over T_{INT} and provides differential outputs to the SAR ADC sampling capacitors. A SAR topology is selected to achieve a low power consumption while providing the required resolution. The value of C_{Int} is tunable to allow for adjustable gain. The integrator is reset at the beginning of every phase via the RST switches. During reset phase, the core OTA is put in unity gain feedback both to empty the integration capacitor as well as to achieve the desired common mode voltage at the OTA input and output nodes. Furthermore, this integration and reset provides a boxcar averaging transfer function detailed in Eq. 2.5.

$$H_{Sinc}(f) = \frac{T_{Int}}{R_{Int} \cdot C_{Int}} \cdot Sinc(T_{Int} \cdot f) \tag{2.5}$$

This low pass transfer function significantly attenuates the high frequency noise content of the TIA output. The feedback capacitors are sized such that the reset kT/C noise of the integrator is insignificant when referred to the channel input. Similar to the OTA, the integrator is shut down outside of sampling windows to save power.

A 12-bit synchronous SAR ADC is implemented using monotonic switching scheme that only needs half the total capacitance compared to traditional switching methods. The ADC uses a 4 fF unit standard cell MOM capacitor to achieve 12-bit linearity. The total ADC sampling cap. is $\sim 16pF$ keeping the ADC kT/C sampled noise standard deviation less than 16 μV. The ADC uses a 1.1V reference voltage for conversion giving an LSB of $\sim$ 265 μV. The SAR ADC uses a 2 MHz reference clock provided by the DBE to perform the conversions. ADC conversion is done shortly after the LED pulse is over and using the 2MHz conversion clock, the ADC output sample is ready in less than 8 μs.

Peripheral circuits

An on-chip PTAT current reference is used to supply the bias current of all analog sub-blocks. The PTAT nature of the reference increases the bias current in proportion to the temperature to maintain a constant noise level in the readout chain. An on-chip HV LED driver, shown in Fig. 2.10 is implemented to drive the LEDs with up to 16 mA of current. The driver uses HV transistors that operate with up to 8 V of supply voltage, enabling the use of OLEDs. The driver is controlled by the timing unit and sinks the current from the LEDs. The drive strength is 5-bit tunable and is separately set for red and IR phases. The entire driver unit is power-gated using HV NMOS switches to minimize wasted power outside of the LED operation phases. Fast start-up circuit quickly brings up the driver bias unit in less than 1 μs. LV (1.1 V) to HV (5-8 V) logic level-shift blocks are implemented within the driver cell to minimize the travel distance of HV logic signals.

The driver unit is tested and its drive current is measured when driving an OLED with about 5.7 nF of parasitic capacitance with up to 16 mA of current. As shown in Fig. 2.11, the current waveform settles in less than 6 μs for all levels of current. The HV shorting

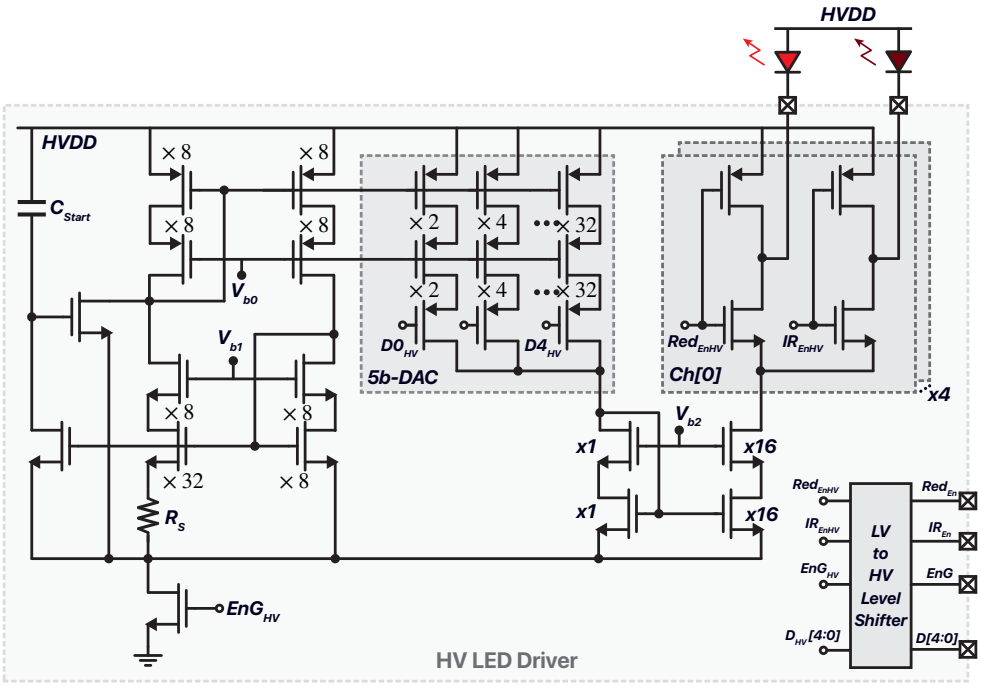


Figure 2.10: The schematic of the HV LED driver is shown. The entire unit is power gate to save power in between the samples.

PMOS switches quickly turn off the OLED once the integration pulse is over bringing the current to zero in less than 7 μs.

2.6 Measurement Results

Chip micrograph and power breakdown

The IC was fabricated in a TSMC 40 nm HV technology and occupies an area of 1.35 × 1.8 mm^2. Fig. 2.12(a) shows the chip micrograph. Two identical channels are implemented on the chip where channel #2 contains features and test amplifiers intended for testing and debugging purposes. The chip power breakdown is depicted in Fig. 2.12(b) & (c). In continuous mode, the sensor consumes a total of 49.7 μW with 45.1 μW, 1.22 μW, and 3.34 μW drawn by the two LEDs, the TFE, and the DBE respectively. Sparse mode significantly lowers the system power consumption to 15.2 µW with LEDs and TFE power going down by ∼75%, while increasing the DBE power by only 2%. The pie chart in Fig. 2.12 shows the breakdown of power consumption of the individual sub-blocks within the TFE in continuous mode where most of the power is dissipated in the ZTIA (79%) to maintain a low input

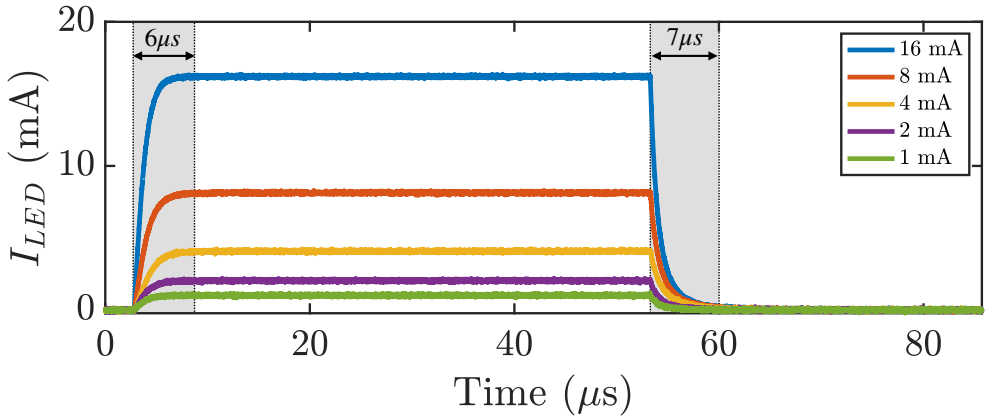


Figure 2.11: The driver current waveform up to 16 mA when driving an OLED with up to 5.7 nF of C_{Par}.

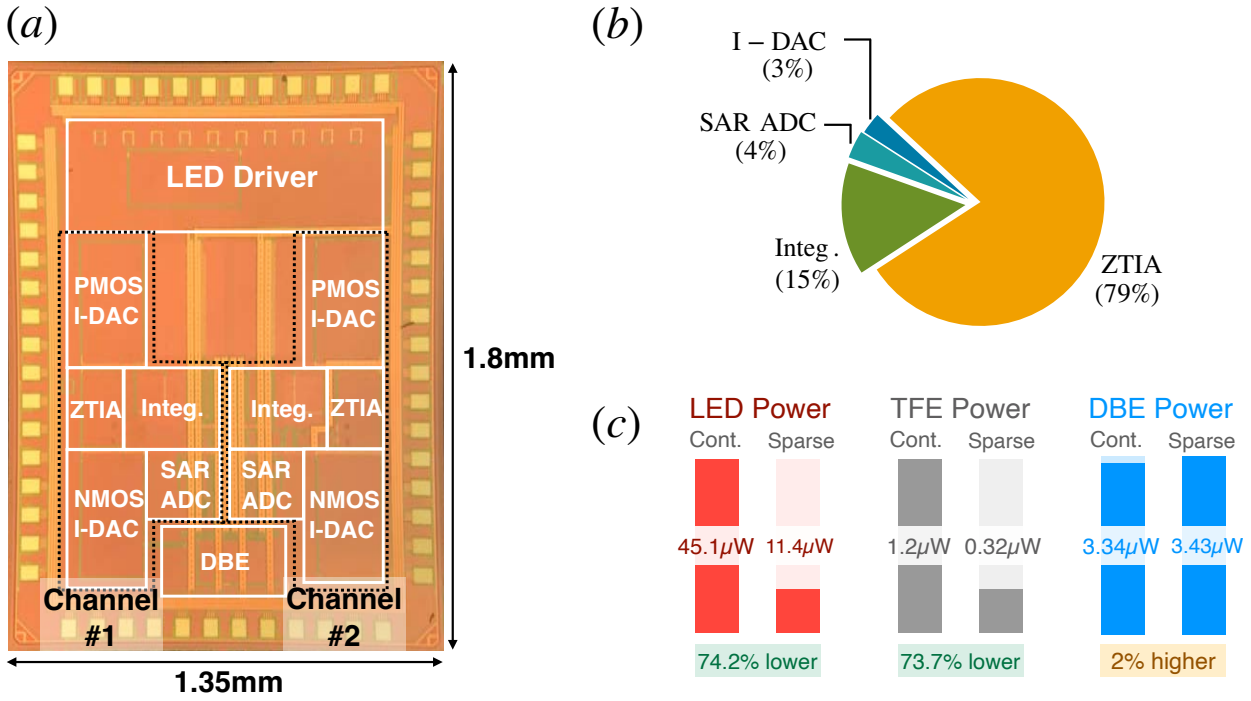


Figure 2.12: Chip micrograph (a). TFE power breakdown in continuous mode. (b) System power reduction between continuous mode and sparse mode. (c)

referred noise.

Electrical measurements

The performance of the TFE was characterized via benchtop electrical measurements and the results are presented. Fig. 2.13(a) shows the input referred noise (IRN) spectrum of the readout at 40 MΩ of overall gain. The measurement was performed with a C_{Par} = 40 pF matching the capacitance of the commercial PD. It achieved a noise spectrum density of 4.8 pA/rtHz and 10.8 pA_{rms} integrated noise over the 5 Hz bandwidth. IRN increased with C_{Par} as plotted in Fig. 2.13(b) for C_{Par} as large as 10 nF, the largest measured capacitance of the OPDs [31]. The ADC output spectrum for a 2 Hz sine wave input with 50 nA_{pp} of amplitude is shown in Fig. 2.13(c). The TFE achieved an SFDR of 68.3 dB and an SNDR of 62.4 dB with the 3^{rd} harmonic forming the largest spur.

The simulation results from section III (Fig. 2.5) were verified via similar benchtop measurements. A set of 48 measurements were performed while providing a sine wave to the TFE with sparse mode enabled. The frequency of the sine wave was swept from 0.5 to 3 Hz, corresponding to 30 to 180 bpm HR. Two different amplitudes were selected for the input sine wave to achieve two distinct SNR levels, 32 dB and 44 dB. Fig. 2.14 presents the measured effective HR error for every experiment. The measured results are well in agreement with the simulation, confirming the performance and robustness of the algorithm. Less than 1 bpm of average error was measured with an SNR as low as 32 dB for HR up to 180 bpm.

In vivo results

A set of *in vivo* experiments were performed with the sensor in both continuous and sparse modes of operation. In these experiments, the sensor was placed on the index finger of a healthy adult in a sitting position, under typical incandescent lighting and at room temperature. To evaluate the accuracy of the sensor output, a clinical grade pulse-oximeter (Wellue HPO) was attached to the subject's ring finger to perform measurements simultaneously with the sensor IC. In the first experiment, commercial PDs and LEDs were used as interface devices and the PPG signal, the HR, and the SpO_2 results were recorded. Fig. 2.15 plots these results against data from the clinical reference. The accuracy of the sensor was maintained after transitioning to sparse mode where the HR and SpO_2 mean absolute errors only rose from 0.3 bpm and 0.5% to 0.4 bpm and 0.7% respectively. The errors were computed based on the total 40 seconds duration of the recording presented in Fig. 2.15 in both modes of operation. Fig. 2.16 shows a set of 30 similar recordings of HR and SpO_2 measurements in sparse mode and compares the results against the clinical reference. The measured standard deviation of error for HR and SpO_2 recordings were 0.24 bpm and a 0.21% respectively.

A similar experiment was performed using a set of flexible organic devices discussed in [31] and [25]. The OPD has a measured C_{Par} of 4.8 nF, less than 10 nA dark current at 0 V bias, and provides a quantum efficiency (QE) of ∼30-40% over the red and IR wavelengths [25]. The red and IR OLEDs exhibit about 5.7 nF and 6.2 nF of parasitic capacitance respectively

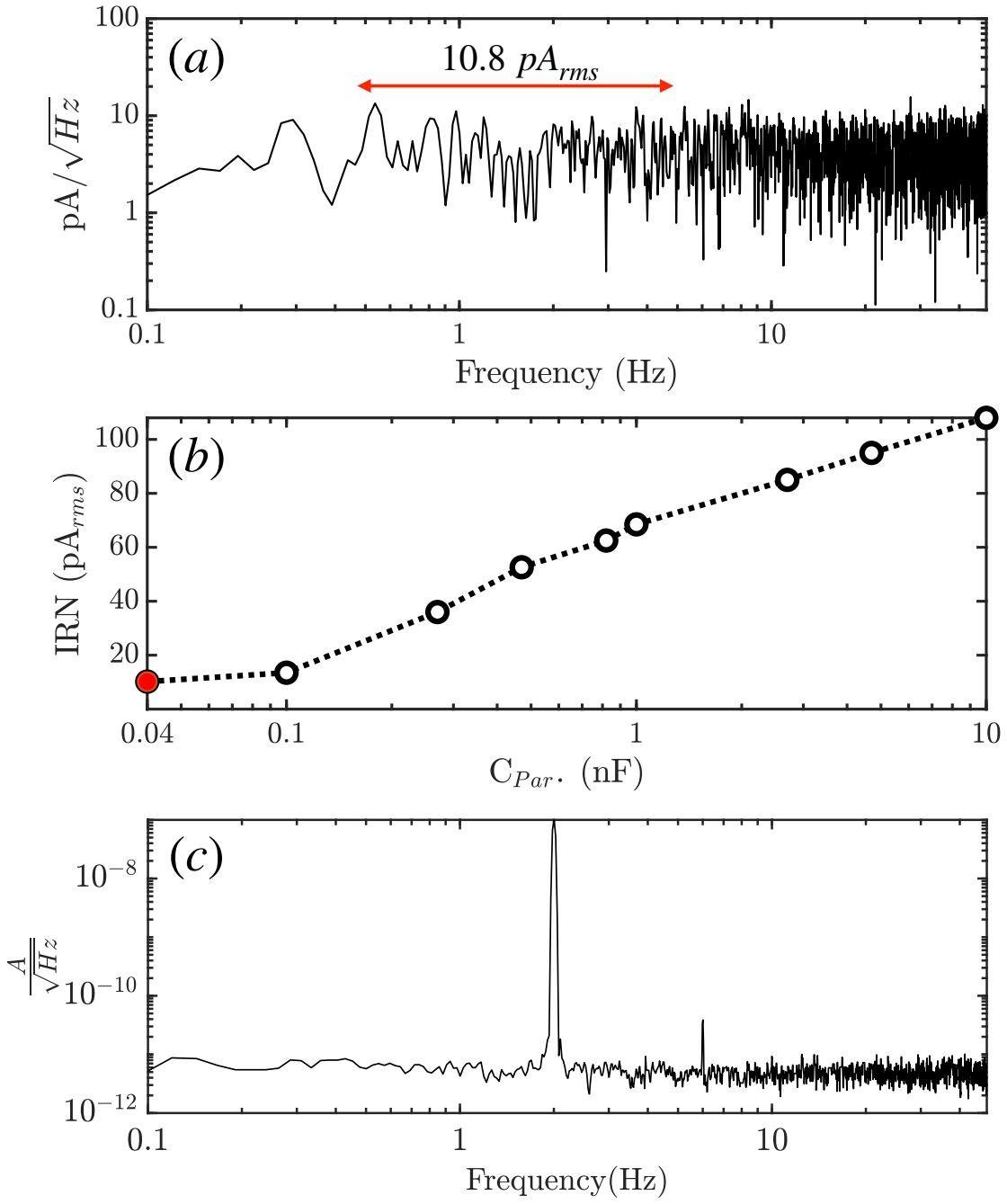


Figure 2.13: Electrical testing results. (a) IRN spectrum for a 40 pF C_{Par}. (b) Integrated IRN over 5 Hz bandwidth vs. C_{Par}. The red dot corresponds to the spectrum from (a). (c) ADC output spectrum for a 2 Hz sine wave input.

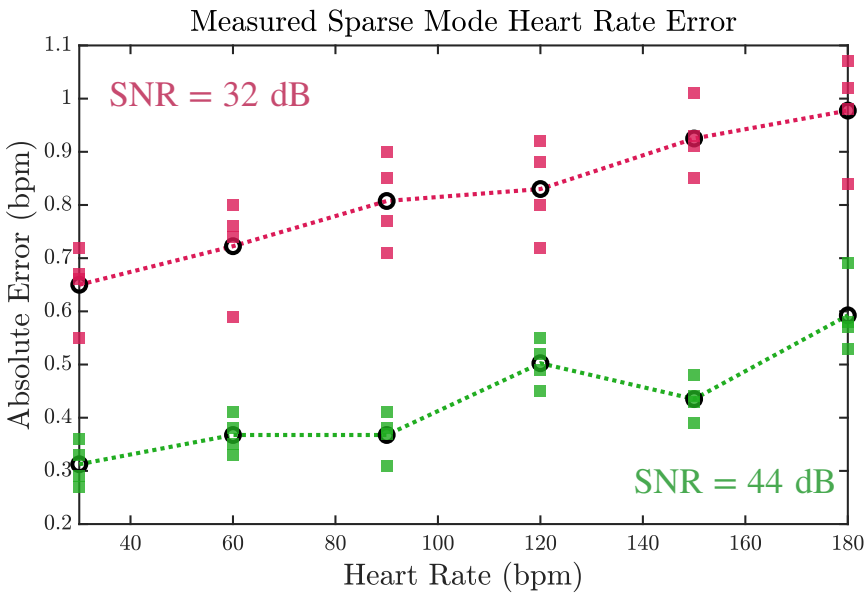


Figure 2.14: Measured sparse mode HR error with input sine waves at different frequencies and at two levels of SNR. Black circles show the average error at each rate. The computed error is the mean absolute error over 8 s windows.

and as shown in [25] require about 5-7 V of forward voltage at 10 mA of current. The PPG waveform, and the corresponding measured HR and SpO_2 are plotted in Fig. 2.17 in both continuous and sparse modes. The sensor achieved less than 1 bpm and less than 1% HR and SpO_2 errors when compared against the clinical reference. The use of organic devices required a higher drive voltage (8 V), an increased drive current as well as a higher (0.5%) duty cycle ratio resulting in overall higher power consumption. However, enabling sparse mode significantly lowered the OLED power by about 75%, improving sensor battery life. Fig. 2.18 presents the measurement setup of the *in vivo* recordings where an FPGA interface is used to read out data via the serial interface and transfer the data to a PC where the results are analyzed and plotted. Fig. 2.19 also presents a summary of the *in vivo* results using (a) commercial and (b) organic devices.

Fig. 2.20 captures an incident where the sparse mode operation is interrupted by a motion artifact that is large enough to create a big difference in sampled PAV values compared to the previously captured PAVs. This causes an unwanted shift in the estimated period and results in the following PAVs to be missed. As shown in the figure, the sensor initially tries to find new PAVs by expanding the observation window and increasing W. Since no new PAVs are found after W reaches W_{Max}, the sensor eventually reverts to continuous mode. Shortly after this transition occurs, the backend re-learns the signal period and the system re-enters sparse mode.

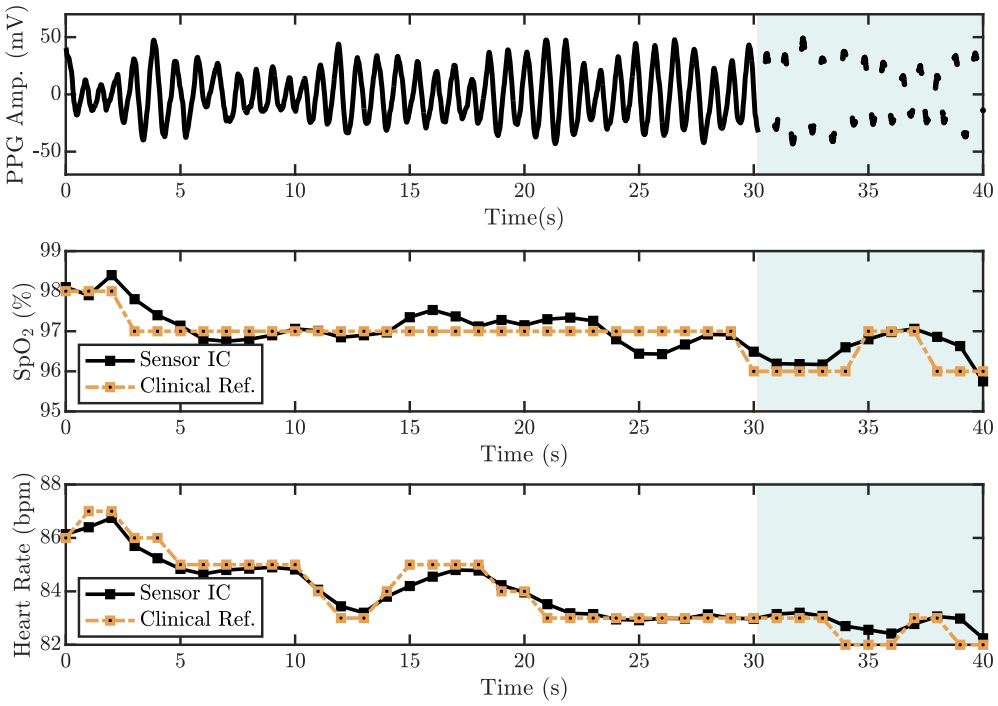


Figure 2.15: *In vivo* verification of the sensor IC in both continuous and sparse modes using commercial silicon PD and LEDs. The PPG waveform and its corresponding HR and SpO_2 measurements are shown.

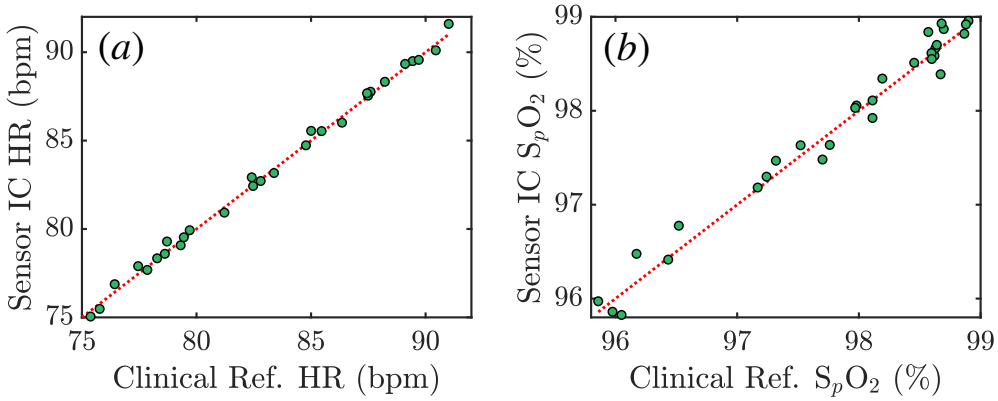


Figure 2.16: HR and SpO_2 measurements from a set of 30 recordings using silicon PD and LEDs. The red dotted line shows the fit line.

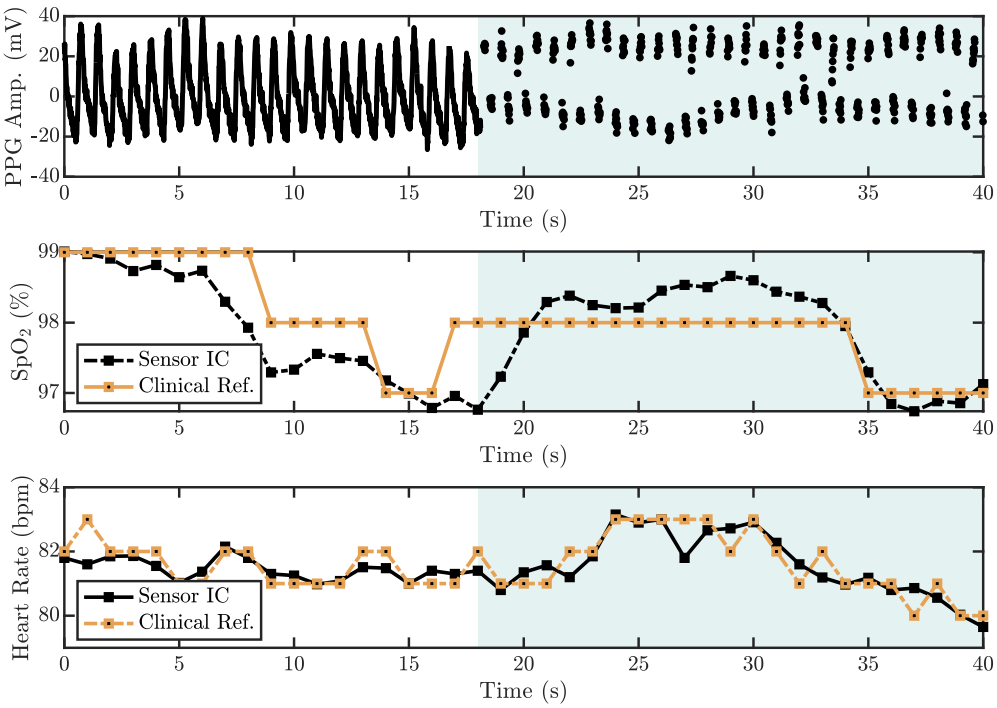


Figure 2.17: *In vivo* verification of the sensor IC in both continuous and sparse modes using organic interface devices (OLEDs & OPDs). The PPG waveform and the corresponding HR and SpO_2 measurements are shown.

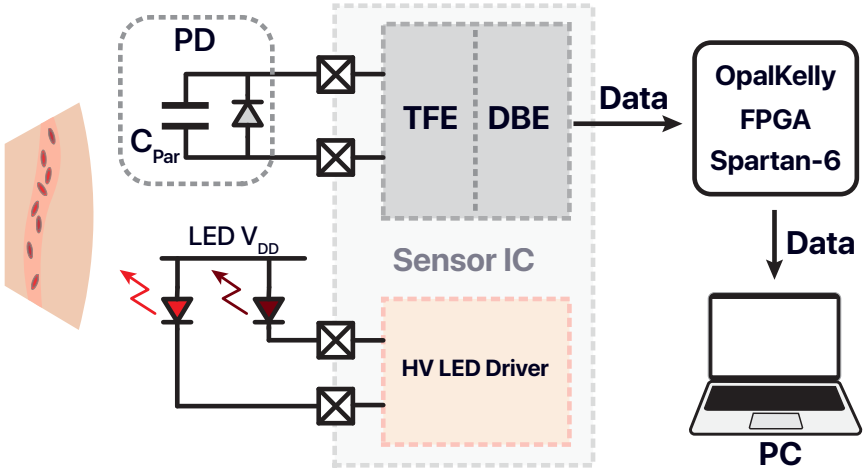
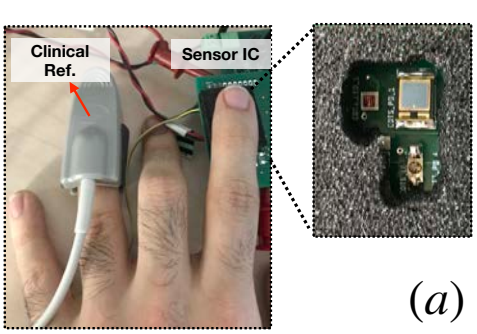
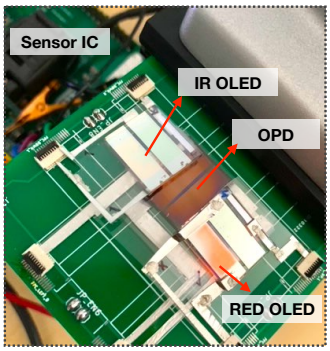


Figure 2.18: *In vivo* recording measurement setup. Data is transferred to a PC via an FPGA.



(a)



(b)

	Cont. Mode	Sparse Mode
LED V_{DD} (V)	5	
Duty Cycle (%)	0.25	
LED Power (μW)	45.1	11.4
SpO_2 Error (%)	0.5	0.7
HR Error (bpm)	0.3	0.4

	Cont. Mode	Sparse Mode
OLED V_{DD} (V)	8	
Duty Cycle (%)	0.5	
LED Power (μW)	727	182
SpO_2 Error (%)	0.35	0.5
HR Error (bpm)	0.3	0.4

Figure 2.19: A summary of the *In vivo* results when using (b) commercial silicon devices and (c) flexible organic devices.

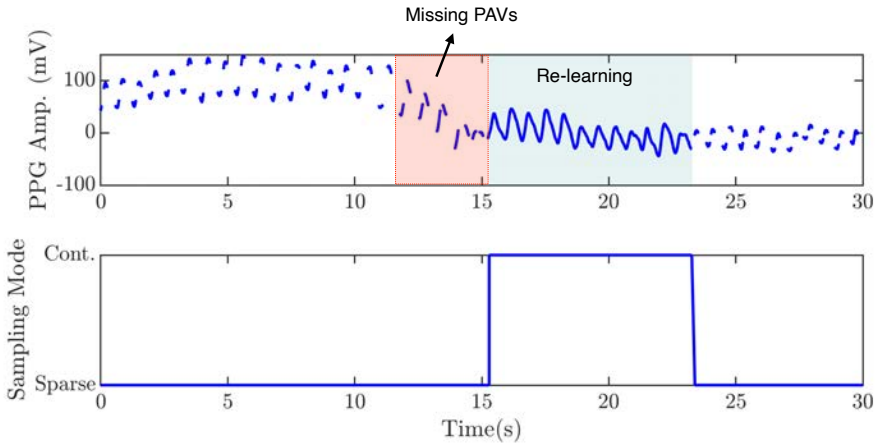


Figure 2.20: Missing PAVs due to motion artifact creating a large change in the sampled PAV values. The backend initially expands W, then reverts to the continuous mode and finally re-gains lock on the PPG.

2.7 Summary & Comparison

A comparison against the most recent prior arts of PPG and SpO_2 sensors is provided in Table 2.7. The LED power is normalized by the number of LEDs in the system since only a single wavelength PPG measurement is required to report HR, while SpO_2 requires two. The TFE power however is not normalized since there could be bias current variations between different phases of operation in prior arts. Compared to state-of-the-art, this work achieves the lowest LED power and one of the lowest total power consumptions while simultaneously delivering the lowest input referred noise. The measured HR and SpO_2 errors are less than 1 bpm and 1% respectively and are lower compared to other works.

The functionality and performance of the proposed sensor IC was characterized using both commercial and flexible organic interface devices. The *in vivo* measurement results confirm the accuracy of the sensor data when operating with a wide range of optical components including organic devices with parasitic capacitances as large as 10 nF. The introduction of reconstruction-free sparse sampling reduces the overall system power by nearly 70% while maintaining the accuracy of the output data.

Table 2.1: Comparison with prior arts of PPG and SpO_2 sensors

Reference	ISSCC 2016 [39]	TBCAS 2017 [54]	TBCAS 2018 [38]	TBCAS 2019 [65]	TBCAS 2019 [10]	ISSCC 2021 [27]	TBCAS 2021 [42]	JSSC 2021 [2]	This work	
									Continuous Mode	Sparse Mode
Technology (nm)	180	180	180	55	180	65	180	65	40 HV	
V_{DD} (V) [LED/Readout]	5/1.5	5/1.2	3.3	2.8/1.2	3.3/1.8	1.8/1	3.3/1.2	-/0.6	5/1.1	
C_{Par} (pF)	1000	155	44	-	–[g]	-	-	-	Si: 40 / OPD: 4800	
Readout Power (μW/Ch.)	87[a]	172	27.4	54	9	24	28	0.532	TFE: 1.22 DBE: 3.34	TFE:0.32 DBE: 3.43
LED Power (μW/LED)	27[a,d]	120[c]	16	102.5	17.5	11.5	305	8.5	22.6	5.7
Total Power (μW/Ch.)	114	292	43.4	156.5	26.5	35.5[a]	333	9.032	27.2	9.45
Sampling Freq. (Hz)	400	128	100	128	25	20	2048	20	100	
Duty Cycle (%)	2	0.4	0.25	-	0.7	0.04	1	1	0.25	
Input Noise (pA/$\sqrt{Hz}$)	-	153	-	6.3	-	-	8.7[a]	20.1	4.8[e]	
SpO_2 Error (%)	1.1[b]	-	-	-	-	-	-	-	0.5[f]	0.7[f]
HR Error (bpm)	-	2[b]	2[b]	-	1.4[f]	1.9[f]	-	-	0.3[f]	0.4[f]

[a]Estimated [b]Max. error [c] 10× Compression Rate [d]Organic LEDs/PDs [e] C_{par} = 40pF (Matching C_{pd}) [f]Mean Abs. error. [g] Low C_{Par} on-chip PD.

Chapter 3

Electrode-Skin Impedance Measurement

3.1 Motivation

Monitoring of brain signals is a gateway to learn about many neurological conditions and diseases. Information about the communication of neurons within the brain is recorded and analyzed to help neuroscientists attain insights on the processes involved in development and progression of different conditions as well as track the prognosis of specific treatments used for any neurological disease. Collection of neural signals attributed to reflexes and motor tasks can also help bypass spinal chord injuries and enable seamless operation of prosthetic limbs. Moreover, many important physiological senses and phenomena such as emotions [37], sleep [51] and drowsiness [83], fatigue [36], seizure [12] etc. have been shown to leave traces in electroencephalograms (EEG) recorded from the brain and thus are detectable. This makes EEG an attractive candidate neural signal that can find immeasurable use in next generation brain-computer interfaces [30, 76].

Recording of EEG is typically done via a network of electrodes contacting the scalp surface as shown in Fig. 3.1. Current clinical standard of acquiring EEG still utilizes similar electrodes and is therefore not convenient for continuous use. Future generations of EEG-based BCI devices however need a recording interface that is compact, light, and unobtrusive to be able to perform monitoring in the background without disrupting the subject's daily activities. In addition, the power consumption of the sensors should be low enough to maintain the sensor battery life. Clearly solutions with scalp electrode arrays are not ideal given their bulky tethered form factor not to mention their unattractive look. Prior arts of EEG recording have been able to perform measurements from the inside of the ear canal [32, 8]. Capturing EEG data from inside the ear has many important advantages compared to scalp recordings. First, the solution is rather discreet without any especially visible protrusions. Second, the recording sensors and electrodes can be embedded into earbuds and earpieces commonly used by millions of users around the globe. These devices can be comfortably

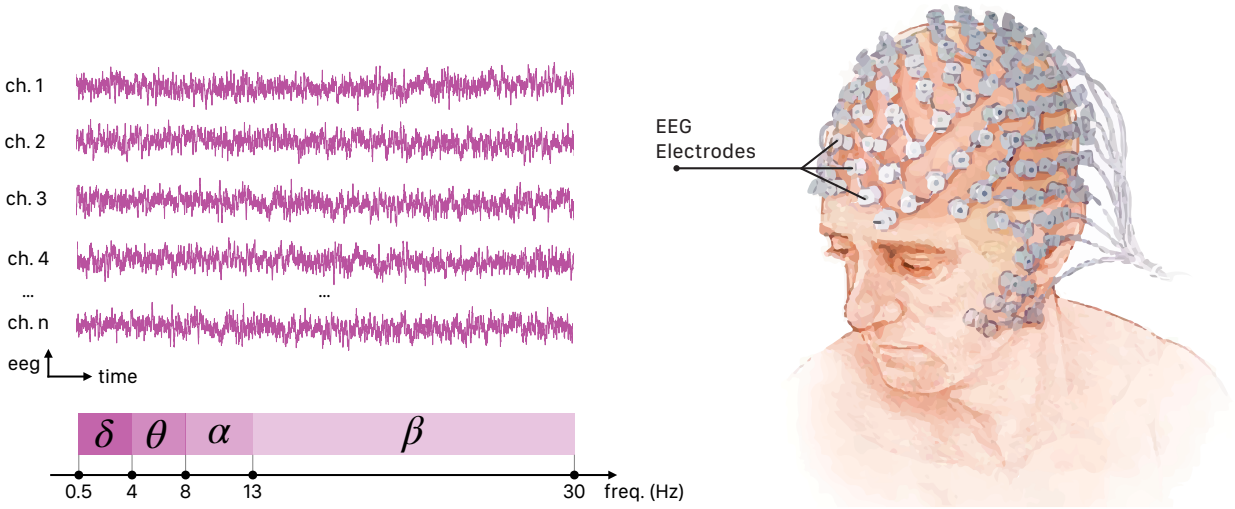


Figure 3.1: EEG signal and its different frequency bands. A network of EEG recording scalp electrodes are shown on the right in a photo adapted from an article on MayoClinic.[18]

worn over long durations with minimal impediment to users' activities. Moreover, the electrical connection can occur with electrodes having a more stable attachment to the skin with multiple contact points around the ear-piece tip. Lastly, despite that the spatial coverage is seemingly limited to the two ears, there are many applications that only require a small number of electrodes and channels which can greatly benefit from a fully wearable ear-EEG recording platform.

To maximize user comfort and increase the longevity of the electrodes, dry electrodes are strongly preferred over wet electrodes. Dry electrodes however typically have much higher contact impedance as their effective surface area is lower than wet electrodes. An increase in the interface impedance has a lot of adverse effects on the recording system and the quality of recordings. For one, the electrode noise is elevated when the interface has higher impedance degrading the SNR at the input. In addition, higher interface impedance raises the inputs' susceptibility to common mode noise and interference such as 60 Hz power line interference, demanding a much higher sensor CMRR. Furthermore, since the contact is not as well established as with the wet electrodes due to numerous air gaps and single point connections, the recording is more prone to motion induced artifact. This is a critical issue for a wearable dry-electrode-based ear-EEG sensor. Fig. 3.2 presents an example of a biopotential, here in-ear EEG, recorded with the presence of motion artifact (MA) due to the subject chewing an apple. As seen, motion can indeed induce large artifacts in-band with the desired signal fully disrupting the measurement. This is even more troublesome given the extremely wide variety of movements and their corresponding artifact with various shapes, amplitudes, frequency bands barring the predictability of the motion and thus achieving a

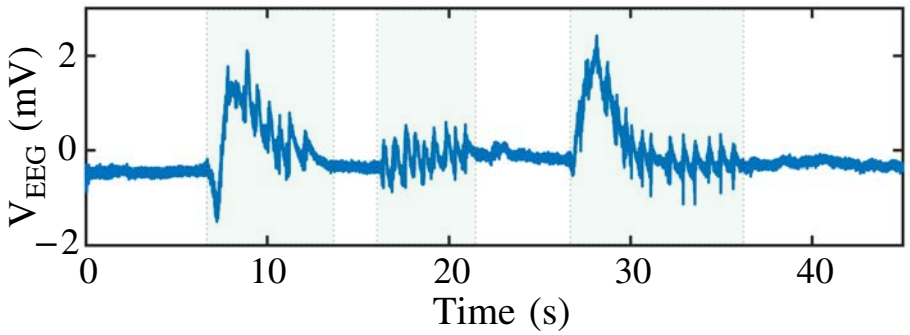


Figure 3.2: Sample recording of Ear-EEG using dry in-ear electrodes where the subject chews an apple in the middle of the recording. Large in-band motion artifact due to the subject chewing is observed completely disrupting the measurement.

robust recording system.

Prior arts of ambulatory biopotential recording have demonstrated various methods to acquire and suppress motion artifact [74, 64, 53]. [53] used dual-electrode setups to detect the biopotential as the common principal component. Post-processing algorithms such as PCA and wavelet transforms have been used to separate out and remove motion related components [64]. Electrode to tissue interface impedance has been used as a proxy to measure a signal that is highly correlated with the motion artifact enabling frontend or backend cancellation of the artifact [74]. Measurement of electrode-skin impedance (ESI) to capture motion artifact is a very attractive approach since it exploits the potential physical correlation of the signals based on the changes on the contact characteristic. Measurement of ESI also provides a means to assess the quality of the contact which can be a useful feature in adaptive control of the recording units. Both analog and digital suppression of MA have been demonstrated by prior arts. However, none of these systems measure the impedance from exactly the same set of electrodes used for biopotential recording. This task is especially challenging as it can disrupt or degrade the quality of the weak biopotential signal when the impedance recording stimuli are introduced. This work presents a front-end IC consisting of 8 simultaneously sampled channels that capture EEG and ESI from the same set of dry electrodes [55]. A shared frontend path is used for both EEG and ESI signals lowering the system power consumption. Measurements are done with a per channel output rate of 1 kS/s large enough to capture the full bandwidth EEG and motion signals. The main focus of this chapter is the impedance acquisition unit of the system and the remainder of this chapter is structured as follows. Section 3.2 goes over the various requirements of the proposed system. Section 3.3 covers the circuit level design and implementation of the system and the benchtop and *in vitro* results from testing the silicon are presented in section 3.4. Section 3.5 provides a comparison of the ESI unit performance in this work against best performing and most relevant prior arts followed by future directions of this work in section 3.6.

3.2 System Overview

System Requirements

Generally, human motions are relatively slow occurring at a sub-1Hz to a few Hz of speed as analyzed and depicted in [46]. However, as shown in recordings from prior arts [9], in many cases motion artifact can appear as large rapid transients in the measured data inducing sudden jumps in the recorded samples. Therefore in order to not lose any correlation between the recorded motion artifact and the measured impedance, the impedance signal is also acquired at the same sample rate as with the biopotential signal. In this work, the target biopotential signal is ear EEG with a bandwidth of $\sim 250\ Hz$. Fig. 3.3(a) shows a simple diagram of the system where the EEG and ESI IC interface the ear canal via electrodes.

The required sensitivity of the impedance sensor greatly depends on the relationship between the changes in impedance and the corresponding motion artifact induced in the biopotential data. [46] provides an analysis where the maximum absolute correlation coefficient $max|c(n)|$ is obtained for the real part, the imaginary part, and the absolute value of the measured impedance for both wet and dry electrodes and over various types of artifacts. As discussed in [9], the highest correlation is seen when the imaginary part of the impedance is used with wet electrodes and for the local types of disturbances such as tapping over, pushing, and stretching under the electrodes. However, reasonable correlation is observed with $max|c(n)|$ greater than 0.6-0.7 when considering the absolute impedance magnitude and with dry electrodes. Assuming perfect correlation, $max|c(n)| = 1$, one can define an artifact transfer ratio (ATR) as the ratio of changes in the relative value of the impedance and biopotential which can then be used to quantify the required resolution on the measured impedance. With first order linear approximations, a wide range of ATR is observed from $\sim 0.01\ mV/\%$ to $\sim 0.1\ mV/\%$ looking at data recorded by our setups and also from prior arts [9, 35, 46]. Considering the worst case of ATR of $\sim 0.1\ mV/\%$, the required accuracy on relative changes in impedance magnitude would be about 1 % to achieve less than $100\mu V$ of error in the biopotential. Achieving sub 1% of impedance magnitude error requires a full bandwidth impedance signal to noise ratio of at least $\sim$ 40 dB. If the artifact bandwidth is $10\times$ smaller, the same $< 1\%$ accuracy can be achieved with only $\sim$ 20 dB of SNR. This sets a target specification for the ESI measuring unit to determine the amplitude of stimulation.

Another important aspect is the range of impedances that is expected for ambulatory EEG and ESI recording. Extensive measurements performed by our colleagues have shown an estimated range of 10 kΩ to 1 MΩ for the electrodes used in our system [29]. Fig. 3.3(b) shows a plot of ESI magnitude over frequency taken from [29]. Achieving the desired SNR when the impedance is at the higher end of the above range is substantially easier than when the electrodes have a solid low-impedance contact. However, the system is targeted to maintain the accuracy for the entire range of ESI. Considering a spot noise floor of $\sim 100\ nV/\sqrt{Hz}$ at the ESI band, achieving 40 dB of SNR for a 10 kΩ ESI requires an impedance signal as large as $\sim 160\ \mu V$ over the complete 250 Hz EEG bandwidth. Such a signal requires a stimulation current of around 16 nA. As a result, a stimulation current range of 5 - 40 nA is employed

in the design. Simultaneous recording of ESI and biopotential necessitates that the ESI recording does not incur significant noise or interference in the biopotential frequency band. This poses a significant challenge in design of the stimulation electronics given that ESI is considerably larger in lower frequency bands than in bands where the biopotential signal resides. Considering a maximum ESI of 1 MΩ, achieving less than $\sim 100\ nV/\sqrt{Hz}$ of voltage noise density at the biopotential band demands a current noise density of $< 100\ fA/\sqrt{Hz}$. Therefore, a maximum current noise density of 55 $fA/\sqrt{Hz}$ in the stimulation current is targeted to not increase the readout noise floor by more than 15 %. Section 3.3 discusses how the current sources are designed and implemented to deliver the target noise performance. Lastly, the system intends to simultaneously record the biopotential signal from a set of 4-8 electrodes. This simultaneous recording of ESI from multiple channels requires a multiplexing scheme that guarantees minimal interchannel leakage. The leakage constraint is even more stringent when a single reference electrode is used for all channels. In this project, a frequency division multiplexing scheme is selected to achieve the desired performance.

Sensor Architecture

Measurement of impedance is typically done by using a stimulation signal, either current or voltage, that is applied to the target impedance and the associated response, voltage or current, recorded by a readout frontend. Then post processing of the acquired response using the knowledge of the stimulation waveform enables extraction of impedance magnitude and phase. Both types of stimulation signal are covered in this work and the pros and cons of each method is discussed in section 3.3.

In order to record the magnitude and phase of impedances with reactive components,

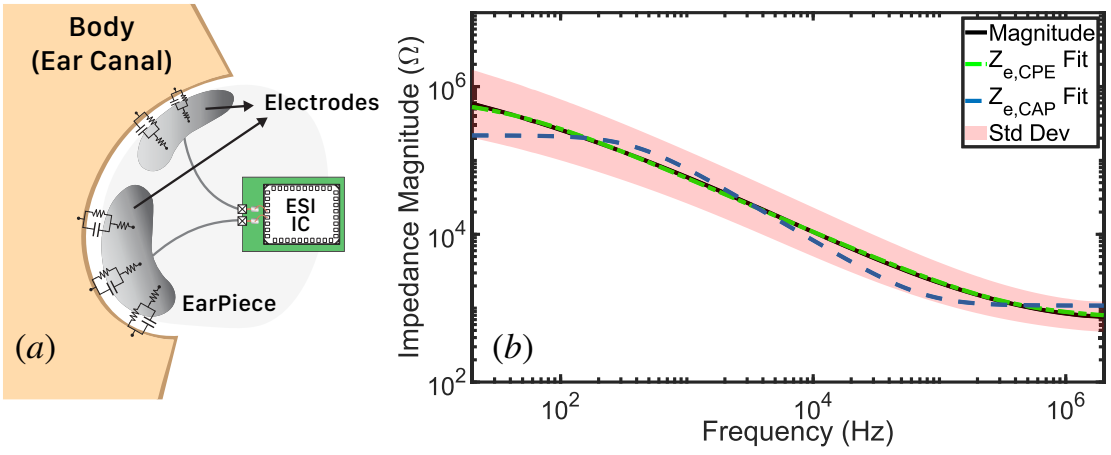


Figure 3.3: (a) The ESI and EarEEG recording system diagram showing two electrodes and the readout IC. (b) The ESI of dry in-ear electrodes from [29]

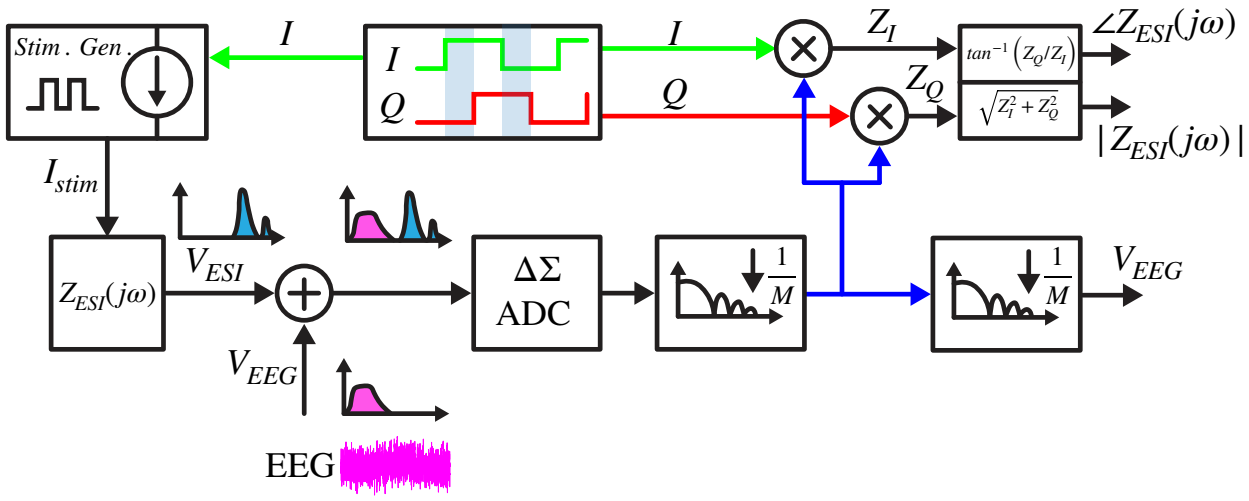


Figure 3.4: Signal Flow diagram of the sensor readout. The stimulation block creates a differential AC current that terminates over the ESI inducing a voltage signal at the stimulation frequency band. This signal is then summed with the desired biopotential signal, here the EEG, and is then acquired via a shared frontend ADC. In the backend, the decimated ADC output is multiplied by in-phase and quadrature components of the stimulation signal allowing for the impedance magnitude $|Z_{ES}(j\omega)|$ and phase $\angle Z_{ES}(j\omega)$ to be extracted.

capacitors or inductors, measurements need to take place at frequencies other than DC and changes in amplitude and phase of the response with respect to the stimulation waveform are used to retrieve ESI information. In-phase and Quadrature (I/Q) demodulation is a technique, dating back to the early days of electronic communication and used by prior arts [73], that utilizes orthogonal demodulation waveforms with 90° of phase shift to extract the magnitude and phase changes of the recorded response. In this technique, the recorded response signal is mixed by the I & Q components of the stimulation waveform, creating I & Q impedance signals Z_I and Z_Q. Then, the overall magnitude and phase of the test impedance can be found as:

$$|Z_{test}(t)| = \sqrt{Z_I(t)^2 + Z_Q(t)^2} \tag{3.1}$$

$$\angle Z_{test}(t) = tan^{-1}\left(\frac{Z_Q(t)}{Z_I(t)}\right) \tag{3.2}$$

The principle of operation of I/Q demodulation is later discussed in appendix B. The discussion is continued by only considering current stimulation; however, all of the discussed principles similarly apply to voltage stimulation as well.

Fig. 3.4 demonstrates the signal flow diagram of the IC readout frontend. The stimulation block creates a differential AC current that is terminated over the ESI inducing a voltage

signal at the stimulation frequency band. This signal is then summed with the desired biopotential signal, here the EEG, and is then acquired via a shared frontend ADC. In the digital backend, the ADC output is multiplied by in-phase and quadrature components of the stimulation waveform extracting the impedance magnitude $|Z_{ESI}|$ and phase $\angle Z_{ESI}$. In this work, a shared readout frontend is used for both impedance and biopotential acquisition. This is because the two signals reside in different frequency bands that can be separated and filtered in the digital backend. Moreover, re-using the same frontend path and sub-blocks saves power while not compromising the accuracy of the recorded data. In addition, connecting parallel frontends to the same electrodes would reduce the impedance seen by the electrodes by at least 2× degrading the recorded biopotential signal quality as well as common mode interference rejection. Using shared frontend path however necessitates that the full-scale range of the ADC is set by the maximum of the two signals and the noise of the ADC is set by the smallest one. Ear EEG signals are typically weak with amplitudes only as large as 100s of μV. The impedance signal however can be bigger depending on the ESI and the stimulation current. Since the expected ESI of dry electrodes can be as large as a few $M\Omega$, the ADC full-scale range is set by the peak impedance signals that can be as large as 10-40 mV.

Prior arts of bio-impedance measurement have used square wave drive and demodulation waveforms to acquire the impedance. Use of square wave considerably simplifies both the implementation of the driver as well as the digital demodulation hardware. Fig. 3.5 shows the analog and digital hardware required for square wave drive and demodulation. The drive can simply be implemented using two constant current sources, I_D, and a butterfly switch toggling at the ESI frequency, f_Z, Fig. 3.5 (a). The output current waveform therefore is an up-modulated square wave current with a peak amplitude of I_D. The digital demodulation, shown in Fig. 3.5(b), can also be viewed as a simple sign flip of the impedance data in phase with the demodulation square wave. This technique significantly reduces the area and energy costs of the impedance measurement hardware and is therefore employed in this work. Using square wave however brings about an issue that can create non-negligible errors in the acquired impedance magnitude and phase. The square wave signal contains components at all odd harmonics of the main harmonic frequency, f_Z. This means that the Z signal also has components at all odd harmonics of f_Z each scaled and phase-shifted by the magnitude and phase of the ESI at that harmonic. All of these higher order harmonics when demodulated using the square wave are down-converted to the base-band, DC to 250 Hz. Consequently, the resulting magnitude and phase outputs are impacted by the ESI profile at higher frequencies. Each harmonic's error and the cumulative error in the absolute $|Z|$ is plotted in Fig. 3.6 for the worst case purely resistive impedances that exhibit no attenuation at higher frequencies. Note that the objective of this project is to track the changes in impedance as a proxy for measuring motion artifact. Therefore, the absolute value of the impedance is not really as important as the relative changes in the impedance. As a result, despite being as large as 10-20%, this error can be neglected in sensor design. One can note that more than half of this error is due to the existence of the 3^{rd} harmonic in both the drive and demodulation signals. Therefore, eliminating this harmonic from either one of the two signals can cut the absolute

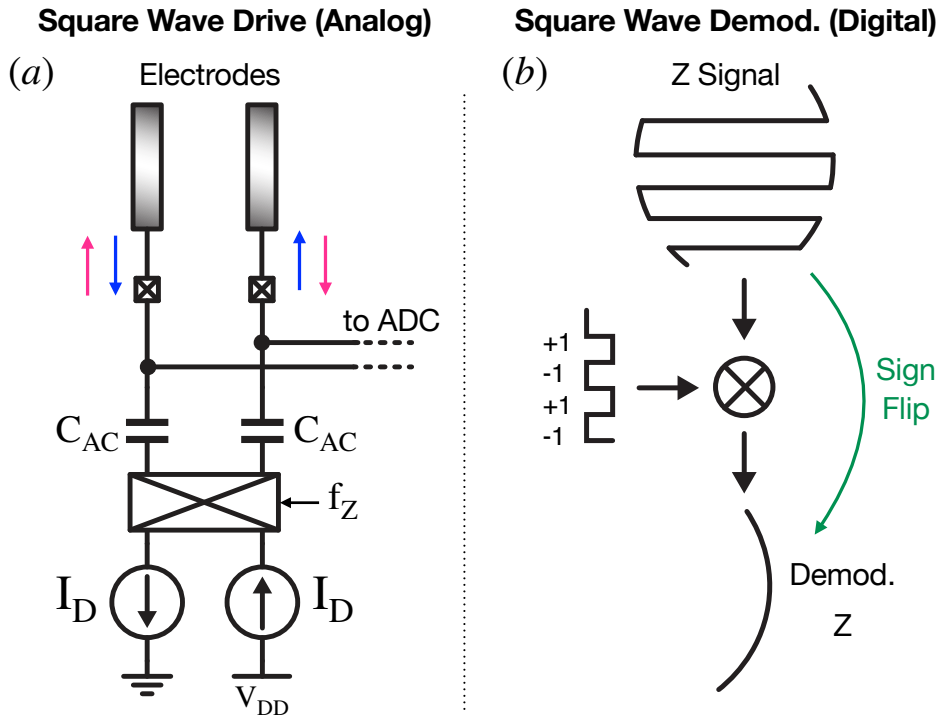


Figure 3.5: Simple square wave drive and demodulation hardware. (a) The drive is implemented using two current sources and a butterfly switch toggling at f_Z. (b) The digital demodulation is as simple as a sign flip in phase with the demodulation signal.

value error by more than half. We thus employ the 3^{rd}-harmonic-free drive which uses the waveform shown in Fig. 3.7 to create the stimulation signal. This balanced waveform only uses three levels of current already existing in the designed hardware i.e. $+I_D$, $-I_D$, and 0. The timing of this signal however mandates that the master clock frequency is divisible by 12 to allow for short phases that only last $\pi/6$ of phase shift. Looking at Fig. 3.7(b), we can see that this technique gets rid of all components that are at an integer multiple of the 3^{rd} harmonic of f_Z.

As a better alternative to square wave or 3^{rd}-harmonic-free signals, we can also employ sine waves at either the driver module or in the demodulation backend. Section 3.3 discusses the implementation of a 4-bit sine wave drive in voltage domain that no longer suffers from the issue of harmonics even with square wave demodulation. We also implement the sine wave demodulation backend that uses digital 8-bit multipliers and an on-chip look-up table (LUT) containing the 8-bit sine wave values. This way, the error in absolute impedance values due to harmonics is completely eliminated for all types of drive signals.

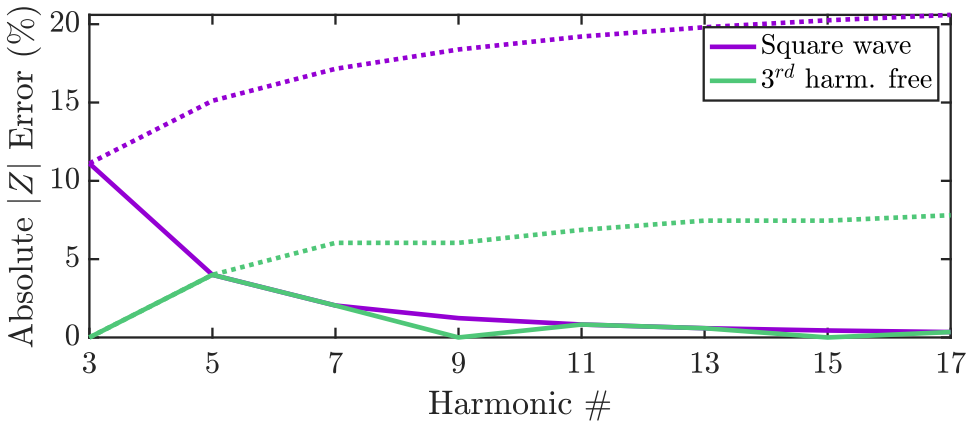


Figure 3.6: Errors induced in the absolute value of the impedance due to higher order harmonic sampling. 3^{rd}-harmonic-free drive reduces this error by more than 50%.

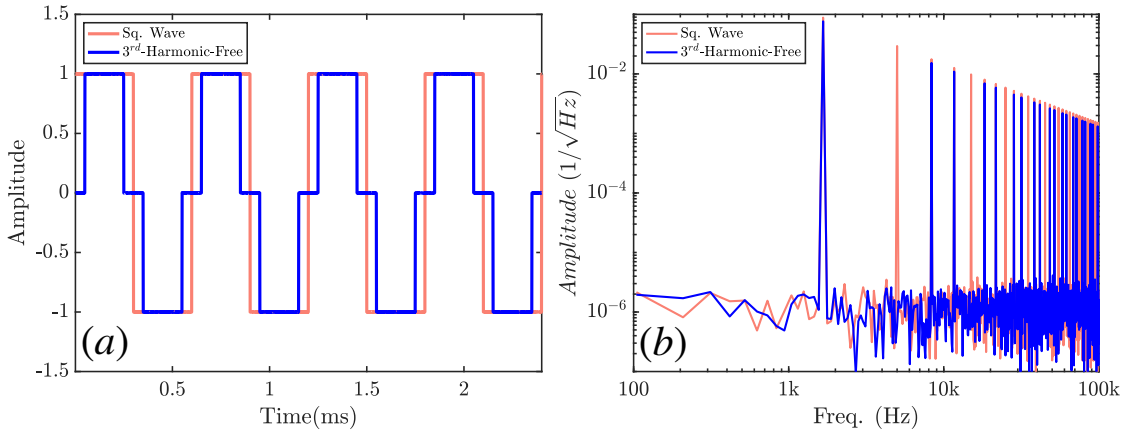


Figure 3.7: 3^{rd} Harmonic free drive vs. square wave drive. (a) The time domain waveforms are shown for $f_Z = 1.6$ kHz. (b) The spectrums associated with "a".

3.3 ESI Recording IC

The ear-EEG IC was designed to simultaneously acquire the low frequency EEG signal as well as the ESI at higher frequency bands. A second order continuous time delta-sigma ADC frontend was used in this work and the details are covered in [55]. The focus of this chapter is only on the ESI recording unit and the following sections cover the stimulation and demodulation hardware of the ESI measurement.

Stimulation Unit

In section 3.2, the two different types of stimulus signals that enable impedance acquisition were discussed and the target sets of specifications for frequency, amplitude, noise, and impedance were reviewed. The following subsections provide details on the how these sub-blocks are designed and implemented to achieve the desired specs.

Active Stimulation

The first type of stimulation requires low noise current sources that can apply a differential current at the input nodes. The target ranges of current are about 5-40 nA while maintaining less than 55 $fA/rtHz$ current noise density. Unlike prior arts that use current mirrors, we employ regulated resistively degenerated current source topologies that offer superior noise performance while achieving > 1 $G\Omega$ output impedance. Fig. 3.8 shows the schematic of the active current driver. The sink and source current sources' output currents are up-modulated using the butterfly switches. Since the input electrodes are approximately at ground potential (0 V), the current sources need to be AC coupled to maintain the correct bias point. Prior art [73] uses large off-chip capacitors for AC coupling that prevent full integration and miniaturization. In this work to remove all off-chip components, on-chip AC coupling capacitors (C_{AC}) are used that provide the isolation at the cost of limiting the peak drive current. The period of the impedance drive ($T_Z = 1/f_Z$) is closely tied to the size of the AC coupling capacitor as well as the drive current amplitude. This is because during every half period of T_Z, the voltages at the drains of MOS devices observe linear ramps towards the rail voltages reducing the V_{DS} of the devices. To avoid getting the devices into triode region region, the differential swing is restricted to about a maximum of $V_{Swing_{max}} = 600$ mV. Therefore, the drive frequency's lower bound is set by Eq. 3.3.

$$f_{Z_{min}} = \frac{I_{stim}}{C_{AC} \cdot V_{Swing_{max}}} \tag{3.3}$$

For the expected range of ESI and a minimum f_Z that is outside the EEG bandwidth ($f_Z > 250$ Hz), a total of 100 pF on-chip C_{AC} per channel is sufficient.

The large degeneration resistor greatly attenuates the noise of the MOS devices, the regulating amplifier, as well as any reference noise originating from the voltage DACs. These resistors (R_P & R_N) form $\sim 98\%$ of the output current noise density and are therefore set to 8.6 $M\Omega$ nominally to achieve < 45 $fA/rtHz$ current noise. The low frequency flicker noise of the amplifiers or reference however can potentially degrade the noise performance. Hence, the amplifiers are internally chopped to up-modulate the flicker noise. Using $f_{chop} = 8 - 16$ kHz, the flicker noise and offset are up-modulated and then fall in the notches of the ADC decimation filter's response and are thus fully removed. The N & P reference voltages are also supplied via resistive DACs (R-DACs) to avoid reference flicker. The value of the reference voltages are 4-bit tunable to adjust the output current level and provide ways for calibration. The sink and source current sources need to provide matched output currents

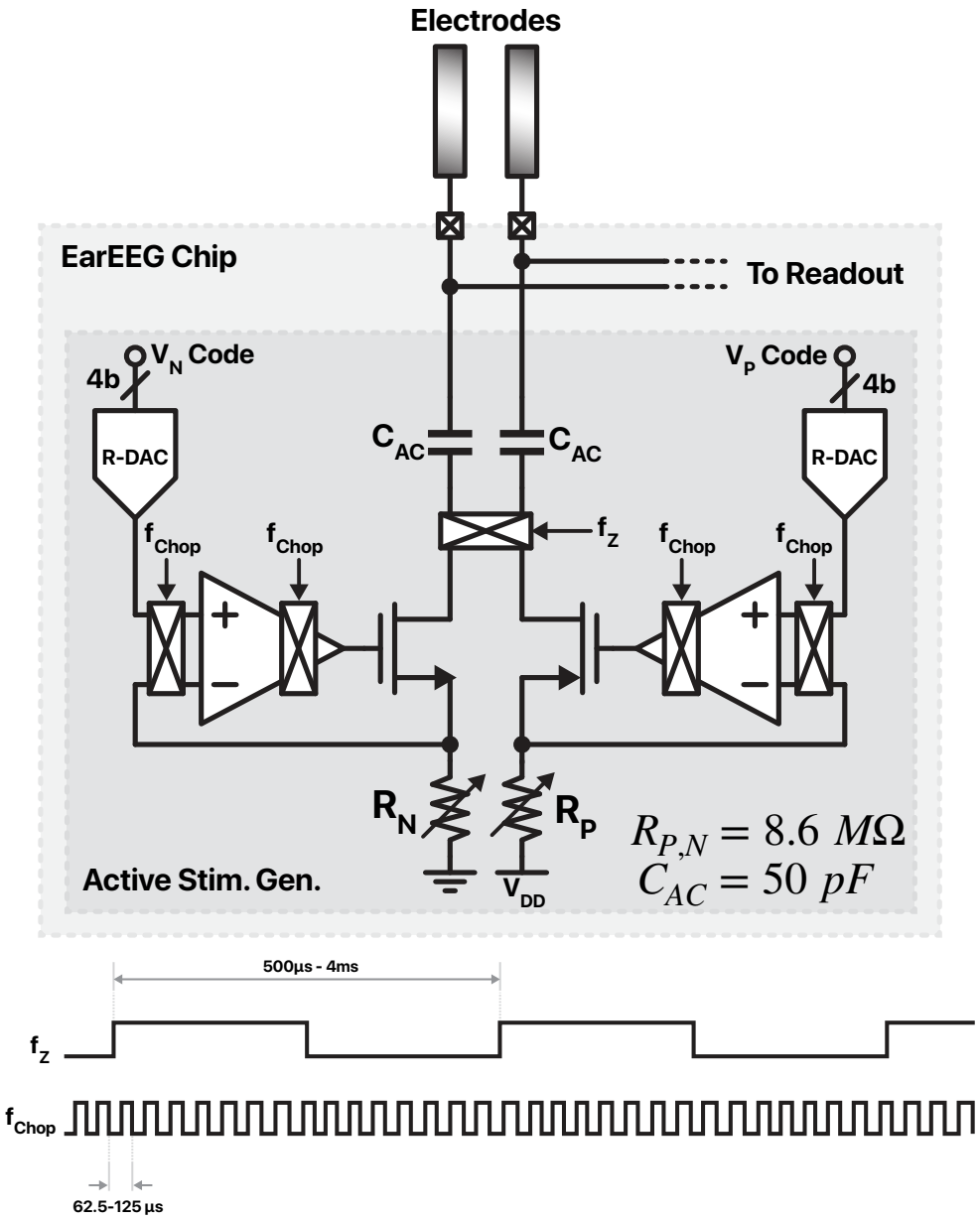


Figure 3.8: The schematic and timing diagram of the active stimulation unit. The timing signals are generated on-chip using the reference master clock.

that not only deliver a charge-balanced stimulation, but also maintain a stable common mode voltage at the current source outputs avoiding biasing issues. To achieve the desired matching, resistors R_P and R_N are 5-bit adjustable within 10% of their value. A one-time calibration of these resistors' codes allows for sufficient matching of the two currents.

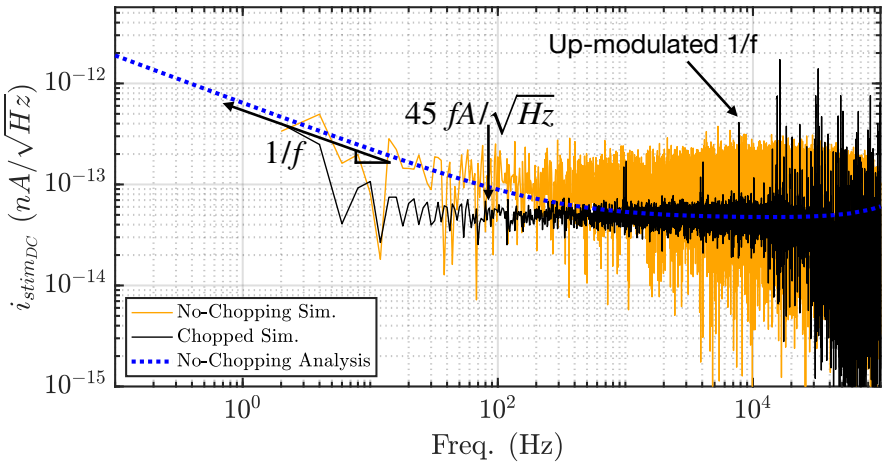


Figure 3.9: The spectrums of the stimulation current sources at 10 nA of drive current. Blue and orange curves shows the analytical and simulated spectra of the drive current without chopping where flicker noise dominates the noise floor over EEG bandwidth. The black curve represents the drive current spectrum with chopping at 8 kHz that results in a significantly reduced current noise density over the EEG band.

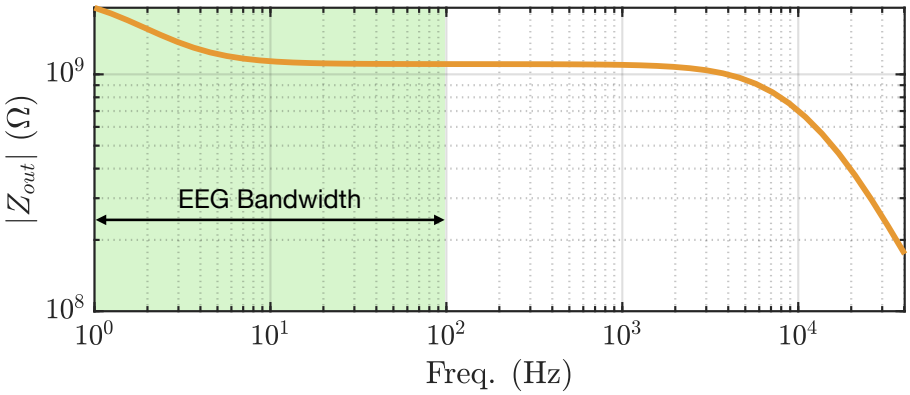


Figure 3.10: Output Impedance of the active stimulation unit. The unit maintains a $> 1\ G\Omega$ output impedance across the entire EEG bandwidth and even up to 3 kHz.

To obtain $> 1\ G\Omega$ output impedance, high-gain OTAs are used as boosting amplifiers that enhance the output impedance of the degenerated MOS devices. Toggling of f_Z switches induces large voltage transients across the P & N current outputs. The bandwidth of the OTAs thus is set high enough to provide fast responses to the transients maintaining the waveform accuracy. The MOS devices and the transistors inside the butterfly switches

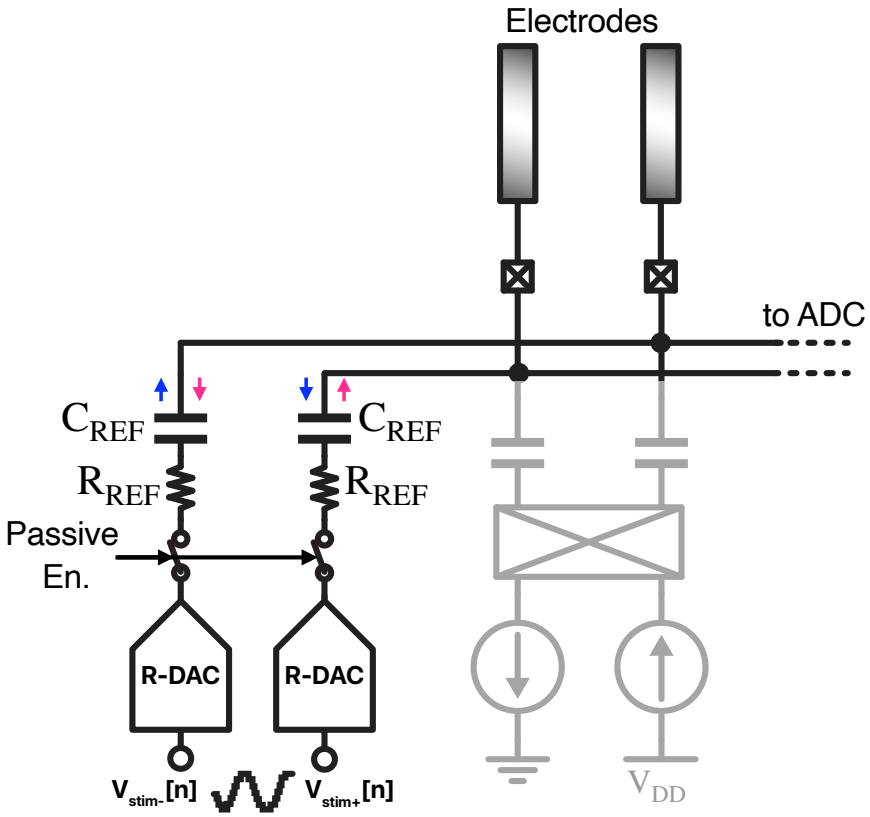


Figure 3.11: Passive stimulation unit block diagram. Enable switches can fully disengage this unit from the inputs, providing isolation as well as increasing the input impedance when using active mode.

are sized small enough to prevent excessive drain and source leakage and drain to bulk parasitic transconductances diminishing the output impedance. Note that the resistance of these switches is not important as they are in series with the large current sources' output impedance. Fig. 3.9 plots the spectrum of the current source outputting a 10 nA DC current. Without chopping, the current noise density is high at frequencies below 250 Hz due to flicker noise, degrading the noise performance of the readout. Chopping at 8 kHz lowers this noise floor to $\sim$ 45 $fA/rtHz$. The simulated output impedance of the active stimulation unit is depicted in Fig. 3.10. The designed module maintains a greater than 1 $G\Omega$ output impedance up to $\sim$ 3 kHz. The result shown is the worst impedance over a Monte-Carlo simulation with 200 runs with both global and local variations.

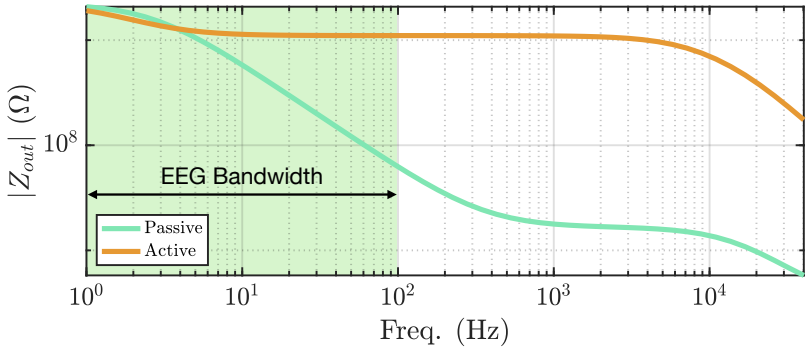


Figure 3.12: Comparison of output impedance between active and passive stimulation units.

Passive Stimulation

Fig. 3.11 shows the block diagram of the passive stimulation unit. The unit consists of two differentially driven 4-bit resistive V-DACs that are run by digital codes coming from the digital backend creating a stimulation signal at f_Z. The backend uses the same LUT values from the sine-wave demodulation to create the DAC codes. The resulting response at the input is induced based on voltage division from the DAC outputs and between the reference impedance impedancez (Z_{REF}) and the ESI. With a one-time calibration of values of Z_{REF} and DAC outputs at any f_Z, the ESI can be extracted using the response signal and a similar demodulation backend. Use of voltage DACs allows for a coarse sinusoidal drive waveform eliminating the issue of harmonics even when using a simple square wave demodulation. In addition, since the reference impedance can be very large at EEG frequency band, the reference and DAC noise is greatly attenuated at the input preventing any EEG SNR degradation. Furthermore, the entire power consumption of the unit occurs in the V-DACs which can be implemented with sub-μW total power. The only disadvantage of the passive drive is that its output impedance is limited by the impedance of the passive elements since there is no active impedance boosting. Fig. 3.12 depicts the output impedance of the passive unit and compares it against the active one.

Demodulation Back-end

As explained earlier, the on-chip digital backend is capable of performing two different types of impedance I/Q demodulation. The first is the simple square wave demodulation in which the decimated ADC output is mixed with the in-phase and quadrature impedance clocks using sign-flip operation. This uses minimal hardware and digital power on the chip and is by far the easiest demodulation method. To calibrate extra delay in the forward path, the phase of I/Q clocks in the demodulation backend can be shifted by 15 integer multiples of 1/16 of the impedance clock period. This allows for having an ideal imaginary impedance

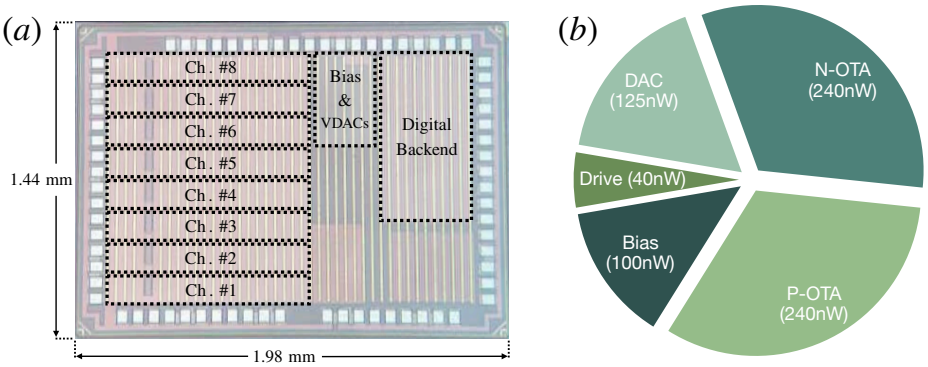


Figure 3.13: Chip micrograph of EarEEG IC and the power breakdown of the stimulation unit.

signal at the output with zero mean and therefore no extra phase calibration is necessary. The second type of demodulation is done by using an on-chip 128 slot LUT containing data for a 128 point per quarter period sine-wave. Therefore, 8-bit sine-wave demodulation can be done via on-chip digital multipliers. To create both in-phase and quadrature components, the starting pointer for the quadrature component begins 1-quarter of the wave behind the in-phase component. Similar to the square-wave demodulation, the starting pointers for both I/Q components can be shifted along the LUT to achieve zero net-phase between the ADC output data and the reference clocks cancelling the delay of the front-end forward path. Unlike the square wave demodulation, sine-wave demod. uses much more digital area and power as it requires the LUT array of registers, two 8-bit digital multipliers as well as the control logic. However, the overall power consumption of the demod. backend still remains well within the IC power budget.

3.4 Measurement results

Chip Micrograph & Power Breakdown

The Ear EEG IC was fabricated in a TSMC 28 nm technology. The chip consisting of eight channels occupied an area of 1.98×1.44 mm^2. Fig. 3.13 shows the IC micrograph as well as the stimulation unit power breakdown. The entire unit consumes a total of ~ 750 nW of power when generating a differential current of 40 nA. Fig. 3.14 shows the layout of the per channel stimulation unit. The unit takes a drawn silicon area of 470 $\mu m \times$ 150 μm mostly dominated by the area of the passive elements C_{AC} and $R_{N,P}$.

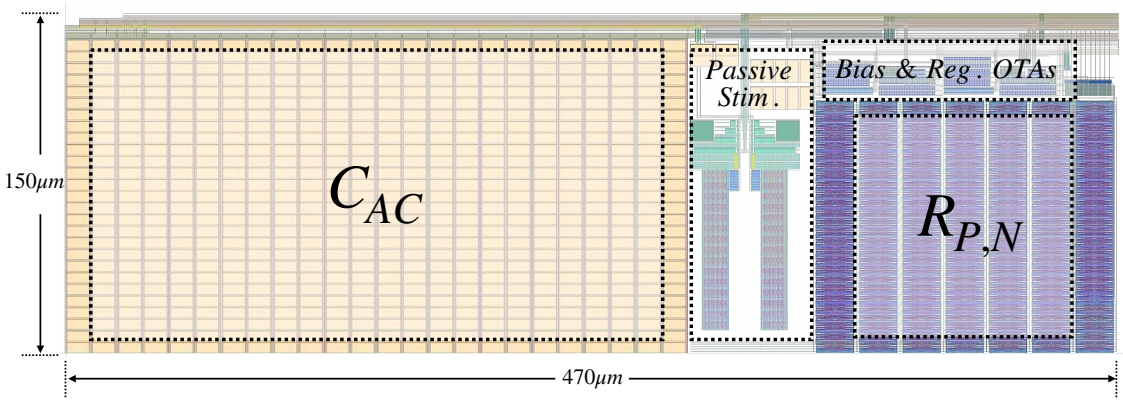


Figure 3.14: The layout of the stimulation block. The area is dominated by the area of the passive elements, C_{AC} and $R_{N,P}$.

Benchtop Measurements

Enabling the stimulation unit, we first recorded the current waveforms using 100 kΩ resistive test terminations. Fig. 3.15 shows oscilloscope captures of square and 3^{rd} harmonic free waveforms at $f_z = 2$ kHz. The time domain captures are shown in sub-figures (a) and (c) while the corresponding spectrums are presented in sub-figures (b) and (d). As observed, the amplitude of the third harmonic is attenuated by more than 60 dB confirming the efficacy of the employed technique. The ESI recording is tested in bench-top settings using explicit on-board resistances. The value of the resistance is swept over a range of $\sim 1\ k\Omega - 2\ M\Omega$ and the acquired resistance value is recorded. Fig. 3.16 (a) presents the plot of acquired resistance versus the test resistance. Two point calibration is performed on the recorded values to remove the effect of offset and gain error. Less than $\sim 2\%$ of error in absolute value of the resistance is measured with test resistances as large as 2 $M\Omega$. The error is reduced to less than $\sim 0.3\%$ for the expected range of ESI highlighted in green shade. The measured results at the higher end are limited by on-board parasitic capacitance preventing the accurate tracking of recorded impedance and test resistance value. Fig. 3.16 (b) plots the associated μ/σ of the same measurement featuring a maximum SNR of $\sim$ 68 dB. A minimum SNR of 40 dB is maintained for the entire expected range of ESI guaranteeing a less than 1% magnitude error.

The voltage readout provides an input referred voltage noise density of $\sim 120\ nV/rtHz$ at around the stimulation bands while the stimulation unit is active. This voltage noise density can be converted to an effective impedance noise density if scaled by the amplitude of the stimulation current. Fig. 3.17 plots the impedance noise spectrum of the ESI readout when a stimulation current of 17 nA is used. The measured noise floor is approximately $\sim 7.2\ \Omega/rtHz$. This results in a total RMS impedance noise of 72 Ω over the 100 Hz EEG bandwidth, more than 40 dB lower than the smallest expected ESI of 10 $k\Omega$. The impedance

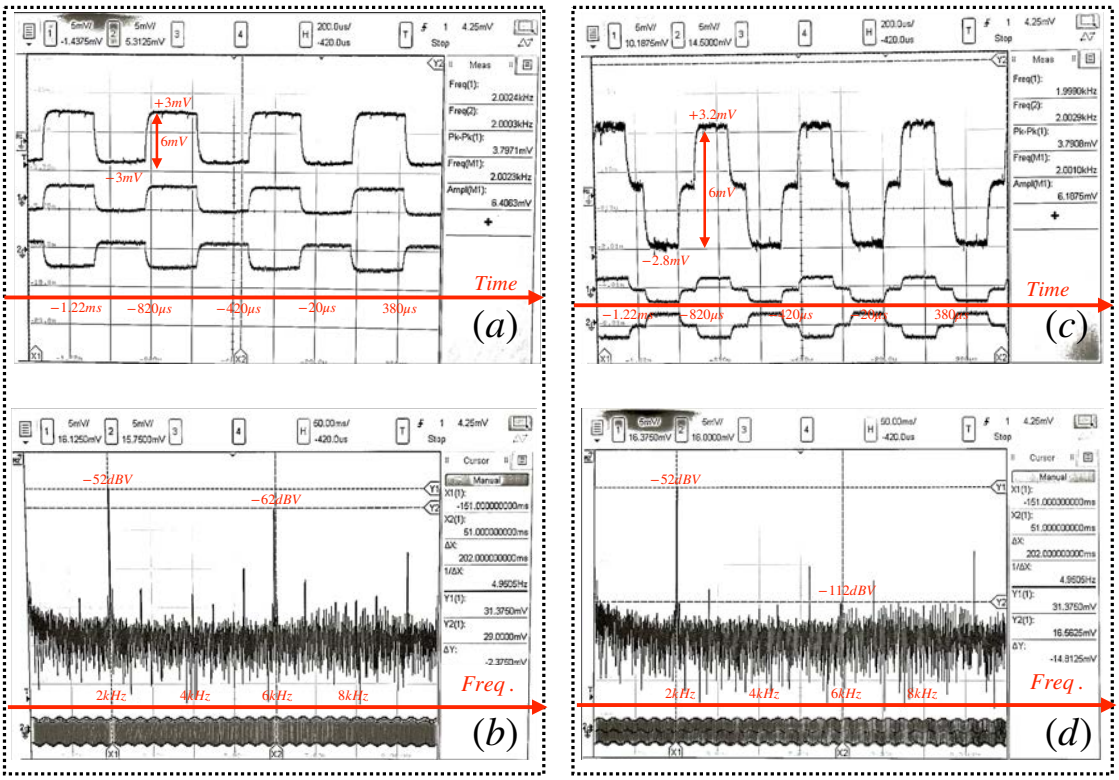


Figure 3.15: Oscilloscope captures of stimulation waveforms over 100 $k\Omega$ test resistances. (a) shows the time domain square wave stimulation waveform at 2 kHz. (b) shows the spectrum of "a" with a 3^{rd} harmonic amplitude $\sim$ 10 dB below the main harmonic. (c) presents the time domain 3^{rd} harmonic free waveform at 2 kHz. (d) exhibits the spectrum of "c" with the 3^{rd} harmonic amplitude attenuated by $>$ 60 dB.

range can be further extended by 8$\times$ via adjusting the amplitude of the stimulation current from 5 to 40 nA. Another experiment is performed using three different electrode models representing impedances measured for electrodes with mean, -1σ, and $+1\sigma$ of impedance magnitude. Fig. 3.18 depicts the results of these measurements. Each model's impedance is measured at four different frequencies, 500 Hz, 780 Hz, 985 Hz, and 1,950 Hz. The dotted lines represent the same impedance measured by the LCR meter (Keysight E4980A-001). As seen, the data from the ESI chip reasonably tracks the accurate impedances over frequency.

3.5 Comparison with Prior Arts

The ESI IC performance is compared against some of the most recent and most relevant prior arts. Table 3.5 shows the comparison chart. Papers [75, 81] aim to acquire extremely

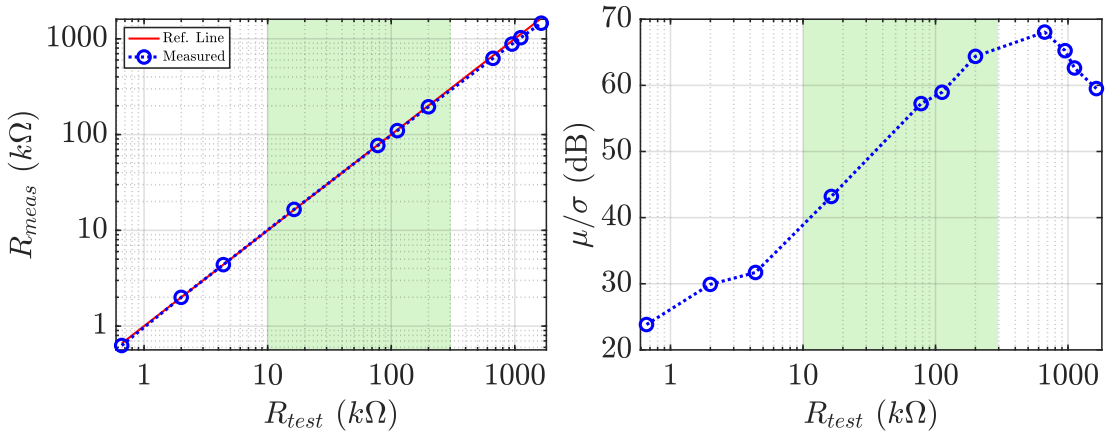


Figure 3.16: Resistive impedance measurement results for a range of $\sim$ 1 $k\Omega$ – 2 $M\Omega$ of differential test resistance. (a) Two point calibration is performed on the values and the fit-line is plotted in solid red. (b) The μ/σ of the measurement in dB signifying a maximum $\sim$68 dB of SNR.

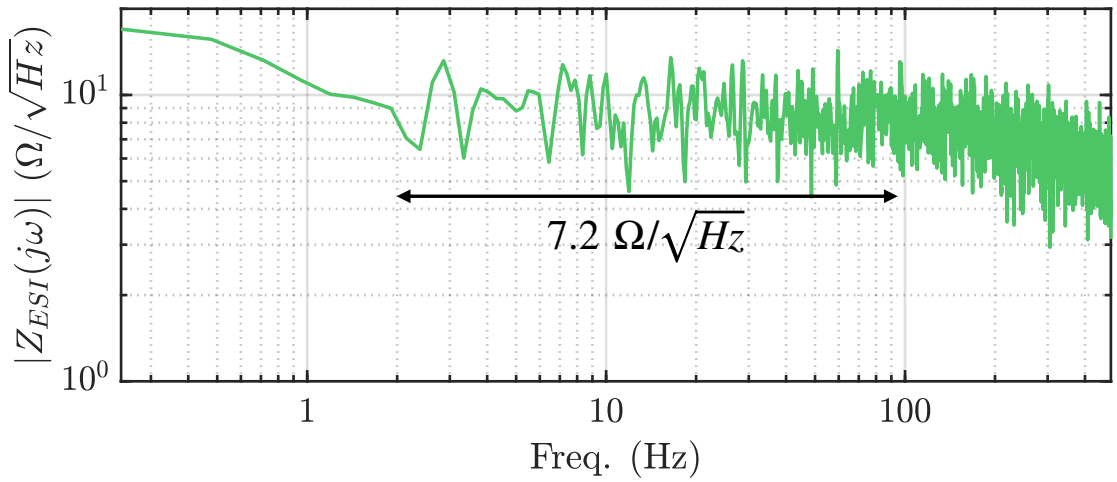
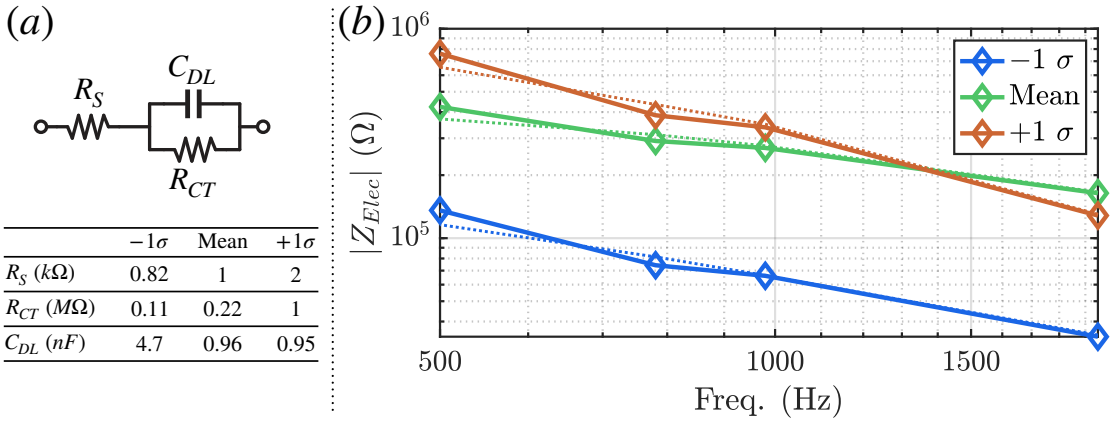


Figure 3.17: Effective impedance noise spectrum of the ESI readout at 17 nA of stimulation amplitude.

small variations in bio-impedance and have impedance noise floors around a few $m\Omega/rtHz$ which is much smaller than the impedance noise floor in this work. However, the overall achieved dynamic range is still lower than the one in this work. Compared to prior art [73] with similar ranges of ESI, this work achieves 10× lower Z-induced voltage noise as well as 20× lower impedance unit power consumption. Furthermore, the measured impedance



	-1σ	Mean	$+1\sigma$
R_S ($k\Omega$)	0.82	1	2
R_{CT} ($M\Omega$)	0.11	0.22	1
C_{DL} (nF)	4.7	0.96	0.95

Figure 3.18: (a) The electrode model consisting of series resistance (R_S), double layer capacitance (C_{DL}) and the parallel resistance (R_{CT}). The values of each element in every model is presented in the table. These values are measured with a benchtop LCR meter. (b) The acquired impedance (solid line) of the electrode model vs. the LCR meter reported impedances (dashed line).

bandwidth is also improved by a factor of 4× compared to [73].

3.6 Future Work

In this work, a low power multi-channel Ear-EEG and ESI recording IC was presented that simultaneously captures the the EEG and ESI signals from the same set of dry electrodes. Bench-top electrical testing and *in vivo* experiments confirmed the functionality and performance of the designed IC. Future generations of this work can however improve on a couple of aspects. Currently, the motion artifact detection and cancellation occurs off-chip via post-processing of the recorded data. MATLAB models are trained that use the ESI data as a proxy to eliminate the motion artifact from the recorded EEG signal. In future, a compact digital core can be implemented on-chip that performs on-line real-time motion artifact cancellation outputting clean EEG data. Off-line and on-line training can be done on the MA cancellation backend to maintain accuracy. Moreover, the impedance data which represents the motion artifact can by itself be used for many classification tasks. An on-chip classifer can be incorporated that detects and classifies various types of motion using ESI data from the all channels. This task can also be accomplished on-line and in real-time.

Table 3.1: Comparison with prior arts of ESI & BioZ recording ICs

Reference	ISSCC 2012 [73]	JSSC 2015 [75]	TBioCAS 2018 [81]	This Work
Technology (nm)	180	180	180	28
V_{DD} (V)	1.2	1.2	1.2	1
BW (Hz)	250	20,000	1000	1000
ESI/ BioZ Power (μW/Ch.)	15.6	58	285	0.75
Z Induced Voltage Noise ($\mu V/\sqrt{Hz}$)	0.54	1.1	0.6	0.045
Current Range (μA)	0.05 - 2 (2-bit)	27 - 117 (2-bit)	10 - 200	0.005 - 0.04 (4-bit)
Motion Artifact Cancellation	Analog	Digital (on-chip)	Digital	Digital (off-chip)

Chapter 4

Low Noise Current Sensing

4.1 Introduction

Recording of very small electrical currents is a frequently required capability of biosensors operating in many different biological settings. This chapter reviews some of the applications that employ high sensitivity current sensors and their typical requirements. Prior arts of these applications are reviewed briefly and then the focus of this work is discussed. A low noise current sensor is then detailed in following sections.

Patch Clamp Recording

With the introduction of patch-clamps in neural recording setups, Fig. 4.1(a), current sensors with single-digit pico-Ampere sensitivities became a necessity since the transfer of ions through the cell membrane induces extremely small electrical current transients that occur over fairly short durations [22, 52]. Activation events recorded by patch-clamps typically require bandwidths as high as 5-10 kHz to capture the complete time-domain information given that the time constant of the membrane charging waveform is about $16 - 20\ \mu s$ [59]. The smallest levels of change in electrical current measured through patch-clamps are typically around 5-10 pA. This is because patch-clamping allows for monitoring of ion currents through single ion channels which only permit very little charge transfer [59]. Whole cell recordings on the other hand can sometimes create current signals as large as 10-20 nA [66].

Prior arts of patch clamp recording mostly use continuous time TIAs that directly interface the pipette electrode output [77, 34]. Despite large bandwidth at the TIA output, the tradeoff between the transimpedance gain and the input referred noise level ultimately limits the performance of the design. In addition, most of these continuous TIA designs suffer from elevated noise floor at lower frequencies due to the flicker noise contributions.

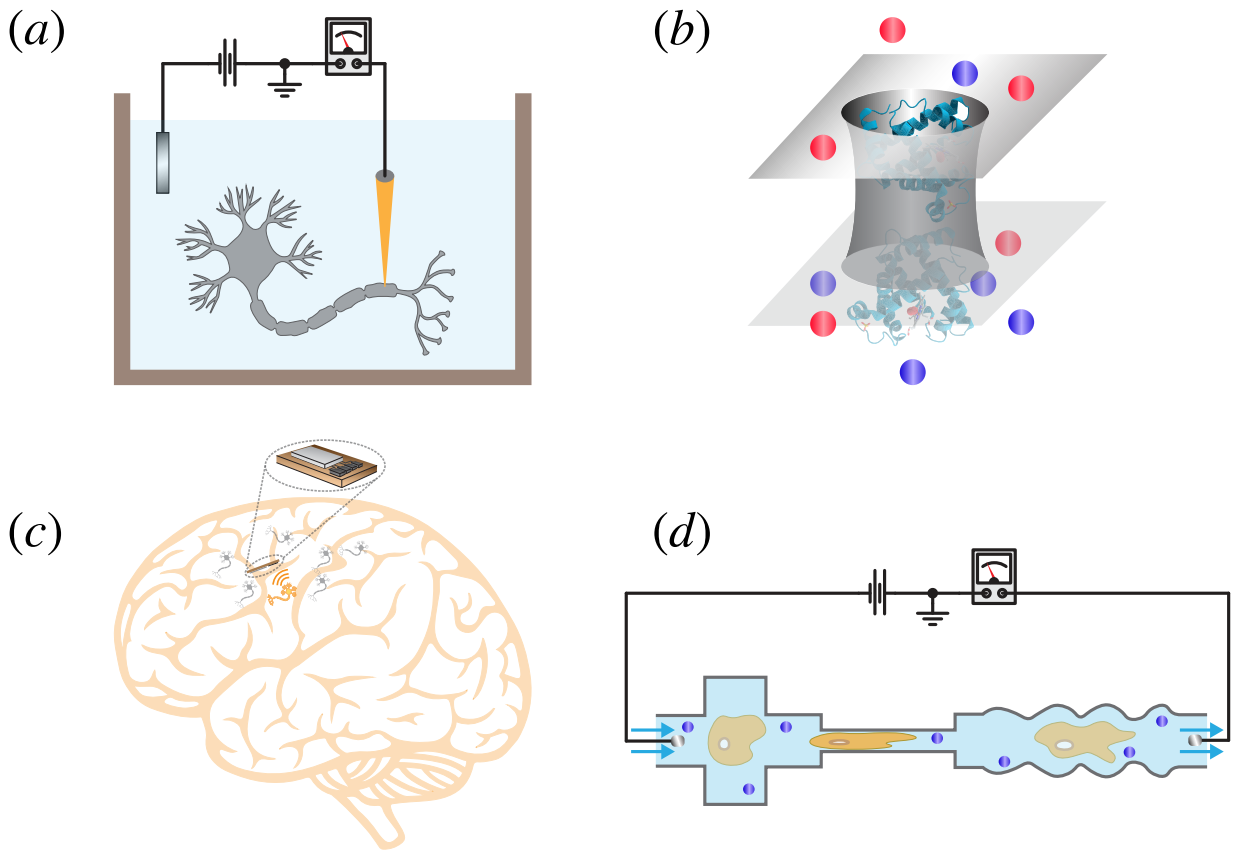


Figure 4.1: Applications for low noise current sensors. (a) Recording of ion channel currents via patch-clamps in neurons. (b) Silicon nano-pores passing various bio-molecules such as proteins. (c) Capturing fluorescence activity of stimulated neurons in brain. (d) Characterization of cells mechanical phenotypes via microfluidic channels.

Si Nanopore Sensing

Silicon nano-pores, Fig. 4.1(b), have been introduced as inexpensive biomolecule detection assays especially in DNA sequencing applications [6]. Passage of specific biomolecules through the nanopore induces a momentary blockage changing the ion based electrical current passing through the pore where depending on the size of the pore and the amount of change in current, the type of the biomolecule can be classified. Current fluctuations occurring across a blocked nanopore can usually exhibit around 1-10pA of change depending on the size of the pore as well as the target biomolecule. The typical speed at which these fluctuations occur can typically range from 1 to 5 kHz, therefore needing a minimum sampling rate of 10 kS/s.

Prior arts of nanopore sensing have explored a variety of approaches to the design of the

current sensor. [69] proposed a two stage integrate-then-differentiate scheme with analog high pass filtering. The achieved noise floor was about 10 $fA/rtHz$ over a bandwidth of 10 kHz. However similar to the patch-clamp sensors, the large transimpedance gain of 330 $M\Omega$ limited the dynamic range and overall the sensor required 30 mW of power to operate. [85] introduced a sigma-delta based direct current to digital converter that significantly reduced the power consumption to $\sim$ 50 μW while achieving a 30 $fA/rtHz$ input current noise density. However, this noise performance only existed for a 10 Hz bandwidth and extending the sensor bandwidth to 10 kHz resulted in two orders of magnitude higher noise floor.

Fluorescence Imaging

Single-pixel monitoring of fluorescence activity of genetically modified neurons is another example in which the fluorescent light induces a small photocurrent in a photodetector that is then acquired using a current sensor [24]. This imaging technique can be further extended into implantable imagers shown in Fig. 4.1(c) that are placed in close proximity of target neurons collecting the fluorescent response with a higher efficiency and therefore reducing the needed stimulation light intensity. To collect the full time-domain fluorescence of optically stimulated neurons, a readout bandwidth as large as 2-5 kHz is usually needed especially when using genetically encoded voltage indicators (GEVI)[45]. Imaging of fluorescence activity with a minimum signal to shot noise ratio of 20 demands at least 400 photons which with a 90% detector conversion efficiency result in about $\sim$ 440 e^- of input signals to the imager IC [28, 58]. With a typical 2 ms time constant for GEVIs [58] and a sampling frequency of 10 kS/s, the allowable standard deviation for every sample taken from each recorded action potential will be about 440 e^- that with a 50 μs integration window results in about $\sim 1.4pA_{rms}$ of input referred RMS noise for the sensor IC. An implantable imager IC sitting nearby the target neurons can significantly increase the numerical aperture (NA) of the readout enhancing the signal strength such that a higher sensor IRN can still be tolerated.

Single pixel imaging is an application that has not been as extensively explored by prior arts as in the case of other applications. A single-pixel fluorescence imager IC was introduced in [24] where a CTIA amplifier was used whose output was sampled and converted by a high resolution delta-sigma ADC. The design delivered a reasonable performance by only consuming about 2.4mW of power. However, the noise and linearity of the system was yet limited by the CTIA block where it at best achieved $\sim$ 160 $fA/rtHz$ of input referred noise density.

Microfluidic Channels Recording

Mechanical deformability and stiffness properties of living cells have been shown to correlate with the development of cancerous properties [80] where an increase in the stiffness can indicate the contribution of the cell to developing tumors. Various methods have been explored by prior arts to evaluate the mechanical viscoelastic properties of the living cells, a technique

known as mechanical phenotyping. Optical and acoustice tweezers have been used by prior arts [40, 43] to assess the response of a floating living cell to certain forces and deformations. However, the throughput of such methods is extremely limited to a few cells per hour [33]. Mechano-nanopore sensing was introduced by [33] that uses a microfluidic contraction channel to perform similar assays with substantially higher throughputs potentially reaching thousands of cells per minute. Fig. 4.1(d) depicts a microfluidic channel that is used for mechanical phenotype characterization of different cells. As shown, a cell is passed through the channel where specific deformations are caused in the cell shape and based on the viscoelasticity properties of the cell, its response to such deformations varies which can be measured by capturing the overall channel resistance or rather recording the small electrical current across the channel [33]. As for recording of electrical currents across microfluidic channels, sub-ms resolution is needed to fully digitize current fluctuations caused by the passage of the cell through the channel [33]. This means that the target sensor requires a sampling frequency in the range of 2-5 kS/s. The deformation of the cell and its recovery when going through contractions exhibit a change in the electrical impedance across the channel. Prior art uses DC channel resistance as a proxy to monitor these changes and the same method is aimed in this work; however, this approach can be further extended to capture the entire frequency domain complex impedance of channel in future works. The change in the electrical current therefore depends on the applied voltage across the channel. Prior art and works by our colleagues indicate an expected current fluctuations of around 20-100 nA when a 5 V DC voltage is applied across the channel [33]. However, applying a voltage as large as 5 V across the cells can potentially result in unfavorable side effects reducing the accuracy of the measurements. Lowering this voltage to around 0.5-1 V would reduce the current signal down to 2-20 nA at the input of the sensor. To find the smallest changes in the input signal, the microfluidic flow current changes can be used as shown in Eq. 4.1 from [33].

$$\frac{\Delta I}{I} = \frac{d^3}{D_e^2 L}\left[\frac{1}{1-0.8(d/D_e)^3}\right] \tag{4.1}$$

where d is the cell diameter, L is the overall channel length, and D_e is the effective channel diameter. With smallest cell sizes being around 4 μm, the changes in the current can even be 5$\times$ smaller than the above ranges. To have a minimum SNR of 40 dB, a minimum detectable signal of $\sim 4\ pA$ is required from the sensor.

Our Focus

Table 4.1 summarizes the requirements of the above applications. As seen, most of these applications can benefit from a current sensor capable of measuring fast and small changes in electrical currents with sensitivities of a few pA and sample rates as high as 5-10 kS/s. Despite potential suitability for all of above applications, the focus of this work is on the recording of electrical currents through microfluidic channels for mechanical phenotype characterization of living cells. The setup used by [33] consisted of a bulky PCB and a separate data acquisition unit (DAQ) to only record from a single microfluidic channel. This work

Table 4.1: Summary of requirements for current sensing applications

Application	Sensitivity (pA)	Bandwidth (kHz)
Patch-Clamping	1-5	5-10
Si Nanopore Sensing	1-10	2-5
Fluorescence Imaging	1-10	1-2
Microfluidic Ch. Recording	4-10	2-5

targets a 4-channel IC that can integrate all the components of the larger setup with a much improved noise performance. A minimum detectable signal of around 1.5-4 pA_{rms} is targeted while achieving a maximum signal of $\sim$ 20 nA matching the required specifications. Furthermore, the target sub-50 fA/rtHz of IRN is targeted over $>$ 2 kHz of bandwidth without sacrificing the dynamic range of the sensor. The remainder of this chapter is organized as follows. In section 4.2, the system requirements as well as sensor architecture are reviewed. Section 4.3 covers the IC design details followed by section 4.4 that goes over the measurement results. A comparison against prior arts is presented in section 4.5 and finally section 4.6 discusses future directions of this work.

4.2 Sensor Overview

Traditional current sensors typically consist of a transimpedance amplifier at the very input that converts the input current into a voltage. This voltage generally contains noise at bandwidths much higher than the input bandwidth. Therefore, the TIA output bandwidth needs to be limited via a filter stage following the TIA. Finally, the output of the filter can be sampled and converted by an ADC. Some current sensors contain current DACs at the input of the chain that help cancel unwanted components of the input signal or provide feedback as in Δ-Σ converters. The addition of an I-DAC at the input however generally results in an elevated sensor noise floor due to the presence of the I-DAC noise. This issue will be reviewed again in the later sections of this chapter. In the first implementation of this work to achieve a low input referred current noise, the classic architecture with no input I-DACs is used.

Architecture

A single readout channel architecture of the IC is diagrammed in Fig. 4.2(a). The input current is first amplified via a single-ended capacitive TIA. A CTIA architecture is used to minimize the input current noise via eliminating the noise of the feedback resistor. The input current is integrated using the CTIA stage which is reset at the beginning of every

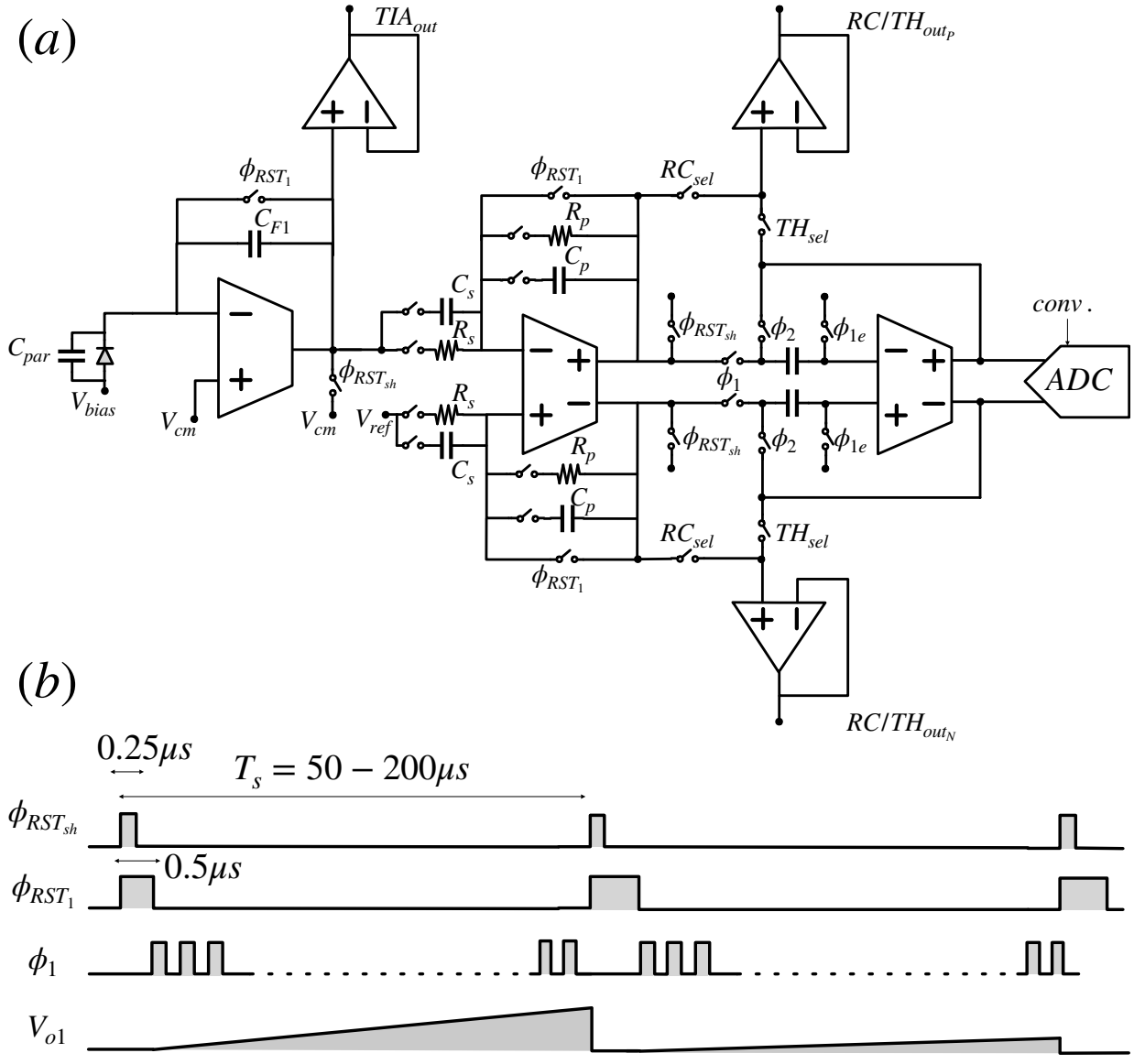


Figure 4.2: Readout channel block-diagram (a) and timing diagram (b)

integration phase. The durartion of the reset phase is extremely short lasting for a maximum of 500 ns allowing the integration period and therefore SNR to be maximized. Once reset switches are open, the input current is integrated across C_{F1} creating a voltage at the TIA output. The size of C_{F1} is 7-bit tunable to set the trans-impedance gain in the range of 5 MΩ to 640 MΩ. Moreover, the integration time is set by the period of the reset signal typically

ranging around 50 μs - 200 μs. The TIA output voltage is then passed into an RC amplifier that serves both as a band-limiting filter as well as an adjustable gain stage with a gain of 1-16×. It is critical to limit the bandwidth of the TIA output voltage prior to sampling given that the noise bandwidth of the TIA output is typically orders of magnitude larger than the bandwidth of the input signal. In addition, the TIA single-ended output signal is converted into a differential signal by being subtracted from a reference voltage V_{ref} equal to the DC bias point of the TIA. The output of the RC amplifier is then sampled by a flip-around track-and-hold (T/H) stage running nominally at $f_s = 1\ MS/s$. This keeps the sampled voltage at the T/H output until the ADC performs the conversion. A 16-bit asynchronous SAR ADC then digitizes the T/H output passing the data into the digital backend. The ADC is time-multiplexed across all four channels running nominally at 4 MS/s. The existence of T/H stages allows for simultaneous sampling of all four channel signals while the ADC is rotating through channels to perform the conversion. The SAR ADC uses a 1-bit redundancy scheme with non-binary weights to allow for foreground calibration of the weights lowering the nonlinearity induced by capacitor mismatch. The unit capacitor of the SAR ADC is sized $\sim 0.25\ fF$ and is manually designed and laid out using custom MOM capacitors. This minimizes the ADC area while delivering >15b of linearity.

The timing diagram of the channel is shown in Fig. 4.2(b). The reset phase is composed of two phases. The short phase, $\phi_{RST_{sh}}$ lasting about half of the reset duration shorts the TIA input and output to the common mode bias voltage, V_{cm}, via low-resistance switches. This quickly empties any charge across input and output capacitances allowing for very fast reset operation. During the second half of the reset phase, shorting switches are open and the OTA is put in a unity-gain feedback via ϕ_{RST_1} letting the TIA to settle to its stable bias point. This is critical since the OTA might have an offset voltage resulting in a bias point different than the applied common mode voltage, V_{cm} and helps prepare the TIA for the integration phase. The same reset scheme is applied to the RC amplifier as well so that once the reset phase is over, all no memory from the previous integration phase is preserved in any sub-block. The T/H block operates in two phases, tracking and retention. During the tracking phase (ϕ_1 & ϕ_{1e}), the 4 pF sampling capacitors differentially sample the RC amplifier output while the T/H OTA is in common-mode reset. In phase 2 (ϕ_2), the caps are disconnected from the input and are flipped around to connect across the T/H OTA. The T/H clock frequency is nominally set at 1 MHz. This oversamples the RC amplifier output signal and the multiple samples are used to lower the noise variance of the output samples enabling ultra-low noise operation. The next subsection discusses this concept in detail.

Channel Oversampling

Using a reset-CTIA induces reset kT/C noise that is sampled across the TIA input capacitors right after the reset switch opens. The sampled kT/C noise is typically very large ruining the noise performance of the system if not cancelled. The majority of prior arts that use CTIA topology employ a correlated double sampling (CDS) scheme to remove the sampled kT/C, offset, and attenuate flicker noise. Two samples are taken, one at the beginning of the

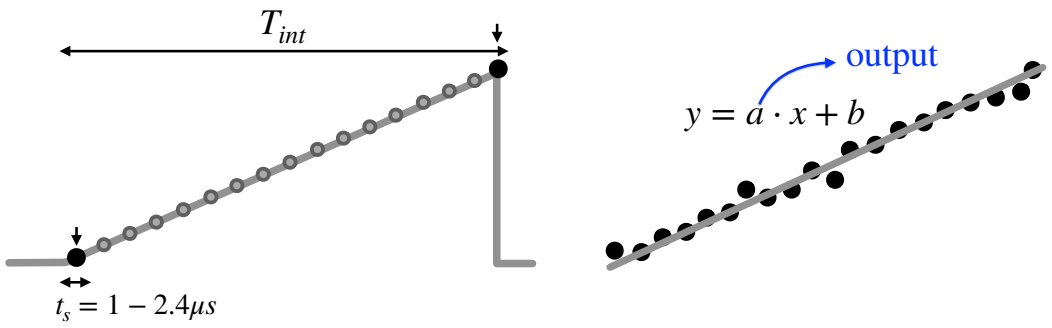


Figure 4.3: Oversampling of the integration ramp. Slope of the fit line represents the net input signal during the integration phase.

integration ramp, and the other at the end of it and the difference of the two samples represents the net output value. However, for the first sample to be an accurate representation of the sampled kT/C, the TIA closed-loop bandwidth has to large enough that it settles to the desired accuracy within the time span of that single sample. As an example, if the first sample is taken only after $t_s = \frac{T_{int}}{100}$, the TIA output has to settle within t_s. This imposes a strict requirement on the bandwidth of the TIA demanding a closed-loop speed that is at least 100× higher. Higher TIA closed-loop bandwidth in turn increases the noise bandwidth at the TIA output further increasing the variance of the output samples.

In this work, we employ the ramp oversampling technique proposed in [19]. Fig. 4.3 shows this scheme where the ramp signal is sampled by the maximum frequency allowable by the TIA closed-loop bandwidth. Then at the output, the slope of the best fit line (least-squared-error) represents the net signal received during the integration phase. Defining the output this way brings major benefits in terms of noise attenuation. First, since the slope of the line is independent of its bias, any sampled kT/C noise that basically acts as a DC shift to all samples is immediately removed. The low frequency flicker noise also sees a much greater attenuation this way compared to results using traditional CDS. This is because CDS is essentially a subset of this technique using only the two end-point samples. The overall transfer function of the applied line-fitting is shown in Eq. 4.2 when using n sample points.

$$\frac{M'(z)}{Y(z)} = \frac{n}{2}\frac{(n-1)z^2 - (n+1)z + (n+1)z^{2-n} - (n-1)z^{1-n}}{z^2 - 2z + 1} \tag{4.2}$$

This transfer function is effectively an n^{th}-order high-pass filter that gets rid of low frequency noise as explained. Appendix D discusses the mathematical analysis behind this approach to further illustrate the effect. To achieve the desired noise level of $< 50\ fA/rtHz$, an external ADC sample rate of 825 kS/s is selected that gives ~ 160 samples with a 200 μs integration period. The following section discusses the designed IC in greater detail and goes over the sub-block optimizations.

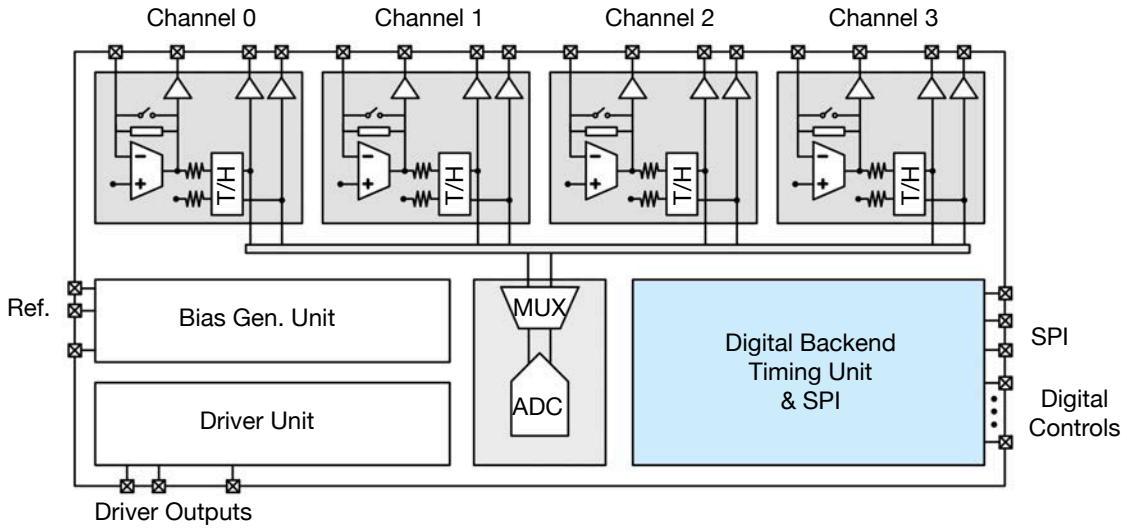


Figure 4.4: Sensor IC full chip block diagram.

4.3 Current Sensor IC

The block diagram of the sensor IC is shown in Fig. 4.4. The chip consists of four simultaneously recorded readout channels sharing a time-multiplexed 16-bit SAR ADC. An on-chip PTAT current reference creates the bias currents for all sub-blocks. Channel timing signals are provided via digital pads while the sub-blocks' configuration settings are programmed via an on-chip serial programming interface (SPI). The ADC data is also read through the SPI using an external FPGA or micro-controller. On-chip logic toggles the ADC input through all four channels as well as a debug-mode auxiliary input. An on-chip 1.8 V current driver unit is also implemented to allow for simultaneous drive and measurement using a single IC.

The CTIA block uses a single-stage gain-boosted folded-cascode OTA shown in Fig. 4.5. A single stage topology guarantees closed-loop stability at any input capacitance and gain while providing the largest speed/power ratio since no compensation is needed. Folded-cascode gain-boosting OTAs enhance the gain of the OTA to greater than 95 dB providing the desired accuracy. Folded-stage top and bottom devices are degenerated to attenuate flicker noise. Cascoding the input stage maintains a low Miller C_{GD} cap at the input enhancing the closed-loop bandwidth of the design. The tail current source consists of a regulated resistor-based current source that has minimal flicker noise while obtaining a very large output impedance enhancing CMRR. The TIA uses a 1.8 V supply voltage to provide sufficient output swing. The single-ended output voltage provides a 600-700 mV linear swing while achieving >80 dB of THD. The input devices are sized large to maximize the current efficiency factor (g_m/I_D) and minimize flicker noise. The common mode input voltage of the TIA is set via an off-chip voltage reference that is sufficiently low-pass filtered to minimize bias voltage noise impact. The TIA uses a nominal bias current of $\sim 5\,mA$ to achieve >30 mS

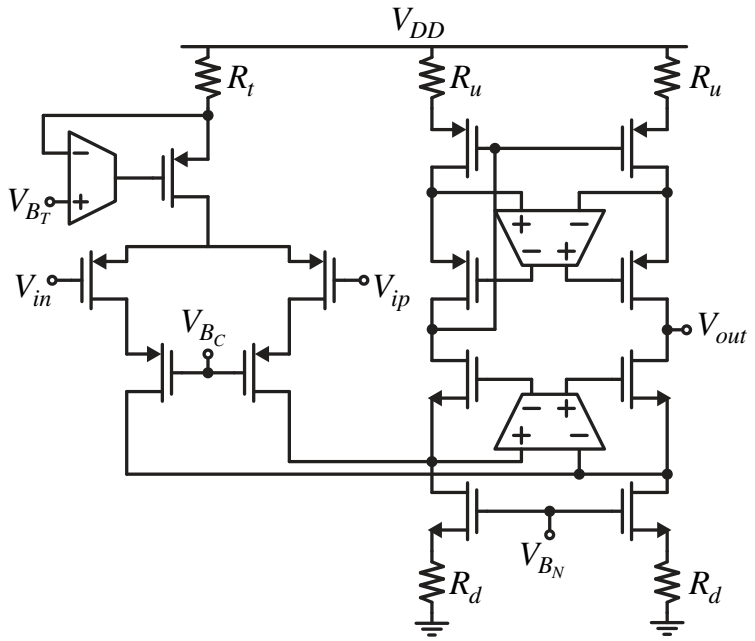


Figure 4.5: The core OTA of the CTIA block.

of transconductance (g_m) in the input devices needed for both noise and speed requirements.

4.4 Measurement Results

Chip Micrograph & Power Breakdown

The sensor IC was designed and fabricated in a TSMC 28 nm 1P10M CMOS technology. The chip occupying an area of 1.8 × 1.53 mm^2 consists of four simultaneously recorded channels. The chip micrograph is shown in Fig. 4.6(a). Each channel occupies an area of 1000 × 240 μm^2 and consumes a total of 11.86 mW of power out of 1.8/1 V supplies. The power breakdown of each channel is also depicted in Fig. 4.6(b) where the TIA power dominates the overall power consumption due to the critical noise floor constraint.

Bench-top measurements

Electrical bench-top testing is performed to assess the performance of the readout channels using an off-chip ADC, AD4001 and ADC driver, AD4940. Fig. 4.7 plots the input referred noise spectrum of the readout channel at a total transimpedance gain of $\sim 38\ M\Omega$ sampling at 5 kS/s with a total input parasitic capacitance of $\sim 35\ pF$. It measures a current noise density of $\sim$ 33 $fA/rtHz$ and a total RMS noise of $\sim$ 1.6 pA_{rms} matching the target

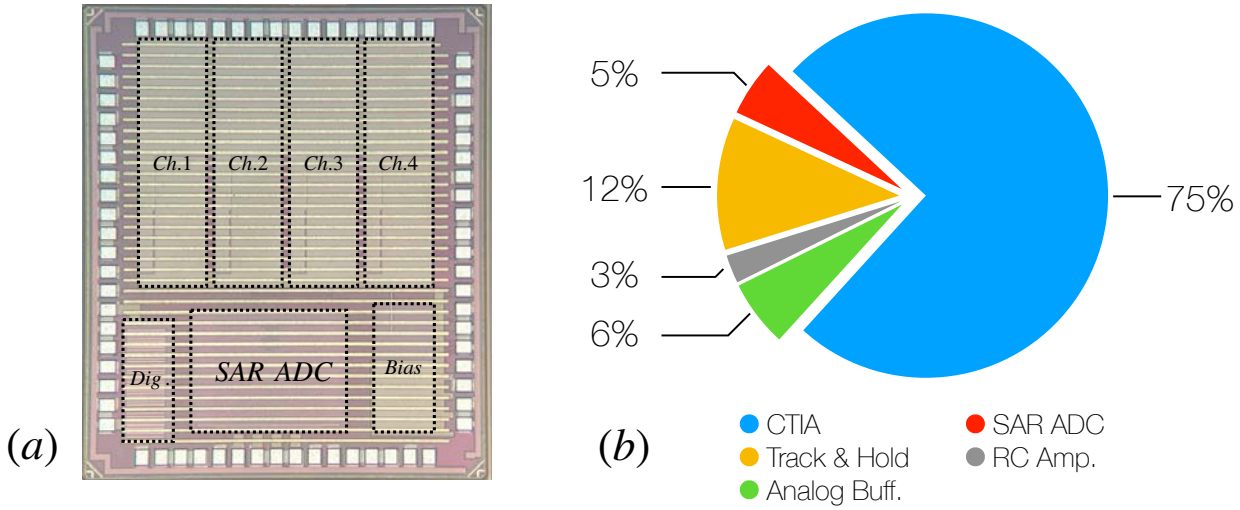


Figure 4.6: Sensor IC chip micrograph (a) and channel power breakdown (b)

specification. This noise floor is achieved while the fast sample rate of the off-chip ADC was set to 825 kS/s taking $\sim$ 160 samples per integration ramp resulting in a noise reduction factor of $\sim$ 3.6. Running the same setup at 1 MS/s would enhance the noise reduction factor to $\sim$ 4.1 lowering the noise floor to $\sim$ 1.4 pA_{rms} without sacrificing other performance metrics.

The static linearity of the channel is measured using ramp inputs from a low distortion wave generator (SRS DS360). An input ramp voltage signal with an amplitude of $\sim 600mV$ is applied in series with a 40 MΩ resistance at the channel input to achieve full scale 600 mV swing at TIA output. The recorded ramps are compared against fit line and the worst case INL and DNL are measured and plotted in Fig. 4.8. Less than 100 ppm worst case INL and less than 10 ppm of worst case DNL are measured while running at full scale linear output range. The linearity of the channel is also characterized using tone test. An input 16 nA_{PP} sine wave current at $f_{in} = 8$ Hz is applied to channel input and the output spectrum is plotted in Fig. 4.9. A total harmonic distortion of $\sim$ 81 dB and an SFDR of $\sim$ 83 dB is measured where the 3^{rd} harmonic is the dominant spur at the output. The source used at the test contains spurs at higher frequencies which are irrelevant to the measured linearity.

4.5 Summary and Comparison

The performance of the IC is compared against current sensors from the most recent prior arts. Table 4.5 shows a comparison chart that contains the most important specifications. To facilitate comparison, two figures of merit are used that represent the overall performance of the sensor. First, the Schreier FoM is used that is typically employed when comparing

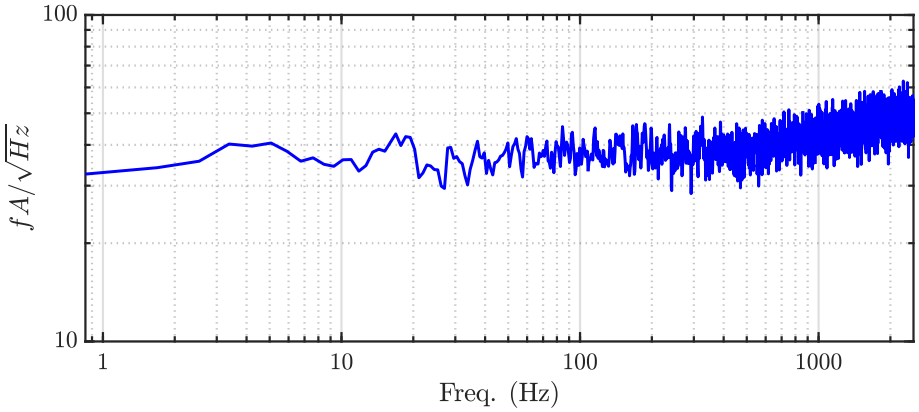


Figure 4.7: Input referred noise spectrum at 5 kS/s and 38 MΩ of transimpedance gain. Slight increase at >500 Hz is due to TIA loop gain drop.

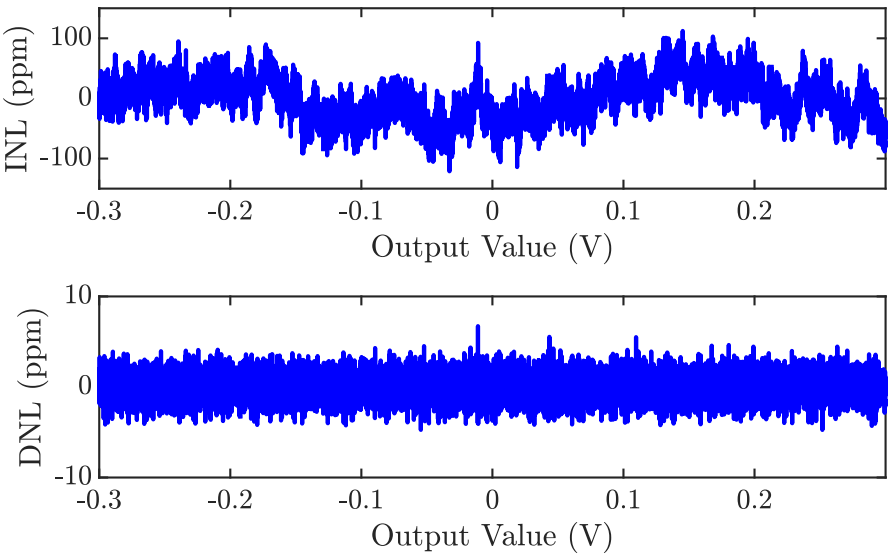


Figure 4.8: Measured INL and DNL of the overall channel using ramp input. Less than 100 ppm worst case INL and less than 10 ppm of worst case DNL are measured.

ADCs with Delta-Sigma architectures. In addition, a new figure of merit (FoM) for current sensors is proposed and used for comparison which is defined as follows.

$$FoM_{CS} = \frac{DR \cdot f_s}{V_{DD} \cdot P} \tag{4.3}$$

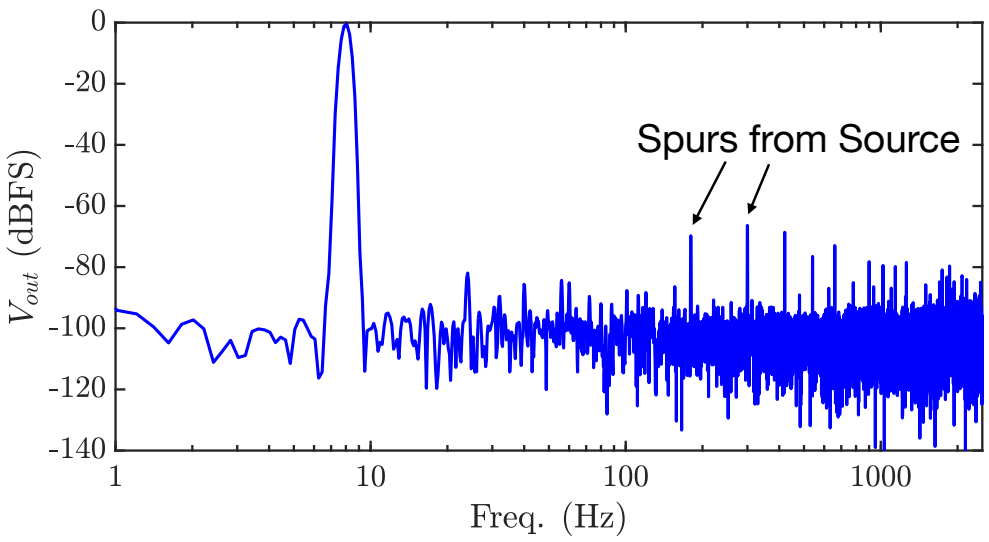


Figure 4.9: Measured spectrum of tone test with 16 nA_{PP} sine wave input at 8 Hz.

with P denoting the sensor power, DR denoting the sensor dynamic range, f_s denoting the sample rate, and V_{DD} denoting the sensor supply voltage. The motivation behind the introduction of this FoM is that as discussed in detail in appendix C, achieving the same dynamic range in an analog amplifier that is limited by the thermal noise is more challenging at lower supply voltages. In other words, changing the V_{DD} has a stronger impact on the sensor dynamic range than merely changing the sensor power. Further discussions of this FoM and its derivation are presented in appendix C. This FoM is used to achieve a more realistic comparison against the prior arts than using only the Schreier FoM especially when the supply voltages of sensors are different. As seen, compared to works with $< 100\ fA/rtHz$ of IRN density, this work achieves the largest SNDR and one of the highest figures of merit. It should be noted that the prior arts with the highest FoMs are all CTDSM direct current to digital converters that achieve a very wide dynamic range at moderate power levels. However, the input referred noise level of these sensors are significantly (2-3 orders of magnitude) larger than that of other works making them unsuitable for sensing of small electrical currents. Next section will discuss these architectures in more detail with ideas to improve their noise performance.

4.6 Future Directions

The first generation IC achieved all target performance specifications that are needed to realize a sensor in the discussed applications. The power consumption of the IC however is about 12 mW which makes it very challenging to power as an implantable device. Next

Table 4.2: Comparison with prior arts of current sensing ICs

Reference	ISSCC 2011 [24]	TBioCAS 2009 [77]	ISSCC 2020 [78]	JSSC 2020 [1]	ISSCC 2021 [41]	TBioCAS 2021 [85]	This Work
Technology (nm)	180	500	55	180	28	180	28
Architecture	CTIA	RTIA	CTDSM	CTIA	CTDSM	CTDSM	CTIA
Area (mm^2)	0.9×1.4	1.15×0.7	0.7×0.7	0.25×0.1	2.8×1.2	0.4×0.27	1×0.24
V_{DD} (V)	1.8	3.3	1.2	3.6	1.2	1.8	1.8
DR (dB)	77	59	102	57.4[a]	87	78	87
IRN ($fA/rtHz$)	160	52	20,000[a]	40[a]	340[a]	30	33
BW (kHz)	0.8	10	2	4.7	1	0.01	2.5
Power (mW)	2.4	0.9[b]	0.454	0.305	0.028	0.05	11.6
FoM_S (kHz/mW)	4.7×10^3	1.98×10^4	1.1×10^6	2.2×10^4	1.6×10^6	3.1×10^3	9.6×10^3
FoM_{CS} (kHz/mW/V)	2.6×10^3	6×10^3	9.16×10^5	6.1×10^3	1.33×10^6	1.72×10^3	5.3×10^3

[a] Estimated [b] TIA power only

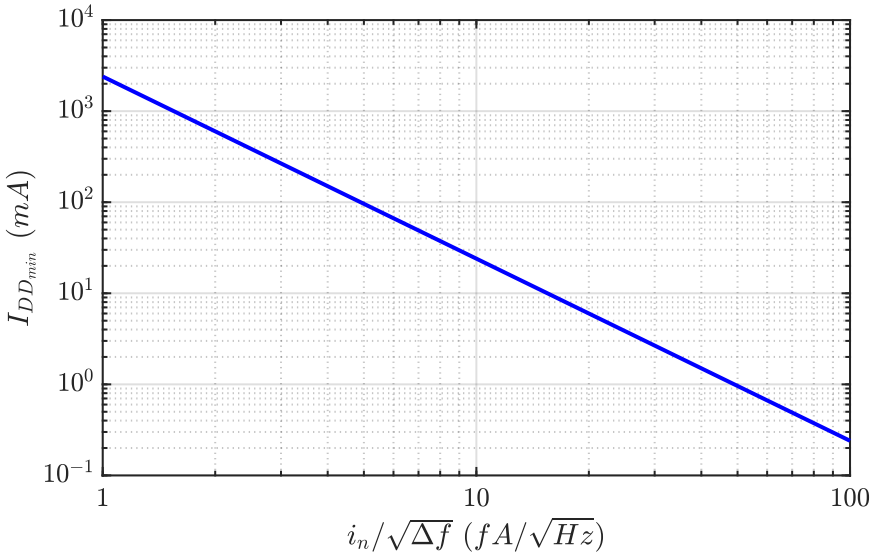


Figure 4.10: Minimum required supply current vs. input referred noise floor. Typical values are used from the design to achieve realistic takeaways.

subsection goes back to the principles of traditional TIA-input architectures and explains why their power consumption is tightly constrained by the dynamic range requirements. Then the following subsection focuses on ideas to significantly reduce the power consumption of the sensor beyond traditional topologies.

Traditional TIA-input architectures

The majority of the sensor power consumption discussed in the previous chapter was spent in the CTIA block to minimize the input referred current noise. While the sampled kT/C and flicker noise are greatly attenuated via the line fitting approach, the thermal noise of the TIA dominates the overall input noise of the sensor. The simple thermal input referred voltage noise density of a single transistor follows the well-known expression below.

$$\frac{\overline{v_{n_{th}}^2}}{\Delta f} = 4kT\gamma\frac{1}{g_m} \tag{4.4}$$

Eq. 4.4 immediately explains the tradeoff between power and noise performance of various designs. A more accurate tradeoff can be observed via Eq. 4.5 where the dynamic range of the sensor is directly impacted by the power, the supply, the speed, as well as the input dependent feedback factor of the TIA.

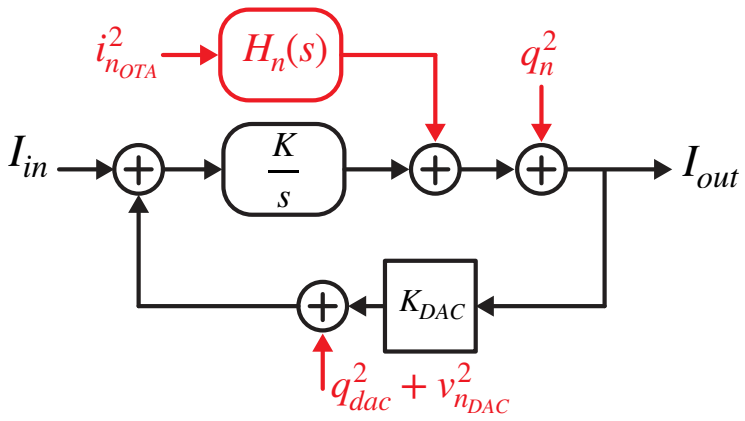


Figure 4.11: Signal flow graph for a first order DSM current converter. The noise sources and their transfer functions are highlighted in red.

$$DR \propto \frac{V_{DD} \cdot P \cdot \beta^2}{f_s} \tag{4.5}$$

Using reasonable values and a simple OTA topology for the design, Fig. 4.10 plots the minimum required supply current vs. the desired input referred current noise density given a fixed maximum current. As it stands, to achieve $\sim 30fA/rtHz$, supply currents of greater than 3 mA are needed which results in an overall power consumption of a few mWs. Therefore, all traditional architectures comprised of only a TIA at the input will inevitably suffer from this bottleneck and therefore cannot provide a better performance.

Δ-Σ Modulated Converters

In reviewing of prior works focused on wide dynamic range current sensors, many of the recent arts utilize non-traditional Δ-Σ Modulator (DSM) architectures for direct current to digital conversion of the input signals. [78] demonstrated simple resistive I-DAC input converters using a reset-then-open technique to minimize the DAC noise. The majority of the power was consumed by the digital backend and decimation filters, but in the analog domain, the noise of the frontend was limited by the input I-DACs and not the TIA. [41] extended this technique by significantly lowering the power consumption of the converter down to $\sim 28\ \mu W$; but the noise floor of the converter is still limited by the I-DACs and not the TIA. This signals of a benefit in using DSM-based architectures in suppressing the TIA noise at lower TIA power levels. To take a closer look, consider the diagram shown in Fig. 4.11. The TIA is modeled as an ideal continuous time integrator which is the loop filter of a first order DSM converter. The input current of the TIA observes this transfer function as

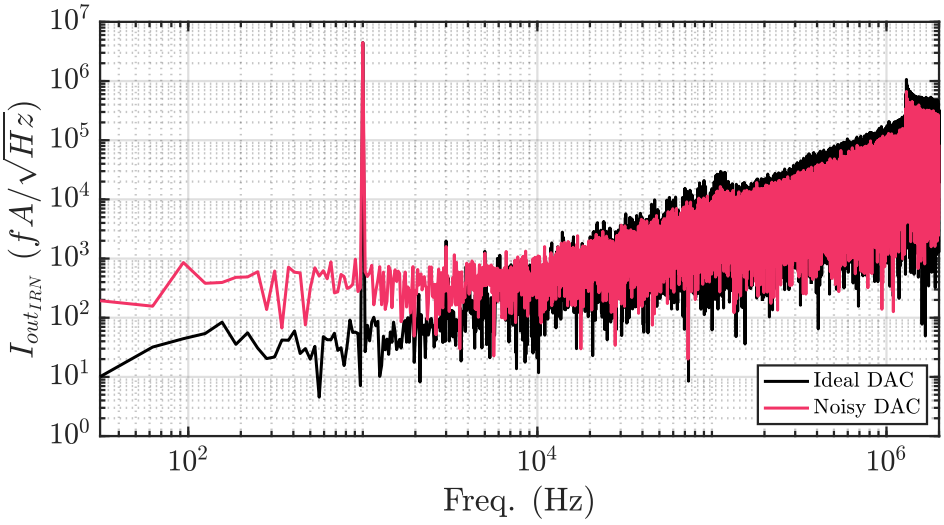


Figure 4.12: Input referred spectrum of a 4 MS/s 1^{st}-order Δ-Σ converter with and without the DAC noise. As seen, the DAC noise completely dominates the input referred noise of the frontend at lower frequencies.

it is continuously integrated over time. The noise of the TIA however is added at its output node while only seeing a low-pass transfer function with a -3 dB corner frequency close to the loop bandwidth. This means that in essence throughout the operation of the converter, the TIA noise spectrum is pretty flat over frequency and can be viewed as an elevated quantizer noise. As a result, the TIA noise once propagated to the modulator's output, I_{out}, goes through the 1^{st} order noise shaping which considerably suppresses its density at lower frequencies. Therefore, the same input referred noise contribution from TIA can be achieved at a much lower power dissipation compared to values from Fig. 4.10. In the case of higher order modulators, since the TIA noise is added to the loop at the output of the first stage, a 1^{st} order noise shaping is the best that can be achieved.

Fig. 4.12 displays the input referred spectrum of a 1^{st}-order Δ-Σ current converter operating at 200 μA of TIA supply current achieving a noise floor of $\sim$ 30 $fA/rtHz$ while running at 4MS/s. Inclusion of the DSM DAC noise however signifcantly increases the noise floor to about 300 $fA/rtHz$ because of the I-DACs resistors Johnson noise. This noise is unavoidable when using noisy DACs simply because of the current that the input DACs need to supply. In addition, when the input amplitude increases, the current of I-DACs goes up as well further increasing the noise floor. As a result, state-of-the-art of Δ-Σ current converters cannot resolve a 1 pA signal on top of a 100 nA input despite having a >100 dB nominal dynamic range. The following subsection introduces a noise shaping return-to-zero (RZ) current DAC that can replace resistive I-DACs in state-of-the-art to further improve the noise performance of the system.

Noise shaping RZ I-DAC

Resistive I-DACs discussed previously generate white wide-band thermal noise that contaminate the signal spectrum right at the input of the sensor. In addition, the quantization noise of the I-DAC also raises the noise floor in the case of multi-bit DSM converters. This work introduces a noise-shaping return-to-zero (RZ) I-DAC that reduces the noise floor at the signal band, significantly improving the in-band SNR. The circuit block diagram of this I-DAC is shown in Fig. 4.13. It consists of P and N sides capable of sourcing and sinking current pulses at their output. Current sources are implemented using regulated capacitively-degenerated topologies where the amplifiers' input voltage is provided via a multi-bit resistive voltage DAC. The R-DACs create a ramp voltage per each current pulse that is then regulated and driven across the C_{DAC}. The current of C_{DAC} as expected is the time-domain derivative of the voltage across it, giving a constant current pulse at the output. Therefore in essence, this I-DAC performs a differentiation on the input DAC code to create the output current. The operation of this I-DAC is as follows. During the reset, $\overline{\phi_N}$ and $\overline{\phi_P}$ switches reset the C_{DAC} capacitors to reset voltages that are slightly below/above the R-DAC's first code. When the reset phase is over, the DAC first code drives the C_{DAC} to the associated voltage overwriting any stored kT/C noise. Then the output switches (ϕ_N and ϕ_P) close and at the same time the R-DAC voltage ramp begins. Non-overlapping clocks drive ϕ and $\overline{\phi}$ signals to make sure no unwanted current flows into the DAC outputs. This process is then repeated for every current pulse, positive or negative, fulfilling the job of the pulsed I-DAC. During the time that $\phi_{N,P}$ is inactive, the output current is zero, and as a result the design works as a return-to-zero I-DAC. The amplitude of the output current pulses depend on the slope of the voltage ramp as well as the size of the C_{DAC} following Eq. 4.6.

$$I_{out} = C_{DAC} \cdot \frac{\Delta V}{\Delta T} \tag{4.6}$$

In the I-DAC shown in Fig. 4.13, there are multiple noise sources that can propagate into the final DAC output. The DAC quantization noise, the Johnson noise of the R-DAC as well as the input referred noise of the amplifier all observe the differentiating transfer function of the DAC. As a result, their noise contribution undergoes a 1^{st}-order noise shaping, thereby being significantly suppressed at the signal band. The differentiation also flattens the flicker noise of the amplifier, effectively acting as an auto-zeroing. The sampled kT/C noise of the reset phase is fully overwritten right before the active phase begins and therefore does not impact the noise performance. However, switching of ϕ and $\overline{\phi}$ switches at the output induces a switched-cap resistance at that node injecting thermal current noise. But since the output impedance of the I-DAC is very large and the drains of the MOS devices have very small parasitic capacitance, this noise contribution of this parasitic resistance remains low. Any voltage noise on the ground and supply rails also goes through the differentiation and hence does not impact the noise performance. Hence, the proposed I-DAC is capable of achieving very low output current noise densities. Fig. 4.14 shows the time-domain and frequency domain representation of the simulated 200 nA I-DAC current pulses repeating at 1 MHz.

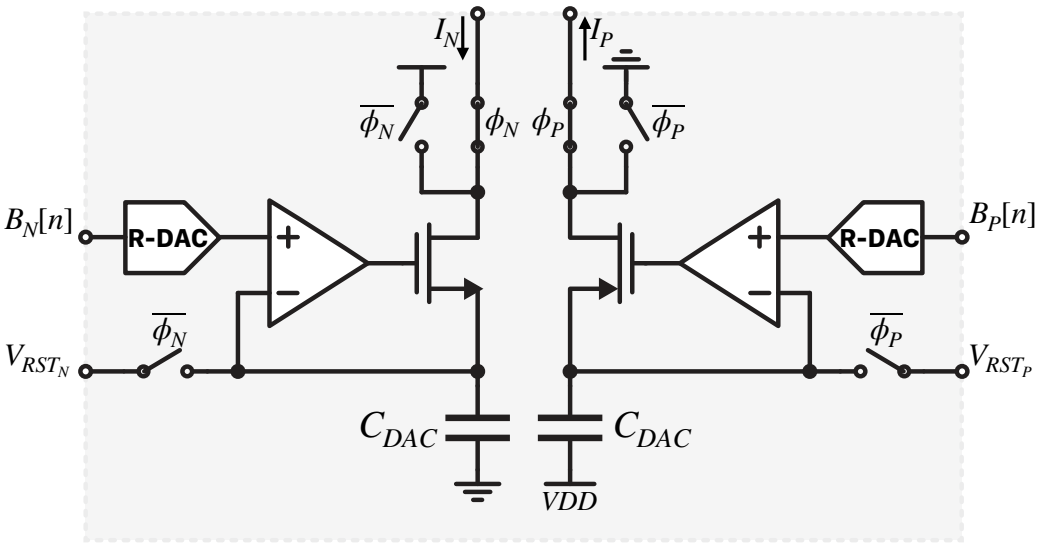


Figure 4.13: Circuit block diagram of the noise-shaping RZ I-DAC.

As shown in Fig. 4.14(a), each 200 nA current pulse includes a short RZ phase lasting only about 20 ns. The spectrum of this current waveform is shown in Fig. 4.14(b). At lower frequencies, the noise floor is ultimately limited by the switched-cap parasitic resistance at the DAC output achieving a very low 30 fA/rtHz current noise density. The shaped noise components increase the noise density with frequency, but the noise floor goes up only at frequencies well outside the signal bandwidth. Please note that the 200 nA DC component is not visible in the spectrum plot simply because of the log-scale definition of the x-axis as well as coherent sampling. Therefore, about a 10× reduction in the I-DAC noise is achieved compared to the conventional resistor-based I-DAC topologies while operating with the same 200 nA full-scale. In this simulation, a 10 pF MOM capacitor is used for C_{DAC} which is completely reasonable for on-chip implementation. Furthermore, the slope of the R-DAC voltage ramp was only 20 $mV/\mu s$ which can easily be implemented on-chip. The R-DAC and the amplifier had a combined $\sim 40\ nV/rtHz$ voltage noise density that can be achieved by only a few μWs of power. Consequently, the proposed I-DAC offers a superior noise performance with minimal chip power and area overhead. This low-noise I-DAC can then be used within a Δ-Σ converter to achieve the optimum noise performance.

Δ-Σ converter with noise-shaping I-DAC

The noise-shaping I-DAC can be employed in the Δ-Σ architecture to significantly improve the noise performance. However, the input-output transfer function of the I-DAC contains a differentiation which can disrupt the overall loop transfer function of the Δ-Σ loop if not addressed properly. For this purpose, a modified Δ-Σ architecture is suggested where the

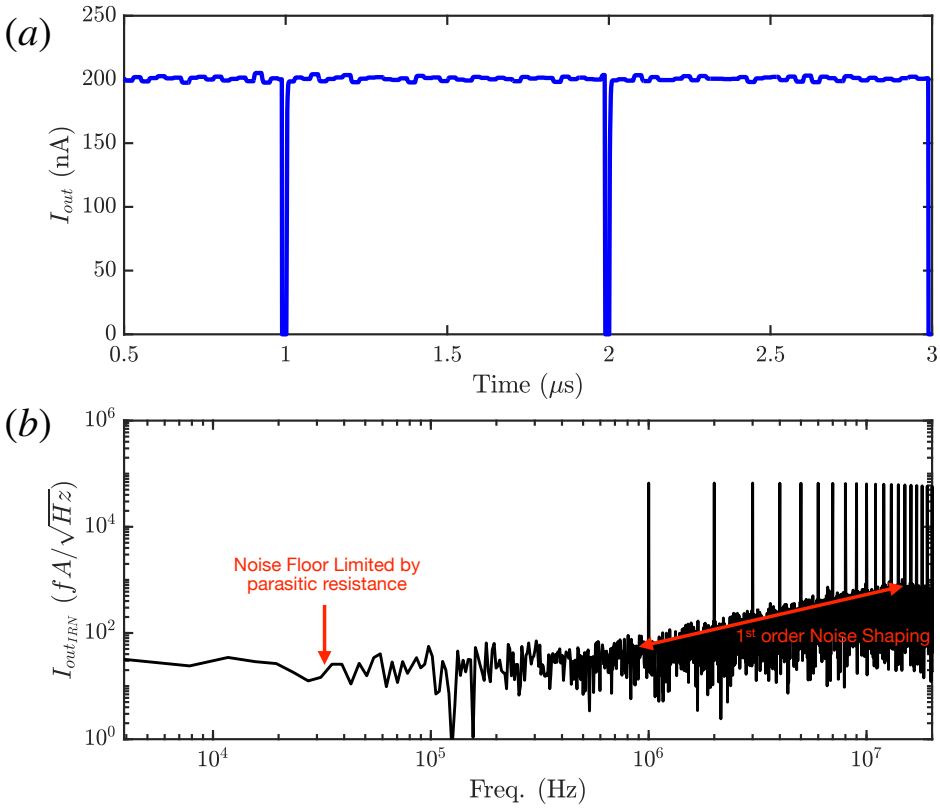


Figure 4.14: NS-RZ I-DAC 200 nA output current time domain waveform (a) and power spectrum density (b)

I-DAC differentiation is compensated using digital up-sampling and integration. This is to essentially create a ramp per DSM output bit so that the I-DAC can create the corresponding current pulse at the input. The digital integration happens using a simple multi-bit accumulator that takes very little digital area and power and does not incur additional noise.

4.7 Final Thoughts

This chapter proposed a low noise high bandwidth current sensor IC achieving 30 fA/rtHz of current noise density at 5 kS/s sampling rate. The bottleneck of the design in terms of power consumption was discussed and alternative solutions were proposed to exploit noise-shaping topologies that can run with a much lower power consumption. Future generations of the proposed IC will exploit the ideas suggested in the final section to deliver the same noise and bandwidth performance at much lower power fulfilling the ultimate target sensor requirements and advancing the noise performance of the state-of-the-art by at least a factor

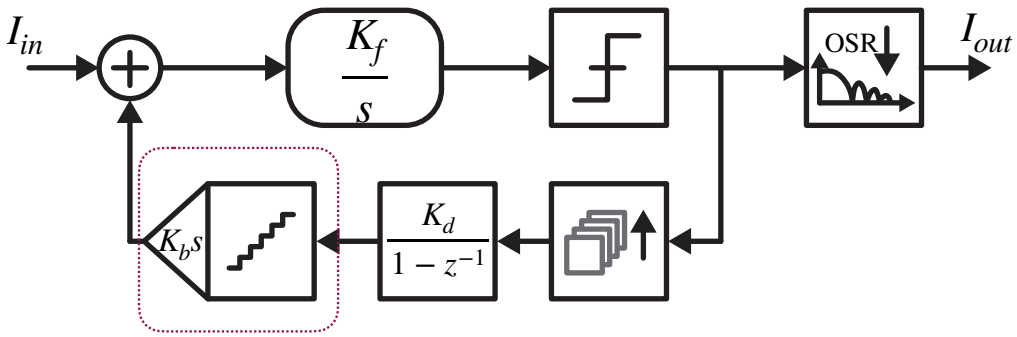


Figure 4.15: Signal flow graph of the modified Δ-Σ current converter using noise shaping RZ I-DAC as highlighted.

of 10×.

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Appendix A

Noise analysis, CTIA vs. ZTIA

In chapter 2, we discussed how for designing a current sensor that handles substantially large parasitic capacitances, C_{Par}, a ZTIA topology can perform better than the CTIA architecture. This appendix covers the analytical description of the TIA noise when operating with a large C_{Par} at the input. For simplicity, the core OTA is modeled as a single stage with a transconductance of g_m. Fig. A.1 shows the representative diagram of the discussed circuit. The two major sources of noise are the amplifier thermal noise modeled as a current source at the OTA output as well as the thermal noise of R_F. Each of these sources impact the TIA output voltage with their specific transfer functions, shown in simplified forms as follows (Eq. A.1 & A.2).

$$H_{v_{n_{R_F}}}(s) = \frac{C_{Par}s + g_m}{C_{Par}C_F R_F s^2 + (C_{Par} + C_F g_m R_F)s + g_m} \tag{A.1}$$

$$H_{i_{n_{g_m}}}(s) = \frac{R_F(C_{Par} + C_F)s + 1}{C_{Par}C_F R_F s^2 + (C_{Par} + C_F g_m R_F)s + g_m} \tag{A.2}$$

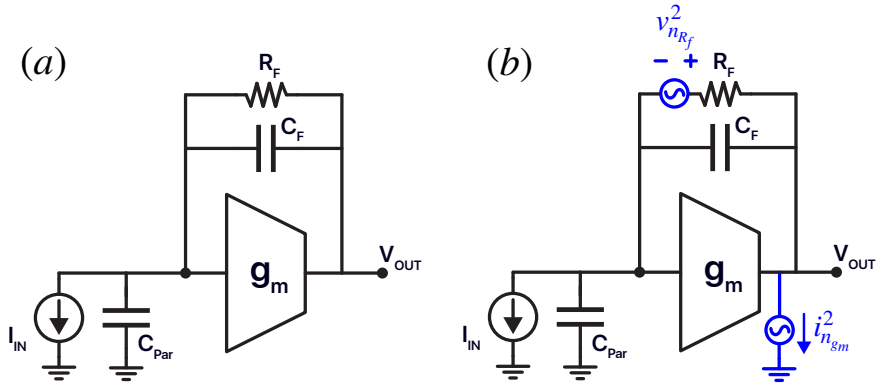

Figure A.1: A simplified diagram of the ZTIA (a) in its noise sources (b).

The power spectral densities (PSD) of the two noise sources can be written as:

$$\frac{v_{n_{R_F}}^2}{\Delta f} = 4kTR_F, \qquad \frac{i_{n_{g_m}}^2}{\Delta f} = 4kT\gamma\alpha g_m \tag{A.3}$$

Where α and γ are parameters relating to the technology and topology of choice and T is the absolute temperature. For simplicity, we assume $\alpha = 1$, $\gamma = 1$. This gives the following PSD for the TIA output noise:

$$S_{N_{out}}(f) \approx 4kT\left(\frac{1}{g_m} + R_F\right) \times \left(\frac{4\pi^2 \frac{R_F}{g_m} C_{Par}^2 f^2 + 1}{16\pi^4 C_F^2 C_{Par}^2 \frac{R_F^2}{g_m^2} f^4 + 4\pi^2\left(\frac{C_{Par}^2}{g_m^2} + R_F^2 C_F^2\right) f^2 + 1}\right) \tag{A.4}$$

At low frequencies, the PSD has a value of,

$$S_{N_{out}}(f) \approx 4kT\left(\frac{1}{g_m} + R_F\right) \tag{A.5}$$

The shape of the PSD in Eq. A.4 changes with the values of C_{Par} and C_F varying with respect to each other. As C_{Par} increases, the PSD begins to peak at higher frequencies. This high frequency noise can however be attenuated through the subsequent stages since it exceeds the observation bandwidth of the frontend. In this work, using a reset integrator as the following block (section IV-C), the required filtering can be achieved. The boxcar averaging applies a Sinc transfer function to the TIA output as follows:

$$H_{Sinc}(f) = \frac{T_{Int}}{R_{Int} \cdot C_{Int}} \cdot Sinc(T_{Int} \cdot f) \tag{A.6}$$

Integrating Eq. A.4 when filtered by the transfer function in Eq. A.6 will determine the variance of a single sample taken at the ADC output. Eq. A.4 can also be used to find the noise PSD of the CTIA topology prior to sampling, via setting $R_F \to \infty$, resulting in:

$$S_{N_{out_{CTIA}}}(f) = 4kT\frac{1}{g_m} \cdot 1/\left(4\pi^2 \frac{C_F^2}{g_m^2} f^2 + \frac{C_F^2}{C_{Par}^2}\right) \tag{A.7}$$

At low frequencies, the OTA input referred voltage noise is boosted by a factor of C_{Par}/C_F at the CTIA output, highlighting the issue of CTIA topology in handling large C_{Par}. In practice, CTIA designs require reset phases inducing reset kT/C noise which will then be removed via CDS. [13] provides a comprehensive analysis of this scheme. The effective output noise PSD of that scheme can be found as:

$$S_{N_{CDS}}(f) = 2(\pi f_C T_{Int} - 1)\left(1 + \frac{C_{Par}}{C_F}\right)^2 \times 4kT\frac{1}{g_m} \cdot Sinc^2(T_{Int} \cdot f) \tag{A.8}$$

where f_C is the closed loop bandwidth of the CTIA. By integrating this PSD, one can find the variance of a sample at the CTIA output. Fig. A.2 shows the variance of samples taken in

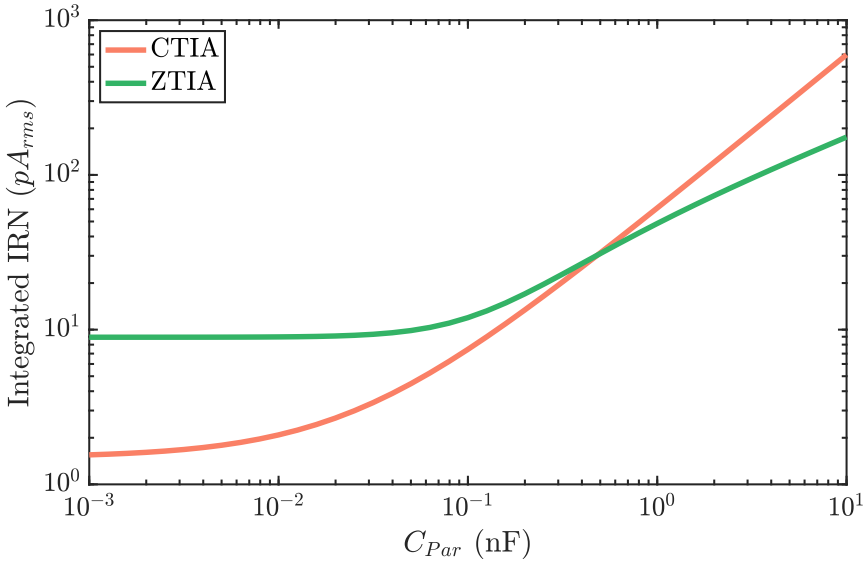

Figure A.2: The input referred standard deviation of a single sample taken in ZTIA and CTIA schemes versus C_{Par}.

both CTIA and ZTIA schemes when C_{Par} changes from 1 pF to 10 nF. The following parameter values were used to produce the graph: $g_m = 2$ mS, $TI_{gain} = 2$ MΩ, and $T_{Int} = 50$ μs, which are typical numbers in the application. For both schemes, similar effective gain, T_{Int}, and g_m are assumed to deliver a fair comparison. This ensures that the same input can be amplified through the chain over the same observation window and using the same TIA power. Thus, based on the comparison results and since this work aims to acquire current out of a wide range of PDs with potentially very large C_{Par}, the ZTIA scheme is selected in the design.

The reader might wonder about the power consumption of the integrator in the ZTIA scheme. Since this block is after the first stage of gain, its input referred noise contribution even with smaller values of C_{Int} can stay negligible and thus its power consumption will not be prominent. It should be noted that some of the assumptions made in [13] are optimistic and in reality, the resulting output noise will be higher. For example, [13] assumes that the first sample of the CDS scheme is taken immediately after the reset phase is over. This cannot be true as the sampled noise charge across C_{Par} during the reset phase needs to be transferred onto C_F and this settling takes time depending on the closed loop bandwidth of the circuit. Thus, based on the comparison results and since this work aims to acquire current out of a wide range of PDs with potentially very large C_{Par}, the ZTIA scheme is selected in the design.

Appendix B

I/Q Demodulation in Impedance Acquisition

In this appendix, the governing equations of I/Q demodulation for impedance magnitude and phase extraction are reviewed. Consider a square wave stimulation current defined as in Eq. B.1 expanded by its Taylor's series.

$$I_{stim}(t) = I_0 \cdot pulse(f_Z t) = I_0 \sum_{i=1}^{\infty} \frac{1}{i} Sin(2\pi i f_Z t) \tag{B.1}$$

The electrode impedance causes a change in the amplitude and phase of the stimulation signal based on its frequency profile. Therefore, a total response voltage of $V_Z(t)$ is received at the channel input across the electrodes as shown in Eq. B.2.

$$V_Z(t) = I_0 \sum_{i=1}^{\infty} \frac{Z_i}{i} Sin(2\pi i f_Z t + \theta_i) \tag{B.2}$$

The ADC acquires the impedance signal and the output codes contain the digitized information. Without loss of generality, we continue writing the demodulation equations in continuous time domain knowing that the f_Z clock is derived from a master clock in the backend maintaining phase synchronicity. The impedance signal is then mixed with in-phase and quadrature components resulting in outputs shown below where i & j are odd integer indices.

$$Z_I(t) = I_0 \sum_{i=1}^{\infty} \frac{Z_i}{i} Sin(2\pi i f_Z t + \theta_i) \times K_{D_I} \sum_{j=1}^{\infty} \frac{1}{j} Sin(2\pi j f_Z t) \tag{B.3}$$

$$Z_Q(t) = I_0 \sum_{i=1}^{\infty} \frac{Z_i}{i} Sin(2\pi i f_Z t + \theta_i) \times K_{D_Q} \sum_{j=1}^{\infty} \frac{1}{j} Sin(2\pi j f_Z t + 90^\circ) \tag{B.4}$$

Equations B.3 & B.4 can be slightly rearranged as follows.

$$\begin{aligned} Z_I(t) &= K_{D_I} I_0 \sum_{i=1}^{\infty}\sum_{j=1}^{\infty} \frac{Z_i}{i \cdot j} Sin(2\pi i f_Z t + \theta_i) Sin(2\pi j f_Z t) \\ &= \frac{K_{D_I} I_0}{2} \sum_{i=1}^{\infty}\sum_{j=1}^{\infty} \frac{Z_i}{i \cdot j} \left[Cos(2\pi(i-j) f_Z t + \theta_i) - Cos\left(2\pi(i+j) f_Z t + \theta_i\right)\right] \end{aligned} \tag{B.5}$$

$$\begin{aligned} Z_Q(t) &= -K_{D_Q} I_0 \sum_{i=1}^{\infty}\sum_{j=1}^{\infty} \frac{Z_i}{i \cdot j} Sin(2\pi i f_Z t + \theta_i) Cos(2\pi j f_Z t) \\ &= -\frac{K_{D_Q} I_0}{2} \sum_{i=1}^{\infty}\sum_{j=1}^{\infty} \frac{Z_i}{i \cdot j} \left[Sin(2\pi(i+j) f_Z t + \theta_i) + Sin\left(2\pi(i-j) f_Z t + \theta_i\right)\right] \end{aligned} \tag{B.6}$$

Low pass filtering Eq. B.5 & B.6 removes all the high frequency components leaving only the baseband components as shown in the following.

$$Z_I(t) = \frac{K_{D_I} I_0}{2} \sum_{i=1}^{\infty} \frac{Z_i}{i^2} Cos(\theta_i) \tag{B.7}$$

$$Z_Q(t) = -\frac{K_{D_Q} I_0}{2} \sum_{i=1}^{\infty} \frac{Z_i}{i^2} Sin\left(\theta_i\right) \tag{B.8}$$

If the demodulation backend has similar gains for I & Q outputs, i.e. $K_{D_I} = K_{D_Q} = K_D$ and the higher order harmonics are attenuated either by observing a much smaller Z_i or via originally performing sine-wave demodulation, one can arrive at the following results.

$$Z_I(t) = \frac{K_D I_0}{2} Z_{f_Z} Cos(\theta_Z) \tag{B.9}$$

$$Z_Q(t) = -\frac{K_D I_0}{2} Z_{f_Z} Sin\left(\theta_Z\right) \tag{B.10}$$

$$|Z_{f_Z}(t)| = \frac{2\sqrt{Z_I(t)^2 + Z_Q(t)^2}}{K_D I_0} \tag{B.11}$$

$$\angle Z_{f_Z}(t) = tan^{-1}\left(-\frac{Z_Q(t)}{Z_I(t)}\right) \tag{B.12}$$

Equations B.11 and B.12 can therefore be used to extract the time domain ESI magnitude and phase in the backend. Note that if there is not enough higher harmonics suppression, the output magnitude and phase results contain information at higher bands too as Eq. B.9 and B.10 suggest.

Appendix C

Current Sensors Figure of Merit

The goal of this appendix is to come up with a quantitative measure of generic current sensors' performance using a defined quantity as Figure of Merit (FoM). The first section develops a FoM for a simple capacitive Transimpedance Amplifiers (CTIA). In section C.2, this FoM is extended to all types of TIA architectures including ZTIAs. Finally, section C.3 reviews the Schrier FoM and provides and discusses the similarities and differences.

C.1 CTIA FoM

Consider a simple CTIA shown in Fig. C.1. There are a number of noise sources whose effect shows up at the output of the CTIA depending how it operates. Reset CTIAs typically exhibit a reset kT/C noise at their output that needs to be cancelled via correlated double sampling or similar techniques as discussed in appendix B. The g_m source itself exhibits

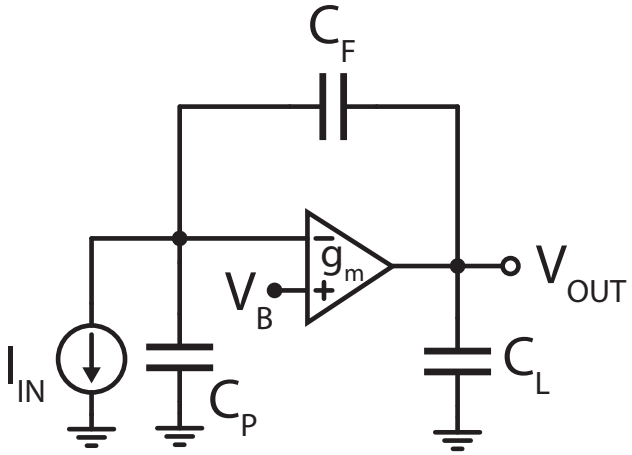

Figure C.1: Simple CTIA diagram with important components shown for the analysis.

different types of noise such as thermal noise, flicker noise, shot noise etc. that ultimately need to be considered upon completing the design. However, for the purpose of this analysis, it is reasonable to assume that the thermal noise of the amplifier is the major and dominant source of noise of the circuit. For this amplifier, the output noise density can be written as shown in C.1.

$$\frac{v_{n_{out}}^2}{\Delta f} = 4kT\gamma\alpha g_m \cdot \left(\frac{1}{\beta g_m}\right)^2 = \frac{4kT\gamma\alpha}{\beta^2 g_m} \tag{C.1}$$

where $\beta = \frac{C_F}{C_F+C_P} \approx \frac{C_F}{C_P}$ is the feedback factor of the TIA. This results in a total output noise variance expressed by Eq. C.2.

$$v_{n_{out}}^2 = \frac{4kT\gamma\alpha}{\beta^2 g_m} \cdot \frac{1}{4\frac{1}{\beta g_m}C_{tot}} = \frac{kT\gamma\alpha}{\beta C_{tot}} \tag{C.2}$$

where $C_{tot} = C_L + C_F||C_P \approx C_L + C_F = C_F\,(1 + C_L/C_F)$ represents the total capacitance driven by the TIA output. This means the larger the output capacitance, the lower the noise variance which is the traditional noise/bandwidth tradeoff. Now we proceed to find the input referred noise variance by dividing the output noise by the square of the transimpedance gain. The transimpedance gain of the TIA depends on the integration time which is inversely proportional to the sample rate of the TIA, Eq. C.3.

$$TI_{gain} = \frac{T_{int}}{C_F} = \frac{1}{f_s C_F} \tag{C.3}$$

As a result,

$$\begin{aligned} i_{n_{in}}^2 &= \frac{kT\gamma\alpha}{\beta C_{tot}} \cdot f_s^2 C_F^2 \\ &= \frac{kT\gamma\alpha}{\frac{C_F}{C_P} \cdot C_F(1 + C_L/C_F)} \cdot f_s^2 C_F^2 \\ &= \frac{kT\gamma\alpha C_P}{(1 + C_L/C_F)} \cdot f_s^2 \end{aligned} \tag{C.4}$$

This makes sense as higher sample rates or higher input parasitic capacitances result in higher the input referred noise. Next the maximum signal that can be acquired by the sensor is reviewed. Suppose the TIA output can support a voltage swing of $V_{Swing} = K_V V_{DD}$. This maximum swing should support that largest input current, $I_{in_{max}}$ when boosted with the transimpedance gain. Therefore,

$$I_{in_{max}} = K_V V_{DD} C_F f_s \tag{C.5}$$

The input dynamic range of the system can now be derived as shown in C.6.

$$\begin{aligned} DR &= \frac{I_{in_{max}}^2}{i_{n_{in}}^2} = \frac{K_V^2 V_{DD}^2 C_F^2 f_s^2}{\frac{kT\gamma\alpha C_P}{(1+C_L/C_F)} \cdot f_s^2} \\ &= \frac{K_V^2 V_{DD}^2 C_F^2 (1 + C_L/C_F)}{kT\gamma\alpha C_P} \\ &= \frac{K_V^2 V_{DD}^2 C_F^2}{kT\gamma\alpha C_P^2} \cdot C_P(1 + C_L/C_F) \end{aligned} \tag{C.6}$$

Note that by assuming a certain sample rate f_s, the TIA needs to be able to drive its load at that speed. This means the core OTA will need a large enough g_m to maintain the required bandwidth. We can thus relate the TIA bandwidth and its supply current as follows:

$$\begin{aligned} f_s &= K_f \frac{\beta g_m}{C_{tot}} \\ &= K_f \cdot \frac{C_F}{C_P} \cdot K_I I_{DD} \cdot \frac{1}{C_L + C_F} \\ &= K_f K_I I_{DD} \cdot \frac{1}{C_P(1 + C_L/C_F)} \end{aligned} \tag{C.7}$$

where K_I represents the current efficiency factor of the entire OTA. Equation C.7 can be rearranged in the following format.

$$C_P(1 + C_L/C_F) = K_f K_I I_{DD} \frac{1}{f_s} \tag{C.8}$$

Combining C.6 and C.8, the overall dynamic range can be rewritten as follows.

$$DR = \frac{K_V^2 V_{DD}^2 C_F^2}{kT\gamma\alpha C_P^2} \cdot K_f K_I I_{DD} \frac{1}{f_s} \tag{C.9}$$

Expression C.9 can again be rearranged to keep all the design specific constants on one side and the measurable specifications on the other side.

$$\frac{DR \cdot f_s \cdot C_P^2}{V_{DD}^2 I_{DD}} = \frac{K_V^2 K_I K_f}{kT\gamma\alpha} \cdot C_F^2 \tag{C.10}$$

All parameters on the right side of C.10 are indicators of the design performance but the C_F. C_F is the feedback capacitance that is going to require a significant amount of area in the TIA design targeting low noise and high performance. As a result, it is possible to relate the value of C_F to the amount of area taken by the TIA. Defining $C_F = K_C \cdot A_{sensor}$, one can arrive at,

$$\frac{DR \cdot f_s \cdot C_P^2}{V_{DD}^2 I_{DD}} = \frac{K_V^2 K_I K_f}{kT\gamma\alpha} \cdot K_C^2 A_{sensor}^2 \tag{C.11}$$

With slight re-arrangements,

$$\frac{DR \cdot f_s \cdot C_P^2}{V_{DD}^2 I_{DD} A_{sensor}^2} = \frac{K_V^2 K_I K_f K_C^2}{kT\gamma\alpha} \tag{C.12}$$

The right side of C.12 only consists of design specific factors representing the performance of the TIA and can thus be defined as a figure of merit. Larger values of this FoM indicates higher performance by the design. Hence,

$$FoM_{CTIA} = \frac{DR \cdot f_s \cdot C_P^2}{V_{DD}^2 I_{DD} A_{sensor}^2} \tag{C.13}$$

C.2 Generic TIA FoM

The FoM in C.13 covers all important aspects of a thermal noise limited CTIA based current sensor. When considering ZTIAs, it is important to note that the feedback resistance can be a non-negligible source of noise dominating the noise floor of the TIA at lower frequencies. Integrating Eq. A.4 for $f : 0 \rightarrow \infty$ gives,

$$\begin{aligned} v_{n_{out}}^2 &= 4kT\left(\frac{1}{g_m} + R_F\right) \cdot \frac{1}{4}\frac{C_F + C_P}{C_F} \cdot \frac{1}{\frac{C_P}{g_m} + R_F C_F} \\ &\approx kT\frac{1/g_m + R_F}{\frac{C_F}{g_m} + R_F\frac{C_F^2}{C_P}} \end{aligned} \tag{C.14}$$

This noise variance can be referred to the input simply by dividing it by the square of the gain, R_F.

$$\begin{aligned} i_{n_{in}}^2 &= \frac{kT}{R_F^2} \cdot \frac{1/g_m + R_F}{\frac{C_F}{g_m} + R_F\frac{C_F^2}{C_P}} \\ &\approx \frac{kT \cdot C_P}{R_F^2 C_F^2} \end{aligned} \tag{C.15}$$

Similar to the previous section, the maximum input signal can also be mapped to the maximum output swing using the gain factor.

$$I_{in_{max}} = \frac{K_V V_{DD}}{R_F} \tag{C.16}$$

And thus the input dynamic range can be written as follows.

$$\begin{aligned} DR = \frac{I_{in_{max}}^2}{i_{n_{in}}^2} &= \frac{\frac{K_V^2 V_{DD}^2}{R_F^2}}{\frac{kT \cdot C_P}{R_F^2 C_F^2}} \\ &= \frac{K_V^2 V_{DD}^2 C_F^2}{kTC_P} \\ &= \frac{K_V^2 V_{DD}^2 C_F^2}{kTC_P^2} \cdot C_P \end{aligned} \tag{C.17}$$

Similar to the CTIA, the sampling frequency of the TIA can be linked to the settling time constant of the feedback loop.

$$f_s = K_f \cdot \frac{1}{R_F C_F} \tag{C.18}$$

Such a settling time constant necessitates that the non-dominant pole of the circuit is at a higher frequency than the dominant pole set by the feedback time constant $\tau_F = R_F C_F$. This requires a minimum OTA transconductane, g_m as described in C.19 where K_x is the pole separation factor.

$$g_m = K_x \frac{C_P}{R_F C_F} \tag{C.19}$$

$$\begin{aligned} K_I \cdot I_{DD} &= K_x \frac{C_P \cdot f_s}{K_f} \\ \rightarrow C_P &= \frac{K_f K_I I_{DD}}{K_x f_s} \end{aligned} \tag{C.20}$$

Plugging in C.17 for C_P from C.20, the following expression is obtained.

$$DR = \frac{K_V^2 V_{DD}^2 C_F^2}{kTC_P^2} \cdot \frac{K_f K_I I_{DD}}{K_x f_s} \tag{C.21}$$

With minor re-arrangements, expression C.21 can be rewritten as,

$$\frac{DR \cdot f_s}{V_{DD}^2 I_{DD}} \cdot \frac{C_P^2}{C_F^2} = \frac{K_V^2 K_I K_f}{kTK_x} \tag{C.22}$$

Note that C.22 is almost identical to C.10. This goes to show that our previous derived FoM for CTIA designs is in fact very much applicable to any TIAs in general and should bear the same conclusions. The ratio $\beta = \frac{C_F}{C_P}$ is a factor that is fundamentally limited based on the capacitor density of the technology used in the design as well as the sensor input parasitic capacitance in every application. Therefore, for sensors designed in the same application and using technologies with similar capacitance densities, this ratio can also be treated as a constant. We therefore proceed to re-define the generic TIA figure of merit as follows.

$$\begin{aligned} FoM_{TIA} &= \frac{DR \cdot f_s}{V_{DD}^2 I_{DD}} \\ &= \frac{DR \cdot f_s}{V_{DD} \cdot P} \end{aligned} \tag{C.23}$$

where P represents the power dissipated by the TIA. Interestingly, Eq. C.23 suggests that designing a TIA for a given dynamic range and sampling frequency as well as a determined power consumption is harder with lower supply voltages. Therefore, when compared against each other, designs in lower feature size technologies using lower V_{DD} are expected to be more difficult and consequently more valuable.

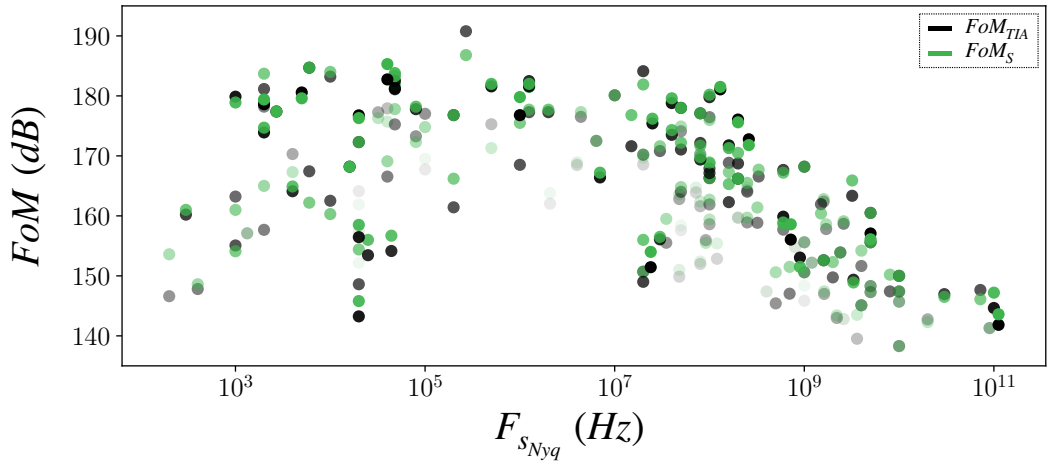

Figure C.2: The plot of FoM_{TIA} and FoM_S for works published in ISSCC to date.

C.3 I-to-D converters FoM

A vast group of recently published current sensors perform direct current to digital conversion using Δ-Σ modulators or other over-sampled architectures. Traditionally, Schreier FoM [57] has been used to compare these designs which is defined as follows.

$$FoM_S = \frac{DR \cdot f_N}{P}$$

where f_N indicates the Nyquist rate of the system in consideration. As discussed in [57], the design first described by the above FoM is based on a switched-capacitor Δ-Σ modulator and the derivation of the FoM assumes that the kT/C noise determines the minimum detectable signal of that frontend. However, [57] also assumes that for a class-A amplifier, the supply current of the frontend is set based on the maximum swing of the modulator output meaning $I_{DD} \propto \Delta V_{out}$ which results in the V_{DD} term being cancelled. Then a case is made in [57] for class-B amplifiers that do not have the above constraint resulting in,

$$P = 4kT \cdot DR \cdot f_N \frac{\overline{\Delta V_{in}}}{V_{DD}}$$

where $\overline{\Delta V_{in}}$ is the voltage difference at the input of the modulator. In practice, for a given input signal, $\overline{\Delta V_{in}}$ stays constant and therefore the result looks very similar to Eq. C.23. Therefore, the proposed FoM can serve not only for TIA based current sensors but also direct I-D converters including Δ-Σ modulator based architectures. Fig. C.2 plots FoMs C.23 and C.3 for works published in ISSCC to date using [50]. As seen, both FoMs display the same patterns with C.23 slightly preferring works with lower supply voltages.

Appendix D

Analysis of Ramp Oversampling

The ramp oversampling (or slope sampling) was a technique employed in chapter 4 where it reduced the overall noise variance at the output of the CTIA. To illustrate this effect, consider the slope of the LS fit line defined using regression analysis shown in Eq. D.1.

$$m[n] = \frac{n\sum_{i=0}^{n-1} x \cdot y - \sum_{i=0}^{n-1} x \cdot \sum_{i=0}^{n-1} y}{n\sum_{i=0}^{n-1} x^2 - \left(\sum_{i=0}^{n-1} x\right)^2} \tag{D.1}$$

in which x defines the time vector of the samples taken uniformly and y defines the vector of the obtained sample values. Replacing these vectors with proper values considering a uniform sample time, t_s provides the following expression.

$$m[n] = \frac{n\sum_{i=0}^{n-1} i\ t_s y[i] - \sum_{i=0}^{n-1} it_s \cdot \sum_{i=0}^{n-1} y[i]}{n\sum_{i=0}^{n-1} i^2 t_s^2 - \left(\sum_{i=0}^{n-1} it_s\right)^2} \tag{D.2}$$

Eq.D.2 can be further simplified into the following form.

$$m[n] = \frac{t_s\left(n\sum_{i=0}^{n-1} iy[i] - \frac{n(n-1)}{2} \cdot \sum_{i=0}^{n-1} y[i]\right)}{t_s^2 \cdot \left(\frac{(n-1)n^2(2n-1)}{6} - \frac{(n-1)^2n^2}{4}\right)} \tag{D.3}$$

Taking the Z transform of Eq.D.3 allows further simplification in the Z domain.

$$M(z) = \frac{n\sum_{i=0}^{n-1} iY(z)z^{i-(n-1)} - \frac{n(n-1)}{2} \cdot \sum_{i=0}^{n-1} Y(z)z^{i-(n-1)}}{t_s \cdot \left(\frac{(n-1)n^2(2n-1)}{6} - \frac{(n-1)^2n^2}{4}\right)} \tag{D.4}$$

The denominator of Eq. D.4 is merely a constant factor set by the number of samples and the sample time of the system and can be ignored when deriving the transfer function. Later when plotting the response, this factor will be included. Considering $M'[z]$ as the numerator, we can write:

$$M'(z) = Y(z)n\left(\sum_{i=0}^{n-1} iz^{i-(n-1)} - \frac{(n-1)}{2} \cdot \sum_{i=0}^{n-1} z^{i-(n-1)}\right) \tag{D.5}$$

With slight rearrangements,

$$M'(z) = Y(z)nz^{-(n-1)}\left(z\sum_{i=0}^{n-1} iz^{i-1} - \frac{(n-1)}{2}\cdot\sum_{i=0}^{n-1} z^i\right) \tag{D.6}$$

Now using geometric series theory, one can re-write D.6 in the following modified form.

$$M'(z) = Y(z)nz^{-(n-1)}\left(z\frac{\partial}{\partial z}\left(\frac{z^n-1}{z-1}\right) - \frac{(n-1)}{2}\cdot\frac{z^n-1}{z-1}\right) \tag{D.7}$$

With expansion and re-arrangements,

$$M'(z) = Y(z)nz^{-(n-1)}\left(z\frac{(n-1)z^n - nz^{n-1}+1}{(z-1)^2} - \frac{(n-1)}{2}\cdot\frac{z^n-1}{z-1}\right) \tag{D.8}$$

Eq. D.8 can be further simplified to give the final expression for the overall transfer function of the slope.

$$\frac{M'(z)}{Y(z)} = \frac{n}{2}\frac{(n-1)z^2 - (n+1)z + (n+1)z^{2-n} - (n-1)z^{1-n}}{z^2-2z+1} \tag{D.9}$$

which is an $(n+1)^{th}$-order high-pass transfer function attenuating all the low frequency noise and sampled kT/C components. It should be noted that the system consists of a down-sampling operation following the above line-fitting that only takes the single slope value for a collection of n samples at the TIA output. The Z transformation of a down-sampler block can be expressed as shown.

$$Y_D(z) = \frac{1}{n}\sum_{k=0}^{n-1} X\left(e^{-j2\pi k/n}z^{1/n}\right) \tag{D.10}$$

The down-sampling effectively scales or stretches the x-axis of the transfer function of the original fit-line, but does not impact the magnitude response. Therefore, we can plot the magnitude effect of the line-fitting technique in Fig. D.1. A fixed integration time of $T_{int} = 100\,\mu s$ has been selected for this plot and the number of samples, n, is swept from 2 (traditional CDS) to 256. As seen, within the frequency band of interest, $f = 0 - \frac{1}{2\cdot T_{int}}$, higher order transfer functions provide larger attenuation to the noise at all frequencies. Traditional CDS is known to increase the σ of white noise by $\sqrt{2}$ given that it combines two uncorrelated noisy samples with each other. This can be seen by the +3dB increase at $f = \frac{1}{2T_{int}}$ in the plot for n = 2. However, the line-fitting also reduces the white noise variance as shown in the plot. Note that higher n also necessitates higher bandwidth which increases the wide-band noise variance by a factor of n. It has been shown [19] that using this technique, the white noise standard deviation is reduced by a factor η shown below,

$$\eta = \sqrt{\frac{n}{12}} \tag{D.11}$$

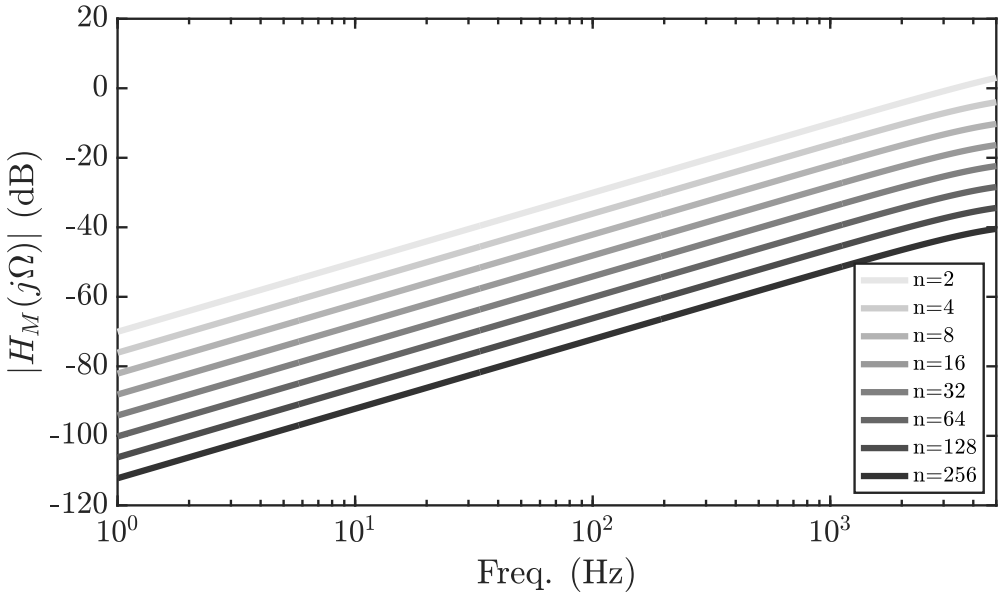

Figure D.1: The magnitude response of the line-fitting transfer function for a fix integration time of $T_{int} = 100\ \mu s$

Using the line-fitting technique allows for significant reduction of noise variance at the output samples. It should be noted that the technique comes with little additional cost. The TIA bandwidth already is set fast enough to perform a CDS while not losing any significant input signal power. Therefore, no extra power or bandwidth overhead is caused by introducing this technique. The only disadvantage of this technique is that it requires post-processing of output data which can require time and digital resources on the chip.