Design of High-Performance Hybrid Switched Capacitor Converters: Modeling, Layout, and Thermal Management

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Acknowledgement

I want to start by thanking my advisor, Professor Robert Pilawa-Podgurski. I firmly believe that joining his research group was the best decision I've ever made. He has cultivated an incredible environment at UC Berkeley, which I've cherished these past six years.
Next, I want to thank everyone in Robert's group; it was a pleasure working with you all.
To the rest of my committee, thank you for providing very helpful feedback on my work. Jessica, you have been an incredible role model for me. Nenad, it has been amazing working with you and your group, and I hope to continue doing so in the future.
Finally, I would like to extend a heartfelt thank you to my family. Without all of your love and support, this would not have been possible.

Thanks Mom and Dad, I dedicate this to you.

Design of High-Performance Hybrid Switched Capacitor Converters: Modeling, Layout, and Thermal Management

By

Logan Horowitz

A dissertation submitted in partial satisfaction of the

requirements for the degree of

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Abstract

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As the world transitions to sustainable energy solutions, the demand for electric vehicles and hyper-efficient data centers has soared. Advanced power electronics play a critical role in addressing the challenges of energy efficiency, performance, and scalability in both sectors. In this work, I detail our recent efforts toward the development of power converters achieving unprecedented performance through novel topologies, improved modeling, optimal component selection, and innovative design. Advanced thermal management strategies are essential to dissipate heat effectively and ensure reliability. I will highlight our recent progress in both of these domains, explore their synergistic impact on improving system performance, and outline promising future directions. Integration of these technologies is pivotal for realizing the future of sustainable transportation and energy-efficient computing, driving both economic and environmental benefits on a global scale.

To Mom and Dad

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I want to start by thanking my advisor, Professor Robert Pilawa-Podgurski. I firmly believe that joining his research group was the best decision I've ever made. I am extremely grateful to Robert for providing such unwavering support. I've learned so much from him technically, professionally, and personally. He has cultivated an incredible environment at UC Berkeley, which I've cherished these past six years.

Next, I want to thank everyone in Robert's group that I have been fortunate enough to work with. Starting with my first mentors: Nate Pallo and Sam Coday. My first cubicle-mates: Joseph Liu, Pourya Assem, Zichao Ye. My collaborators: Rose Abramson, Nathan Ellis, Elisa Krause, Finn Giardine, Marrin Nerenberg, Ben Liao, Sahana Krishnan. Everyone else in the group: Zitao, Zichao, Ting, Ivan, Sophia, Maggie, Kelly, Dennis, Emmi, Khalid, Nagesh, Biesterfeld, Shuyu, Leheng, Jack, and Yayun. It was a pleasure working with you all.

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To the rest of my committee, thank you for dealing with my lack of punctuality, and for providing very helpful feedback on my work. Jessica, you have been an incredible role model for me and provided so much inspiration for what I hope to accomplish as a young professor. Nenad, it has been amazing working with you and your group, and I hope to continue doing so in the future.

Finally, I would like to extend a heartfelt thank you to my family. Without all of your love and support, this would not have been possible.

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Chapter 1

Background

Power electronics are used across many different industries and applications. Broadly, they convert one form of electrical energy to another. Often, they are used to bridge the gap between the voltage supplied by a source (e.g. battery, solar panel, wind turbine, electrical grid, etc.) and a load (motor, electric vehicle (EV), processor, lighting, etc.). There are many dimensions to power converter design evaluation, but this work will focus on the maximization of efficiency and power density. Two different applications will be used as examples: Electric Vehicle Inverters & Data Center Power Delivery.

Five different steps in the power converter design process are identified here:

1. Topology & Modulation
2. Parameter Optimization
3. Component Sizing & Selection
4. Layout & Packaging
5. Thermal Management

These are depicted in Fig. 1.1 and will serve as the main areas of focus in this work.

Topology & Modulation

Power converters typically consist of switching elements such as transistors or diodes and passive components such as capacitors and inductors. A topology is defined by the components in the circuit as well as the connections between them. Modulation defines the timing by which the switching elements are turned on/off. Together, these two properties define how the circuit will operate. The first step in power converter design is to determine the most suitable topology and modulation.

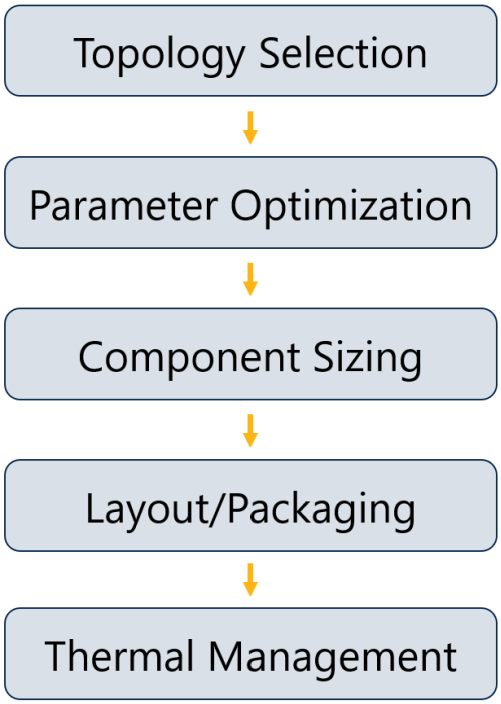


Figure 1.1: Five steps to high-performance power converter design.

Parameter Optimization

Once the topology and modulation are selected, there are many resultant design parameters which must be determined. The next step is to estimate performance of the converter as a function of these parameters in order to choose the best design point before fabrication.

Component Sizing & Selection

Once a design point has been chosen, all of the components can be selected. In practice, this has a large impact on converter performance. It is critical to incorporate the best switches and passive components, and then to utilize them effectively.

Layout & Packaging

Finally, once all of the components and connections are determined, it remains to put them together properly. There are many intricacies to component placement and printed circuit board (PCB) routing. The use of multiple PCBs also opens up new design space. A converter with high power density will inherently require components to be densely packed, which creates greater challenges, especially when dealing with high voltages.

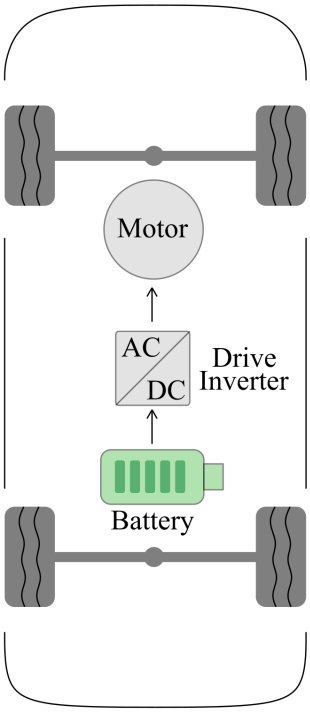


Figure 1.2: Simplified description of EV drivetrain highlighting the 'Drive Inverter' which converts dc voltage from the battery to ac power for the motor.

Thermal Management

As the density of power converters and computing electronics continues to grow, the heat flux which must be removed from these systems is growing in proportion and creating bottlenecks to further miniaturization. This is causing a radical shift away from conventional air-cooling to more advanced solutions. Future work will need to co-design the electrical and thermal systems to continue advancing performance.

1.1 Electric Vehicles

Transportation accounts for over 15 % of global energy-related emissions [3]. The electrification of vehicles offers a promising path to significantly reduce this pollution. Electric automobiles have gained widespread popularity, with sales growing by more than 20 % annually [3, 17]. Meanwhile, substantial progress has also been made toward partially and fully electric commercial aircraft. Multiple organizations have already demonstrated successful flight [80, 52], while there are many research projects underway to develop this technology further [101]. Both automobiles and aircraft rely on high-performance powertrains that demand extreme efficiency and power density [54, 16].

In order to accommodate increasing power levels, many automobile manufacturers have increased their main bus voltage to 800 V (Hyundai, Audi, Porsche, Tesla Cybertruck, etc.). There are many different applications for power converters in these vehicles including: dc-dc down-conversion from 800 V down to low-voltage system bus (48 V and below), dc-dc up-conversion from battery to main bus voltage (e.g. 400 V up to 800 V), ac-dc rectification from the grid to charge the battery, and dc-ac inversion from battery to main drive motor. Hardware demonstrations in Chapter 6 will focus on the final application: design of the inverter which takes electrical energy from the battery pack and delivers it to the motor(s). Fig. 1.2 highlights the role this plays in the powertrain of a battery electric vehicle. To improve power density, advanced motor designs often eliminate heavy magnetic materials such as steel and iron [41]. This greatly diminishes the electric machine inductance, however, thus requiring the inverter to deliver low-distortion current. Together with the increased bus voltage (800 V), this imposes strict requirements for the inverter. It is very difficult to simultaneously achieve high efficiency, high power density, and low distortion with conventional converter designs, which motivates work presented here.

1.2 Data Centers

The rapid growth of machine learning, artificial intelligence (AI), and the Internet of Things (IoT) is driving massive expansion in internet technology (IT) infrastructure. Data centers now account for approximately 2% of global energy consumption, and this is projected to continue growing exponentially [3, 22]. This has driven extreme changes across many aspects of data center infrastructure, including power delivery. Fig. 1.3 demonstrates the power delivery architecture for data centers starting from high-voltage ac on the grid and ending at the point-of-load (PoL), which primarily comprises the central processing units (CPUs) and graphics processing units (GPUs) running computations. Traditionally, a 3-stage dc-dc conversion architecture has been utilized, whereby a 400 V dc voltage is derived from the grid, and then stepped down through three converters: 400V to 48V, then 48V to 12V, and finally 12V to PoL. More recently, industry has been moving toward a 2-stage solution involving a 400V to 48V conversion and a 48V to PoL stage. These series conversions lead to increased size, large dc bus capacitors between stages, and cascaded efficiency penalties. As a result, there is significant room for improvement, which motivates work presented here.

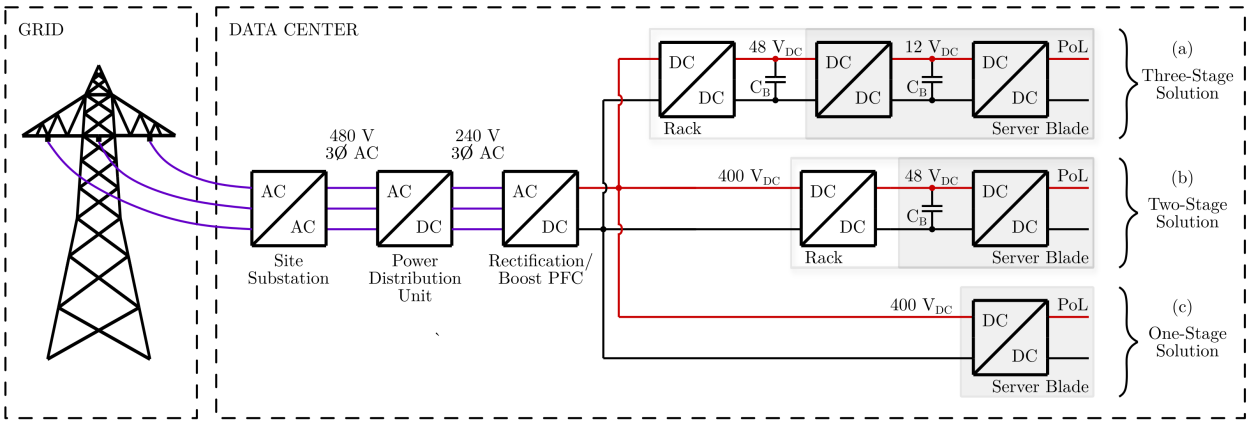


Figure 1.3: Data center power delivery architecture. (a) Traditional 3-stage design, (b) Recent 2-stage solution, (c) 1-stage approach proposed in this work.

Chapter 2

Topology & Modulation

2.1 EV Inverters

In order to realize the next generation of electric vehicles, aggressive targets have been set for drivetrain performance [54, 16]. System efficiency and power density are of top priority. High performance motors have eliminated the use of heavy magnetic materials such as steel or iron in order to reduce weight [41]. This decreases the electric machine inductance greatly, thus requiring the inverter to supply a low-distortion drive current. Moreover, size and weight reductions are further achieved through high rotational speed, which requires high electrical frequency.

The aforementioned constraints are challenging to meet with traditional inverter approaches based on half-bridge switching modules, depicted in Fig. 2.1. These designs typically use slow, high-voltage devices, and therefore operate at a relatively low switching frequency. This generates large volt-seconds upon the filtering elements, which dominate the size of the inverter and limit performance.

Proposed Approach

Multilevel topologies provide an attractive alternative to more traditional 2 or 3-level implementations, because they allow for utilization of devices with lower blocking voltage and correspondingly high figure-of-merit (FOM) [8, 6]. Fig. 2.2 demonstrates that as you move from 650 V devices down to 100 V, your loss metric decreases by more than 10x.

Fig. 2.3 provides a survey of all commercially available inductors and capacitors from the supplier Digikey. It can be seen that the energy density of the best capacitor is more than 1000x higher than that of the best inductor. This motivates the use of hybrid switched capacitor converters, which rely primarily on capacitors for energy storage and reduce the inductive energy storage requirements dramatically compared to conventional switched-inductor type topologies [125, 109].

The flying capacitor multilevel (FCML) converter has demonstrated particular promise due to a number of additional performance benefits [73, 36, 78, 46, 45, 44]. Under phase-

shifted pulse width modulation (PSPWM), it generates a frequency multiplication effect which drastically reduces the volt-seconds applied to the filter inductor [8], as depicted in Fig. 2.4. This, in turn, enables the size of this inductor to be reduced greatly. Additionally, the FCML comprises many small, lower-voltage components so heat generation is distributed across a large surface area, which is advantageous for cooling. Overall, the FCML topology is amenable to high efficiency, high density power conversion.

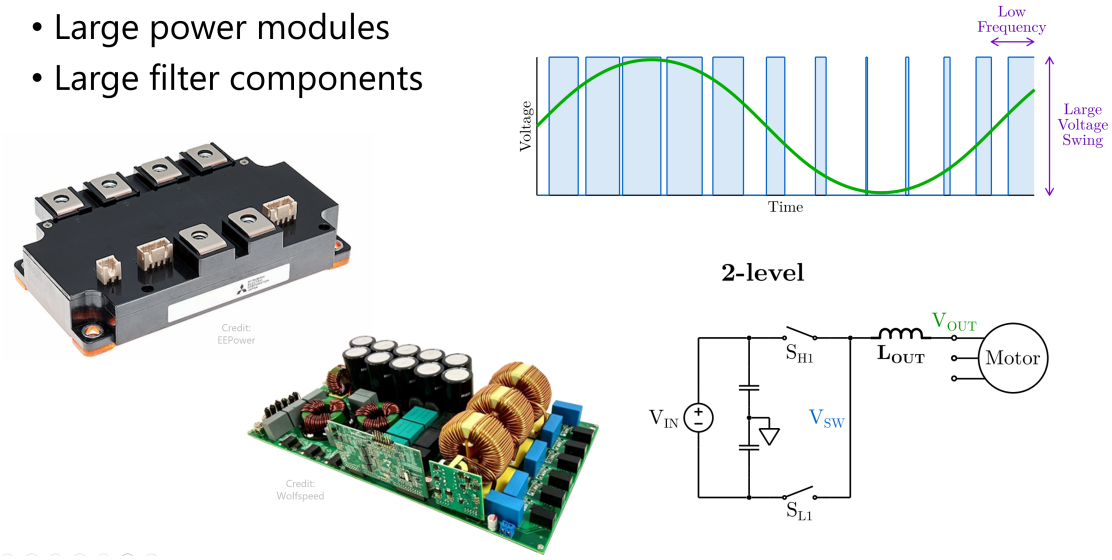


Figure 2.1: Conventional inverter design architectures feature bulky high-voltage devices operating at low switching frequency, which leads to large volt-seconds and bulky passive components.

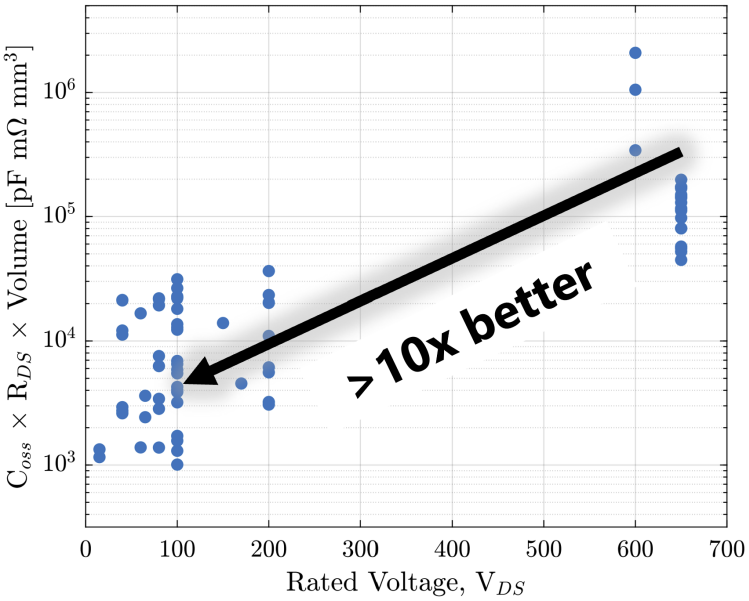


Figure 2.2: Power transistor loss metric (output capacitance multiplied by on-resistance) as a function of blocking voltage. 100 V devices have greater than a 10x reduction in this metric compared to 650 V devices, motivating the use of multi-level converters.

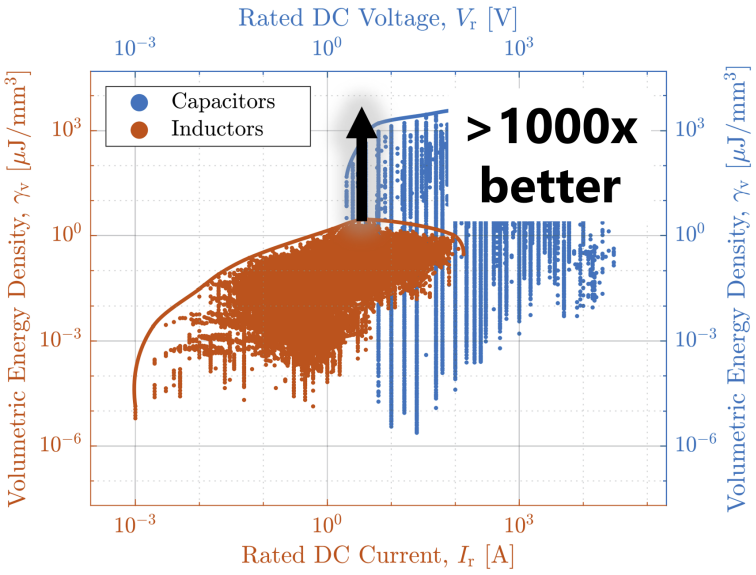


Figure 2.3: Volumetric energy density for commercially available passive components from the supplier Digikey. The best capacitors offer more than 1000x the density of the best inductors, motivating the use of converters relying on capacitive energy storage.

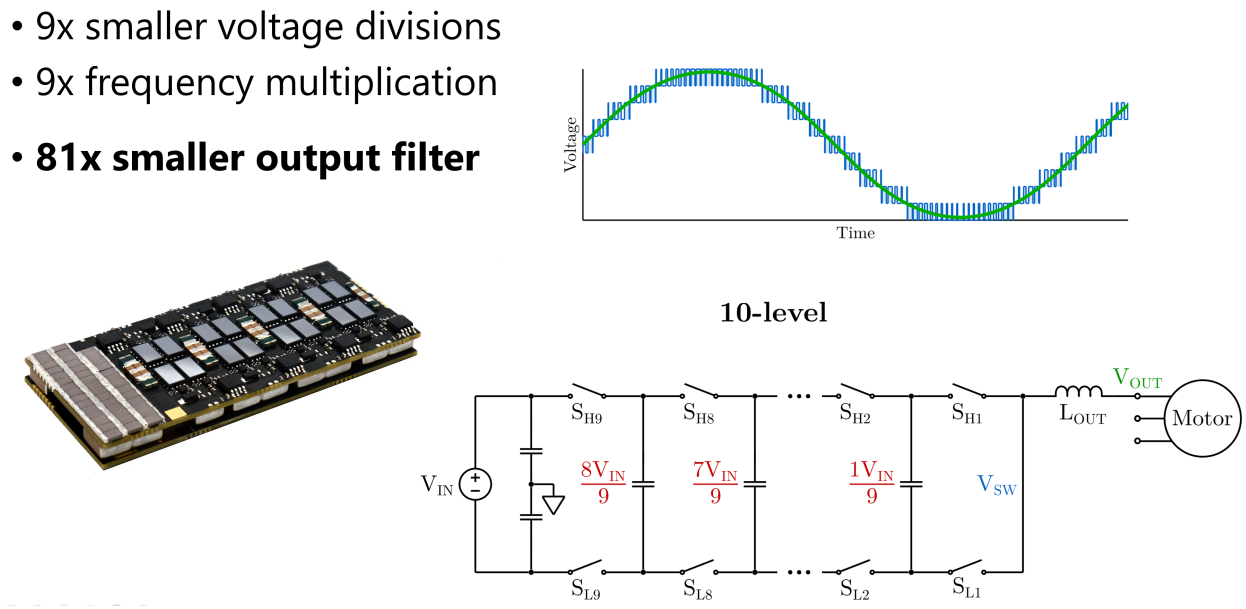


Figure 2.4: Unconventional flying capacitor multilevel (FCML) converter topology. Example 10-level design shown which enables an 81x reduction in output inductor size compared to the 2-level converter.

2.2 Data Center Power Delivery

The modern datacenter power supply architecture is complex, with many cascaded stages to step from the ac grid voltage down to the low operating voltages of CPUs, GPUs and ASICs (shown in Fig. 1.3). Typically, there is an ac to 400 V dc conversion, then conversion to a distribution voltage of 48 V, another conversion to a 12 V bus, and then a final conversion to point-of-load (PoL) [82]. Fig. 1.3a demonstrates this approach, which will be referred to as a three-stage design because of its three separate dc-dc conversion stages. Fig. 1.3b highlights a two-stage design, which is currently gaining popularity, wherein a direct 48 V to PoL conversion occurs [7, 4, 123]. Fig. 1.3c illustrates the proposed single-stage approach [21] proposed here, with direct 400 V to PoL conversion. Multi-stage designs suffer from increased complexity, and also require the use of bus capacitors (C_B) between each stage to ensure that the voltages are held steady. These bus capacitances can be even larger than the converters [122], so eliminating them by performing direct conversion from HVDC to PoL has many benefits for overall system performance.

Novel Topology

To address the challenge of extreme conversion ratio from 400 V to 1 V, we combine two popular power conversion topologies — the flying capacitor multilevel (FCML) converter [74, 62] and LLC converter [67, 23] — to arrive at the proposed flying capacitor LLC (FCLLC) topology, having advantages of each. The FCLLC comprises a step-down switched-capacitor network which resonates with a subsequent transformer-based stage, resulting in complete soft-charging of the flying capacitors [102, 90], galvanic isolation, and an additional step-down through the transformer. As a result of the two inherent cascaded voltage conversions, the FCLLC is especially suited for extreme conversion ratios. Moreover, the use of low-voltage devices improves semiconductor figure-of-merit.

The FCML converter (Fig. 3.9a) has demonstrated impressive performance in a variety of applications [62, 78, 46, 93]. Comparatively, the LLC converter (Fig. 3.9b) and related variants have seen widespread use in both 48 V to PoL and 400 V to 12 V applications [4, 99, 34]). The high-frequency transformer enables a high conversion ratio and provides galvanic isolation to comply with safety considerations, while the resonant operation allows for high switching frequency, and thus small size, while maintaining low losses. The schematic for an FCML is given in Fig. 2.5a, while the LLC is shown in Fig. 2.5b. Conventionally, an LLC consists of a primary-side half-bridge (or full-bridge) which generates a square wave voltage driving a resonant capacitor in series with the primary-side leakage inductance of a transformer. Additionally, a switching stage on the secondary side rectifies and filters the high frequency waveform to dc.

For the FCLLC (Fig. 2.5c), the LLC's primary-side half-bridge and series resonant capacitor are replaced by an N-level FCML stage. This allows for the removal of several components when compared with two independent cascaded FCML and LLC stages (redundant components highlighted in purple in Fig. 2.5). The output filter of the FCML stage

can be completely removed, and the front-end half-bridge and resonant capacitor C_R of the LLC can also be removed. This extends recent work [49], which retains the separate resonant capacitor. In that design, the flying capacitance must be much larger than C_R so that the flying capacitors act as stiff dc voltage sources and do not participate in the resonance. In the proposed work, the flying capacitors themselves are used to resonate with the leakage inductance of the transformer, allowing them to be orders of magnitude smaller than if they have to provide a stiff voltage. Certain states have one capacitor connected in series, while others have two — thus this is a multi-resonant topology with differing resonant frequencies per phase and an associated increase in control complexity. The FCML and LLC stages are fully merged and so is the operation of this new topology.

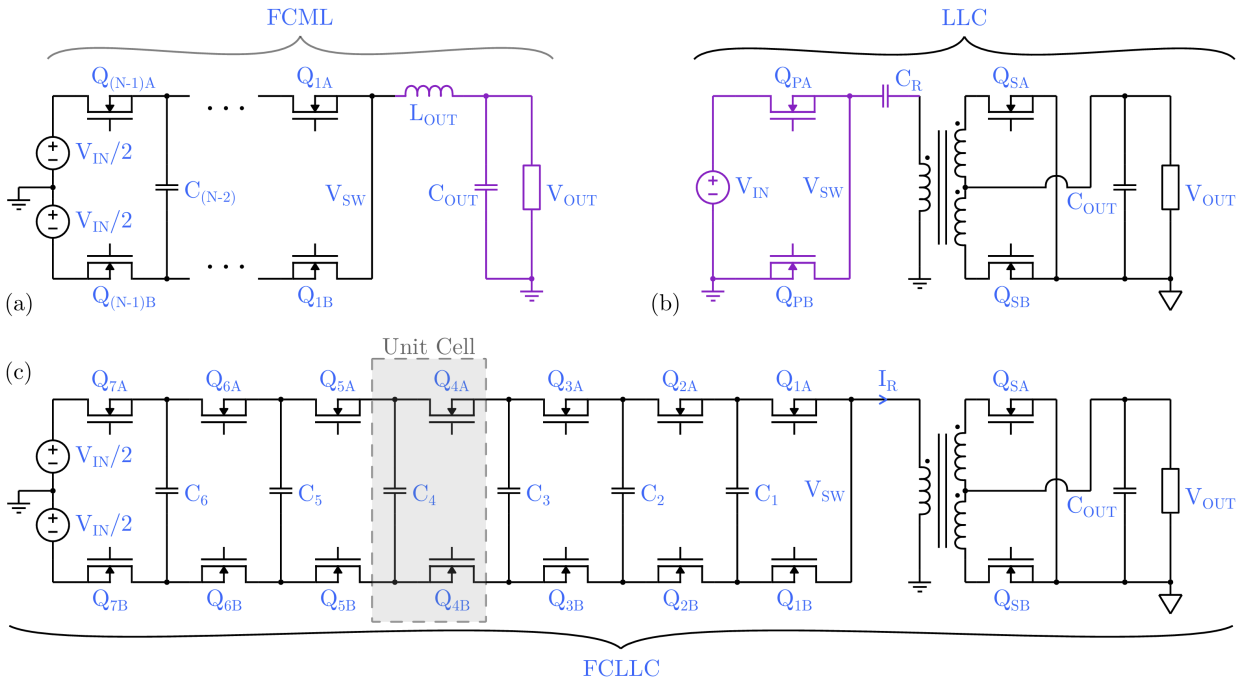


Figure 2.5: Proposed FCLLC topology. (a) Standard FCML, (b) LLC with half-bridge primary, (c) Combined topology with redundant components (highlighted in purple) removed.

Modulation Scheme

For this subsection only, a 4-level FCLLC is discussed to simplify the diagrams and discussion: operation with any other level count can be extended from this description. Prior work has discussed the modulation and multi-ratio capabilities for a resonant FCML (rFCML) converter [57, 15, 2, 25]. Fig. 2.6 shows the equivalent circuit for all 6 states of the switched-capacitor network in a 4-level FCLLC. For the 4-level rFCML, switching states 1, 3, and 5 are all necessary for a 2/3 conversion ratio; and states 2, 4, and 6 are all those necessary for

a 1/3 conversion ratio. During FCLLC operation, these six switching states are interleaved, to provide an ac voltage and current for the transformer primary.

In states 1, 2, 4, and 5, there is a single flying capacitor, C_F, connected in series with the transformer. The duration of these states is $t_1 = \pi\sqrt{L_R C_F}$, where L_R is the leakage inductance of the transformer. In states 3 and 6, there are two flying capacitors connected in series, so these have duration $t_2 = t_1/\sqrt{2}$. The total number of states is $N_S = 4 + 2(N-3)$, with an overall period $T = 4t_1 + 2(N-3)t_2$. Each primary-side switch commutes only once per period with a duty cycle of 50%. Frequency multiplication occurs, such that the resonant frequency seen by the transformer and output rectification is $(N-1)/T$. Relevant modulation, voltage, and current waveforms are illustrated in Fig. 2.7, with every flying capacitor successfully achieving net zero charge balance in a full switching cycle. The conversion ratio of this stage is $M_{\mathrm{FCML}} = 1/(2(N-1))$.

In the LLC stage, the voltage conversion ratio is $M_{\mathrm{LLC}} = \lambda/K$, where K is the turns ratio between the primary and secondary windings, and λ is the frequency-dependent gain of the LLC network. The overall voltage conversion ratio of the FCLLC converter is therefore

$$M_{\mathrm{FCLLC}} = M_{\mathrm{FCML}} \cdot M_{\mathrm{LLC}} = \lambda/(2K(N-1)) \tag{2.1}$$

The FCLLC provides a new degree of freedom and enables the designer to choose how to split the conversion ratio between the level-count of the resonant switched capacitor network and the turn ratio of the transformer.

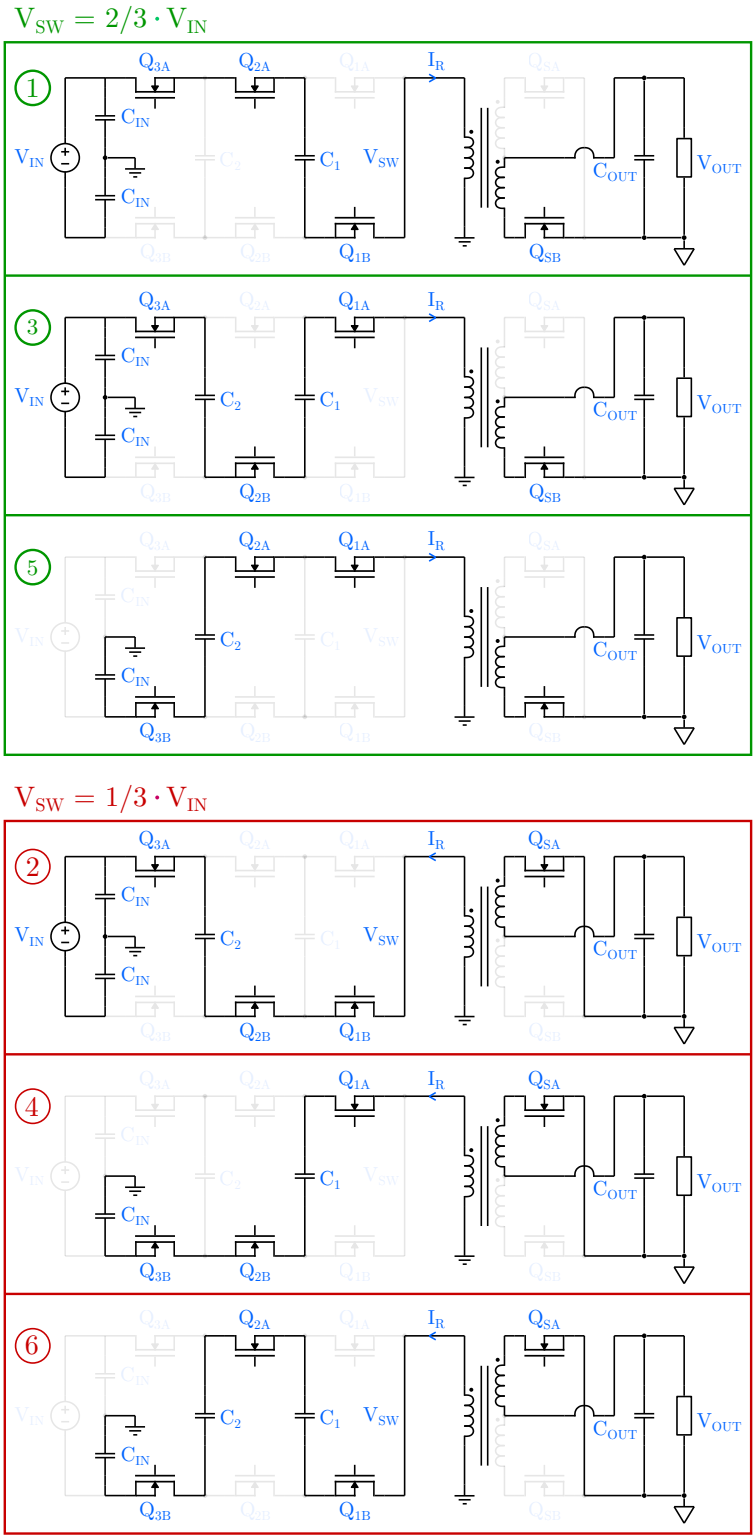


Figure 2.6: Equivalent circuits for each state of a 4-level FCLLC. The set of states with resonant conversion ratios of 2/3 and 1/3 are highlighted in green and red respectively.

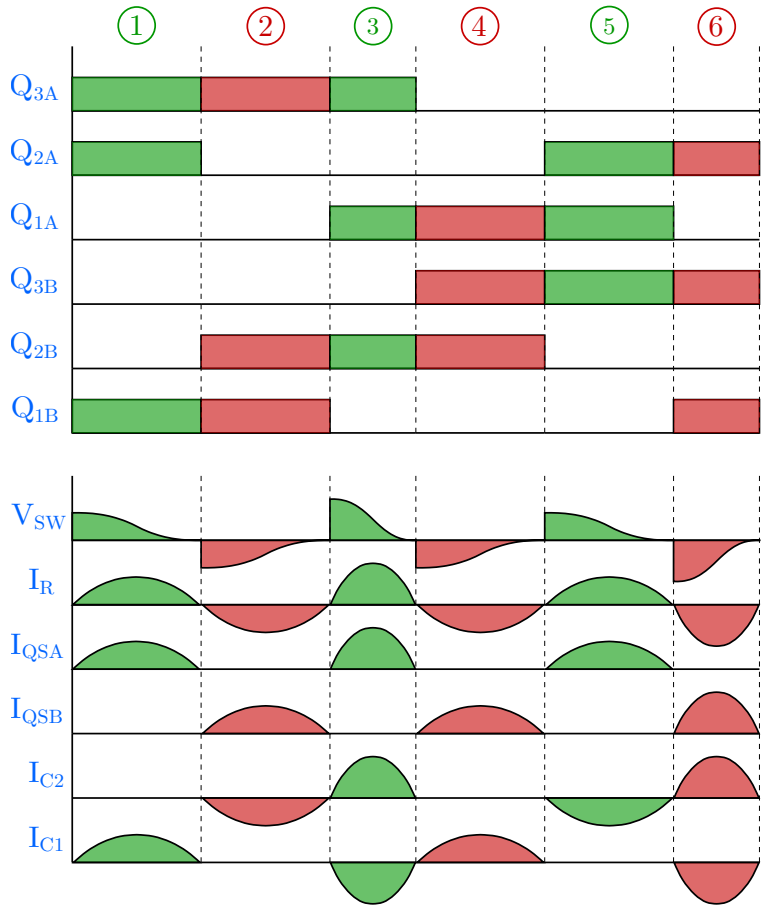


Figure 2.7: Key waveforms of proposed topology demonstrating interleaved states and the resultant frequency multiplication effect.

2.3 Topological Comparison

There are countless power converter topologies, each with different energy storage capabilities, loss mechanisms, switching devices, and control techniques [32, 68, 65]. They can be broadly classified into three different categories: 1) Switched magnetics (SM) converters, which utilize magnetic components (inductors or transformers) to provide all of the energy storage and processing. The buck, boost, and flyback topologies are canonical examples [32]. 2) Switched capacitor (SC) converters, wherein capacitors are solely utilized to provide voltage translation. The series-parallel and Dickson topologies are popular examples [103]. 3) Hybrid converters (HC), in which both capacitors and inductors/transformers are used for energy processing, often resulting in a design that is denser and more efficient than SM or SC alternatives. The Ćuk, SEPIC, flying capacitor multilevel converter (FCML) and LLC are prevalent examples [32, 73, 51]. Hybrid switched capacitor (HSC) converters are a subset of this group, in which one or more inductors are added to an SC topology to provide capacitor soft-charging and potentially regulation [89, 60].

It is difficult, in practice, to compare these disparate topologies on a fair and useful theoretical basis because each comes with different scaling laws, energy storage mechanisms, thermal limits, etc. Therefore, simplified metrics are utilized, which capture certain aspects of a design and serve as a proxy for more detailed, application-specific analysis. One traditional approach for assessing SM converters is to compute the total active switch stress and to normalize this by the output power to achieve an active switch utilization metric (M_{VA}) [32]. This provides a simple way to estimate the relative semiconductor loss and corresponding volume for different topologies. The analysis was extended to incorporate charge sharing losses in SC converters, such that SC and SM converters could now be compared [81, 83, 86, 103, 70]. A complementary metric was developed which evaluates the overall volume of the passive components [60, 119]. These two metrics – one to assess loss (switch stress) and one to predict size (passive volume) – have been widely utilized to compare and characterize HSC topologies.

Existing passive volume metrics (PVMs) have not considered transformers, and in this work it is shown that they do not adequately consider the scaling trends and losses of inductors. An extension is presented here, in which K_g and K_{gfe} methods are utilized for magnetic component sizing. A unified framework is then developed, which enables more accurate comparison of SM, SC, and HC topologies via a modified PVM which includes passive component losses. It is shown that the relative performance of various topologies depends heavily on the output power and switching frequency of the converter.

Limitations of Existing Passive Volume Metrics

There are various PVMs, which are based on differing assumptions [60, 70, 69, 119, 121, 26], but the basic approach is as follows: First, the peak energy stored by each of the passive components is determined and the results are summed.

Table 2.1: Symbol Definitions & Values Used

Symbol	Units	Description	Value
M_{PV}	-	Standard volume metric	-
S_{PVL}	cm^3	Proposed voume metric	-
M_{VA}	-	Switch stress metric	-
P_{out}	W	Output power	-
P_{loss}	W	Power loss	-
γ	-	Loss ratio (P_{loss}/P_{out})	0.05
A_C	cm^2	Core area	-
W_A	cm^2	Winding area	-
MLT	-	Mean length of turn	-
K_g	cm^5	Inductor size metric	-
K_{gfe}	cm^x	Transformer size metric	-
S_L	cm^3	Magnetics size	-
E_L	J	Inductive energy	-
E_C	J	Capacitive energy	-
ρ_L	J/cm^3	Inductor density	-
ρ_C	J/cm^3	Capacitor density	0.2

Symbol	Units	Description	Value
f_{sw}	Hz	Switching frequency	-
D	-	Duty cycle	-
λ	V·s	Primary volt-seconds	-
N	-	Conversion Ratio	-
L	H	Inductance	-
I_{pk}	A	Peak inductor current	-
I_{rms}	A	RMS inductor current	-
I_{tot}	A	RMS winding currents	-
I_{out}	A	Average output current	-
V_{in}	V	Input voltage	-
V_{out}	V	Output voltage	-
ρ	Ω·cm	Winding resistivity	2e-6
B_{pk}	mT	Peak B-field	400
K_u	-	Winding fill factor	0.5
K_{fe}	W/cm^3T	Core loss coefficient	-
β	-	Core loss exponent	2.7

$$E_L = \sum_k \frac{1}{2} L_k I_{pk,k}^2 \tag{2.2}$$

$$E_C = \sum_k \frac{1}{2} C_k V_{pk,k}^2 \tag{2.3}$$

Next, these values are divided by the energy densities of the components.

$$S_L = \frac{E_L}{\rho_L} \tag{2.4}$$

$$S_C = \frac{E_C}{\rho_C} \tag{2.5}$$

The passive energy storage requirements (E_L and E_C) will be proportional to the output power of the converter and inversely proportional to the switching frequency. The final step is to normalize the results such that these parameters cancel out, as shown in (2.6). Table 2.1 defines the symbols used in this work.

$$M_{PV} = \frac{f_{sw}}{P_{out}}(S_L + S_C) \tag{2.6}$$

The resulting equation for M_{PV} depends only on the topology, not on any converter operating parameters such as input voltage, output power, or switching frequency. This approach then allows for general topology comparisons irrespective of application details, but has limited accuracy. Component energy densities (ρ_L and ρ_C) must be estimated, and it is assumed that they are independent of frequency or output power. While this is true for capacitors, both the efficiency and power density of inductors depend on their size and the switching frequency [109, 40]. Moreover, magnetic components have non-negligible winding and core losses which affect converter performance. In contrast, ceramic capacitors offer such low ESR that the conduction losses are often negligible. Even Class II ceramic capacitors, which engender hysteresis losses, can be treated as roughly ideal components if they are not operating with extremely large voltage ripple [72, 71, 19]. For these reasons, the approach proposed in this work involves a modified treatment of magnetic components, but uses the standard energy storage method when considering capacitors.

Existing metrics either focus on pure SC converters [81, 83, 86, 103, 70], estimate passive volume without considering any losses [60, 119, 121, 26], do not include inductor losses [87], or consider only how winding loss scales with inductance [69]. Prior work has not included transformers in quantitative density comparisons, although qualitative analysis has been performed [63]. SC converters may have considerable charge sharing loss [115], which can be included with an output impedance model [103, 70], but additional optimization constraints are required. While inductor energy storage comparison is reasonable between hybrid switched capacitor converters, it is not a sufficient metric to compare inductor size across different families of topologies. Also, the energy storage approach is not suitable for transformers as they ideally do not store energy. As a result, PVMs have primarily been used to compare HSC converters without transformers only.

Improved Magnetic Component Sizing

Introducing K_g & K_{gfe} Methods

The design of magnetic components is multi-dimensional; there are many material options, winding arrangements, and competing constraints. One commonly used technique for the design of inductors is the K_g method (the following equations and discussion are adapted

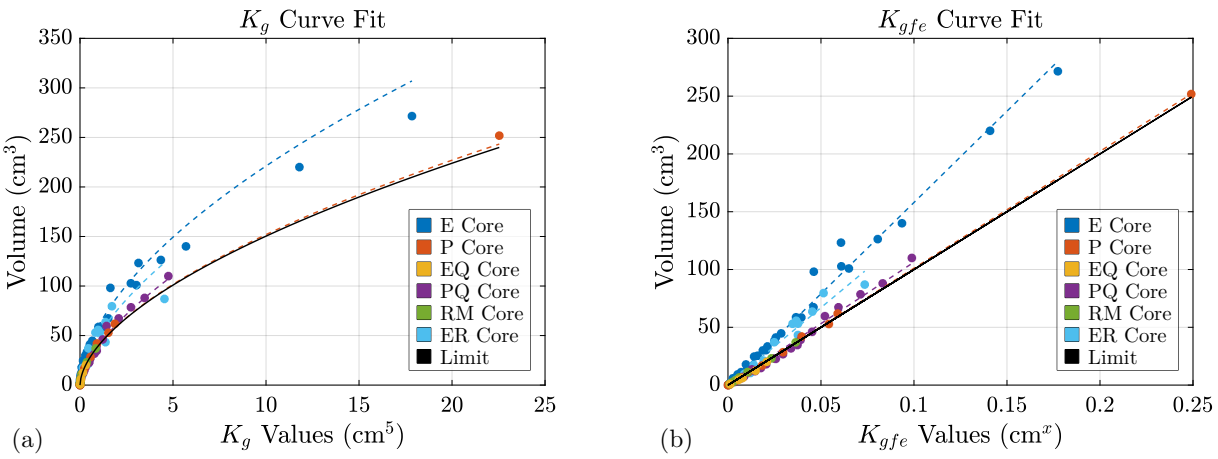


Figure 2.8: Empirical relationship between sizing metrics and box volume of commercially available cores. (a) K_g metric versus volume with limit line in black, (b) K_{gfe} metric versus volume with limit line in black.

Table 2.2: Core Volume vs. K_g

Shape	No.	Best Fit Eq.	r^2
E Core	34	$S_L = 60 \cdot (K_g^C)^{(.5665)}$	.994
P Core	16	$S_L = 40 \cdot (K_g^C)^{(.5795)}$	.999
EQ Core	5	$S_L = 40 \cdot (K_g^C)^{(.6052)}$	.997
PQ Core	19	$S_L = 40 \cdot (K_g^C)^{(.6324)}$	.994
RM Core	8	$S_L = 40 \cdot (K_g^C)^{(.5508)}$	.998
ER Core	18	$S_L = 50 \cdot (K_g^C)^{(.5978)}$	.989
Limit	–	$\mathbf{S_L = 40 \cdot K_g^{(.575)}}$	–

from [32]). This can be applied in situations where core loss is negligible relative to winding loss (e.g. typical power converter filter/energy-storage inductors). A core geometry value is computed, as shown in (2.7).

$$K_g^C = \frac{A_c^2 W_A}{(MLT)} \tag{2.7}$$

The electrical constraints of the inductor can be combined into another value, given in (2.8). The 10^8 factor is included for conversion to cm.

Table 2.3: Core Volume vs. K_{gfe}

Shape	No.	Best Fit Eq.	r^2
E Core	34	$S_T = 1,580 \cdot K_{gfe}^C$	.988
P Core	16	$S_T = 1,010 \cdot K_{gfe}^C$	.999
EQ Core	5	$S_T = 906.0 \cdot K_{gfe}^C$	.989
PQ Core	19	$S_T = 1,060 \cdot K_{gfe}^C$	.993
RM Core	8	$S_T = 1,010 \cdot K_{gfe}^C$	.999
ER Core	18	$S_T = 1,340 \cdot K_{gfe}^C$	.967
Limit	–	$\mathbf{S_T = 1,000 \cdot K_{gfe}}$	–

$$K_g^E = \frac{(10^8)\rho L^2 I_{pk}^2}{B_{pk}^2 R K_u} \tag{2.8}$$

This equation can be rewritten in terms of power loss for the component using the relation $P_{loss} = I_{rms}^2 R$.

$$K_g^E = \frac{\rho L^2 I_{pk}^2 I_{rms}^2}{B_{pk}^2 P_{loss} K_u} \tag{2.9}$$

These two values (K_g^C and K_g^E) can be related to determine the core size requirements of a given application. This can be understood as follows: In order for an inductor to provide inductance L with peak current I_{pk} and winding loss P_{loss}, the core geometry must be large enough to provide space for the windings and avoid saturation. Eq. (2.10) states this mathematically:

$$K_g^C \geq K_g^E \tag{2.10}$$

K_{gfe} is an extension to the K_g method which considers cases where core loss is non-negligible (e.g. typical power converter AC transformers), and optimizes sizing of the component to minimize the sum of winding and core loss. Again, a core geometry value is derived.

$$K_{gfe}^C = \frac{W_A A_C^{2(\beta-1)/\beta}}{(MLT) l_m^{2/\beta}} \left[(\frac{\beta}{2})^{-\frac{\beta}{\beta+2}} + (\frac{\beta}{2})^{\frac{2}{\beta+2}} \right]^{-\frac{\beta+2}{\beta}} \tag{2.11}$$

The electrical constraints are combined into another value,

$$K_{gfe}^{E} = \frac{(10^8)\rho\lambda^2 I_{tot}^2 K_{fe}^{2/\beta}}{4K_u P_{loss}^{(\beta+2)/\beta}} \tag{2.12}$$

These two values (K_{gfe}^{C} and K_{gfe}^{E}) can be related to determine the core size requirement. This can be understood as: A transformer subjected to volt-seconds λ, conducting a total rms winding current of I_{tot}, with core loss coefficients K_{fe} and β, will provide a good balance of core and winding loss if the core geometry is large enough.

$$K_{gfe}^{C} \geq K_{gfe}^{E} \tag{2.13}$$

For all of these equations, some of the parameters depend on winding and core material (ρ, K_u, B_{pk}, K_{fe}, β), while the others can be derived as a function of the output power and switching frequency of the converter, given a certain topology (L, I_{pk}, I_{rms}, I_{tot}, λ).

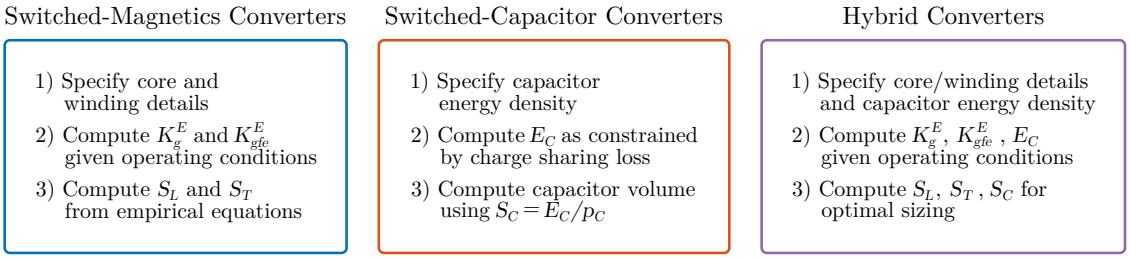


Figure 2.9: Diagram demonstrating the simple three-step process for deriving the proposed passive volume metric, S_{PVL}. The specifications and losses considered depend on the type of topology.

Relating K_g^C & K_{gfe}^C to Volume

To determine a relationship between the core geometry values (K_g^C and K_{gfe}^C) and component volume, 100 different commercial cores of various sizes and shapes were surveyed. Fig. 2.8a plots the box volume for each core as a function of the K_g^C value, while Fig. 2.8b does the same for K_{gfe}^C. A best fit trend-line was found for each core shape, and is plotted with dotted lines. The solid black line is an empirically determined "limit line" which describes the minimum achievable volume for a given K_g^C/K_{gfe}^C value. Equations (2.14) and (2.15) define these limit lines, which are used to compute magnetic component volume in subsequent analysis. Tables 2.2 and 2.3 provide information regarding individual core trends and the extracted limits.

$$S_L = 40 \cdot (K_g^C)^{(0.575)} \tag{2.14}$$

$$S_T = 1000 \cdot (K_{gfe}^C) \tag{2.15}$$

Unified Passive Volume Framework

The aim of this section is to develop a unified PVM which is amenable to comparison of all SM, SC, and HC topologies. In contrast to existing methods, this approach requires P_{out} and f_{sw} to be specified. The results are therefore less general but potentially more accurate, while also providing intuition as to which topologies are better suited towards high power or high frequency applications. The proposed metric, S_{PVL}, defines the size of the passive components while including passive component losses, as shown in (2.16). Here, S_L and S_T are obtained using the K_g and K_{gfe} methods as computed in (2.14) and (2.15), while S_C is obtained by the standard peak energy storage analysis as shown in (2.5).

$$S_{PVL}(f_{sw}, P_{out}) = (S_L + S_T + S_C) \,|\, P_{loss} \tag{2.16}$$

There are 3 steps required for computing this modified PVM— **Step 1:** Define the core material, capacitor technology, and winding specifications. More specifically, the following parameters must be specified: B_{pk}, β, K_{fe}, K_u, ρ, and ρ_C. These can be derived from the datasheets of selected components/materials. **Step 2:** Compute K_g^E for every inductor, K_{gfe}^E for every transformer, and E_C for every capacitor, as a function of P_{out}, P_{loss}, and f_{sw}. These can be determined from topology-dependent specifications. If there are multiple types of passive components, derive the optimal values of each to minimize overall size. **Step 3:** Set $K_g^C = K_g^E$ and $K_{gfe}^C = K_{gfe}^E$. The volume of all inductors and transformers can be computed using (2.14) and (2.15) respectively, while the volume of the capacitors is found using E_C/ρ_C. These results are summed to determine the total volume for the passive components of the converter. Fig. 2.9 illustrates an outline of the approach. The proposed passive volume metric can then be used to compare all types of converter topologies, including 1) switched-magnetics topologies (e.g. the buck converter), 2) pure switched-capacitor topologies (e.g. the series-parallel converter), and 3) hybrid topologies (e.g. the LLC converter), as demonstrated in the following sections.

Switched-Magnetics Topology

Consider a buck converter (Fig. 2.10a) operating in boundary conduction mode (BCM). We begin by calculating K_g^E for the filter inductor at our given operating condition, as defined in (2.9). The terms can be separated into core/winding characteristics and operating parameters.

$$K_g^E = \underbrace{\frac{\rho}{B_{pk}^2 K_u}}_{\text{Core/Winding Info}} \cdot \underbrace{\frac{L^2 I_{pk}^2 I_{rms}^2}{P_{loss}}}_{\text{Operating Parameters}} \tag{2.17}$$

Step 1: In this example, it is assumed that the windings are made of copper, which determines ρ. A somewhat conservative fill factor (K_u) of 0.5 is chosen. A peak B-field, B_{pk}, of 400 mT is chosen based on PC Mn-Zn materials [76]. **Step 2:** For a buck converter

operating in BCM, the peak current (I_{pk}) and the RMS current (I_{rms}) can be written in terms of the average output current.

$$I_{pk,buck} = 2I_{out} \tag{2.18}$$

$$I_{rms,buck} = \frac{2I_{out}}{\sqrt{3}} \tag{2.19}$$

In BCM, the peak current ripple is equal to the average output current. The inductance required for this magnitude of ripple can be computed as:

$$L_{buck} = \frac{(1-D)V_{out}}{2f_{sw}I_{out}} \tag{2.20}$$

By combining these terms and simplifying, (2.17) can be rewritten in terms of P_{out}, the loss ratio γ, and f_{sw}, as in (2.21).

$$K^E_{g,buck} = \frac{(10^8)4\rho(1-D)^2P_{out}}{3\gamma K_u B^2_{pk} f^2_{sw}} \tag{2.21}$$

Step 3: The inductor volume is computed using (2.14):

$$S_{L,buck} = 40 \cdot \left[K^E_{g,buck}\right]^{(0.575)} \tag{2.22}$$

Switched-Capacitor Topology

Next, consider a series-parallel SC converter with all capacitor values equal to some capacitance, C. A 4-1 step-down topology is shown in Fig. 2.10b. **Step 1:** A capacitor energy density (ρ_C) of $0.2\,\mathrm{J/cm^3}$ is chosen based on a high-performance ceramic capacitor operating at half its maximum voltage [112]. **Step 2:** Pure switched capacitor converters exhibit charge sharing losses due to hard charging between capacitors. An effective output impedance, which models these losses, can be calculated from the modulation scheme of the converter [103].

$$R_{out,SP} = \frac{N-1}{4N^2 f_{sw} C} \tag{2.23}$$

The associated power loss is given here.

$$P_{loss} = I^2_{out} R_{out} \tag{2.24}$$

The total energy stored by the capacitors can be computed as well using the standard approach given in (2.3).

$$E_{C,SP} = (N-1) \cdot \frac{1}{2} C V^2_{out} \tag{2.25}$$

These results can be combined to determine the total energy storage in terms of P_{out}, P_{loss} and f_{sw}.

$$E_{C,SP} = \frac{(N-1)^2}{2N^2} \frac{P_{out}}{\gamma_C f_{sw}} \tag{2.26}$$

Step 3: The capacitor volume is found by dividing $E_{C,sp}$ by the component density.

$$S_{C,SP} = \frac{E_{C,sp}}{\rho_C} \tag{2.27}$$

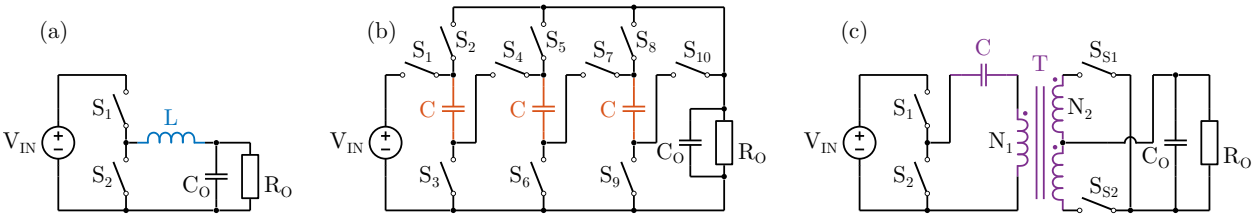


Figure 2.10: Example topologies for comparison. (a) Buck converter, (b) 4-1 series-parallel converter, (c) Half-bridge LLC converter.

Hybrid Topology

Consider a half-bridge LLC converter (Fig. 2.10c), operated at the series resonant frequency. We begin by calculating K_{gfe}^E for the transformer at our given operating condition, as defined in (2.12). The terms can be separated into core/winding characteristics and operating parameters.

$$K_{gfe}^E = \underbrace{\frac{(10^8)\rho K_{fe}^{2/\beta}}{4K_u}}_{\text{Core/Winding Info}} \cdot \underbrace{\frac{\lambda^2 I_{tot}^2}{P_{loss}^{(\beta+2)/\beta}}}_{\text{Operating Parameters}} \tag{2.28}$$

Step 1: Here, we use the same winding parameters and capacitor energy density as the previous examples. The core loss coefficients (K_{fe} and β) are chosen based on PC Mn-Zn materials [76]. **Step 2:** The volt-seconds applied to the primary winding can be identified from the operating waveforms as:

$$\lambda = \frac{V_{in}}{4 f_{sw}} \tag{2.29}$$

The sum of RMS winding currents can also be found by inspection.

$$I_{tot} = \frac{\pi}{2}(2+\sqrt{2}) \frac{P_{out}}{V_{in}} \tag{2.30}$$

With this information, (2.28) can be rewritten in terms of P_{out}, P_{loss} and f_{sw}.

$$K^E_{gfe,LLC} = \frac{(10^8)\rho\pi^2(2+\sqrt{2})^2 K_{fe}^{2/\beta} P_{out}^{(\beta-2)/\beta}}{256 K_u \gamma^{(\beta+2)/\beta} f_{sw}^2} \tag{2.31}$$

There is no charge sharing loss in this converter, as the capacitor and inductor resonate together, but the capacitor size can still be optimized based on energy storage requirements.

$$E_{C,LLC} = \frac{1}{2} C V_{pk,LLC}^2 \tag{2.32}$$

$$V_{pk,LLC} = \frac{V_{in}}{2} + \frac{P_{out}}{2 f_{sw} C V_{in}} \tag{2.33}$$

The derivative of E_C is taken with respect to capacitance to determine the minimal energy storage achievable with optimal capacitor sizing, $E^*_{C,LLC}$.

$$E^*_{C,LLC} = \frac{P_{out}}{2 f_{sw}} \tag{2.34}$$

Step 3: The transformer volume is computed by applying (2.15) to the K_{gfe} value given in (2.31).

$$S_{T,LLC} = 1000 \cdot \left[K^E_{gfe,LLC}\right] \tag{2.35}$$

The capacitor volume is found by dividing $E^*_{C,sp}$ by the component density.

$$S_{C,LLC} = \frac{E^*_{C,LLC}}{\rho_C} \tag{2.36}$$

These values are added together to find the overall passive component size.

$$S_{LLC} = S_{T,LLC} + S_{C,LLC} \tag{2.37}$$

Topology Comparison

To compare how the volume of these topologies scales with output power and switching frequency, Fig. 2.11 provides a plot showing S_{PVL} vs. f_{sw} for each of the three converters. The total passive component loss is held constant across all topologies (at a loss ratio of 0.05 or 95 % efficiency), and the converters are analyzed for a 4-to-1 step-down conversion ratio. The output power, P_{out}, is swept from 100 W to 1 kW, while the switching frequency is swept from 100 kHz to 1 MHz. Table 2.1 lists the fixed values utilized in this analysis. The conditions used for these comparisons are arbitrary, and these examples are simply meant to demonstrate the types of conclusions which can be obtained using the proposed framework, not to draw definitive conclusions about the relative performance of these topologies in general. Examining Fig. 2.11, we find that the BCM buck converter has the largest passive

volume in all cases, while the series-parallel is the smallest at low power levels, but becomes larger than the LLC converter at high output power and switching frequency.

The proposed metric can be utilized in conjunction with switch stress calculations to compare these topologies in terms of both passive volume and semiconductor losses. This provides a more complete view of converter performance. In Fig. 2.12, S_{PVL} vs. M_{VA} is plotted across conversion ratios ranging from 2:1 to 10:1. Here, the switching frequency is fixed at $f_{sw} = 500\,\text{kHz}$ and again the output power, P_{out}, is swept from 100 W to 1 kW. Examining Fig. 2.12, it can be seen that the performance of the LLC varies little with respect to changes in P_{out} and is completely independent of conversion ratio, because the turns ratio can be adjusted without affecting any other operating parameters. In contrast, the total passive volume of the series-parallel is heavily dependent on output power, while the switch stress increases dramatically for larger conversion ratios. The BCM buck converter volume is the largest in all cases, and varies significantly across P_{out}. Its switch stress is strongly dependent on the conversion ratio, N, as well.

These examples highlight the necessity of comparing different types of converters under specific P_{out} and f_{sw} conditions. They also give a theoretical basis for certain empirical topological decisions. For example, the use of pure SC designs is very common in low-power on-chip applications, but nearly absent in higher power discrete converters. When both are implemented as a DCX stage (i.e. with no regulation), the LLC is often denser than a buck converter. It is also well suited to high conversion ratio design.

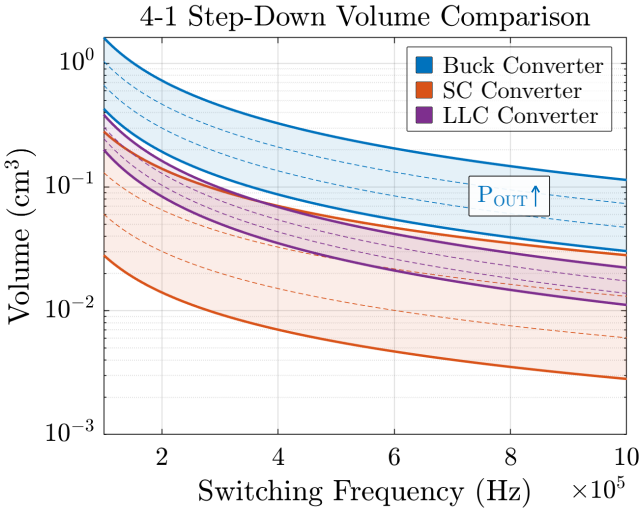


Figure 2.11: Passive volume computed by proposed S_{PVL} metric for three different converters. Plotting volume vs. f_{sw} for a fixed 4-1 step-down conversion with output power swept from 100 W -1 kW.

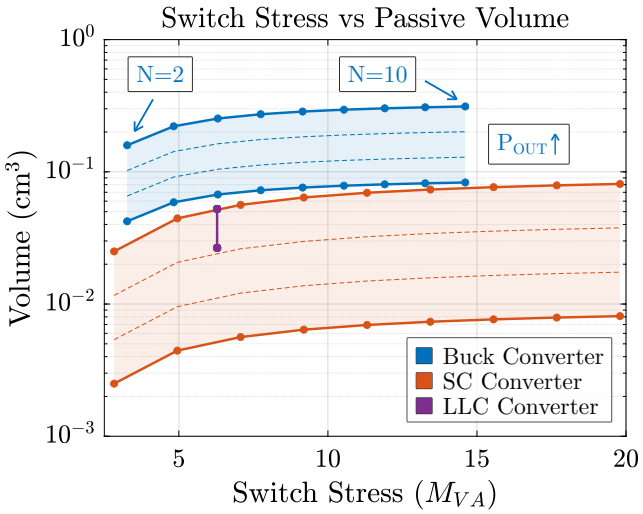


Figure 2.12: Passive volume computed by proposed S_{PVL} metric for three different converters. Plotting volume vs. switch stress across a conversion ratio from 2:1-10:1 for a fixed switching frequency of 500 kHz with output power swept from 100 W -1 kW.

Conclusion

It is important to compare topologies on a theoretical basis to derive initial estimates for which might be best suited to a given application. Switch stress metrics can be applied to all converters, but existing passive volume metrics are mostly applicable to HSC designs. A new PVM is proposed here, which utilizes K_g and K_{gfe} methods for magnetic component sizing, thus enabling inclusion of passive component losses. This allows for comparison of all types of topologies. Combining the proposed metric with switch stress analysis provides a more complete view of topology performance.

Chapter 3

Parameter Optimization

3.1 Commutation Loop Inductance

The switching speed of power transistors has increased dramatically in recent years, due in large part to improvements in packaging as well as the proliferation of commercial wide-bandgap devices, such as gallium-nitride high-electron-mobility transistors (GaN HEMTs) [79, 64, 75]. With reduced on-resistance, lower output capacitance, and minimal package inductance, especially for flip-chip and BGA packages, these switches are capable of extremely high dv/dt transitions. As such, converter performance is now greatly determined by PCB layout.

The switching cell of a buck converter provides a canonical example, as shown in Fig. 3.1. When the converter is in state 1, the input capacitor and high-side switch, C_{IN} and Q_{HS}, carry the load current. When the converter is in state 2, the low-side switch, Q_{LS}, carries this current. These components see a step-change in operating current upon state transitions and therefore define the commutation loop.

Parasitics arising from the routing of this commutation loop must be minimized to take full advantage of high switching speed [95, 94, 85, 110]. Commutation loop inductance can be detrimental in multiple ways. If the devices are switched quickly, energy stored in the current flowing through this inductance will be rapidly transferred to the C_{OSS} of the off-state device. This leads to over-voltage, as well as electromagnetic interference from the resultant high-frequency ringing [11]. If this behavior is mitigated by slowing the switching transition (e.g., by increasing the gate resistance), converter performance will suffer due to increased overlap loss.

Although these parasitic inductances in switching loops significantly affect operation and performance, their impact is often difficult to estimate at the design stage. At the same time, performance metrics of power converters are tightly coupled, requiring an understanding of trade-offs associated with operating parameters, such as switching speed, and physical constraints imposed by the hardware implementation of the converter. As a result, multi-objective optimization programs have become popular [59, 13, 77].

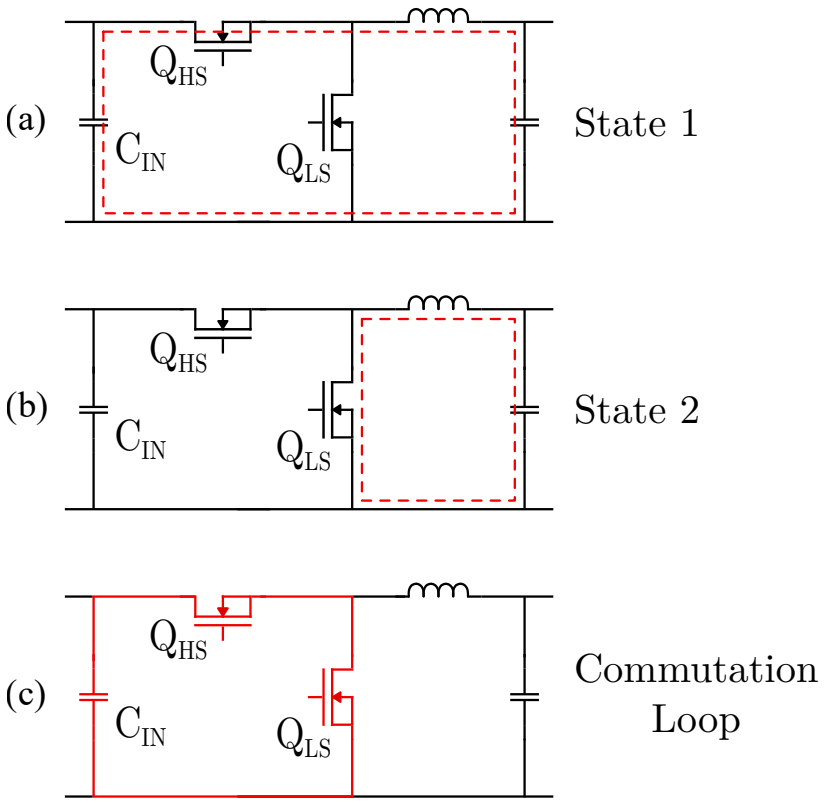


Figure 3.1: Highlighting the commutation loop for a buck converter (a) Current path when Q_{HS} is on, (b) Current path when Q_{LS} is on, (c) Components with step-change in conducted current upon state transition.

In this work, we present a new technique which utilizes partial inductances [88] and linear algebra to evaluate commutation loop inductance. The proposed technique is efficient and platform-independent, to facilitate integration within existing converter design and analysis scripts. This allows for rapid iteration and fast parametric sweeps of loop geometries. Users can therefore optimize a design before fabrication, and develop more accurate predictions of converter performance. Existing simulation/modeling tools are either highly detailed finite element analysis (FEA) that require a full electrical design to simulate (e.g., Ansys Q3D), or are intended for general purpose use (e.g., FastHenry [56]) or the design of semiconductor power modules [33]. These tools also require the use of a specialized software package. This represents a barrier towards integrating accurate commutation loop considerations as part of the design process.

Analytical Framework

Segmentation

A segmentation process approximates the loop into straight segments and divides them at each corner or turn. This greatly simplifies the calculations as current paths become either parallel segments, which influence each other magnetically according to known formulas [42, 38], or perpendicular segments, whose interaction is ignored. This approach is especially suited for PCB commutation loops, where conductors are either horizontal planes or vertical vias. Moreover, component and trace spacing is typically limited by either the rectangular package dimensions or by creepage/clearance limitations between conductors. As a result, diagonal current flow in-plane is often negligible, and the perpendicular approximation is sufficient.

Next, each segment is labeled with a starting and ending node. Mesh and nodal analysis are used to determine the overall circuit schematic. As such, the proposed technique can be employed to study commutation loops containing an arbitrary number of parallel or series current paths without requiring further specification. This functionality is particularly applicable to cases with paralleled capacitors, paralleled switches, or other programming studies. The netlist derived at this stage is stored in binary matrices defined by the relations in (3.1) and (3.2).

$$\mathbf{0} = \mathbf{C}_N\mathbf{I} \qquad (3.1) \qquad\qquad \mathbf{0} = \mathbf{C}_M\mathbf{V} \qquad (3.2)$$

Here, $\mathbf{C}_N$ represents the nodal matrix indicating that the current flow out of every node equals zero. Similarly, $\mathbf{C}_M$ is the mesh matrix indicating that the voltage drop around every loop equals zero.

Meshing

At high frequency, the magnitude of current density through a conductor is highly position-dependent due to skin and proximity effects [58]. These effects cause nearly all of the current to flow at the edges of the conductor. To account for this, a meshing stage further divides each loop segment into sub-segments along the length of the conductor. To limit model complexity, the proposed approach utilizes a meshing technique for which the number of sub-segments is independent of frequency; Fig. 3.2 shows how only the edge of the conductor is divided into a uniform grid of skin-depth (δ) thick sub-segments, while the inner portion remains lumped together. As the frequency increases, the width of the outer sub-segments simply become thinner. Compared to fully meshing the conductor, the number of sub-segments can be reduced greatly, while the edges of the conductor are always measured with high fidelity.

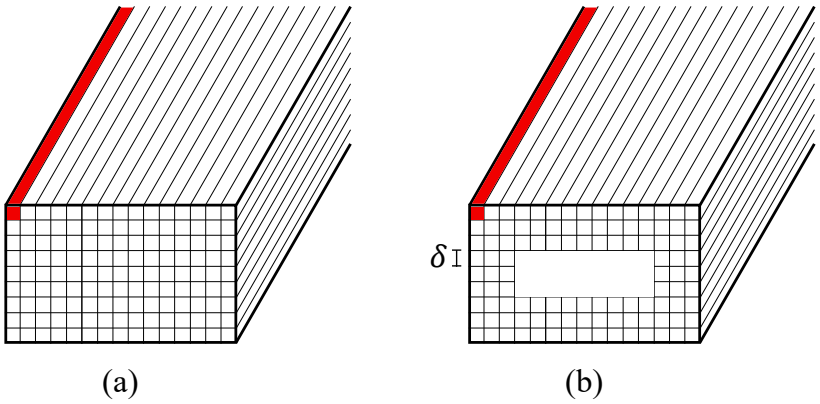


Figure 3.2: Illustration of meshing with one sub-segment highlighted. (a) Uniform grid, (b) Proposed mesh with reduced number of sub-segments covering outer 3 skin depths.

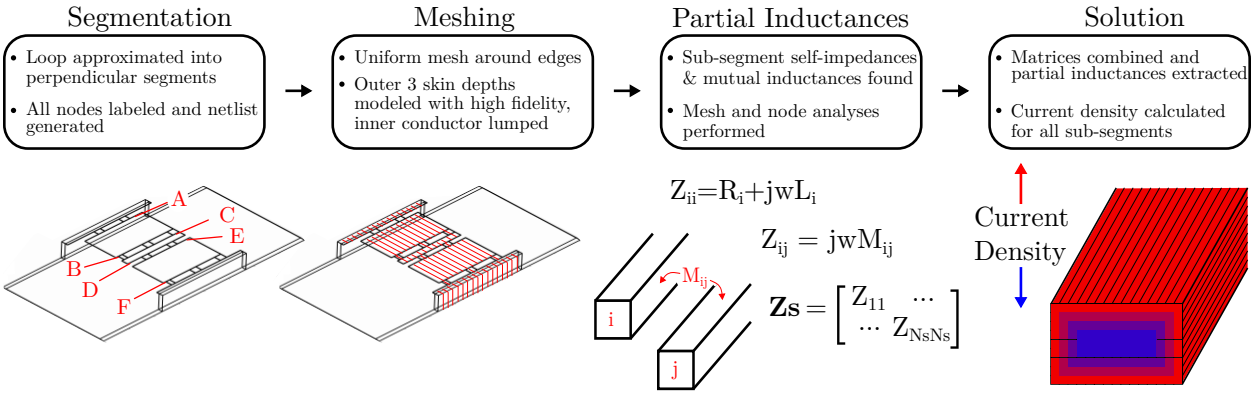


Figure 3.3: Summary of proposed analytical approach.

Partial Inductances

While closed-form approximations for the DC inductance of simple loops have been derived [96], precisely computing the high-frequency inductance of typical commutation loops is not practical. Even for simple geometries, combining the inverse quadratic magnetic field equation with exponential current densities makes the problem intractable. Therefore, the proposed analytical technique extends prior work on partial inductance modeling [96, 97, 98]. With the segmentation and netlist previously defined, the resulting problem can be written concisely as (3.3).

$$V_i = I_i(R_i + jwL_i + jw\sum_j M_{i,j}) \tag{3.3}$$

Here, V_i, and I_i are the voltage across and current through the ith sub-segment. R_i and

jwL_i are the self-impedance of this sub-segment; and $M_{i,j}$ is the mutual inductance between sub-segments i and j.

Considering all of the sub-segments of the loop, (3.3) can be extended to matrix form, as shown in (3.4).

$$\underbrace{\begin{bmatrix} V_1 \\ \vdots \\ V_{N_S} \end{bmatrix}}_{\text{Vs}} = \underbrace{\begin{bmatrix} Z_{1,1} & \dots & Z_{1,N_S} \\ \vdots & Z_{i,j} & \vdots \\ Z_{N_S,1} & \dots & Z_{N_S,N_S} \end{bmatrix}}_{\text{Zs}} \underbrace{\begin{bmatrix} I_1 \\ \vdots \\ I_{N_S} \end{bmatrix}}_{\text{Is}} \tag{3.4}$$

Here, N_S is the total number of sub-segments. On the diagonals, $Z_{i,i} = R_i + jwL_i$ and for the off-diagonals, $Z_{i,j} = jw\sum M_{i,j}$. Equation (3.4) can be rewritten with admittance and simplified by noting that the voltage drop across every sub-segment within the same segment is identical. Therefore, the admittances of all the sub-segments in a segment can be summed, the sub-segment currents can be summed, and the matrix can be written in terms of segments instead of sub-segments.

$$\underbrace{\begin{bmatrix} I_1 \\ \vdots \\ I_N \end{bmatrix}}_{\text{I}} = \underbrace{\begin{bmatrix} Y_{1,1} & \dots & Y_{1,N} \\ \vdots & Y_{p,q} & \vdots \\ Y_{N,1} & \dots & Y_{N,N} \end{bmatrix}}_{\text{Y}} \underbrace{\begin{bmatrix} V_1 \\ \vdots \\ V_N \end{bmatrix}}_{\text{V}} \tag{3.5}$$

Here, N is the number of segments. I_p is the current through segment p; V_q is the voltage across segment q; and $Y_{p,q}$ is the admittance between segments p and q, found by summing the admittances between all of their sub-segments.

At frequencies of interest (determined by the slew rate of the switch transition, e.g. 100 MHz for WBG devices), δ widths are on the order of microns, while segments may have lengths which are many orders of magnitude larger. This vast range of scales makes most mutual inductance formulas numerically unstable–or at the very least inaccurate. Correspondingly, the proposed implementation selects an appropriate formula to calculate mutual inductance based on the geometry for each pair of sub-segments. For example, if the thickness of the conductor is much smaller than the length and width, it can be approximated as a surface as opposed to a rectangular prism.

Solution

The solution to the loop inductance problem can be found by combining (3.1), (3.2) and (3.5) into (3.6).

$$\mathbf{0} = \begin{bmatrix} \mathbf{C}_N\mathbf{Y} \\ \mathbf{C}_M \end{bmatrix} \mathbf{V} \tag{3.6}$$

Without loss of generality, the current through the loop is chosen to be 1 A, such that the voltage across each segment represents its impedance. This equation is then solved for $\mathbf{V}$ using this constraint. Given that the entries in $\mathbf{V}$ correspond to the impedance of each segment, the overall loop inductance may be computed as the sum of the imaginary components, which is shown in (3.7), where f is the frequency.

$$L = \frac{\mathrm{Im}\{\sum_{q=1}^{N} V_q\}}{2\pi f} \tag{3.7}$$

The current through each sub-segment is computed as well by dividing the segment voltages, V_q, by the impedance of each sub-segment (from $\mathbf{Z}_S$) within that segment. Fig. 3.3 summarizes the process of the proposed technique.

Experimental Validation

To investigate the accuracy of the proposed technique and develop a high-precision methodology for experimental verification, two versions of a characterization PCB were fabricated each with four different types of half-bridge switching cell layouts (utilized in e.g., a buck or boost converter), and a flying capacitor multilevel (FCML) cell. These layouts were designed in lateral, lateral with ground plane beneath, hybrid, and vertical topologies [110, 94], which represent common approaches to commutation loop routing, and are illustrated in Fig. 3.4.

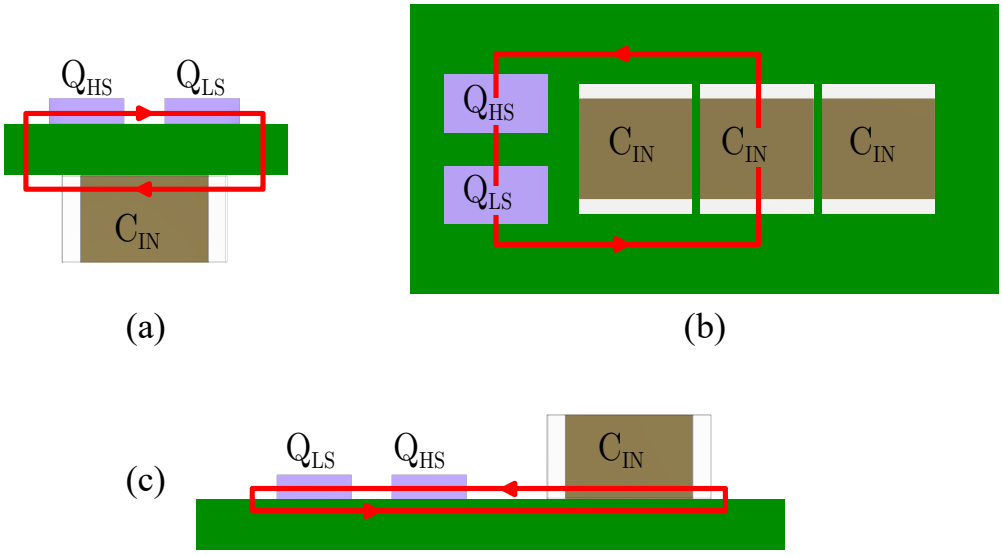


Figure 3.4: Typical half-bridge switching cell designs with path of current flow highlighted. (a) Vertical layout, (b) Lateral layout, (c) Hybrid layout.

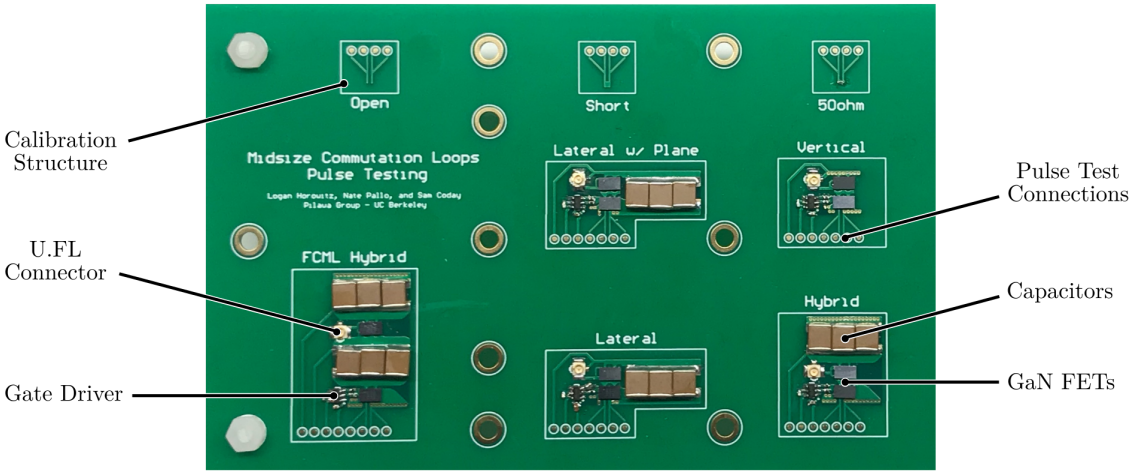


Figure 3.5: Pulse testing PCB with various switching cell designs and calibration structures.

To highlight applications in high-power-density designs, each assembled circuit utilized EPC2034C [29] BGA switches and high-energy-density surface-mount ceramic capacitors. One PCB version was designed for precise measurements using an impedance analyzer, with the capacitors and high-side switch pads shorted to capture only the impedance imposed by the PCB routing. The second PCB was designed for pulse testing, with all components populated, as shown in Fig. 3.5.

The aforementioned analytical methodology was implemented as a MATLAB script, but is not reliant on any specific capabilities of the program, and could thus be implemented in Python or other programming languages. The bulk of computation time goes into calculating the mutual inductances for the impedance matrix in (3.4). For each of the loop designs on the characterization PCB, the overall inductance was computed at various frequencies with this program. To measure the loop inductances with FEA software, the copper from the layouts was extracted and the AC inductance across frequency was computed in Q3D for each loop. For both of these programs, the components are modeled as thin copper shorts.

Next, a Keysight E4990A impedance analyzer was used with 42941A probe to measure the inductance of each loop. Calibration structures were placed on the PCB, as shown in Fig. 3.5, to provide a short, open, and 50Ω reference load with the exact same preceding connections as for the loops themselves. The board is held in a vise, and the probe is similarly held by a clamp at fixed height. The impedance measurement is taken at 100 MHz, which is a sufficiently high frequency to measure the small reactance reliably [24].

Finally, the inductance was also estimated by measuring the ringing frequency of the drain-to-source voltage of the high-side transistor during a switching transition. A new 'single pulse test' circuit was used to generate this transition, as shown in Fig. 3.6. As opposed to a double pulse test, the large inductance is replaced by a resistance, and there is no need for a large decoupling capacitance. Only a single voltage measurement is taken. Other

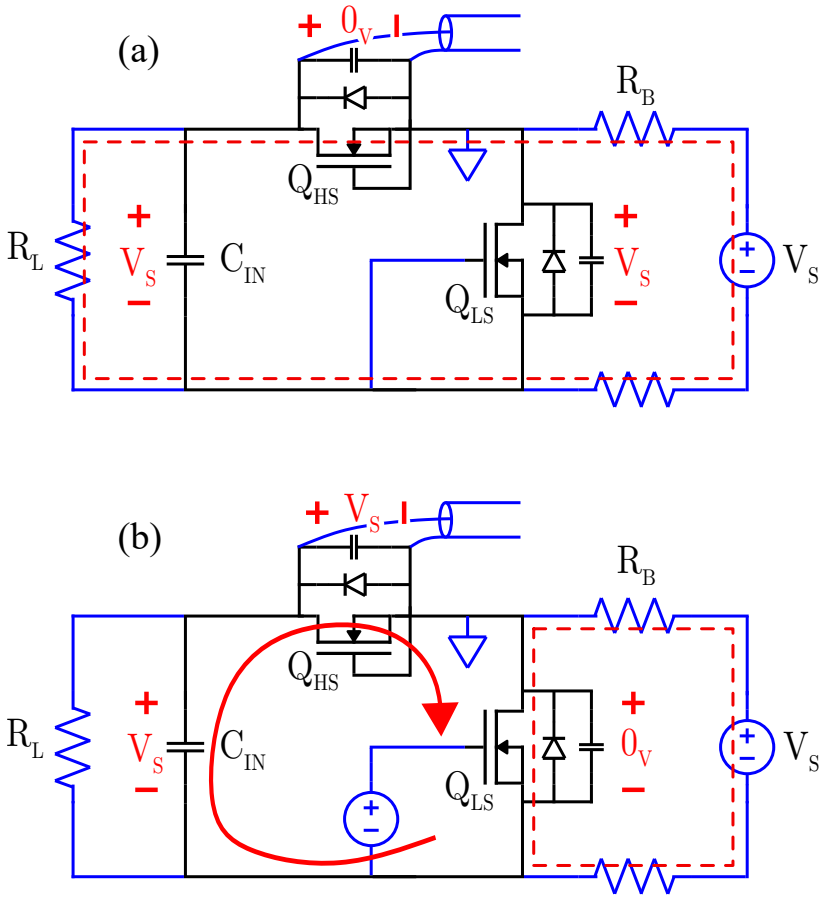


Figure 3.6: Single pulse test circuit. The switching cell is shown in black, and connections to the circuit are shown in blue. Red lines indicate current flow for each state. (a) Q_{LS} is initally off and the measured voltage is zero, (b) Q_{LS} turns on and the V_{DS} of the high-side transistor rises to V_S with some overshoot and ringing.

information about switching losses or voltage overshoot under realistic operating conditions cannot be extracted from this setup. The functionality is as follows.

1) Initially, Q_{LS} is off, and a small current flows from the supply through R_B, R_L, and the body-diode of Q_{HS} (or, as in the case of GaN transistors used here, reverse conduction). As such, the output capacitance (C_{OSS}) of Q_{LS} is charged up to the supply voltage and the V_{DS} of Q_{HS} is zero.

2) Then, Q_{LS} is turned on, forcing its V_{DS} to zero. The C_{OSS} of the high-side transistor must then charge to the supply voltage. The resistors are chosen to have high impedance compared to C_{IN}, ensuring that the high-side transistor C_{OSS} is charged from C_{IN}. The parasitic inductance of this loop and C_{OSS} of the high-side transistor provide the only non-negligible series impedances, such that they determine the amplitude and frequency of the voltage overshoot.

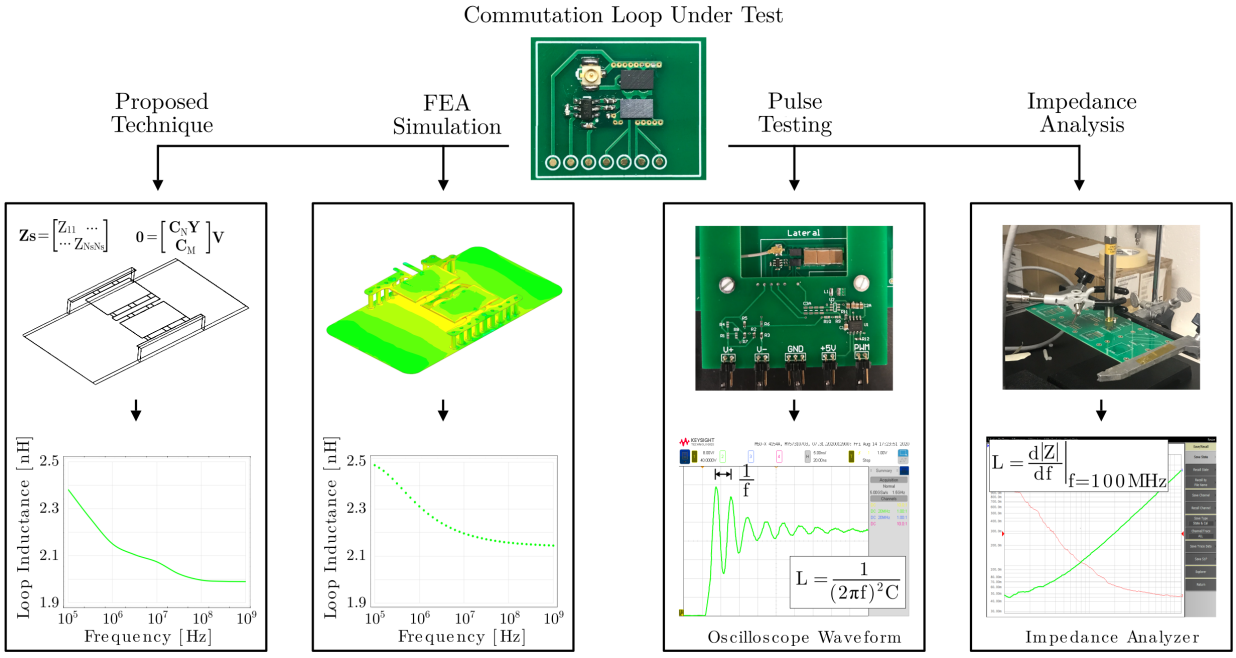


Figure 3.7: Flow diagram illustrating various measurement techniques.

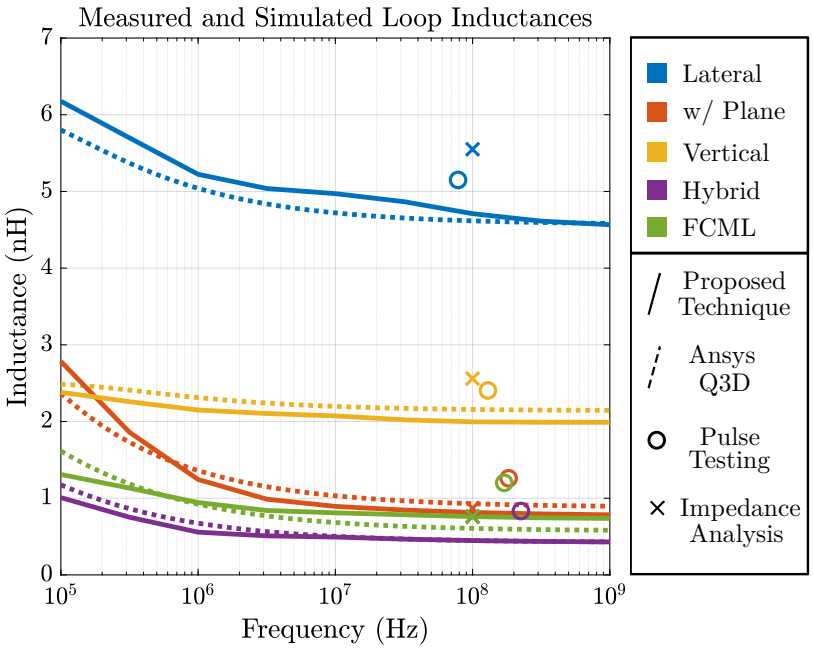


Figure 3.8: Inductance across frequency for each of the loops.

Table 3.1: Measured and Simulated Commutation Loop Inductance at 100 MHz

Loop Type	Proposed Technique	FEA Simulation	Pulse Testing	Impedance Analysis
Lateral	4.71 nH	4.62 nH	5.15 nH	5.55 nH
Lateral w/ Plane	0.81 nH	0.93 nH	1.26 nH	0.87 nH
Vertical	2.00 nH	2.16 nH	2.41 nH	2.56 nH
Hybrid	0.45 nH	0.45 nH	0.83 nH	0.76 nH
FCML Hybrid	0.58 nH	0.60 nH	1.20 nH	0.79 nH

3) The ringing frequency in the voltage measurement is extracted and the value of C_{OSS} at the blocking voltage in the experiment is obtained from the device datasheet. From there, the inductance value can be computed as $L = 1/(2\pi f)^2 C$.

To ensure a reliable voltage measurement for this high-frequency waveform, a 1.5 GHz, 5 GSa/s, Keysight InfiniiVision MSOX4154A oscilloscope is used with 750 MHz N2894A passive probe. The connection is made with a uFL connector placed very close to the loop, which is run with a coax cable directly to a uFL-to-probe-tip adapter. All of the other connections to the switching cell do not affect the measurement, and can be made with high-inductance paths. This 'single pulse test' extends prior work, providing a new half-bridge version of the design for FCML switching cells by [85].

A summary of these measurement techniques is shown in Fig. 3.7. The corresponding results are shown in Fig. 3.8. Table 3.1 summarizes the results at 100 MHz. The estimated inductance values by the proposed program were within 20% of FEA in all cases. The error is likely attributable to the approximation of each loop into straight, perpendicular segments, and discrete meshing of the conductors. The measured results show good agreement with simulation.

Conclusion

A computationally efficient approach for estimating commutation loop inductance is presented here. Based on partial inductances, it is platform-independent and may be scripted into existing converter design and analysis programs. In addition, the effect of design choices such as stackup or component selection can be analyzed before fabrication. The mathematical technique is described and an implementation is created in MATLAB. The accuracy of the proposed method is compared to a commercial FEA simulation tool as well as measurements on multiple hardware prototypes. The results show reasonable accuracy, within 20% of FEA across all frequencies and commutation loop designs, and agreeing with hardware measurements.

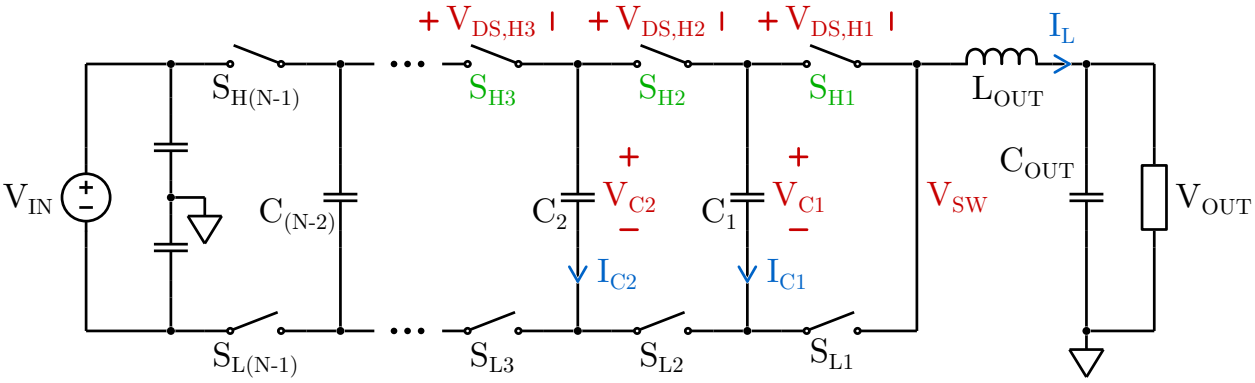


Figure 3.9: Simplified schematic for an N-level FCML.

3.2 Loss Modeling

To accurately predict the theoretical performance of a given converter, precise loss modeling is essential. In an FCML converter, the blocking voltages of the switches depend on the voltages across the flying capacitors. To improve power density, the size of these capacitors must be minimized, which inherently results in larger voltage ripple. Additionally, the flying capacitor voltages vary throughout each switching cycle, leading to significant differences in the blocking voltage at switch turn-on and turn-off. In inverter applications, this effect is further compounded by variations in load current over the ac cycle, which also influence capacitor voltage ripple.

To capture all of these dynamics, an improved loss model is proposed. For an N-level FCML, the switches nominally block:

$$V_{NOM} = \frac{V_{IN}}{N-1} \tag{3.8}$$

In the ideal case, called "balanced operation", each capacitor blocks successively higher fractions of the input voltage.

$$V_{Cx} = \frac{xV_{IN}}{N-1} \tag{3.9}$$

Fig. 3.9 presents the simplified schematic of an N-level FCML with relevant signals highlighted. Fig. 3.10 plots operating waveforms for this converter performing dc-dc conversion using PSPWM. The flying capacitor currents are shown (I_{C1} and I_{C2}) with clear charging and discharging phases during each switching period. Charge accumulates on the capacitors during these cycles which causes the voltages (V_{C1} and V_{C2}) to deviate from the nominal values in (3.9). This changes the drain-to-source voltages across the devices ($V_{DS,H1}$ - $V_{DS,H3}$) and therefore affects the switching loss calculations. We begin with fixed parameters for the input voltage (V_{IN}), output voltage (V_{OUT}), and average output current (I_{OUT}). Under dc-dc conversion, the duty cycles for all of the high-side transistors (D_H) will be identical.

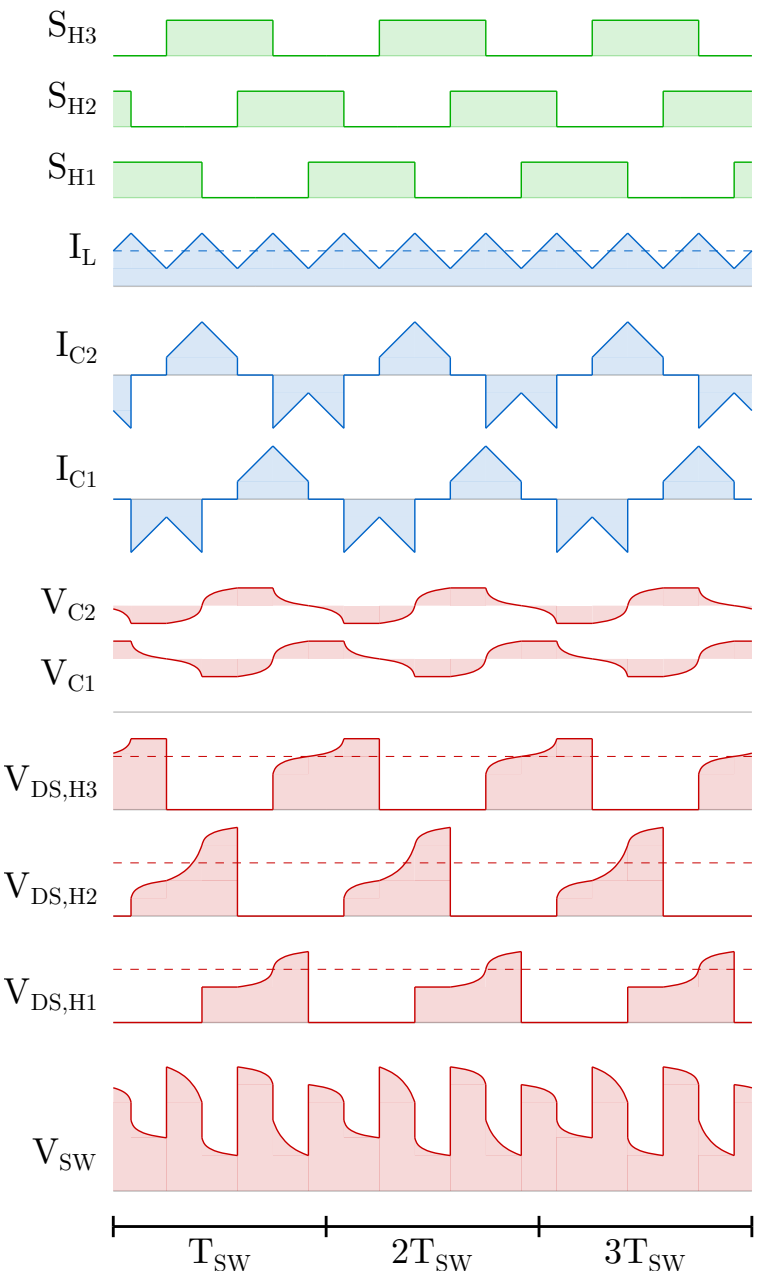


Figure 3.10: Key waveforms for a 4-level FCML during dc-dc operation demonstrating the impact of flying capacitor voltage ripple on switch blocking voltages. Gate signals are shown in green, currents in blue, and voltages in red.

$$D_H = V_{OUT}/V_{IN} \tag{3.10}$$

Each low-side transistor has a complementary gate drive signal to its high-side counterpart. These modulation signals determine the duration of flying capacitor charge/discharge intervals, T_C [8].

$$\begin{aligned} \text{If } D_H < \frac{1}{N-1}: &\quad T_C = D_H T_{SW} \\ \text{If } \frac{1}{N-1} \leq D_H \leq \frac{N-2}{N-1}: &\quad T_C = \frac{T_{SW}}{N-1} \\ \text{If } \frac{N-2}{N-1} < D_H: &\quad T_C = (1-D_H)T_{SW} \end{aligned} \tag{3.11}$$

Here, $T_{SW} = 1/f_{SW}$ is the duration of the switching period. We can now determine the voltage ripple on each flying capacitor due to the conducted current, as modulated by the duty cycle signals. All of the flying capacitors will have an identical quantity of charge added/removed each period, but the capacitance values can differ.

$$\begin{aligned} \text{If } D_H < \frac{1}{N-1}: &\quad Q_C = D_H I_{OUT} T_{SW} \\ \text{If } \frac{1}{N-1} \leq D_H \leq \frac{N-2}{N-1}: &\quad Q_C = \frac{I_{OUT} T_{SW}}{N-1} \\ \text{If } \frac{N-2}{N-1} < D_H: &\quad Q_C = (1-D_H) I_{OUT} T_{SW} \end{aligned} \tag{3.12}$$

$$\Delta V_{Cx} = \frac{Q_C}{2C_x} \tag{3.13}$$

Finally, we can determine the voltage blocked by each transistor during its relevant switching transitions. Device S_{Hx} blocks the difference in neighboring capacitor voltages, $V_{Cx} - V_{C(x-1)}$. When flying capacitor voltage ripple is included, this value varies during the switching period. During the high-side turn-on transition, it is at its maximum:

$$\begin{aligned} \text{If } x = 1: &\quad V_{ON,Hx} = V_{NOM} + \Delta V_{C1} \\ \text{If } x = N-1: &\quad V_{ON,Hx} = V_{NOM} + \Delta V_{C(N-2)} \\ \text{Else}: &\quad V_{ON,Hx} = V_{NOM} + \Delta V_{Cx} + \Delta V_{C(x-1)} \end{aligned} \tag{3.14}$$

Assuming that the input voltage is a stiff DC bus, the first and last devices (Q_{H1} and $Q_{H(N-1)}$) only have one flying capacitor connected across them. The rest of the devices have flying capacitors on both sides, however, so they must block a higher voltage when accounting for ripple. During the high-side turn-off transition, the blocking voltage is at a minimum:

$$\begin{aligned} \text{If } x = 1: \quad & V_{OFF,Hx} = V_{NOM} - \Delta V_{C1} \\ \text{If } x = N-1: \quad & V_{OFF,Hx} = V_{NOM} - \Delta V_{C(N-2)} \\ \text{Else}: \quad & V_{OFF,Hx} = V_{NOM} - \Delta V_{Cx} - \Delta V_{C(x-1)} \end{aligned} \tag{3.15}$$

These results are then used for switching loss calculations in the multi-objective optimization.

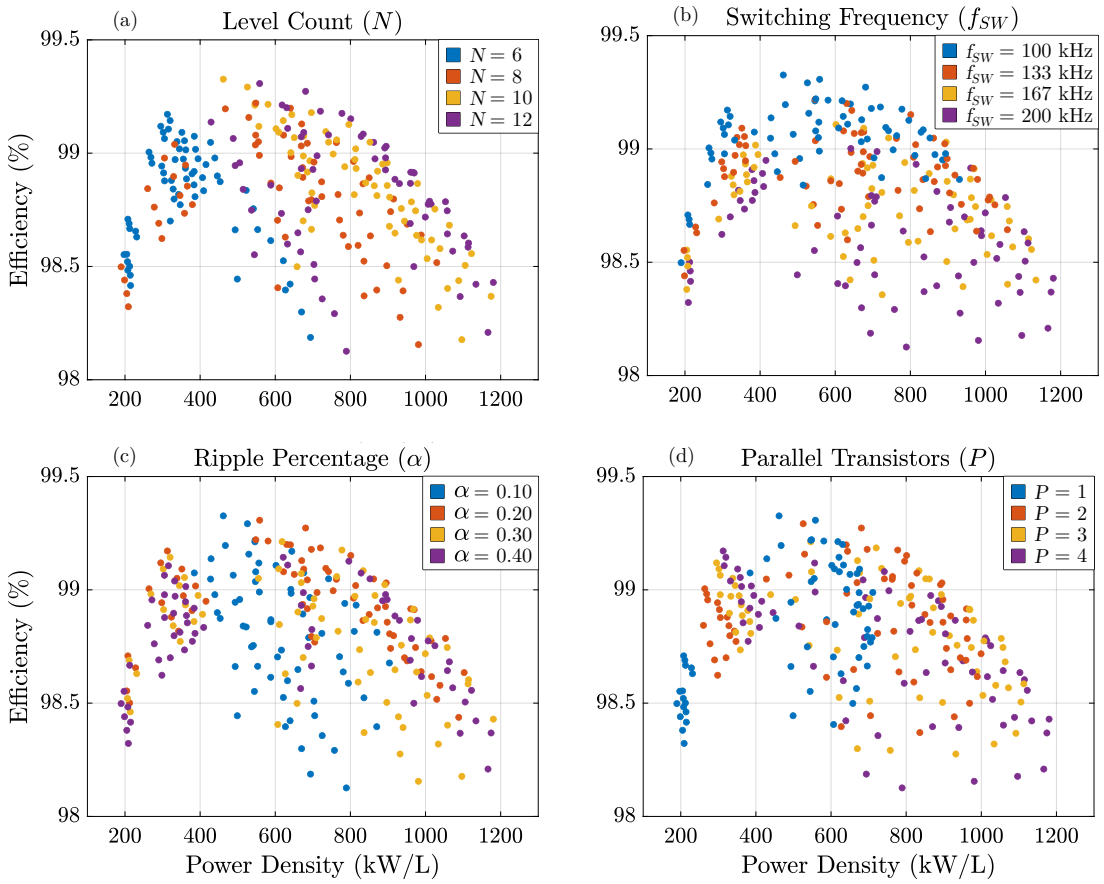


Figure 3.11: Estimated performance for various converter designs with the colors indicating various parameters. (a) Level count (N), (b) Switching frequency (f_{SW}), (c) Flying capacitor voltage ripple ratio (α), (d) Number of transistors in parallel (P).

3.3 Multi-Objective Optimization

Approach

In virtual prototyping, there is a trade-off between simplicity and accuracy. Straightforward theoretical analysis can be carried out to compare various FCML designs in terms of switch stress or passive volume [32, 60, 43]. In practice, however, the performance of these converters depends heavily on practical constraints such as available components, layout challenges, thermal limits, etc. As a result, a more bespoke design approach is in order. Multi-objective optimization techniques have proven effective for identifying promising design candidates in these applications [77, 6]. The proposed methodology is an iterative process with five steps:

1. Sweep design parameters
2. Choose suitable components
3. Compute efficiency and maximum power
4. Estimate converter volume
5. Assess design in layout

The first step is to determine relevant, independent design parameters to sweep. The selected parameters and their range of values swept in this work are given in Table 3.2. For each design, the next step is to choose suitable components based on the parameters. For example, the level count (N) combined with the ripple ratio (α) determines the blocking voltage of the switches, which dictates which transistors should be used. Based on the active and passive components selected, converter efficiency and maximum power may be estimated using the aforementioned loss model. Next, the volume can be estimated using existing techniques that model the energy storage densities of passive components [60, 43]. Finally, candidate designs may be evaluated in layout to determine how well the components fit together in practice. Based on these results, the range of values can be adjusted for each sweep parameter to find an overall "optimal design". This process is depicted in Fig. 3.12.

Key Takeaways

Fig. 3.11 plots efficiency versus power density for all of the potential converter designs. In Fig. 3.11a, data points are color-coded according to level count. Higher level counts allow for a reduction in filter inductor size but increase the required volume for capacitors, PCB, and active components. These results show that for the converter voltage and power level considered in this work, the power density improves with increasing level count, reaching an optimal balance around $N = 10$. Beyond this point (e.g. $N = 12$), further increases in level count do not yield higher density. Fig. 3.11b indicates the switching frequency of each design. Greater switching frequencies will enable reduced passive component size

Table 3.2: Design Parameters

Parameter	Value
Input Voltage (V_{IN})	600 V
Level Count (N)	[6, 8, 10, 12]
Ripple Percentage (α)	[0.10, 0.20, 0.30, 0.40]
Parallel Transistors (P)	[1, 2, 3, 4]

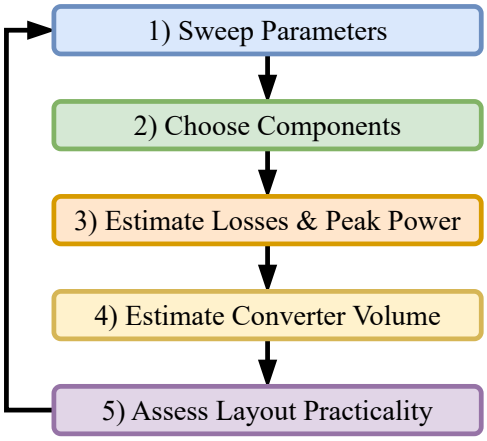


Figure 3.12: Proposed multi-objective optimization framework.

and therefore improved power density, at the expense of reduced efficiency. The range of 100 kHz $< f_{SW} <$ 200 kHz provides a reasonable trade-off for this application. At lower switching frequencies, the efficiency is barely improved, while at higher frequencies the losses limit power density. Fig. 3.11c indicates the flying capacitor voltage ripple of each design. Prior work has generally maintained ripple factors $\alpha \leq 0.1$ to limit hysteretic losses in the capacitors [8, 72, 20] and prevent over-voltage stress on the switches. However, this analysis reveals that operating with significantly larger ripple can lead to substantial gains in power density—due to the reduction in flying capacitor size—without severely impacting efficiency. While slightly higher voltage-rated switches are necessary to tolerate increased ripple, the tradeoff is favorable in the range $0.20 < \alpha < 0.40$. Fig. 3.11d illustrates the number of parallel transistors used in each design, P. Increasing the parallel count theoretically improves power density, since the converter's power capability scales linearly with P, while PCB and active component volume grow more slowly. In practice, however, values of $P > 1$ can introduce excessive cost and layout complexity.

Chapter 4

Component Sizing & Selection

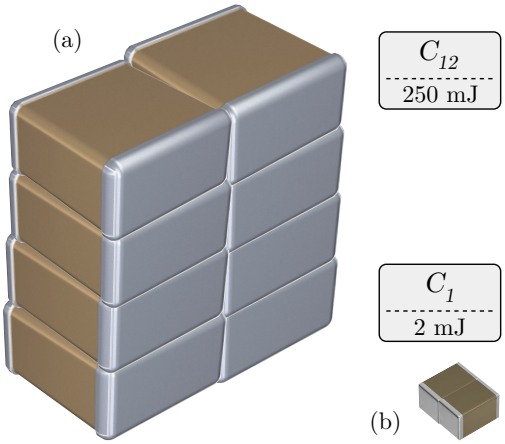


Figure 4.1: Size comparison between properly sized flying capacitors in the proposed design. (a) The largest capacitor, C_{12}, storing 250 mJ of energy, (b) The smallest capacitor, C_1, storing 2 mJ. This demonstrates the importance of using different components for each.

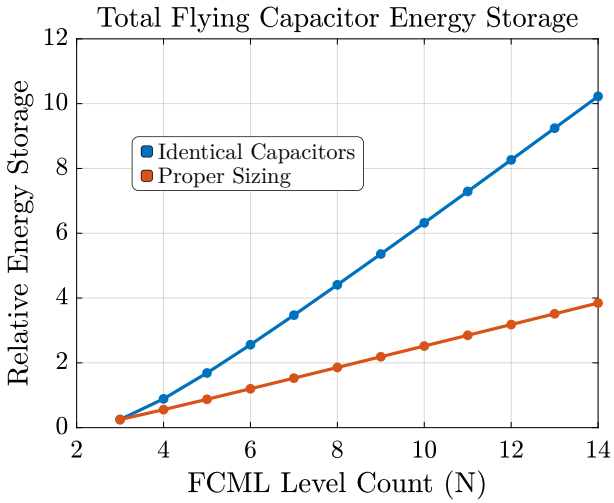


Figure 4.2: Total flying capacitor energy storage. Identically sized capacitors capable of handling the highest blocking voltage compared against properly sized capacitors designed for each individual blocking voltage.

4.1 Flying Capacitor Design

For an N-level FCML, there are $(N-2)$ flying capacitors, with the nth capacitor blocking a nominal voltage of $V_n = nV_{IN}/(N-1)$. Identical capacitance is used at each node to ensure that all of the switches see the same voltage across them when considering flying capacitor

$$C_F = \frac{1}{\frac{N_{SA}}{N_{PA}C_A} + \frac{N_{SB}}{N_{PB}C_B}} \tag{4.1}$$

$$V_F = N_{SA}V_{RA} + N_{SB}V_{RB} \tag{4.2}$$

$$(N_{PA}/N_{PB})^* = \frac{C_B V_{RB}}{C_A V_{RA}} \tag{4.3}$$

$$\min_{V_F} | \, (V_F > V_n + V_\Delta) \rightarrow N^*_{SA}, N^*_{SB} \tag{4.4}$$

$$N_{PB} > (\frac{C_R}{C_B})(\frac{N^*_{SA}V_{RA}}{V_{RB}} + N^*_{SB}) \tag{4.5}$$

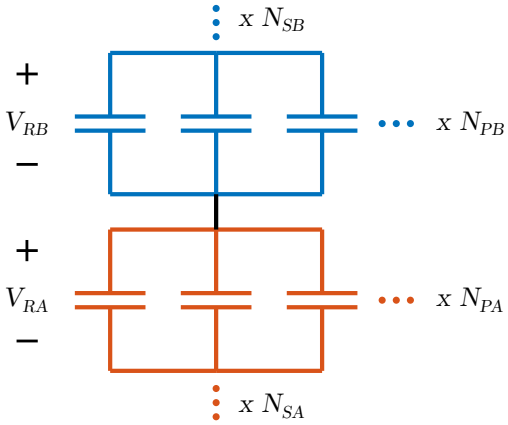


Figure 4.3: Schematic for each flying capacitance with labeled parameters for optimization.

voltage ripple. As each capacitor stores an energy of $\frac{1}{2}CV^2$, its energy storage requirement is proportional to n^2. In a 14-level FCML, C_1 should theoretically be 144 times smaller than C_{12} (assuming identical energy densities). Fig. 4.1 shows the size difference between the components used for C_1 and C_{12} in this work. In contrast, conventional designs usually make the highest and lowest flying capacitors only 2-3 times different in size because the same components are used, simplifying layout and assembly. Fig. 4.2 illustrates the total energy storage for all of the flying capacitors in an FCML with different design approaches. The simplest approach uses identical capacitors all rated for the highest blocking voltage, while the proposed approach utilizes capacitors rated to their individual blocking voltages. For high level counts, this can lead to greater than 50 % reduction in size.

Component Selection

A unique combination of capacitors must be used for every flying capacitance in order to optimize for its unique energy storage requirement. The range of blocking voltages required is $V_{IN}/(N-1)$ to $(N-2)V_{IN}/(N-1)$, which corresponds to $61.5\,V - 738.5\,V$ for $V_{IN} = 800\,V$, chosen in this work. The first step is to determine which capacitors have the highest energy density within these voltage ranges, by simply computing $(C(V) * V^2)/(size)$ for each of them. Here, $C(V)$ accounts for any nonlinearity in small-signal capacitance across DC bias voltage (e.g. in class II ceramic capacitors). Either volume or mass may be used as the size metric. A comprehensive survey was done, with the aid of recently published work [125]. Two capacitors were chosen, capacitor A (C_A) with a rated voltage $V_{RA} = 100\,V$, offering

the highest energy density for voltages between $50\,V - 100\,V$, and capacitor B (C_B) with $V_{RB} = 450\,V$, providing the highest density for voltages between $100\,V - 450\,V$. Note that a single capacitor technology has the highest density across a relatively wide range of voltages.

Capacitance Optimization

Given the two types of capacitors selected, the appropriate combination may be computed (this can be extended to more than two as well). It will consist of a certain number (N_{SA}) of C_A capacitors in series with a number (N_{SB}) of C_B capacitors. N_{PA} and N_{PB} capacitors will be connected in parallel at each node, with blocking voltages of V_{RA} and V_{RB} respectively. Fig. 4.3 shows a schematic drawing that illustrates this design approach, where the overall capacitance is calculated in (4.1), while the total blocking voltage is provided in (4.2).

The optimal ratio between N_{PA} and N_{PB} can be found by ensuring that all of the capacitors have a blocking voltage proportional to their rated voltage, as computed in (4.3). The optimal values for N_{SA} and N_{SB} are given in (4.4), where V_Δ is the worst-case peak ripple on the capacitor. A series combination of C_A and C_B should be selected such that the minimum total blocking voltage is achieved, which is still greater than the worst case voltage on that flying capacitor. The number of parallel capacitors can now be determined by combining (4.1), (4.3), & (4.4) to ensure C_F is greater than C_R, the required capacitance to meet voltage ripple constraints. This is done in (4.5).

4.2 Decoupling Capacitor Design

For a power converter operating under hard-switching conditions, significant dv/dt and di/dt will occur during the switching transition. When a device turns on, its conducted current must rise rapidly while its blocking voltage falls, and the reverse is true during turn-off. Ideally, these changes would happen instantaneously and the overshoot/settling time would be minimal. In reality, there is a parasitic inductance associated with the loop connecting the switching components, known as commutation loop inductance [32]. This causes the circuit to have a high quality factor, leading to large voltage overshoot and oscillation during switching transitions. As such, switch stress and electromagnetic interference (EMI) are increased, while reliability is diminished. These problems are especially relevant for wide-bandgap devices such as gallium-nitride high-electron-mobility transistors (GaN HEMTs) [95, 14, 78, 61], which offer an improved figure of merit as compared to other technologies [5]. The small on-resistance and output capacitance of these devices causes the switching circuit to be especially underdamped, so excessive overshoot can occur.

In order to mitigate these issues, the quality factor of the circuit must be reduced. This is typically done by increasing the gate resistance, thereby slowing the switching transition, but converter efficiency will be reduced due to the increased overlap loss. Another option is to decrease the commutation loop inductance. This can improve performance somewhat, but large bulk capacitors are typically required to meet voltage ripple constraints under load.

As such, their package inductance is considerable and they may need to be placed far from the power path. The use of a much smaller capacitor located closer to the switches, called a decoupling capacitor, allows for a reduced commutation loop inductance. Advanced layout techniques can be used to reduce this inductance further, but they are not always feasible as they require extra board area and increase manufacturing cost [46, 85, 116].

The process for decoupling capacitor sizing in power delivery networks (PDNs) has been studied [39, 100]. Power converter switching transitions differ from PDN load steps, however, because both the voltage and current at the converter input change throughout the switching interval. A detailed analysis specific to this application is therefore in order. Prior art has developed analytical models for transistor switching performance [113, 118], but these works focus on a boost-type switching circuit and utilize simplified models which neglect non-linear effects that are shown in this paper to be important. Reference [18] determined the proper sizing of decoupling capacitance to minimize EMI, but did not include the dependence on load current. This work builds upon these efforts by developing a model of the switching dynamics which provides insight for an empirically determined optimal decoupling capacitance in GaN-based power converters.

Model Analysis

Simplified Circuit Model

Fig. 4.4a shows the simplified schematic of a synchronous buck converter undergoing a high-side turn-on, with the switch node voltage, V_{SW}, labeled. Subsequent analysis will focus on this circuit. The input voltage source may be ignored because it is assumed to have a higher impedance path than C_{IN}. The output filter and load can be treated as a current sink because the current through the large filter inductance will be roughly constant during the short switching interval. These simplifications yield Fig. 4.4b. Next, the input capacitor is separated into bulk and decoupling capacitance, each with a corresponding series parasitic inductance. Mutual inductance between these paths is neglected. The large bulk capacitance may be approximated as a voltage source because its voltage will be constant during the switching event. This gives Fig. 4.4c. Q_{LS} is off during the high-side turn-on, so its equivalent circuit is C_{OSS} in parallel with a body diode. The diode is on during the dead-time, but not during the transition itself, so it affects the initial conditions of the model but can be excluded from Fig. 4.4d. The device model of Q_{HS} is considered in Fig. 4.4e. Most of the current through Q_{HS} will be conducted by the channel, i_{ch}, and drain-to-source capacitance, C_{DS}, so the gate drive can be treated separately. Miller feedback is still considered, but the current through C_{GD} is not included in the main circuit. Finally, the voltage across and current into Q_{HS} are both strictly positive during the switching transition, so its channel can be viewed as a variable resistance controlled by the gate voltage, as in Fig. 4.4f.

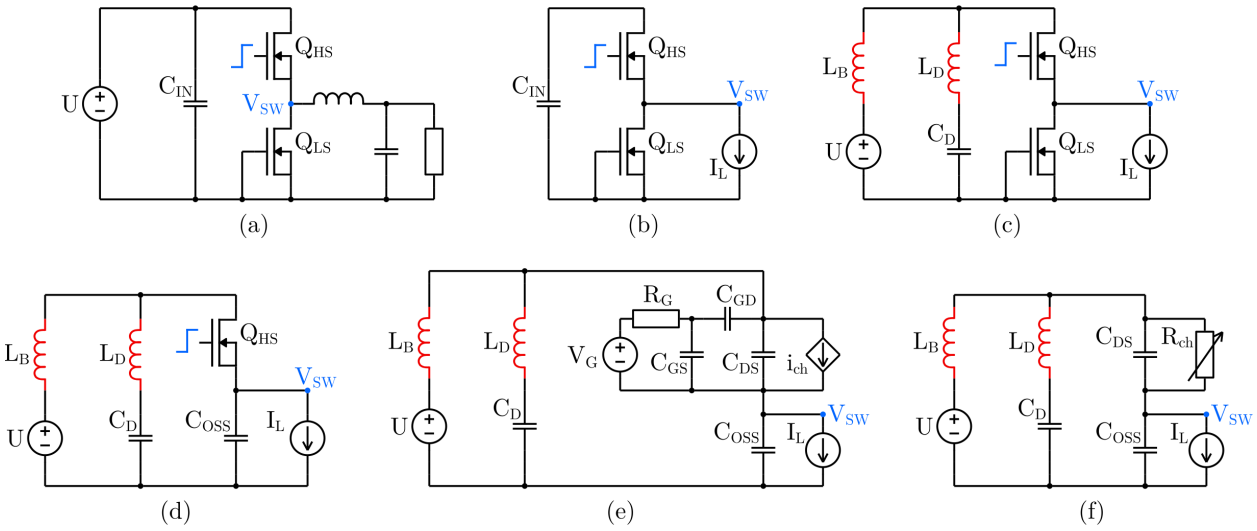


Figure 4.4: Switching transition circuit models. (a) Synchronous buck converter high-side turn-on, (b) Input voltage removed and output filter treated as current sink, (c) Input capacitance separated into bulk and decoupling loops with bulk capacitance approximated as voltage source, (d) Low-side transistor replaced with output capacitance, (e) High-side transistor device model included, (f) Gate drive removed with channel modeled as controlled resistance.

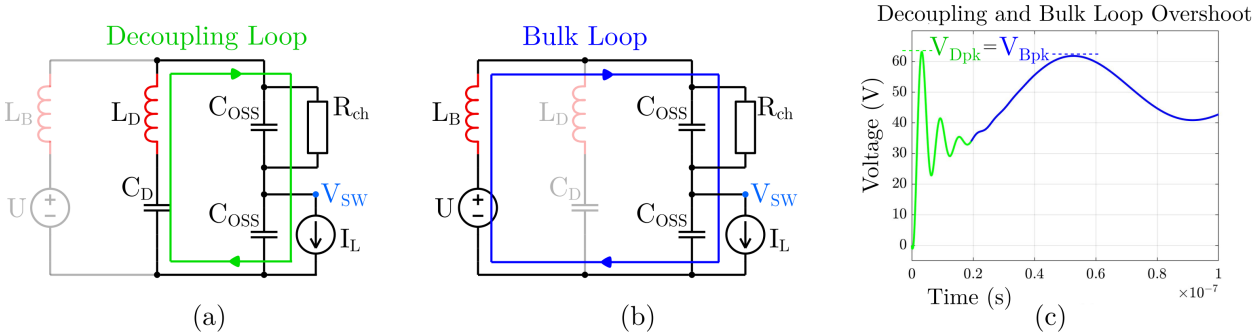


Figure 4.5: Linear second order circuits. (a) Decoupling loop, (b) Bulk loop, (c) Simulation illustrating initial decoupling loop overshoot followed by bulk loop overshoot for V_{SW}.

Linear System Model

If a linear charge-equivalent capacitance value is used for C_{OSS}, and R_{ch} is assumed roughly constant, the circuit in Fig. 4.4f can be treated as a linear fourth order system. These assumptions will be dropped later, but are useful for intuition. In the following analysis, it will be assumed that both the bulk and decoupling loops are underdamped, which is reasonable for a well-designed, high-efficiency converter. In addition, it is assumed that L_D

is much smaller than L_B. This is always true in practice, because otherwise the decoupling path serves no purpose. Given these assumptions, the circuit can be treated as two weakly coupled linear second order systems. The linear loop models are shown in Fig. 4.5, along with simulation results demonstrating the decoupling and bulk overshoots.

The initial dynamics are due almost entirely to the decoupling loop, which acts first before the current in L_B ramps up. C_D begins fully charged to the input voltage. During the switching transition, charge transfers to the output capacitance and load current. If C_D is too small, it loses all of its voltage during this process. The underdamped bulk loop will then generate significant overshoot as it charges up C_{OSS} the rest of the way. If C_D is large enough, however, it will maintain its voltage, so the bulk overshoot will be small because C_{OSS} is already charged up. If C_D is too large, it causes excessive decoupling loop overshoot on the switch node.

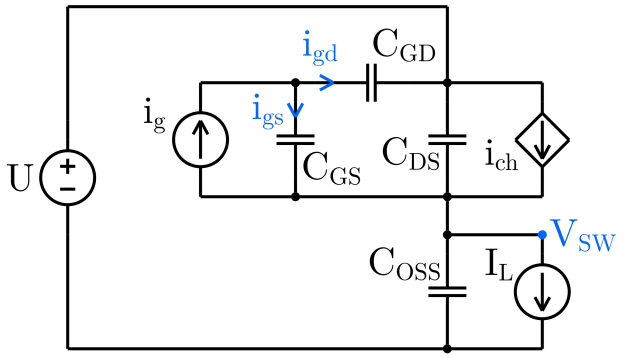


Figure 4.6: Simplified schematic highlighting Q_{HS} device model.

Non-Linear Effects

The gate-to-drain capacitance of Q_{HS} is a non-linear component which significantly affects the switching dynamics. Fig. 4.6 shows a simplified circuit model without inductances, which are neglected here so that a useful analytical derivation of V_{SW} may be computed.

$$\dot{V_{GS}} = \frac{i_{gs}}{C_{GS}} = \frac{i_g - i_{gd}}{C_{GS}} \tag{4.6}$$

$$i_{gd} = C_{GD}\dot{V_{GD}} \approx C_{GD}\dot{V_{SW}} \tag{4.7}$$

$$\dot{V_{SW}} = \frac{i_{ch} - I_L}{C_{SW}} \tag{4.8}$$

$$\dot{i_{ch}} = \frac{\partial i_{ch}}{\partial V_{GS}} \frac{\partial V_{GS}}{\partial t} \approx g_m \dot{V_{GS}} \tag{4.9}$$

Equations (4.6)-(4.8) can be obtained through visual inspection, while (4.9) is derived from the saturation model of a transistor. Here, $i_g = (V_G - V_{GP})/R_G$, where V_{GP} is the gate plateau voltage of the device for the given load current. $C_{SW} = C_{OSS} + C_{DS}$, is the total capacitance on the switch node. The approximation in (4.7) is valid because the dv/dt of the switch node is much greater than that of V_{GS}. Combining (4.6)-(4.9) leads to (4.10).

$$\dot{i_{ch}} = \frac{g_m}{C_{GS}}(i_g - C_{GD}\dot{V_{SW}}) = \frac{g_m}{C_{GS}}(i_g - C_{GD}\frac{i_{ch} - I_L}{C_{SW}}) \tag{4.10}$$

The differential equation in (4.10) can be solved for i_{ch}, with an initial value of I_L.

$$i_{ch} = I_L + \gamma C_{SW}(1 - e^{-\alpha t}) \tag{4.11}$$

$\dot{V}_{SW}$ can be computed by combining this result with (4.8).

$$\dot{V_{SW}} = \gamma(1 - e^{-\alpha t}) \tag{4.12}$$

Here, $\gamma = i_g/C_{GD}$ and $\alpha = (g_m C_{GD})/(C_{GS}C_{SW})$. It is clear by looking at (4.12) that the maximum derivative of the switch node voltage is γ. V_{SW} cannot change faster than this because of the negative feedback loop with the gate drive through C_{GD}. When the device begins to turn on, this capacitance is small, so L_D and L_B restrict the rise of V_{SW}. As the drain-to-source voltage drops, however, the value of C_{GD} rises dramatically. For example, the EPC2218 GaN HEMT exhibits a 50x increase in the value of C_{GD} when its V_{DS} value goes to zero [30]. This is a non-linear characteristic which causes more damping at higher switching speeds. Skin and proximity effect are also increased at higher switching speeds [58]. As a result, the decoupling loop overshoot is damped more than the bulk loop overshoot, and much more than the linear model predicts. Decoupling loop overshoot is actually not a concern in practice due to these non-linear effects, and large C_D values do not increase overshoot. Fig. 4.7 plots simulation results with linear C_{GD} versus non-linear C_{GD} and illustrates this damping effect.

Optimal Decoupling Capacitor Sizing

An approximate optimal value for C_D can be estimated based on the previous conclusions, using voltage overshoot and decoupling capacitor size as the performance metrics. The decoupling loop must source the initial load current before the bulk inductor current ramps up. During this time, as the switch node voltage rises from $0\,V$ to the input voltage, U, the average voltage across L_B is approximately $U/2$. Given the fundamental inductor equation, $di_L/dt = v_L/L$, the following equation calculates the time necessary for the bulk inductance to carry the full load current, in the worst case.

$$t_D = \frac{2L_B I_{ML}}{U_{ML}} \tag{4.13}$$

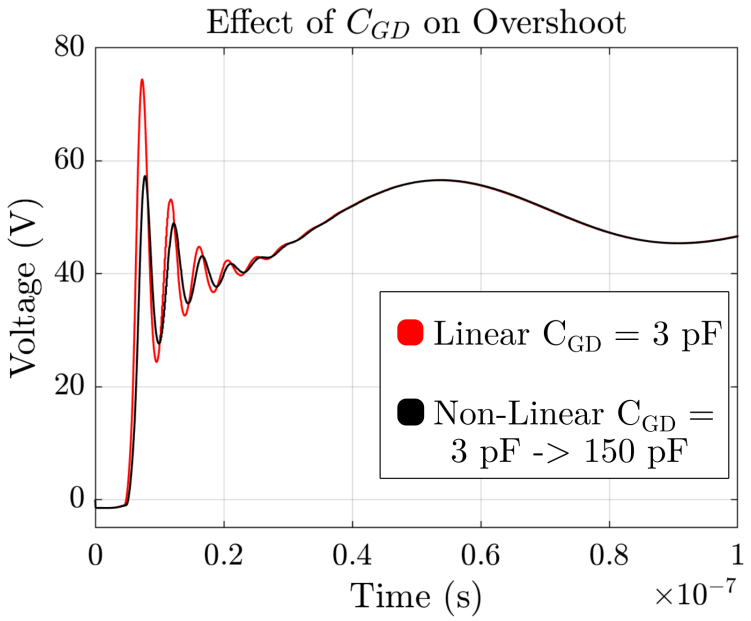


Figure 4.7: Simulation results demonstrating effect of non-linear C_{GD} on voltage overshoot. Using actual datasheet gate-drain capacitance curve for EPC2218.

Here, I_{ML} is the max load current and U_{ML} is the minimum input voltage for which that current will be drawn. The charge required from the decoupling capacitance during this time is

$$Q_R = \frac{2L_B I_{ML}^2}{U_{ML}} \tag{4.14}$$

while the charge on C_D is

$$Q_D = C_D U_{ML} \tag{4.15}$$

These equations can be rearranged to determine the required capacitance value to source the load current.

$$C_{R1} = \frac{2L_B I_{ML}^2}{U_{ML}^2} \tag{4.16}$$

The decoupling capacitor must be large enough to charge up C_{OSS} as well.

$$C_{R2} = C_{OSS} \tag{4.17}$$

C_D must be larger than these two requirements; if $C_D = C_{R1}$ or $C_D = C_{R2}$, the voltage on the decoupling capacitor will drop all the way to zero during t_D. It is empirically determined that a margin of 10x provides enough charge to source these loads, without excess size. Larger

values of C_D require bigger packages with more package inductance, which is detrimental to performance, while smaller values exhibit more overshoot. As such, $C_D = C_D^*$ is deemed optimal. This is the inflection point in Fig. 4.9b, yielding the following design guideline for the optimal sizing of C_D.

$$C_D^* = 10 * \max\{C_{OSS}, \frac{2L_B I_{ML}^2}{U_{ML}^2}\} \tag{4.18}$$

Table 4.1: Switching Cell Parameters

Parameter	Value(s)
Switching Device	EPC2218, EPC2212
Blocking Voltage	10 V – 80 V
Load Current	0 A – 40 A
Gate Resistance	5 Ω, 10 Ω
Decoupling Capacitance	0 nF – 300 nF
Bulk Capacitance	6.6 uF
Decoupling Loop Inductance	1 nH
Bulk Loop Inductance	3.5 nH, 14.5 nH

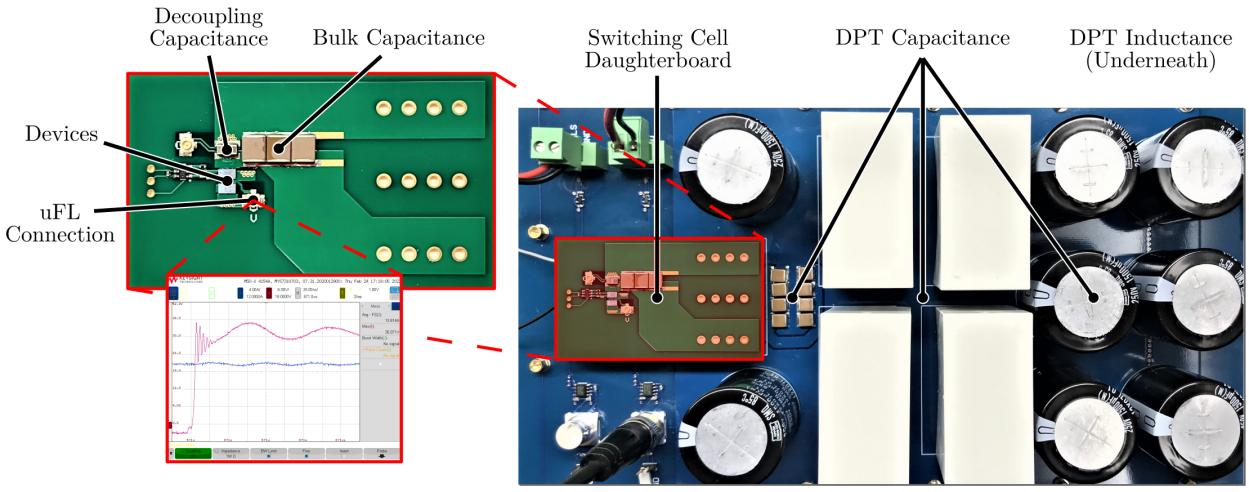


Figure 4.8: Hardware setup with double pulse testing motherboard and half-bridge switching cell daughterboard.

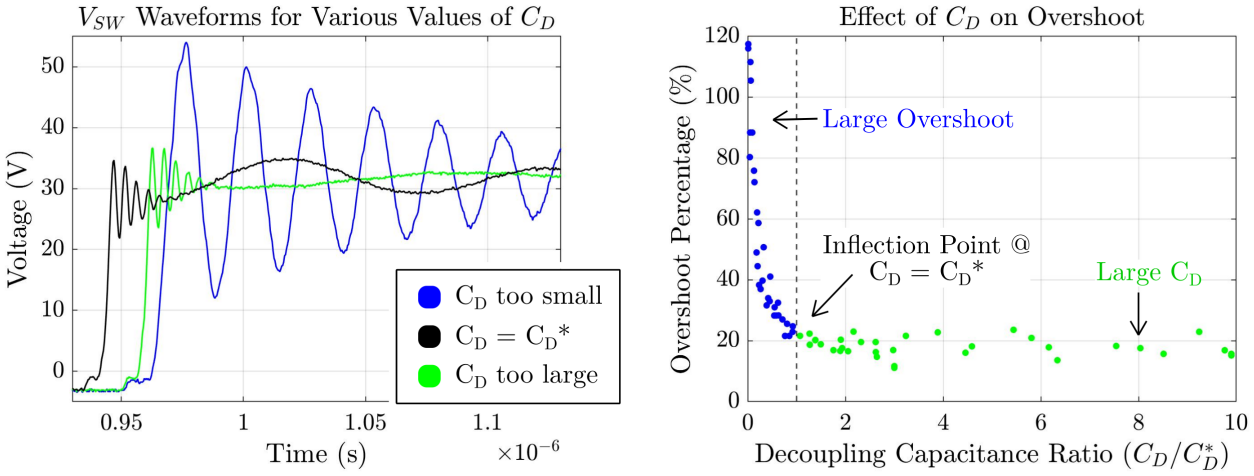


Figure 4.9: (a) Experimental waveforms demonstrating minimal overshoot at $C_D = C_D^*$, (b) Experimental results showing inflection point at $C_D = C_D^*$ and that overshoot percentage is small for $C_D > C_D^*$.

Hardware Results

In order to validate the proposed model and conclusions, a system for double pulse testing (DPT) is employed. The design utilizes a motherboard which houses the large inductance and capacitance required for the test. Modular daughterboards can be swapped in, each containing a different half-bridge switching cell. This setup allows for the following parameters to be swept: blocking voltage, load current, switching device, decoupling capacitance, bulk capacitance, decoupling loop inductance, and bulk loop inductance. For switch node measurements, a 1.5 GHz, 5 GSa/s, Keysight InfiniiVision MSOX4154A oscilloscope is used with 750 MHz N2894A passive probe connected to a surface-mount uFL connector. EPC GaN HEMTs are used as the switching devices for all of the tests. Fig. 4.8 shows the setup.

Fig. 4.9a shows V_{SW} waveforms for three different values of decoupling capacitance, with a blocking voltage of 30 V, load current of 27 A, 10 Ohm gate resistance, 1 nH decoupling loop inductance, 3.5 nH bulk loop inductance, and EPC2218 switching device. The overshoot percentage is very large (80%) with $C_D = 5.6nF$, and much smaller (13%) for the optimally sized $C_D = 60nF$. When the decoupling capacitance is increased beyond the optimal point, to $C_D = 300nF$, the peak overshoot percentage increases slightly to (23%). More than 200 DPT measurements are made across various operating points. Table 4.1 lists the parameter variations for these tests. Fig. 4.9b plots the percent overshoot of V_{SW} as a function of C_D/C_D^*. The inflection point at $C_D = C_D^*$ is clearly visible. Experimental data shows consistently that throughout all measurements, a C_D value below C_D^* leads to increased overshoot, while increasing the value of C_D beyond C_D^* has little effect. According to the linear model, there would be excessive decoupling loop overshoot at high values of C_D/C_D^*, but the damping effect of C_{GD} counteracts this so that overshoot remains constant beyond

the inflection point.

Conclusion

This work has presented a simplified circuit model describing converter operation during the high-side turn-on switching transition of a synchronous buck converter. Weakly coupled linear second order systems are derived and it is determined that separate decoupling and bulk loop overshoots will occur. The most important deviation from the linear model is described: non-linear gate-drain capacitance, which causes decoupling loop overshoot to be highly damped. Finally, a simple empirical optimal point is found for the sizing of C_D, which achieves minimal overshoot without excess size. Future work will expand these results to other switching transitions and devices.

Chapter 5

Layout & Packaging

5.1 Stacked-PCB Design

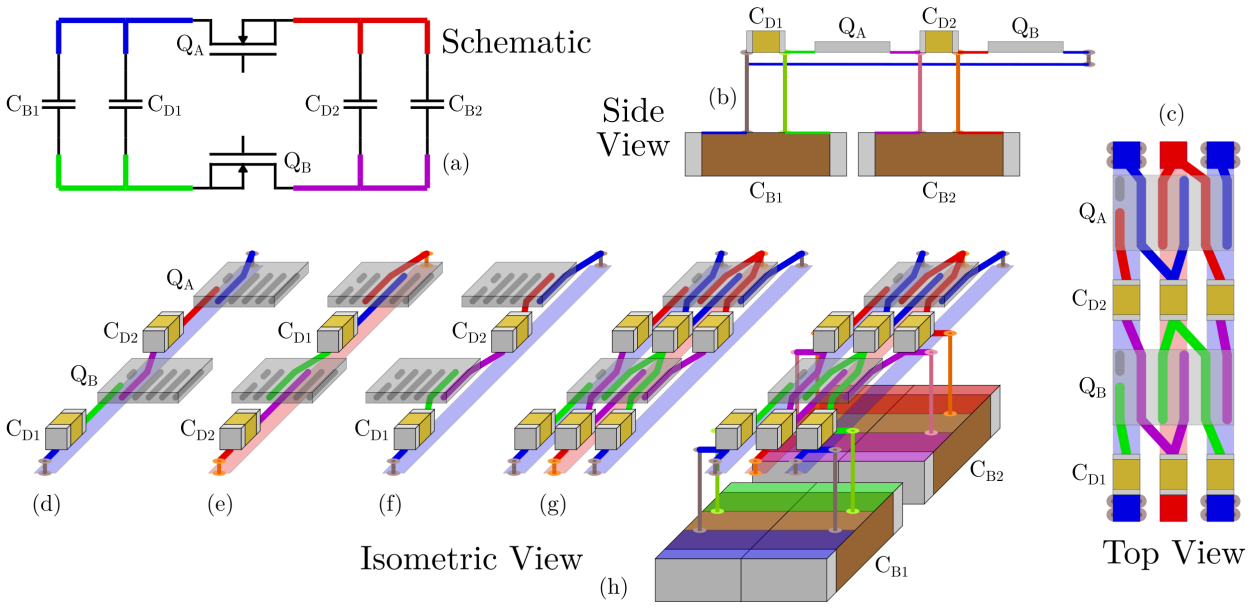


Figure 5.1: Proposed commutation loop design. (a) schematic with color-coded nets, (b) side view, (c) top view, (d)-(f) isometric view highlighting separate paths, (g) combined hybrid paths, (h) including bulk capacitors.

The FCML topology contains many floating switches, each with isolated gate drive circuitry, which takes up a large portion of board area. The devices used in high-performance designs have very low on-resistance and high current limits (1.4 mOhm, 101 A for the EPC2302 used in this design [31]). The routing resistance must therefore be minimized to avoid excess conduction loss. The outer copper layers of the PCB are typically the thickest, so they

should be reserved for the power path. The use of vias and inner layers for the conduction path reduces density. High-power converters generate considerable EMI from their switching actions, which can interfere with low-voltage control signals. Signal integrity is crucial in FCMLs because the switches are not rated to the full input voltage, so false turn-ons can lead to complete system failure.

The use of a separate daughterboard PCB for the gate drive circuitry resolves both of these issues. In the proposed design, a 6-layer daughterboard is used. Layers 1 and 2 contain the gate drive components and routing, while layer 3 provides shielding pours. Layers 4-6 are empty so that there is 1 mm of FR4 separating the shields and the power path. The ground-referenced control signals enter from the top and bottom of the daughterboard through castellated vias soldered onto the motherboard. A digital isolator, with isolated power, provides gate signals referenced to the source of each switch. A high-current gate driver with split-gate outputs is connected to the switches again through castellated holes. Fig. 5.2a and 5.2b highlight the schematic and layout of the gate drive PCB switching cell, respectively. The area on the motherboard beneath the signal domain is used for routing gate signals from the main controller. The area on the motherboard beneath the switching domain is used for power path routing. This enables an extremely dense design where high-voltage clearances are satisfied and the sensitive ground-referenced control signals are distanced from noisy power nodes in both the vertical and horizontal directions, and have shielding layers beneath them. Moreover, the power path is completely uninterrupted on all layers of the motherboard.

Table 5.1: Commutation Loop Comparison

Switching Cell Design	Electrically Thin	Hybrid & E-thin	Hybrid Reference	Proposed Design
Simulated Inductance	1.15 nH	450 pH	521 pH	443 pH
Measured Inductance	2.85 nH	940 pH	—	1.14 nH
Board Area	370 mm^2	330 mm^2	420 mm^2	420 mm^2

Commutation Loop Routing

Prior work has demonstrated the severe impact that parasitic commutation loop inductance has on switching performance. It degrades both the reliability and efficiency [95, 94, 11]. A hybrid layout (utilizing the closest inner layer as a return path) with decoupling capacitors has been shown [46] to provide the lowest inductance to date for high voltage designs. In this work, a novel commutation loop layout is employed, which features 3 anti-parallel hybrid paths. It relies on the interleaved pads of the chip-scale packaged land-grid-array (LGA) EPC devices. It does not require any advanced manufacturing techniques from the PCB manufacturer, but does have smaller clearances than the standard hybrid approach, and thus a more limited voltage range.

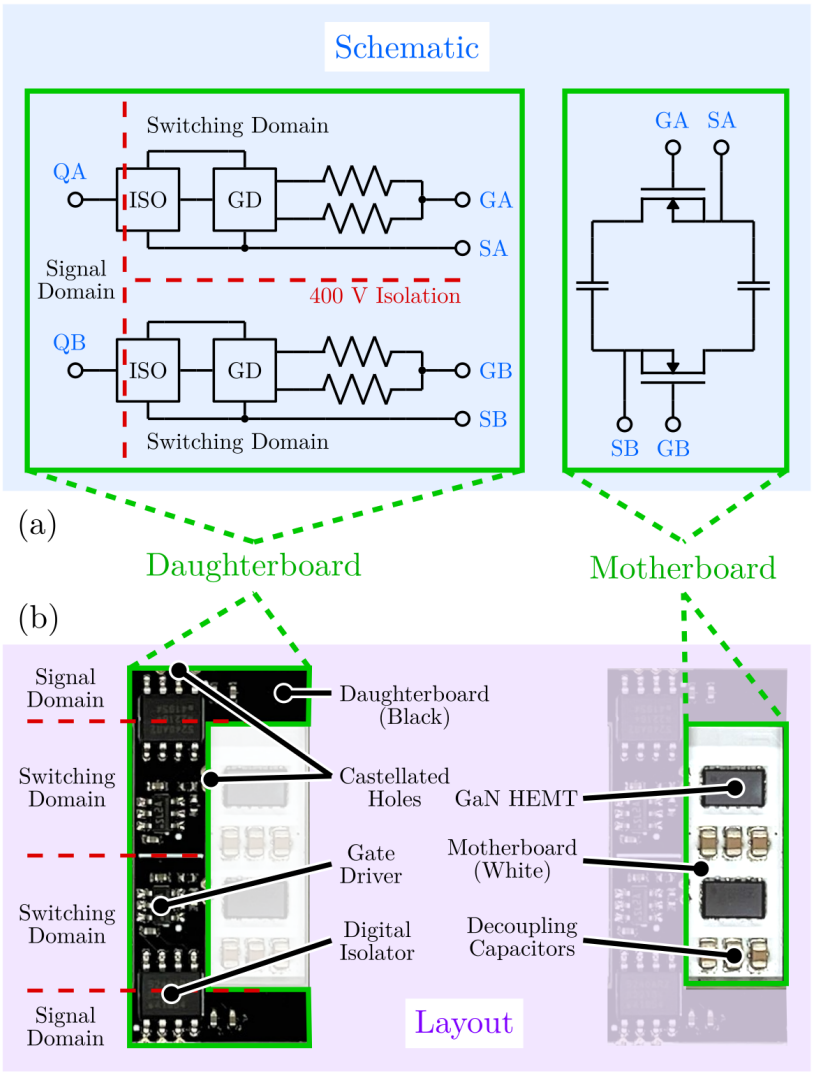


Figure 5.2: Stacked PCB design with gate drive circuitry on daughterboard and power path on motherboard. (a) Schematic, (b) Layout with separate low-voltage signal domains and high-voltage switching domains on the daughterboard, which is matched by the motherboard.

The advanced commutation loop layout is shown from a variety of angles in Fig. 5.1. Fig. 5.1a shows the schematic drawing of a single switching cell, with color-coded nets corresponding to the traces in other parts of the figure. Fig. 5.1b and 5.1c show side and top views respectively, while Fig. 5.1d-f highlight each hybrid path in isometric view. Note that the direction of current flow in each path is alternating. This provides flux cancellation which reduces inductance. Fig. 5.1g and 5.1h combine the paths and show the connections to bulk capacitors on the bottom of the motherboard, also in isometric view. The inductance values of both the decoupling and bulk capacitor loops are important for voltage overshoot during

switching transitions [47]. Ansys Q3D was used to simulate the commutation loop inductance of this proposed design. Hardware measurement of the inductance was also performed with a Keysight E4990A Impedance Analyzer and 42941A probe, using the method in [14]. The simulated inductance is 443 pH while the measured value is 1.14 nH. The large difference between simulated and measured inductance is attributable to the package inductance of the devices and capacitors, which are not accounted for in simulation. The simulated value assesses the PCB routing only, with all components modeled as copper sheets. Table 5.1 compares the proposed design to prior art, both of which use blind and buried vias. As each design uses different components, the comparison is not entirely equal. To provide a fair reference, an alternate layout was made with a standard hybrid loop; this yielded a simulated inductance of 521 pH. The proposed design achieves comparable performance to the state of the art, without the need for blind or buried vias.

5.2 Dual-PCB Design

In Section 4.1, an optimal sizing scheme for FCML flying capacitors was developed. This section complements that work by developing a layout which can properly include those capacitors into an overall converter layout. Fig. 5.3 shows component placement for the dual-PCB design. The 'Top Board' has active circuitry on the top and passive components on the bottom. The 'Bottom Board' is mirrored, such that the active circuitry is on the bottom and the flying capacitors are on the top. This design allows the two PCBs to be combined such that the flying capacitors fit neatly together, as shown in Fig. 5.4. The largest flying capacitor (C_{12}) is paired with the smallest (C_2), the next biggest with the next smallest (C_{11} and C_3), and so on. This allows all of the uniquely sized flying capacitors to fit together within a compact box volume. Moreover, the routing for the active circuitry remains modular, which simplifies design.

5.3 Decoupling Device

Prior work has shown that a power converter's commutation loop inductance, which arises from the physical layout of the switching components, is critical to its performance[47, 94, 11]. This parasitic inductance affects the switching speed, voltage overshoot, and electromagnetic interference. For designs with small, surface-mount devices, it may be minimized through the use of clever layout techniques[46, 85, 14, 116]. But for many applications, power transistors with larger through-hole packages (e.g. TO-220, TO-247, TO-252) are used, due to their low junction-to-case thermal impedance and compatibility with heat sinks, both of which allow for high power handling capability. These devices have long leads which inhibit low commutation loop inductance design. Fig. 5.5a shows a standard buck converter schematic with the commutation loop inductance modeled as L_{BIG}. During switching transitions, this large inductance will resonate with the output capacitance, C_{OSS}, of the devices, and large

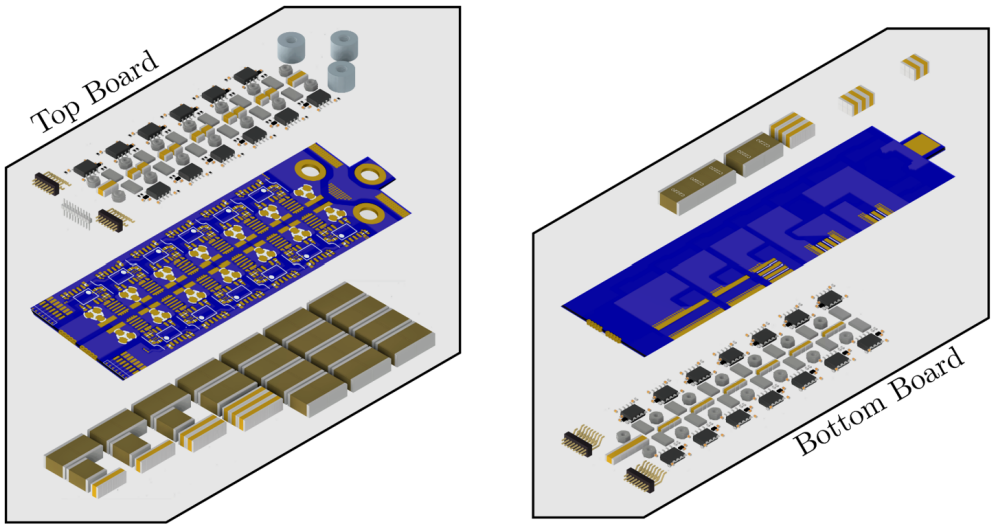


Figure 5.3: Component placement for dual-PCB design. The Top Board has active circuitry on the top and passive components on the bottom. The Bottom Board is mirrored.

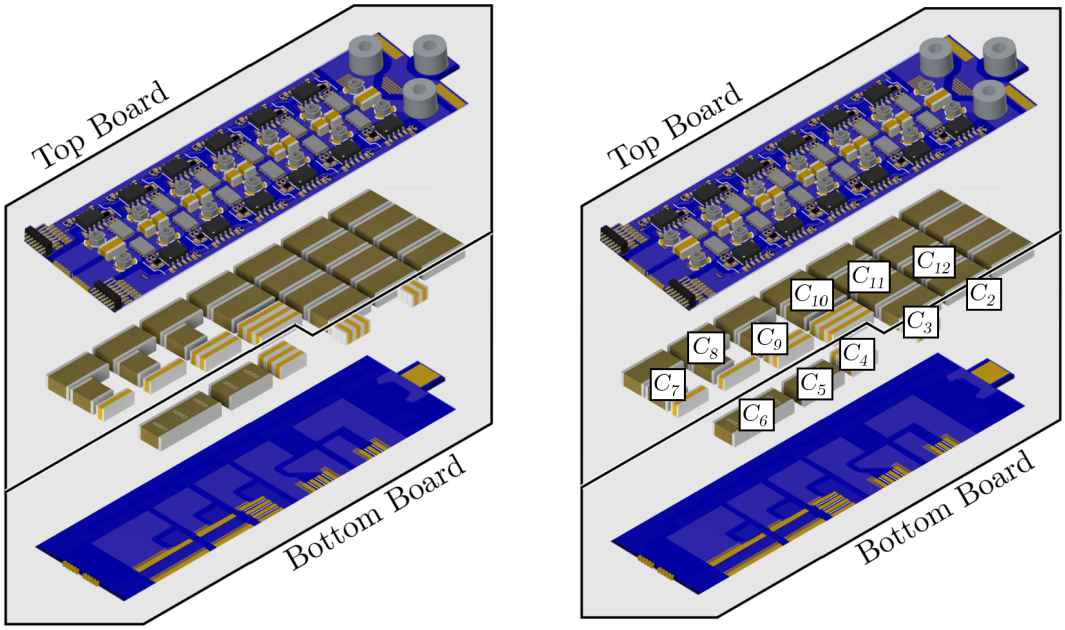


Figure 5.4: Dual-PCB stacking design. (a) Flying capacitors fit together between the Top Board and Bottom Board, (b) Larger flying capacitors on one PCB are paired with smaller ones on the other so everything fits together neatly.

voltage overshoot will occur. Furthermore, the large gate-to-source inductance can lead to false turn-ons via the Miller effect. In order to mitigate these issues, gate resistance may be increased to slow down the switching transition, but this will cause even greater overlap loss. Alternatively, various snubber circuits have been developed to reduce overshoot, overlap loss, and output capacitance hard-charging loss [114]. These circuits are designed to redirect the reactive energy in the main commutation loop. Dissipative snubbers typically do not provide significant efficiency improvements, while regenerative snubbers require extra active circuitry along with magnetics, which increases size, complexity, and cost [27, 50, 1, 9].

In this work, a small surface-mount switch is added in parallel to the large through-hole power transistor in a buck converter to improve switching performance. Unlike other snubbers, this switch will act in place of the main power device during the switching transitions, and will form a much smaller commutation loop together with the low-side anti-parallel diode and decoupling capacitors. The switching transition can therefore be fast with low overlap loss. The use of hybrid switches has been demonstrated, typically for a field-effect transistor (FET) in parallel with an insulated gate bipolar transistor (IGBT) [35, 66]. This work extends prior art by paralleling a GaN HEMT with a Silicon FET and focusing on commutation loop and gate drive design considerations to develop a practical, high-performance solution.

Design

This work proposes a circuit which provides a parallel low inductance path during the switching intervals. One active switch is required, which is named a decoupling device. Along with a decoupling capacitor and low-side anti-parallel diode, it comprises a small commutation loop which undergoes the hard-switching transitions, while the main power transistor handles the steady-state current conduction. Two different gate drive methods are compared for use within a buck converter.

Normal Buck Operation

Fig. 5.5b shows the modulation diagram for a standard buck converter. There are 4 states of circuit operation. State 1: The high-side transistor, Q_H, turns on, and the high-side on phase begins. This turn-on is "hard" or lossy. The large di/dt in L_{BIG} causes voltage overshoot on the switch node which generates EMI and can damage the active devices if their blocking voltage is not sufficiently overrated. Energy stored in the output capacitance of Q_H ($C_{OSSH}V_{IN}^2/2$) and the energy required to charge up the output capacitance of the low-side transistor, Q_L, ($C_{OSSL}V_{IN}^2/2$) are both lost. In addition, during the switching transition, Q_H conducts current and blocks voltage simultaneously, which creates overlap loss proportional to the duration of the switching interval. These switching loss mechanisms diminish efficiency and generate heat. State 2: Q_H turns off slowly due to L_{BIG} and incurs overlap loss once again. The buck converter will naturally soft-discharge the output capacitances here, so hard-charging loss and diode conduction loss can be greatly reduced or even eliminated,

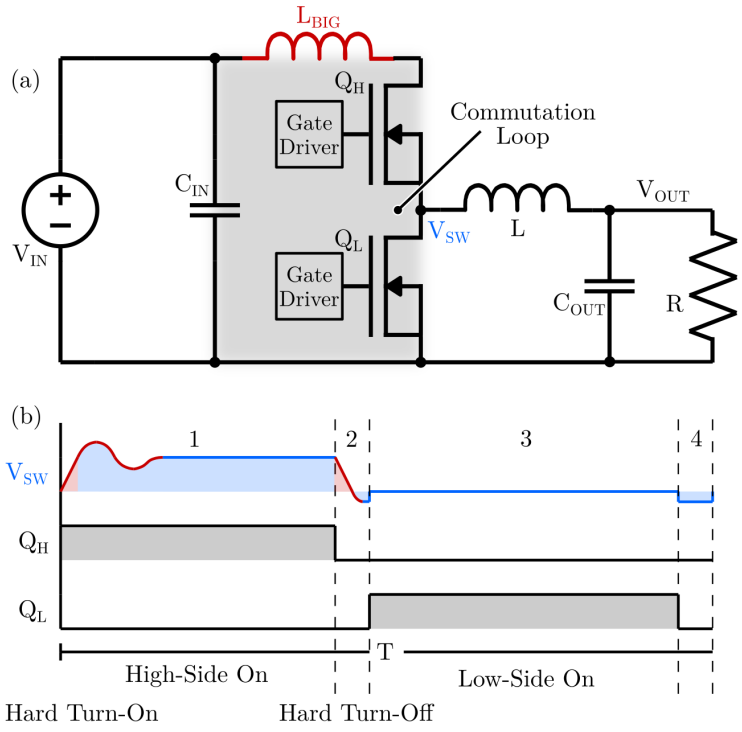


Figure 5.5: Normal buck converter with commutation loop inductance modeled as a single lumped L_{BIG}. (a) Schematic, (b) Modulation diagram highlighting the overshoot, reduced switching speed, and EMI caused by this parasitic inductance.

provided that the deadtime duration is controlled appropriately and the switch can turn off quickly enough, which may be challenging for large parts. State 3: Q_L turns on softly and the low-side on phase begins. State 4: Q_L, turns off and diode conduction occurs.

Method I: Interval Only

Fig. 5.6a shows the schematic and the modulation diagram for Method 1. The decoupling device is labeled Q_D. It is placed in parallel with Q_H because the high-side transistor has hard transitions in a buck converter (in a boost topology, the decoupling device would be connected parallel to the low-side power transistor). The decoupling device operates only during the switching intervals, and remains off during the rest of the period. For this method, there are 8 separate states of circuit operation. State 1: Normal high-side on phase. State 2: Q_D turns on so that it can carry the full load current during the high-side turn-off transition. State 3: Q_H turns off softly because Q_D maintains current conduction. State 4: Q_D turns off very fast with little overlap loss as a result of a highly compact gate drive loop and small commutation loop inductance, L_{SMALL} (highlighted in green in Fig. 5.6a). Subsequently, as with the conventional buck, the output capacitances of Q_H and Q_L are soft-charged and

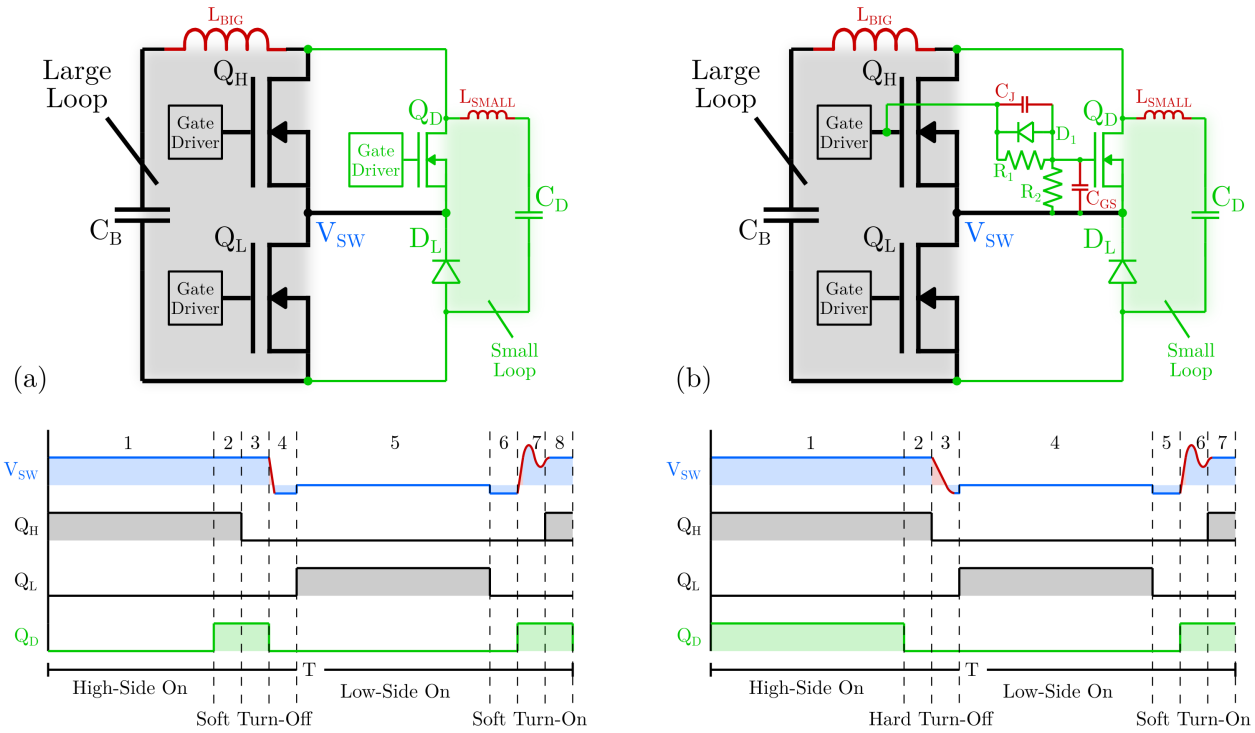


Figure 5.6: Schematic and modulation diagram for each decoupling device method. Main loop shown in black, decoupling loop in green, and parasitic components in red. (a) Method 1: Requires separate gate driver and two on-times for Q_D, (b) Method 2: Gate signal voltage divider utilized so only one high-side gate driver is needed.

discharged, respectively, with low loss until the switch node, V_{SW}, reaches zero volts and diode D_L begins conducting. State 5: Normal low-side on phase. State 6: Q_L turns off and diode D_L resumes conduction for the allotted deadtime duration (ideally short for reduced losses). State 7: Q_D turns on and initiates fast rise in switch node voltage, with low overlap loss or overshoot due to L_{SMALL}. State 8: Q_H turns on softly because Q_D is already on and begins to conduct the load current. The decoupling switch is not sized to carry the full load current continuously, only during the short switching transitions, so it can be small and it does not require a heatsink. The gate signals of the main power transistors are unaffected by the addition of the decoupling switch, but Q_H now turns on and off softly, and the switching transitions are much faster than what is achievable with only the large commutation loop, leading to reduced overlap loss. One major drawback of this method is that the decoupling switch requires its own high-side gate driver and PWM signal. This adds cost and complexity, but brings improvements in efficiency which in many applications may be preferred.

Method II: Fully Parallel

An alternative option is to utilize the same gate signal for both Q_H and Q_D. GaN HEMTs and Silicon FETs have different optimal gate drive voltages, however, so 3 small surface-mount passive components must be added to divide the gate signal down. In this case, the only added circuitry is Q_D and these passives (along with D_L and C_D, which are often utilized even without a decoupling device). Fig. 5.6b shows the schematic and modulation for this option. Q_D will naturally turn on before Q_H, due to its much lower gate capacitance and package inductance. It will also turn off before Q_H, producing no altering effect. However, as previously noted, the high-side turn-off transition is inherently soft in a buck converter, and thus the high-side turn-on is much more important for efficiency. With Method I, the switch could be sized very small because it does not carry the load current for long. For Method II, Q_D must be sized with sufficiently large R_{DSON} so that Q_H carries most of the current when both Q_D and Q_H are on, but it cannot be so large that it creates excess loss or heat while it carries the full load current during the switching transition. In this work, the on-resistance of Q_D is chosen to be approximately 10x that of Q_H. State 1: Normal high-side on phase. State 2: Q_D turns off before Q_H (due to smaller $R_{Gate}C_{ISS}$ time constant). Here, D_1 enables this fast turnoff by the gate driver. State 3: Q_H is turned off slowly due to L_{BIG} and diode-conduction dead-time occurs. State 4: Normal low-side on phase. State 5: Diode-conduction dead-time after Q_L turns off. State 6: Q_D turns on before Q_H and initiates fast rise in switch node voltage, with little overlap loss and minimal overshoot or ringing due to the small commutation loop inductance, L_{SMALL}. The junction capacitance of D_1, C_J, is sized such that it forms a high-frequency voltage divider with the input capacitance of the decoupling device, C_{GS}. R_1 and R_2 form the low-frequency portion of the divider. Together, these components allow for the GaN switch to be driven at any voltage level lower than the Silicon gate drive voltage, with minimal delay. State 7: Q_H turns on softly because Q_D is already on.

Table 5.2: Hardware Prototype Component List

Component	Part Number	Parameters
Main Power Transistors (Q_H,Q_L)	IXYS IXFH180N20X3	200 V, 6.3 mΩ
Decoupling Device 1 (Q_{D1})	EPC 2207	200 V, 22 mΩ
Decoupling Device 2 (Q_{D2})	EPC 2012C	200 V, 100 mΩ
Bulk Capacitors (C_{IN})	TDK CGA9P3X7T2E225K250KA	250 V, 2.2 uF
Decoupling Capacitors (C_D)	TDK C2012X7T2W473K125AA	450 V, 47 nF
Anti-Parallel Diode (D_L)	Vishay V3P22HM3/H	200 V, 3 A
Gate Driver	TI LM5114A	5 V, 7.6 A

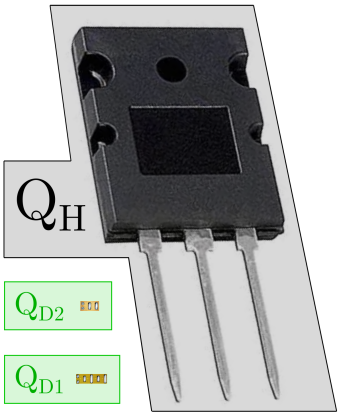


Figure 5.7: Demonstrating size difference between the main power and decoupling devices.

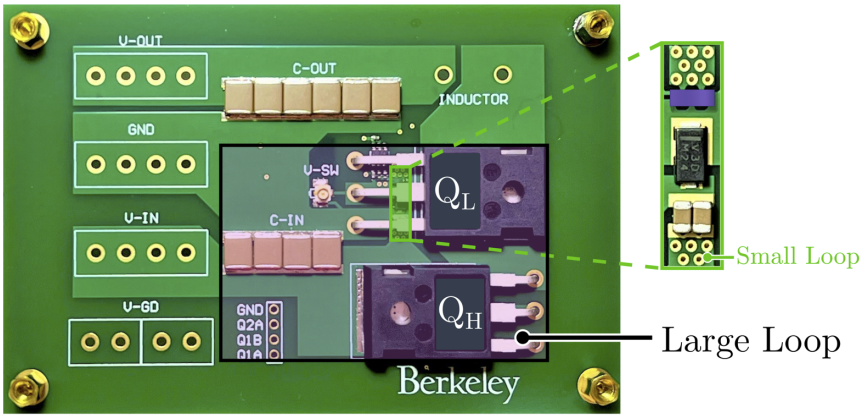


Figure 5.8: Annotated picture of hardware used for measurements. Large commutation loop of Q_H, Q_L, and C_{IN} highlighted. Small commutation loop of Q_D, C_D, and D_L shown in green inset.

Results

A 50 V, 250 W buck converter is designed to assess the merit of the proposed decoupling device and corresponding gate drive circuit. Fig. 5.8 shows an annotated picture of the hardware. The main power transistors are placed very close together, with the drain tabs soldered onto the PCB. This provides the lowest possible commutation loop inductance for the large loop, and real designs (e.g. with the power transistors mounted to heatsinks) could see far worse performance if decoupling is not employed. Q_D, C_D, and D_L are placed underneath the leads of the low-side device, as shown in the inset of Fig. 5.8, with a hybrid layout [94, 48] to minimize the small loop inductance as well. Fig. 5.7 highlights the dramatic difference in size for the decoupling devices utilized in this work (chip-scale land grid array package) versus the main power transistors (TO-247 package). Table 5.2 lists the components used. Efficiency measurements with forced air cooling are taken at a switching frequency of 50 kHz, as shown in Fig. 5.11 and Fig. 5.12, comparing operation without the decoupling device, Method I with an EPC2207 used for Q_D, and Method II with an EPC2012C as Q_D. As can be seen, up to a 55% reduction in power loss can be achieved when the proposed decoupling is employed. Fig. 5.9 shows the switch node, input, and output voltage, while Fig. 5.10 demonstrates the drastic decrease in rise time afforded by this technique.

Conclusion

This paper has presented a circuit design which places a small GaN HEMT in parallel with the large Silicon through-hole power transistor to greatly reduce the commutation loop inductance and increase the switching speed. Two different gate drive schemes are

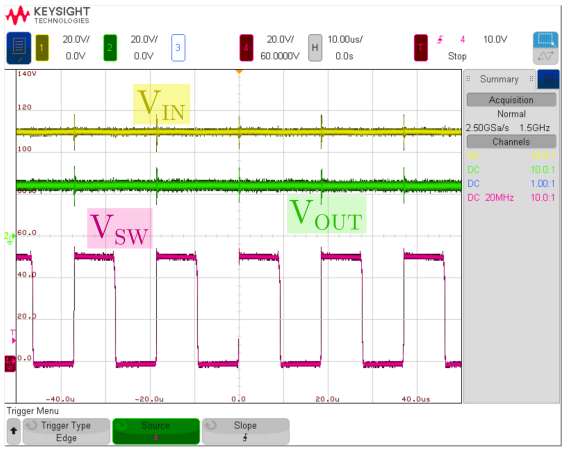


Figure 5.9: Measured switch node and output voltage waveforms.

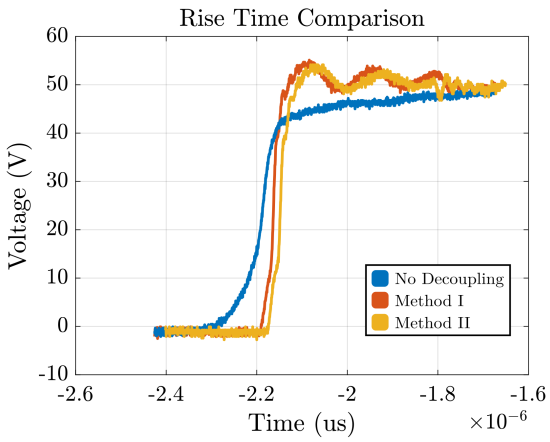


Figure 5.10: Measured rise times for each method.

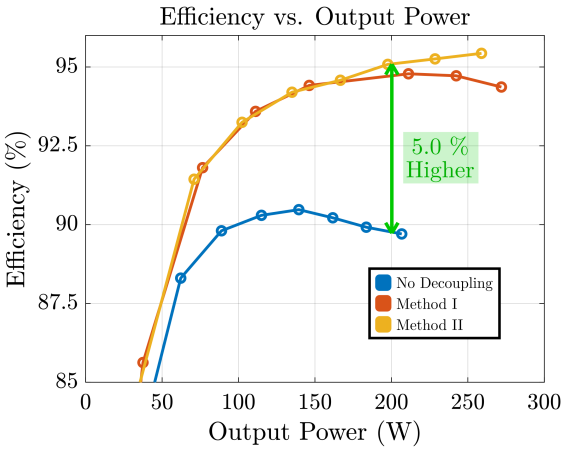


Figure 5.11: Measured efficiency data across output power.

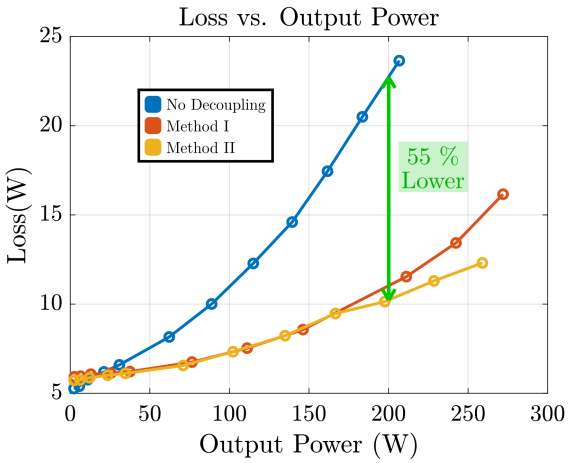


Figure 5.12: Total converter loss across output power.

explained and then compared experimentally in a 50 V, 250 W buck converter. For both methods, significant improvements in efficiency were realized. More than 50% of the losses were eliminated with the decoupling device added. Method 1 allows for fast turn-on and turn-off switching transitions. Method II does not require an added gate signal or driver, but still achieved very similar efficiency results to Method I, so it provides good performance with minimal added complexity and cost.

Chapter 6

Thermal Management

As electric vehicles (EVs) and data centers push the boundaries of performance and efficiency, they are also confronting a critical thermal challenge: rapidly increasing power densities and heat fluxes. In EVs, power electronics such as inverters, onboard chargers, and battery systems must manage high currents and switching speeds within compact, lightweight packages. Similarly, data centers are deploying increasingly dense servers and high-performance computing units that generate substantial heat in confined spaces. In both domains, traditional air-cooling methods are becoming insufficient to maintain optimal thermal conditions, threatening system reliability, efficiency, and longevity.

To address these challenges, the industry is undergoing a significant shift toward more advanced thermal management strategies—most notably, liquid cooling. In data centers, liquid cooling solutions such as direct-to-chip cold plates and immersion systems offer superior heat removal capabilities, enabling higher server densities and reducing overall energy consumption for cooling infrastructure. In EVs, liquid cooling is now commonly applied to batteries, power electronics, and traction motors to ensure consistent performance under dynamic load conditions and wide ambient temperature ranges.

The move toward liquid cooling in both EVs and data centers reflects a broader trend: thermal management is no longer a passive concern but a central enabler of progress. As power and performance demands continue to grow, efficient and scalable cooling solutions are essential for unlocking the next generation of mobility and computing technologies.

6.1 Cooling Solutions

The simplest and most widely used method for cooling is forced air convection, where fans drive airflow across electronic components to enhance heat transfer. When used in conjunction with a heat sink, which increases surface area and directs thermal energy away from hot spots, the effectiveness of air cooling improves significantly. However, as heat fluxes approach or exceed the practical limits of air-based systems, liquid cooling using cold plates becomes a compelling alternative. These systems circulate a coolant through a metal plate in contact

with high-power components, offering a much higher thermal conductivity and heat transfer capacity. For the most thermally demanding environments—such as data centers hosting high-density computing clusters or power electronics in electric vehicles—liquid immersion cooling is emerging as a next-generation solution. In this approach, components are fully or partially submerged in a dielectric fluid, allowing direct, uniform heat removal from all surfaces and eliminating the need for complex heat sinks or cold plates.

Each of these methods represents a step forward in thermal performance, with trade-offs in complexity, cost, and infrastructure. As electronic systems evolve, especially in sectors like automotive and computing, the choice of cooling strategy becomes a defining factor in system architecture and scalability.

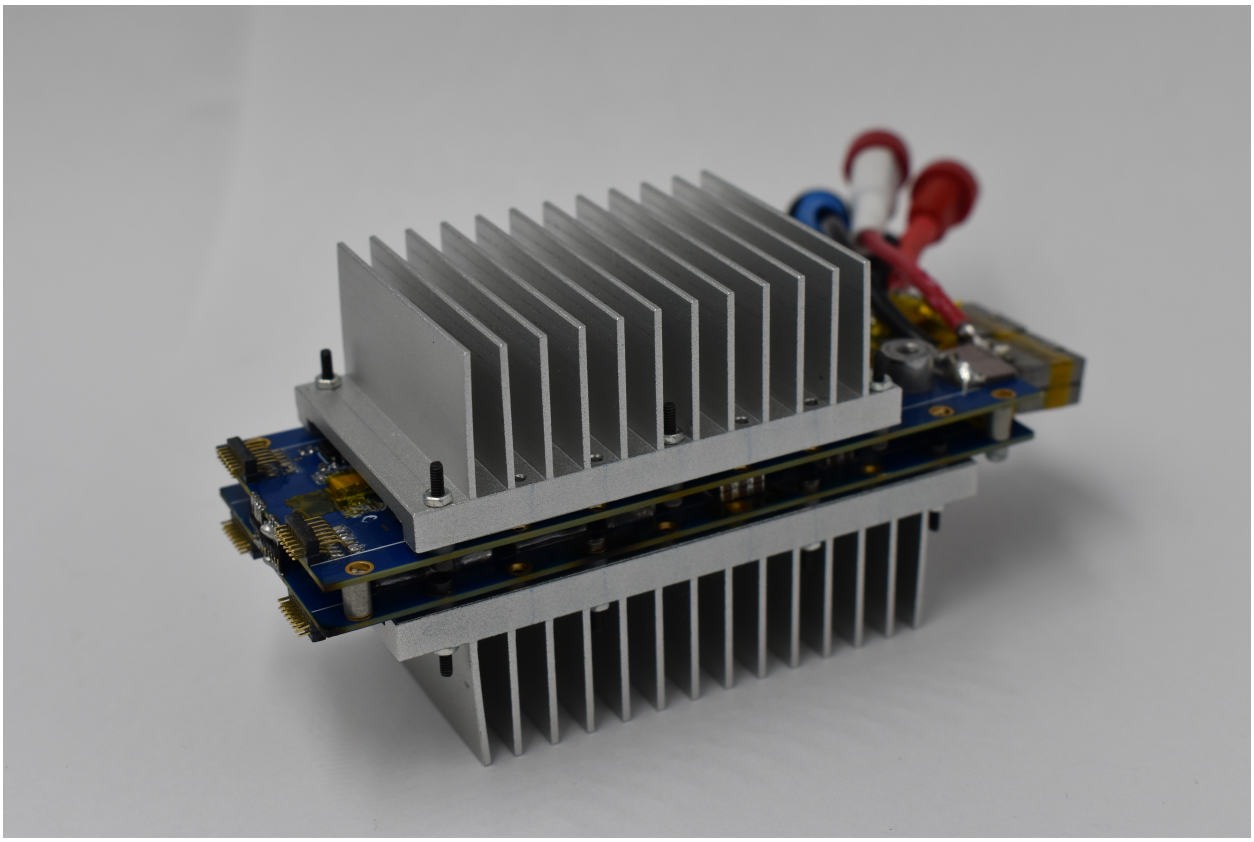


Figure 6.1: Photograph of inverter prototype with attached monolithic heat sinks. An insulating gap pad is placed between the transistors and the heat sink to prevent electrical short circuits.

Forced Air

Forced air convection is the most broadly used cooling technique because of its simplicity and reliability. In contrast to subsequent approaches, there is no mating between different materials. This elimiates concerns for coefficient of thermal expansion (CTE) mismatch, pump-out of thermal pastes, degradation of thermal interface materials (TIMs), uneven mounting pressure, excess mounting pressure, or insufficient mounting pressure. Also, air cooling may be considered more reliable than liquid cooling because it avoids concerns for leaks, corrosion, biological growth in the fluid, particles in the fluid causing excess erosion, and the need for water-tight pumping/tubing. All of the FCML inverter hardware prototypes presented in the next chapter were tested with this cooling method.

Forced Air with Heat Sink

The addition of a heat sink significantly alters system design. All power converters feature multiple switching devices at different voltage potentials. For top-side cooled devices, the top surface of the package is exposed for cooling, but is usually electrically shorted to a node (either the drain or source) of the transistor to minimize thermal resistance between the junction and case. This creates limitations, though, for the cooling system because if different devices are placed in direct contact with an electrically conductive surface (such as a metal heat sink), they would short-circuit and the system would fail. Instead, there needs to be an electrically insulating layer between any conductive surface and the transistor packages. This is a serious impediment to high-performance thermal management design. In general, electrically conductive materials are thermally conductive and vice versa. Therefore, in order to to minimize thermal resistance, conductive materials are still primarily used. The short-circuit problem has been addressed in a few different ways.

An electrically insulating gap pad may be placed between the transistors and the metal heat sink, enabling the use of a single, monolithic heat sink for all of the transistors. This provides a very simple, cost-effective solution with considerably higher performance than without the heat sink. Fig. 6.1 shows a hardware photograph of an inverter prototype mounted to monolithic heat sinks on the top and bottom. The gap pad will typically have a thermal conductivity (<20 W/mK) far lower than metal, however, and will bottleneck the thermal performance of the system. Thinner, or more thermally conductive pads (such as graphite) will be less compliant, thus hindering reliability.

To avoid this constraint, an alternative approach is to use an individual heat sink for every transistor. The gap pad can thus be removed, and the heat sink may be mounted directly to the devices along with a thin layer of thermal paste to ensure good connection. This improves thermal performance because the thermal resistance of the gap pad is eliminated, but many new complexities are introduced. First, the converter must accommodate many more mounting holes around each of the devices. For high-density designs, this can significantly increase converter size. Second, the cost and complexity increases dramatically because the number of heat sinks and mounting assemblies is much higher. Third, each indi-

vidual heat sink will be much smaller, which diminishes some performance benefits realized from the removal of a gap pad. Fourth, reliability is a concern with so many separate mounting assemblies and great care must be taken during production. Despite these challenges, it has been shown that a significant performance increase can be realized by moving toward this modular heat sinking approach [84].

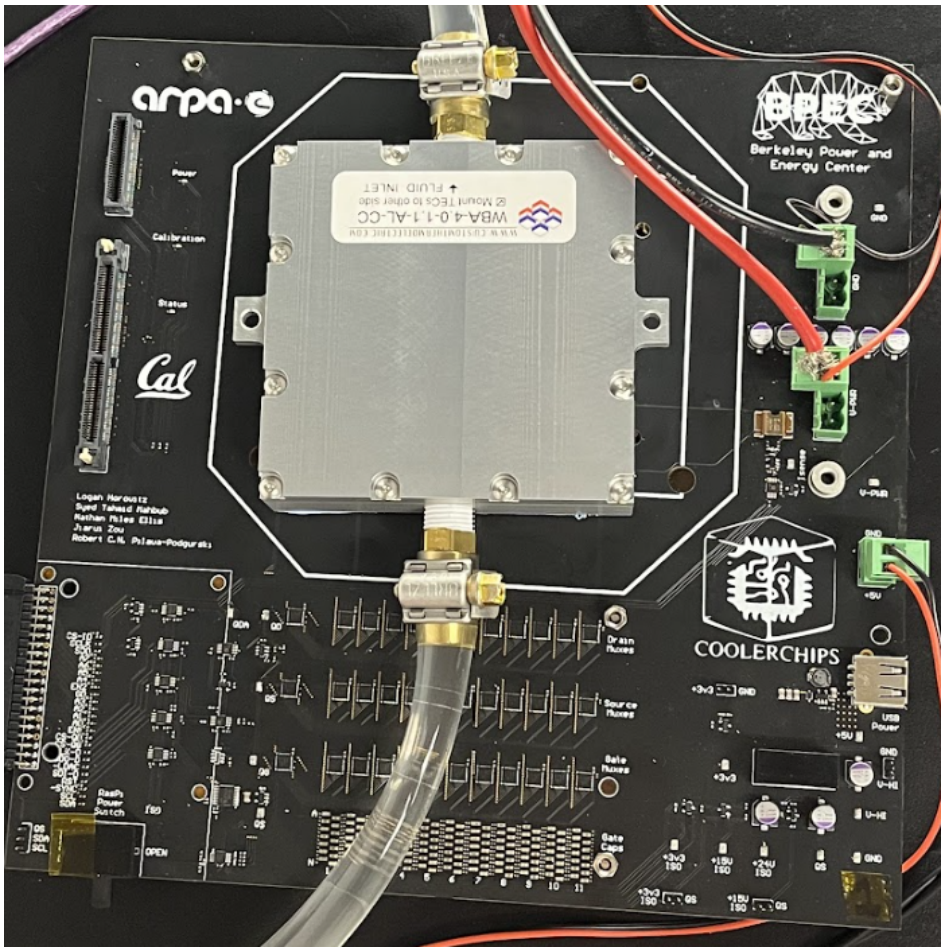


Figure 6.2: Photograph of electronic system with liquid cold plate mounted on top. Inlet and outlet tubes are clearly visible. An electrically insulating gap pad is used to prevent short-circuits.

Liquid Cooling with Cold Plate

Liquids have the potential to remove a much higher heat flux due to the larger specific heat and thermal conductivity of the working fluid. An analogous approach may be taken to the monolithic heat sink with forced air convection, whereby a monolithic liquid cold plate

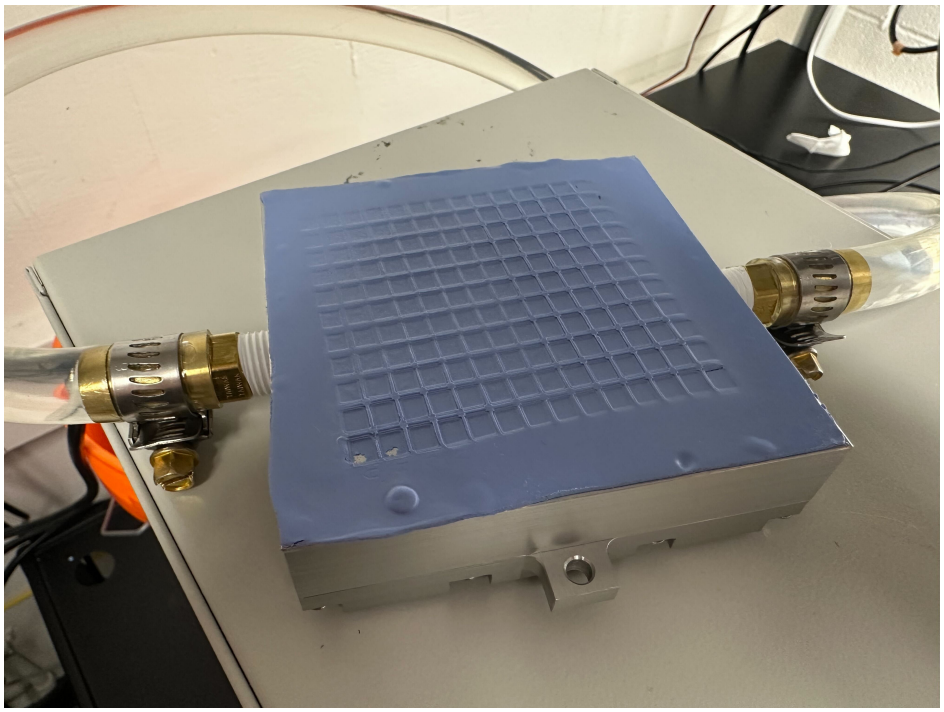


Figure 6.3: Photograph of insulating gap pad after removal from liquid cooling setup. There is a noticeable difference in the amount of compression each transistor sees, indicating that thermal performance will not be uniform across devices.

mounted to the transistors. Again, an electrically insulating gap pad will be necessary to prevent short-circuit between the devices. The reliability and cost of this system will be worse than air-cooling, but the efficiency is much higher. The weight and volumetric density will be reduced as well, and the large inlet and outlet tubes in Fig. 6.2 will take up even more volume. Fig. 6.3 shows indentations in the gap pad after removal from the system. It can be seen that there is a significant disparity in the depth of indentation between different devices, indicating varying thermal resistances. This is a serious concern for long-term reliability of the system, and therefore represents a weakness of this monolithic mounting approach.

Liquid Immersion Cooling

The form factor of aforementioned cooling solutions is insufficient. Upon looking at Fig. 6.1, it is immediately obvious that the size and weight of the heat sink will be non-negligible. Despite the fact that this heat sink design was painstakingly optimized, it is still larger and heavier than the converter itself. In order to continue pushing the forefront of advanced converter design, we need to reimagine the cooling solutions as well.

Immersion cooling consists of directly bathing active components in the working fluid. The same concern for electrical shorts arises, necessitating the use of electrical insulation

somewhere. One approach has been to use dielectric (electrically insulating) fluids. Many companies have developed special engineered fluids with improved thermal conductivity and a low boiling point (e.g. 45 degrees Celsius) so two-phase solutions may be considered (unlike the 100 degree Celsius boiling point of water, which is prohibitively high for data center electronics). Unfortunately, all of the fluids developed to date are significantly worse than water across many dimensions: worse thermal conductivity, worse specific heat, worse for the environment, more expensive, more difficult to source, etc. Water would be the ideal working fluid because it is abundant, non-toxic, and offers very good thermal properties. Water is electrically conductive, however, which has traditionally prohibited its use in these applications.

Our collaborators have proposed a different approach: coat the electronics with a thin layer of dielectric material, and then perform liquid immersion cooling with water. In theory, this offers many attractive benefits: the coating can be extremely thin and therefore low thermal resistance, immersion cooling is high-performance, and water is the ideal fluid. In practice, there are many challenges. Developing a coating material which is simultaneously conformal enough to coat the electronics with a watertight seal, robust enough to deal with thermal expansion and contraction, electrically insulating, and highly thermally conductive, is very challenging. Moreover, erosion and corrosion concerns are dire because the coating thickness is typically on the order of microns. To address these issues, an improved approach was proposed [37]. First, the electronics are coated with a thin layer of parylene C, which is known to be highly conformal, and is the most common material utilized for these applications. Next, a multi-step process is used to coat a layer of copper on top of the parylene. This copper acts as a heat spreader and an erosion barrier for the thin dielectric layer. Various thicknesses of copper were explored ranging up to 600 microns. Overall, it was demonstrated that similar or superior (for thicker copper coating) thermal performance can be achieved compared to a heat sink, with far lower volume and mass. Fig. 6.4 shows an example PCB which is coated in this manner. This cooling method fits the form factor of the converter far better, and may be considered a promising emerging cooling strategy.

Figure 6.4: Photograph of copper-coated power electronics converter.

6.2 Thermal Test Vehicles

As the adoption of liquid cooling accelerates in both electric vehicles and data centers, the development of reliable and effective thermal management systems becomes increasingly dependent on accurate, repeatable testing. This is where thermal test vehicles (TTVs) play a critical role. TTVs are engineered hardware platforms that mimic the thermal behavior of actual electronic components—such as power modules, CPUs, or battery cells—while providing a more convenient testing environment. They enable researchers, engineers, and thermal solution providers to evaluate the performance of cooling strategies under controlled and representative conditions.

In EV power electronics, TTVs are essential for validating cold plate designs, coolant flow configurations, and interface materials before integrating with costly silicon-based devices. Power modules in inverters, DC-DC converters, and onboard chargers operate under high-voltage, high-temperature conditions, where even small thermal inefficiencies can lead to reduced efficiency or premature failure. TTVs allow thermal engineers to replicate the heat flux profiles and spatial thermal gradients of these modules, facilitating detailed investigations of thermal resistance, pressure drop, and cooling uniformity across a wide range of operating scenarios—without risking real, expensive components.

In data centers, where cooling infrastructure accounts for a significant portion of operational energy use, TTVs are even more valuable. As facilities move toward liquid-cooled server racks and direct-to-chip cold plate configurations, it becomes critical to assess system-level performance prior to deployment. TTVs designed to emulate CPUs, GPUs, or other heat sources allow for systematic evaluation of coolant distribution, thermal contact quality, and transient thermal response. These test platforms also help identify integration issues and verify compliance with thermal specifications—key steps in reducing downtime, improving energy efficiency, and accelerating time-to-market for liquid-cooled server architectures. As shown in Fig.1, the thermal design power (TDP) of data center GPUs has tripled in recent years, while server-class CPUs have also experienced a dramatic TDP increase [104, 53]. Meanwhile, high-speed network equipment and high-density voltage regulation modules (VRMs) further contribute to the cooling burden within the constrained server environment [117, 124].

Ultimately, TTVs serve as a vital bridge between thermal design and real-world deployment. They offer a safe, scalable, and repeatable approach to optimizing cooling technologies, supporting the transition to higher power densities and more sophisticated thermal solutions in both mobility and cloud computing sectors.

Thermal Test Vehicle Requirements

The purpose of a TTV is to mimic the thermal operating conditions of a commercial GPU or CPU, while providing an accessible testing environment to assess performance of the cooling solution [105]. There are three main aspects to this:

1. **Heat Generation:** The system must be capable of generating very large amounts of heat (kW scale for modern and emerging computing platforms) in a small surface area ($< 100\,\mathrm{cm}^2$) with a controllable spatial and temporal profile.

2. **Temperature Sensing:** Accurate temperature measurements should be recorded at the surface of the heater with good spatial fidelity.

3. **User Interface:** Users should be able to quickly and easily specify operating conditions for tests such as power levels, hotspots, and duration. Data collection and transmission should be amenable to integration within existing testing platforms.

Existing Commercial Solutions

It is possible to test cooling systems with the end-use electronics themselves, such as an actual data center server blade, but high-performance commercial servers are extremely expensive and inflexible. There are also strict limitations in the amount of heat that can be generated before the server shuts down, and there is typically little control of how the heat is localized spatially along the surface.

An alternative approach is to use an array of mechanical heaters, such as copper pads, and to conduct current through them to dissipate power. Each heater is usually fairly large, however, so the heat cannot be localized acutely. Moreover, a complex mechanical assembly is required to extract the operating temperature. If each heater in the array is individually addressable, it will require its own temperature sensor and power supply, which drastically increases the complexity and cost.

Another option involves designing application specific integrated circuits (ASICs) to simultaneously perform heat generation and temperature sensing [10, 55, 111, 107, 12]. This technology is very expensive to develop and difficult to scale to large enough size and power levels. Additional circuitry would be required to communicate between ICs, which would complicate the electrical design.

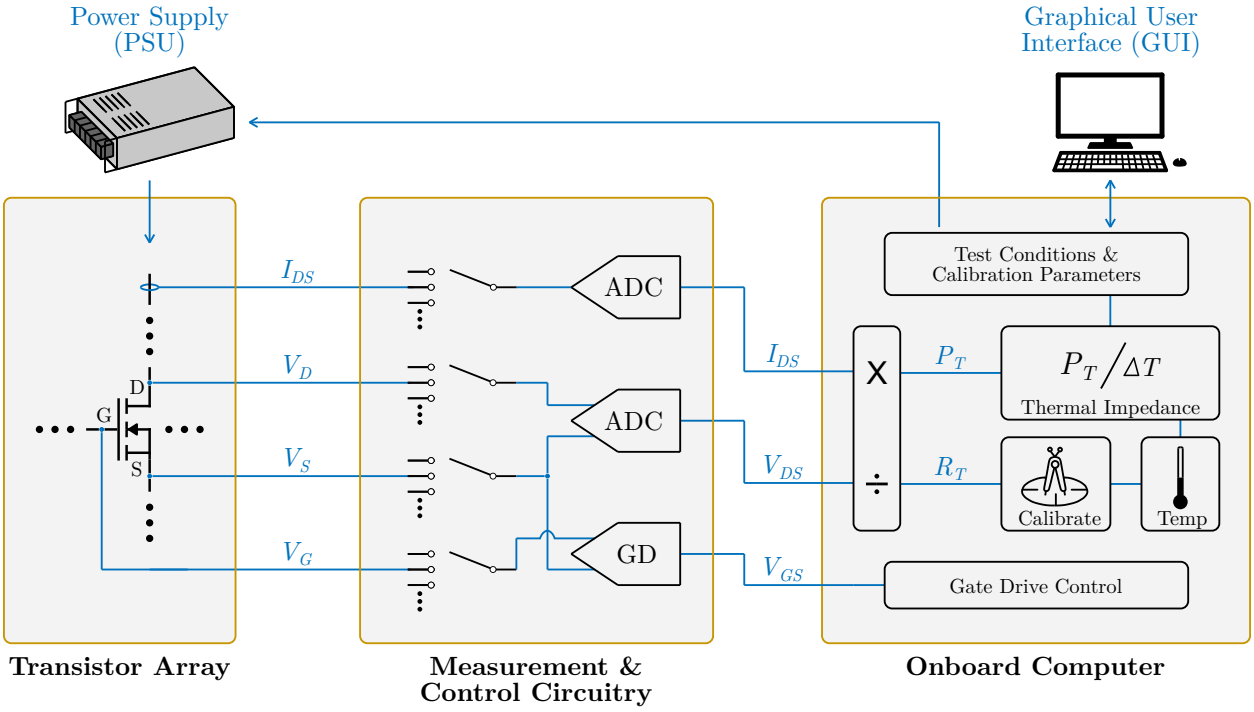


Figure 6.5: Overall schematic for the proposed thermal test vehicle design approach. The three main aspects are an array of power transistors, measurement/control circuitry, and onboard computer.

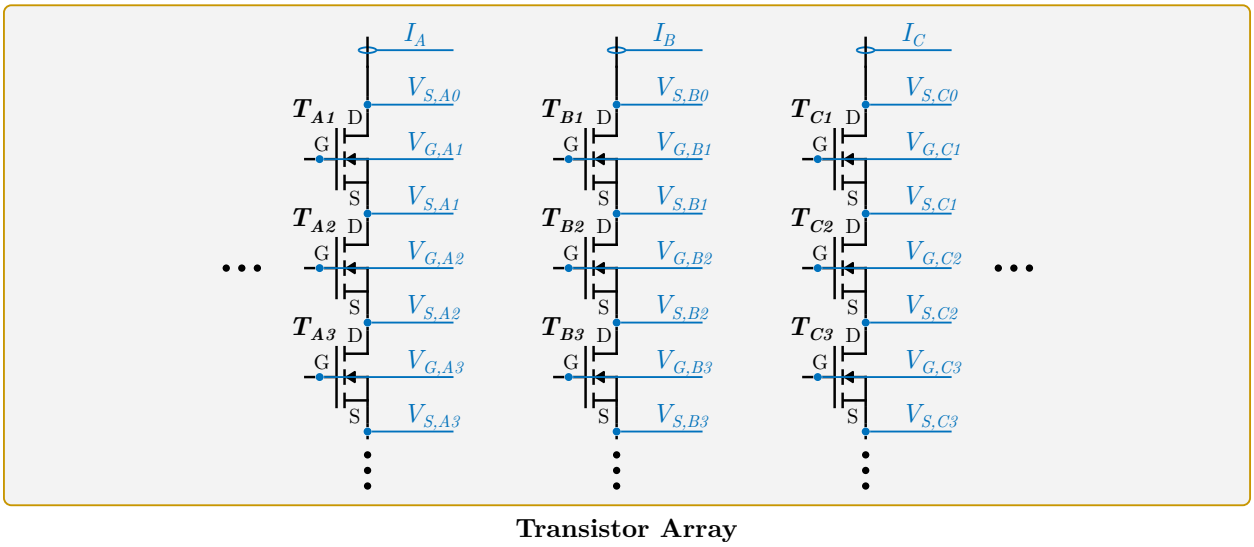


Figure 6.6: Detailed schematic showing the transistor array. The drain-to-source current (I_{DS}), drain voltage (V_D), gate voltage (V_G), and source voltage (V_S) of each transistor are connected to the measurement/control circuitry.

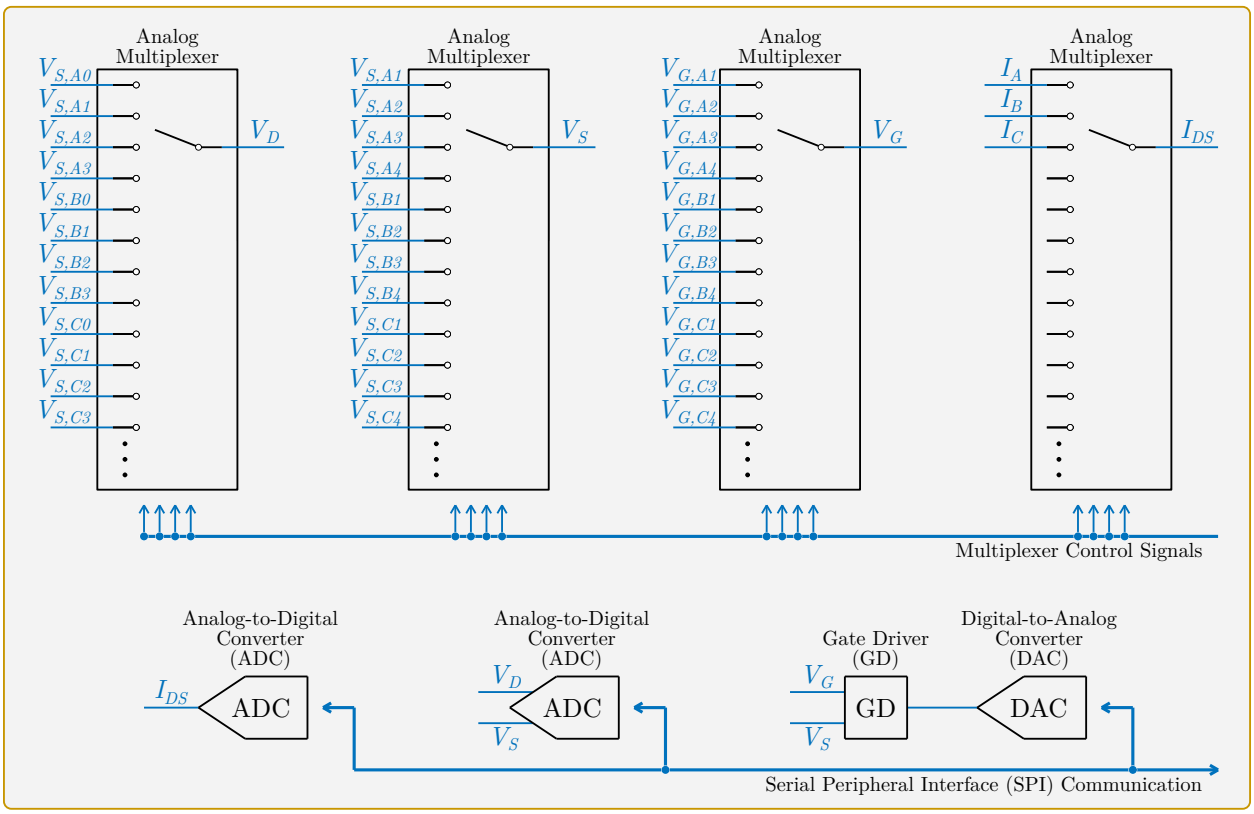


Figure 6.7: Detailed schematic showing the measurement and control circuitry. The transistor signals are connected through analog multiplexers so they can be sampled individually. Analog-to-digital converters (ADCs) are used to measure I_{DS} and V_{DS}, while a digital-to-analog converter (DAC) is utilized to generate V_{GS}.

Proposed Approach

Fig. 6.5 provides an outline of the proposed design, highlighting the three main sections: transistor array, measurement/control circuitry, and onboard computer.

Transistor Array

A power supply (PSU) is used to conduct current through an array of power transistors, thus generating heat due to conduction losses. Fig. 6.6 shows a detailed schematic with relevant signals. The number of transistors and size of each individual transistor can be adjusted. This provides a great deal of flexibility in implementation, such that the TTV can be modified to match the dimensions of a desired commercial GPU or CPU. The total power generated by the array may be adjusted by controlling the output current of the PSU. Each

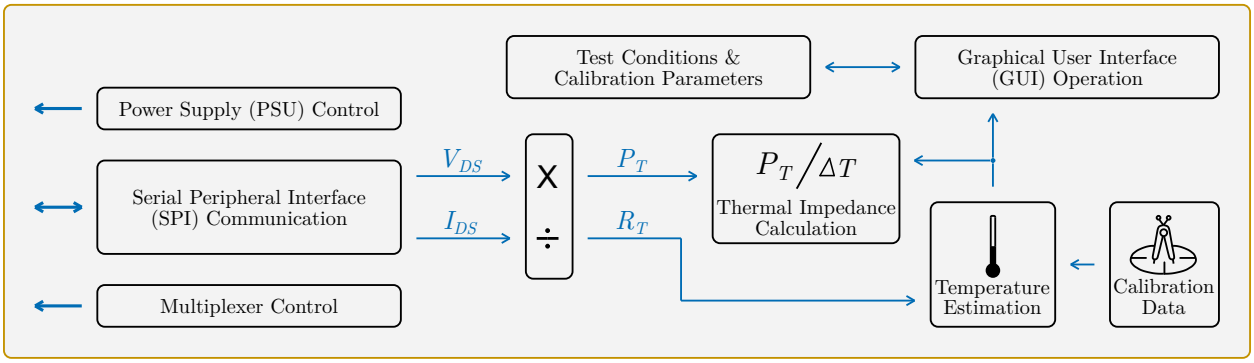


Figure 6.8: Detailed schematic showing operations of the onboard computer. Based on test conditions specified in the graphical user interface (GUI), appropriate control signals are generated for the power supply, SPI communication, and analog multiplexers. Measured results are used to estimate thermal performance. which is reported by the GUI.

transistor acts as a variable resistor, so there is individual control of the power dissipated in every device. This enables the generation of custom heat maps, hot spots, and pulsed power profiles which can mimic a desired testing scenario. For each device, the drain-to-source current (I_{DS}), drain voltage (V_D), gate voltage (V_G), and source voltage (V_S) are connected to the analog multiplexers of the measurement/control circuitry.

Measurement/Control Circuitry

Fig. 6.7 provides a schematic of the measurement and control circuitry. Signals from the array connect through analog multiplexers, such that each transistor can be addressed individually. A digital-to-analog converter (DAC) generates the gate drive voltage, while analog-to-digital converters (ADCs) are used to record I_{DS} and V_{DS}. The power dissipated by the transistor (P_T) is computed by multiplying these values, while its on-resistance (R_T) can be found by dividing them.

$$P_T = V_{DS} \cdot I_{DS} \tag{6.1}$$

$$R_T = V_{DS}/I_{DS} \tag{6.2}$$

The on-resistance of a transistor is temperature-dependent, so the junction temperature of each device (T_T) may be extracted as a function of the measured on-resistance and applied gate-to-source voltage (V_{GS}).

$$T_T = f(R_T, V_{GS}) \tag{6.3}$$

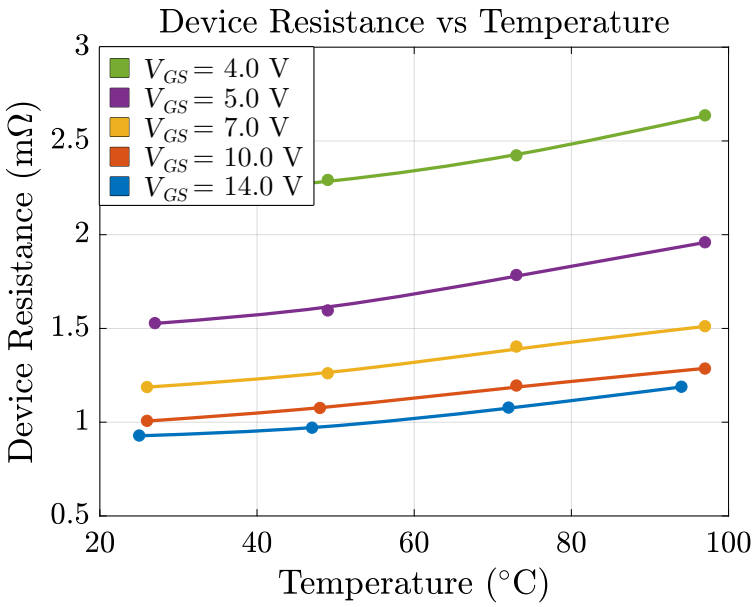


Figure 6.9: Measured device resistance as a function of temperature for different applied gate-to-source voltages. These trends enable temperature estimation and controllable power dissipation in every transistor.

Fig. 6.9 illustrates measured results for the on-resistance of the devices used in this work as a function of temperature and gate-to-source voltage. This enables temperature estimation with good spatial fidelity, without requiring additional mechanical assembly. The system only requires a single power supply, one gate driver, and two high-precision ADCs, which significantly reduces complexity, component count, and cost. The use of standard, commercially available components also lends to a large reduction in cost compared to existing solutions.

Onboard Computer

A small, onboard computer is included to handle all of the low-level control, store calibration data, and to provide an accessible interface. It can be connected directly to a computer monitor where a graphical user interface (GUI) will enable users to specify testing profiles and heat maps. This enables live data collection and visualization. Fig. 6.10 shows an example where a user can select from three different heat maps, and the temperature of every transistor is displayed with color-mapping. Serial peripheral interface (SPI) protocol is utilized for communication with the measurement circuitry, while digital control signals set the analog multiplexer outputs. The measured resistance of each transistor (R_T) is used to estimate its temperature, along with stored calibration data. Fig. 6.8 shows the main operations of the onboard computer.

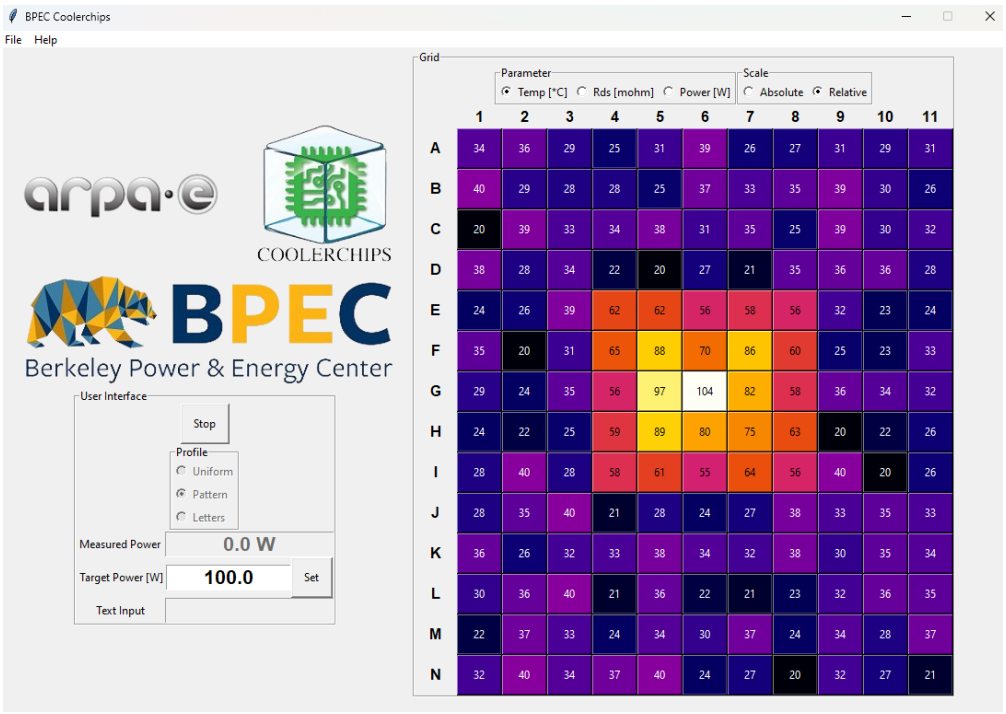


Figure 6.10: Graphical user interface enabling the selection of different thermal test profiles and live visualization of measured characteristics.

Conclusion

Thermal challenges in data centers have been growing rapidly. To address these concerns, high-performance cooling solutions must be developed and tested. This work proposes an affordable, highly flexible, and scalable TTV design using an array of power transistors, associated measurement circuitry, and onboard computer. Overall, the proposed approach offers the following features:

- High power and high heat flux
- Flexible, scalable, affordable design
  - Standard commercial components
  - Standard contract manufacturing
- Simple setup
  - Single power supply
  - No external temp. sensors
  - No programming required

Chapter 7

Hardware Demonstrations

7.1 FCLLC Converters

Gen I

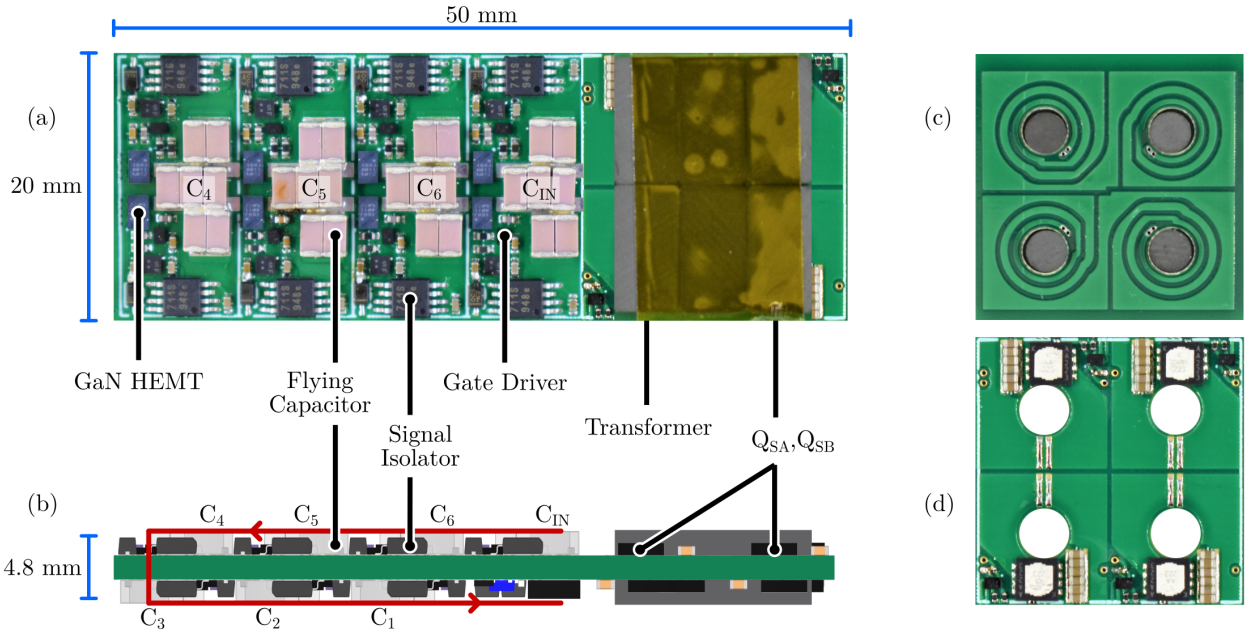


Figure 7.1: Hardware photograph of proposed 8-level 400 V to 1 V FCLLC converter with matrix transformer inset to PCB. Key components are annotated, with the power path shown in red. (a) Top view, (b) Side view, (c) Primary windings of transformer, (d) Secondary windings and output rectification.

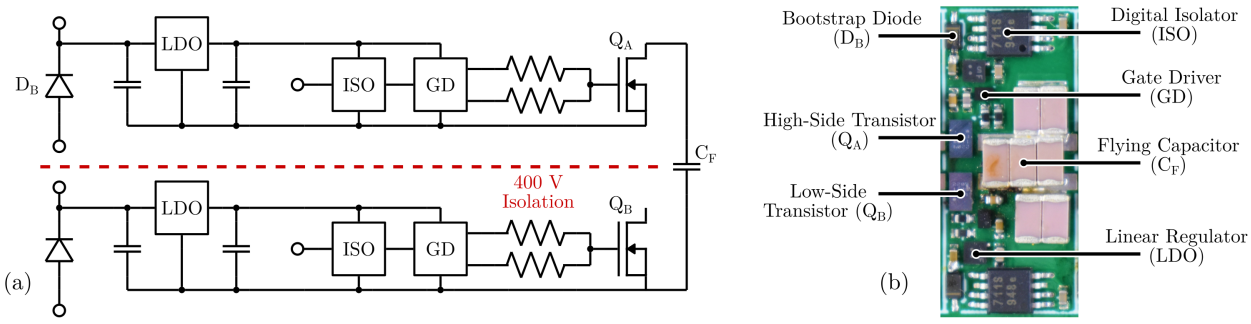


Figure 7.2: Cascaded bootstrap gate drive architecture for 8-level FCLLC design. (a) Detailed schematic for unit cell highlighted in Fig. 3.9c, (b) Layout of unit cell with annotated components. $(N-1)$ of these cells are connected in series to form the primary side of the converter.

Hardware Design

To validate the proposed topology and application, a 400 V to 1 V, 8-level FCLLC converter is fabricated ($M_{\text{FCML}} = 1/14$). An annotated hardware photograph is given in Fig. 7.1. Chip-scale packaged gallium-nitride high-electron mobility transistors (GaN HEMTs) are used due to their superior figure-of-merit (FOM) versus silicon transistors at this voltage level [6]. A cascaded bootstrap power supply architecture is used to power all of the floating gate drivers with low dropout regulators (LDOs) ensuring a reliable 5 V supply for the GaN switches [120]. Digital signal isolators provide the level-shifted gate signals. Fig. 7.2 illustrates the gate drive architecture and details all of the components for each unit cell; the 8-level converter contains $(N-1) = 7$ of these cells connected in series.

A planar matrix transformer is utilized to maximize power density and reduce manufacturing complexity, with detailed design guidelines of one such implementation provided in [34]. The transformer is inset to the PCB such that its height is level to rest of the components. A 24-to-1 turns ratio is selected, so $M_{\text{LLC}} = \lambda/24$. The parameter λ is selected such that the overall conversion ratio is $M_{\text{FCLLC}} = 1/400$, i.e. this design choice is suitable for direct 400 V to 1 V conversion when operated slightly above resonance. The power path wraps around the board, beginning at C_{IN} next to the transformer, continuing to the left before going through vias and returning along the bottom of the PCB (illustrated by red arrow in Fig. 7.1). Relevant components are provided in Table 7.1, while operating parameters are given in Table 7.2. The converter box dimensions are 20 mm by 50 mm by 4.8 mm, including all passive components, devices, and gate drive circuitry; the total box volume is 4800 mm^3.

Experimental Results

To demonstrate the converter operation, measurements at 400 V input and 1 V output have been collected, with relevant waveforms shown in Fig. 7.3. Efficiency measurements were

Table 7.1: FCLLC Component List

Component	Part Number	Parameters
Primary Switch	EPC 2204	100 V, 4.4 mΩ
Secondary Switch	ON NTTFS1D2N02P1E	25 V, 0.86 mΩ
Flying Capacitor	TDK CGA5L4C0G2W153J160AA	450 V, 15 nF
Output Capacitor	TDK CL05A226MQ5QUNC	6.3 V, 22 uF
Gate Driver	TI LMG1020	5 V, 7.6 A
Digital Isolator	NVE IL 711S-1E	1000 V
LDO	ON NCP715MX50TBG	5 V, 50 mA

Table 7.2: FCLLC Parameters

Parameter	Value
Input Voltage	400 V_{DC}
Output Voltage	1.0 V_{DC}
Switching Frequency	100 kHz
Peak Output Power	65 W
Peak Efficiency	81.5 %
Power Density	223 W/in^3

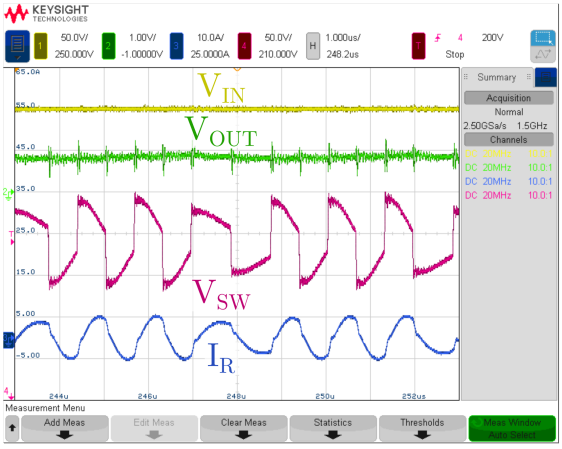


Figure 7.3: Measured waveforms for 8-level FCLLC prototype performing 400 V to 1 V conversion at full load.

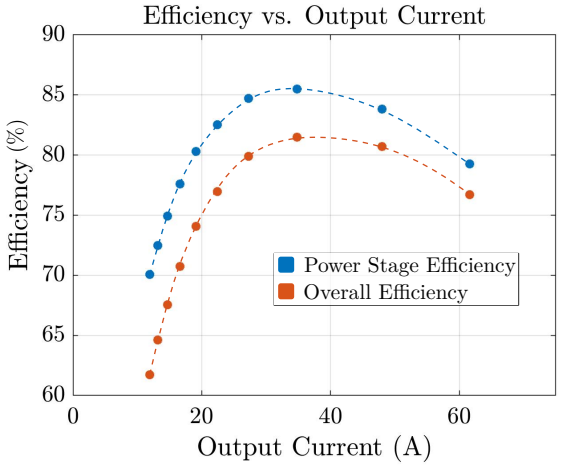


Figure 7.4: Efficiency measurements under 400 V to 1 V conversion across load. Power stage efficiency (excluding gate drive loss) and overall efficiency provided.

taken with forced air cooling and without heat sinking, as shown in Fig. 7.4. Peak efficiency is recorded at 85.5% for the power stage and 81.5% including gate drive losses. The full load efficiencies are 74.8% and 72.5%, respectively. The maximum output power of 65.4 W, yields a power density of 223 W/in^3. A comparison to state of the art designs in high conversion ratio data center applications is given in Table 7.3.

Table 7.3: FCLLC Comparison with State of the Art

Reference	Number of Stages	Stage Conversion Ratios	Stage Efficiencies	Stage Densities (W/in³)	Overall Conversion Ratio	Overall Efficiency	Overall Density (W/in³)
Vicor BCM [28] + Vicor PRM [29] + Vicor VTM [30]	3	384 : 48 48 : 48 48 : 1.2	96% 97.5% 90.4%	1106 1134 531	320	84.6%	272*
CPES LLC [22] + Flex BMR [31]	2	380 : 12 12 : 1	97.6% 90.5%	900 250	380	88.3%	195*
Vicor Mini [32]	1	375:2	74.6%	40	187.5	74.6%	40
Proposed FCLLC	1	400 : 1	81.5%	223	400	81.5%	223

* Power density for multi-stage designs does not include bus capacitors, so system density will be lower

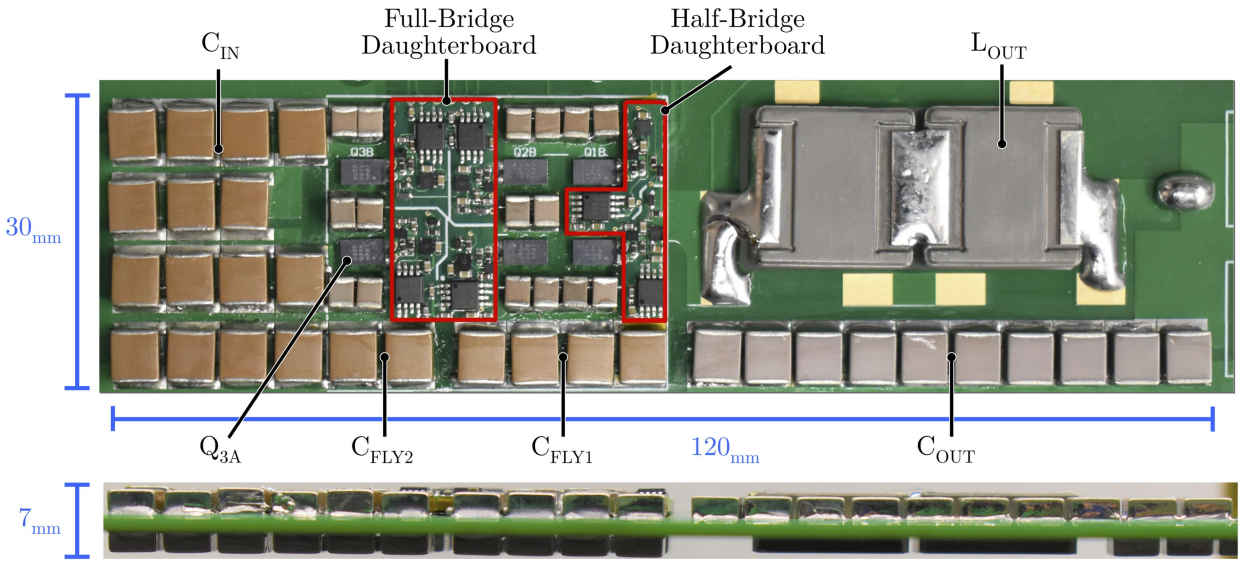


Figure 7.5: Layout of 4-level FCML converter with proposed switching cells utilizing gate drive daughterboards.

7.2 FCML Inverters

Gen I

A 4-level FCML was designed and fabricated, as shown in Fig. 7.5. The motherboard is 6 layers and 1.6 mm thick. Blind and buried vias are used for the electrically thin routing. A cutout is utilized for the placement of the 2 series output inductors so that their height is level to the rest of the converter. Relevant components are listed in Table 7.4. The FCML

Table 7.4: Gen I Inverter Component List

Component	Part Number	Parameters
GaN HEMT	EPC 2034C	200 V, 6 mΩ
Bulk Capacitor	TDK C5750X6S2W225K250KA	450 V, 2.2 uF
Decoupling Capacitor	Kemet C1210X223JDGACAUTO	1000 V, 22 nF
Output Inductor	Bourns SRP1770C-6R8M	22 A, 6.8 uH
Output Capacitor	TDK CGA9N4C0G2E154J230KN	250 V, .15 uF
Gate Driver	TI LMG1020YFFR	5 V, 7 A
Digital Isolator	NVE IL 711S-1E	1000 V
LDO	ON NCP715MX50TBG	5 V, 50 mA

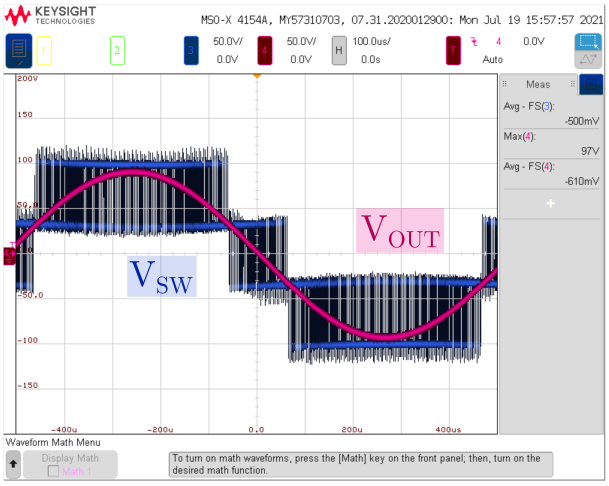


Figure 7.6: Waveform showing the switch node (Vsw) and output voltage (Vout) during light load. The DC input voltage is 200 V, the output is a 950 Hz, 64 V_{RMS} sine wave.

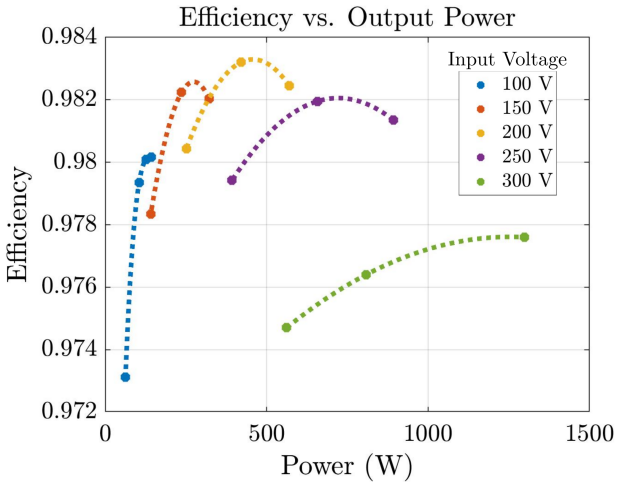


Figure 7.7: Converter efficiency (including gate drive losses) operating as an inverter under various DC input voltages and output powers. The output is a sine wave at 950 Hz with a peak amplitude of .45 times the input voltage.

is operated as an inverter with a 950 Hz sine wave output, which demonstrates the cascaded bootstrap gate drive functionality at a range from .1-.9 duty ratio. A split-bus design is used, so that the output has a peak amplitude of approximately .45 times the DC input voltage. The switching frequency of the devices is 115 kHz. Due to the frequency multiplication effect of the FCML, however, the output switching frequency is 345 kHz. Table 7.5 lists significant converter parameters. Efficiency measurements were taken for a range of input

Table 7.5: Gen I Inverter Parameters

Parameter	Value
Input Voltage	300 V
Output Voltage	95 V_{RMS}
Output Frequency	950 Hz
Peak Output Power	1.3 kW
Peak Efficiency	98.3 %
Effective Switching Frequency	345 kHz

voltages and output powers with forced air cooling and without heatsinking, plotted in Fig. 7.7. The converter achieves a peak efficiency of 98.3%, including gate drive losses, for a 200 V DC input voltage, 64 V_{RMS} sine wave output voltage, and a load current of 6.6 A. Peak power is recorded at 1.3 kW with an efficiency of 97.8%, for a 300 V DC input voltage, 95 V_{RMS} sine wave output voltage, and 13.8 A load current. The converter exhibits excellent passive balancing and low distortion, despite a small output filter size, as demonstrated by the waveforms in Fig. 7.6. The power density is computed using the peak power divided by the minimum-sized box volume which contains the converter (including power devices, gate drive circuitry, passive components, and output filter). This yields a volume of 100 mm x 30 mm x 7 mm, or 1.28 $inch^3$. Given a peak power of 1.3 kW, the power density is 1 kW/in^3.

Gen II

Table 7.6: Gen II Inverter Component List

Component	Part Number	Parameters
GaN HEMT	EPC 2302	100 V, 1.4 mΩ
Bulk Capacitor	TDK C5750X6S2W225K250KA	450 V, 2.2 uF
Decoupling Capacitor	TDK C2012X7T2W473K125AA	450 V, 47 nF
Output Inductor	Vishay IHLP6767GZER3R3M5A	32 A, 3.3 uH
Output Capacitor	TDK C5750C0G2E154J230KE	250 V, 150 nF
Gate Driver	TI LM5114	5 V, 7.6 A
Digital Isolator	Analog ADUM5240ARZ	2500 V

A 400 V, 3.6 kW, 8-level FCML with stacked PCBs was fabricated. The simplified schematic and annotated hardware photograph are depicted in Fig. 7.8. Both boards are 6 layers and 1.6 mm thick. The output inductors are inset to a cutout in the motherboard. Relevant components are listed in Table 7.6 The FCML is operated as an inverter with 950

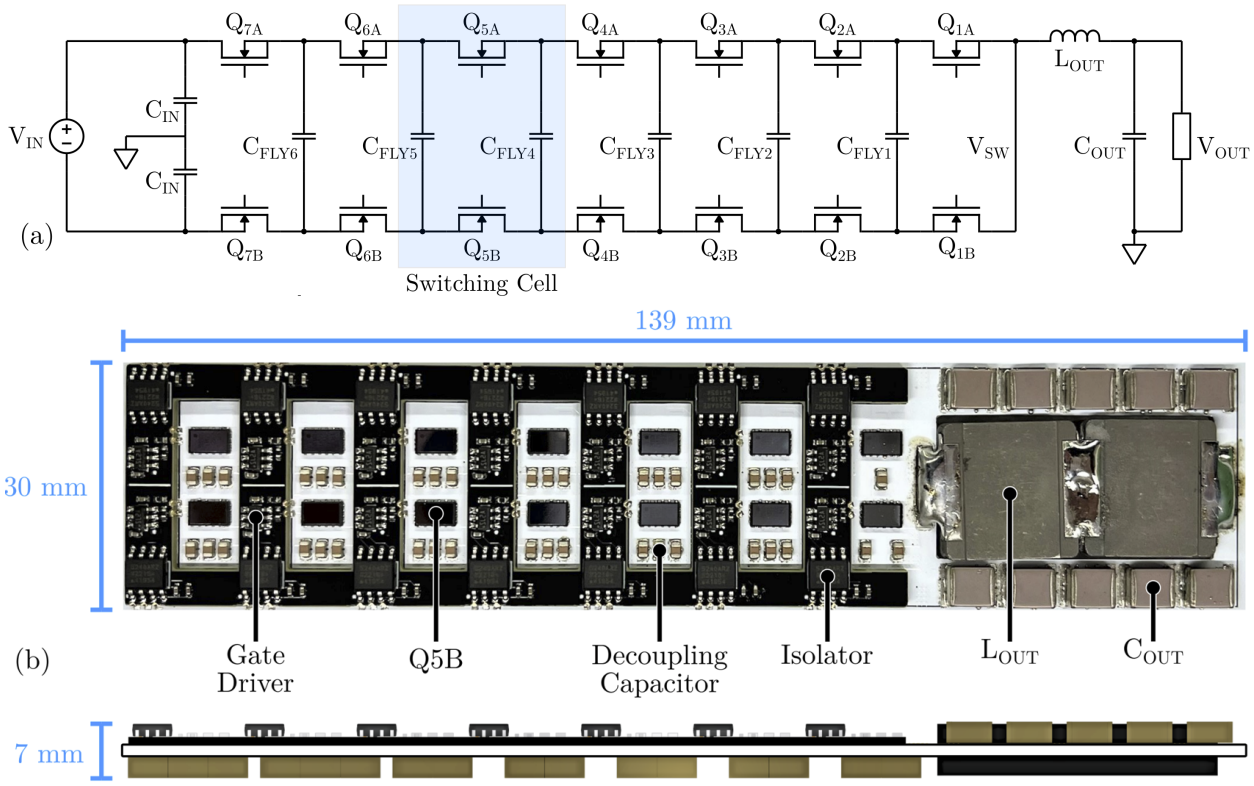


Figure 7.8: Proposed 8-level FCML prototype. (a) Simplified schematic, (b) hardware image with labels

Hz sine wave output. The switching frequency is 102 kHz, which corresponds to a 714 kHz effective switching frequency for the output filter, due to the frequency multiplication effect of the FCML. Table 7.7 summarizes the converter parameters. Efficiency measurements are taken with a 400 V DC input voltage and 135 Vrms sine wave output voltage. These are shown in Fig. 7.10. The converter achieves a peak efficiency of 98.1 %, including gate drive losses, for an output power of 1.7 kW. Peak power is recorded at 3.67 kW, with an efficiency of 97.3 %. Given a mass of 70 g and box volume of 1.78 in^3, this yields a gravimetric density of 52.5 kW/kg and volumetric density of 2.06 kW/in^3 (126 kW/L). Forced air cooling is used for these tests, but no heatsink is attached. The converter exhibits excellent passive balancing and low output distortion, as demonstrated by the V_{SW} and V_{OUT} waveforms in Fig. 7.9.

Table 7.7: Gen II Inverter Parameters

Parameter	Value
Input Voltage	400 V_{DC}
Output Voltage	135 V_{RMS}
Output Frequency	950 Hz
Effective Switching Frequency	714 kHz
Peak Output Power	3.67 kW
Peak Efficiency	98.1 %
Gravimetric Density	52.5 kW/kg
Volumetric Density	126 kW/L

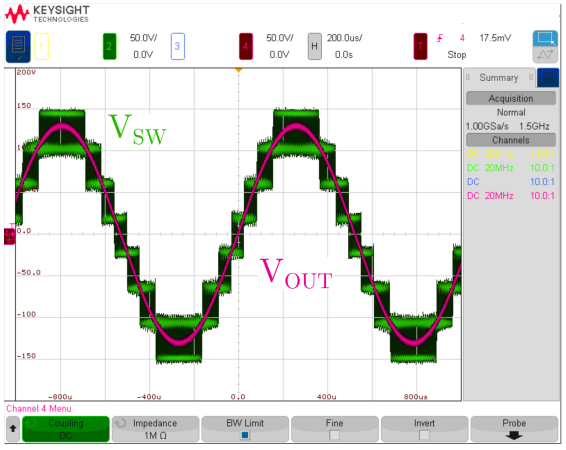


Figure 7.9: Converter operating waveforms demonstrating 8-level operation with passive balancing.

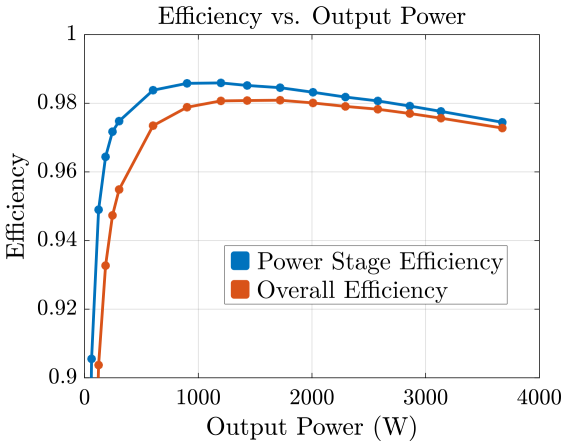
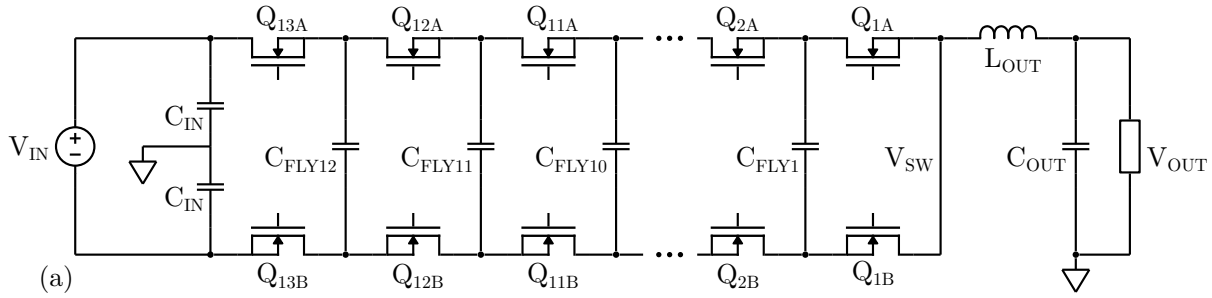


Figure 7.10: Efficiency measurements for inverter operation with 400 V DC input voltage. Power stage efficiency (excluding gate drive loss) and overall efficiency.

Gen III

An 800 V, 10 kW, 14-level dual-PCB FCML was fabricated. A simplified schematic is given in Fig. 7.11a, with the layout depicted in Fig. 7.11b. It is a dual PCB design: the conduction path begins at power connectors on the right side of the top board, travels the length of the PCB, traverses headers to the bottom board, and then travels back to the right and up through the output filter (highlighted by red loop in side view of Fig. 7.11b). The bulk flying capacitors are located in-between the two circuit boards, while all of the active devices are on the outside of the converter to provide opportunities for double-sided cooling of the power semiconductors. Both boards are 6 layers and 1.0 mm thick with blind vias. Relevant components are listed in Table 7.8. The FCML is operated as an inverter with 950 Hz sine wave output, as dictated by the high density electric machine fundamental frequency. The switching frequency is 150 kHz, which corresponds to a 1.95 MHz effective switching frequency for the output filter, due to the frequency multiplication effect of the FCML. Table 7.9 summarizes the converter parameters. Efficiency measurements are taken with an 800 V dc input voltage and 270 V rms sine wave output voltage. These are shown in Fig. 7.13. Forced air cooling is used for these tests, without heatsinking. The converter exhibits excellent passive balancing and low output distortion, as demonstrated by the V_{SW} and V_{OUT} waveforms in Fig. 7.12. A peak efficiency of 98.3 % is achieved, including gate drive losses, for an output power of 3.4 kW. Peak power is recorded at 10.4 kW, with an efficiency of 97.3 %. Given a mass of 59.8 g and box volume of 1.68 in^3, this yields a gravimetric density of 175 kW/kg and volumetric density of 6.2 kW/in^3 (380 kW/L).



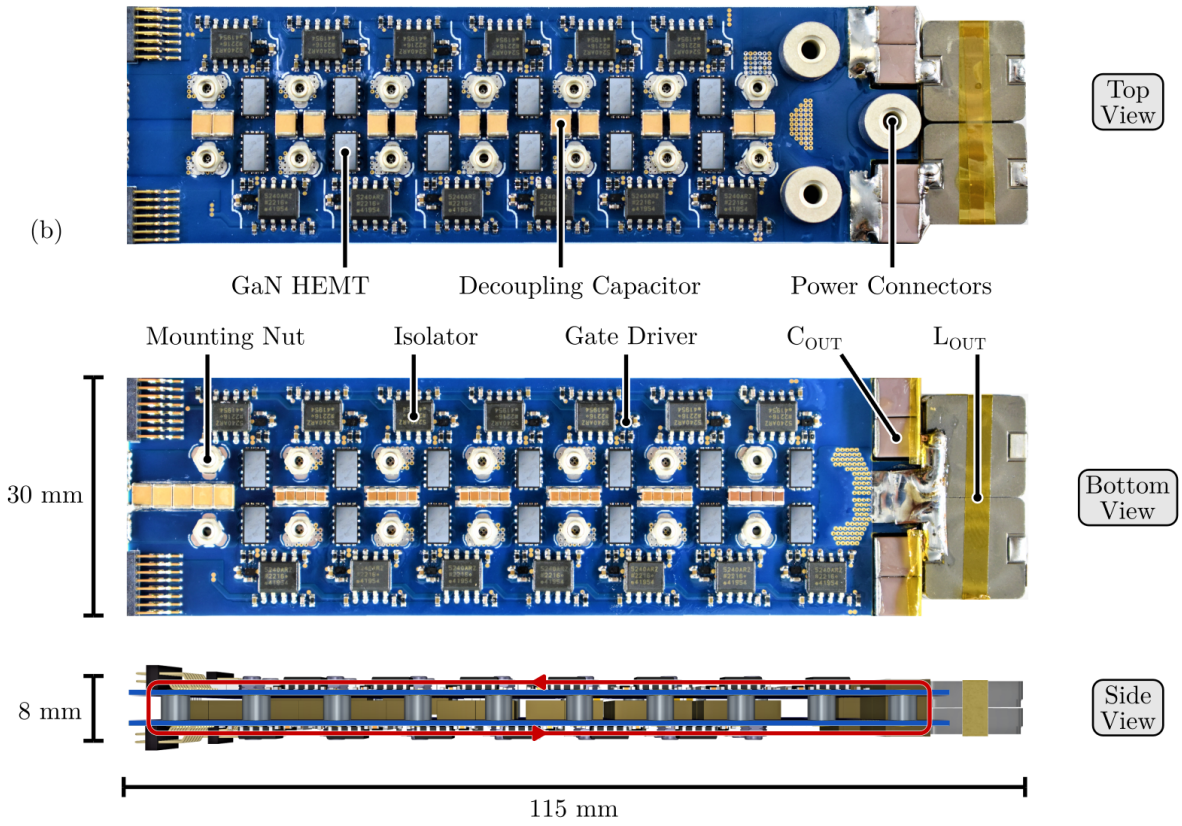


Figure 7.11: Proposed 800 V, 10 kW, 14-level FCML prototype with optimized flying capacitors. (a) Simplified schematic, (b) Annotated hardware photograph from top, bottom, and side view with the power path highlighted in red.

Table 7.8: Gen III Inverter Component List

Component	**Part Number**	**Parameters**
GaN HEMT	EPC2302	100 V, 1.4 mΩ
Gate Driver	TI LMG1020	5 V, 7.6 A
Digital Isolator	ADUM 5240ARZ	2500 V
C_A	TDK C2012X5R2A475K125AC	4.7 uF, 100 V
C_B	TDK C5750X6S2W225K250KA	2.2 uF, 450 V
L_{OUT}	Vishay IHLP5050CEER1R0M01	1 uH, 24 A

Table 7.9: Gen III Inverter Parameters

Parameter	Value
Input Voltage	800 V_{DC}
Output Voltage	270 V_{RMS}
Effective Switching Frequency	1.95 MHz
Peak Output Power	10.4 kW
Peak Overall Efficiency	98.3 %
Gravimetric Density	175 kW/kg
Volumetric Density	380 kW/L

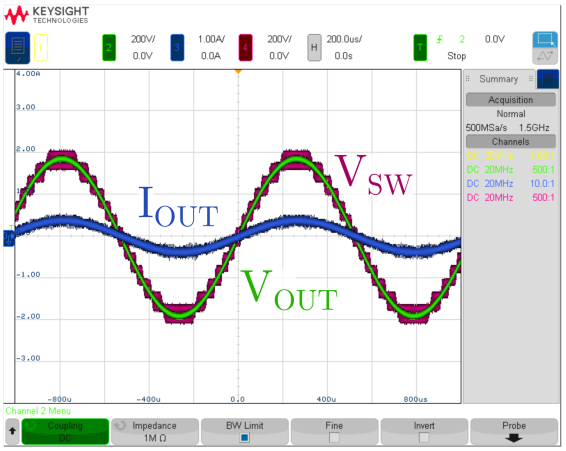


Figure 7.12: Converter operating waveforms demonstrating 14-level operation with passive balancing and low output distortion.

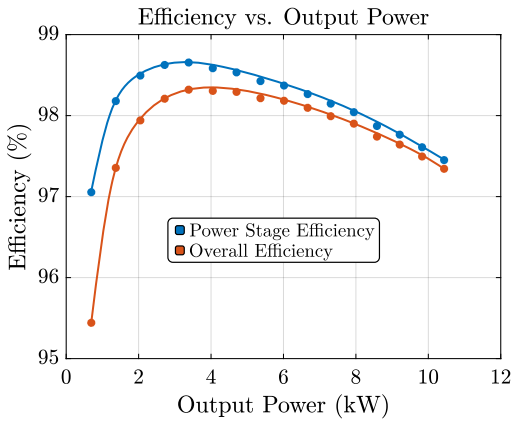


Figure 7.13: Efficiency measurements for inverter operation with 800 V dc input voltage. Power stage efficiency (excluding gate drive loss) and overall efficiency.

Gen IV

A 600 V, 6.6 kW, dual-PCB 10-level FCML inverter was fabricated to validate the design optimization. Fig. 7.14 shows a photograph of the fully assembled hardware prototype. Converter specifications are detailed in Table 7.10. Efficiency measurements were taken across load under these operating conditions. A peak efficiency of 97.34 %, including gate drive losses, was achieved at an output power of 4.84 kW. Peak power was recorded at 6.61 kW, with a full load efficiency of 97.16 %.

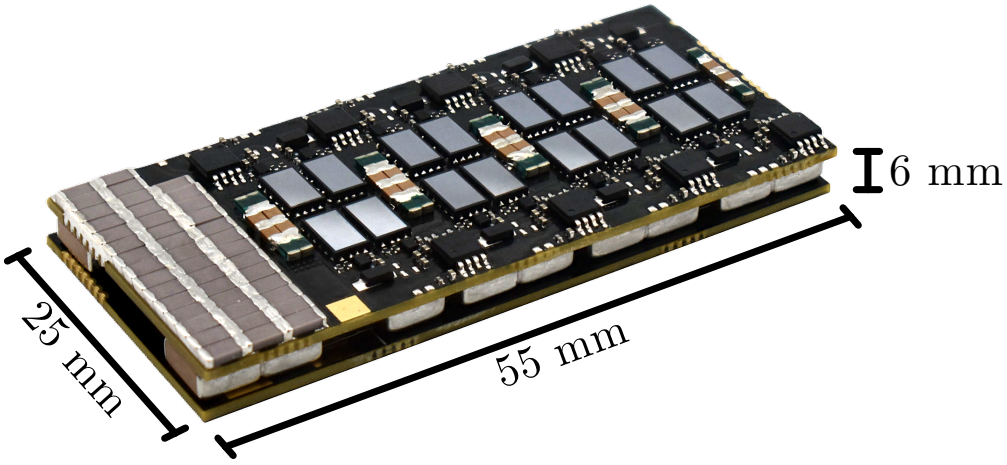


Figure 7.14: Photograph of assembled hardware prototype.

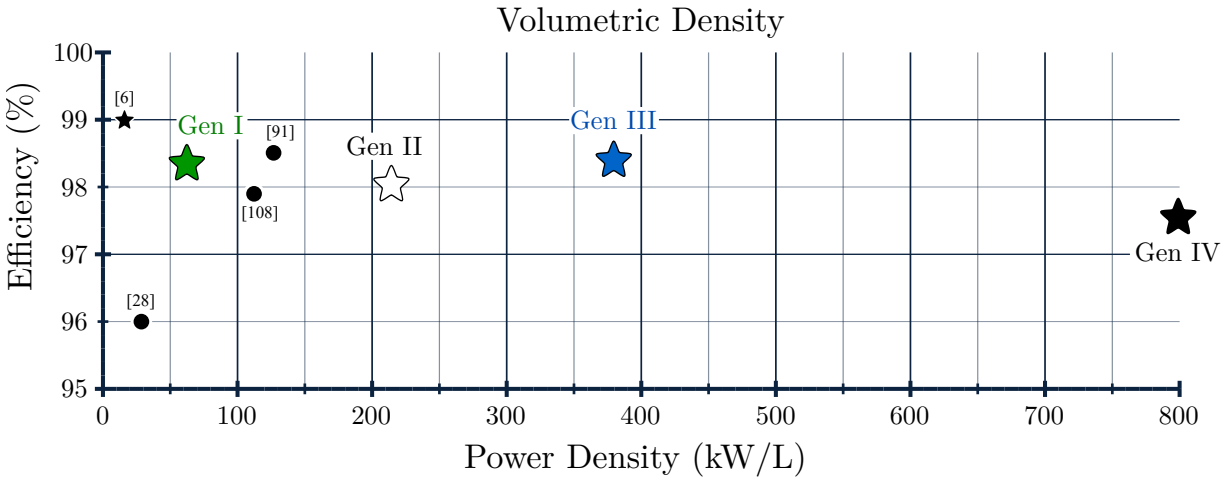
Table 7.10: Gen IV Inverter Parameters

Parameter	Value
Input Voltage	600 V dc
Output Voltage	200 V RMS
Effective Switching Frequency	1.8 MHz
Maximum Power	6.6 kW
Volumetric Density	800 kW/L
Gravimetric Density	250 kW/kg

Comparison to State-of-the-Art

The performance of this work is compared to state of the art medium-voltage inverters for motor drive applications. Fig. 7.15a plots the peak efficiency vs. gravimetric power density, while Fig. 7.15b shows the volumetric power density. For the gravimetric power density calculations, the mass for the PCBs and all of the power stage components including: all gate drive components, power transistors, flying capacitors, decoupling capacitors, output inductors, and output capacitors are included. For the volumetric power density calculation, the minimum box volume enclosing all of these components in the converter is used.

Many of the designs in this comparison feature 2- or 3-level topologies. These designs output slow PWM waveforms with very large volt-seconds, which places a heavy burden on the filtering components. The filters would need to be very large or potentially inefficient. As a result, some of the reported designs neglect filtering. They assume that the inductance of the motor being driven can act as a sufficient filter. This approach will not work for high-performance motors with reduced inductance, and could be quite inefficient for standard motors due to winding losses and core losses in the magnetic materials. In addition, the large dv/dts at the output cause common-mode current into the bearings of the motor which significantly worsens EMI. For these reasons, it is essential to include proper filtering when reporting inverter performance in these applications. Designs without filters are designated with a circular icon in Fig. 7.15, while designs with filters have a star icon. The proposed designs achieve the highest power density to date by some margin.



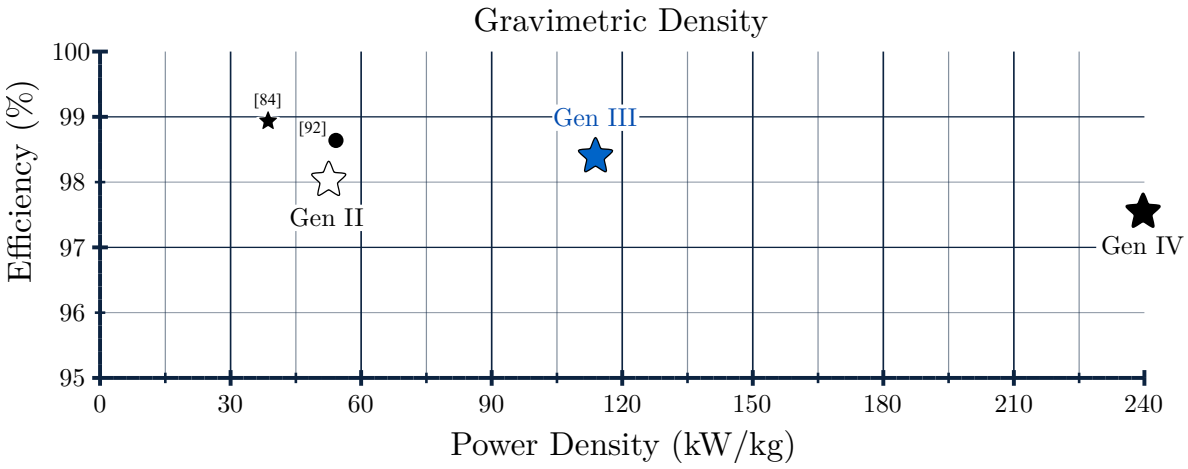


Figure 7.15: Performance comparison to state of the art.

7.3 TTV Prototypes

The proposed MCM testbed involves a novel design with the use of an array of power transistors to provide a mock thermal load which mimics the characteristics of a real commercial CPU or GPU. As this design has never been attempted before, we began by exploring different options for the electrical design. We considered various approaches, each with their own drawbacks and limitations.

Series vs. parallel transistors: The first dilemma involved the determination of how the array of power transistors would be connected. The parallel connection of transistors has the advantage of placing the potential of every device equally. Therefore, a conductive TIM could be used and there would be no concern of this interfering with electrical signaling and shorting out connections on the MCM. Unfortunately, this approach would require a separate current sensor measurement for every device, because we cannot predict how current will split between parallel transistors. In addition, this arrangement would require a power supply which outputs very high current at very low voltage, which may be unrealistic. By contrast, the series connection of transistors would enable us to use a single current measurement and more reasonable power supply operating conditions, with the drawback of different potentials.

Bare die vs. metallized packages: Next, we considered the characteristics of the transistor package. We want the device to closely match a CPU or GPU silicon material. Therefore, it was determined that the use of GaN-on-Si transistors would provide an ideal match, while also being commercially viable and affordable. Si transistors could be used, but often come with a metallized package which covers up the pure silicon die.

Size of first revision testbed: We wanted to develop a first revision prototype to validate the proposed MCM concept, but the complexity of using >100 transistors with the associated connections appeared too risky for an unproven approach. We decided, therefore, that we would first design a simplified version with 12 transistors. If this worked correctly, we would begin scaling upward from there.

Method for controlling the transistors:

The use of series transistors creates a challenge of controlling the transistors because they are all at different voltage potentials. The use of a dedicated signal isolator for each transistor would be costly and bulky. Instead, a simplified approach was developed, whereby signal multiplexers would cycle through the array, allowing for brief connections and communications with each transistor, without dedicated circuitry for each.

After all of these dilemmas were resolved, we began the design of the first revision prototype printed circuit board.

Gen I

Software Development

In order to operate the MCM, we need to develop a full software stack capable of controlling the electrical components on the printed circuit board, allowing a user to interact with the board to specify desired testing parameters, and displaying the results in an intelligible manner. For the initial prototype, our team had decided to utilize a small single-board computer called a Raspberry Pi. This comes with certain challenges when compared to using a microcontroller: it runs a full Linux operating system which makes it much more difficult to achieve fast, reliable control of peripherals. The main benefit, however, is that it can be directly interfaced with a computer monitor (via HDMI cable). This reduces cost and minimizes overall system complexity greatly, as all of the software can be written in one language on one device, as opposed to having a distributed control architecture. The proposed plan is to develop software in Python on the Raspberry Pi to determine if it is possible to achieve the desired electrical specifications using this device. If not, the backup plan is to split control between a microcontroller (performing low- level operations) and a Raspberry Pi (generating the user interface).

Low-Level Control: The first layer of software involves direct interface with the components on the custom printed circuit board. The proposed electrical approach involves a multiplexing scheme whereby the controller must select a particular transistor in the array, set its gate voltage to a desired value, then measure its gate-to-source voltage, drain-to-source voltage, and the conducted current. The multiplexers can be controlled via binary logic and a lookup table to store the necessary logic signals for each specific transistor. Measurements can be taken by communicating with the analog-to-digital converters (ADCs) on the PCB. This is done using a low-level communication protocol named serial peripheral interface (SPI).

User Interface: All of the low-level control details must be abstracted away behind a convenient user interface. This will enable a user to specify their desired testing conditions and export the results. During this quarter, data visualization code was developed to enable plotting of all measurements during operation (transistor gate-to-source voltages, transistor drain-to-source voltages, and transistor drain-to-source currents). Subsequent work will focus on design of a graphical user interface for control of the MCM.

Electrical Testing: A first revision prototype PCB was designed. As this design has never been attempted before, we first wanted to verify basic functionality and the utility of this methodology before continuing on to a full-scale electrical design with more transistors. The initial prototype has 12 transistors. In this quarter, we tested the board in 6 different dimensions: power-up, multiplexing, gate voltage drive, voltage measurement, current measurement, and temperature trend.

1. Power-Up: The first test for the board is to simply determine if it can be powered on and all of the voltage rails reach the desired values. There are four voltage rails on the design. All of the voltage rails powered up successfully.

2. Multiplexing: The next step is to check that the multiplexing scheme is working correctly, such that we are able to turn all of the transistors on and perform measurements. This involves sweeping through the array, thus validating both the software and hardware layout of the design. We were successful in driving all of the transistors and conducting power through the array.

3. Gate Voltage Drive: The third test involved sweeping the gate drive voltage to change the effective resistance of the transistors. Unfortunately, the component we selected to do this (a programmable LDO) can only change the voltage upon startup, so the board would need to be powered down for each change. This is something we will correct in subsequent revisions.

4. Voltage Measurement: The multiplexing scheme is designed to extract each transistor's precise gate, drain, and source voltage. This is the most sensitive part of the project. The drain-to-source voltage is amplified to improve measurement fidelity. In order to make these measurements, the controller must communicate with the ADCs to take a measurement, and the electrical design must be sufficient to provide the correct voltage with low noise/interference. Successful voltage measurements were made for all of the transistors, albeit with more noise than desired. The electrical design will be adjusted slightly in subsequent revisions to reduce this noise level.

5. Current Measurement: The current conducted through the array is fed across a sense resistor, amplified, and then measured by an ADC. This measurement was made successfully, and the results were sufficiently accurate.

6. Temperature Trend: The operating mechanism for the proposed TTV is reliant on the change in effective resistance of the transistors as a function of temperature. It is critical that our circuitry is accurate enough to detect these changes precisely. Voltage and current measurements were made, and the effective resistance was plotted versus time for different current loads. We were able to distinguish a very clear change in device resistances as they increased in temperature. A thermal camera was used to verify the measurement. This indicates that the proposed mechanism is viable.

Hardware Design

We began with the simplest possible approach: an array comprising 12 large Si power transistors. Fig. 7.16 shows a hardware photograph. The goals were simply to verify basic functionality and derisk a full prototype design.

Overall, these results obtained with this prototype were highly encouraging. They demonstrated that the proposed approach is valid, and encourage the development of a full-scale array with many transistors to provide a high-performance TTV. The next steps will involve implementation of this high- performance second revision design. Aside from small hardware fixes, the main difference in the next revision is the utilization of much smaller

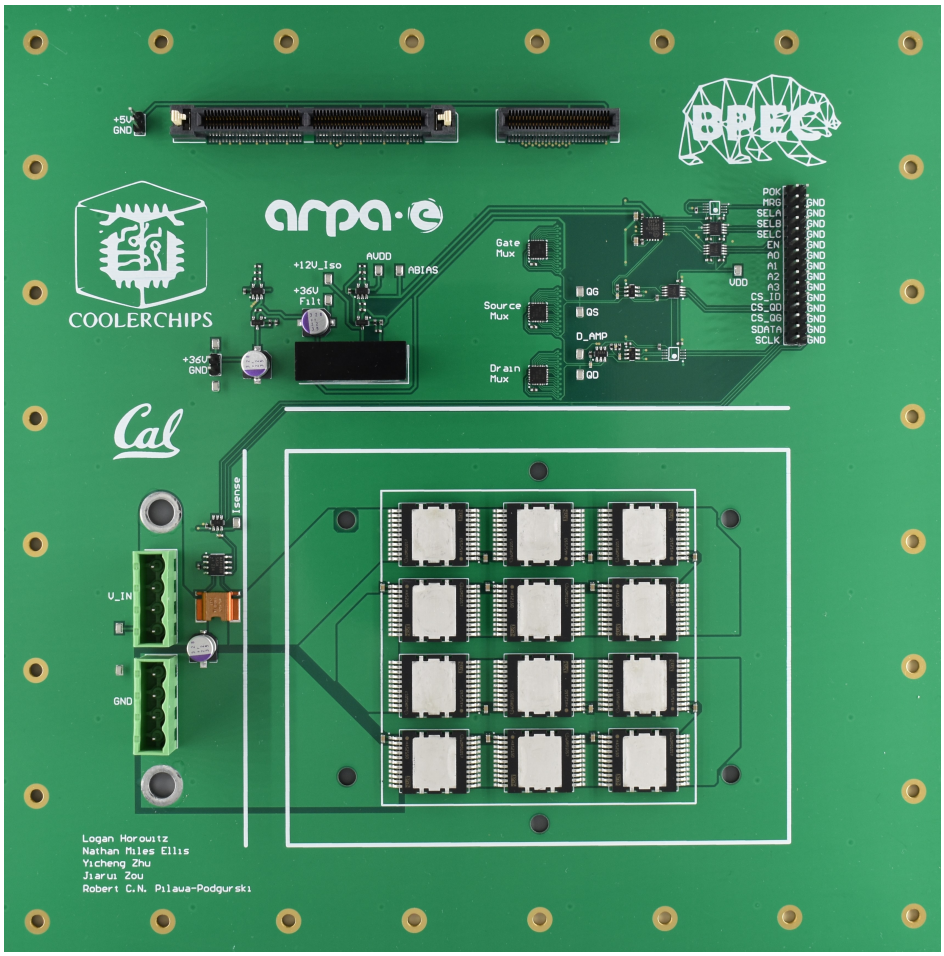


Figure 7.16: Hardware photograph of Gen I TTV prototype.

transistors such that the spatial localization is greatly improved and hotspot generation can be done with high fidelity. The new design contains 154 uniquely controllable transistors, as compared to 12 in the current design. This comparison may be easily visualized in Fig. 7.17.

Gen II

We had previously demonstrated our first revision prototype, which contained 12 transistors in the array. This represented an initial validation of the design approach. Next, a second-generation prototype containing 154 transistors was developed. This provides much greater flexibility in the heat maps which can be generated, and much better spatial fidelity in the temperature measurements. Fig. 7.18 shows an annotated hardware photograph of the second revision prototype.

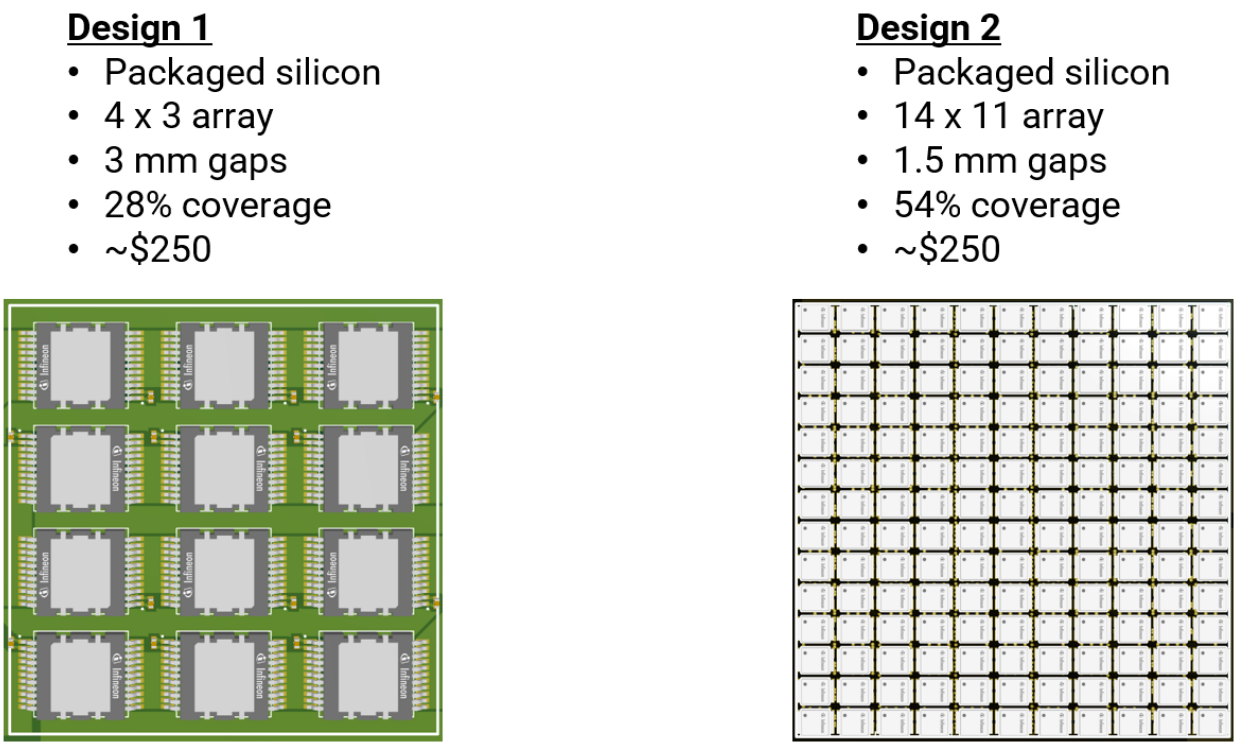


Figure 7.17: Comparison of the transistor array for Gen I TTV prototype and proposed Gen II TTV prototype.

Software Development and Hardware Validation

The second revision prototype represents a large increase in complexity from the initial design, necessitating development time to properly handle all of the low-level control. In addition to this, a GUI was added. This allows for user interaction to specify the testing environment and heat profile to be generated. It also reports the measured device characteristics live during testing. These features were developed and then integrated with the low-level control code to provide a complete solution.

The second revision hardware prototype contains hundreds of electrical components so the first step in using the board was to validate correct electrical operation. Fortunately, the design functioned as expected and we were able to perform all of the necessary measurements.

Energy Innovation Summit Demo

In order to display this work, a demonstration was devised for the ARPA-E Energy Innovation Summit 2024. Live operation was exhibited, with custom heat profiles generated, a thermal camera used to display the results and a GUI for user interaction. Fig. 7.19 shows an image of the setup.

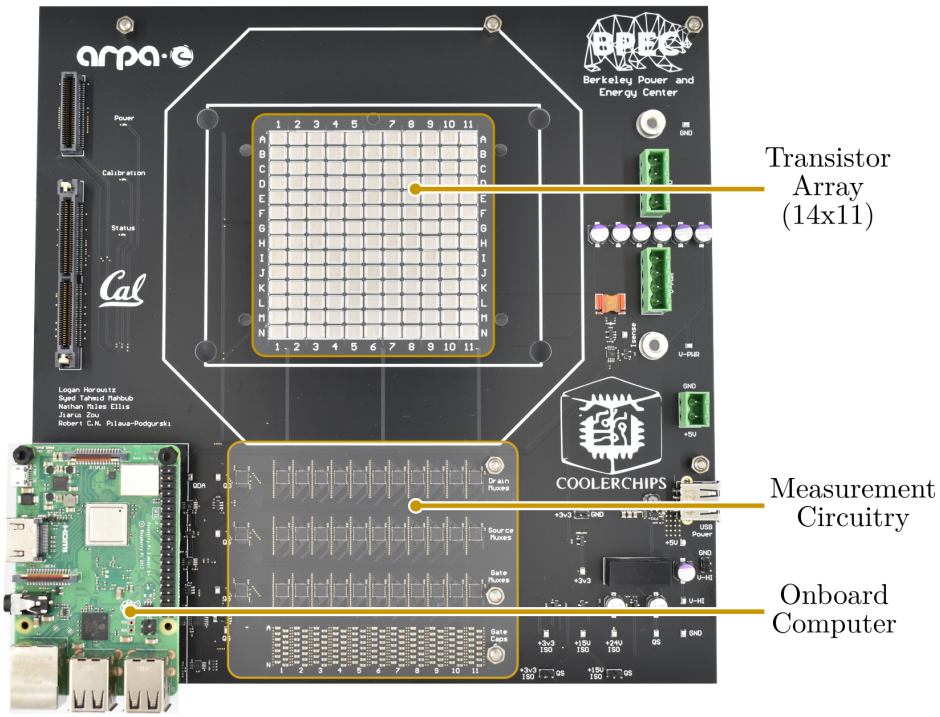


Figure 7.18: Photograph of the second revision hardware prototype with the transistor array, measurement circuitry, and onboard computer highlighted.

To summarize the overall results: a flexible TTV design capable of generating custom heat profiles up to 500 W was achieved. Precise resistance measurements were taken with verified changes over temperature such that this relationship may be mapped in the future.

Figure 7.19: MCM TTV Demo for ARPA-E Energy Innovation Summit 2024. Includes a fully functional TTV operating in real-time with the thermal camera and GUI reporting the results.

Gen III

In theory, the proposed TTV design is amenable to highly flexible transistor array sizing and component selection. In practice, the previous prototypes contain all of the circuitry on a single PCB, which means that the entire system would need to be redesigned every time. Moreover, the entire system needs to be replaced if a transistor breaks during testing. To combat these issues, a modular design approach was adopted for Gen III. The transistor array is separated onto its own PCB, and the signals are brought to a motherboard PCB which houses all of the control and compute circuitry. This greatly reduces the cost of the transistor array PCB, enabling destructive or permanent testing approaches to be used. It also simplifies the redesign process for new designs with different transistors and component count. Fig. 7.20 shows the full modular system with separate PCBs.

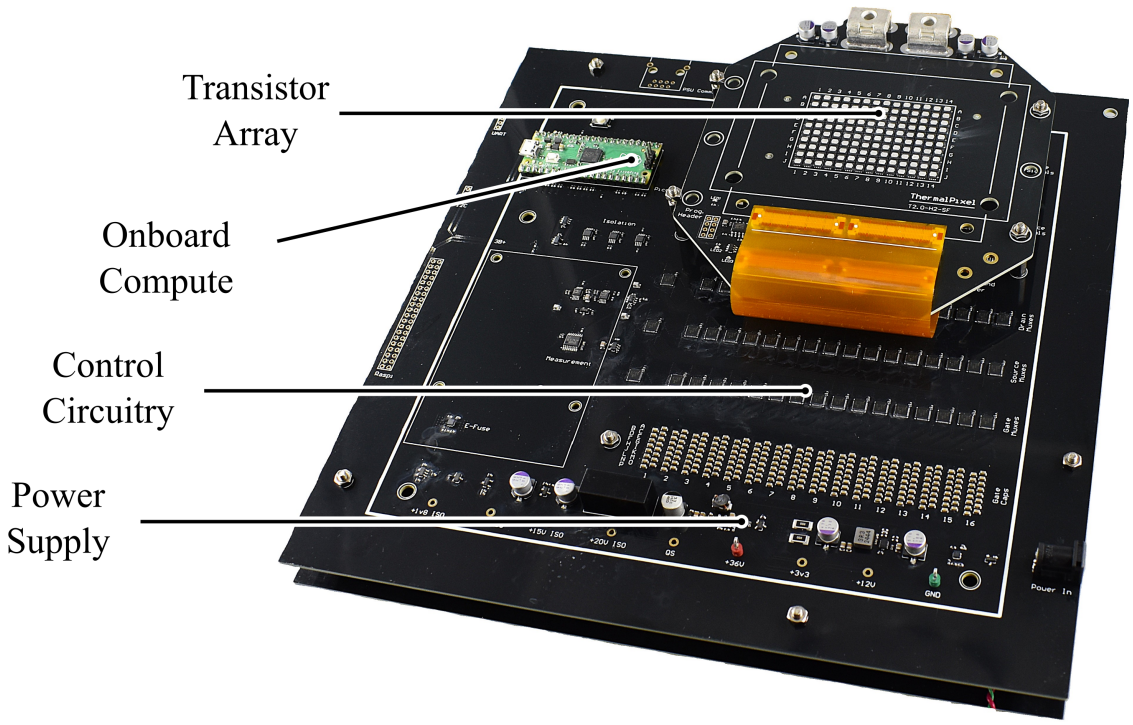


Figure 7.20: Gen III TTTV prototype with modular design. The transistor array is separated from control/compute circuitry onto separate PCBs.

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