Sub-THz Transmitter Design Techniques for High Speed Wireless Communication

Meng Wei

Electrical Engineering and Computer Sciences
University of California, Berkeley

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by

Meng Wei

A dissertation submitted in partial satisfaction of the

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Committee in charge:

Professor Ali Niknejad, Chair
Professor Martin White
Professor Jun-Chau Chien

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Abstract

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Achieving 100 + Gb/s data throughput is a key objective and an active area of research for future 6G communication, therefore, sub-THz(100-300GHz) is of great interest due to its potential to meet this data rate requirement. However,designing an energy efficient silicon-based sub-THz wireless system is challenging due to the high free space path loss and low active device gain at these frequencies. This dissertation addresses these problems by proposing architecture-level and circuit-level techniques.

This dissertation consists of wireless transmitter design techniques at both 140GHz and 200 GHz. We first introduce two iterations of a packaged 4 element phased-array 140GHz transmitter. A slotline-based power combiner is utilized for high output power generation. In addition,the TX system efficiency is enhanced by employing negative resistance compensation (NRC) in the up-conversion mixer, intensively utilizing low insertion loss(IL) slot line based interstage matching networks and current re-use Gm-cells in baseband(BB) amplifiers. Fabricated in 28nm CMOS technology, the 4 element phased-array 140GHz transmitter not only achieves 100 + Gb/s data rate with competitive energy efficiency, but it also achieves high EIRP with high system efficiency. Next, we propose a multi-way power combined 200 GHz PA which employs different gain boosting techniques and low loss broadband multi-way power splitters/combiners. Last, we present a novel power efficient 200GHz digital transmitter(DTX) architecture: an oscillator array assisted digital IQ sharing transmitter. The proposed DTX architecture not only leverages digital scaling for power/performance but also utilizes amplifiers in saturation region with enhanced power efficiency. A 200GHz low phase-noise sub-sampling phase-locked loop (SS-PLL) is also included to stabilize the frequency of the harmonic oscillator array.

To my family

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Finally, I would like to give my greatest gratitude to my parents.

Chapter 1

Introduction

1.1 Motivation

As operators worldwide continue to deploy 5G, the next generation of wireless communications technology is also gradually taking shape. 6G has the potential to shape the communications industry and push communications technology to make a significant societal impact[32]. Industry has already started the standards development process, and sub-terahertz (sub-THz) (100-300GHz) system's are a focus of 6G research since it will play a crucial role for meeting one Key Performance Indicator (KPI) for 6G: 100+ Gb/s data rate.

However, designing an energy efficient silicon-based sub-terahertz (sub-THz) system poses several challenges. First, the limited intrinsic transistors gain at sub-THz frequency bands adversely affects the implementation of a power and energy efficient system. Second, the free space path loss at these frequencies is relatively high, as shown in Fig. 1.1. One way to mitigate path loss is by designing phased-array systems.

1.2 Thesis Organization

This dissertation consists of six chapters. Chapter 2 presents a 140GHz packaged transmitter supporting 24 Gbps 16-QAM and 24 Gbps 64-QAM at 5.3pJ/bit efficiency, tested with over-the-air measurements.

Chapter 3 demonstrates a D-band 4-element Phased-array TX chip which not only achieves 100 + Gb/s data rate with competitive energy efficiency, but also achieves high EIRP with high system efficiency.

Chapter 4 demonstrates a 200GHz multi-way Power Combined PA. Different gain boosting techniques are analyzed and utilized in the power combined PA. Moreover, slotline based power splitters and power combiners are also employed to reduce the insertion loss.

Chapter 5 proposes an oscillator array assisted digital IQ Sharing 200GHz Transmitter. It leverages the amplifiers operating in the saturation region with enhanced power efficiency,

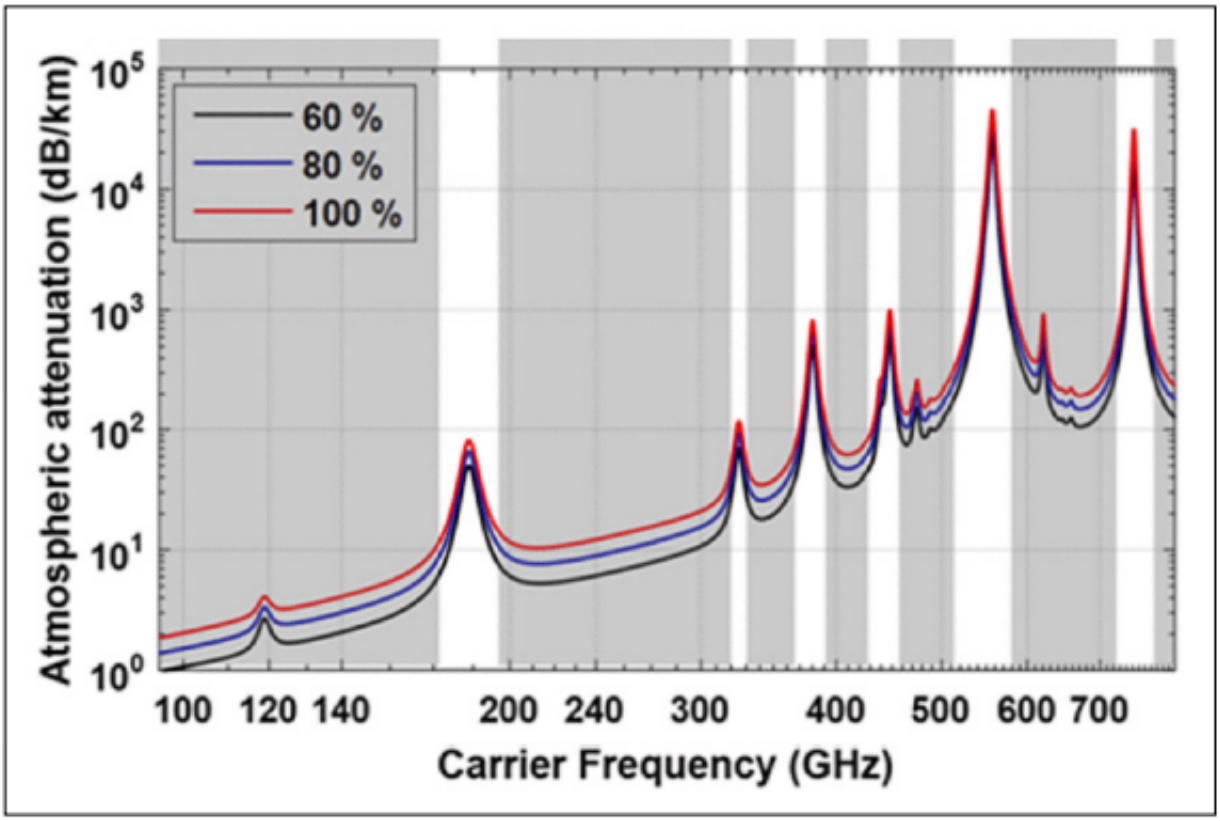


Figure 1.1: Attenuation of signals as frequency increases / wavelength decreases[25].

and can also support spectral efficient modulation schemes like 16QAM. In addition, it includes a sub-sampling PLL to stabilize the frequency of the harmonic oscillator array.

Chapter 6 summarizes the dissertation.

Chapter 2

Charm Transmitter Version 1 (V1)

Growing demand for data across all communication requires an increase in both of capacity and density of back-haul point-to-point (PTP) and point-to-multipoint (PTMP) data links[15]. A D band (110-170GHz) phased-array transceiver offers an attractive means to increase the capacity by leveraging the large available bandwidth and overcomes the high free-space path loss by adopting large array gain. Recent advances in process scaling are enabling > 100GHz transceiver implementations in low-cost CMOS technologies for commercial applications. In addition, to meet the requirements of future commercial systems above 100GHz, a low-cost and high-performance packaging platform is required. Recent publications have demonstrated high performance D band transceivers capable of high-order and wide-bandwidth modulation [15, 2, 27, 3, 24]. However, very few are packaged or are tested with an on-chip PLL.

This chapter presents a 4-channel D-band packaged integrated transmitter. The focus of this work is on the transmitter (TX), which achieves 9-10.6dBm EIRP at Psat (per channel), and 24Gbps with 16-QAM and 64-QAM modulation at 5.3pJ/b efficiency in 28nm CMOS technology, which is suitable for MU-MIMO applications.

2.1 D-band TX Architecture

Figure. 2.1 shows the block diagram of the simplified TX chip. We attach four IC's on the interposer (package), and each of the IC's has four channels for a total of 16 active elements. The TX ICs are designed to be directly attached to the feed points of the antennas on the interposer. The chip on the interposer is mounted on the PCB as a ball grid array (BGA) module. The chip integrates four TX elements. The transmitter employs the direct up-conversion architecture, and it consists of an input matching network with ESD protection, a two stage broadband baseband amplifier, I/Q double balanced Gilbert cell up-conversion mixers, and a three-stage power amplifier.

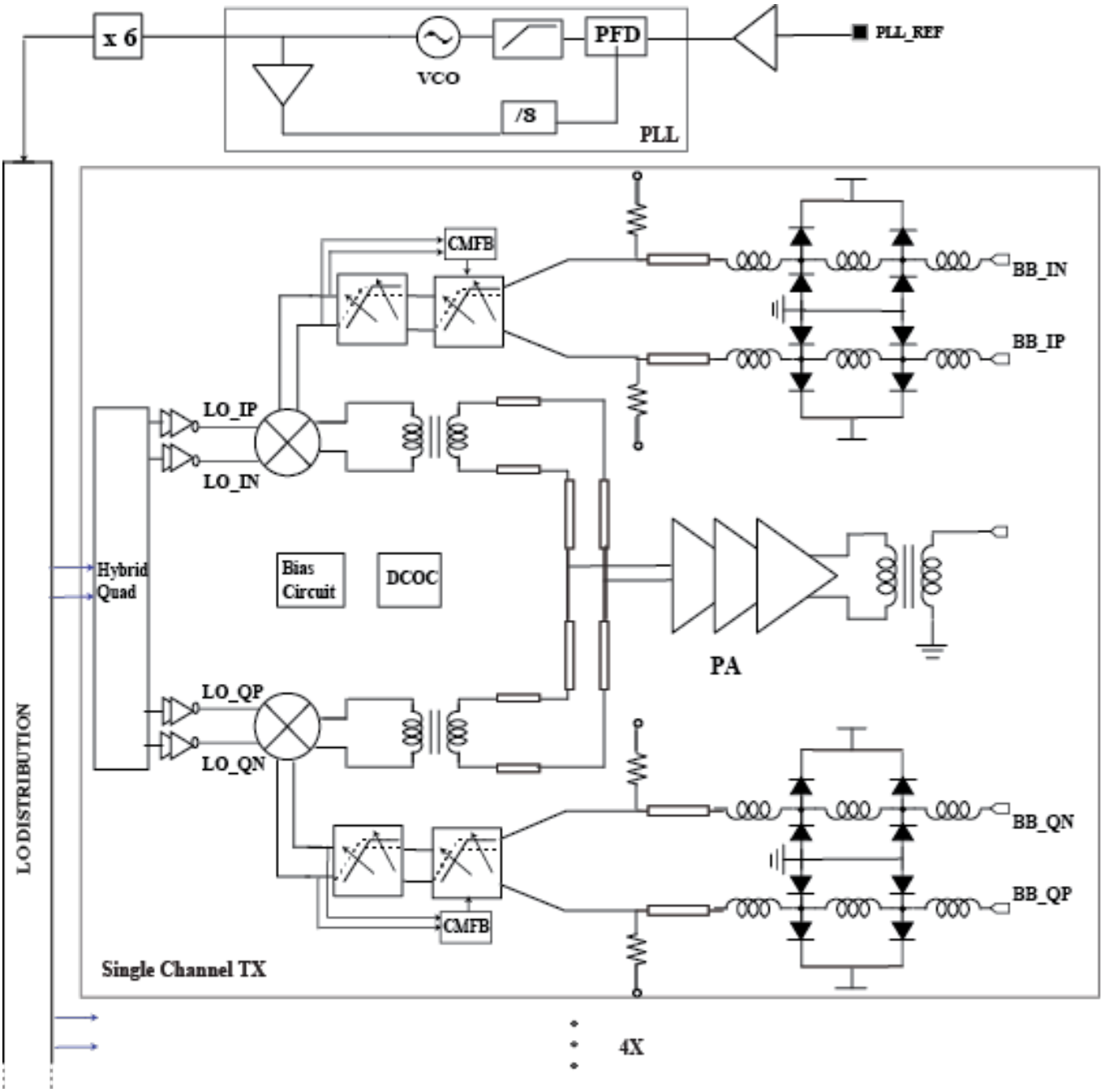


Figure 2.1: Diagram of the D-band TX.

2.2 Input Matching Network

The input pad network is designed to provide a bandwidth greater than 10GHz while also achieving low return loss. The cascading L-C sections extends the pad bandwidth with a given C_{pad}. To reduce the return loss, the inductors are sized such that the characteristic impedance of the LC-π network is roughly equal to the termination resistor[23]. In this design, a three segment LC-π network is utilized to achieve $>$ 10GHz bandwidth. The parasitic capacitance from the bump and interconnect, the two ESD protection diodes, the first-stage BB amplifier and termination resistor, are distributed across three inductor segments to meet the return loss and bandwidth requirements. The silicon bump-pad network and the package traces were simulated together using a full-wave 3-D EM simulator to accurately capture the interaction between two. The input pad network achieves >10GHz 1-dB-bandwidth and <-12.8dB return loss from DC to 10GHz in simulation. The layout of this input pad network is shown in Fig. 2.2.

2.3 Re-configurable Low Power Broadband Baseband Amplifier with Compact Area

As shown in Fig. 2.3, a low power broadband analog baseband is implemented by cascading two differential re-configurable wideband amplifiers. The broadband analog baseband achieves a small area, due to the absence of passive inductors. This analog baseband can provides a gain range of 14dB and performs filtering.

The baseband amplifier, shown in Fig. 2.3, consists of PMOS and NMOS differential transistor pairs in order to increase the total g_m and thus reduce power consumption. The folded active inductor consisting of M2 and M3 is employed to further improve the bandwidth. M3 operates at triode region to allow modulation of the channel resistance to realize a variable resistor. In this way, the bandwidth is programmable by tuning the gate voltage of M3. The gain control in the BB amplifier is achieved using voltage DACs to adjust the gate voltage of the tunable transistor M4, as shown in Fig. 2.3. DC offset cancellation circuit (DCOC) are employed in the analog baseband to calibrate LO leakage. M7 operates in the saturation region to reduce the load effect of the current DACs on the baseband amplifier[29].

2.4 Up-conversion Mixer

Fig. 2.4 also shows the quadrature up-conversion mixer. In the quadrature mixer implementations, if the output nodes of in-phase and quadrature cells are connected to sum the output current, the output capacitance increases and thus reduces the bandwidth of the mixer[16]. Our design utilizes two separate output matching network (transformer based matching network and transmission-line (T-Line) based matching network) for the I/Q mixer cells, and the T-Line based matching network also acts as a combiner to combine the I and Q path

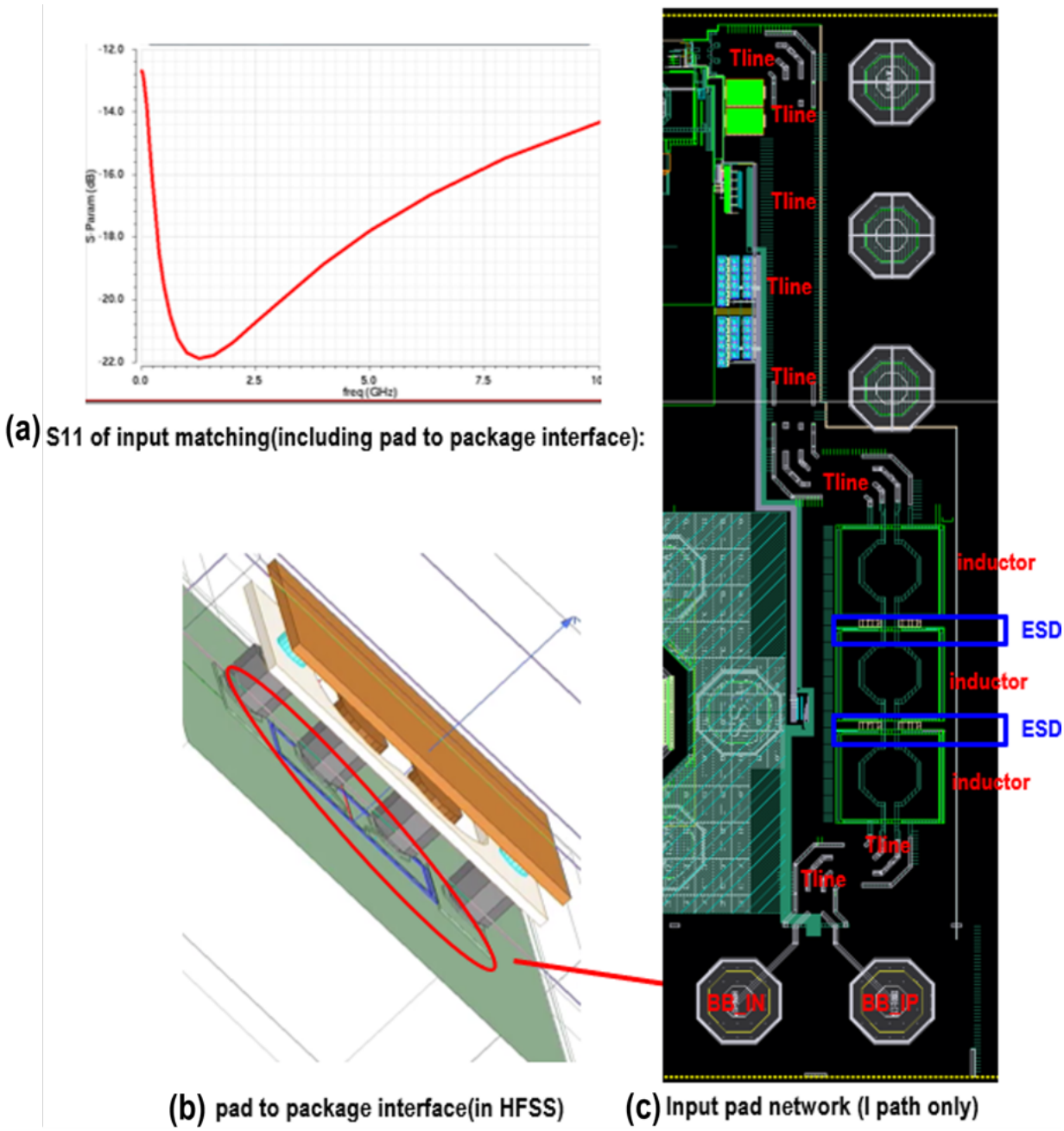


Figure 2.2: (a) S11 of input matching network. (b) HFSS view of pad to package interface. (c) Layout of input pad network(I path only).

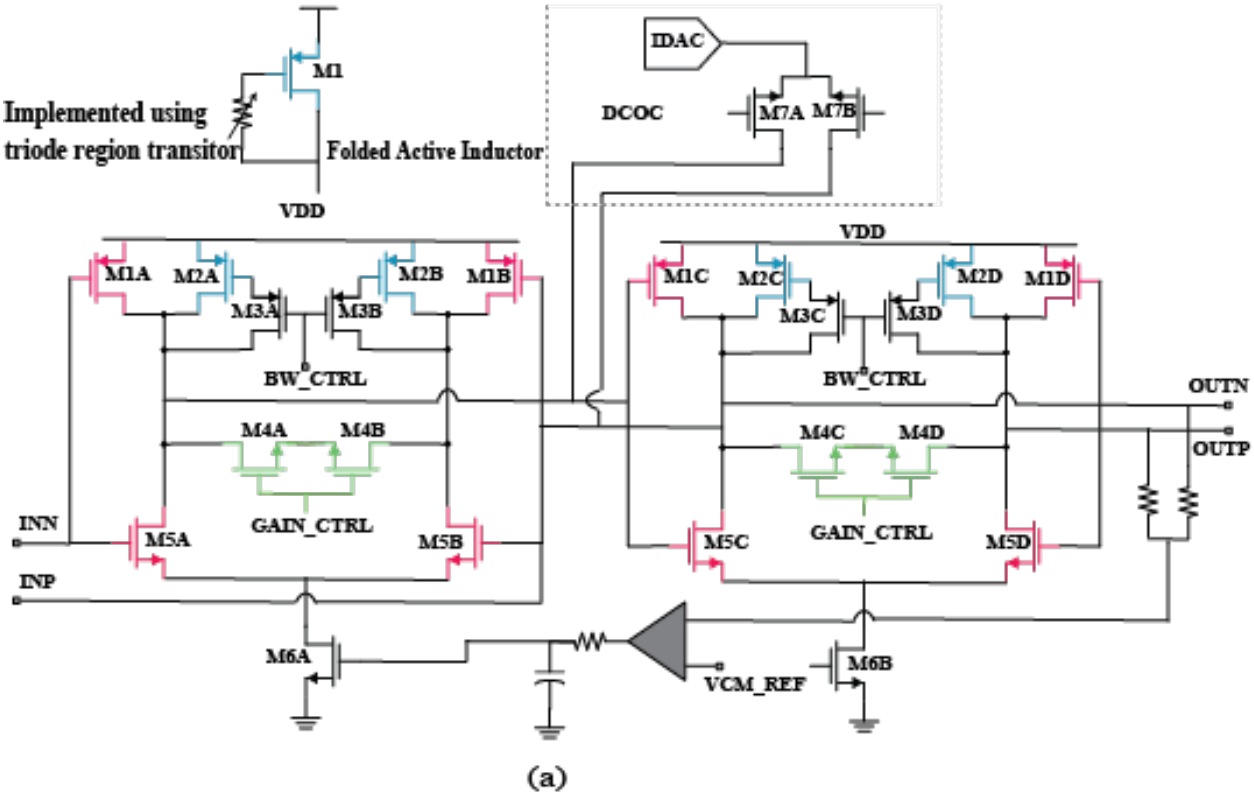


Figure 2.3: Diagram of the broadband baseband amplifier.

together. As shown in Fig. 2.4, the value of Z2 is optimized for conversion gain and linearity, and the value of Z1 is selected to achieve the desired bandwidth. In addition, the mixer and transformer layout were generated using Berkeley Analog Generator(BAG)[9], which is an open-sourced circuit generation framework.

2.5 Fully Packaged PA

Fig. 2.5 shows the simplified diagram of the fully packaged PA. The PA consists of a cascade of three transformer-coupled, capacitively neutralized differential pair (NDP). With the utilization of neutralization, both Gmax and differential mode stability can be improved. However, the common-mode stability will degrade. To stabilize the common mode, a series resistor Rg is tied to the center tap of the gate coils.

Fig. 2.6 shows the load pull simulation results of the PA output stage. An optimum load impedance Zopt,diff=21+j30 ohm is chosen for the output stage. The three-stage PA achieves > 25GHz 3dB BW in simulation. The simulated OP1dB and Psat at 140GHz is 4.3 dBm and 7 dBm, respectively. The simulated PAE and power gain is shown in Fig. 2.6.

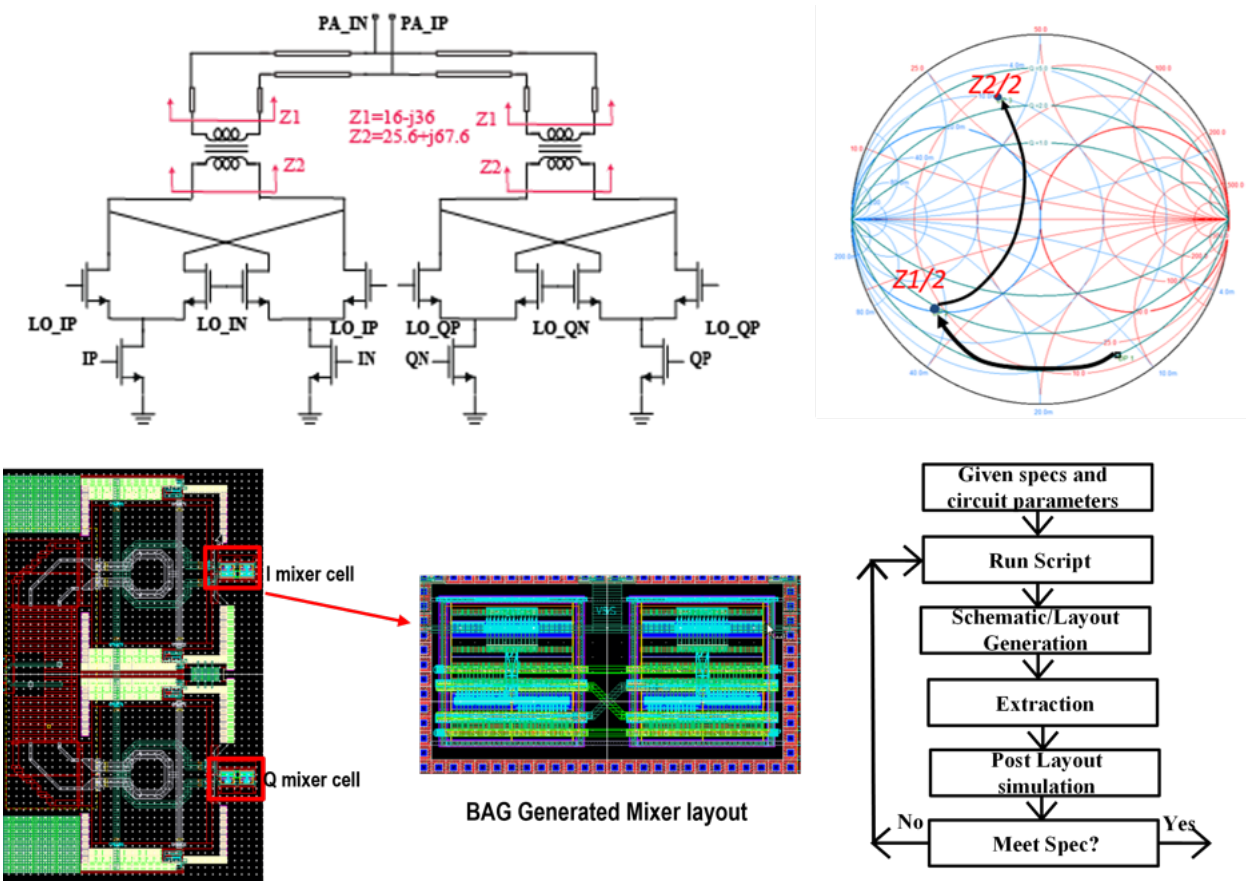


Figure 2.4: Block Diagram of Up-conversion Mixer, and BAG generated mixer layout.

The 3-stage PA shows around 15dB power gain in simulation, and the PAE at Psat is 6.75 %.

2.6 Measurement Results

This transmitter IC has been fabricated in 28nm CMOS. As shown in Fig. 2.7, the single channel TX only occupies 1.1 mm^{2}active die area.

2.6.1 TX Psat, OP1dB and EIRP

The TX EIRP related measurements are performed with a WR-6 standard gain horn antenna cascaded with an LNA. The EIRP versus frequency is presented in Fig. 2.8. The TX module results in an EIRP of 9-10.6 dBm and 5.1-6.8 dBm at P_{sat} and OP $_{1dB}$, respectively, at 128-

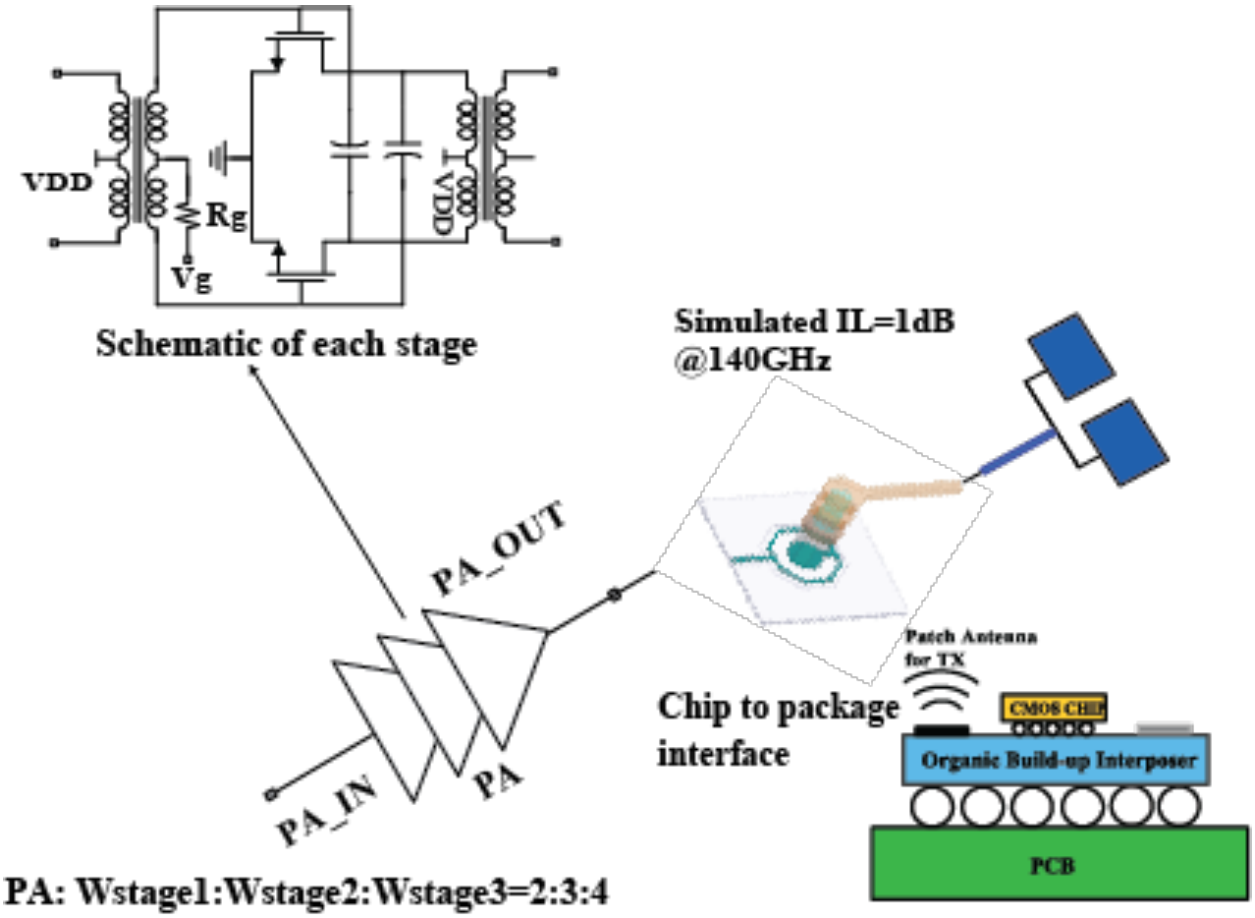


Figure 2.5: Simplified diagram of fully packaged PA.

140 GHz. We also plot the TX P_{sat}/OP_{1dB} versus frequency with and without de-embedding the loss of chip-to-package transition and routing to the antenna.

2.6.2 TX Gain and Bandwidth

To measure the TX gain or bandwidth, the TX is configured as a single sideband (SSB) transmitter. The baseband frequency is swept for both lower sideband (LSB) and upper sideband(USB) configurations. As shown in Fig. 2.9(a), the TX exhibits a measured 3dB BW of more than 12GHz (BW limited by the test setup). Fig. 2.9(b) also shows how the inductive peaking can be controlled by adjusting the tunable resistor of the active inductor. The boost at high frequency can be utilized to compensate for the high frequency loss of the baseband routing on the interposer and PCB.

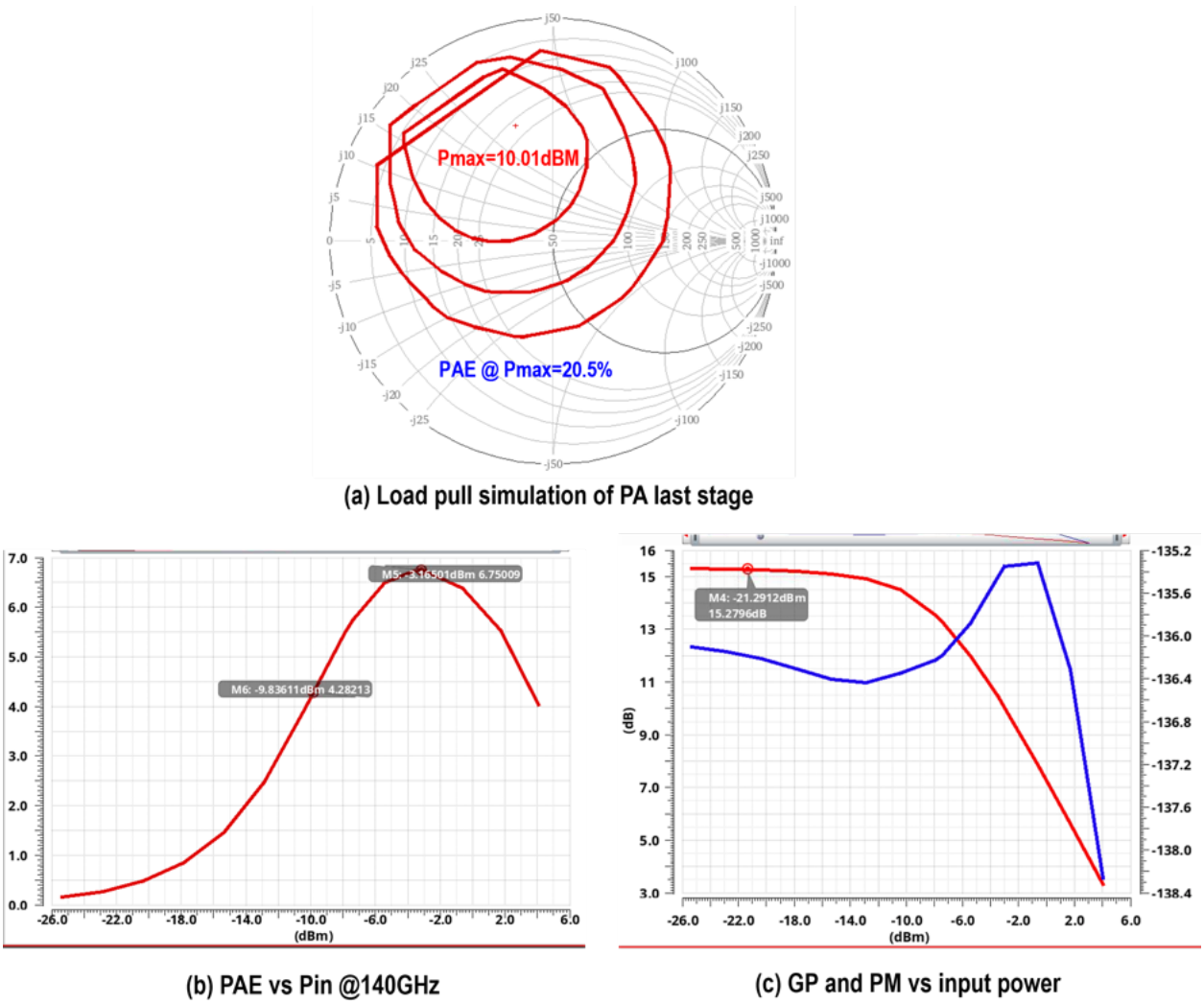


Figure 2.6: (a) Load pull simulation of PA last stage. (b) Simulated PAE vs input power Pin. (c) Simulated GP and PM vs input power.

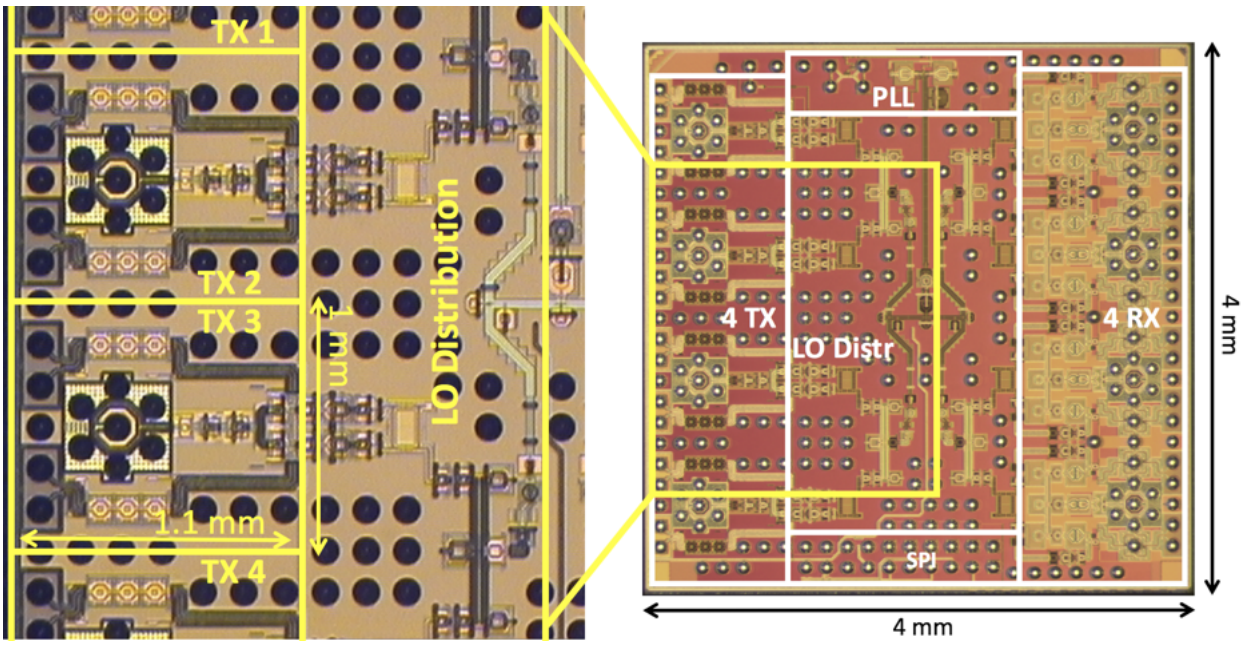


Figure 2.7: Die photograph of the CMOS D-band TX.

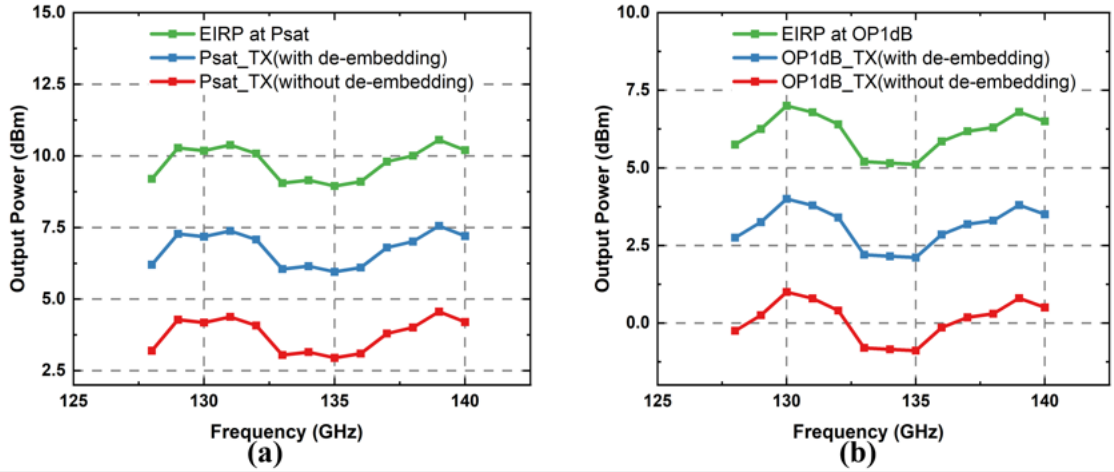


Figure 2.8: (a) Measured EIRP at P_{sat} of the D-band TX. (b) Measured EIRP at OP_{1dB} of the D-band TX.

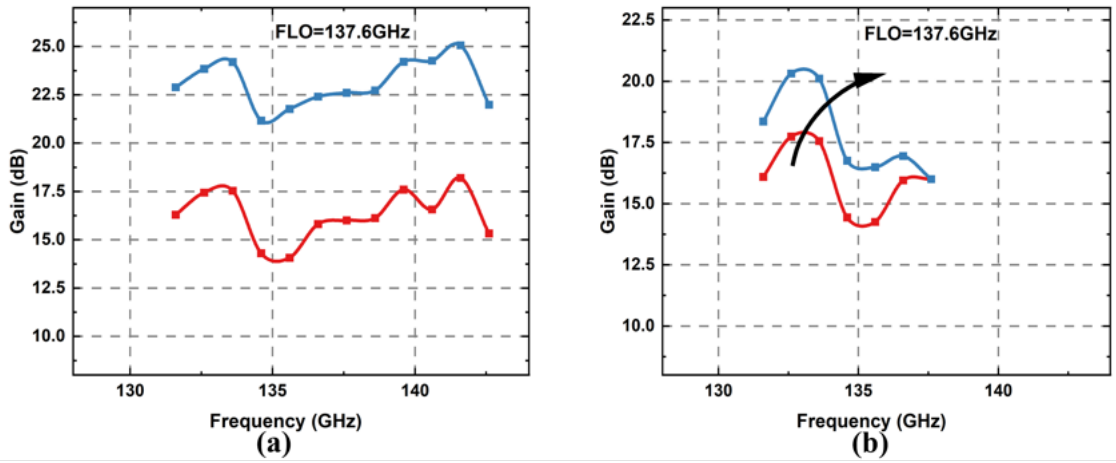


Figure 2.9: Measured power gain versus frequency at different gain settings.

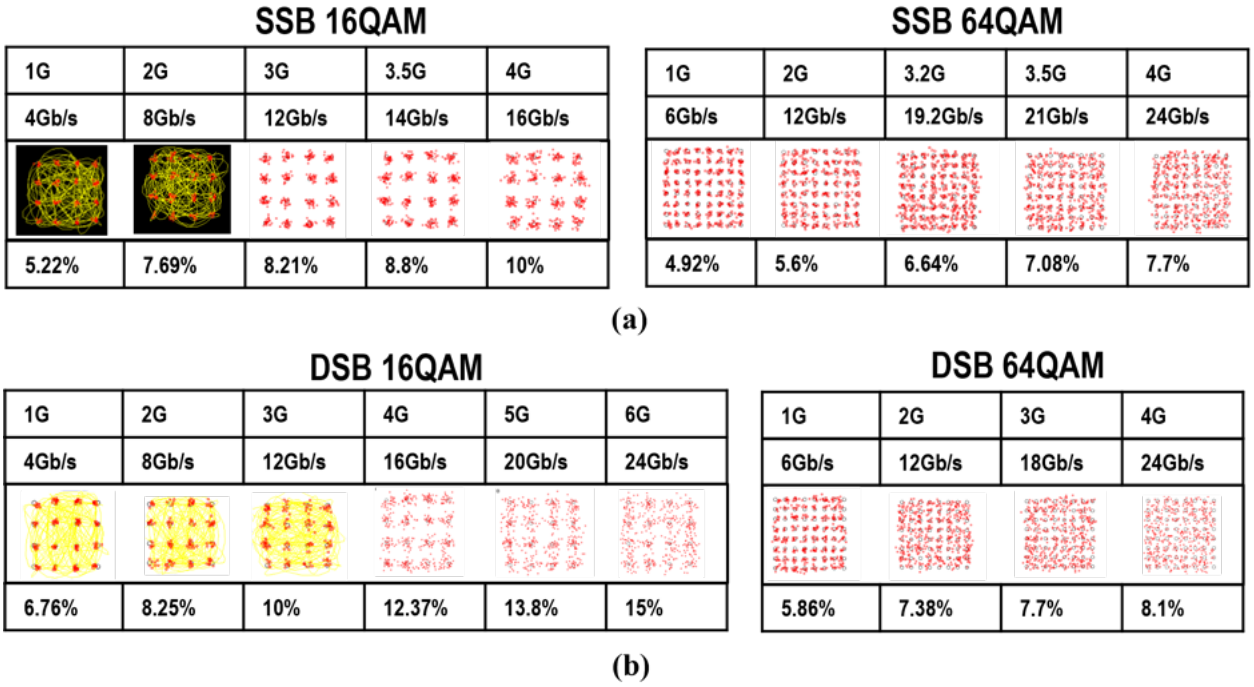


Figure 2.10: EVM measurement results of D-band CMOS TX.

Table 2.1: Comparison of Calculated EVM and measured EVM in SSB Mode.

Symbol Rate	Calculated EVM	Measured EVM	EVM_{PN}
2 Gbaud	7.37%	7.69 %	6.47%
3 Gbaud	8.9%	8.21 %	7.87%
4 Gbaud	10.4%	10 %	9.14%

2.6.3 TX EVM Measurements

We build an external receiver consisting of a horn antenna, LNA and mixer to characterize the TX's EVM performance, and measure the TX EVM for both SSB and DSB configurations. A Keysight M8196A AWG generates 16- and 64-QAM waveforms to feed the TX baseband input, and the down-converted signal is demodulated by Keysight 89600 VSA with internal equalization. Regarding the SSB mode, limited by the test setup, the maximum symbol rate of the data which can be fed into the TX baseband is 4Gbaud. Therefore, in SSB mode, the TX can support up to 16Gbps 16-QAM and 24Gbps 64-QAM (Fig.2.10(a)). In addition, the EVM performance in SSB mode is also limited by the SSB LO phase noise. In terms of the DSB mode, the TX can support up to 24Gbps 16-QAM and 24Gbps 64-QAM (Fig.2.10(b)). The maximum data rate is limited by the phase noise performance of LO signal although the carrier recovery circuit and other digital processing algorithms in VSA's demodulator can compensate the phase noise to some extent. The relationship between the TX EVM and impairments can be expressed as ,

$$\approx \sqrt{\frac{1}{SNDR^2} + EVM_{LOFT}^2 + EVM_{PN}^2 + EVM_{IMRR}^2 + EVM_{GF}^2} \tag{2.1}$$

Where EVM_{PN}, EVM_{IMRR}, EVM_{LOFT}, and EVM_{GF} represent the degraded EVM due to integrated phase noise(IPN) of a carrier, I/Q mismatch, LO leakage, and gain flatness, respectively. Therefore, the actual EVM contribution of LO phase noise after compensation can be estimated from (2.1). To simplify our analysis, we take the SSB mode as the example. In this case, the EVM_{IMRR}, EVM_{LOFT}, and EVM_{GF} are close to 0 (with equalization). For 1G symbol rate 16-QAM, the calculated RX SNDR in test is about 32dB. Therefore, the calculated EVM_{PN} is about 4.58% and IPN is about -26.7dBc, which has $>$ 5dB improvement compared to the IPN (-21.2dBc for 1GHz BW) of the PLL SSB phase noise (normalized at the LO frequency). We use the IPN with compensation to estimate the EVM at higher symbol rates, and the calculation matches well with the measurements (Table I). It implies that the on chip PLL's phase noise is the main contributor to EVM, which limits the maximum data rate which the TX can support.

Table 2.2 summarizes the measurement results of the complete TX and compares the results to the state-of-the-art D band TXs. The packaged TX achieves comparable performance, while integrating all components of a transmitter into a single package with high energy efficiency.

Table 2.2: Performance Comparison of state-of-the-art D-band transmitters.

	[2] ***IMS'2021***	[3] ***SSCL'2021***	[27] ***VLSI'2021***	[15] ***ISSCC'2022***	[24] ***JSSC'2022***	This Work
Package	Yes	No	No	Yes	No	Yes
Technology	22 nm FD SOI	45 nm SOI	28 nm Bulk CMOS	130 nm SiGe BiCMOS	45 nm SOI	28nm Bulk CMOS
Antenna Integration	Yes	No	No	Yes	Yes	Yes
Frequency(GHz)	131-137	140-158	140-160	130-164	136-147	>132-144
EIRP at Psat(dBm)	13	N/A	N/A	N/A	28-32	9-10.6
TX Psat(dBm)	1.95	0.1	13	12	Unknown	6-7.62(w/de-embedding) 3-4.6(wo/de-embedding)
TX Pdc(mW)	210	420	586	265	231*8	128
Package Loss(dB)	0.85-1.1	N/A	N/A	unknown	N/A	1
Data Rate Modulation	15Gbps 64-QAM	8*10.56Gbps 64-QAM(channel bonding)	10Gbps 16-QAM	30Gbps/14Gbps 64-QAM/256-QAM	>16Gbps 16-QAM/64-QAM	24Gbps 16-QAM/64-QAM
On-chip PLL	No	No	*	No	No	Yes

Chapter 3

Charm Transmitter Version 2 (V2)

3.1 Introduction

Silicon-based sub-THz (100-300GHz) systems will play a significant role to meet the 100+ Gb/s in future wireless communication system. Specifically, D band (110-170GHz) transceivers implemented in a bulk CMOS process provides an attractive and cost-effective solution to achieve the 100+ Gb/s data rate.By placing the carriers at the frequency bands further away from fmax for CMOS, it is feasible to balance the design trade-offs such as gain, bandwidth, power handling capability and efficiency from active device and thus enable the implementation of energy efficient systems. Furthermore,bulk CMOS technology provides the solution to achieve a high integration and low-cost system. However, wireless signals suffer from severe path loss at D band frequencies, which requires the transmitter to provide high output power and acceptable power efficiency to overcome the high propagation loss and meet the system design budget. Both the transistors' low breakdown voltage and significant loss of passive network in bulk CMOS technology limit the maximum output power and efficiency.

While recent publications have demonstrated high performance D-band transmitters capable of high-order and wide-bandwidth modulation, very few of them have achieved simultaneous high data rate (> 100 Gb/s) and high output power. On one hand, the published works demonstrating >100 Gb/s data rate achieve only moderate output power with limited TX power efficiency. [1] fabricated in SiGe BiCMOS achieves the data rate of 200 Gb/s using 32QAM, however, the Psat of this phased array TX is -8 dBm with 2.5W DC power consumption. [11] demonstrates 120 Gb/s data rate, while achieving -5 dBm output power with 292 mW. [22] also implemented a fully integrated D-band TX achieving 160 Gb/s (16QAM) for +0.8 dBm output power. On the other hand, recently, D-band transmitter modules[14, 24] have demonstrated high effective isotropic radiated power (EIRP). However,the max reported data rate of these works have still fallen short of 100 Gb/s. [14] achieves > 16 Gb/s data rate with 28dBm EIRP at OP1dB. [24] adopts channel bonding to attain 57.6 Gb/s data rate with EVM of 15.1 - 17.9 % (-14.9 - -16.4 dBc), and 26.4dBm EIRP at OP1dB with 25dBi antenna gain. This work fills the gaps in the D band TX implementation, demonstrat-

ing a D-band TX module which not only achieves > 100 Gb/s data rate with competitive energy efficiency but also achieves high EIRP with high system efficiency(η = Pout/Pdc).

This chapter presents the design of a D-band TX module that targets next generation wireless communication and therefore attempts to achieve both high data rate and high EIRP with high system efficiency through a combination of techniques by (1) leveraging a slotline-based power combiner for high output power generation, (2) intensively employing low-loss slotline based matching networks, (3) utilizing negative resistance compensation (NRC) techniques in the up-conversion mixer for conversion gain and linearity enhancement via a combination of NMOS and PMOS cross-coupled pairs, and (4) implementing low power baseband amplifiers via current re-use g_m-cells.

The overall TX architecture is presented in Section 3.2, while Section 3.3 describes the implementation of slot line based passive structures and circuits. Section 3.4 presents measurement results. Finally, Section 3.5 concludes the chapter.

3.2 Overview of the 140GHz TX Module

The block diagram of the D-band 4-element Phased-array TX chip is shown in Fig.3.1. The TX ICs are designed to be directly attached to the feed points of the antennas on the interposer. The chip on the interposer is mounted on the PCB as a ball grid array (BGA) module. In order to increase the EIRP and thus overcome the free space path loss, phased-array systems are desired. Compared with other beamforming architectures, the digital beamforming(DBF) architecture features the highest beamforming precision, highest precoding freedom, flexible multibeam ability, and fast beam steering speed[6]. The main constraint of utilizing DBF in D-band frequency is the power consumption of high speed (>25 GS/s) ADC/DAC. However, this limitation is being gradually overcome. Recent publications have demonstrated high speed ADC/DAC with low power consumption, which can be leveraged in DBF Systems. A DBF architecture is therefore used at D-Band[Fig. 3.1], and this work presents a 4-element D-Band phased-array transmitter.

Regarding the single channel TX, it adopts the direct up-conversion architecture. The employment of the zero-IF architecture can eliminate the image signal without external filtering. In addition, this architecture result in enhanced efficiency since the signal processing bandwidth is equal to that of the desired signal. The conceptual diagram in Fig. 3.1 shows how this is achieved: taking specially produced BB data and creating a RF signal with independent signals appearing above and below the LO. In practical applications, the combined BB signals will be generated in the digital domain.

As shown in Fig. 3.1, the single channel TX includes the input matching network with ESD protection, the re-configurable analog baseband, an I/Q Gilbert cell based up-conversion mixer with negative resistance compensation (NRC) and slotline-based I and Q path combiner, and 2-way power combined PA. The DC offset cancellation circuit (DCOC) are employed in the baseband to calibrate LO leakage. In the following section, we present the

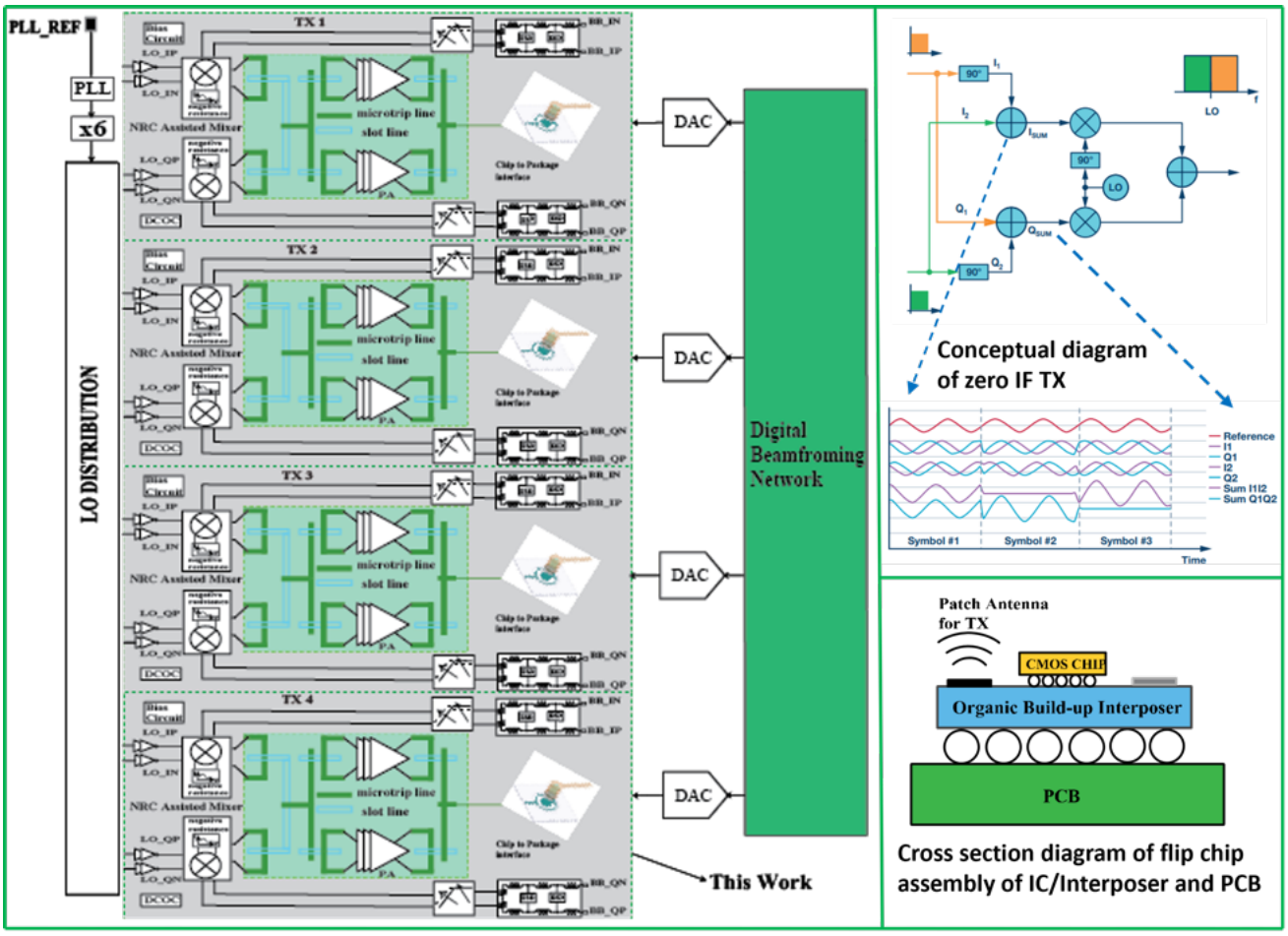


Figure 3.1: Overview of the D-band TX Module.

working principle of each circuit block and techniques to achieve simultaneous high data rate and improved EIRP with enhanced system efficiency.

3.3 Circuit Implementation

3.3.1 Slot Line Based Passive Structures

Although the slotline was first proposed for use in microwave integrated circuits by Cohn [30] in 1969, slot line based passive structures are scarcely used in mm-wave and sub-THz integrated circuits. Until recently , slotline based passive structures[26],[8],[12], and [19] have been utilized in sub-THz integrated circuits and achieved superior performance from the perspective of both bandwidth and insertion loss. This chapter explores more variants

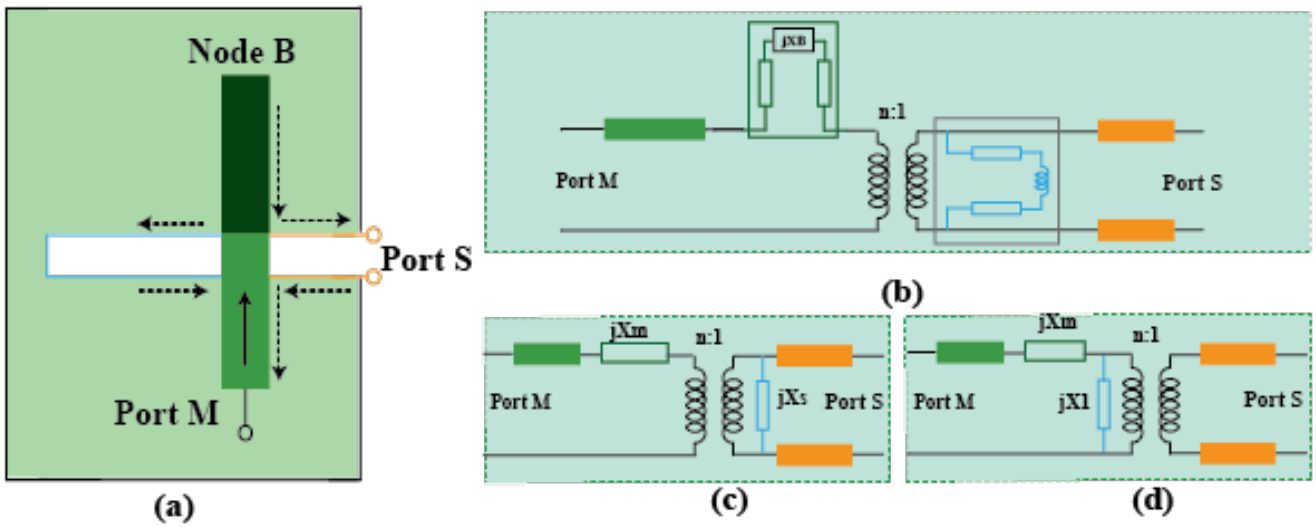


Figure 3.2: (a) Layout of the M-to-S transition. (b) Equivalent circuit model of the M-to-S transition. (c) Simplified equivalent circuit model with jXm and jXs. (d) Transforming Xs to the other side.

of slot line based passive structures and provide detailed analysis of these structures.

3.3.1.1 Microstrip-to-Slotline(M-to-S) Transition

Slotlines are usually incorporated with microstrip lines, and the microstrip-to-slotline transition has been comprehensively analyzed by many investigators. Fig. 3.2 shows the diagram of the M-to-S transition and its equivalent circuit model. Z_{0s} and Z_{0m} refer respectively to the characteristic impedances of slot line and microstrip line. θ_s and θ_m are the electrical lengths of the extended portions of the slotline and microstrip line respectively. The transformation turn ration n is a function of Z_{0s} and Z_{0m}, and describes the coupling between the slot line and microstrip line.

Assuming the input signal is fed to the microstrip from the bottom side. The return path of the extended microstrip line encounters the slotline and continues traveling along the edges of the slot, making the transformer in series with the return path of the microstrip. Moreover, at the cross junction of the slotline and microstrip line, the return currents induces a slotline magnetic field and together with transverse electric field to propagate along the slotline, so the slotline (blue stub) is connected in parallel with the transformer. Due to the reciprocity of the metal structures, this kind of transition can happen in a reverse fashion from the slotline to the microstrip line.

The circuit model in Fig. 3.2(b) can be redrawn as in Fig. 3.2(c) for further analysis. Fig. 3.2(d) shows the circuit after transforming X_S to the other side of the transformer and

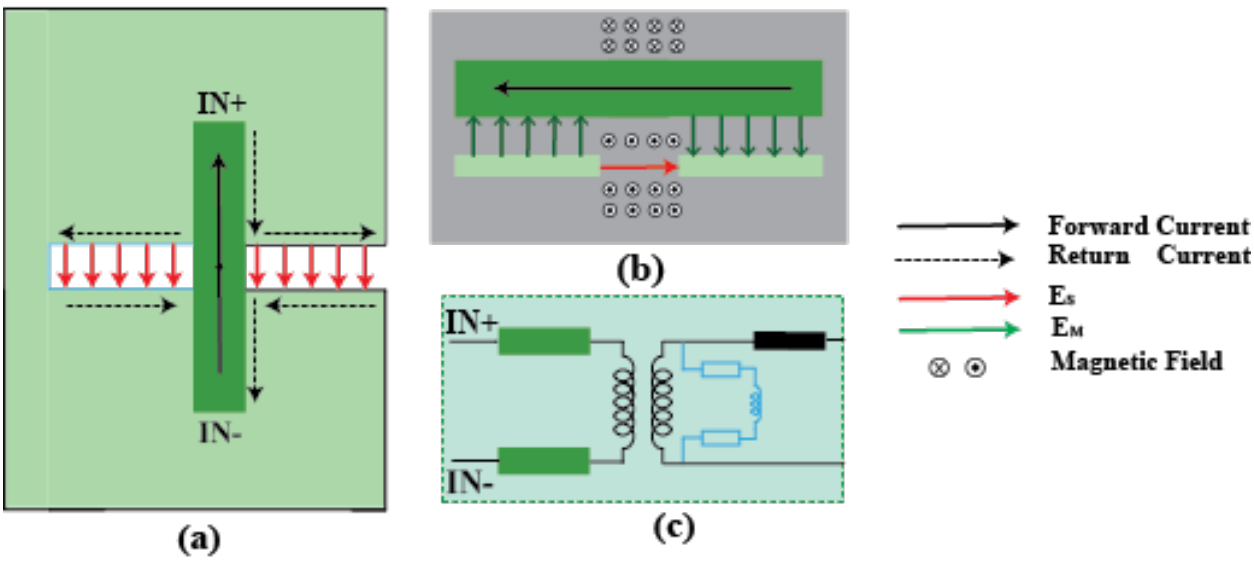


Figure 3.3: (a) M-to-S Transition layout and electrical field distribution. (b) Cross section of the M-to-S Transition layout and electrical field distribution. (c) Equivalent circuit model of the M-to-S transition when two out-of-phase signals are fed to this structure.

$X_1 = n^2 * X_S$. Here,

$$jX_s = Z_{0s}\frac{jX_{0s} + jZ_{0s}tan\theta_s}{Z_{0s} - X_{0s}tan\theta_s} \tag{3.1}$$

and

$$jX_m = Z_{0m}\frac{jX_B + jZ_{0m}tan\theta_m}{Z_{0m} - X_B tan\theta_m} \tag{3.2}$$

3.3.1.2 Extension to Two Inputs (in-phase and out-of-phase)

As indicated in Fig. 3.3, when the two out-of-phase (odd-mode) signals generated from the differential amplifier are fed into this M-to-S transition, a time-varying electrical field E_M and magnetic field H_M also start traveling along the microstrip line. This magnetic field induces a time-varying electric field E_S at the cross section of the slot line and microstrip line, and this electrical field results in a time varying current along the edges of the slot. This current produces the slotline time-varying field H_S. The TEM wave inside the slot will then propagate to the output port. Since the electrical field E_M is orthogonal to the electrical field E_S, it mitigates the issue of the parasitic capacitor in transformers and thus achieves a perfectly balanced output. In addition, Fig. 3.4 also shows how the in-phase (even-mode) signals are suppressed.

The equivalent circuit can be obtained from Fig. 3.2 and is shown in Fig. 3.3.(c). We can observe how the series combining is achieved in this transition, and this M-to-S transition is also called microstrip-slotline series T-junction[31].

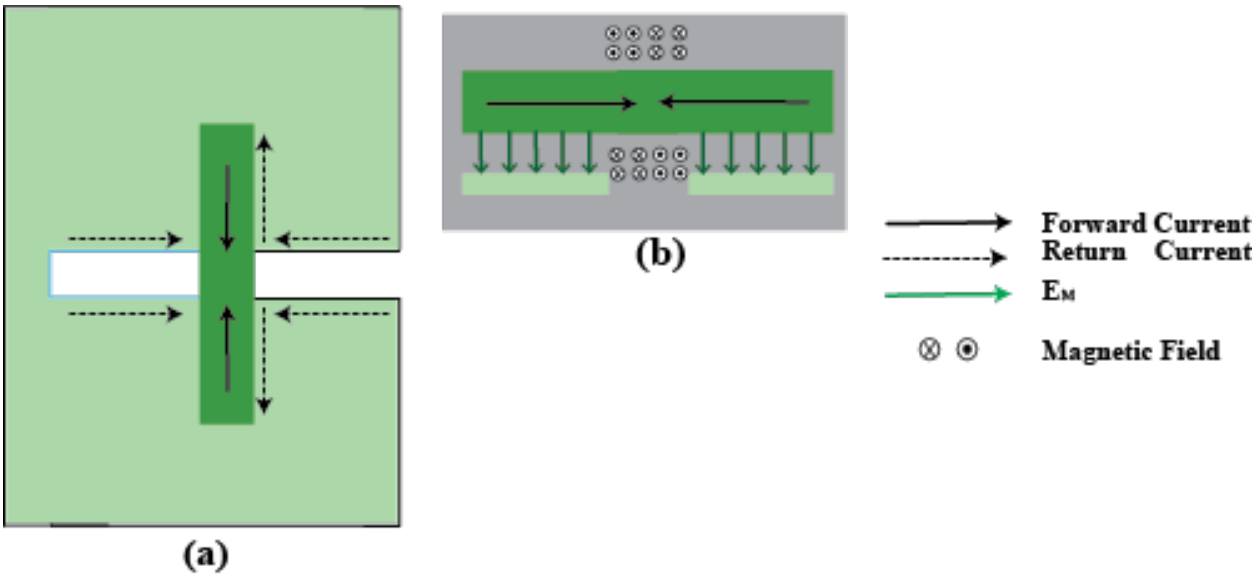


Figure 3.4: (a) M-to-S Transition layout and electrical field distribution, (b) cross section of the M-to-S Transition layout and electrical field distribution when two in-phase signals are fed to this structure.

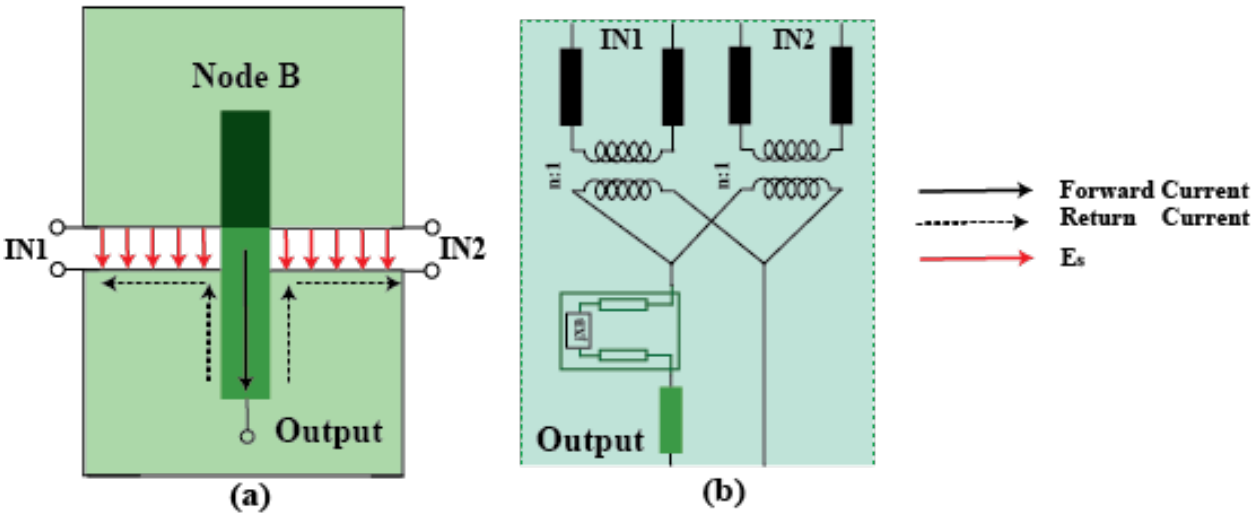


Figure 3.5: (a) S-to-M Transition layout and electrical field distribution. (b) Equivalent circuit model of the S-to-M transition when two in-phase signals are fed to this structure.

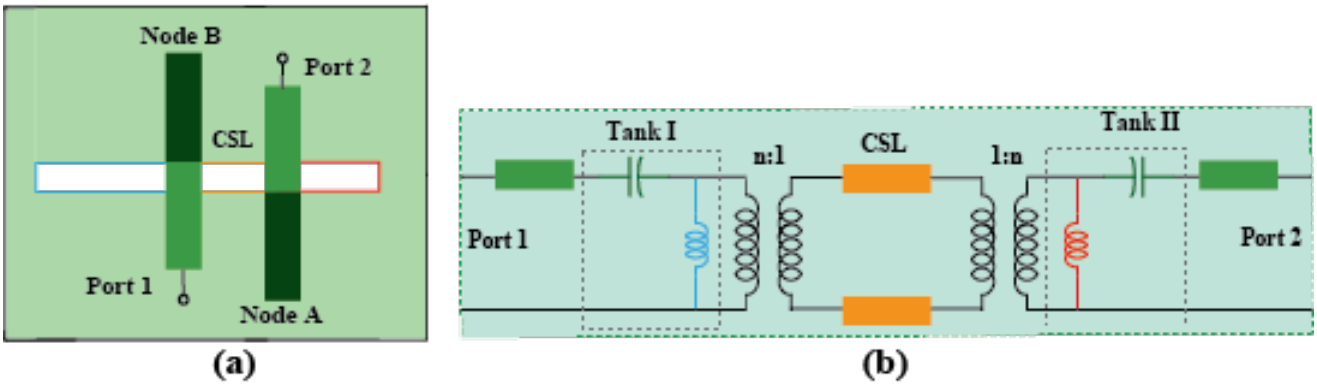


Figure 3.6: (a) Layout of the cascading M-to-S and S-to-M transitions. (b) and (c) show the equivalent circuit models of the cascading M-to-S and S-to-M transitions with floating nodes B and C.

Another T-junction can be obtained in the S-to-M transition. When the in-phase (even-mode) signals are fed into this transition, the slotline arms and the microstrip arm are connected in parallel to each other, and thus creating parallel combining. The configuration of this transition, the corresponding electrical field distribution in the slotline and the equivalent circuit model are shown in Fig. 3.5.

3.3.1.3 Analysis of Cascaded M-to-S and S-to-M Transitions

By cascading M-to-S and S-to-M transitions, two or three resonant modes can be created to achieve a wideband performance. Fig. 3.6(a) depicts the layout of the cascaded M-to-S and S-to-M transitions. If both node B and node A are floating nodes, we can produce the equivalent circuit model in Fig. 3.6(b). This equivalent circuit model consists of two microstrip open-circuited stubs, two slotline short-circuited stubs, and one connecting slotline (CSL). For further analysis, we can redraw Fig. 3.6(b) in Fig. 3.6(c). The two tanks are coupled together through CSL, creating two resonant frequencies. The lower and upper cutoff frequencies can be chosen to be far away from each other to acquire the desired wide bandwidth. The ABCD matrix of cascaded series open-circuited stub and shunt short-circuited stub shown in Tank I/II of Fig. 3.6(c) can be calculated as

$$Cascaded\_ABCD = \begin{bmatrix} 1 & -j * Z_{0m} * cot(\theta_m) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ -j * (1/Z_{0s)} * cot(\theta_s)/(n^2) & 1 \end{bmatrix} \tag{3.3}$$

$$= \begin{bmatrix} 1 - Z_{0s} * cot(\theta_s) * cot(\theta_m)/Z_{0s)}/(n^2) & -j * Z_{0m} * cot(\theta_m) \\ -j * cot(\theta_s)/Z_{0s}/(n^2) & 1 \end{bmatrix} \tag{3.4}$$

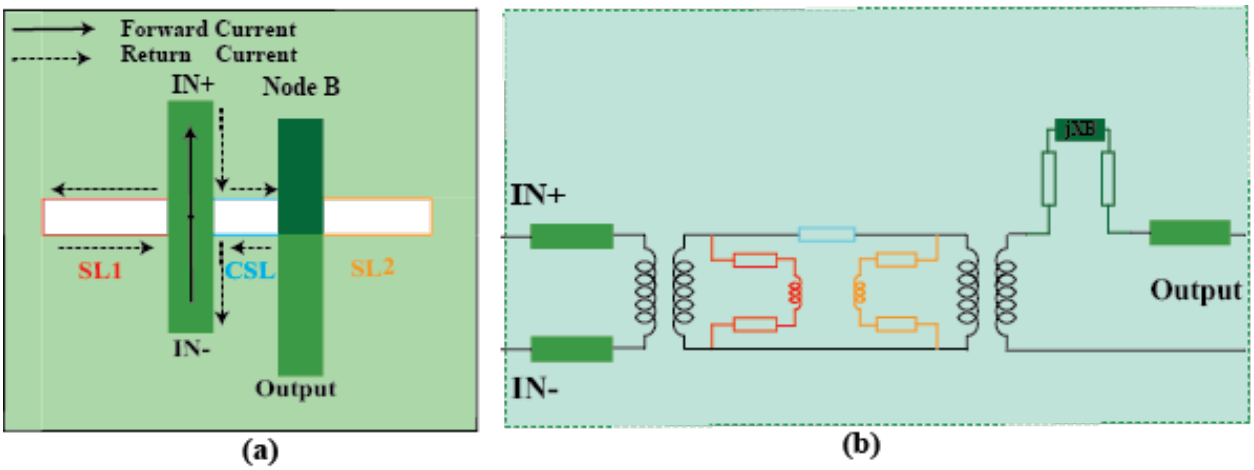


Figure 3.7: (a) Layout of the slot balun. (b) Equivalent circuit model of the slot balun.

3.3.1.4 Slot Line Based Power Combiners and Power Splitter

Although increasing the transistor size of the PA output stage can increase the output power, large transistor size will bring extra routing parasitics and thus result in lower power gain and efficiency. In order to further boost the output power with reasonably high efficiency, power combiners are employed. However, traditionally power combiners such as transformer based differential two-way power combiners suffer from high insertion loss and imbalanced impedances at their input ports. The non-uniform impedances at the input ports will cause non-optimal loading of each PA output stage cells and thus affect the combined output power. The combination of the M-to-S transition and S-to-M transition provides a solution to achieve a low loss, broadband and balanced power combiner.

Fig. 3.7 shows the general configuration of the 2-way slotline based power combiner. The 2-way slotline based power combiner (slot balun) consists of one M-to-S transition (series combining) and one S-to-M transition. The two transitions are connected together through a short slot line. As discussed in the previous sections, different from conventional baluns, the slot balun can suppress the undesired common mode over the entire operation bandwidth and achieve perfect balance. The slot balun also features greater design flexibility. As illustrated in the equivalent circuit model of the slot balun (Fig. 3.7(b)), there exist multiple ways to create multiple resonators and thus enable multi-resonating modes, which is crucial to achieve the bandwidth enhancement. Among these options, we can choose the one which provides the lowest loss after the bandwidth requirement is satisfied. Fig. 3.8 and Fig. 3.9 shows two of these options.

Regarding option 1, we engineer the extended portion of the microstrip in the S-to-M transition to a short-circuited stub, and transforming the CSL, SL1 and SL2 to the other side of the transformer.

Regarding option 2, we engineer the extended portion of the microstrip in the S-to-M

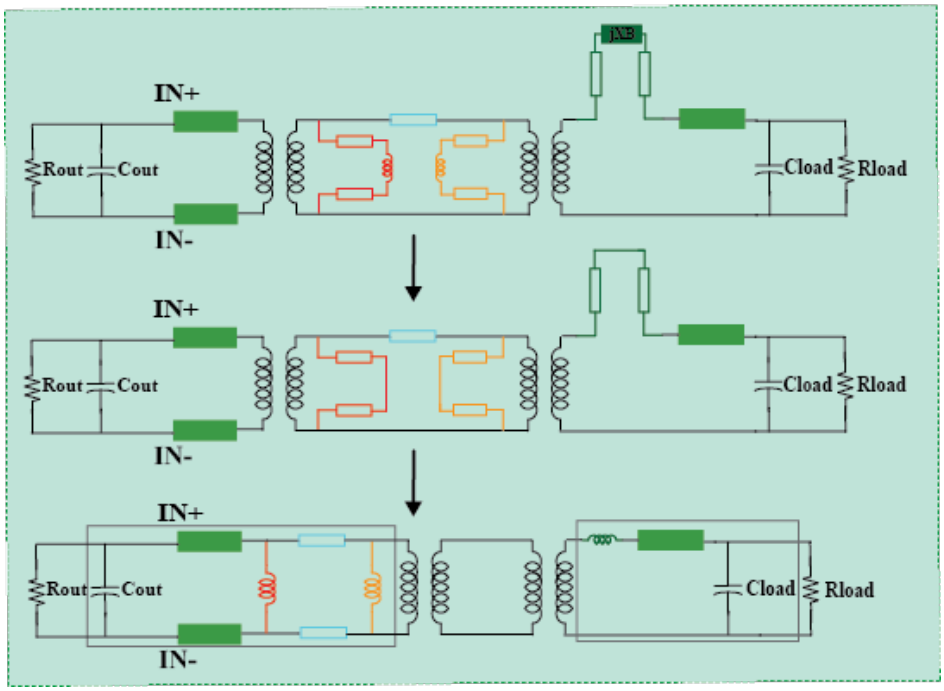


Figure 3.8: Option 1.

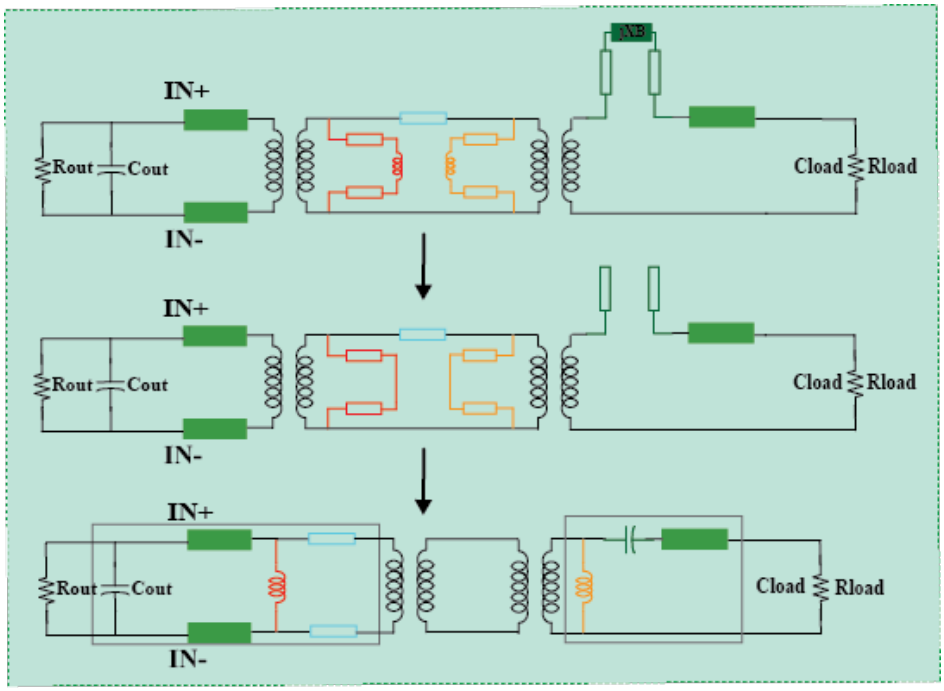


Figure 3.9: Option 2.

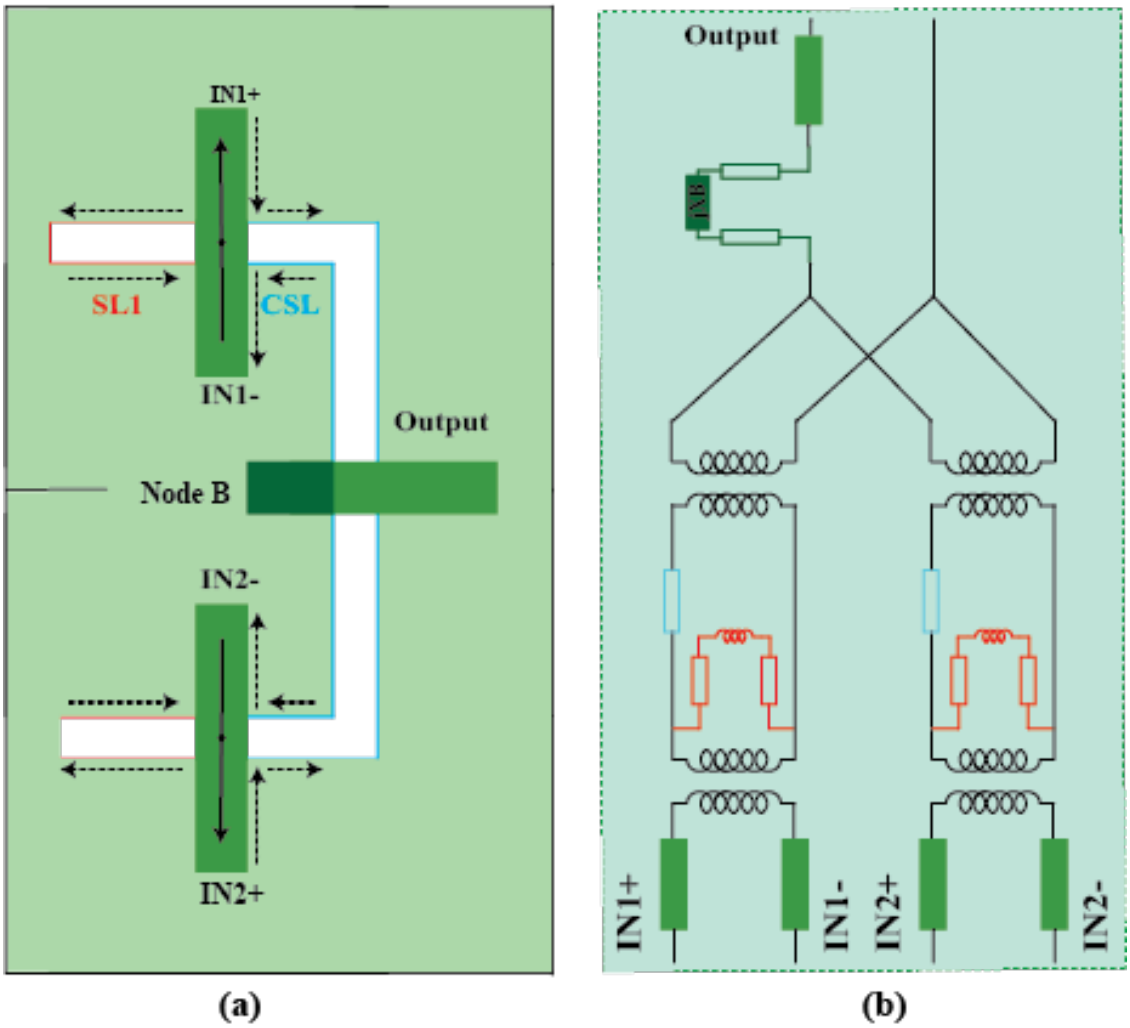


Figure 3.10: (a) Layout of the 4-way slotline based power combiner. (b) Equivalent circuit model of the 4-way slotline based power combiner.

transition to a open-circuited stub, and transforming the CSL, SL1 and SL2 to the other side of the transformer.

Fig. 3.10 shows the general configuration of the 4-way slotline based power combiner. The 4-way slotline based power combiner is comprised of two M-to-S transitions (series combining) and one S-to-M transition.

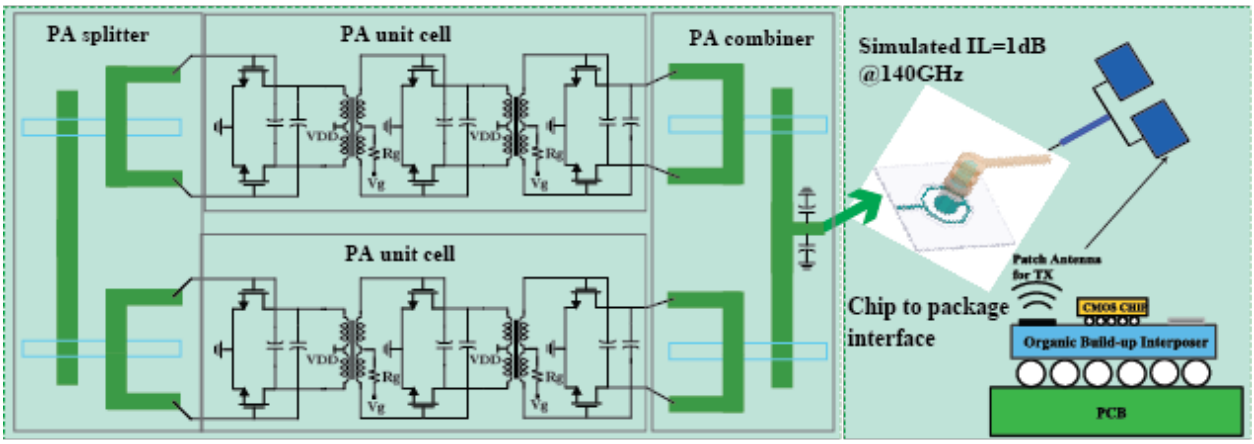


Figure 3.11: Diagram of the 2-way power combined PA.

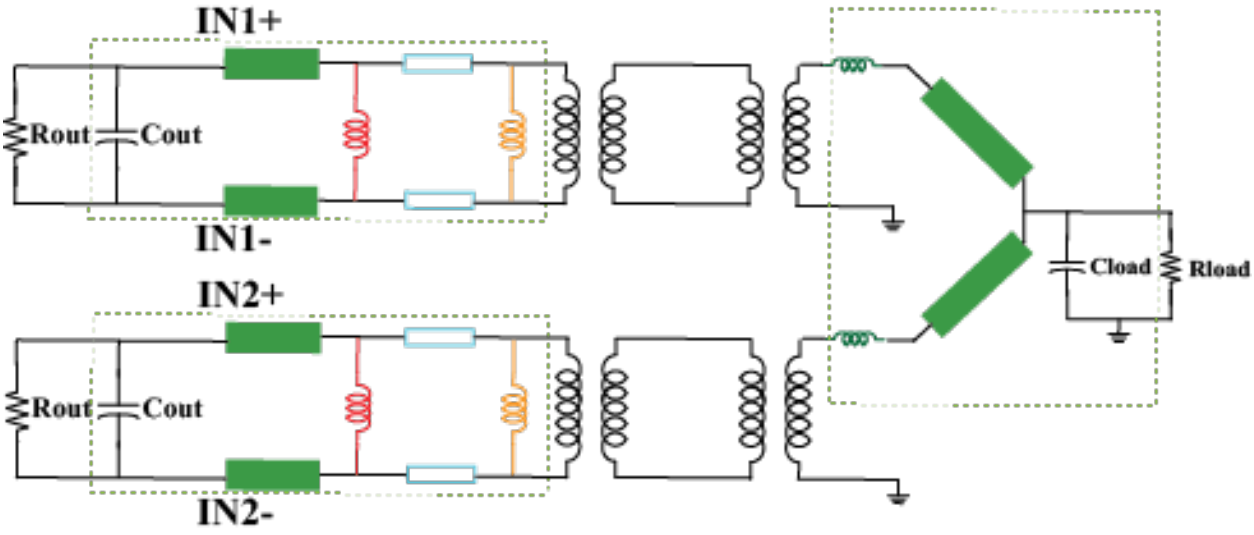


Figure 3.12: Circuit model of the power combiner

3.3.2 PA Design with Slotline Based Power Splitter and Power Combiner

Fig. 3.11 shows the 2-way differential PA unit cell which consists of a cascade of three NMOS capacitively neutralized differential pair (NDP), two driver stages for enough gain, and one power stage. The size ratios of the three stages are 1:1.5:2.4, chosen based on both the cascaded linearity and power efficiency. The utilization of neutralization can improve both Gmax and differential mode stability. Nevertheless, the common-mode stability will degrade. To stabilize the common mode, a series resistor Rg is connected to the center tap of the gate coils.

To improve output power, a slotline based power combining network is implemented, which features compact layout, low loss and wide bandwidth. As shown in Fig. 3.11, the power combining network consists of two slot baluns and one zero-degree combiner. Fig. 3.12 shows the equivalent circuit model of this power combining network.

3.3.3 Quadrature Up-Conversion Mixer with Negative Resistance Compensation (NRC)

Fig. 3.13 shows the schematic of the quadrature up-conversion mixer. The input G_m-cell is based on a partially neutralized differential pair. This helps to reduce the input capacitance of the mixer and improves the conversion gain of the mixer without degrading the linearity of the mixer. Negative resistance compensation (NRC) is utilized to further improve the conversion gain and linearity of the up-conversion mixer. The NRC is implemented via a combination of NMOS and PMOS cross-coupled differential pairs. The PMOS cross-coupled differential pair can also injects current to the input G_m cell and thus results in slight linearity improvement of the mixer.

Based on the simplified circuit model shown in Fig. 3.14, the conversion gain with and without the NRC can be briefly derived. Since RF current produced by M1 is split between C_{mid} and the resistance seen at the source of LO switch transistor M3 ($1/g_{m3}$), the conversion gain (CG) without NRC can be expressed as

$$\frac{2}{\pi} * g_{m1} * Rp * \frac{gm3}{\sqrt{(g_{m3})^2 + (C_{mid})^2 * w^2}} \tag{3.5}$$

Here C_{mid} is the parasitic capacitance at Node mid, contributed by the capacitance of the LO switch transistors, input G_m transistors and routing parasitic capacitance.

After insertion of the cross-coupled differential pairs, the CG can be expressed as

$$\frac{2}{\pi} * g_{m1} * Rp * \frac{gm3}{\sqrt{(g_{m3} - g_{nrc})^2 + (C_{mid} + C_{nrc})^2 * w^2}} \tag{3.6}$$

Here g_{nrc} is the sum of the equivalent input transconductance of the NMOS and PMOS cross-coupled differential pairs, and C_{nrc} is the extra parasitic capacitance intruduced by the

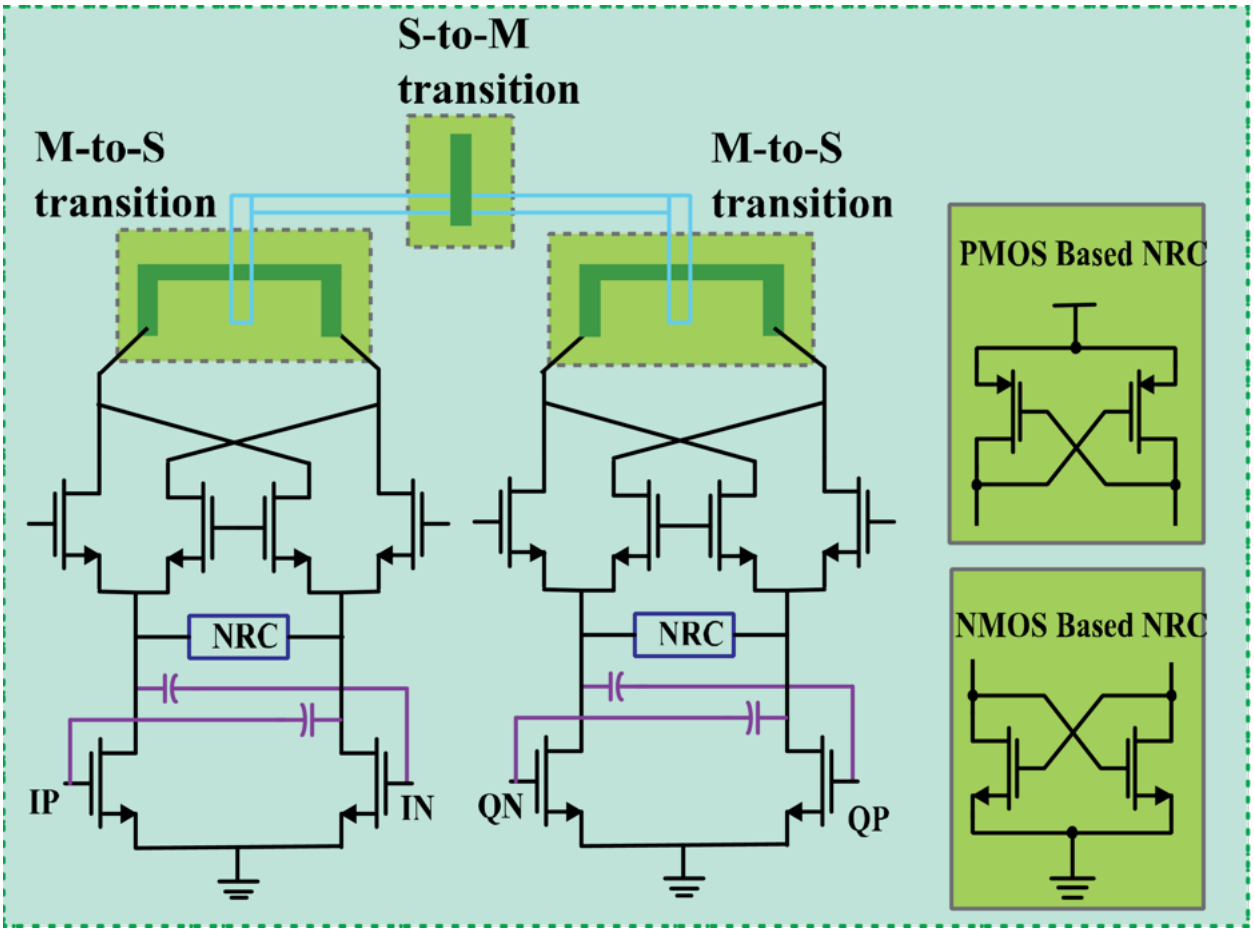


Figure 3.13: Schematic of the up-conversion mixer.

NMOS and PMOS cross coupled differential pairs. Comparing (3.5) and (3.6), CG can be enhanced by employing the NRC technique, and CG can achieve a significant improvement if g_{nrc} is close to g_{m3}. In addition, negative capacitance can be introduced at Node mid to further push the performance. In our design, compared with C_{mid}, C_{nrc} is much smaller and thus this parasitic capacitance has minimal effect on CG.

The I and Q mixer path are combined together through a slotline power combiner. This slotline power combiner is composed of two M-to-S transitions (series power combining) and one S-to-M transitions (parallel power combining), achieving simultaneous impedance matching and power combining.

To maintain the linearity after cascading the mixer and PA together, one should guarantee that the mixer's OP1dB is a few dBm higher than the IP1dB of the PA. Compared to PA without power combining, the PA with power combining will have higher OP1dB. However, if the PA with power combining utilizes the same number of stages as that of the PA without power combining, its gain won't increase and thus its IP1dB will increase. Higher gain is

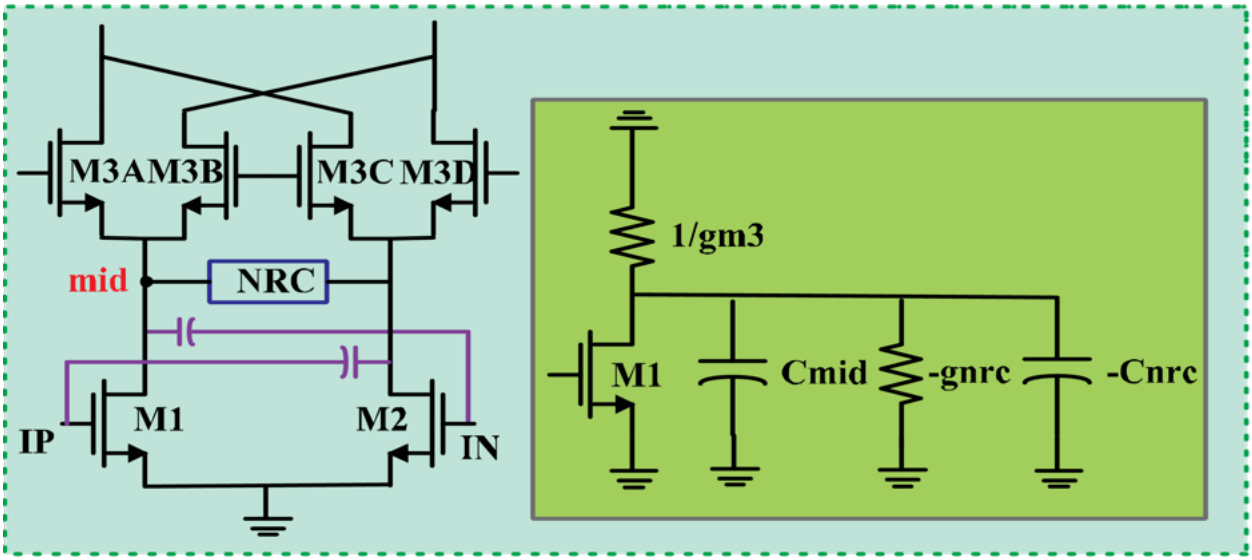


Figure 3.14: Simplified circuit model for mixer conversion gain calculation.

usually preferred (especially for power combining PA), which results in lower IP1dB for the same output power and this further relaxes the requirement on the OP1dB of the up-conversion mixer. However, at D-band, the higher gain PA will require one to cascade more stages and cause more power consumption. The improved CG and linearity of the up-conversion stage eliminates the necessity of adding another stage in the PA, resulting in enhanced power efficiency of the whole TX.

3.3.4 TX Baseband

3.4 Measurement Results

This transmitter IC has been fabricated in 28nm bulk CMOS process, and flip-chip attached to an interposer. The chip on the interposer is mounted on the PCB as a ball grid array (BGA) module. As shown in Fig. 3.15, the single channel TX only occupies 1.1mm^2 active die area.

3.4.1 Single Channel TX Measurement

3.4.1.1 TX Psat, OP1dB and EIRP

The TX EIRP related measurements are performed with a WR-6 standard gain horn antenna cascaded with a LNA placed at 1.45m from the chip. The EIRP versus frequency is presented in Fig. 3.16. The TX results in an EIRP of 17.3dBm and 13.8dBm at P_{sat}

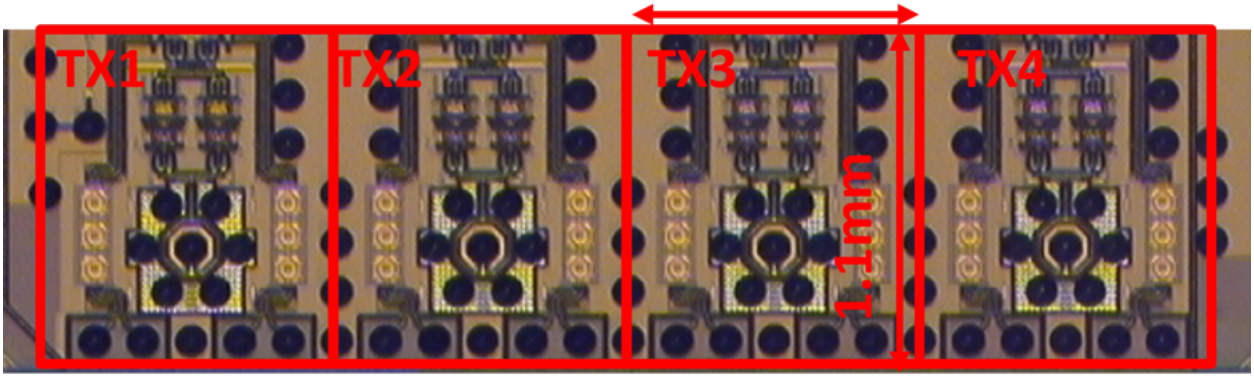


Figure 3.15: TX chip photo.

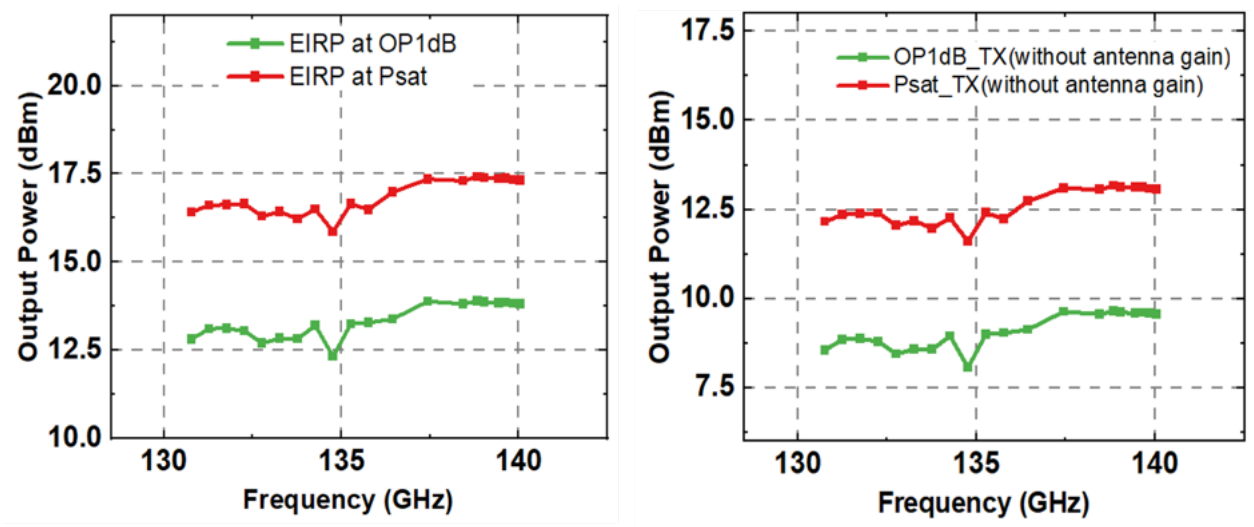


Figure 3.16: TX EIRP and TX de-embedded P_{out} versus Frequency.

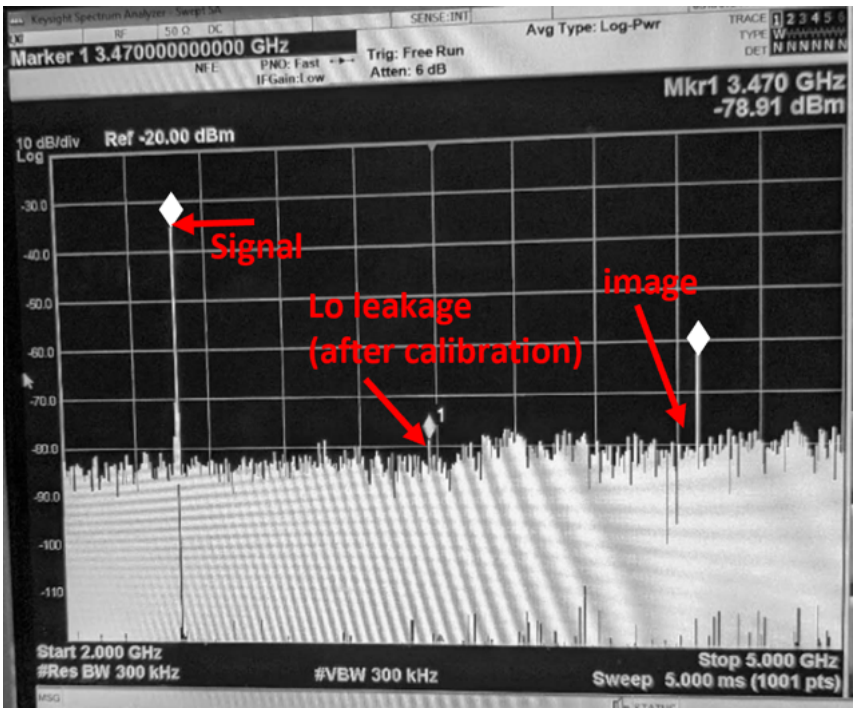


Figure 3.17: TX CW measurement.

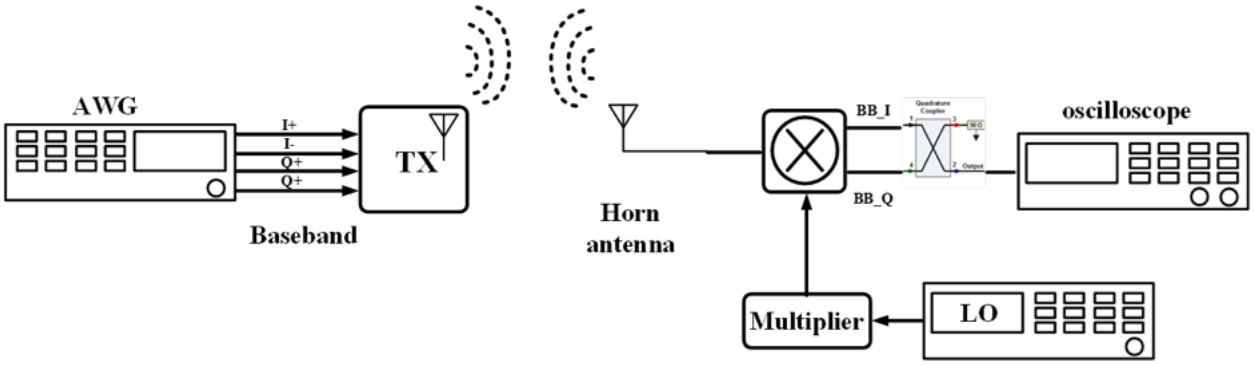


Figure 3.18: OTA test setup with SSB mode off chip RX.

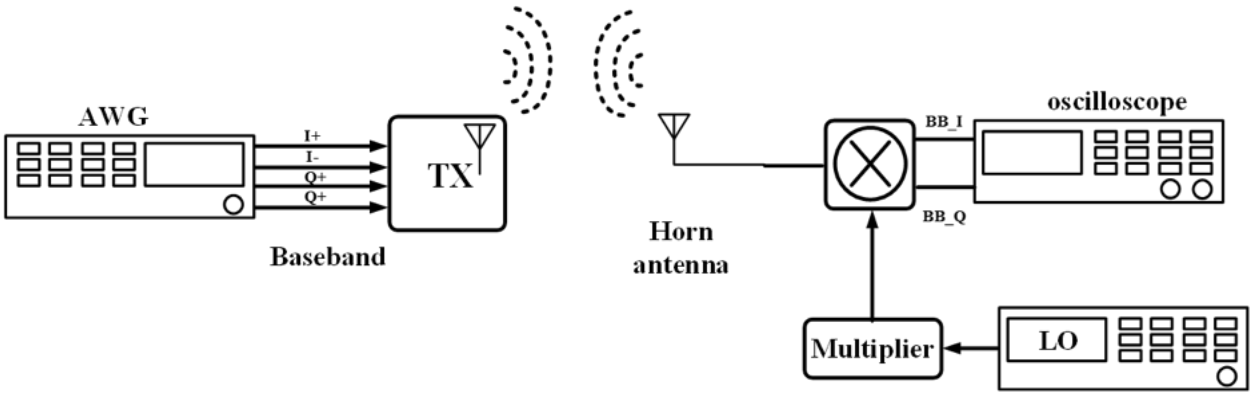


Figure 3.19: OTA test setup with DSB mode off chip RX.

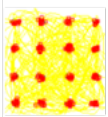
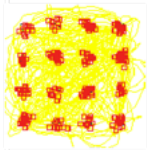
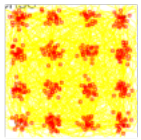
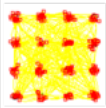
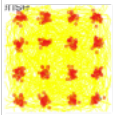
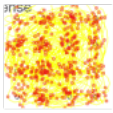
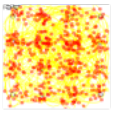
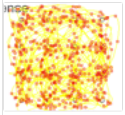
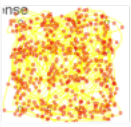
Single channel TX				
Symbol rate	4GHz	8GHz	10GHz	
Data rate	16Gb/s	32Gb/s	40Gb/s	
EVM	4.32%	6.8%	8.82%	

Figure 3.20: EVM measurement results of single channel TX with off chip SSB RX.

and OP $_{1dB}$, respectively, at 140 GHz. We also plot the TX P_{sat}/OP_{1dB} versus frequency after de-embedding the antenna gain (here the antenna gain also takes into account the chip-to-package interface loss and the T-line routing loss).

3.4.1.2 CW Measurement

Fig. 3.17 shows the measured TX CW spectrum down-converted to 2.47 GHz. The TX exhibits < -42dBc LO leakage after calibration and >25dBc IRR.

Single channel TX						
Symbol rate	4GHz	8GHz	16GHz	20GHz	25GHz	25.4GHz
Data rate	16Gb/s	32Gb/s	64Gb/s	80Gb/s	100Gb/s	101.6Gb/s
EVM	6.54%	7.8%	13.7%	14.6%	15.5%	15.9%

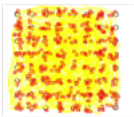
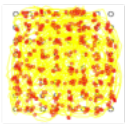
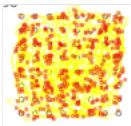
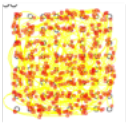
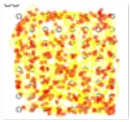
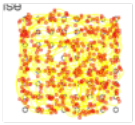
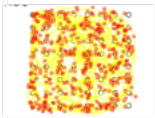
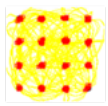
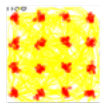
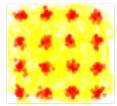
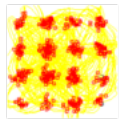
Single channel TX							
Symbol rate	4GHz	8GHz	16GHz	20GHz	22GHz	23.4G	24G
Data rate	24Gb/s	48Gb/s	96b/s	120Gb/s	132Gb/s	140.4Gb/s	144Gb/s
EVM	5.84%	6.1%	6.4%	6.77%	7%	7.3%	7.6%

Figure 3.21: EVM measurement results of single channel TX with off chip DSB RX.

3.4.1.3 TX EVM Measurements

In the OTA measurement, not only the off chip RX's SNDR plays a significant role in the measured EVM performance, but also off chip RX's image rejection ratio(IRR) will affect the measured EVM numbers. In order to accurately characterize the TX performance, as shown in Fig. 3.18 and Fig. 3.19, we configure the off chip RX in two different modes: single side band (SSB) RX and double side band (DSB) RX. For the SSB RX, the image issue of the complex mixer will be eliminated and it also capture less phase noise. It is clear that we can get better EVM number when the off RX is configured into SSB RX. However, when SSB RX is utilized, only one oscilloscope channel can be used, which will limit the max data rate which can be supported in the measurement. When DSB RX is employed, we can combine two oscilloscope channels to improve the max data rate which can be supported in the testing.

Single channel TX				
Symbol rate	4GHz	8GHz	10GHz	12GHz
Data rate	16Gb/s	32Gb/s	40Gb/s	48Gb/s
EVM	3.38%	5.9%	7.2%	9.23%

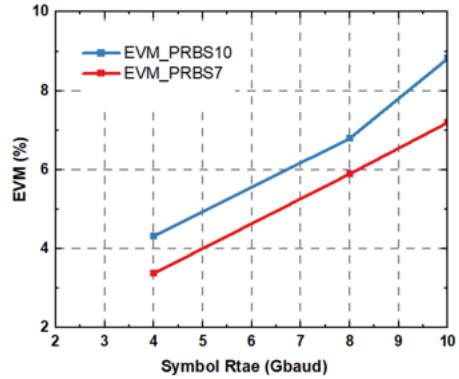


Figure 3.22: EVM measurement results of different input PRBS patterns.

3.4.1.4 TX EVM Measurements with SSB mode off chip RX

To measure the TX EVM, a Keysight AWG generates 16-QAM waveforms to feed the TX baseband I/Q differential inputs, and the down-converted signal is demodulated by Keysight 89600 VSA with internal equalization. Since the bandwidth of the oscilloscope in the measurement is 13GHz and the lower cut off frequency of the hybrid coupler is 1GHz, the max symbol rate we can support in this setup is lower than 12GHz. Fig. 3.20 shows the measured EVM results with different symbol rates in 16-QAM operations.

3.4.1.5 The effect of Data Dependent Jitter (DDJ) on EVM

In the EVM measurement, we also evaluate the effect of data dependent jitter (DDJ) on EVM by feeding 16-QAM waveforms based on different PRBS patterns (PRBS7, PRBS10,and PRBS11). Long PRBS sequence lengths offer more randomness, which stresses the interface more, leading to a higher likelihood of inducing bit-errors. Fig. 3.22 shows the measured EVM results with different symbol rates in 16-QAM operations with PRBS7. Since PRBS10 and PRBS 11 provides similar results, we compare the EVM results of PRBS7 and PRBS10 in Fig. 3. It is clear that the EVM results using PRBS7 is better than those using PRBS10. In this thesis, we only report results using PRBS10.

3.4.1.6 TX EVM Measurements with DSB mode off chip RX

To measure the TX EVM, a Keysight AWG generates 16-QAM and 64-QAM waveforms to feed the TX baseband I/Q differential inputs, and the down-converted signal is demodulated by Keysight 89600 VSA with internal equalization. Fig. 3.21 shows the measured EVM results with different data rates in 16-QAM and 64-QAM operations.

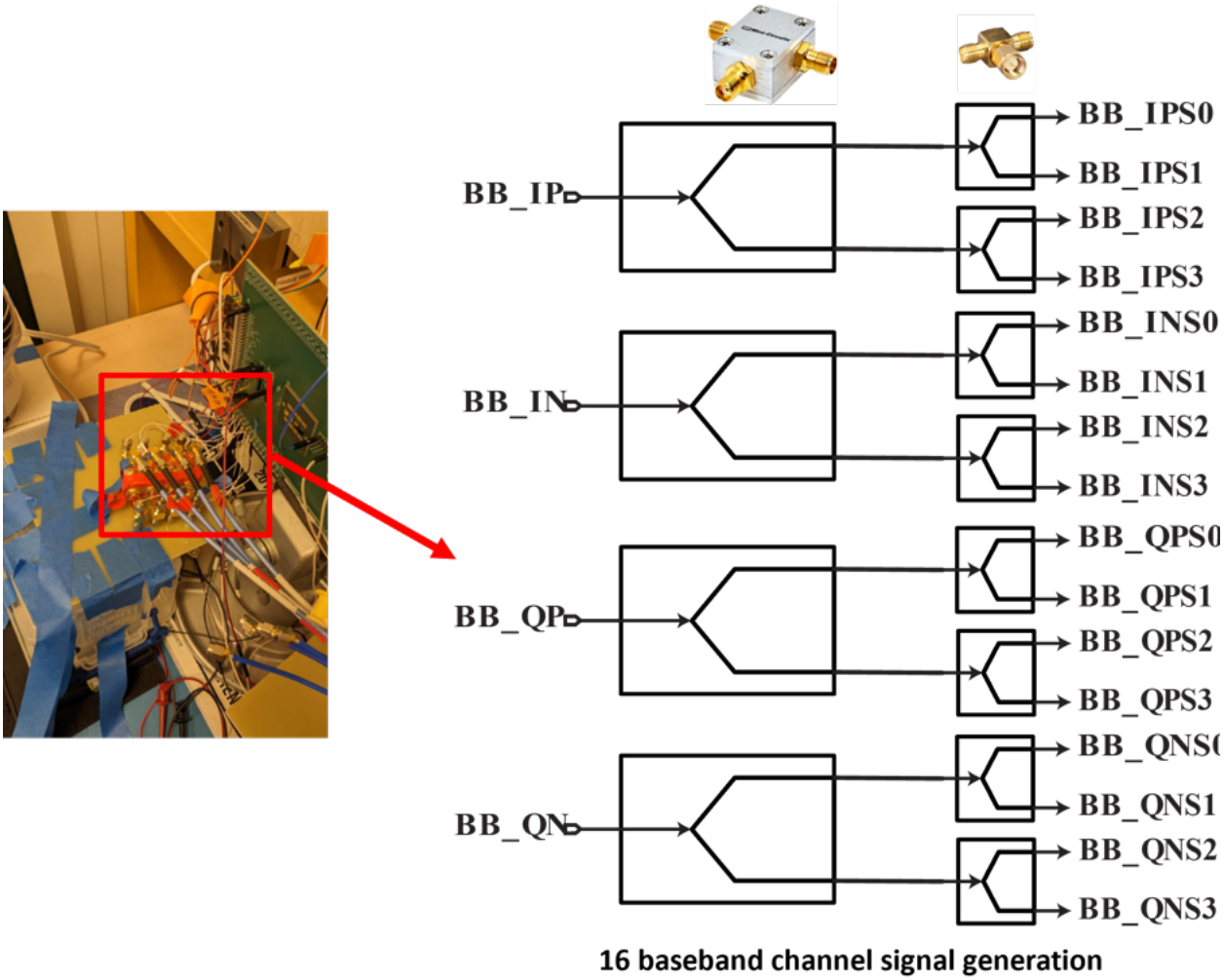


Figure 3.23: 4 Element Phased-array TX test setup.

3.4.2 4 Element Phased-Array TX Measurement

Regarding the 4 Element Phased-array TX, it will require 16 baseband signals since each TX need 4 signals: I+,I-,Q+,and Q-. As shown in Fig. 3.23, in order to generate 16 baseband signals, a 16-way power splitter consisting of 4 mini-circuit 2-way power splitters and 8 SMA 2-way splitters is built.

3.4.2.1 Phased-array TX EIRP

The 4-element phased-array TX EIRP related measurements are performed in a similar fashion as the single channel TX EIRP measurements. The EIRP versus frequency is presented in Fig. 3.24. The 4-element phased-array TX results in an EIRP of 17.3dBm at P_{sat}, at 140

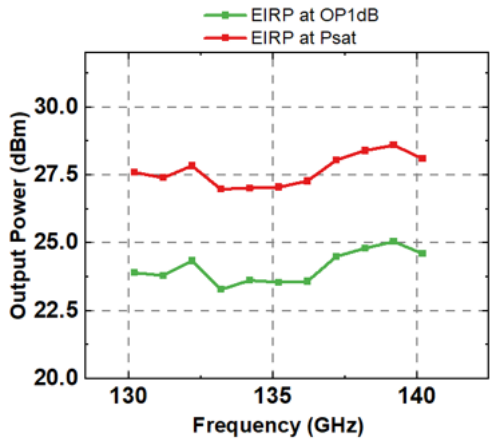
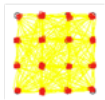
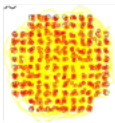


Figure 3.24: 4 Element Phased-array TX EIRP versus frequency.

Phase array TX	
Symbol rate	4GHz
Data rate	16Gb/s
EVM	3.4%

Phase array TX	
Symbol rate	4GHz
Data rate	28Gb/s
EVM	4%

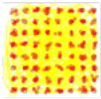
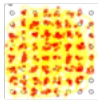
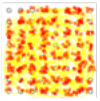
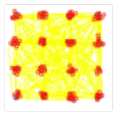
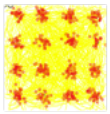
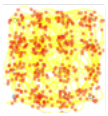
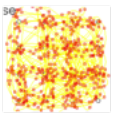
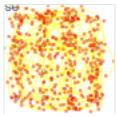
Phase array TX			
Symbol rate	4GHz	8GHz	12GHz
Data rate	24Gb/s	48Gb/s	72b/s
EVM	3.49%	5%	5.79%

Figure 3.25: 4 Element Phased-array TX EVM measurement with SSB mode off chip RX.

TX Array					
Symbol rate	4GHz	8GHz	16GHz	20GHz	25GHz
Data rate	16Gb/s	32Gb/s	64Gb/s	80Gb/s	100Gb/s
EVM	5.6%	8.3%	14.4%	15%	15.9%

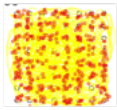
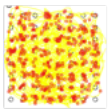
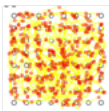
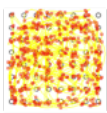
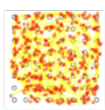
TX Array					
Symbol rate	4GHz	8GHz	16GHz	18GHz	18.4GHz
Data rate	24Gb/s	48Gb/s	96b/s	108Gb/s	110.4Gb/s
EVM	6%	6.2%	6.52%	7.09%	7.4%

Figure 3.26: 4 Element Phased-array TX EVM measurement with DSB mode off chip RX.

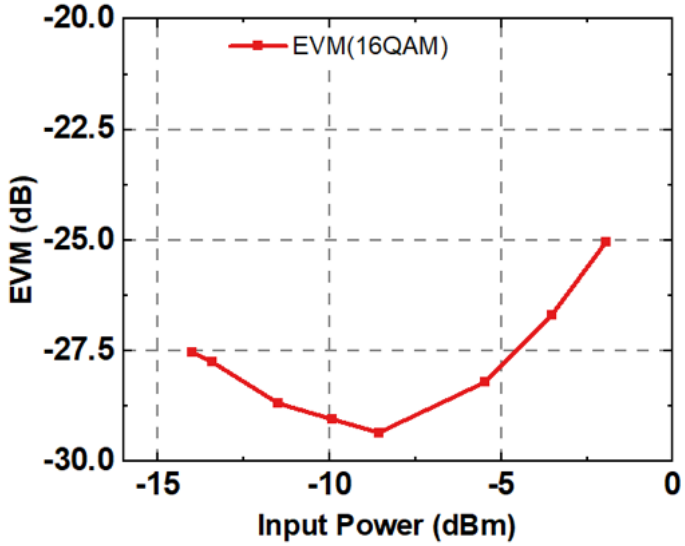


Figure 3.27: 4 Element Phased-array TX EVM bathtub plot with DSB mode off chip RX.

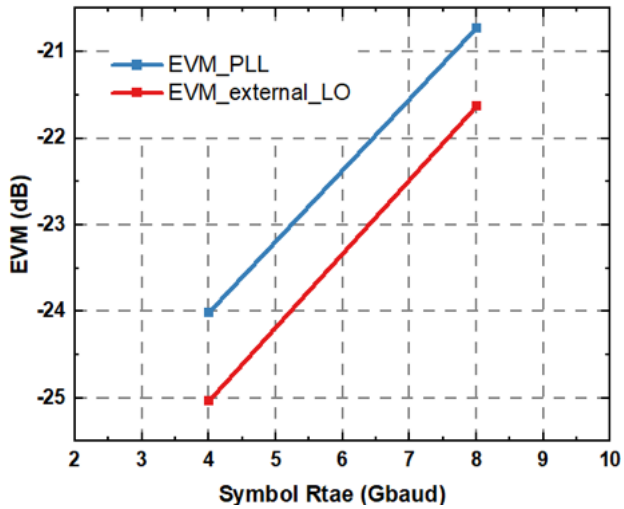


Figure 3.28: 4 Element Phased-array TX EVM using external LO source and on chip PLL with DSB mode off chip RX.

GHz. Compared with the single element TX, the EIRP of 4-element phased-array TX is boosted by 10-11 dBm over the frequency band, which is slightly lower than the theoretical value of 12dB. It is because of the antenna coupling and increased IR drop due to increased DC current.

3.4.2.2 Phased-array TX EVM Measurements with SSB mode off chip RX

Similar to the test setup in section 3.4.1.5, a Keysight AWG generates 16-QAM, 64QAM and 128-QAM waveforms to feed the TX baseband I/Q differential inputs, and the down-converted signal is demodulated by Keysight 89600 VSA with internal equalization. Fig. 3.25 shows the measured EVM results with different symbol rates in 16-QAM, 64QAM and 128-QAM operations.

3.4.2.3 Phased-array TX EVM Measurements with DSB Mode Off-Chip RX

Similar to the test setup in section 3.4.1.6, a Keysight AWG generates 16-QAM, and 64-QAM waveforms to feed the TX baseband I/Q differential inputs, and the down-converted signal is demodulated by Keysight 89600 VSA with internal equalization.Fig. 3.26 shows the measured EVM results with different symbol rates in 16-QAM, and 64QAM operations.

Fig. 3.27 shows the the measured EVM versus the input power of the 16-way power splitter (here the data rate is 16 Gb/s). When input power is low, the EVM is limited by the SNR; when the input power is high, the EVM is limited by the linearity.

We also compare the EVM results with external LO source and on chip PLL. As shown in Fig. 3.28, with external LO source, the EVM is improved by 1dB.

3.5 Conclusions

Table 3.1 summarizes the measurement results of our single channel D-band TX and compares the results to the state-of-the-art single channel D-band TXs. The packaged single channel TX achieves competitive performance with low power consumption.

Table 3.2 summarizes the measurement results of our 4-element phased-array D-band TX and compares the results to the state-of-the-art phase-array D-band TXs. The packaged phased-array TX achieves the best energy efficiency among all the phased-array D-band TXs.

Table 3.1: Performance Comparison of state-of-the-art single channel D-band transmitters.

	[3] ***SSCL'2021***	[4] ***VLSI'2021***	[1] ***ISSCC'2022***	[5] ***ISSCC'2022***	This Work
Package	No	No	Yes	No	Yes
Technology	45 nm SOI	28 nm Bulk CMOS	130 nm SiGe BiCMOS	22 nm CMOS	28nm Bulk CMOS
Antenna Integration	No	No	Yes	No	Yes
Frequency(GHz)	140-158	140-160	130-164	116-164	>132-144
EIRP at Psat(dBm) (single channel)	N/A	N/A	N/A	N/A	17.3
TX Psat(dBm)(single channel)	0.1	13	12	Unknown	13.65
TX Pdc(mW)(single channel)	420	586	265	173(Pout=0.8dBm)	141@OP1dB
TX OP1dB/Psat DC-RF Eff(%)(single channel)	-/0.24	-/3.4	-/6	0.69- % /-	6/10.6
Package Loss(dB)	N/A	N/A	unknown	N/A	1
Data Rate Modulation	8*10.56Gbps 64-QAM(channel bonding)	10Gbps 16-QAM	30Gbps/14Gbps 64-QAM/256-QAM	160Gbps 16-QAM	100Gbps/144Gbps 16QAM/64-QAM

Table 3.2: Performance Comparison of state-of-the-art phased-array D-band transmitters.

	[1] ***JSSC'2023***	[24] ***JSSC'2022***	This Work
Package	Yes	Yes	Yes
Technology	130 nm SiGe BiCMOS	45 nm SOI	28nm Bulk CMOS
Antenna Integration	Yes	Yes	Yes
Frequency(GHz)	110-170	136-147	>132-144
EIRP at Psat(dBm)	-8(4 element)	32(8 element)	27-28(4 element)
TX Pdc(mW)	2500	1850	470
Energy eff(pJ/b)	12.5	115.6	4.28
Data Rate	180Gbps/200Gbps	16Gbps	100Gbps/110Gbps
Modulation	16-QAM/32-QAM	16-QAM/64-QAM	/16QAM/64-QAM

Chapter 4

200GHz PA

4.1 Introduction

Future wireless communication is exploring sub-terahertz and terahertz spectra to achieve ultra high data throughput. 200GHz is another appealing carrier frequency since wide, contiguous bandwidths are available at this frequency. However, designing a silicon-based PA with high bandwidth and output power at 200GHz is still a challenge. Specifically, placing the carrier frequency at the boundary of where practical amplification leads to limited power gain and reduced power handling capability of the transistors.

This work presents a 200GHz multi-way power combined PA which not only achieves reliable amplification at 200GHz but also generates sufficient output power.

This chapter is organized as follows. Section 4.2 presents the architecture of the proposed power combined 200GHz PA and gain boosting techniques at sub-THz frequencies. Section 4.3 describes the circuit implementation, and section 4.4 presents the simulation results.

4.2 200GHz Multi-Way Power Combined PA Topology

4.2.1 16-Way Se(8-Way Diff)Power Combined 200GHz Power Amplifier

Fig. 4.1 shows the simplified schematic of the 16-way power combined 200GHz PA. The 16-way power combined PA utilizes 8 slotline based 2-way combiner and one zero-degree combiner to achieve high output power. The splitter is implemented using one coupled-line based splitter and four slot-line based splitters. Gain boosting amplifier cells are utilized for optimal power gain and output power.

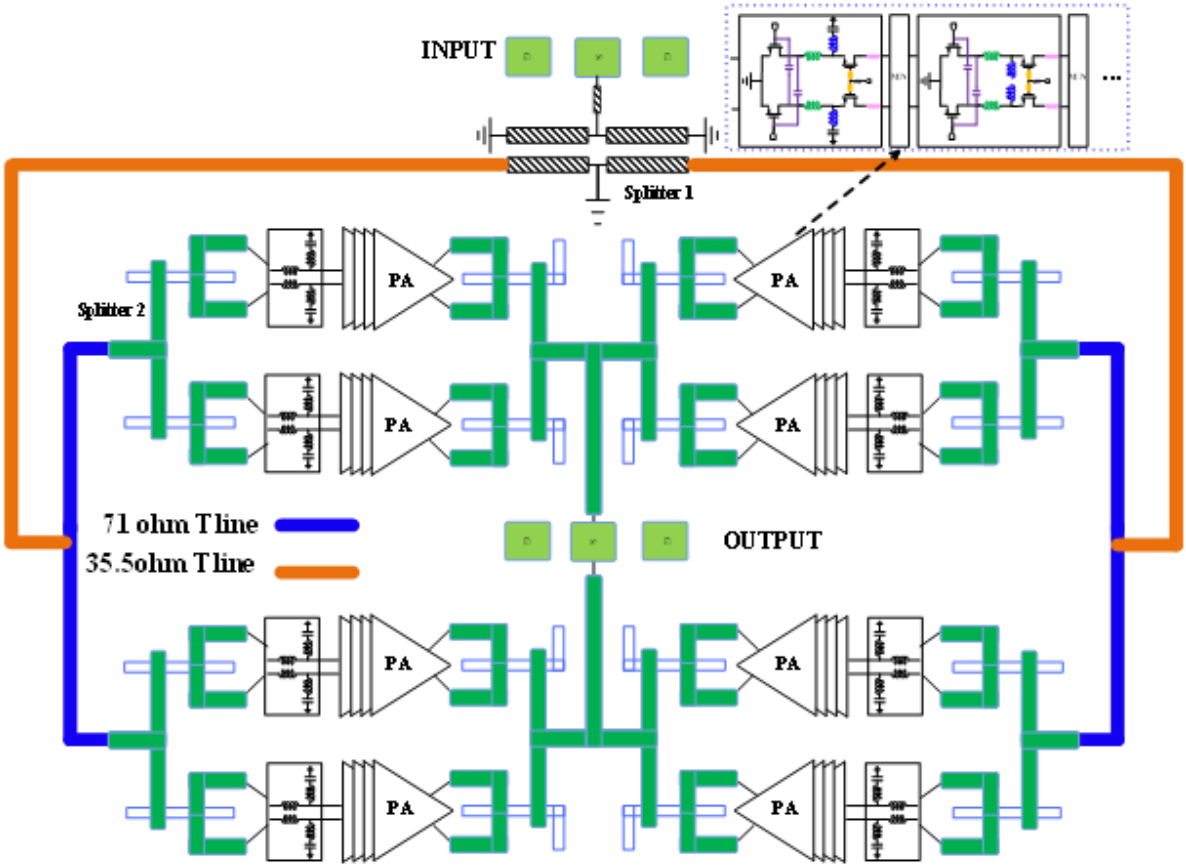


Figure 4.1: Simplified schematic of 16-way 200GHz PA.

4.2.2 Gain Maxima Definitions

In this section, we review the three important gain maxima definitions which are used to evaluate the active devices.

Maximum Available Gain (Gma)

Maximum available gain (Gma) of a two-port is defined as the ratio of the available power from the output port of the two port to the available power from the source. Gma is achieved when the source and load impedances are conjugately matched to the input and output ports of the two-port simultaneously. Gma here is the same as the "Gmax" in cadence spectre RF simulation. Simultaneous matching is possible only when the two-port is unconditionally stable [33].

Gma is only defined at the frequencies where stability factor $k > 1$. Gma of an active 2

port (A2P) can be written as a function of its parameters:

$$G_{ma} = |\frac{Y_{21}}{Y_{12}}|(K - \sqrt{K^2 - 1}) \tag{4.1}$$

HereY_{ij} is the Y parameter of the A2P, and i,j=1,2.

Unilateral Power Gain (U)

U is defined as Gma of an A2P that is unilateralized using a linear-lossless-reciprocal (LLR) embedding. U is given below as a function of the Y-parameters of the A2P.[17]

U is invariant under LLR embedding and is an invariant figure of merit of a linear two port. In other words, U is only a function of the A2P parameters and LLR embedding does not change it. U is obviously not the highest power gain that can be obtained from the active device. If the device is active ($U > 1$), the maximum power gain from the device is infinite, which is in evidence when the device is used in an oscillator circuit.[17]

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(Re[Y_{11}] \cdot Re\,[Y_{22}] - Re[Y_{12}] \cdot Re\,[Y_{21}])} = \frac{|A - 1|^2}{2K_f|A| - 2Re[A]} \tag{4.2}$$

$$A = \left|\frac{Y_{21}}{Y_{12}}\right|$$

Maximum Achievable Gain(Gmax)

Maximum achievable gain (Gmax) is the maximum Gma of an LLR embedded A2P. If we embed an A2P by a tunable LLR embedding and match the input and output of the resulting two-port, Gmax is the maximum power gain, and is given as [17]

$$G_{max} = (2U - 1) + 2\sqrt{U(U - 1)} \tag{4.3}$$

In fact, the main purpose of utilizing gain boosting techniques is to boost the Gma close to Gmax by choosing proper embedding network.

4.2.3 Gain Boosting Techniques at Sub-THz Frequencies

In this section, we discuss different gain boosting techniques used at sub-THz amplifier design. We first re-visit the the gain boosting technique with the simple embedded passive network: capacitance-based neutralization and over-neutralization techniques, and then describe another gain boosting technique with more complicated embedded passive network.

4.2.3.1 Capacitance-based Neutralization and Over-neutralization Techniques

Fig. 4.2 shows the Gma,U, Gmax and Kf of a 17.28um RF transistor versus frequency. It is worth pointing out that the Gma curve of the transistor without any neutralization corresponds to the stability factor Kf of one. For frequencies below the knee point, neutralization can help to boost the Gma and stabilize the device. After the knee point, defined as the "near fmax" region, there is only a small difference between the Gma with neutralization and U. Therefore, over-neutralization is introduced at the "near fmax" region.

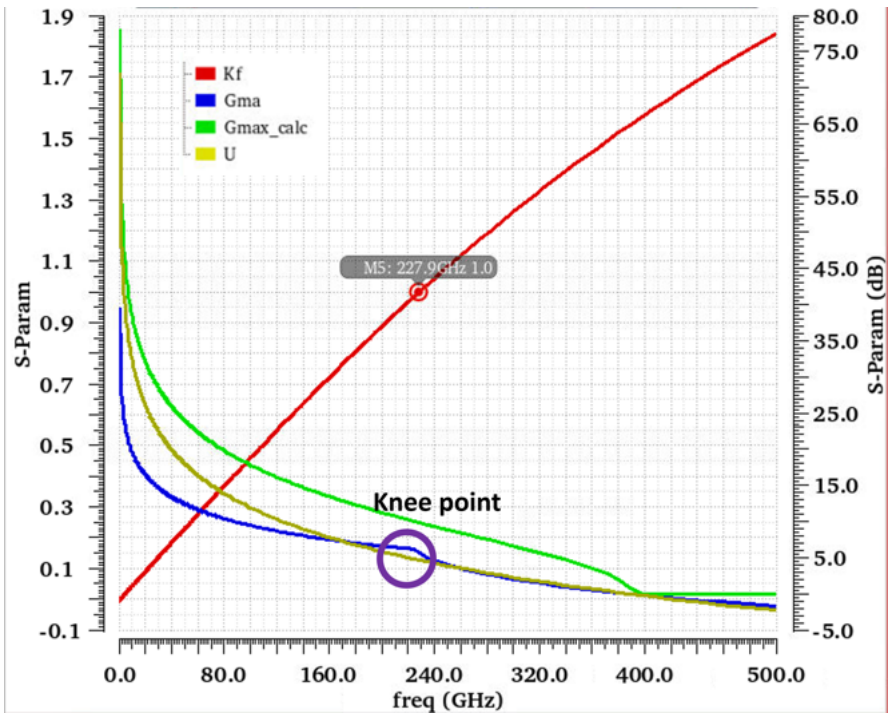


Figure 4.2: Power gains and the stability measures of a 17.28um RF transistor in Intel 22nm (pre-layout results).

When the device operates at near the fmax region, Kf of the original device without any neutralization capacitance is greater than 1, and the original device is unconditionally stable and Gma is close to that of the neutralized device. As illustrated in Fig. 4.3, at the near fmax region, significant gain boosting is achieved by adopting the over neutralization technique, compared with neutralization technique.

4.2.3.2 Gain Boosting Techniques with Higher Order Embedded Network

When the stability factor K_f is equal to 1 and the phase θ of Y_{21}/Y_{12} is 180 degree, the Gma of the device with embedding passive network will reach Gmax. However, it is difficult

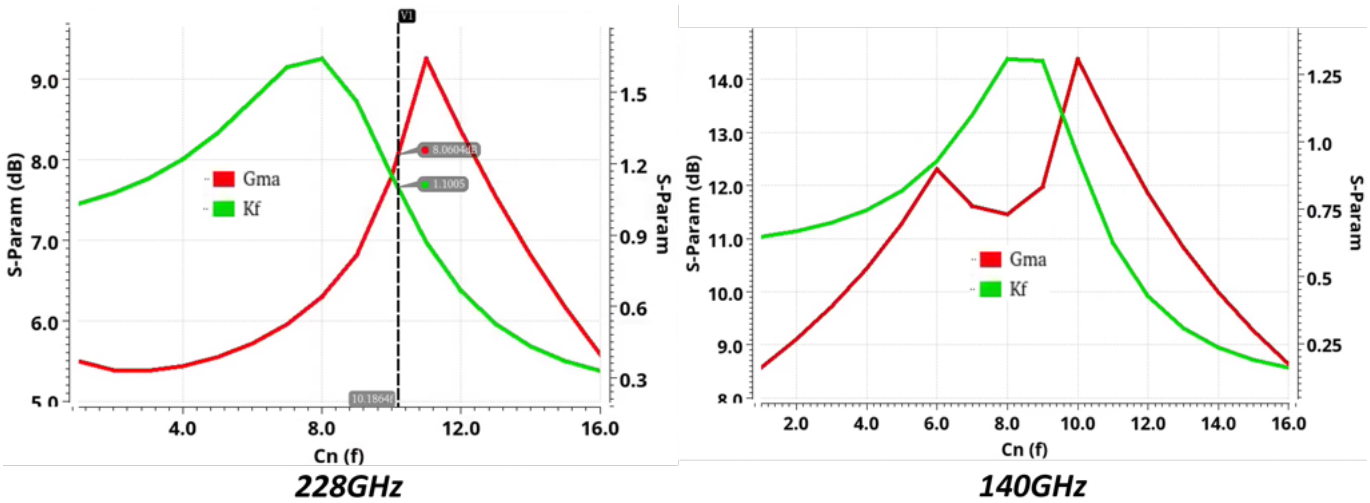


Figure 4.3: Gmax versus neutralization capacitance at 228GHz and 140GHz of a 17.28um RF transistor in Intel 22nm(pre-layout results).

to satisfy these two conditions at the same time for a wide frequency range. Therefore, a simplified gain-boosting condition is adopted[10].

Compared with the phase θ, Gma is more sensitive to Kf. Therefore, the condition Kf=1 is utilized to derive the requirement of the embedded passive network. If Kf is equal to 1, then U can be expressed as [10]

$$U = \frac{|A-1|^2}{2|A| - 2Re[A]} \tag{4.4}$$

We can re-arrange (4.4) with A = Areal + j*Aimag

$$2U\sqrt{A_{real}^2 + A_{imag}^2} - 2UA_{real} = (A_{real}-1)^2 + (A_{imag})^2 \tag{4.5}$$

With help of the symbolic solver in Matlab, Areal can be solved with respect to Aimag and U. Although there exist four solutions, only one of them is practical.

$$A_{real} = S(A_{imag}, U) \tag{4.6}$$

As shown in Fig. 4.4, the added passive elements Ygs and Yds, implemented using inductors or T-lines, can help to decrease the sensitivity of Gma over the embedded passive components values in Ygd by reducing the quality factors of both the input and output impedances. With the embedded passive network, the new transfer parameter ratio is[10]

$$A_{core} = \frac{Y_{core,21}}{Y_{core,12}} = \frac{Y_{cas,21} - Y_{gdt,21}}{Y_{cas,12} - Y_{gd,12}} \tag{4.7}$$

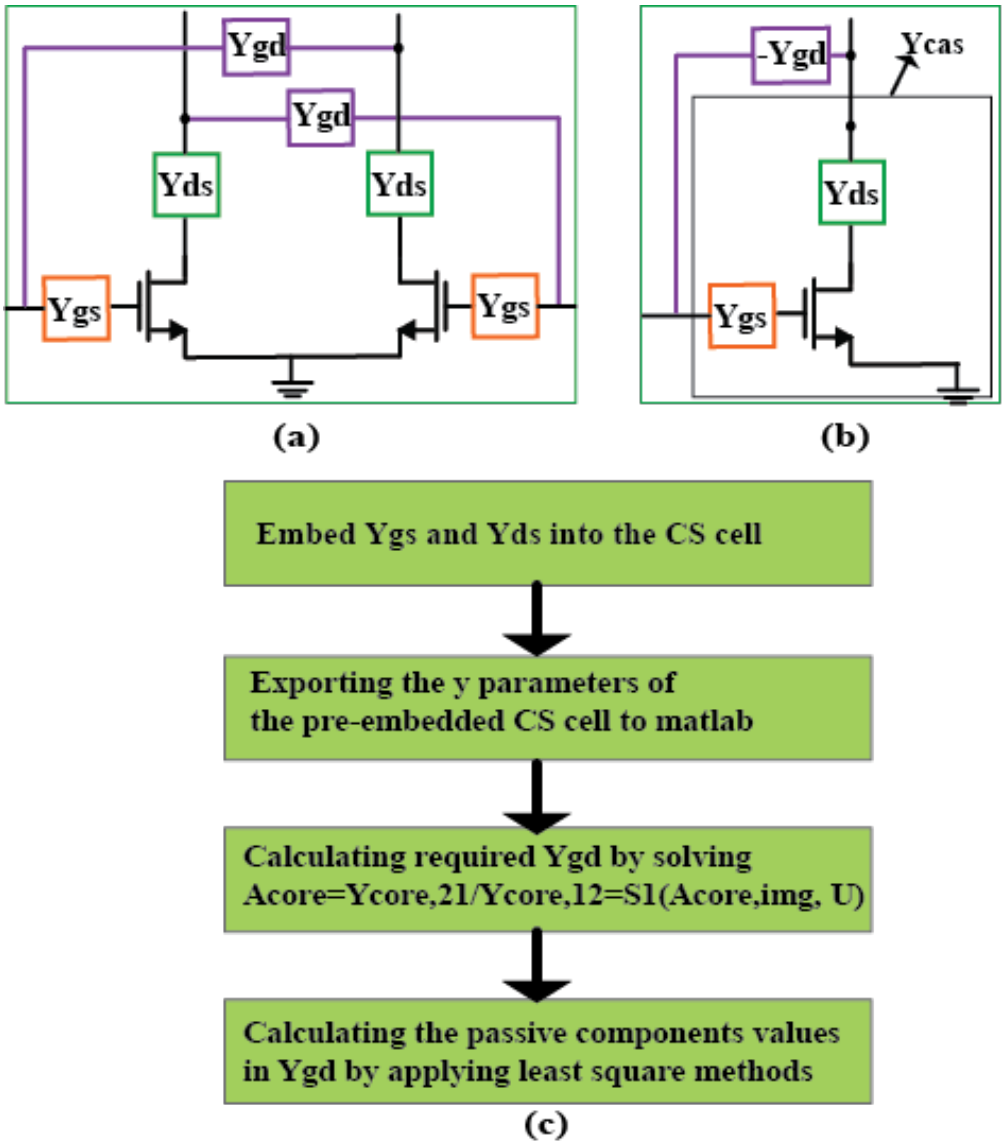


Figure 4.4: (a) Schematic of the differential pair with the embedded network. (b) Schematic of the equivalent half circuit model. (c) Flow chart of deciding the values of the passive components in the embedded network

After plugging (4.7) to (4.6), we can calculate the required $Y_{gd,12}$ and $Y_{gd,21}$ value: Ygdtar.

Since a device with a simple embedded passive network consisting of cross connected capacitors cannot satisfy (4.6) across a wide frequency range, a high-order passive network is required. An embedded network which is comprised of a T-line (TL) in series with the capacitor is introduced to increase the order of the cross-connected passives[10].

The ABCD matrix of this network can be expressed as

$$\begin{aligned}\begin{bmatrix} A & B \\ C & D \end{bmatrix} &= \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{TL} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{CC} \\ &= \begin{bmatrix} cos(\beta l) & jZ_0 sin(\beta l) \\ jsin(\beta l)/Z_0 & cos(\beta l) \end{bmatrix}_{TL} \begin{bmatrix} 1 & 1/(jwC_{cc}) \\ 0 & 1 \end{bmatrix}_{CC}\end{aligned}$$

Then we can convert the ABCD parameters to Y parameters:

$$\begin{aligned}Ygd &= \begin{bmatrix} D/B & (BC-AD)/B \\ -1/B & A/B \end{bmatrix} \\ &= \begin{bmatrix} 1/(jZ_0 tan(\beta l) + 1/(jwC_{cc})) & -jwC_{cc}/(cos(\beta l) - C_{cc}Z_0 wsin(\beta l)) \\ -jwC_{cc}/(cos(\beta l) - C_{cc}Z_0 wsin(\beta l)) & (1 + C_{cc}Z_0 wcot(\beta l)/(C_{cc}wZ_0^2 - jcot(\beta l)Z_0)) \end{bmatrix}_{CC}\end{aligned}$$

By making Y12 equal to Ygdtar at the center frequency, we can calculate the Ccc as

$$\frac{2 * Y_{gdtar} cos(\beta l)}{jw(2 * Z_0 Y_{gdtar} sin(\beta l) + 1)} \tag{4.8}$$

The optimal Z0 and l can be calculated by applying least squares methods.[10]

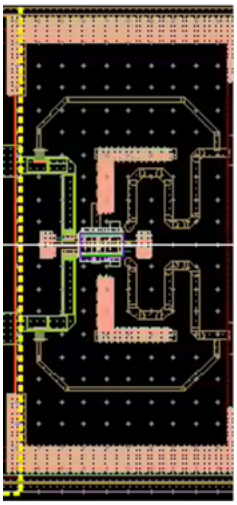
$$\min_{Z_0,l} = \sum_{f_l}^{f_h} (Y_{gdtar} - Y_{gd,12})^2 \tag{4.9}$$

Here fl and fh represent lower cutoff frequency and upper cutoff frequency, respectively.

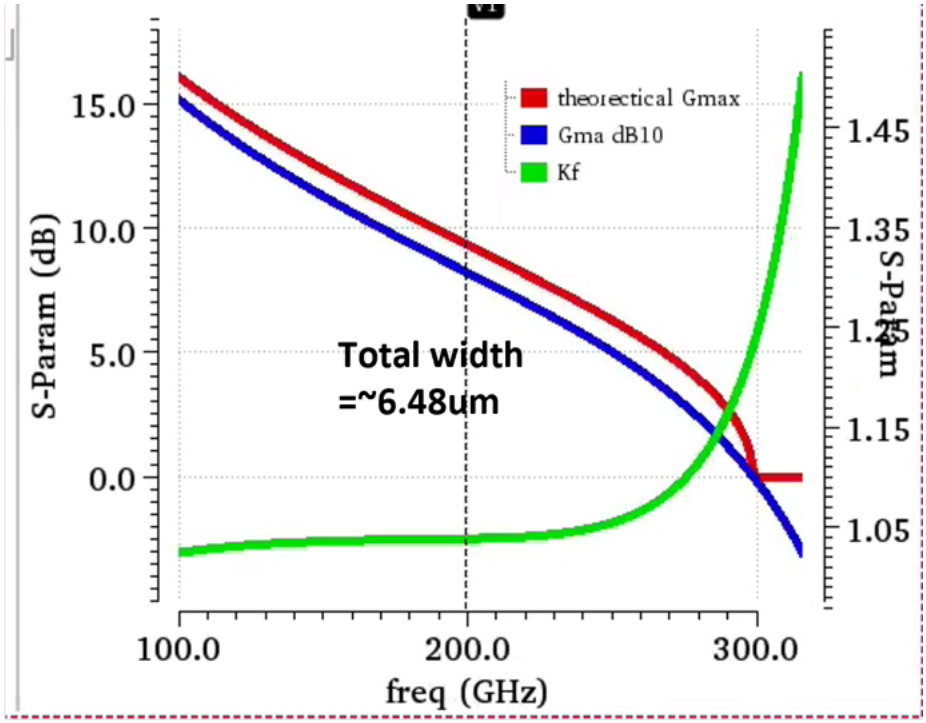
4.3 Circuit Implementation

4.3.1 Embedded Common Source Cell

The embedded common source cell is built based on the principle discussed in section 4.2.5.2. Fig. 4.5 shows the simulated Gma, Gmax and Kf versus frequency, and OP1dB with power matching, PAE at OP1dB, Gp with power matching, Gp with conjugate matching, and Psat at 200GHz. It is clear that the embedded common source cell brings enhanced power gain.



Layout of the gain boosting cell



@200GHz

OP1dB@ Power matching	PAE@ OP1dB	Gp @ Power matching	Gp @conjugate matching)	Psat
0.4dBm	10.6%	6.9dB	7.75dB	>2.8dBm

Figure 4.5: Simulated results of a embedded common source cell.

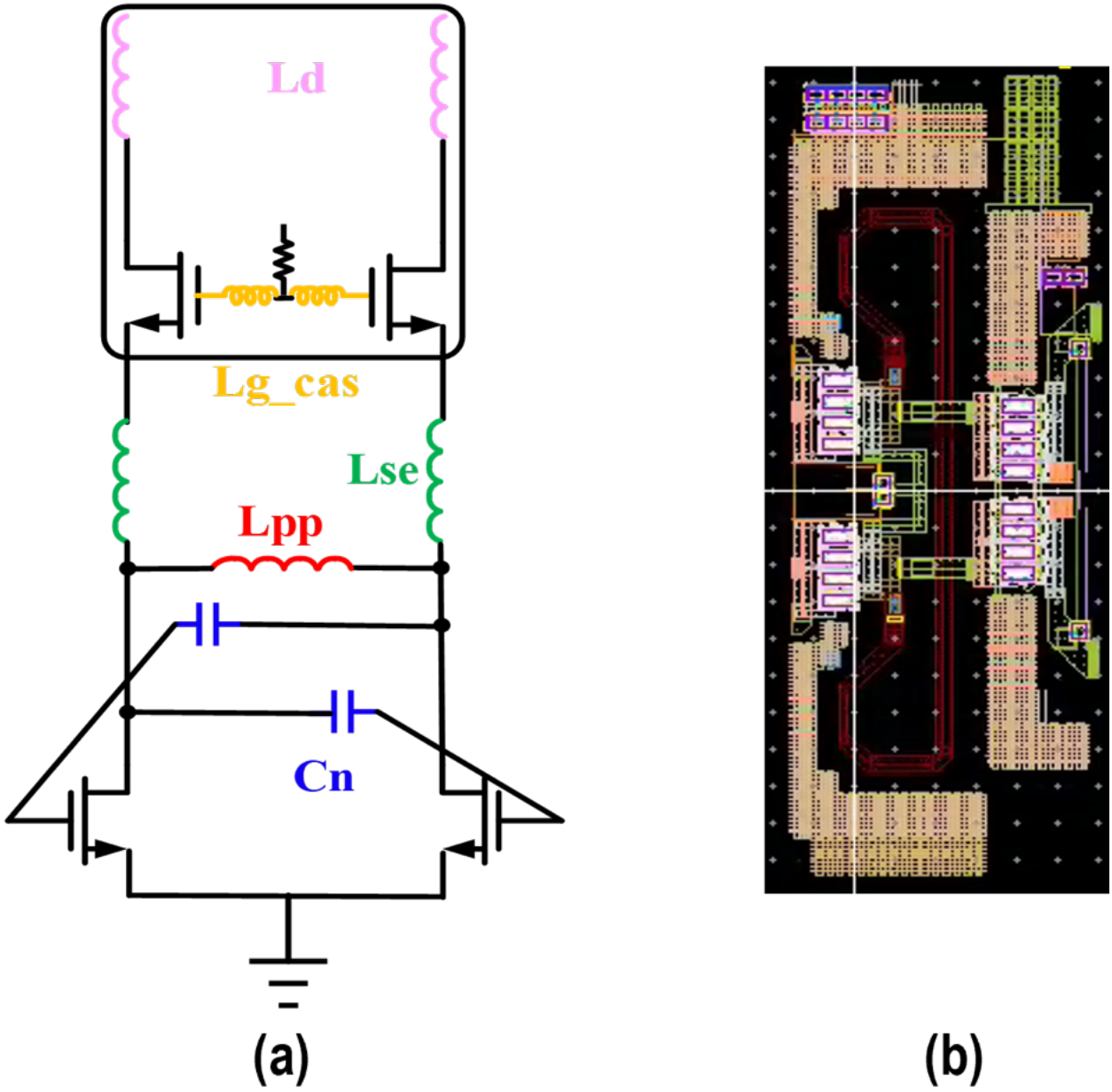


Figure 4.6: Block diagram of the 16-way power splitter.

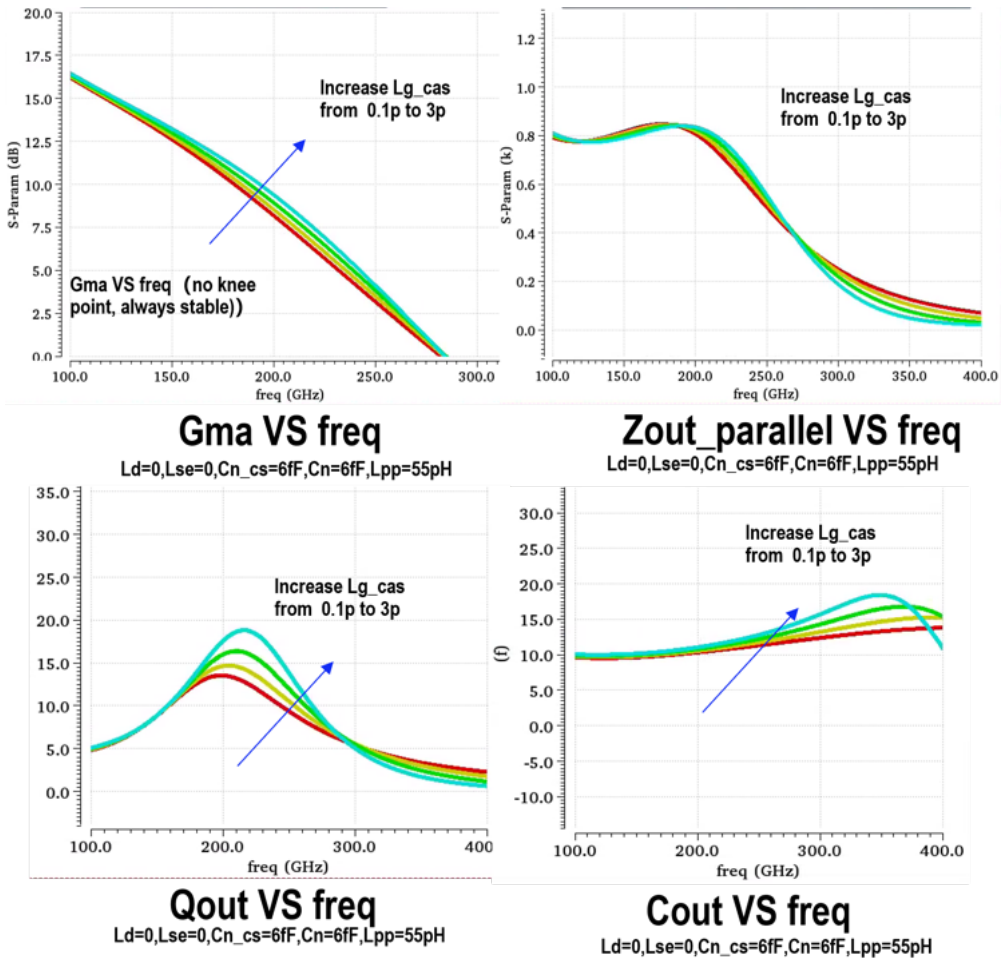


Figure 4.7: The effect of Lg_cas on Gma, Zout, Qout, and Cout.

4.3.2 Pre-embedded Cascade Cell

4.3.2.1 Gain Boosting with Lg_cas

Recent publications[18, 13] utilize this inductive gain boosting techniques by introducing an inductance at the base/gate of BJT/MOS transistor. Fig. 4.7 shows the simulated Gma, Zout_parallel, Qout and Cout for various values of Lg_cas. It is clear that Lg_cas can help to improve the Gma with a small penalty on Zout and Qout. The optimal Lg_cas value is a trade off between these specifications.

4.3.2.2 Gain boosting with Cn

As shown in Fig.4.8 ,increasing Cn can help to increase Gma but it has a relatively big impact on the Zout_parallel, Qout and OP1dB. The feedback network due to the introduction of

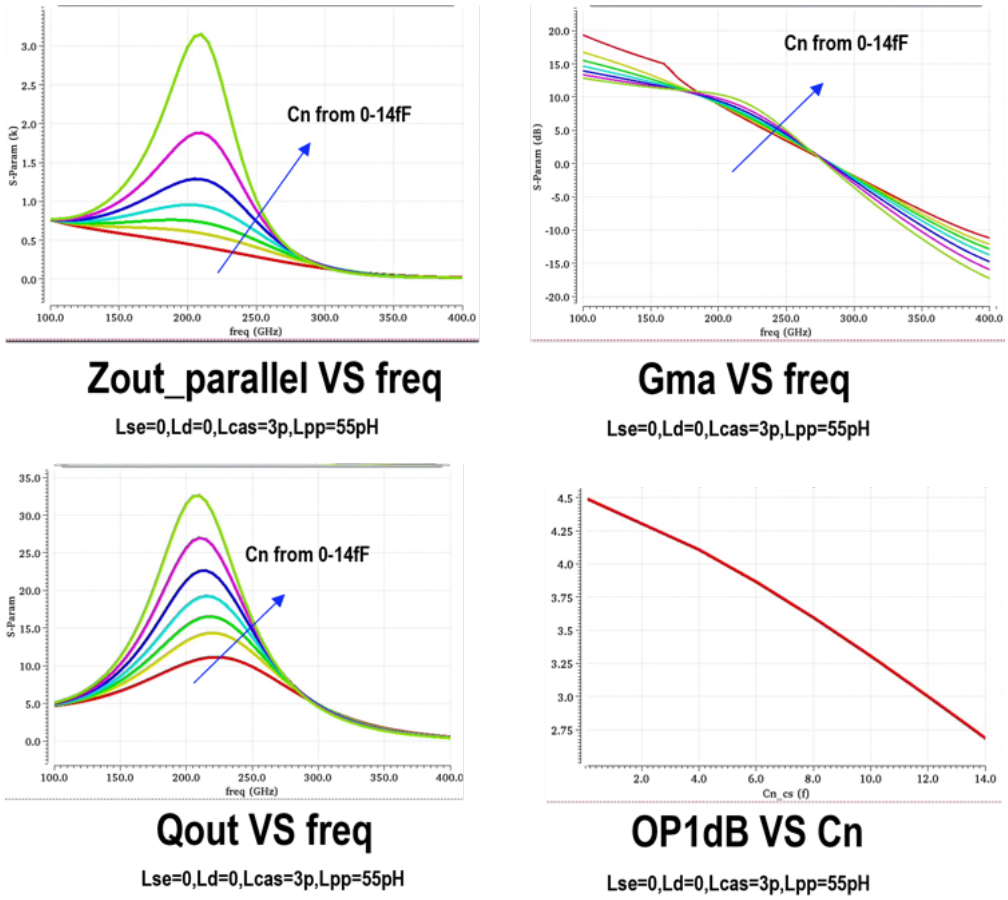


Figure 4.8: The effect of Cn on Zout, Gma, Qout, and OP1dB.

Cn directly influences the impedance seen by the amplifier cell, and thus the power delivery capability is affected.

4.3.2.3 Gain Boosting with Lpp

As shown in Fig. 4.9, LPP with a proper value can boost Gma. Lpp can help to resonate out the parasitic capacitance, however, it will also degenerate M2, resulting higher output impedance and thus reduced output power. Since Lpp has limited Q, when Lpp is small, we can sometimes see that lower output impedance with the insertion of Lpp.

4.3.2.4 Gain Boosting with Lse

The series inductor Lse, combined with the capacitance at the source node of M2 and the capacitance at the drain node of M1, forms a high order low pass filter with expanded

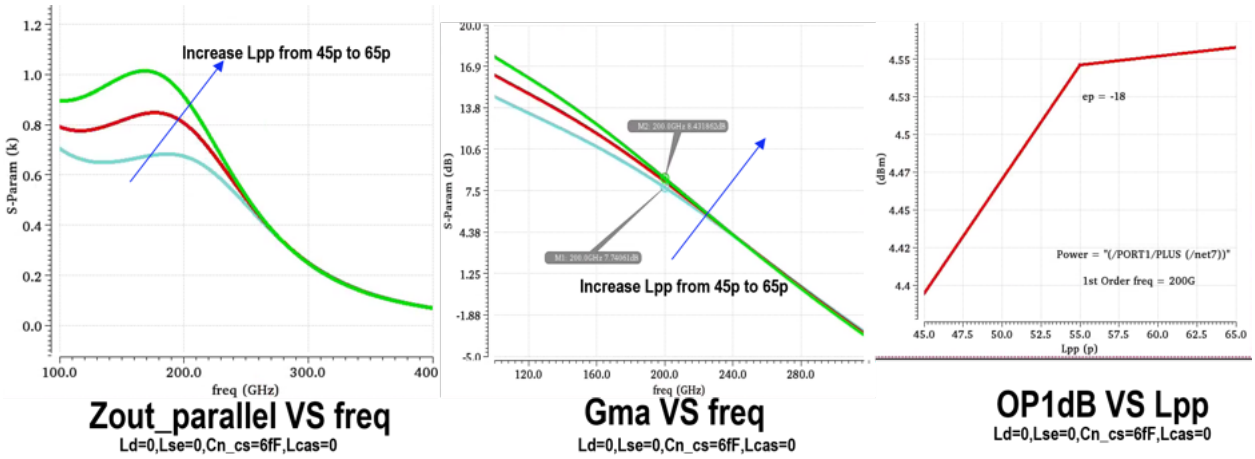


Figure 4.9: The effect of Lpp on Zout, Gma, and OP1dB.

bandwidth. Fig. 4.10 shows that Lse can help to boost Gma with a small penalty of higher Qout.

4.3.2.5 Gain Boosting with Ld

One disadvantage of employing a cascode cell in finfet technology is the quality factor Qout for output impedance is relatively high, resulting in higher insertion loss when a passive matching network is included. One solution is to introduce a small desensitization inductor at the drain terminal. As shown in Fig. 4.11, Ld can help to reduce both the Zout and Qout with a very small penalty on Gma.

4.3.2.6 Simulation Results of the Pre-Embedded Cascode Cell

Different pre-driver and output stages will require different combinations of these passive elements, since pre-driver stage prefer higher power gain while output stage prefer higher power delivery capability. Fig. 4.12 shows the simulated Gma and Kf versus frequency, and OP1dB at power matching, PAE at OP1dB, Gp with power matching, Gp with conjugate matching and Psat at 200GHz. Depending on the specific requirements of the amplifier cells, the proper combination of the passive elements resulting preferable Gma and power handling capability can be chosen.

4.3.3 Power Splitters and Combiners

4.3.3.1 16-way power splitter

As shown in Fig. 4.13, the 16-way power splitter is implemented using one coupled line (CL) based splitter and four slotline (SL) based splitter. The topologies of the selected splitters

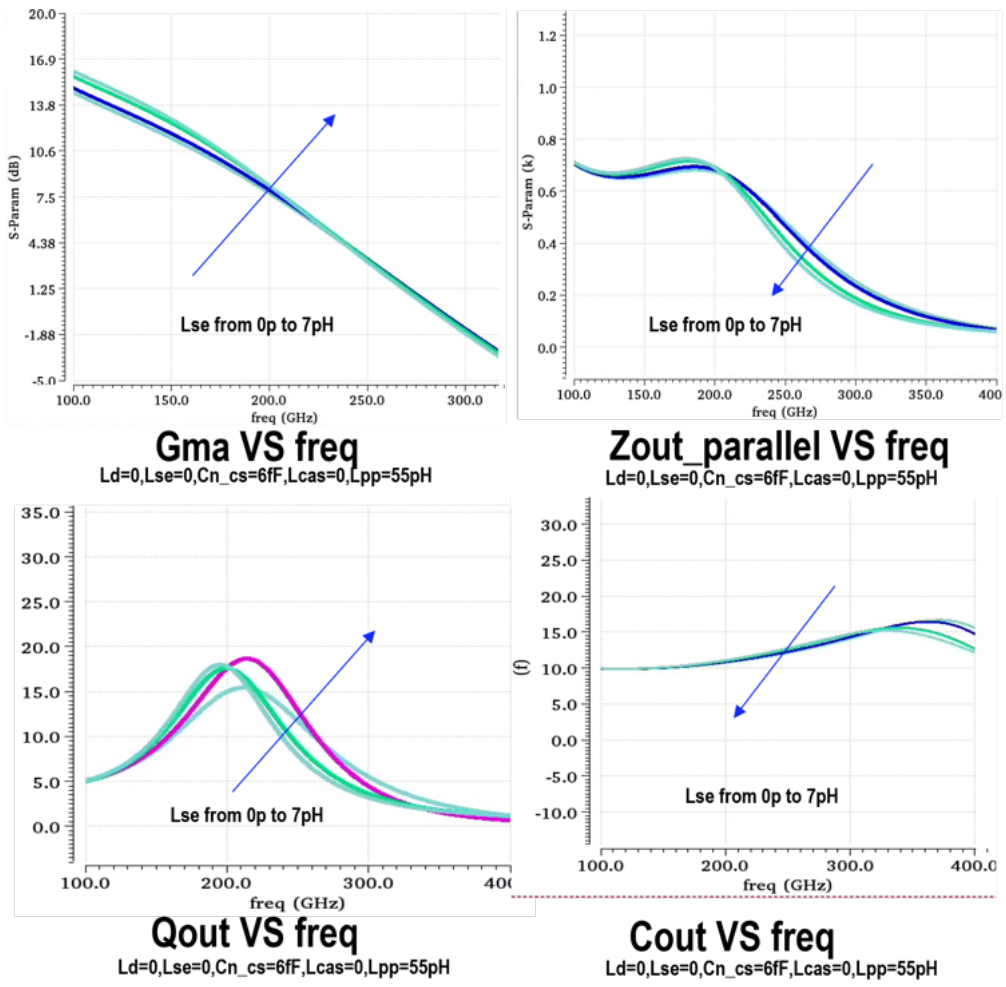


Figure 4.10: The effect of Lse on Zout,Gma, and OP1dB.

provides more freedom in impedance transformation, enabling simultaneous wide bandwidth and low loss. The input of the SL splitter (splitter 2) is broadband matched to 71 ohm, and Fig. 4.14 shows the simulated input impedance of splitter 2.

4.3.3.2 16-way power combiner

As mentioned before, a low loss power combiner should be leveraged to enhance the output power. As is shown in Fig 4.15, the proposed combiner consists of 8 slot baluns and one zero degree combiner. The co-simulation with PA shows that the impedances looking into the 16 different nodes are very uniform, and the loss of the slot balun and zero degree combiner at 200GHz is -1.2dB and -0.655dB, respectively.

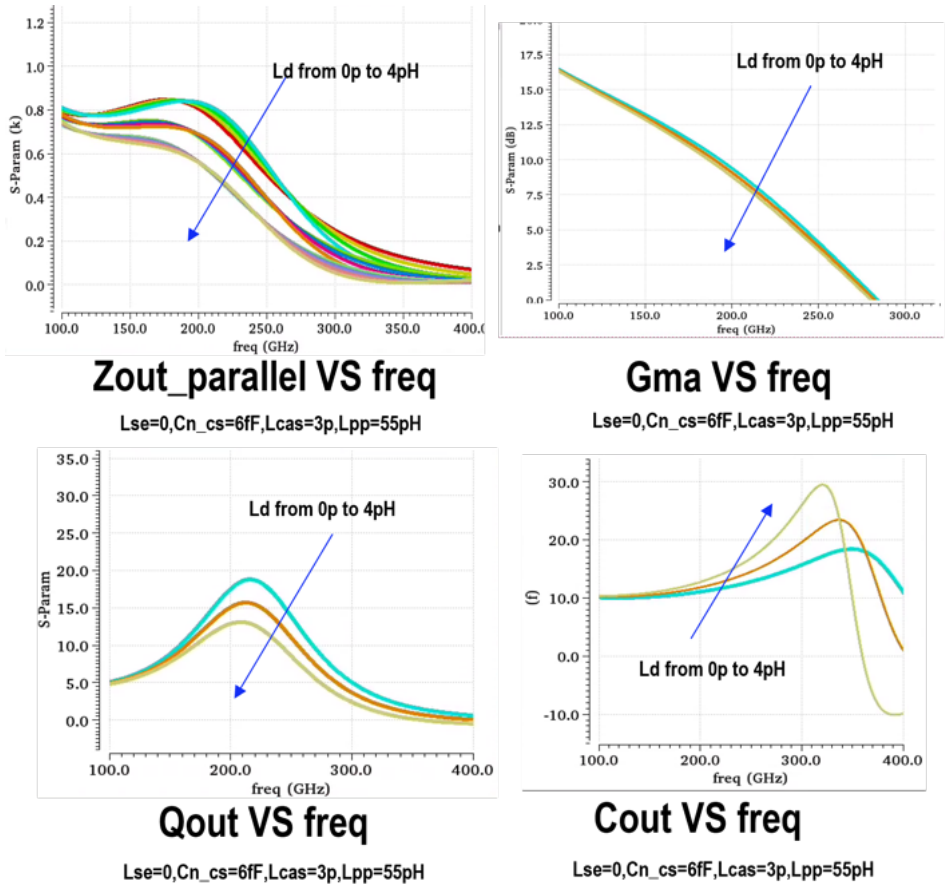
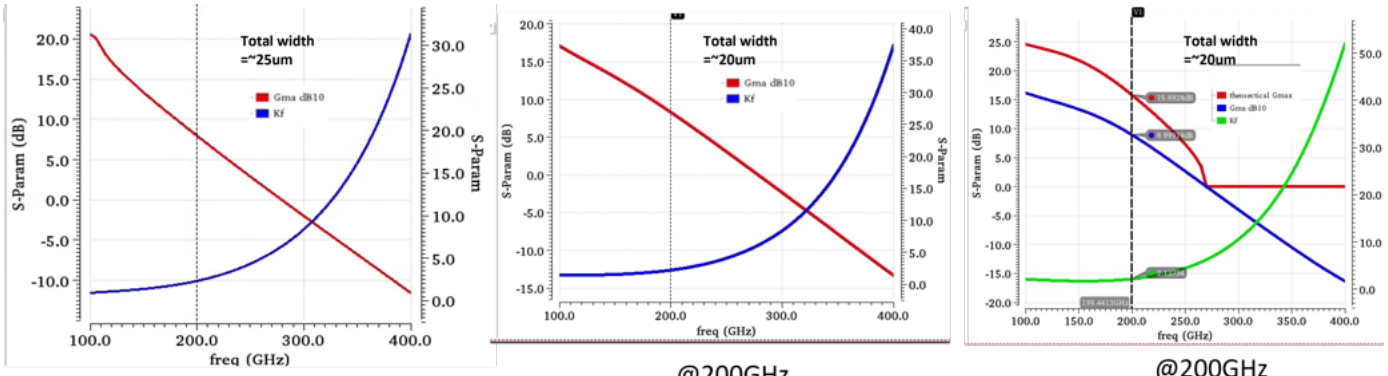


Figure 4.11: The effect of Ld on Zout,Gma, Qout and Cout.

4.4 Simulation Results

4.4.1 Simulation Results of the 16-way Power Combined 200GHz PA

As shown in Fig. 4.16, the simulated S21 is higher than 16dB at 200 GHz, and it achieves higher than 25% fractional bandwidth. The simulation results show that the 200GHz PA achieves around 13dBm OP1dB and around 17dBm Psat at 200GHz. The PAE at OP1dB and peak PAE are 1.48 % and 3.44 %, respectively.



@200GHz

OP1dB@ Power matching	PAE@ OP1dB	Gp @ Power matching	Gp @conjugate matching)	Psat
7.79dBm	8.6%	7.18dB	7.97dB	>10dBm

@200GHz

OP1dB@ Power matching	PAE@ OP1dB	Gp @ Power matching	Gp @conjugate matching)	Psat
6.33dBm	7.85%	7.44dB	8.31dB	>9dBm

@200GHz

OP1dB@ Power matching	PAE@ OP1dB	Gp @ Power matching	Gp @conjugate matching)	Psat
5.6dBm	6.9%	7.78dB	8.99dB	>8.7dBm

Figure 4.12: Simulation results of the pre-embedded cascode cell.

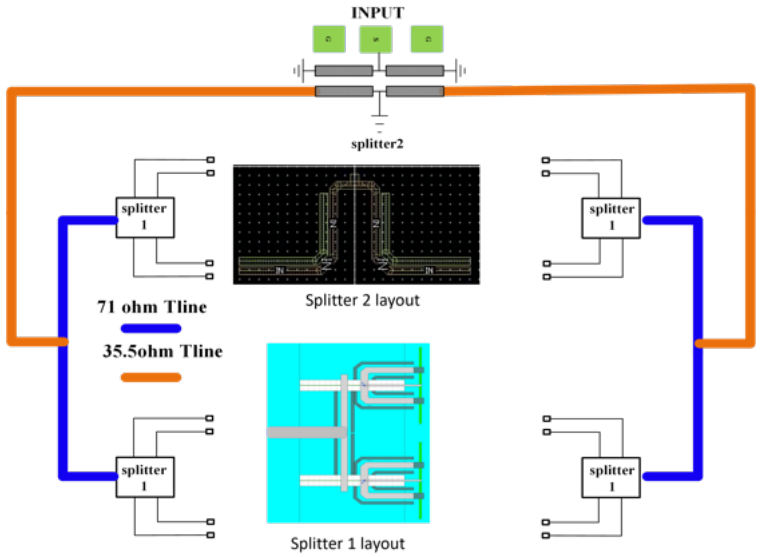


Figure 4.13: Block diagram of the 16-way power splitter

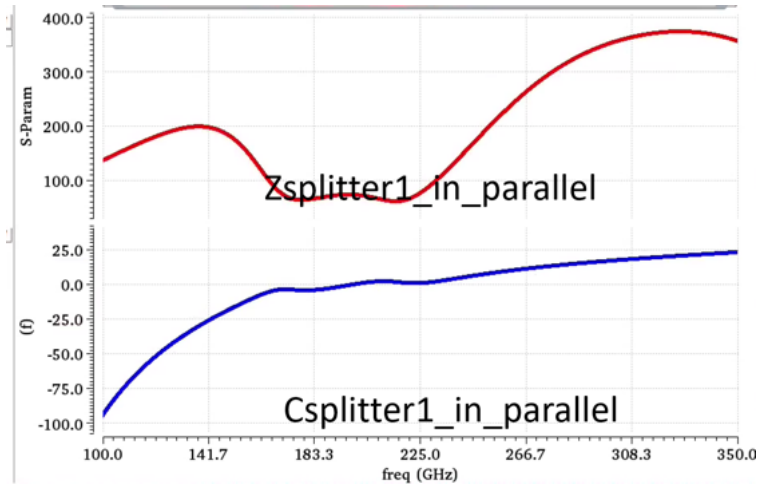


Figure 4.14: Simulated input impedance of splitter 2

4.4.2 Simulation Results of the 4-way SE (2-way Differential) Power Combined 200GHz PA

In this section, we show the simulation results of two different options: one option is a four-stage PA on each way, all the driver stages and output stages are using pre-embedded cascode cells; the other option is also a four-stage PA, the driver stage far away from the output stage is utilizing the embedded CS cell, the remaining driver stages and the output stage are employing the pre-embedded cascode cell. The second option shows higher simulated power efficiency than that of the first one.

As shown in Fig. 4.17, regarding option 1, at 200GHz, the simulated OP1dB and Psat are 7.75dBm and 11.9 dBm, respectively. The simulated PAE at OP1dB is 1.72 %, and the peak PAE is 4.05 %. Its Gp is 11.8 dB when Pout is equal to 11.9dBm. In addition, the simulation results show that the 4-way combined PA achieves 25 % fractional BW, and its S21 at 200GHz is 18.2 dB. In terms of option 2, at 200GHz, the simulated OP1dB and Psat are 7.72dBm and 11.6 dBm, respectively. The simulated PAE at OP1dB is 1.85 %, and the peak PAE is 4.33 %. The gain Gp is 11.6dB when Pout is equal to 11.6dBm. Moreover, the simulation results show that the 4-way combined PA achieves 21 % fractional BW, and its S21 at 200GHz is 17.2 dB.

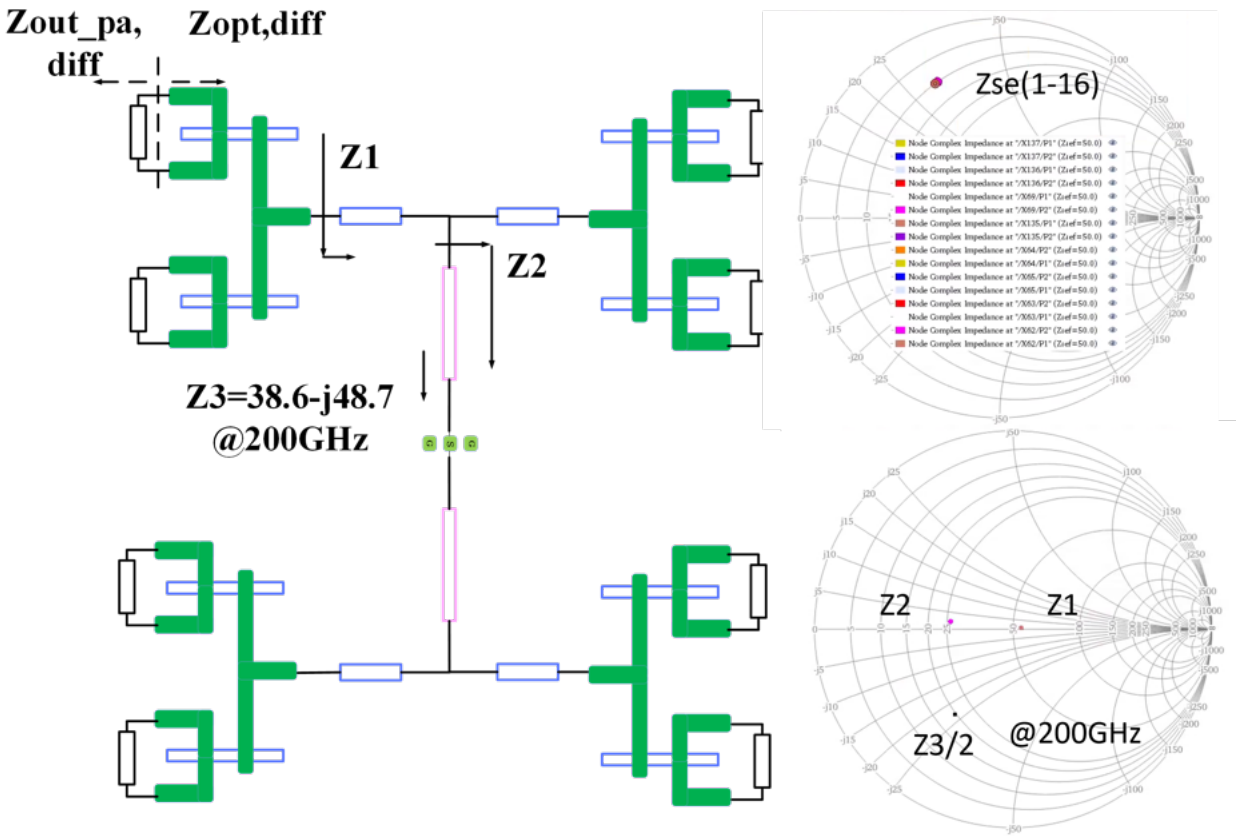


Figure 4.15: (a) Block diagram of the 16-way power combiner. (b) Impedance transformation trajectory on the Smith Chart. (c) The impedance looking into the 16 different nodes on the Smith Chart.

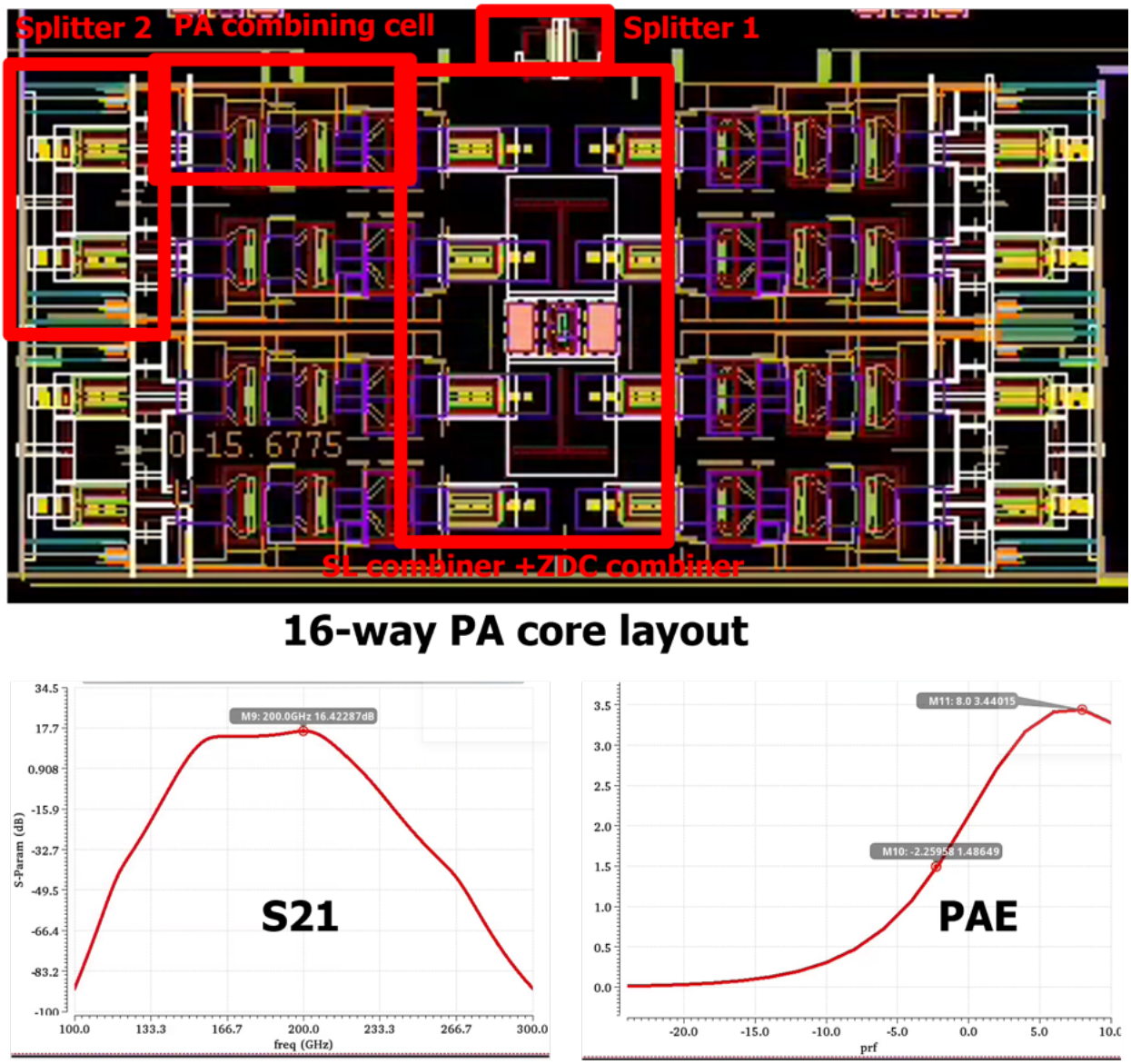


Figure 4.16: Layout and simulation results of the 16-way power combined 200GHz PA.

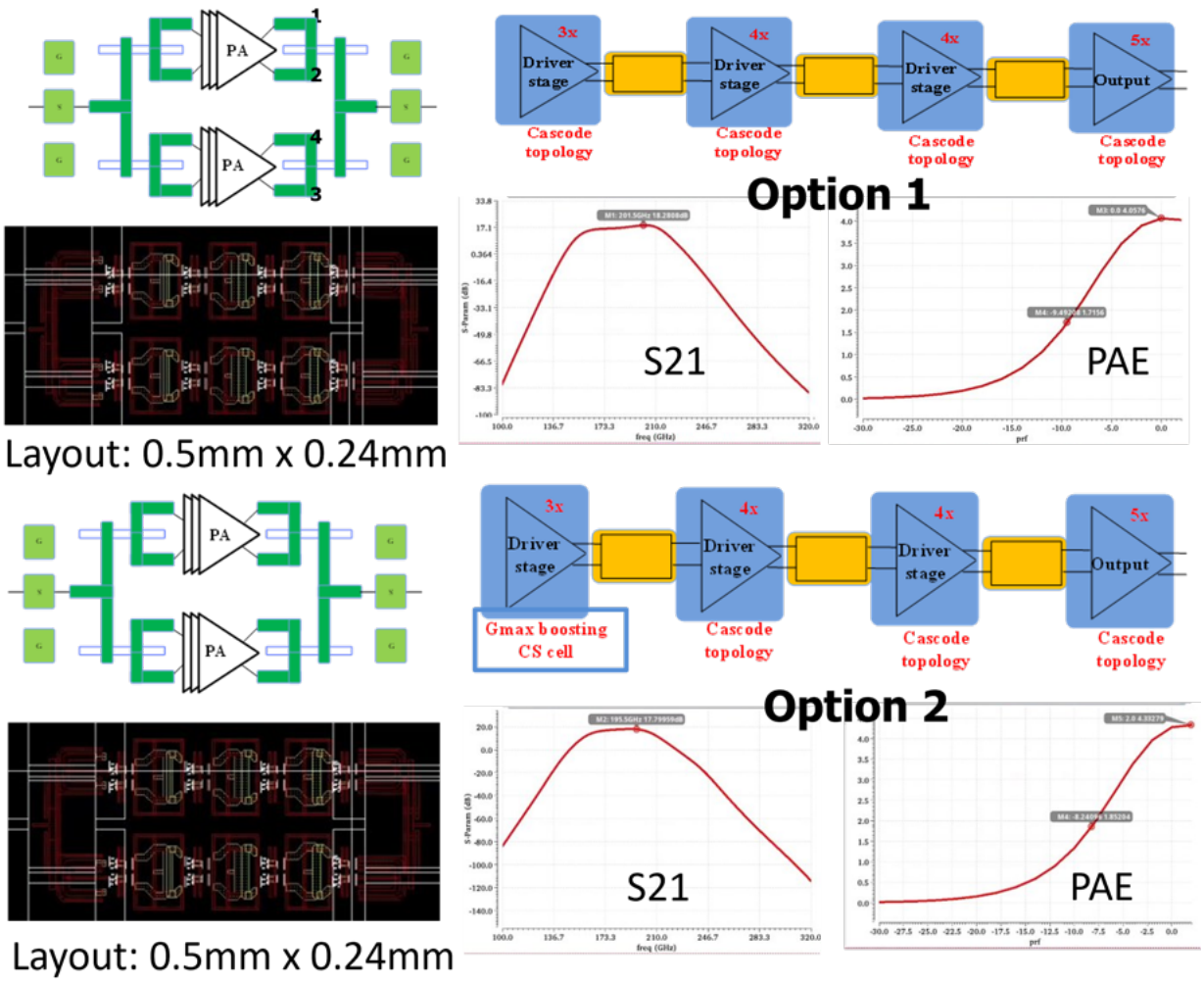


Figure 4.17: 4-way power combined PA.

Chapter 5

200GHz Digital Transmitter(DTX)

5.1 Introduction

The high power consumption of 200GHz transmitters utilizing traditional direct up-conversion analog architecture will reduce the efficiency of the whole system. Harmonic oscillator array based 200GHz transmitters can improve the efficiency to some extent, however, the data rate it can support is usually very low.

This chapter presents the design of an oscillator Array Assisted Digital IQ Sharing 200GHz TX, which achieves both enhanced efficiency and higher data rate. The overall DTX architecture is presented in section 5.2, while section 5.3 and 5.4 describe the circuit implementation of LO generation and data path, respectively. Section 5.4 presents the simulation results.

5.2 200GHz DTX Architecture

5.2.1 Overview

Most 200GHz transmitters utilize one of four general architectures illustrated in Fig. 5.1: a) Direct Up-conversion Analog TX Architecture, b) Heterodyne Analog TX Architectures, c) Traditional Digital Cartesian TX Architectures and d) Harmonic Oscillator Array Based TX Architectures. Among these TX architectures, a) and b) can support complicated modulation schemes such as 16QAM, 64QAM and 128QAM. c) can also be employed in M-QAM transmitters, however, the resolution of RF-DAC will limit its capability in supporting higher-order modulation schemes. For example, with a 2 bits RFDAC, c) can only support 16QAM and QPSK.

Direct Up-conversion Analog TX Architecture

As shown in Fig. 5.1, a direct up-conversion architecture eliminates the need for IF stages. The I/Q quadrature modulator takes the baseband signal and up-converts it to the desired

RF frequency. This eliminates the need for IF components such as filters, amplifiers, mixers and LOs. This architecture can support complex modulation schemes, however, it will usually require linear power amplifier.

Heterodyne Analog TX Architecture

The heterodyne architecture involves two steps of mixing, and thus two mixer stages and two intermediate frequencies (IFs) are employed. This approach requires many local oscillators (LOs), filters and amplifiers in the IF stages, which is expensive and power hungry.

Traditional Digital Cartesian TX Architecture

In traditional analog Cartesian transmitters, the replica of the digital signal is filtered by a reconstruction filter. In digital Cartesian transmitters, the direct Digital-to-RF Converter functions as a DAC featuring an inner Sinc filtering characteristic H(f). Therefore, by increasing the sampling rate of digital filtering blocks (FIR or IIR), we can acquire a spectrum which can satisfy the specification. Compared with digital polar transmitter, it does not require a Cordic block and does not suffer from PM bandwidth expansion.

$$H(f) = 20log(\frac{sin(\pi \frac{f}{f_{sample}})}{\frac{f}{f_{sample}}}) \tag{5.1}$$

Harmonic Oscillator Array Based OOK/ASK TX Architecture

Since the power efficiency of a linear power amplifier at 200+ GHz is extremely low, recent publications[5] have demonstrated oscillator array based 200+ GHz Transmitter with enhanced efficiency. However, these transmitters can only support relatively simple modulation schemes like OOK and BPSK, and thus limit the maximum data rate they can achieve.

5.2.2 Proposed Oscillator Array Assisted Digital IQ Sharing 200GHz TX Architecture

Introduction of the Proposed Digital IQ Sharing TX Architecture

The architecture of the proposed oscillator Array Assisted Digital IQ Sharing 200GHz TX is shown in Fig. 5.2. The TX consists of a low phase noise sub-sampling PLL with a 1 x 3 harmonic oscillator array, and three identical phase modulation paths. The phase modulation path also includes a saturation amplifier chain which utilizes amplifiers in saturation region with enhanced power efficiency.

Basics of Digital IQ Sharing TX Architecture

In traditional digital Cartesian transmitters, when we acquire the output power by combining the signals of I PA path and Q PA path, it will result in 3dB output power loss and degraded

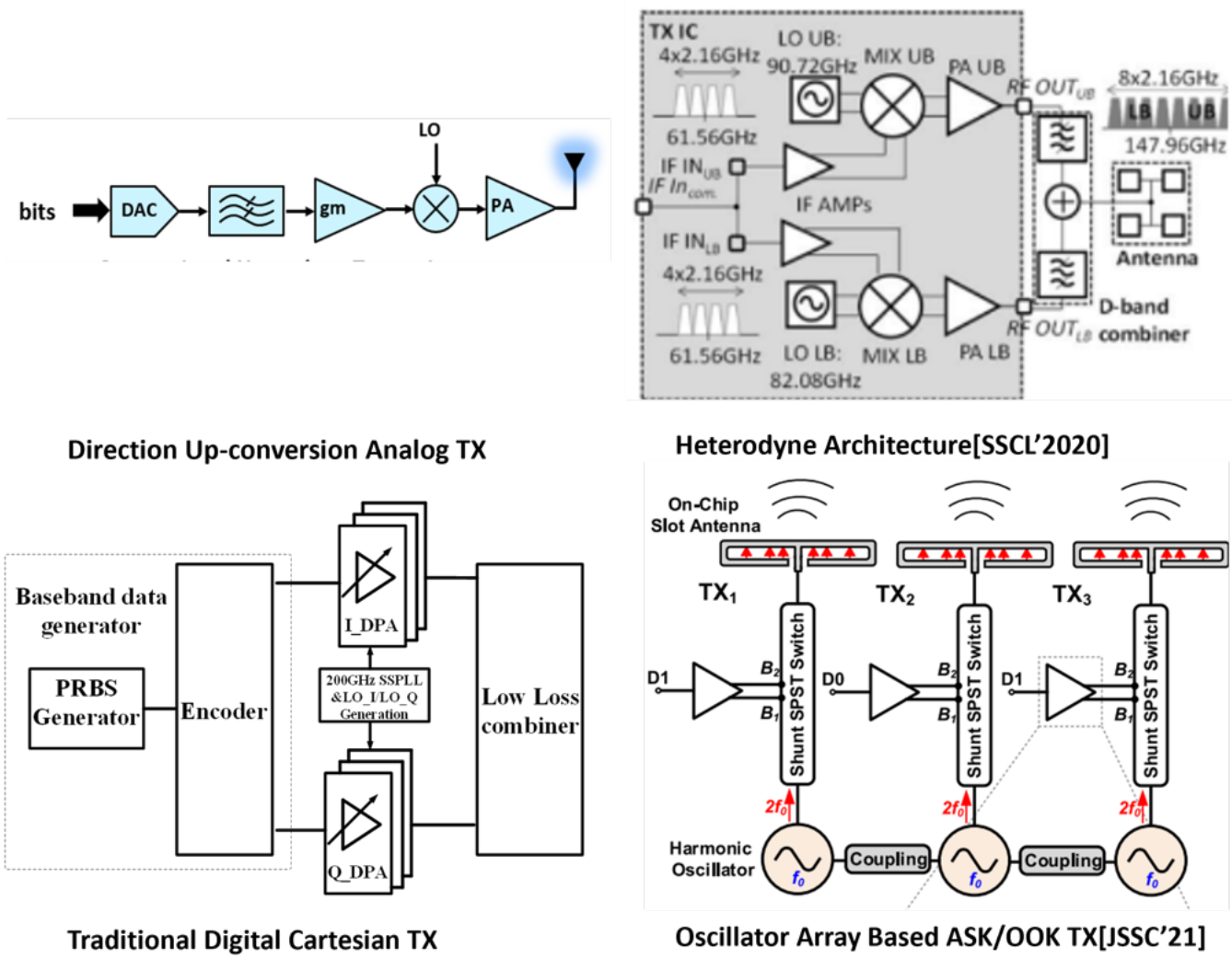


Figure 5.1: Different transmitter architectures.

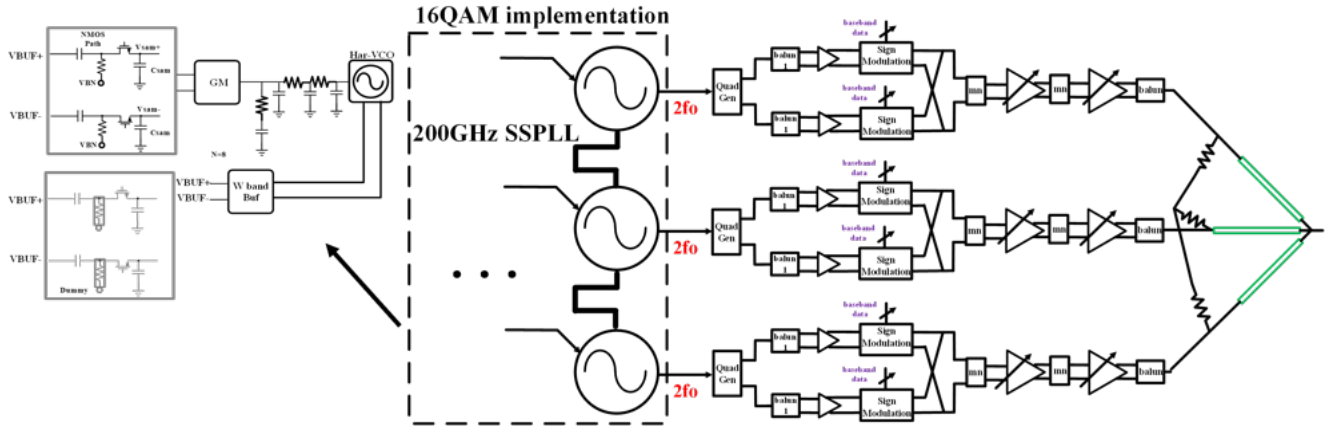


Figure 5.2: Architecture of the proposed DTX.

power efficiency (if the amplitude of I PA is equal to that of Q PA) due to the 90 phase difference. In order to address the issue of the 3dB loss, an I/Q power-cell sharing method is proposed through a different method of I and Q combining as well as a new digital baseband signal mapping. Fig. 5.3 shows the concept of the proposed IQ sharing method. When I[i] =1, Q[i] =1, the signal fed into DPA is LO_IP; when I[i] =0, Q[i] =0, the signal fed into DPA is LO_IN; when I[i] =0, Q[i] =1, the signal fed into DPA is LO_QP; when I[i] =1, Q[i] =0, the signal fed into DPA is LO_QN. Therefore, in the proposed IQ sharing DTX, the output signal can be obtained by combining appropriate numbers of vectors xn, yn, xp, yp, and thereby the 3dB loss can be avoided. while in traditional Cartesian transmitters, the output signals can be obtained by combining the vectors in, ip, jn, and jp. When I[i] =1, Q[i] =1, the signal fed into I-DPA is LO_IP and the signal fed into Q-DPA is LO_QP; when I[i] =0, Q[i] =1, the signal fed into I-DPA is LO_IN and the signal fed into Q-DPA is LO_QP; when I[i] =0, Q[i] =0, the signal fed into I-DPA is LO_IN and the signal fed into Q-DPA is LO_QN; when I[i] =1, Q[i] =0, the signal fed into I-DPA is LO_IP and the signal fed into Q-DPA is LO_QN. For example, in the proposed TX, point A is achieved by summing 32 vector xn. While in traditional Cartesian TX, A is acheived by combining 32 vector in and 32 vector jn together, resulting in 3dB loss.

Fig. 5.4 shows the conceptual diagram of the oscillator array assisted digital IQ Sharing TX. Regarding the TX supporting the 2 ˆ N QAM, it consists of a 1 x N-1 harmonic oscillator array, and three phase modulation paths. As shown in Fig. 5.4, take B in the 64QAM constellation diagram for example, after the IQ sharing process, we can obtain the output from each phase modulation path, and then sum them together through the combiner.

To verify the function of the IQ sharing DTX, a simulation model consisting of verilog-A modules is built. Fig.5.5 shows the demodulated results using a 16QAM 80Gb/s signal.

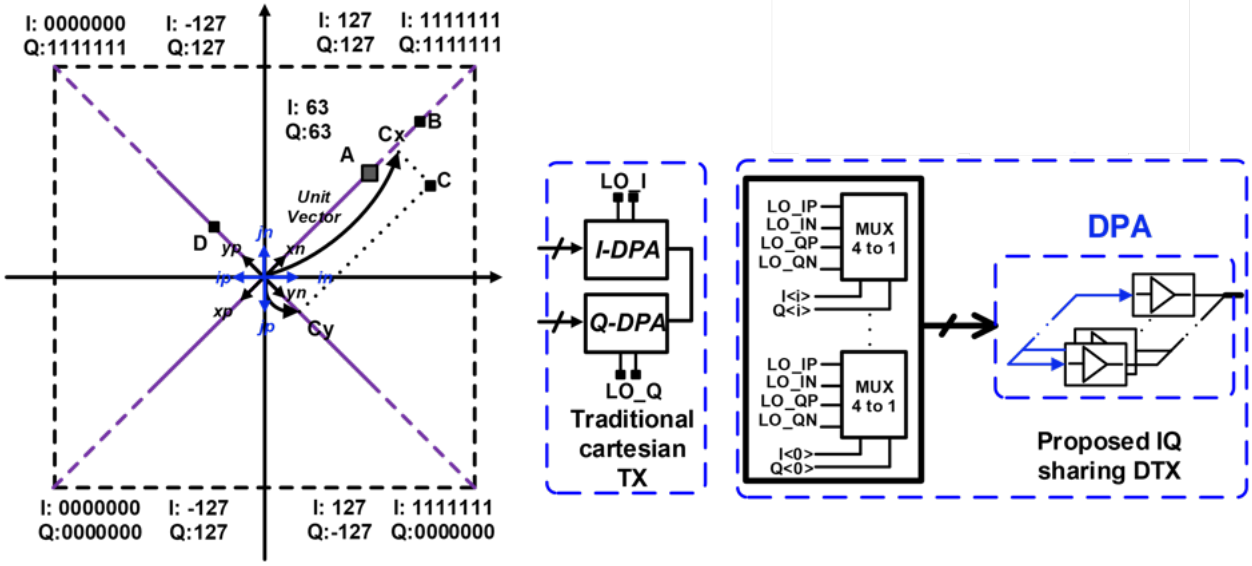


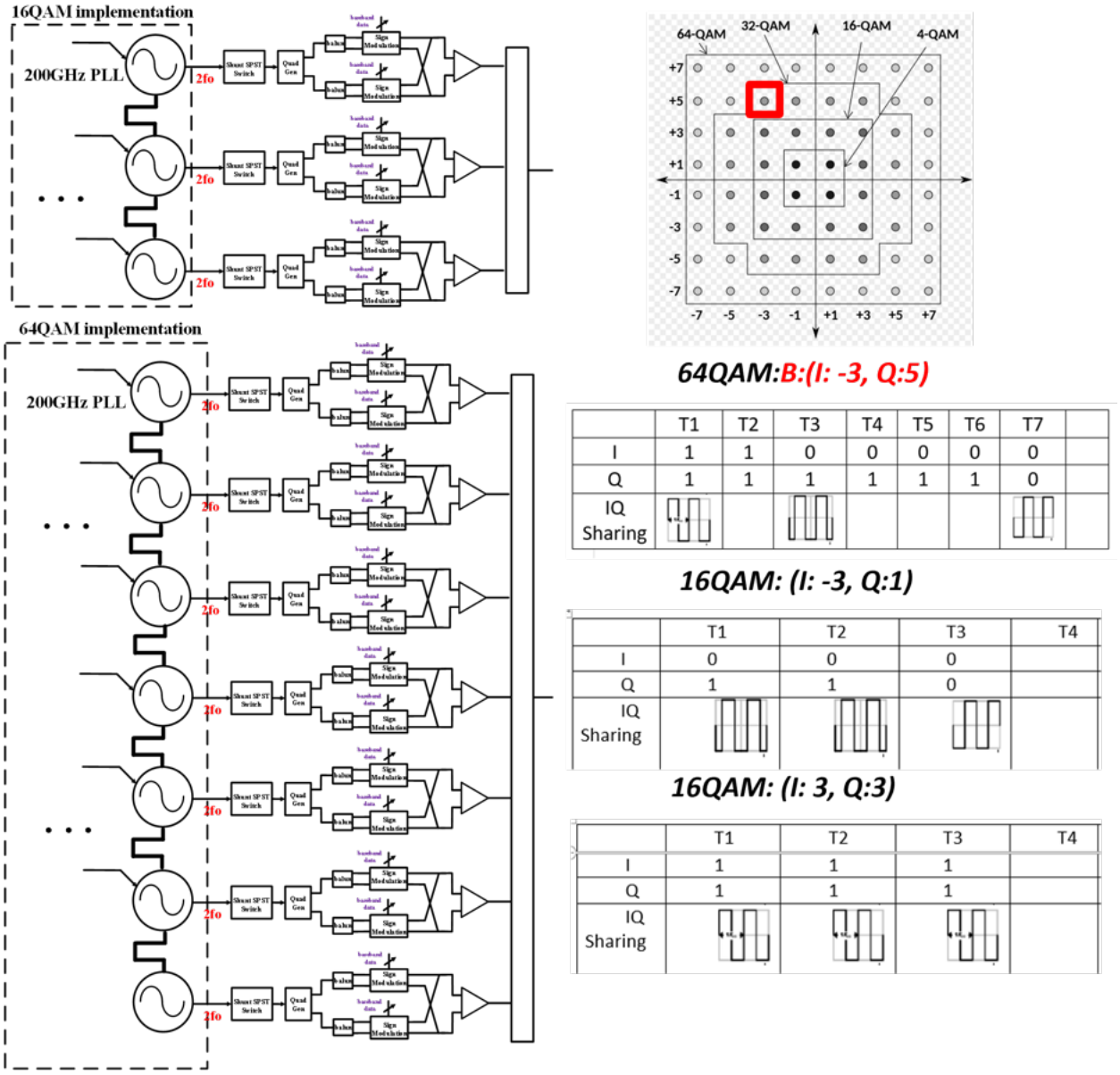
Figure 5.3: Concept of the proposed IQ sharing method.

5.3 Circuit Implementation-LO Generation

5.3.1 200GHz SSPLL topology

It is necessary to stabilize the frequency in order to get the LO signal with low phase noise, so a PLL is required. Sub-sampling PLL(SSPLL) is suitable for mmwave and sub-THz frequencies since it eliminates the need of the power-hungry dividers. In addition, SSPLL is also friendly for technology scaling: 1) utilizing the S&H as a phase error detector 2) small loop filter 3) transconductor for current integration. Fig. 5.6 also shows the noise contributors in a classical CPPLL and SSPLL, it is clear that the SSPLL can achieve better trade off between noise and power consumption. The 200GHz TX employs a SSPLL with a harmonic oscillator array, which achieves simultaneous high output power and low PN.

Fig. 5.7 shows the conceptual diagram of the 200GHz PLL architecture[7]. The cascaded SSPLL is leveraged in order to achieve low PN by stablizing the sub-THz signal, and the 2nd harmonic coupled oscillator array in this architecture is for generating relatively high power at 200GHz. Since sub-THz VCOs usually suffer from poor phase noise, wide PLL loop bandwidth is required to suppress the VCO noise. The cascaded PLL topology is able to achieve a higher loop bandwidth than that of a single-stage PLL. In addition, the inherently high PD gain of SSPLL also contributes to the low in-band phase noise. When the reference frequency is low, the SSPLL will be faced with the issue of harmonic locking: multiple harmonic signals are present within the tuning range (TR). Therefore, a frequency-locked



	T1	T2	T3	T4	T5	T6	T7	
I	1	1	0	0	0	0	0	
Q	1	1	1	1	1	1	0	
IQ Sharing								

	T1	T2	T3	T4
I	0	0	0	
Q	1	1	0	
IQ Sharing				

	T1	T2	T3	T4
I	1	1	1	
Q	1	1	1	
IQ Sharing				

Figure 5.4: Conceptual diagram of the oscillator array assisted digital IQ Sharing TX.

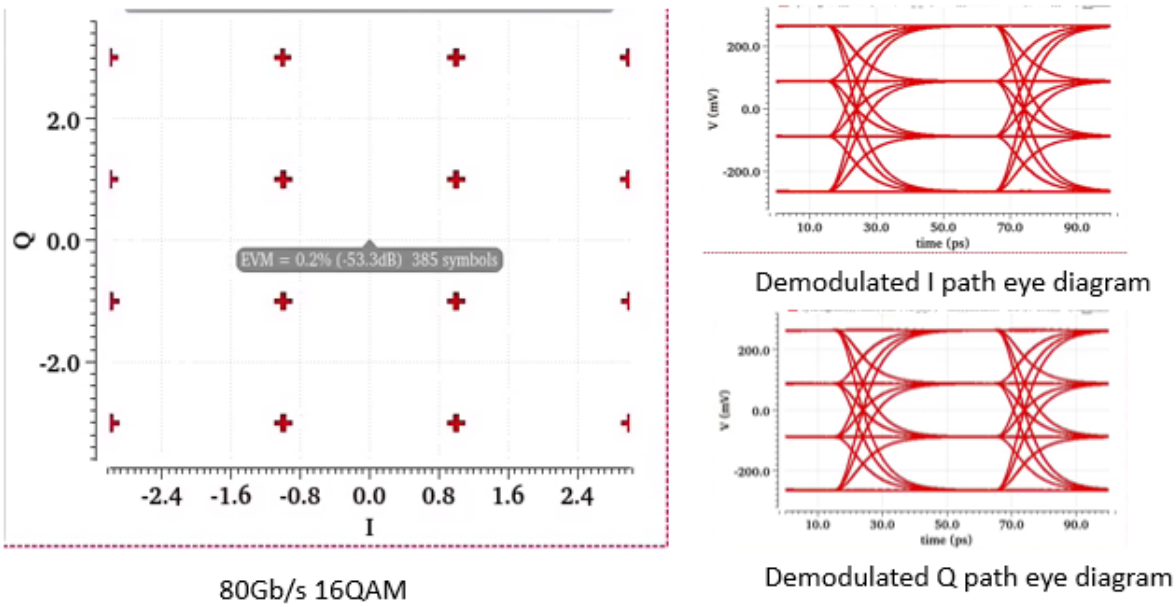


Figure 5.5: Constellation and eye diagrams of the demodulated signal.

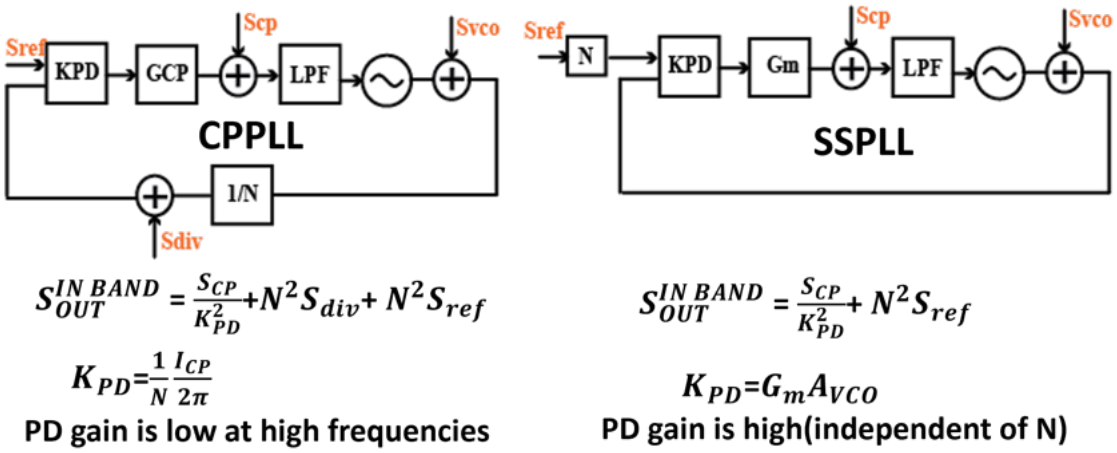


Figure 5.6: Noise contributors of CPPLL and SSPLL.

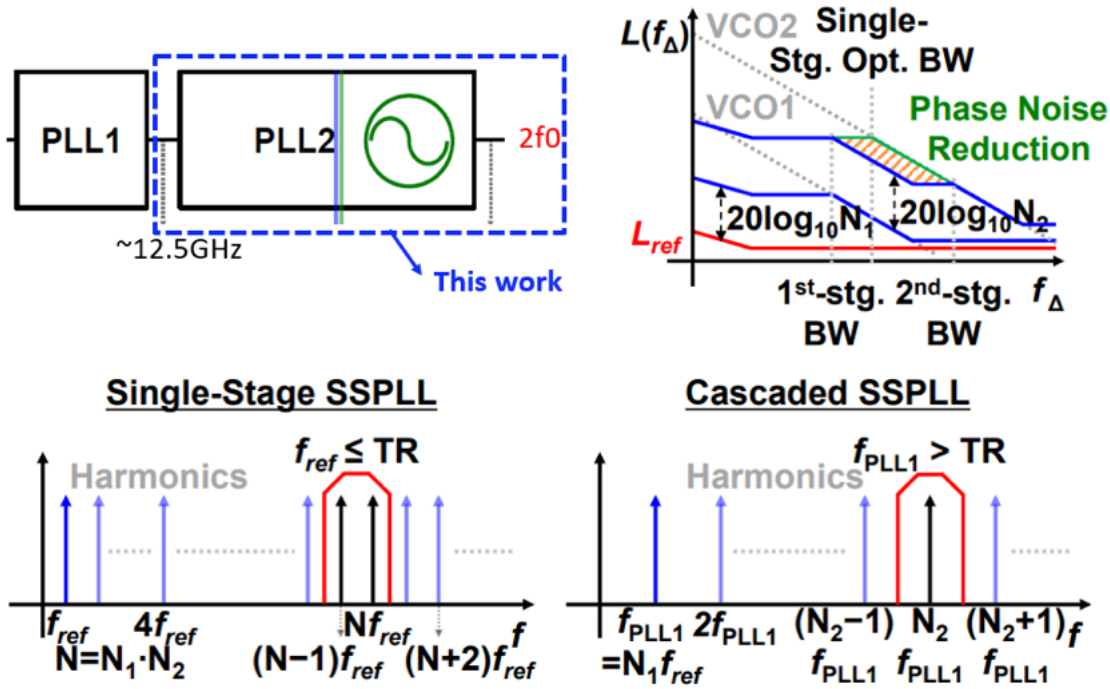


Figure 5.7: Conceptual diagram of SSPLL[7].

loop (FLL) with various dividers is required. However, with a cascaded SSPLL topology, a higher reference signal can be used, and thus these problems can be eliminated because only one harmonic signal exists in the TR[7].

Fig. 5.8 shows the overall architecture. It consists of a differential sub-sampling phase detector (SSPD), a transconductor, a loop filter, a 2nd harmonic coupled oscillator array, and a W-band buffer. A dummy sampler is also included to reduce the spur due to BFSK effect with mismatch. The on-chip loop filter is adjustable: tunable RZ,CZ and CP.The W-band buffer is employed to guarantee the amplitude of the sampling signal is large enough.

5.3.2 2nd Harmonic Coupled Oscillator Array

The 2nd Harmonic Coupled Oscillator Array enables higher output power, better phase noise and the implementation of IQ sharing logic.

5.3.2.1 Harmonic Oscillator Design

In this harmonic Oscillator, the oscillator is oscillating at 100GHz, and we extract the 2nd harmonic at 200GHz from the fundamental frequency (f0) of 100GHz. The maximum fun-

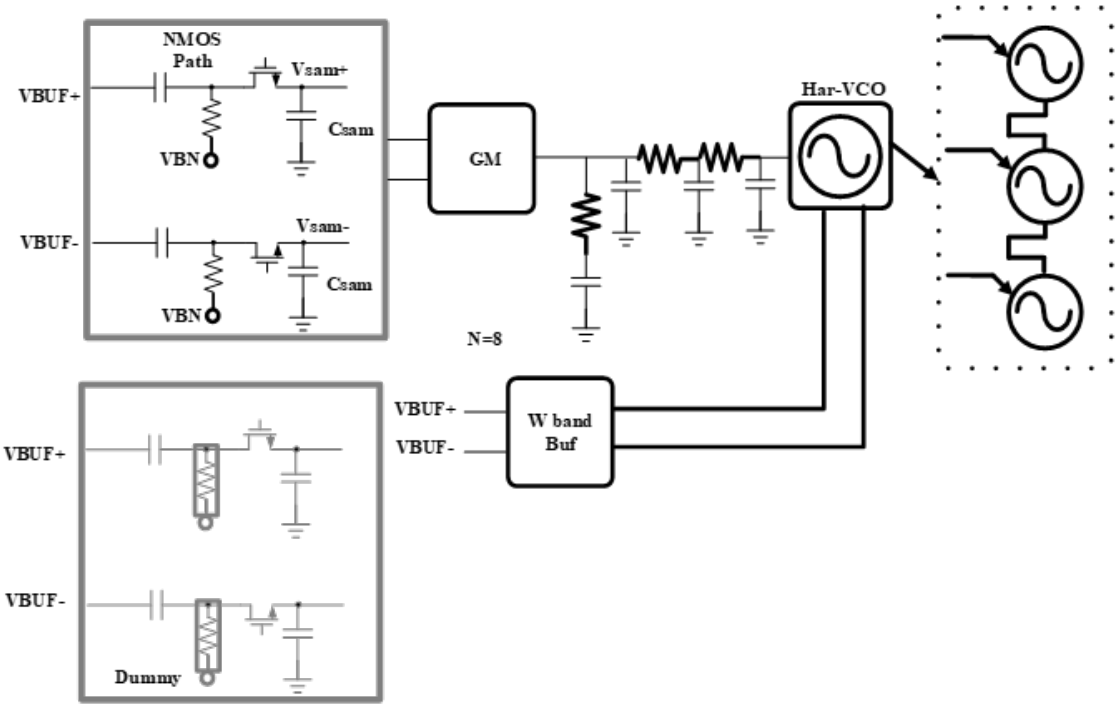
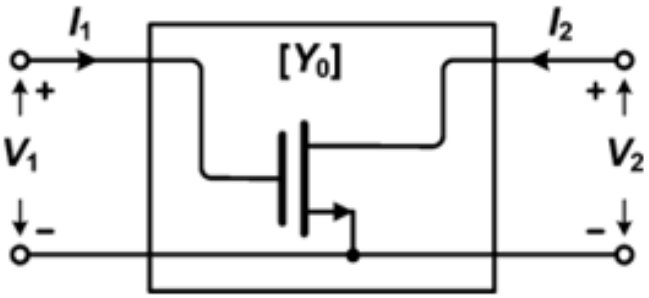


Figure 5.8: Diagram of the 200GHz SSPLL.



$$[Y_0] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$$

$$A = \frac{V_2}{V_1}$$

Figure 5.9: Two-port network representation of an NMOS transistor

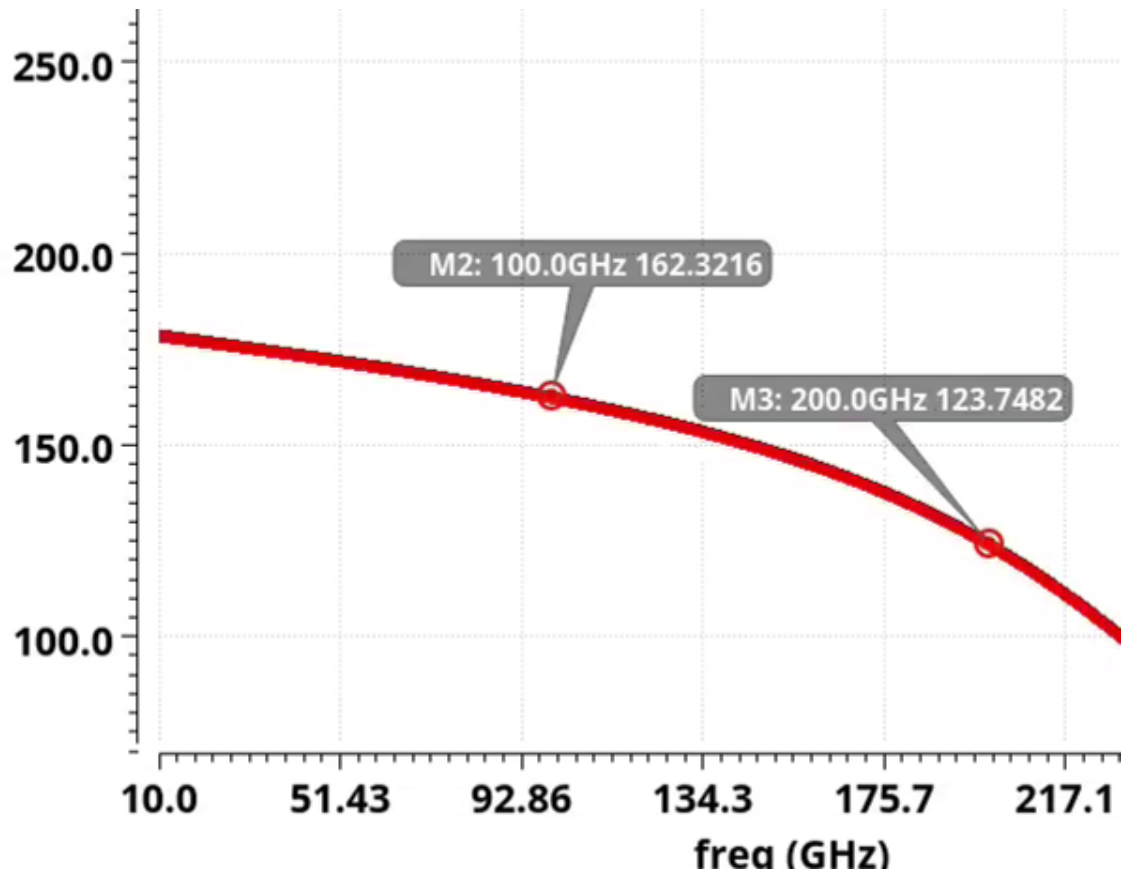


Figure 5.10: Simulated optimal phase.

damental power Pout of the two port network in Fig.5.9 can be calculated as[20]

$$Pout = -Re(V_1 I_1^*) - Re(V_2 I_2^*) \tag{5.2}$$

$$= -g_{11}\left|V_1\right|^2 - g_{22}\left|V_2\right|^2 - \left|V_1\right|\left|V_2\right|\left[(g_{12}+g_{21})\,cos\angle A + (b_{21}-b_{12})sin\angle A\right] \tag{5.3}$$

Here g_{ij} and b_{ij} are the real and imaginary parts of y_{ij}. To maximize the third term in (5.3), the optimal phase should be[20]

$$\angle A_{opt} = (2k+1)\pi - \angle(y_{21} + y_{12}^*) \tag{5.4}$$

Fig. 5.10 shows the optimum phase of the gate–drain for a RF NMOS in the Intel 16nm process, and at 100GHz, this device requires 162.32 degree. Considering that a phase shift of 180 degree is required across each stage for the oscillation in a cross-coupled oscillator, the remaining phase should be compensated through a gate transmission line. Therefore, a phase of 16.68 degree is required and it is feasible from the perspective of layout implementation.

Fig. 5.11 shows the topology of the harmonic oscillator. Harmonic positive feedback (HPF) between the fundamental frequency and second harmonic[21] is leveraged to enhance

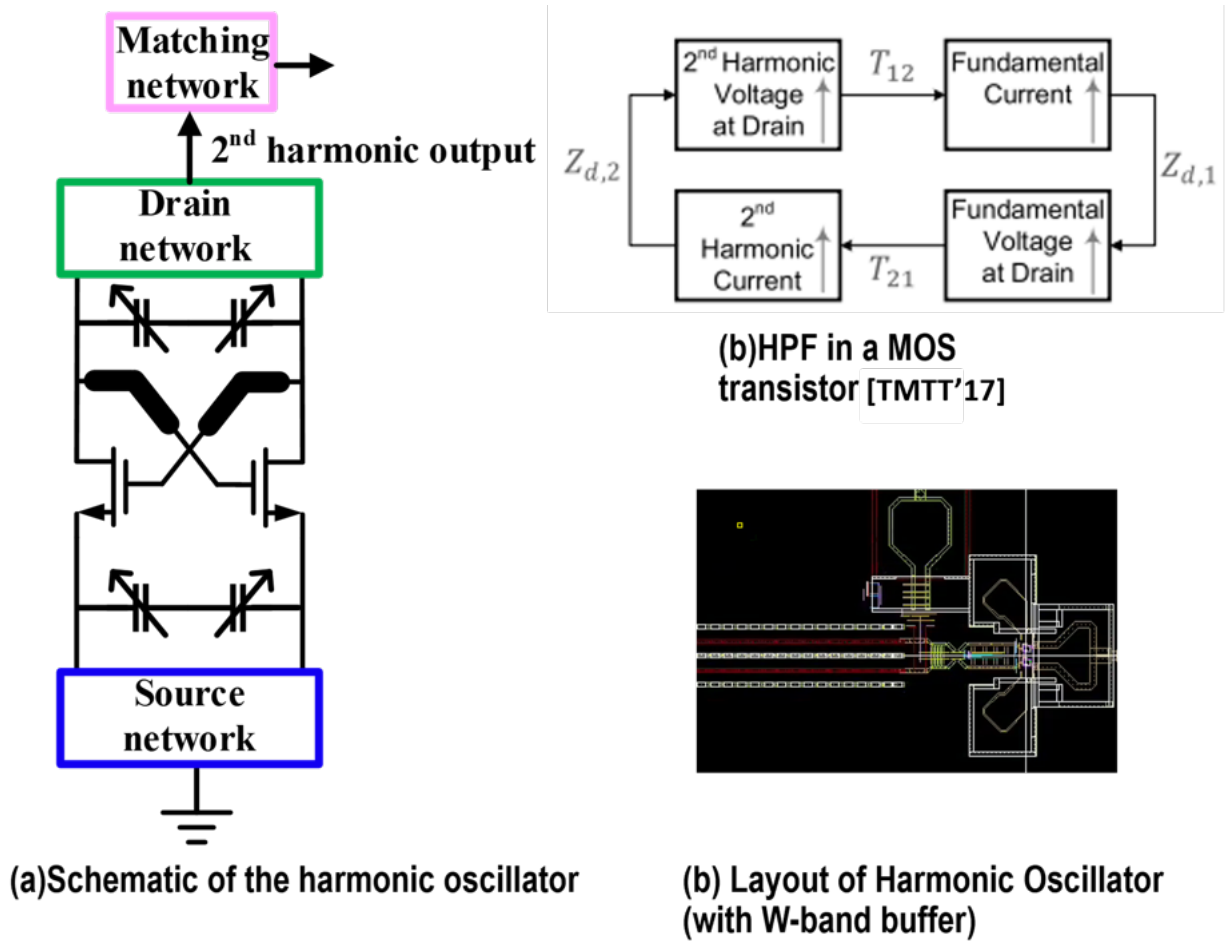


Figure 5.11: (a) Schematic of the harmonic oscillator. (b) HPF in the MOS transistor[21]. (c) Layout of the harmonic oscillator

the harmonic power. As shown in Fig. 5.11, regarding the second harmonic generation, the translation from fundamental frequency to second harmonic and the translation from second harmonic to fundamental frequency is a positive feedback process[21]. The HPF loop has its maximum effect on the second harmonic generation if 1) the drain impedance at both the fundamental frequency and second harmonic is resistive, and 2) the transistors operate more in the triode region. In addition, the cross section T-lines can also be utilized to provide the optimal phase between gate and drain at the fundamental frequency in order to enhance the oscillator fundamental output power.

In terms of the implementation of this harmonic oscillator, specifically, as shown in the half circuit in Fig.5.12, at the fundamental frequency f0, the high impedance path at the source node degenerates the equivalent noise source of the device and thus reduce the noise contribution to the output[21]. It also prevents the voltage clipping at the source

and enables deeper operation of the transistors at the triode region. To ensure the strong harmonic current integration, the fundamental swing should be boosted before arriving at the gate node of the other half. The cross section T-line(TLg) can help with this fundamental enhancement. Moreover, TLg with high Zo also helps with higher second harmonic at gate node. Both source and drain tanks include varactors. To further increase the tuning range, capacitor arrays are added at the source terminal instead of the drain terminal because the extra capacitor array at the drain terminal will lower the quality factor of the drain tank, reducing the impedance at 2f0 and thus affecting the generated harmonic output power.

5.3.2.2 In-Phase 2nd Harmonic Coupling

As is shown in Fig. 5.12, the three harmonic oscillators are coupled together using three half wavelength T-lines in a star configuration. In order to achieve robust in phase 2nd Harmonic Coupling, we choose node 2 to do the super-harmonic harmonic coupling. Any mismatch between the three OSCs will result in the difference in their free running frequency, which will lead to the phase mismatch and phase noise degradation. Our solution is to use the varactors at the source node to tune the free running frequency of the three OSCs to be similar to each other, and thus the negative effect of the mismatch between the self oscillating frequencies of the three oscillators can be eliminated. In addition, one nice thing about this method is that it have minimal effect on the generated 2nd harmonic power level. If the varactor is added at the drain terminal, it will degrade the quality factor of the drain tank and thus affect the generated 2nd harmonic power.

5.3.3 I/Q Generation and 3-way Power Combiner

As shown in Fig. 5.13, the proposed I/Q generator is based on a 3dB branchline coupler. It is comprised of 4 ports: Input (P1), Output 1 (P2) and Output 2 (P3). The fourth port (P4) is terminated at 50 ohms for the signal splitter and is isolated from the input. Fig. 5.13(b) shows the layout of hybrid quad, and the Zo is chosen to be 35 ohm. In addition, this hybrid quad also includes a 3 bits tunable isolation resistor to compensate the quadrature errors caused by PVT variations.

The proposed combiner is a radial 3-way Wilkinson combiner with “star isolation resistor” configuration. This 3-way combiner is also co-designed with the GSG pad. Therefore, an LC plus L matching network is inserted between the 3 way combiner and GSG pad to account for the parasitics of the GSG pad. The insertion loss of this combiner at 200GHz is around 1dB.

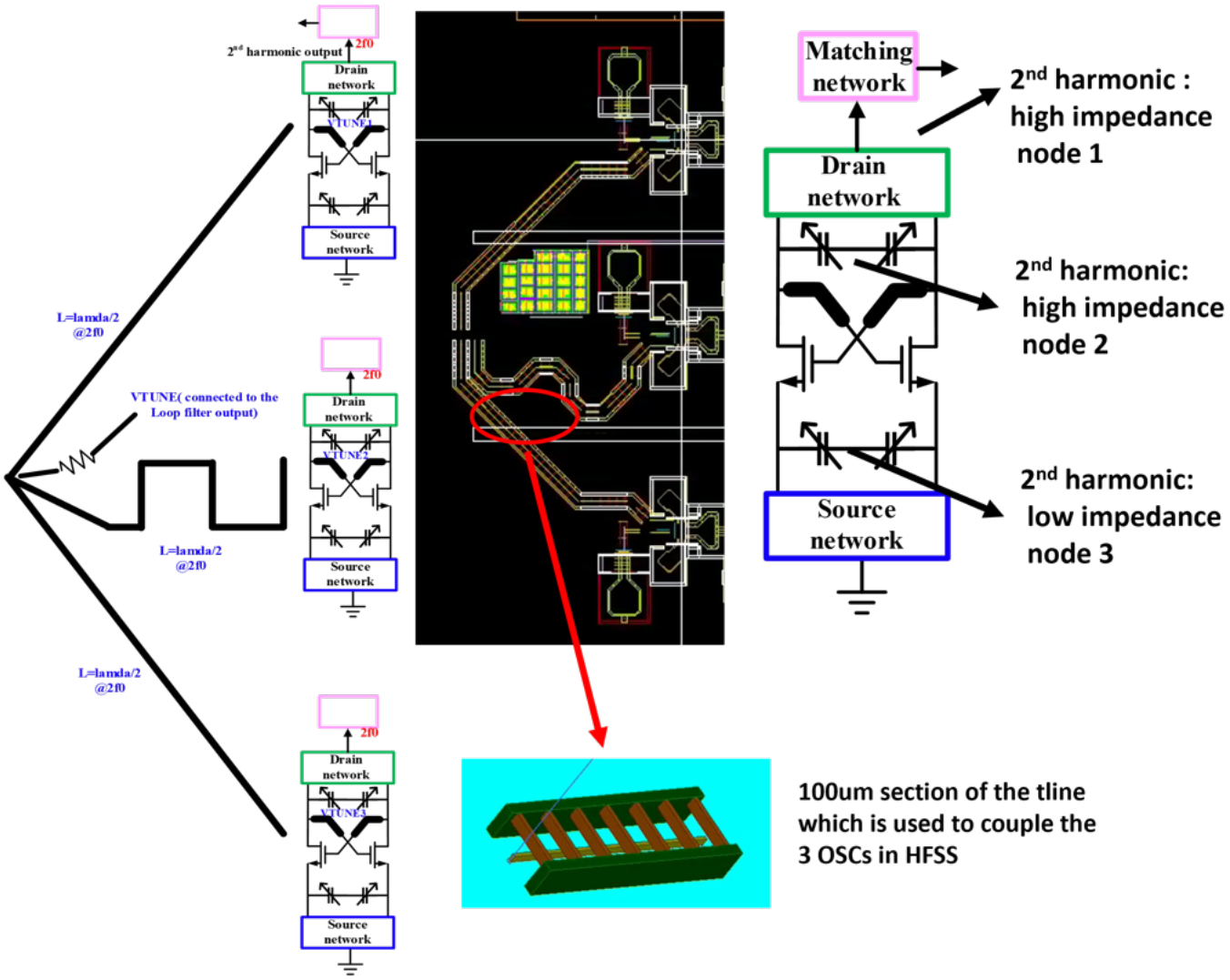


Figure 5.12: 1x3 harmonic oscillator array.

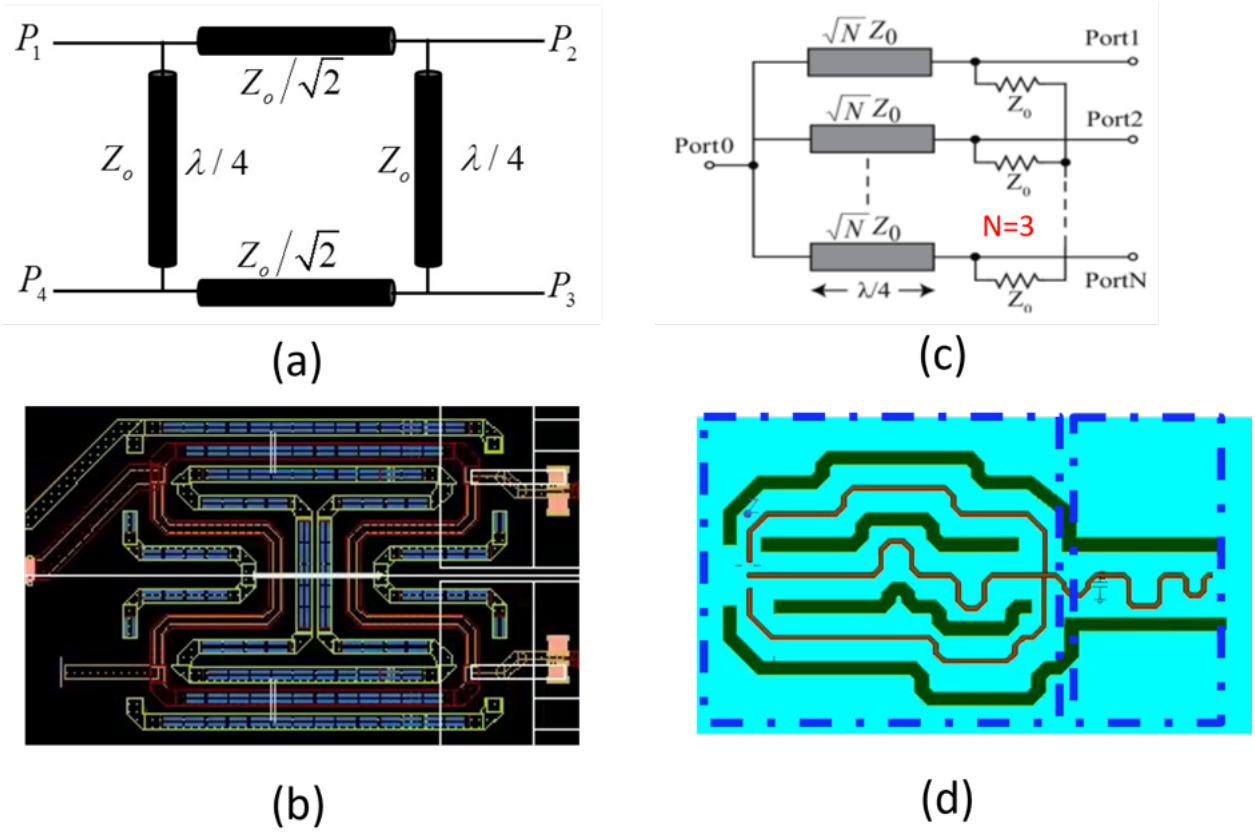


Figure 5.13: (a) Schematic of the branchline hybrid quad. (b) Layout of the brachline hybrid. (c) Schematic of the power combiner. (d) HFSS layout view of the power combiner, and the LC network between combiner and GSG pad.

5.4 Circuit Implementation-Data Path

5.4.1 I/Q sharing Circuit

The IQ sharing circuit achieves the function of the 4 to 1 multiplexer. It chooses the required LO signal based on the baseband data. As shown in Fig. 5.14, regarding the LO input differential pair(DP), it is a DP without using any neutralization. A series inductor is inserted between the LO DP and baseband switches to expand the bandwidth. If neutralized LO DP is utilized, a combination of parallel inductor and series inductor will be required to achieve better power matching. We also plug this circuit to the system level EVM testbench, and the demodulated constellation diagram and EVM of a 80Gb/s 16QAM signal are shown in Fig. 5.14.

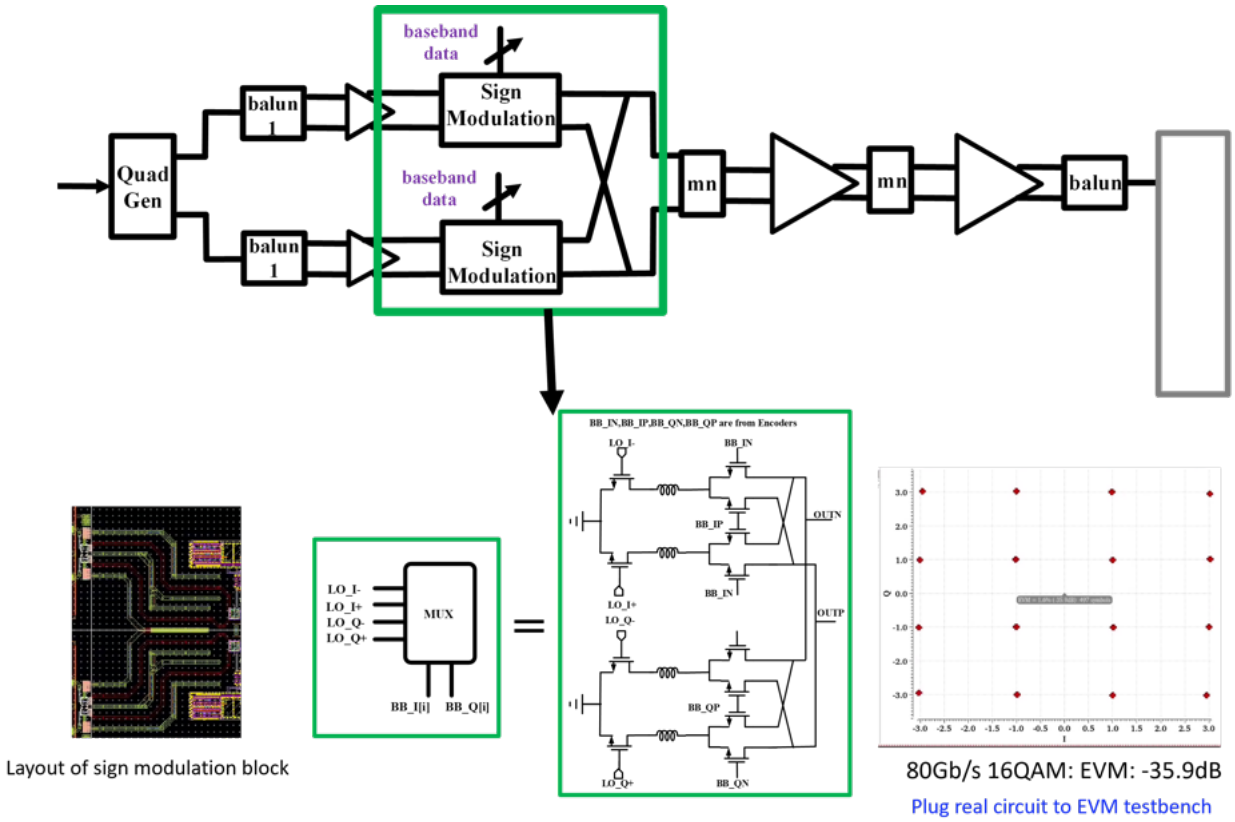


Figure 5.14: Schematic, layout and simulated EVM results of the IQ sharing block.

5.4.2 Saturated Amplifier Chain

As shown in Fig. 5.15, the saturated amplifier chain consists of two driver stages and one output stage. The driver stage adopts the gain boosting technique with higher order embedded network as explained in chapter 4, and the output stage utilizes the over-neutralized CS cell operating at saturation region. The simulated small-signal BW and large signal bandwidth of this saturated amplifier chain is 45 GHz and 50+ GHz, respectively. In addition, the simulated power efficiency of cascaded buffers at 2dBm output power level is about 5.5%

5.4.3 Baseband Data Generator

As shown in Fig. 5.16, the baseband(BB) data generator consists of half rate $2 \wedge 10$-1 PRBS generators and encoders. The encoder converts the I/Q BB PRBS data to the I/Q BB data which can be utilized in the IQ sharing circuit. The post extraction simulation results show that the proposed BB generator can support up to 88 Gb/s 16QAM signal.

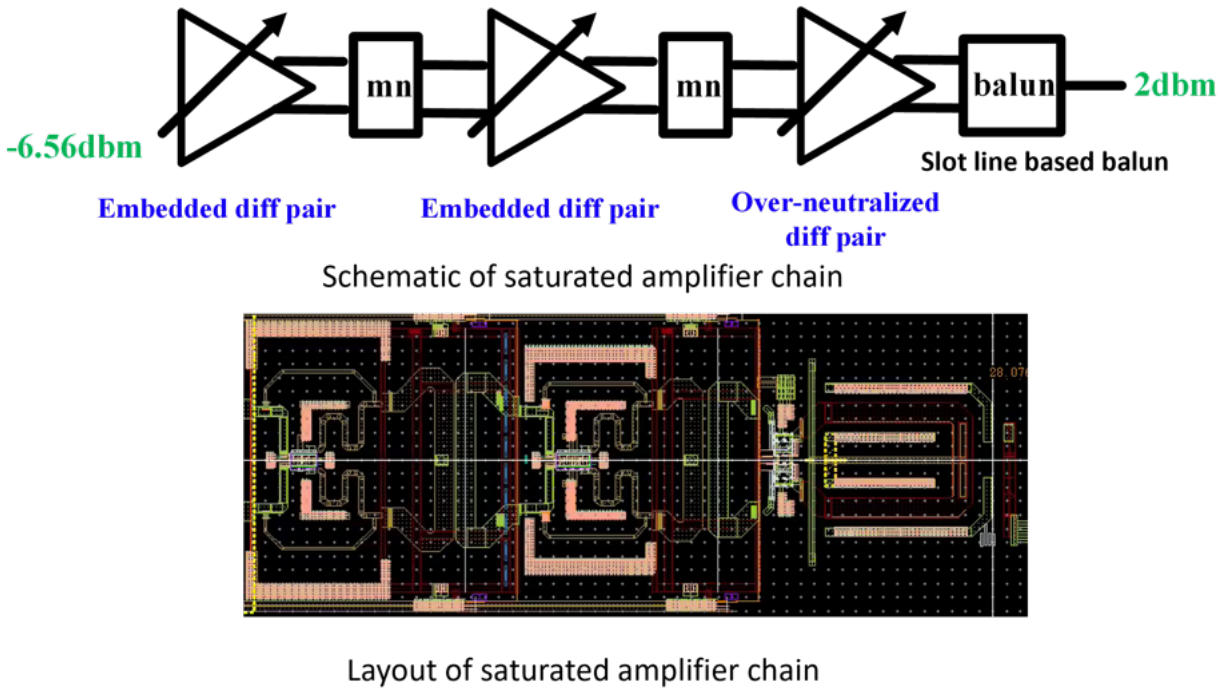


Figure 5.15: Schematic and layout of the saturated amplifier chain.

5.5 DTX Simulation Results

5.5.1 EVM Simulation Results

In order to verify the performance of the DTX, we plug the circuits in the green rectangular to the EVM testbench (shown in Fig. 5.17). The simulated EVM of 80Gb/s 16QAM signal with 5.5 dBm peak output power is -26.9dB, and its corresponding diagram is shown in Fig 5.17. Table 4.1 summarizes the simulation results of our 200GHz TX and compares the results to the state-of-the-art 200GHz TXs. The proposed TX achieves the best energy efficiency among all the 200GHz TXs.

5.5.2 SSPLL Full Loop Simulation Results

Fig. 5.18 shows the phase noise plots with different reference clocks featuring different phase noise performance. Regarding Fig. 5.18(a), the frequency of the reference clock is 12.525 GHz, and its phase noise at 100 kHz and 1 MHz frequency offsets are -104 dBc/Hz and -114 dBc/Hz, respectively (normalized at 100.2 GHz), the SSPLL full lopp simulation results show that the 200.4 GHz signal has a phase noise of -104.16 dBc at 1 MHz frequency offset and -111.9 dBc at 10MHz frequency offset. In terms of Fig. 5.18(b), the frequency of the reference clock is 12.525 GHz, and its phase noise at 100 kHz and 1 MHz frequency offsets

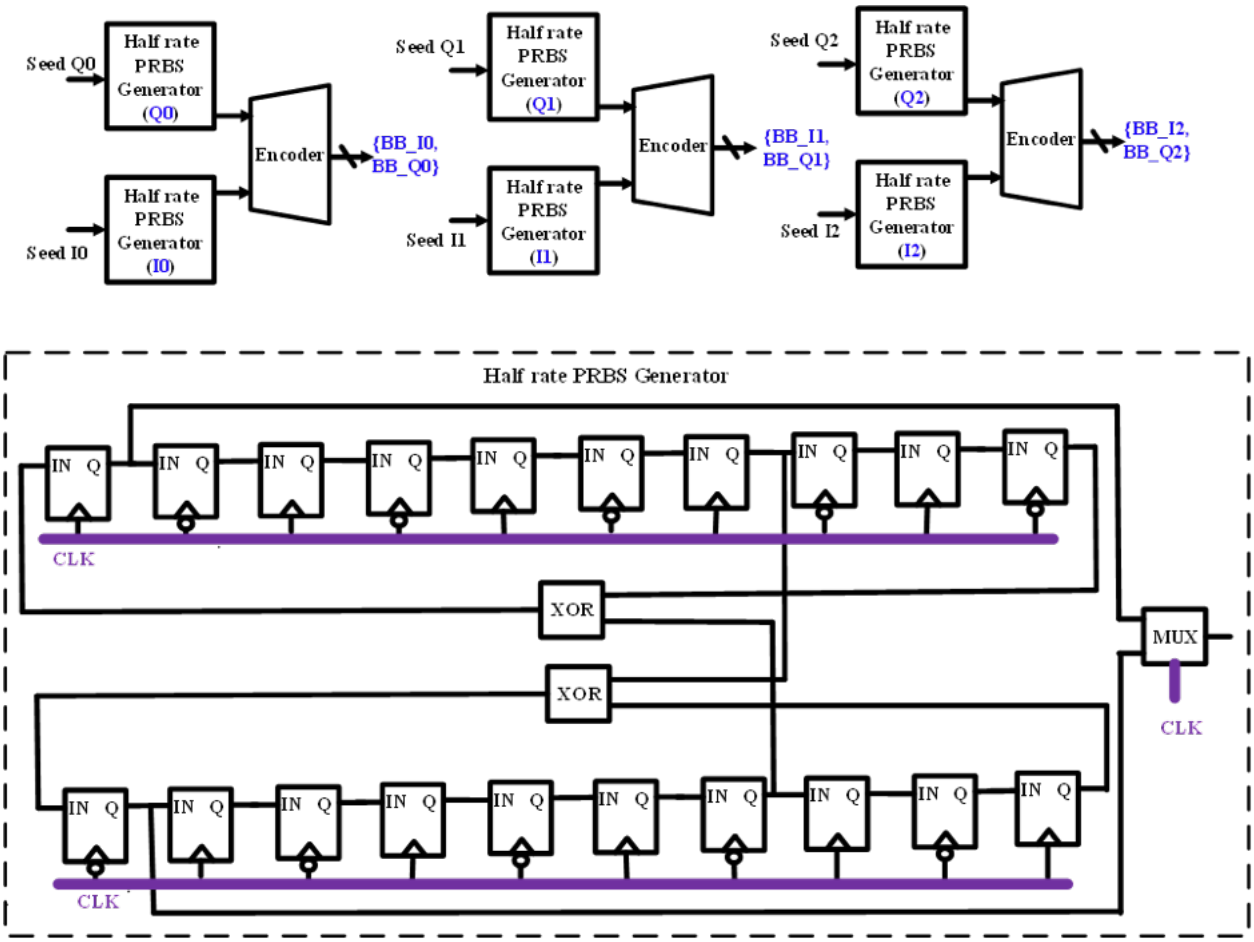


Figure 5.16: Diagram of the baseband data generator.

are -94 dBc/Hz and -104 dBc/Hz, respectively (normalized at 100.2 GHz), the SSPLL full lopp simulation results show that the 200.4 GHz signal has a phase noise of -96 dBc at 1 MHz frequency offset and -107.7 dBc at 10MHz frequency offset.

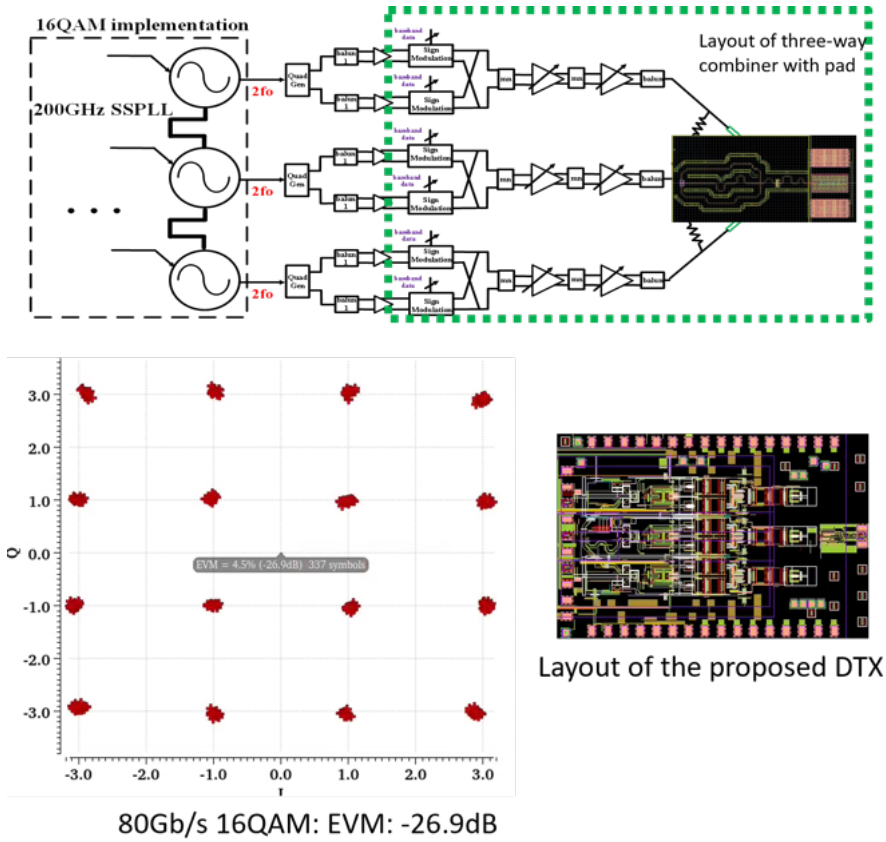


Figure 5.17: DTX EVM simulation.

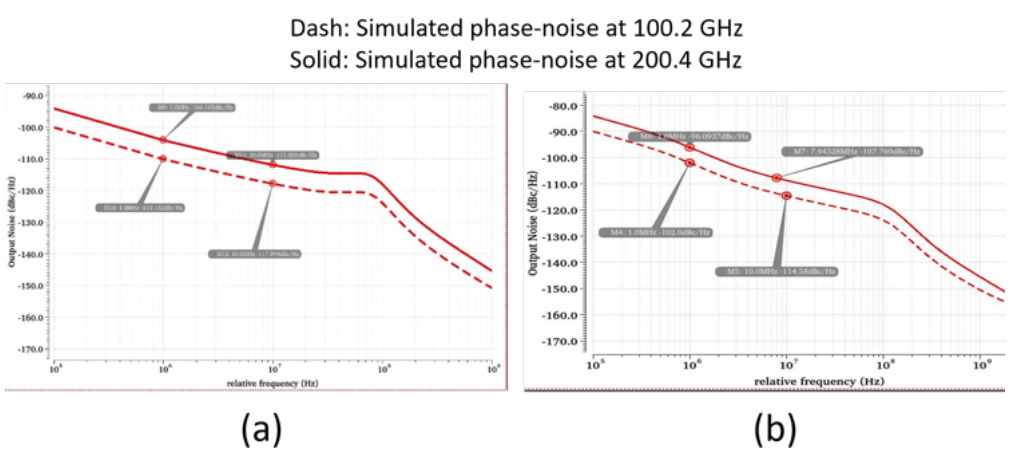


Figure 5.18: SSPLL phase noise plots.

Table 5.1: Performance Comparison of State-of-the-Art 200GHz Transmitters.

	[5] ***JSSC'2022***	[28] ***JSSC'2022***	[4] ***ISSCC'2019***	This Work
Antenna Integration	Yes	No	No	No
Technology	55 nm SiGe BiCMOS	135 nm SiGe BiCMOS	40nm Bulk CMOS	16nm Bulk CMOS
Antenna Integration	Yes	No	No	No
Frequency(GHz)	225	220	265	200
TX-Ppeak for Digital and OOK TX /TX-OP1dBm for Analog TX	-3 (per element)	3	-1.6	5.5
TX Pdc(mW)	165	640	1790	220
Energy eff(pJ/b)	8.3	57.1	22.38	2.75
Data Rate	20Gbps	11.2Gbps	80Gbps	80Gbps
Modulation	OOK	16-QAM	16QAM	16QAM

Chapter 6

Conclusion

6.1 Thesis Summary

In this dissertation, we demonstrated transmitter design techniques for high speed wireless communication at both 140GHz and 200GHz. At 140GHz, we presents two iterations of achieving an energy and power efficient transmitter module with both high data rate and high EIRP. Specifically, we (1) leverage a slotline-based power combiner for high output power generation, (2) intensively employed low-loss slotline based matching networks, (3) utilized NRC techniques in the up-conversion mixer for conversion gain and linearity enhancement via a combination of NMOS and PMOS cross-coupled pairs, and (4) implemented low power baseband amplifiers via current re-use g_m-cells. The measurement results validates the effectiveness of these techniques.

At 200GHz, we investigated different gain boosting techniques, and utilized these gain boosting techniques in the 200GHz PA. To further boost the output power, low lossy multi-way slotline based power combiners and splitters were employed. We also proposed a novel power efficient 200GHz digital transmitter architecture: an oscillator array assisted Digital IQ sharing Transmitter, which not only leverage digital scaling for power/performance, but also utilizes amplifiers in saturation region with enhanced power efficiency. The proposed 200GHz digital transmitter also include a 200GHz low phase noise SSPLL to stabilize the frequency of the oscillator array.

6.2 Future Directions

Regarding the 140GHz phase-array transmitter module, there are some possible options for future work: 1) further improving the output power and bandwidth, 2) demonstrating a complete digital beamforming transmitter system, 3) developing complete automatic calibration algorithms.

In terms of the 200GHz transmitter and PA design, they can be improved and expanded in a few aspects: 1) exploring more effective and robust gain boosting techniques, 2) deep anal-

ysis of the harmonic oscillator working mechanism and present better solutions for achieving simultaneous phase noise and harmonic power optimization, 3) improving the output power and efficiency of the IQ sharing circuits.

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