Cryogenic Optical Link: Device, Circuit, and System

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By

Bozhi Yin

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Abstract

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High-bandwidth density and energy-efficient readout interfaces connecting the superconductor electronic (SCE) integrated circuits (IC) with room-temperature environments are essential for emerging quantum and classical superconducting computing applications, which motivate the design of cryogenic optical links.

This work addresses four challenges in this communication link. First, a comprehensive link model, which consists of superconductor and semiconductor electronic/photonic components, is built to analyze the performance and energy efficiency of the link. Then, a novel cryogenic optical link based on the monolithic silicon photonic process and laser-forwarded coherent architecture is proposed to balance power consumption at cryogenic and room-temperature environments and improve overall energy efficiency. Next, an accurate device model is necessary for circuit design nowadays, while little is known about the transistor's behavior at cryogenic temperatures. A detailed theoretic analysis and device characterization of transistors from monolithic silicon photonic processes is presented. Following that, a proof-of-concept single-chip CMOS electronic-photonic cryogenic transmitter is designed and implemented in the 45RFSOI process. The link experiment at cryogenic temperatures with the direct drive from superconductor IC demonstrates its function, performance, and energy efficiency. Compared to the existing solution, our work shows the best energy efficiency by eliminating the extra discrete cryogenic amplifier requirement. Finally, a new type of EOPLL, including a boundless phase shifter-based phase rotator and dLev comparator-based phase estimator, is proposed to solve the inevitable time-varying phase offset issue in the laser-forwarded coherent architecture. A proof-of-concept coherent receiver with proposed EOPLL is designed and implemented in the 45SPCLO process.

To my family.

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Acknowledgments

Looking back at my five-and-a-half-year journey at Berkeley, I am glad I worked with great advisors, amazing professors, and wonderful colleagues and friends.

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Chapter 1

Introduction

Cryogenic technology and integrated circuits are becoming increasingly important in future computing systems. Josephson junction-based devices are used to form qubits for quantum computing [1]. In classical digital computing applications, Josephson junction-based superconductor electronic circuits can be much more energy efficient, especially for applications that must operate at cryogenic temperatures below 10 K [2–4]. Both applications require control and communication interfaces that operate at room temperature. However, traditional electrical interconnects significantly increase the complexity of the cryogenic systems - coax cables and solder joints are bulky and fragile, causing intermittent failures, and enable heat-leak paths that lower the overall energy efficiency [5]. The wireless solution can mitigate heat leakage [6], but its scalability is constrained by antenna dimensions and potential signal interference. Optical interconnects offer an opportunity to improve the reliability, density, and energy efficiency of the cryogenic solutions dramatically [7–9].

Existed cryogenic optical link solution [9–16] requires additional discrete cryogenic amplifies for signal amplification and impedance match when interfacing with superconductor electronics, which limits the bandwidth density and energy efficiency of the system and eventually impedes system scalability [5].

In this research, we leverage the integration of electronics and photonics in a monolithic CMOS photonic platform to implement a cryogenic optical link connecting the superconductor electronic IC to the room-temperature environment.

1.1 Thesis Organization and Contribution

The rest of this thesis details the modeling, analysis, design, and experiments involved in building an energy-efficient cryogenic optical link that crosses cryogenic and room-temperature environments for superconductor computing system.

In Chapter 2, the author introduces the basics of superconductor electronics (SCE) and its application in classical computing systems as digital electronics. The lack of scalable superconductor memory motivates the research on cryogenic optical links that can connect

superconductor computing cores with room-temperature memory. After analyzing the pros and cons of traditional electrical links and existing optical solutions, the author proposes a cryogenic optical link that is built on the monolithic silicon photonic process and laser-forwarded coherent architecture.

Chapter 3 outlines the laser-forwarded coherent architecture and the key photonic device (the micro-ring modulator). A comprehensive model is proposed to perform system-level optimization to address the trade-offs in this complicated system consisting of superconductor and semiconductor electronic/photonic components.

An accurate device model is required to predict the function and performance of circuits operating at cryogenic temperatures. Chapter 4 presents the fundamental transistor behavior at cryogenic temperatures. Following that, the characterization results of transistors from two monolithic silicon photonic processes, including DC, delay, and noise characterization, are presented, paving the way to design analog and mixed-signal circuits in cryogenic electronic-photonic systems. This work is done in collaboration with Xiangwei Kong and Yuean Gu. Parts of this work appear in

- **B. Yin**, X. Kong, Y. Gu and V. M. Stojanović, "Cryogenic Characteristics of MOSFET in Monolithic Silicon-Photonic Process," in IEEE Transactions on Electron Devices, doi: 10.1109/TED.2024.3392871.

In Chapter 5, a micro-ring modulator-based cryogenic optical transmitter is designed and implemented in the 45RFSOI process. After a full electro-photonic package, a complete link characterization is performed with the direct drive from the superconductor IC, followed by a detailed energy efficiency analysis based on the measured results. Finally, a superconductor multichip module is designed to integrate the superconductor IC with the electro-photonic IC onto the same substrate and further improve throughput and energy efficiency. This work is done in collaboration with collaborators from Boston University: Hayk Gevorgyan, Deniz Onural, Bozhan Zhang, and Professor Milos Popovic. Parts of this work appear in

- H. Gevorgyan et al., "Cryo-Compatible, Silicon Spoked-Ring Modulator in a 45nm CMOS Platform for 4K-to-Room-Temperature Optical Links," 2021 Optical Fiber Communications Conference and Exhibition (OFC), San Francisco, CA, USA, 2021, pp. 1-3.
- **B. Yin**, H. Gevorgyan, D. Onural, A. Khilo, M. A. Popović and V. M. Stojanović, "Electronic-Photonic Cryogenic Egress Link," ESSCIRC 2021 - IEEE 47th European Solid-State Circuits Conference (ESSCIRC), Grenoble, France, 2021, pp. 51-54, doi: 10.1109/ESSCIRC53450.2021.9567813.

and a paper is currently being reviewed by Nature Electronics.

Chapter 6 analyzes the phase fluctuation issue in the laser-forwarded coherent architecture. To address this issue, an EOPLL, consisting of a dLev comparator-based phase estimator and thermal boundless phase shifter-based phase rotator, is proposed. To prove

the new architecture, a proof-of-concept coherent receiver is designed and implemented in the 45SPLCO process, in which design objectives, circuit implementation, packaging flow, and measurement results are detailed.

Chapter 2

Background

2.1 Introduction to Superconductor Electronics (SCE)

When certain materials are below a critical temperature (T_c), the material becomes superconducting. The distinctive physics of superconductors, such as zero direct current (DC) resistance for sufficient small current, enables the creation of circuits that are otherwise challenging or impossible to achieve. For instance, a superconducting loop with inductance L and circulating current I stores magnetic flux $\Phi = LI$. Unlike a loop made with resistive material, the current can circulate as long as the material stays superconducting, which is analogous to an ideal capacitor.

The critical temperature of known superconductors ranges from near absolute zero to about 203K. Superconductor electronics (SCE) are functional electronic circuits incorporating active and passive elements that are superconducting below the critical temperature. In general, its application tends to cluster in temperature around the boiling point of liquid nitrogen (77K), the boiling point of liquid helium (4.2K), and the superfluid helium-4 temperature range below about 2.17K [4]. Among different superconductors, the workhorse is niobium (Nb), which has $T_C \approx 9K$. It is a conventional low-temperature superconductor suitable for circuit operation typically at 4 to 5K, and supported by multiple foundaries [17].

Here, we introduce several key devices and technologies used in the SCE system.

Josephson Junction (JJ) based digital logic

The Josephson junction is formed by separating two superconductor electrodes with a thin insulator, as shown in Fig. 2.1. Quantum tunneling of Cooper pairs through the thin barrier layer allows a supercurrent to flow between two electrodes with zero voltage drop. The maximum supercurrent is called the critical current, I_C. When the current through a JJ exceeds the critical current, it switches (the superconducting phase difference across the junctions jumps by 2π) and produces a single flux quantum (SFQ) output. The SFQ

digital logic represents digital "1" and "0" by the presence and absence of magnetic flux quanta within a circuit element. Its switching energy $E_{sw} \approx I_C\Phi_0 = 2 \times 10^{-19}J = 0.2aJ$ for $I_C = 100\mu A$ [4]. For comparison, the switching energy of a transistor in advanced CMOS technology is $E = CV_{DD}^2 = 5.6 \times 10^{-16}J$ assuming $C = 1fF$ and $V_{DD} = 0.75V$. The several orders of magnitude lower in switching energy makes JJ-based computing architecture attractive in supercomputing systems [8, 18].

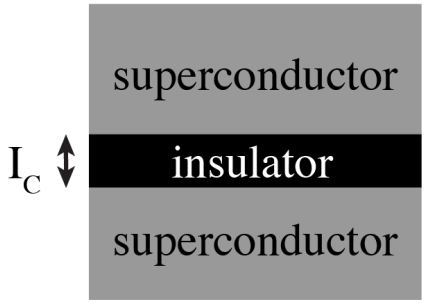


Figure 2.1: Strcutre of Josephson Junction.

SCE memory

Memory is a key block in computers based on von Neumann architecture and has been a bottleneck in many modern high-performance computing (HPC) systems [19]. The superconductor electronic memory can be classified by memory device technology: Josephson junction logic circuits, magnetic devices, or nanowire superconductor devices; and by use: register, cache, or main memory. The status of memory is summarised in Table. 2.1 [4].

Despite the different technologies used in memory design, the largest demonstrated superconducting random-access memory (RAM) is only 4 kibit (4096 bits), limited by the size of the superconductor devices, which is far below the requirement of main memory in the computing system. Today's HPC systems are dominated by x86 architectures coupled with 2–3GB of main memory per core [19]. Even with the smallest superconductor memory with a bit cell area of $26.5\mu m^2$, the area of $424000mm^2$ is required to achieve 2GB memory.

The hybrid JJ-CMOS memory, putting the CMOS memory core along with the superconductor chip at the cryogenic temperature, can leverage the capability of large-scale integration in advanced CMOS processes and potentially provide a large enough main memory. However, the interface between SFQ and CMOS logic with totally different voltage domains causes a huge power consumption. For instance, the read and write power of a 64 Kibit CMOS memory chip fabricated by TSMC using 65nm technology are 12mW and 21mW at 1GHz operation [20], leading to the energy efficiency of 183fJ/bit and 320fJ/bit at 4K. Compared to the energy of SFQ logic at the order of 10^{-18}J/bit, the energy for memory access becomes significant and dominates the whole system's power. Inside the Hybrid-CMOS

Table 2.1: Superconductor Memory Status

Name	Bit Cell Area [μm^2]	Latency [ns]		Energy [fJ]		Static Power	Bits
		Read	Write	Read	Write		
shift register, ac-biased	300 (15×20)						202280
shift register		0.02	0.02	0.1	0.1	0.2mW	64
vortex transition memory	99(9×11)	0.1	0.1	100	100		72
Josephson Junction RAM	484 (22×22)					4.5mW	4096
Reciprocal quantum logic	1452 (33×44)						1024
PTL-RAM	1452 (331×44)						512
Spin Hall effect magnetic tunnel junction	2470 (38×65)	0.1	2	1000	8000		16
Superconducting nanowire memory	26.5 (5×5.3)	0.1	3	10	10		8
Hybrid: JJ-CMOS [20]		0.4	0.4	183	320		65536

memory, the majority of the power consumption comes from the interface circuit, where the millivolt superconductor logic signals are amplified to 60mV and then drive a very sensitive CMOS comparator to produce the required volt-level signals.

Refrigeration

Unlike other computing systems, the SCE-based computing system must operate at deep-cryogenic temperatures requiring refrigeration. Therefore, cryogenic refrigeration's power cost must be accounted for when calculating overall energy efficiency. One key figure of merit in evaluating refrigerators is specific power, defined as the input power divided by cooling power:

$$\text{Specific Power} = \frac{\text{W at 300K}}{\text{W at T cold}} \tag{2.1}$$

where T cold is the target temperature at which we want the system to operate. The typical specific power of refrigerators is listed in Table 2.2 [4]:

Table 2.2: Specific power range for cryogenic refrigeration

T cold	Cooling Power Range	Specific Power [W/W]
80K	1.4W to 190kW	5.4×10^{1}
40K	1.1W to 61.5kW	1.69×10^{2}
20K	2W to 320W	4.56×10^{2}
4.5K	120W to 1000W	4.87×10^{2}
4.2K	0.08W to 2.7W	9.24×10^{3}
100mK	0.25mW to 1mW	3.22×10^{7}
20mK	6μW to 30μW	1.09×10^{9}

As we can observe from Table 2.2. The lower the temperature we want to achieve, the higher the cooling penalty we need to pay, which raises a design consideration: we can distribute the function of the system and the corresponding power over the different temperature stages to optimize the figure of merit (energy per bit). Furthermore, cooling capability significantly decreases at low temperatures, impeding the scalability of the system.

2.2 Interconnection Requirement of SCE

For SCE-based computing systems, the on-chip communication can be performed with Josephson transmission lines (JTL) or passive transmission lines (PTL). Chip-to-chip communication using SFQ pulses has also been demonstrated [17].

But power and data also need to move between the cryogenic and room temperature environments with very low heat loads to the cryogenic environment. As we discussed in the previous section, the lack of scalable and area-efficient RAM prevents the implementation

of superconducting computing. One way to bypass the issue of non-existent cryogenic RAM is to let the superconductor computing core access the room-temperature memory through an energy-efficient communication link that crosses the cryogenic and room-temperature environments.

The most challenging is data movement from a cryogenic environment due to the small energy in an SFQ pulse and the refrigeration penalty on any energy dissipated in amplifying or converting signals at cryogenic temperature. This is also called a cryogenic egress link.

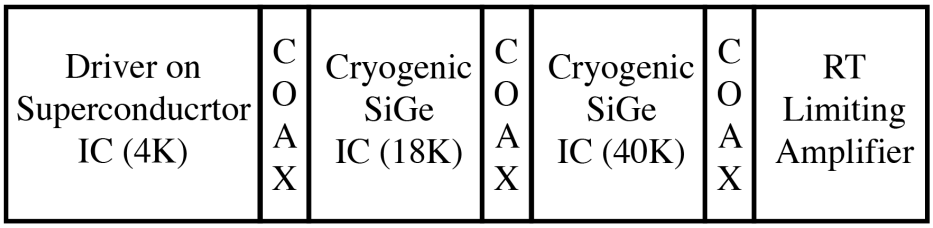


Figure 2.2: Electrical cryogenic egress link.

Hybrid superconductor-semiconductor digital data links are proposed to solve the issue of interconnection. As shown in Fig. 2.2, cryogenic signal amplifiers are placed at multiple temperature stages to reduce total power consumption [5]. However, the heat load induced by the heat-leak path (coaxial cable) between different temperature stages degrades the overall energy efficiency. Besides that, the electrical interconnects significantly increase the complexity of the cryogenic systems - coax cables and solder joints are bulky and fragile, causing intermittent failures.

Therefore, building an energy-efficient and high-reliability cryogenic egress link has recently gained much interest.

2.3 Heater leakage in Cryogenic Egress Link

In the above section, we mentioned that the heat leakage in the traditional electrical link could be much larger than the power consumed by active devices and eventually dominate the power consumption. Here, let's quantitatively calculate its value and compare it with the heat load generated by another type of wire, fiber.

The heat flow conducted across small temperature differences can be calculated using the formula:

$$Q = -KA\frac{dT}{dx} \approx -KA\frac{\Delta T}{L} \tag{2.2}$$

where K is the thermal conductivity, A is the cross-section area, ΔT is the temperature difference, and L is the length of the heat conduction path. Thermal conduction across significant temperature differences should be calculated using the thermal conductivity integral.

But here, we assume the thermal conductivity of material does not change with temperature for simple calculation: $K_{BeCu} = 107W/(m \times K)$ and $K_{SiO2} = 1.4W/(m \times K)$

0.047" semi-rigid coaxial cable made with BeCu is usually used in cryogenic applications. The diameter of the cable's inner conductor, dielectric, and outer conductor is 0.28mm, 0.94mm, and 1.2mm, respectively. Assuming the cable has a length of 0.29m and is thermalized at an intermediate temperature of 40K, then the heat load on the 4K stage caused by this cable can be estimated by the following equation:

$$\begin{aligned} Q_1 &= Q_{inner\_conductor} + Q_{outer\_conductor} \\ &= \frac{107mW}{mm \times K} \times \pi(0.14mm)^2 \times \frac{(300-4)K}{290mm} + \frac{107mW}{mm \times K} \times \pi(0.6^2 - 0.47^2)mm^2 \times \frac{(40-4)K}{290mm} \\ &= 12.5mW \end{aligned} \tag{2.3}$$

The measured heat load of this cable is 2.2mW [5], which means our calculation method does not off too much.

For glass fiber, the cladding and the core are manufactured together from the same silicon dioxide-based material. The manufacturing process adds different amounts of dopants to the core and cladding to maintain a difference in refractive indexed between them of about 1%. Therefore, we can assume the thermal conductive path of the single-mode fiber is full of SiO2 and has a diameter of 125um. Then we can use the same equation to estimate the maximum heat load introduced by the optical fiber with the same length as above coaxial cable.

$$Q_2 = \frac{1.4mW}{mm \times K} \times \pi(0.0625mm)^2 \times \frac{(300-4)K}{290mm} = 17.5\mu W \tag{2.4}$$

Compared to the electrical interconnection, the heat leakage is reduced by roughly 1000 times due to the glass fiber's larger thermal resistance and smaller cross-section area. Thermal anchoring and longer fiber length can further reduce heat load without sacrificing. As a result, Sub-μW level heat load caused by the fiber is much smaller than power consumed by other components in the link and can be neglected in calculating energy efficiency.

2.4 Emerging Solutions of the Cryogenic Egress Link

Wireless solution

To reduce the heat leakage between two temperature stages in the communication link, one straightforward method is using wireless communication, which eliminates all physical connections between two environments. However, it has been demonstrated that a large portion of the millimeter wave sent by the room-temperature transmitter is absorbed by the refrigerator and causes the heat load [6]. Furthermore, free-space wireless communication must cross the refrigerator, which is limited in size. This leads to a limited overall link capacity due to the large size of antennas and substantial interference between signals.

Electronic-photonic solution

Compared to wireless methods, optical interconnects provide significant bandwidth outside the cryogenic environment via multiple fibers and wavelengths per fiber. Additionally, since optical fibers have negligible heat leakage, optical interconnects emerge as a promising option for cryogenic egress links due to their high reliability, density, and energy efficiency [7–9].

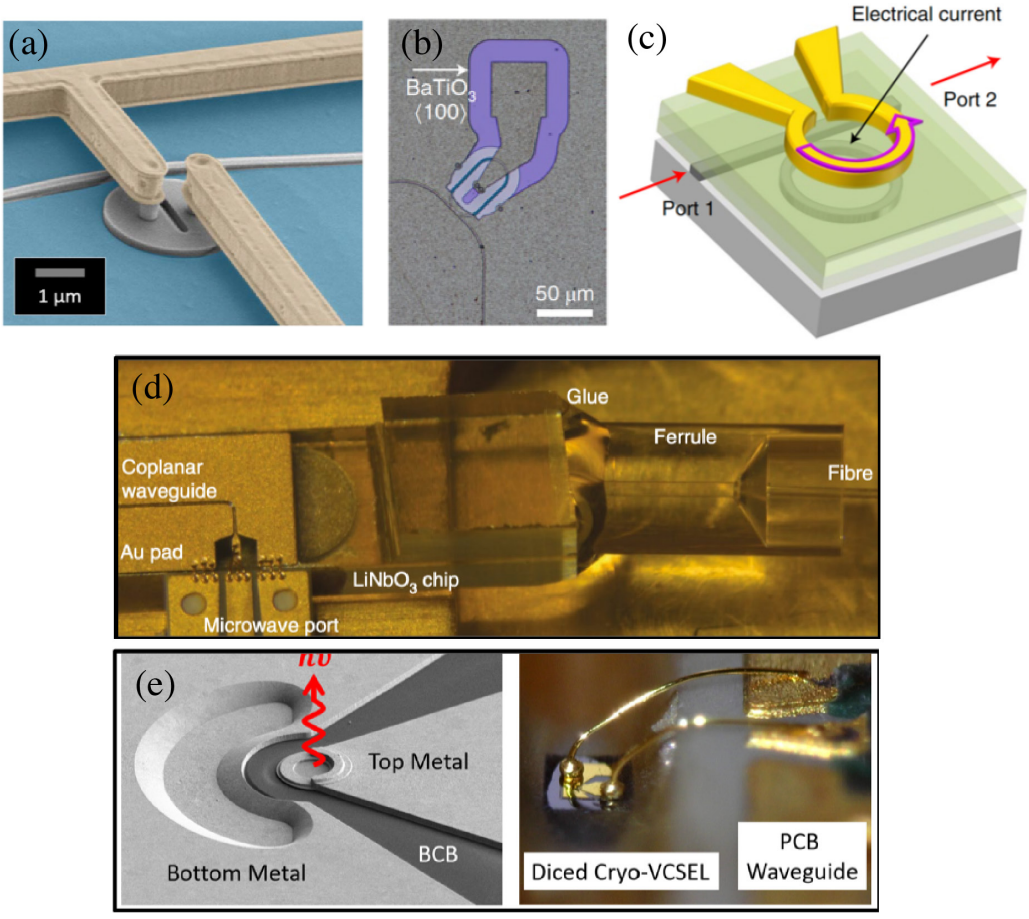


Figure 2.3: Existed electronic-photonic solution for cryogenic egress link: (a). Micro-Disk modulator[10], (b) BaTiO3 modulator[11], (c) Garnet magneto-optic modulator[9], (d) LiNbO3 modulator[15], and (e) Cryo-VCSEL[16].

The largest challenge in this electronic-photonic (EO) interface is to convert the very low-swing ($\sim$ 1 mV) electric output of superconductor electronic circuits to the optical domain, which requires unprecedented conversion efficiency or additional electrical amplification.

As shown in Fig. 2.3, several optical modulators with different modulation mechanisms, including the carrier plasma dispersion effect in silicon [10], the electric-optic Pockels ef-

fect in barium titanate [11] and in lithium niobate [9], the DC Kerr effect in silicon [12], the electro-absorption effect in graphene [13] and in InP-on-Si quantum well [14], and the magneto-optic effect in garnet [15], have been proposed and demonstrated at the cryogenic temperature. Furthermore, a cryogenic vertical-cavity surface-emitting laser (VCSEL) has also been demonstrated at 4 K recently [16]. However, these EO interfaces require either a large voltage swing (tens of millivolts to a few volts [10, 11, 14, 16]) or a large current swing ($\pm$110 mA [15]) to operate.

As a result, additional discrete cryogenic amplifiers are needed for signal amplification and impedance match when interfacing with superconductor electronics, which limits the bandwidth density and energy efficiency of the system and eventually impedes system scalability [5]. Besides that, the existing work focuses on a single device and lacks the analysis of performance and energy efficiency at the system level.

2.5 Proposed monolithic electronic-photonic cryogenic egress link

In this work, we leverage the integration of electronics and photonics in a monolithic CMOS photonic platform to implement a single-chip optical interface connecting the SCE IC to room-temperature memory.

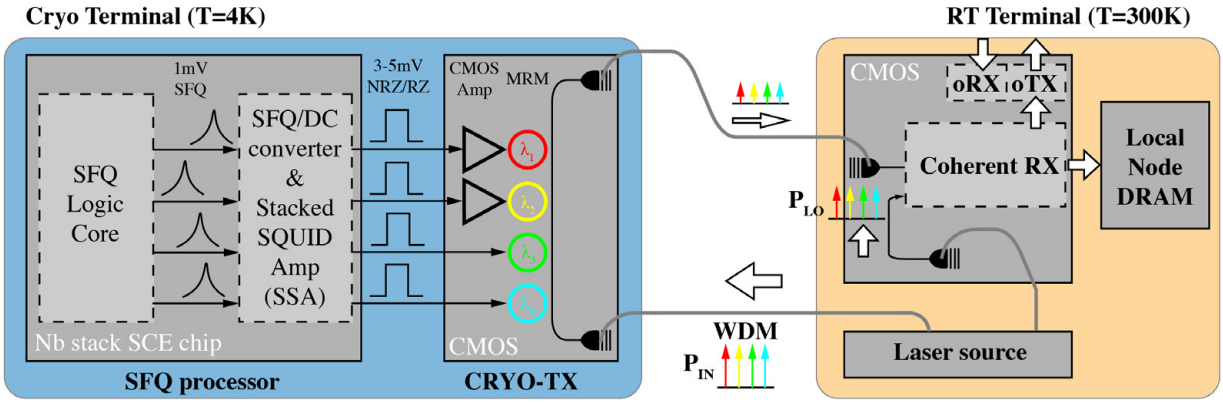


Figure 2.4: Proposed electronic-photonic egress link connecting cryo compute node with its RT main memory.

As shown in Fig. 2.4, SFQ voltage pulses from the Logic Core go to the SFQ/DC converter and SQUID stack amplifier (SSA) [21] that output millivolt-level Non-Return-to-Zero (NRZ) pulses for transmission to the CRYO-TX chip, where the NRZ signals are amplified by a low-noise CMOS amplifier, the output of which drives a micro-ring modulator (MRM) on the same chip. Less than 10μm distance between transistors and photonic components makes

parasitic capacitance negligible and thus significantly improves energy efficiency. The MRMs resonating at different wavelengths are cascaded on a single bus waveguide to implement multi-channel wavelength-division multiplexing (WDM) transmission.

We utilize this transmitter and the coherent receiver to create a new, laser-forwarded coherent link that reduces the energy dissipated in the cryo environment, thereby optimizing the overall link energy consumption.

Chapter 3

Electronic-photonic Co-Optimization of the Cryogenic Egress Link

In this chapter, the author first introduces the architecture of the laser-forwarded coherent link which is employed in the cryogenic egress link, and compares it with the traditional coherent link. Following that, the key device in this optical link, the micro-ring modulator, is detailed. Next, the cryogenic egress link is divided into several blocks and modeled separately. Finally, the system simulation result based on the link model is presented to guide the chip design.

3.1 Laser-forwarded Coherent Link

Coherent detection is a technique for realizing high-capacity transmission owing to its excellent spectral efficiency, and it has been widely used in long-haul optical systems [22, 23]. In these optical transmission systems, like metro area networks, analog-to-digital converters (ADCs) and digital signal processing (DSP) are heavily used to compensate for the impairments of optical fiber over long-range transmission, leading to massive power consumption.

Nowadays, data center (DC) traffic contributes the majority of global internet protocol traffic, and nearly 77% of the overall DC traffic stays inside the local network of the source DC [24]. It is produced from storage, production, development, and authentication of DC data and transmitted over distances ranging from 500m to 10km. Since the fiber impairments in these short-reach links are insignificant, the low-power DSP-free coherent-lite link has gained increasing interest as a promising alternative solution [24–29].

Because the requirement of equalization capability is relaxed, carrier phase recovery (CPR) becomes a critical issue that needs to be resolved in these analog signal-based coherent receivers. The architecture of analog signal-based CPR can be divided into two categories: Optical PLL (OPLL) and Electrical PLL (EPLL) [26]. In an OPLL, since the LO laser is frequency-modulated by the frequency correction signal, it requires an LO laser with a wideband frequency modulation response and short propagation delay along the en-

tire optical and electrical path in the feedback loop, which is usually limited by the ability to integrate photonic components (especially laser) closely with the electronic part. On the other hand, the EPLL uses a single sideband (SSB) mixer in each polarization to de-rotate the incoming signals since the transmitter and LO lasers are not phase-locked. The EPLL demonstrated in recent literature [28, 29] suffers from limited phase tracking bandwidth. It also requires high-quality tunable lasers with narrow linewidth for lower phase noise. The above drawbacks degrade phase recovery capabilities and prevent usage.

Another type of coherent-lite link employs laser-forwarded link architecture [24, 30–33], which forwards the unmodulated laser light directly to the receiver and thus implements self-homodyne detection. Since the signal and reference are derived from the same laser source, phase recovery can be eliminated as long as the two signals are synchronized within the coherence time of phase noise. Therefore, this architecture has also been gaining much attention recently since it further simplifies the issue of CPR and reduces power. The downside of this architecture is the requirement of extra fiber to propagate LO light to the receiver, which reduces the overall throughput of this optical communication system. However, the cost of extra fiber can be amortized in the dense wavelength-divison multiplexing (DWDM) link, where multiple LO light at different wavelengths can be carried on a single fiber.

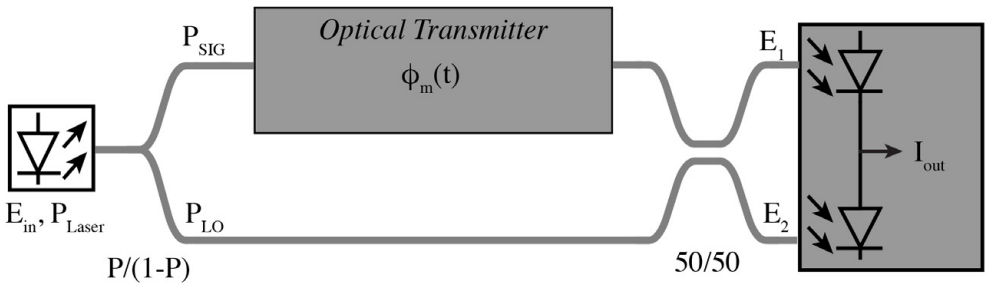


Figure 3.1: Typical architecture of the phase-modulated laser-forwarded coherent link.

The typical schematic of phase-modulated laser-forwarded coherent is shown in Fig. 3.1, where the light from continuous wave (CW) laser is first split into signal light with $P_{sig} = P \times P_{laser}$ and LO light with $P_{LO} = (1-P) \times P_{laser}$. The optical transmitter modulates the signal path with phase modulation of $\phi_m(t)$. After beating with the LO light, the electrical field at the output of the ideal 50/50 coupler can be written as:

$$\begin{bmatrix} \vec{E}_1 \\ \vec{E}_2 \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} \sqrt{P}\vec{E}_{in} e^{j[\phi_m(t)+\phi_1]} \\ \sqrt{1-P}\vec{E}_{in} e^{j\phi_2} \end{bmatrix} \tag{3.1}$$

where ϕ_1 and ϕ_2 are the static optical delay at two paths. The optical power that hits the balanced photodetector is:

$$\begin{bmatrix} P_1 \\ P_2 \end{bmatrix} = \begin{bmatrix} |\vec{E}_1|^2 \\ |\vec{E}_2|^2 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} P_{laser} + 2\sqrt{P(1-P)} \times P_{laser} \times \cos[\phi_m(t) - \Delta\phi] \\ P_{laser} - 2\sqrt{P(1-P)} \times P_{laser} \times \cos[\phi_m(t) - \Delta\phi] \end{bmatrix} \tag{3.2}$$

where $\Delta\phi = \phi_1 - \phi_2$ is the optical delay difference between two arms. It's not hard to find the output optical power contains two terms: DC power $P_{laser}/2$ and the data-dependent term $\pm\sqrt{P(1-P)}P_{laser}\cos[\phi_m(t) - \Delta\phi]$. Therefore, the final photocurrent can be driven as follows:

$$I_{out} = R(P_1) - R(P_2) = 2R\sqrt{P(1-P)} \times P_{laser} \times \cos[\phi_m(t) - \Delta\phi] \tag{3.3}$$

where R is the responsivity of the photodetector.

As we can observe from the above equation, the final current only contains the phase information encoded at the transmitter. The maximum achievable signal current is $I_{out,pp} = 2R \times P_{laser}$ when power splitting ratio $P = 1/2$, phase modulation $\phi_m(t) \in [0, \pi]$, and $\Delta\phi = m \times \pi$, $m \in \mathbf{Z}$. As a reference, the maximum achievable signal current in an intensity-modulation direct detection (IMDD) scheme is $I_{out,pp} = R \times P_{laser}$ when the extinction ratio of the optical transmitter is large enough. Another benefit of the laser-forward coherent link is that a big portion of the light can bypass the transmitter path with a huge insertion loss and eventually increase the signal-to-noise ratio by several dB [30]. This benefit is further enhanced in cryogenic egress links due to the cooling penalty of the refrigerator, which will be discussed in the following sections.

3.2 Micro-ring Based Optical Modulator

Thanks to the success of silicon photonics, the silicon ring resonator can be made with an unprecedented small size, leading to incomparable drive efficiency and sensitivity. Therefore, it has been widely used in different areas, like the optical modulator in high-speed communication [34–38], sensor elements in bio system [39], and optical filters in communication and quantum system [40].

As shown in Fig. 3.2, a generic ring resonator consists of an optical waveguide looped back on itself, such that resonance occurs when the optical path length of the resonator is exactly a whole number of wavelengths. r and k are the self-coupling and cross-coupling coefficients of the waveguide coupler and satisfy $r^2 + k^2 = 1$, assuming no losses in the coupling section. $\phi = \beta L$ is the single-pass phase shift, with L the round trip length and β the propagation constant of light at the circulating mode. a is the single-pass amplitude transmission, including both propagation loss in the ring and the couplers. With all the above definitions, we can derive the transmission ratio between the output and input electrical field:

$$\frac{E_{out}}{E_{in}} = e^{j(\pi+\phi)} \frac{a - re^{-j\phi}}{1 - rae^{j\phi}} \tag{3.4}$$

By squaring the above equation, we can obtain the intensity transmission T of the ring resonator as:

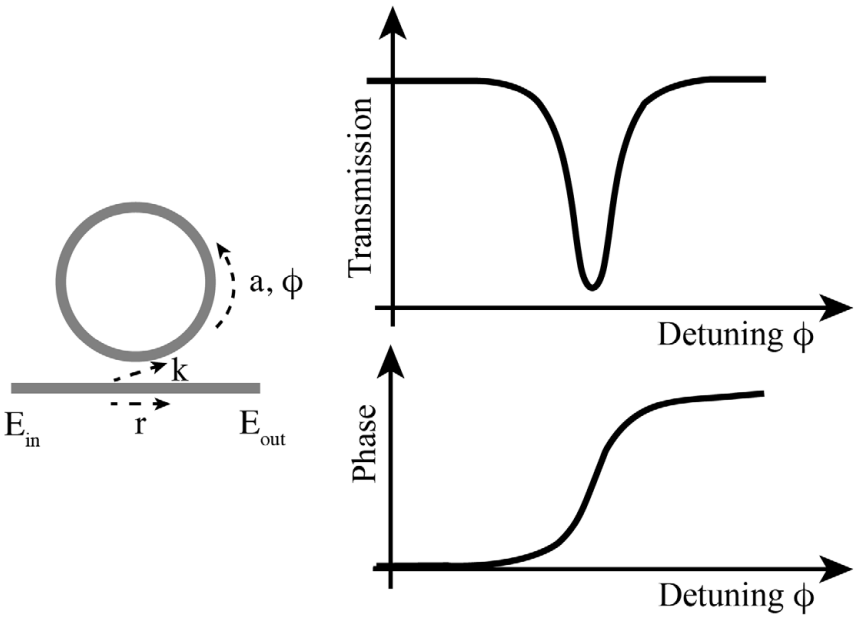


Figure 3.2: Microing Resonator: schematic (left) and response (right)

$$T = \frac{I_{out}}{I_{in}} = \frac{a^2 - 2ra\cos(\phi) + r^2}{1 - 2ra\cos(\phi) + (ra)^2} \tag{3.5}$$

As expected, when ϕ is a multiple of 2π, all energy resonances inside the cavity and transmission drop to 0 under the critical coupling ($a = r$). We can also calculate the effective phase shift ψ at the output port of the ring resonator:

$$\psi = \pi + \phi + \arctan\frac{r\sin\phi}{a - r\cos\phi} + \arctan\frac{ra\sin\phi}{1 - ra\cos\phi} \tag{3.6}$$

The intensity and phase response of the ring resonator is plotted on the right in Fig. 3.2. The shape of phase response depends on the relationship between a and r. When $r = a$ (critical coupling), the effective phase ψ abruptly shifts by π near the resonance wavelength, while for $r < a$ (over coupling) and $r > a$ (under coupling), the output electrical field shows a continuous positive and negative phase delay [41].

By changing the voltage applied on the PN junction around the waveguide, we can change the carrier concentration in the ring resonator and thus detune ϕ and convert the electrical drive signal to the optical domain. Therefore, the microring modulator (MRM) can be used as either an intensity or phase modulator. However, it should be noted that the nonlinearity of the free carrier effect and resonance response result in the nonlinear phase/intensity change in voltage, which makes voltage DAC necessary when using MRM in advanced modulation format [38, 42]. Furthermore, when MRM is used in quadrature phase shift key (QPSK),

the modulated field transits along an arc to the low-power level, leading to both frequency chirp and intensity dips [43]. But for binary phase shift key (BPSK), the effectiveness of MRM has been demonstrated [30, 34].

3.3 Link Model of the Cryogenic Egress Link

We can analyze the cryogenic optical link, including superconductor and semiconductor electronic/photonic parts operating at different temperatures, by breaking it into pieces and optimizing it at the system level.

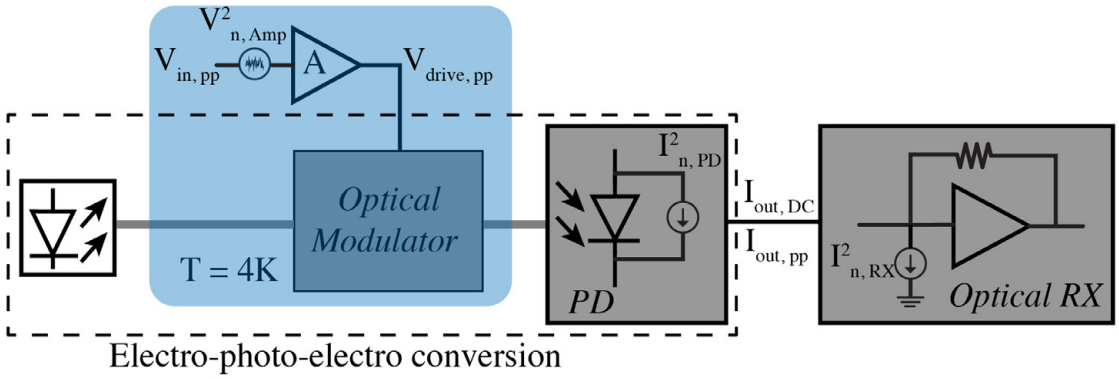


Figure 3.3: Abstraction of the cryogenic optical link.

As shown in Fig. 3.3, the voltage signal $V_{in,pp}$ from the superconductor IC is amplified by a cryogenic pre-amplifier with the gain of A. As an active circuit, the input-referred noise power of the amplifier is $V^2_{n,Amp}$. Next, the output voltage is applied to the optical modulator for optical modulation. The modulated optical light then transmits along the optical fiber and is converted back to the current signal by the photodetector. No matter the type of optical modulation, the electro-photo-electro conversion can be treated as a G_m stage that converts voltage signals to current as a function of laser power and other parameters of photonic components. The output of this G_m stage is DC and signal current, $I_{out,DC}$ and $I_{out,pp}$, which are used to calculate the shot noise of PD and the link SNR.

The following sections use the micro-ring modulators (MRM) for analysis.

Cryogenic Low-Noise Amplifier

Fig. 3.4 shows the simplified model of the cryogenic transmitter, where the 50Ω termination resistor R_{term} is employed for broadband impedance match, a CMOS amplifier is utilized to amplify the weak input signal, and a micro-ring modulator (MRM) is used electronic-photonic conversion. For simplicity, a common-source amplifier is chosen as the amplifier

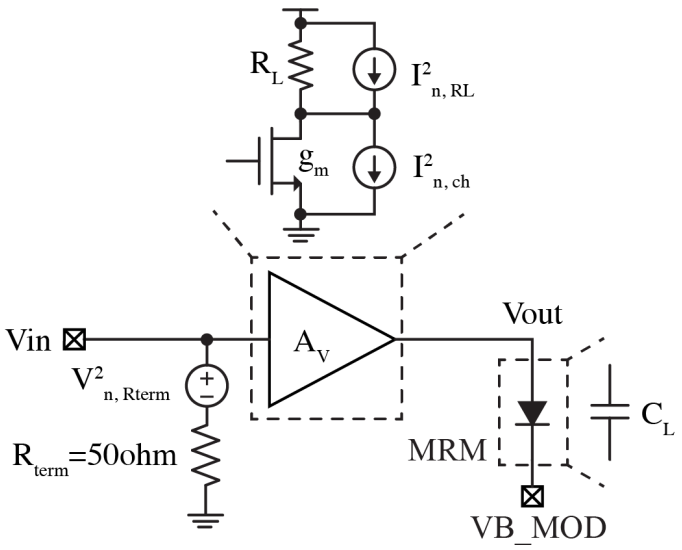


Figure 3.4: Noise model of the cryogenic optical transmitter.

block here for link analysis. The MRM, in which the PN diode operates at the reverse-biased region for high bandwidth, is modeled as a load capacitor C_L. All noise sources are also included in the same figure: voltage noise of the termination resistor $V^2_{n,R_{term}} = 4K_BTR_{term}$; current noise of the load resistor $I^2_{n,R_L} = 4K_BT/R_L$; the channel noise of transistor at cryogenic temperatures is dominated by shot noise with expression $I^2_{n,ch} = 2F_sqI_D$, rather than thermal noise [44]. The mid-band output noise power density can then be expressed as:

$$V^2_{n,out}(f)/\Delta f = 4K_BTR_{term} \times A_v^2 + (\frac{4K_BT}{R_L} + 2F_sqI_D) \times R_L^2 \tag{3.7}$$

Assuming the load resistor R_L is much smaller than the intrinsic resistor of the transistor, and the transistor is biased at the saturation region, then we can get the following equations: $A_V \approx g_mR_L$, $BW = 1/(R_LC_L)$, $GBW = A_v * BW = g_m/C_L$, and $g_m \approx \frac{2I_D}{V*}$, where $V*$ is the overdrive voltage of the transistor. Therefore, the input-referred integrated noise can be calculated with:

$$\begin{aligned}\overline{V^2_{n,in}} &= \frac{V^2_{n,out}(f) * BW}{A_v^2} \\ &= 4K_BTR_{term} \times BW + \frac{BW}{g_m}(\frac{4K_BT}{A_v} + 2F_sq\frac{I_D}{g_m}) \\ &= 4K_BTR_{term} \times BW + \frac{1}{A_vC_L}(\frac{4K_BT}{A_v} + F_sqV*)\end{aligned} \tag{3.8}$$

At the power consumption of:

$$P_{amp} = VDD \times I_D = \frac{VDD \times GBW \times C_L \times V*}{2} \tag{3.9}$$

Assuming the required bandwidth is a fraction of the data rate ($BW = 0.75 f_b$) for ISI-free communication and the output voltage swing of SCE IC is $4mV_{pp}$, and picking $200mV$ and $30fF$ for $V*$ and C_L, we can plot the integrated noise power and the corresponding signal-to-noise ratio (SNR) as the function of data rate. As shown in Fig. 3.5, the channel shot noise is the dominant noise source among a large range of data rates and gain because the thermal noise significantly decreases with the reduced temperature. Another observation is that reducing the overdrive voltage can further improve the noise. But even with the current low-gain ($A_v = 10$) and strong-inversion ($V_{ov} = 200mV$) bias configuration, the calculated SNR ($16.7dB$) is still larger than the SNR ($13.9dB$) required for achieving the BER of $1e-12$ for the link using NRZ code, which the following equation can derive:

$$BER = \frac{1}{2} erfc(\frac{V_{in,pp}}{2\sqrt{2} \times \overline{V_{n,in}}}) = \frac{1}{2} erfc(10^{SNR/20}) \tag{3.10}$$

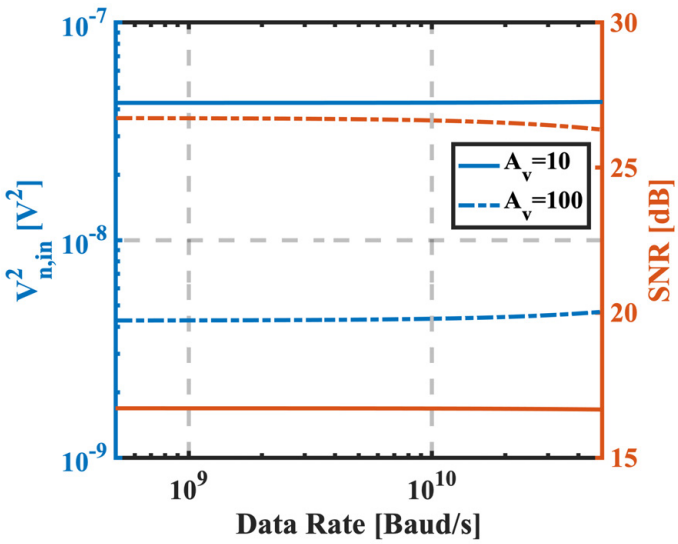


Figure 3.5: Noise and SNR of cryogenic amplifier with T=4K.

Electro-Photo-Electro conversion

In terms of optical modulation, we consider two different types of micro-ring modulator(MRM)-based optical links: Intensity Modulation and Direct Detection (IMDD) and Phase Modulation Laser-forwarded coherent Link (LF). As shown on the top of Fig. 3.6, the voltage

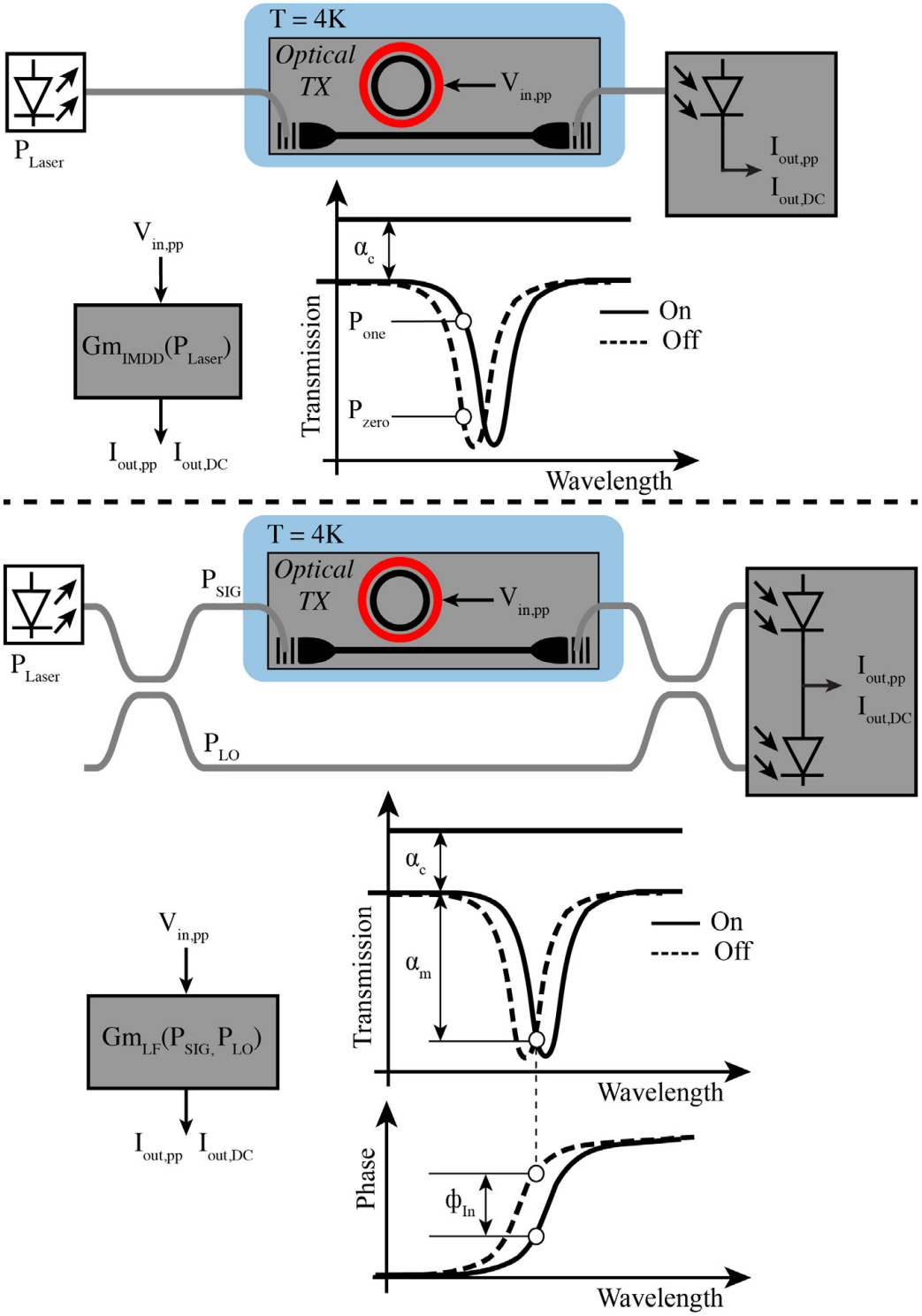


Figure 3.6: Model of the EOE conversion: Intensity Modulation and Direction Detection (IMDD) (top) and Phase-Modulated Laser-Forwarded Coherent Link (bottom).

difference between bit zero and one induces the change of the waveguide's refractive index, alternating the resonance wavelength of MRM, and thus generating different optical power P_{zero} and P_{one}. Therefore, for a given drive voltage, there is always a bias point that can maximize the optical modulated amplitude (OMA). We can list the key equations from the IMDD link as follows:

$$I_{out,DC} = R(P_{one} + P_{zero})/2 \tag{3.11}$$

$$I_{out,pp} = R(P_{one} - P_{zero}) \tag{3.12}$$

$$I^2_{n,PD} = 2qI_{out,DC} \times BW = qR(P_{one} + P_{zero}) \times BW \tag{3.13}$$

$$P_{loss\_at\_4K} = P_{laser} - (P_{one} + P_{zero})/2 \tag{3.14}$$

where R is the responsivity of PD, $I^2_{n,PD}$ is the shot noise power of PD, and $P_{loss\_at\_4K}$ is the light lost in the 4K environment due to different loss mechanism, which loads the refrigerator and impacts overall energy efficiency.

On the other hand, as discussed in section 3.1, the P_{LO} in the laser-forwarded coherent link (shown at the bottom of Fig. 3.6) can bypass the insertion loss in the transmitter, reducing the light lost in the 4K environment and thus improving the link efficiency. Similarly, we can drive the key equations from LF configuration:

$$I_{out,DC} = \frac{R}{2}(\alpha_c \alpha_m P_{sig} + P_{LO}) \tag{3.15}$$

$$I_{out,pp} = 2R\sqrt{\alpha_c \alpha_m P_{sig} P_{LO}}[\cos(\phi_{in} + \phi_0) - \cos(\phi_0)] \tag{3.16}$$

$$I^2_{n,PD} = 2qI_{out,DC} \times BW \times 2 = R(\alpha_c \alpha_m P_{sig} + P_{LO}) \times BW \times 2 \tag{3.17}$$

$$P_{loss\_at\_4K} = P_{sig}(1 - \alpha_c \alpha_m) \tag{3.18}$$

where α_c and α_m are coupling loss and insertion loss of the modulator, ϕ_{in} is the effective phase delay induced by the applied voltage, and ϕ_0 is the static phase difference between signal and LO lights. For a given ϕ_{in}, the signal current can be maximized by tuning ϕ_0.

Room-Temperature optical receiver

A typical analog front-end (AFE) architecture of the optical receiver, resistor feedback TIA, is shown in Fig. 3.7. This kind of TIA is widely used in current high-speed receiver designs. The author uses this circuit to discuss the trade-off between noise, performance, and power for the system design. Assuming the input pole is the dominant pole of the TIA, then the simplified noise model is shown in the same figure, in which the gate-drain capacitor (C_{gd}) and load capacitor are ignored for simplicity. The input impedance of the TIA itself can be expressed as:

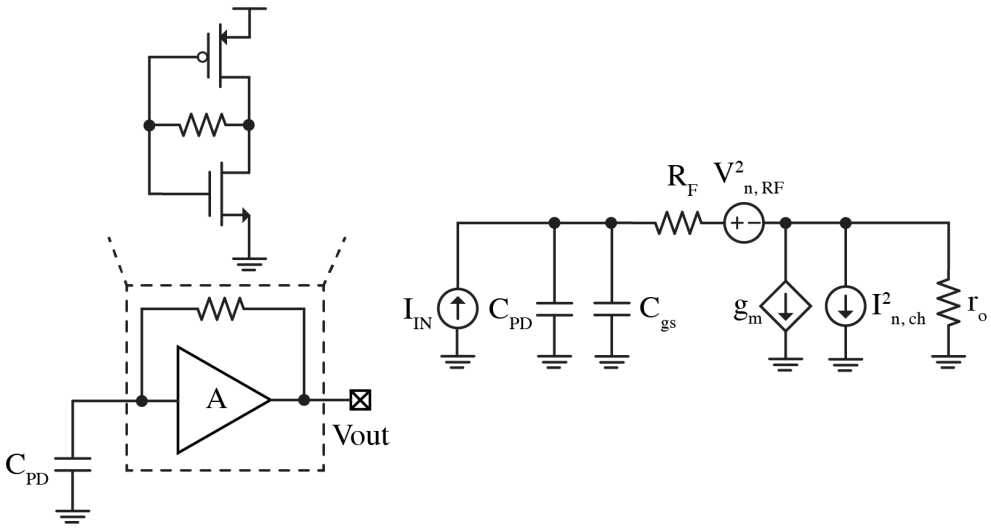


Figure 3.7: Noise model of the optical receiver.

$$\begin{aligned} Z_{in} &= \frac{R_F + r_o}{1 + g_m r_o} \\ &\approx \frac{R_F}{g_m r_o} + \frac{1}{g_m} \end{aligned} \tag{3.19}$$

Depending on the data rate and transistor process, the feedback resistor (R_F) could be much smaller than the intrinsic resistor (r_o) of transistors or comparable with r_o. Therefore, the 1st term in eq. 3.19 can not be simply ignored, and the $3dB$ bandwidth can be derived as

$$f_{BW} = \frac{1}{2\pi(C_{gs} + C_{PD})Z_{in}} \tag{3.20}$$

where C_{PD} is the capacitance of the photodetector (PD). According to the PDK model, between two terminals of the detector, there is a capacitance composed of the junction capacitance and a metal fringe capacitance. The metal fringe capacitance, calculated from the geometry of the metal fingers, is about 0.7fF. When PD is biased with -1V, the depletion width is about 0.7um for the detector with 0.7um width of the intrinsic width, resulting in a capacitance of approximately 10fF. Given that the depletion width of the PIN junction is dominated by the intrinsic width and relatively independent of the bias condition, we pick 10fF and 20fF capacitance values for single PD and balanced PD, respectively. Therefore, unlike typical optical receivers, in which C_{PD} dominates, the input gate-source capacitance (C_{gs}) can be easily comparable or larger than C_{PD} in the monolithic silicon-photonic process.

At the same time, the input-refer noise density of the above circuit can be expressed as:

$$\begin{aligned} i_n^2(f) &= i_{n,R_F}^2(f) + i_{n,ch}^2(f) \\ &= \frac{4K_BT}{R_F} + \frac{4K_BT\gamma}{g_m R_F^2}|1 + sR_F(C_{PD} + C_{gs})|^2 \\ &= \frac{4K_BT}{R_F} + \frac{4K_BT\gamma}{g_m R_F^2} + \frac{4K_BT\gamma}{g_m} \times [2\pi f(C_{PD} + C_{gs})]^2 \end{aligned} \tag{3.21}$$

Looking at the above noise equation, it's not hard to find that the noise density is inversely proportional to R_F. So, one basic design choice is maximizing the R_F until the bandwidth requirement can not be met.

3.4 Energy Efficiency Optimization of the Cryogenic Egress Link

By aggregating the model of components mentioned above, we can build a link model of cryogenic optical links. The first step is to fit the measurement result [45] to the analytical model. As shown in Fig. 3.8, there is a good agreement between measured and fitted response, making our system simulation strongly correlated to the silicon data.

With the matched device model, we can predict the behavior of the modulator and evaluate the system performance. Assuming the laser power is 5dBm, and the end-to-end coupling loss on the transmitter chip is 8dB, we can plot the SNR of two different link architectures as a function of the voltage applied to the modulator, shown in Fig. 3.9. For both architectures, the lower the amplifier gain, the worse the noise figure and the worse the SNR. Compared to the IMDD scheme, the laser-forwarded architecture shows a 3 to 4 dB boost in SNR because the LO path bypassed the lossy transmitter.

Besides the SNR, which is calculated by signal and noise current, the energy efficiency of the whole link is another key metric of the figure we care about. The power consumed by different components in the link can be categorized into two parts.

- Power consumed at room temperature, including the power consumed by laser, room-temperature optical receiver: $P_{RT} = P_{laser,WPE} + P_{RX}$.
- Power consumed at cryogenic temperature (4K in our case), including the power consumed by the cryogenic amplifier, and light lost in the cryogenic station: $P_{4K} = P_{amp} + P_{loss\_at\_4K}$.

When combining two parts to calculate the total power consumed at room temperature, the cooling penalty of the refrigerator needs to be considered:

$$\begin{aligned} P_{Total} &= P_{RT} + P_s \times P_{4K} \\ &= \frac{P_{laser}}{\eta_{laser}} + P_{RX} + P_s \times (P_{amp} + P_{loss\_at\_4K}) \end{aligned} \tag{3.22}$$

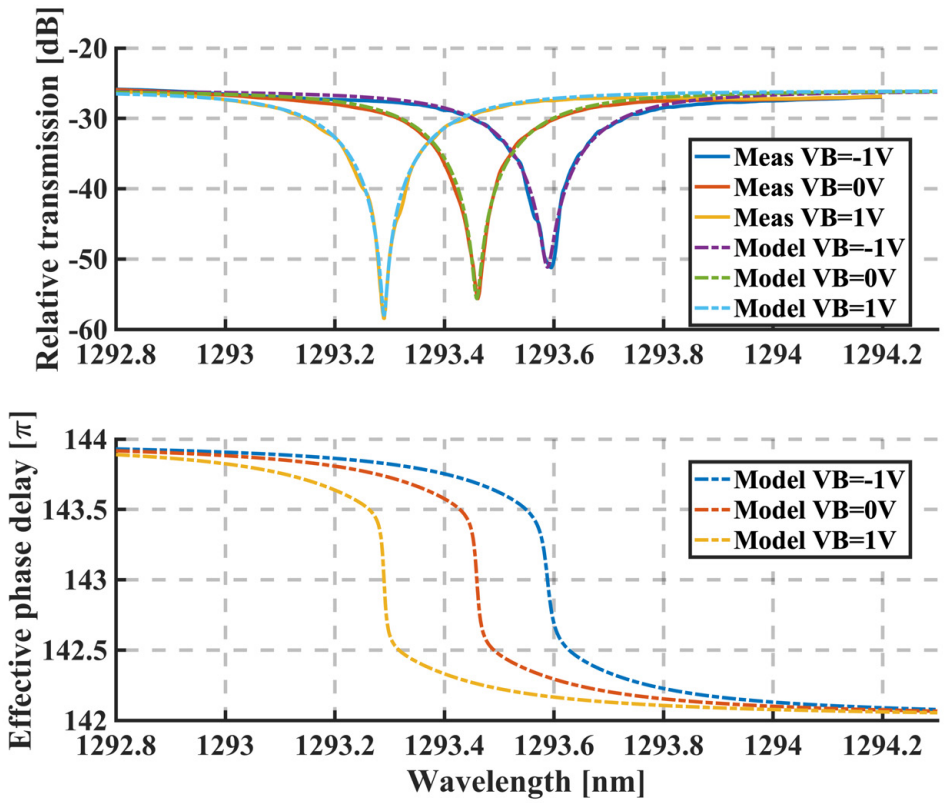


Figure 3.8: Measued and fitted response of micro-ring modulator.

where P_{laser} is the optical power of the laser, $\eta_{laser} = 10\%$ is the wall-plug efficiency of the laser [46], $P_s = 500W/W$ [4] is the specific power of 4K refrigerator introduced in section 2.1. For the purpose of analysis, the energy efficiency of the room temperature coherent receiver is assumed to be 0.95pJ/bit [30]. The overall link energy efficiency referenced to 4K environment can be expressed as:

$$EE_{4K} = \frac{P_{total}}{f_b \times P_s} \tag{3.23}$$

where fb is the link data rate and is equal to 20Gbps.

As discussed in section 3.3, to achieve less than 1e-12 BER, the SNR needs to be larger than 14dB. With this constraint, we can plot the breakdown of energy efficiency as the function of drive voltage, shown in Fig. 3.10, which gives us a clear trade-off in this cryogenic optical link:

- At low drive voltage, the total energy of the link is dominated by the optical loss at 4K environment. This happens because the small drive voltage causes weak modulation,

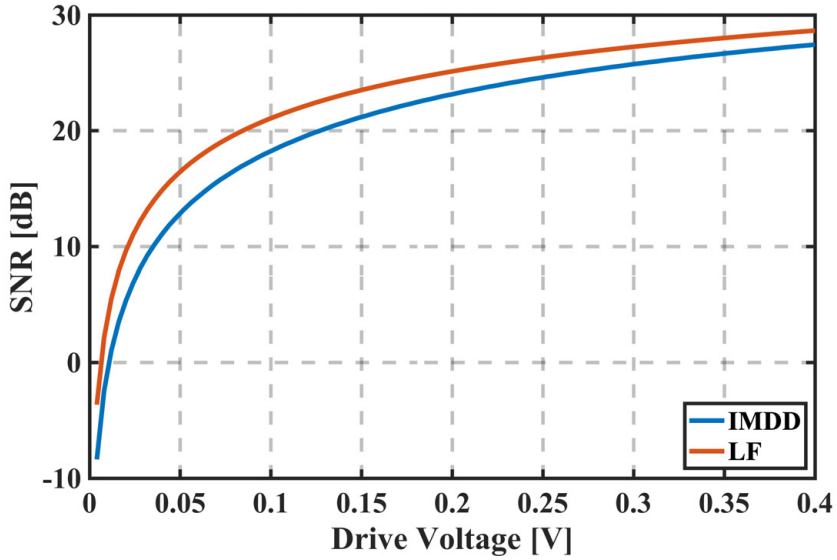


Figure 3.9: Simulated SNR of IMDD and Coherent link under the 5dBm laser power, 20Gbps data rate, and 8dB end-to-end coupling loss in transmitter.

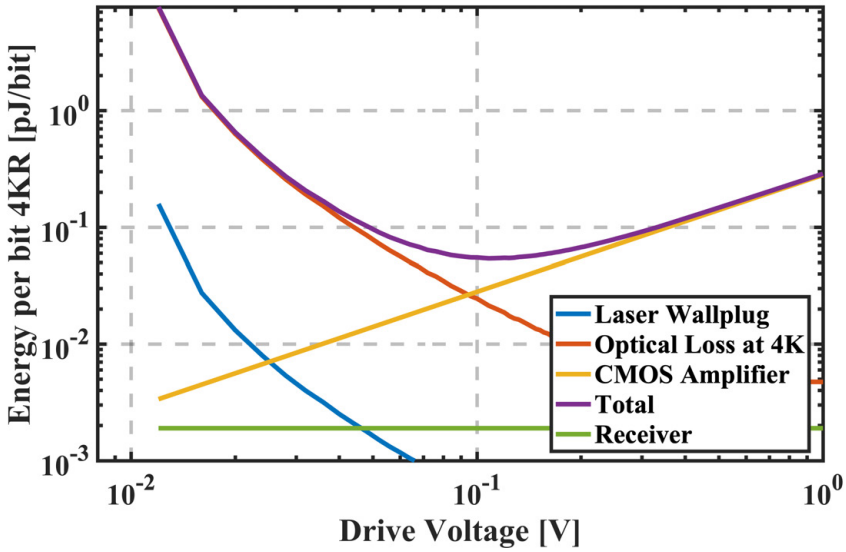


Figure 3.10: Energy efficiency breakdown of laser-forwarded coherent link operating at 20Gbps with >14dB SNR.

requiring high optical power at the receiver to meet the target BER. Even if only a small portion of the laser power goes into cryostat, that can dominate the whole link energy. With the help of the CMOS amplifier, the required laser power is significantly reduced due to the improved modulation depth.

- At high drive voltage, the power consumption of the pre-amplifier itself could dominate the system. As a result, the overall link efficiency is minimized around 100mV point.

Chapter 4

Characteristics of MOSFET at cryogenic temperatures

Nowadays, very-large-scale integration (VLSI) semiconductor chip design heavily relies on the compact device model provided by the chip foundry to predict the function and performance. However, these industry compact device models, like the BSIM family and EKV, do not scale properly with temperature and thus cannot accurately capture the electric behavior of CMOS devices at cryogenic temperatures ($\leq 50K$). In this Chapter, we first introduce the fundamental behavior of MOSFET at cryogenic temperature, then present the characterization results of MOSFET from two monolithic silicon photonic processes, enabling the analog and mixed-signal circuit design in the cryogenic electro-optic system.

4.1 Fundamental behavior of MOSFET at cryogenic temperatures

Threshold voltage (V_{TH})

The accurate model of the transistor's threshold voltage plays a crucial role in technology optimization and circuit design. For instance, in low-power circuit design, the transistor is usually biased closely to the threshold voltage to maximize transconductance efficiency (g_m/I_D). In that case, a small misc-prediction of V_{TH} could lead to orders of magnitude difference in the drain current. The major temperature dependency terms of V_{TH} are following two parts [47]:

Bandgap Widening and scaling of Fermi-Dirac Occupation Function. With the decreasing temperature from 298K to 4.2K, the Si bandgap increases from 1.12 to 1.17eV. The Fermi-Dirac occupation function scales exponentially, approaching a step function at 4K. Therefore, more band bending is required to generate sufficient overlap between the Fermi-Dirac occupation function and the density-of-states in the conduction band, increasing the threshold.

Intrinsic Carrier-Density scaling. Since the Boltzmann statistics are still valid at the cryogenic temperatures, the intrinsic carrier density (n_i) of the semiconductor can be expressed as:

$$n_i = \sqrt{N_C N_V} e^{-E_g/2kT} \tag{4.1}$$

where N_C and N_V are the effective density of states of the conduction and valence band. The exponential dependency on $-E_g/T$ leads to a significant decrease in n_i and thus increases the inversion threshold $V_{TH} = 2\Phi_F$.

Besides the above two major factors, the incomplete ionization or freezeout of the substrate makes the threshold $2\Phi_F - \Delta\Phi$, where $\Delta\Phi$ is dependent on temperature and doping and at the range of few mV. On the other hand, the process of field-assisted dopant ionization is negligible at the inversion threshold.

Subthreshold swing (SS)

As is well known, the current flow of the MOSFET increases exponentially for voltages below the threshold voltage, like a lateral bipolar junction transistor. The current-voltage characteristic of the MOSFET in this region is usually defined as subthreshold swing (SS):

$$SS = n \times ln(10) \times KT/q \tag{4.2}$$

where the slope factor ($n = 1 + C_{dep}/C_{ox}$) can be extracted with the SS measured at room temperature. However, the cryogenic characterization of SS in advanced CMOS devices reveals at least one order of magnitude larger values at 4K compared with the expected value given by Eq. 4.2 in different technologies [48–52], including both bulk and SOI CMOS processes.

It has been demonstrated by numerical simulation that this general saturation of SS at deep-cryogenic temperatures is caused by exponential band tail and Fermi-Dirac statistics. More specifically, when thermal energy becomes smaller than the band-tail extension (W_t), the SS(T) limit follows the temperature-independent $n(W_t/q)$ rather than $n(KT/q)ln10$ [53]. This also means that a perfect MOS switch with $SS = 0$ cannot be obtained in the presence of a band tail.

Mobility (μ)

The carrier mobility can be determined as the inverse of the sum of the scattering rates corresponding to all relevant scattering modes. There are two main imperfections in the crystal that cause carrier collision or scattering: phonon scattering and ionized impurity scattering. Phonon, particle representation of the vibration of the atoms in the crystal, distorts the periodic crystal structure and thus scatters the electron [54]. The mobility contributed by phonon is:

$$\mu_{phonon} \propto \tau_{ph} \propto \frac{1}{\text{phonon density} \times \text{carrier thermal velocity}} \propto T^{-3/2} \tag{4.3}$$

So, the phonon scattering mobility increases when temperature decreases. While for impurity scattering, in which the dopant ions are fixed charge in the crystal and make electrons and holes change the direction of motion through the coulomb force, its mobility can be expressed as:

$$\mu_{impurity} \propto \frac{T^{3/2}}{N_a + N_d} \tag{4.4}$$

where N_a and N_d are the dopant concentrations of the acceptor and donors in the semiconductor material. Therefore, the total mobility can be written as:

$$\frac{1}{\mu} = \frac{1}{\mu_{phonon}} + \frac{1}{\mu_{impority}} \tag{4.5}$$

As we can observe from the above equation, at small dopant concentrations, μ decreases with increasing T, indicative of the dominance of phonon scattering. At very high dopant concentrations and low temperatures where impurity scattering is expected to dominate, μ indeed increases with increasing T. Due to the incomplete ionization of dopants at deep-cryogenic temperatures, the overall mobility increases with decreasing temperature.

4.2 Characterization of MOSFET in monolithic silicon-photonic process

Electronic-photonic integrated circuits offer an opportunity to dramatically improve the reliability, density, and power efficiency of cryogenic interconnection solutions [55, 56]. So far, in literature, devices from several different technologies, 0.16um, 40nm [48], 28nm bulk CMOS [49, 50], 28nm FD-SOI [51], and 16nnm FinFET [52] have been measured and analyzed. However, little is known about the impact of deep cryogenic temperatures on the transistor behavior in processes suited for electronic-photonic integration. 45RFSOI process, a Silicon Photonics platform [57] that is well positioned for these cryogenic applications, has only been characterized at cryogenic temperatures for digital applications [58]. 45SPCLO process, a 45nm CMOS-Silicon Photonic 300mm high-volume manufacturing platform developed by GlobalFoundaries for next-generation, low power, and high-speed optical interconnects [59], has not been previously characterized at cryogenic temperatures.

In this section, we present transistors' measured DC, delay, and noise characteristics in these two monolithic Silicon Photonic processes to enable analog and mixed-signal design in these processes for operation at cryogenic temperatures.

DC characterization

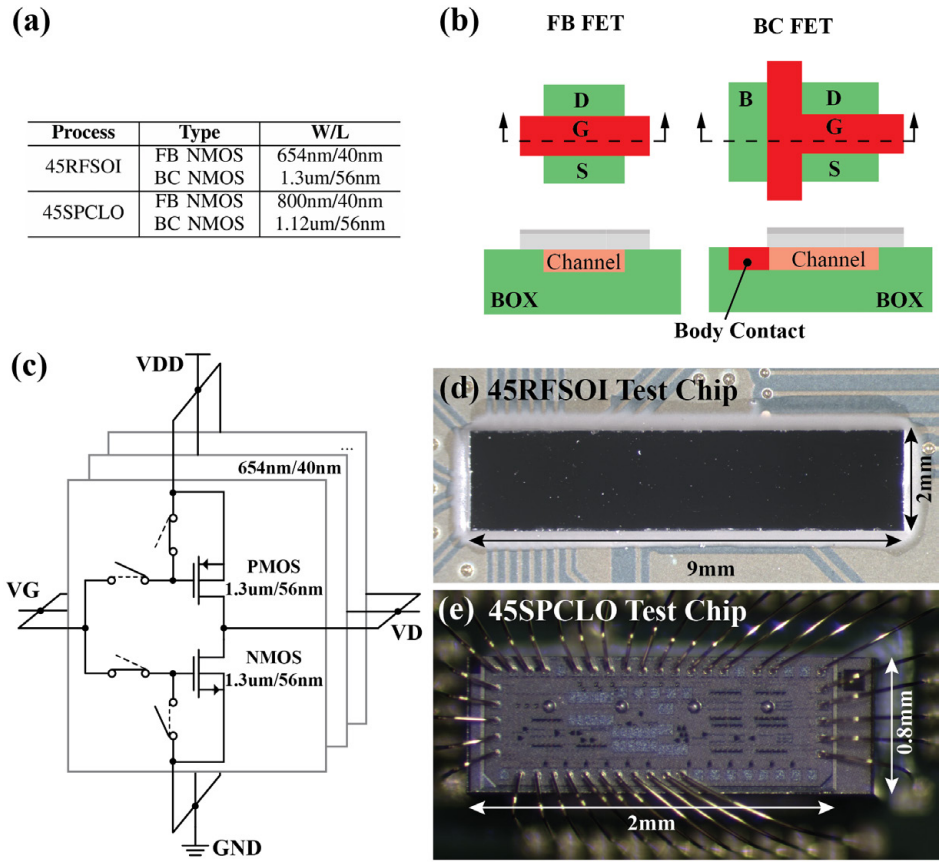


Figure 4.1: (a) Device table, (b) Comparison between FB and BC FET, (c) Test circuit used for device characterization, Micrograph of the (d) 45RFSOI and (e) 45SPCLO test chip.

Figure 4.1(a) summarizes the tested devices with different types and dimensions. Different types of transistors from the same chip were characterized for each process. Among them, the floating-body (FB) and the body-contacted (BC) are two available types of MOSFETs in these commercial PD-SOI processes. With the help of the body contact shown in Fig. 4.1(b), the BC FETs have better control over DC operation points and thus are widely used in analog and mixed-signal circuits, while the FB FETs gain the greatest speed benefits from the SOI process by minimizing parasitics. Figure 4.1(c) presents the circuit used for IV characterization, in which the gate and drain nodes of these transistors are shared and enabled through the switch and scan chain. As shown in Fig. 4.1(d) and (e), the 45RFSOI test chip is flip-chip attached to the printed circuit board (PCB), while the 45SPCLO test chip is wire-bonded to the PCB. In both cases, the thermal-conductive epoxy is used for die attach, and the bottom layer of the PCB is poured with copper before being directly

mounted on the cold plate to ensure good thermal conduction. The measured I-V plots of all transistors under temperatures from 300 K down to 2.5 K are shown in Fig. 4.2.

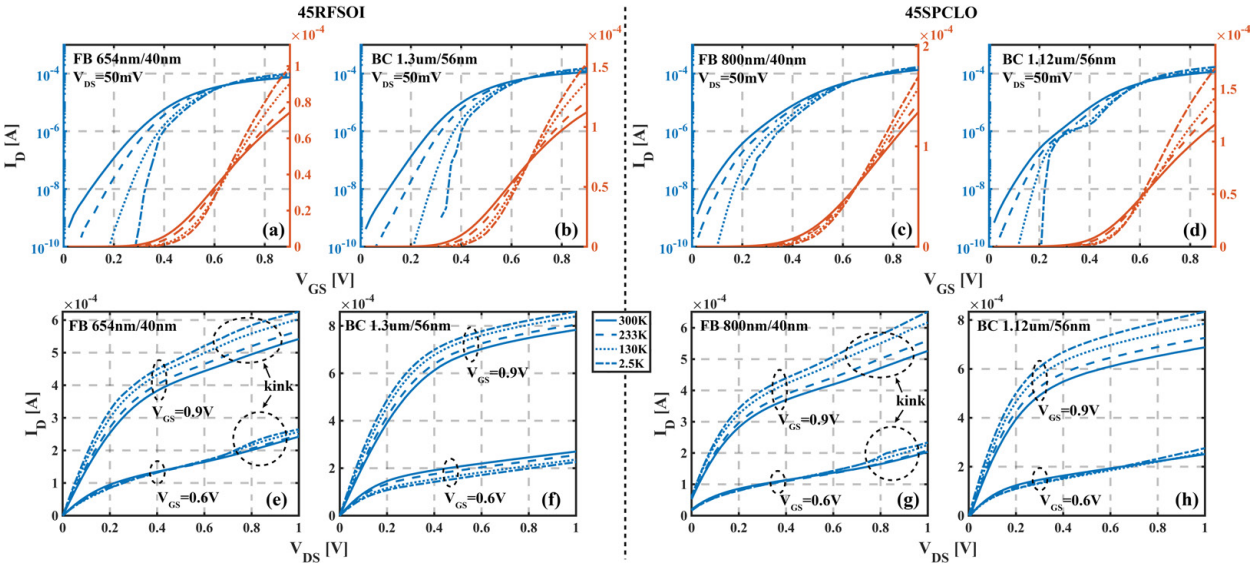


Figure 4.2: (a-d) I_D vs. V_{GS} of transistors operating in the linear region (V_{DS}=50mV) in both log (left) and linear (right) scale; (e-h) I_D vs. V_{DS} of transistors operating in both weak (V_{GS}=0.6V) and strong (V_{GS}=0.9V) inversion regime.

Subthreshold Swing (SS) and Transconductance (g_m)

For both processes, the measured SS of the BC FETs, shown in Fig. 4.3(a, b), start to deviate from the thermionic limit (Eq. 4.2) at ∼50 K and eventually saturate to ∼7 mV/dec, which is far away from the theoretical value of 0.5 mV/dec at 2.5 K. A theory of a disorder-induced tail in the density of state at the conduction band edge has been proposed recently to explain this saturation of the SS at deep cryogenic temperatures [53, 60].

The transconductance (g_m) and transconductance efficiency (g_m/I_D), derived from the measured data, are shown in Fig. 4.3(c, d). For the same bias current, the peak g_m increases by ∼ 25% at the cryogenic temperature due to the rise of mobility when operating at the saturation region. Owing to the reduced SS, the transconductance efficiency at low temperatures is several times higher than the room temperature value when working in the subthreshold region, making it suitable for low-power circuit design.

Threshold Voltage (V_{TH}) and Carrier Mobility (μ_{eff})

Another well-known phenomenon of MOSFET at cryogenic temperature is the increase of V_{TH} caused by the carrier freeze-out effect. Fermi-Dirac scaling and bandgap widening

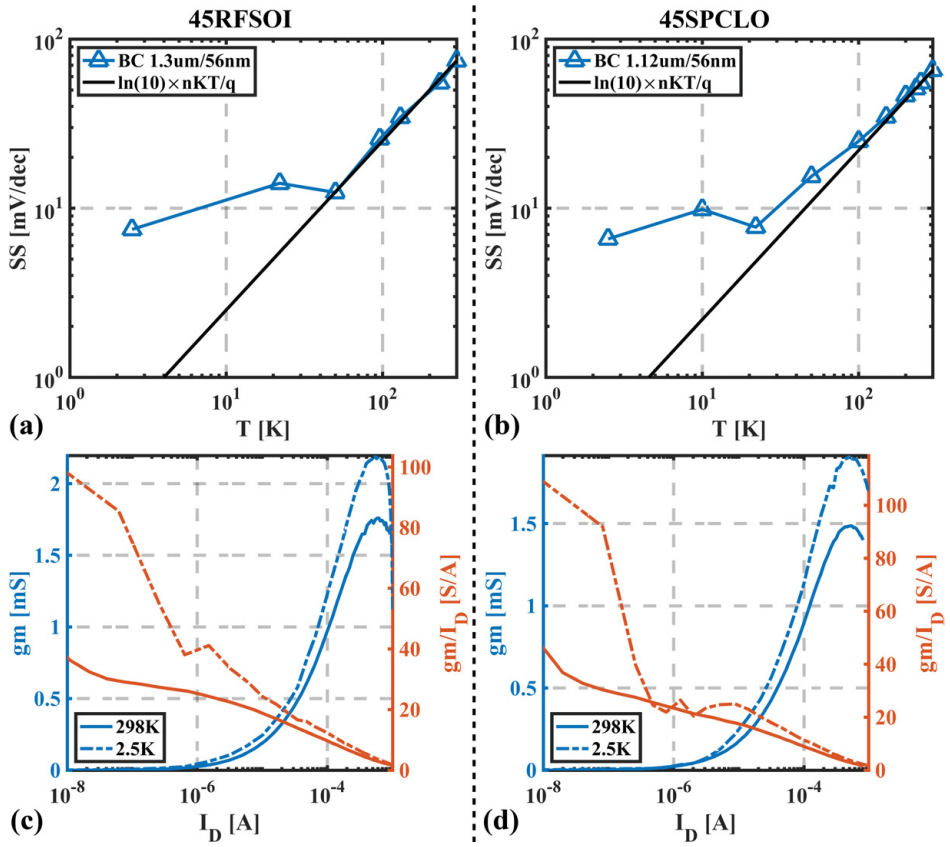


Figure 4.3: (a, b) SS of the BC NMOS transistors with V_{DS} of 0.05V versus temperature, (c, d) g_m and g_m/I_D of the BC NMOS transistors with V_{DS} of 0.95V versus I_D.

lead to a strong decrease in intrinsic carrier density and thus an increase in the inversion threshold [49]. The V_{TH} of FB and BC FETs operating in both linear and saturation regions are extracted from Fig. 4.2(a-d) with the linear extrapolation method [61] and shown in Fig. 4.4(a, e). As expected, V_{TH} increases with temperature decrease and eventually saturates. The V_{TH} at $2.5K$ is overall higher than that at $300K$ by $\sim 100mV$ and $\sim 90mV$ for 45RFSOI and 45SPLCO processes, respectively. The DIBL of different types of devices is plotted as the function of temperature in Fig. 4.4(b, f), in which the DIBL shows a relatively temperature-independent trend.

By biasing the transistor in the linear region, we are able to extract the low-field carrier mobility with the following equation [62]:

$$\mu_{eff}C_{ox} = -\frac{2L}{W} \times \frac{\partial g_{ds}}{\partial V_{DS}} \tag{4.6}$$

The extracted $\mu_{eff}C_{ox}$ of BC FETs are shown in Fig. 4.4(c, g) as the function of overdrive voltage $(V_{GS} - V_{TH})$. The carrier mobility can be determined as the inverse of the sum of

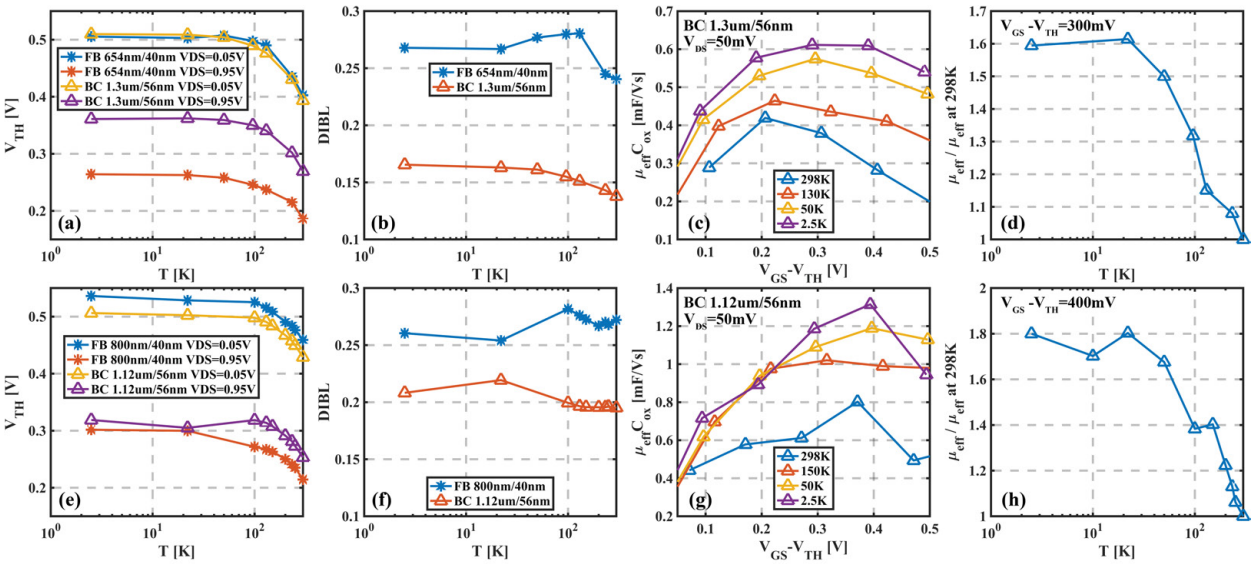


Figure 4.4: Key parameters of (a-d) 45RFSOI and (e-h) 45SPCLO transistors: V_{TH} versus temperature; index of DIBL versus temperature; $\mu_{eff}C_{ox}$ versus V_{GS}-V_{TH} at different temperatures; $\mu_{eff}(T)/\mu_{eff,\ 298K}$ versus temperature.

the scattering rates corresponding to all relevant scattering modes. The phonon scattering, $\propto T^{-3/2}$, is significantly reduced at the cryogenic temperature and thus causes an increase in $\mu_{eff}C_{ox}$, assuming the gate oxide capacitance is temperature independent. But with the continuing increase of the overdrive voltage, the mobility starts to degrade due to surface roughness scattering under the high vertical field. As a result, the maximum mobility is achieved when $V_{GS} - V_{TH} = 0.3V$ and $0.4V$ for the transistors from two processes. Based on this, we find that the mobility improves by $\sim 2\times$ compared to that at $300K$, as shown in Fig. 4.4(d, h).

The sudden increase of drain current in Fig. 4.2(e, g) is a common phenomenon in FB devices, called the kink effect. The impact ionization current at the drain flows to the body and forward biases the body-source diode. The body potential increases with this diode voltage and thus causes a reduction in V_{TH}, which leads to the sudden change in current when the impact ionization becomes significant [63]. As both V_{TH} and μ_{eff} increase at the cryogenic temperature, the kink effect becomes more obvious.

Delay characterization

The ring oscillator (RO) based test structures, averaging measurement over tens or hundreds of transistors and thus immune to the local random variation, have long been used to characterize the CMOS process [58][64]. The schematic of two ROs with different stage numbers

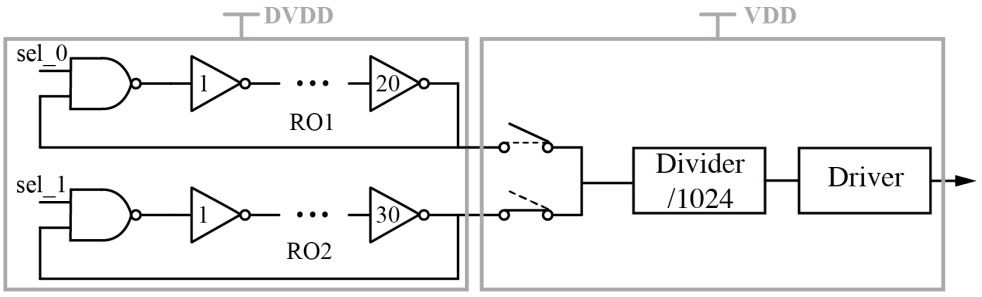


Figure 4.5: Block diagram of the test structure with two ring oscillators.

(20 and 30) designed in 45RFSOI process is shown in Fig. 4.5, in which the ROs are built with PDK standard cells with the fanout of 1, followed by an on-chip frequency divider to generate a low-frequency output. Two power supplies, DVDD and VDD, are used for oscillator core and peripheral circuits, respectively. Therefore, we can measure the oscillation frequency and current consumed in the active state (I_A) of each RO, and the total current consumed in the quiescent state (I_Q).

Figure 4.6(a) shows the frequency of ROs at $300K$ and $2.5K$. As expected, the increase of threshold voltage at cryogenic temperature, whose impact becomes weaker with higher supply voltage, is more than compensated by the increase in mobility and leads to the overall increase of the driving capability. By dividing the difference in clock period between two ROs by 20, we can get the average delay per inverter stage, shown in Fig. 4.6(b). $\sim 21\%$ improvement ($5.02ps$ vs. $4.15ps$) in gate delay at $2.5K$ can be observed when using $1V$ supply voltage, which is mostly owing to the increase of ON current ($635.9\mu A$ vs. $735.4\mu A$ in Fig. 4.2(e)). Fig. 4.6(c) presents the I_A of RO2 and I_Q of two ROs, where the quiescent state current is significantly reduced at the cryogenic temperature while the active state current increases by a little bit. The power consumption of the RO operating in the active state can be written as:

$$P = C \times V_{DVDD}^2 \times f = (I_A - I_Q) \times V_{DVDD} \tag{4.7}$$

where C and f are the total capacitance and oscillation frequency of RO, respectively. Fig. 4.6(d) shows the capacitance C calculated by plugging test results into the above equation. The decrease of the gate capacitance at higher supply voltage could be from the poly-Si depletion under the strong inversion region[54]. In contrast, the capacitance ratio between room and cryogenic temperature is very close to one, meaning that the gate capacitance is almost temperature-independent.

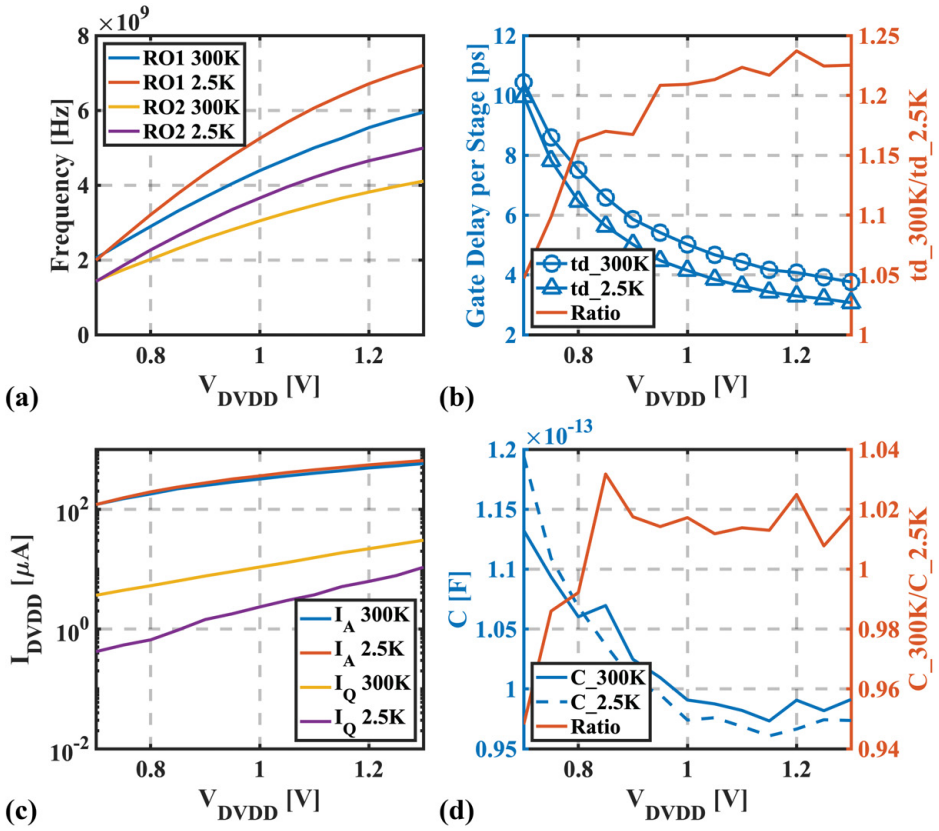


Figure 4.6: (a) Frequency of ROs; (b) Gate delay at different temperatures and their ratio; (c) IDDA of RO2 and IDDQ of two ROs; and (d) Capacitance at different temperatures and their ratio. versus DVDD.

Noise Characterization

Random Telegraph Noise (RTN), generally considered as $1/f$ noise [54], is caused by the stochastic capture and emission of carriers into traps at the gate oxide or the SiO2/Si interface [65], behaving as the current to fluctuate randomly between discrete levels across a broad timescale. The test circuit shown in Fig. 4.1(b) is reused to characterize the RTN, in which the drain current of transistors is sampled by the waveform generator/fast measurement unit (WGFMU) module of Agilent B1500A. Since the body-connected FET from these PD-SOI processes is more often used in analog mixed-signal circuit design compared to the floating-body device, the RTN analysis mainly focuses on FETs BC NMOS $1.3\mu m/56nm$ and BC NMOS $1.12\mu m/56nm$ from 45RFSOI and 45SPCLO processes, respectively.

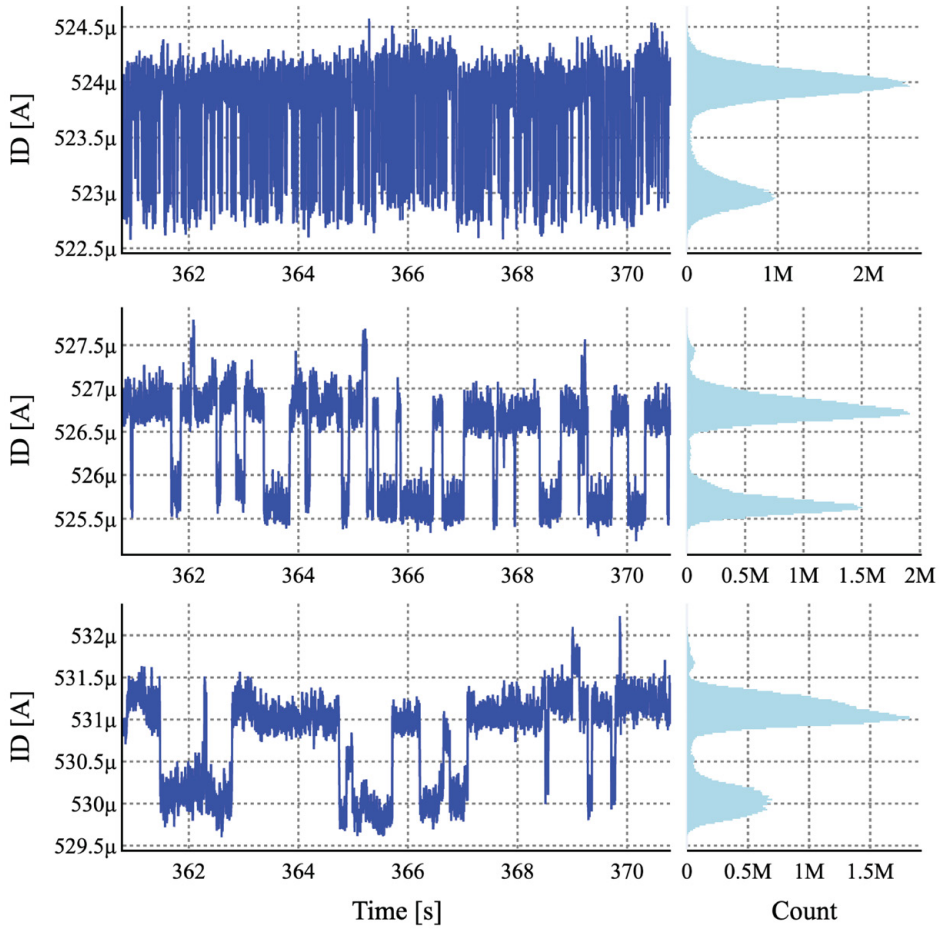


Figure 4.7: Sampling waveform and histogram of BC 1.12um/56nm FET from 45SPCLO process at temperature 100K, 50K, and 12K (from top to down). Bias condition: V_{GS}=0.9V and V_{DS}=0.2V.

Time Domain Analysis

The transistor current is first sampled at 10 KHz with WGFMU. Figure 4.7 shows the time domain waveform alongside the corresponding histogram at various temperatures under the same bias conditions, in which we can find the random current jumps between two or three unique levels on top of the background white noise. As the temperature increases, the carriers can cross the barrier more easily. In addition to the increased channel carrier concentration due to lower threshold voltage, the trap becomes more easily filled. Similarly, the carrier can more easily escape the trap with increased thermionic energy. As a result, even at the same bias condition, capture time (τ_c) and emission time (τ_e) decrease with temperature increase.

The quantitative analysis of time-domain RTN can be found in Fig. 4.8, in which the

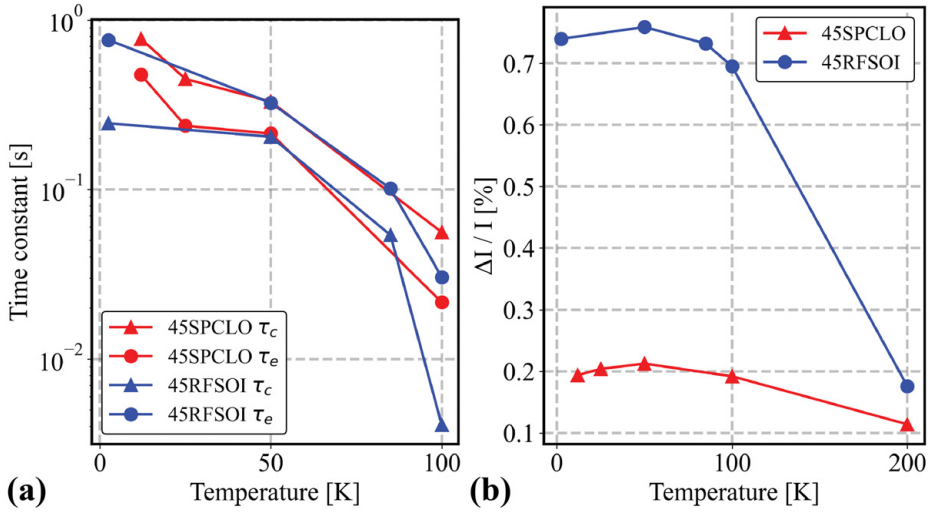


Figure 4.8: (a) Impact of temperature on τ_c and τ_e of RTN, (b) Impact of temperature on the magnitude of RTN. 45RFSOI FET is biased with V_{GS}=0.65V and V_{GS}=0.2V; 45SPCLO FET is biased with V_{GS}=0.9V and V_{GS}=0.2V.

time constants (τ_c and τ_e) and relative magnitude ($\Delta I/I$) of RTN are extracted with Kernel Density Estimation (KDE) and Thresholding after applying discrete wavelet transform on the raw data to reduce the influence of thermal noise. When the temperature decreases, the magnitude of RTN in both processes increases, and τ_c and τ_e increase, consistent with the observation in [66].

Frequency Domain Analysis

The classical model used to describe the low-frequency noise of MOSFET is based on carrier number fluctuation (CNFs) with correlated mobility fluctuation (MFs), in which the current fluctuation comes from the dynamic trapping and de-trapping of the free carrier into traps located in the oxide near the interface, and also the fluctuation of the scattering rate induced by the insulator charge fluctuation [67]. The equivalent input gate voltage spectral density is then given by [68]:

$$S_{vg} = \frac{qkTN_{BT}}{WLC_{ox}^2\alpha} \cdot \frac{1}{f} \cdot \left(1 + \Omega\frac{I_D}{g_m}\right)^2 \tag{4.8}$$

where N_{BT} is the volumetric gate dielectric trap density per unit energy, α is the exponent of wentzel–kramers–brillouin (WKB) tunneling probability for a rectangular barrier, Ω is a coefficient of mobility.

Based on equation 4.8, the S_{vg} should diminish with decreasing temperatures when maintaining identical bias conditions. In Fig. 4.9, the observed input-referred gate voltage spectral density aligns with this anticipated decline from 300 K to 50 K. However, at 2.5 K, a

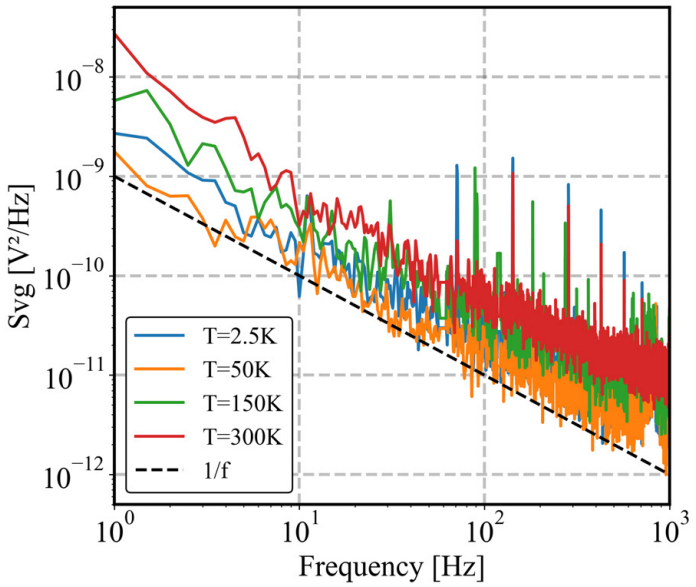


Figure 4.9: Input gate voltage spectral density (S_{vg}) of 45SPCLO transistor under different temperatures. Bias condition: V_{GS}=V_{TH} and V_{DS}=50mV.

notable increase in noise spectral density can be observed. The sudden increase of the RTN at deep cryogenic temperature has also been observed in other literature[68, 69]. A recent study suggests that the cause of the excess noise could be the band-tail states in the channel acting as additional capture/emission centers at cryogenic temperatures [68]. Our measurement results, shown in Fig. 4.10, illustrate a similar pattern, in which the normalized noise value ($S_{vg} \cdot f/T$) remains constant over a wide range of temperatures, and the excess noise shows up when the temperature is lower than 50 K. This corner temperature is consistent with the temperature where the saturation of the subthreshold swing starts to occur, as depicted in Fig. 4.3(a, b). This correlation validates the theory of the origin of the excess noise.

Impact on Circuit Design

From the perspective of a circuit designer, the very low-frequency part of the RTN is usually out of the bandwidth we care about. Therefore, the corner frequency, where the $1/f$ noise equals white channel noise, could be a good indicator of quantifying RTN's impact. Typically, the channel noise is dominated by the thermal noise, scaling linearly with temperature. However, it has been observed that the channel noise is dominated by the shot noise instead of thermal noise when the channel length is less or equal to 10nm, where the effective channel length is comparable with the mean free path (l_m) of the carrier so that the current of quasi-

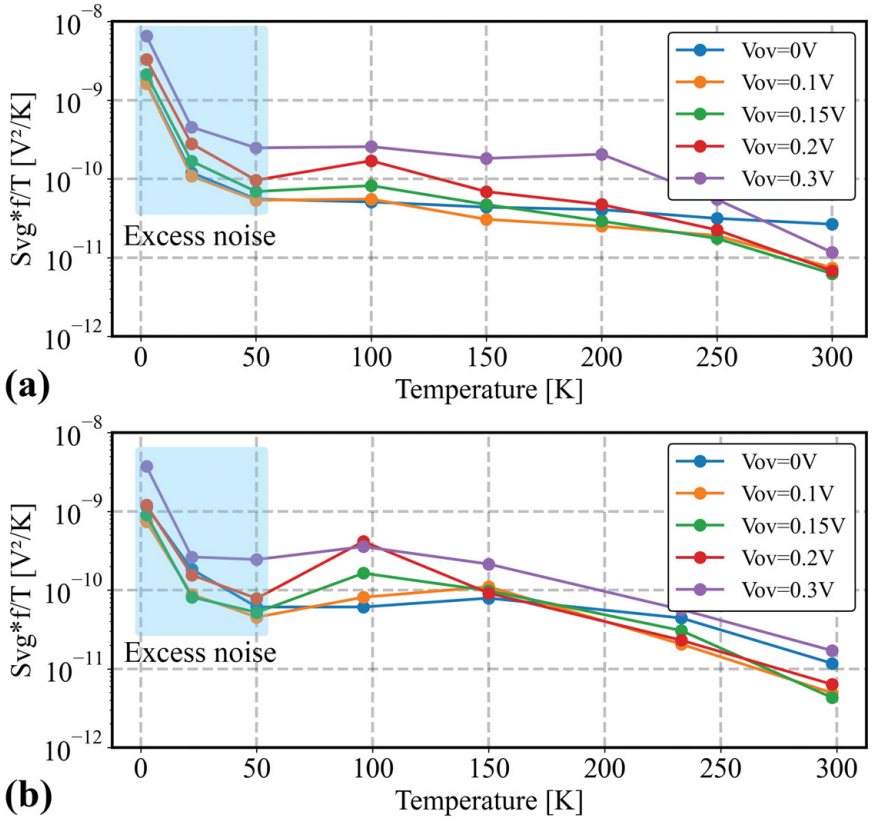


Figure 4.10: Plot of Svg·f/T versus temperature under different V_{ov} for (a) 45SPCLO and (b) 45RFSOI transistor. V_{DS}=50mV.

ballistic MOSFET mainly depends on the carrier injection from the source after crossing the energy barrier [70]. This effect is further enforced at cryogenic temperatures due to increased mobility and l_m. As a result, the channel noise for MOSFETs can be expressed as [70]:

$$S_{id} = 2k_s q I_{DS} \tag{4.9}$$

where k_s is the shot noise suppression factor of MOSFETs due to the scatterings in the channel, and q is the electron charge. For our processes with 45nm channel length, k_s is roughly 0.4 [71].

Figure 4.11(a) shows a good agreement between the simulated noise PSD with the PDK model and the measured low-frequency noise PSD at room temperature. The thermal and shot noise contribution can be calculated based on the simulation results. With the help of the measured g_m at different temperatures, we can also predict the thermal noise PSD at 2.5K with the classical thermal noise equation $S_{id} = 4K_B T\gamma g_m$, which is plotted in Fig. 4.11(b) along with the shot noise PSD derived from (4.9) and the measured RTN PSD. As we can observe, the shot noise is much larger than the thermal noise at cryogenic temperatures

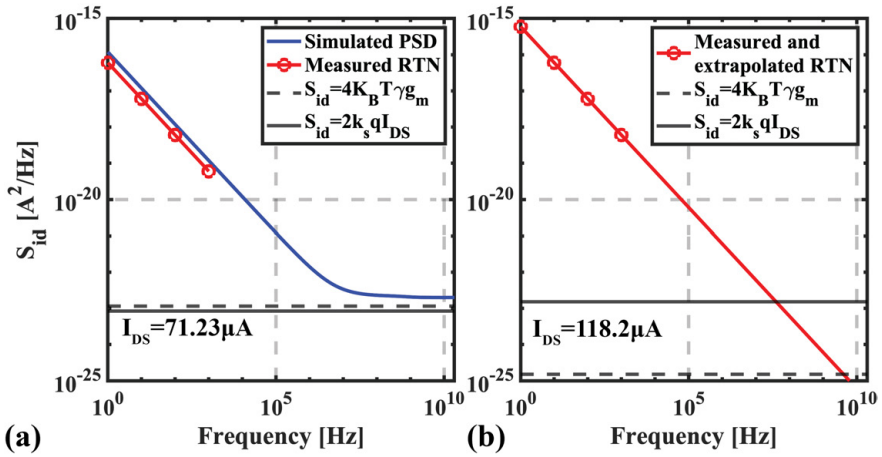


Figure 4.11: Plot of Sid of BC NMOS 1.12um/56nm at (a) 300K and (b) 2.5K. Bias condition: V_{GS}-V_{TH}=0.2V and V_{DS}=50mV.

and dominates channel noise. The increased RTN pushes the corner frequency by around one order of magnitude to 40 MHz for the measured device. In a word, directly using the thermal noise equation to estimate the noise performance of circuits at cryogenic temperatures could lead to a significant underestimation.

4.3 Summary

This Chapter presents measured DC, delay, and noise characterization of MOSFET from two monolithic silicon photonics processes down to 2.5K, along with the underlying theory. The improved SS, transconductance efficiency, and ON current at cryogenic temperatures can significantly enhance the performance of analog, mixed-signal, and digital circuits. On the other hand, the increased RTN induced by the band-tail state and the temperature-independent shot noise in the channel make noise analysis critical in designing low-noise Cryo-CMOS circuits, Finally, these characterization results pave the way to devise compact models to fill the gap in device behavior at cryogenic temperatures, bringing us closer to the realization of the advanced cryogenic computing system.

Chapter 5

Micro-ring based Cryogenic Optical Transmitter

Based on the system-level simulation described in Chapter 3, we know there is optimum gain in the pre-amplifier that can minimize the energy efficiency of the whole cryogenic egress link in terms of J/bit. In this Chapter, we design and implement a micro-ring-based cryogenic transmitter by leveraging the close integration between electronic and photonic components in a monolithic silicon photonic process. The characterization results are analyzed along with the comparison with other proposed solutions.

5.1 Design of the cryogenic transmitter

The block diagram of the CMOS amplifier is shown in Fig. 5.1(a). Since the superconducting quantum interference device (SQUID) at the output stage (SQUID stack amplifier) of the SCE IC alternates between superconductive and resistive state and thus changes its output impedance (20 Ω to 80 Ω [21]), a 50 Ω termination resistor, and AC coupling structure are used to reduce the signal reflection and isolate the circuit interface. The core circuit is a G_m-TIA amplifier, where the transconductance (G_m) stage is biased at the subthreshold region to leverage the improved transconductance efficiency due to the increased subthreshold swing at cryogenic temperature [72, 73], while the trans-impedance amplifier (TIA) stage is biased at the saturation region for higher bandwidth.

The detailed schematic of the CMOS amplifier is shown in Fig. 5.1(b), whose output drives the anode of the micro-ring modulator (MRM). In contrast, the cathode of the modulator, VB_MOD, is connected to a source/monitor unit (SMU) for biasing. During the link experiment, in which the superconductor electronics (SCE) integrated circuit (IC) directly drives the optical transmitter, node VTERM is connected to another SMU whose voltage is equal to the output DC voltage (10 mV) of the SCE IC.

2 μA bias current is supplied to the amplifier through node IBIAS, and the cascode current mirror is used to multiply the current and make sure the core transistor (CUR12)

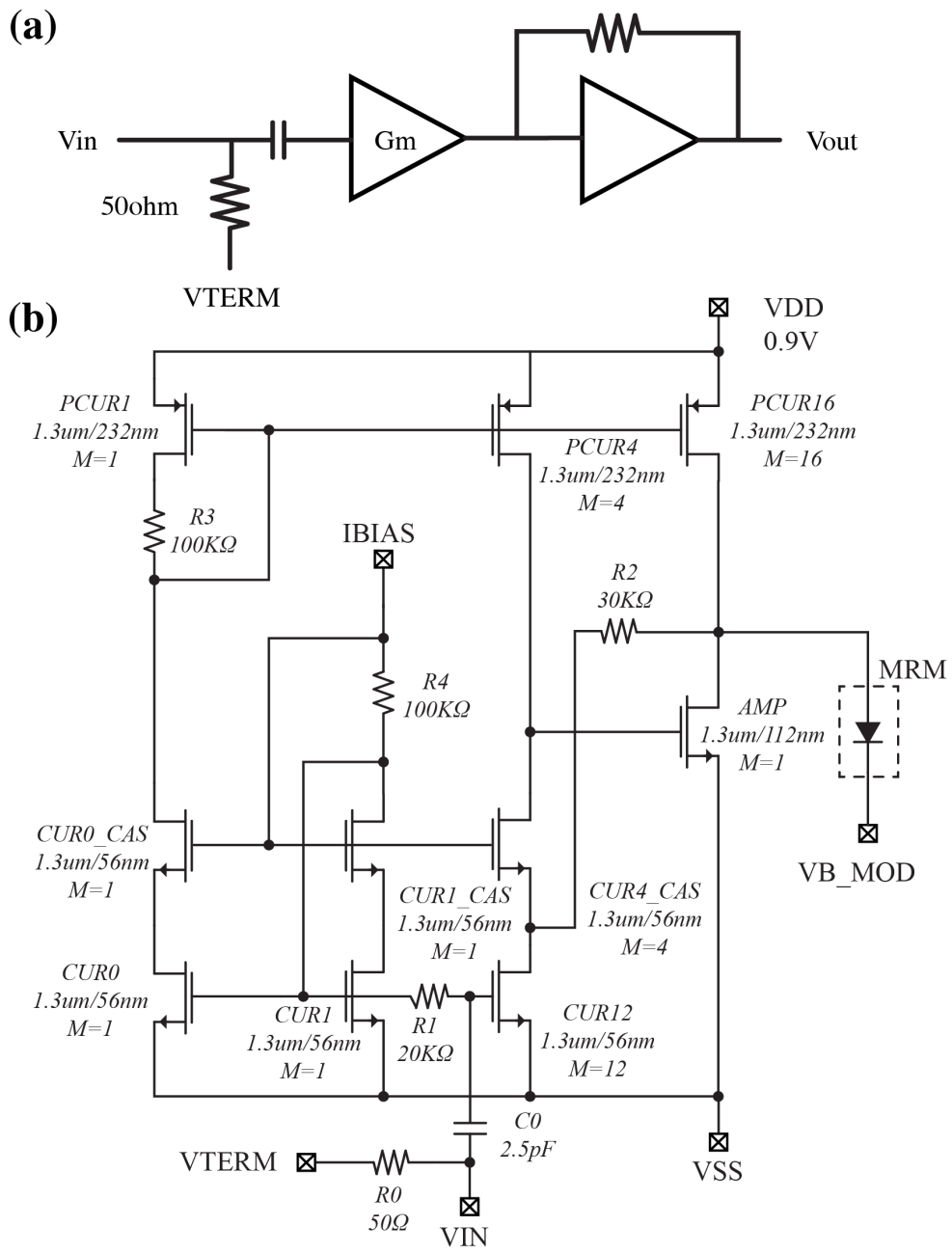


Figure 5.1: (a) Block diagram and (b) Schematic of the cryogenic CMOS amplifier.

can be properly biased at the subthreshold region. As is well know, the drain current and the corresponding transconductance (g_m) of MOSFET operating at the subthreshold region

can be written as:

$$I_{ds} = \frac{W}{L} I_{ds,0} \exp \frac{q(V_{gs} - V_T)}{nkT} \tag{5.1}$$

$$g_m = \frac{\frac{W}{L} I_{ds,0} \exp \frac{q(V_{gs} - V_T)}{nkT}}{n\frac{kT}{q}} = \frac{I_{ds}}{n\frac{kT}{q}} \tag{5.2}$$

Furthermore, the subthreshold swing of the MOSFET can be expressed as

$$SS = n \times ln(10) \times \frac{kT}{q} \tag{5.3}$$

Therefore, for a given current, the g_m can be appropriately estimated if we know the SS of the transistor at the cryogenic temperature:

$$g_m = \frac{I_{ds}}{SS} \times ln(10) \tag{5.4}$$

Transistors CUR4_CAS, PCUR4, PUCR16, AMP, and resistor R2 form the feedback TIA. The feedback configuration makes the design less susceptible to temperature change, which leads to the expression of the amplifier gain:

$$Av = g_m \times R_F = \frac{I_{ds} R_F}{SS} \times ln(10) \tag{5.5}$$

However, the SS does not follow the function of temperature given by equation Eq. 5.4, but saturates at the deep cryogenic temperatures due to the increase of interface-trap density close to the band edge [60]. Two examples show that 28nm FDSOI process [73] and 32nm FDSOI process [74] have SS of 15mV/dec and 44mV/dec at 4K, respectively. To avoid extreme conditions, 35mV/dec of SS is chosen. Therefore, the PDK model with the simulation temperature of 60K is used to get SS of 35mV/dec and simulate our design. Since our circuit topology is not sensitive to temperature variation, other cryogenic behavior of transistors, like the increase of the threshold voltage and mobility, has limited effects on our design.

The AC simulation shows that the amplifier can provide 28 dB mid-band gain and 854 MHz bandwidth (Fig. 5.2(a)) for 30 fF modulator load capactiance. A clear 1 Gbit/s eye-diagram that amplifies 4 mV_{pp} input to nearly 100 mV_{pp} can be observed in the transient simulation (Fig. 5.2(b)).

Since the partial etch step of body silicon does not exist in this standard CMOS process, a rib waveguide, the most common waveguide structure used to build resonant ring modulators, is unavailable. Therefore, an alternative structure, a spoked-ring resonator cavity (Fig. 5.3(a)), is used that allows the confinement of light in the silicon layer and placement of the metal contacts without causing excess loss [57, 75]. The vertical PN junction is formed at the region where the intensity of the optical field is the highest (Fig. 5.3(b)), providing optimum overlap between the optical mode and free carriers near the space charge region.

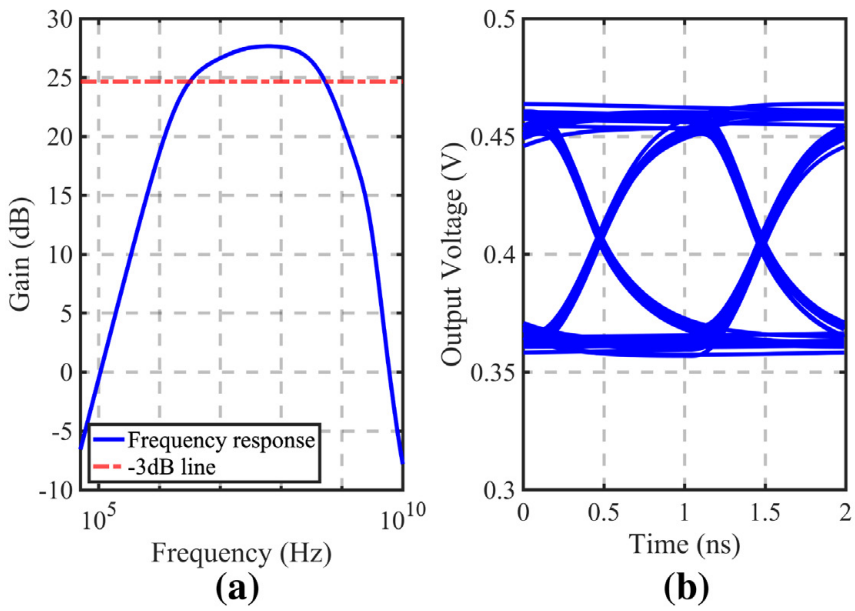


Figure 5.2: Simulated (a) frequency and (b) transient response of the cryogenic CMOS amplifier

Compared to previous modulators with lateral PN junction built in the same process [57, 75], the modulator with vertical PN junction shows more than 10x improvement in terms of modulation efficiency due to the larger overlap of the optical mode and depletion region [45].

The carrier freeze-out effect at the cryogenic temperature is mitigated through the increase of doping concentration at the cost of higher optical absorption and lower quality factor of the resonator [10, 45]. This lower quality factor is co-optimized with the gain of the integrated CMOS amplifier to achieve target optical modulation amplitude (OMA) performance with minimized energy consumption.

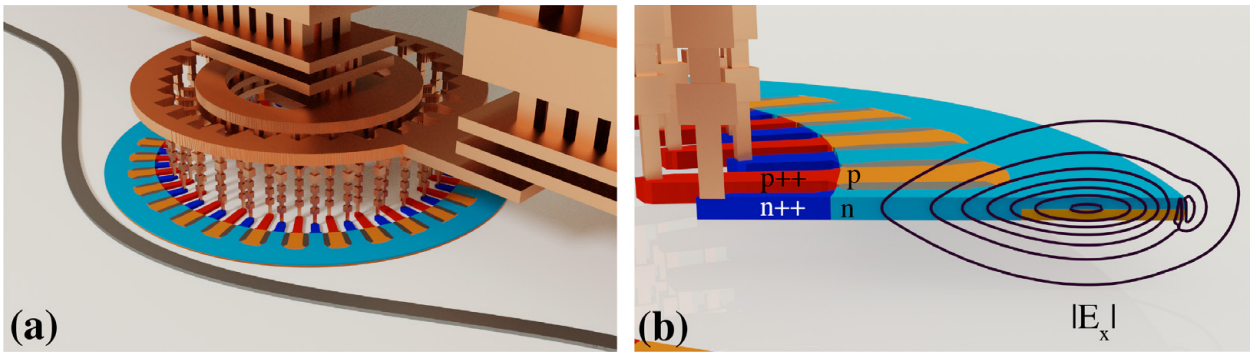


Figure 5.3: (a) Perspective view of the micro-ring modulator and (b) its cross-section, showing the vertical p-n junction formed in the optical guided region of the resonator.

5.2 Realization and Experiment Results

The integrated electro-optic transmitter chip was fabricated using GlobalFoundry's 45RFSOI process, a commercial high-performance 45 nm CMOS SOI process. The micrograph of the transmitter unit is shown in Fig. 5.4, including a micro-ring modulator with input and output grating couplers, where the grating couplers with the opposite and same direction are used for standalone and packaged measurement, respectively; a low-power CMOS amplifier, closely integrated with modulator; an electrostatic discharge (ESD) cell, used to protect the CMOS device from the static electricity; and decoupling capacitors used to bypass the power supply from other noisy circuitry.

Characterization of the integrated cryogenic transmitter

The optical modulator and the whole optical transmitter were characterized in the cryogenic probe station (Montana s200), shown in the inset of Fig. 5.5(a), where the chip board is placed on the middle piezo-controlled XYZ cold stage, fiber probe holders are attached to the left and right positioners. The power supply, modulator bias signal, and low-frequency control signals are supplied through phosphor bronze cryogenic wires and an on-board pin header, while the high-frequency signals are fed through BeCu coaxial cables and on-board G3PO RF connectors.

As shown in Fig. 5.5(a), by sweeping the wavelength of the optical carrier and monitoring the output power on the power meter, we can get the normalized transmission spectrum of the modulator with different bias voltages generated by the source/monitor unit (SMU). The transmission spectrum of the optical modulator with different DC bias voltages (the voltage drop between anode and cathode of MRM, VB) at the temperature of 4 K, in Fig. 5.5(b), shows that the resonance extinction ratio varies between 17 dB and 26 dB. A comparison of the extracted resonance shift between different temperatures, in Fig. 5.5(c), indicates

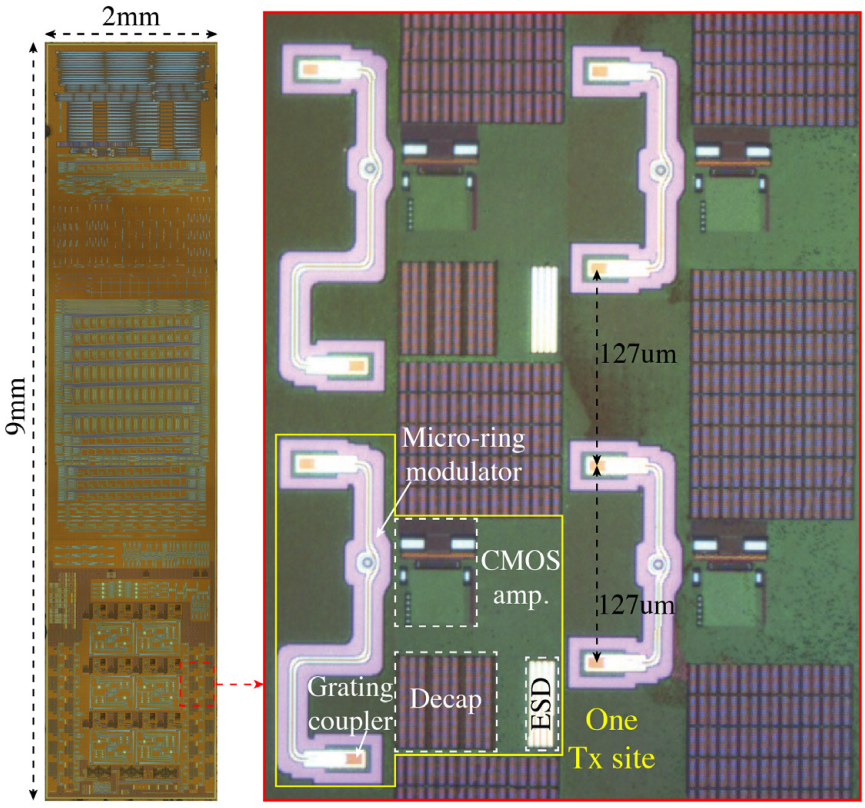


Figure 5.4: Micrographs of the whole chip and the transmitter unit cell.

an average modulation efficiency of 20 GHz/V, which slightly degrades in the reverse bias region at 4 K due to carrier freeze-out effect.

When measuring the frequency response (S21) of the whole transmitter, the laser is parked at the wavelength where the modulator has a 3dB insertion loss. The RF signal is applied to the transmitter from a vector network analyzer (VNA). The modulated optical signal is converted to an electrical signal through a high-speed photodetector before being received by VNA. The measured frequency response of the electro-optic transmitter with different bias voltages at 4 K is plotted in Fig. 5.5(d), showing a 3 dB bandwidth of 500 MHz when the modulator is reverse-biased. The bandwidth decreases to 236 MHz when the modulator enters the forward bias region with 1V bias voltage.

The data modulation experiment is implemented with phase-modulated laser-forwarded coherent detection (PM-LFCD) scheme (Fig. 5.6(a)) [30, 55], where the laser wavelength is fixed around the resonance wavelength of the ring modulator to get the maximum phase response. The pseudo-random bit sequence (PRBS) generated from a bit pattern generator (BPG) is sent to the optical transmitter after 30 dB attenuation as the low-swing driving signal. The modulated light is demodulated by interfering with the forwarded laser signal

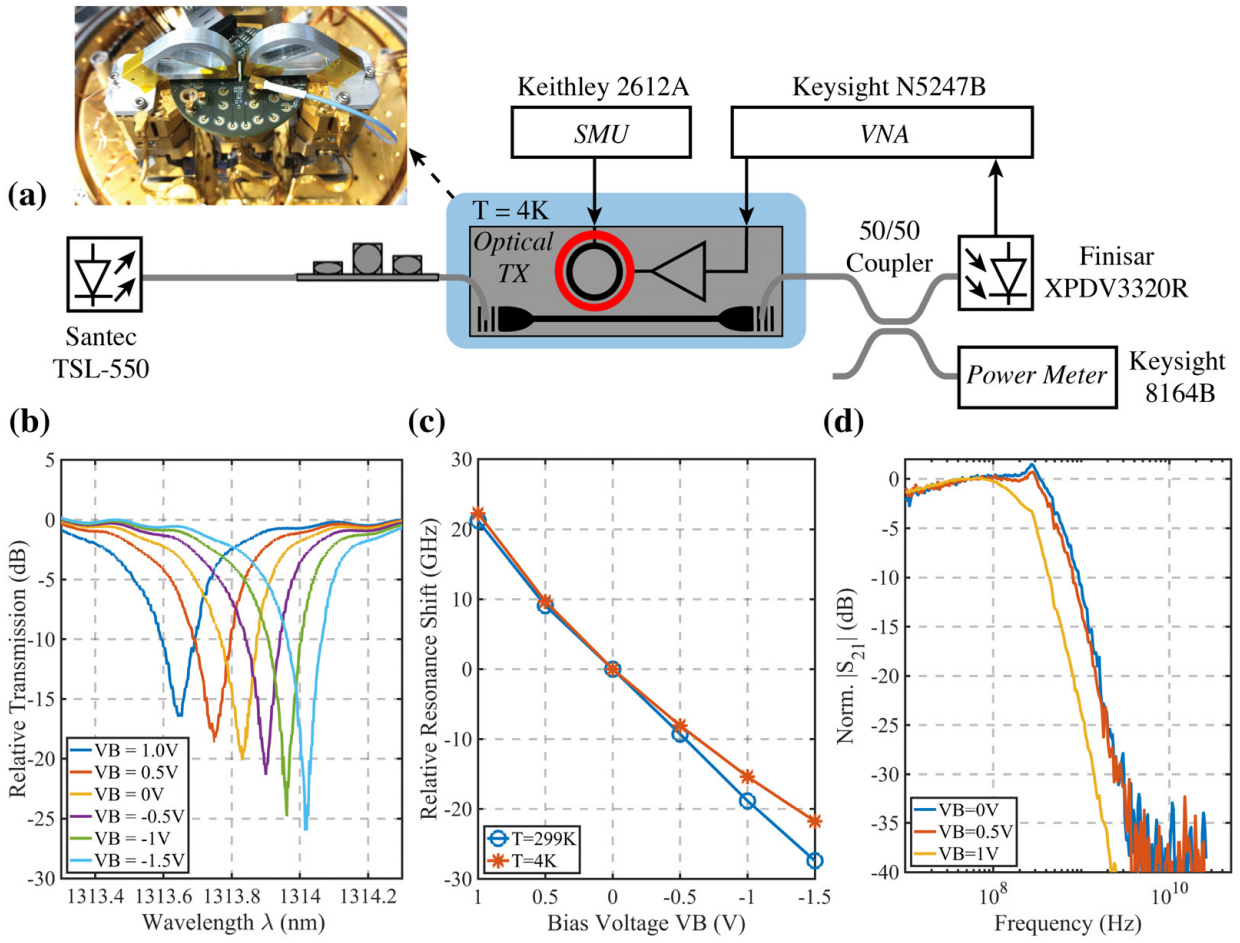


Figure 5.5: (a) Schematic of the experiment setup for device characterization. (b) Optical transmission response of MRM with different bias voltage at 4 K. (c) Relative resonance shift versus bias voltage at 4 K and 299 K. (d) Frequency response (S21 efficient) of the integrated optical transmitter with different bias voltages at 4 K.

through a 50/50 coupler, converted to an electrical signal with a balanced detector, and eventually recorded on the oscilloscope. Fig. 5.6(b) and (c) show the measured 1 Gbit/s eye diagrams at 4 K with 4 mV and 10 mV drive voltage, respectively, indicating that the drive signal with only several millivolts is enough to drive our optical transmitter and get an open eye diagram. The pair of eye diagrams demonstrates that a drive voltage 2.5 times smaller requires the laser power to double to achieve a comparable signal swing at the receiver. However, this adjustment comes at the expense of the signal-to-noise ratio (SNR).

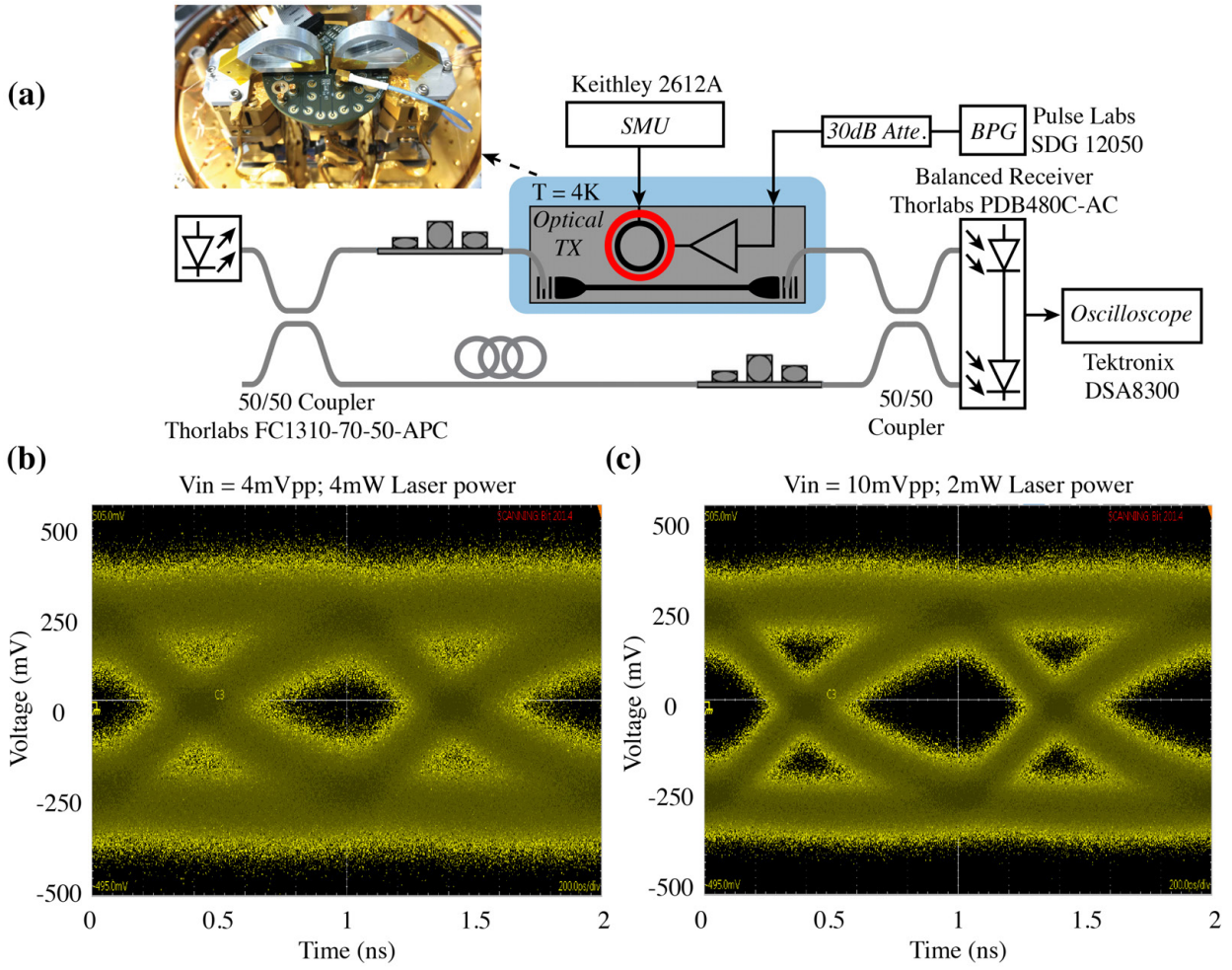


Figure 5.6: (a) Schematic of the experiment setup for data modulation with external bit-pattern-generator (BPG). 1 Gbit/s eye diagram with (b) 4 mV_{pp} and (c) 10 mV_{pp} external drive voltage measured at 4 K.

Cryogenic egress link demonstration with Superconductor chip

To emulate the situation of the real application, the optical transmitter needs to be fully packaged so that it can be placed and tested with the SCE IC in the same cryogenic station. The EO packaging procedure is shown in Fig. 5.7, where the electronic-photonic chip is first flip-chip bonded on the FR4 print circuit board (PCB). Next, the silicon substrate of the chip is etched with XeF2 to enable the guided optical mode to be confined in the transistor body silicon layer. Finally, the multi-channel V-groove fiber array is actively aligned to the on-chip grating couplers and glued on the chip through cryogenic epoxy (Stycast 1266). The epoxy was cured at room temperature for 16 hours.

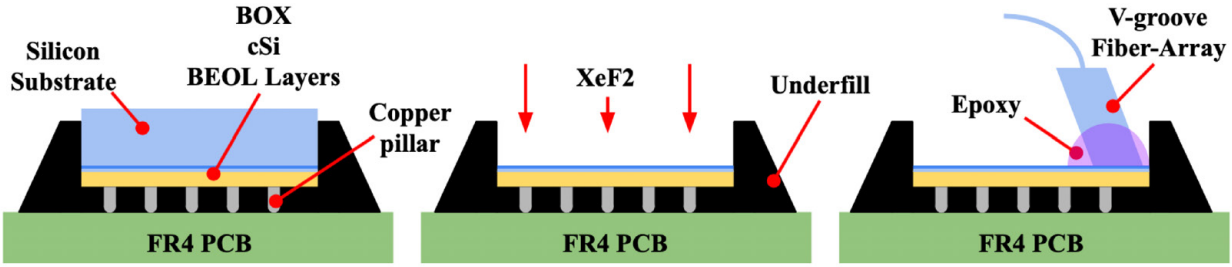


Figure 5.7: Package flow of the EO transmitter.

The micrograph of the fully packaged chip is shown in Fig. 5.8(a), where the V-groove fiber array is aligned to the on-chip grating coupler and fixed through cryogenic epoxy. The micrograph of the SCE chip, designed by Hypress Inc with MIT Lincoln Laboratory's Superconductor Electroncis process [76], is shown in Fig. 5.8(b). Fig. 5.8(c) shows the measurement setup inside the cryostat, where the optical transmitter is mounted on the 4 K plate of the cryostat to avid any heat transfer from another temperature stage to 4 K stage, and the SCE module housing the SCE chip is mounted on the other side of the 4 K plate to make sure that the chip can operate in the superconducting state. The interconnection between the SCE module and the optical transmitter is employed through radio-frequency (RF) coaxial cable.

The end-to-end transmission spectrum of the packaged optical transmitter is shown in Fig. 5.9, in which the center wavelength of the grating coupler at room temperature is around 1305 nm, as expected. However, the center wavelength shifted to 1290 nm at 4 K, which is caused by the tilt of the fiber array due to different thermal expansion coefficients of material at cryogenic temperatures. As a result, the coupling loss degrades from 6dB/facet to 8dB/facet at the target wavelength (1310nm).

With the test setup shown in Fig. 5.8(c), the cryogenic egress optical link is first demonstrated in the intensity-modulated direct detection (IMDD) configuration. As shown in Fig. 5.10(a), a field-programmable gate array (FPGA) is used to generate reference clock for the SCE IC. On the SCE IC, SFQ-based on-chip PRBS generators drive SSA, which generates NRZ outputs. One of the outputs is amplified by a commercial amplifier before recording by a sampling oscilloscope, while the other output directly drives our optical transmitter. A tunable laser set to $1,314$ nm provides the optical carrier. The modulated optical signal is detected by a photodiode and then monitored by the sampling oscilloscope.

Fig. 5.10(b) shows the 1Gbit/s eye diagram with 67 mV_{pp} voltage swing after 23dB off-chip amplification. This indicates that the output swing of the SCE IC is roughly 4.7 mV_{pp}. The clean optical eye diagram, shown in Fig. 5.10(c), demonstrates that the optical transmitter works properly at cryogenic temperature while directly driven by the SCE IC. The noise shown in the eye diagram is mainly contributed by the thermal and shot noise of the off-the-shelf optical receiver used in the test setup.

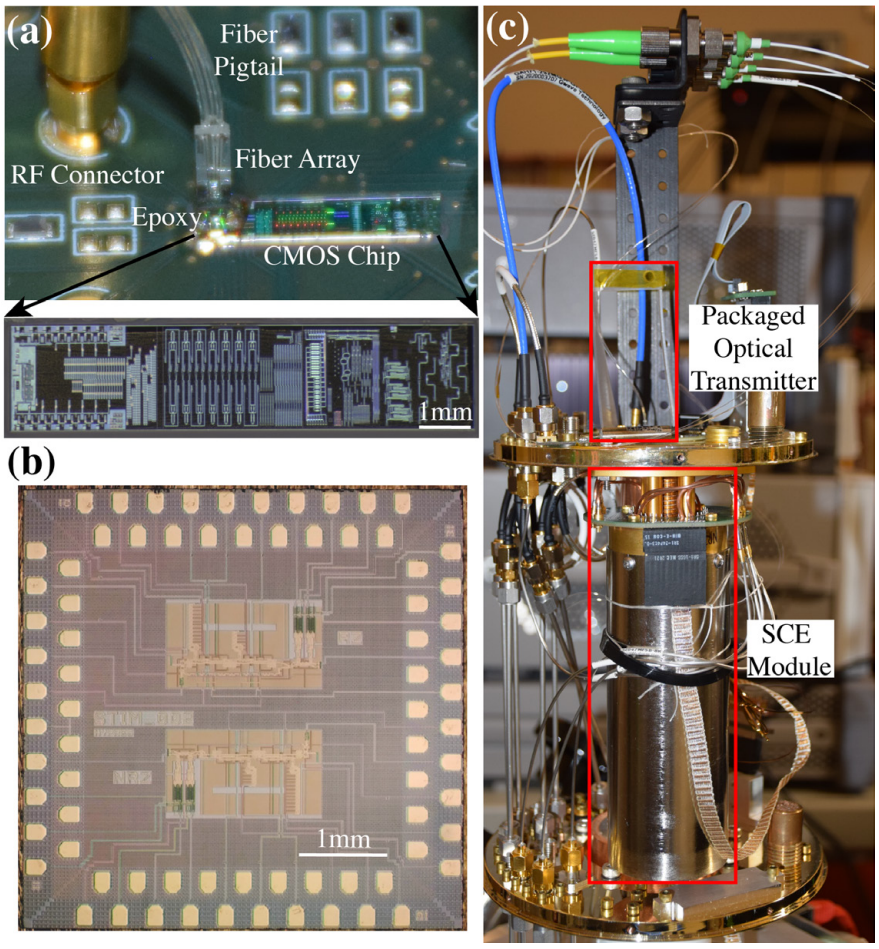


Figure 5.8: Micrograph of the (a) packaged optcial transmitter and (b) superconductor electronics (SCE) chip. (c) Test setup of the optical transmitter and SCE module in the cryostat.

The cryogenic egress optical link is then demonstrated in the phase-modulated laser-forwarded coherent detection (PM-LFCD) configuration [30, 55] scheme (Fig. 5.11(a)). Compared to IMDD test scheme, a power splitter is used to split the optical carrier into the signal light P_{SIG} and LO light P_{LO}. The modulated signal light from the cryostat interferes with LO light through a 50/50 coupler and is then fed into a balanced detector. The demodulated electrical signal is finally recorded on a real-time oscilloscope to measure bit error rate (BER). It should be noted that the minimum BER can be measured is 1e-6 because the maximum number of data bits that can be stored in this real-tim scope is 1000000.

As mentioned in the previous chapters, with the help of laser-forwarded coherent configuration, the required laser power and corresponding light lost in the cryostat can be significantly reduced, thus improving energy efficiency. Fig. 5.11(b) shows the link BER as

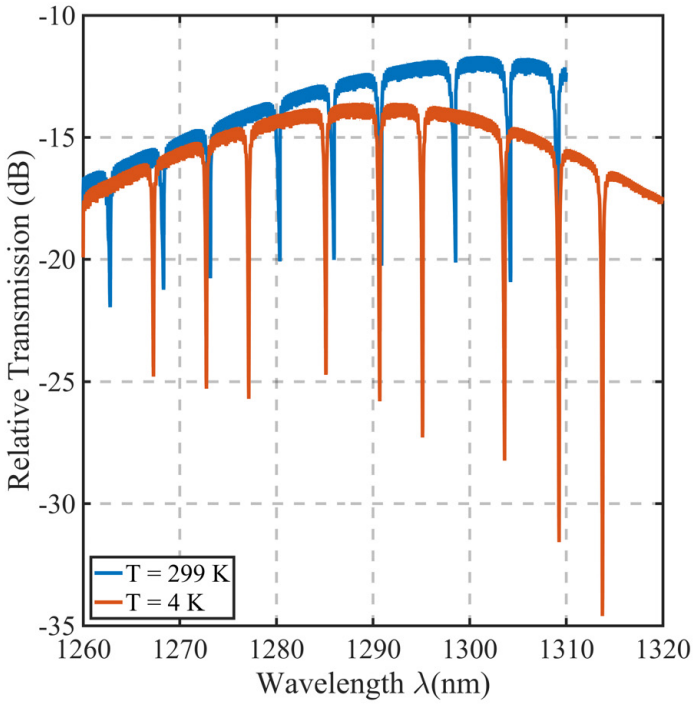


Figure 5.9: End-to-end spectrum of the packaged optical transmitter at 4 K and 299 K.

the function of laser power under different test configurations. Compared to the IMDD case, the required laser power to achieve the same BER is reduced by nearly 9 dB when the power splitting ratio (P_{SIG}/P_{LO}) of PM-LFCD is equal to 50/50.

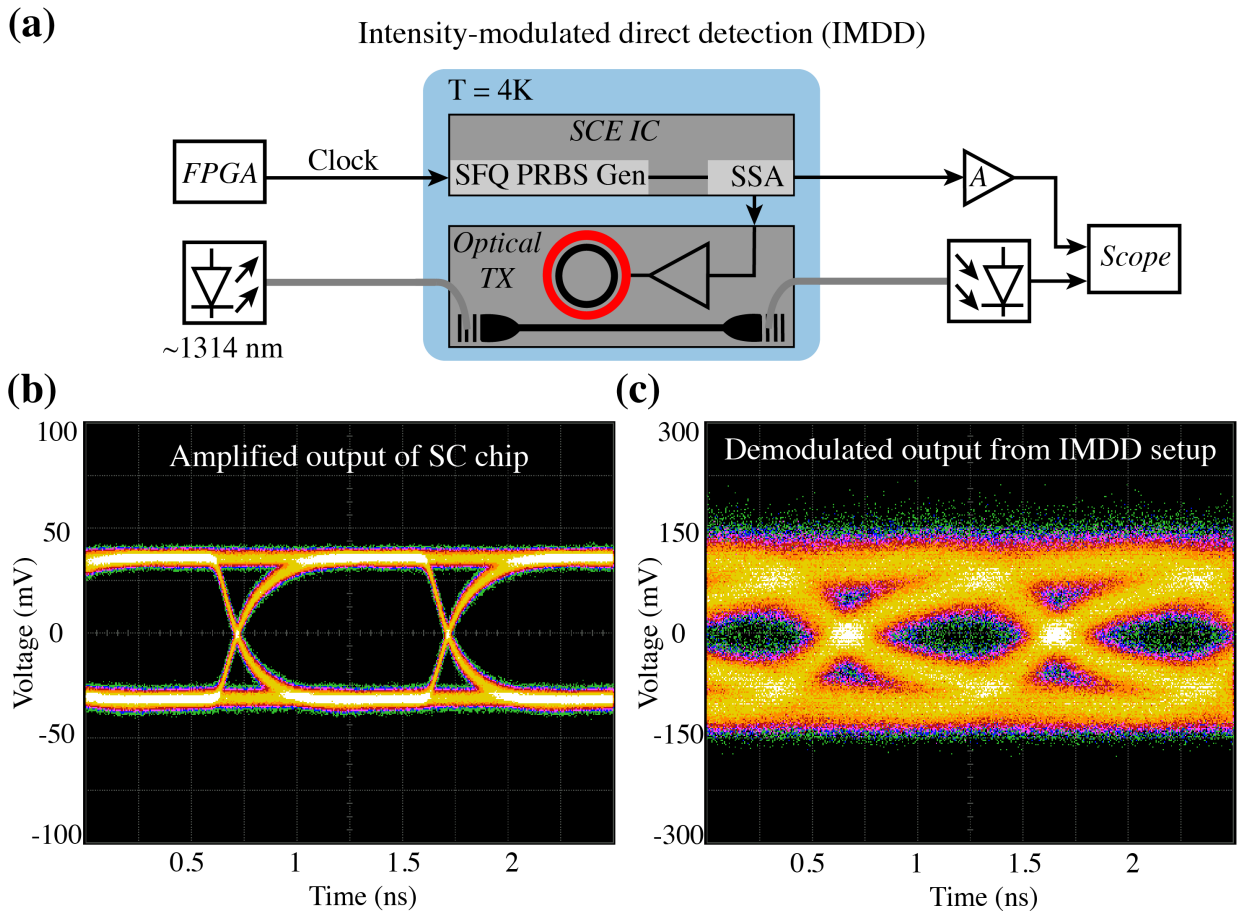


Figure 5.10: (a) Schematic of the experimental setup for IMDD test. (b) 1 Gbit/s output eye diagram of SCE IC after signal amplification. (c) 1 Gbit/s demodulated eye diagram in IMDD test.

5.3 Analysis of Noise and Energy Efficiency

Calculation of energy efficiency

The energy efficiency of interconnection between environments with different temperatures is one of the key metrics directly related to the scalability of the cryogenic system [8]. Although some electronic-photonic interfaces have been demonstrated at cryogenic temperatures recently, a universal calculation method for end-to-end energy efficiency has not been developed to date. Here we describe our calculation method considering the power consumption of all active components inside and outside the cryogenic station as well as the thermal loading effects.

The refrigeration efficiency of the commercial, 60 Hz 4 K cryogenic refrigerators varies

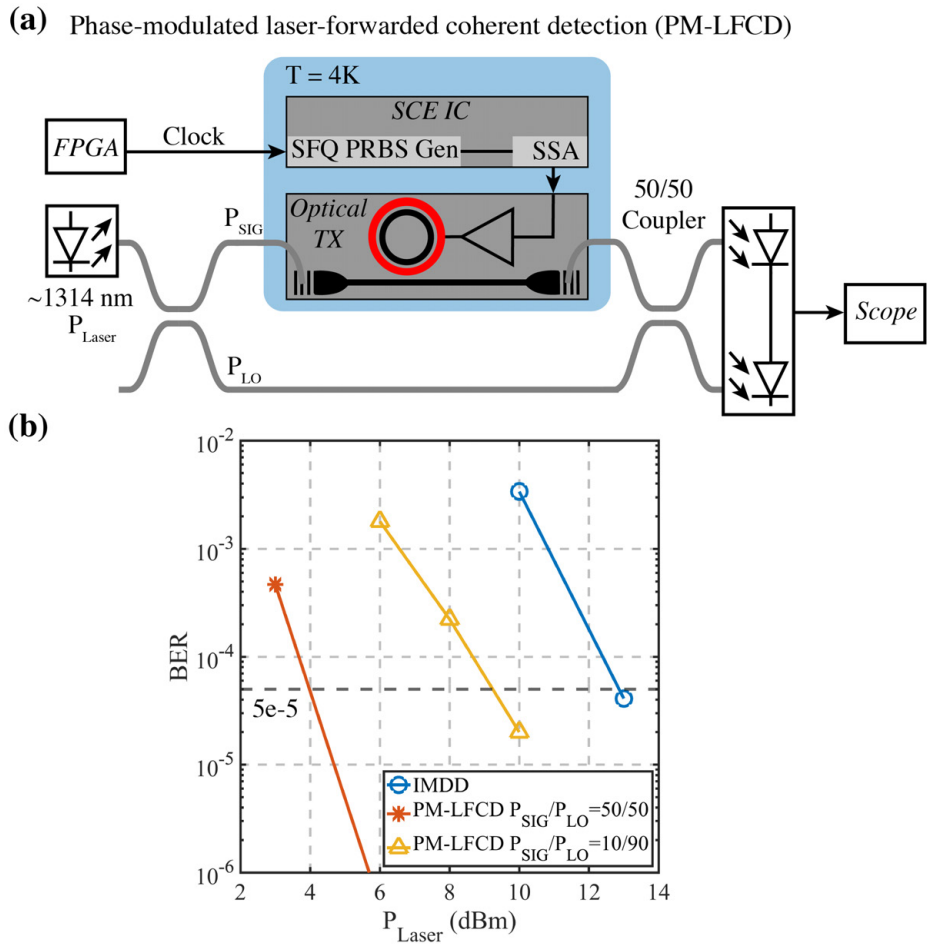


Figure 5.11: (a) Schematic of the experimental setup of PM-LFCD test. (b) BER versus laser power (P_{Laser} under different test configurations).

from several hundred to several thousand W/W [8]. Here we pick 500 W/W as the refrigeration efficiency $\eta_{cooling,4K}$ for the following energy efficiency analysis [5], which means for each watt dissipated at the 4 K environment, the refrigerator need to consume 500 W to maintain the temperature. Although there is such a significant imbalance power penalty between different temperatures in this communication link, the power consumed by components at the room temperatures as well as loading effects cannot be neglected entirely in some cases, especially when targeting ultra-high end-to-end energy efficiency.

The complete measurement setup of our link demonstration and energy-efficiency analysis is plotted in Fig. 5.12. The energy related to the optical transmitter consists of two parts, the wallplug energy consumed by the laser at room temperature ($P_{Laser,WPE}$), and the power dissipated at 4 K temperature (which loads the fridge and is converted to the cryostat

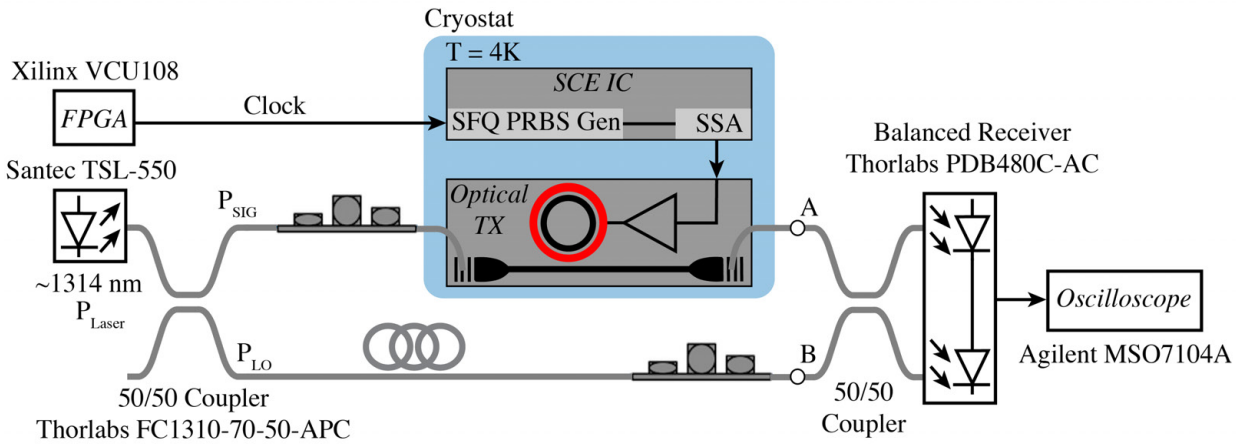


Figure 5.12: Measurement setup for link demonstration and energy-efficiency analysis.

wallplug energy, ($P_{Cryo,WPE}$)). The power dissipation at 4 K includes the electric power of the CMOS amplifier (P_{Amp}) and the optical power lost in the cryostat ($P_{LightLossInCryo}$). The heat leakage between the room and 4 K temperature, contributed by cryogenic DC wires and optical fiber, is negligible in our setup.

By turning on/off the on-chip CMOS amplifier at 4K, we can find the current consumed by the amplifier and thus calculate its power consumption:

$$P_{Amp} = V_{supply} \times I_{amp} = 0.9V \times 55\mu A = 49.5\mu W \tag{5.6}$$

To estimate the optical power lost in the cryostat, 0 dBm optical carrier parked at 1313.5 nm far from the modulator resonance, is supplied by a tunable laser to figure out the optical loss in the measurement setup. -22.68 dBm and -5 dBm optical power can be observed at nodes A and B (Fig. 5.12), respectively. Given that the splitting ratio of the power splitter (50/50 coupler) is 50/50 and the end-to-end coupling loss is 17.56 dB (8.78 dB/facet), the optical loss in the test setup, including the excess loss of power splitter, the insertion loss of polarization controller and the loss of optical connector, in the signal path and LO path are $\alpha_{sig,setup}$ = 2.12 dB and $\alpha_{LO,setup}$ = 2 dB, respectively. Therefore, only -5.12 dBm optical power enters the cryostat if the laser power is 0 dBm. For simplicity, let's assume that the power splitting ratio of the power splitter is $P_{SIG}/P_{LO} = k/(1-k)$ and the optical loss in the setup, $\alpha_{sig,setup}$ and $\alpha_{LO,setup}$, do not change with the splitting ratio. Then the optical power entering cryostat is

$$P_{LightEnterCryo} = P_{Laser} + 10log(k) - \alpha_{sig,setup} \tag{5.7}$$

Fig. 3.6 shows the response of the modulator under phase modulation, where the coupling loss α_c is 17.56 dB, ϕ_{In} is the phase difference under modulation, and α_m is the insertion loss of the modulator. In addition to the small resonance shift due to the limited drive

voltage, the laser wavelength is parked close to the resonance wavelength for a large phase modulation ϕ_{In}. So, the insertion loss α_m is close to the extinction ratio of modulator 18 dB. Therefore, it's OK to assume that almost all of the optical power entering the cryostat is then dissipated inside it, which means

$$P_{LightLossInCryo} \approx P_{LightEnterCryo} \tag{5.8}$$

Assuming the wall-plug efficiency of the laser is $\eta_{Laser} = 10\%$ [46], we can calculate the power consumed by the laser at room temperature:

$$P_{Laser,WPE} = P_{Laser}/\eta_{Laser} \tag{5.9}$$

Similarly, the power consumed by the cryostat can be calculated as:

$$P_{Cryo,WPE} = (P_{Amp} + P_{LightLossInCryo}) * \eta_{cooling,4K} \tag{5.10}$$

We can then figure out the total power consumed by the transmitter-related components at room temperature:

$$P_{Tot,RT} = P_{Laser,WPE} + P_{Cryo,WPE} \tag{5.11}$$

Finally, the 4 K referenced energy efficiency can be written as:

$$EE_{4K} = P_{Tot,RT}/\eta_{cooling,4K}/r_b \tag{5.12}$$

where r_b is the link data rate.

For our PM-LFCD link with a splitting ratio of 50/50, where $4dBm$ laser power is required to achieve 5e-5 BER (Fig. 5.11(b)), the energy efficiency can be written as:

$$\begin{aligned} EE_{4K} &= [P_{Amp} + (P_{Laser} + 10log(k) - \alpha_{sig,setup}) + \frac{P_{Laser}}{\eta_{Laser} * \eta_{cooling,4K}}]/r_b \\ &= [49.5\mu W + (4dBm + 10log(0.5) - 2.12dB) + \frac{4dBm}{10\% * 500W/W}]/1Gbps \\ &= 870.6fJ/bit \end{aligned} \tag{5.13}$$

As we can see from the diagram of energy efficiency breakdown (Fig. 5.13(a)), most of the power is from the optical loss at 4 K. Therefore, the easiest way to improve energy efficiency is to change the splitting ratio of the power splitter which reduces the optical power entering the cryostat. Given that 4 dBm laser power is required to achieve the BER of 5e-5 when the power splitting ratio is 50/50, the required laser power at different power splitting ratios to achieve the same signal-to-noise ratio (SNR) by using the following equation [30].

$$SNR = \frac{I^2_{rms,sig}}{I^2_{rms,noise}} = \frac{(I_{sig}/\sqrt{2})^2}{I^2_{n,amp} + I^2_{n,PD,shot} + I^2_{n,rx,thermal}} \tag{5.14}$$

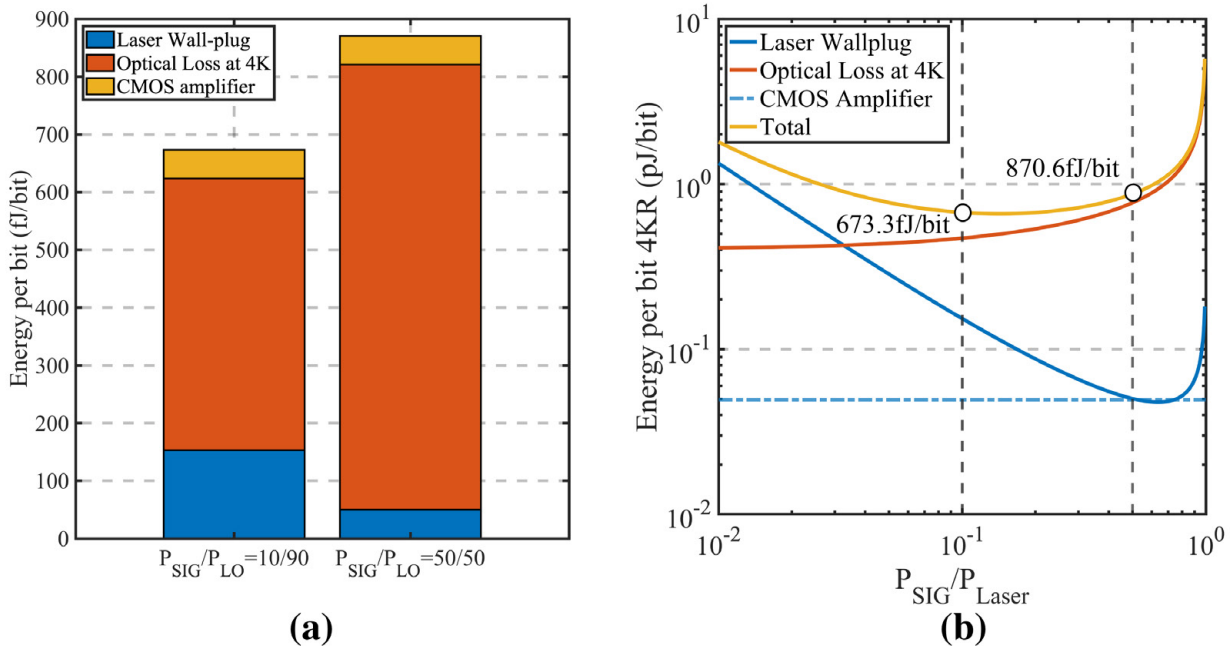


Figure 5.13: (a) Breakdown of energy efficiency at 4 K with splitting ratio P_{sig}/P_{LO} of 50/50 and 10/90. (b) Energy efficiency versus splitting ratio of the power splitter.

where the noise of cryogenic amplifier ($I_{n,amp}$), the shot noise of photodetector ($I_{n,PD,shot}$), and the thermal noise of photoreceiver ($I_{n,rx,thermal}$) are the three major noise sources in this communication link.

As mentioned in the section, PDK model and 60 K temperature is used to evaluate our cryogenic CMOS pre-amplifier. The simulated noise summary is shown in Fig. 5.14(a), where the dominant noise sources are all channel noise of transistors even at $T = 60K$. Then the total output RMS noise at 4 K can be estimated with the following equation:

$$V_{n,out,4K} = V_{n,out,60K} \times \sqrt{4K/60K} = 8.16mV \times \sqrt{4K/60K} = 2.1mV \tag{5.15}$$

Given that the simulated mid-band gain of the pre-amplifier is 27.6dB, the input-refer voltage can be estimated as:

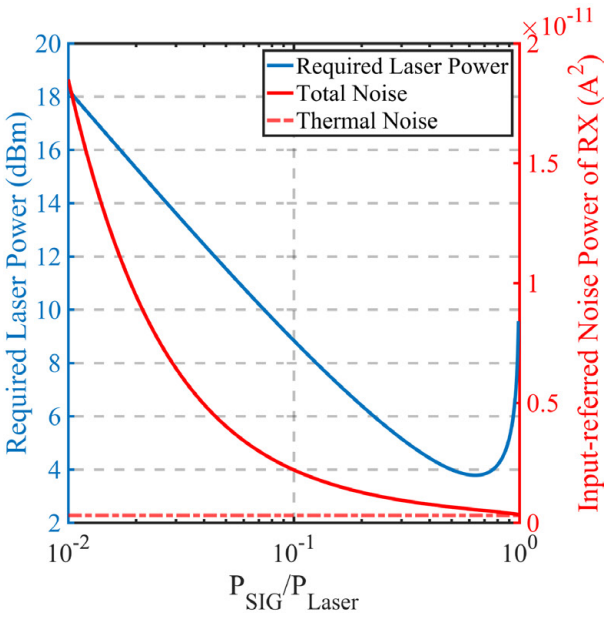
$$V_{n,in,4K} = V_{n,out,4K}/10^{27.6/20} = 87.5\mu V \tag{5.16}$$

which corresponds to 26 dB SNR at the output of the amplifier and can be ignored compared to the other two noise sources at the BER level of 5e-5 (corresponding to 7.6 dB SNR). Therefore the equation of SNR (Eq. 5.14) can be simplified as:

Device	Param	Noise Contribution
/X17/I1<0>/T0	id	0.00187045
/X0/X_AMP/X_NCUR12<0>/M0	id	0.00184864
/X0/X_AMP/X_NCUR12<1>/M0	id	0.00184864
/X0/X_AMP/X_NCUR12<10>/M0	id	0.00184864
/X0/X_AMP/X_NCUR12<11>/M0	id	0.00184864
/X0/X_AMP/X_NCUR12<2>/M0	id	0.00184864
/X0/X_AMP/X_NCUR12<3>/M0	id	0.00184864
/X0/X_AMP/X_NCUR12<4>/M0	id	0.00184864
/X0/X_AMP/X_NCUR12<5>/M0	id	0.00184864
/X0/X_AMP/X_NCUR12<6>/M0	id	0.00184864
/X0/X_AMP/X_NCUR12<7>/M0	id	0.00184864
/X0/X_AMP/X_NCUR12<8>/M0	id	0.00184864
/X0/X_AMP/X_NCUR12<9>/M0	id	0.00184864
/X0/X_PMOS_CUR/X_PCUR4<0>/M0	id	0.00170399
/X0/X_PMOS_CUR/X_PCUR4<1>/M0	id	0.00170399
/X0/X_PMOS_CUR/X_PCUR4<2>/M0	id	0.00170399
/X0/X_PMOS_CUR/X_PCUR4<3>/M0	id	0.00170399
/X0/X_AMP/X_NCUR0/M0	id	0.00144336
/X17/T1	id	0.0011925
/X0/X_AMP/X_NCUR4_CAS<3>/M0	id	0.00102408

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.00816597

(a)



(b)

Figure 5.14: (a) Simulated noise summary of the pre-amplifier. (b) Required laser power and corresponding input-refered noise at the input of receiver versus splitting ratio of the power splitter for $BER = 5e-5$.

$$
\begin{aligned}
SNR &\approx \frac{(I_{sig}/\sqrt{2})^2}{I_{n,PD,shot}^2 + I_{n,rx,thermal}^2} \\
&= \frac{[4R\sqrt{10^{-(\alpha_{sig}+\alpha_{LO})/10}k(1-k)}P_{Laser}cos(\phi_{in}(t))/\sqrt{2}]^2}{2qR(k \times 10^{-\alpha_{sig}/10} + (1-k) \times 10^{-\alpha_{LO}/10})P_{Laser}\Delta f + I_{n,rx,thermal}^2}
\end{aligned}
\tag{5.17}
$$

where the optical loss in the signal path is $\alpha_{sig} = \alpha_{sig,setup} + \alpha_c + \alpha_m$, and the optical loss in the LO path is $\alpha_{LO} = \alpha_{LO,setup}$. The responsivity, bandwidth, and input-referred thermal noise of photoreceiver are $R = 0.85A/W$, $\Delta f = 1.6GHz$ and $I_{n,rx,thermal} = 0.56\mu A_{rms}$, respectively.

Using Eq. 5.17, we can plot the required laser power for the SNR corresponding to the BER=5e-5 and the respective input-referred noise power as the functions of power splitting ratios (Fig. 5.14(b)). With the decrease of the power splitting ratio, more light hits the photodetector through the LO path, and thus shot noise starts to dominate. Compared to the measurement result in Fig. 5.13(a), the required laser power predicted by the SNR calculation is only 0.2 dB lower (8.8 dBm vs. 9 dBm) when the power splitting ratio is equal to 10/90, which might be caused by the different excess losses between the two power splitters.

Another important observation from the plot of energy efficiency (Fig. 5.13(b)) is that while the optimum link gain is achieved with the power splitting ratio of 50/50, teh split ratio for optimum energy efficiency depends on optical loss at 4 K (coupling loss and insertion loss of modulator), refrigeration, and laser efficiency. For our link with 50/50 and 10/90 splitting ratiom the 4 K referenced energy efficiency is measured to be 870.6 fJ/bit and 673.3 fJ/bit, respectively. For comparison, in the IMDD scheme, the energy efficiency at the same BER is 12.25 pJ/bit, dominated by the optical loss, due to the large laser power that needs to be provided to the 4 K environment.

Comparison with literature

Using the same calculation method mentioned above, we can compare the performance of our work with other EO interfaces [10, 11, 14–16] that have been demonstrated at the cryogenic temperature.

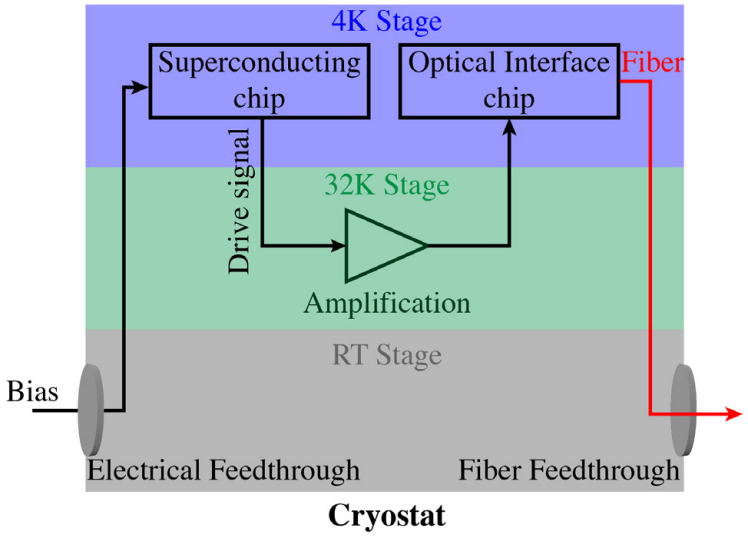


Figure 5.15: Experiement setup with extra cryogenic amplifier.

Since a superconducting chip cannot directly drive them, the power consumed by the extra cryogenic amplifier as well as the heat leakage from the resulting electrical connections should also be accounted for when analyzing energy efficiency. Assuming that the commercial cryogenic amplifiers are placed in the 32 K temperature stage (Fig. 5.15 [16]) with refrigeration efficiency $\eta_{cooling,32K} = 57W/W$ [5], $1.5GHz$ cryogenic amplifier can provide $45dB$ gain G_0 with $24mW$ power consumption P_0, and $4GHz$ cryogenic amplifier can provide $33dB$ gain G_0 with $27.2mW$ power consumption P_0, the energy efficiency of the cryogenic amplifier referenced to 4 K can be estimated with the following equation:

$$EE_{CryoAmp,4K} = 10^{(G_{elec}-G_0)/20} \times P_0 \times \frac{\eta_{cooling,32K}}{\eta_{cooling,4K} \times r_b} \tag{5.18}$$

where G_{elec} is the required electrical gain of cryogenic amplifiers, calculated from

$$G_{elec} = 20 \times log10(V_{drive}/4.7mV_{pp}) \tag{5.19}$$

The impact of the heat leakage between the 4 K and 32 K temperature stages can be calculated with the following equation:

$$EE_{HL,4K} = 2 \times P_{HL,40K-4K} * \frac{32K - 4K}{40K - 4K} \div r_b \tag{5.20}$$

where $P_{HL,40K-4K}$, $2.47mW$ heat leakage from 40 K to 4 K, is caused by a single 0.29 m long coaxial cable with silver-clad BeCu center conductor and BeCu outer conductor [5].

Regarding the active optical components, we can then calculate the energy efficiency of laser as:

$$EE_{Laser,4K} = \frac{P_{Laser}}{\eta_{Laser}} \div \eta_{cooling,4K} \div r_b \tag{5.21}$$

Table. 5.1 compares our work with other demonstrated cryogenic EO interfaces. As we can see, the existence of the discrete cryogenic amplifier [10, 11, 14, 16] significantly degrades the energy efficiency although it is placed in the 32 K stage having a low cooling penalty. On the other hand, larger laser power and/or an extra optical amplifier [10, 11, 14, 15] are required to achieve the target BER when directly driven by the weak signal, which degrades the system's energy efficiency. Our monolithic electro-photonic solution provides a good trade-off between the different active components and shows the best overall energy efficiency.

Potential improvement in energy efficiency

In above link experiment, the 17.56 dB fiber-to-chip coupling loss (8.78 dB/facet) significantly degrades the system's energy efficiency. The on-chip fiber-attach solution with self-aligned structures, developed by the same chip foundry in a new electronic-photonic 45SPCLO process — a derivative of the 45RFSOI CMOS process, shows high yield and high performance ($\leq$ 1.5 dB/facet loss) [77].

If the coupling loss α_c could be reduced from 2×8.78 dB/facet to 2×1.5 dB/facet, we can plug this new α_c into Eq. 5.17 to re-calculate the required laser power for BER of 5e-5 under different power splitting ratios, and then get a new plot of energy efficiency versus power splitting ratio. As shown in Fig. 5.16, the optimal energy efficiency is 100.6fJ/bit with a power splitting ratio of 5/95.

Table 5.1: Comparison with Other Demonstrated Cryogenic EO Interfaces

Type of EO interface	Bit rate (Gb/s)	Required drive signal	Electrical drive energy[a] (fJ/bit)	Heat leakage[b] (fJ/bit)	Optical loss at 4K[c] (fJ/bit)	Laser [d] (fJ/bit)	Total (fJ/bit)
BaTiO3 ring modulator [11]	20	$1.7V_{pp}$	45(1255)	192	N/A	N/A	1447
Si Micrdisk modulator [10]	10	$1.8V_{pp}$	80(2659)	384	31.6	0.63	3076
Ce:YIG mag-optic modulator [15]	2	$\pm 110mA$	3900(N/A)	N/A	N/A	N/A	3900
InP-on-Si ring, QW device [14]	1	$10mV_{pp}$	0.01(32.7)	3842	3370	67.4	7312
Cryo-VCSEL [16]	10	$250mV_{pp}$	160.9(369.2)	384	0[e]	0[e]	914
Monolithic EO interface (this work) with 50/50 power splitter	1	$4.7mV_{pp}$	49.5	0	770.9	50.2	870.6
Monolithic EO interface (this work) with 10/90 power splitter	1	$4.7mV_{pp}$	49.5	0	470.5	153.3	673.3

[a] The numbers in parenthesis are the energy efficiency of the cryogenic amplifier chain if the required drive voltage is larger than $4.7mVpp$.

[b] Heat leakage caused by the BeCu coaxial cables between different temperature stages.

[c] Fiber-to-chip coupling loss is included for a fair comparison between different EO interfaces.

[d] Wall-plug power of the laser. $\eta_{Laser} = 10\%$.

[e] For direct-modulated laser, the optical loss and laser power have already been counted in its electrical DC power (160.9fJ/bit).

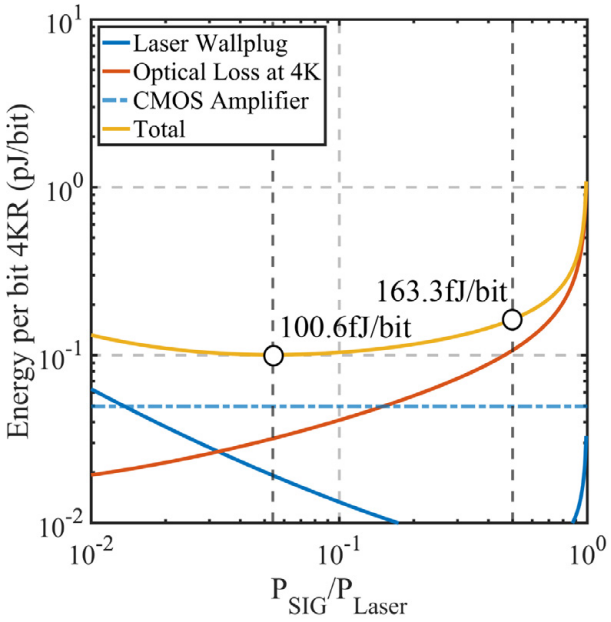


Figure 5.16: Energy-efficiency versus splitting ratio of the power splitter when $BER = 5e-5$ and $\alpha_c = 3dB$.

5.4 Superconductor Multi-Chip-Module (MCM)

Multi-chip-module (MCM), system-in-package (SiP), and heterogeneous integration use packaging technology to integrate dissimilar chips, optical devices, and/or packaged chips with different materials and functions, from different fabless house, foundries, wafer sizes, and feature sizes into a system or subsystem on different substrates or stand alone. Traditional MCM primarily encompasses a 2D integration, whereas SiP offers the potential for 3D integration, referred to as vertical-MCM or 3D-MCM. Heterogeneous integration shares similarities with SiP but is geared towards finer pitches, featuring increased input/output (I/Os), higher density, and enhanced performance [78].

These packaging technologies have been widely used in current high-performance systems. Fig. 5.17 shows several examples: (a) is NVIDIA's Pascal 100 GPU, built on TSMC's 16nm process and is supported by four HBM2 (16GB) fabricated by Samsung. Each HBM2 consists of four DRAMs with Cu pillar + solder cap bumps and a base logic die with TSVs straight through them. The GPU and HBM2 are on top of a TSV interposer ($1200mm^2$), which is fabricated by TSMC with a 65nm process [78]; (b) is AMD's 3rd Gen EPYC Server CPU with V-Cache, a 3D-stack technology that attaches additional cache onto a high-performance processor through hybrid bonding to significantly improve bandwidth and power [79]; (c) is Intel Stratix10 FPGA with Ayar Labs TeraPHY optical I/O chiplet on an AIB-connected, EMIB enabled MCM, enabling <5pJ/bit multi-Tb/s die-to-die IO connectivity at <10ns

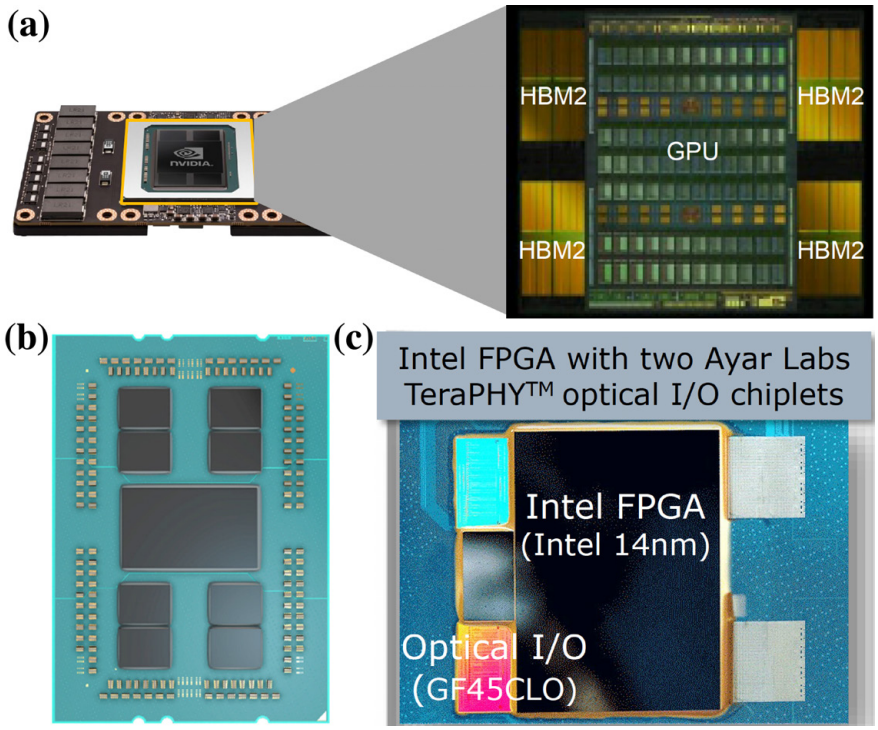


Figure 5.17: MCM examples (a) NVIDIA Pasca 100 GPU [78]. (b) AMD 3rd Gen EPYC Server CPU [79]. (c) Intel FPGA with Optical I/O chiplets [80].

SoC-to-SoC latency and with up to 2 km in reach [80].

Although we have experimentally demonstrated our cryogenic optical egress link with good energy efficiency, the existence of the RF interconnect (coaxial cable and connector) between the superconductor electronics chip and the photonic IO chip, shown in Fig. 5.8(c), still prevents the scalability of the superconducting computing system. Therefore, we propose a superconductor multi-chip module as the final solution for this communication link.

The packaging scheme of SC MCM is shown in Fig. 5.18, in which the photonic chip (Chip 2) and the SC chip (Chip 1) are first flip-chip attached on the MCM substrate and underfilled. Then, the assembled MCM and the FR4 PCB with an open cavity at the center are attached to an oxygen-free copper shim with silver paint, a good electrical and thermal conductive material. Next, gold wires are bonded between the MCM substrate and PCB for electrical connection, and the fiber array is aligned and glued on the photonic chip for light in/out. Finally, the packaged sample is attached to the cold head and fixed with screws. This stack-up structure makes the thermal resistance between the cold head and SC chip small enough so that the SC chip can operate in the superconducting state. Within this MCM, all high-speed signals generated by the SC computing chip are directly fed to our photonic chip through superconducting transmission lines on the MCM substrate with

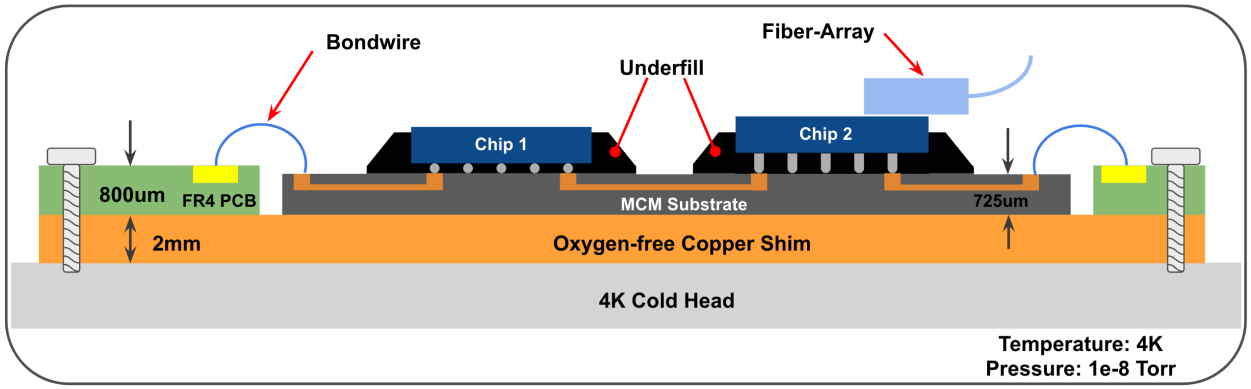


Figure 5.18: Packaging scheme of the Superconductor MCM.

negligible loss and then converted to the optical domain for light transmission. Only the DC and control signal must be supplied through bond wire and on-board connection, which can be made at low cost. The combination of short-pitch on-substrate transmission lines and the capability of DWDM communication of micro-ring-based optical links can greatly increase the communication bandwidth.

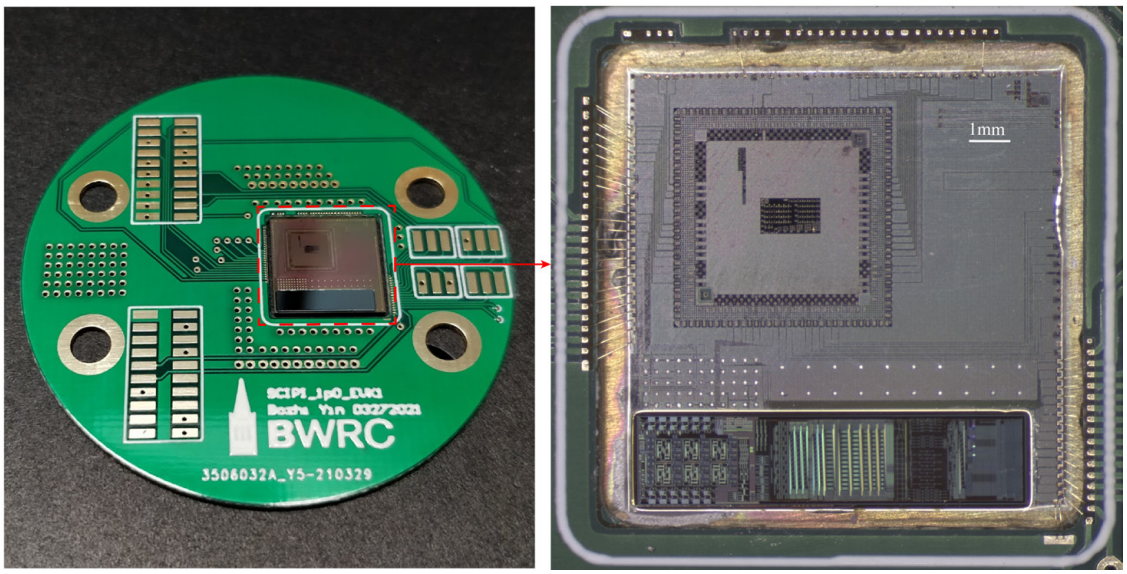


Figure 5.19: Packaged MCM sample.

Fig. 5.19 shows one of the packaged MCM samples. As shown in the zoom-in figure on the right, the 10x10 mm MCM substrate is designed and fabricated in MIT Lincoln Lab's SMCM-4M process [17], a niobium-based integrated-circuit fabrication process with four Nb

metal layers of interconnects separated by PECVD silicon oxide dielectric and one resistor layer. Our 2x9 mm photonic chip has been flip-chip attached to the substrate of MCM. The silicon substrate of the photonic chip was removed to confine the light in the waveguide. The region on the top left of MCM substrate is designed for the flip-chip assembly of the 5x5 mm SC chip.

Unfortunately, these superconductor MCMs weren't thoroughly tested due to the discontinued support of our collaborator, who designed the SC chip. However, the author believes the superconductor MCM is one of the important directions that enable the scaling and performance improvement of the superconducting computing system, just like what their room-temperature counterparts do in the current industry [78–80].

5.5 Summary

This chapter introduces the design of our single-chip cryogenic optical transmitter, which enables direct readout from a superconducting chip having only a millivolt-level output swing. The link test and energy analysis demonstrate that the monolithic integration of electronic and photonic offers a better energy efficiency than other demonstrated EO interfaces, making it a competitive interconnect solution for future cryogenic computing systems. We also point out that the energy efficiency can be easily improved from 673.3 fJ/bit to 100.6 fJ/bit using the new process with reduced coupling loss.

Furthermore, a superconductor multi-chip module (MCM) was proposed to solve the scaling bottleneck in the current superconducting computing system.

Chapter 6

Room temperature Coherent Receiver

Chapter 3 introduced one type of coherent-lite receiver with laser-forwarded architecture as a promising solution for receiving data at room temperature in cryogenic egress links. However, this self-homodyne system has an inevitable issue of time-varying phase offset. In this chapter, this issue is first introduced, followed by our proposed solution: an electro-optic phase-locking loop (EOPLL) consisting of a dLev comparator-based phase estimator and boundless phase shifter (BPS) based phase rotator. Finally, a proof-of-concept laser-forwarded coherent receiver is designed and implemented in a monolithic silicon photonic process to verify this idea.

6.1 Slow varying phase offset in laser-forwarded coherent link

As mentioned in section 3.1, the laser-forwarding coherent architecture eliminates the conventional receiver DSP required in the coherent link and greatly simplifies the receiver design. Self-homodyne detection is accomplished inside the receiver by beating the signal light with the LO light from the same laser source. However, even if two light beams are from the same laser source, a slowly varying phase change has been observed in this kind of fiber-optical interferometer [24, 30, 55, 81, 82]. This inevitable slowly varying rotation is due to any small path mismatch between the signal and LO paths, which vary slowly in time due to ambient acoustic, mechanical, pressure, and temperature changes [24, 81], leading to current fluctuation at the output of balance PD:

$$I(t) \propto 1 + cos[\phi(t) + \phi_n(t)] \tag{6.1}$$

where $\phi(t)$ is the phase modulation signal and $\phi_n(t)$ is the phase fluctuation caused by the environment. Unlike the typical statistical phase noise, the phase fluctuation caused by the environment can continuously drift along one direction over multiple π ranges and thus overwhelm the data. However, since the phase fluctuates at a very slow rate ($< 100kHz$), it can be compensated through a feedback mechanism: fiber stretch and phase modulator with

tuning range as large as 8.6π are used in [55, 81] and [82], respectively. DSP is employed in [24] to provide common phase rotation.

These existing solutions require either discrete photonic components or high-power DSP, which impede the link's scalability and counter the intention of a DSP-free coherent-lite link. Therefore, a low-power integrated phase tuning is required to adopt the laser-forwarding coherent link in the real system.

6.2 Boundless phase shifter (BPS)

Typical linear phase shifters (PS) supported in the silicon photonic process generate a tunable optical delay by controlling the effective index of the waveguide through changing temperature or free carrier concentration. For such PS, the phase shift tunability is up to a few $\pm\pi$ radians. Therefore, if we want to directly use a linear phase shifter to compensate for the phase fluctuation with more than 2π range, a reset in the control signal is required to switch the optical delay of PS from 0 to 2π. The impact of this transition on the transmitted data can be ignored only if the transition speed is faster than the data rate, which is almost impossible to realize due to the size of the phase delay element. As a result, the PS with continuous unbounded phase shift tunability is required.

Several techniques that offer boundless optical phase delays have been proposed and demonstrated in the literature. For instance, the single-sideband modulation technique introduced in references [83–85] employs quadrature sinusoidal signals for continuous linear phase modulation. A significant challenge with this method is the generation of unwanted sidebands. The serrodyning technique, outlined in [86] and [87], utilizes sawtooth periodic electric signals to achieve infinite linear phase shifts and consequent frequency shifts in the optical signal. However, this technique is impacted by issues like periodic resetting of phase modulation and the non-zero fall time of the sawtooth control signal, which lead to undesirable spurious sidebands. An unlimited range optical phase modulation method, introduced in [88], employs a cascade of multiple phase shifters with limited phase shift range and directional couplers with adjustable split ratios, making it challenging to produce the control signals which is necessary to minimize phase errors in high-speed applications. The boundless PS method proposed in [89] features a sequential combination of a 1×2 Mach-Zehnder interferometer (MZI) switch, a line phase shifter (including PS and passive waveguide), and a 2×1 MZI switch, complemented by analog signal control elements to lower power consumption. Precise synchronous switching of the phases of the MZIs and the line phase shifter is essential for this approach.

The use of IQ modulators for single-sideband modulation is the most attractive method among the above because of its ease of implementation. The issue of generating unwanted harmonics of this method is not critical in laser-forwarding coherent links because the boundless phase shifter is used for continuous phase compensation instead of providing optical frequency shifting.

Operation of Mach-Zehnder Modulator (MZM)

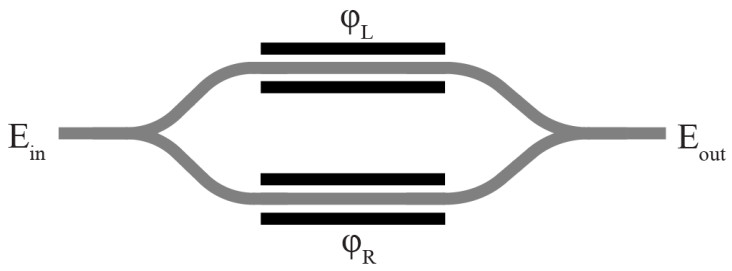


Figure 6.1: Typical structure of MZM.

Before talking about the operation of BPS, let's first look at the basics of MZM, which is used to build BPS. As shown in Fig. 6.1, the light is first split into two arms through a power splitter and combined after passing through two delay lines with the delay of ϕ_L and ϕ_R. Assuming no loss and a perfect 50/50 splitter/combiner, the output field can be written as:

$$\begin{aligned} \vec{E}_{out} &= \frac{1}{\sqrt{2}}\left(\frac{\vec{E}_{in}}{\sqrt{2}}e^{j\phi_L} + \frac{\vec{E}_{in}}{\sqrt{2}}e^{j\phi_R}\right) \\ &= \vec{E}_{in}\cos(\Delta\phi)e^{j\phi_0} \end{aligned} \tag{6.2}$$

where $\Delta\phi = \frac{\phi_R - \phi_L}{2}$ and $\phi_0 = \frac{\phi_R + \phi_L}{2}$. The intensity response of MZM is:

$$P_{out} = |E_{out}|^2 = \frac{1}{2}|E_{in}|^2[1 + \cos(\phi_R - \phi_L)] \tag{6.3}$$

If we can apply a differential drive signal to two arms, generating $\phi_R = -\phi_L = \phi_m$, then the modulation becomes a pure intensity modulation, and Eq. 6.2 can be simplified as:

$$\vec{E}_{out} = \vec{E}_{in}\cos(\phi_m) \tag{6.4}$$

IQ modulator-based boundless phase shifter (BPS)

The schematic of IQ modulator-based BPS is shown in Fig. 6.2 [82], where α_{sig} and β_{sig} are the differential drive signals of the MZM at I-arm and Q-arm, and γ_{sig} is the bias signal for generating $\pi/2$ phase difference between two arms. According to the response of MZM

shown in Eq. 6.4, we can derive the overall transfer function of BPS as:

$$\begin{aligned}\vec{E}_{out} &= \frac{1}{\sqrt{2}}(\vec{E}_{out,I} + \vec{E}_{out,Q}) \\ &= \frac{\vec{E}_{in}}{2}[\cos(\alpha_{sig}) + \cos(\beta_{sig}) \times e^{j\gamma_{sig}}] \\ &= \frac{\vec{E}_{in}}{2}[\cos(\alpha_{sig}) + j \times \cos(\beta_{sig})]\end{aligned} \tag{6.5}$$

Then, we can get both the intensity and phase response of the BPS:

$$|\frac{E_{out}}{E_{in}}|^2 = \frac{1}{4} \times [\cos^2(\alpha_{sig}) + \cos^2(\beta_{sig})] = \frac{r^2}{4} \tag{6.6}$$

$$\theta_{BPS} = \tan^{-1}[\frac{cos(\beta_{sig})}{\cos(\alpha_{sig})}] + m\pi \tag{6.7}$$

where m is an integer to compensate for the effect of phase wrapping, and r should be a constant since we want the output intensity of BPS to be constant while changing phase.

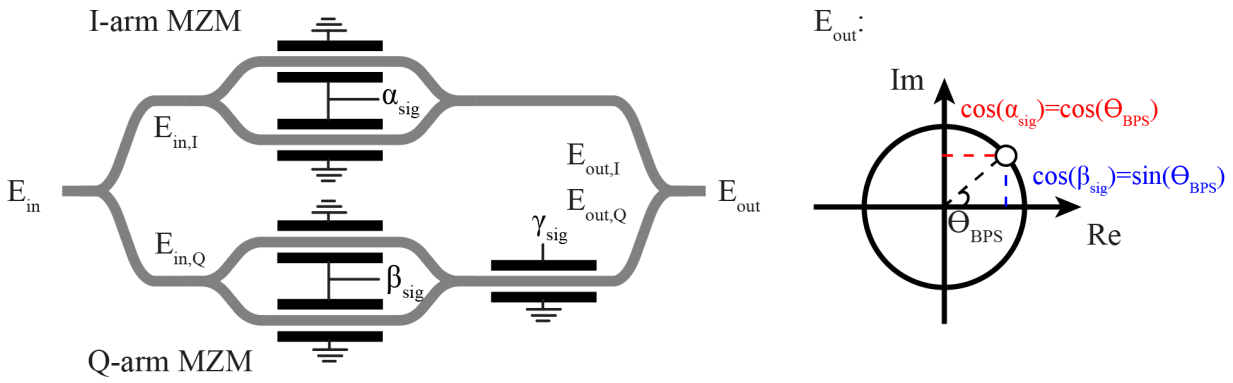


Figure 6.2: Structure of boundless phase shifter (left) and the complex plane plot of its output E field (right).

Solving the above equations, we can find that α_{sig} and β_{sig} need to be triangular-shaped, having a peak-to-peak amplitude of 2π and separated by a phase delay of $\pi/2$ from each other. A more intuitive way to understand this result is by looking at the complex plane plot shown in Fig. 6.2: to get the maximum constant amplitude of $\cos(\alpha_{sig}) + j\sin(\beta_{sig})$, we need to set $\cos(\alpha_{sig}) = \cos(\theta_{BPS})$ and $\cos(\beta_{sig}) = \sin(\theta_{BPS})$, and thus a $\pi/2$ phase difference is required between α_{sig} and β_{sig}. Furthermore, compared to a linear phase shifter with 2π tuning range in which resetting of the drive signal is required when transient from 0 to 2π, the phase control of BPS relies on the ratio of two independent drive signals so that it

can realize reset-free continuous phase change: when E-field move along the circle on the complex plane, two drive signals α_{sig} and β_{sig} continuous change over time.

Assuming two arms of MZM are driven by the differential signal: $\alpha_{sig} = \frac{VI}{V_\pi}\pi$ and $\beta_{sig} = \frac{VQ}{V_\pi}\pi$. We can get the response of BPS by sweeping drive voltage VI and VQ, shown in Fig. 6.3, in which the boundless phase shift can be achieved with a continuous drive signal.

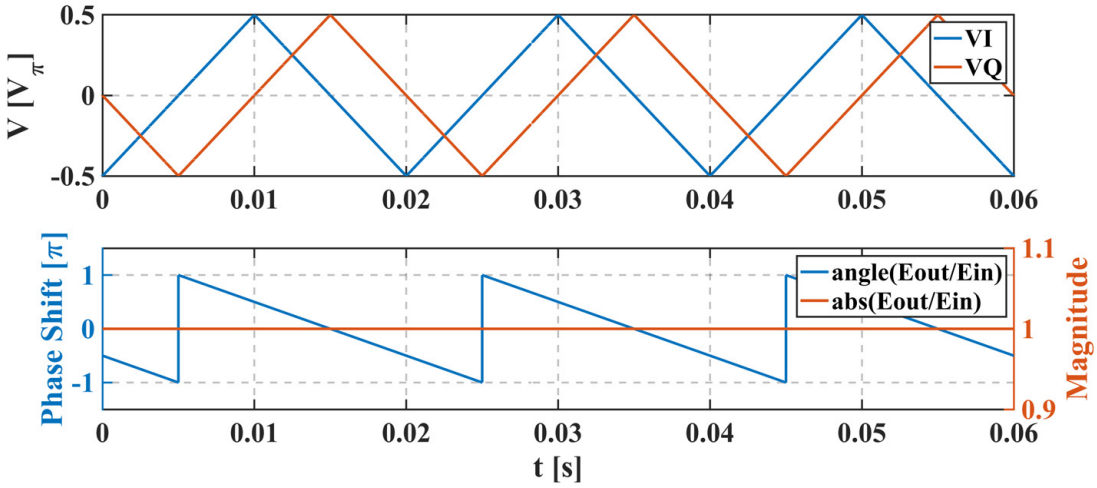


Figure 6.3: Response of BPS by driving dual-arm of MZM.

Proposed thermal boundless phase shifter (BPS)

As we can observe from Eq. 6.6, the IQ modulator-based BPS has an intrinsic loss of 6dB. Besides that, peak-to-peak π phase change is necessary for each MZM arm to perform continuous boundless phase shifting. If the electrical PN junction-based phase shifter is employed to build MZM, like [82], the insertion loss induced by either long waveguide or absorption of free carrier would further degrade the power performance of BPS. For instance, the $V_{pi}L$ of a reverse-biased PN junction phase shifter in an advanced monolithic silicon photonic process (45SPCLO [59]) is about $1.64Vcm$ with the optical loss of $7.5dB/cm$. Given that the maximum allowed supply in this process is 1.8V, even if we can utilize the AC couple technique to double the output voltage swing to 3.6V, the PN junction-based linear phase shifter still contributes to another 3.4dB optical loss for π phase tuning range.

On the contrary, the thermal phase shifter has a higher phase tuning efficiency that can make the device compact and optical insertion loss negligible, but at the cost of static power. However, the sealed undercut technology in the recent silicon photonic process, which creates an air gap under the BOX layer to increase the thermal resistance, can significantly improve the heater efficiency and reduce the power required for π phase shift (P_π) from 35mW to 7mW [59].

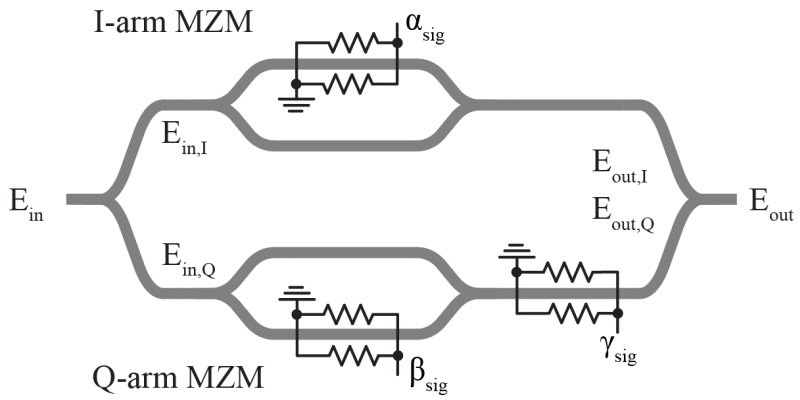


Figure 6.4: Structure of proposed thermal boundless phase shifter.

Therefore, we propose a thermal phase shifter-based BPS, shown in Fig. 6.4. Since the modulation efficiency of the thermal phase shifter is much larger than the PN junction-based phase shifter, there is only one thermal phase shifter per MZM with a single-ended drive signal, which can reduce the thermal crosstalk between two arms and make the layout even more compact. But the drawback is also apparent. With the single-arm drive, the phase term ϕ_0 inside MZM's transfer function (Eq. 6.2) is nonzero, and thus the phase is modulated along with the intensity at the same time in MZM. So, the transfer function of BPS needs to be revised from Eq. 6.5 to the new one:

$$\begin{aligned} \vec{E}_{out} &= \frac{1}{\sqrt{2}}(\vec{E}_{out,I} + \vec{E}_{out,Q}) \\ &= \frac{\vec{E}_{in}}{2}[\cos(\frac{\alpha_{sig}}{2})e^{j\alpha_{sig}/2} + \cos(\frac{\beta_{sig}}{2})e^{j(\beta_{sig}/2+\gamma_{sig})}] \end{aligned} \tag{6.8}$$

If $\gamma_{sig} = \frac{\pi}{2} + \frac{\alpha_{sig}-\beta_{sig}}{2}$, the above transfer function can be simplified to:

$$\vec{E}_{out} = \frac{\vec{E}_{in}}{2}e^{j\alpha_{sig}/2}[\cos(\frac{\alpha_{sig}}{2}) + j \times \cos(\frac{\beta_{sig}}{2})] \tag{6.9}$$

Compared to the BPS with a dual-arm drive, the single-arm version has an extra phase shift term $e^{j\alpha_{sig}/2}$. As shown in Fig. 6.5, when sweeping the heater power $PI = \frac{\alpha_{sig}}{\pi}P_\pi$ and $PQ = \frac{\beta_{sig}}{\pi}P_\pi$, we can still get a continuous phase change at the output of BPS, but at the cost of some dead zone where the output phase doesn't change. Since the dead zone can be predicted in advance by an already known applied drive signal, its effect can be mitigated by adjusting the control code to maintain a continuous phase.

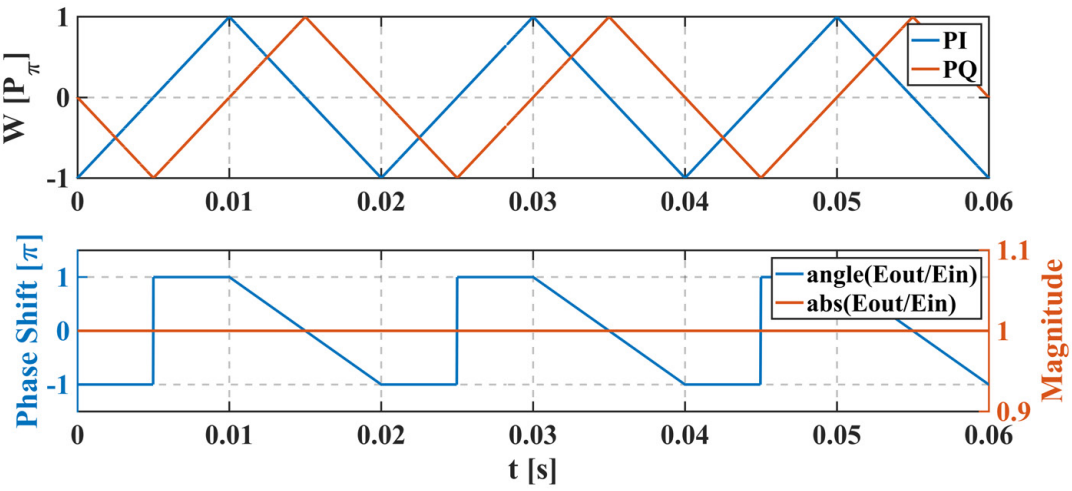


Figure 6.5: Response of BPS by driving single-arm of MZM.

6.3 Design of the Coherent-Lite Receiver

To demonstrate the function of the phase compensation loop in the laser-forwarding coherent links, a 16Gbps electro-photonic coherent receiver was designed in the monolithic silicon photonic process.

Receiver Architecture

The architecture of the coherent-lite receiver is shown in Fig. 6.6, in which the photonic and electronic circuits are closely integrated with less than $5\mu m$ distance.

On the photonic side, signal and LO light are coupled into the chip through two grating couplers and propagate along the silicon waveguide. The LO light then passes through the boundless phase shifter, which is built by adiabatic couples [90] and the PDK thermal phase shifter with the undercut. It finally beats with the signal light through another 2x2 adiabatic coupler, hits the balance photon detector(BPD), and generates the demodulated current.

On the electronic side, the clock path consists of a current mode logic (CML) clock receiver and clock distribution network, which provides an 8GHz low-jitter clock. In the data path, the electrical current from BPD is fed into the inverter-based trans-impedance amplifier (TIA) for current-voltage conversion, which is then converted to a differential signal by the post-amplifier. A dummy TIA connected to the dummy BPD is employed to provide common-mode voltage and suppress supply noise at the cost of degraded Rx sensitivity due to increased noise power. The amplified analog signal is quantized by the even and odd sampler array at half-rate to reduce power consumption. Two samplers in each array operate as data and error samplers, whose functions will be introduced later. 8-bit voltage DACs

provide different threshold voltage to each sampler for offset compensation and eye sweep. The quantized half-rate data are sent to the digital backend for further deserialization and BER checks. The 10-bit power density modulation (PDM) logic is also synthesized inside the digital backend and used to drive the on-chip PDM driver, thus compensating for the phase fluctuation in laser-forwarded links through BPS.

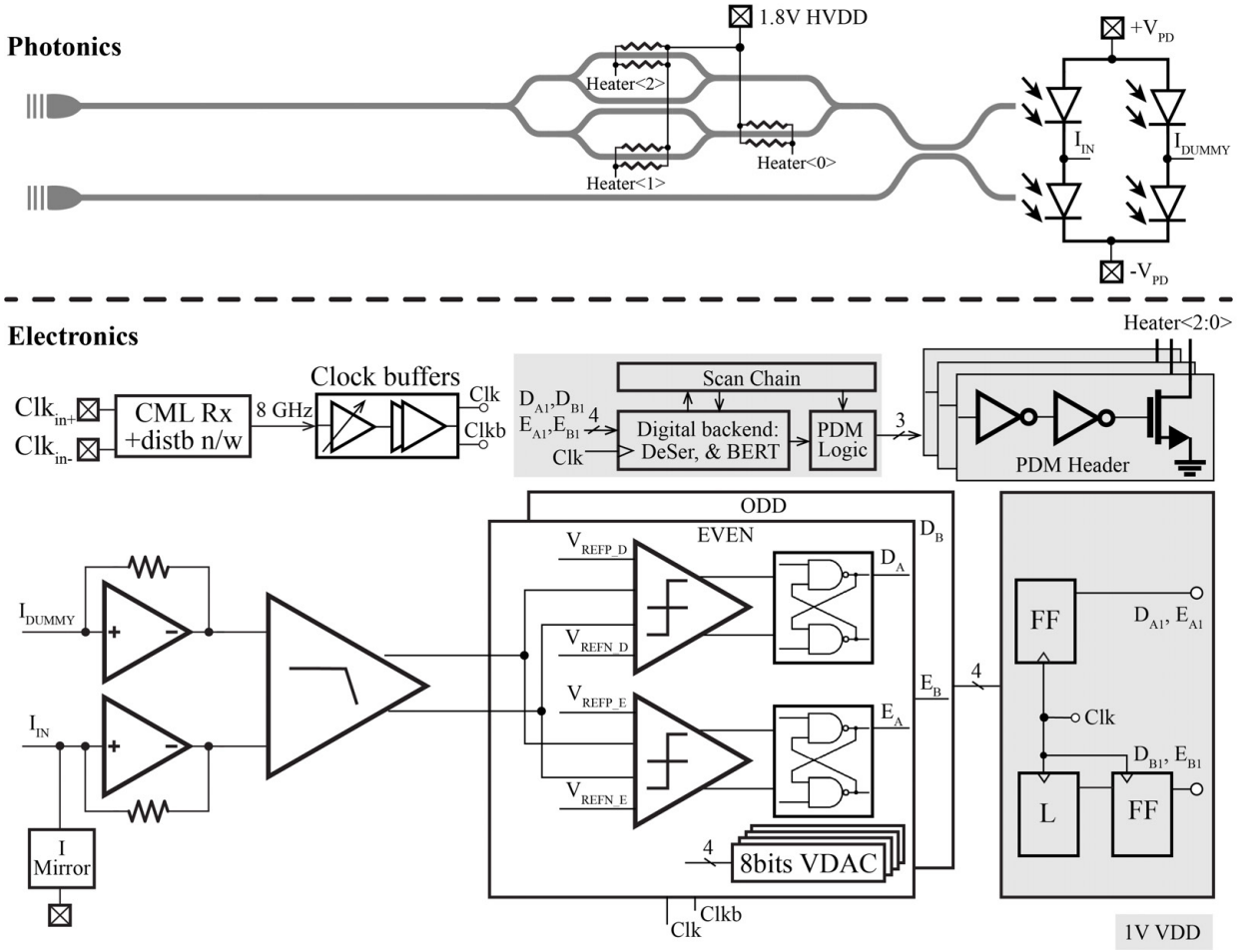


Figure 6.6: Architecture of the coherent receiver

The receiver has three supply domains: 1V VDD, 1.2V AVDD, and 1.8V HVDD, which are used for the digital core, analog front-end and clock network, and heater resistor, respectively.

dLev-based phase tracking mechanism

In analog signal-based coherent-lite receivers, besides the BPS used for phase control, another critical block, a phase estimator that can filter out modulated data and estimate the phase error, is required. Two different phase estimators were proposed and demonstrated in DSP-free coherent receivers [28, 29, 82]: the conventional Costas loop requires linear and wideband analog multipliers, and the multiplier-free XOR-based Costas loop relies on precise delaying and adding the in-phase and quadrature components [91]. Furthermore, both architectures require the analog processing circuits to operate at the full rate, causing a large power consumption.

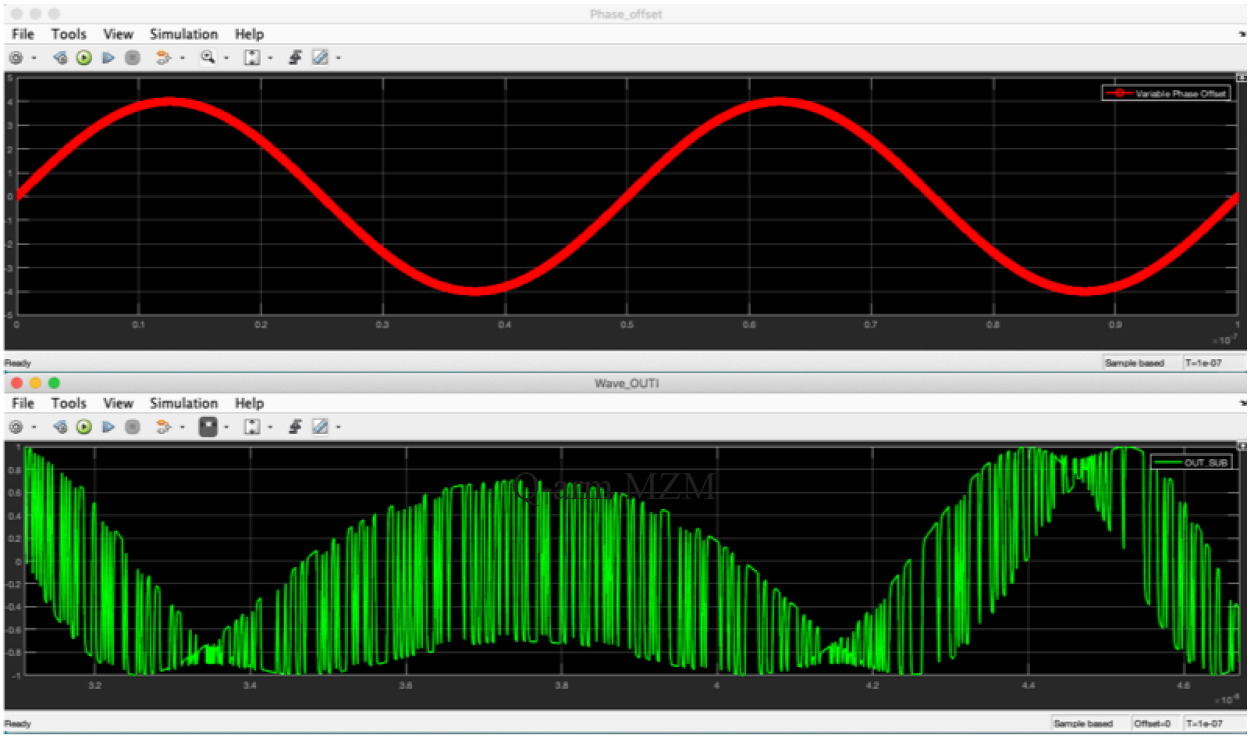


Figure 6.7: System simulation of the optical link under the impact of the phase fluctuation: Injected sinusoidal phase fluctuation (top) and the corresponding demodulated transient data (bottom).

We proposed a dLev-comparator-based phase estimator that can be easily implemented in the laser-forwarded coherent link under BPSK modulation and only consumes little power due to low-rate operation. To understand its operation principle, we need to revisit the output current of the laser-forwarded coherent receiver by updating Eq. 3.3 to:

$$I_{out} = R(P_1) - R(P_2) = 2R\sqrt{P(1-P)} \times P_{laser} \times \cos[\phi_m(t) - \Delta\phi(t)] \tag{6.10}$$

where the delay difference $\Delta\phi$ between two optical paths is not constant but a time-varying value. Assuming the PRBS phase modulation in the transmitter is $\phi_m(t) \in [0, 3\pi/4]$ and the slow phase fluctuation $\Delta\phi$ is a sinusoidal waveform with 2π range, we can plot the output current, shown in Fig. 6.7. The time-varying current swing can be understood by treating the phase fluctuation as a bias term that changes the effective gain of the cos function. Therefore, the phase fluctuation can be compensated by locking the current swing $I_{out,pp}$ to the maximum value.

Then, let's look back to the receiver architecture of the proposed receiver shown in Fig. 6.6. In each interleave stage (even and odd), there are two samplers: one is a data sampler used to perform data quantization and deserialization, while the other operates as a dLev comparator with a tunable threshold voltage whose output is processed by digital back-end to extract signal swing. Since the $\Delta\phi$ changes very slowly ($< 100kHz$), the dLev comparator from different interleaving stages does not need to be turned on simultaneously, which can further reduce power. Finally, the on-chip finite state machine (FSM) generates real-time PDM control codes for BPS based on the measured signal swing.

Comparator

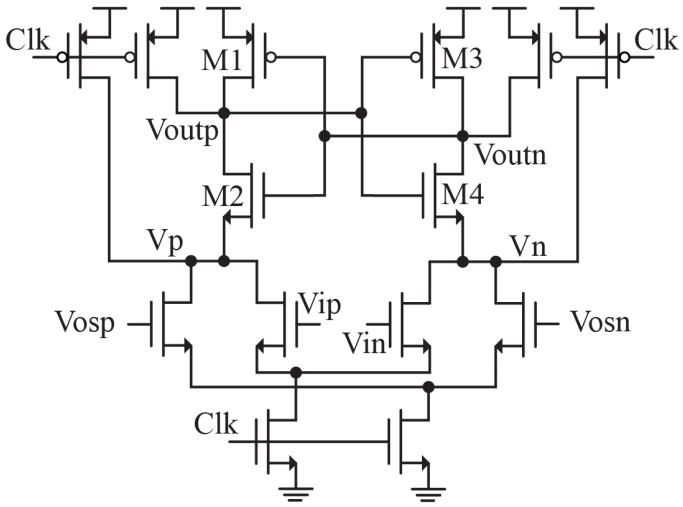


Figure 6.8: Schematic of the comparator.

Comparators are used everywhere in electronic circuits where the analog voltage needs to be converted to digital outputs. One class of comparators, dynamic comparators, first amplifies a static input voltage by converting it to current and integrating it on a capacitor over a well-defined time window. The amplified voltage is then fed into the regenerative latch to be further amplified to a binary signal. Compared to the comparator based on a cascade

of high-gain amplifiers, the dynamic comparator consumes zero static current, making it popular in different applications.

The StrongArm [92] and Double-Tail [93, 94] are two typical structures of dynamic comparators, have been systematically analyzed [95]: The StrongArm latch, a single-windowed integrator followed by a regenerative latch, is the most efficient comparator architecture but requires a well-controlled input common-mode voltage and a minimum supply voltage. The double-tail comparator is better when low supply or input bias is unsuitable since its complementary preamplifier offers a built-in level shift.

Therefore, StrongArm architecture is employed in our comparator design, shown in Fig. 6.8, where the auxiliary input pair driven by $Vosp$ and $Vosn$ is used for offset compensation and eye monitor. The voltage integrated on node Vp and Vn through the current difference between two differential pairs triggers the evaluation of the cross-coupled inverter composed of M1-4 to get a digital out.

Voltage DAC

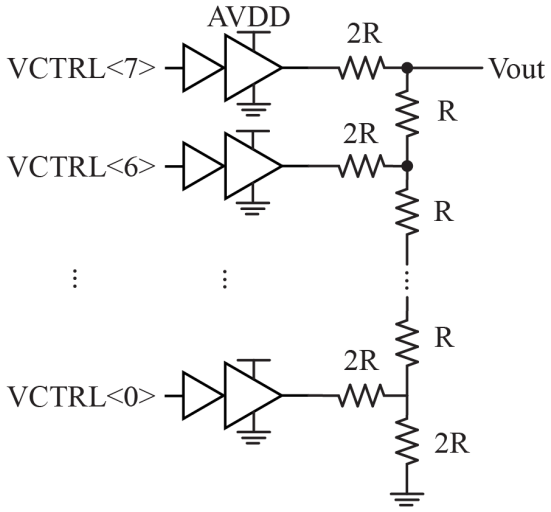


Figure 6.9: Schematic of the voltage DAC

Voltage DACs are designed to provide a reference voltage to compensate for the dynamic comparator's voltage offset and assist the comparator with an eye sweep. As shown in Fig. 6.9, the 8-bit binary control signal drives the R-2R resistor ladder through the inverter. One key metric of DAC is the linearity. To ensure that the output voltage of VDAC can settle within 10ns for close-loop phase compensation, the unit resistor with $R = 27K\Omega$ and $510\mu m$ is adopted to trade-off area and local mismation of resistor unit.

As we can observe from the differential non-linearity (DNL) simulation result shown on the left of Fig. 6.9, the VDAC output voltage is monotonic over most control codes except

the middle code where the transition of the most significant bit (MSB) occurs. Since the condition of $|DNL| > 1$ only occurs once over the whole control code, it can be known in advance by the control algorithm and thus skipped. From the 100-sample Monte-Coar (MC) simulation, we can find that the mean of the worst DNL is -0.2 with a standard deviation of 0.47. The transient simulation of VDAC shows that the worst settling time is $5.93ns$, which is fast enough for the requirement of control loop.

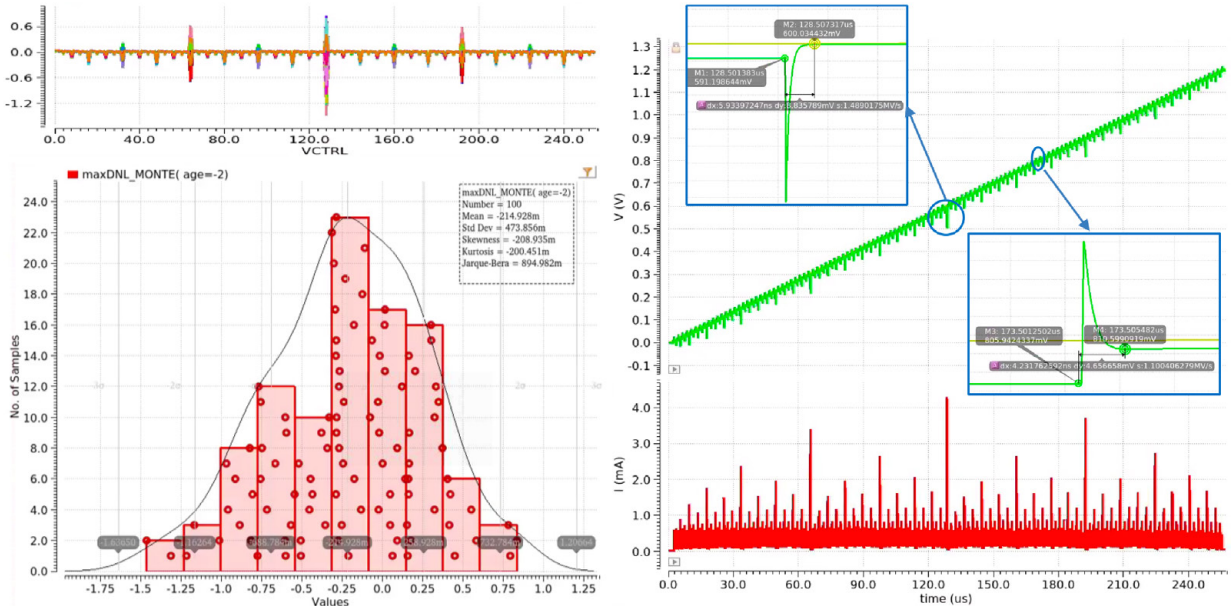


Figure 6.10: Post-layout simulation result of VDAC: DNL at different process corners and max DNL over MC (left) and transient settling simulation of VDAC.

Thermal phase shifter and PDM driver

The thermal phase shifter unit is another key component of this electro-photonic system. The one supported in the monolithic silicon-photonic process uses N+ RX silicide resistors to generate heat in the rib waveguide to produce a phase shift of the light. To improve the heater efficiency, the phase shifter is designed with a horse-shoe shape to concentrate the heat. Furthermore, the sealed undercut technique, which creates an air gap under the BOX to increase the thermal resistance from the device to the silicon substrate, is utilized.

The layout view of the horse-shoe shape phase shifter is shown in Fig. 6.11, where the N+ silicide resistors are located on the two sides of the rib waveguide. Its resistance can be calculated by the following equation:

$$R = \frac{R_s L + 2R_{end}}{W} \tag{6.11}$$

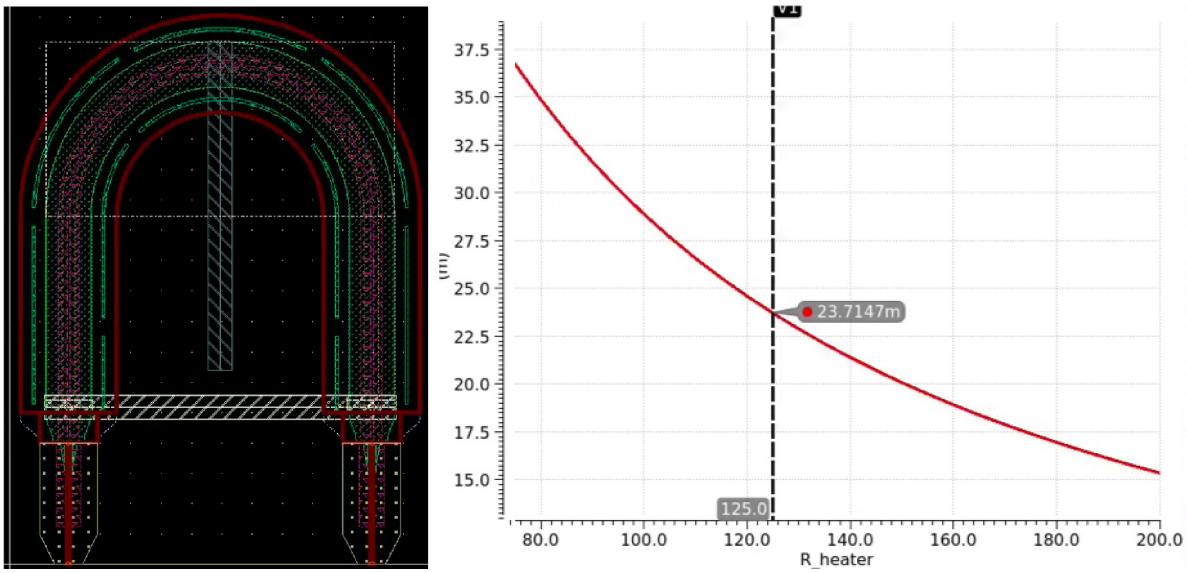


Figure 6.11: The layout of the thermal phase shifter (left) and the maximum power that can be delivered from the heater driver (right).

where R_s and R_{end} are sheet and end resistance, and W and L are resistor size. Based on the process information provided in the PDK, we can derive the resistance value as 125Ω. Meanwhile, we can find that the maximum heater power delivered from the heater driver to this heater resistor is about 23mW, which can provide more than 3π phase tuning range under the assumption of $P_\pi = 7mW$.

6.4 Realization and Experiment Results

Chip micrograph and package scheme

The integrated electro-optic receiver chip was fabricated using 45SPCLO process, a 45nm CMOS-Silicon Photonic 300mm high-volume manufacturing platform developed by Global-Foundaries for next-generation, low power, and high-speed optical interconnects [59]. The micrograph of the 2 x 1mm receiver chip is shown in Fig. 6.12, including two coherent receiver units and two standalone boundless phase shifter test structures. In each optical coherent receiver, the signal and LO light are coupled into the chip through two grating couplers (GC) among the GC array with 127um pitch. Since mechanical stability is critical in coherent optical experiments, the multiple-channel fiber array will be aligned to GC, attached, and glued during experiments. Before conducting a complex optical package for the coherent experiment, the IMDD experiment can be performed to verify the function of the whole electric part by coupling light to the GC, which is connected to the dummy BPD,

through a single fiber probe.

The standalone boundless phase shifters, which are put on the side of the chip and are the same as the ones used in the coherent receivers, can be used for phase and power characterization before performing the close-loop experiment.

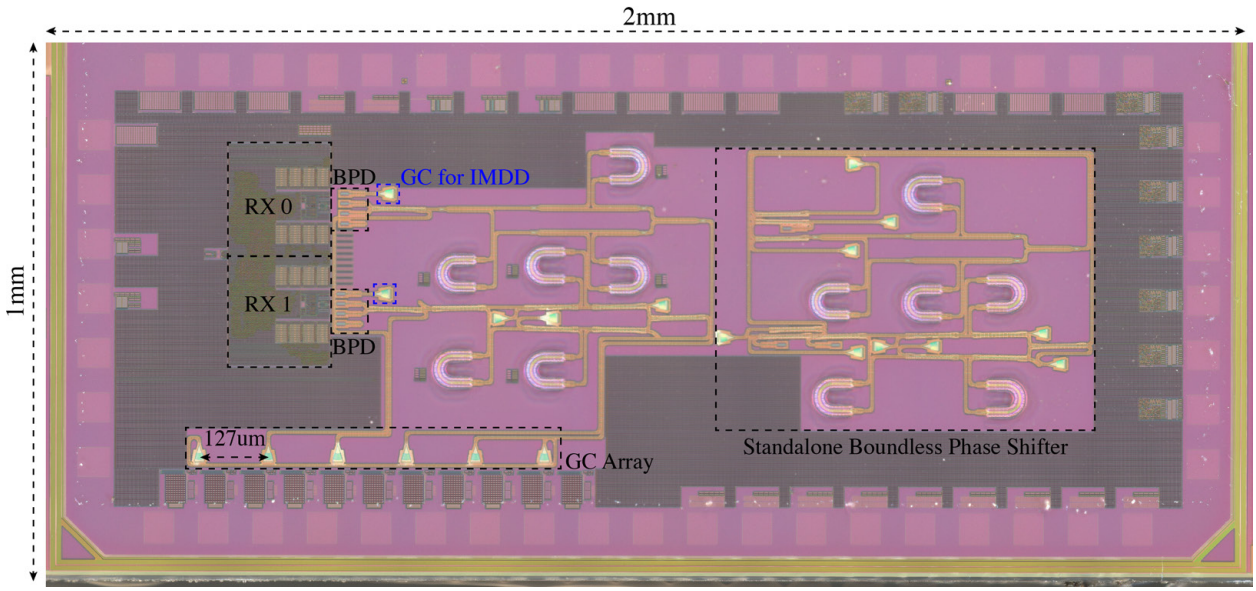


Figure 6.12: Microgarph of the coherent receiver.

Fig. 6.13 shows the package schemes for different experiments. The test chip is wire-bonded on the PCB, where the DC and RF signals are connected to rectangular pin headers and high-speed SMPS connectors, respectively. Two package schemes are adopted: in the top one, all signal pads are wire-bonded for standalone device characterization and probe-only optical experiments, while in the bottom one, the pads on the bottom row are left open to leave enough space to land fiber array for coherent experiments.

Characterization of the standalone device

To characterize the standalone boundless phase shifter, we must first characterize the thermal phase shifter used in each MZI structure to determine the initial bias point. The test setup is shown in Fig. 6.14, where light is coupled in and out from the chip through two auxiliary grating couplers around one MZI. One terminal of the heater resistor in the thermal phase shifter is connected to the ground, while the other terminal is connected to the PAD and driven by the heater driver. The heater driver is controlled by FPGA with a power-density modulated (PDM) signal. Therefore, the heater power can be linearly controlled by the control code (H_{code}), and the power delivered to the heater can be expressed as:

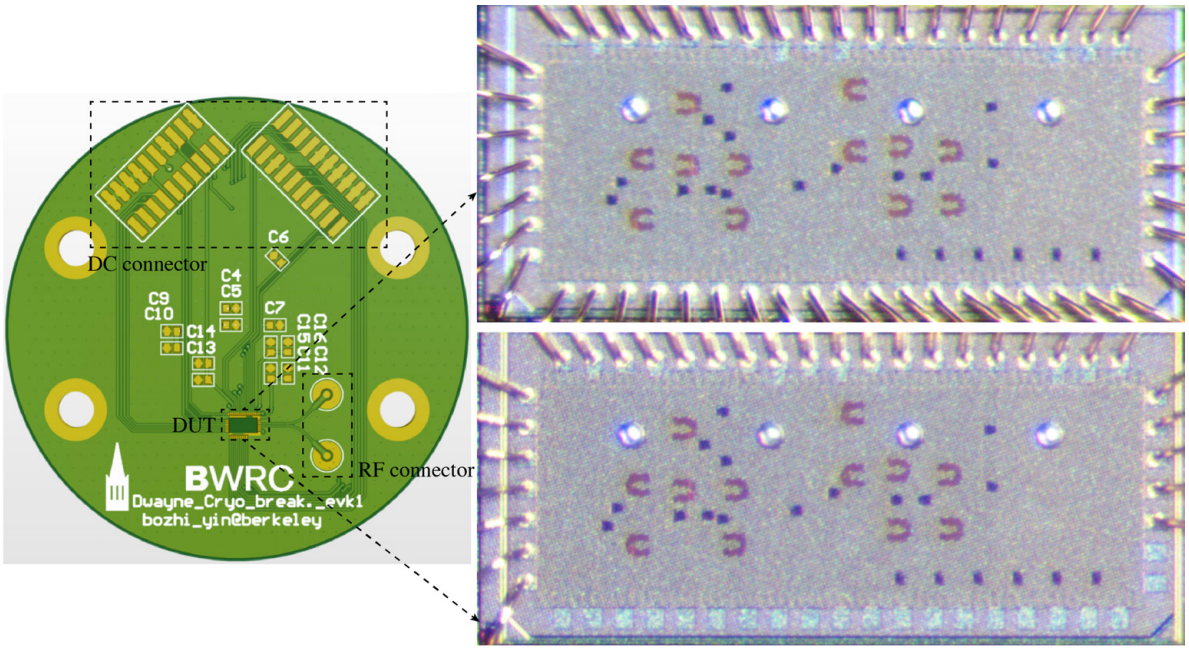


Figure 6.13: Package schemes of coherent receiver for standalone and IMDD experiments (Top) and Coherent experiments (Bottom).

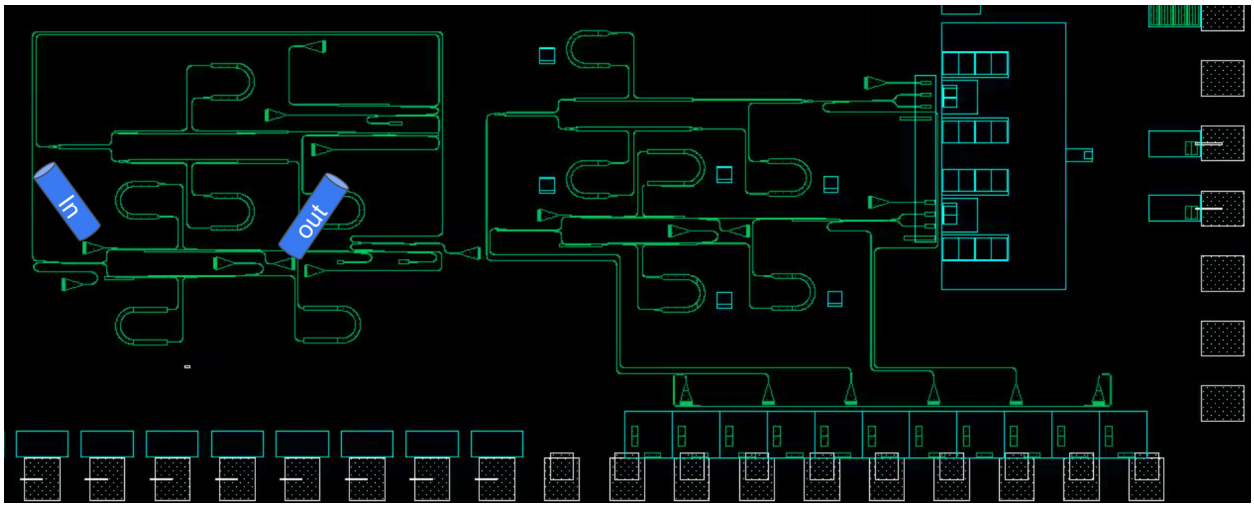


Figure 6.14: Characterization setup of thermal phase shifter unit.

$$P = (\frac{HVDD}{R_{heater} + R_{drv}})^2 * R_{heater} \times \frac{H_{code}}{max(H_{code})} \tag{6.12}$$

where R_{heater} is the heater resistance value (160Ω) and R_{drv} is the output impedance of the heater driver, H_{code} is an 8-bit binary control signal with a maximum value of 255. HVDD is the adjustable supply voltage for heater power range control. By sweeping the PDM control code, we can observe the power transmission followed by Eq. 6.3, shown in Fig. 6.15. The more than 30dB extinction ratio between constructive and destructive interference indicates that the splitting ratio of the rapid adiabatic coupler is better than $50 \pm 1\%$. The phase response extracted from the power transmission with Eq. 6.3 is also shown in Fig. 6.15. According to the datasheet of the heater driver, its output impedance (R_{drv}) is roughly 20Ω when $HVDD = 2.4V$. Therefore, the $P\pi$ of the thermal phase shifter is 9.3mW, slightly larger than the value (7mW) reported in the PDK. One possible reason for this difference is that the heater terminal is directly connected to the PAD through high-level metal and eventually bonded to PCB for driving, which provides a path to thermal ground with low thermal resistance and degrades heater efficiency. When the heater is driven by an on-chip PDM driver, the thermal efficiency can be improved.

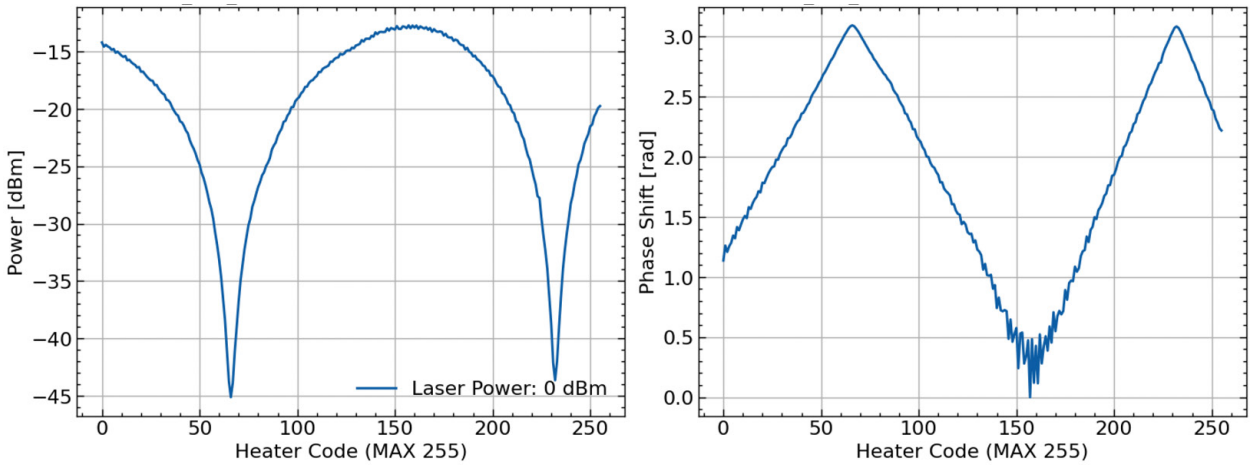


Figure 6.15: Characterization result of thermal phase shifter unit under 2.4V HVDD: transmission of MZI (left) and response of phase shifter (right).

IMDD link test

The IMDD test setup is shown in Fig. 6.16. A Mach-Zehnder modulator (MZM) made of lithium niobate (LiNbO3) and featuring a 25-GHz electro-optic bandwidth modulates a 1310 nm continuous-wave (CW) input laser using a pseudorandom binary sequence (PRBS) of $2^{31}-1$. The data for this modulation is produced by a pattern generator and is subsequently amplified to an adequate level using a power amplifier (PA). 90% of the modulated optical light is coupled to the receiver after passing through a polarization controller, while the other 10% power is fed to the oscilloscope for real-time monitoring. The measured optical

eye diagram, with an 8dB extinction ratio (ER), is shown on the right of Fig. 6.16. Therefore, by measuring the average current I_{AVG} flowing through the PD from SMU, we can calculate the optical modulation amplitude (OMA) of the light received by the receiver with the following equation:

$$OMA = 2 \times I_{AVG} \times \frac{10^{ER/10} - 1}{10^{ER/10} + 1} \tag{6.13}$$

With the above method, we don't need to figure out the coupling loss and responsitivity of PD, which are largely impacted by test setup and process variation, respectively. Furthermore, the clock synthesizer also generates a half-rate differential clock with a tunable delay to the receiver for deserialization.

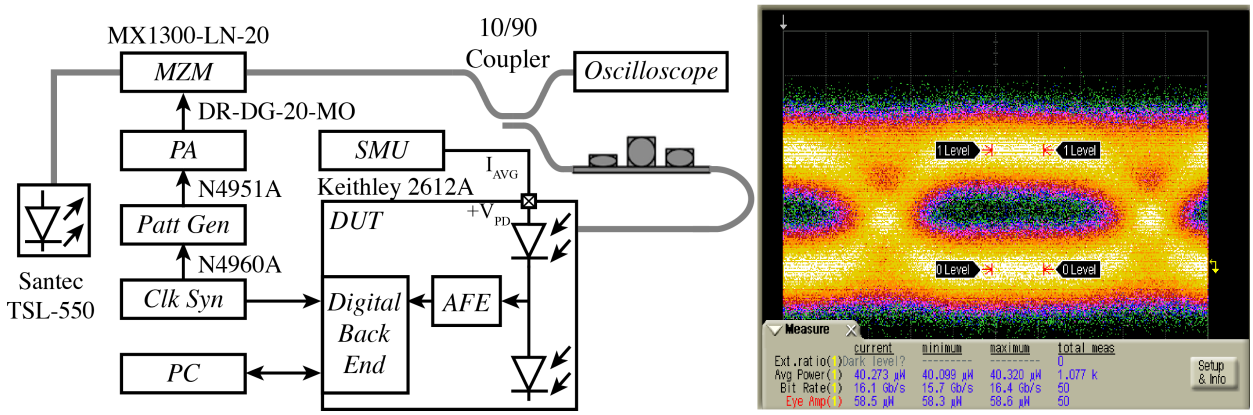


Figure 6.16: IMDD test setup (left) and the 16Gbps optical TX eye diagram (right).

By sweeping the clock delay and the threshold voltage of the on-chip sampler, we can get the statistical eye by counting the ratio of 1 in the digital back end. Since the receiver's input is a PRBS pattern with a balance of 0 and 1, the ratio of 1 is close to 0.5 at the center of the eye and only changes around the edge of the eye diagram. Compared to the BER-based eye-opening monitor (EOM) measurement, this method reduces the testing time and doesn't require the BER checker to be fully functional. The measured 4Gbps and 16Gbps statistical eye diagrams are shown in Fig. 6.17. The rise and fall times are longer than expected, indicating the slightly low bandwidth caused by the process variation.

The BER is measured at different laser power for sensitivity tests. As shown on the left in Fig. 6.18, the minimum required OMA to achieve $BER < 1e-12$ is roughly -13dBm. Fig. 6.18 also show the bathtub plot, in which about 0.1 UI time margin can be observed for $BER < 1e-12$ and $OMA = -13dBm$.

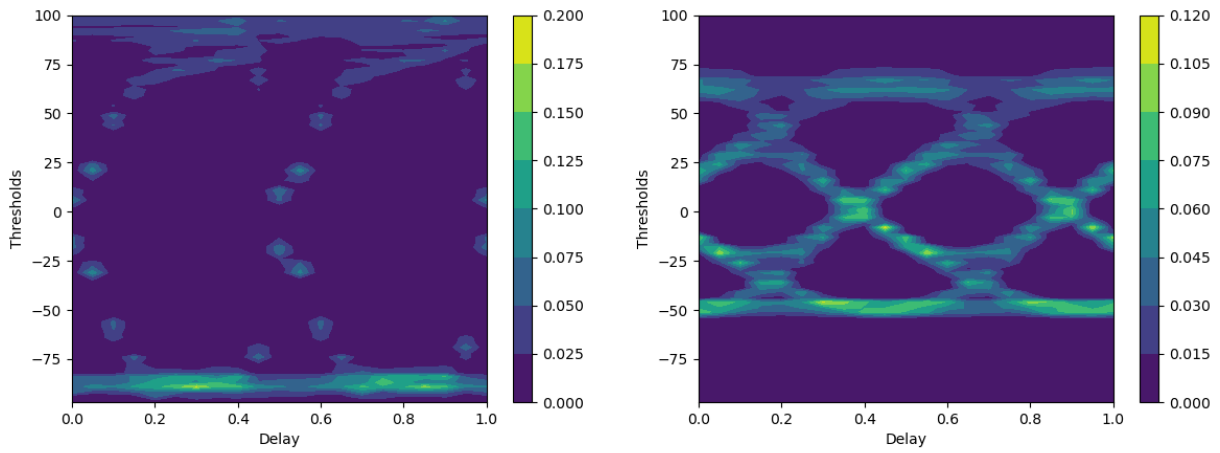


Figure 6.17: Measured statistical eye diagram at 4Gbps (left) and 16Gbps (right).

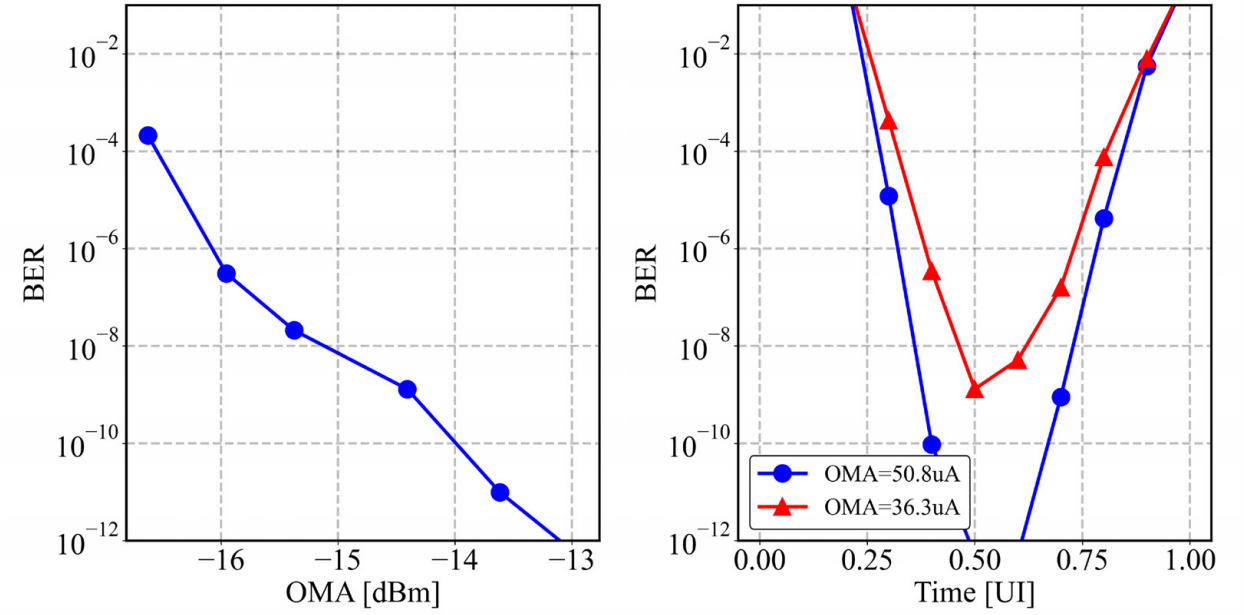


Figure 6.18: Sensitivity (left) and Bathtub plot (right) of the IMDD receiver at 16Gbps.

6.5 Summary

In this Chapter, we briefly introduce the time-varying phase fluctuation issue in the laser-forwarded coherent link. To resolve this issue at low design complexity and power, we proposed an EOPLL, including a dLev comparator-based phase estimator and a thermal

boundless phase shifter-based phase rotator. A 16Gbps half-rate coherent receiver is implemented in the monolithic silicon photonic process (45SPCLO) to verify this idea. The measurements finished so far suggest that the key photonic components, whole electronic analog front-end, and digital back-end work as expected: receiver shows less than -13dBm sensitivity at $BER = 1e - 12$ when configured as IMDD link.

Chapter 7

Final Thoughts and Conclusions

7.1 Key Contributions

Superconductor electronics outperform other beyond-CMOS technologies in terms of energy efficiency and have become strong candidates for future supercomputing systems. However, the lack of high-density superconductor memory and the heat-leak path of traditional electrical links prevent the scale of superconductor computing systems. This work presents a novel cryogenic optical link, based on the monolithic silicon photonic process and laser-forwarded coherent architecture, to address this issue and unlock the door to building large-scale superconductor computing systems.

The main contribution of this thesis can be organized as follows:

- A comprehensive link model is built to analyze the performance and energy efficiency of the cryogenic optical link consisting of superconductor electronic and semiconductor electronic/photonic components.
- A full device characterization of transistors from two monolithic silicon photonic processes is presented, along with the theoretical analysis, paving the way for analog, mixed-signal circuit design at cryogenic temperatures.
- A micro-ring modulator-based cryogenic optical transmitter is designed and implemented in the 45RFSOI process. Full link characterization at cryogenic temperatures with the direct drive from superconductor IC demonstrates the transmitter's function, performance, and energy efficiency.
- Proposed an EOPLL to compensate for the inevitable time-varying phase offset in the fiber-based self-homodyne coherent receiver. A 16Gbps coherent receiver is designed and implemented in the 45SPCLO process to demonstrate this idea.

7.2 Future Directions

The energy-efficient cryogenic egress link design can be used not only for superconductor computing but also for the control interface in quantum computing, which has become an active research area in recent years. The presented cryogenic optical transmitter is a first proof-of-concept demonstration, which still has room to improve:

- The device characterization result presented in this work can be utilized to build an accurate compact model at cryogenic temperature. With that, the bandwidth of the integrated amplifier can be further co-optimized with the modulator to rebalance and improve energy efficiency.
- The 17.56dB fiber-to-chip coupling loss in the demonstrated cryogenic transmitter significantly degrades the system's energy efficiency. The on-chip fiber-attach solution with self-aligned structures, supported in the 45SPLCO process, can greatly improve the stability of fiber coupling and reduce coupling loss to 3dB [77], which could improve the energy efficiency to 100.6fJ/bit if used.
- The analog pre-amplifier in the current cryogenic transmitter design could be replaced with a dynamic amplifier with high regeneration gain, especially for large arrays in which the power of generating and distributing the clock can be amortized.

Then, the laser-forwarded coherent-lite receiver is also a popular candidate in short-reach optical links due to its energy efficiency. Due to time limitations, the designed proof-of-concept receiver has not been fully characterized yet. Besides the chip characterization, some directions can be explored:

- Since the phase offset in the self-homodyne link changes very slowly, the error sampler used to extract signal swing can operate at a very low speed or use an analog peak detector to reduce power consumption.
- It's also worthwhile to check the wavelength dependency of time-varying phase offset. It has been demonstrated that the feedback control signal for phase compensation can be applied to two laser tones with 100GHz channel spacing [81]. If the accepted wavelength window is large enough, we can combine the benefit of both laser-forwarded coherent link and DWDM to improve throughput further.
- One drawback in the current EOPLL demonstration is the 6dB intrinsic loss of the boundless phase rotator, which degrades the energy efficiency of the whole link. The lossless phase rotator design could be a promising direction.

Finally, although the focus of this work is the cryo-CMOS interface for superconductor computing, the author wants to point out the evolution of superconductor electronics:

- Certainly, energy consumption per bit in SFQ is lower by one or two orders of magnitude compared with all other perspectives technologies beyond CMOS, and so is the extrapolated power consumption by future supercomputers even including the cryocooling overhead when compared with semiconductor computer technologies at the exascale performance level of 10^{18} floating point operations per second (flop/s) [18].

- The major disadvantage of RSFQ logic circuits has been the large SQUID cell size, severely limiting the integration level. Compared to the semiconductor process in 2020, the gate set area of SCE is 25000× larger. If we ignore the difference in device fabrication and compare the gate size to CMOS with an equivalent feature size of 350nm, there is still a 60× difference [4]. Therefore, whether superconductor electronics can scale as semiconductor counterparts becomes one of the key questions that need to be answered.

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