Cryogenic and RF Performance of Negative Capacitance Field-Effect Transistors

Aditya Varma

Electrical Engineering and Computer Sciences
University of California, Berkeley

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by

Aditya Dev Varma

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Committee in charge:

Professor Sayeef Salahuddin, Chair
Professor Ali Niknejad

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University of California, Berkeley

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Abstract

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Negative capacitance (NC) field effect transistors have received significant research interest in CMOS electronics for their ability to increase the intrinsic device capacitance (C_{gg}) and transconductance (g_m) without degradation to carrier transport, while maintaining a high degree of CMOS compatibility due to the use of HfO_2 and ZrO_2 thin-film dielectrics. In this thesis, we expand upon two aspects of the current research on this emerging device technology. First, cryogenic RF and DC measurements are performed on p-type NCFETs on a silicon-on-insulator (SOI) platform. The maintenance of NC performance enhancements at 77 K in p-type devices is confirmed, along with substantial increases in g_m, indicating the attractiveness of NCFETs for fully complimentary, low-temperature logic and mixed-signal circuit design. Furthermore, an in-depth analytical study of the RF noise performance of negative capacitance FETs is performed, in order to understand how the recovery of the cutoff frequency (f_T) from parasitic capacitance suppression affects RF noise. We find favorable scaling trends in the minimum noise figure NF_{min}, noise measure N_M, and noise sensitivity R_n when compared to the scaling performance of interfacially thinned dielectrics. Future work and applications of NCFETs in integrated circuit design are discussed in closing.

यो न हृष्यति न द्वेष्टि न शोचति न काङ्क्षति
शुभाशुभपरित्यागी भक्तिमान्यः स मे प्रियः ॥ 17 ॥
Bhagawan Sri Krishna, *Bhagavad Gita*, Chapter 12 Verse 17

This thesis is dedicated with love to Ramesh K. Verma.
1937 - 2021

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Acknowledgments

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I am most grateful for the mentorship and collaboration I received from Nirmaan Shanker, who taught me how to conduct RF/cryogenic measurements and offered significant amounts of his time to assist my research. In addition, I would like to thank Suraj Cheema, whose encouragement to explore new applications of NCFETs served as inspiration to follow novel lines of research and inquiry. I would also like to extend my sincere appreciation to Mohamed Mohamed, who supervised my internship at MIT Lincoln Laboratory in the summer of 2023, and who went out of his way to support my research. I would also like to highlight the members of the NC subgroup - Jong Ho, Chirag, Koushik, Chia-Chun, Junhao, Urmita, Yejin, and Sophia - for making the group a welcoming and exciting place to be a graduate student. A thanks is also due to my peers Kevin Lu (with whom I have survived much of the Berkeley EECS curriculum) and Ashwin Rammohan for several helpful exchanges regarding RF modeling.

Finally, I would like to especially thank my family for their unconditional love and support throughout five often tumultuous years at the University of California, Berkeley. Their encouragement, patience, and full faith has been instrumental to the completion of this thesis.

Chapter 1

Introduction to HfO_2-ZrO_2 (HZH) Negative Capacitance FETs

In the relentless march towards low-power, high density electronics, the insulating layer in modern transistors - often referred to as the 'gate dielectric' or 'gate stack' - has been a crucial driver of improved electronics performance. The gate dielectric functions as a capacitor within the MOSFET device structure, allowing a voltage applied to the gate terminal to modulate the amount of charge in the channel [36]. For logic applications, the MOSFET is operated as a digital switch, with conducting and insulating channel states allowing implementation of complex logic functionality [46]. These two states of the MOS device can be indicated by an absolute current level, sometimes referred to as I_{on} and I_{off}.

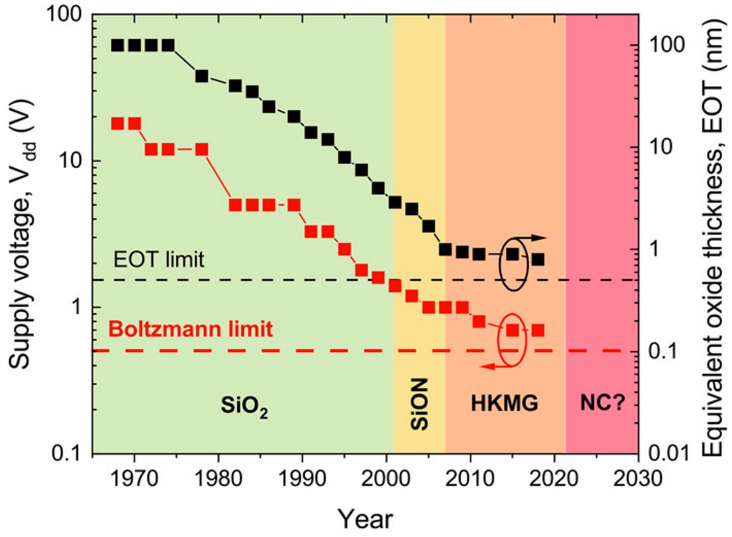

Figure 1.1: Scaling trend of effective oxide thickness (EOT) vs power supply V_{dd}. Figure Credit: [34]

From first principles, current is proportional to charge, and the channel charge is determined by the gate dielectric capacitor via $Q = C \times V$ [36, 54]. This means that improving the ability of the capacitor to control the channel charge (e.g. its permittivity, or dielectric strength κ) can reduce the needed gate voltage V_{ov} to achieve a current of I_{on}. Since the power supply is lower bounded by a multiple of V_{ov} [46], reducing the gate voltage shows a path to reduce the overall operating voltage, thus lowering CMOS power consumption. Figure 1.1 shows the historical efficacy of this trend.

In the 1990s, Intel and other semiconductor manufacturers began to look beyond silicon's natural dielectric - SiO_2 - and examined different materials systems for better dielectric performance [7]. Of particular promise were two binary oxides - HfO_2 and ZrO_2 - that could be integrated in a CMOS-compatible fashion to increase the effective dielectric constant (κ). Since capacitance is given as $\kappa\epsilon_0\frac{A}{T_{ox}}$, using a material with a higher κ than SiO_2 can improve the capacitance. This idea has led to the notion of effective oxide thickness (EOT). For a given non-SiO_2 material, the EOT states how thick an SiO_2 layer needs to be to produce an equivalent capacitance. The CMOS-compatibility of HfO_2 and ZrO_2 has led to the integration of the high-κ metal gate (HKMG) into modern transistors, which has been a primary mechanism of MOSFET improvement in the 2000s. This has enabled modern transistors with high-κ dielectrics to achieve an ultrathin 9.5 Å EOT [41, 13], where it has remained for several years.

In the years 2011-2012, it was discovered that HfO_2 [8] and ZrO_2 [43] films exhibit ferroelectricity. Ferroelectricity describes a material's tendency to spontaneously polarize in response to an electric field; two key properties include that this polarization is switcheable by applying an electric field in the opposite diection, and that a ferroelectric material will remain polarized even after the removal of the external electric field. The discovery of ferroelectricity in this materials system enabled the possibility of negative capacitance (NC) transistors in silicon CMOS, which will be explained below.

1.1 Landau Theory of Negative Capacitance

The central idea behind negative capacitance in a transistor is as follows: suppose we have the MOS device structure in Figure 1.2.

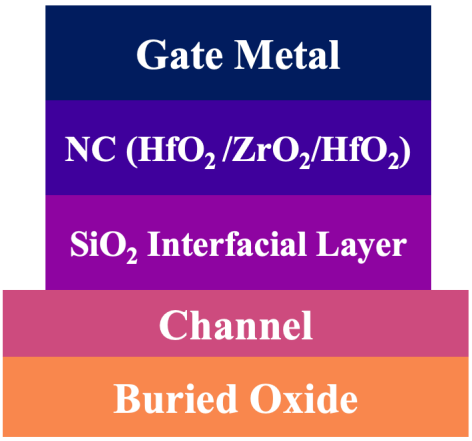

Figure 1.2: Cross-sectional schematic of a silicon-on-insulator (SOI) gate-stack transistor with a negative capacitance (NC) dielectric.

The total capacitance of the dielectric layers (the NC layer plus the SiO_2 layer) is given by a series capacitor equation:

$$\frac{1}{C_{total}} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{NC}} \tag{1.1}$$

The corresponding effective oxide thickness (EOT) equation is:

$$EOT_{total} = EOT_{SiO_2} + EOT_{NC} \tag{1.2}$$

Now, suppose that the capacitance $C_{NC} < 0$ or equivalently $EOT_{NC} < 0$. Then equation 1.1 implies:

$$C_{total} = \frac{|C_{NC}|C_{SiO_2}}{|C_{NC}| - C_{SiO_2}} \tag{1.3}$$

where the more negative C_{NC} is, the larger the capacitance. Similarly, equation 1.2 would read [29]:

$$EOT_{total} = EOT_{SiO_2} - |EOT_{NC}| \tag{1.4}$$

which suggests the effective oxide thickness can be reduced without any physical thinning of the overall dielectric layer. This begs the question - how can we realize a dielectric layer with a negative EOT? One means of doing so is by manipulating a material's ferroelectricity[1].

[1]The original theory of negative capacitance in a ferroelectric material can be attributed to Rolf Landauer in the 1960s [38]; the first presentation of adapting this idea for integration into a MOSFET was presented by Salahuddin and Datta in [47].

We will adopt the Landau free energy landscape view in order to explain how to realize such an effect (Figure 1.3).

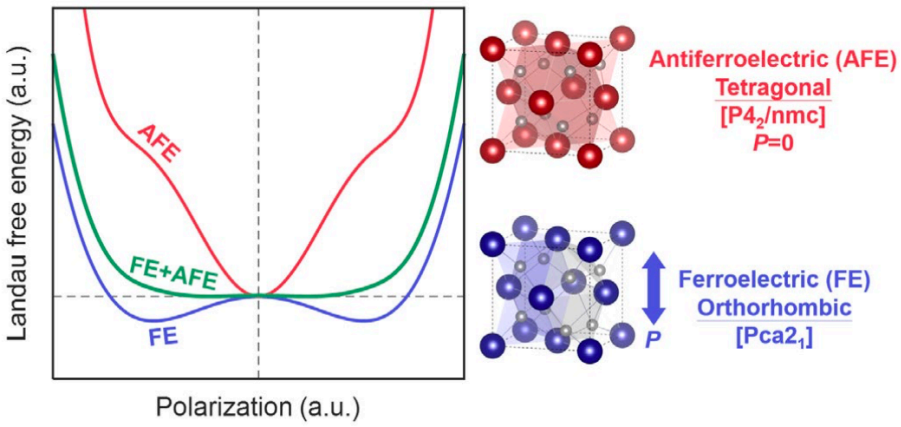

Figure 1.3: Free energy landscape of a mixed order ferroelectric-antiferroelectric (FE-AFE) system. Figure Credit: [39]

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The energy landscape of a ferroelectric material is in blue. The two minimal energy states correspond to the polarized states of the ferroelectric material, which explains why the materials remain polarized even without an externally applied electric field (i.e. these states are energetically stable). Capacitance is related to the concavity / convexity of these free energy curves - a convex energy landscapes (like the two polarized states) represent positive capacitance. However, the transition region between the two stable states has a *concave* characteristic – indicating a negative capacitance. However, this region is very energetically unstable, and the presence of any charge will shift the material into one of its two stable states.

Now we can consider what happens if we add a second material that has antiferroelectric properties (essentially, a material that strongly disfavors the two stable states of the ferroelectric material). As shown in Figure 1.3, the overall energy landscape can be flattened, as represented by the green curve. This composite curve manages to stabilize the ferroelectric layer in the otherwise unstable negative capacitance operating state, leading to an enhancement in permittivity and capacitance.

1.2 Prior Work and Transistor-Level Integration

Although ferroelectricity was demonstrated in HfO_2 and ZrO_2 in [8, 43], the thickness limits of this behavior in these films was not well known. In order to be integrated into modern

transistor gate stacks, the dielectric is generally no thicker than 2-3 nanometers [41], whereas ferroelectricity is *typically* an effect that weakens when the material thickness is reduced. Contrary to this general expectation, emergent ferroelectricity in ultrathin films of ZrO_2 - down to 5Å thickness - was demonstrated in [15], and ferroelectricity in 1 nanometer doped HfO_2 films was confirmed in [16] due to size effects counterintuitively stabilizing the material polarization. In [17], a 1.8 nanometer trilayer gate stack composed of HfO_2 - ZrO_2 - HfO_2 (HZH) films was demonstrated for advanced transistor applications, with a remarkably low effective oxide thickness (EOT) of 6.5 Å - particularly notable as the HZH dielectric was deposited on top of 8 Å of SiO_2, confirming that the EOT provided by the HZH layer is indeed negative.

Integration of the HZH gate stack into 90 nm NMOS SOI transistors was demonstrated in [39], showing substantially higher transconductance (g_m) than industry benchmarks. Reproduction of the gate stack process in MIT Lincoln Laboratory's Microelectronics Laboratory was announced in [52], notably including PMOS devices. Cryogenic characterization of nFET devices was performed in [40], demonstrating the potential of NCFETs for low-temperature high-performance computing, and ETSOI devices in a short-channel platform were reported in [61]. Reliability studies, such as [52] showed that end-of-lifetime (EOL) characteristics are not degraded by the presence of the NC gate dielectric, and carrier mobility was likewise unaffected compared to high-κ HfO_2 control. The most recent studies of the HZH materials system have focused on transport-related effects; namely, increases in carrier injection velocity due to electrostatic confinement effects [29].

1.3 Thesis Outline

This thesis makes two main contributions in view of the existing literature - confirmation of the negative capacitance effect in p-type MOSFETs at low temperature, and a study of the RF noise performance of negative capacitance FETs.

As much of this thesis draws upon RF measurement and characterization, the second chapter addresses these fundamentals as a basis for the remainder of the thesis. Next, cryogenic measurement and characterization of p-type NCFETs on an SOI platform is performed to confirm the stability of the HZH gate dielectric at low temperature for high-performance computing applications. In the fourth chapter, the effect of EOT scaling on the RF noise performance of short-channel MOS devices is explored via analytical noise modeling. The final chapter summarizes the contributions of this thesis with a view to future work.

Chapter 2

RF Measurement and Parameter Extraction of NCFET Devices

Two important experimental signatures of negative-capacitance (NC) in a MOS structure are a hysteresis-free enhancement in total gate capacitance, due to improvement in the effective oxide thickness (EOT), and enhancements in transconductance (g_m) on account of increased Q_{inv} [51]. In the nanoscale regime, series resistances, trace capacitance and inductance from external pad structures, and fabrication-related parasitic components distort the quality of semiconductor device performance, necessitating RF measurements for accurate device characterization [9]. RF measurements are especially powerful in this regard, as they allow analytical corrections for series impedance and pad parasitics via methods from two-port linear systems theory. In this section, we describe a measurement and analysis protocol that enables high-quality device parameter extraction up to 40 GHz, emphasizing the role of two-port network theory in the calculations. RF measurements are performed on 90 nm nFET SOI devices from MIT Lincoln Laboratory [51] harnessing a negative capacitance (NC) dielectric gate stack to illustrate the measurement and extraction procedure.

2.1 Experimental Measurement Setup

All measurements in this thesis were conducted using a Lakeshore TTPX Cryogenic Probe Station with Lakeshore's GSG-100-40A-26U-E GSG microwave probes (K connector, 40 GHz, 100 µm pitch) as shown in Figure 2.1. An HP 8720 (40 GHz) Vector Network Analyzer is used to provide RF signals, and DC bias is provided by a Keysight B1500 Semiconductor Device Analyzer, whose SMU ports are connected to the DC bias ports of the VNA. Measurement control is conducted via Keysight's IC-CAP tool, and calibration is managed via WinCAL calibration software.

Prior to beginning all measurements, calibration of the network analyzer is performed using the short-open-load-through (SOLT) technique with a FormFactor (Cascade) GSG 101-190 Impedance Standard Substrate (100 - 250 um pitch). For the low-temperature

measurements reported in this paper, a liquid nitrogen tank is connected to the cryogenic flow port of the probe station, with probe arm, radiation shield, and substrate chuck temperatures monitored by various temperature sensors installed within the probe station.

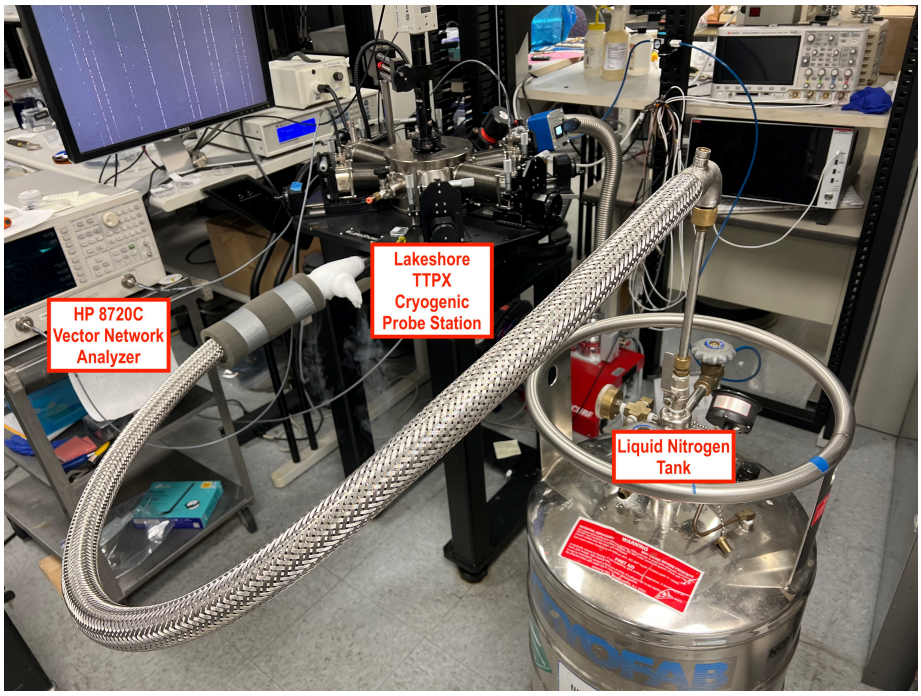

Figure 2.1: Experimental setup for RF Measurements.

2.2 RF Small-Signal Modeling

The literature is exhaustive on small-signal models for RF semiconductor devices [9]. Most small-signal circuits vary only slightly in modeling of specific physical phenomena, as the general model has proven powerful enough to describe devices as diverse as GaN transistors, III-V HEMTs, planar Si FETs, and advanced geometry structures such as FinFETs [22]. In this section, we will review the parameter extraction methodology used in this thesis (drawn from [9]), with an emphasis on leveraging two-port linear network theory.

All extracted results are from a software tool (rfu5.py) that I developed in my senior year of undergraduate study. rfu5 utilizes Python 3.9 with a matplotlib and Jupyter-Notebook integrated front-end, leveraging the excellent scikit-RF microwave engineering package for numerous computations [3]. I am indebted to MATLAB analysis scripts by Wenshen Li for serving as a valuable reference for constructing several features in rfu.

MOSFET Small-Signal Equivalent Circuit

The small-signal equivalent circuit model used for RF analysis is depicted in Figure 2.2. The elements g_m and R_{ds} represent the classic quasi-static small-signal parameters - namely the device transconductance ($g_m \triangleq \frac{dI_{ds}}{dV_{gs}}$) and output resistance ($R_{ds} = r_0 \triangleq (\frac{dIds}{dVds})^{-1}$). The capacitance elements C_{gs} and C_{gd} represent a partition of the total gate capacitance, and satisfy $C_{gg} = C_{gs}+C_{gd}$. C_{ds} models capacitive effects between the source and drain terminals. C_{ds} is typically much smaller than C_{gs} or C_{gd}, though it is important to include in RF models as it can shunt the effective output impedance r_0.

The remaining elements $L_s, R_s, L_d, R_d, L_g, R_g$ represent series inductance and resistance, and can be seen as a frequency-dependent extension of the commonly discussed R_{gate} and R_{sd} parameters. It is important to note that all of these parameters represent physical quantities associated with the device - no elements fully external to the MOSFET itself have been introduced yet.

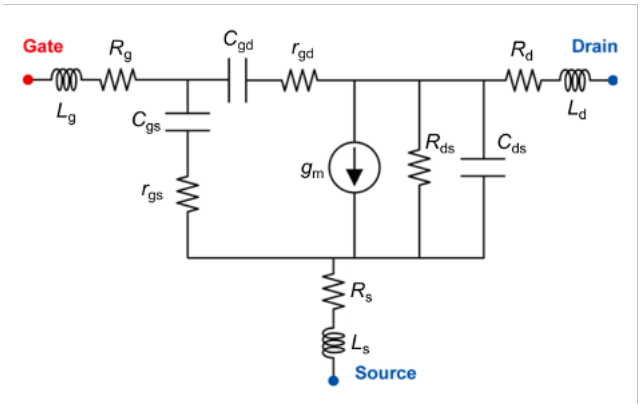

Figure 2.2: Small-signal equivalent circuit used for RF parameter extraction.

The resistances r_{gs}, r_{gd} model non-quasi-static (NQS) effects, which are mostly relevant when the device operating frequency approaches that of the intrinsic carrier transit time τ. g_m is additionally modeled with a phase factor $e^{-j\omega\tau}$ when considering NQS effects. This device model will be referred to as the 'DUT' (Device Under Test) for the remainder of this section.

2.3 Extrinsic Element De-Embedding and Extraction

Open-Short Structure De-Embedding

Calibration brings the reference plane of the VNA right to the probe tip (the VNA sees the impedance that the probe tip sees, without resistances and losses through the connecting

cables). However, the pad structure of the MOSFET itself introduces another network of parasitic elements that separate our reference plane from the DUT model. We typically model this pad structure as a series resistance and inductance alongside a shunt capacitance. The overall DUT structure therefore appears as in Figure 2.3. For this reason, we often fabricate 'dummy structures' that are electrically open (no connection between the two ports) and electrically short (direct connection between the two ports). Since the open structure has no component bridging the two ports, it only contains the parallel capacitance elements. Similarly the short structure will contain all the parasitic elements, without the DUT. Figure 2.3 illustrates all three of these structures.

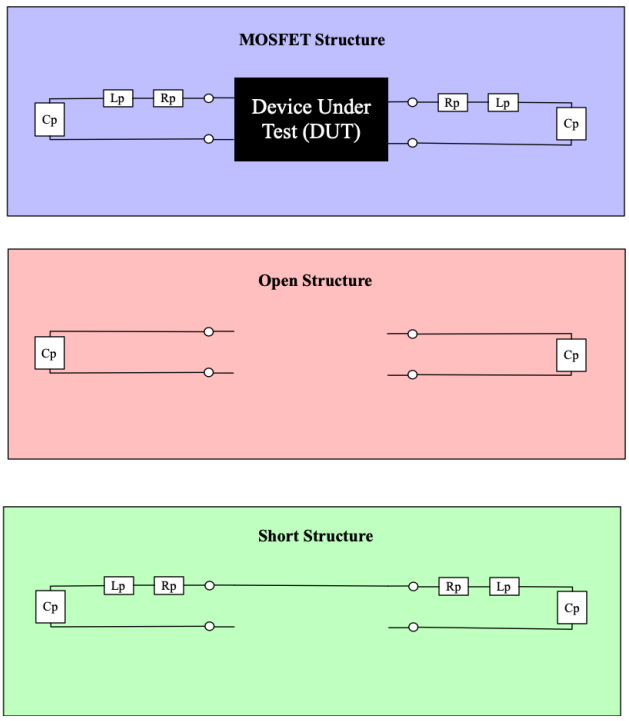

Figure 2.3: Open/Short de-embedding structure diagram.

Two-port network theory - particularly that of scattering (S) parameters – avails us here; the reader is recommended to a reference (e.g. [10]) for in-depth information on S-parameters. Briefly the following properties are recanted:

1. $S = \begin{bmatrix} S_{11} & S_{21} \\ S_{12} & S_{22} \end{bmatrix}$

   where $|S_{11}|^2$ = reflected power from port 1, $|S_{22}|^2$ = reflected power from port 2, $|S_{21}|^2$ transmitted power from port 1 to port 2, $|S_{12}|^2$ = transmitted power from port 2 to port 1.

2. *Z* parameters hold the 'impedance representation' of S-parameter information; namely impedance at port 1, port 2, between ports etc. **For two-port networks in a series configuration, the overall Z-parameters are given as the sum of the individual Z-parameters (See Figure 2.4).**

3. *Y* parameters hold the 'admittance representation' of S-parameter information; namely admittance at port 1, port 2, between ports etc. **For two-port networks in a parallel/shunt configuration, the overall Y-parameters are given as the sum of the individual Y-parameters (See Figure 2.4).**

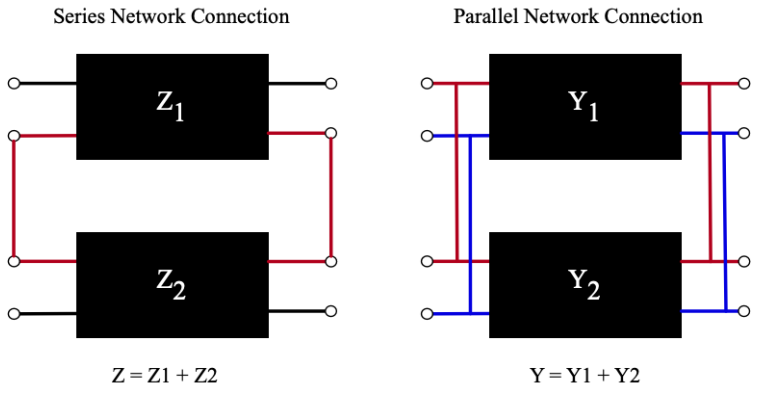

Figure 2.4: Series and Shunt Network Connections.

Given this background, and the measured S parameters of the open structure, short structure, and MOS device, we can de-embed the pad parasitics entirely via the process in Figure 2.5. The leftmost columns indicate the parameter representation used to conduct the arithmetic operation. First, we can subtract the open structure Y parameters from the MOS structure Y parameters, since their network representations are in a parallel configuration. This gives us the Y parameters of the DUT plus Lp/Rp (call this A). Similarly, we can subtract the Y parameters of the open structure from the Y parameters of the short structure to get the Y parameters of the Lp/Rp network (call this B). Since the Lp/Rp impedance network (network B) is in a series configuration with the DUT network, we must convert networks A and B to Z parameters in order to subtract (B) from (A) and recover the Z-parameters of the device-under-test.

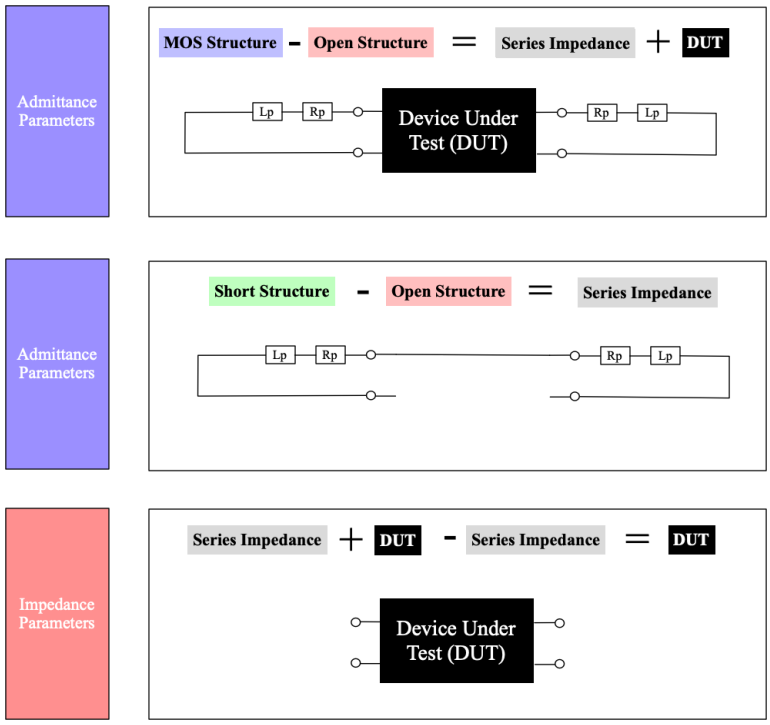

Figure 2.5: De-embedding procedure diagram.

Extrinsic Inductance/Resistance De-Embedding via Cold Bias Conditions

Having de-embedded the pad parasitics, we have the S-parameter representation of the circuit in Figure 2.2. We would like to separate the device structure of Figure 2.2 further into an 'intrinsic' small-and 'extrinsic' small- signal circuit, as shown in Figure 2.6. One may verify that $Z_{series} + Z_{int} = Z_{ext}$[1]. Therefore, once we determine the elements $L_s, R_s, L_d, R_d, L_g, R_g$, we can simply subtract Z_{series} from the DUT parameters to obtain the intrinsic device model.

[1]This is a fun exercise, as it is not immediately obvious if one draws the series-connected model, but tracing the impedances from port to port leads to the same Z-parameter expressions.

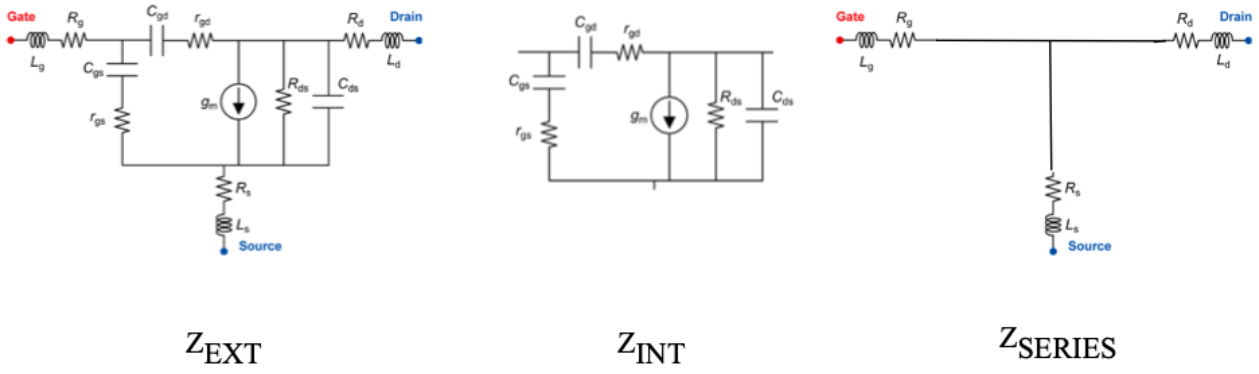

Figure 2.6: Intrinsic and Extrinsic MOSFET device model (Vgs > Vt)

The small-signal circuit in Figure 2.2 assumes $V_{gs} > V_t$. For $V_{gs} = 0$ the transconductance element can be neglected due to absence of the field-effect, leaving us with a purely capacitive and resistive circuit network. This 'off state' small-signal model of the transistor is referred to in the literature as the 'cold-FET' condition [2] [9]. The small signal network under these conditions is represented in Figure 2.7.

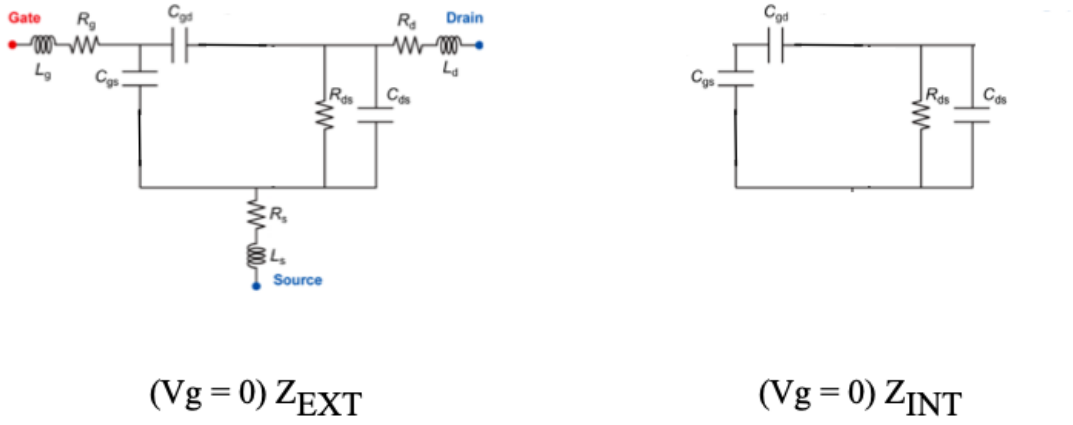

Figure 2.7: Intrinsic and Extrinsic MOSFET device model in the off-state (Vgs < Vt).

Extracting $L_s/L_d/L_g$ and $R_s/R_d/R_g$

From a Z-parameter analysis in [9] the following relations can be shown for the resistances:

[2]Strictly speaking, the cold-FET condition assumes Vgs = 0 V and Vds = 0 V. As will be discussed shortly, it is often useful to sweep Vgs while holding Vds to 0 volts in order to compensate g_{ds} dependencies in the Z-parameters.

$$Re(Z_{22} - Z_{12}) = R_d + \frac{1}{2g_{ds}} \tag{2.1}$$

$$Re(Z_{12}) = R_s + \frac{1}{2g_{ds}} \tag{2.2}$$

$$Re(Z_{11} - Z_{12}) = R_g - \frac{1}{4g_{ds}} \tag{2.3}$$

Similarly for the inductances:

$$\frac{Im(Z_{22} - Z_{12})}{\omega} = L_d - \frac{C + 2C_{ds}}{4g_{ds}^2} \tag{2.4}$$

$$\frac{Im(Z_{12})}{\omega} = L_s - \frac{C + 2C_{ds}}{4g_{ds}^2} \tag{2.5}$$

$$\frac{Im(Z_{11} - Z_{12})}{\omega} = L_g - \frac{C_{ds}(C + 2C_{ds})}{4g_{ds}^2 C} - \frac{1}{2C\omega^2} \tag{2.6}$$

From the following equations, we see that we should be able to recover L_s, R_s, L_d, R_d and R_g entirely from the Z-parameters above if we can remove the g_{ds} dependencies. Since $g_{ds} \propto Q_{inv} \propto C_{ox}V_{ov}$, measuring the S-parameters of the structure for varying V_{gs} bias values while keeping V_{ds} at 0 volts will allow us to extrapolate the values of the above expressions to $\frac{1}{V_{ov}} = 0$, where eqns. (2.1 - 2.5) simply become R_d, R_s, R_g, L_d and L_s respectively. We perform this extrapolation for each frequency point, and then determine the values of each component from linear fits across the measured frequencies. Figure 2.8 shows the R_g extraction, and Figure 2.9 shows the R_{sd} extraction and V_{ov} extrapolations for a 90 nm NMOS device. Figure 2.10 shows the extractions for inductances L_s and L_d.

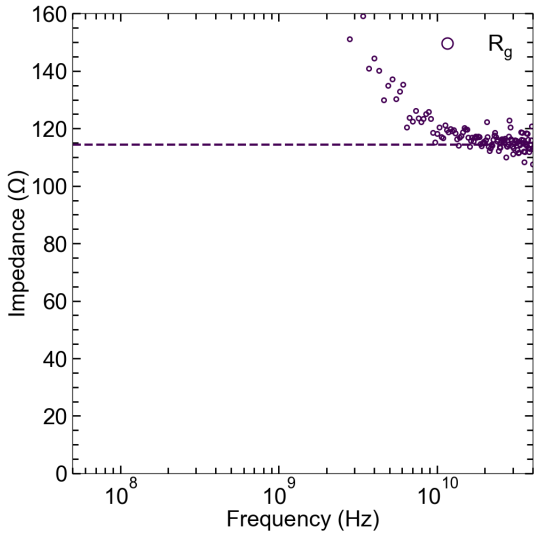

Figure 2.8: Extracted gate resistance vs. frequency via ColdFET method

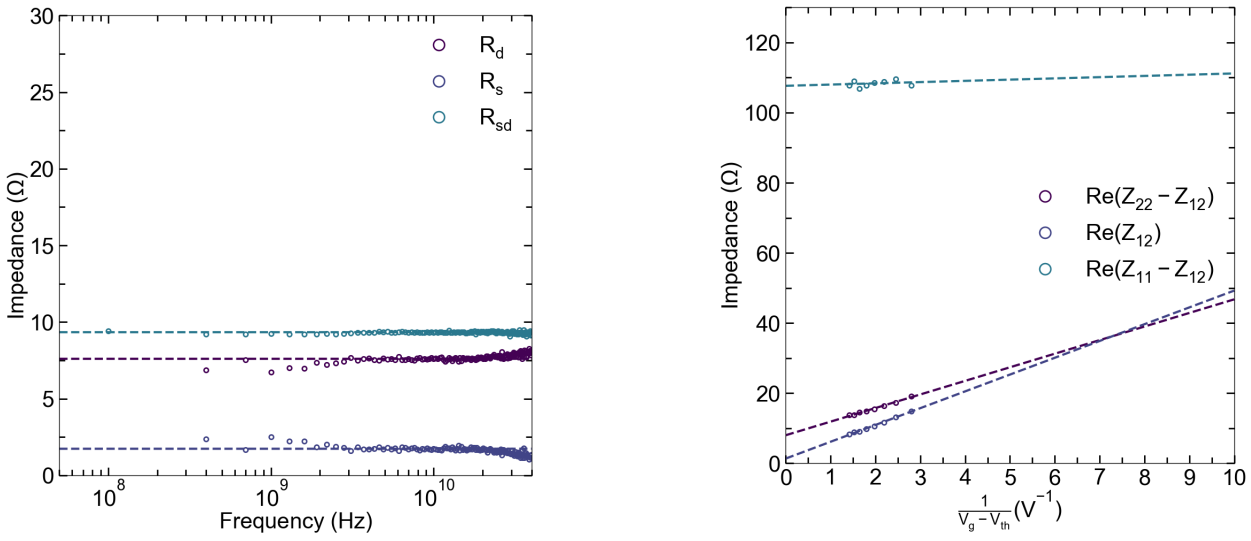

Figure 2.9: Extracted R_{sd} vs. V_{ov} and frequency via ColdFET method

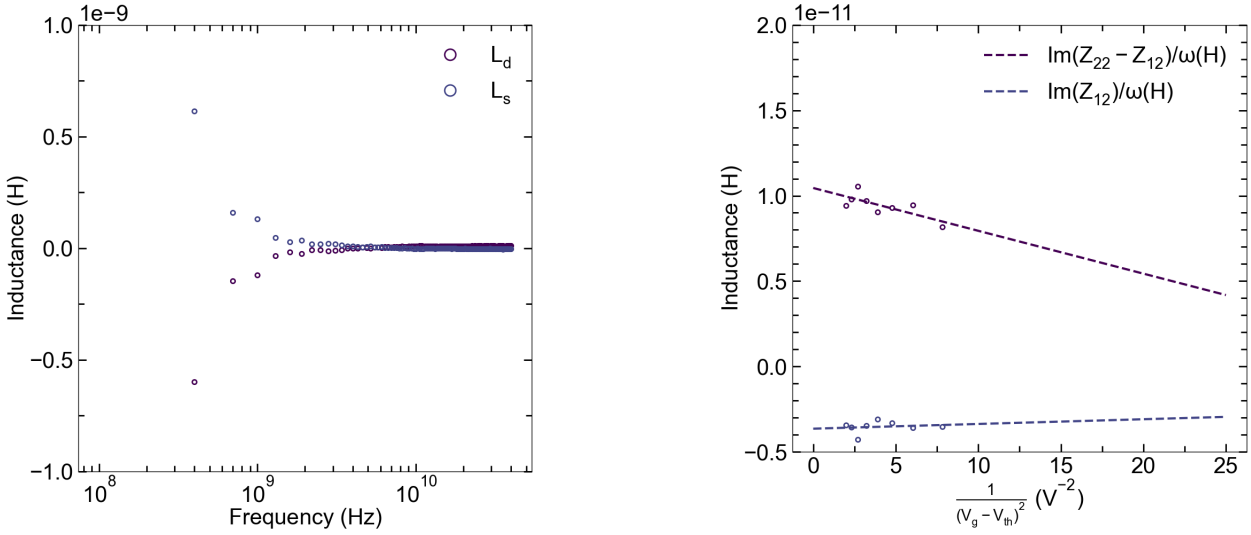

Figure 2.10: Extracted L_s/L_d vs. V_{ov} and frequency via ColdFET method

For L_g the analysis is more involved since there is both a $\frac{1}{\omega^2}$ dependency and a g_{ds}^2 dependency. We can tackle the L_g extraction by doing the following:

1. For the S-parameters at each V_{gs} bias point, extrapolate the value of Equation 2.6 against $\frac{1}{\omega^2}$ to get a value as $\frac{1}{\omega^2} \to 0$.
2. Now across the V_{gs} bias points, extrapolate the value of Equation 2.6 against $\frac{1}{V_{ov}^2}$ to extract the value of L_g as $\frac{1}{V_{ov}^2} \to 0$.

Figure 2.11 shows this extrapolation against frequency and V_{ov} for a 90 nm NMOS device. Often, as in Figure 2.11, the extracted L_g may be negative, in which case, subsequent computations treat L_g as 0 in order to preserve the physicality of the model.

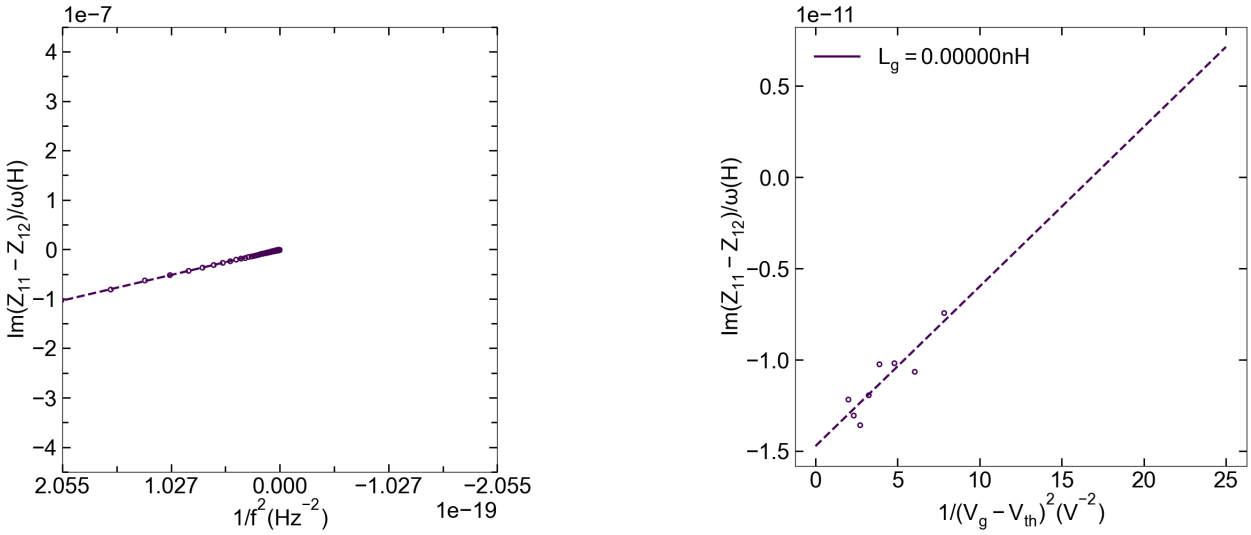

Figure 2.11: Extracted L_g vs. V_{ov} and frequency via ColdFET method

After extraction of the parameters R_d, R_s, R_g, L_d, L_s and L_g, we can construct the Z-parameters of the network Z_{SERIES} in Figure 2.6 as follows:

$$Z_{11} = R_g + R_s + j\omega(L_g + L_s) \tag{2.7}$$

$$Z_{12} = Z_{21} = R_s + j\omega(L_s) \tag{2.8}$$

$$Z_{22} = R_s + R_d + j\omega(L_d + L_s) \tag{2.9}$$

The intrinsic device model Z_{INT} is then calculable as $Z_{EXT} - Z_{SERIES}$, where Z_{EXT} is from the measured device S-parameters after the open-short de-embedding described earlier.

Extracting Parasitic Capacitance from Cold-FET S-parameters

Accurate extraction of the device parasitic capacitance is also desirable, as it allows for projection of the device's intrinsic high-frequency performance. Note that the capacitances C_{gd} and C_{gs} can be expressed in terms of their intrinsic and parasitic components; namely $C_{gd,tot} = C_{gd,i} + C_{gd,par}$ and $C_{gs,tot} = C_{gs,i} + C_{gs,par}$. In the off-state, the MOS capacitor within the MOSFET structure is not active, and therefore $C_{gd,i}$ and $C_{gs,i}$ tend to 0, leaving us with $C_{gd,tot} = C_{gd,par}$ and $C_{gs,tot} = C_{gs,par}$. Therefore, we want to extract the parasitic capacitances from S-parameters taken under bias conditions of $V_{gs} = V_{ds} = 0V$. This portion of the analysis assumes the parasitic capacitances show minimal gate voltage dependence.[3]

Using the model on the right-hand side of Figure 2.7, we compute the following relations:

[3]This assumption is reasonable for the device structures discussed in this thesis, as will be shown shortly.

$$Y_{11} = j\omega(C_{gs} + C_{gd}) \tag{2.10}$$

$$Y_{12} = Y_{21} = -j\omega C_{gd} \tag{2.11}$$

$$Y_{22} = j\omega(C_{gd} + C_{ds}) + \frac{1}{R_{ds}} \tag{2.12}$$

which yields the following expressions for the parasitic capacitances:

$$C_{gs,par} = \frac{Im(Y_{11} + Y_{12})}{w} \tag{2.13}$$

$$C_{ds,par} = \frac{Im(Y_{12} + Y_{22})}{w} \tag{2.14}$$

$$C_{gd,par} = \frac{-(Im(Y_{21} + Y_{12}))}{2w} \tag{2.15}$$

The extracted parasitic capacitances for a 90 nm NMOS device are shown in Figure 2.12.

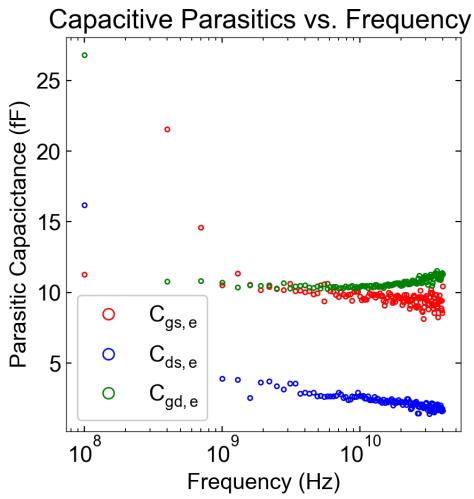

Figure 2.12: Capacitive parasitics vs. frequency via ColdFET method

2.4 Intrinsic Device Element Extraction

Having performed open-short de-embedding, and after determining Z_{series} and the parasitic capacitances via the method in Section 2.3, we retrieve the intrinsic device model in the

middle of Figure 2.6 via $Z_{INT} = Z_{EXT} - Z_{SERIES}$. In this section, we introduce the Y-parameter equations for the intrinsic device model and extraction methods for capacitance and transport related parameters.

Intrinsic Admittance Parameter Model

The full equations for the Y-parameters of the intrinsic device model, including NQS effects, are as follows:

$$Y_{11,int} = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} r_{gs}} + \frac{j\omega C_{gd}}{1 + j\omega C_{gd} r_{gd}} \tag{2.16}$$

$$Y_{12,int} = \frac{-j\omega C_{gd}}{1 + j\omega C_{gd} r_{gd}} \tag{2.17}$$

$$Y_{21,int} = \frac{g_m e^{-j\omega\tau}}{1 + j\omega C_{gs} r_{gs}} - \frac{j\omega C_{gd}}{1 + j\omega C_{gd} r_{gd}} \tag{2.18}$$

$$Y_{22,int} = \frac{1}{R_{ds}} + j\omega C_{ds} + \frac{j\omega C_{gd}}{1 + j\omega C_{gd} r_{gd}} \tag{2.19}$$

Note r_{gs}, r_{gd} are the NQS resistances and not the series resistances $R_g/R_s/R_d$.
The equations for each element in the intrinsic device model are as follows:

$$C_{gs} = \frac{-1}{\omega Im(\frac{1}{Y_{11,int}+Y_{12,int}})} \tag{2.20}$$

$$C_{ds} = \frac{Im(Y_{22,int} + Y_{12,int})}{\omega} \tag{2.21}$$

$$C_{gd} = \frac{1}{\omega Im(\frac{1}{Y_{12,int}})} \tag{2.22}$$

$$r_{gs} = Re(\frac{1}{Y_{11,int} + Y_{12,int}}) \tag{2.23}$$

$$r_{gd} = -Re(\frac{1}{Y_{12,int}}) \tag{2.24}$$

$$R_{ds} = Re(\frac{1}{Y_{22,int} + Y_{12,int}}) \tag{2.25}$$

$$\tau = \frac{-1}{\omega}(\measuredangle(\frac{Y_{21,int} - Y_{12,int}}{Y_{11,int} + Y_{12,int}}) + \frac{\pi}{2}) \tag{2.26}$$

$$g_{m,int} = \frac{-|\frac{Y_{21,int}-Y_{12,int}}{Y_{11,int}+Y_{12,int}}|}{Im(\frac{1}{Y_{11,int}+Y_{12,int}})} \tag{2.27}$$

$C_{gg,i}$ Extraction

To validate the enhancement in EOT from negative capacitance (NC) devices, we want to obtain the intrinsic capacitance per unit area. To do this, RF measurements are conducted on SOI devices of varying gate lengths (lithographed lengths 90, 120, 150 nm) with the same width (W = 20 um). The device $C_{gg} = C_{gs} + C_{gd}$ is then extracted for each channel length from $Im(Y_{11})/\omega$. Figure 2.13 shows this extraction for the three channel lengths as a function of Vg (0 V to 1.6 V in 200 mV steps). The floor capacitance at Vg = 0 V (which constitutes the parasitic capacitance) is subtracted from the dispersions depicted in Figure 2.13.

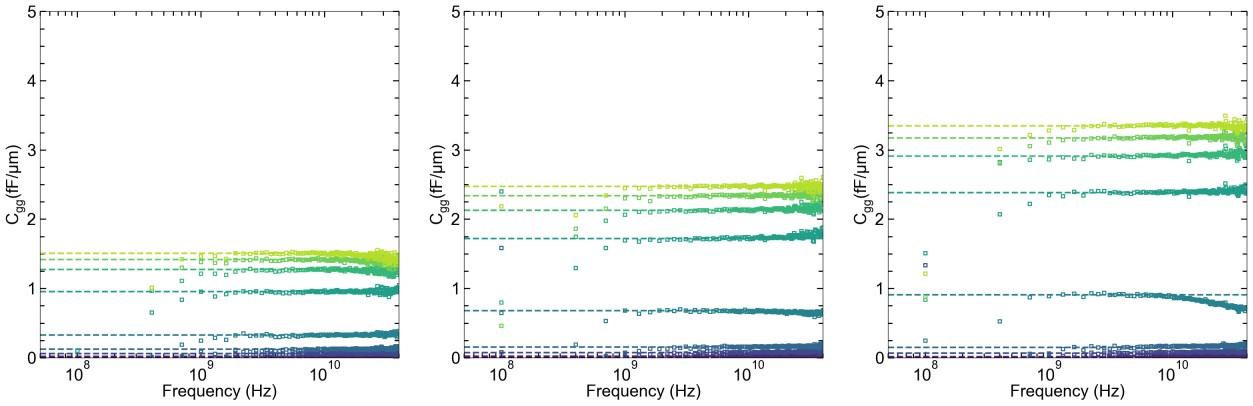

Figure 2.13: C_{gg} extracted for 90/120/150 nm (left-to-right, respectively) NMOS devices.

This extraction provides us C_{gg}/W for three different channel lengths – recall our desired quantity is $\frac{C_{gg}}{WL} = C_{gg,i}$. We can obtain this by extracting the slope of $\frac{C_{gg}}{W}$ vs. channel length at each Vg point. We may use the lithographed gate length here for calculations, as dopant lateral diffusion is assumed to affect adjacent devices similarly, so L_{eff} reductions do not impact the slope extraction of C_{gg}/W vs. $L_{channel}$. Figure 2.14 shows the C_{gg} per Lg curves, and the quality of the slope fitting across Vg bias points. The final extracted intrinsic $C_{gg,i}$ is compared against capacitance-voltage characteristics generated using the numerical simulation tool SCHRED [59], confirming a 7.5 angstrom effective oxide thickness (EOT) in this set of measured devices.

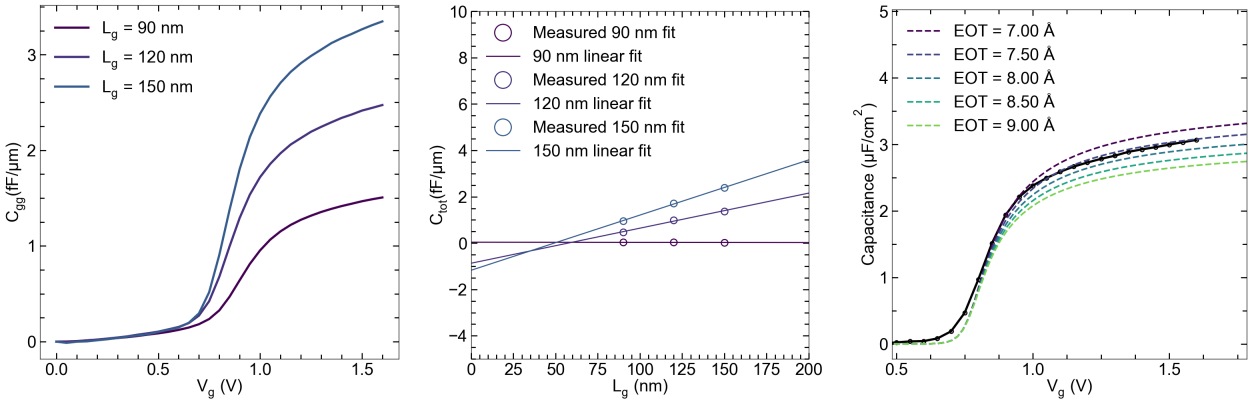

Figure 2.14: $C_{gg,i}$ is extracted using the slope of C_{gg}/W versus channel length L_g. The effective oxide thickness (EOT) is determined via matching the inversion capacitance to SCHRED simulations.

f_T, f_{MAX}, and $g_{m,int}$ Extraction

The intrinsic and extrinsic device conductances $g_{m,e}$ and $g_{m,i}$ can be extracted using Equation 2.27 on the intrinsic and extrinsic device structures in Figure 2.6. The value of g_m at each bias point is fit across frequency - Figure 2.15 shows minimal frequency dispersion of the transconductance across the 100 MHz - 40 GHz spectrum. A high intrinsic $g_{m,i}$ of 1.645 mS/um at room-temperature is extracted, representing a 10% increase over the extracted $g_{m,e}$ value.

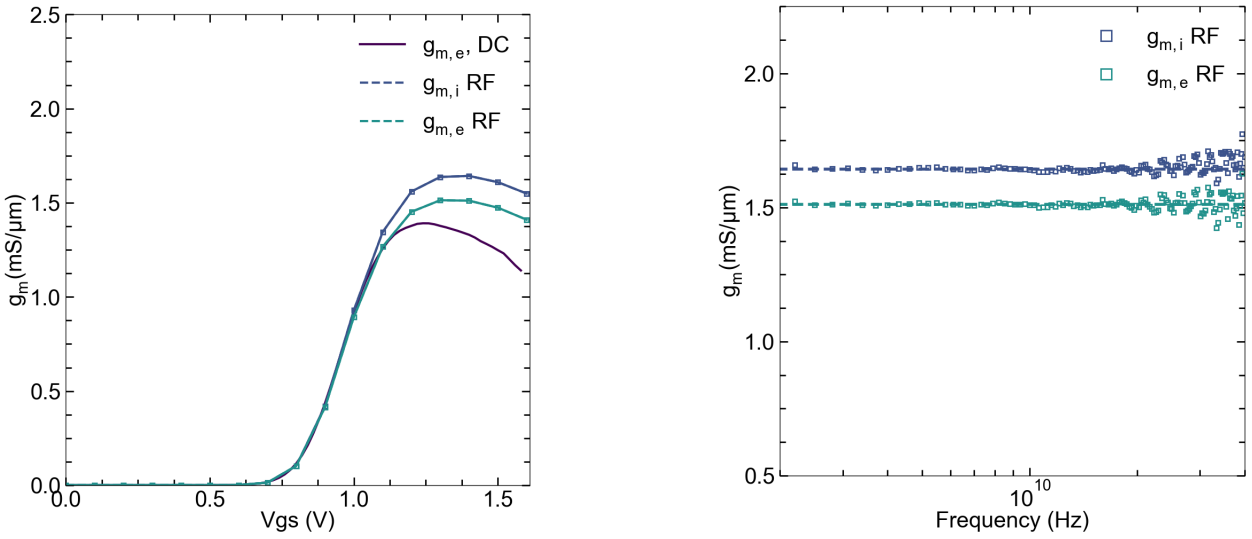

Figure 2.15: Transconductance (g_m) increases as a function of the gate voltage as strong inversion operation is reached. $g_{m.i}$ and $g_{m,e}$ are calculated by linear fits across frequency for each V_g bias point.

The parameters f_T and f_{MAX} represent the maximum short-circuit current gain frequency, and maximum power gain frequency respectively [30] [51]. f_T is a concept adapted from the bipolar transistor that relates to the device speed. A device's f_T can be determined from the $|H_{21}|$ 'hybrid' parameter (another relative of the S-parameter family of representations), as H_{21} generically represents the short circuit current gain for any two-port system. f_{MAX} is the maximum frequency where power gain can be delivered by the two-port network under consideration, and is computed by extrapolating the Mason invariant $|U|$ to 0 dB [30]. Mason's invariant computes the power gain of the two port network assuming that the two-port system's feedback has been removed (ex. in the Y-parameter representation, feedback would come from Y_{12}; in the MOS structure, C_{gd} is a physical form of feedback). For this reason, U is often called the unilateral gain [30], as it assumes the existence of a network that cancels the feedback, making the device gain "one-way" (unilateral).

f_T and f_{MAX} are extracted from 20 dB/decade linear fits of $|H_{21}|$ and $|U|$ (90 nm NMOS device) for both the intrinsic and extrinsic device structures in Figure 2.6. An extrinsic f_T of 126 GHz and f_{MAX} of 50 GHz is extracted - the low f_{MAX} is on account of the high gate resistance of 120 ohms.

When computing the intrinsic f_T and f_{MAX}, we remove all series resistances, and also remove the parasitic capacitances computed in section 2.3 by subtracting the Y-parameters of the parasitic capacitance network from the intrinsic device model in Figure 2.6. Figure 2.16 displays the extrinsic and intrinsic f_T/f_{MAX} extraction for a 90 nm NMOS device. An intrinsic f_T of 307 GHz and f_{MAX} of 310 GHz is obtained, representing a 1.44x and 6.20x

increase as compared to the extrinsic case. The f_{MAX} improvement, while large, is expected given the significant gate resistance is removed in the intrinsic calculation. Similarly, since $f_T = \frac{g_m}{2\pi \times C_{gg}}$, removing C_{par} from C_{gg} increases f_T.

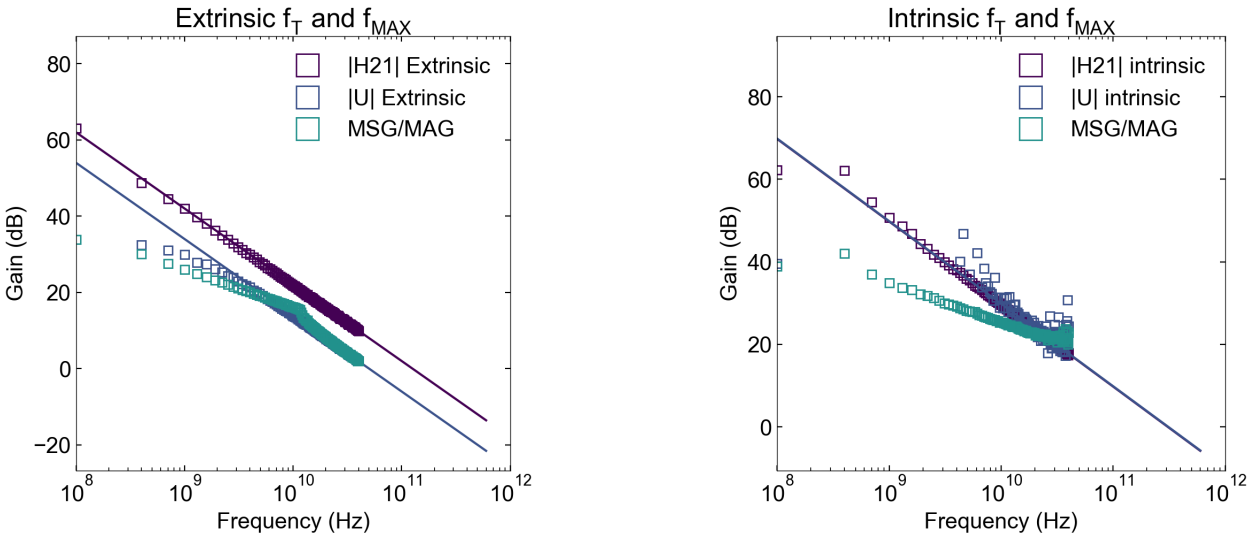

Figure 2.16: f_T and f_{MAX} extraction. The removal of extrinsic parasitics significantly improves high-frequency performance.

Model Validation

Using the extracted parameter values in this section, one may plug the values back in to the analytical equations for the Y-parameters and compare the resulting model S-parameters to the measured S-parameters on the Smith chart. Figure 2.17 shows the model vs. measurement fit for the 90 nm device discussed in this section, demonstrating outstanding agreement between the extracted parameter values and the measured S-parameters.

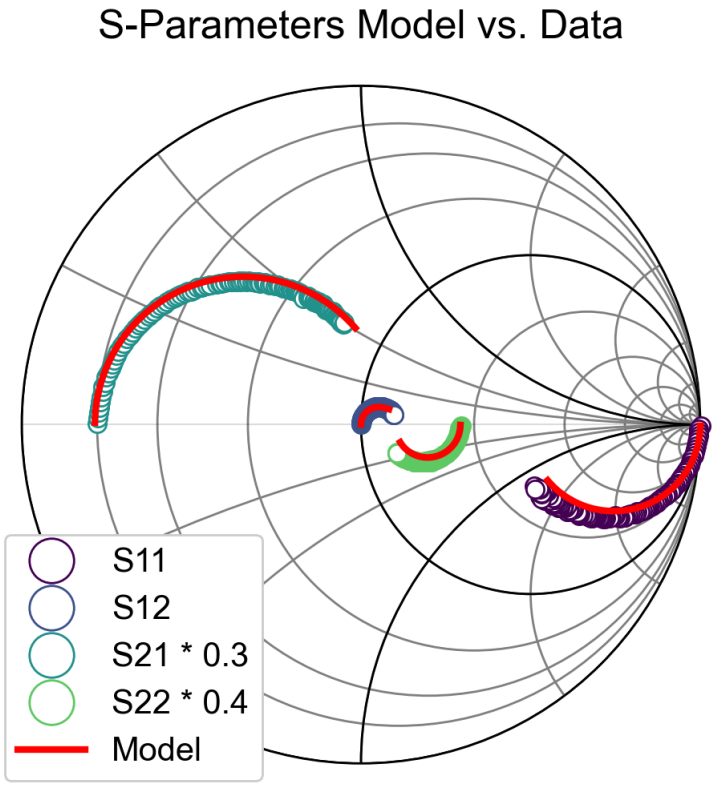

Figure 2.17: Modeled vs. Measured S-parameters of 90 nm NMOS device; an excellent fit is achieved up to 40 GHz. S_{21} is multiplied by 0.3 to ensure depiction within the Smith radius, and S_{22} is multiplied by 0.4 to prevent overlap with other parameters.

Chapter 3

Cryogenic Measurement and Characterization of PMOS NCFET Devices

Cryogenic electronics are emerging as an attractive technology for ultra low-power computing applications. At the device level, lower temperatures lead to a myriad of performance benefits, including higher transconductance, on-off current ratios, reduced subthreshold swing, and higher cutoff frequencies [5, 44, 13, 28, 48, 24]. In this section, we study the RF and DC cryogenic performance of PMOS NCFETs. While low-temperature RF characterization for NMOS NCFETs was reported in [40], PMOS devices harnessing an NC gate dielectric yet to be studied at low-temperature. From a materials science perspective, low-temperature study of the HZH dielectric is interesting as it allows us to indirectly analyze the material phase. Since negative capacitance leverages depolarization of ferroelectricity, it is important that the HfO_2 layers be in the orthorhormbic material phase, which is a relatively more ordered phase compared to e.g. the monoclinic phase, which is a non-ferroelectric material state. Since we are reducing the temperature, and therefore the ambient thermal energy available to the materials system, we would expect it becomes increasingly likely that a phase transition to a less ordered state occurs. This work confirms the persistence of the NC performance enhancement in PMOS devices at low temperature, which suggests that the material phase is maintained down to 77 K. Additionally, the demonstration of p-type devices is critical to show the feasibility of NC for fully complimentary logic circuits [46]. RF and DC measurements validate the performance of the NC dielectric, and the temperature dependence of the transconductance (g_m), injection velocity (v_{x0}) threshold voltage (V_t), and cutoff frequency (f_T) is explored. Cumulatively, these results demonstrate that NC gate oxides are a compelling performance booster for low-power, energy-efficient CMOS systems.

3.1 RF C-V Extraction at 77 K

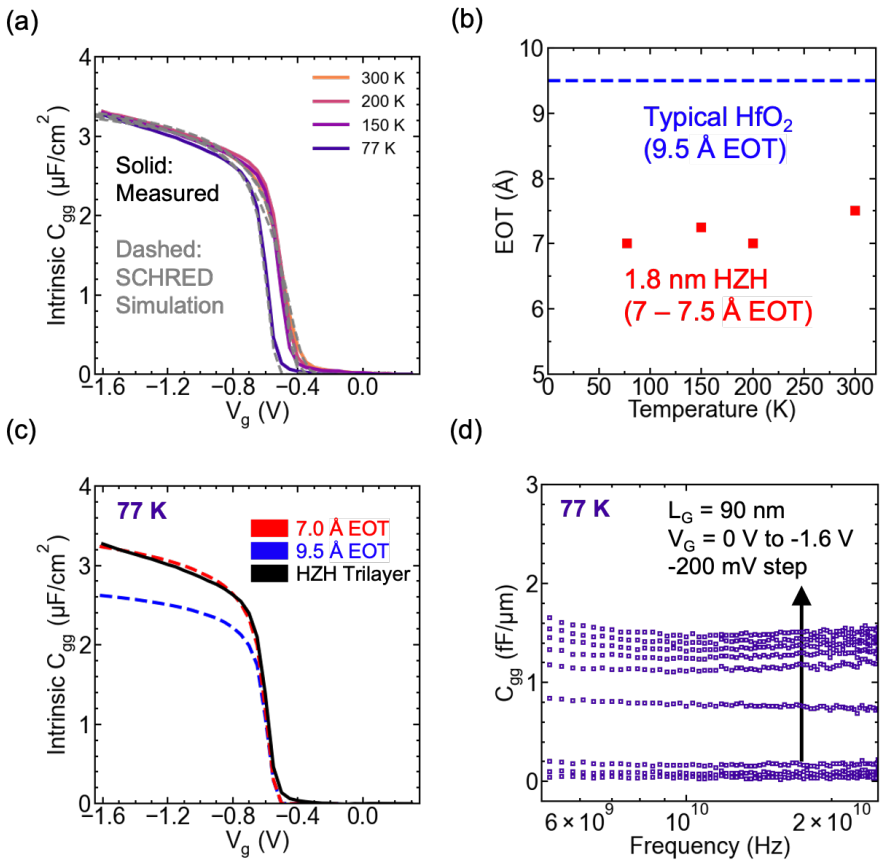

Figure 3.1: RF C-V characterization of p-type NCFET devices at low temperature.

The p-type NCFETs studied in this chapter were fabricated at MIT Lincoln Laboratory's Microelectronics Laboratory in a gate-replacement, self- aligned 90-nm silicon-on-insulator CMOS process, as described in [51]. RF measurement and characterization was carried out at temperatures of 300 K, 200 K, 150 K, and 77 K, per the methodology discussed in Chapter 2, with C-V extraction performed using the Cold-FET method of [9]. The NC gate dielectric demonstrates sub-8Å EOT down to 77 K (Fig. 3.1a-b), achieving a 7.0Å EOT at 77 K (Fig 3.1c). Notably, the intrinsic gate capacitance ($C_{gg} = C_{gs} + C_{gd}$) shows minimal dispersion across frequency, confirming that the capacitance enhancement is not a transient effect (Fig. 3.1d). The 7.0 Å achieved represents a 26% increase in capacitance compared to what is achievable with state of the art high-κ dielectrics [13, 41].

3.2 DC Device Characterization

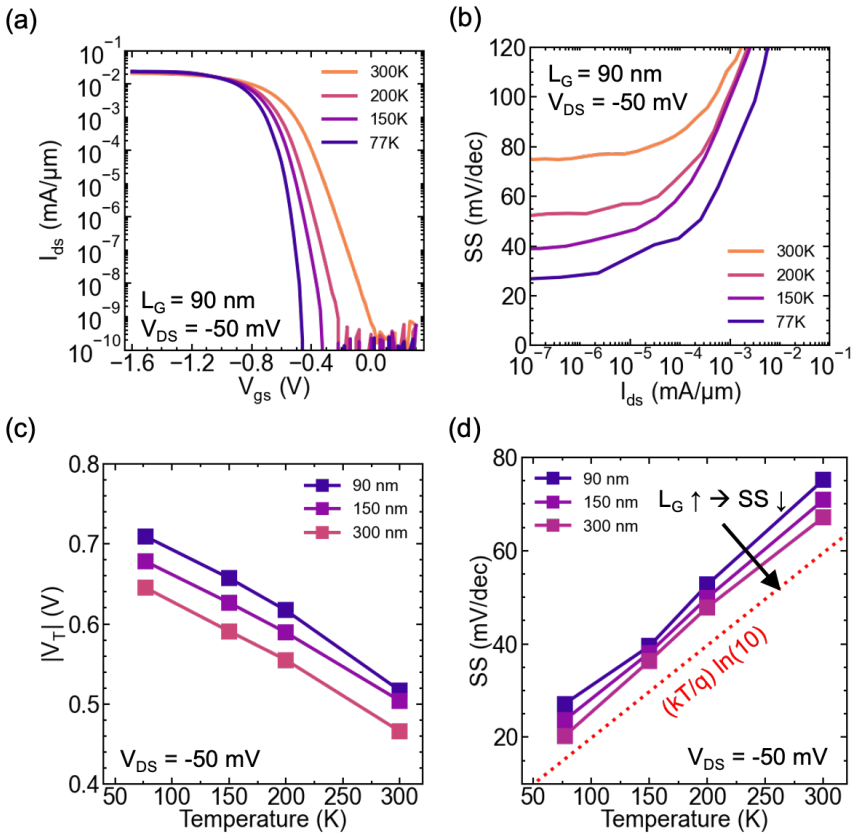

Figure 3.2: DC Id-Vg, SS, and V_t trends of PMOS devices at low temperature.

DC devices with channel lengths from 90 nm to 300 nm Lg were also measured and characterized to understand the influence of temperature on the device electrostatics. From the transfer characteristics in Fig. 3.2a, the decrease in the subthreshold slope is visible, as the 77 K characteristic undergoes a higher current increase for an incremental gate voltage compared to the 300 K characteristic. Fig. 3.2b shows the extracted subthreshold swing (SS) values directly; the SS decreases from 75 mV/decade at 300 K to approximately 25 mV/decade at 77 K. This is around 8-9 mV/dec larger than the thermal switching limit $\frac{kT}{q}ln(10)$. The subthreshold swing approaches $<$ 20 mV/decade as the channel length increases (Fig. 3.2d) on account of a smaller C_{dep} to C_{ox} ratio, since the depletion capacitance is mostly dictated by the drain bias and channel/drain dopings.

In Fig 3.2a, the increase in device threshold voltage (V_t) is also apparent, as a larger absolute gate voltage is required at 77 K to achieve the same current compared to 300 K.

This is confirmed by extracting V_t using a constant current of 100 nanoamperes times the device aspect ratio W/L (Fig. 3.2c). A roughly 200 mV increase is V_t is observed, consistent with theoretical expectations due to the decrease in thermal carrier density [28].

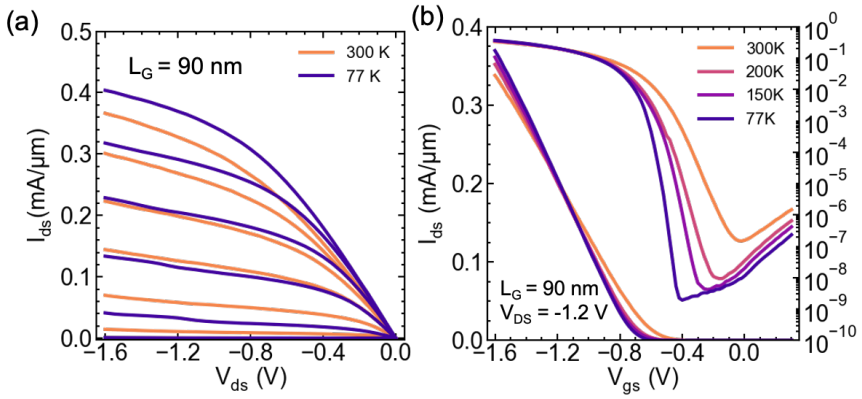

Figure 3.3: DC Id-Vd characteristics and Id-Vg characteristics under high-Vd bias conditions.

The Id-Vd characteristics of a 90 nm DC device are shown in Figure 3.3a. Unfortunately, the on-state current of the device is limited by a high series contact resistance of $\approx$ 970 Ω-μm, which requires the application of a high V_{ds} of 1.6 volts to achieve an intrinsic V_{ds} close to 1 V. Nonetheless, a reasonable 32% improvement in I_{on} at $V_{ov} = 0.89V$ is acheived at 77 K compared to 300 K. Figure 3.3b shows the presence of gate-induced drain leakage (GIDL) at higher V_{ds}, though the effect is ameliorated at low temperature compared to higher temperatures. An I_{on}/I_{off} ratio in excess of five orders of magnitude is still achievable at these conditions, which indicates suitability for digital logic applications.

3.3 RF Small-Signal Characterization and Benchmarking

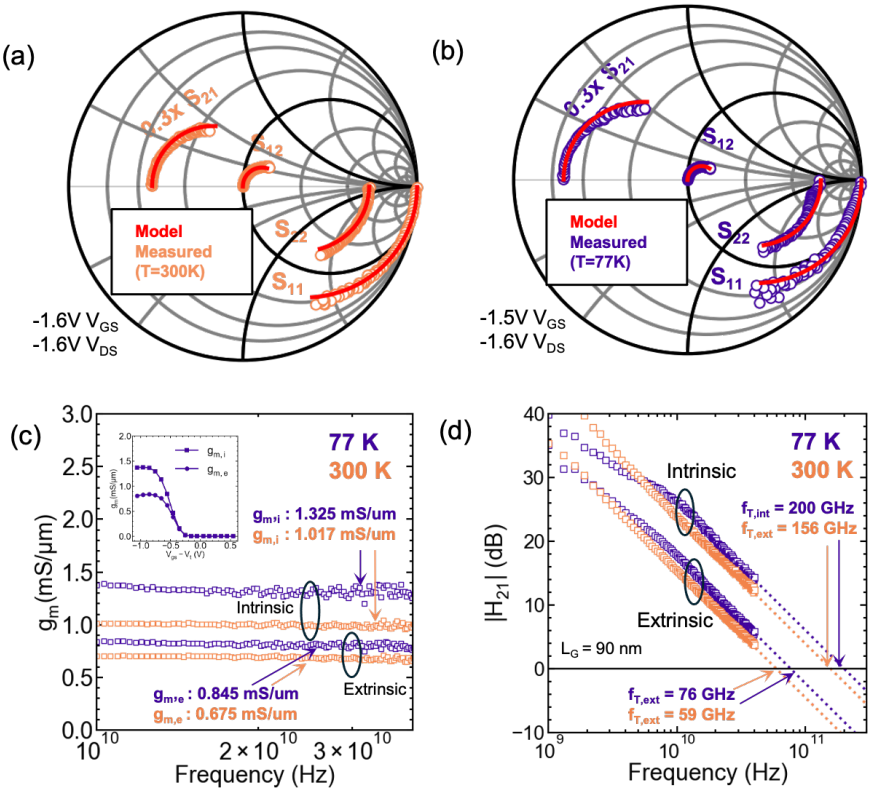

Figure 3.4: (a, b) Smith Chart modeling at 300 K temperature and 77 K - the S_{21} parameter is decreased to 0.3 times the measured value to keep it inside the S-circle. (b) g_m shows minimal dispersion at both 77 K and 300 K. (d) $f_{T,i}$ is extracted at room temperature and 77 K from the $|H_{21}|$ parameter.

Using the techniques in Chapter 2 section 4, small-signal parameter extraction and model validation was performed at 77 K and 300 K. The S_{21} parameter magnitude is decreased to 0.3x in order to keep it inside the S-circle, as the device is active. In both cases, the modeled S-parameters demonstrate good agreement with the measured S-parameters, which indicates that extracted small-signal parameters are accurate. The intrinsic $g_{m,i}$ on the $L_g = 90$ nm device shows a high value of 1.325 mS/μm, a 30% increase over the room temperature value of 1.017 mS/μm (Fig. 3.4c). The cutoff frequency f_T is extracted from the $|H_{21}|$ parameter, showing a similar 30% increase at 77 K, which leads to a 200 GHz activity limit (Fig. 3.4d).

The enhancement in both $g_{m,i}$ and f_T can be understood from improved carrier transport at low temperature, as expressed by the temperature dependence of the injection velocity V_{inj}.

In strong inversion,

$$g_m = \mu C_{ox}(V_{gs} - V_t) \propto C_{ox} v_{inj} \tag{3.1}$$

and similarly [39];

$$f_T = \frac{g_m}{2\pi(C_{gg,i} + C_{par})} = \frac{v_{inj}}{2\pi L_g}(1 + \frac{C_{par}}{C_{gg,i}})^{-1} \tag{3.2}$$

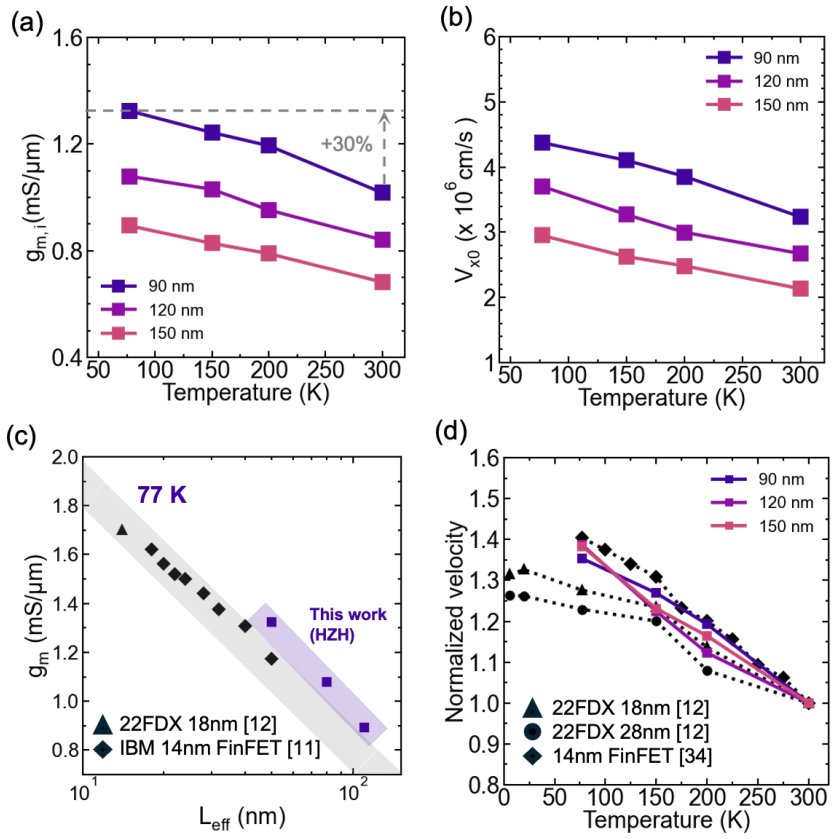

Figure 3.5: $g_{m,i}$ and v_{inj} vs temperature; benchmarked g_m and v_{inj} against industrial MOS devices.

which indicates that the improvements in both of the small signal parameters can be tied back to injection velocity. At low temperatures, it is known that decreased Coulomb and phonon scattering [29] improves electron and hole velocities. The RF-extracted v_{inj} (Fig. 3.5b) shows a 37% increase at 77 K, which suggests that faster carrier transport is

behind the I_{on}, f_T and $g_{m,i}$ improvements. The temperature-dependent velocity trend is similar to that of GlobalFoundries FDX devices [13] and 14 nm FinFET devices [35], further confirming carrier velocity is not harmed by the NC gate dielectric. The superior $g_{m,i}$ enabled by both the low-EOT gate stack and the carrier velocity boost leads HZH PMOS devices to exceed industrial scaling trends [11, 13](Fig. 3.5c). Notably, this is without implementation of a silicon germanium (SiGe) channel, which is present in FDX devices [13, 12]. This suggests that strain-engineered channels are a compelling mechanism to further improve the performance of HZH PMOS devices. Prior literature on SiGe channels suggests a hole mobility enhancement of roughly 35% from strain effects [23, 53, 42]. Using this as a rough figure of the expected improvement, we can project the RF performance of p-type NCFETs with SiGe channels. Figure 3.6b demonstrates the classic $\frac{1}{L_g^2}$ trend of the intrinsic f_T. In strong inversion, and without parasitic capacitance (hence, intrinsic) f_T can be written as:

$$f_T = \frac{g_m}{2\pi C_{gg}} = \frac{\mu C_{ox}\frac{W}{L}(V_{gs}-V_t)}{2\pi C_{ox}WL} = \frac{\mu(V_{gs}-V_t)}{2\pi L^2}. \tag{3.3}$$

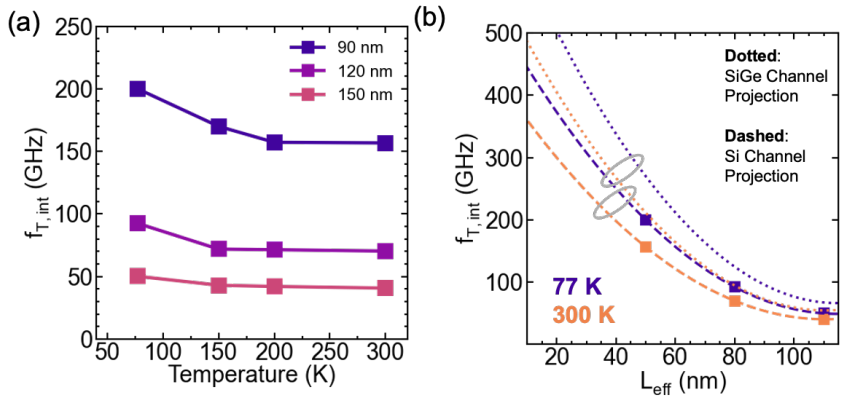

Figure 3.6: $f_{T,i}$ vs. temperature and predicted scaling trend with a silicon-germanium (SiGe) channel.

Figure 3.6b demonstrates the expected $f_{T,i}$ scaling trend with a SiGe channel, which indicates scaling well into the sub-THz analog regime with continued channel length reduction at both 300 and 77 K. Cumulatively, the boost in $g_{m,i}$ and promising performance projections when paired with further device optimization demonstrates the viability of p-type NCFETs for advanced cryogenic computing.

Chapter 4

Analytical RF Noise Modeling of Low-EOT Field Effect Transistors

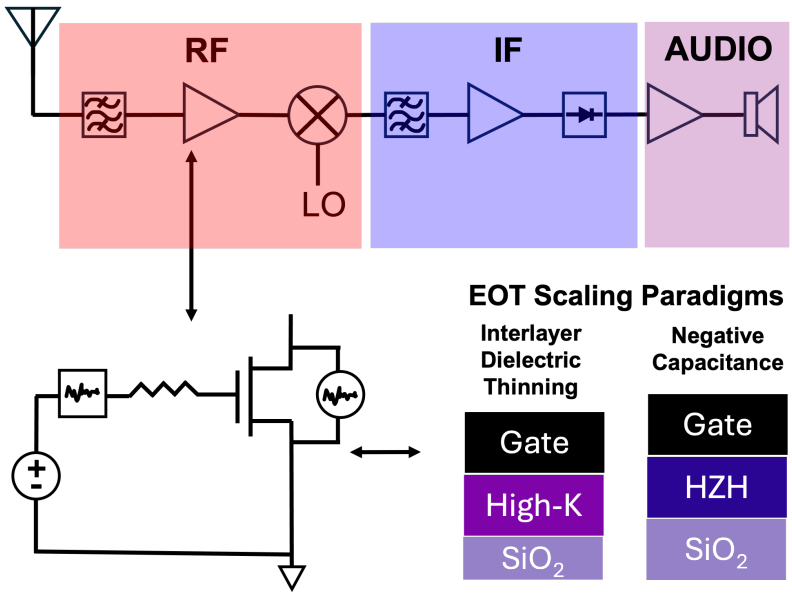

Figure 4.1: The superheterodyne receiver architecture, with RF, IF, and AUDIO components. LNAs head the receiver chain after an initial filter stage.

Next-generation cellular technologies are expected to reach into the sub-THz regime (100 GHz+); to-date, silicon CMOS remains the most promising candidate for fully integrated RF circuits in this frequency regime [31, 49, 62]. In order to build integrated communications systems in this frequency range, sufficient MOSFET cutoff frequency (f_T) is necessary. For short-channel RF MOSFETs, f_T is generally smaller than classical predictions, due to the presence of parasitic capacitance (C_{par}) [56].

Recently, low-EOT dielectrics have received attention for their ability to reduce the equivalent oxide thickness (EOT) and increase $C_{gg,i}$ relative to C_{par}, thereby improving the overall f_T [60, 39]. EOT scaling, initially proposed as a means to continue the largely digital march of Moore's law, has now become a candidate for advancing RF performance. However, the impact of effective oxide thickness (EOT) scaling on the RF noise performance of MOS transistors has yet to be considered in any literature study. Without reasonable noise characteristics, constructing functioning RF receivers in a superheterodyne architecture (Fig. 1) becomes a challenging task, as analog to digital converters in the RF front-end cannot receive symbols without sufficient signal-to-noise ratio (SNR). Understanding the impact of EOT scaling on the MOS transistor's RF noise is therefore imperative to assessing the practicality of low-EOT transistors for next-generation RF applications.

Substantial amounts of effort has been placed into constructing physics-based, analytical compact models for the various noise sources in the MOS transistor [19, 25, 20, 21, 27, 26, 37]. Advances in computer aided design methods [33, 45] have made fully analytical noise models of two-port systems available for accurate predictions of RF noise. Such models can demonstrate good accuracy even for short-channel devices [14], relying only upon accurate RF measurement and parameter extraction as covered in Chapter 2.

In this chapter, we examine the impact of two EOT scaling paradigms on the RF noise performance of MOSFETs in a common-source (CS) configuration. We consider negative capacitance EOT scaling against interfacial layer dielectric (ILD) thinning. ILD thinning is a method which directly reduces the physical thickness of the insulating dielectric (typically the SiO_2 layer) in order to increase the capacitance [2, 51]. We use the $L_g = 90$ nm device characterized in Chapter 2 for all projections – Table I lists the extracted intrinsic and extrinsic device parameters for reference. We will demonstrate that NC EOT scaling is a compelling technology booster for noise-sensitive, high-frequency RF applications. This is on account of a relatively constant NF_{min} and improved R_n, N_M, f_{MAX} and f_T under the presence of parasitic capacitance similar to that of industrial RF technologies [13]. While interfacial thinning will reduce the EOT, the mobility degradation due to interfacial thinning leads to undesirable RF performance. This suggests that mobility enhancement techniques should be utilized to carefully manage the effects of lowering the EOT via thinning the interfacial layer.

4.1 Noise Parameters and EOT Scaling

The results of this study are conducted at the maximum g_m bias point on the measured $L_g = 90$ nm device. It is assumed that reducing the EOT has the strongest effect on the parameters g_m, $C_{gs,i}$, and $C_{gd,i}$, though EOT scaling is also expected to reduce the output conductance g_{ds} via mitigation of short channel effects. Since we are assuming g_m, $C_{gs,i}$, and $C_{gd,i}$ are the main parameters affected by EOT scaling, we simply need to develop a physical model for how these change with C_{ox}. C_{gs}, C_{gd}, and g_m are all proportional to the inversion charge density Q_{inv} [36], and in strong inversion $Q_{inv} \propto C_{ox}$. This implies the total

Table 4.1: Extracted RF Parameters for $L_g = 90nm$ NCFET

Symbol	Quantity	Parameter Value
R_g	Extrinsic Gate Resistance	119.3 Ω
R_d	Extrinsic Drain Resistance	7.60 Ω
R_s	Extrinsic Source Resistance	1.74 Ω
L_g	Extrinsic Gate Inductance	0 H
L_d	Extrinsic Drain Inductance	1.042×10^{-11} H
L_s	Extrinsic Source Inductance	0 H
$C_{gs,e}$	Parasitic Gate-Source Capacitance	9.75 $\times 10^{-15}$ F
$C_{gd,e}$	Parasitic Gate-Drain Capacitance	10.5 $\times 10^{-15}$ F
$C_{gs,i}$	Intrinsic Gate-Source Capacitance	15.96 $\times 10^{-15}$ F
$C_{gd,i}$	Intrinsic Gate-Drain Capacitance	1.59 $\times 10^{-15}$ F
C_{ds}	Total Drain-Source Capacitance	1.50 $\times 10^{-15}$ F
$g_{m,i}$	Intrinsic Transconductance	32.87 $\times 10^{-3}$ S
r_{ds}	Output Resistance	293.6 Ω
r_{gs}	NQS Gate-Source Resistance	22.1 Ω
r_{gd}	NQS Gate-Drain Resistance	28.9 Ω
τ	Transit Time Parameter	596 $\times 10^{-15}$ s

Parameters are extracted at a DC operating point of $V_{gs} = 1.4V$, $V_{ds} = 1.0V$.
Device width is 20 μm.

intrinsic gate capacitance $C_{gg,i} = C_{gs,i} + C_{gd,i}$ and the transconductance g_m should both scale proportionally to C_{ox}. Note that the ≈ 20-25% improvement in $g_{m,i}$ and C_{gg} closely tracks the C_{ox} difference between the HfO_2 control and HZH reported in [39]. This suggests that even these simple relations yield relatively accurate scaling predictions.

Since strong inversion physics dictates that direct proportionality is a good approximation for the scaling behavior of these parameters, all that remains is to determine the inversion capacitance difference for varying EOTs under fixed bias conditions. In order to quantify this, capacitance vs. voltage characteristics corresponding to EOTs from 9.5 Å to 3 Å were generated using simulations from a self-consistent Poisson-Schrodinger solver (SCHRED) [59] with doping, channel thickness, and metal work-functions calibrated to device parameters. Using SCHRED C-V simulations for each EOT, the increase/decrease factor in capacitance (θ_{EOT}) relative to the measured 7.5 Å EOT was computed. S-parameters for each EOT simulation were then generated by scaling the following intrinsic element parameters as follows:

$$g_{m,new} = g_m \times \theta_{EOT} \tag{4.1}$$

$$C_{gs,new} = (C_{gs,int} \times \theta_{EOT}) + C_{gs,par} \tag{4.2}$$

$$C_{gd,new} = (C_{gd,int} \times \theta_{EOT}) + C_{gd,par} \tag{4.3}$$

$$\theta_{EOT} = 1.0 + \frac{C_{ox,new} - C_{ox,7.5}}{C_{ox,7.5}} \tag{4.4}$$

The above forms the basis for a projection model for NCFETs. A few additional considerations are needed to produce a scaling model for ILD thinning. Since NCFET EOTs begin at 7.5 Å EOT, and high-κ metal gates achieve 9.5 Å EOT without the use of interlayer thinning [41], we start NC scaling simulations from 7.5 Å and ILD thinning simulations from 9.5 Å by down-scaling the g_m and $C_{gg,i}$ by θ_{EOT}. For interfacially thinned dielectrics, remote phonon scattering increases due to a closer proximity of the high-K dielectric to carriers in the channel [2]. In order to model the mobility degradation due to interfacial thinning, a 20 cm^2/Vs rate of mobility reduction per angstrom thinned is assumed, per the empirical trend discussed in [2].

This means, when considering the trend of g_m for interfacial thinning, we must account for both the charge improvement and the mobility degradation. Luckily, this is not too difficult. In strong inversion, the device transconductance can be written as [36]:

$$g_m = \mu C_{ox} \frac{W}{L}(V_{gs} - V_t) \propto \mu \times Q_{inv} \tag{4.5}$$

The above equation demonstrates we can separately consider the effects of the capacitance enhancement (via improvement in Q_{inv}) and remote phonon scattering (via degradation to μ). The g_m scaling equation used for interfacially thinned dielectrics is finally constructed as:

$$g_{m,new} = g_m \times \theta_{EOT} \times \theta_\mu \tag{4.6}$$

where θ_{EOT} is the EOT improvement factor as previously elaborated, and θ_μ is the decrease factor in mobility relative to the mobility at 9.5 Å EOT:

$$\theta_\mu = (\mu_{9.5} - 20 \times (9.5 - EOT_{new}))/\mu_{9.5} \tag{4.7}$$

A mobility value at 9.5 Å EOT is all that is required to compute θ_μ. For this work, a mobility of 210 cm^2/Vs is extracted from MIT Virtual Source Model (MVS) device fittings of NCFET SOI devices [51], which is also similar to the mobility reported in [39]. Although those mobility values were extracted for NC devices at a 7.5 Å EOT, we use this value for ILD simulations starting at a 9.5 A EOT, since NC gate dielectric transistors have demonstrated very similar mobility to control high-K devices in multiple experimental trials [51, 52, 39]. It is important to note higher starting mobility values will help ameliorate the relative g_m degradation from interfacial thinning, since the empirical rate of degradation is fixed.

4.2 Modeling using the Noise Correlation Matrix Method

The noise parameters NF_{min}, $Y_{opt} = G_{opt} + jB_{opt}$ and R_n are calculated from the noise correlation matrix method described in [14, 18, 45, 33]. The intrinsic Y-parameters described in Chapter 2 are used in the correlation matrix method as Y_{int}.

For a MOSFET, the two main noise sources to consider are the channel thermal noise and the gate induced noise, each of which requires a separate compact model.

For the channel noise power spectral density (PSD), the following compact model is used [27, 26, 14, 50]:

$$S_{iD} = 4k_B T \gamma_{nd} g_m \tag{4.8}$$

The formulation of the induced gate noise PSD as given in [26, 27, 4] is also adopted:

$$S_{iG} = 4k_B T \delta_{ng} \frac{(\omega C_{gs})^2}{5 n g_m} \tag{4.9}$$

In Equations (15) and (16), γ_{nd} is the excess drain thermal noise parameter, δ_{ng} is the induced gate noise coefficient, and n is the subthreshold slope nonideality factor.

In order to correctly model the EOT scaling behavior, any dependence of these three noise model parameters on the EOT must be captured.

EOT Dependence of RF Noise Model Parameters

The sub-threshold slope factor n is the easiest to determine the scaling behavior of, as it has a clear thermal limit, and a simple equation that relates its dependence on the oxide capacitance. The factor n is given as [36]:

$$n = \frac{SS}{ln(10)kT/q} = (1 + \frac{C_{dep}}{C_{ox}}) \tag{4.10}$$

where SS represents the sub-threshold swing. Using the measured sub-threshold swing from the device transfer characteristics, C_{dep} is extracted using the oxide capacitance for EOT = 7.5 A. C_{ox} is then adjusted by θ_{EOT} as EOT varies, which changes n to properly adjust S_{iG} with EOT scaling.

The excess thermal noise parameter γ_{nd} is among the more challenging RF variables to model, as its physical origins may come from different sources, ex. velocity saturation and hot carrier effects [55], and as γ_{nd} can be considerably higher than long channel expectations [25, 37, 27, 57]. However, as this chapter focuses on the scaling behavior of the noise with oxide capacitance, we assume the long channel value of 2/3 [14], making clear acknowledgement of the above caveats. In terms of EOT dependence, the traditional expression for γ_{nd} is: [57, 55]:

$$\gamma_{nd} = \frac{S_{id}}{4k_B T g_{ds,0}} \tag{4.11}$$

where S_{id} and $g_{ds,0}$ are both proportional to the inversion charge density Q_{inv}. Since $Q_{inv} \propto C_{ox}$, and the numerator and denominator have the same Q_{inv} dependence, we conclude γ_{nd} should not experience significant fluctuation with EOT scaling.

The induced gate noise coefficient δ_{ng} is taken to be a constant at $\frac{4}{3}$, in line with literature values for strong inversion bias conditions. Most of the RF modeling literature that has studied δ_{ng} has noted that its strongest dependency is on the bias conditions [4, 26].

Lastly, we consider the EOT dependence of the parameter c_g (noise correlation coefficient) although it is not explicitly written in the power spectral density expressions. In a MOSFET, the gate noise and drain current noise PSDs are not independent of each other, as the AC coupling between the gate and channel terminals means noise fluctuations on one side of the gate capacitor generally induce noise on the other capacitor terminal as well [19, 37, 20]. c_g represents the correlation between these two noise sources.

The correlation coefficient is classically given as [27, 58]:

$$c_g = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \tag{4.12}$$

where $\overline{i_g^2}$ and $\overline{i_d^2}$ correspond to our notation of S_{iG} and S_{iD} respectively. From the van der Ziel MOS noise correlation theory [18, 58], $S_{ig} \propto C_{gs}^2/g_{ds,0} \propto Q_{inv}$, $S_{iD} \propto Q_{inv}$, and $\sqrt{S_{iG}S_{id}^*} \propto C_{gs} \propto Q_{inv}$, which implies c_g should not vary too strongly with EOT. Regardless, it is known that c_g becomes smaller than the long-channel limit of 0.395j with reductions in device channel length [18, 19, 25]; for the channel length under consideration, low levels of noise correlation are very likely. In summary, of y_{nd}, d_{ng}, c_g and n, only the latter is expected to fluctuate significantly with EOT scaling, up until the thermal swing limit.

4.3 Projection Results

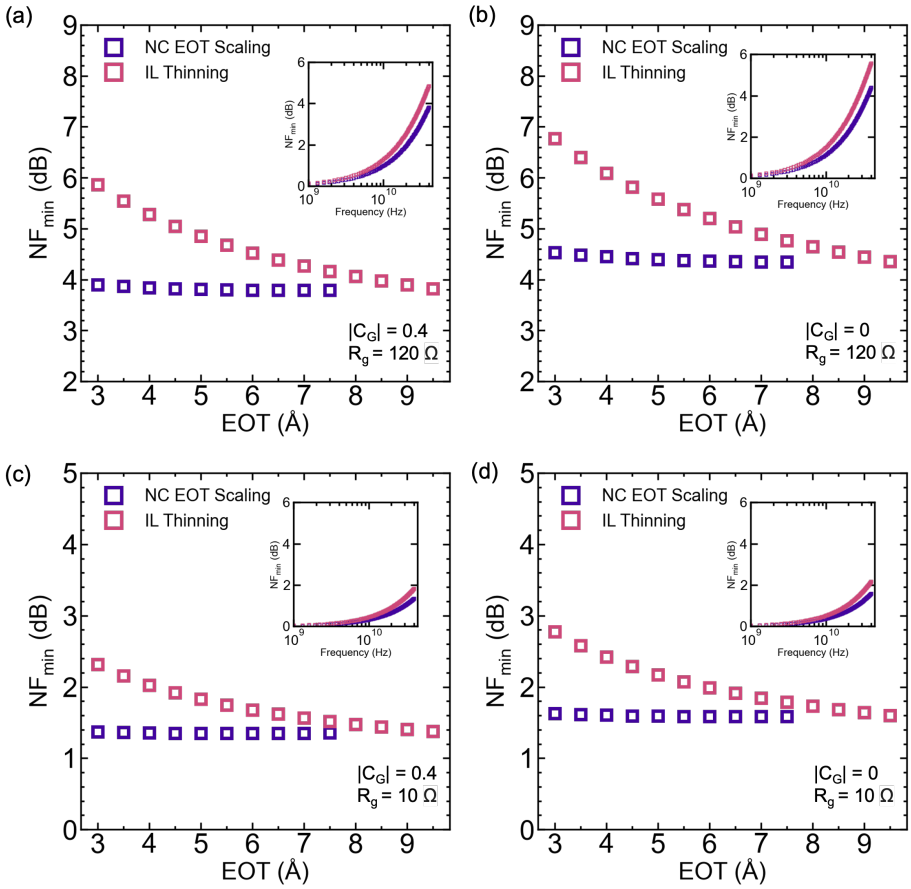

Figure 4.2: Scaling of NF_{min} under high and low R_g assumptions, and varying correlation. Insets are frequency behavior at 5 angstrom EOT.

Fig. 4.2 shows the modeled NF_{min} projection at 40 GHz from NC-based EOT scaling and interfacial layer thinning. While ILD thinning causes a rise in NF_{min}, NC-based EOT scaling shows minimal change in NF_{min} down to 3Å (Fig 3a). The divergence in behavior between the two scaling approaches can be understood through a 'noise compensation' effect in NC-based EOT scaling, wherein any increase in noise current from higher Q_{inv} is matched by the recovery in device current gain from parasitic capacitance suppression. This effect leads to an unchanged output signal-to-noise ratio.

Under moderate frequency assumptions [1],

$$F_{min} \approx 1 + 2(\frac{\omega}{\omega_T})\sqrt{g_m R_g \frac{\gamma_{nd}}{\alpha}} \tag{4.13}$$

Expanding ω_T:

$$F_{min} \approx 1 + 2(\frac{f}{\frac{g_m}{C_{gg,i}+C_{par}}})\sqrt{g_m R_g \frac{\gamma_{nd}}{\alpha}} \tag{4.14}$$

Grouping like quantities, Equation 4.14 simplifies to:

$$F_{min} \approx 1 + 2(\frac{(C_{gg,i} + C_{par})f}{\sqrt{g_m}})\sqrt{R_g \frac{\gamma_{nd}}{\alpha}} \tag{4.15}$$

Since EOT scaling affects g_m and $C_{gg,i}$ assuming a fixed C_{par}, an unchanged noise figure implies the improvement in device current gain (f_T) corrects for any increase in the channel thermal noise PSD ($\propto g_m$). By contrast, the degradation in the noise performance of ILD thinning suggests the g_m is deteriorating; i.e. mobility is degrading faster than the scaling of inversion charge. Since the intrinsic capacitance improvement is the same, a weaker g_m scaling trend will lead to higher NF_{min} as suggested by Equation 4.15.

It is notable that this trend does not seem to be a strong function of either the gate resistance or the correlation coefficient. An R_g of $\approx 10\Omega$, which can be achieved through optimized layout techniques [1], is simulated vs. the measured 120 Ω (Fig. 4.2a, 4.2b), Likewise, the uncorrelated noise source case is also simulated (Fig. 4.2b, 4.2d); although the uncorrelated case demonstrates higher overall noise performance, the scaling behavior is unchanged.

Another quantity of interest in low noise RF design is the two-port noise sensitivity parameter R_n. To achieve NF_{min}, one must have the optimal source admittance Y_{opt}. Matching with a source admittance of Y_{opt} is challenging due to noise match and power match design tradeoffs, and on account of process variation. The noise sensitivity parameter R_n informs us of the penalty we suffer in the noise figure as we deviate from Y_{opt}. R_n plays this role as follows [14]:

$$F = F_{min} + \frac{R_n}{G_s}|Y_s - Y_{opt}|^2 \tag{4.16}$$

where Y_s is the source admittance and $G_s = \Re(Y_s)$. One compact model for R_n is [14, 4]:

$$R_n \approx R_g + \frac{\gamma_{nd}}{g_m} \tag{4.17}$$

Examining Equation 4.17, it is reasonable to use the quantity $R_n - R_g$ as a metric of the intrinsic noise sensitivity of the device, since the gate resistance can be reduced with processing and layout techniques. R_n is simulated across EOT in Fig. 4.3. Our simulations of R_n are consistent with prior reports of minimal variation across frequency [20, 21, 26, 14], which is also implied by the analytical model of Equation 4.17. The trend in Fig. 4.3 is then

simply explained by the trend in g_m. The higher g_m of NCFETs allows for a smaller noise sensitivity (Fig. 4.3a & b). Similarly, the degradation in g_m from remote phonon scattering leads to a higher intrinsic noise sensitivity for IL-thinned devices (Fig. 4.3 a).

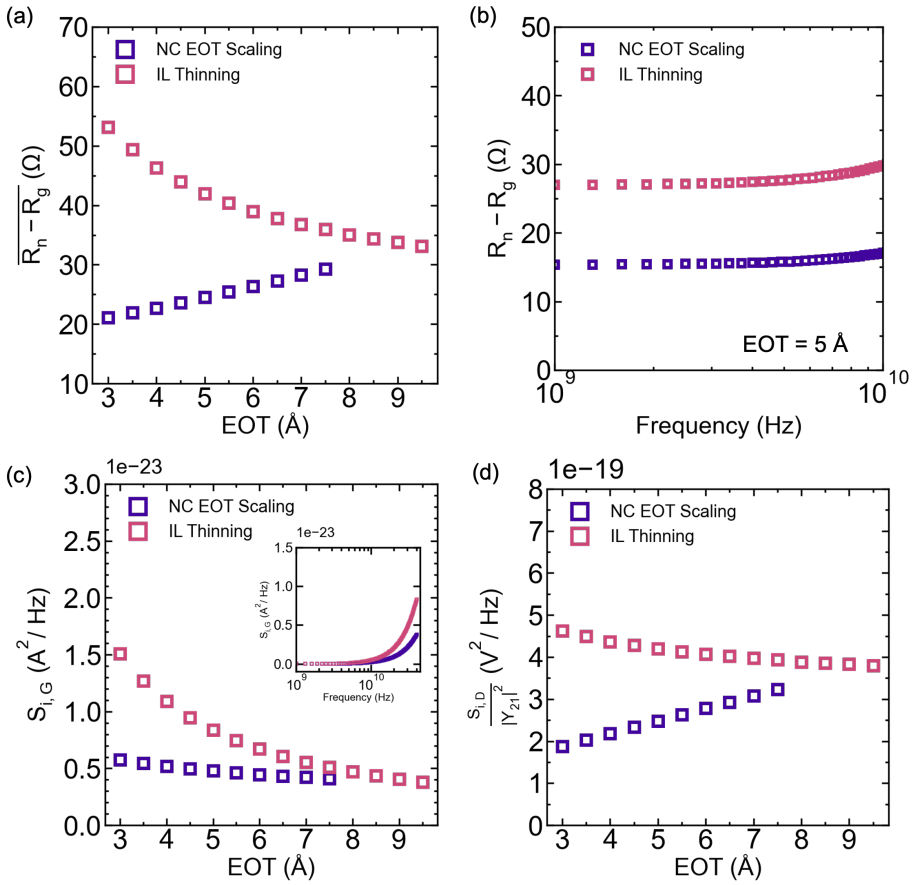

Figure 4.3: Scaling of the noise sensitivity parameter (R_n) and the noise power spectral densities S_{iD} and S_{iG}. 4(c) Inset: 5A EOT simulation.

The input referred noise power spectral densities S_{iG} and S_{iD} are simulated versus EOT at 40 GHz (Fig. 4.3 c & 4d). Because $S_{iG} \propto \frac{(C_{gs}+C_{gs,par})^2}{g_m}$, a similar noise compensation effect as discussed earlier happens for NC EOT scaling, whereas ILD g_m degradation increases S_{iG}. The input-referred $S_{iD}/|Y_{21}|^2$ follows the behavior of R_n, as expected. This relation can be elucidated from two-port theory. R_n can be considered as the ratio of two Thevenin/Norton equivalent input noise sources $\overline{v_n^2}$ and $\overline{i_n^2}$, which arise from modeling the MOSFET as a noiseless two-port system with noisy input sources [4]. In this view, input-referring S_{iD} creates an equivalent voltage noise that contributes to $\overline{v_n^2}$. Thus, if the Norton equivalent noise current source $\overline{i_n^2}$ varies weakly, R_n should track the input-referred S_{iD}.

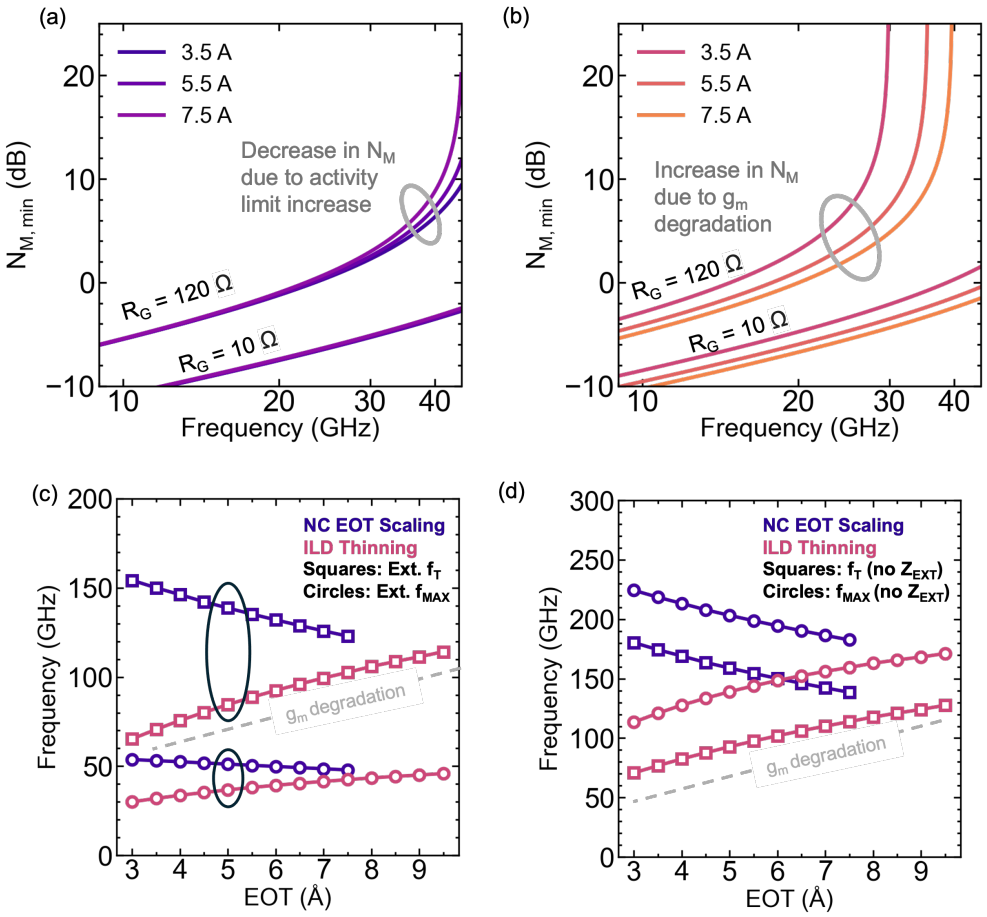

Figure 4.4: Noise measure due to NC EOT scaling and interfacial layer thinning. Extrinsic and intrinsic f_T/f_{MAX} vs. EOT explain the behavior in N_M.

When designing an RF LNA, it is important to provide ample gain alongside a good signal to noise ratio. This suggests that a good figure of merit for amplifier performance is one that accounts for both the noise and the gain under consideration [32]. This motivates our study of the noise measure (N_M) scaling performance, which is depicted in Figure 4.4. The noise measure is computed as given in [6]:

$$N_M = \frac{NF - 1}{1 - \frac{1}{G}} \tag{4.18}$$

The power gain G is computed as the available two-port gain (G_{av}) assuming a source-matched admittance of Y_{opt}:

$$G_{av} = \Re(\frac{Y_{opt}}{Y_{eq}})|\frac{Y_{21}}{Y_{11} + Y_{opt}}|^2 \tag{4.19}$$

where the Norton equivalent admittance Y_{eq} is simply the two-port output admittance $Y_{eq} = Y_{22} - \frac{Y_{12}Y_{21}}{Y_{11}}$.

N_M is known to increase at a rapid rate near the maximum power gain frequency f_{MAX} (sometimes called the activity limit [6]). The f_{MAX} is low in this device due to an un-optimized R_G, which means the large increase in N_M is clearly visible around 40 GHz. However, NC EOT scaling reduces the noise measure in this regime (Fig. 4.4a), which is not implied by the scaling behavior of NF_{min} that we have discussed so far. Examining Equation 4.18, this implies that NC EOT scaling increases the available power gain G. We will show that this is directly implied by the increase in f_T due to suppression of parasitic capacitance.

f_T is analytically given as:

$$f_T = \frac{g_m}{2\pi \times (C_{gg,i} + C_{par})} \tag{4.20}$$

Considering EOT scaling, f_T can be written as:

$$f_T(\theta_{EOT}) = \frac{(g_m)(\theta_{EOT})}{2\pi \times ((C_{gg,i})(\theta_{EOT}) + C_{par})} \tag{4.21}$$

which is monotonically increasing for $\theta_{EOT} \geq 1$.

f_{MAX} can further be analytically expressed as:

$$f_{MAX} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_s) + 2\pi f_T R_g C_{gd}}} \tag{4.22}$$

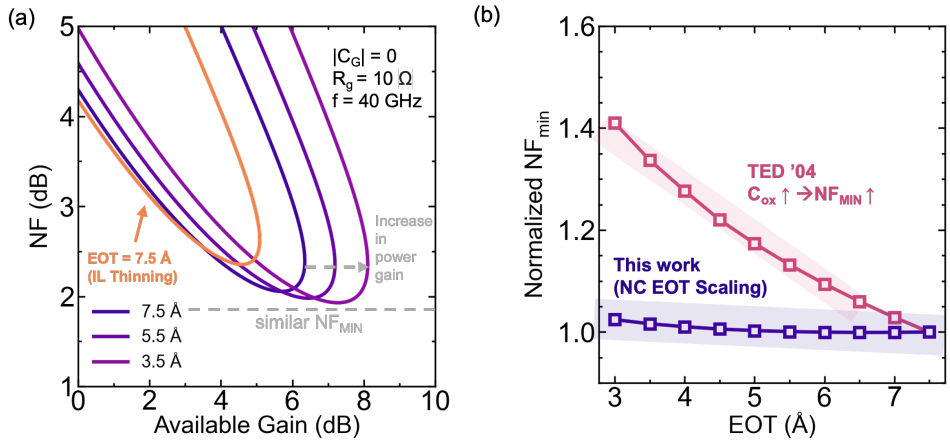

Figure 4.5: Noise Figure vs. Gain contours and scaling trend vs. literature reports.

which clearly demonstrates that an increase in f_T implies an increase in the corresponding power gain activity limit f_{MAX}, given the numerator of Equation (4.22) is a stronger function of f_T than the denominator. Fig. 4.4c and 4.4d show the simulated increases in f_T and f_{MAX} from NC EOT scaling. Comparing Fig. 4.4c-d to the behavior in Fig. 4.4a-b, it is clear an increase in f_T from NC EOT scaling drives an increase in f_{MAX}, which cumulatively reduces N_M. Due to the severe g_m degradation, ILD thinning decreases both activity limits, which induces an increase in the N_M.

In closing, we consider how to visualize the tradeoff NC dielectrics offer, and how the approach of this work differs from previous literature reports. In Figure 4.5 (a), the noise figure is simulated against the available power gain for real Y_s swept from 10^{-4} S to 10^4 S at an operating frequency of 40 GHz. The three NC curves demonstrate a similar NF_{min} while G_{av} improves, which accords with previous arguments. As a fun aside, the smaller noise sensitivity R_n can be directly visualized from the reduced convexity of the 3.5Å curve compared to the 7.5Å curve. Comparing against the IL-thinned 7.5Å EOT curve, we see a higher R_n, lower power gain, and higher NF_{min}. This suggests that the harm to g_m from IL thinning must be managed carefully to leverage EOT scaling benefits for RF integrated circuits. One approach to improve the IL scaling performance would be to increase the initial unscavenged mobility by a strain engineered channel [23, 53]. With NC EOT scaling, the unharmed carrier transport [52] allows circuit designers to fully leverage the effects of increasing g_m and $C_{gg,i}$. By considering the influence of C_{par} suppression in this work, we unveil a notably different scaling trend to prior predictions [4], where an increase in C_{ox} was expected to increase the minimum noise figure. However, as silicon CMOS scales into the tens of nanometers for RF applications, accurately modeling the recovery of f_T is crucial to understand the scaling behavior of this emerging device technology.

Chapter 5

Conclusion

In closing, we have covered a low-temperature study of p-type NCFET devices from 300 K to 77 K, and an analytical examination of the RF noise performance with NC-enabled EOT scaling. The results of this work suggests a few compelling pathways ahead for future research:

1. Given the confirmation of NC in both n and p-type devices, simulation of key integrated circuit blocks (e.g. SRAM, logic circuits, VCOs, ring oscillators) across temperature is now possible. Since NC dielectrics enable a higher current for a fixed gate voltage, this improvement can potentially be traded off against the supply voltage to meet the DARPA target of a 200 mV power supply for logic computing [24].

2. While most of the work on negative capacitance FETs has focused on their suitability for digital electronics, there is a paucity of work on their application in analog/RF electronics. Future research in NCFETs may focus on realizing higher f_T in short-channel devices, and on optimization of device electrostatics / fabrication for improved self-gain and reduced contact resistance in pFETs.

3. As RF applications tend into the sub-THz regime, confirming the stability of the NC gate dielectric (i.e. minimal capacitance dispersion) into this frequency regime remains to be demonstrated, as the highest frequency testing in the literature has been to 40 GHz. Operation of NC dielectrics in the sub-THz regime will be additional proof that the dielectric enhancement is not a transient effect.

The frontiers of negative capacitance device research continue to be explored, with numerous exciting applications and discoveries cementing a pathway for improved silicon CMOS performance for years to come.

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