A Data Converter Assisted Beamforming Technique

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By

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Professor Ali Niknejad
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Abstract

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Directional communication, a pivotal feature in 5G technology and beyond, expands channel capacity by leveraging spatial information from a multiple-antenna front-end. Fully digital beamforming facilitates advanced signal processing techniques like spatial blocker suppression and beam search. However, in the presence of spatial blockers, the digital backend requires high dynamic range data converters and other front-end components to maintain information integrity. Since the system is typically designed based on worst-case scenarios, the high dynamic range modules can consume substantial energy. This has sparked increased interest in beamforming or spatial filtering research in the analog/RF front-end. While inserting a spatial filter in the signal path can attenuate spatial blockers early and benefit the following signal path, it generally increases the power budget and additional noise.

In this work, we present the design of an integrated phase shifter based on switched capacitors. Subsequently, the proposed phase shifter is utilized in the beamformer. The baseband beamforming operation is executed in the charge domain, immediately preceding the analog-to-digital conversion. This approach diverges from existing research, which typically incorporates additional active beamforming blocks in the signal path, necessitating supplementary gain stages. Instead, our proposed beamformer is fully passive and integrated into successive approximation register (SAR) ADCs with the existing circuitry. The modification is limited to the sampling phase of the SAR ADC to ensure compatibility with the beamforming functions, without impacting the ADC's throughput.

The proposed data converter assisted beamforming method leads to low area and power overheads while maintaining compatibility with various other spatial filtering methods. Two test chips were fabricated using 16nm node technology. The measured data converter beamformer demonstrated a null depth exceeding 32dB with arbitrary programmability, consuming 52.1mW for each digital output beam.

To My Family

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Acknowledgments

After nearly six years at Berkeley, my fascinating PhD journey has reached its end. I've been working in the industry for about a month since I left school. In comparison, I would describe the PhD experience as painting, where surprising and wild ideas can be drawn on canvas, and their shining points can be emphasized. In contrast, industry work is more like sculptural arts. The design must stand and be reasonable from all angles. Many research works by PhD students have yet to be used for products, as most of them would be considered "high risk" by the industry. I find myself enjoying both worlds. I would definitely recommend pursuing a PhD for students who want more experience in integrated circuits.

I would like to express my deepest gratitude to my advisor, Professor Borivoje Nikolic. Thank you for guiding me in my research direction and patiently answering my questions. I still vividly remember the first time we met at BWRC. I was visiting from China with my undergraduate school team. We were exploring universities and reaching out to professors for possible graduate school opportunities. I was incredibly fortunate to receive your reply stating that you could meet me in BWRC in an hour. Unfortunately, at that exact time, our team was visiting "another school" 40 miles away. I jumped into an Uber, and despite the Bay Area's notorious afternoon traffic, the driver managed to get me to BWRC in an hour. After a brief conversation with you and some of your students, I knew Berkeley could be the perfect fit for me. Half a year later, when Berkeley's offer arrived, I felt like my dream had come true and accepted it without hesitation.

I would like to extend my gratitude to Professor Ali Niknejad and Professor Vladimir Stojanovic from BWRC, as well as Professor Aaron Parsons from Astronomy, for graciously accepting my invitation to be on my committee and providing valuable feedback on the project.

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Chapter 1

Introduction

The capacity of wireless systems has been steadily increasing due to advancements in wireless standards and technology. The first widely deployed analog cellular system, known as the Advanced Mobile Phone System (AMPS), was developed in North America in the 1980s [1]. Later, AMPS partially transitioned to digital, leading to the deployment of the Digital AMPS (D-AMPS) standard in 1993 [2]. Wireless network speed has increased exponentially in the past decades [3]. However, emerging technologies and applications still demand more. For example, intelligent automobiles with fully autonomous driving features are approaching the horizon [4]. VR/AR technology is also gaining attention as the next generation of human-machine interfaces [5]. The global pandemic in recent years has inadvertently accelerated the trend toward remote work, which is expected to continue even after the pandemic ends.

These emerging demands continue to drive the search for advanced fundamental techniques that can further improve network capacity and transmission speed while reducing cost and power consumption. For example, due to computational limitations, automobiles may need to offload some computation tasks to cloud servers and wait for the results [6]. However, this approach can be risky as network coverage and latency are critical in such applications, and current wireless communication solutions may not meet the required standards.

Similarly, many consumer wearable VR/AR devices are powered by portable batteries, which can compromise the immersive experience when bulky battery packs must be attached. Unfortunately, the advancement of battery technology in recent decades has not kept pace with the demand for computational capability. Low latency and ultra-low power wireless transmission solutions could help alleviate this challenge. For instance, dense computation could be performed in a nearby computational resource and then transmitted back to the wearable device, which would only need to collect data, transmit, and display information. This approach could significantly extend the device's battery life and improve the user experience when transmission energy is less than the computation. Furthermore, the demand for high-speed wireless connectivity is also being driven by the increasing prevalence of smart devices and the Internet of Things (IoT). These devices require constant and reliable connectivity for real-time data exchange, which puts further strain on existing wireless networks. As a result, there is a growing need for innovative wireless communication solutions to support

the massive connectivity demands of the future.

For wireless hardware researchers, designing wireless infrastructure with larger capacity, lower latency, and lower power consumption is fundamentally beneficial for almost all emerging technologies and applications and even inspires ideas that haven't yet materialized or seem impossible at this moment. Researchers have devoted significant effort to improving channel efficiency to increase network capacity further. State-of-the-art coding techniques have pushed spectral efficiency close to the Shannon limit [7]. Additionally, network capacity can be increased by utilizing higher bandwidth or spatial multiplexing. While available bandwidth below 6GHz is limited, ample bandwidth is available in the mm-wave range [8], such as the unlicensed V-band and lightly licensed E-band [9].

A significant limitation of mm-wave technology is its high attenuation and absorption when propagating through the atmosphere. To compensate for path loss, increasing the density of the base stations or the transmission power per TX channel is necessary. Spatial multiplexing addresses this issue by concentrating most of the power in a specific direction to achieve a better signal-to-noise ratio (SNR). With more antennas on the front-end, a base station can achieve better spatial selectivity and support more orthogonal beams. Many researchers have combined high frequency and spatial multiplexing to significantly increase system throughput [10]. However, similar to many other complex systems, most of this work involves trade-offs among several different aspects to realize the proposed features. For example, analog front-ends with embedded spatial notch filters require the insertion of multiple spatial notch cancellers in the signal path, which also attenuates the desired signal. Multiple gain stages must be added to compensate for the gain loss, resulting in high power consumption and lack of scalability [11]. Another approach is forming beams in the analog domain for power efficiency [12]; however, this method has limited spatial resolution because of the limited phase shifter control step.

In this dissertation, we discuss a novel method for baseband beamforming. Two critical components, the phase shifter and the beamformer, are implemented with programmable switched capacitor arrays and efficiently integrated with the data converters. No additional component is required in the gain path. This approach offers the significant advantage of achieving accurate phase adjustment and spatial resolution, and incurs very low area and power overhead. To validate the concept, we designed two prototypes for the phase shifter and beamformer separately. This work utilizes Berkeley analog generator (BAG) to assist the design process. The prototypes are successfully brought up after fabrication and measured.

This dissertation is structured as follows. In the remaining part of this chapter, we provide background information on directional communication, review state-of-the-art hardware and systems designed by other researchers, and introduce the design tool developed by UC Berkeley that we used in our work. Chapter 2 presents the proposed phase shifting and beamforming method, followed by a discussion of its feasibility from a high-level perspective. Chapters 3 and 4 delve into the design details, challenges, and considerations, with Chapter 3 focusing on the phase shifter and Chapter 4 on the beamformer. Chapter 5 showcases the measurement setup and results of the chip prototype. Finally, Chapter 6 concludes the dissertation and outlines future work.

1.1 Directional Communication

Over the past decade, there has been a rapid proliferation of wireless mobile devices. This surge in wireless connectivity has led to an increasing demand for high-speed, low-latency wireless links, especially in dynamic environments. According to the Shannon–Hartley theorem, the channel capacity is constrained by the available bandwidth and signal-to-noise ratio (SNR) with an arbitrarily low error rate.

$$C = B \log_2(1 + \frac{Signal}{Noise}) \tag{1.1}$$

In a wireless system that supports multiple user equipment (UE), the other UEs in the network are considered noise for a specific UE. Keeping different UE well separated from each other can improve the SNR and further increase the channel capacity. As illustrated in Fig. 1.1, separating users in the time or frequency domain has been widely used. For instance, the IEEE 802.22 standard first developed cognitive radio (CG) regional network standard, which allows sensing the spectrum and allocating available channels to users [13]. In 5G and beyond, the spatial domain provides another degree of freedom to reduce user interference. The multiple-antenna technique enables non-uniform gain in space, further improves the spectrum efficiency, and reduces transmitted power.

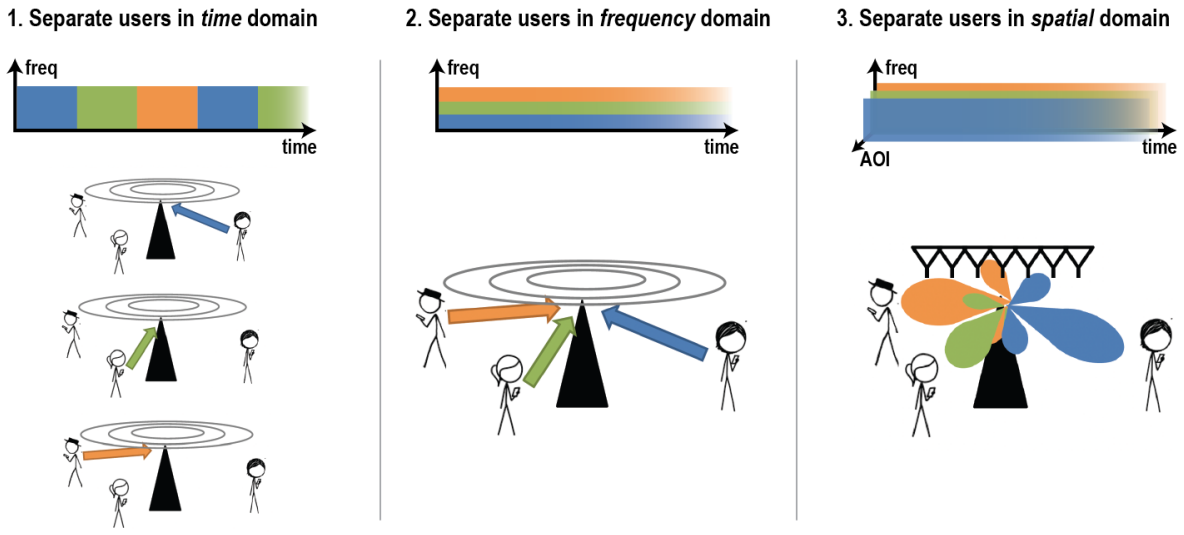


Figure 1.1: Diagram of separating users in time, frequency, and spatial domains to improve network capacity.

1.1.1 Background of Phased Arrays

Using antenna arrays to create non-uniform spatial gain is not a recent development. The first antenna array was constructed over a hundred years ago [14]. Shortly after that, Brown experimented with two antennas spaced half a wavelength apart, feeding them with different phase signals [15]. He observed that the signal was strongest in the plane defined by the two antennas. In 1901, in preparation for his groundbreaking transatlantic wireless experiment, Guglielmo Marconi constructed a massive antenna array consisting of four hundred wires suspended from 20 masts, each 200 feet tall, arranged in a circle. Marconi conducted numerous experiments with multiple antennas to enhance gain in specific directions [16].

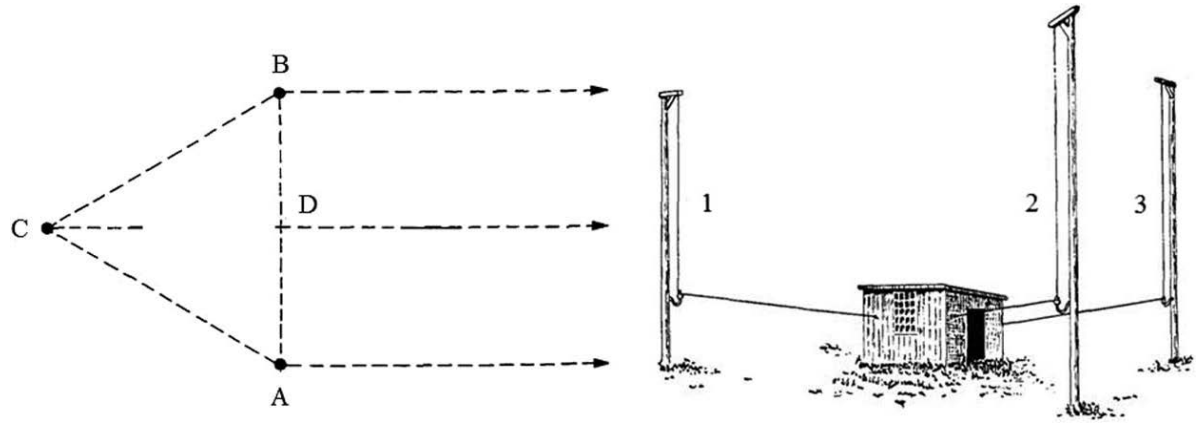


Figure 1.2: Ferdinand Braun's three element array [15].

Nobel Prize winner Ferdinand Braun positioned three monopoles in a triangle configuration, as depicted in Fig. 1.2. The signal at antenna C had a phase of 100° and twice the amplitude of the signal at antennas A and B, which had a phase of 0°. They discovered that the array emitted a cardioid pattern. Braun was the first to use phase to steer the main beam, earning him credit as the inventor of the antenna array. Subsequently, passive and active phased arrays have been primarily utilized in military radar and commercial broadcasting. As we progress into the 21st century, the size and cost of phased arrays have decreased alongside the radio wavelength, leading to their integration into everyday commercial applications and wireless standards [17].

Using multiple antennas can be power-intensive, as the system power tends to increase with the number of antennas. However, a significant advantage of employing multiple antennas is the potential improvement in SNR.

Consider a scenario where a receiver system comprises two identical antennas. The received signals will have the same phase if the signal source is equidistant from both antennas. The summation of these signals will result in doubling the amplitude, meaning the total receiving power is four times that of using a single antenna in this scenario. Conversely, the

noise in the two paths to the receiver is uncorrelated. This means that the total noise power is only doubled. Consequently, the SNR is doubled compared to a single antenna receiver. For a front-end receiver with N antennas, the system SNR ideally improves by a factor of N compared to the SNR of a single antenna front-end.

$$\begin{aligned} \mathrm{SNR}_N &= \frac{(N \cdot \mathrm{Signal})^2}{N \cdot \mathrm{Noise}} \\ &= N \cdot \mathrm{SNR}_1 \end{aligned} \tag{1.2}$$

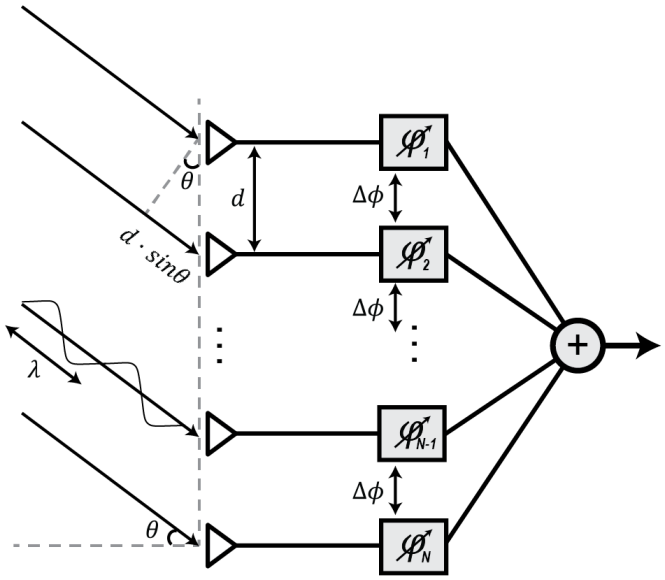


Figure 1.3: Phase delay calculation between each antenna element. N antennas with spacing d are used in the phased array.

When the distances from the signal source to the antennas are unequal, a controllable phase adjustment or delay must be applied before summation to align the phases; otherwise, it could lead to gain loss. For instance, in the previous example of a 2-antenna front-end, if the difference in distance is half a wavelength, the received signals will have reversed amplitudes, and their summation will cancel each other out. Figure 1.3 illustrates the geometry for determining the delay between antenna elements.

For simplicity, assume the distance from the signal source to the antenna plane is significantly larger than the antenna spacing d. The receiving signal can be approximated as parallel input. For a signal with the angle of arrival (AoA) θ, the travel distance difference between the adjacent antenna is:

$$\Delta d = d \cdot \sin\theta \tag{1.3}$$

The wavelength λ corresponds to the phase of 2π. Each antenna element's resulting phase difference is $\Delta\phi$. The antenna spacing d is typically picked as half-wavelength $\lambda/2$, preventing under-sampling and aliasing effect (grating lobes) [10]. The resulting phase difference is:

$$\begin{aligned} \Delta\phi &= 2\pi \cdot \frac{\Delta d}{\lambda} \\ &= 2\pi \cdot \frac{(\lambda/2)\sin\theta}{\lambda} \\ &= \pi \cdot sin\theta \end{aligned} \tag{1.4}$$

The simplified phase array model holds true when the transmitter is located far away from the antennas relative to the signal's wavelength. In such cases, the angle of incidence (AOI) difference between each antenna element is negligible, and they can be considered to be in parallel with each other. However, if the transmitter is close to the antenna array or if the array is large in scale, the phase difference between antenna elements is no longer a fixed constant. In such scenarios, using an array of phase differences $[\Delta\phi_1, \Delta\phi_2, ..., \Delta\phi_{N-1}]$ can help align the signals better.

Additionally, in the case of wideband signals, a single phase difference $\Delta\phi_f = c/\lambda$ cannot represent the real-time delay for all frequencies in the band. Instead of adjusting the signal phase, an actual delay module should be applied to each antenna element. The delay for each component is calculated from the distance difference $\Delta t = \Delta d/c$, where Δd is the distance difference and c is the speed of light.

Using more antennas not only improves the signal-to-noise ratio (SNR) but also enhances spatial selectivity. As illustrated in Fig. 1.4 (a), the spatial pass-band becomes narrower with an increase in the number of antennas. For angles of incidence θ ranging from -90° to 90°, there is a straightforward 1-1 mapping between θ and phase difference $\Delta\phi$: $f : \theta \rightarrow \Delta\phi$. Conversely, controlling the phase delay can steer the direction, denoted as $g : \Delta\phi \rightarrow \theta$.

Figure 1.4 (b) demonstrates that applying a different phase shift to each adjacent element leaves only the desired direction unaffected, while other directions are attenuated. By subtracting the beam from the input, a notch is created, which can be used to filter out undesired spatial interference or blockers.

1.1.2 MIMO Transceivers

The previous chapter mainly discusses a simple multiple in, single out (MISO) transceiver case. Let x denote the real transmitted signal, and vector $\hat{y}$ denote the actual received signal by the antenna array. $\hat{H}$ is the channel matrix.

$$\begin{aligned} \hat{y} &= \hat{H}x \\ \text{where } \hat{H} &= \rho\omega' \\ &= \rho[1, e^{-j\Delta\phi}, e^{-2j\Delta\phi}, ..., e^{-j(N-1)\Delta\phi}]' \end{aligned} \tag{1.5}$$

ρ is the attenuation coefficient from the transmitter to the antenna array. In this simpli-

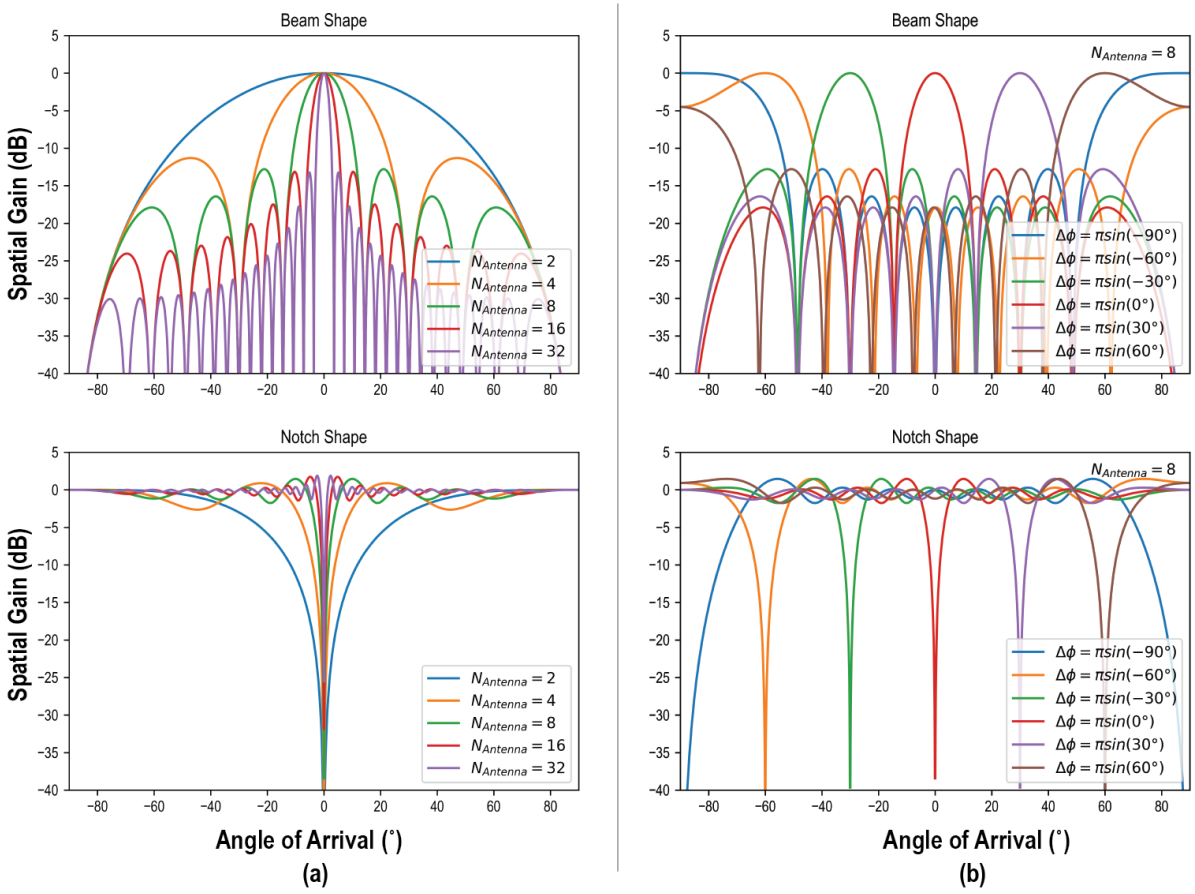


Figure 1.4: Conjugate beam shape with (a) different array size. (b) different phase delay applied to adjacent antenna elements.

fied case, ω is the delay vector, which only has one degree of freedom $\Delta\phi$, and assumes that $\Delta\phi$ is known as prior knowledge. The conjugate transpose of $\hat{H}$ can be calculated as $\hat{H}^*$. Then, we can estimate the original signal $\hat{x}$ from the received signal $\hat{y}$ and $\hat{H}^*$:

$$\hat{x} = \hat{H}^* \hat{y} \tag{1.6}$$

This method is commonly referred to as conjugate beamforming. Depending on the relative distance from the transmitter to the antenna array, an amplifier may be necessary for the datapath if the attenuation coefficient is also a vector $\rho = [\rho_1, \rho_2, ..., \rho_N]$. In this scenario, signals are combined in proportion to the root-mean-square (RMS) signal power, a technique known as maximum ratio combining (MRC), as it maximizes the signal-to-noise ratio (SNR). When the transmitter is far from the antenna array and the amplitude difference is negligible, MRC can be approximated as conjugate beamforming.

The antenna array's selectivity in the spatial domain enables the transmission of multiple beams simultaneously. The maximum number of distinguishable beams is limited by the number of antennas, denoted as N [18]. This concept is known as multiple-input, multiple-output (MIMO) on the receiver side. For a transmitted signal vector x and the received signal vector $\hat{y}$, the relationship can be expressed as follows:

$$\hat{y} = Hx + n \tag{1.7}$$

$$\begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_N \end{bmatrix} = \begin{bmatrix} h_{1,1} & h_{1,2} & \dots & h_{1,M} \\ h_{2,1} & h_{2,2} & \dots & h_{2,M} \\ \vdots & \vdots & \ddots & \vdots \\ h_{N,1} & h_{N,2} & \dots & h_{N,M} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_M \end{bmatrix} + \begin{bmatrix} n_1 \\ n_2 \\ \vdots \\ n_M \end{bmatrix} \tag{1.8}$$

Here, n represents the overall noise vector on the antenna array. In linear algebra, the maximum number of independent channels is given by $min(N, M)$.

When the number of antennas N is much greater than the number of users K, typically with $N/K > 10$, the system is called Massive MIMO. Employing a significantly large array size enables near-optimal beam tracking and steering, but it also introduces hardware and power overhead. Designing such a system presents additional challenges, including managing multiple elements and achieving interference resilience and energy efficiency.

1.1.3 Beamformer Topologies

Many researchers propose MIMO receivers with various placement architectures, as illustrated in Fig. 1.5. Typically, positioning beamformers or spatial filters early in the signal path can eliminate spatial blockers early, require fewer components, and help address design challenges such as linearity and dynamic range requirements for the analog baseband and data converters. However, designing the beamformer itself poses challenges, including limited spatial resolution, reduced gain, and increased power overhead. Conversely, placing the

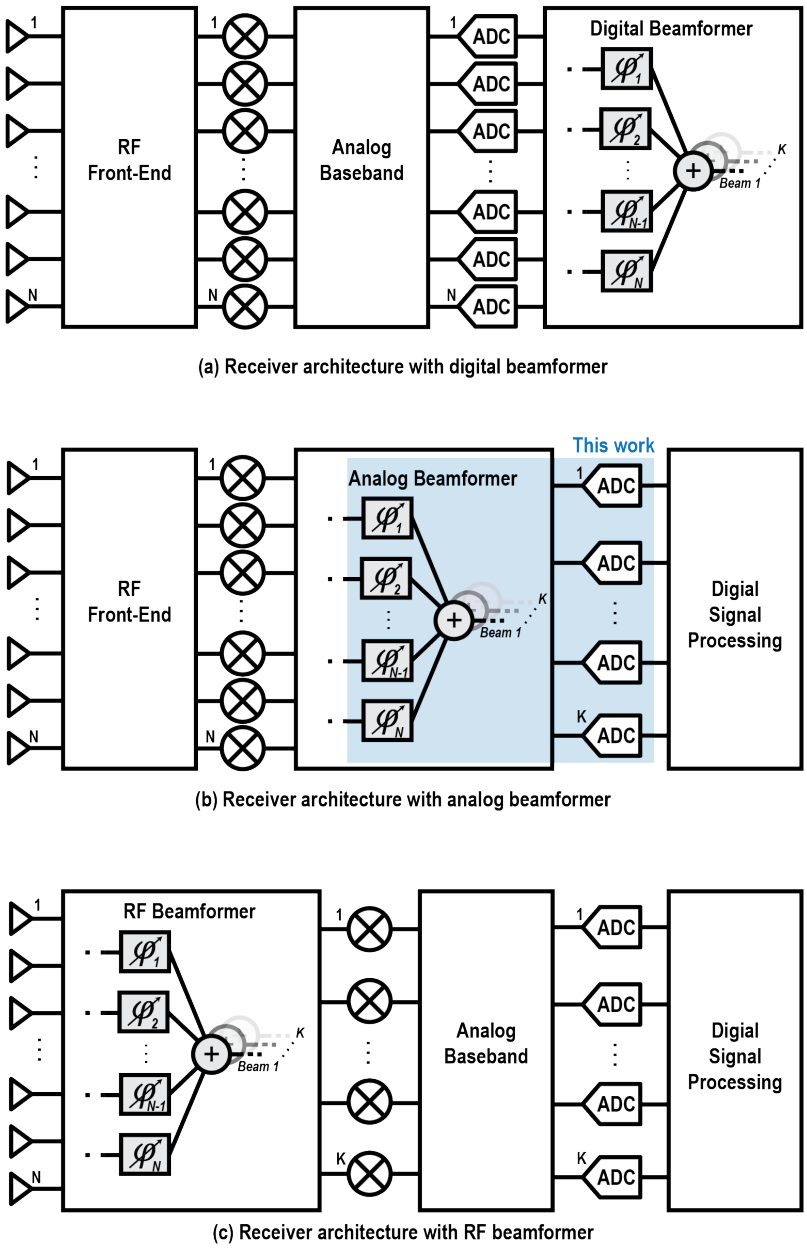


Figure 1.5: MIMO receiver architectures with different beamformer locations: (a) digital beamformer in the digital signal processor. (b) analog beamformer in baseband. (c) RF beamformer.

beamformer in later stages, such as digital signal processing (DSP), offers more flexibility. However, the entire RF and analog front-end must process all spatial information in this

approach.

Digital beamforming, as depicted in Fig. 1.5 (a), offers the highest achievable resolution and flexibility. Multiple stages and alignments, along with different algorithms including machine learning (ML)-based approaches, can be instantiated in digital signal processing (DSP) [19] [20] [21]. Fig. 1.6 illustrates an MRC beamformer array based on the systolic array, which is efficiently implemented in DSP. However, a limitation of implementing the entire beamforming process in DSP is that each signal path must carry all spatial contents and convert them into digital outputs. In a busy network where blockers are present, this would necessitate high dynamic range components, leading to heavy power consumption.

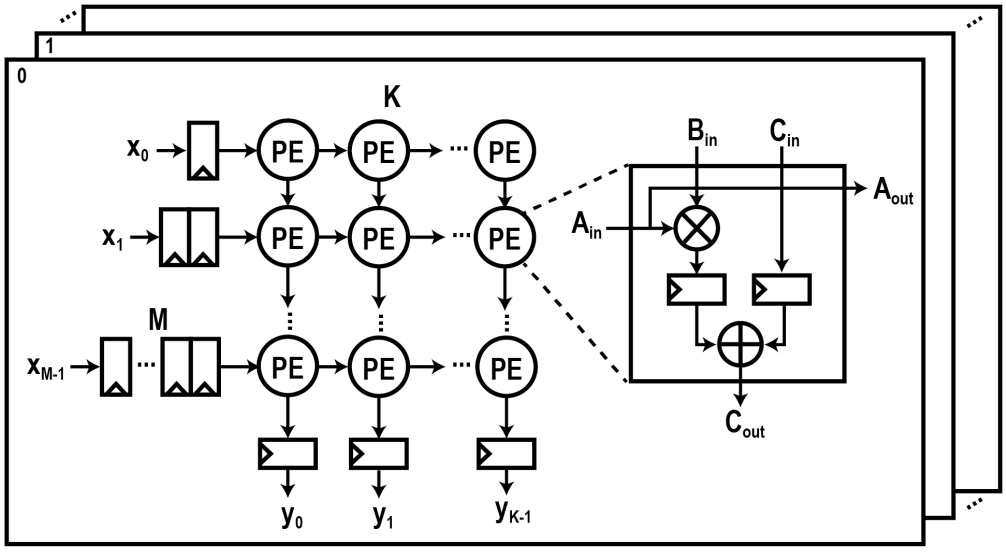


Figure 1.6: A systolic array-based MRC beamformer implemented in DSP [22].

To address this challenge, digital beamforming can be combined with spatial filtering in RF or baseband stages. This approach aims to eliminate the strongest blocker(s) in the earlier stages, but the information from other directions is still preserved and the dynamic range requirement is relaxed. Fig. 1.7 shows the diagram of digital beamforming with spatial notch filter (SNF) in analog baseband or RF domain. The SNF can be implemented as a phase-shifting matrix. For example, L. Zhang et al. designed a wideband current domain SNF in the analog baseband [23], which can achieve a flexible notch shape and deep notch depth. However, such method requires precise LO distribution[10], and typically consumes high energy, which limits the scalability of the MIMO system. Alternatively, we can design the SNF, which can detect the direction of the blocker and subtract it from each signal path. This method creates a single notch and is more energy efficient when the spatial

blockers are limited. For instance, M. Huang et al. proposed an autonomous SNF in the baseband to cancel blockers [24], and further employed cascading stages to cancel multiple spatial blockers [11][25]. However, these methods also lack scalability as the number of antennas increases rapidly. Additionally, each SNF stage can only create a single spatial notch. Multiple stages must be inserted in the signal path to cancel multiple blockers in a dynamic wireless environment, which reduces the overall signal amplitude and necessitates additional gain compensation.

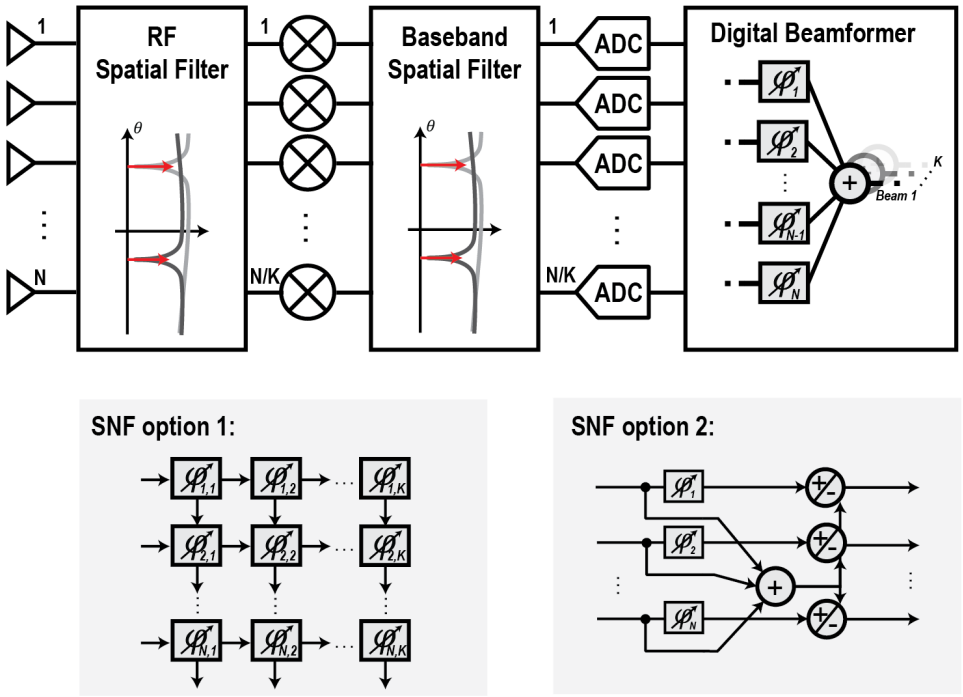


Figure 1.7: Digital beamforming with SNF before data converters.

Conversely, implementing beamforming or spatial filtering in the RF front-end, or even at the antenna level [26], leverages the entire signal chain to mitigate the effects of spatial blockers. As depicted in Fig. 1.5 (c), when the number of antennas N is much larger than the number of users K ($N \gg K$), the number of mixers and data converters can be significantly reduced, resulting in power savings and area reduction, as these components are typically high-performance blocks. Additionally, removing spatial blockers at an early stage relaxes the dynamic range requirements, preventing mixers and data converters from being saturated by large amplitude spatial interference. However, active beamformers, such

as those described in [27] and [28], usually require a high power budget and precise LO distribution. On the other hand, ultra-wideband passive beamformers suffer from high gain loss in the RF frequency domain [29].

The baseband beamformer, illustrated in Fig. 1.5 (b), represents a compromise solution compared to the other two options. It reduces the number of data converters in the signal chain, which can be a significant contributor to the power consumption of the receiver [10]. Besides, with limited spatial resolution, an analog beamformer can be more energy-efficient. For instance, M. Soer et al. implemented a passive constant G_m vector modulator in the baseband [30], which has constant input impedance and output resistance, and thus leverages the calibration. L. Zhang et al. implemented a spatial filter together with a spectrum filter in a mixer-first front-end [31], which demonstrates high in-band OIP3. B. Lin et al. designed a multi-stage spatial filter for a 2D antenna array [32]. L. Zhang et al. proposed a gyrator-based scalable spatial notch filter [33]. Various design choices are available for the baseband beamformer; however, most of them require additional circuit in the signal path, necessitating gain compensation and increased silicon area. In this work, we propose an efficient charge-domain baseband beamforming method. The proposed method utilizes existing circuitry, integrates the phase shifter and beamformer into the data converter, and does not require significant gain compensation.

1.2 Data Converters

At high carrier frequencies, massive MIMO transceivers can access increased bandwidth, which requires medium-to-high resolution and high-speed ADCs. The state-of-the-art ADC usually employs pipelined or time-interleaved (TI) architecture to meet these demands. However, these ADCs can become significant power consumers in the receiver [10], and further limit the system performance.

1.2.1 ADC Figure of Merit

Benefiting from technology advance and innovative topologies, the performance of data converters has been continually improving. Fig. 1.8 illustrates the figure of merit (FOM) in the top conferences over the past few decades [34].

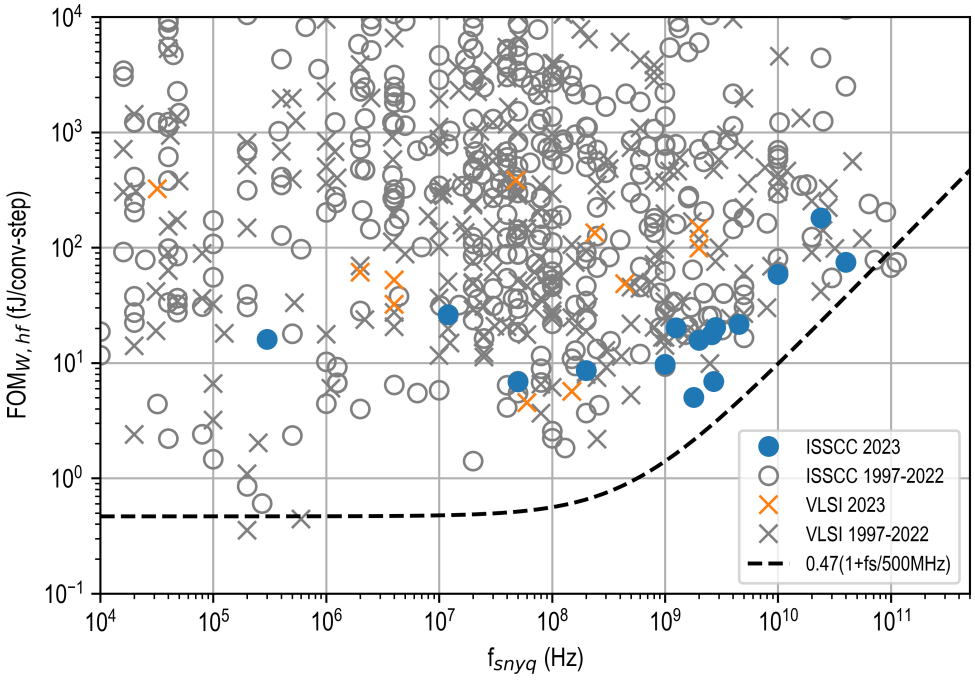


Figure 1.8: ADC figure of merit survey. Data from [34].

Walden's FOM (FOM$_W$) is defined by three parameters: ADC power consumption (P), sampling frequency (f_S), and number of bits (B). It indicates that doubling the bandwidth is as challenging as adding an extra bit. Walden's FOM provides accurate approximations when $f_S < 500$ MHz and $B \leq 12$.

$$\text{FOM}_W = \frac{P}{f_S \cdot 2^B} \ \big(fJ/\text{conv-step}\big) \tag{1.9}$$

In the high dynamic range region ($B > 12$ or $\text{DR} > 74dB$), Schreier's FOM (FOM_S) is more commonly used, as noise and distortion are taken into account:

$$\text{FOM}_S = \text{SNDR} + 10\log_{10}\frac{\text{BW}}{P} \ \big(dB\big) \tag{1.10}$$

where SNDR is the signal to noise and distortion ratio, and BW is the bandwidth of the ADC.

Note that in Fig. 1.8, when the sampling frequency is high, it is challenging to follow the ideal FOM_W, typically because of non-idealities such as timing, parasitic, and limited bandwidth. The envelope is approximated by:

$$\begin{aligned} \text{FOM}_{W,env} &= A_0\big(1 + \frac{f_S}{f_0}\big) \\ \text{where } f_0 &\approx 500\text{MHz} \\ A_0 &= \text{avg}\big(\min_3(\frac{P_i}{f_{S,i} \cdot 2_i^B})\big) \end{aligned} \tag{1.11}$$

1.2.2 Trends in ADC Architecture

Fig. 1.9 illustrates the published trend in ADC architectures in recent years, revealing several notable observations. SAR ADCs are gaining popularity for several reasons. Firstly, as a mixed-signal component, the digital control logic scales nicely with technological advancements, making SAR ADCs more area-efficient and energy-efficient. Additionally, the increased number of metal layers allows for greater metal-oxide-metal (MOM) capacitance in a given area. Moreover, SAR ADCs are more straightforward to design compared to other architectures when operating under the exact performance specifications and constraints. In contrast, scaling switched capacitor poses challenges in deep-micrometer technology due to transistor leakage degradation, which is undesirable for pipeline or sigma-delta switched capacitor ADCs. Architectures that rely on high-gain amplifiers also do not benefit significantly from advancements in technology, as the intrinsic gain of transistors is decreasing.

1.2.3 SAR-ADC-Assisted Spectral Filtering

When prior knowledge of the analog input exists, researchers have explored integrating signal processing functions into data converters. In such cases, data converters not only translate data from analog to digital but also aid in information processing, leading to the term analog-to-information converters (AICs). For example, J. Kang et al. proposed a SAR ADC with an embedded FIR filter [35]. In this design, illustrated in Fig. 1.10 (a), the capacitor array can

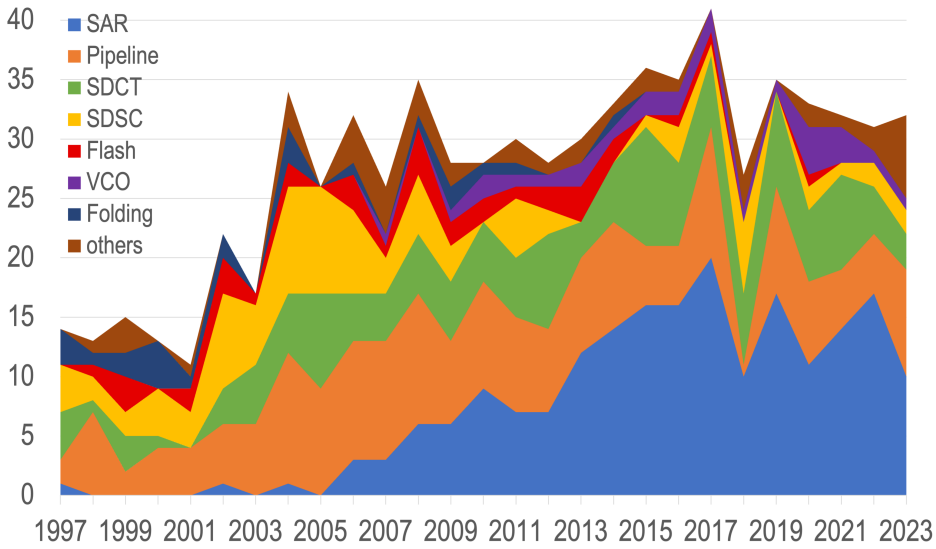


Figure 1.9: ADC architecture survey. Data from [34]

be reconfigured during the sampling stage. The M-order filter impulse response performs during the sampling phase, which is divided into multiple SAR clock cycles.

$$y[n] = b_0 \cdot x[n] + b_1 \cdot x[n-1] + ... + b_M \cdot x[n-M] \tag{1.12}$$

In each cycle i ($1 \leq i \leq M$) of the sampling phase, the weight b_i is represented by the amount of the capacitor connected to the sampler, and the input information is stored as charge on the capacitor plate. Since each capacitor is used only once in the sampling phase, the sampling power doesn't increase significantly. At the end of the last sampling cycle M, all capacitors are connected together for charge redistribution, and then the N-cycle SAR bit test begins.

By adjusting the number of taps and the capacitor ratio, it's possible to realize FIR filters of different orders and frequency responses, which can filter out-of-band noise and interference. The key advantage of this approach is its area and power efficiency, as it utilizes existing components, and the overall energy in a complete cycle remains the same. However, this approach involves a trade-off between information and data rate, as each digital output requires $M + N$ cycles instead of N cycles.

Building on this concept, D. Lin et al. proposed an FIR and IIR filtering SAR ADC [36], depicted in Fig. 1.10 (b). Here, the infinite impulse response (IIR) is achieved by periodically sharing charge with a capacitor that retains all historical inputs, allowing for additional attenuation of out-of-band signals. However, a drawback of this method is that not every

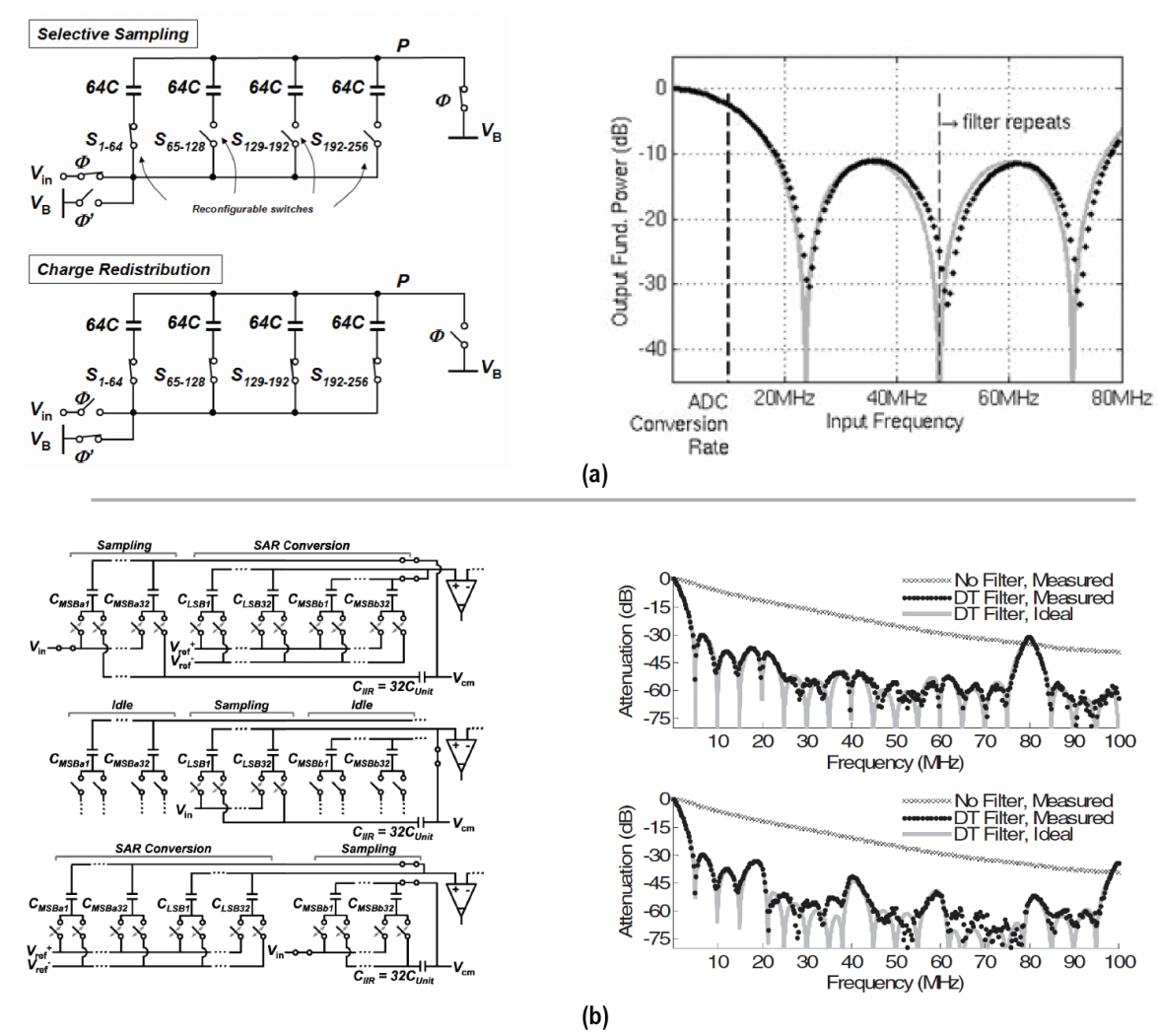


Figure 1.10: (a) SAR ADC with integrated FIR filter [35]. (b) SAR ADC with integrated FIR/IIR filter [36].

capacitor is effective during the selective sampling phase. To meet noise specifications, the minimum total capacitor area must be multiplied according to the available FIR/IIR stages. A. Whitecombe also adapted the integrated FIR in the design of multi-channel RF-digital receiver [37].

1.3 Analog Design Automation

Since the invention of the first integrated circuits, design complexity has grown exponentially. Digital circuits have followed Moore's Law since the early 1960s until recently. The exponentially increased computational power of systems benefits not only from technological advancements but also from the development of computer-aided design (CAD) tools. These tools have greatly improved the productivity of digital circuit engineers.

In contrast, analog circuit design is highly customized and often requires manual layout. Non-recurring engineering (NRE) costs are challenging to reduce when transferring to a new technology node. The availability of CAD tools for analog design is limited. Analog design typically relies on experience and intuition, which are difficult to standardize.

Many researchers have attempted to address the challenges of analog circuit design automation. For example, in [38], transistor sizing in operational amplifiers (op-amps) is transformed into a geometric optimization problem. Using global optimization methods can lead to optimal amplifier designs based on given specifications [1]. In [39], numerical optimization is employed to adjust device parameters using schematic simulation results, bridging the gap between approximated design equations and actual circuit models. Additionally, [40] utilizes estimated layout parasitics provided by an automated place-and-route tool for the optimization problem. Efforts have also been made in the industry to automate analog design, as seen in [41] [42]. However, many analog designers hesitate to adopt these tools, often citing "aesthetic" issues with the results produced by such automation [43].

1.3.1 Berkeley Analog Generator

The BAG framework, pioneered by Crossley *et al.* [44], improves analog and mixed-signal IC design by treating circuit design as the creation of executable circuit generators. Rather than manually designing specific circuit blocks, designers encapsulate methodologies in these generators to automatically generate circuit schematics, layouts, and simulation setups based on given specifications. This approach significantly reduces the iteration time for designing and optimizing analog circuits, leading to cost savings in R&D. Designers can easily reproduce circuits with similar specifications or port layouts to different technology nodes using these generators. The BAG framework is primarily used for designing analog and mixed-signal integrated circuits (ICs).

Here's a general overview of how BAG is used:

1. Specification: Define the circuit specifications, such as gain, bandwidth, and power consumption.

2. Circuit Generator: Use the BAG framework to create a circuit generator that automatically produces the desired circuit based on the specifications. This involves defining the circuit topology, parameters, and constraints.

[1] when constrains are posynomial

3. Generation: Use the circuit generator to automatically generate the circuit schematic and layout based on the specifications.

4. Simulation and Verification: Simulate the generated circuit to verify its performance against the specifications using the tools provided by BAG.

5. Iteration: If the circuit does not meet the specifications, iterate on the generator or the specifications until the desired performance is achieved.

6. Porting: Once the design is finalized, easily port the layout to similar technology nodes using BAG's capabilities.

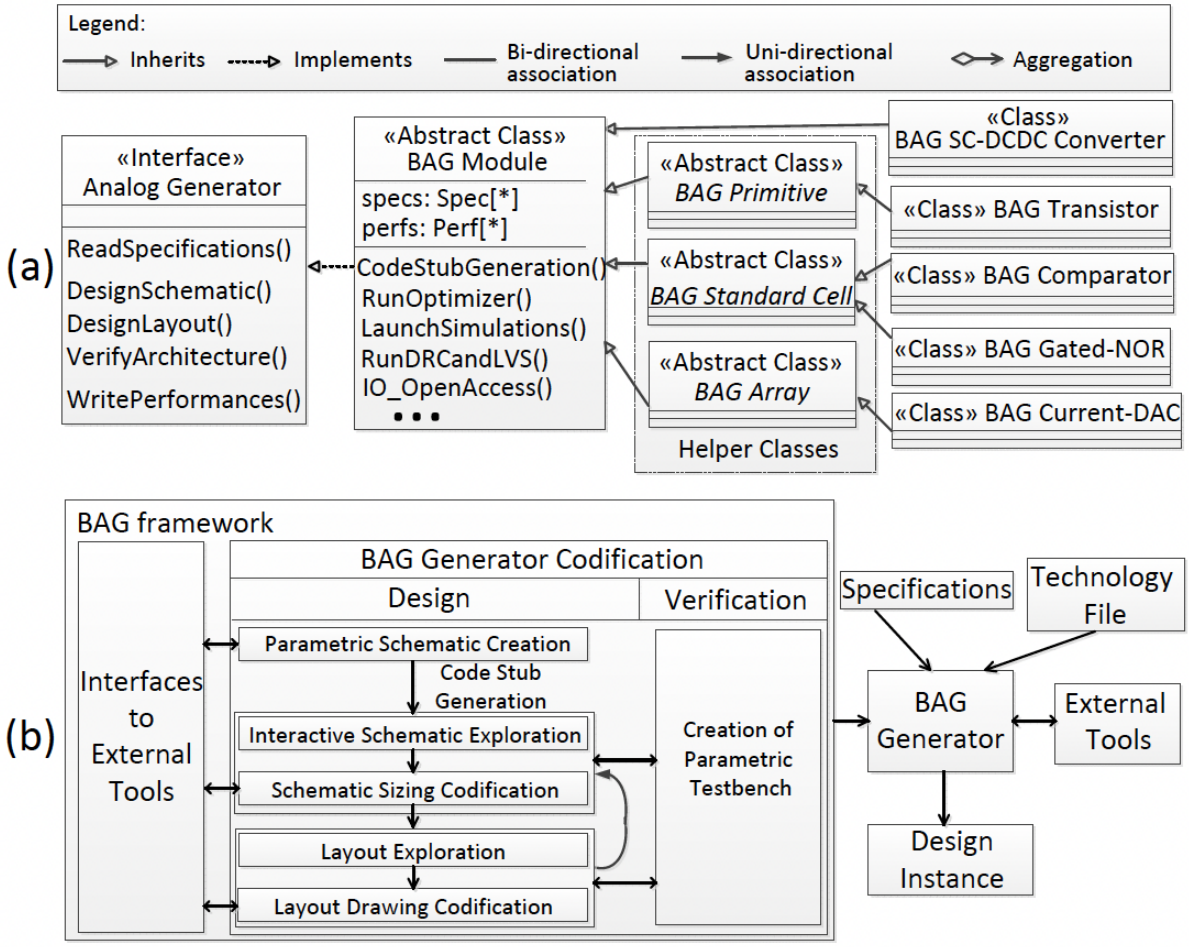


Figure 1.11: (a) Generator interface with BAG classes. (b) BAG design flow [44].

BAG simplifies the analog circuit design process by automating many repetitive tasks, allowing designers to focus more on the creative aspects of circuit design.

The BAG framework has seen important development over the past decade since its initial introduction. BAG2, released in 2018 [43], introduced a universal AMS verification framework and two new layout generation engines: XBase and Laygo. XBase offers a wide range of Python classes and functions for designing analog/mixed-signal circuits using parameterized primitives, while Laygo is an alternative engine that relies on manually designed layout primitives for compact customized circuits.

Subsequently, BAG 3.0 was developed by Blue Cheetah Analog Design (BCA). One significant enhancement in BAG 3.0 was the migration of the back-end from Python to C++, aimed at accelerating layout manipulation and netlisting calls [45]. Currently, the latest version of BAG, known as BAG 3++, is still in active development as of 2023 [46] by Berkeley Wireless Research Center (BWRC).

The majority of the circuit design discussed in this work is based on the BAG2 Laygo space and BAG 3.0, leveraging their capabilities and advancements in analog and mixed-signal IC design automation.

Chapter 2

Charge-Domain Beamforming

In this chapter, we introduce a charge domain beamforming method driven by the computational capabilities of data converters, addressing the growing need for enhanced network capacity in densely populated directional communication environments. Figure 2.1 illustrates that our approach involves an N-antenna front-end receiver with antennas spaced at intervals of half the wavelength, $\lambda/2$. An $N \times N$ baseband beamformer precedes the ADC in the receiver chain.

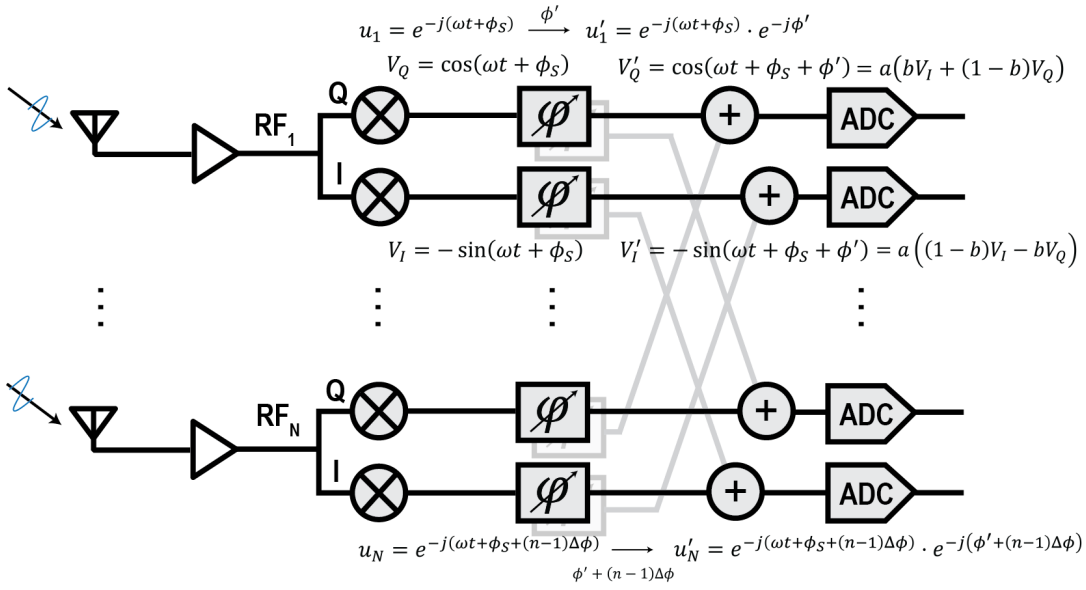


Figure 2.1: Diagram of a baseband beamformer.

For each beamformer, an incoming signal at angle θ exhibits a phase difference of $\Delta\phi = \pi \cdot \sin(\theta)$ between adjacent antenna elements, as per Equation 1.4. The phase shift applied to each channel is adjustable from 0 to 2π, depending on the desired angle of arrival. This adjustment allows the input signal at the ADC to be focused on a specific direction or to provide significant attenuation to undesired directions, effectively suppressing spatial blockers and relaxing the ADC specifications. Fig. 2.2 shows an intuitive example. Assume the directions of a blocker and the desired signal are known, and the blocker's amplitude is 10× larger than the signal. If the phase adjustment between each channel is set to $\pi \sin 45°$, the desired input signal swing remains the same, while the blocker is attenuated by 13.7×.

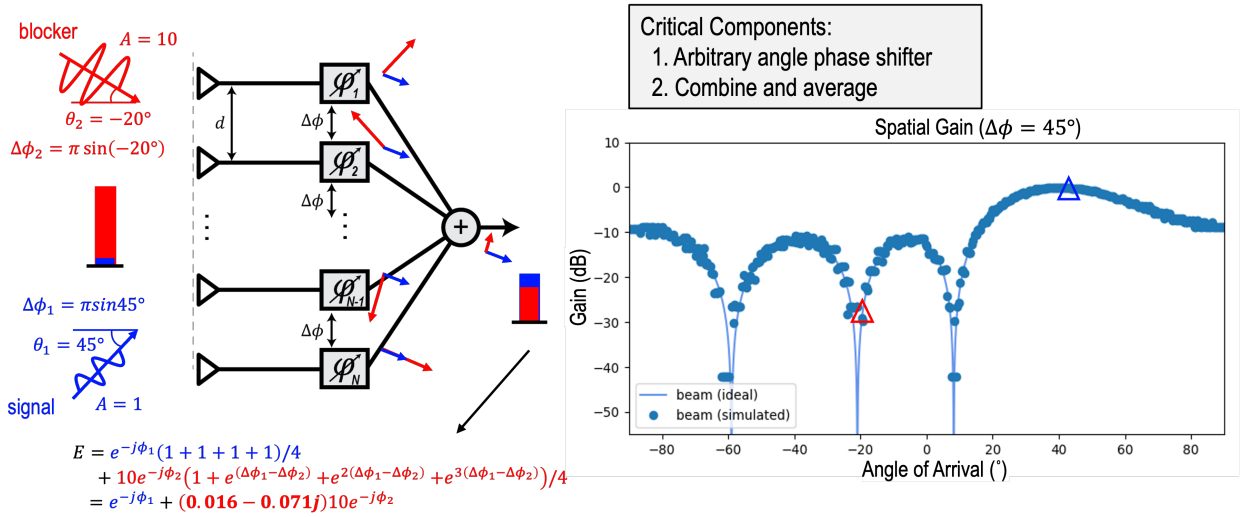


Figure 2.2: Example of spatial blocker attenuation.

To implement this functionality, two critical components are required: a wide-range phase shifter for precise phase adjustments of each channel, and a signal combiner to average all shifted signals to form a beam.

2.1 Charge Domain Phase Shifter

In this section, we begin by examining the phase shifter solution. In Figure 2.1, the desired phase-shifted I/Q signal can be expressed as a linear combination of the original I/Q signals. It's important to note that the coefficients for $V_I^{'}$ and $V_Q^{'}$ are symmetric. By applying sum and difference formulas to isolate the $\phi^{'}$ term, the coefficients are defined as:

$$
\begin{aligned}
V_I^{'} &= a\big((1-b)V_I - bV_Q\big) \\
V_Q^{'} &= a\big(bV_I + (1-b)V_Q\big) \\
\text{where } a &= \sin(\phi^{'}) + \cos(\phi^{'}) \\
b &= \frac{\sin(\phi^{'})}{a}
\end{aligned}
\tag{2.1}
$$

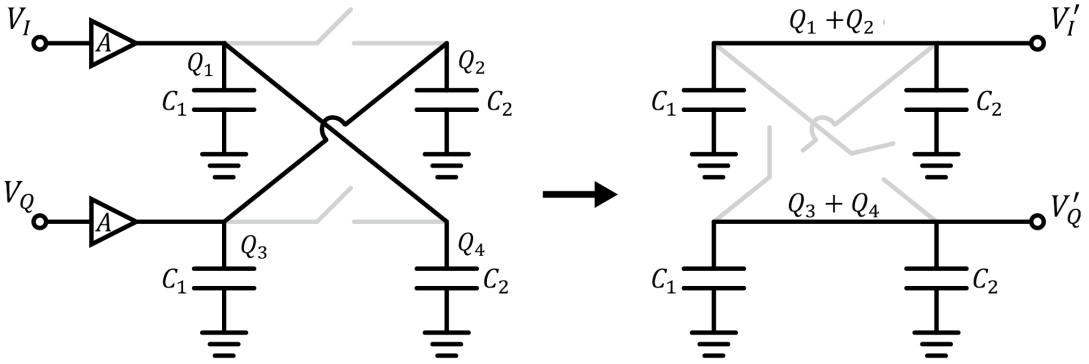


Figure 2.3: Sampler circuit which uses two capacitors.

This functionality can be realized by using two variable capacitors. Assume the capacitance ratio of these capacitors can be arbitrarily set and only limited by matching. As illustrated in Figure 2.3, during the sampling phase, the top-left and bottom-right capacitors sample from the I channel, while the bottom-left and top-right capacitors sample from the Q channel. After the sampling phase, the top and bottom capacitors are disconnected from the source, but the charge remains on the top plate. Subsequently, the top and bottom capacitors are grouped, and charge sharing occurs at their sampling plates. The output voltage is then calculated as:

$$
\begin{aligned}
V_I^{'} &= A\big(\frac{C_1}{C_1+C_2}V_I + \frac{C_2}{C_1+C_2}V_Q\big) \\
V_Q^{'} &= A\big(\frac{C_2}{C_1+C_2}V_I + \frac{C_1}{C_1+C_2}V_Q\big)
\end{aligned}
\tag{2.2}
$$

Comparing Eq. 2.1 and 2.2, we can select the values of C_1 and C_2 such that $b = C_2/(C_1+C_2)$. It's important to note that b and $1-b$ can be negative. The negative sign for

each possible term can be achieved by reversing the sampling plate of a specific capacitor C_{1-4}. Furthermore, based on the desired phase shift $\phi^{'}$, the compensation gain A should be set as:

$$\begin{aligned} A &= |\sin(\phi^{'}) + \cos(\phi^{'})| \in [1, \sqrt{2}] \\ \frac{C_2}{C_1} &= \tan(\phi^{'}) \in [0, +\infty) \end{aligned} \tag{2.3}$$

2.1.1 Integration with SAR ADC

We propose an elegant method to implement the required capacitors. The two capacitors, C_1 and C_2, with re-configurable features, can be integrated with the binary-encoded capacitor DAC in a SAR ADC. Based on the desired phase $\phi^{'}$, the ratio of C_1 to C_2 can be calculated, and the capacitor DAC is divided into two groups to sample from different sources in the sampling phase. At the end of the sampling phase, the capacitor DAC is regrouped for charge averaging and the subsequent bit trial. This approach allows for very precise phase shifting, as the coefficient resolution is determined by the DAC's available bits.

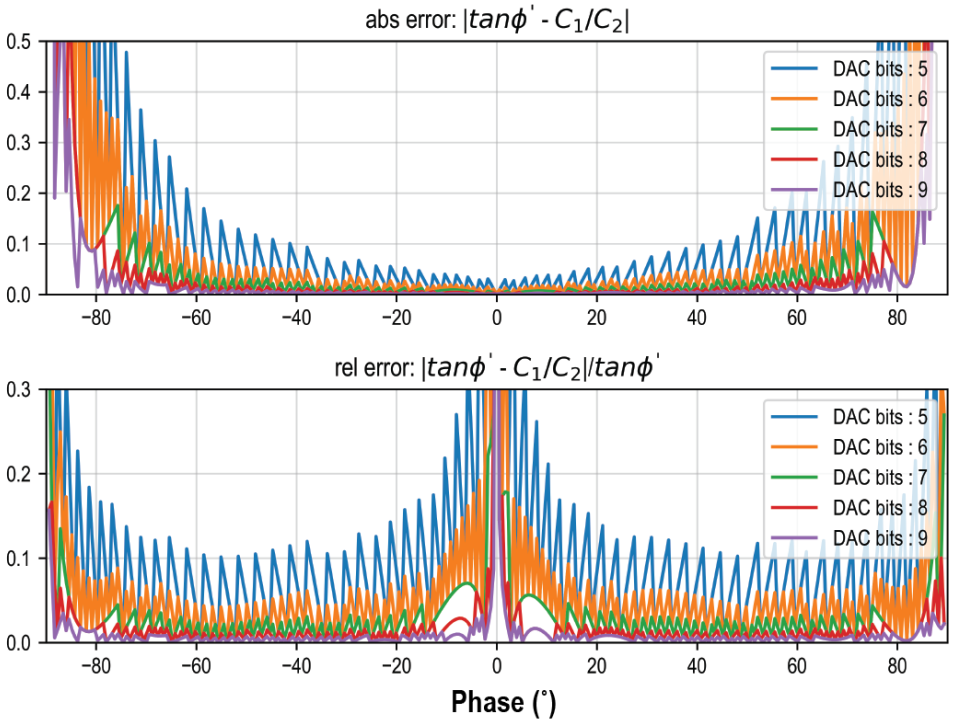


Figure 2.4: Capacitor DAC bits versus the absolute and relative phase error.

Fig. 2.4 shows the relationship between the available bits for C_2/C_1 and the error from $\tan(\phi')$. With a 7-bit capacitor DAC, the relative error of $|C_1/C_2|$ from $|\tan\phi'|$ is within 5% for over 96% of the phase space. The non-ideal match only occurs near 0° and ±90°.

Using the capacitor DAC as a phase shifter offers several advantages. First, it does not introduce new components into the signal path, thus avoiding adding noise and requiring additional gain stages. Second, it does not affect the ADC throughput, as it only modifies the sampling phase. Charge sharing occurs at the end of the sampling phase, which coincides with the start of the SAR ADC's most significant bit (MSB) trial. The primary constraint is that the voltage should settle correctly for the MSB test within the first ADC clock period. Additionally, this method can achieve high precision. Fig. 2.5 shows the diagram of the phase shifter integrated into two SAR ADCs.

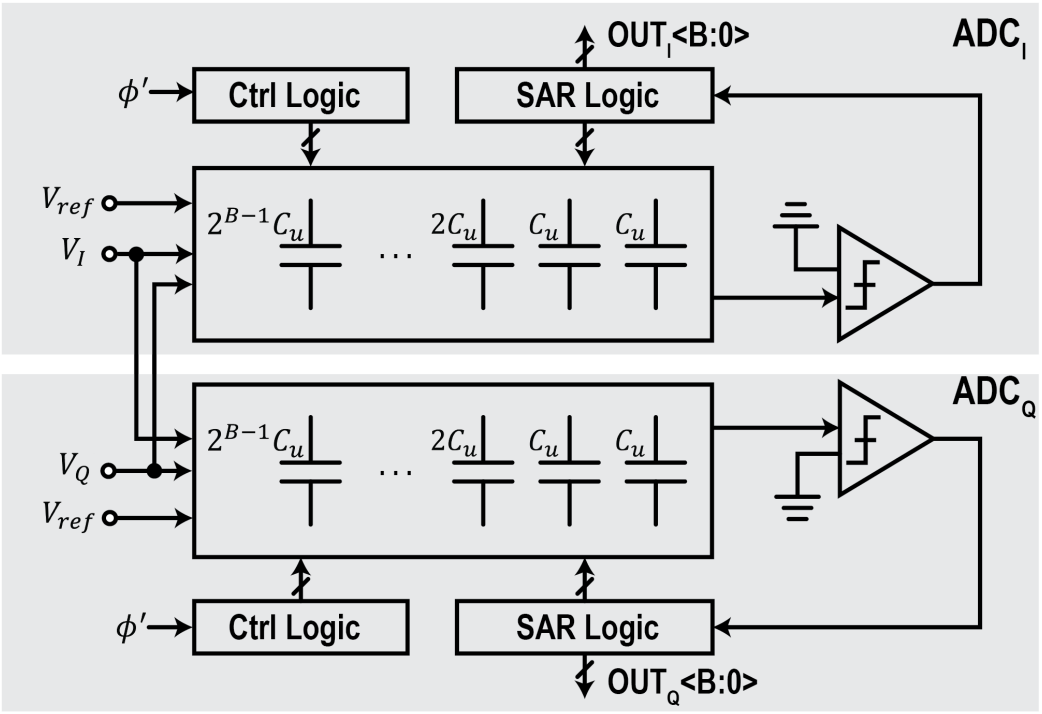


Figure 2.5: Diagram of SAR ADC with integrated phase shifter.

2.1.2 Phase Constellation and Gain Compensation

The resulting constellation map with the capacitor DAC implementation is shown in Fig. 2.6. The achievable phase space forms a square that is rotated by 45 degrees. Two different

operation modes are possible to create a circular constellation trace. Fig. 2.6 (a) shows the maximum circle within the phase space, indicating that not all capacitors are used in the sampling phase to achieve an overall unity gain. Shifting by 0°, 90°, 180°, and 270° will result in a maximum gain drop of $1/\sqrt{2}$ (3dB). In (b), all capacitors are always used for sampling; however, a variable-gain amplifier (VGA) is needed to provide phase-dependent gain from 1 to 3dB to ensure that different channels have the same signal amplitude. Noise from VGA is also introduced in this case.

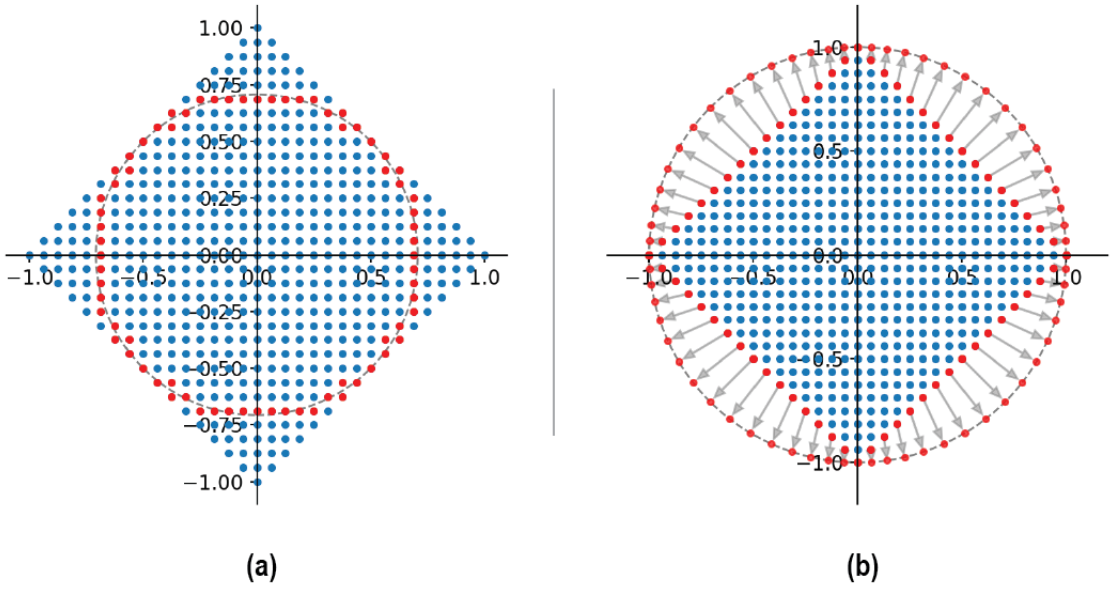


Figure 2.6: A 4-bit constellation map with two modes. (a) The capacitor value is selected for maximum unified gain. (b) All capacitors are always used. External gain compensation is required to align gain among different channels.

2.2 Charge Domain Beamformer

2.2.1 Multi-Channel Combination

The phase shifts for each channel are solely determined by the desired angle of arrival: $\Delta\phi_{1..N} \leftarrow f(\theta)$. After adjusting the phase of each channel, the next step involves summing and averaging the signals to create a beam and attenuate signals from undesired directions:

$$
\begin{aligned}
V_{I,beam} &= \frac{1}{N}(V_{I,1}^{'} + V_{I,2}^{'} + ... + V_{I,N}^{'}) \\
V_{Q,beam} &= \frac{1}{N}(V_{Q,1}^{'} + V_{Q,2}^{'} + ... + V_{Q,N}^{'}),
\end{aligned}
\tag{2.4}
$$

The signal-averaging step is also straightforward in the charge domain. It's worth noting that the charge averaging among channels can occur immediately after the end of the sampling phase, which coincides with the time when local averaging on C_1 and C_2 takes place. As illustrated in Fig. 2.7, all capacitors in the I and Q channels are connected when sampling is completed. Now, the total capacitor for a SAR ADC is $N \cdot (C_1 + C_2)$. Each ADC can output a single beam with $N - 1$ spatial notches. Multiple SAR ADCs with capacitor DACs for each channel should be instantiated to form multiple beams.

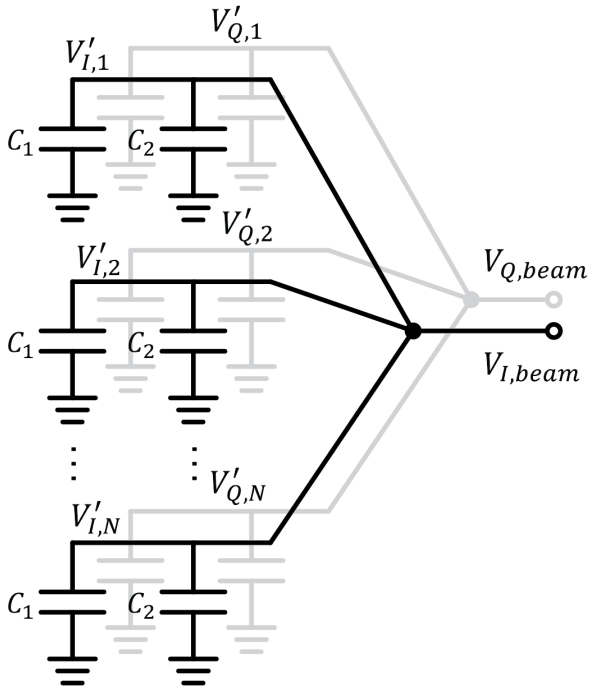


Figure 2.7: Charge domain sum and average to form a beam.

2.2.2 Beamformer Integrated with SAR ADC

Fig. 2.8 shows the diagram where a multi-channel capacitor DAC is integrated inside two SAR ADCs. The total capacitance in the SAR ADC is mainly determined by noise and

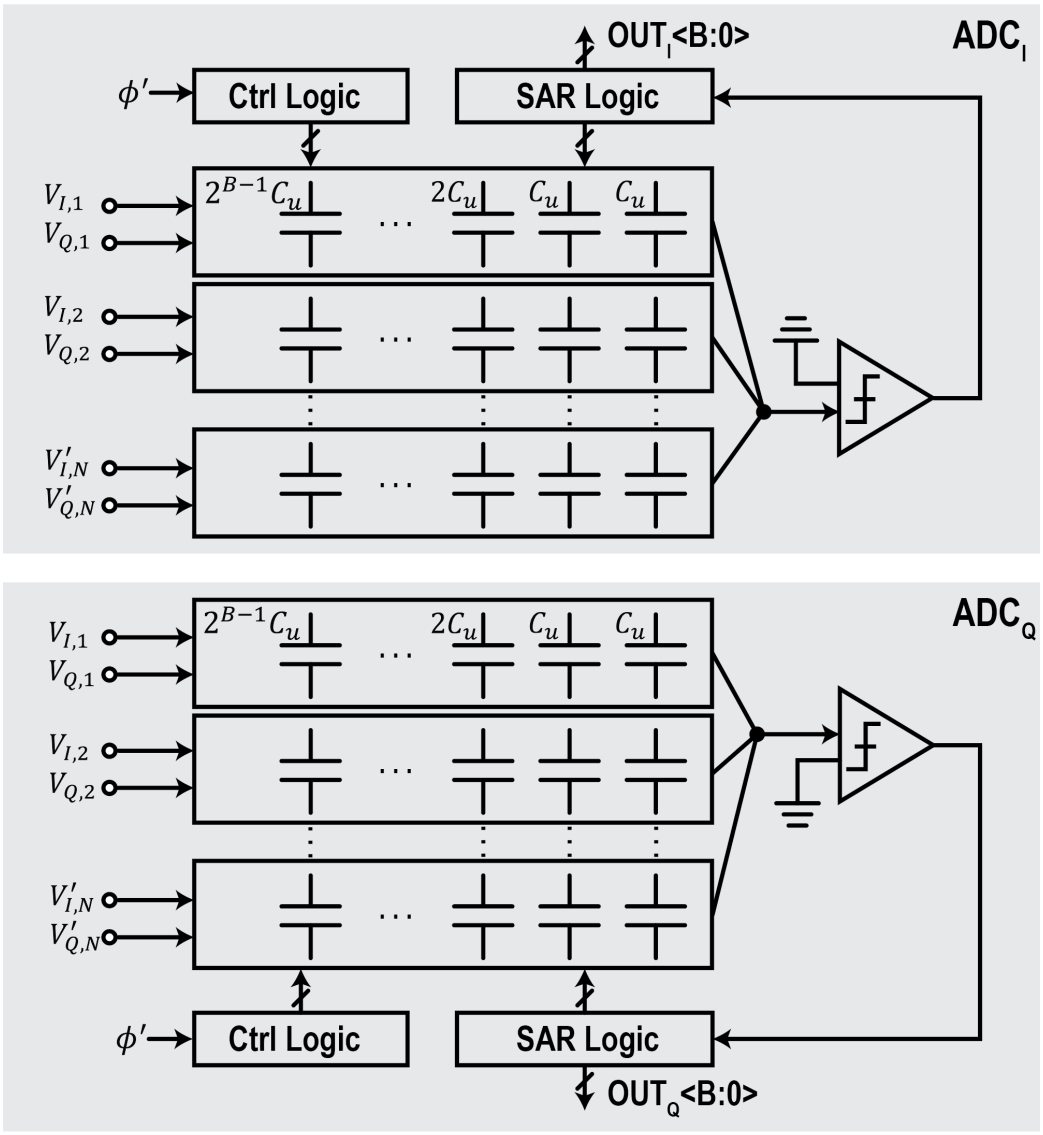


Figure 2.8: Diagram of SAR ADC with integrated beamformer.

mismatch requirements, while the mismatch can be calibrated. Assume the input swing is V_{sw}. The integrated thermal noise should be at least less than half of the voltage step:

Table 2.1: SAR ADC resolution versus minimum total and unit capacitance limited by the integrated thermal noise, when voltage swing is 1V.

SAR ADC resolution B	C_{tot}	C_{unit}
6	0.067fF	1.05aF
7	0.271fF	2.12aF
8	1.08fF	4.21aF
9	4.34fF	8.48aF
10	17.4fF	17.0aF
11	69.5fF	33.9aF
12	277fF	67.6aF
13	1.11pF	135aF
14	4.44pF	271aF

$$\begin{aligned} \sqrt{\frac{k_B T}{C_{tot}}} &\leq \frac{1}{2} \cdot \frac{V_{sw}}{2^B} \\ C_{tot} &\geq k_B T \cdot \left(\frac{2 \cdot 2^B}{V_{sw}}\right)^2 \\ C_{unit} &= \frac{1}{2^B} C_{tot} \end{aligned} \tag{2.5}$$

Table 2.1 indicates that for SAR ADC resolutions ranging from low to moderate, ideally, the minimum overall capacitance required is relatively low and does not pose a bottleneck for the design. The major limitation lies in the mismatch requirement of the unit capacitor. When further division of the unit capacitor is not feasible, duplicating the capacitor bank to meet this requirement would introduce additional area overhead. However, the total capacitor area remains relatively small due to fewer bits, making it an acceptable trade-off. In this work, we identify that the primary constraint is from the capacitor DAC routing parasitic, so we choose the C_{unit} accordingly. The following chapters will introduce more details about the design.

Chapter 3

SAR ADC with Integrated Phase Shifter

In Chapter 2.1, we propose to use the capacitor array in SAR ADC for the arbitrary phase shifter. This chapter provides design details, simulation results, and a taped-out prototype of the SAR ADC pair with an integrated phase shifter.

3.1 Switched-Capacitor based Phase Shifter

A SAR ADC with a monotonic switching scheme is preferred, as this topology can significantly reduce switching energy and circuit area [47]. Consider a typical capacitor unit used in a differential SAR capacitor array, as illustrated in Fig. 3.1. One side of the capacitor plate is connected to the sampler output node and other capacitor units, and it is always tied to the comparator input. The other plate is grounded during the sampling phase and then decided by the SAR control logic based on the comparison result during bit testing. We will use this typical capacitor unit as a starting point.

3.1.1 Capacitor Unit Extension

From Eq. 2.1 2.2, to implement the phase shifting function, each capacitor unit must have the following features:

1. Channel I/Q selection for processing, meaning each binary capacitor should sample from either the I channel or the Q channel, based on the absolute value of the coefficient.

2. Sampling plate selectivity. According to the coefficient sign, each binary capacitor unit can sample from either the top plate or the bottom plate because all the top plates will be connected back together as a conventional SAR ADC.

The required functions can be enabled by adding a few switches between the sampler and both of the capacitor plates. Fig. 3.2 shows a capacitor and its controls in an I-channel

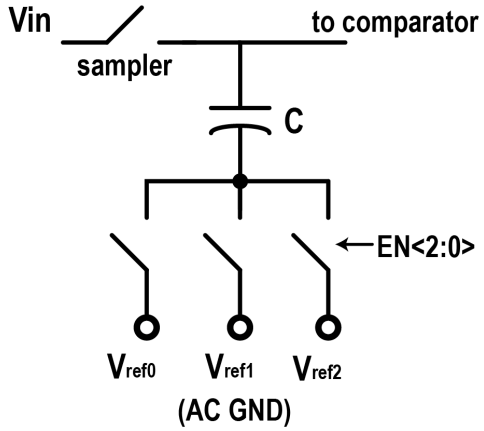


Figure 3.1: A capacitor unit in differential capacitor array of SAR ADC.

ADC. S_3, S_4 provide access to the bottom plate, which allows sampling reversely when S_7 is on and S_5, S_6 are off. S_5 will always be on when the sampling phase ends. During the SAR bit decision phases, switches S_3, S_4, S_6, and S_7 should all remain off. The control logic for switches S_{0-7} during the sampling phase is summarized in Table 3.1.

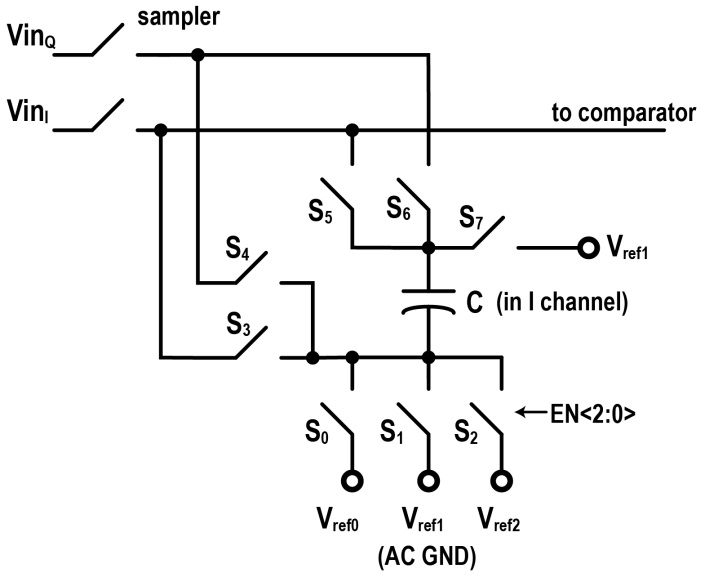


Figure 3.2: A capacitor unit with extended functionality.

Table 3.1: Switch logic in the sampling phase.

Sample from	Sample Plate	Switch on	Switch off
Same channel	top	S_1, S_5	$S_0, S_2, S_3, S_4, S_6, S_7$
	bottom	S_3, S_7	$S_0, S_1, S_2, S_4, S_5, S_6$
The other channel	top	S_1, S_6	$S_0, S_2, S_3, S_4, S_5, S_7$
	bottom	S_4, S_7	$S_0, S_1, S_2, S_3, S_5, S_6$

The added switches are implemented by NMOS transistors and placed close to the capacitors they control. Metal-oxide-metal (MOM) capacitors are preferred due to their superior symmetry, matching characteristics, and density [47][48][49]. Fig. 3.3 illustrates the top view of a multi-layer sandwich capacitor, with the gray metal representing the top plate. Enclosing the top plate with the bottom plate helps reduce the effects of parasitic capacitance. The compact layout of the unit capacitor simplifies cascading in the y axis. Cascading in the z axis, by utilizing multiple metal layers, increases the capacitance of the unit capacitor C_{unit} and reduces the ratio of parasitic capacitance. The dimension along the x axis can also be used to set the unit capacitance, taking into account power and noise specifications. However, a major constraint is the available area, as the capacitor array occupies a significant portion of the SAR ADC area.

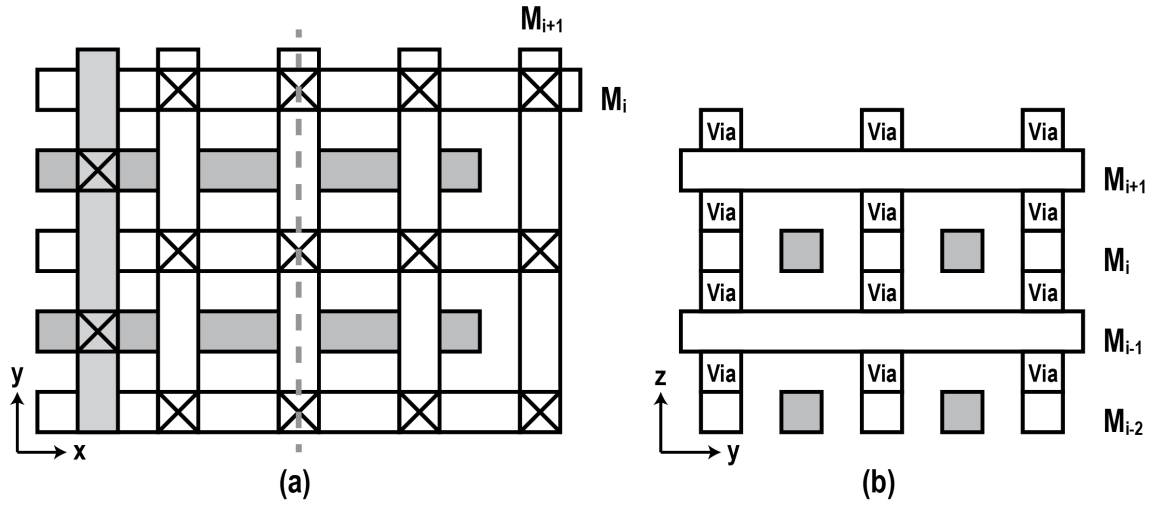


Figure 3.3: Compact and cascadeable MOM capacitor diagram. (a) Top view. (b) Cross section.

3.1.2 Switch Timing

Switch timing is crucial for ensuring the correctness of the computation, as the insertion of new switches in the signal path and changes in the connection to the comparator can lead to undesired charge leakage. Incorrect timing or switching order can result in voltage level mismatch, gain loss, or comparison failure.

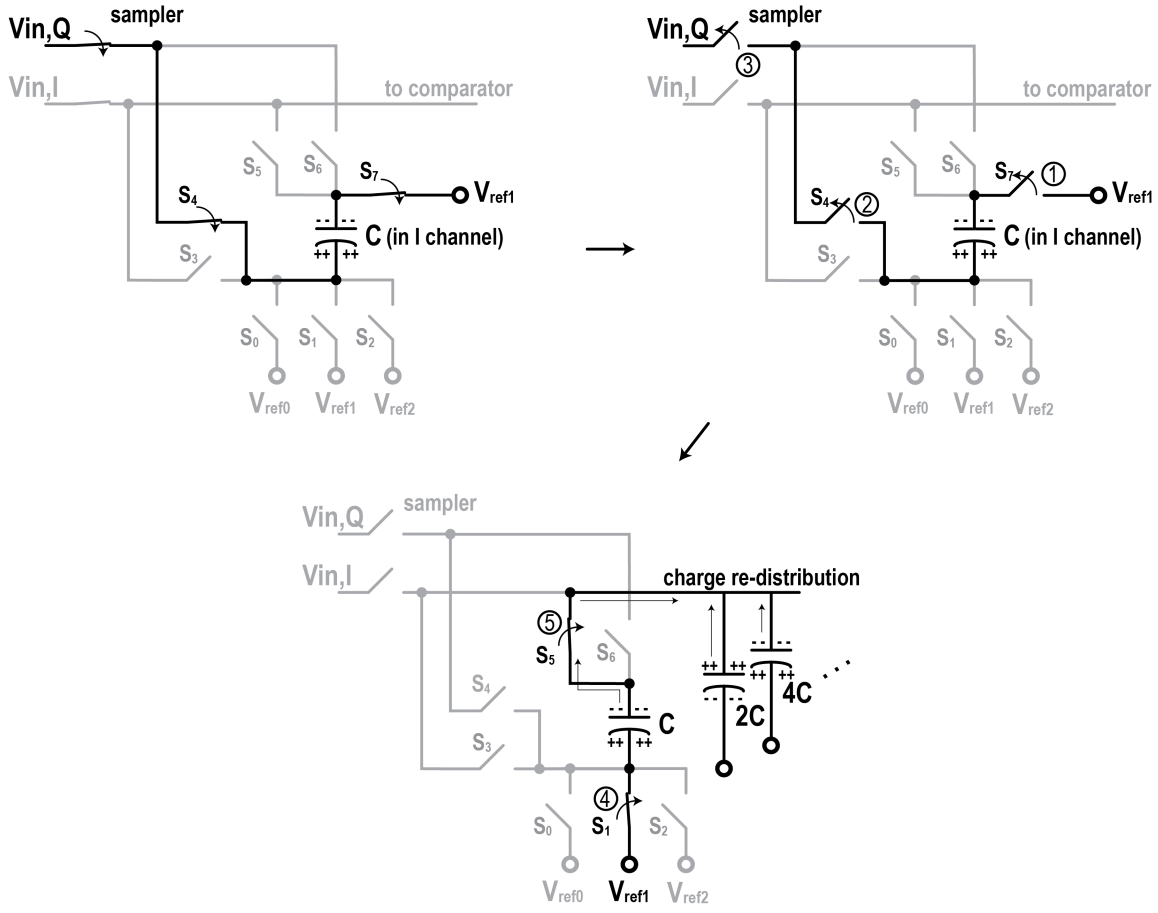


Figure 3.4: Example of switch timing. Capacitor unit in I channel ADC samples from Q channel on the bottom plate.

An example in Fig. 3.4 demonstrates the desired switch sequence when a unit capacitor is sampling from the adjacent channel and in reverse mode. Switches S_4 and S_7 must be turned off before switches S_1 and S_5 switch on to preserve the sampled charge on the capacitor plate. To avoid additional charge injection caused by the inserted switch S_4, S_4 should be turned

off slightly before the sampler. Charge averaging is performed on the input node of the comparator at the end of the sampling phase. The voltage at the comparator input node settles to the desired value along with the launch of the SAR MSB bit trial. Table 3.2 lists the complete critical timing order for different operation modes.

Table 3.2: Switch order in the sampling phase, to avoid undesired charge leakage.

Sample Channel	Sample Plate	1. Switch On	2. Switch Off	3. Switch On
Same channel	top	S_1, S_5	-	-
	bottom	S_3, S_7	S_3, S_7	S_1, S_5
The other channel	top	S_1, S_6	S_6	S_5
	bottom	S_4, S_7	S_4, S_7	S_1, S_5

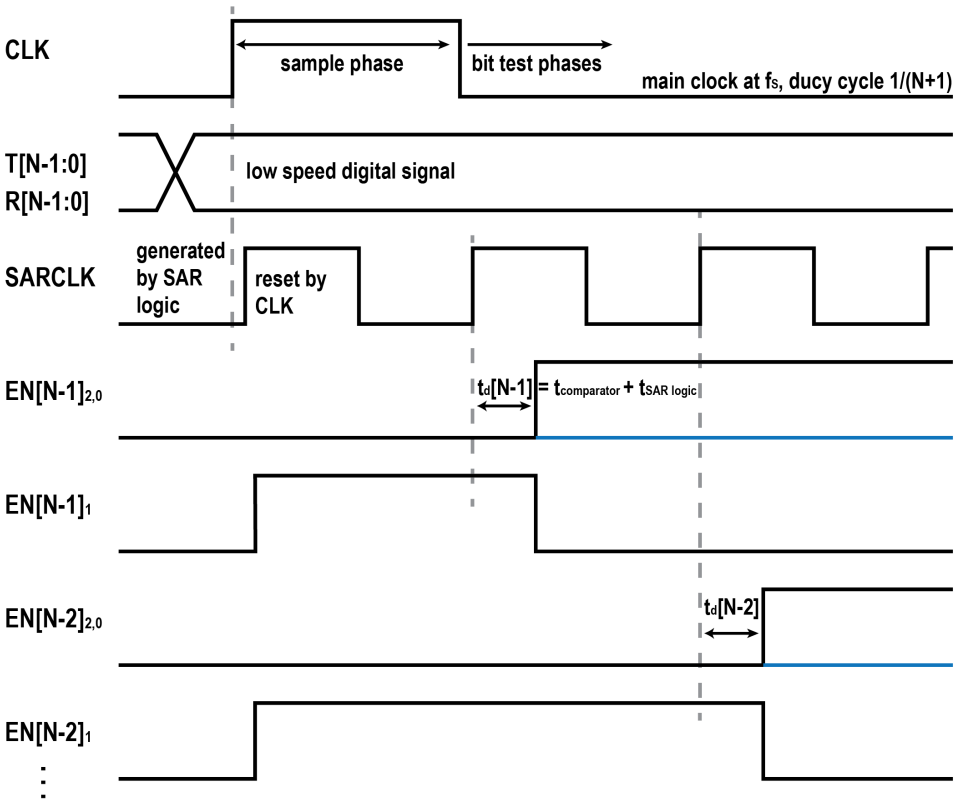


Figure 3.5: Digital signal timing related to the capacitor control.

Each capacitor C_i ($C_i = 2^i C_{unit}$) in the binary capacitor bank takes two additional control signals T_i, R_i. T_i and R_i are defined as follows:

1. T_i. $T_i = 0$, capacitor samples from same channel; $T_i = 1$, from the other channel.

2. R_i. $R_i = 0$, capacitor samples on top plate; $R_i = 1$, on bottom plate.

T_i and R_i are set externally based on the desired signal's angle of arrival. Fig. 3.5 shows the control sequence. The frequency of T_i and R_i varies from kHz to sub-MHz, which is significantly lower than the frequency of the ADC main clock signal clk, based on the algorithm efficiency and digital clock speed. $EN_i[2:0]$ is generated by the SAR logic back-end according to the comparison result. The complete control logic for both the sampling phase and bit decision phases is given below:

$$\begin{aligned} S_{i,2:0} &= EN_{i,2:0}(\overline{clk} + \overline{R_i}) \\ S_{i,3} &= \overline{T_i} \cdot R_i \cdot clk \\ S_{i,4} &= T_i \cdot R_i \cdot clk \\ S_{i,5} &= \overline{T_i} \cdot \overline{R_i} \cdot clk + \overline{clk} \\ S_{i,6} &= T_i \cdot \overline{R_i} \cdot clk \\ S_{i,7} &= R_i \cdot clk, \end{aligned} \tag{3.1}$$

Combining Table 3.2 and equation 3.1, the timing can be satisfied by simply adding delay from clk to $S_{i,1}$ and $S_{i,5}$, because when triggered by clk, the switching behavior of $S_{i,1}$ and $S_{i,5}$ always happen lastly. The control logic can be implemented with two 2-input universal logic gates or custom-designed CMOS gates. Figure 3.6 shows an example of controlling the delay between S_5 and S_6 with standard NAND and NOR cells. In this example, the signal timing is designed by adding additional delay stages and utilizing different transition times in a 2-input logic gate due to the layout asymmetry. Arranging the input order is also helpful for other switch controls. Similarly, to deliberately increase the delay of $S_{i,1}$, the trigger signal clk should be connected to the slower input pin of the NAND/NOR gate.

$$\begin{aligned} S_{i,5} &= \overline{T_i} \cdot \overline{R_i} \cdot clk + \overline{clk} = \overline{(T_i + R_i) \cdot clk} \\ S_{i,6} &= T_i \cdot \overline{R_i} \cdot clk = \overline{(\overline{T_i} + R_i) + \overline{clk}} \end{aligned} \tag{3.2}$$

Figure 3.7 shows the extracted simulation results for four different cases. All the switch timing is satisfied.

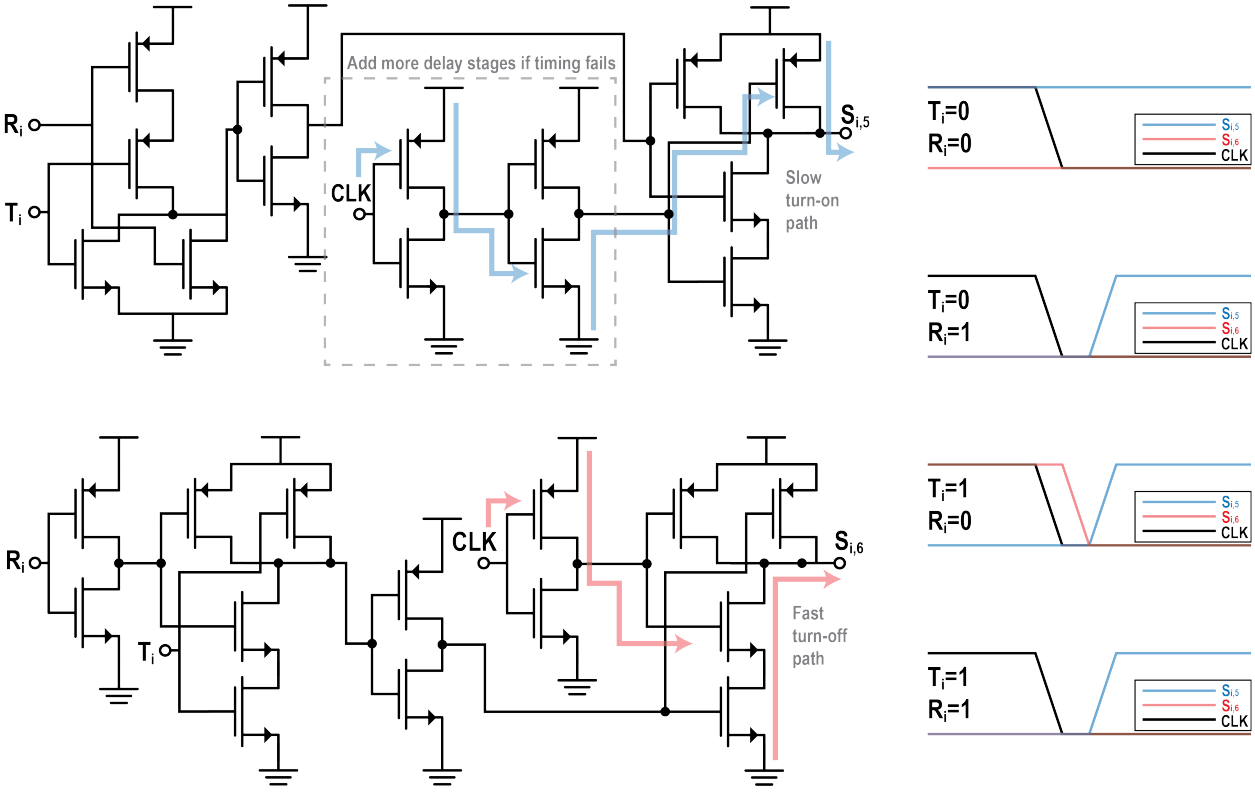


Figure 3.6: Example of switch control signal timing design. The transition of $S_{i,5}$ should always follow $S_{i,6}$. Note that CLK has an additional delay for $S_{i,5}$, and $\overline{CLK}$ is connected to the NMOS that connects to output for faster switching.

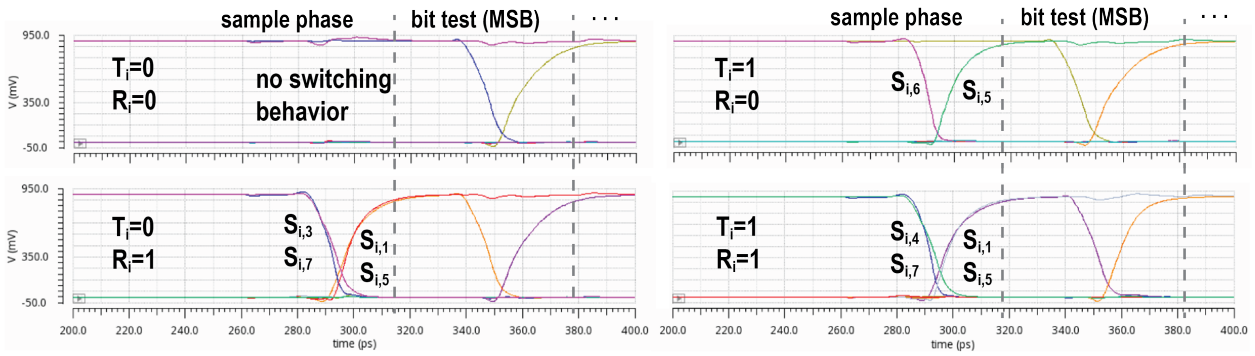


Figure 3.7: Simulation result of the switch control sequence.

3.1.3 Switch Non-ideality

Table 3.3: Comparison table for single-transistor sampler and 2 serial transistor sampler.

	SNR (dB)	SINAD (dB)	ENOB	SFDR (dB)
Single switch	58.73	51.86	8.32	52.87
2 switches	54.00	47.43	7.59	48.50

Inserting an additional transistor S_5 into the signal path can have adverse effects on the input signal. This includes increased harmonics due to parasitic capacitance and reduced gain resulting from a larger RC constant and longer settling time. The simulation results comparing the use of a single-transistor sampler to an equivalent 2-transistor sampler are shown in Fig. 3.8. Even order harmonics are lower because of the differential topology. When using 2 switches, both even and odd order harmonics amplitudes are increased by around 3dB. Table 3.3 provides a summary of the comparison. Generally, adding a transistor in the signal path leads to a loss of 0.7-bit ENOB and 0.6 dB gain drop, without considering the impact of the different control signals on the second switch. To compensate for the increased sampling path resistance, wider switches with bootstrapping can further improve the sampler performance.

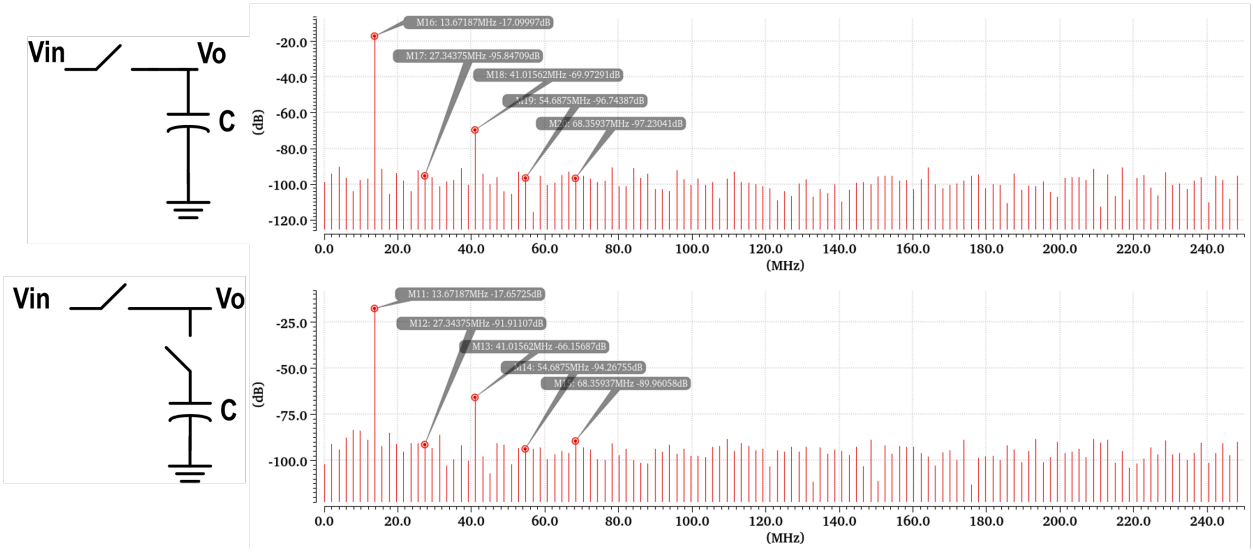


Figure 3.8: Simulation results with single-transistor sampler versus the equivalent two serial transistor sampler.

3.2 SAR Analog Front-end with Integrated Phase Shifter

This section covers the SAR front-end components, including the binary capacitor bank, top and bottom switch arrays, strong-arm comparator, and front-end integration. Besides, we demonstrate how the BAG framework aids in the design process.

3.2.1 Capacitor Bank and Switch Array

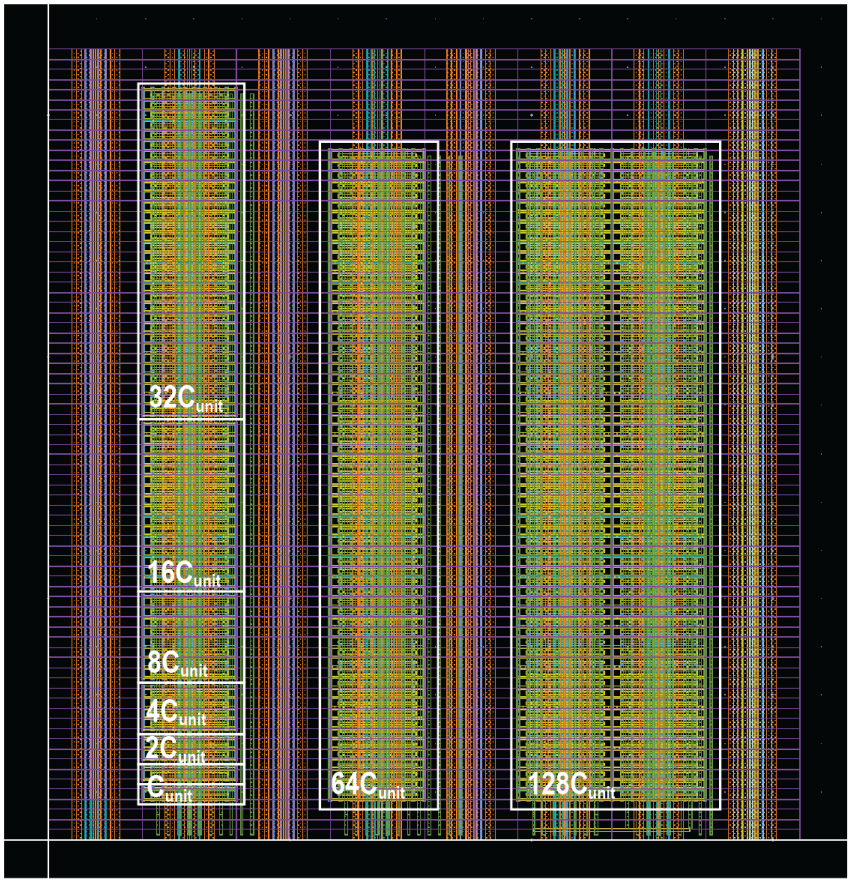


Figure 3.9: Example layout of an 8-bit capacitor DAC.

The arrangement of unit capacitors is designed to create a square-like capacitor bank, taking layout considerations into account. Initially, the size of each unit capacitor is determined by both matching requirements and the available layout grid specified by BAG Laygo

space [43]. The capacitor is constructed by using metals 2 through 5 to form a metal-oxide-metal (MOM) capacitor, with each unit capacitor approximately $0.9fF$ in size. Fig. 3.9 illustrates this layout. To enhance accuracy, the capacitor unit for the least significant bit (LSB) is positioned in the lower-left corner, serving as the center of the entire differential capacitor bank. Capacitors are first stacked vertically, with a 1-unit space between them for separation and easier routing. Subsequently, the larger-weight capacitors expand horizontally. For differential implementation, it is preferable for the overall height to be slightly larger than the width.

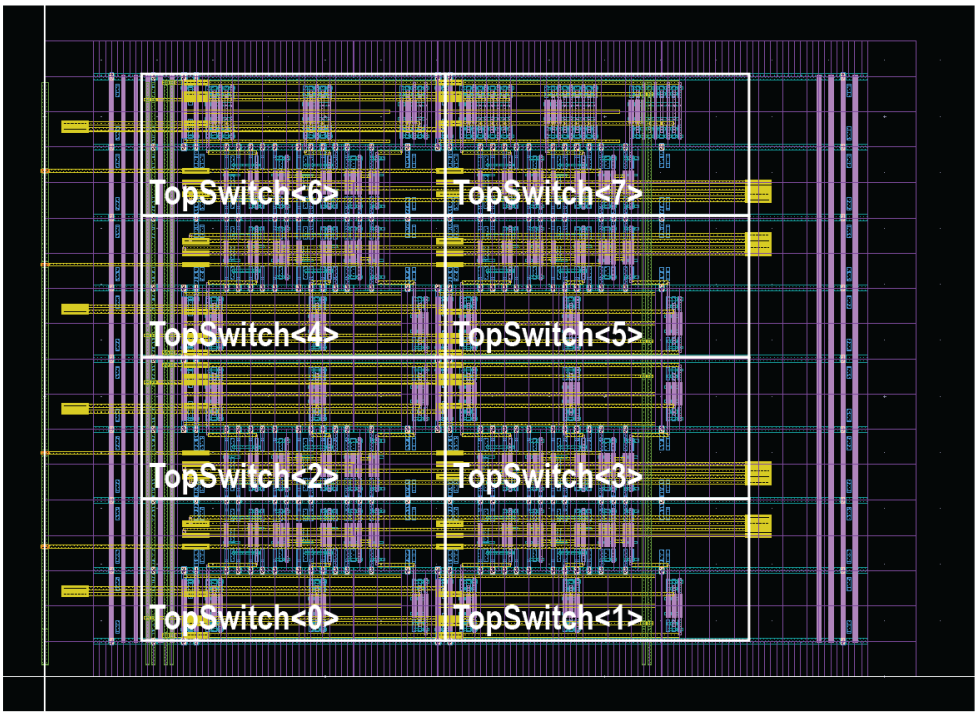


Figure 3.10: Example layout of the switch array connected to the capacitor top-plate (transistor layout is not shown)

The inserted switches, as discussed in Section 3.1, are divided into two types and grouped together to form a top switch array and a bottom switch array. The primary consideration is to minimize the discrepancy introduced by layout and to use the space more efficiently. An example of the top switch array is shown in Fig. 3.10. Inside each sub-block, the top row consists of logic gates that implement Equation 3.1. The bottom row represents the actual pass transistors as switches. The overall horizontal space is determined by the wider row, and the logic gates are placed as close as possible to the transistor gate that they are

controlling. The transient simulation result is shown in Fig. 3.11. When driving the different sizes of the capacitors, the top switching array adds 15-28ps to the sampler settling time.

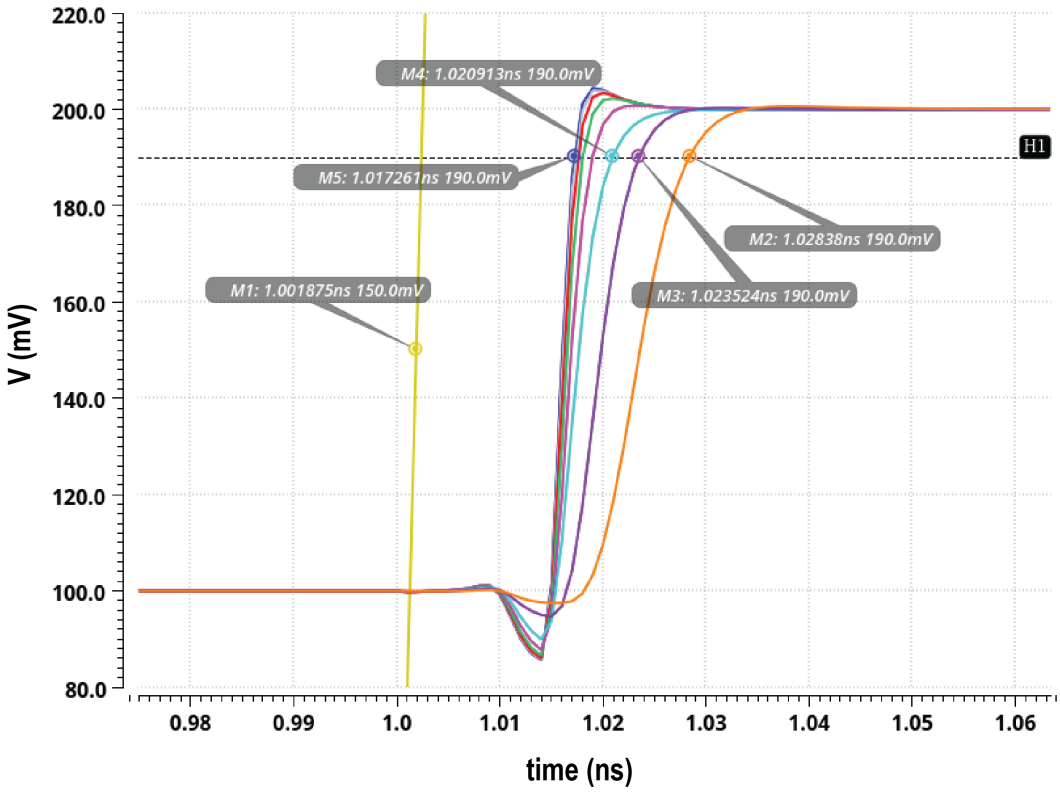


Figure 3.11: Transient response of the top switch array.

3.2.2 Strong-Arm Comparator

The SAR ADC's input common-mode voltage is set to 0.35V. With a monotonic switching SAR scheme, the common-mode voltage on the capacitor gradually decreases to 0. Therefore, a strong-arm comparator with a PMOS input pair is employed. The schematic of the strong-arm comparator is depicted in Fig. 3.12. When `CLK` is low, all the internal nodes are reset to `GND` through NMOS pass transistors to eliminate the residual signal. When `CLK` is at a high level, the comparator becomes active. The offset calibration pair's size ratio to the input pair is 1:8. A simple output buffer is used to provide rail-to-rail comparison results for the SAR back-end logic.

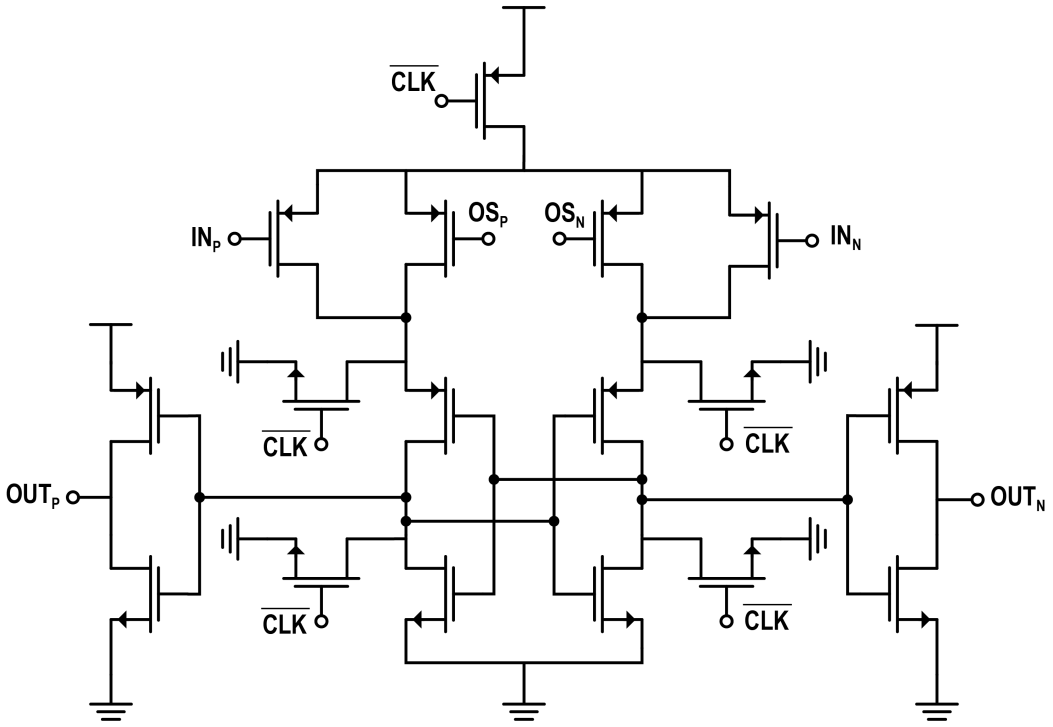


Figure 3.12: Strong arm comparator with PMOS input pair. Transistors for offset calibration and reset are shown.

BAG is a powerful framework for optimizing analog/mixed-signal (AMS) circuits. Fig. 3.13 illustrates the BAG-assisted design procedure for the strong-arm comparator under development. Initially, the comparator specifications, such as speed, noise, and power, are derived from system requirements. These specifications are then summarized in a `.yaml` file, which can be easily modified in iterations or for future use. Similarly, the allowed search space can be specified, defining the range of transistor sizes, for example, based on available area or power budget. Keeping this information separate allows the generator to be independent of specific specifications or technology nodes, making it more general and shareable with others who may not have access to the technology specifics.

At the start of the generator, an initial solution is calculated based on these `.yaml` files. For instance, the total delay of the comparator can be calculated as $t_{tot} = t_{on} + t_{int} + t_{re-gen} + t_{buf}$. Each delay component can be estimated using parasitic capacitance (C_{gs}, C_{gg}, C_{dd}, etc.) and resistance (r_o, gm, etc.) at the internal node, which can be acquired through BAG's API for calculation.

Next, a schematic and a testbench template need to be manually created for the BAG

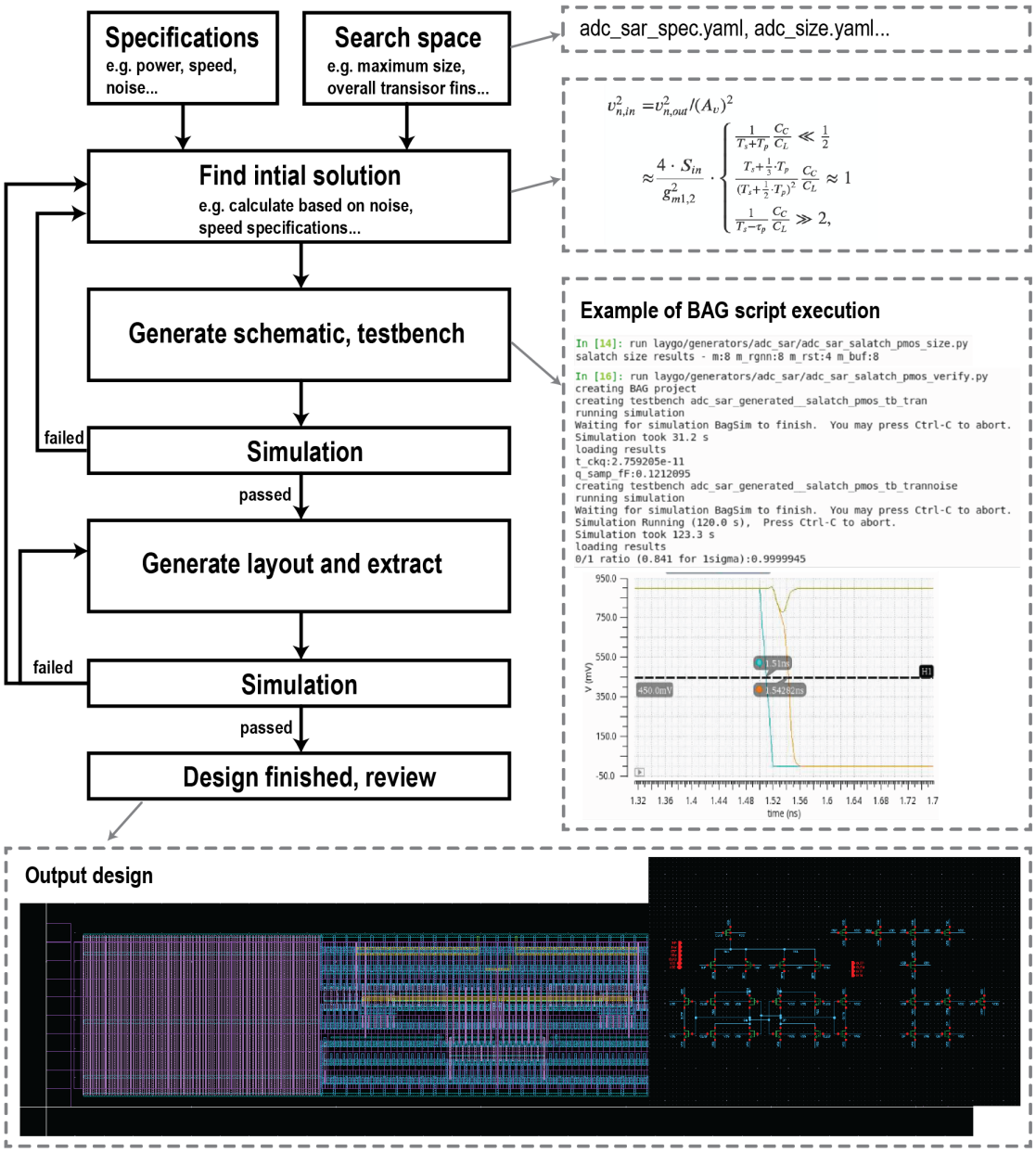


Figure 3.13: Design the strong-arm comparator using BAG flow.

schematic generator. The schematic includes only the chosen topology, while the transistor primitives are left empty for BAG to set the values in each iteration.

Finally, the layout generator includes the designer's insights. Only relative, virtual coordinates should be used to place transistors or sub-blocks [43]. Since all routing is automatic and on the grid, a well-written layout generator should always deliver DRC clean circuits, significantly reducing labor and saving time for post-layout simulation and optimization.

3.2.3 SAR Phase Shifter Analog Front-End

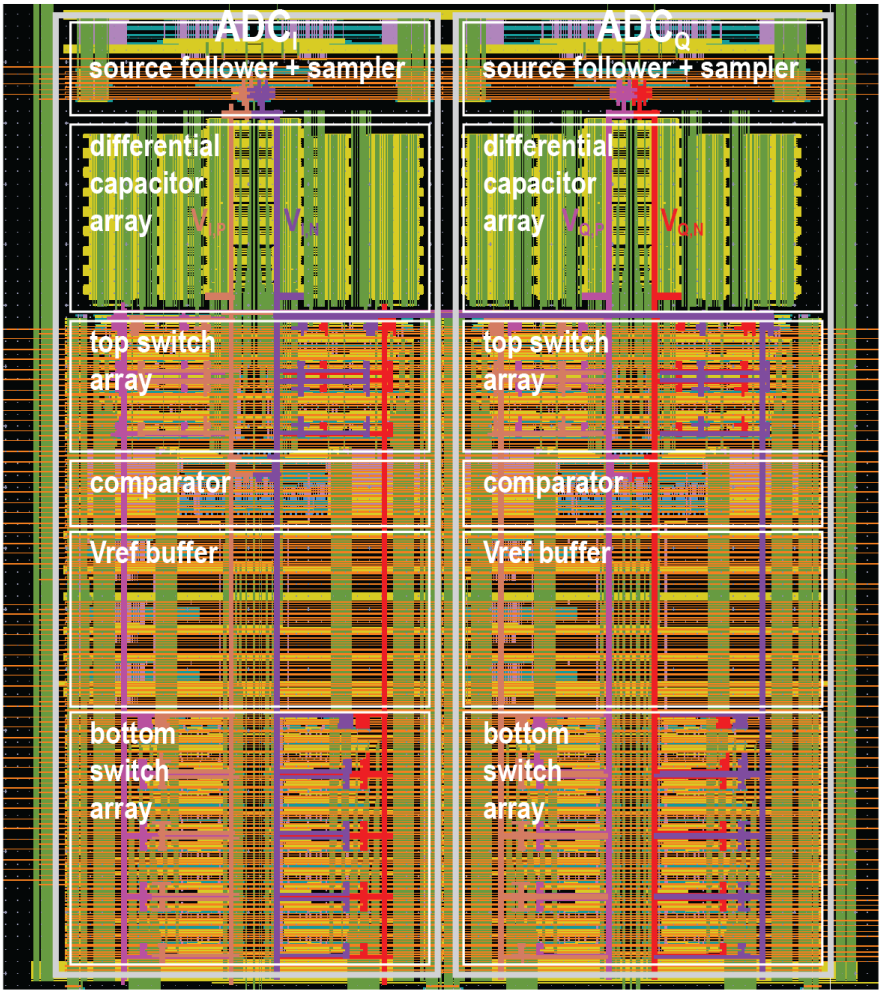


Figure 3.14: Analog front-end of the phase shifter embedded SAR ADC. Highlighted sampler output shows I/Q integration

Fig. 3.14 illustrates the integrated phase shifter layout in the front-end of 2 SAR ADCs. Each channel's SAR ADC is differential, to minimize common mode noise, even-order har-

monic, and symmetric mismatch. The sub-blocks are designed to have the same width for vertical stacking. The highlighted traces represent the I/Q channel sampler distribution lines, connecting to both plates of each capacitor unit. The top switch array is positioned adjacent to the capacitor array to minimize parasitic capacitance and resistance, which could otherwise reduce the sampler's gain. The reference voltage local buffers and the bottom side capacitor array are situated below the strong-arm comparator.

3.3 SAR Back-End and Peripheral Circuits

3.3.1 SAR Back-End

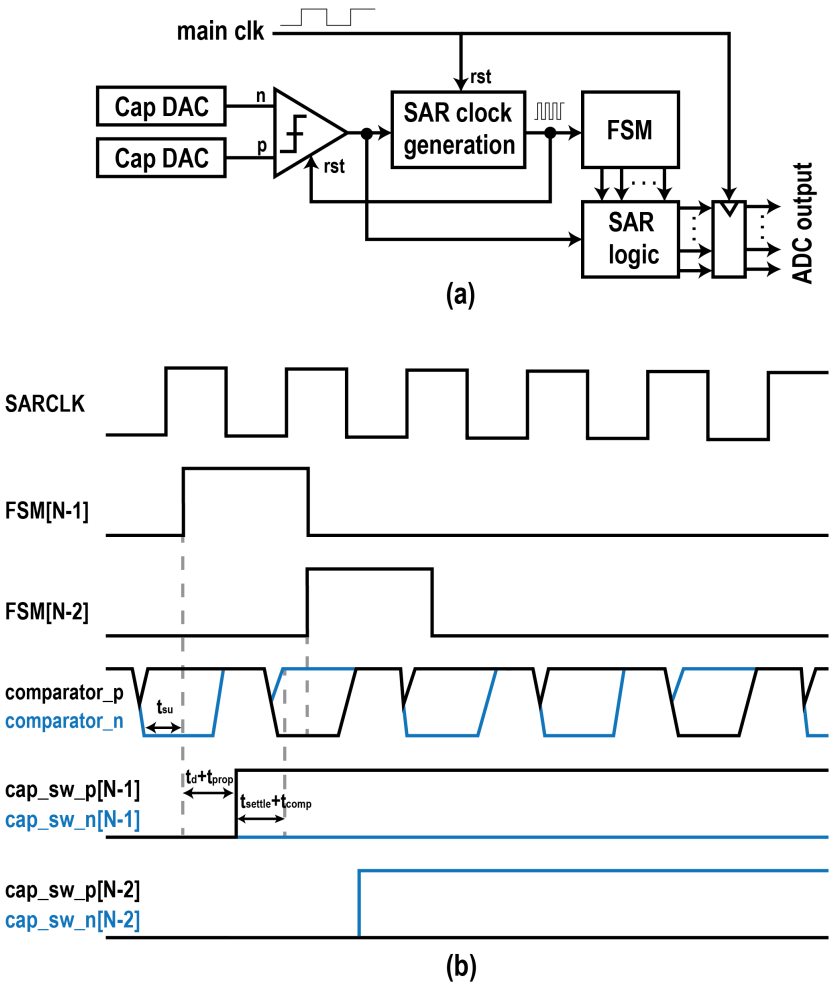


Figure 3.15: (a) SAR back-end diagram. (b) Timing diagram.

Since the capacitor control function is integrated into the switch array in the SAR front-end, the SAR back-end only needs to implement normal SAR control and logic. Fig. 3.15 (a) illustrates the high-level blocks, and Fig. 3.15 (b) depicts an example timing diagram. The clock generation module generates an asynchronous SAR clock within a cycle of the main sampling clock. The asynchronous SAR clock is also reset by the rising edge of the sampling clock. The finite state machine (FSM) operates at the SAR clock frequency. The FSM

selects the window that determines which SAR bit corresponds to the current comparator result. Based on the FSM selection and comparator results, the SAR logic generates the corresponding capacitor DAC control signal and updates it at every SAR clock edge. The setup time t_{su} is defined by how much time the comparator should deliver the result before the FSM selection, as the FSM selection is treated as a trigger signal for the SAR logic block. The SAR logic module also produces the ADC output and synchronizes it with the main clock through the output register.

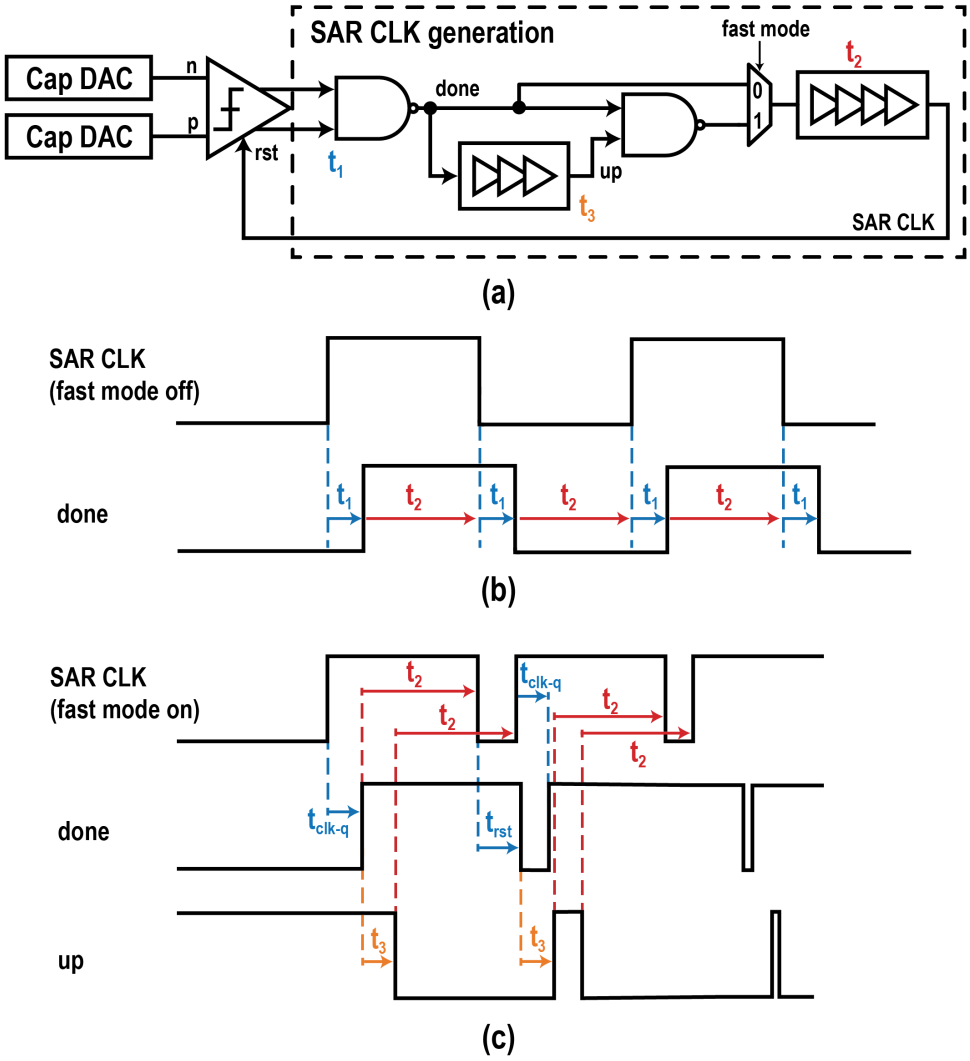


Figure 3.16: (a) Asynchronous clock generation with fast mode and bypass option. (b) Fast mode disabled. The SAR clock has a constant pulse width. (c) Fast mode enabled. SAR clock pulse gradually disappears, which can save switching energy when timing is satisfied.

In the SAR asynchronous clock generation module, two operational modes are available to potentially enhance the speed and power performance of the back-end. Illustrated in Fig. 3.16, enabling the fast mode entails inserting a digitally controlled delay line to generate a narrow pulse. This action causes the low-level period of the SAR clock to become narrower and eventually disappear. Consequently, this eliminates additional switching energy after all bit tests are completed. However, meticulous timing analysis for the entire sampling cycle is required to ensure correctness. Conversely, when the fast mode is disabled, the SAR clock generation module operates like an inverter-based ring oscillator.

3.3.2 On-Chip Reference Voltage Generation

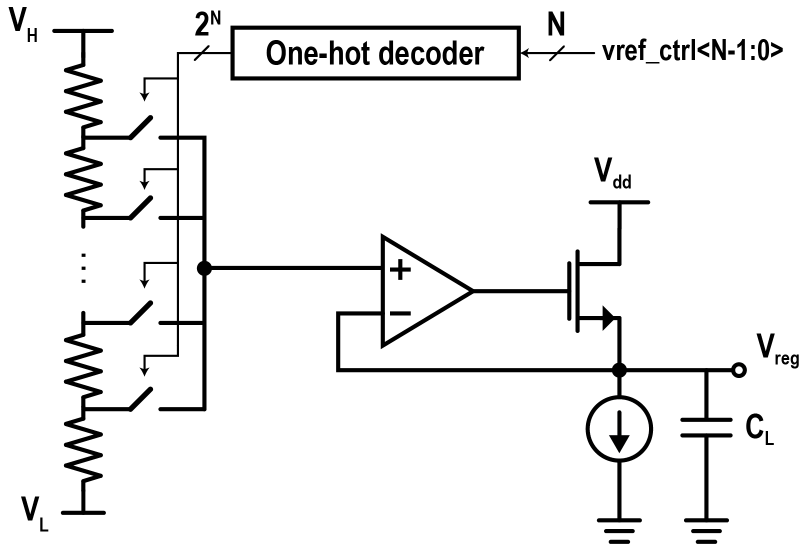


Figure 3.17: On-chip reference voltage generator and LDO.

The reference voltages needed by the SAR ADC are internally generated on the chip. The diagram in Fig. 3.17 illustrates the digitally controlled reference voltage generation module. A 7-bit resistor ladder divides the voltage range from V_L to V_H. A synthesized digital one-hot decoder block converts the 7-bit control signal to select the desired output. An LDO regulator with an NMOS pass transistor is employed for reduced output resistance and improved power supply rejection (PSR) [50][51]. Besides, the required reference voltages are set below $V_{dd}/2$, enabling the use of the NMOS pass transistor.

Fig. 3.18 depicts the frequency response of the LDO loop under varying load capacitances of 100pF, 200pF, and 500pF. A bandwidth exceeding 500MHz is achieved when the load is

less than 200pF, which corresponds to the intended use case. A PSR of -24.6dB is achieved within this bandwidth.

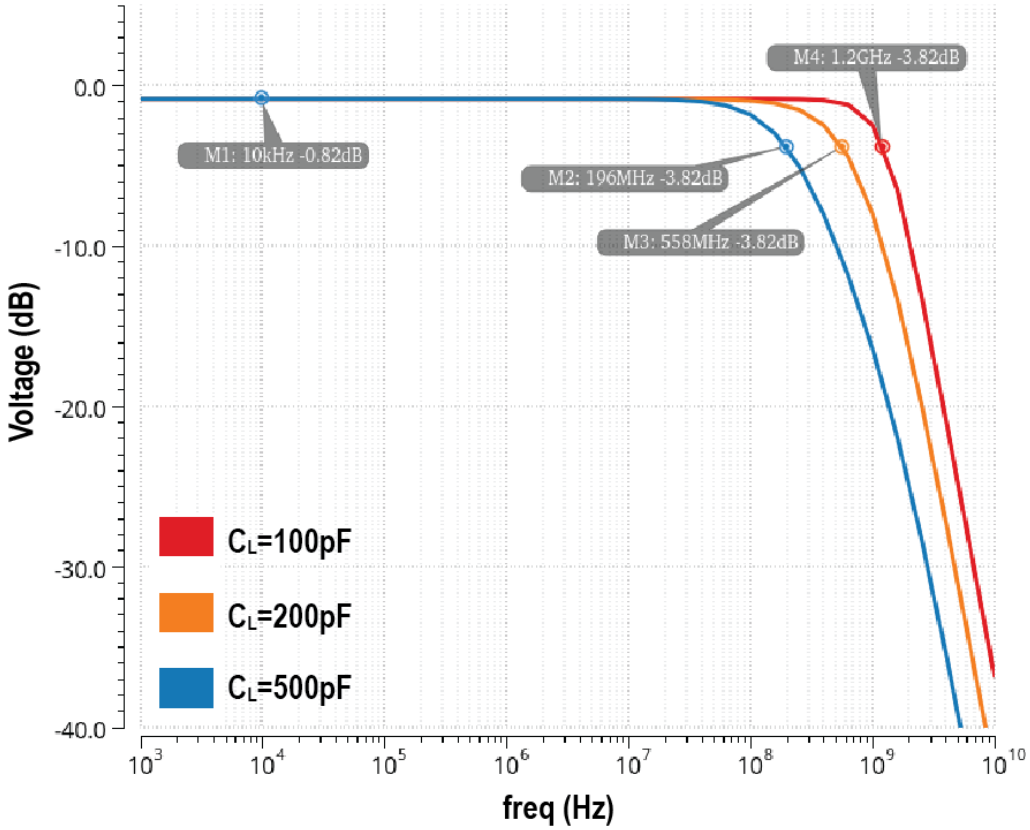


Figure 3.18: Frequency response of the super source follower.

3.3.3 Scan Chain Controller

A synthesized digital scan chain is utilized for non-critical control signals, such as capacitor DAC programming, strong-arm comparator offset calibration, sampler offset calibration, voltage reference selection and calibration, and SAR asynchronous clock operation mode. This scan chain is controlled by an FPGA through a hand-shake interface, which will be detailed in Chapter 5. The scan chain contains 784 bits. It supports writing at speeds up to 48MHz and reading from the chip at speeds up to 12MHz.

3.4 Phase Shifter Simulation Results

3.4.1 ADC Performance

When all the capacitor bank control signals are set to 0, the phase shifter applies 0° phase shifting and runs as two independent SAR ADC. The transient simulation result at the output of the comparator is shown in Fig. 3.19. Each 9-bit dual SAR ADC runs at F_S = 400MS/s with $\text{FOM}_{W,hf}$ = 36fJ/conv-step. The average simulated SNR with single-tone input is 42.3 dB. The SNDR is 40.1dB, which equals to 6.37 ENOB.

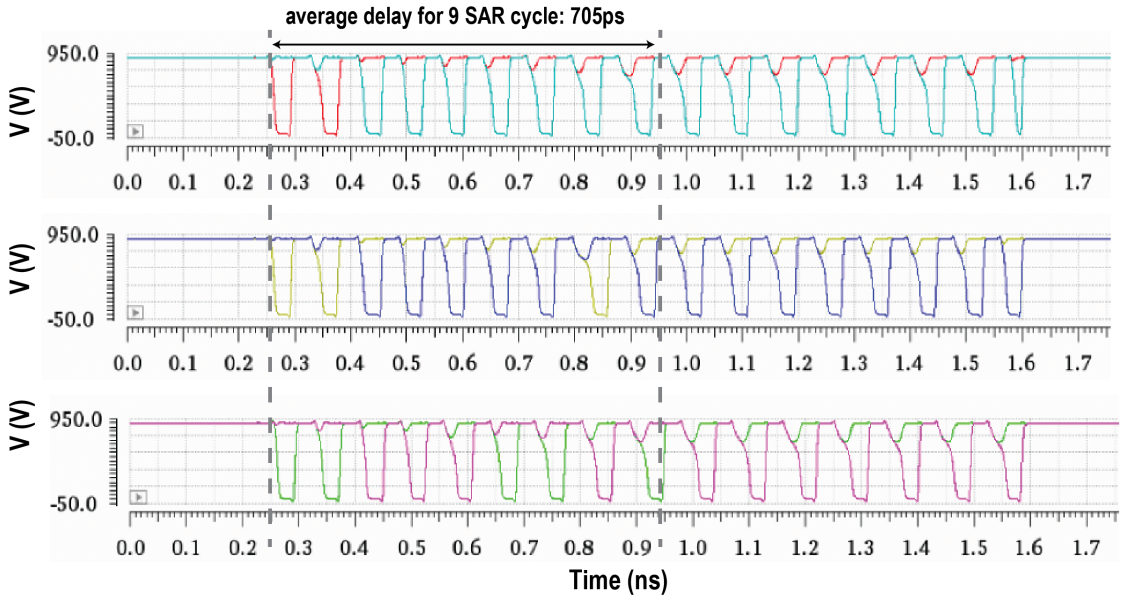


Figure 3.19: Transient simulation result with DC input.

3.4.2 Phase Shifter Performance

Fig. 3.20 displays the simulated phase constellation without calibration. It's important to note that the constellation edge exhibits slope mismatch in different quadrants due to the gain mismatch between the regular sampling units and the flipped capacitor units. We will further discuss the calibration method in the measurement chapter. The sparsest phase region with the all-capacitor sampling scheme is near 45°, where the phase shifter still has 1°resolution.

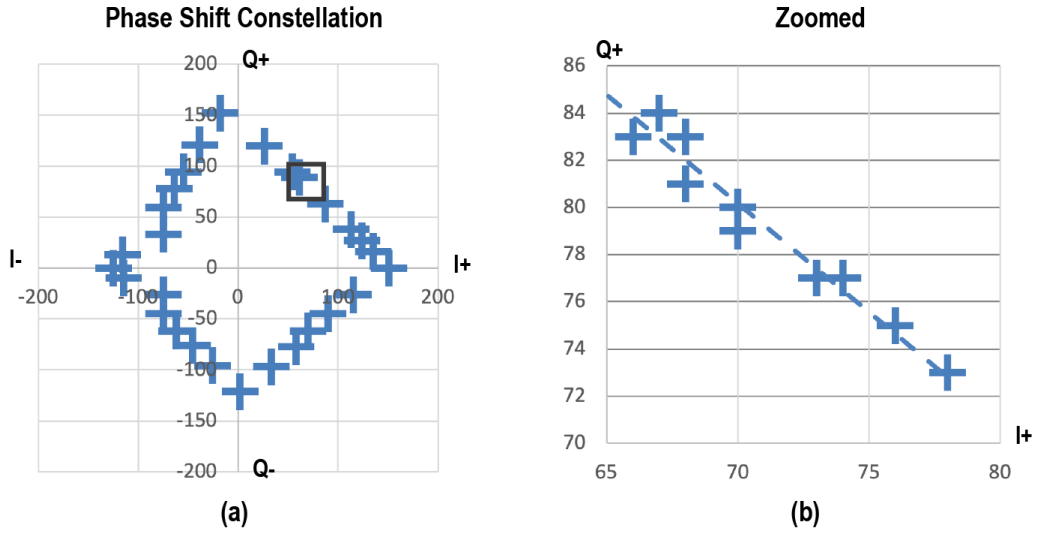
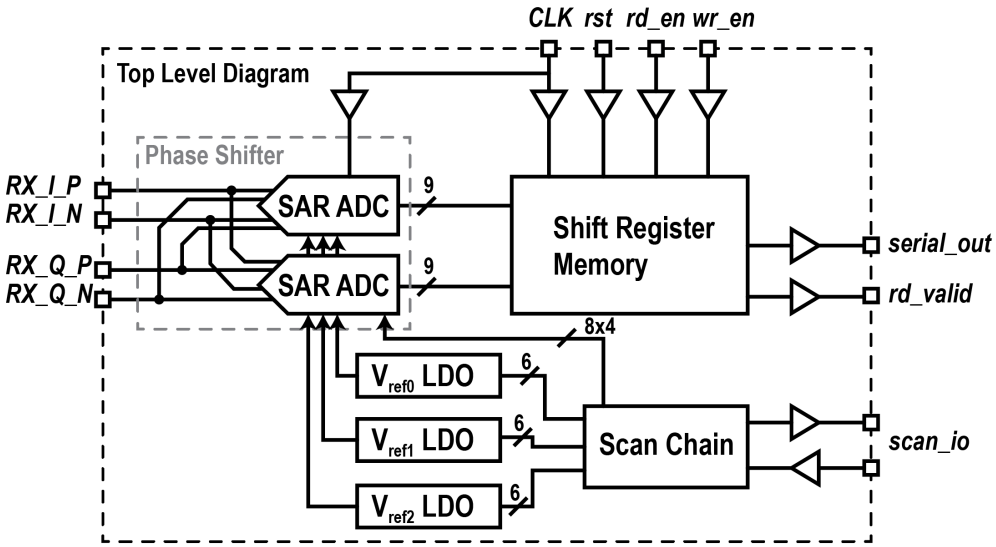


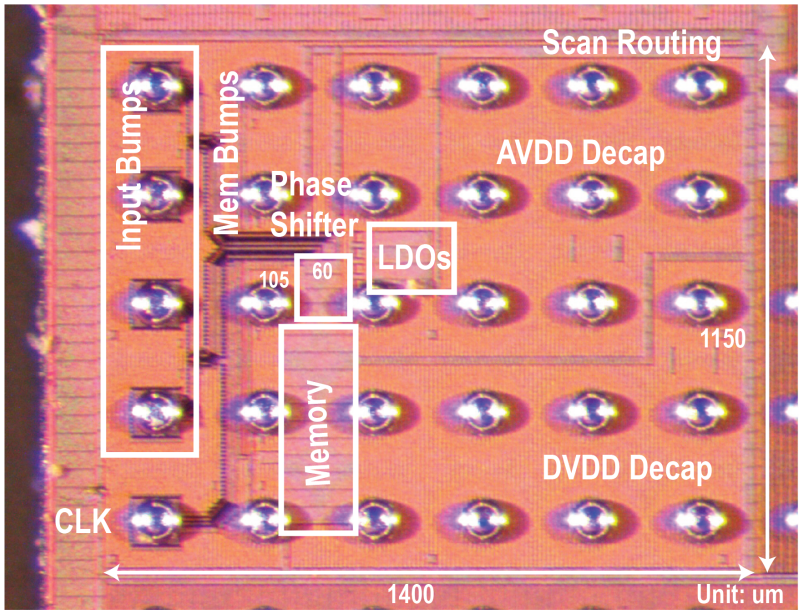
Figure 3.20: Extracted simulation results without calibration. (a) 8-point skipped. (b) Zoomed near 45°.

3.5 SAR Phase Shifter Test Chip

To verify the proposed SAR ADC with an integrated phase shifter, we designed a compact test chip that contains a SAR phase shifter and the supporting circuits. As shown in Fig. 3.21 (a), the phase shifter comprises two 9-bit SAR ADCs with the proposed programmable capacitor array. The 9 × 2-bit digital output is collected by a shifter register memory on the chip. The 18 × 256 (4.5kb) shift register memory captures the output data at the ADC operation frequency and sends out the data through the slow serial interface. Due to the constraints in the available chip area, only 10 edge bumps can be assigned at will. Consequently, the digital interface is simplified and only the necessary ports are kept. The reference voltages are also generated on the chip using resistor ladders and LDOs because of the lack of available bumps. The scan chain is shared among several independent designs on the same chip and is located in another sub-chip, so the scan is routed on lower metal layers to this design. Fig. 3.21 (b) shows the chip photomicrograph. The total area is $1.4 \times 1.15\text{mm}^2$. The SAR phase shifter is $60 \times 105\text{um}^2$ and is placed near the input bumps to minimize the layout non-ideality. The LDOs and the shift register memory are placed next to the phase shifter. Decoupling capacitors are filled in the empty space for analog and digital power. The BGA grid is 245um and the 10 bumps for inputs and outputs are located on the left. Chapter 5 will discuss measurement setup and results.



(a)



(b)

Figure 3.21: (a) Top-level diagram of the phase shifter test chip. (b) Chip photo with BGA.

Chapter 4

SAR ADC based Beamformer

In Chapter 3, we delve into the implementation of a precise and compact phase shifter. This chapter will use the proposed SAR phase shifter and design an integrated beamformer. To form a beam, a sum-and-average step is necessary after adjusting the phase and before the analog-to-digital conversion. The proposed beamformer architecture is illustrated in Fig. 4.1. The highlighted blocks pertain to the same SAR ADC in the I/Q channel. The capacitor DAC is segmented into multiple smaller slices for different channels, adhering to

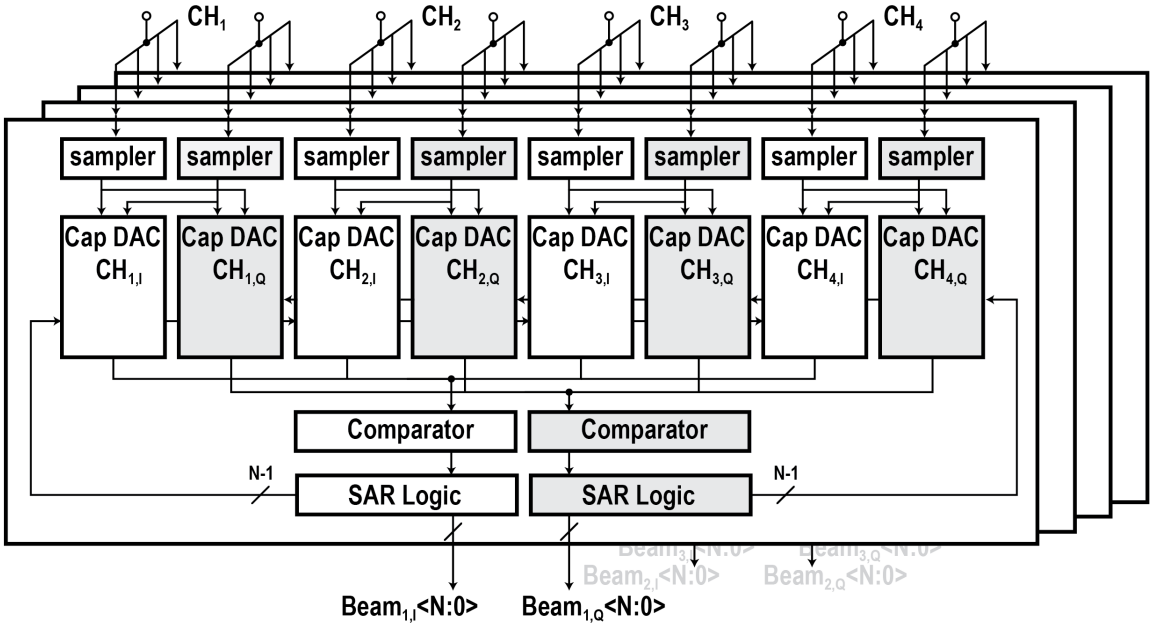


Figure 4.1: Architecture of a 4x4 SAR ADC beamformer.

the constraints discussed in Chapter 2. The outputs of these capacitor DACs are then merged and connected to the strong-arm comparator, followed by the SAR logic. Each beamformer slice's output is a 2N-bit digitized beam of the I and Q channels. The VGAs for compensating for phase-related gain in each channel are located off-chip.

4.1 Phase Shifter Optimization

In section 3.4.2, it's observed that the phase shift in different quadrants exhibits different gains, and a phase discontinuity occurs due to the MSB capacitor transition. While these non-idealities can be easily calibrated when testing the phase shifter alone, they can pose challenges to the beamformer's overall performance. This is because the charge offset will accumulate across all channels before the AD conversion, making it difficult to calibrate all channels. Therefore, the first step is to enhance performance from a layout and floorplan perspective.

4.1.1 Capacitor DAC

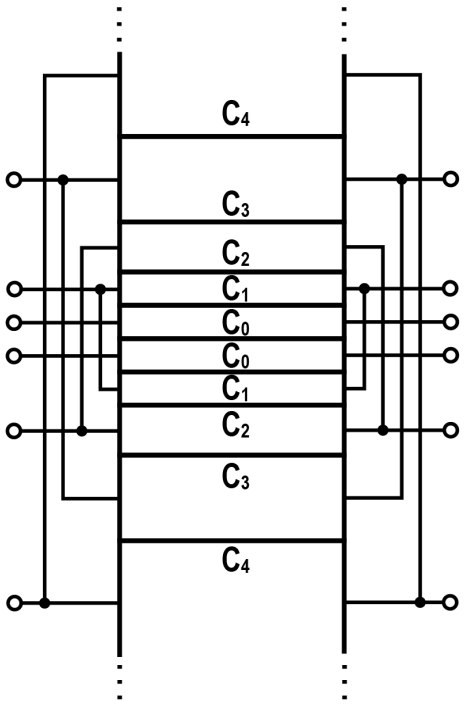


Figure 4.2: Diagram of the 1-D capacitor DAC.

The capacitor units are stacked along the y-axis, as shown in Fig. 4.2. The capacitor array is symmetric to enhance accuracy in the center. The main reason for this optimization is that in the 2-D capacitor DAC discussed in Chapter 3.2, the major glitch occurs during the transition when large capacitors in the horizontal direction are enabled, which is expected due to differences in capacitor shape and surroundings. Although this mismatch can be calibrated in a SAR phase shifter, performing the same in the beamformer is challenging since we need to identify the mismatch from each channel and calibrate accordingly. Therefore, improving the matching of capacitor DAC is beneficial.

Fig. 4.3 shows the extracted simulation result comparison of the capacitor DAC's DNL and INL. DNL is improved from -1.82 to -0.50 LSB. INL is improved from +1.25/-1.18 to 0.57/-0.45 LSB.

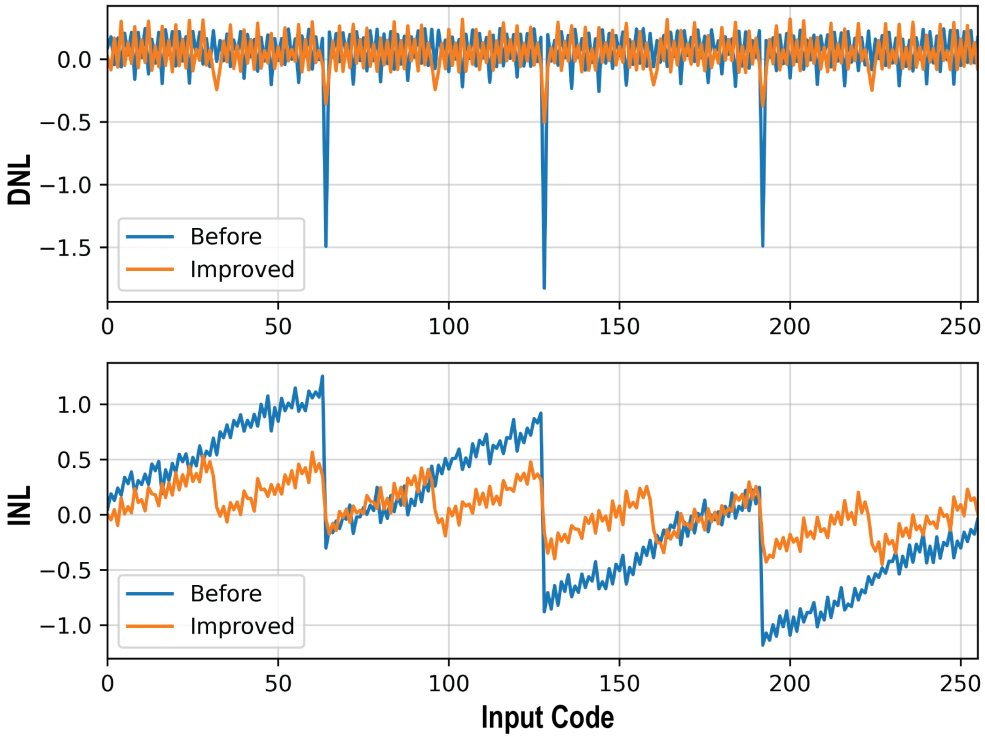


Figure 4.3: DNL, INL of the improved 1-D capacitor DAC comparing with the 2-D capacitor array in Chapter 3.2.

4.1.2 Switch Array

The switch array is another source of the systematic mismatch. In Fig. 3.14, the routing length to access each plate differs when capacitors are sampled from top or bottom plates, as the top switch array and the bottom array have different distances to the capacitors. With the optimized 1-D capacitor DAC, it is easier to improve the layout symmetry. As shown in Fig. 4.4, the switches are placed next to the capacitor DAC, which results in balanced top-plate sampling and bottom-plate sampling. The post-simulation result shows the RC constant mismatch is reduced by 65%.

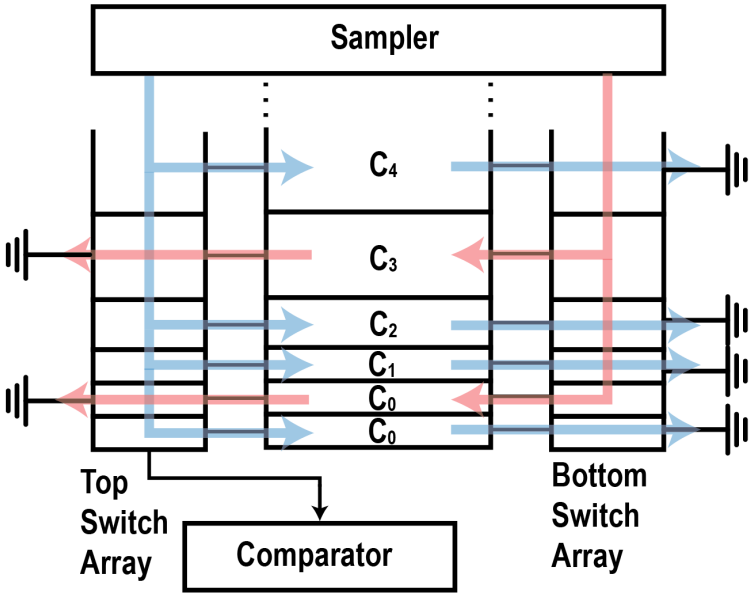


Figure 4.4: New switch array with improved sampling balance.

4.1.3 Channel Floorplan

Fig. 4.5 compares the optimized 1-D channel layout with the 2-D version. The differential capacitor bank is implemented and placed at the center of each channel. Therefore, the top and bottom switch arrays are moved to the same side, but it would not increase the asymmetry of sampling. Compared to the phase shifter SAR front-end with a 2-D capacitor array, the overall area remains the same, while the mismatch and parasitic introduced by layout are significantly improved and would leverage the effort of calibration.

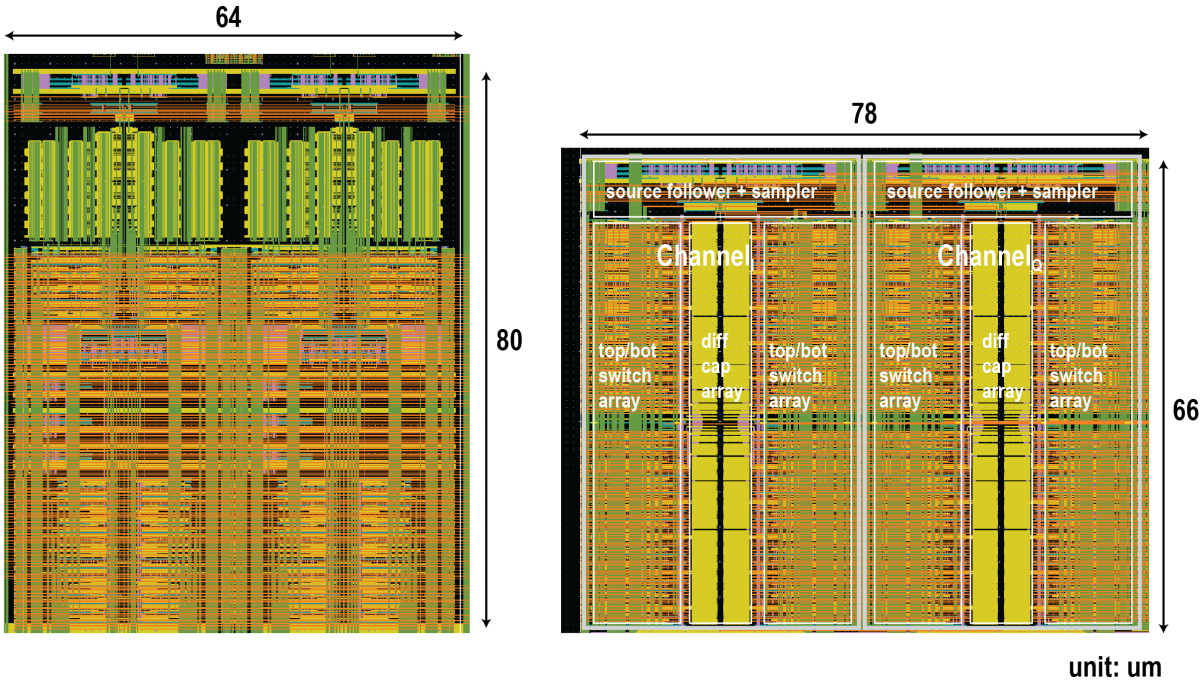


Figure 4.5: Optimized phase shifter SAR front-end

4.2 Beamformer

As discussed in section 2.2.1, an average step is required to form a beam. At the end of the sampling phase, each capacitor unit i in channel j holds the charge $Q_{i,j} = C_{i,j}V_j$. The average of all capacitors in all channels is the desired voltage level.

$$V_{\text{OUT}} = \frac{\sum_{i,j} Q_{i,j}}{\sum_{i,j} C_{i,j}} \tag{4.1}$$

$$\begin{aligned} V_I^{'}(t) &= \frac{1}{N}\sum_{i=1}^{N}\left(a_i V_{I,i}(t) + b_i V_{Q,i}(t)\right) \\ V_Q^{'}(t) &= \frac{1}{N}\sum_{i=1}^{N}\left(c_i V_{I,i}(t) + d_i V_{Q,i}(t)\right) \end{aligned} \tag{4.2}$$

$$\begin{aligned} \text{where } c_i &= b_i \\ d_i &= -a_i \end{aligned}$$

4.2.1 Charge Sharing Trace

Charge sharing trace is the routing trace which connects all the sampling capacitors in each channel. Fig. 4.6 illustrates the implementation of the global charge-sharing trace. The charge-sharing trace passes through the middle of the capacitor DAC for a minimum overall charge moving distance.

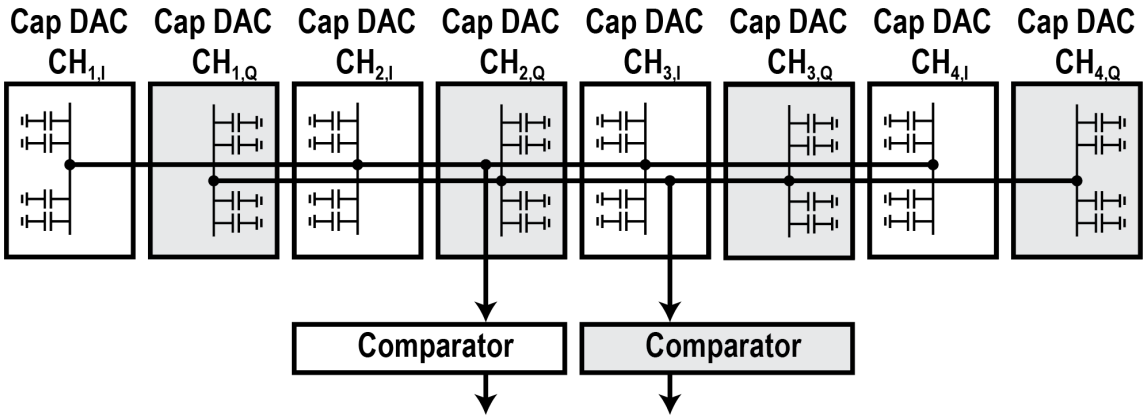


Figure 4.6: Global charge sharing trace. Only a single-ended capacitor is shown for simplicity.

4.2.2 Residual Charge on Parasitic Capacitance

When multiple channels are enabled, the parasitic effect of the global charge-sharing trace should not be neglected because it will increase the settling time after the sampling phase, and the comparator can give a wrong result of the MSB test. A stronger connection of the charge-sharing trace decreases the parasitic resistance, and the overall settling time is reduced. However, it will also increase the parasitic capacitance at the comparator input, where the residual charge of the previous conversion results in the error. Besides, the parasitic capacitance causes a systematic gain error because of the charge-sharing effect. It is a design trade-off. To resolve this issue, the parasitic capacitor is reset to AC ground voltage level through an additional transistor during the sampling phase. The top switch array is also slightly modified. Fig. 4.7 shows the concept. The simulation result shows that adding a resetting switch improves the average ADC SNR by 2-2.5 dB.

4.2.3 Back-End Timing

Typically, the comparator has a longer delay when the input voltage difference is small, as it takes more time to reach the threshold of the strong-arm comparator. It indicates that the

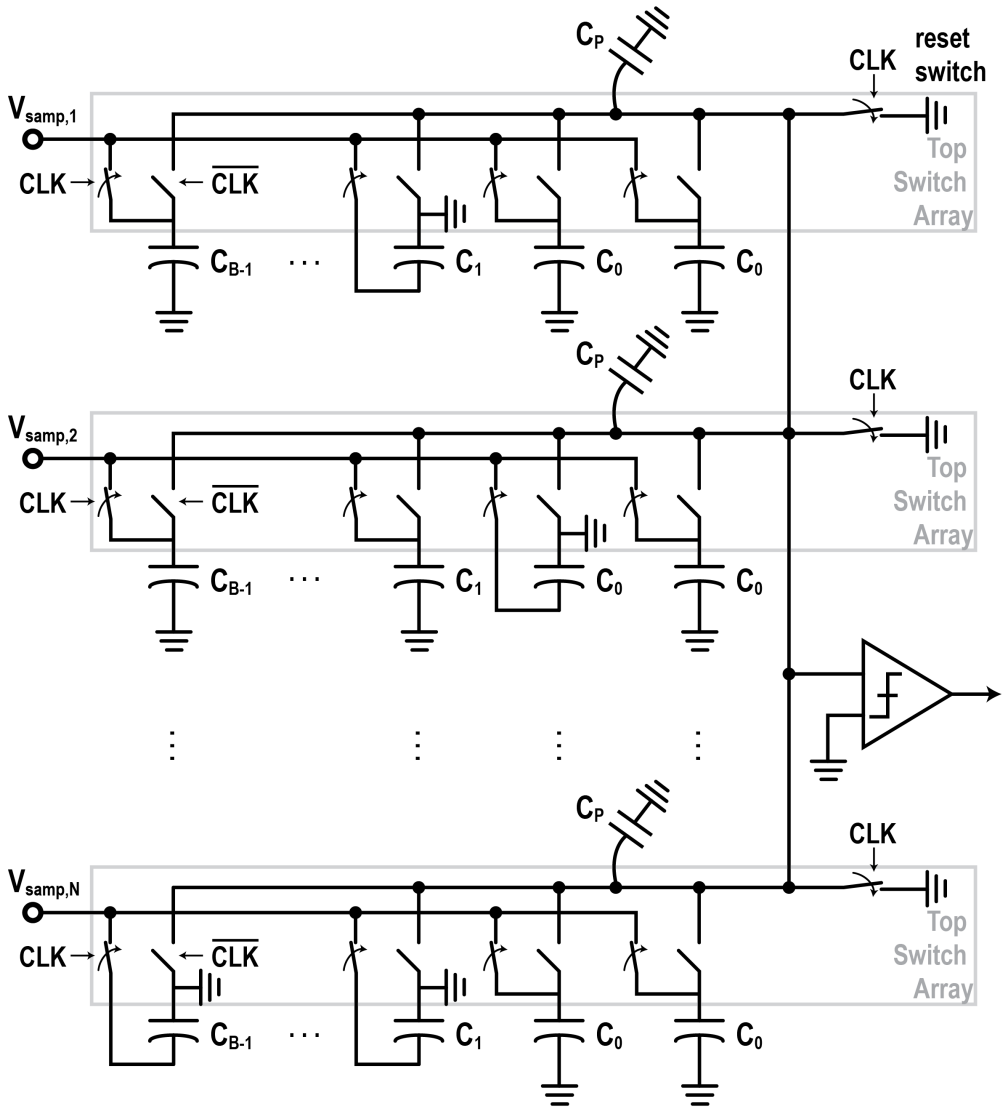


Figure 4.7: Parasitic capacitance and the resetting switch.

LSB bit-test limits the SAR clock frequency. However, the MSB bit-test requires additional settling time in our proposed beamformer SAR method, and the simulation shows that MSB is the major timing constraint. To satisfy the timing requirement, simply slowing the SAR clock by Δt will result in a $B \cdot \Delta t$ overall delay increment. Instead, an adjustable delay line is enabled only for the first SAR rising edge after the main sampling clock transits. Fig. 4.8 shows the transient simulation results with different delay times enabled. From the figure, when Δt changes, it only delays the time that the first rising edge of the SAR clock, while

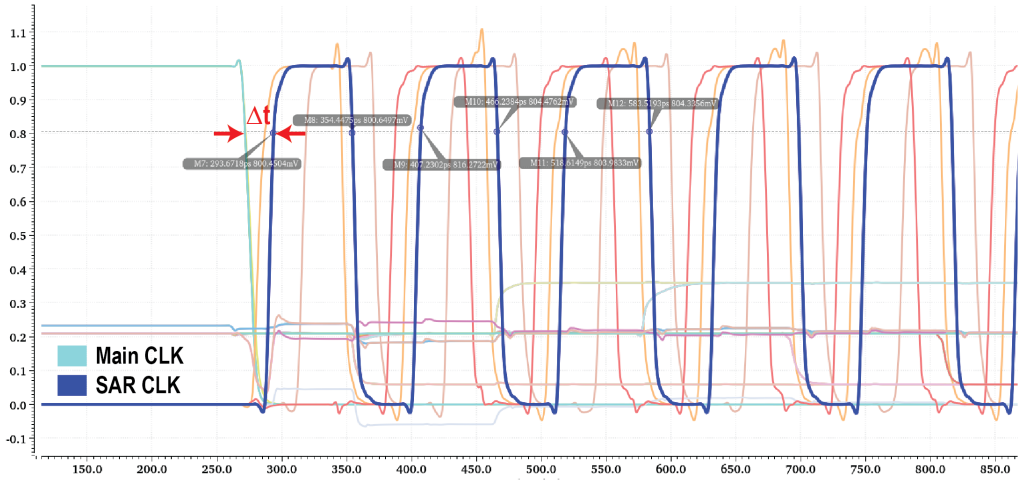


Figure 4.8: Adjustable delay for the first SAR clock period for the worst-case settling constraint.

the following SAR clock is unaffected. It avoids significant performance degradation and guarantees the correctness of the result.

4.2.4 Beamformer SAR ADC Programmed as SNF

Although the goal is to design a beamformer, it is also possible to use the proposed hardware as a configurable spatial notch filter and perform digital beamforming in DSP, with a cost of gain. In equation 4.2, we choose $c_i = b_i$ and $d_i = -a_i$ so that the resulted beamformer has the maximum gain. However, the coefficient a_i, b_i, c_i, d_i can be configured arbitrarily since each unit capacitor has the flexibility. Therefore, each beamformer can also be configured as a spatial notch filter:

$$
\begin{aligned}
V_{I,i}^{'}(t) &= V_{I,i}(t) - V_{I}^{'}(t) \\
&= V_{I,i}(t) - \frac{1}{N}\sum_{i=1}^{N}\big(a_i V_{I,i}(t) + b_i V_{Q,i}(t)\big) \\
&= \frac{1}{N}\big(- a_1 V_{I,1}(t) - b_1 V_{Q,1}(t) - ... + (N - a_i)V_{I,i}(t) - b_i V_{Q,i}(t) - ... \\
&\quad - a_N V_{I,N}(t) - b_N V_{Q,N}(t)\big) \\
V_{Q,i}^{'}(t) &= \frac{1}{N}\big(- b_1 V_{I,1}(t) + a_1 V_{Q,1}(t) - ... - b_i V_{I,i}(t) + (N + a_i)V_{Q,i}(t) - ... \\
&\quad - b_N V_{I,N}(t) + a_N V_{Q,N}(t)\big)
\end{aligned}
\tag{4.3}
$$

We need to set the coefficients so that each term has the correct relative ratio. The $|N \pm a_i|$ term is significantly larger than the rest $a_{i..N}, b_{i..N}$. It means most of the capacitor unit not in channel i is idle and will result in a gain drop of $20\log_{10}(N)$dB.

4.3 Simulation Results

We implemented the proposed beamformer in Fig. 4.1. The capacitor DAC in SAR ADC is divided into four channels for the phase shifting and beamforming feature. Each beamformer samples four channels and outputs a 9-bit I/Q digital beam. The beamformer operates as a typical SAR ADC when the input channels are shorted. Fig. 4.9 shows the simulated ADC spectrum with a single sine wave input, when the beamforming feature is disabled. The input is a low-frequency single-tone sine wave at $7/128F_S$, and the sampling clock frequency is $F_S = 500MHz$. The SAR ADC has 40.6dB SNDR and 6.52 ENOB.

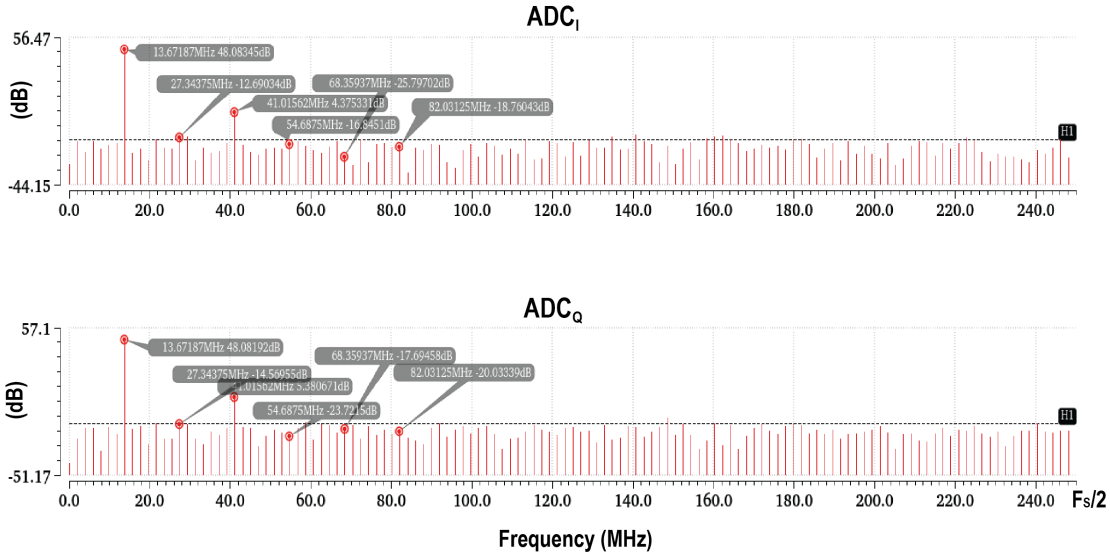


Figure 4.9: 256-point FFT result from SAR beamformer transient simulation.

Fig. 4.10 shows the SAR beamformer simulation result when 9-bit SAR ADC with 8-bit capacitor DAC is used. For each desired beam center direction, the capacitor DAC in each channel is programmed to achieve the corresponding phase shift. The spatial notch is determined after the analog-to-digital conversion. As shown in the figure, the SAR beamformer demonstrates selective spatial gain, and the location of the beam/notch center aligns accurately with the digital control. Three deep nulls can achieve over 40 dB. Note that the depth

of the spatial notch and nulls primarily relies on the matching of capacitors across channels, as accurate phase shifting and amplitude matching are essential for signal cancellation in a specific direction.

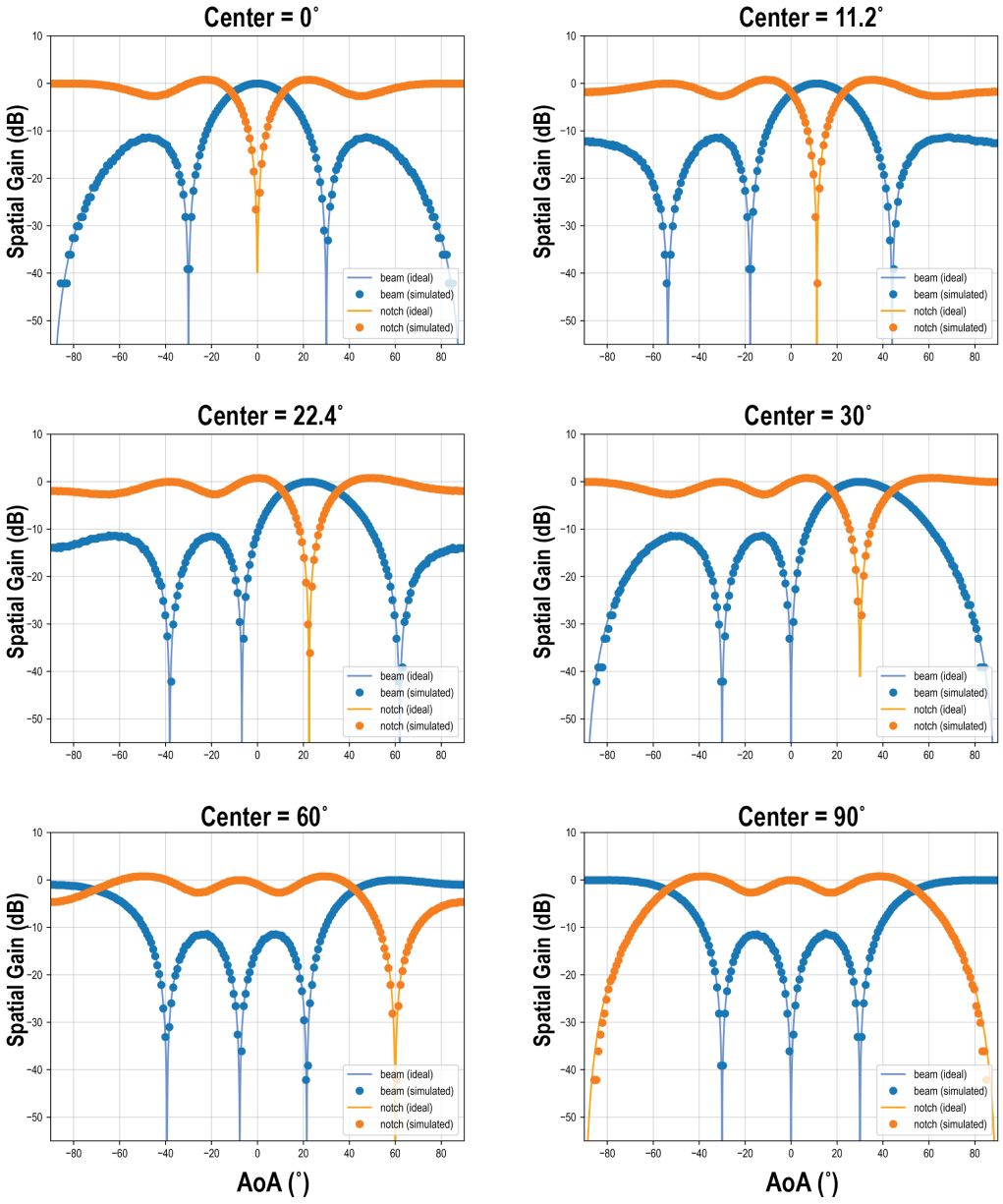


Figure 4.10: Simulation result of the beamformer. Notch is calculated after the analog-to-digital conversion.

4.4 SAR Beamformer Test Chip

Fig. 4.11 shows the top level of the test chip. The test chip is $2 \times 2\text{mm}^2$, which takes a quadrant in a $4 \times 4\text{mm}^2$ die. The test chip is also using Intel 16 technology. Four 9-bit 4-1 beamformers are placed on the chip. The 4×4 beamformer measures $300 \times 470\text{um}^2$. Similarly to the phase shifter chip, the output is captured by a shift register memory with a width of $9 \times 2 \times 4$ bits. The shift register memory can be read out from its serial port. The gain compensation for each channel is applied off-chip by digitally controlled variable gain amplifiers (VGAs).

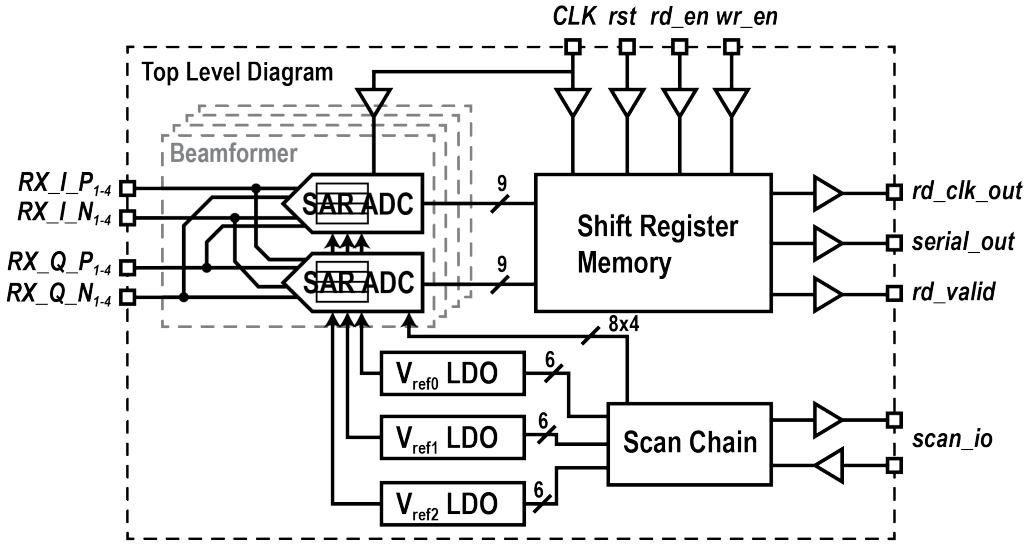


Figure 4.11: Top level block diagram of the beamformer test chip.

Chapter 5

Measurement Results

This chapter provides an overview of the test equipment, the test plan for both the phase shifter chip and the beamformer chip, and the digital interface used for accessing data. It also presents the measurement results and discussions.

5.1 Phase Shifter Test Setup

5.1.1 Device Under Test (DUT)

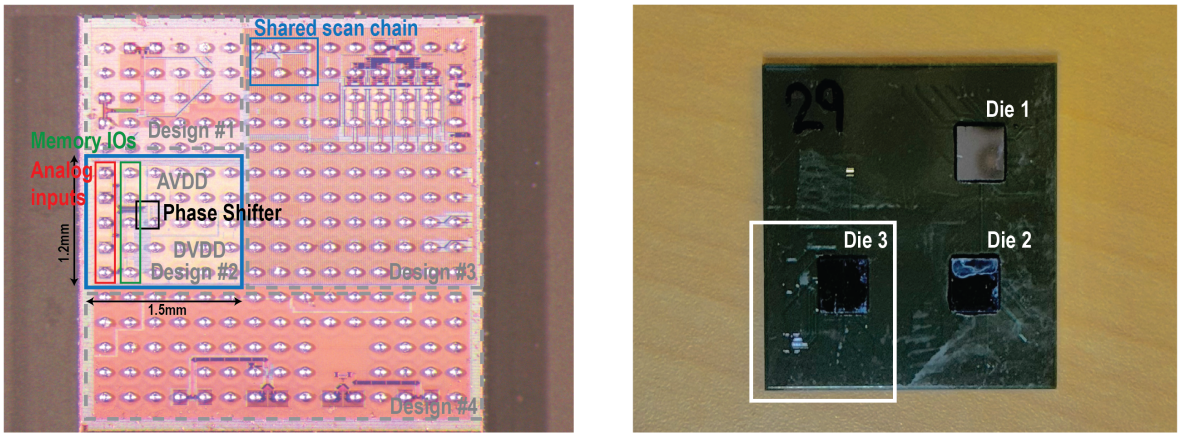


Figure 5.1: Device under test (DUT-1) (a) Phase shifter flip-chip die photo (bump up). (b) BGA package top view.

The initial tape-out of the proposed SAR ADC-based phase shifter was in August of 2022, using Intel 16 technology and being one of four designs on the same chip. We use DUT-1 to denote this chip in the subsequent sections. Fig. 5.1 (a) shows the photo of DUT-1. The die is divided into four rectangular regions with separate isolated power domains, and the phase shifter unit is located on the middle left. The active area of our design is $1.5 \times 1.2\text{mm}^2$. Due to the area constraints, only the outermost two rings of bumps, totaling 10 bumps in this sub-chip, can be freely designated as signals and IOs. In Fig. 5.1 (a), the five bumps on the left of the sub-chip are assigned to differential I/Q channel inputs and a single-ended clock. The remaining five are designated as memory IOs. On this chip, four designs use a shared scan chain, which provides digital control for circuits such as DC biasing and offset. 128 bits of the scan output are routed to our sub-chip for DC reference control, capacitor unit functionality settings, SAR back-end tuning, etc. Fig. 5.1 (b) shows the package top view. Three dies are flipped and attached to a single package because the package is supposed to support the testing for all designs, and one of the other designs requires loop-back testing for their serial link. For our SAR phase shifter prototype, only the sub-chip in the lower left chip (die 3) is enabled and connected to the BGA package.

5.1.2 Test Plan

The high-level testing architecture of the phase shifter chip is shown in Fig. 5.2. DUT-1 requires two power domains: AVDD at 0.9V and DVDD at 0.85V. A two-stage LDO provides the low-noise power supplies to the chip. The first stage takes $\tilde{5}$V voltage from a power supply unit (PSU), bringing it down to 3.3V; the second I^2C-controlled stages bring it down to 0.9V and 0.85V separately. Level shifters transfer 3.3V FPGA signal to 0.85V for the chip digital interface, i.e., the scan chain IOs and the memory IOs. A correlated I/Q differential signal and a square wave single-ended clock are required as analog input. The inputs are fed into the chip through edge-mounted SMAs.

5.1.3 Test PCB

The phase shifter and beamforming chips have similar digital interfaces and memory designs. We adopt a two-board design to test both chips efficiently and reduce cost. The testing board in Fig. 5.2, colored in light green, is divided into a host board (powerboard) and a chipboard, as shown in Fig. 5.3.

The power board contains an insulation displacement connector (IDC) for FPGA connection, a multi-purpose socket connector (MPSC) for board-to-board connection, the level shifters for digital IOs, and the LDOs. Note that a spare second-stage LDO is also placed on board, providing an additional power domain through I^2C-controlled interface for the beamforming chip's reference voltage. Since most of the shared functions are placed on the powerboard, the cost of the chipboard is reduced because the chipboard has fewer components and is smaller in size. The chipboard contains a single BGA package, power bypass

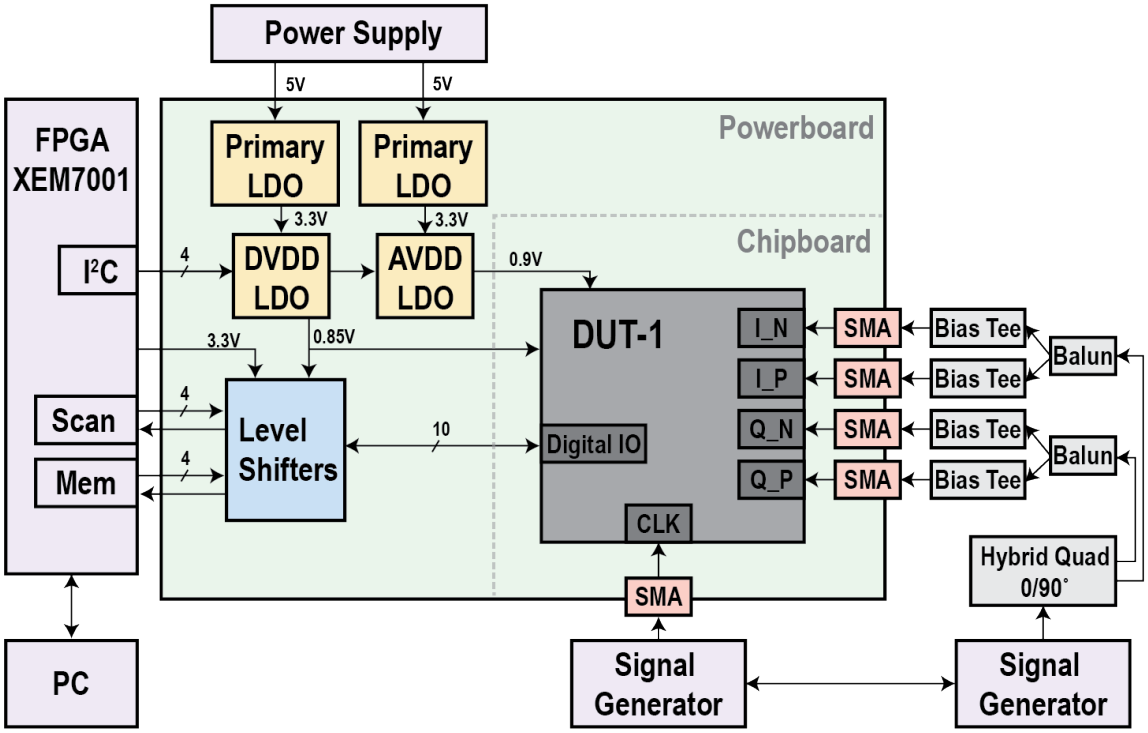


Figure 5.2: Test plan diagram for DUT-1.

headers, and SMA connectors for analog inputs. Two boards are connected with an 84-pin MPSC board-to-board connector.

5.1.4 FPGA and Memory Interface

The on-chip shift register memory saves the phase shifter and beamformer's digital output. Fig. 5.4 shows the data read-out method. The shift register memory in both chips has parallel writing and serial reading ports. The writing ports are synchronized with the ADC sampling clock, while the reading ports are synchronized with the slow scan clock. The ADC converts and outputs data after it is enabled. When the FPGA sets `wr_en` to high, the shift register memory saves data, regardless of the overflow. Once the `wr_en` is set to low, the data in memory will not change and will be held until `rd_en` is high. The serial output will be synchronized with the slow clock, and `rd_valid` is set to high when data is ready. The state machine on FPGA takes the command line input from the terminal, provides the corresponding signal, and monitors the returned data. In the beamformer chip, the memory size exceeds the FPGA buffer, so the data is read out several times by batch, which is also

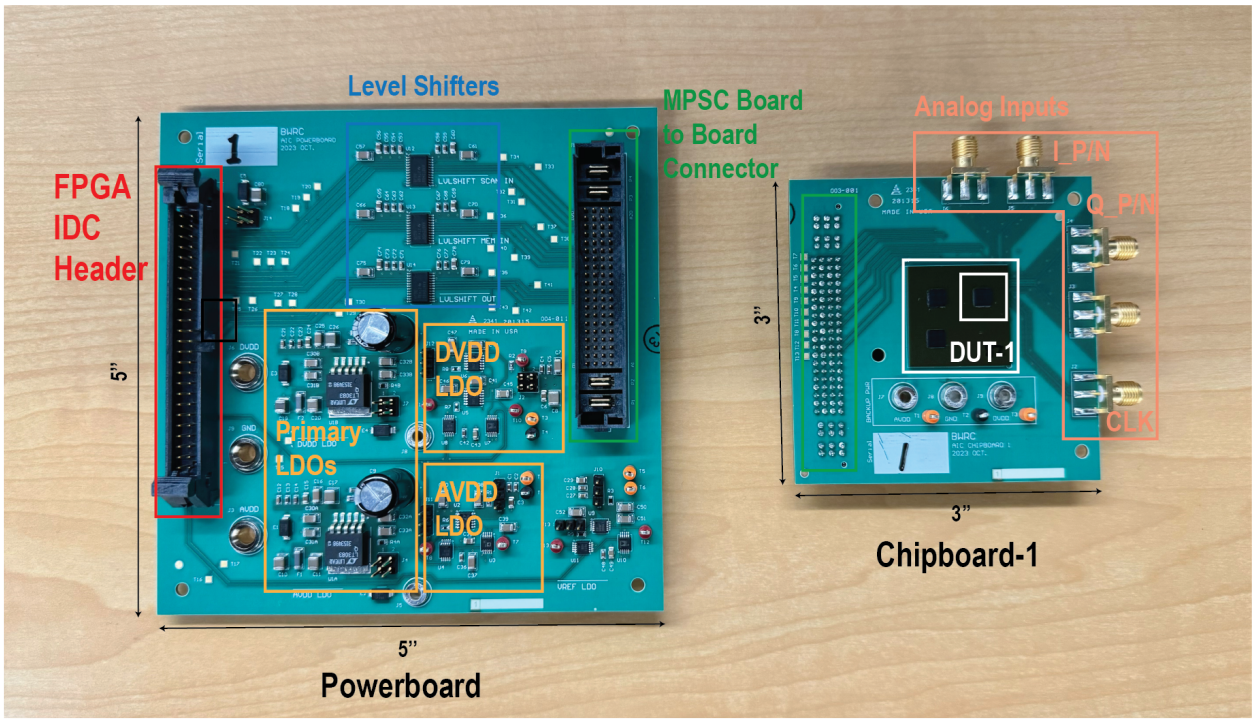


Figure 5.3: Test PCB for DUT-1

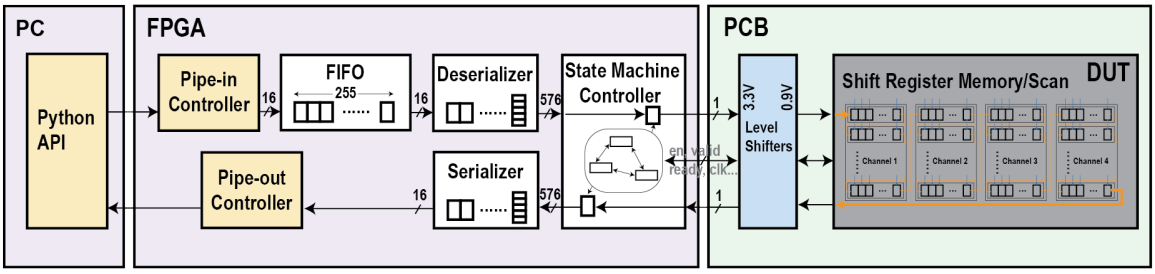


Figure 5.4: Digital Interface showing serial-in and serial-out datapath.

controlled by the state machine. The PC communicates with the FPGA using the provided Python API [52]. The Verilog modules, colored in white, are customized for this testing infrastructure.

5.2 Beamformer Test Setup

5.2.1 Design Under Test

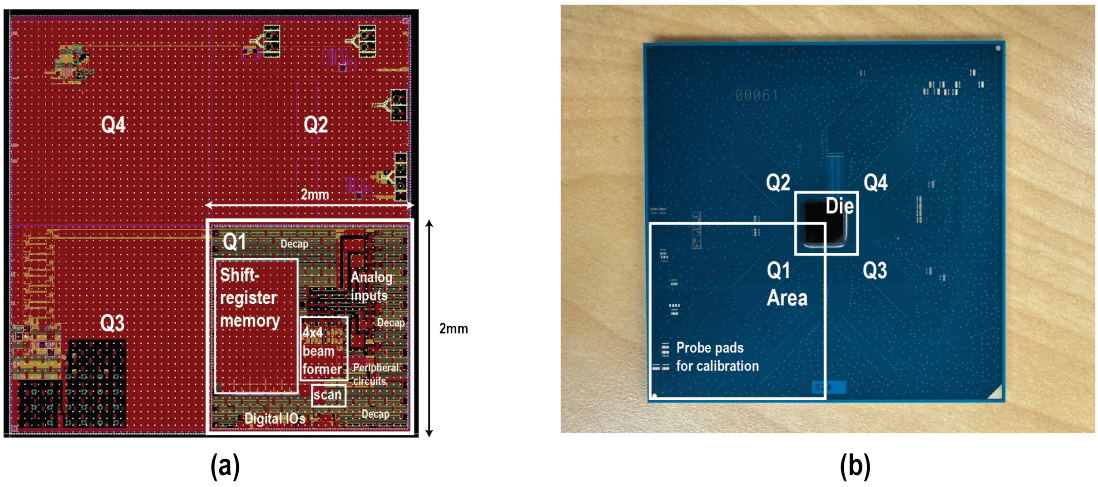


Figure 5.5: Design under test (DUT-2) (a) Beamformer chip top-level layout screenshot. (b) package top-view.

The proposed 4-channel beamformer was taped out in Q2 2023 and used Intel 16 technology as well. This chip will be referred to as DUT-2. Similar to the previous tape out, this shuttle contains four different projects. The $4 \times 4\text{mm}^2$ chip has rotational symmetry, and each quadrant has its power domains. As shown in Fig. 5.5 (a), the design is in the lower right corner. Fig. 5.5 (b) shows the package with a single die in the center. The die was flipped along the y-axis during package assembly and attached to the package. A customized socket by Ironwood is designed for the package. The elastomer socket can support signals up to 40GHz [53]. Using a socket allows testing multiple chips with a single PCB, which reduces the PCB cost and provides flexibility for our testing.

5.2.2 Test Plan

The testing architecture of DUT-2 is similar to DUT-1, as shown in Fig. 5.6. Since DUT-2 contains a 4×4 beamformer, four differential I/Q correlated inputs are needed. The required inputs can be generated in two different ways for separate purposes. For quick bringing up, calibration, debugging the hardware/software, or measuring single-user performance, the simpler 4-channel correlated signals are generated on PCB. The single channel or single-tone

input is provided by a signal generator and split by a one-to-four power splitter for impedance matching. The following voltage-controlled phase-shifting components delay each channel according to the desired AoA. For multi-user tests, a 4-channel arbitrary waveform generator (AWG) can directly generate and provide the required inputs collected by antennas. Selecting from two modes requires a multiplexer (MUX) option on board, which is realized by SMA connectors and short coax cables.

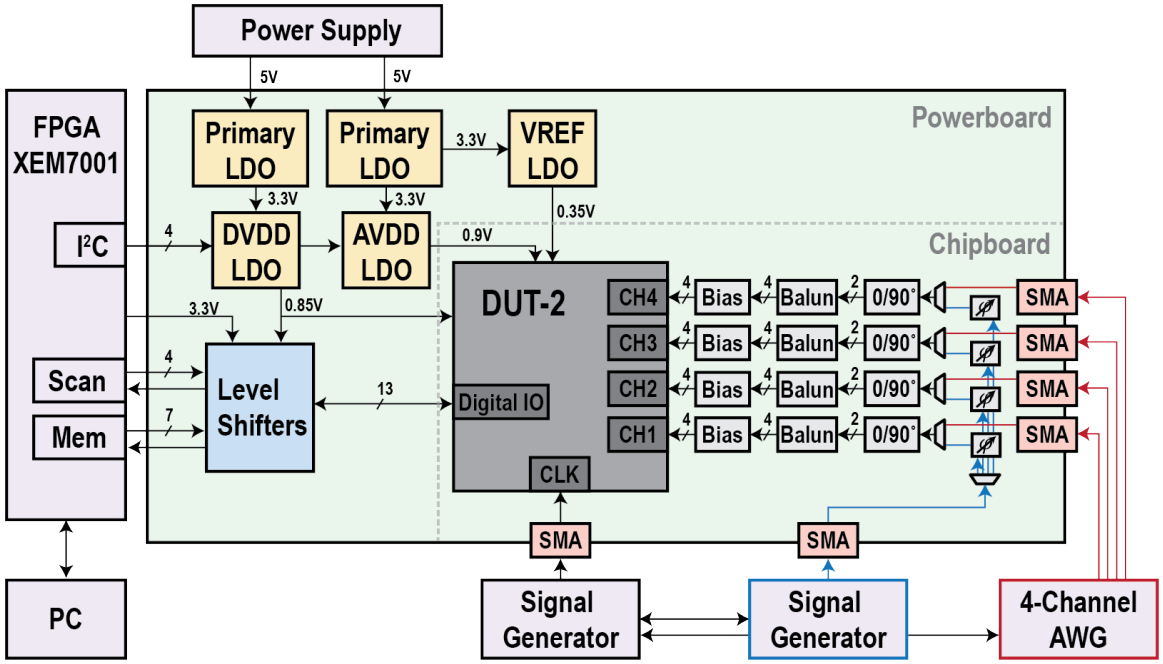


Figure 5.6: High-level test plan for DUT-2.

5.2.3 Test PCB

Fig. 5.7 shows the test PCB for DUT-2. As detailed in Section 5.1.3, the powerboard is designed with redundancy, which can provide the additional IOs required by chipboard 2. The same MPSC board-to-board connector is used on chipboard 2. The signal traces are carefully routed, and the length discrepancy is kept to within 1% to enhance signal integrity. The surface-mounted SMAs are used as mux gates. Short SMA female-to-female cables are used as board jumpers when testing single input. For multi-user parallel input, the SMAs connect directly to an AWG, and the right side of the board is not utilized. The use of a customized socket significantly boosts the chipboard's reusability, leading to cost savings for both the PCB and components.

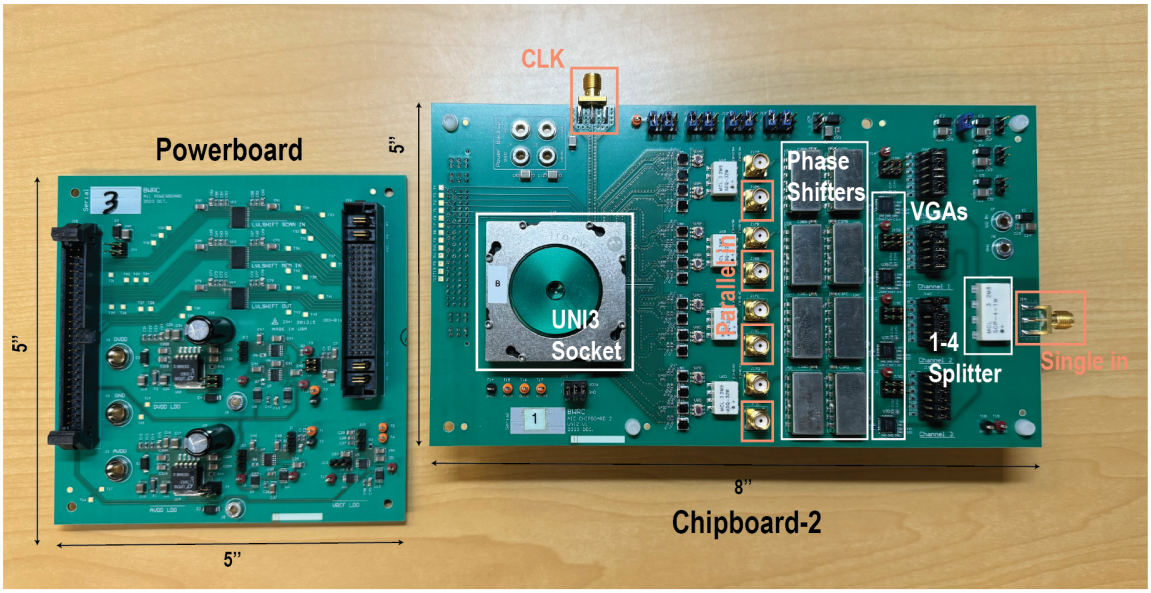


Figure 5.7: Test PCB for DUT-2.

5.3 ADC Performance Measurements

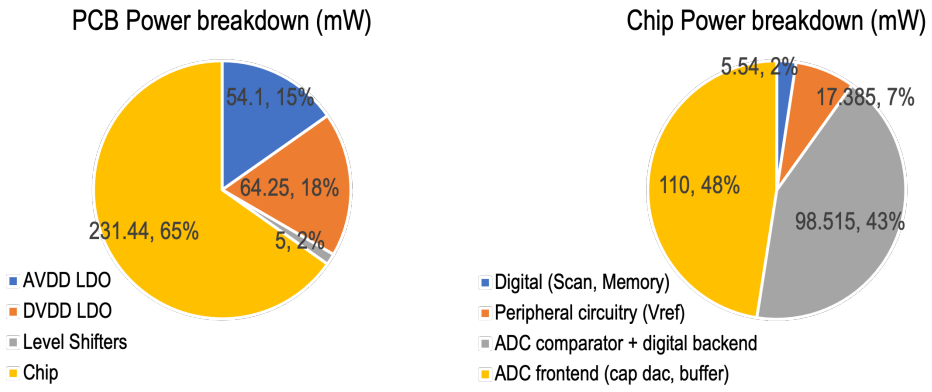


Figure 5.8: Measured PCB power and chip power.

Fig. 5.8 shows the measured power. The ADC front-end and back-end can be measured separately by turning on or off the sampling clock and activating or deactivating the capacitor bank. The power is measured when ADC is sampling at 250MHz.

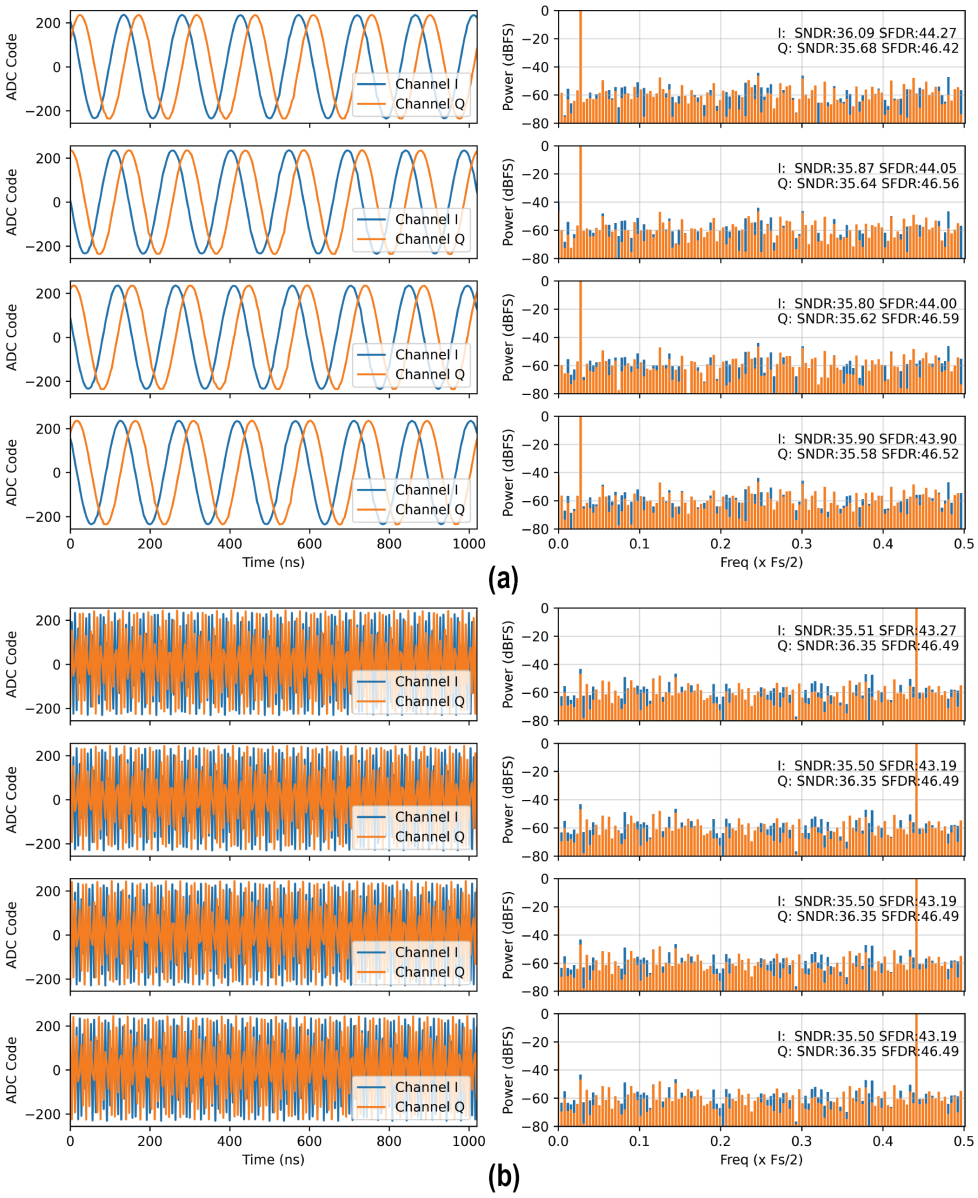


Figure 5.9: Measured time-domain waveform and 256-point FFT.

Fig. 5.9 shows the measured performance for four beamformer ADCs placed on the chip. All four channel inputs are shorted together to test each beamformer like two regular data

converters. The time-domain data is directly captured by the shift register memory on the chip and then read out by batch through the serial output to FPGA. The left part of the figure shows the digital code versus time with only common mode alignment. The right part of the figure is the real-time 256-point FFT result, which is limited by the on-chip memory depth. Fig. 5.9 (a) shows the low-frequency input, where $F_{sig} = 6.83\text{MHz} = 7/256F_S$. The best SNDR is 36.1dB, and the SFDR is 46.7 dB. Fig. 5.9 (b) shows the results with near Nyquist frequency single-tone input at $F_{sig} = 110.35\text{MHz} = 113/256F_S$. The measured results have 35.5 dB SNDR and 46.9 dB SFDR. Using a differential topology suppressed the even-order harmonics, improving the SFDR. However, due to the limited memory depth, we cannot capture longer continuous real-time outputs to reveal higher-order harmonics in the spectrum. Consequently, the higher noise floor contributes to the harmonic bins, resulting in inaccurate calculations.

5.4 Beamformer Measurements

5.4.1 Test Setup

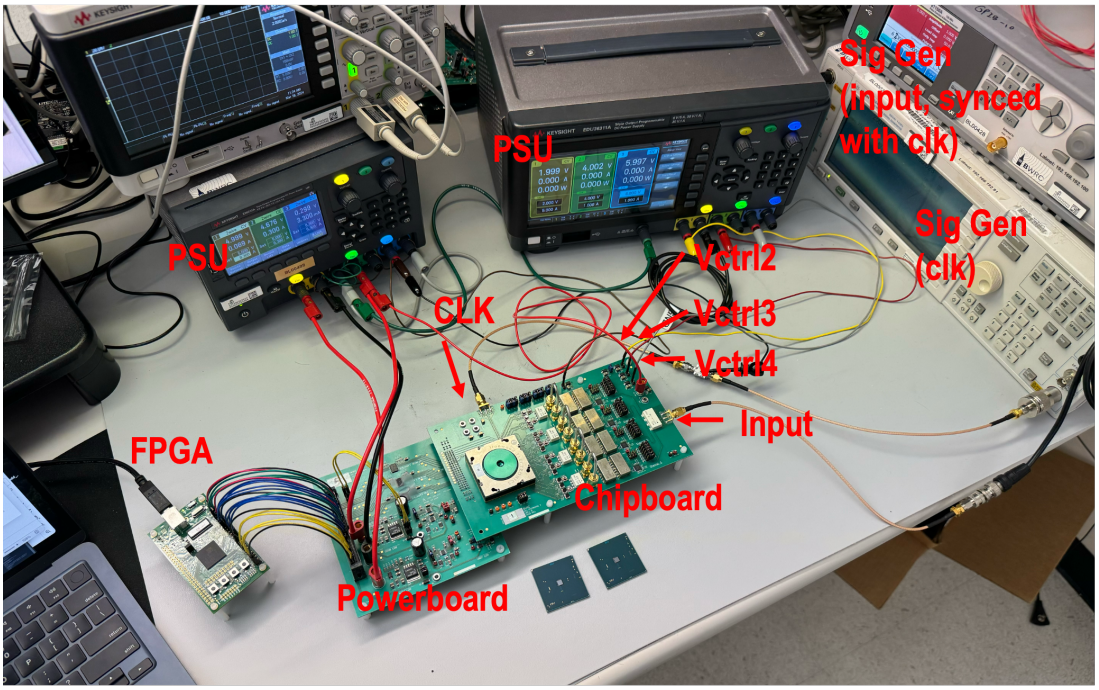


Figure 5.10: Test setup for single user beamformer measurement.

Fig. 5.10 demonstrates the beamformer test setup. One power supply unit (PSU) provides `AVDD` LDO, `DVDD` LDO, and DC biasing voltage for the main clock. $\texttt{V}_{\texttt{ctrl1}}$ is always set

to GND, meaning no phase shift is applied to the first channel. The second PSU sets $V_{ctrl2-4}$. The oscilloscope verifies the phase difference between channels. The signal generator for the input signal is synchronized with the main clock. The read and write control, the capacitor DAC programming, calibration, and tuning are performed by setting scan chain values through the command line from a PC.

5.4.2 Measurement Results

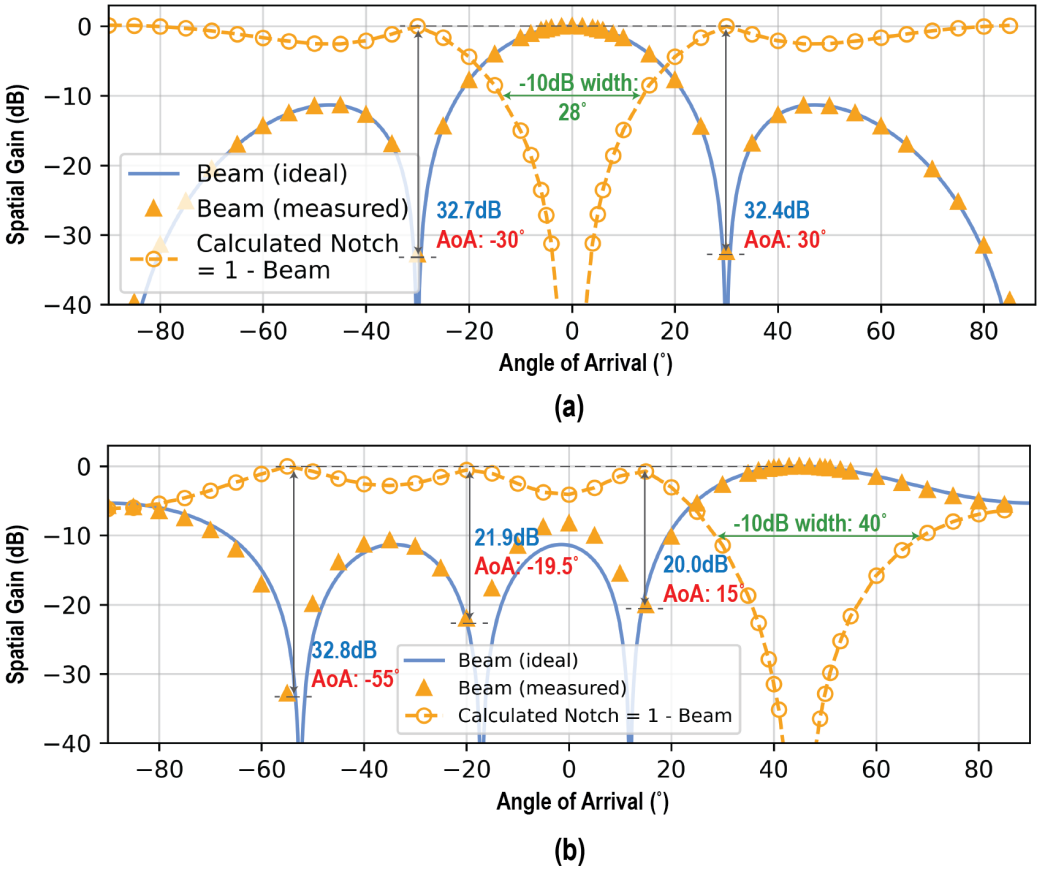


Figure 5.11: Measured spatial gain with normalized RMS power. (a) Center at 0° (b) Center at 45°.

Fig. 5.11 displays the measured spatial gain without calibration when the beamformer is programmed to center at 0° and 45°, respectively,. Each data point is the average normalized RMS power of 10 independent measurements. The figure shows that the spatial gain matches the ideal shape well. When centered at 0°, all the capacitor control code is 0. Fig. 5.11 (a)

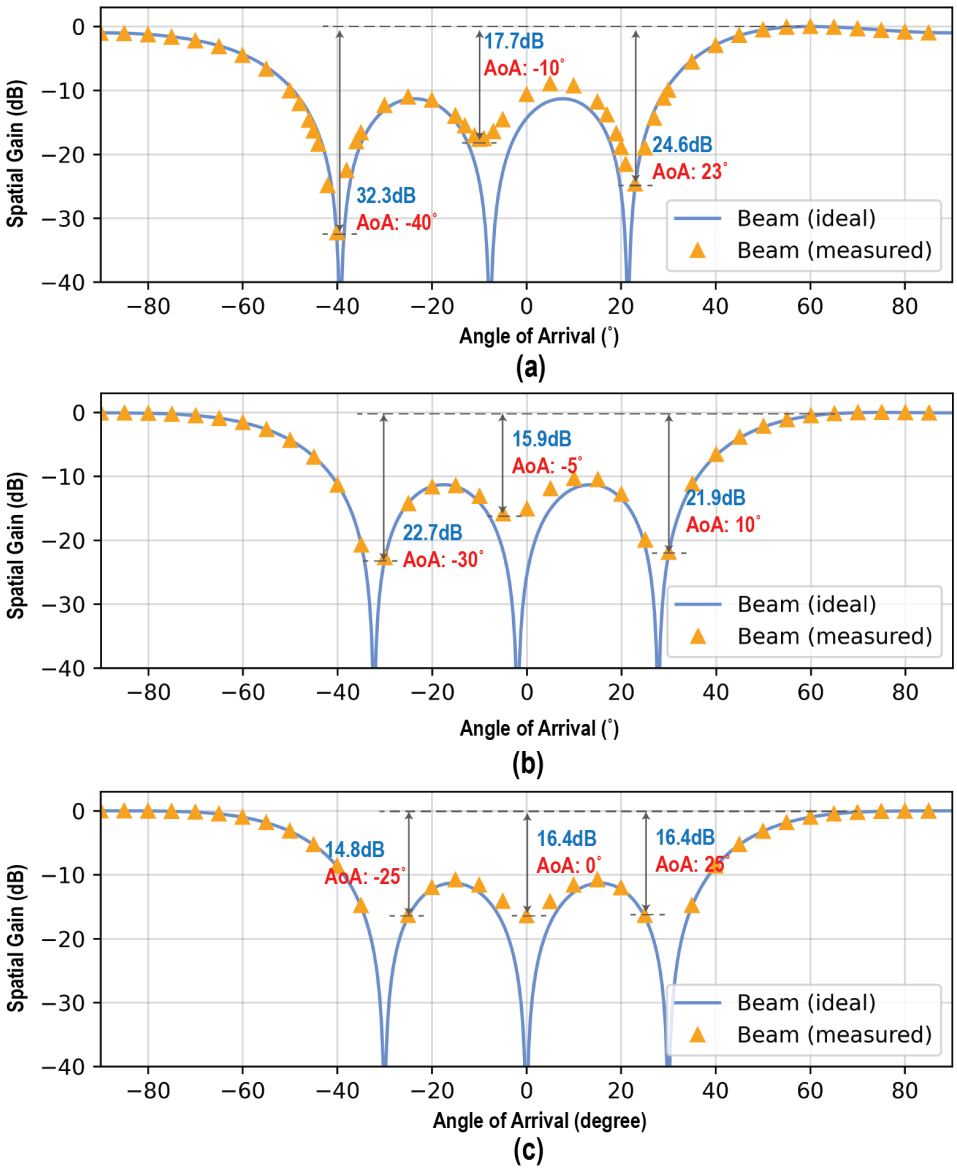


Figure 5.12: More measured spatial gain center at (a) 60°(b) 75°(c) 90°.

shows that two adjacent nulls have over 32 dB attenuation at -30° and 30°, and the null at 90° is over 40 dB. When the beamformer points at 45°, three nulls are still observable, but the shape is slightly mismatched because of the gain mismatch by capacitor flipping. The following subsection will elaborate on this effect and propose an on-chip calibration method. Fig. 5.12 shows more measurement results when the beamformer is set at 60°, 75°, and 90°.

Similarly, the notch depths are less ideal, while the maximum gain location of the beam matches well with the ideal case.

5.4.3 On-chip Calibration

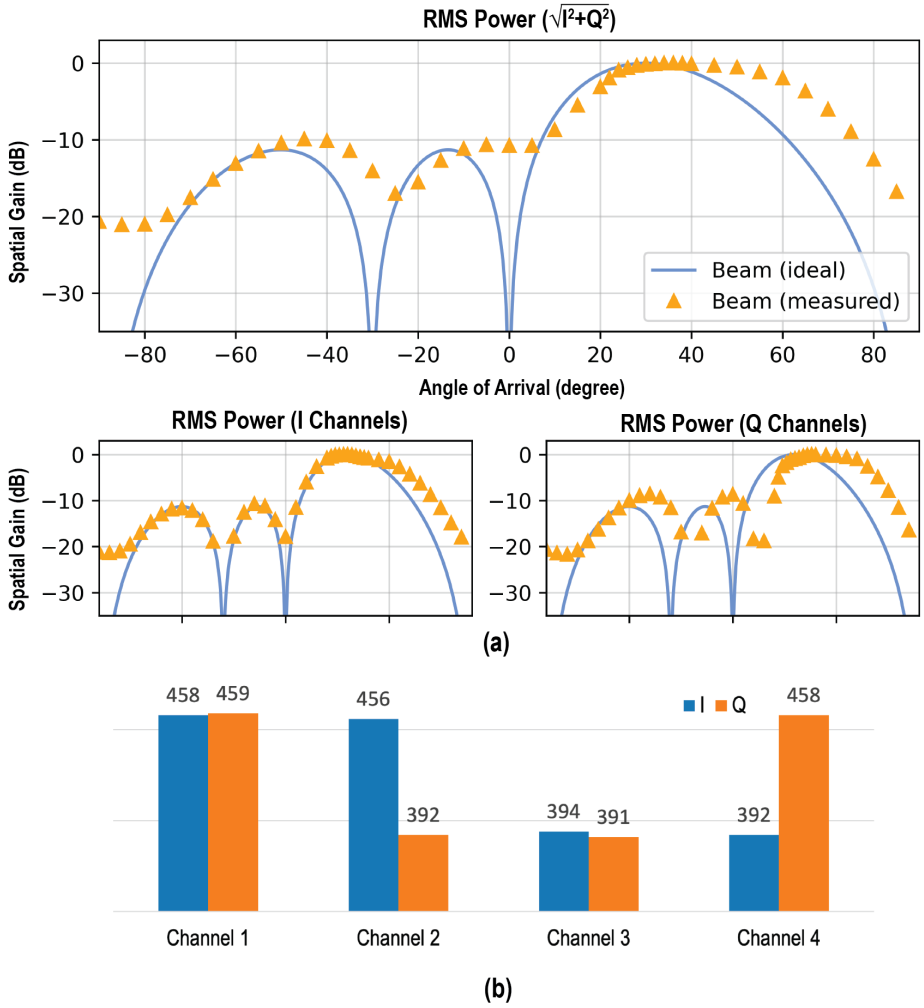


Figure 5.13: Non-ideal beam shape caused by channel gain mismatch. (a) Beamforming results for I and Q channels separately. Some of the notches are less attenuated or shifted. (b) Averaged maximum swing for each channel

The programmable capacitor DAC also provides on-chip calibration capability. We observe from the measurements that when the reversed unit capacitor ratio is unbalanced, the gain offset is large and cannot be compensated externally from the input side. In the worst

case, all capacitors sample reversely in some channels, while in the other channels, no capacitor is reversed. Fig. 5.13 (a) shows this effect. We can see that when the angle of arrival is 30°, the three spatial notches are not apparent because the location of the notch is shifted. Appendix A.1 includes the capacitor DAC control code at 30°.

Since the capacitor DAC is highly programmable, we can intentionally reverse part of the capacitor to match the gain with the minimum channel after finding each signal strength. For example, in Fig. 5.13 (b), $\text{channel}_{3,\,Q}$ has the minimum amplitude because all the capacitor unit is reversed and result in charge loss. We apply a calibration ratio to all other channels to align with this minimum gain by reversing a small portion of capacitors in the sampling phase. This calibration will slightly drop gain, depending on the channel mismatch. Fig. 5.14 shows the calibration results. Compared to the pre-calibration result, three spatial notches are over 32dB with only a 1.31dB gain drop. Setting the beam center at 30 °is already the maximum possible mismatch. Appendix A.2 shows the updated control code with calibration.

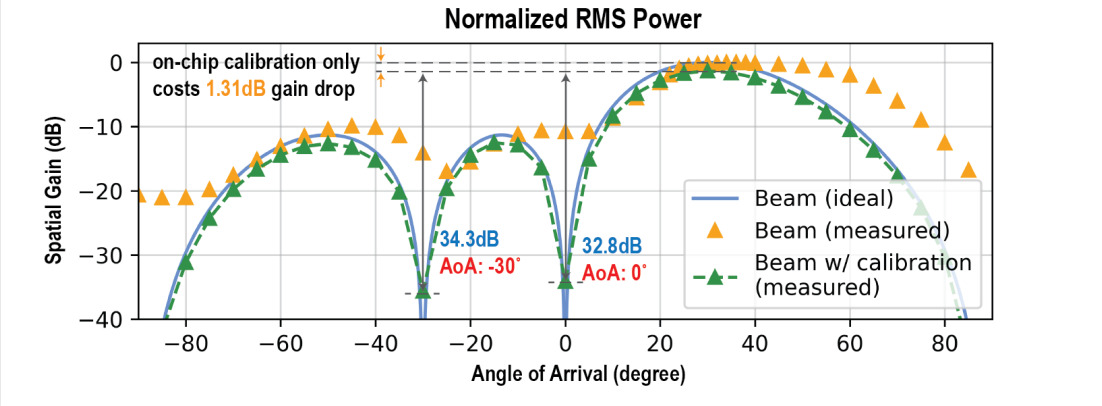


Figure 5.14: On-chip calibration improvement for 30°angle of arrival

5.4.4 Comparison with State-of-the-Art

Table 5.1 shows the comparison table for our proposed beamformer with the state-of-the-art published work. Our design integrates a 4×4 beamformer into the ADC layer, resulting in a compact, power-efficient, flexible system with high spatial resolution. The beamformer is fully passive, which enables good linearity. Each beamformer can be programmed arbitrarily from 0-180°and consumes 52.1mW. It is important to note that most designs do not have integrated data converters on-chip, making direct comparisons with our work challenging. The proposed ADC-integrated beamformer can also be applied with other spatial notch solutions. The limitation of our design is that the beamformer operates in an open-loop configuration, requiring information about the incoming signal. Extending it to a closed-loop form is feasible, but the steering speed would depend on the digital module and algorithm.

	This work	JSSC'21 [12]	JSSC'17 [54]	ISSCC'22 [55]	ISSCC'19 [11]	ISSCC'18 [56]	ISSCC'20 [57]	JSSC'17 [58]
Architecture	**MIMO beam-former ADC**	MIMO beam-former	MIMO beam-former	MIMO mmWave SNF	MIMO Array-based SNF	MIMO SSA	MIMO SNF	MIMO SNF
Beamforming Type	**Analog**	Analog	Analog	Digital	Digital	Digital	Digital	Digital
Technology	**16nm FFT**	22nm FD-SOI	65nm CMOS	40nm CMOS	45nm CMOS	130nm SiGe BiCMOS	65nm CMOS	65nm CMOS
Frequency (GHz)	**0.1-0.5**	0.7-5.7	1-2.5	23-29	27-41	22-30	28	0.1-3.1
Gain (dB)	**-**	41	12	30	36	33	16	43
No. of Inputs/Outputs	**4/4**	4/4	4/4	4/4	4/4	8/2	4/4	4/4
Spatial Suppression in IF (dB) (1/2/3 SNF notches)	33	20(16)	20	35(40)/ no/no	62/50/51	54/41/no	37/no/no	24/no/no
Minimum $> 10dB$ Cancellation Notch Width (°)	28-40	N/A	N/A	8.5-14/ 22-24	27-32	48-58	11/22	27
Blocker/Signal AOI Difference in Measurement (°)	0-180	N/A	N/A	26	30	30	N/A	N/A
Power /RX Element (mW)	52.1	19-35	6.5-9	56.1	70-85	70	112.4	29-37
Chip Area (mm^2)	0.165	0.52	0.2	2.8	23.4	21.6	10.6	2.25

Table 5.1: Comparison with state of the art.

Chapter 6

Conclusion and Future Work

6.1 Summary

In this dissertation, we present a novel method for performing baseband beamforming. Two critical components, the phase shifter and the beamformer, are implemented using programmable switched capacitors and efficiently integrated with the SAR ADC, eliminating the need for additional components in the gain path. This approach provides significant advantages in achieving accurate phase adjustment and spatial resolution while incurring minimal area and power overhead. Two prototypes have been taped out using advanced technology. The chips were successfully tested and achieved the state performance.

6.2 Key results

In this thesis, we introduce a novel baseband beamforming method, outlining the key contributions as follows:

1. **Accurate Phase Shifter:** We proposed, analyzed, and taped out a switch capacitor-based phase shifter integrated with SAR ADC. This phase shifter offers highly accurate phase resolution using existing hardware.

2. **Beamformer Integrated with SAR ADC** We also proposed, analyzed, and taped out a baseband beamformer utilizing the aforementioned phase shifter. This beamformer demonstrates well-matched spatial gain. Additionally, we discovered and verified an on-chip calibration method.

The advantages of our proposed beamformer include the following:

1. **Area Efficiency:** The design is compact. It integrates within the SAR ADC and requires only minor modifications to the existing hardware.

2. **High Spatial Resolution:** The use of fully passive charge domain beamforming allows high spatial resolution.

3. **Compatibility:** Our beamformer design is compatible with other spatial notch filter designs.

4. **Technology Scalability:** The MOM Capacitor and SAR back-end components scale effectively with technological advancements.

6.3 Future Work

6.3.1 Performance Improvement

Our prototype is based on a baseline SAR ADC. The SAR ADC is fully generated by BAG Laygo space, and many sub-modules are adapted and reused for our proposed phase shifter and beamformer. We can explore improvements to the SAR ADC design to enhance throughput, such as developing a faster back-end or employing a different comparator typology. Additionally, a time-interleaved architecture shows promise for greatly increasing the ADC throughput and is compatible with our design.

The primary limitation of increasing the sampling clock frequency is the presence of layout non-idealities and challenges in clock distribution. The channel phase shifter is arranged horizontally in our design, leading to long charge-sharing traces. To mitigate this issue, we can relocate non-critical signal control components, such as unit capacitor programming gates, away from the channel module. This adjustment has the potential to significantly reduce the x-axis dimension of the layout and improve the performance.

Inserting a topside switch array adds an extra transistor in the signal path, which degrades the sampler's performance. Alternatively, combining the sampler with the plate-selecting logic could eliminate the need for the additional switch and potentially enhance the sampler's signal-to-noise ratio (SNR).

6.3.2 Extension to SNF without Gain Loss

Similar to other voltage domain or current domain spatial notch designs, once the beam from a particular direction is obtained, it can be subtracted from each channel to create a spatial notch. In Equation 4.3, adding an additional capacitor unit equal to the total beamformer capacitance in each channel can prevent gain loss. Alternatively, providing flexibility for each capacitor DAC to sample from any channel can be considered. However, it can be expected that this approach poses greater layout challenges.

6.3.3 Beamformer Scalability

In this study, we demonstrate a 4×4 beamformer designed for inputs from a 4×1 antenna array. The specific shape of the antenna array is not crucial. For instance, if the inputs are from a 2×2 antenna array, adjusting the coefficient term that represents the capacitor allocation is sufficient. Moreover, with careful design and layout optimization, we expect that scaling up the proposed beamformer to support 16-32 antennas is feasible.

6.3.4 Closed-loop Beamforming

The beamformer implemented in this work operates in an open-loop configuration. We assume that the signal's angle of arrival is known by calculation or provided as prior information, allowing us to configure the capacitor array accordingly. However, in real-world scenarios, a closed-loop configuration is often preferred due to rapid changes in the network. Implementing a beam search DSP for capacitor programming would be a meaningful effort. Spatial sensing and blocker detection in the front-end is also an intriguing topic, as it can provide valuable information for analog components. A low-power, low-resolution beamformer can be used as a detector for spatial content. Scaling down our design holds promise for serving this purpose effectively.

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Appendix A

Chapter 5 Supplementary Material

A.1 Capacitor DAC Control (Before Calibration)

```
// -------------------- Capacitor DAC Control Code ------------------------
// Configuration for AoA=30 degree
Angle of arrival:  30.0
Phase shift for antenna array: [ 1.+0.j  0.-1.j -1.-0.j -0.+1.j]

Channel 1: 0.0 degree
Gain compensation: 1.000
Capacitor assignment: C1: 512  C2:   0
T_I code: 00000000, T_Q code 00000000
R_I code: 00000000, R_Q code 00000000

Channel 2: 270.0 degree
Gain compensation: 1.000
Capacitor assignment: C1:   0  C2: 512
T_I code: 11111111, T_Q code 11111111
R_I code: 00000000, R_Q code 11111111

Channel 3: 180.0 degree
Gain compensation: 1.000
Capacitor assignment: C1: 512  C2:   0
T_I code: 00000000, T_Q code 00000000
R_I code: 11111111, R_Q code 11111111

Channel 4: 90.0 degree
Gain compensation: 1.000
Capacitor assignment: C1:   0  C2: 512
```

```
T_I code: 11111111, T_Q code 11111111
R_I code: 11111111, R_Q code 00000000
// ---------------------------------------------------------------------
```

A.2 Capacitor DAC Control (After Calibration)

```
// -------------------- Capacitor DAC Control Code ------------------------
// Configuration for AoA=30 degrees with measured calibration ratio
Angle of arrival:  30.0
Phase shift for antenna array: [ 1.+0.j  0.-1.j -1.-0.j -0.+1.j]
Calibration ratio:
 [[0.17 0.17]
 [0.16 0.  ]
 [0.01 0.  ]
 [0.   0.17]]
Channel 1: 0.0 degree
Gain compensation: 1.000
Capacitor assignment: C1: 512  C2:   0
T_I code: 00000000, T_Q code 00000000
R_I code: 00000000, R_Q code 00000000 (w/o calibration)
R_I code: 00101010, R_Q code 00101010 (w/ calibration)

Channel 2: 270.0 degree
Capacitor assignment: Gain compensation: 1.000
C1:   0  C2: 512
T_I code: 11111111, T_Q code 11111111
R_I code: 00000000, R_Q code 11111111 (w/o calibration)
R_I code: 00101001, R_Q code 11111110 (w/ calibration)

Channel 3: 180.0 degree
Gain compensation: 1.000
Capacitor assignment: C1: 512  C2:   0
T_I code: 00000000, T_Q code 00000000
R_I code: 11111111, R_Q code 11111111 (w/o calibration)
R_I code: 11111100, R_Q code 11111111 (w/ calibration)

Channel 4: 90.0 degree
Gain compensation: 1.000
Capacitor assignment: C1:   0  C2: 512
T_I code: 11111111, T_Q code 11111111
R_I code: 11111111, R_Q code 00000000 (w/o calibration)
```

```
R_I code: 11111110, R_Q code 00101010 (w/ calibration)
// ---------------------------------------------------------------------
```