On May 4, 2011, Intel Corporation announced what it called the most radical shift in semiconductor technology in 50 years.

A new 3-dimensional transistor design will enable the production of integrated-circuit chips that operate faster with less power…

THE WALL STREET JOURNAL. * * * * Thursday, May 5, 2011

CORPORATE NEWS

Intel Rethinks Chip's Building Blocks

By Don Clark

Intel Corp. showed off what it called the most radical shift in semiconductor technology in more than fifty years, a design that could produce more powerful chips for gadgets without taxing their batteries.

The company plans to change a key part of each chip into a vertical, fin-like structure, a similar principle to the way high-rise buildings pack more office space in a city. The parts being changed—transistors—are the building block of nearly all electronic products; today's microchips can contain billions of the tiny switching elements.

Intel said its latest technology could bring more computing power to smartphones and tablet computers as well as speed up corporate data centers—all while sharply reducing power consumption.

Though rivals also have been exploring similar technologies, Intel is the first to commit to using the so-called 3-D approach in high-volume production, a gamble that analysts said could help Intel match the performance advantages of rivals that have largely kept Intel's chips out of the smartphone market.

"We've been talking about these 3-D circuits for more than 10 years, but no one has had the confidence to move them into manufacturing," said Dan Hutcheson, a chip-manufacturing specialist with the firm VLSI Research.

Intel executives demonstrated working chips based on the new approach at a gathering Wednesday in San Francisco. They indicated the first microprocessors would likely be targeted for high-end desktop computers and server systems and arrive in early 2012.

For decades, chip manufacturers have raced to shrink the size of components, which increases the performance of chips while decreasing the cost of each computing function. Competition has spurred companies to introduce ever-smaller processes every couple of years.

Intel executives say the shift to 3-D transistors brings more benefits than simply moving to a new generation of manufacturing technology. For example, if designers keep performance consumption constant, the new technology consumes half the power as Intel's existing production method.

"That is an unprecedented gain," said Mark Bohr, who holds the title of Intel fellow and leads its development of new manufacturing processes. "We've never achieved that kind of performance gain at low voltage."

Chip designers have long worked in more than two dimensions, with transistors topped by layers of interconnecting wiring. Intel's shift relates to a part of each transistor that determines how fast electricity flows and how much current may leak out, affecting power consumption.

Intel engineers replaced a flat channel for conducting electrons with a fin-shaped structure surrounded on three sides by a device called a gate that turns the flow on and off. The three-dimensional shape, Mr. Bohr said, lets more current flow during the "on" state and less current to leak when the transistor is switched "off."

Intel disclosed the underlying approach in research papers in 2002, and has spent the intervening years perfecting it. It has opted to shift completely to the new transistors for its next manufacturing process—slated to create chips with circuit dimensions measured at 22 nanometers, or billionths of a meter. Intel's current chips use 32-nanometer technology.

Departures from conventional manufacturing technologies tend to increase costs, and chip companies try to avoid them. Mr. Bohr said Intel concluded it could move to the new technology with a 2% to 3% increase in the cost of a finished silicon wafer, each of which contains hundreds of chips.

Others are expected to use the approach at some point, too, but not until they have shrunk their circuitry beyond 22 nanometers.

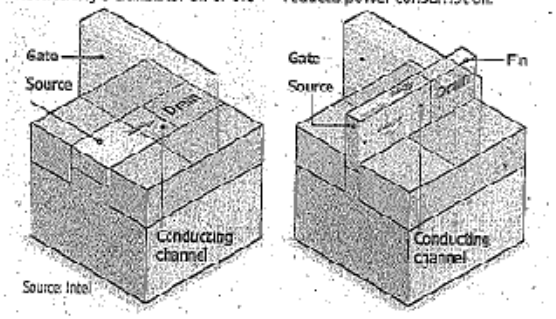
Globalfoundries, a production service spun off from Advanced Micro Devices Inc., said Wednesday it will use conventional transistors for its forthcoming 20-nanometer process. "We don't see the need" for technologies like 3-D transistors until subsequent production processes, a spokesman said.

Intel's Move Into 3-D

The chip maker breaks from conventional approaches to make transistors.

Conventional transistor: Electrons flow between components called a source and a drain, forming a two-dimensional conducting channel. A component called a gate starts and stops the flow, switching a transistor on or off.

Intel's new transistor: A fin-like structure rises above the surface of the transistor with the gate wrapped around it, forming conducting channels on three sides. The design takes less space on a chip, and improves speed and reduces power consumption.



The 3-D Tri-Gate transistor is a variant of the FinFET developed at UC-Berkeley, and will be used in Intel's 22-nm microprocessors.

History and Future of the FinFET

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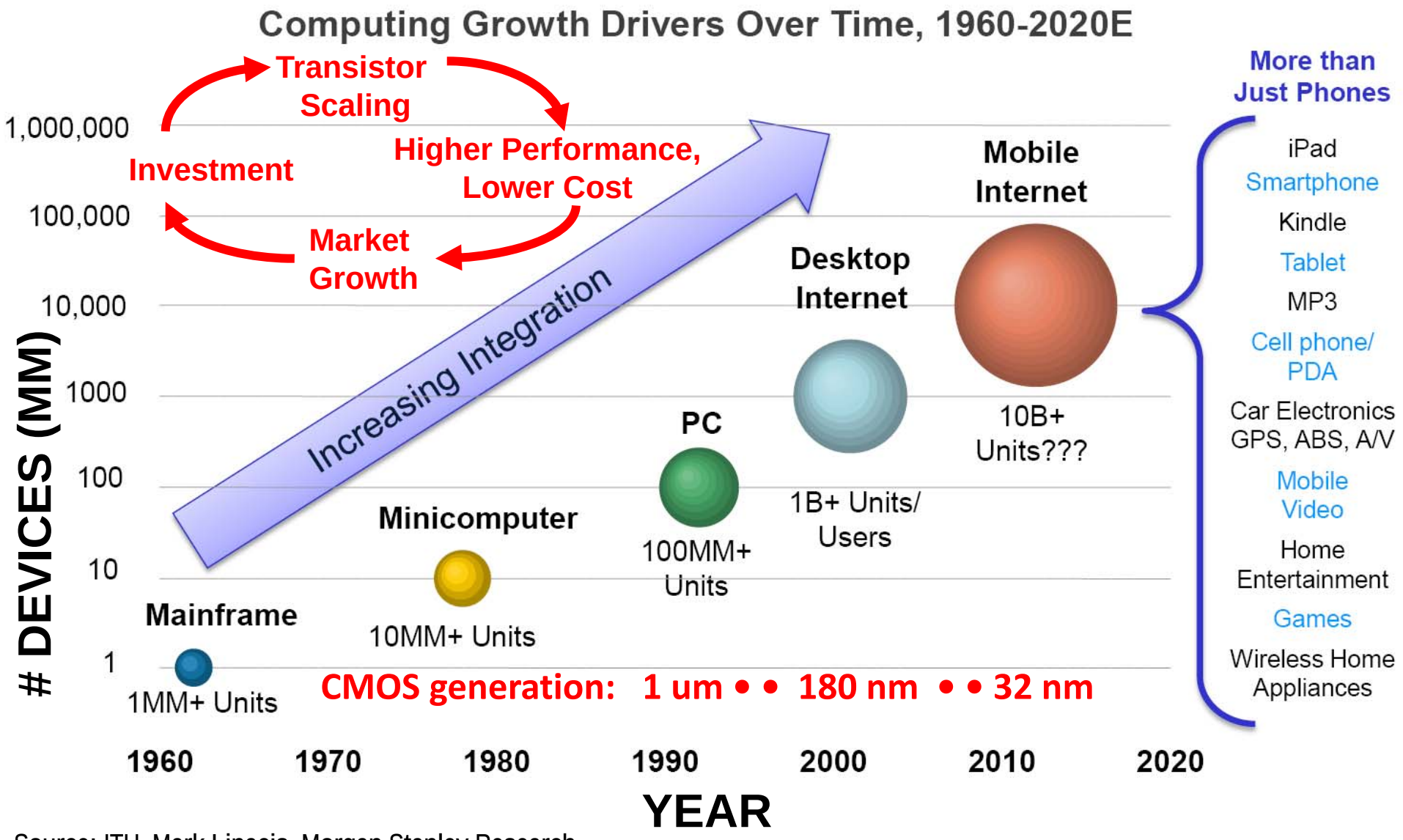
University of California, Berkeley, CA 94720-1770 USA

October 12, 2011

Impact of Moore's Law



Source: ITU, Mark Lipacis, Morgan Stanley Research

1996: The Call from DARPA

- 0.25 μm CMOS technology was state-of-the-art
- DARPA Advanced Microelectronics Program Broad Agency Announcement for 25 nm CMOS technology

1998 International Technology Roadmap for Semiconductors (ITRS)

	1999	2002	2005	2008	2011	2014	2017	2020
Technology Node	180 nm	130 nm	100 nm	70 nm	50 nm	35 nm	25 nm	18 nm
Gate Oxide Thickness, T_{OX} (nm)	1.9-2.5	1.5-1.9	1.0-1.5	0.8-1.2	0.6-0.8	0.5-0.6		
Drive Current, I_{DSAT}	*Solutions being pursued*			*No known solutions*				

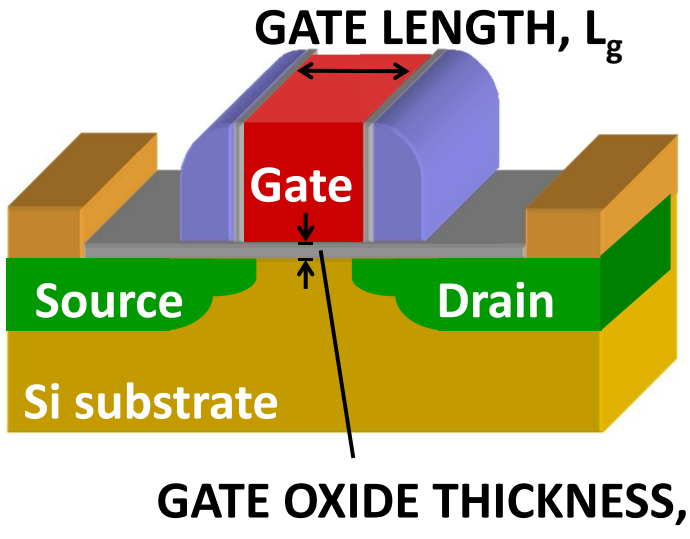
End of Roadmap

→ UC-Berkeley project "Novel Fabrication, Device Structures, and Physics of 25 nm FETs for Terabit-Scale Electronics"

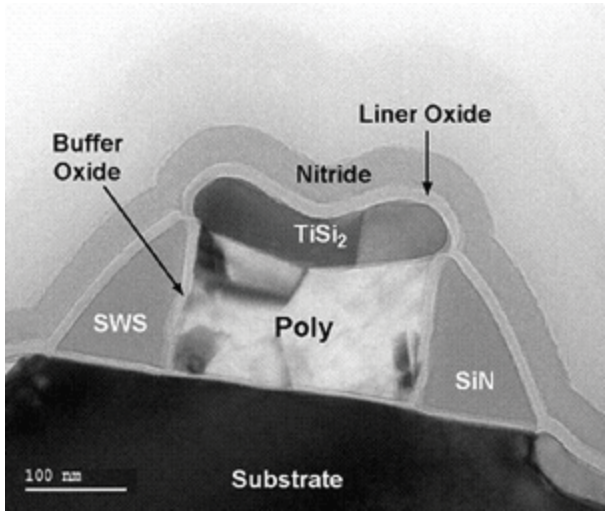
- $5.2M over 4 years (June 1997 through July 2001)

MOSFET Basics

Metal Oxide Semiconductor Field-Effect Transistor:



0.25 micron MOSFET XTEM



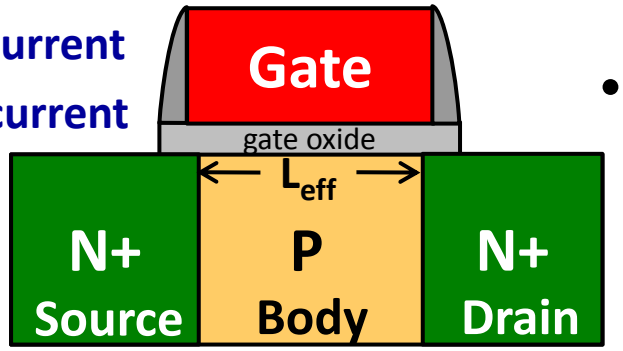
http://www.eetimes.com/design/automotive-design/4003940/LCD-driver-highly-integrated

MOSFET Operation: Gate Control

Desired characteristics:

- High ON current
- Low OFF current

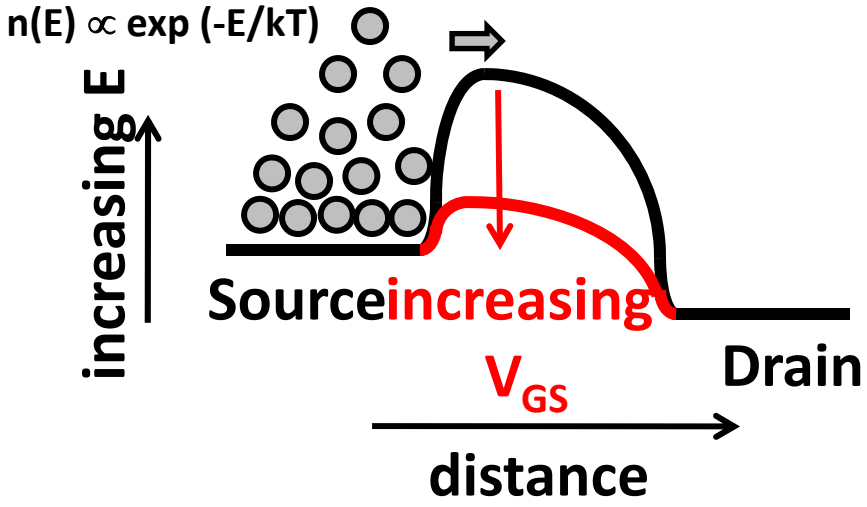
N-channel MOSFET cross-section

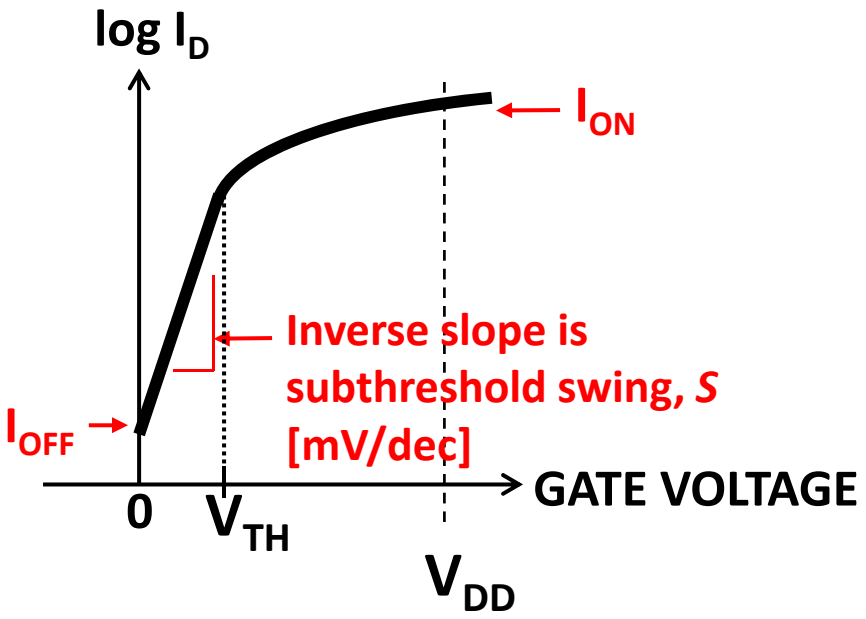


- Current between Source and Drain is controlled by the Gate voltage.
- "N-channel" & "P-channel" MOSFETs operate in a complementary manner

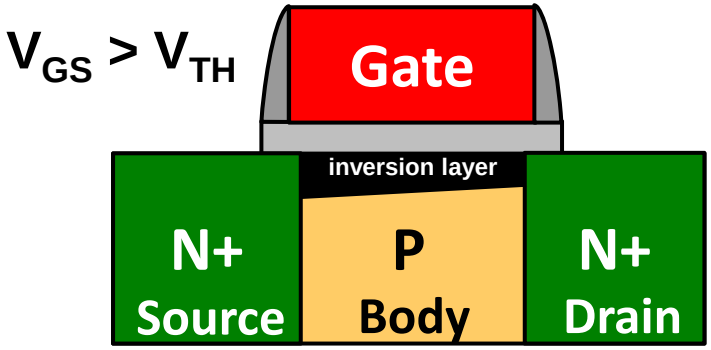
  "CMOS" = Complementary MOS

Electron Energy Band Profile





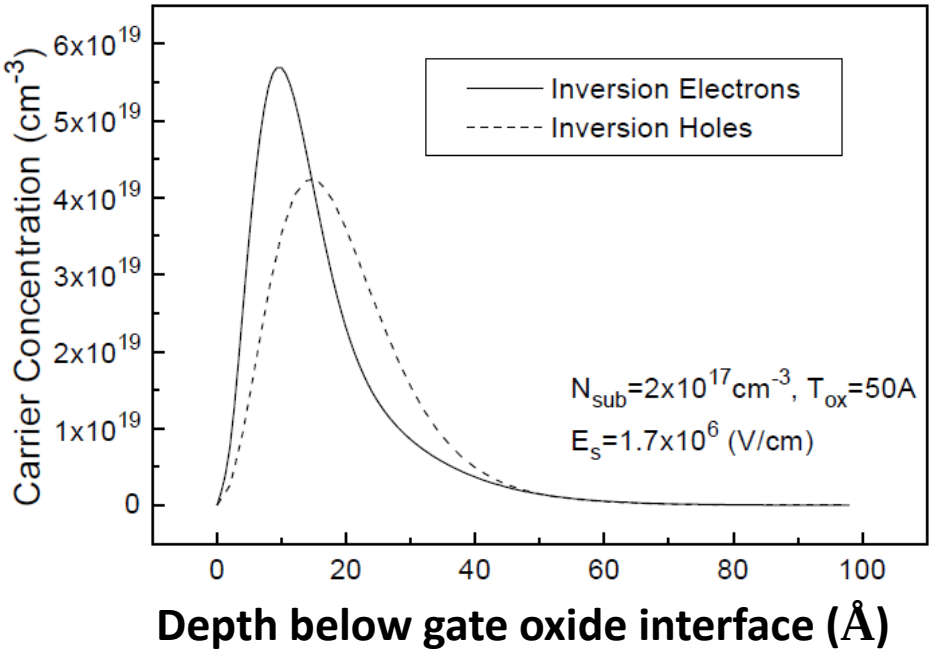
Inversion-Layer Thickness



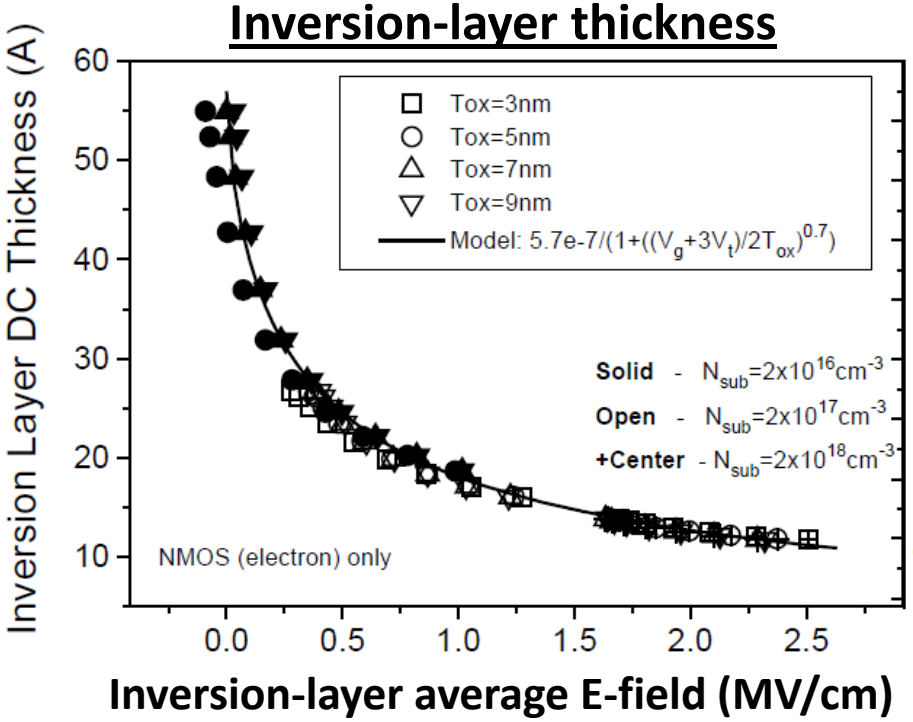
The average depth of the inversion layer below the Si/oxide interface is referred to as the *inversion-layer thickness*.

- **2-3 nm (depending on gate voltage)**

Inversion-layer depth profile

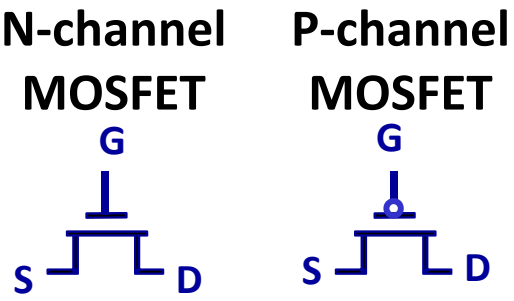


Inversion-layer thickness

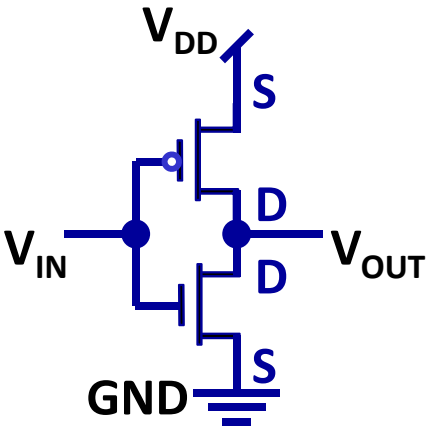


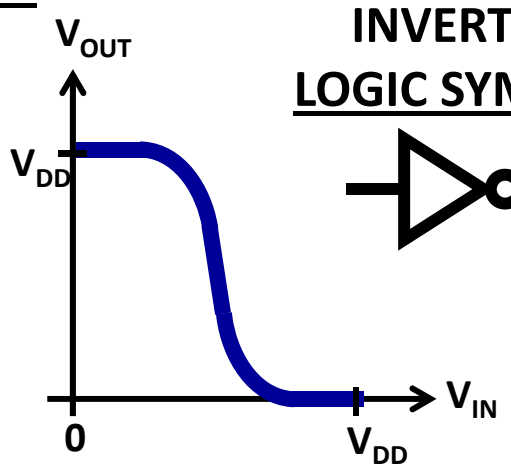
CMOS Devices and Circuits

CIRCUIT SYMBOLS



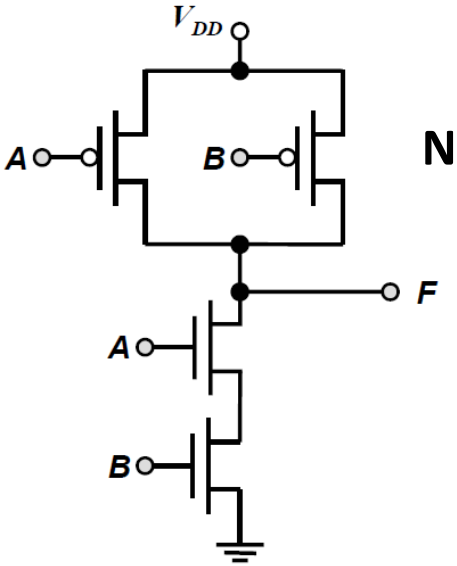
CMOS INVERTER CIRCUIT





INVERTER LOGIC SYMBOL

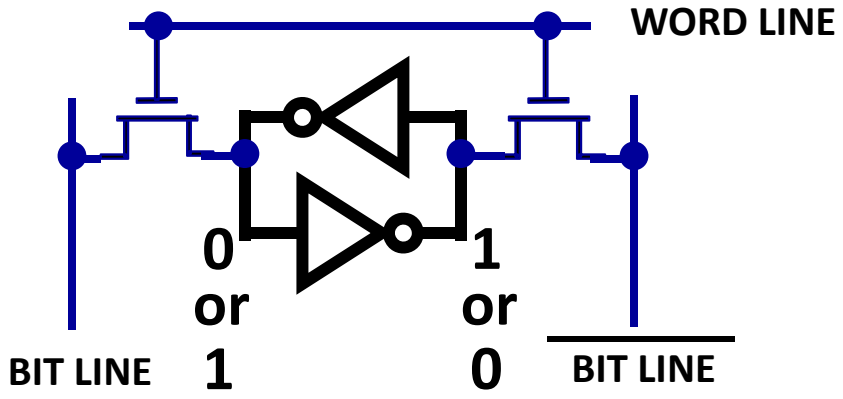
CMOS NAND GATE



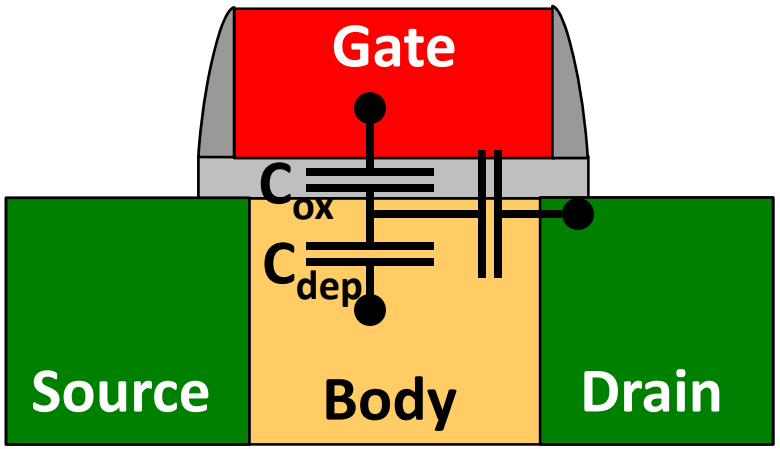
NOT AND (NAND) TRUTH TABLE

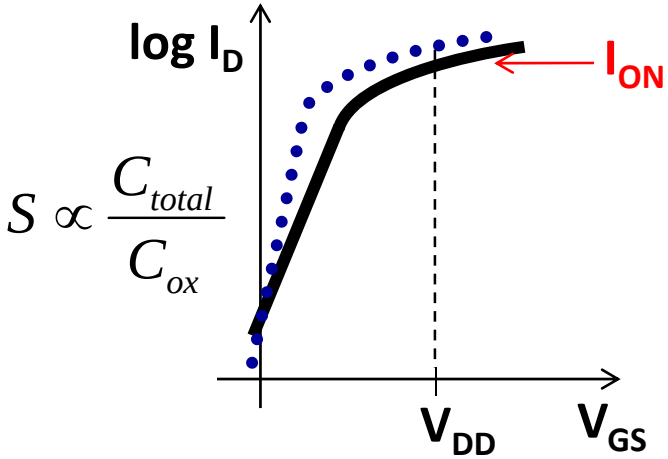
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

STATIC MEMORY (SRAM) CELL



Improving the ON/OFF Current Ratio

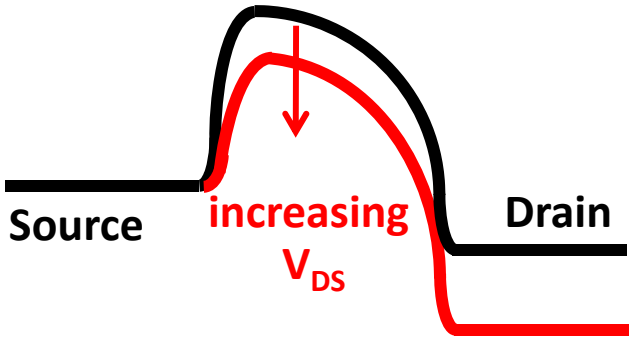


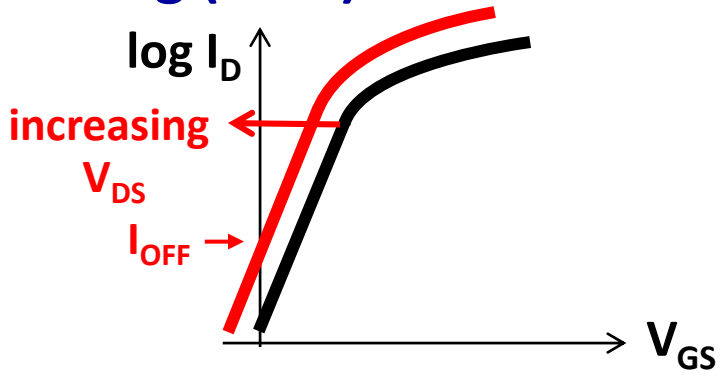


- **The greater the capacitive coupling between Gate and channel, the better control the Gate has over the channel potential.**

  →higher I_{ON}/I_{OFF} for fixed V_{DD}, or lower V_{DD} to achieve target I_{ON}/I_{OFF}

  →reduced drain-induced barrier lowering (DIBL):





MOSFET in ON State ($V_{GS} > V_{TH}$)

width velocity inversion-layer charge density

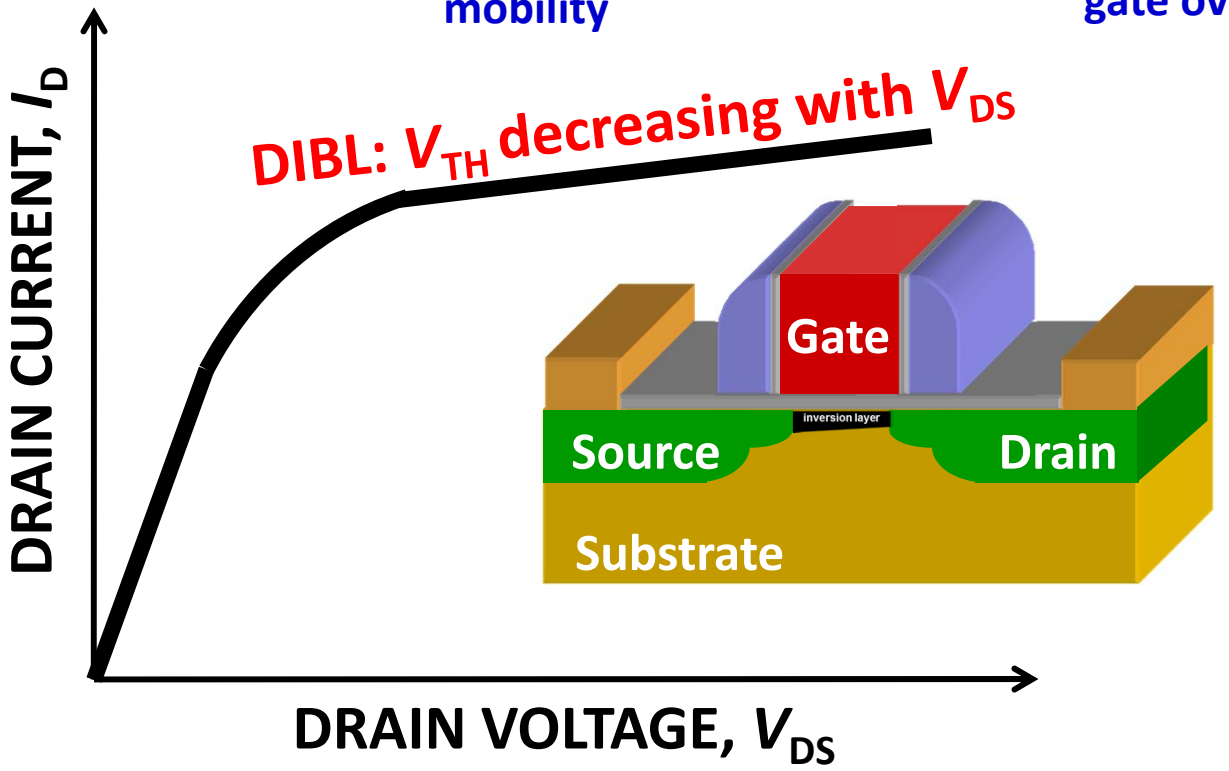
$$I_D = W \times v \times Q_{inv}$$

gate-oxide capacitance

$$v \propto \mu_{eff} \qquad Q_{inv} \propto C_{ox}(V_{GS} - V_{TH})^{\eta}$$

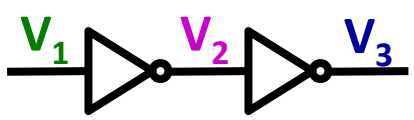
mobility

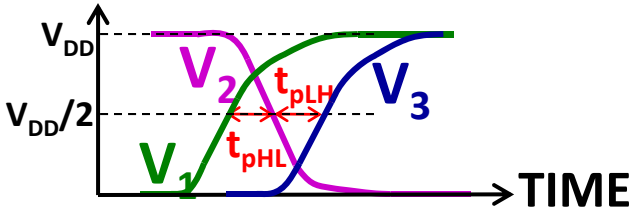
gate overdrive



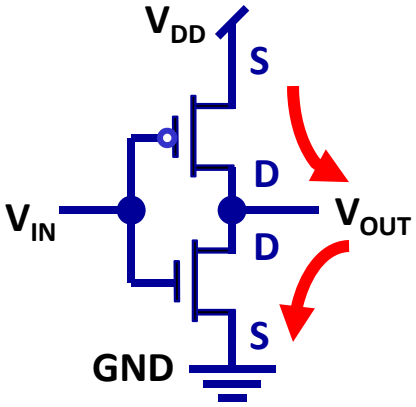
Effective Drive Current (I_{EFF})

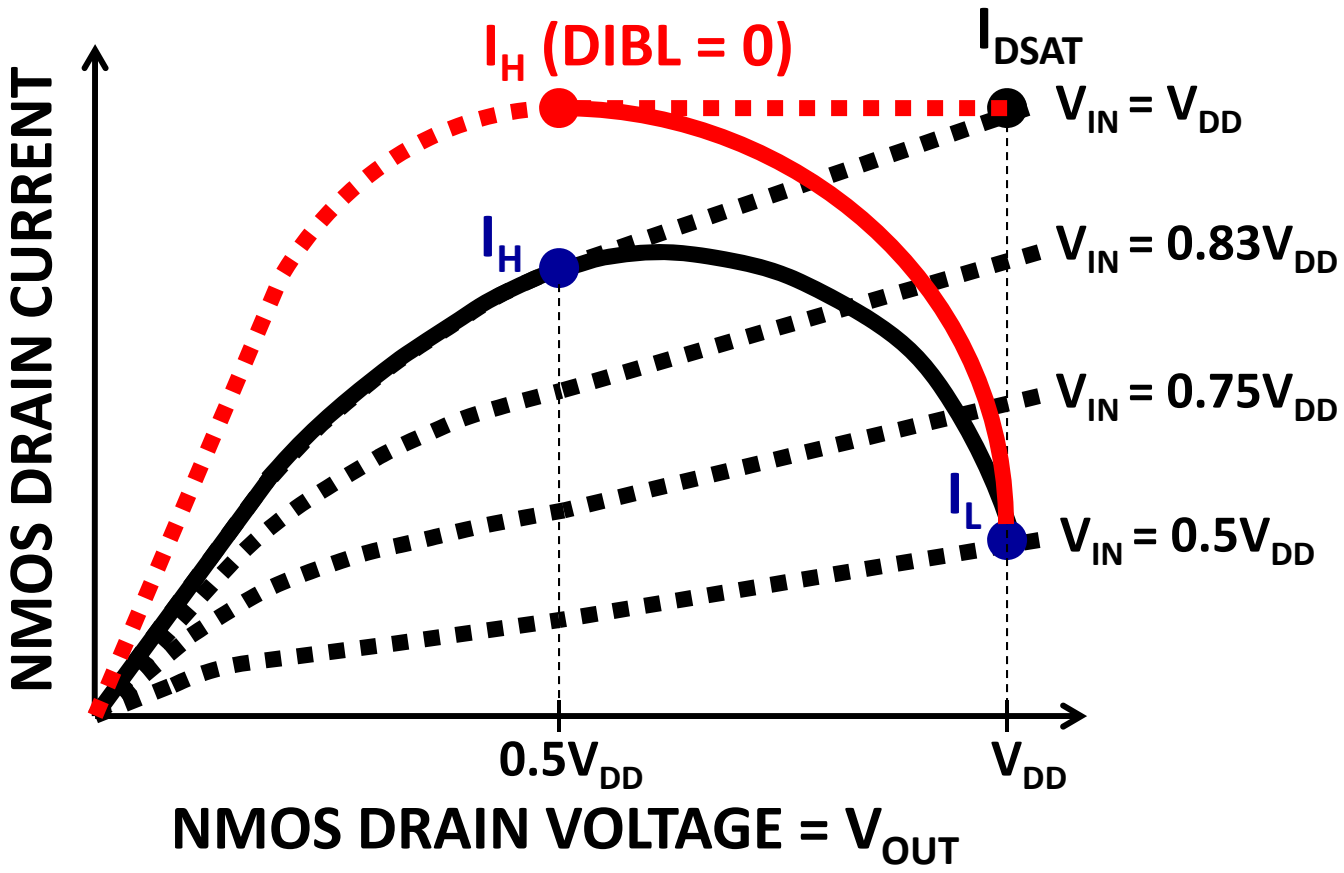
CMOS inverter chain:





$$I_{EFF} = \frac{I_H + I_L}{2}$$

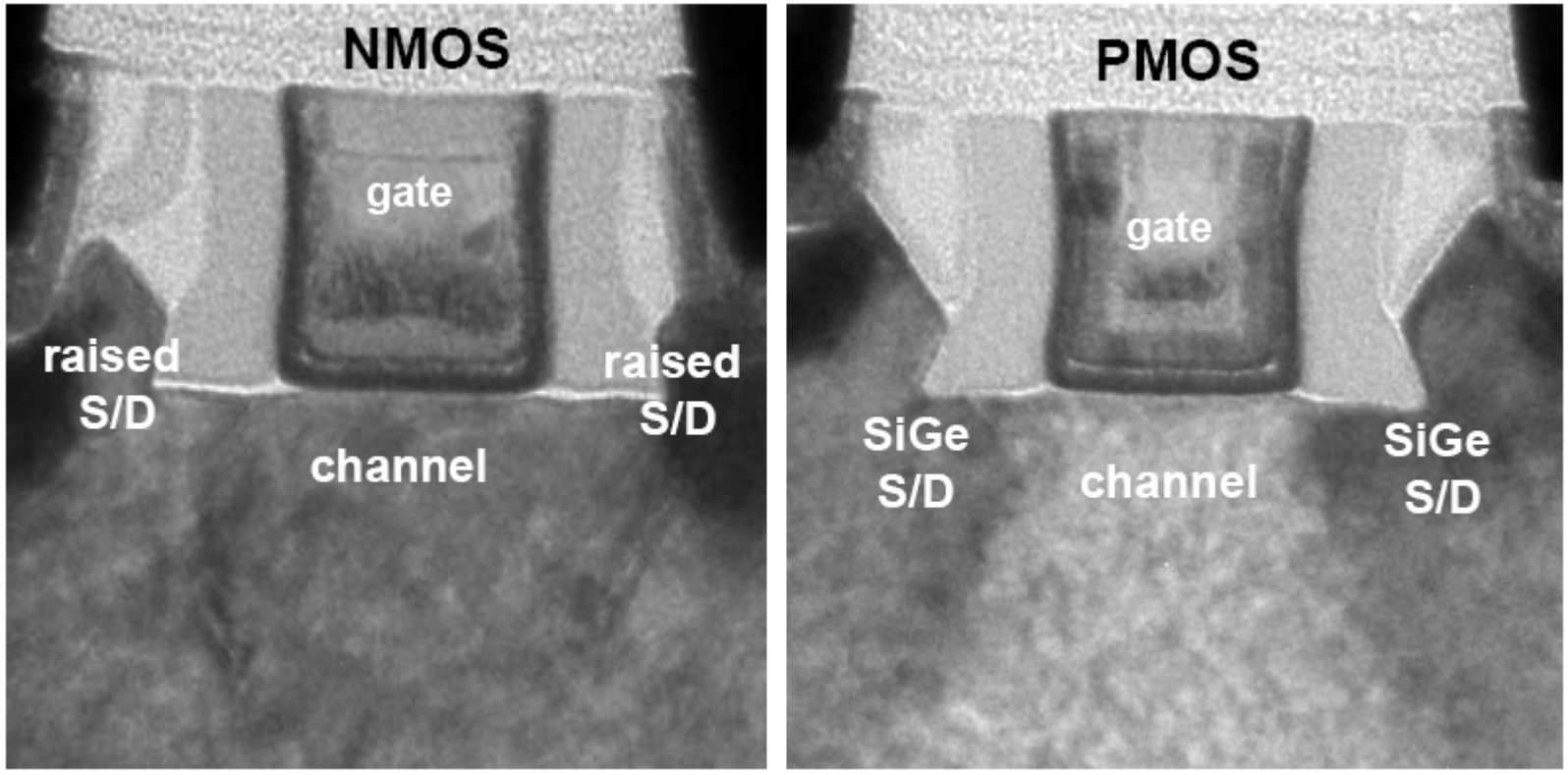




Performance Boosters

- Strained channel regions → $\mu_{eff}\uparrow$
- High-k gate dielectric and metal gate electrodes → $C_{ox}\uparrow$

Cross-sectional TEM views of Intel's 32 nm CMOS devices



A Journey Back through Time…

The UC-Berkeley AME Team

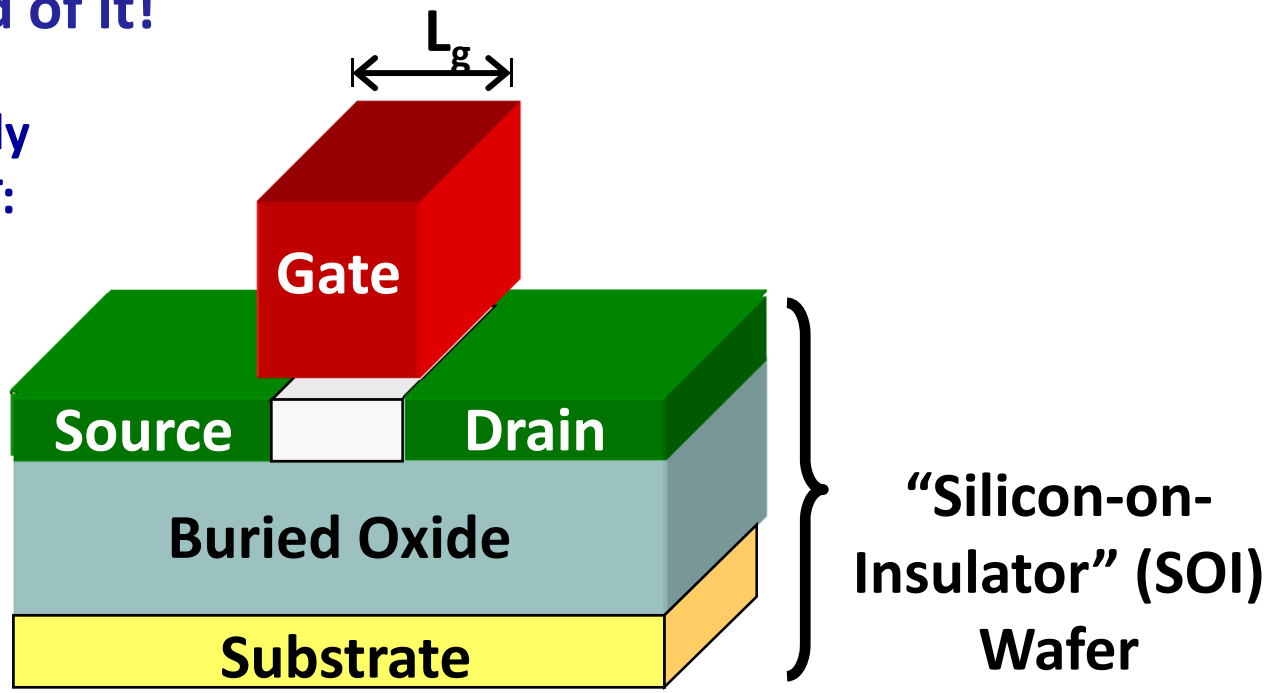
- **PI/co-PIs: Chenming Hu, Jeff Bokor, Tsu-Jae King**
- **Post-doc: Vivek Subramanian**
- **Industrial visitors:**
  - **Digh Hisamoto** (Hitachi CRL)
  - **Hideki Takeuchi** (now with Mears Technologies)
- **Graduate students (alphabetical order):**
  - **Leland Chang** (now with IBM TJ Watson Research)
  - **Yang-Kyu Choi** (now with KAIST)
  - **Xuejue "Cathy" Huang** (now with Intel Corp.)
  - **Jakub Kedzierski** (now with MIT Lincoln Lab)
  - **Charles Kuo** (now with Intel Corp.)
  - **Wen-Chin Lee** (now with TSMC)
  - **Nick Lindert** (now with Intel Corp.)
  - **Stephen Tang** (now with Intel Corp.)
  - …

Why New Transistor Structures?

- Off-state leakage (I_{OFF}) must be suppressed as L_g is scaled down
  - allows for reductions in V_{TH} and hence V_{DD}
- Leakage occurs in the region away from the channel surface

→ Let's get rid of it!

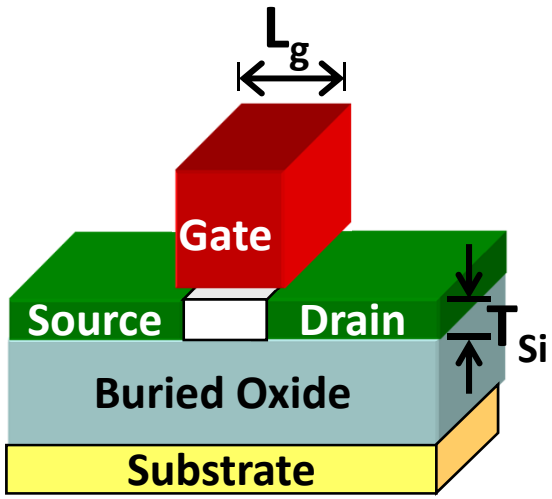
Thin-Body MOSFET:



Thin-Body MOSFETs

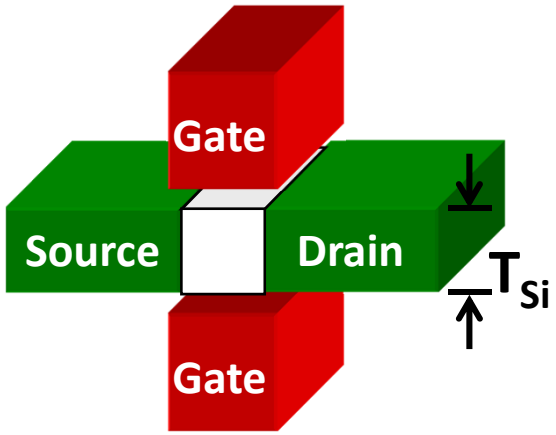
- I_{OFF} is suppressed by using an adequately thin body region.
  - Body doping can be eliminated
    - → higher drive current due to higher carrier mobility
    - → Reduced impact of random dopant fluctuations (RDF)

Ultra-Thin Body (UTB)



$T_{Si} < (1/4) \times L_g$

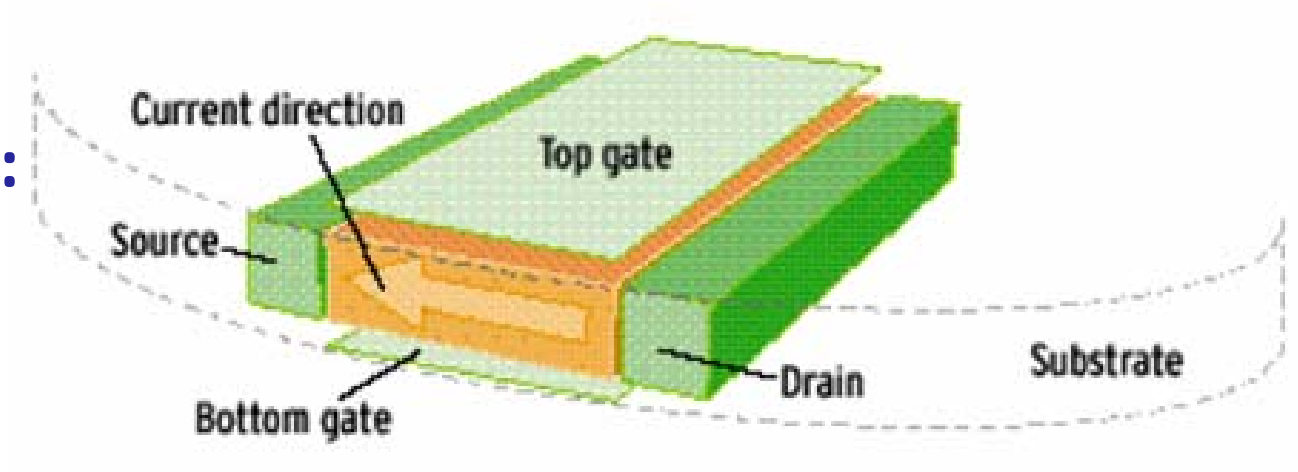
Double-Gate (DG)



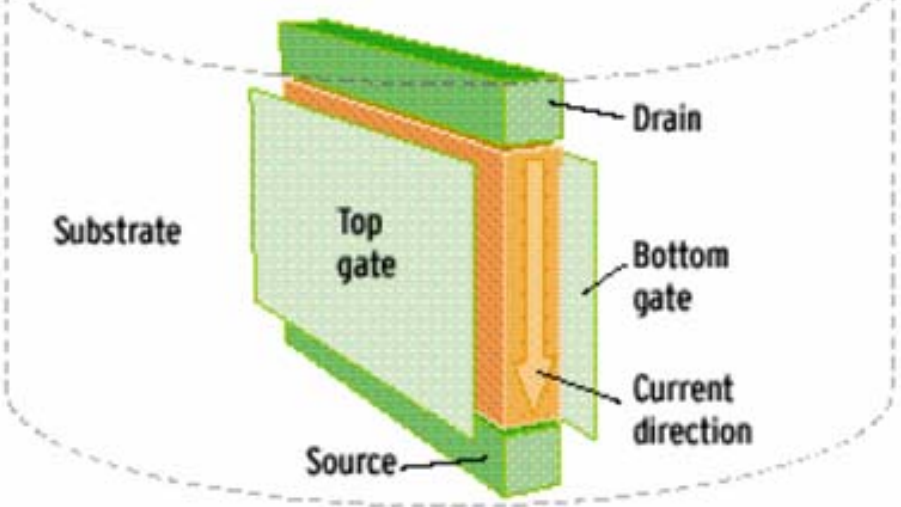
$T_{Si} < (2/3) \times L_g$

Double-Gate MOSFET Structures

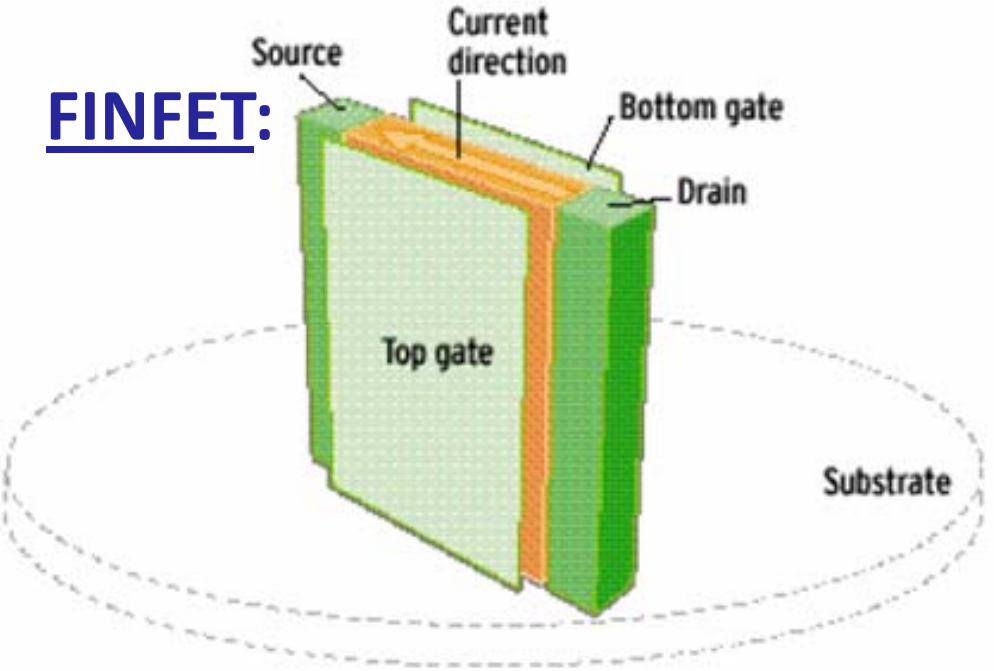
PLANAR:



VERTICAL

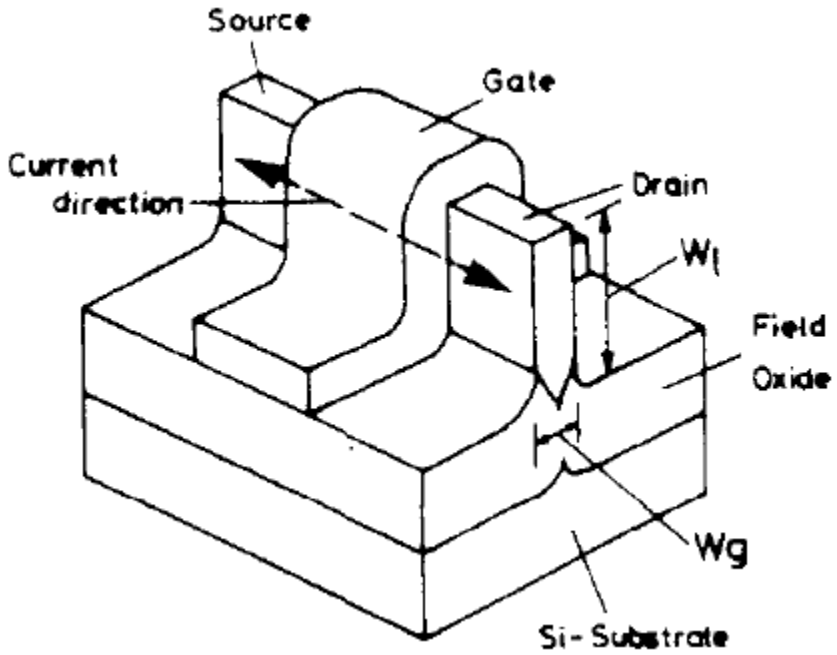


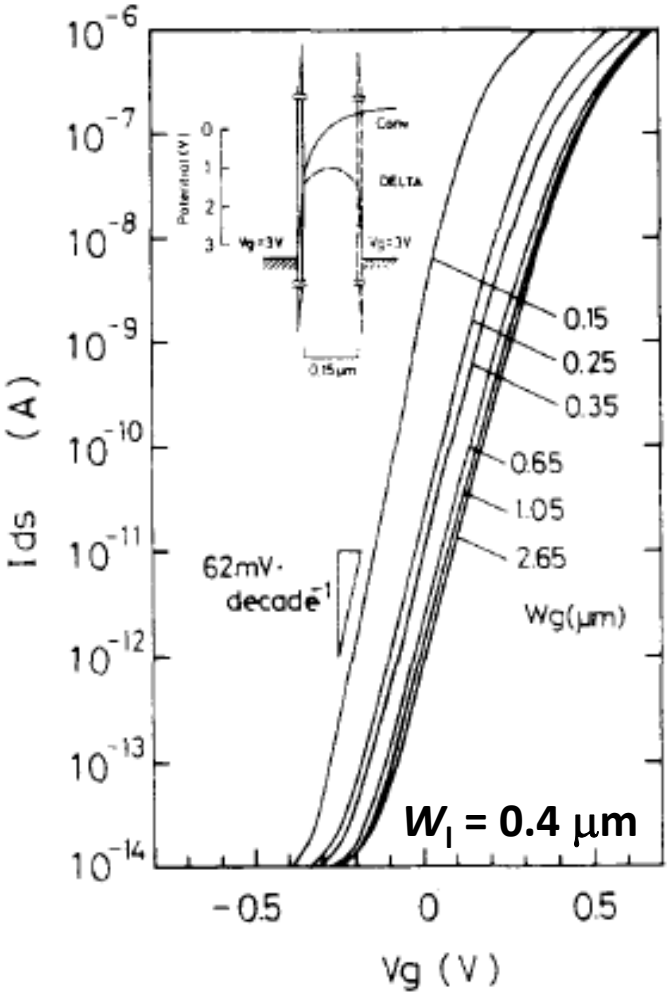
FINFET:



DELTA MOSFET

D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda (Hitachi Central Research Laboratory),
"A fully depleted lean-channel transistor (DELTA) – a novel vertical ultrathin SOI MOSFET,"
IEEE Electron Device Letters Vol. 11, pp. 36-39, 1990

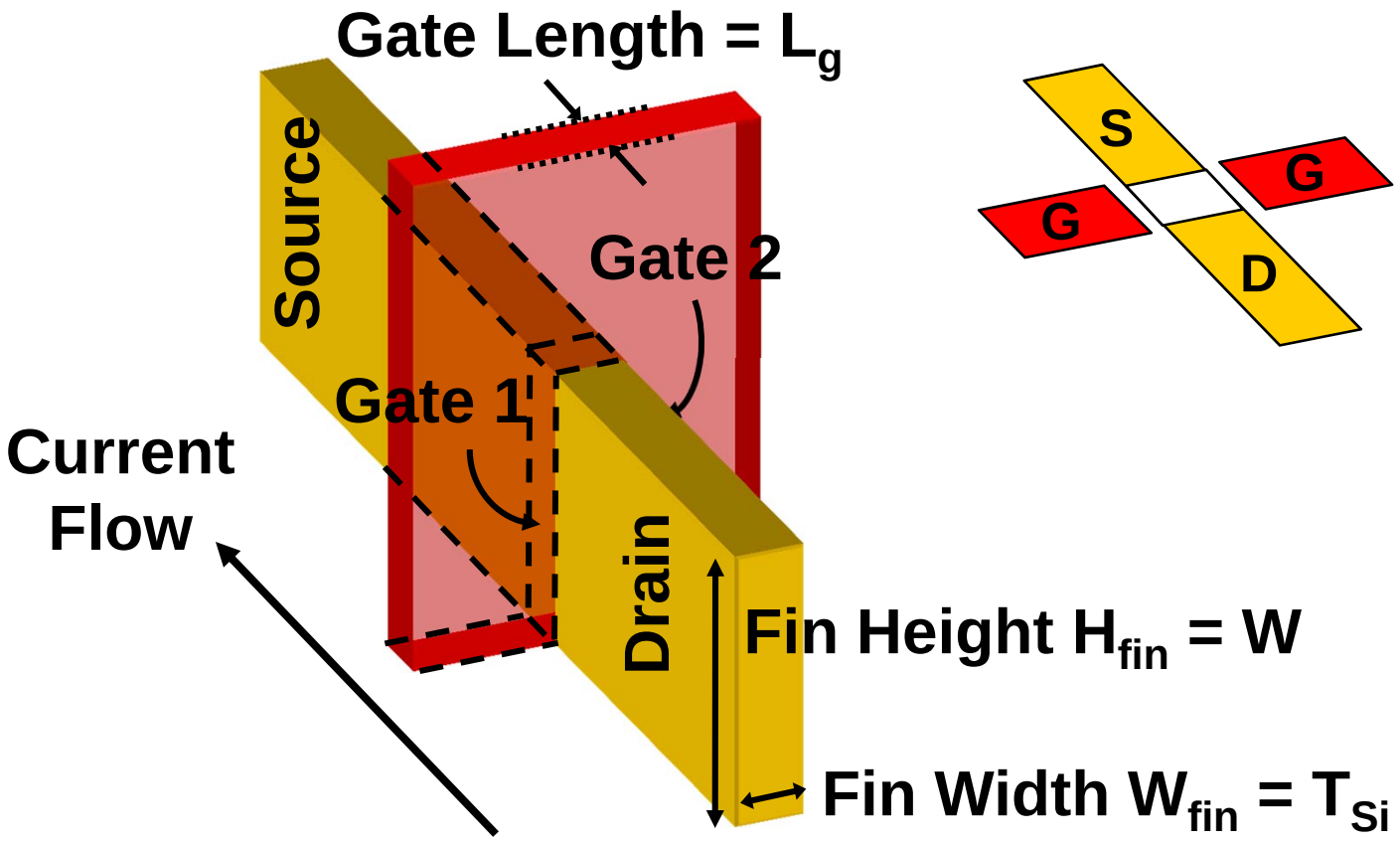




- **Improved gate control observed for W_g < 0.3 μm**
  - L_{EFF}= 0.57 μm

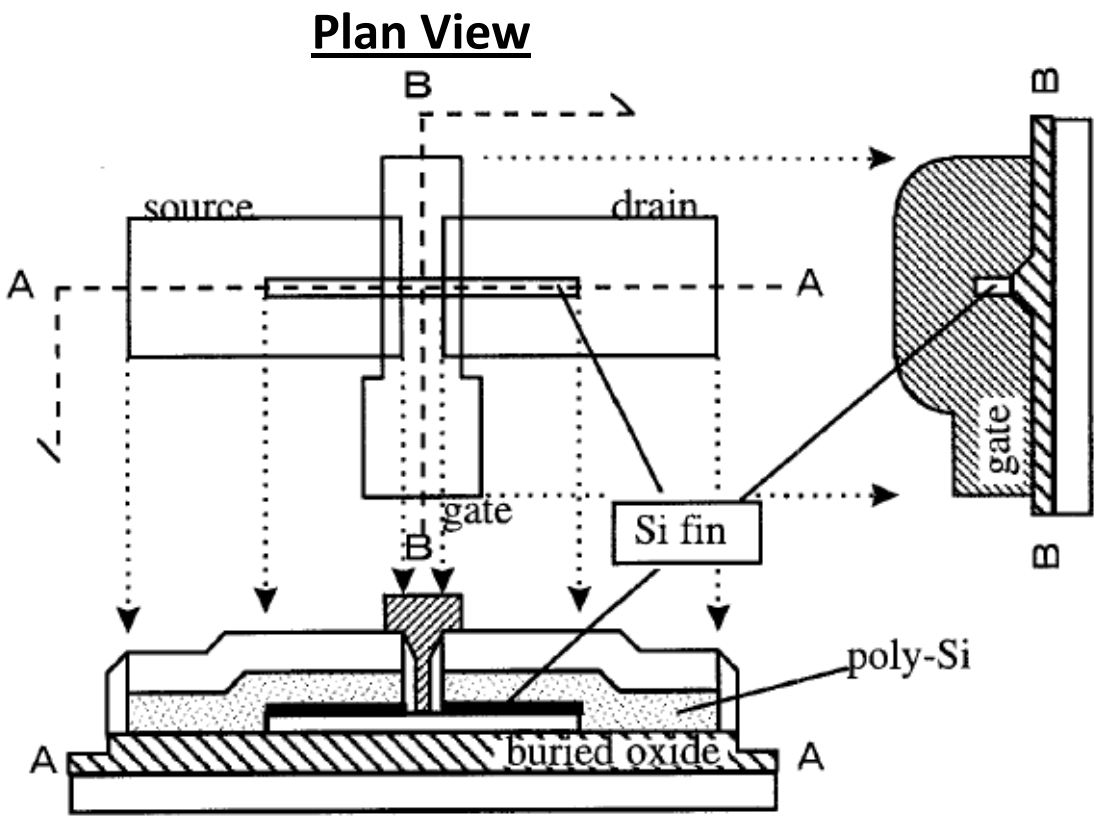
Double-Gate FinFET

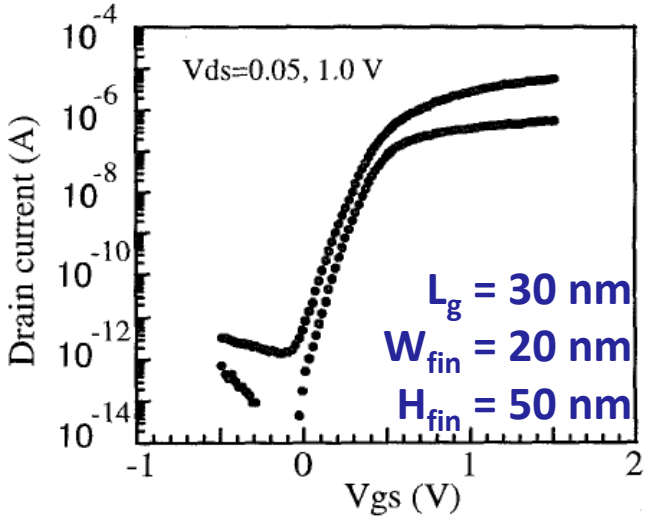
- Self-aligned gates straddle narrow silicon fin
- Current flows parallel to wafer surface

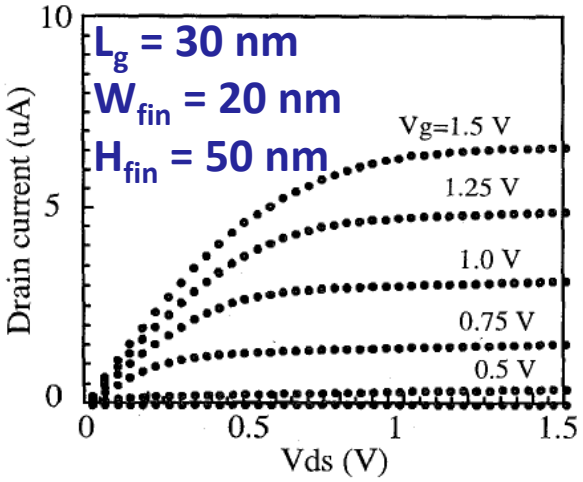


1998: First n-channel FinFETs

D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T.-J. King, J. Bokor, and C. Hu,
"A folded-channel MOSFET for deep-sub-tenth micron era,"
IEEE International Electron Devices Meeting Technical Digest, pp. 1032-1034, 1998







- Devices with L_g down to 17 nm were successfully fabricated

1999: First p-channel FinFETs

X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," *IEEE International Electron Devices Meeting Technical Digest*, pp. 67-70, 1999

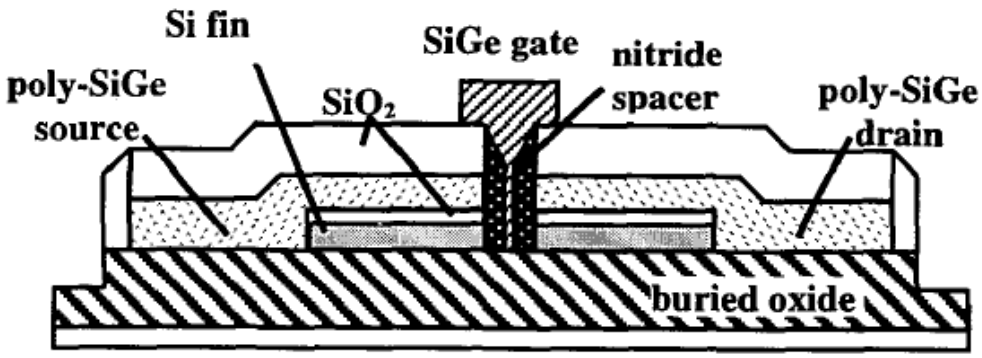
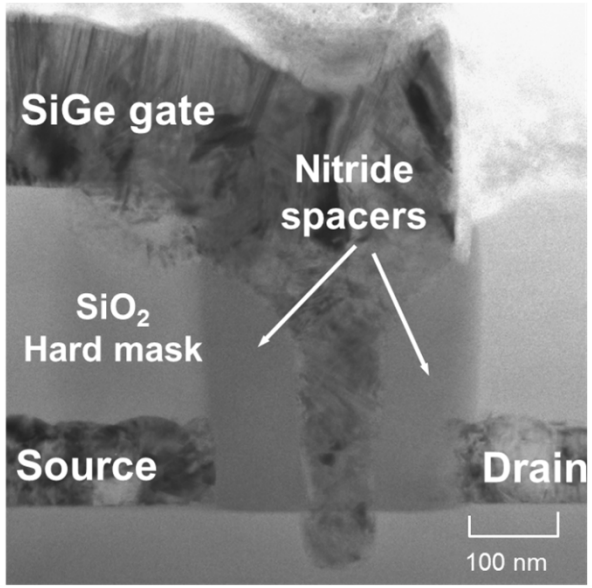
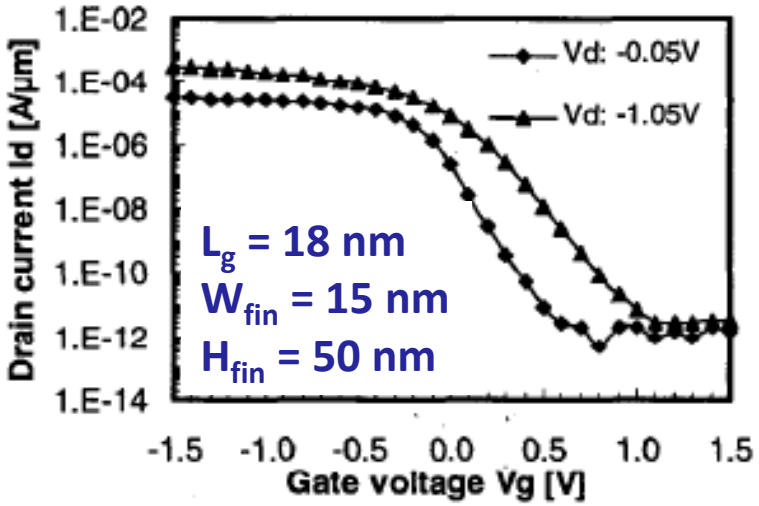
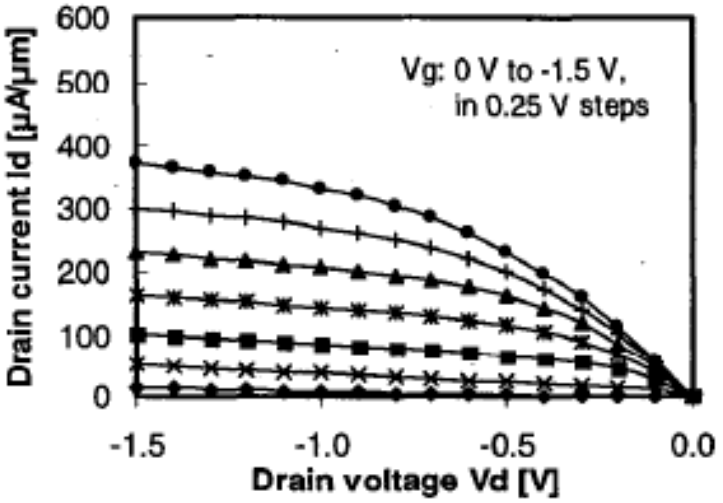


Figure 1: Schematic drawing of FinFET



Transmission Electron Micrograph





Recognition

The New York Times

MONDAY, DECEMBER 6, 1999

Computer Chip Researchers Set to Showcase Advances

A Shift to Further Miniaturization Is Seen

By JOHN MARKOFF

Computer chip researchers are gathering for an industry conclave in Washington this week, where a range of technical presentations are expected to revive the recently flagging spirts of the semiconductor community.

The announcements planned by **I.B.M., Lucent's** Bell Laboratories, **Motorola**, the University of California at Berkeley and other research laboratories at the International Electron Device Meeting suggest that researchers are finding ways to accelerate the speed at which chip makers can further shrink the size of the microscopic transistors that are the basic component of microelectronic systems.

Word of the advances are significant now, since a number of prominent semiconductor researchers have been expressing concerns that the industry might be approaching fundamental physical limits that might curtail chip development.

"This is important because in the last five years there has been a doomsday feeling among semiconductor researchers," said Chenming Hu, a University of California at Berkeley electrical engineering professor. A research team led by Mr. Hu will present a paper detailing a new kind of transistor that the research team believes can be scaled down to just 18 nanometers — or about the width of 100 atoms. That would be about one-twentieth the size of today's smallest transistors.

The Berkeley researchers predict that the new transistor design could lead to devices that store 400 times as much data as today's densest memory chips.

While such a transistor might not be common for another decade, the Berkeley announcement indicates that it might be possible to extend the future of microscopic semiconductor circuitry well beyond the year 2014, when some researchers have been predicting that the technology would meet its theoretical limits.

Since the 1960's, the chip industry has operated under an assumption that had proved so reliable that it is known as Moore's Law — named for the Intel co-founder Gordon Moore, who had observed that the number of transistors that chip makers could fit on a given piece of silicon was doubling every 18 months. But recently, even Mr. Moore himself has warned that the growth rate was coming at such spiraling costs that Moore's Law might no longer be sustainable.

This week's meeting, however, may indicate that the circuiteers have made new breakthroughs in their quest for the infinitessimal.

I.B.M. will also report on a new complementary metal oxide semiconductor, or CMOS, chip-making technology that the company says should pave the way for a generation of microprocessors that will reach computing speeds above a billion operations a second. The new technology is based on a relatively new kind

Developments in transistors will be prominent.

of manufacturing process known as silicon-on-insulator, which offers higher speeds and lower power consumption than conventional silicon-based CMOS chips.

The company would not state specific product dates but said it generally makes such technology announcements a year to 18 months before products are introduced.

Researchers at Motorola Laboratories have developed a new class of materials known as perovskites (pronounced per-AHV-skights) that will permit a new class of transistors.

DARPA Significant Technical Achievement Award
presented at DARPATECH 2000 Symposium

2000: Call from the Industry

- **SRC Solicitation: Novel Devices for Information Processing**

  "Proposals are sought related to novel device structures, arrays or nanosystems that have the potential to process and store information at a speed, density and energy efficiency that greatly exceed (100x) those projected for silicon CMOS at the 35-nm node."

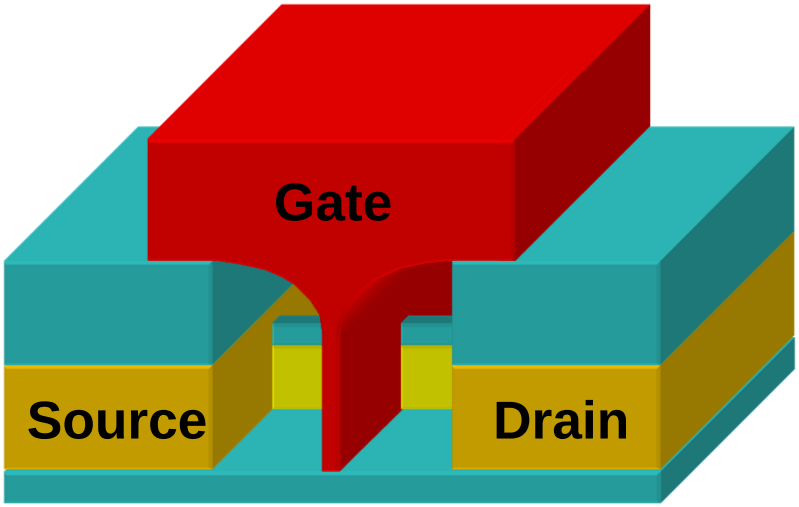
→ UCB Project: "FinFET -- A Double-Gate MOSFET Structure"

  - **Task 1: Develop a FinFET process flow compatible with a conventional planar CMOS process.**
  - **Task 2: Demonstrate compatibility of the FinFET structure with a production environment.**
  - **Funded October 2000 through September 2003 @ $300k/yr**
  - **New graduate students: Pushkar Ranade** (now with Intel Corp.)
    Peiqi Xuan (now with Marvell Technology)

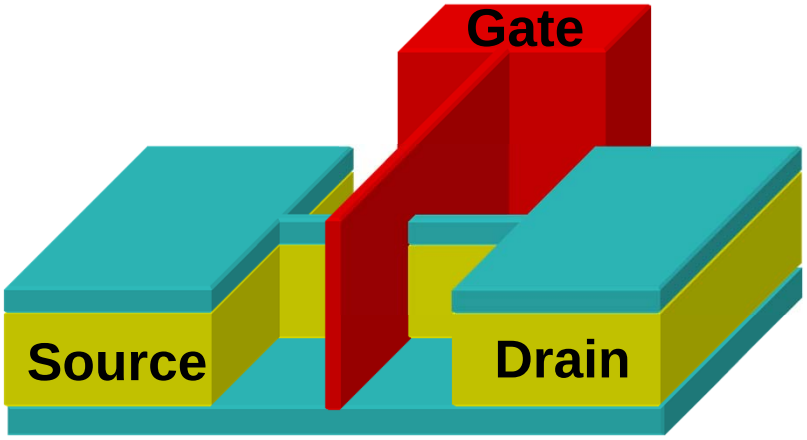
- **Chenming Hu goes to Taiwan Semiconductor Manufacturing Company (2001-2004)**

FinFET Structures

Original:



Improved:



UC-Berkeley FinFET Patent

(12) **United States Patent**
Hu et al.

(10) **Patent No.: US 6,413,802 B1**
(45) **Date of Patent: Jul. 2, 2002**

(54) **FINFET TRANSISTOR STRUCTURES HAVING A DOUBLE GATE CHANNEL EXTENDING VERTICALLY FROM A SUBSTRATE AND METHODS OF MANUFACTURE**

(75) Inventors: **Chenming Hu**, Alamo; **Tsu-Jae King**, Fremont; **Vivek Subramanian**, Redwood City; **Leland Chang**, Berkeley; **Xuejue Huang**; **Yang-Kyu Choi**, both of Albany; **Jakub Tadeusz Kedzierski**, Hayward; **Nick Lindert**, Berkeley; **Jeffrey Bokor**, Oakland, all of CA (US); **Wen-Chin Lee**, Beaverton, OR (US)

(73) Assignee: **The Regents of the University of California**, Oakland, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/695,532**
(22) Filed: Oct. 23, 2000

(51) **Int. Cl.**[7] **H01L 21/00**; H01L 21/84

(52) **U.S. Cl.** **438/151**; 438/283

(58) **Field of Search** 438/151, 157, 438/201, 223, 241, 258, 279, 283, 437, 588, 594, 259, 270, 303, 305, 589, 592

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,356,824	A	10/1994	Chouan et al.	437/41
5,604,368	A *	2/1997	Taur et al.	257/348
5,646,058	A *	7/1997	Taur et al.	438/283
5,773,331	A	6/1998	Solomon et al.	438/164
5,804,848	A	9/1998	Mukai	257/270
5,899,710	A	5/1999	Mukai	438/156
6,214,670	B1 *	4/2001	Shih et al.	438/259

OTHER PUBLICATIONS

V. Subramanian et al., "A Bulk–Si–compatible Ultrathin-body SOI Technology for sub–100nm MOSFETS," Proceedings of the 57th Annual Device Research Conference, pp. 28–29 (1999).

Hisamoto et al., "A Folded–channel MOSFET for Deepsub–tenth Micron Era," 1998 IEEE International Electron Device Meeting Technical Digest, pp. 1032–1034 (1998).

Huang et al., "Sub 50–nm FinFET: PMOS," 1999 IEEE International Electron Device Meeting Technical Digest, pp. 67–70 (1999).

Auth et al., Vertical, Fully–Depleted, Surrounding Gate MOSFETS on sub–0.1μm Thick Silicon Pillars, 1996 54th Annual Device Research Conference Digest, pp. 108–109 (1996).

Hisamoto et al., "A Fully Depleted Lean–Channel Transistor (DELTA)—A Novel Vertial Ultrathin SOI MOSFET," IEEE Electron Device Letters, v. 11(1), pp. 36–38 (1990).

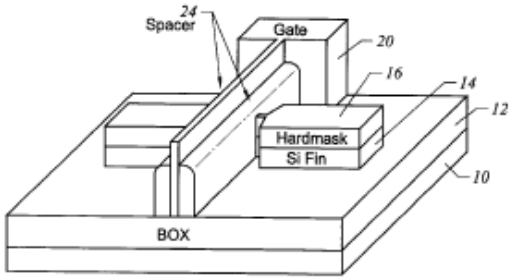
(List continued on next page.)

Primary Examiner—David Nelms
Assistant Examiner—Phuc T. Dang
(74) *Attorney, Agent, or Firm*—Townsend and Townsend and Crew LLP; Henry K. Woodward

(57) **ABSTRACT**

A FinFET device is fabricated using conventional planar MOSFET technology. The device is fabricated in a silicon layer overlying an insulating layer (e.g., SIMOX) with the device extending from the insulating layer as a fin. Double gates are provided over the sides of the channel to provide enhanced drive current and effectively suppress short channel effects. A plurality of channels can be provided between a source and a drain for increased current capacity. In one embodiment two transistors can be stacked in a fin to provide a CMOS transistor pair having a shared gate.

28 Claims, 4 Drawing Sheets



What is claimed is:

1. A method of fabricating a double gate MOSFET device comprising the steps of:

a) providing a silicon on insulator (SOI) substrate with a first silicon layer overlying an insulating layer and having an exposed major surface,

b) providing an etchant mask on the major surface,

c) patterning the etchant mask to define source, drain, and channel regions and expose surrounding portions of the silicon layer,

d) etching the exposed silicon layer and forming source, drain, and channel regions extending from the insulator layer, the channel being a fin with a top surface and two opposing sidewalls,

e) forming a gate dielectric on sidewalls of the channel region,

f) depositing gate material over the etchant mask and the gate dielectric,

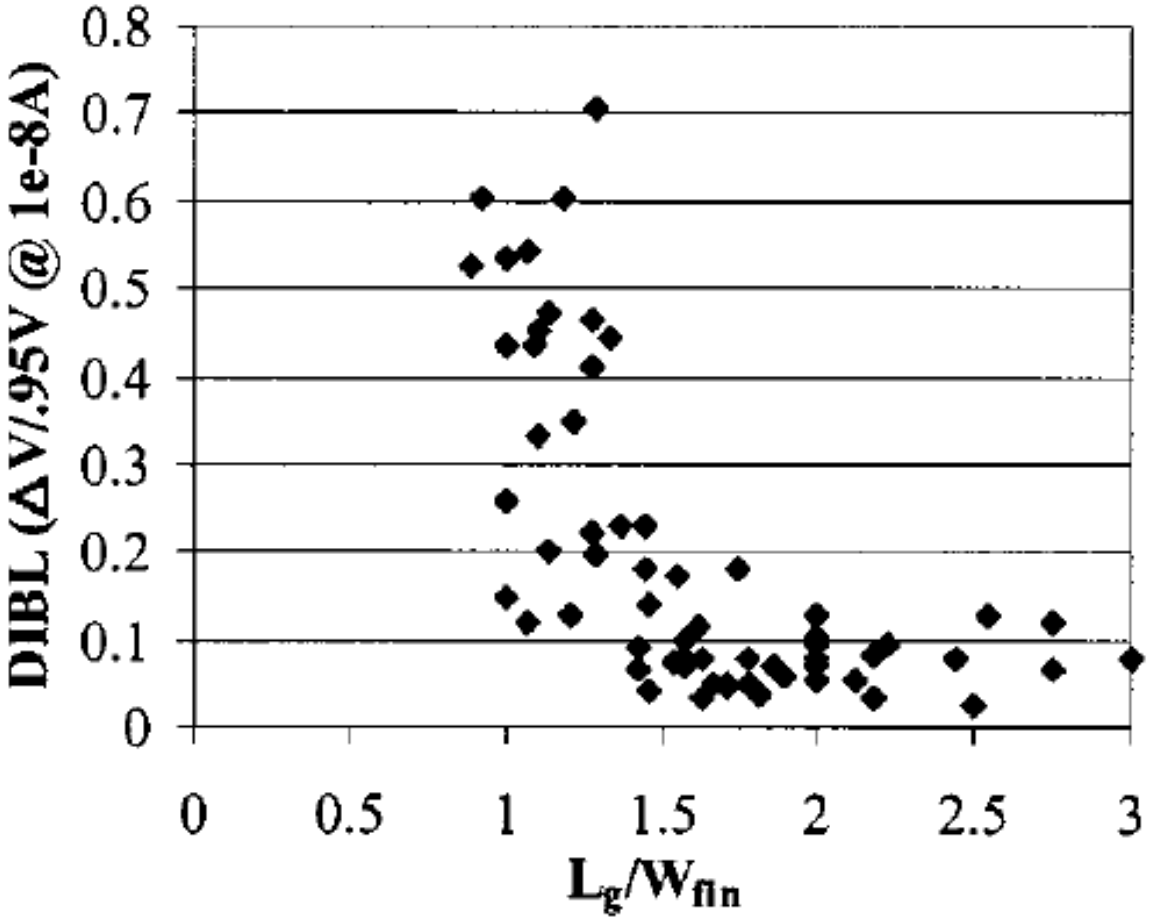
g) selectively masking and etching the gate material to form a gate on the top surface and sidewalls of the channel region and separated from the channel region by the gate dielectric and the etchant mask,

h) forming dielectric spacers between the gate and the source and drain regions, and

i) doping the source and drain regions.

+ 27 additional claims…

Fin Width Requirement



- **To adequately suppress DIBL, $L_g/W_{fin} > 1.5$**

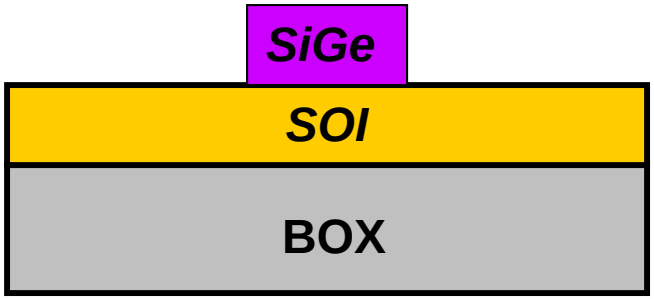
→ **Challenge for lithography!**

Sub-Lithographic Fin Patterning

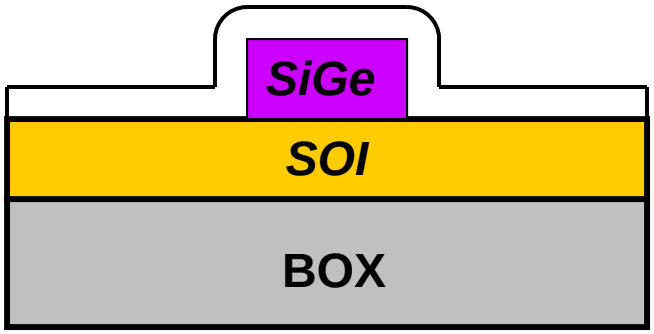
Spacer Lithography

a.k.a. Sidewall Image Transfer (SIT) and Self-Aligned Double Patterning (SADP)

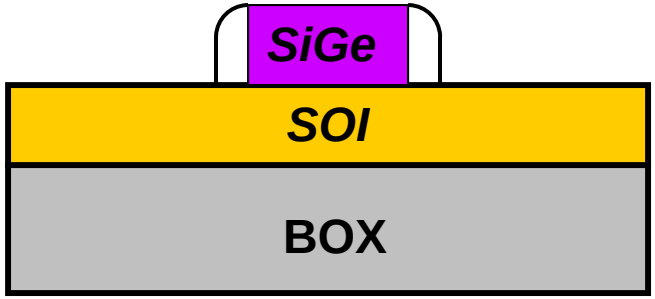
1. Deposit & pattern sacrificial layer



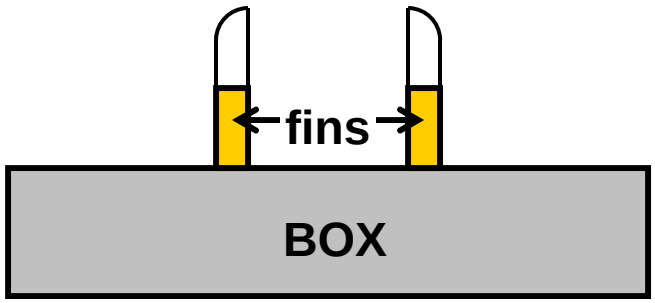
2. Deposit mask layer (SiO_2 or Si_3N_4)



3. Etch back mask layer to form "spacers"



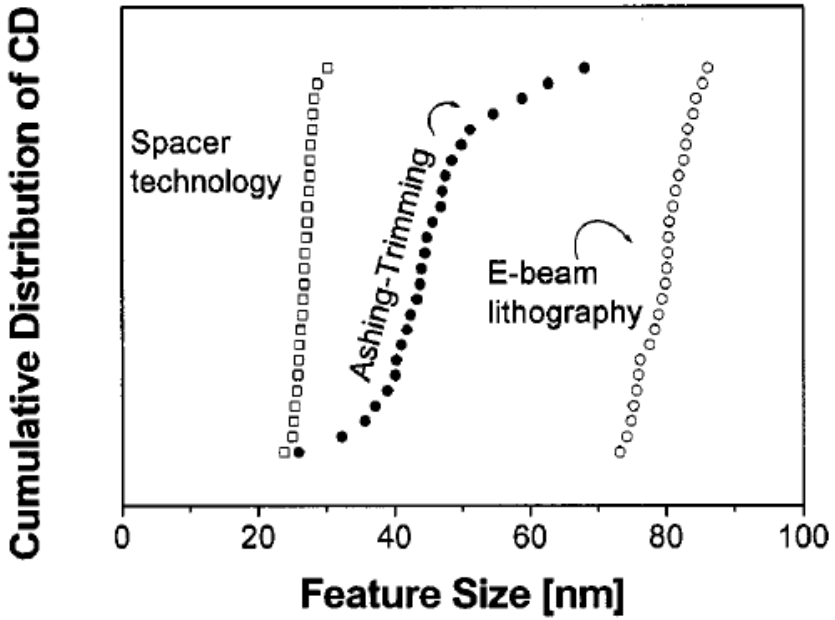
4. Remove sacrificial layer; etch SOI layer to form fins



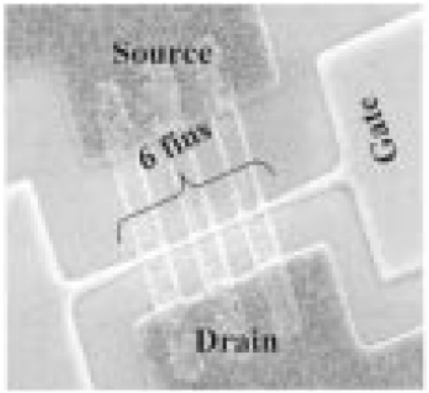
Note that fin pitch is 1/2× that of patterned layer

Benefits of Spacer Lithography

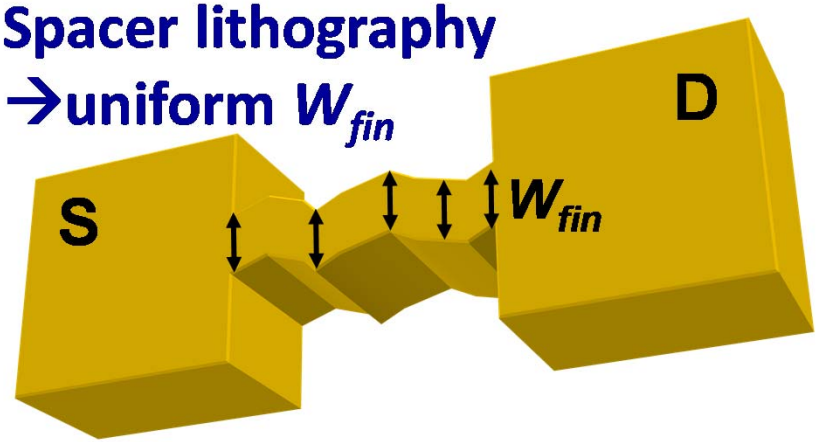
- **Spacer litho. provides for better CD control and uniform fin width**



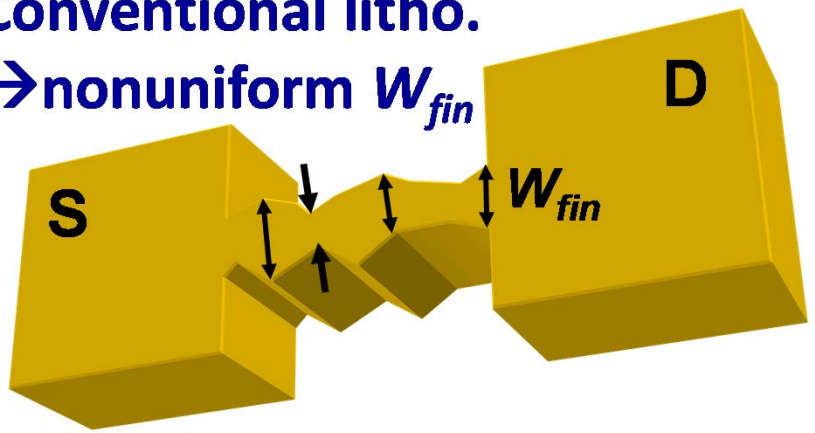
SEM image of FinFET with spacer-defined fins:



Spacer lithography
→uniform W_{fin}



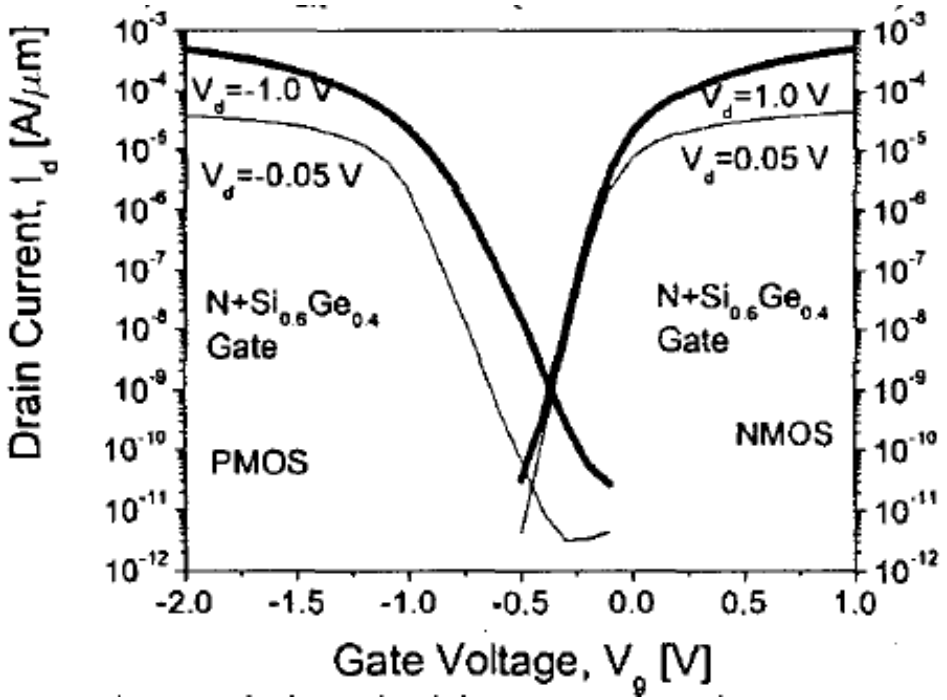
Conventional litho.
→nonuniform W_{fin}

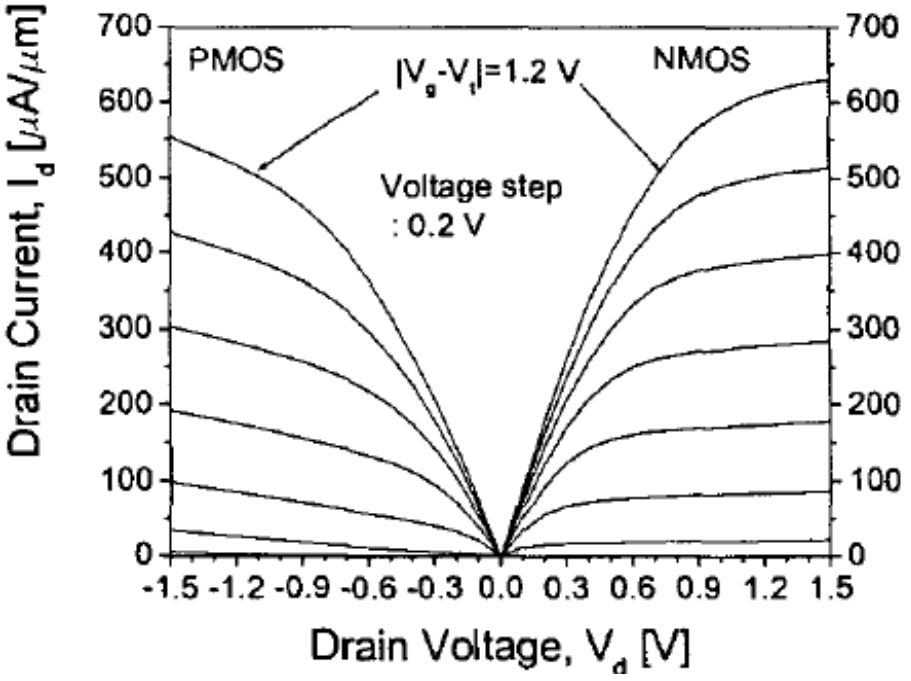


Spacer-defined FinFETs

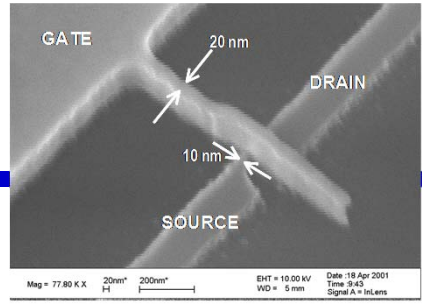
Y.-K. Choi, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Anderson, T.-J. King, J. Bokor, and C. Hu,
"Sub-20nm CMOS FinFET technologies,"
IEEE International Electron Devices Meeting Technical Digest, pp. 421-424, 2001

L_g = 60 nm, W_{fin} = 40 nm

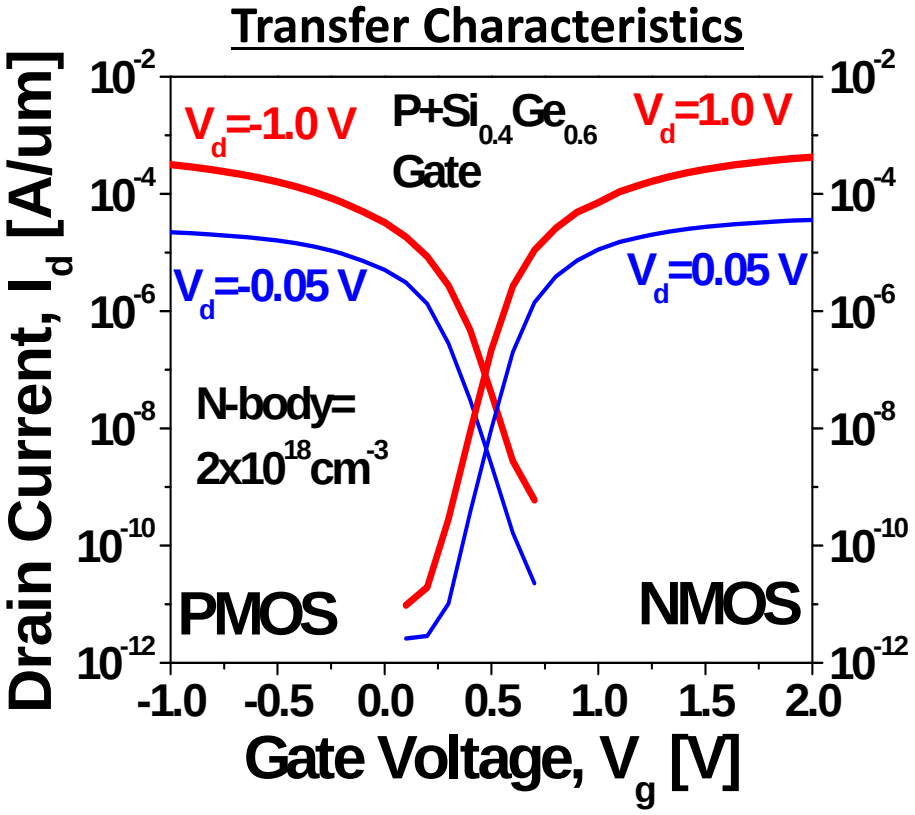


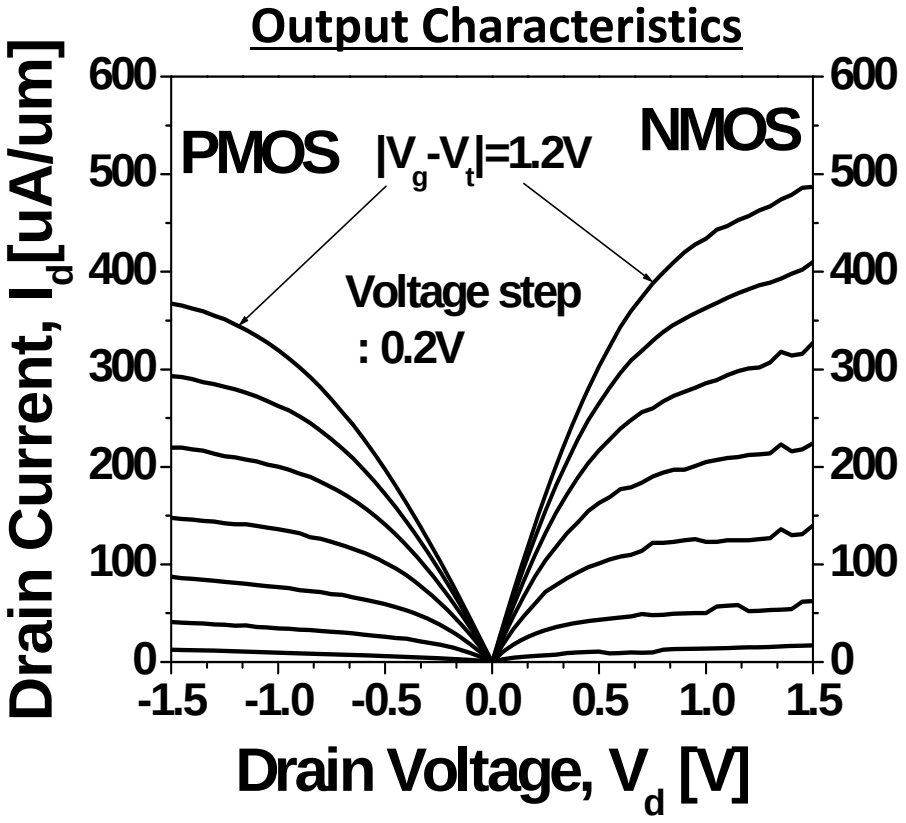


2001: 15 nm FinFETs



Y.-K. Choi, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Anderson, T.-J. King, J. Bokor, C. Hu,
"Sub-20nm CMOS FinFET technologies,"
IEEE International Electron Devices Meeting Technical Digest, pp. 421-424, 2001

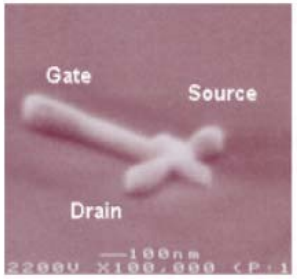




W_{fin} = 10 nm; T_{ox} = 2.1 nm

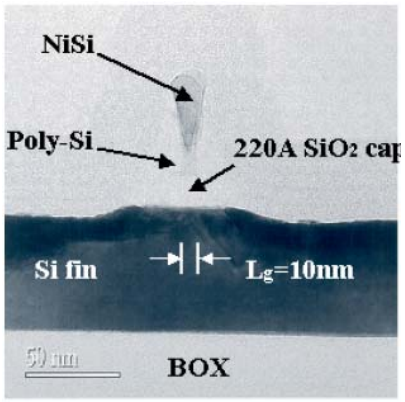
2002: 10 nm FinFETs

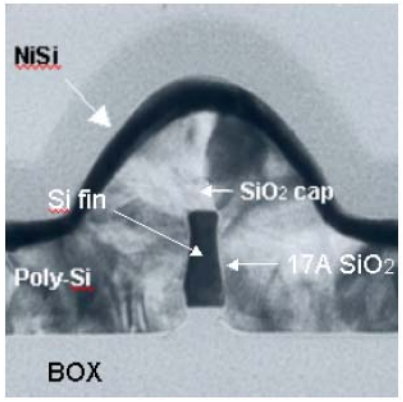
SEM image:

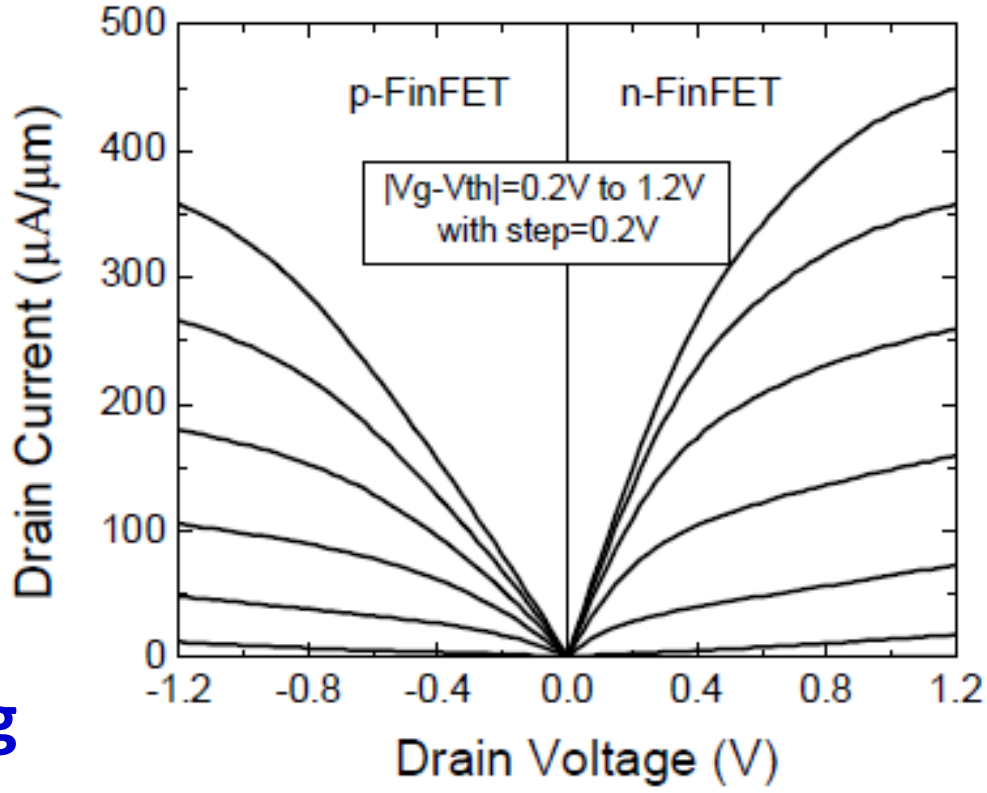


B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Hu, T.-J. King, J. Bokor, M.-R. Lin, and D. Kyser,
"FinFET scaling to 10nm gate length,"
International Electron Devices Meeting Technical Digest, pp. 251-254, 2002

TEM images







- **These devices were fabricated at AMD, using optical lithography.**

DARPA/SRC Focus Center Research Program

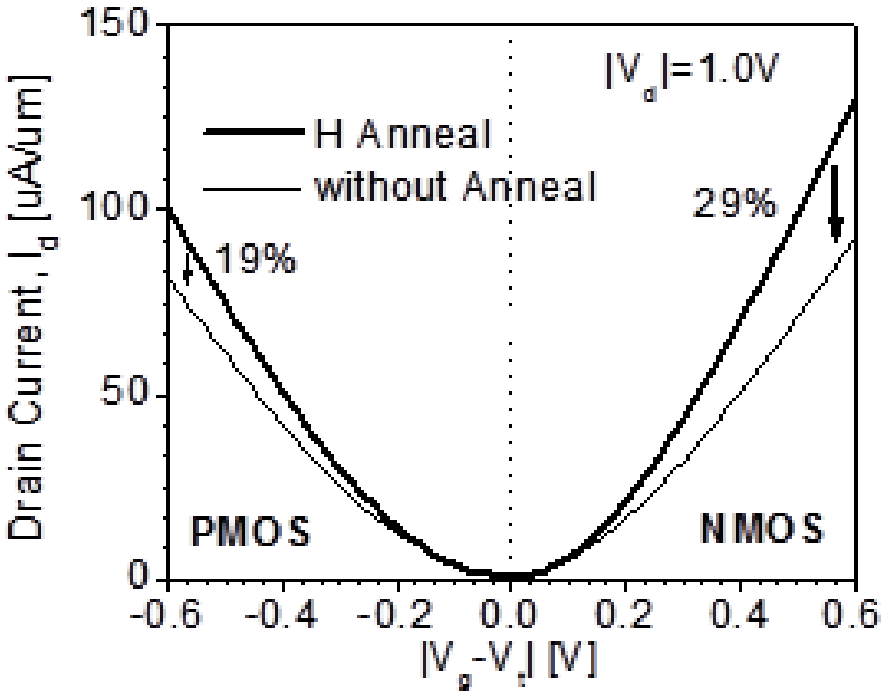
- **Center for Materials, Structures, and Devices (MSD)**
  - **Approaches for enhancing FinFET performance**
  - **Funded April 2001 through August 2003**
  - **Student: Daewon Ha** (now with Samsung Electronics)

- **Center for Circuits and Systems Solutions (C2S2)**
  - **FinFET-based circuit design**
  - **Funded August 2003 to July 2006**
  - **Students:**
    - **Sriram Balasubramanian** (now with GLOBALFOUNDRIES)
    - **Zheng Guo** (now with Intel)
    - **Radu Zlatanovici** (now with Intel Corp.)

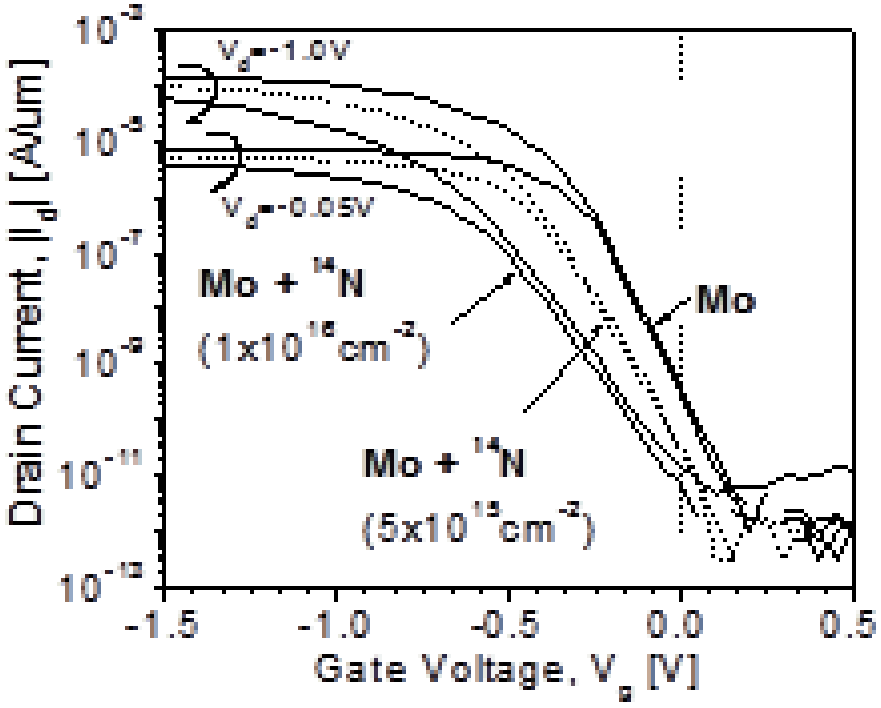
FinFET Process Refinements

Y.-K. Choi, L. Chang, P. Ranade, J. Lee, D. Ha, S. Balasubramanian, A. Agarwal, T.-J. King, and J. Bokor,
"FinFET process refinements for improved mobility and gate work function engineering,"
IEEE International Electron Devices Meeting Technical Digest, pp. 259-262, 2002

Fin-sidewall smoothening for improved carrier mobilities

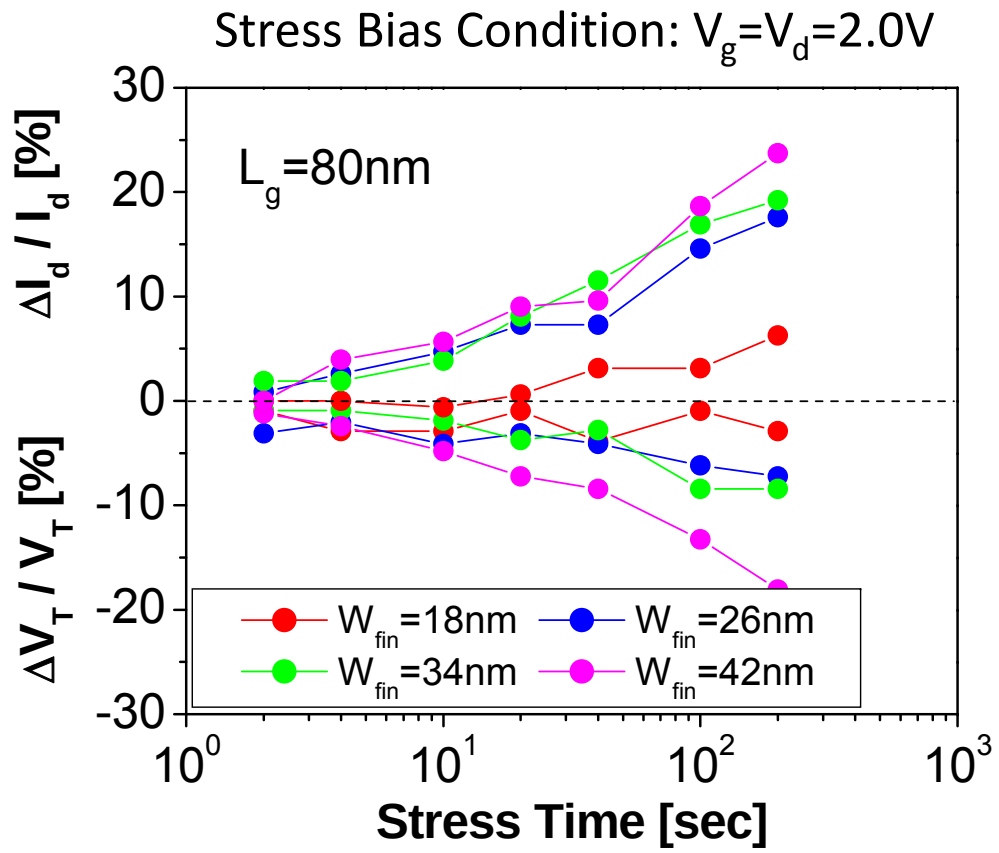


Gate work function tuning for V_{TH} adjustment



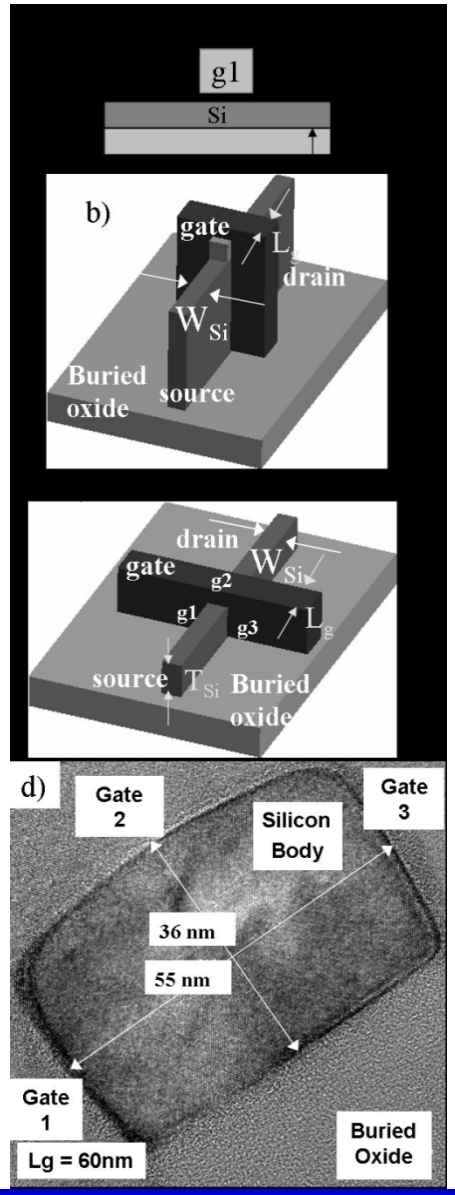
FinFET Reliability

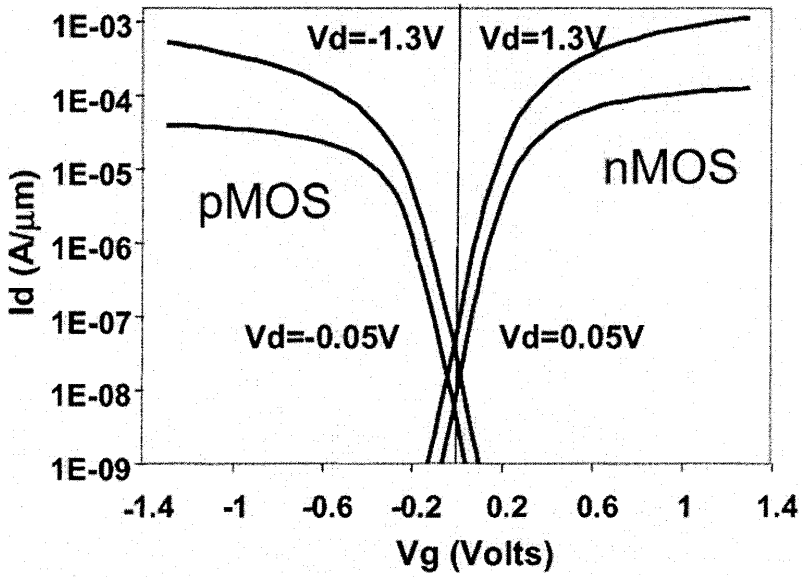
Y.-K. Choi, D. Ha, J. Bokor, and T.-J. King, "Reliability study of CMOS FinFETs,"
***IEEE International Electron Devices Meeting Technical Digest*, pp. 177-180, 2003**

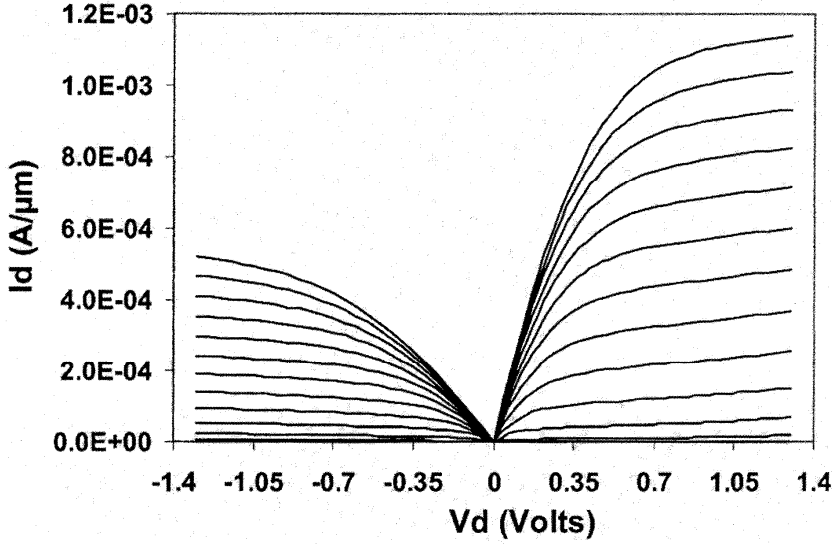


- **Narrower fin → improved hot-carrier (HC) immunity**
- **HC lifetime and oxide Q_{BD} are also improved by smoothening the Si fin sidewall surfaces** (by H_2 annealing)

Tri-Gate FET (Intel Corp.)







L_g = 60 nm
W_{fin} = 55 nm
H_{fin} = 36 nm

B. Doyle *et al.*, *IEEE Electron Device Letters*, Vol. 24, pp. 263-265, 2003

Bulk FinFET (Samsung Electronics)

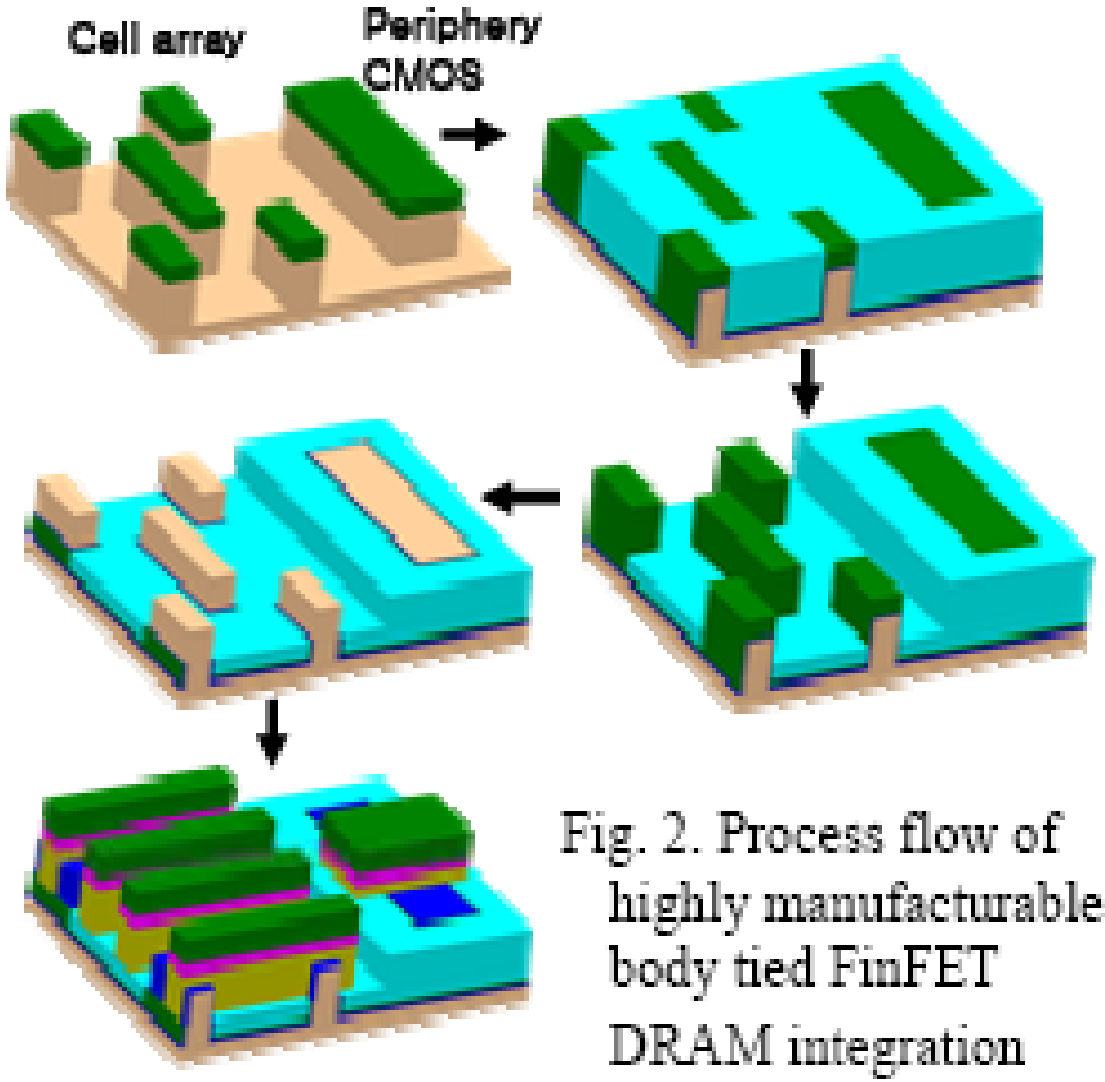
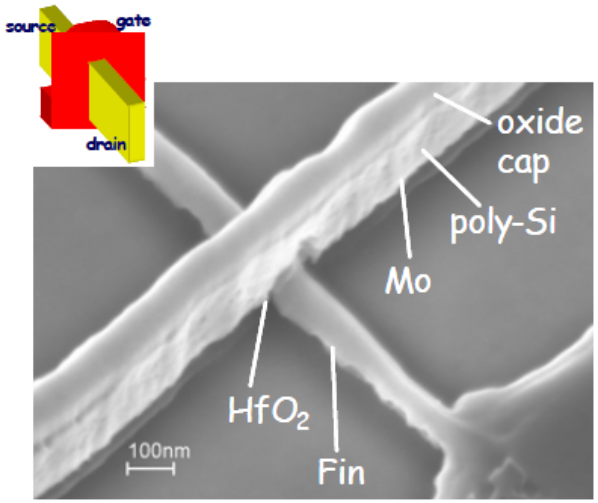


Fig. 2. Process flow of highly manufacturable body tied FinFET DRAM integration

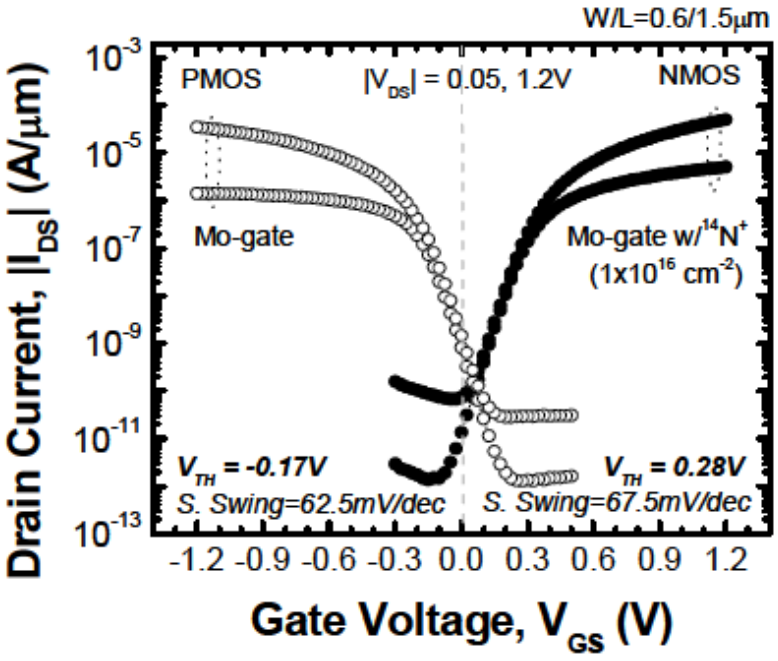
- **FinFETs can be made on bulk-Si wafers**
  - ✓**lower cost**
  - ✓**improved thermal conduction**
- **90 nm L_g FinFETs demonstrated**
  - **W_{fin} = 80 nm**
  - **H_{fin} = 100 nm**

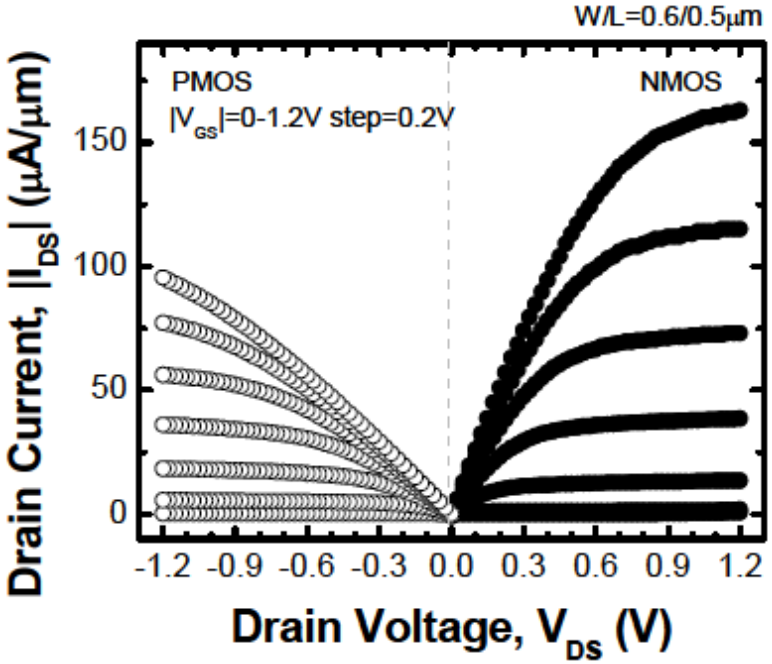
  DIBL = 25 mV

2004: High-k/Metal Gate FinFET



D. Ha, H. Takeuchi, Y.-K. Choi, T.-J. King, W. Bai, D.-L. Kwong, A. Agarwal, and M. Ameen, "Molybdenum-gate HfO_2 CMOS FinFET technology," *IEEE International Electron Devices Meeting Technical Digest*, pp. 643-646, 2004

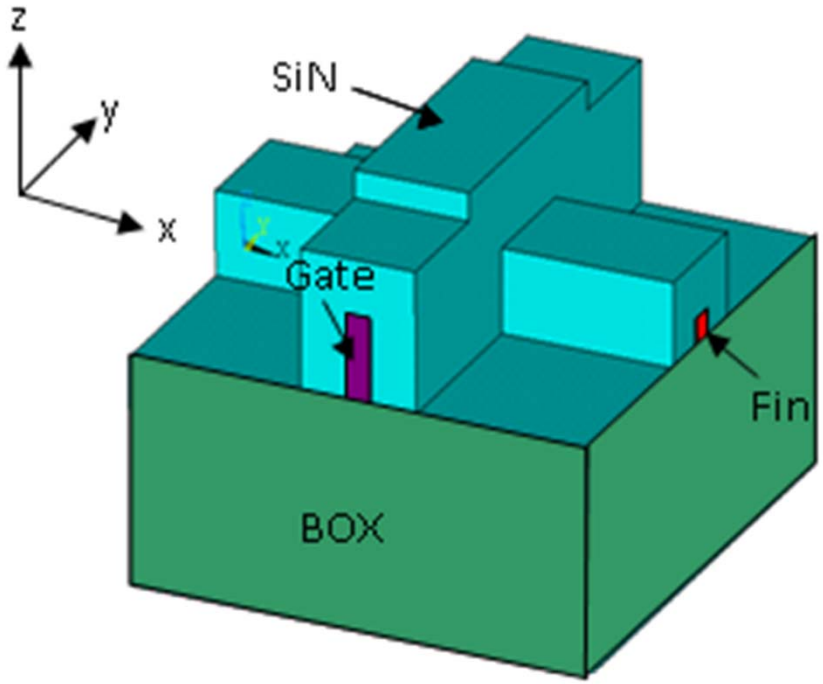




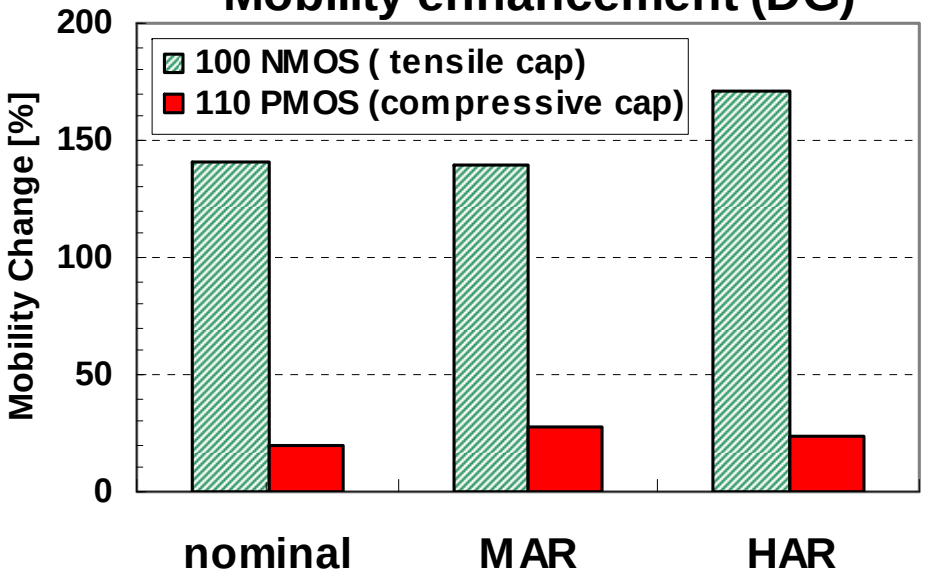
2005: Strained FinFET Technology

K. Shin and T.-J. King,
"Dual stress capping layer enhancement study for hybrid orientation FinFET CMOS technology,"
IEEE International Electron Devices Meeting Technical Digest, , pp. 988-991, 2005

3-D structure used for simulations



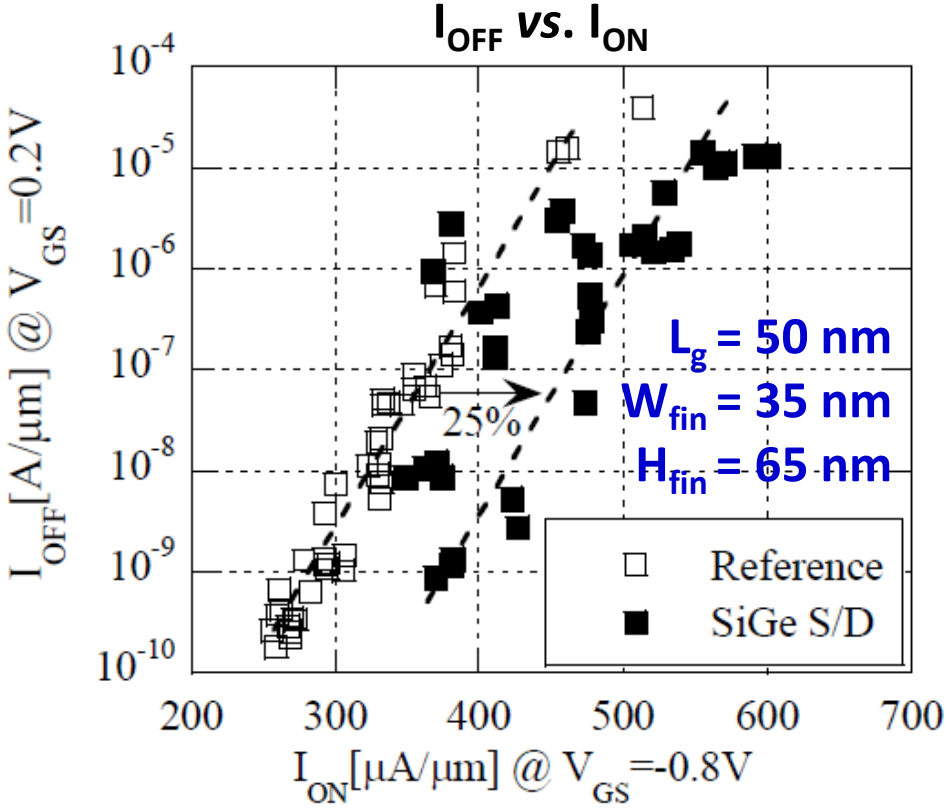
Mobility enhancement (DG)



	Fin Height	Fin Width
nominal	50 nm	50 nm
MAR	100 nm	50 nm
HAR	100 nm	25 nm

I_{DSAT} Increase with SiGe S/D (IMEC)

Process flow:

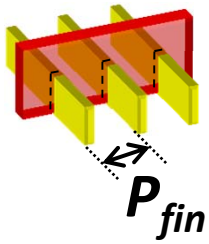


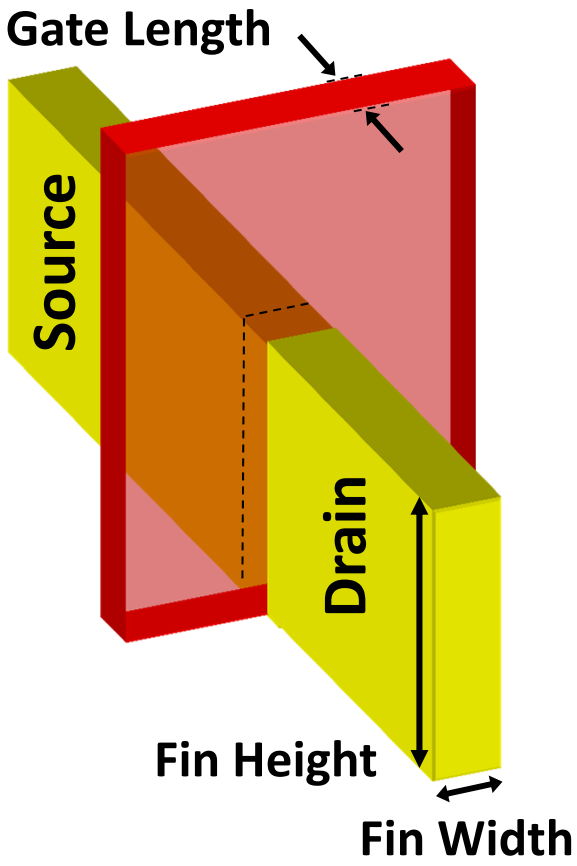
- **25% improvement in I_{DSAT} is achieved with silicon-germanium source/drain, due in part to reduced parasitic resistance**

P. Verheyen *et al.* (IMEC), *Symposium on VLSI Technology Digest*, p. 194-195, 2005

FinFET Design Considerations

- **Fin Width**
  - Determines DIBL
- **Fin Height**
  - Limited by etch technology
  - Tradeoff: layout efficiency *vs.* design flexibility
- **Fin Pitch**
  - Determines layout area
  - Limits S/D implant tilt angle
  - Tradeoff: performance *vs.* layout efficiency

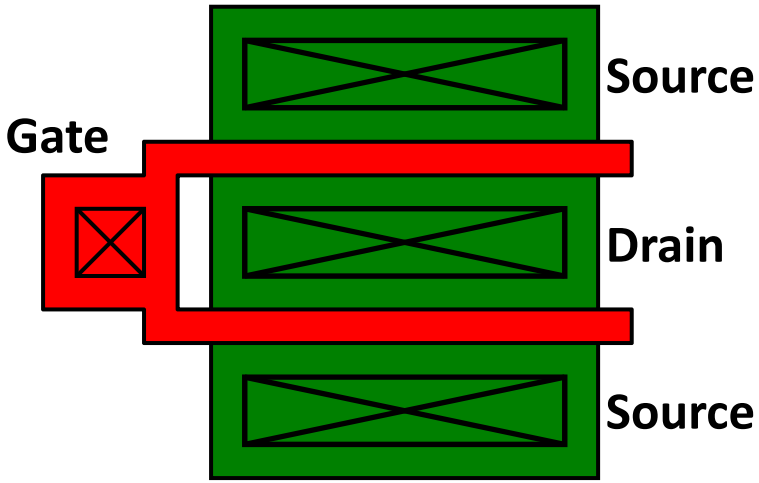




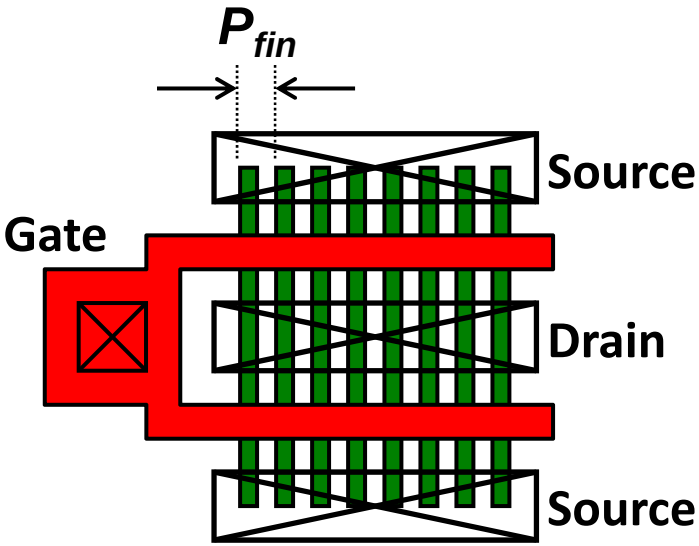
FinFET Layout

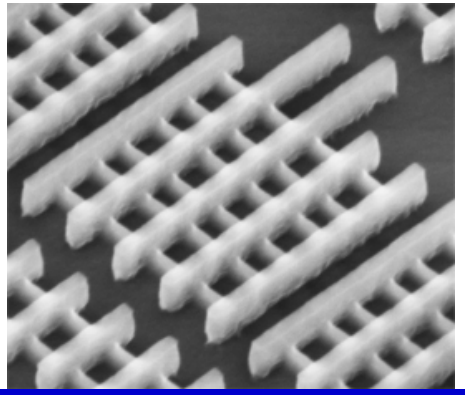
- **FinFET layout is similar to that of a conventional MOSFET.**

Bulk-Si MOSFET



FinFET



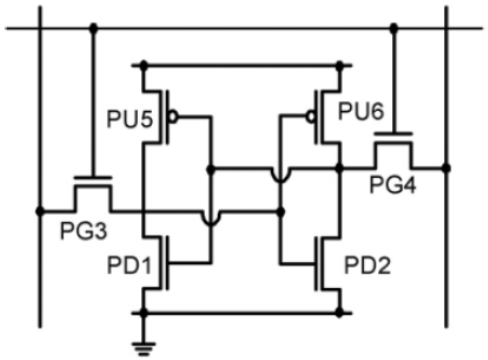


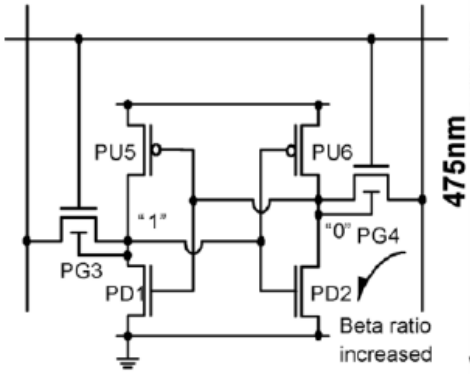
Intel Corp.

FinFET-based SRAM Design

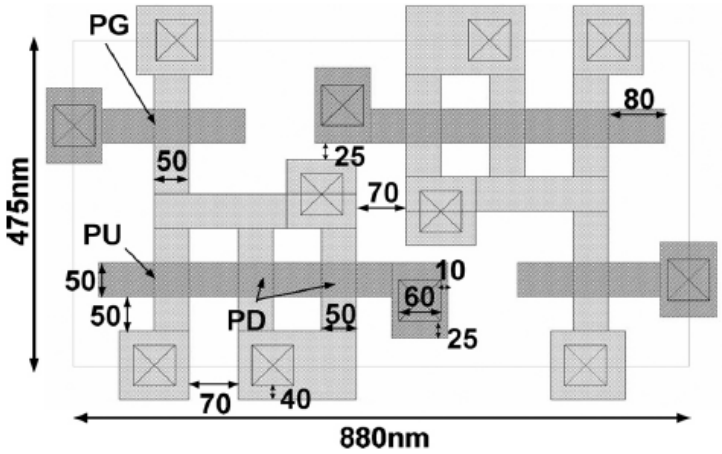
Best Paper Award: Z. Guo, S. Balasubramanian, R. Zlatanovici, T.-J. King, and B. Nikolic, "**FinFET-based SRAM design**," *Int'l Symposium on Low Power Electronics and Design*, pp. 2-7, 2005

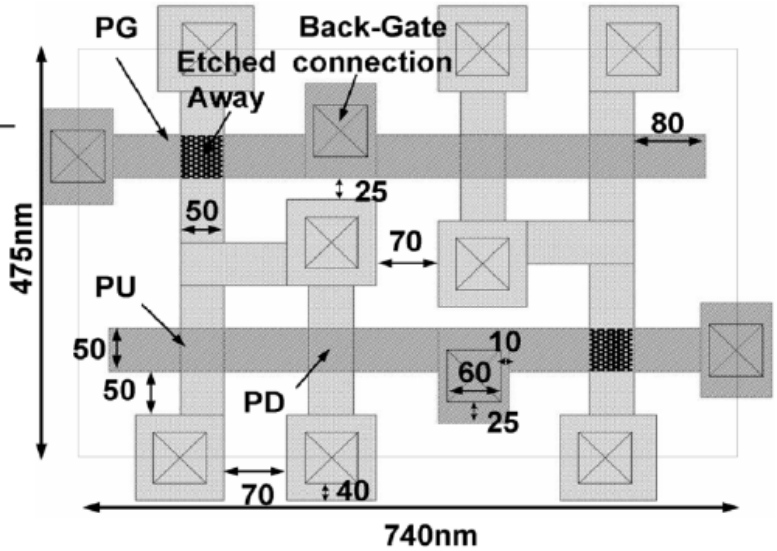
6-T SRAM Cell Designs



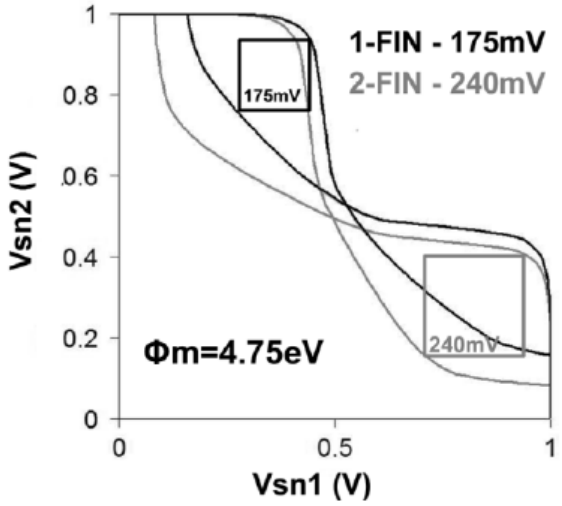


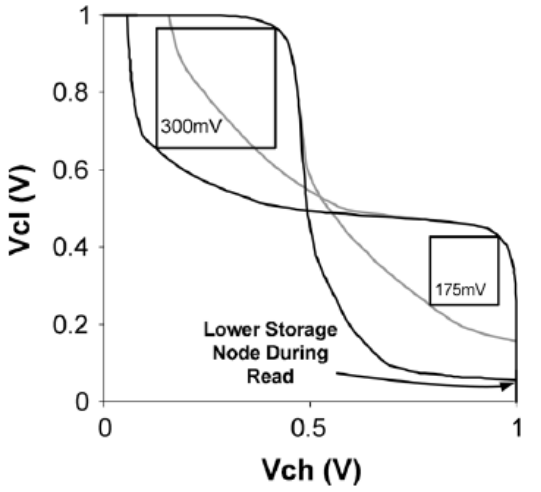
Cell Layouts





Butterfly Curves

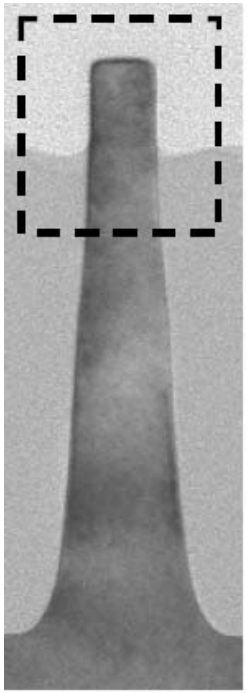




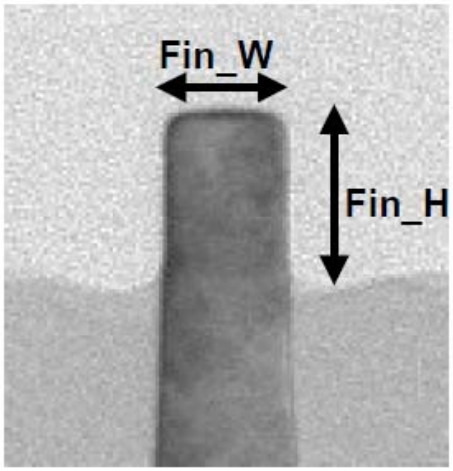
State-of-the-Art FinFETs

22nm/20nm high-performance CMOS technology

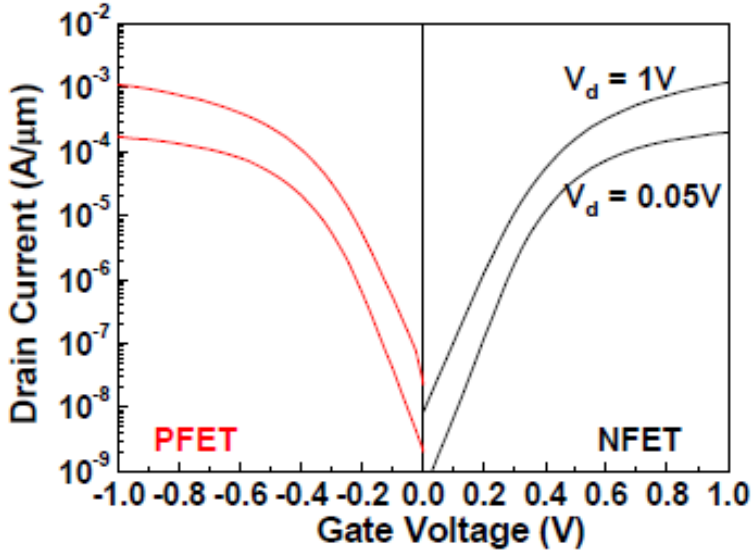
- L_g = 25 nm

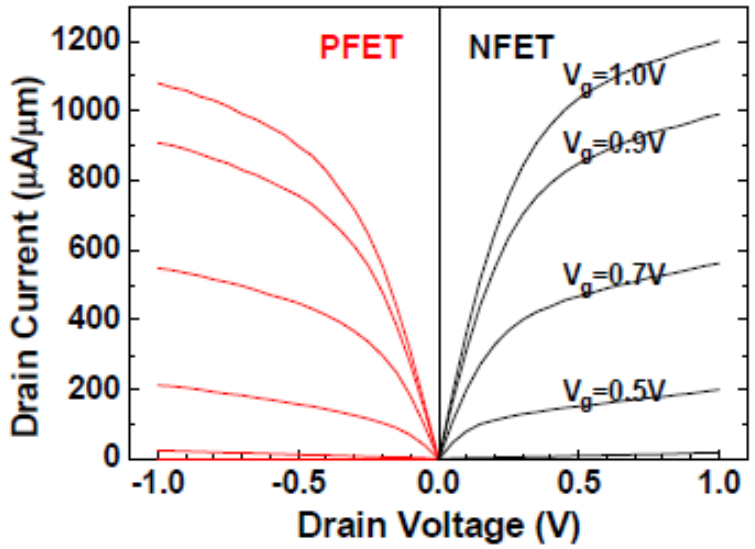


XTEM Images of Fin

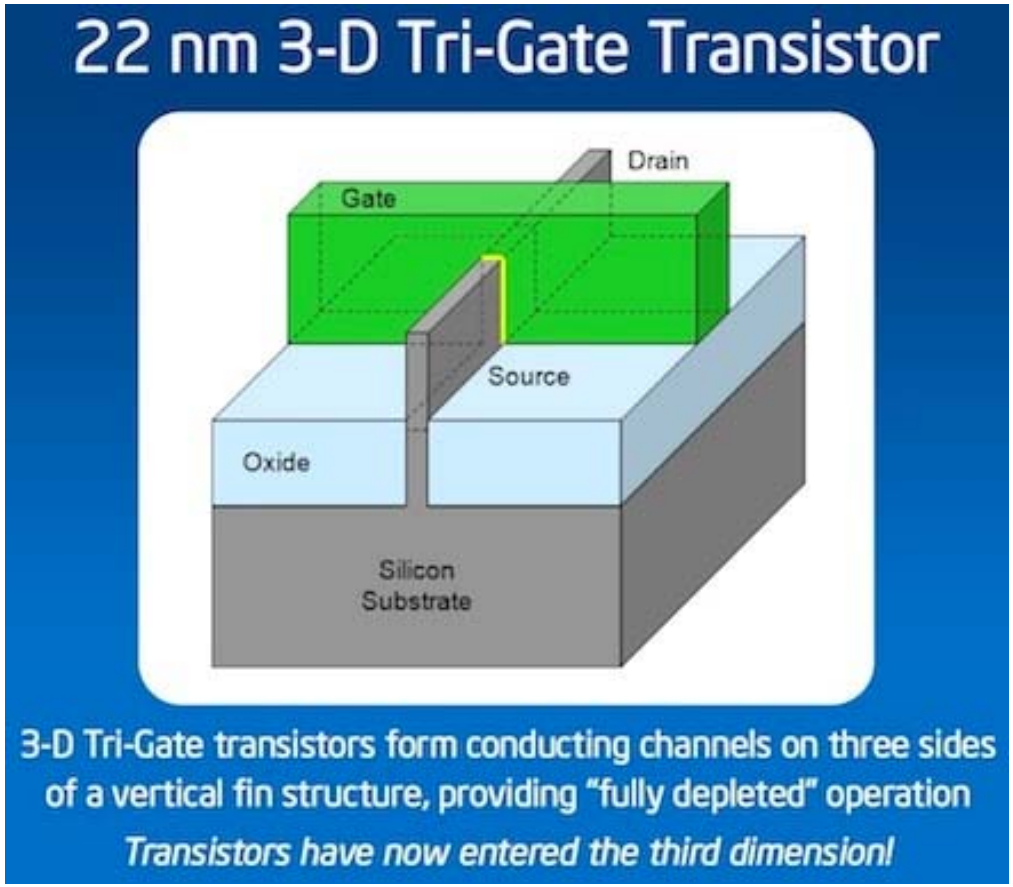


Weff = 2 x Fin_H + Fin_W





May 4, 2011: Intel Announcement



- **Ivy Bridge-based Intel® Core™ family processors will be the first high-volume chips to use 3-D Tri-Gate transistors.**
- **This silicon technology breakthrough will also aid in the delivery of more highly integrated Intel® Atom™ processor-based products…**

Looking to the Future…

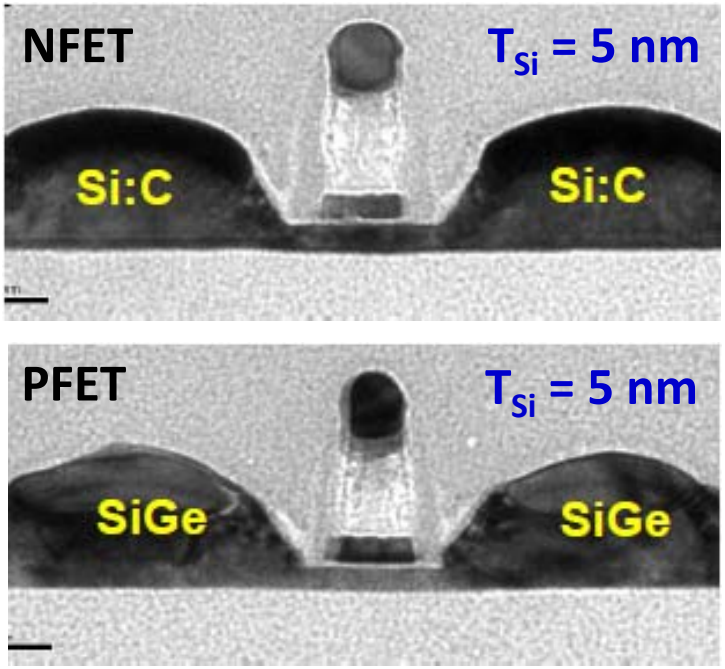
2010 International Technology Roadmap for Semiconductors (ITRS)

	2012	2014	2016	2018	2020	2022	2024
Gate Length	24 nm	18 nm	15 nm	13 nm	11 nm	10 nm	7 nm
Gate Oxide Thickness, T_{OX} (nm)							
Drive Current, I_{DSAT}							

End of Roadmap (always ~15 yrs out)

The Competition: UTB SOI MOSFET

Cross-sectional TEM views of 25 nm UTB SOI devices

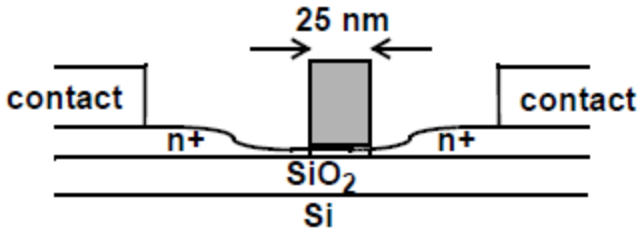


K. Cheng *et al.* (IBM), *Symposium on VLSI Technology Digest*, pp. 128-129, 2011

	20nm ETSOI	22nm Bulk finFET*
L_G (nm)	22	> 25
Pitch (nm)	80-100	100
I_{OFF} (nA/ μm)	1	1
NFET I_{on} (μA/μm)	920	960
PFET I_{on} (μA/μm)	880	850

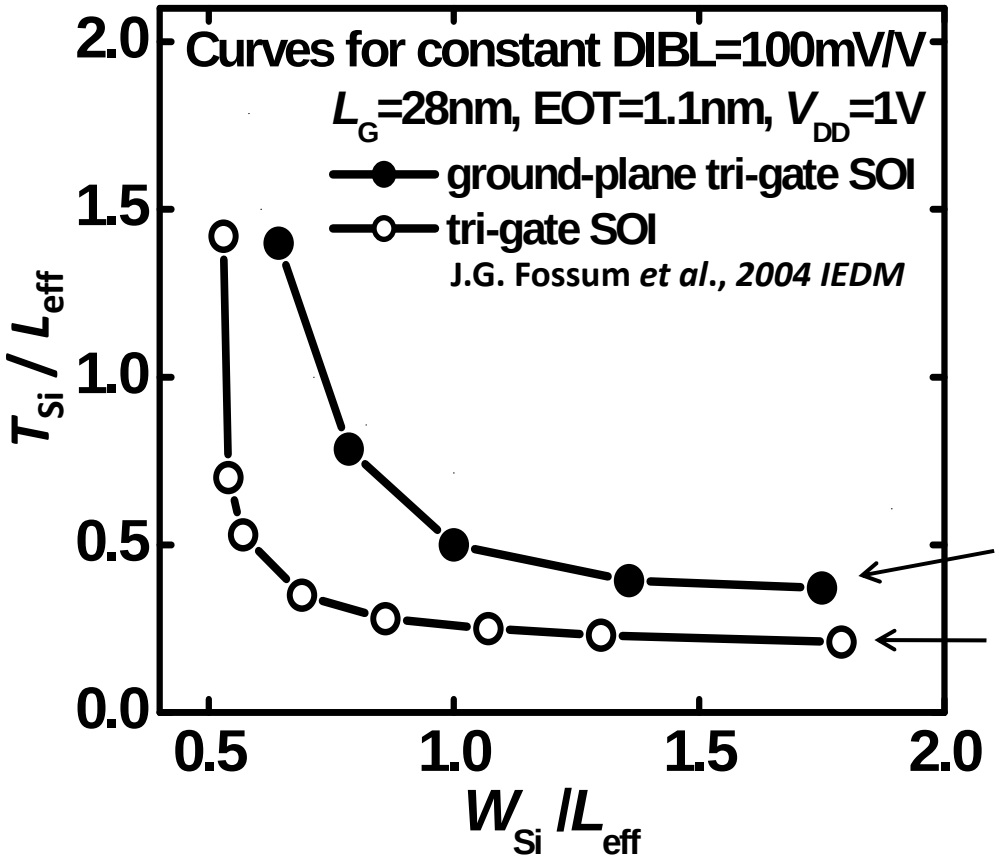
B. Doris, *IEEE SOI Conference* 2011

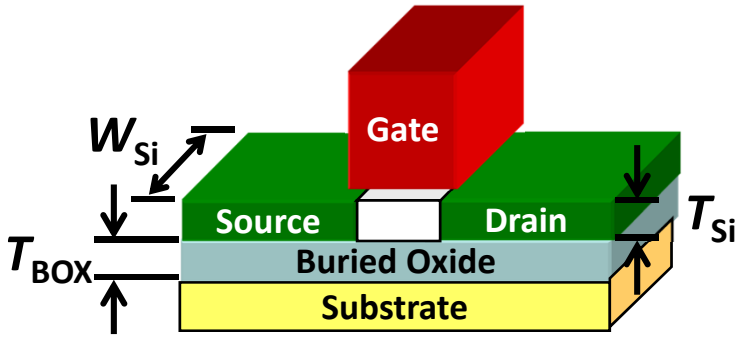
*C.C. Wu *et al.*, *IEEE IEDM*, 2010



UC-Berkeley DARPA AME proposal (Feb. 1997)

Tri-Gate MOSFET Design



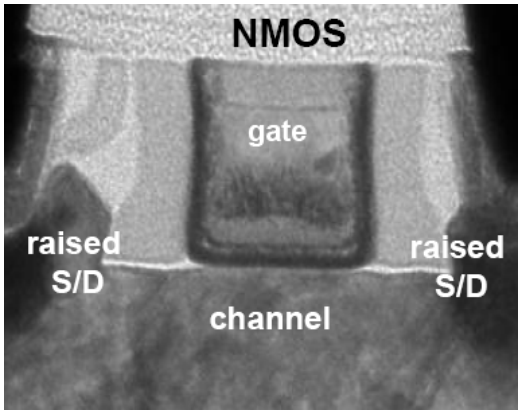


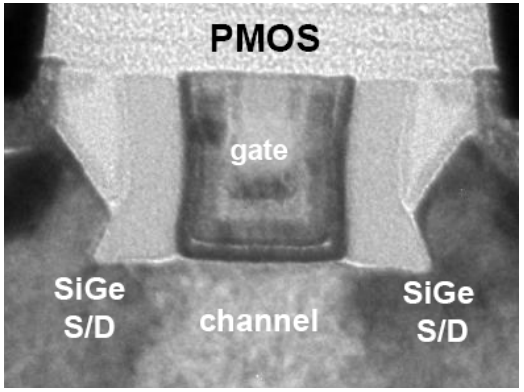
- To ease the fin width requirement, one can
  - decrease T_{si}
  - reduce T_{BOX}

→ reduce fin aspect ratio…

MOSFET Evolution

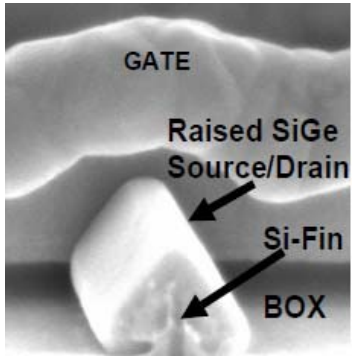
32 nm planar



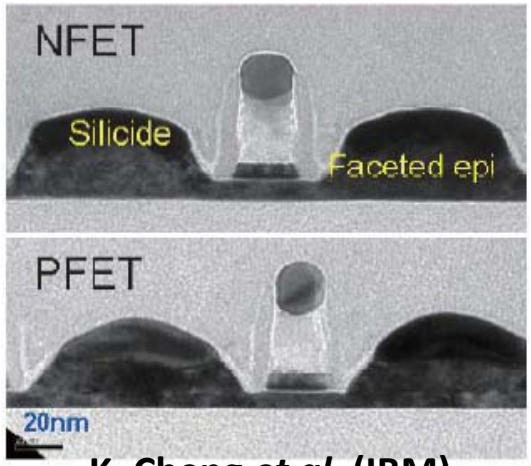


P. Packan *et al*. (Intel), *IEDM* 2009

22 nm thin-body

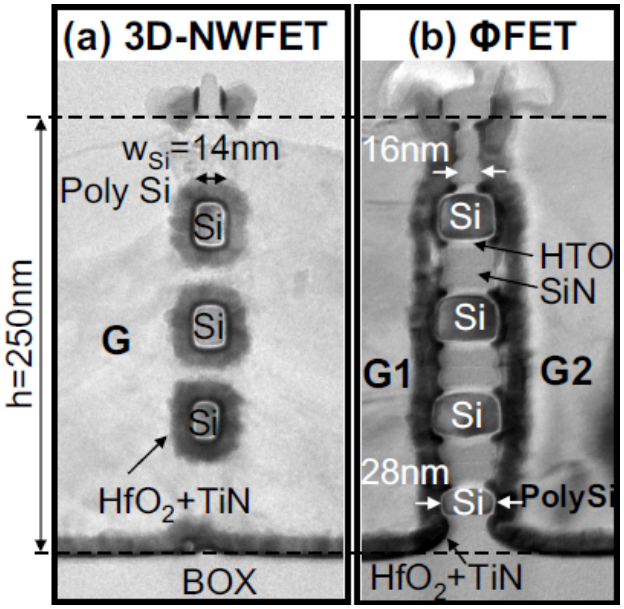


J. Kavalieros *et al*. (IBM) *Symp. VLSI Technology* 2006



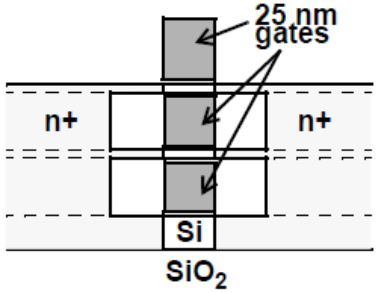
K. Cheng *et al*. (IBM) *Symp. VLSI Technology* 2009

beyond 10 nm nanowires?



C. Dupré *et al*. (CEA-LETI) *IEDM* 2008

UC-Berkeley DARPA AME proposal: (Feb. 1997)



Reflection


Prof. Subramanian


Digh Hisamoto


Hideki Takeuchi


Xuejue Huang


Wen-Chin Lee


Jakub Kedzierski


Yang-Kyu Choi


Stephen Tang

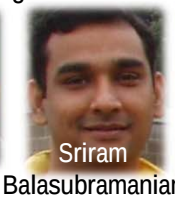

Leland Chang


Nick Lindert


Pushkar Ranade, Charles Kuo, Daewon Ha


Peiqi Xuan


Kyoungsub Shin


Sriram Balasubramanian


Zheng Guo


Radu Zlatanovici


Prof. Nikolic

"The DARPA-sponsored Berkeley work in the 1990s…and then Intel internal research in the 2000s contributed to developing increased confidence that multi-gate transistors would one day be the next step in transistor evolution… Both Intel and Berkeley can take pride in the fruits of university – industry partnership in research."

– Mark Bohr, Intel Senior Fellow

Additional Acknowledgements

- UC Berkeley Microfabrication Laboratory
  - birthplace of the FinFET
- Special thanks to
  - Carol Sitea
  - Sim Kallan and Elise Mills

  for their help in reconstructing history