On May 4, 2011, Intel Corporation announced what it called the most radical shift in semiconductor technology in 50 years. A new 3-dimensional transistor design will enable the production of integrated-circuit chips that operate faster with less power.

Intel Rethinks Chip’s Building Blocks

By Don Clark

Intel Corp. stunned off what it called the most radical shift in semiconductor technology in more than five years, a design that could produce more powerful chips for gadgets without taking their batteries.

The company plans to change a key part of each chip into a vertical, Fin-like structure, a simpler process, the way high-rise buildings pack more office space in a city. The parts being charged—transistors—are the building block of nearly all electronic products; today's microchips can contain billions of the tiny switches.

Intel said its new technology could bring more computing power to smartphones and tablet computers as well as speed corporate data centers—while sharply reducing power consumption.

Though rivals have also been exploring similar technologies, Intel is the first to unveil, in a move the company said it could be a radical breakthrough in high-volume production, a gamble that analysts said could help Intel retain the performance advantages of chips that have largely kept Intel chips out of the smartphone market.

"We've been talking about these 3-D circuits for more than 10 years, but no one has had the confidence to move them into manufacturing," said Dan Hutcheson, a chip-manufacturing specialist with the firm VLSI Research.

Intel executives demonstrated working chips based on the new approach at a gathering Wednesday in San Francisco. They indicated the first microprocessors would likely be targeted for high-end desktop computer and server systems and arrive in early 2012.

For decades, chip manufacturers have raced to shrink the size of components, which increases the performance of chips while decreasing the cost of each computing function. Competition has spurred companies to introduce ever-smaller processors every couple of years.

Intel executives say the shift to 3-D transistors brings more benefits than simply moving to a new generation of manufacturing technology. For example, if designers keep performance constant, the new technology consumes half the power as Intel's existing production method.

"That is an unprecedented gain," said Mark Bohr, who heads the unit of Intel below and leads its development of new manufacturing processes. "We've never achieved that kind of performance gain at low voltage.

Chips designers have long worked in more than two dimensions, with transistors layered by layers of interconnecting wiring, but the shift refers to a part of each transistor that determines how fast electricity flows and how much current may leak out, affecting power consumption.

Intel engineers replaced a flat channel for conducting electrons with a three-dimensional structure surrounded on three sides by a structure called a gate that turns the flow on and off. The three-dimensional shape, Mr. Bohr said, lets more current flow during the "on" state and less current to leak when the transistor is switched "off." Intel disclosed the underlying approach in research papers in 2002, and has spent the intervening years perfecting it. It has opted to shift completely to the new transistors for its next manufacturing process—slated to create chips with circuit dimensions measured at 22 nanometers, or billionths of a meter. Intel's current chips use 32-nanometer technology.

"Outsourcing conventional manufacturing technologies lead to increases costs, and chip companies trying to avoid them. Mr. Bohr said that could mean it could move to the new technology with a 2% to 3% increase in the cost of a finished silicon wafer, each of which contains hundreds of chips.

Others are expected to use the approach at some point, too, but not until they have churned each circuitry beyond 22 nanometers.

The 3-D Tri-Gate transistor is a variant of the FinFET developed at UC-Berkeley, and will be used in Intel's 22-nm microprocessors.
History and Future of the FinFET

Tsu-Jae King Liu

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720-1770 USA

October 12, 2011
Impact of Moore’s Law

Computing Growth Drivers Over Time, 1960-2020E

Transistor Scaling
Investment
Market Growth
Higher Performance, Lower Cost
Increasing Integration

CMOS generation: 1 um ● ● 180 nm ● ● 32 nm

Source: ITU, Mark Lipacis, Morgan Stanley Research

http://www.morganstanley.com/institutional/techresearch/pdfs/2SETUP_12142009_RI.pdf
1996: The Call from DARPA

- 0.25 \( \mu \text{m} \) CMOS technology was state-of-the-art
- DARPA Advanced Microelectronics Program Broad Agency Announcement for 25 nm CMOS technology

1998 International Technology Roadmap for Semiconductors (ITRS)

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<tr>
<td>Technology Node</td>
<td>180 nm</td>
<td>130 nm</td>
<td>100 nm</td>
<td>70 nm</td>
<td>50 nm</td>
<td>35 nm</td>
<td>25 nm</td>
<td>18 nm</td>
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<tr>
<td>Gate Oxide Thickness, ( T_{\text{OX}} ) (nm)</td>
<td>1.9-2.5</td>
<td>1.5-1.9</td>
<td>1.0-1.5</td>
<td>0.8-1.2</td>
<td>0.6-0.8</td>
<td>0.5-0.6</td>
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<tr>
<td>Drive Current, ( I_{\text{DSAT}} )</td>
<td><strong>Solutions</strong></td>
<td><strong>No known</strong></td>
<td><strong>being pursued</strong></td>
<td><strong>solutions</strong></td>
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→ UC-Berkeley project “Novel Fabrication, Device Structures, and Physics of 25 nm FETs for Terabit-Scale Electronics”
- $5.2M over 4 years (June 1997 through July 2001)
MOSFET Basics

Metal Oxide Semiconductor Field-Effect Transistor:

GATE LENGTH, $L_g$

GATE OXIDE THICKNESS, $T_{ox}$

0.25 micron MOSFET XTEM

http://www.eetimes.com/design/automotive-design/4003940/LCD-driver-highly-integrated
MOSFET Operation: Gate Control

Desired characteristics:
- High ON current
- Low OFF current

N-channel MOSFET cross-section

- Current between Source and Drain is controlled by the Gate voltage.
- “N-channel” & “P-channel” MOSFETs operate in a complementary manner
  “CMOS” = Complementary MOS

Electron Energy Band Profile

\[ n(E) \propto \exp\left(-\frac{E}{kT}\right) \]

Increasing \( E \) = \( V_{GS} \) (Source) to Drain

Inverse slope is subthreshold swing, \( S \) [mV/dec]

[Diagram of MOSFET with gate oxide, N+ Source, P Body, N+ Drain, and Electron Energy Band Profile]
Inversion-Layer Thickness

The average depth of the inversion layer below the Si/oxide interface is referred to as the \textit{inversion-layer thickness}.

- 2-3 nm (depending on gate voltage)

\[ V_{GS} > V_{TH} \]

\[ N_{sub} = 2 \times 10^{17} \text{ cm}^{-3}, \quad T_{ox} = 50 \text{Å} \]

\[ E_s = 1.7 \times 10^5 \text{ (V/cm)} \]

\[ \text{Model: } 5.7 \times 10^{-7} \left( 1 + \frac{(V_g - 3V_t)}{2T_{ox}} \right)^{0.7} \]

\[ \text{NMOS (electron) only} \]
CMOS Devices and Circuits

CIRCUIT SYMBOLS
N-channel MOSFET
P-channel MOSFET

CMOS INVERTER CIRCUIT
\[ V_{IN} \rightarrow V_{OUT} \]

INVERTER LOGIC SYMBOL

CMOS NAND GATE

NOT AND (NAND) TRUTH TABLE

\[
\begin{array}{ccc}
A & B & F \\
0 & 0 & 1 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]

STATIC MEMORY (SRAM) CELL

WORD LINE

BIT LINE

0 or 1

0 or 1

0

1
The greater the capacitive coupling between Gate and channel, the better control the Gate has over the channel potential.

→ higher $I_{ON}/I_{OFF}$ for fixed $V_{DD}$, or lower $V_{DD}$ to achieve target $I_{ON}/I_{OFF}$

→ reduced drain-induced barrier lowering (DIBL):
MOSFET in ON State ($V_{GS} > V_{TH}$)

\[ I_D = W \times v \times Q_{inv} \]

- **width**
- **velocity**
- **inversion-layer charge density**

\[ v \propto \mu_{eff} \]

- **mobility**

\[ Q_{inv} \propto C_{ox} (V_{GS} - V_{TH})^n \]

- **gate-oxide capacitance**
- **gate overdrive**

DIBL: $V_{TH}$ decreasing with $V_{DS}$
Effective Drive Current ($I_{EFF}$)

CMOS inverter chain:

$\begin{align*}
&V_1 \rightarrow V_2 \rightarrow V_3 \\
&V_{DD} \rightarrow S \rightarrow D \rightarrow V_{OUT} \\
&V_{IN} \rightarrow GND
\end{align*}$

Effective Drive Current ($I_{EFF}$)

$I_{EFF} = \frac{I_H + I_L}{2}$

$I_H$ (DIBL = 0)

$I_{DSAT}$

$V_{IN} = V_{DD}$

$V_{IN} = 0.83V_{DD}$

$V_{IN} = 0.75V_{DD}$

$V_{IN} = 0.5V_{DD}$

NMOS DRAIN CURRENT

NMOS DRAIN VOLTAGE = $V_{OUT}$

M. H. Na et al., IEDM Technical Digest, pp. 121-124, 2002
Performance Boosters

- Strained channel regions $\rightarrow \mu_{\text{eff}} \uparrow$
- High-k gate dielectric and metal gate electrodes $\rightarrow C_{\text{ox}} \uparrow$

Cross-sectional TEM views of Intel’s 32 nm CMOS devices

P. Packan et al., IEDM Technical Digest, pp. 659-662, 2009
A Journey Back through Time...
The UC-Berkeley AME Team

- **PI/co-PIs:** Chenming Hu, Jeff Bokor, Tsu-Jae King
- **Post-doc:** Vivek Subramanian
- **Industrial visitors:**
  - Digh Hisamoto (Hitachi CRL)
  - Hideki Takeuchi (now with Mears Technologies)
- **Graduate students (alphabetical order):**
  - Leland Chang (now with IBM TJ Watson Research)
  - Yang-Kyu Choi (now with KAIST)
  - Xuejue “Cathy” Huang (now with Intel Corp.)
  - Jakub Kedzierski (now with MIT Lincoln Lab)
  - Charles Kuo (now with Intel Corp.)
  - Wen-Chin Lee (now with TSMC)
  - Nick Lindert (now with Intel Corp.)
  - Stephen Tang (now with Intel Corp.)
Why New Transistor Structures?

- Off-state leakage ($I_{OFF}$) must be suppressed as $L_g$ is scaled down
  - allows for reductions in $V_{TH}$ and hence $V_{DD}$

- Leakage occurs in the region away from the channel surface

→ Let’s get rid of it!

Thin-Body MOSFET:

- “Silicon-on-Insulator” (SOI) Wafer
Thin-Body MOSFETs

- $I_{OFF}$ is suppressed by using an adequately thin body region.
  - Body doping can be eliminated
    - higher drive current due to higher carrier mobility
    - Reduced impact of random dopant fluctuations (RDF)

**Ultra-Thin Body (UTB)**

$T_{Si} < \frac{1}{4} \times L_g$

**Double-Gate (DG)**

$T_{Si} < \frac{2}{3} \times L_g$
Double-Gate MOSFET Structures

**PLANAR:**

**VERTICAL**

**FINFET:**
DELTA MOSFET


- Improved gate control observed for $W_g < 0.3 \, \mu m$
  - $L_{EFF} = 0.57 \, \mu m$
Double-Gate FinFET

- Self-aligned gates straddle narrow silicon fin
- Current flows parallel to wafer surface

Gate Length \( L_g \)

Fin Height \( H_{\text{fin}} = W \)

Fin Width \( W_{\text{fin}} = T_{\text{Si}} \)
1998: First n-channel FinFETs

“A folded-channel MOSFET for deep-sub-tenth micron era,”

- Devices with $L_g$ down to 17 nm were successfully fabricated
1999: First p-channel FinFETs


![Schematic drawing of FinFET](image1)

- $L_g = 18$ nm
- $W_{fin} = 15$ nm
- $H_{fin} = 50$ nm

![Transmission Electron Micrograph](image2)
Recognition

DARPA Significant Technical Achievement Award
presented at DARPATECH 2000 Symposium
2000: Call from the Industry

• SRC Solicitation: Novel Devices for Information Processing

  “Proposals are sought related to novel device structures, arrays or nanosystems that have the potential to process and store information at a speed, density and energy efficiency that greatly exceed (100x) those projected for silicon CMOS at the 35-nm node.”

→ UCB Project: “FinFET -- A Double-Gate MOSFET Structure”
  – Task 1: Develop a FinFET process flow compatible with a conventional planar CMOS process.
  – Task 2: Demonstrate compatibility of the FinFET structure with a production environment.
  – Funded October 2000 through September 2003 @ $300k/yr
  – New graduate students: Pushkar Ranade (now with Intel Corp.)
    Peiqi Xuan (now with Marvell Technology)

• Chenming Hu goes to Taiwan Semiconductor Manufacturing Company (2001-2004)
FinFET Structures

Original:

Improved:
What is claimed is:

1. A method of fabricating a double gate MOSFET device comprising the steps of:
   a) providing a silicon on insulator (SOI) substrate with a first silicon layer overlying an insulating layer and having an exposed major surface,
   b) providing an etchant mask on the major surface,
   c) patterning the etchant mask to define source, drain, and channel regions and expose surrounding portions of the silicon layer,
   d) etching the exposed silicon layer and forming source, drain, and channel regions extending from the insulator layer, the channel being a fin with a top surface and two opposing sidewalls,
   e) forming a gate dielectric on sidewalls of the channel region,
   f) depositing gate material over the etchant mask and the gate dielectric,
   g) selectively masking and etching the gate material to form a gate on the top surface and sidewalls of the channel region and separated from the channel region by the gate dielectric and the etchant mask,
   h) forming dielectric spacers between the gate and the source and drain regions, and
   i) doping the source and drain regions.

+ 27 additional claims...
• To adequately suppress DIBL, $L_g/W_{\text{fin}} > 1.5$

→ Challenge for lithography!

Sub-Lithographic Fin Patterning

Spacer Lithography
a.k.a. Sidewall Image Transfer (SIT) and Self-Aligned Double Patterning (SADP)

1. Deposit & pattern sacrificial layer
2. Deposit mask layer (SiO₂ or Si₃N₄)
3. Etch back mask layer to form “spacers”
4. Remove sacrificial layer; etch SOI layer to form fins

Note that fin pitch is 1/2× that of patterned layer
Benefits of Spacer Lithography

- Spacer litho. provides for better CD control and uniform fin width

- SEM image of FinFET with spacer-defined fins:

**Spacer lithography** → uniform $W_{fin}$

**Conventional litho.** → nonuniform $W_{fin}$

Spacer-defined FinFETs

Y.-K. Choi, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Anderson, T.-J. King, J. Bokor, and C. Hu,
"Sub-20nm CMOS FinFET technologies,"

\[ L_g = 60 \text{ nm}, \quad W_{\text{fin}} = 40 \text{ nm} \]
2001: 15 nm FinFETs

Y.-K. Choi, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Anderson, T.-J. King, J. Bokor, C. Hu,
"Sub-20nm CMOS FinFET technologies,"

Transfer Characteristics

Output Characteristics

\[ W_{\text{fin}} = 10 \text{ nm}; \quad T_{\text{ox}} = 2.1 \text{ nm} \]
2002: 10 nm FinFETs


- These devices were fabricated at AMD, using optical lithography.
DARPA/SRC Focus Center Research Program

• Center for Materials, Structures, and Devices (MSD)
  – Approaches for enhancing FinFET performance
  – Funded April 2001 through August 2003
  – Student: Daewon Ha (now with Samsung Electronics)

• Center for Circuits and Systems Solutions (C2S2)
  – FinFET-based circuit design
  – Funded August 2003 to July 2006
  – Students:
    • Sriram Balasubramanian (now with GLOBALFOUNDRIES)
    • Zheng Guo (now with Intel)
    • Radu Zlatanovici (now with Intel Corp.)
FinFET Process Refinements


Fin-sidewall smoothening for improved carrier mobilities

Gate work function tuning for $V_{TH}$ adjustment
FinFET Reliability


- Narrower fin $\rightarrow$ improved hot-carrier (HC) immunity
- HC lifetime and oxide $Q_{BD}$ are also improved by smoothening the Si fin sidewall surfaces (by $H_2$ annealing)
Tri-Gate FET (Intel Corp.)

L_g = 60 nm
W_{fin} = 55 nm
H_{fin} = 36 nm

**Bulk FinFET (Samsung Electronics)**

- FinFETs can be made on bulk-Si wafers
  - **lower cost**
  - **improved thermal conduction**
- 90 nm $L_g$ FinFETs demonstrated
  - $W_{\text{fin}} = 80$ nm
  - $H_{\text{fin}} = 100$ nm
  - DIBL = 25 mV

---

C.-H. Lee et al., *Symposium on VLSI Technology Digest*, pp. 130-131, 2004
2004: High-k/Metal Gate FinFET

2005: Strained FinFET Technology

K. Shin and T.-J. King,
“Dual stress capping layer enhancement study for hybrid orientation FinFET CMOS technology,”
IEEE International Electron Devices Meeting Technical Digest, , pp. 988-991, 2005

3-D structure used for simulations

Mobility enhancement (DG)

<table>
<thead>
<tr>
<th></th>
<th>100 NMOS (tensile cap)</th>
<th>110 PMOS (compressive cap)</th>
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<tr>
<td>Mobility Change [%]</td>
<td></td>
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<tr>
<td>nominal</td>
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<tr>
<td>MAR</td>
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<td>HAR</td>
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<tr>
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<th>Fin Height</th>
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<tr>
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<tr>
<td>MAR</td>
<td>100 nm</td>
<td>50 nm</td>
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<tr>
<td>HAR</td>
<td>100 nm</td>
<td>25 nm</td>
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$I_{DSAT}$ Increase with SiGe S/D (IMEC)

Process flow:

- 25% improvement in $I_{DSAT}$ is achieved with silicon-germanium source/drain, due in part to reduced parasitic resistance.

P. Verheyen et al. (IMEC), Symposium on VLSI Technology Digest, p. 194-195, 2005
FinFET Design Considerations

- **Fin Width**
  - Determines DIBL

- **Fin Height**
  - Limited by etch technology
  - Tradeoff: layout efficiency vs. design flexibility

- **Fin Pitch**
  - Determines layout area
  - Limits S/D implant tilt angle
  - Tradeoff: performance vs. layout efficiency
FinFET Layout

• FinFET layout is similar to that of a conventional MOSFET.

Bulk-Si MOSFET

FinFET

Source

Drain

Gate

Source

Drain

Source

Intel Corp.
**FinFET-based SRAM Design**


**6-T SRAM Cell Designs**

**Cell Layouts**

**Butterfly Curves**

\[ \Phi_m = 4.75 eV \]
State-of-the-Art FinFETs

22nm/20nm high-performance CMOS technology
• $L_g = 25$ nm

C.C. Wu et al. (TSMC), IEEE International Electron Devices Meeting, 2010
May 4, 2011: Intel Announcement

- Ivy Bridge-based Intel® Core™ family processors will be the first high-volume chips to use 3-D Tri-Gate transistors.
- This silicon technology breakthrough will also aid in the delivery of more highly integrated Intel® Atom™ processor-based products...

http://newsroom.intel.com/community/intel_newsroom/blog/2011/05/04/intel-reinvents-transistors-using-new-3-d-structure
Looking to the Future...

### 2010 International Technology Roadmap for Semiconductors (ITRS)

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<tbody>
<tr>
<td>Gate Length</td>
<td>24 nm</td>
<td>18 nm</td>
<td>15 nm</td>
<td>13 nm</td>
<td>11 nm</td>
<td>10 nm</td>
<td>7 nm</td>
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<tr>
<td>Gate Oxide Thickness, $T_{OX}$ (nm)</td>
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<td>Drive Current, $I_{DSAT}$</td>
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End of Roadmap (always ~15 yrs out)
The Competition: UTB SOI MOSFET

Cross-sectional TEM views of 25 nm UTB SOI devices

NFET

Si:C

PFET

SiGe

$T_{Si} = 5$ nm

K. Cheng et al. (IBM), Symposium on VLSI Technology Digest, pp. 128-129, 2011

B. Doris, IEEE SOI Conference 2011

UC-Berkeley DARPA AME proposal (Feb. 1997)

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<tr>
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<th>20nm ETSOI</th>
<th>22nm Bulk finFET*</th>
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<tbody>
<tr>
<td>$L_G$ (nm)</td>
<td>22</td>
<td>&gt; 25</td>
</tr>
<tr>
<td>Pitch (nm)</td>
<td>80-100</td>
<td>100</td>
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<td>$I_{OFF}$ (nA/μm)</td>
<td>1</td>
<td>1</td>
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<tr>
<td>NFET $I_{on}$ (μA/μm)</td>
<td>920</td>
<td>960</td>
</tr>
<tr>
<td>PFET $I_{on}$ (μA/μm)</td>
<td>880</td>
<td>850</td>
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*C.C. Wu et al., IEEE IEDM, 2010
Tri-Gate MOSFET Design

Curves for constant DIBL=100mV/V

$L_g=28\text{nm}$, $EOT=1.1\text{nm}$, $V_{DD}=1\text{V}$

ground-plane tri-gate SOI

tri-gate SOI

J.G. Fossum et al., 2004 IEDM

To ease the fin width requirement, one can

- decrease $T_{si}$
- reduce $T_{BOX}$

→ reduce fin aspect ratio...
MOSFET Evolution

32 nm planar

22 nm thin-body

Beyond 10 nm nanowires?

J. Kavalieros et al. (IBM)
Symp. VLSI Technology 2006

P. Packan et al. (Intel),
IEDM 2009

C. Dupré et al. (CEA-LETI)
IEDM 2008

K. Cheng et al. (IBM)
Symp. VLSI Technology 2009

UC-Berkeley DARPA AME proposal:
(Feb. 1997)

UC-Berkeley DARPA AME proposal:
(Feb. 1997)
“The DARPA-sponsored Berkeley work in the 1990s...and then Intel internal research in the 2000s contributed to developing increased confidence that multi-gate transistors would one day be the next step in transistor evolution... Both Intel and Berkeley can take pride in the fruits of university – industry partnership in research.”

— Mark Bohr, Intel Senior Fellow
Additional Acknowledgements

• UC Berkeley Microfabrication Laboratory
  – birthplace of the FinFET

• Special thanks to
  – Carol Sitea
  – Sim Kallan and Elise Mills

for their help in reconstructing history