Distinguished Lecture Series

EECS COLLOQUIUM

Spring 2016

Wednesday
January 27
4:00 - 5:00 pm

Refreshments
served at 3:30

Hewlett-Packard Auditorium
306 Soda Hall

Transforming Nanodevices into Nanosystems: The N3XT 1,000X

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Abstract

The computing demands of future abundant-data applications far exceed the capabilities of today's electronics, and cannot be met by isolated improvements in transistor technologies, memories, or integrated circuit (IC) architectures alone. Transformative nanosystems, which leverage the unique properties of emerging nanotechnologies to create new IC architectures, are required to deliver unprecedented performance and energy efficiency. However, emerging nanomaterials and nanodevices face major obstacles such as inherent imperfections and variations. Thus, realizing working circuits, let alone transformative nanosystems, has been infeasible.

The N3XT (Nano-Engineered Computing Systems Technology) approach overcomes these challenges through recent advances across the computing stack: (a) transistors using nanomaterials such as one-dimensional carbon nanotubes (and two-dimensional semiconductors) for high performance and energy efficiency, (b) high-density non-volatile resistive and magnetic memories, (c) Ultra-dense (e.g., monolithic) three-dimensional integration of logic and memory for fine-grained connectivity, (d) new architectures for computation immersed in memory, and (e) new materials technologies and their integration for efficient heat removal.

N3XT hardware prototypes represent leading examples of transforming scientifically-interesting nanomaterials and nanodevices into actual nanosystems. Compared to conventional approaches, N3XT architectures promise to improve the energy efficiency of abundant-data applications significantly, in the range of three orders of magnitude, thereby enabling new frontiers of applications for both mobile devices and the cloud.

Biography

Professor Subhasish Mitra directs the Robust Systems Group in the Department of Electrical Engineering and the Department of Computer Science of Stanford University, where he is the Chambers Faculty Scholar of Engineering. Before joining Stanford, he was a Principal Engineer at Intel.

Prof. Mitra's research interests include robust systems, VLSI design, CAD, validation and test, emerging nanotechnologies, and emerging neuroscience applications. His X-Compact technique for test compression has been key to cost-effective manufacturing and high-quality testing of a vast majority of electronic systems, including numerous Intel products.

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