Frequency Translation Techniques for High-Integration High-Selectivity Multi-Standard Wireless Communication Systems

by

Jacques Christophe Rudell

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Although a thesis published at any university may only have one name on the cover, there are undoubtedly many others who have made a critical contribution toward the eventual completion of such a large endeavor. This is certainly true for both myself and this thesis. Without the help, advice, and encouragement of many individuals this work would have never been completed. I would not characterize my life over the last few years as fun, however it has certainly been an interesting journey. The people you meet, the friends you make, and life's little experiences make living as a graduate student, particularly in Berkeley, very interesting.

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If fellow graduate students could be considered great support, then the staff at Berkeley could be thought of as a strong foundation. I am very grateful for the many staff members who work hard everyday to make the graduate student experience in electrical engineering, at Berkeley, A LOT less painful. In the grad. office, I thank Ruth Gjerde and Mary Byrnes for the many useful tips on navigating the Berkeley bureaucracy. I also thank many of the assistants to Professor Gray who have helped out on many items, particularly with purchase orders, including Carol Sitea, Dianne Chang, Flora Oviedo, Marilyn Witbeck, and Deirdre Bauer. Other staff members who came to the rescue on numerous occasions include Tom Boot, Elise Mills, Kevin Zimmerman, Sue Mellers, and Brian Richards.

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To my Parents
Jackson and Anne-Marie Rudell

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Chapter 1

Introduction

1.1 Recent Trends in Wireless Communication Technologies

The 15 years prior to the written form of this thesis has seen a tremendous growth in the wireless communication market. A few years ago, in the early 1990s, cellular telephones were considered a luxury affordable by only upper income individuals. In addition, such mobile communication devices were realized with bulky and power hungry hardware, limiting their practical use in everyday life. Today the growth in the number of users utilizing portable communication systems becomes plainly obvious when walking down a busy city street or across a college campus where one may observe several people conversing over a mobile phone. This growth in the mobile communications market has been fueled by a continued reduction in the cost, size and increased battery life of the hardware which is used to realize modern mobile wireless devices [1.1] (see figure 1). Moreover, this size and cost reduction has enabled a whole new class of applications used by such devices. New consumer applications for mobile communications include the Global Positioning System (GPS), used by weekend hikers and recreational boaters, to wireless meter reading used by utility companies to allow rapid acquisition of monthly home electric and water usage. Today one might step into a cafe and notice several customers sitting at a table, working with a laptop

networked to the internet via a mobile communication device. Each successive generational improvement in communications hardware further promotes the number of consumers utilizing existing applications and enables new applications for wireless systems.

Commensurate with the explosive growth in the wireless communication market is a proliferation in the standards which dictate how the mobile devices will communicate with each other. Between wireless communications applications, and even within a given application, there are vastly differing requirements on the hardware which is used to realize modern radios. Examples again might include cellular telephony, where in the United States there are several digital and one analog standards utilized by various service providers. Today one might buy a cellular phone which uses the North American Digital Cellular Standard (IS-95) or the Analog Mobile Phone (AMPS) standard, or any one of half a dozen other cellular standards. Likewise, any given cellular phone in Europe might utilize AMPS (but on a different carrier frequency than the US) or GSM (Global System Mobile). Therefore, one phone typically operates off of one or at most two standards, and is rendered useless when moving either to other regions of the country, which don't subscribe to a phone's standard, or between countries, which at a minimum, might have similar standards, but operate on a different carrier frequency. Adding to this, there are now applications which require the services provided by multiple RF platforms (standards). In the US, the FCC has mandated that all cellular phones sold after the year 2001 must have the ability to report a phone's position when an emergency 911 called has been placed. Many envision the realization of such a phone through the ability to use the Global Positioning System (GPS). This would require a mobile cellular phone to have the hardware capable of utilizing both a cellular phone standard as well as GPS. Other examples of multiple RF platforms become obvious in the data communication arena, where users might have a laptop or Personal Communications Device (PDA) that they would like to operate off of both an indoor Wireless Local Area Network (WLAN) standard while inside a building, then

move to a longer range cellular standard once the PDA has been moved to an outdoor environment.

(a) (b) (c)

Figure 1. (a) Martin Cooper who is often credited with making the first cell phone call using (b) a Motorola DYNA-TAC (1973). This phoned weighed 2.5 lbs and had a form factor of 9 x 5 x 1.75 inches with a 35 minute talk time. (c) 1999 Motorola StarTac 70000. Modern cell phones often have talk times in excess of 5 hours, weigh less than 4 ounces with form factors below 4.0 x 1.8 x 0.7 inches.

Concurrent with the trends in the wireless communications industry described above is a parallel advancement in semiconductor technologies. Moore's Law states that every 18 months the density of silicon technologies will increase by 2x. This trend may be observed in figure 2 where the relative f_t (a common figure of merit for the speed of a single transistor) is plotted verses the year. Particularly interesting are the trends for common digital CMOS technologies. It was only recently, in the early 1990s, that researchers began investigating the potential of using digital CMOS processes to implement high frequency "front-end" radio components [1.2]. Implementation of any analog circuitry in contemporary digital silicon CMOS has a particular advantage with respect to cost, which is enabled by the sheer volume of digital IC products relative to those in the mixed signal and analog markets. In addition, integrating the analog

transceiver components of a wireless communications system in CMOS holds the advantage that potentially someday, all of the analog and digital components of a mobile transceiver could be integrated on to a single piece of silicon. With the substantial advantages in terms of cost and size, clearly, the demand exists for new radio architectures and innovative circuit design techniques which facilitate high levels of radio integration in CMOS.

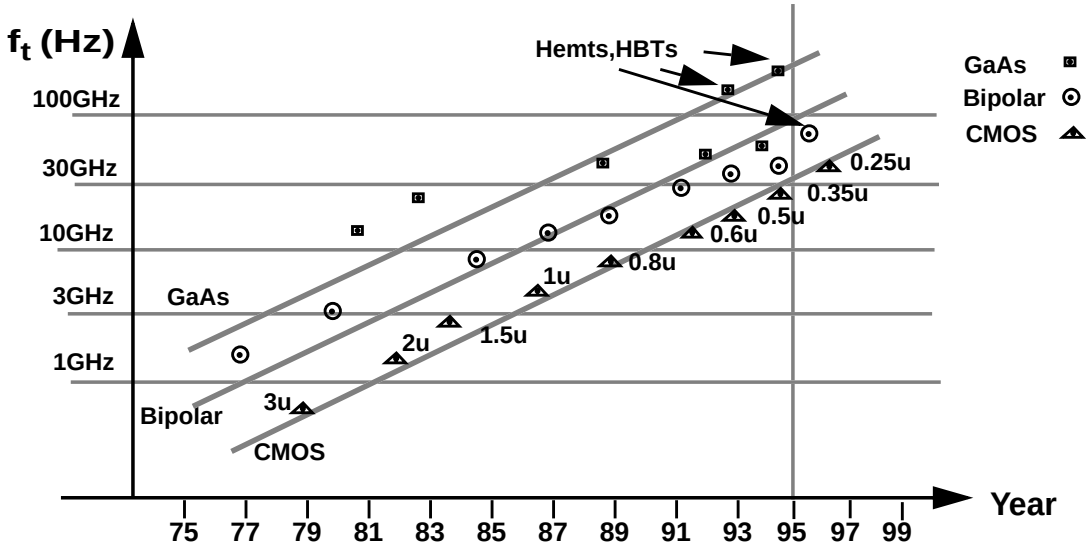
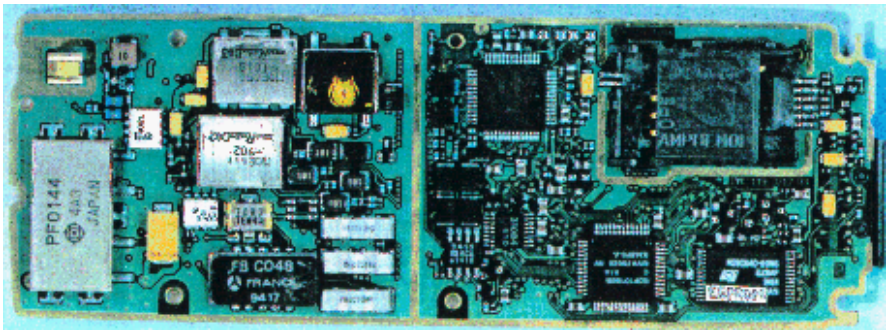


Figure 2. Increasing CMOS device (f_t) throughout the 1990s.

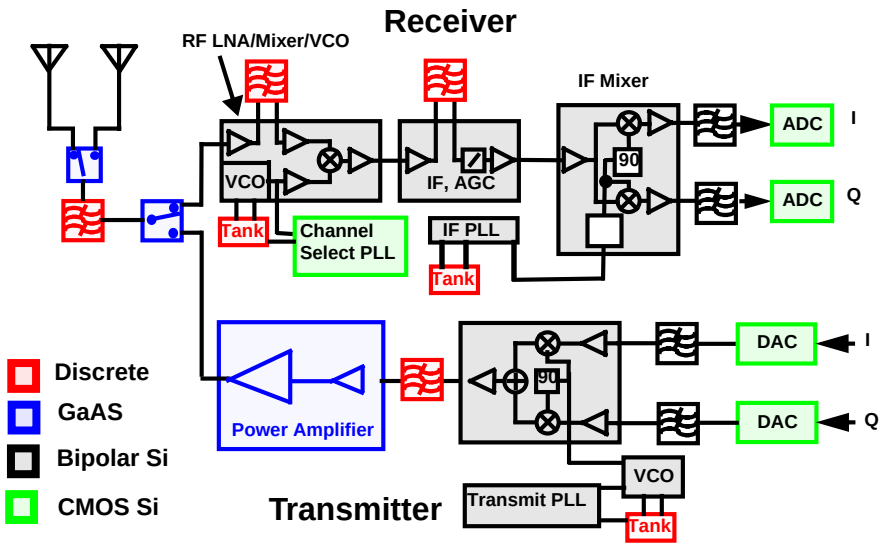
1.2 Transceiver Analog Front-End Hardware.

As mentioned before existing hardware solutions for the analog portion of a transceiver are typically realized with a multi-component solution. As an example, figure 3(a) shows a modern cellular phone with the printed circuit board exposed. In figure 3(b) is shown a block diagram illustrating a conventional super-heterodyne transceiver system. The individual components which are used to realize most transceivers in production today, are done so with several integrated circuit technologies which include Gallium Arsenide for the higher frequency front-end components, Silicon Bipolar for either Radio Frequency (RF) front-end components and/or the realization of any Intermediate Frequency (IF) components, and silicon

CMOS for the lower frequency analog and digital baseband. In addition, several discrete high-Q filters are usually implemented in the signal path to provide sharp attenuation of both adjacent channel or alternate band energy. Other components include discrete inductors and capacitors for the realization of the Voltage-Controlled Oscillators (VCO) used by the frequency synthesizer found in the transceiver.



(a) 1997 Cellular Phone



(b) Block Diagram illustrating the many components

Figure 3. Conventional Super-Heterodyne transceiver shown in a (a) cellular phone and (b) block diagram form.

Many of the discrete filters shown in figure 3 as well as the higher frequency circuitry are designed for a given (fixed) frequency. Likewise, the baseband is designed for a particular channel bandwidth and modulation scheme associated with a standard.

Commercially available transceivers are designed to meet the worst-case channel conditions dictated by a set of standards. Therefore, in order for the transceiver to provide multi-standard operation, it would require the duplication of many discrete components found in figure 3 making a portable transceiver prohibitively large.

The long-term vision/goal for mobile wireless transceivers is to merge all of the components shown in figure 3 into a single piece of silicon in an inexpensive technology such as CMOS. By doing so, the advantages are clearly evident in terms of size and cost. The implication with respect to the hardware is that an integrated radio can provide more functionality, possibly allowing a single transceiver to operate off of multiple RF standards while optimizing a radio's performance as well as the power consumption [1.3].

The translation of all the components shown in figure 3 to a single piece of silicon is not a trivial task. The question at hand is how to achieve the same level of transceiver performance, for a given power consumption, in terms of selectivity and sensitivity on the receiver side and power output and spurious emission on the transmitter section.

Assume for the moment, that it is conceivable to integrate an entire radio on a chip. The question then arises as how to enable programmability between various RF standards. The transceiver design for each standard in general have different carrier frequencies, channel bandwidths as well as modulation schemes, just to name a few. Table 1 list some of the characteristics and requirements of just a few cellular, PCS, and cordless telephone standards. Hardware on a single chip radio could potentially be replicated to address the various standards, possibly going to the extreme of integrating complete multiple receive and transmit paths. However, the most efficient solution for a

multi-modal / multi-standard radio would be the maximum reuse of hardware between the various standards.

Parameter	AMPS	IS54	GSM	DECT	CT2	PHP	802.11FH
Origin	EIA / TIA	EIA / TIA	ETSI	ETSI	UK	Japan	IEEE
Access	FDD	FDM / FDD /TDM	FDMA / TDMA	TDMA / FDMA	FDM / TDD	TDM/TDD	FHSS / FDMA
Modulation	FM	pi/4QPSK	GMSK, diff	GFSK	GFSK	pi/4-DQPSK	(G)FSK
Baseband filter		Root raised cosine	Root raised cos. beta=0.3	Gaussian BT=0.5	Gaussian BT=0.5	Root Nyquist alpha=0.5	500khz LP
Data rate per RF channel	NA	48kb/sec (2bits/sym-bol)	270.8kb/sec	1.152Mb/sec	72kb/sec	384kb/sec	1Mb/s - 2Mb/s
FM Deviation	3khz	NA	NA	288kHz	14.4-25.2kHz	NA	~150kHz
RF Channel frequencies	824.04-848.97(X) 869.04-893.97(R)	824.04-848.97(X) 869.04-893.97(R)	890-915(X) 935-960(R)	0:1897.344Mhz, 9:1881.792Mhz	1:864.15Mhz 40:868.05Mhz	1895-1911Mhz	2.4-2.5G
No of RF Channels	833	833	124	10	40	52	75
Channel Spacing	30kHz	30kHz	200khz	1.728Mhz	10kHz	300kHz	1Mhz
Synthesizer switching speed	slow	slow		30us(BS) 450us(HS)	1ms(ch-ch) 2ms	30us(BS) 1.5ms(HS)	several us
Frequency Accuracy	2.5ppm	200hz		50kHz	10kHz	3ppm	
Speech channels per RF Channel (full/half rt)	1	3	8/16	12/24	1/1	4/8	NA
Speech coding	Analog com-panded	VCELP 8kb/s	RELP-LTP 13kb/sec	32kb/s ADPCM	32kb/s ADPCM	32kb/s ADPCM	NA
Frame Length	NA	40ms		10ms(12Tx+12Rx)	2ms (1Tx+1Rx)	5ms (4Tx+4Rx)	
Peak Power:	3W(6max)	3W(6max)	3W(20max	250mW	10mW	100mW	1 watt
Power Control rqmt	7 steps	7 steps		no	no		no

Table 1: Sample specifications from a few Cellular, Cordless and PCS standards.

One approach to the implementation of a single-chip multi-standard radio is the implementation of a “software radio”. Here the idea is to digitize the entire signal band immediately from the antenna on the receive side, and likewise perform a digital-to-analog conversion immediately before the antenna on the transmit side (figure 4). The potential advantage of this approach is that all of the signal processing is performed in the digital domain allowing the possibility of a low-power DSP implementation which can be made programmable between the various standards. However, for obvious practical reasons, the software radio lies more in the domain of science fiction rather than realistic production-worthy hardware. Such a radio used on a

2 GHz cellular application would require an Analog-to-Digital Converter (ADC) with approximately 20 bits and a Nyquist rate of up to 5 GHz, certainly not achievable in CMOS or silicon Bipolar at the time this thesis was written. This implies that some analog signal processing must take place between the digital radio components and the antenna. However, the potential advantages with respect to programmability between standards is evident in a transceiver solution with a maximum amount of digital hardware. In summary then, with respect to realizing a multi-standard transceiver in silicon, the transceiver components in the analog domain should be designed such that a maximum amount of reuse between standards may take place and the signal should be digitized as close to the antenna on the receive side, and converted to an analog signal as close to the antenna on the transmit side.

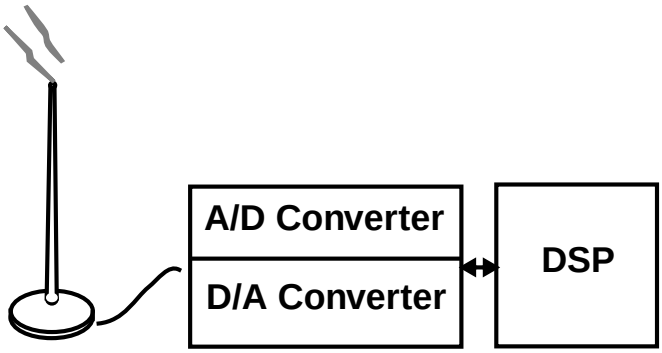


Figure 4. Ideal Software / All Digital Radio.

1.3 Research Objectives

The work which is highlighted in this thesis looks at some of the issues with respect to realizing the analog hardware components associated with a front-end radio receiver. Specifically, this thesis describes work which focuses on the issues of receiver integration from three aspects; receive architectures targeted at integration, implementation of image-rejection functions and the circuit design issues associated with the synthesis of CMOS active current commutating mixers. The work described in this thesis has resulted in the following contributions:

• Various receiver architectures were examined from the perspective of facilitating high levels of silicon integration. The exploration of the different architectures resulted in the introduction of a new receiver system, called Wide-Band IF, which attempts to facilitate integration of the entire signal path as well as full integration of the frequency synthesizer section including the tank circuitry associated with the Voltage-Controlled Oscillators (VCOs). This architecture also retains some generic properties which can potentially be re-used between various standards, allowing a single receiver to address multiple applications. To demonstrate both performance compatible with modern cellular and cordless telephone standards, as well as illustrating some multi-standard operation, two prototype receivers were built based on the Wide-band IF concept. One device seeks to demonstrate compatibility with the DECT standard while the other attempts to show compatibility with both the DECT and GSM standards.

• Another component of this thesis is devoted to the practical aspects of implementing the Wide-band IF architecture. Specifically, this work examines several techniques which perform image rejection without the need of an external discrete filter. A set of Weaver image-rejection mixers was used in both prototypes. In addition, the image-rejection mixers in the second prototype, were built to auto-calibrate out the phase and gain mismatch within the mixer. This ultimately improves the image-rejection performance.

• An analysis is given of active current commutating mixers. This is done with a set of intuitive guidelines for designing active mixers in either CMOS or BiPolar. A few example designs of active mixers, some of which were the first designed in CMOS, are presented.

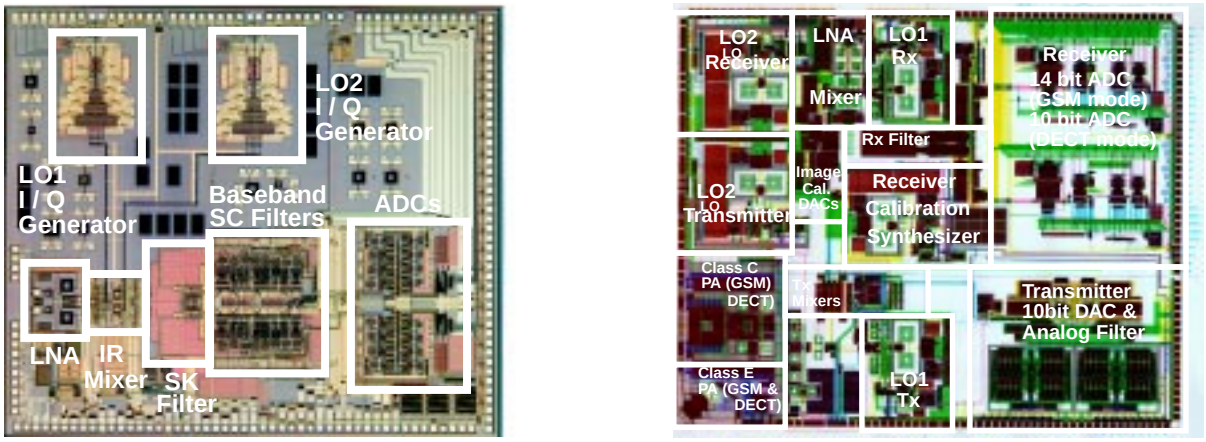
• High side-band suppression is achieved using an image-rejection mixer with accurate LO quadrature phases. This thesis presents a discussion of various circuits which generate accurate quadrature phase and the issues surrounding their design. A new VCO buffer quadrature generation circuit is presented which realizes accurate phase without the need of power hungry buffers while minimizing the loading on an LC-based VCO without degrading the tank Q.

1.4 Overview and Organization of Thesis

Many of the issues discussed with respect to integration and implementation of multi-modal radios will be addressed in the thesis. Specifically, this thesis focuses on receiver architectures which are both amenable to integration and multi-standard operation. As an example implementation of an integrated radio system, an architecture named Wideband IF with Double Conversion (WBIF) will be described and two prototypes based on the Wide-Band IF system will be given. From a circuit design perspective, this thesis explores the implementation of frequency translation systems (mixers) in commercially available CMOS. In particular, issues surrounding the

implementation of dual conversion image-rejection mixers will be described. A self-calibrating image-rejection mixer with the capability to adaptively tune out the phase and gain mismatch found within the mixer will be described. This will then lead to a discussion of the design issues surrounding the realization of the mixers used by this receiver architecture.

To demonstrate the concepts introduced in this thesis, two integrated receiver prototypes were realized in a standard CMOS process. Die photos of these chips are shown in figure 5. For the sake of clarity, these two projects will be given separate names which will be used throughout the text in this thesis. The first integrated receiver to be built during the period of this work was designed to illustrate some of the concepts with respect to integration in CMOS. This first prototype was designed to meet the specifications of a moderate performance European cordless telephone system known as the Digitally Enhanced Cordless Telecommunications (DECT) standard. For the purposes of this thesis, the DECT prototype and or project will be referred to as either the first generation receiver or simply the DECT project/receiver. The second prototype receiver implemented during the period of this work was implemented to demonstrate even higher levels of radio integration as well as increased levels of selectivity and sensitivity performance. The second generation device also attempts to illustrate the ability to operate on both wide and narrow band standards, to illustrate concepts with respect to a multi-standard radio system. The example device was designed to meet both the specifications of DECT and the upbanded version of the european cellular standard Global Systems for Mobile Communications (DCS 1800). From this point on in this thesis, the dual-mode DECT / DCS1800 chip will be referred to as either the 2nd generation receiver or simply the DECT/DCS1800 prototype. Both the first and second generation devices are shown in figure 5.



(a) (b)

Figure 5. Die photos of both the 1st and 2nd generation receivers discussed throughout this thesis. (a) DECT prototype receiver (b) DECT/DCS1800 prototype transceiver.

This thesis has the following organization:

Chapter 2 - An overview of the fundamental issues surrounding receiver design are discussed. Specifically, the influence of noise and distortion on a receiver's sensitivity and selectivity are given. This will be used to help characterize some of the more recent integrated receiver architectures which have been proposed including Wideband IF in chapter 3.

Chapter 3 - Examination and overview of several recently proposed architectures which attempt to facilitate radio receiver integration. The relative strengths and weakness of such architectures are evaluated based on the promise with respect to integration and the potential for multi-standard operation.

Chapter 4 - A key component used in any receiver system is the frequency translation section. Chapter 4 gives an overview of different single-sideband (image-

reject mixers) mixers which have been proposed. A description of the image-rejection mixer system used in the implementation of the wideband IF architecture is described.

Chapter 5 - A detailed description of the self-calibrating image-rejection system used by the second generation DECT/DCS1800 prototype is given.

Chapter 6 - With a knowledge of the mixer architecture used by the Wideband IF system, a more detailed analysis is given of active mixer design. These design guide lines were used in the realization of two prototype chips.

Chapter 7 - Much of the mixer supporting circuitry is discussed in this chapter. In particular, generating accurate quadrature phases with minimal power consumption is essential to realizing high-sideband suppression image-rejection mixers. A new method of generating quadrature phases will be discussed in this chapter. In addition, some of the standard cell bias circuitry will be examined.

Chapter 8 - The measured results as well as conclusions drawn from the data and research obtain in this thesis are given. In addition, some thoughts about the potential direction of research in the area of integrated transceiver systems is given.

1.5 References

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Chapter 2

Receiver Fundamentals

2.1 Introduction

The impetus to develop very inexpensive small radio receivers was reviewed in chapter 1. The realization of a single-chip radio implemented in a CMOS technology is a clear candidate to address all of the desired features associated with future wireless systems. The question now arises as to the technical challenges associated with integrating a radio on to a single chip. This chapter reviews some of the classic issues associated with a radio receiver design with an emphasis on figures of merit which are particularly challenging when attempting to integrate all the receiver functionality onto a single chip. Specifically, this chapter examines two of a receiver's key figures of merit, sensitivity and selectivity. Many of what might be classified as a receiver's sub-figures of merit influence the overall selectivity and sensitivity performance of the receiver. In particular, the gain distribution, noise performance of the individual receiver components, linearity, image rejection as well as reciprocal mixing all affect both the sensitivity and selectivity of the receiver.

This chapter first covers some of the basic concepts with respect to sensitivity. This is followed with an example computation of the sensitivity and noise figure of an

integrated receiver. The discussion will then turn to the fundamentals of selectivity performance. The sub-figures of merit related to the selectivity performance are reviewed with a discussion on both the computation and implication on integrated receivers.

Throughout this chapter, some examples of required performance are given for both the Digital Enhance Cordless Telecommunications (DECT) standard and several flavors of the Global System for Mobile communications GSM) standards which include GSM-900, DCS-1800, and PCS-1900. Some of the specifications regarding the physically layer are reviewed as well as a discussion of the implication on the radio receiver performance from both the perspective of sensitivity and selectivity. This chapter then concludes with a discussion of the overall implication on the of various receiver figures of merit when trying to integrate an entire radio on one chip. This discussion serves as good background for material presented in chapter 3 which looks at several suggested receiver architectures targeting high levels of integration.

2.2 Sensitivity, Noise Figure and Gain

In radio design, probably two of the broadest and most comprehensive figures of merit are the sensitivity and selectivity performance of a receiver. The *sensitivity* performance of receiver is defined as the minimum allowable desired band signal power at the receiver input, such that there is a sufficient signal-to-noise ratio at the receiver output to adequately extract the desired received information. The sensitivity test is usually performed with only the desired signal applied to the receiver; there are no interfering signals found at other frequencies.

The implication of the sensitivity on the overall receiver relates to the maximum range the receiver may wandered from the transmitter (figure 6). The lower the receiver’s sensitivity, the weaker the signal that may be receiver and recover useful information. This implies that a receiver with a low sensitivity may range a greater

distance from the basestation (in the case of many cellular applications) or from another mobile transmitter. The overall receiver sensitivity is directly related to the noise figure of the receiver which is impacted by both the noise performance of the individual receiver blocks as well as the distribution of gain down the receiver channel. As will be seen later in the special case of integrated receivers, the sensitivity and selectivity of the receiver trade-off with each other, and the power consumption.

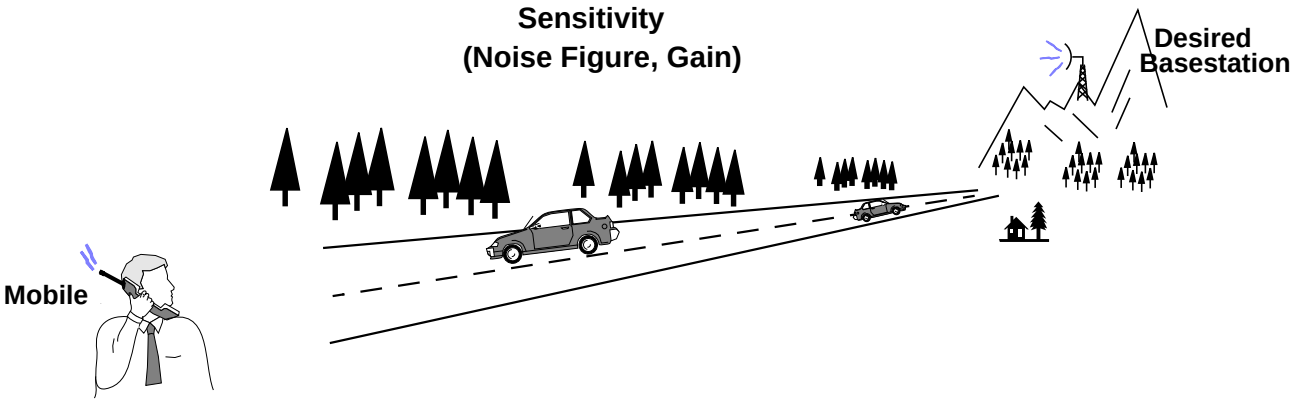

Figure 6. Sensitivity of the receiver determines the maximum range a mobile may wander from the basestation. The sensitivity is usually characterized without any interfering signals.

The true definition of sensitivity is the minimum detectable signal (typically specified in units of dBm) at the receiver input, such that there is a sufficient signal to noise ratio at the output of the receiver for a given application. The input to the receiver can be modeled with a source resistance found in series with the input of the receiver, this as shown in figure 7. Depending on how the input signal power is interpreted, two different signal levels for the sensitivity may be obtained. The confusion now arises when the input of the receiver is matched to a certain impedance; in the simplified example shown below, this would be when the real impedance $R_{in} = R_s$. Is the sensitivity defined at V_s (the source generating signal) or is the sensitivity defined by the voltage across the input terminals of the receiver?

"Industry jargon" typically refers to an open-circuit voltage as "hard" and closed circuit voltage as the "soft"[2.1] definition of sensitivity. True radio-philes

prefer the “hard” definition of sensitivity which is with an open circuit input to the receiver. However, most radio measurement equipment including the input to a receiver

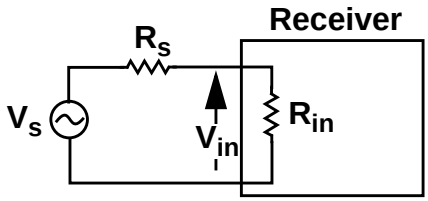

Figure 7. Input of the receiver with a source. Vin is the closed circuit voltage while Vs is the open-circuit voltage.

are matched to a 50Ω environment, leading to the more typically used definition of sensitivity as the soft voltage across the input terminal of a block with a matched input impedance. Therefore, the actual sensitivity is defined as the available signal power (definition of available signal power will be given later) delivered to the input terminal of the receiver. The simple definition of sensitivity is the minimum signal power delivered to R_{in} such that a sufficient SNR may be obtained at the output of the receiver to maintain the BER required of the particular radio system. For the purposes of obtaining the required sensitivity for the two prototype receivers described later, the “soft” definition of sensitivity will be used[1]. To further clarify the definition of sensitivity, assume we have a receiver where the input impedance is matched to a 50Ω source resistance and the receiver sensitivity is -113dBm, then the open-circuit voltage (Vs in figure 7) corresponding to this sensitivity is 1μV.

2.2.1 Receiver Noise Figure and Sensitivity: The Conventional Approach

A good way to understanding the process of calculating receiver noise figure begins with the original and definitive paper written by Friis in 1944 [2.2]. This paper outlines the procedure to analyze the noise figure of a cascaded two port network. Starting as Friis did with a simple example of a source loaded with a 4 terminal device

1. The definition of the physical layer in virtually all radio standards use the soft definition of sensitivity.

and an output circuit (see figure 8) we can quickly re-derive the noise figure equation. Using this model we now need to define a few terms as Friis did in his original paper.

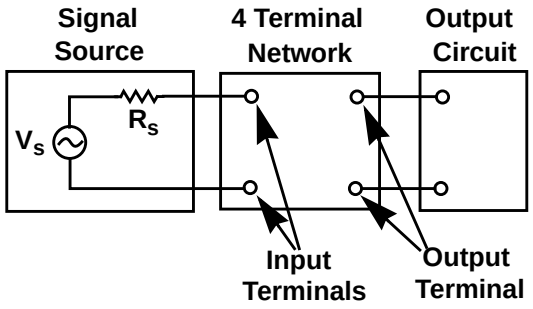

Figure 8. Simple 4-Terminal network which was used to propose the well known definition of noise figure by Friis in 1944.

For maximum power transfer from V_s to the input terminal of the network, a matched impedance is needed; the power delivered from the source to the input terminals is then $V_s^2/4R$. The power of the signal delivered to the input *under a matched condition* is often referred to as the ***available signal power*** which will be defined as S_g. For a receiver, the available signal power at the receiver input to adequately recover desired information was defined as the sensitivity. Likewise, the available signal power at the output terminals of the network, will be defined as S. Therefore, the ***available power gain*** G of the four terminal device is S/Sg. The available thermal noise power from the source resistance delivered to the input terminals is defined as,

$$\frac{4kTR \cdot \Delta f}{4R} = kT \cdot \Delta f(\text{watts}) \qquad \text{(Eq 2.1)}$$

Note that in the original definition of noise figure, the *available noise power* at the output of the source is due to the thermal noise source to the left of input terminals and not the noise generated by the input devices of the terminal. A useful number to remember which will aid in rapidly determining the available noise power delivered from the source (or input noise floor) of any receiver under the condition of a matched input impedance is -173.8 dBm/Hz (referenced to 1mW) or -186.8 dBV/Hz (referenced

to 1V). Knowing the bandwidth of interest (typically the channel bandwidth), one can quickly calculate the available noise power at the receiver input in dBm using,

$$\text{Noise Floor (dBm)} \cong [-173.8 + 10\log(B)](\text{dBm}) \quad \text{(Eq 2.2)}$$

or if 50Ωs is assumed, the noise floor in dBV is,

$$\text{Noise Floor (dBV)} \cong [-186.8 + 10\log(B)](\text{dBV}) \quad \text{(Eq 2.3)}$$

where B is the signal bandwidth.

Next, define N to be the available noise power at the output of the 4 terminal device. The noise factor is simply defined as the *available* signal-to-noise ratio at the signal source terminals to the *available* signal-to-noise ratio at the output of the network. A summary of the definitions used by Friis are given below.

kTB : Available noise power from the source
N : Available noise power at the output terminals of the network
Sg : Available signal power at the output of the source
S : Available signal power at the output of the network
F : Noise Factor
NF : Noise Figure, noise factor in dB NF=10log(F).
G : (Available signal power at the output)/(Available signal power at the input)

The noise factor for the 4 terminal network can then be expressed as,

$$F = \frac{\left(\frac{S_g}{kTB}\right)}{\left(\frac{S}{N}\right)} = \left(\frac{S_g}{kTB}\right)\left(\frac{N}{S}\right) \quad \text{(Eq 2.4)}$$

which is straight from Friis paper. Using the fact that $G=S/S_g$, equation 2.4 can expressed as,

$$F = \left(\frac{1}{G}\right)\left(\frac{N}{kTB}\right) \quad \text{(Eq 2.5)}$$

From equation 2.5 and the fact that the available noise power at the output is simply, N=FGkTB which includes the noise from the signal source. The available noise at the output due to the network only is then,

$$(F-1)GkTB(\text{watts}) \qquad \text{(Eq 2.6)}$$

When evaluating the noise figure for a cascaded network, the same approach may be used to find the available signal and noise powers at the input and output as was done above. For example, if as Friis presents in his paper, network 1 is cascaded with network 2 as shown in figure 9. The available noise power at the output terminals of

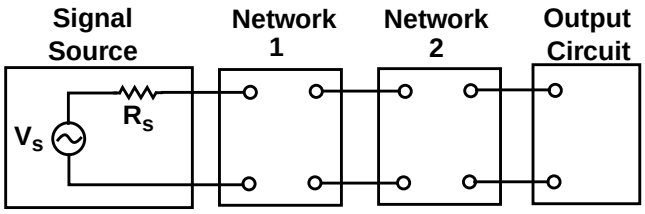

Figure 9. Cascaded network.

network 2 is,

$$N_{12} = F_{12}G_{12}kTB \qquad \text{(Eq 2.7)}$$

Substituting in the gain for network 1 and network 2 we can express equation 2.7 as,

$$N_{12} = F_{12}G_1G_2kTB \qquad \text{(Eq 2.8)}$$

The available noise power at the output of network 2, can be expressed as,

$$N_1 = F_1G_1kTB \qquad \text{(Eq 2.9)}$$

Simply multiplying by the gain in network 2 gives the available noise power at the output of network 2 due to noise sources in network 1 or

$$F_1G_1G_2kTB \qquad \text{(Eq 2.10)}$$

From equation 2.6 the available noise power due to noise sources in network 2 can be expressed as,

$$(F_2-1)G_2kTB \qquad \text{(Eq 2.11)}$$

The total available noise power at the output, may now be written as the sum of the noise sources due to networks 1 and 2 reflected to the output[2],

$$N_{12} = F_1 G_1 G_2 kTB + (F_2 - 1) G_2 kTB \quad \text{(Eq 2.12)}$$

Using equation 2.10, equation 2.11, and equation 2.12, the overall noise factor of networks 1 and 2 may be found,

$$F_{12} = F_1 + \frac{(F_2 - 1)}{G_1} \quad \text{(Eq 2.13)}$$

Equation 2.13 can be generalized even further as the following expression for an arbitrary length of N cascaded networks,

$$F_N = F_1 + \frac{(F_2 - 1)}{G_1} + \ \ldots + \frac{F_n - 1}{\prod_{i=1}^{n} G_i} \quad \text{(Eq 2.14)}$$

Often times discrete front-end filters along the signal path have net loss (G<1) in the power gain, commonly called the insertion loss. In this case, the available signal power outputted by the source in figure 9 is reduced by the amount equal to the insertion loss. For example, a network where the terminals are shorted together would correspond to a 0 dB insertion loss. The noise figure is then equal to the insertion loss.

Equation 2.14 is a classic equation derived by Friis to compute the noise factor of N cascaded stages and has been used in the design of discrete component radios for more than 50 years. Friis equation is convenient for computing cascaded noise figures when the individual components along the signal path are characterized with respect to a noise factor. It further assumes that the impedance is matched at the input and output of the an individual block resulting in the available noise and signal power at the input and output of each block.

From equation 2.14, it becomes clear, that a low noise figure receiver is accomplished by a good design in the very front-end components. If the noise figure were the only issue one was trying to address in the design of a receiver, then placing as much gain as close to the beginning of the receive chain as possible is desired. By

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2. In Friis original paper on cascaded noise figure computation[2.2], there is a slight error in his equivalent expression of equation 2.12 shown above.

making the value of G_1 as large as possible will have the affect of minimizing the noise contribution of all the blocks in the receive chain which follow the block with gain G_1. As will be shown later in the discussion on selectivity, placing too much gain on the very front-end of a receiver, degrades the linearity performance of the latter stage blocks if there is no filtering in the signal path. An additional aspect to a very low noise figure receiver is achieved through minimizing the noise factor of the very first block (F_1). Thus, both maximizing the gain of the first block while minimizing the noise contribution is typically the function of one of the very front-end components. This component usual is characterized by a low noise figure with high gain. Thus, the reason for the often used name, low noise amplifier (LNA).

It is often times convenient in discrete radio designs to use Friis equation, as the industrial standard is to design many components with common values for the input and output impedances, such as 50Ωs. However, in the case of a receiver that is fully integrated, the input and output of each block along the receiver chain is made to drive a node impedance directly, i.e. the output of an LNA is connected directly to the mixer input port. In this situation, the concept of available signal power is somewhat meaningless and inconvenient, particularly when computing the comprehensive noise figure of the receive channel. Therefore, in this work, when deriving the noise figure of the entire receiver, a slight modification was made to Friis equations which simplifies the translation of the noise performance of the individual blocks, to the overall noise performance of the receiver chain. The approach to computing the comprehensive noise figure of an integrated receiver is now reviewed in the next section.

2.2.2 Integrated Receiver Noise Figure Calculation

The noise figure calculation for the entire receiver, used in this work, is separated into two parts. First, the noise analysis is carrier out on the integrated portion of the receiver in terms of equivalent noise voltages (or resistances as will be shown

later), and the component voltage gain. Then all of the noise components in the integrated portion of the receiver chain (all the blocks on chip), are referred to the chip receiver input. This would be the interface between the last discrete component, at the receiver front-end, and the first integrated block. In the case of both receivers discussed later in this thesis, the interface is between the discrete balun found on the test board and the low noise amplifier input (LNA); this is illustrated in figure 10. The integrated receiver noise sources referred to the input, are then compared to the *available noise power* generated by the source impedance found on the board. Comparing the noise sources at the receiver input, to the available noise power of the source resistance can then be used to determine the noise figure of just the integrated portion of the receiver. Next, the noise factor (and figure) working back to the antenna, are determined by simply applying Friis equation recursively. The procedure for the noise figure computation used for the receivers described in this work, is summarized below:

1) On the front-end of the receiver, the insertion loss of individual discrete components are used to find the available signal power at the input of the chip. Because the input impedance of the LNA is matched to 50Ω, the available noise power at the LNA input can be computed in both dBm and dBV. This available noise power at the LNA input, is converted to a noise voltage across the input impedance of the LNA.

2) For the integrated receiver blocks (everything after the LNA), all the noise computation is made with respect to an equivalent input noise resistance. Although, the resistances is completely factitious, it is a convenient measure of the noise associated with the individual components along the receiver chain. The noise resistance is easily reflected back to the receiver input where it may be compared to the noise contribution from the source resistance. With this comparison, a good intuitive feel may be given as to the percentage noise contribution of any block along the receiver chain, to the overall receiver noise figure/factor. The equivalent noise resistance will be defined as R_{eq}, corresponding to an rms noise voltage power spectral density where,

$$\overline{V_{eq}^{2}}/(Hz) = 4kTR_{eq} \qquad \text{(Eq 2.15)}$$

R_{eq} is found by translating the equivalent input noise voltage at the input of a an individual receiver component along the receiver chain (figure 10), to a noise resistance with,

$$R_{eq} = \frac{\overline{V_{eq}^{2}}/(Hz)}{4kT} \qquad \text{(Eq 2.16)}$$

All the blocks in the receiver signal path were designed to meet a equivalent input noise resistance target. The design of each block was then done so by referring all of the noise generated within the circuit, to an equivalent input noise resistance. The equivalent input noise resistance associate with each circuit block in the receive chain, was then used to compute the entire receiver noise figure. Some examples of referring all of the noise sources in a mixer, to an equivalent input noise resistance are given in chapter 5.

In summary then, the noise figure of the receiver is calculated in two steps, using the input of the chip as a boundary where the noise level, signal level, and the SNR are converted from available signal powers to rms noise voltages from which R_{eq} is easily found as well as the signal voltages as shown in the example receiver, figure 10. The overall noise contribution of the *integrated section of the receiver* is calculated by reflecting the equivalent noise sources along the receiver chain back to the LNA input. This is then compared to the available noise power delivered to the LNA by the source resistance (50Ω) on the board. The available noise power due to a 50Ω output impedance from the last board component is *kT50*. The available noise power delivered by the source resistance to the LNA input, under a matched condition is then *(kT50)/4*. Remember that the voltage attenuation between the source and the matched impedance point is divided by two in voltage, and four in power. Assuming the source resistance is 50Ω, the available noise power from the source can be simply defined as an equivalent noise resistance where,

$$R_{board} = \frac{50\Omega}{4} = 12.5\Omega \qquad \text{(Eq 2.17)}$$

Because R_{board} represents the available noise power deliver to the receiver input from the source resistance, the equivalent input noise resistance from the integrated portion of the receiver reflected to the LNA input, may be compared directly with R_{board}. Using the Wide-Band IF receiver architecture as an example of computing the equivalent input noise resistance of the entire receiver chain (see figure 10), reflected to the board chip interface, the total equivalent noise resistance from the integrated portion of the receiver can be defined as $R_{Integrated}$ and described by,

(Eq 2.18)

$$R_{Integrated} = R_{LNA} + \frac{R_{Mixer1}}{Av_{LNA}^{2}} + \frac{R_{Mixer2}}{(Av_{LNA} \cdot Av_{Mixer1})^{2}} + \frac{R_{BB}}{(Av_{LNA} \cdot Av_{Mixer1} \cdot Av_{Mixer2})^{2}}$$

The noise factor of the integrated section of the receiver is then,

(Eq 2.19)

$$F_{Integrated} = \frac{R_{board} + R_{LNA} + \frac{R_{Mixer1}}{Av_{LNA}^{2}} + \frac{R_{Mixer2}}{(Av_{LNA} \cdot Av_{Mixer1})^{2}} + \frac{R_{BB}}{(Av_{LNA} \cdot Av_{Mixer1} \cdot Av_{Mixer2})^{2}}}{R_{board}}$$

Where A_v is the voltage gain of the respective receiver components, i.e. A_{VLNA} is the voltage gain from the input to the output of the LNA. With the noise factor for the integrated section of the receiver, the noise figure/factor of the receiver, back to the antenna may be calculated using Friis equation. Again, referring to the example shown in figure 10, and using the results from equation 2.19, the overall receiver noise factor including the discrete components is,

$$F_{Receiver} = F_{RFfilter} + \frac{F_{TR}}{G_{RF}} + \frac{F_{Balun}}{G_{RF}G_{TR}} + \frac{F_{Integrated}}{G_{RF}G_{TR}G_{Balun}} \qquad \text{(Eq 2.20)}$$

Where G is the power gain, or in this case the insertion loss, of the front-end components.

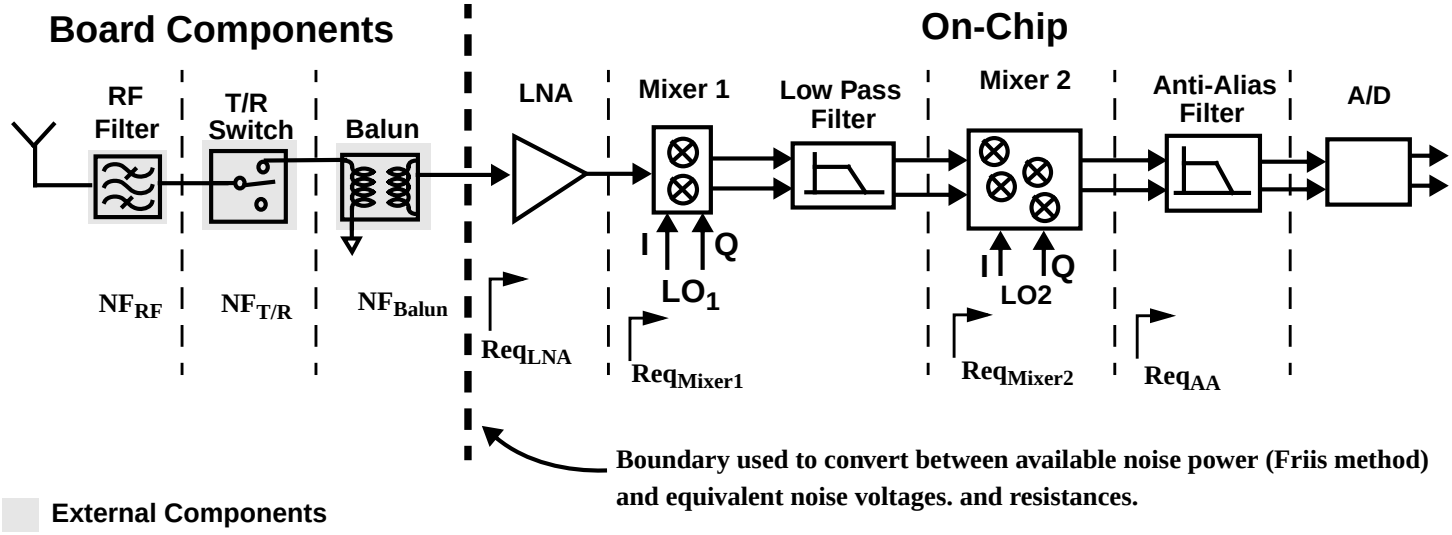

Figure 10. Model showing the boundary for the two step noise calculation used to model the Wide-Band IF receiver

There exists a direct relationship between the receiver sensitivity and the receiver noise figure. Remembering the receiver sensitivity is defined as the minimum required available signal-to-noise ratio at the input of the receiver to get a sufficient SNR at the receiver output, an estimate of the receiver's sensitivity based on the overall noise figure and the noise floor at the front-end can be made. By definition, the receiver sensitivity is the minimum required available signal-to-noise ratio at the input of the receiver to get a sufficient SNR at the receiver output. An estimate of the receiver's sensitivity based on the overall noise figure and the noise floor at the front-end can now be made,

$$\text{Sensitivity(dBm)} = \text{NF}_{\text{Receiver}}\text{(dB)} + \text{CNR}_{\text{output}}\text{(dB)} + \text{NFloor(dBm)} \qquad \text{(Eq 2.21)}$$

Where CNR_{output} is the required carrier-to-noise ratio at the receiver output to meet the minimum BER requirements of a standard or application. *NFloor* is the noise floor defined by equation 2.2. The higher the noise figure, obviously the weaker the receiver sensitivity. Therefore, the need to minimize the overall noise factor becomes apparent for any receiver, integrated or discrete. In the domain of integrated receivers,

the problem of lowering the noise figure of the receiver is difficult, as care needs to be taken when applying gain to the very front-end of the receiver. As will be seen in chapter 3, integrated receivers suffer from a lack of high-Q filtering in the signal path, particularly at high frequency. This tends to be problematic as interfering signals in other bands are now present, which can be received with a much greater magnitude than the desired signal. The interfering signals then set a limit to the amount of front-end gain which may be applied to a receiver. Thus, making a practical highly-integrated receiver with a low noise figure and sensitivity an interesting challenge.

In the next section, the other receiver key figure of merit, selectivity, is explored.

2.3 Selectivity

A receiver's *selectivity* performance is a measure of the ability to separate the desired band about the carrier, from unwanted interfering signals received at other frequencies. This situation is most often characterized by a weak received desired signal in the presence of a strong adjacent or alternate band user. In practice, good selectivity performance of the receiver may be required when a mobile device is physically far from its corresponding basestation (see figure 11) while simultaneously, there are other users, either within the same system or running off of a different standard which are physically close to the mobile receiver which is trying to receive a very weak desired signal. The transmitter associated with the desired signal is far from the receiver while the interfering users are close; this gives rise to the often used term "near-far problem". The interferer could be close both physically and in frequency.

Unlike sensitivity, which has a clear quantitative description and a direct link to both receiver gain and noise figure, selectivity is influenced by many impairments in the receive signal path. The linearity associated with many of the receiver components along the signal path influence the selectivity. Reciprocal mixing of the oscillator phase

noise with an interfering signal, will likewise heavily influence the receiver selectivity performance. Depending on the receiver architecture, a high degree of image-rejection may be required to obtain a good immunity to undesired received signals which lie within the image band.

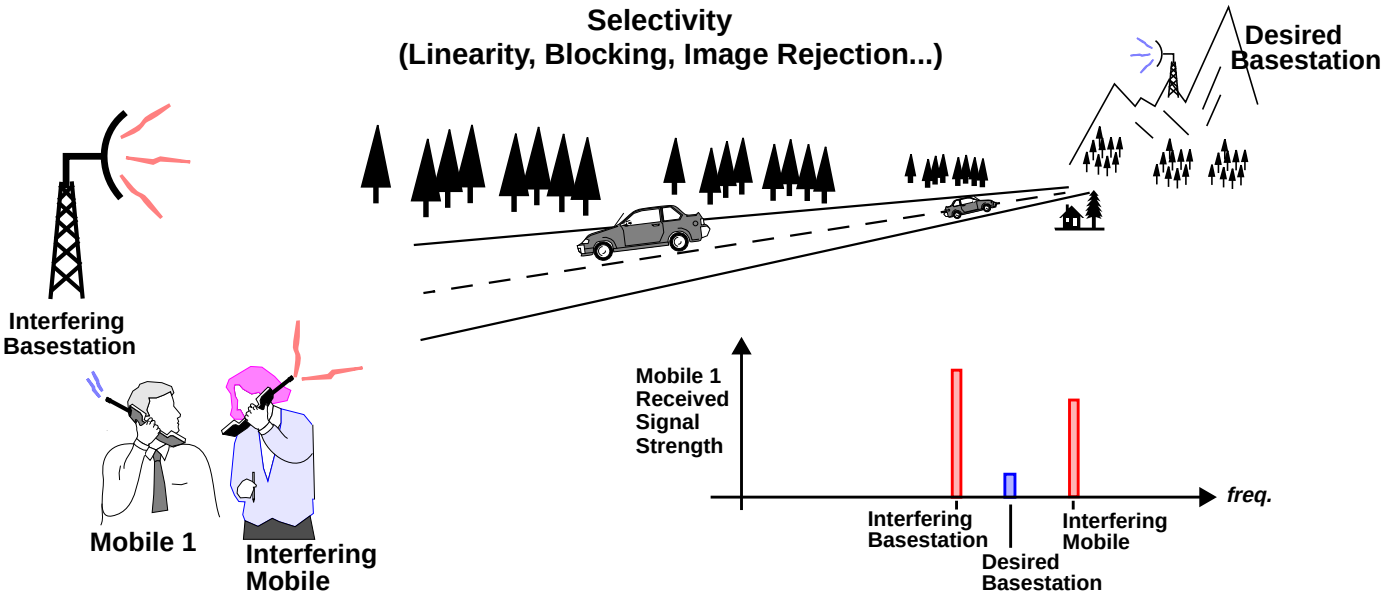

Figure 11. Selectivity determines the range in the presence of other strong interfering user. This is the “Near-Far” problem.

The following section will give some common definitions and requirements of receiver selectivity performance. As an example, some of the selectivity performance requirements of the DECT and GSM standards are reviewed. Using both DECT and GSM as specific examples, a discussion is then given on some of the “sub-figures” of merit which influence the selectivity performance. These include, second and third order intermodulation performance, and oscillator phase noise.

2.3.1 Blocking and The Selectivity Definition

Most radio standards which exist today, specify the selectivity requirements of a radio receiver in the physical layer definition. One of the key selectivity requirements outlined in a standard is the blocking performance. Similar to the near-far problem described above, the blocking performance is typically defined with a desired signal

applied to the receiver which is 3dB above the required reference sensitivity. Simultaneously, an additional signal is applied to the receiver (called a blocker) at a defined offset frequency from the carrier with a certain magnitude. The receiver must then have the ability to maintain a minimum bit error rate (BER) in the presence of the blocking signal.

The impact of a strong AM blocker on the BER cannot be understated, particularly in the case of an integrated receiver, as will be discussed later. A large AM blocker will cause degradation on the carrier-to-interference ratio of a desired signal through three predominant mechanisms. First, the blocker will cause gain compression, which has the unfortunate affect of reducing the gain on the desired signal. Second, the blocker can potentially mix with the oscillator sidebands, dropping an interfering component directly in the desired signal band. The third mechanism of interference to the desired signal happens when the blocker goes through a second order non-linearity in the receive chain. This problem is particularly sever in direct conversion receivers.

An additional specific condition which is usually outline in a radio standard are definitions on the third order non-linearity performance of a receiver. This test is done separate from the blocking test and is often referred to as a third order intermodulation test. Here, the receiver is being exercised to test the immunity to a pair of undesired signals which line up in frequency such that when both the interfering signals passing through a third order non-linearity, an interfering component is created in the desired signal band. Some examples of third-order-intermodulation specifications for GSM and DECT are reviewed in later sections of this chapter with a method to estimate the comprehensive intermodulation performance of an entire receive channel based on the linearity performance of the individual components.

2.3.1.1 GSM Blocking Definition

In the GSM standard, the blocking test is performed by applying a GMSK modulated desired signal 3dB above the required receiver reference sensitivity. Then a single unmodulated tone (simple sinewave) is applied to the receiver at discrete increments of 200 kHz from the desired signal with a magnitude as shown in the specific blocking requirements of GSM, E-GSM, DCS1800, and PCS1900 [2.3]. Note, the following blocking requirements are given for the mobile station(MS) only, a separate set of specifications exist for the base station.

The blocking requirements are similar among the different GSM standards with some exceptions which are outlined below. For fully integrated radios, one of the more difficult specifications to meet in the GSM standard is the 3 MHz blocker which is typically 76 dB above the desired carrier. Although many standards have ridged requirements on the radio blocking profile, they allow a relaxation in the blocking profile at some offset frequencies from the carrier, to allow for inherent spurious signals within the receive signal path. These might be spurious tones which are simply a feature of a particular frequency synthesizer architecture. In GSM, the relaxed blocking specifications are called “spurious response frequencies”. The frequency of the relaxed blocking requirements are selected by the user and each channel is allowed a different set of spurious response frequencies. For example, if one were to set a spurious response frequencies for channel 800 in DCS 1800, then move to channel 805, the user can again assign a new set of spurious response frequencies. Depending on the flavor of GSM (GSM 900, DCS 1800, or PCS 1900) there are anywhere from 6 to 12 inband expectations and up to 24 out-of-band exceptions per channel. When the spurious response exception is used, the magnitude of the AM blocker may be relaxed to -49 dBm[2.4].

The GSM blocking test is performed by applying a GMSK modulated signal 3 dB above the required reference sensitivity. This is usually from -99 to -97 dBm, again

depending on the flavor of GSM[2.4]. A single blocker is then applied to the receiver at a given offset from the carrier frequency with a magnitude as shown in figure 12. Under this condition, the receiver must maintain a 10^{-3} BER. The test is repeated with a single blocker at each of the frequency offsets shown in figure 12. The desired signal is then changed to another channel, and again the process of applying a lone blocker, is repeated for each frequency offset shown in figure 12.

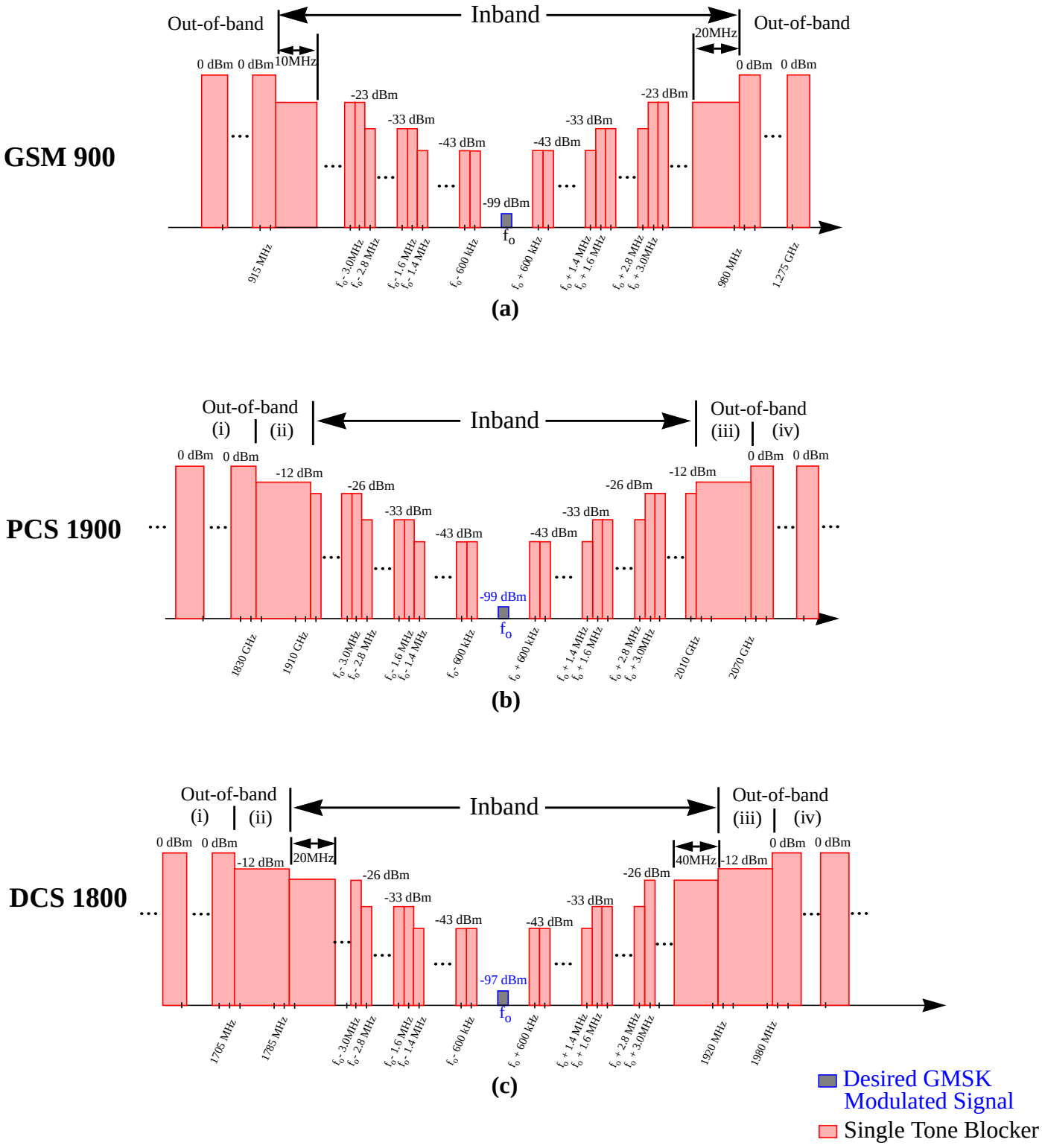

Figure 12. Required blocking performance for (a) GSM 900, (b) PCS 1900 and (c) DCS 1800.

2.3.1.2 DECT Blocking Definition

DECT has considerably easier blocking requirements as compared to GSM. This is expected as DECT is a relatively moderate performance standard. Similar to many Wireless Local Area Network (WLAN) standards, the mobile does not wander as far from the basestation when compared to a a cellular standard like GSM. Given that the possible range of the mobile from the basestation is smaller, so to will be the range of potential signal magnitudes that are received. Worse case, the desired signal will come in stronger (compared to cellular) and the difference in magnitude between the desired signal and an interferer will be smaller as compared to the case where the mobile may wander far from the basestation (cellular). Thus, the selectivity, and the sensitivity performance are more relaxed in cordless telephone and WLAN standards. A set of test conditions for the DECT standard [2.5] are given for both the inband and out-of-band blocking signals.

2.3.1.3 Inband blocking requirements:

The mobile must maintain a 10^{-3} BER when a -73 dBm desired signal is applied to the receiver input and while a a single blocker is simultaneously applied. The blocker is a GMSK modulated signal of power level and frequency offset as shown in figure 13. The blocking requirements include a -83dBm Co-Channel blocker (The Co-Channel blocker is an interfering signal applied in the same band as the desired signal).

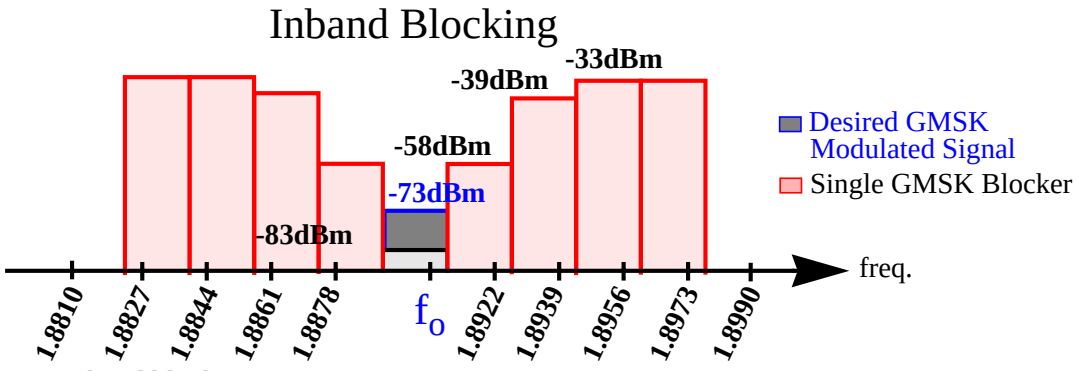

Figure 13. DECT Inband blocking requirements.

All of the inband blocking tests are repeated for each of the adjacent channels.

2.3.1.4 Out-of-band Blocking Requirements:

A desired -73dBm input signal is applied to the receiver in channel 4. Then a single unmodulated blocker (simple sinewave) is applied in each of the following bands with the signal strength indicated in figure 14. Since a 10^{-3} BER must be maintained, this maps to an approximate C/I ratio of 10 dB at the output of the receiver using GMSK modulation.

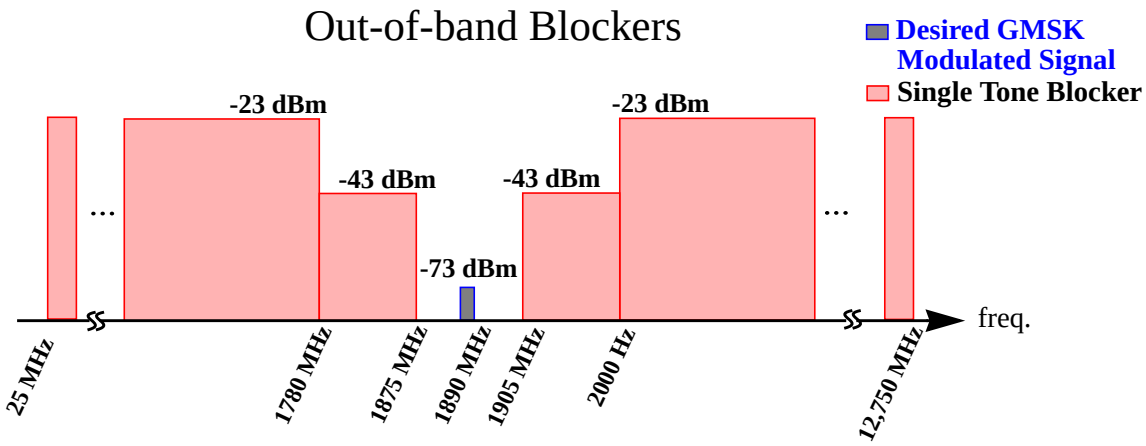

Figure 14. Out-of-Band DECT blocking requirements.

2.3.1.5 Blocking Performance, Reciprocal Mixing and LO Phase Noise

A Local Oscillator (LO) is used with a mixer in the receiver signal path to frequency translate the desired signal spectrum about the carrier to a lower frequency. Phase noise is a measure of the spectral purity of the local oscillators used in this operation. Figure 15 illustrates how undesired sideband energy from the local oscillator (phase noise) “reciprocal mixes” with adjacent channels or out-of-band signals. The reciprocal mixing can potentially result in frequency translating a blocker, to fall within the desired signal band at the output of the mixer. Interference in the desired signal band from the blocker reciprocal mixing degrades the receiver (C/I) ratio. The oscillator must then be designed such that under a worst case blocking condition, the reciprocal

mixing of the blocker with the phase noise of the oscillator will produce an interference component far below the desired signal level.

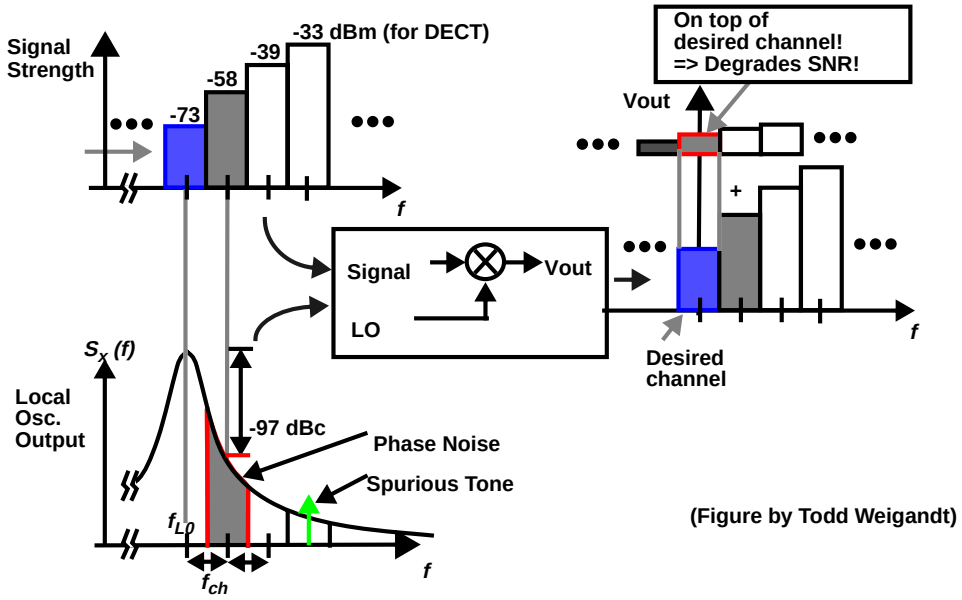

Figure 15. Reciprocal mixing of the blocker and phase noise. DECT blocking profile used as an example.

2.3.1.6 Estimation of Interference from Reciprocal Mixing

Based on the blocking profile given by a standard, along with the known phase noise performance of the oscillator used by the mixer, the amount of interference created in the desired signal band from reciprocal mixing may be estimated. One method to perform the phase noise calculation assumes that the receiver channel is noiseless and the only interference produced within the desired signal band is due to the phase noise reciprocal mixing with a blocker [2.6]. The method to calculate the phase noise performance required of the oscillator is illustrated in figure 16. Here, the phase noise is assumed to be flat across the band of interest at a certain offset from the carrier. The interference component that is then produced when the blocker mixes with the phase noise sidebands, is compared to the desired signal which mixes with the carrier energy.

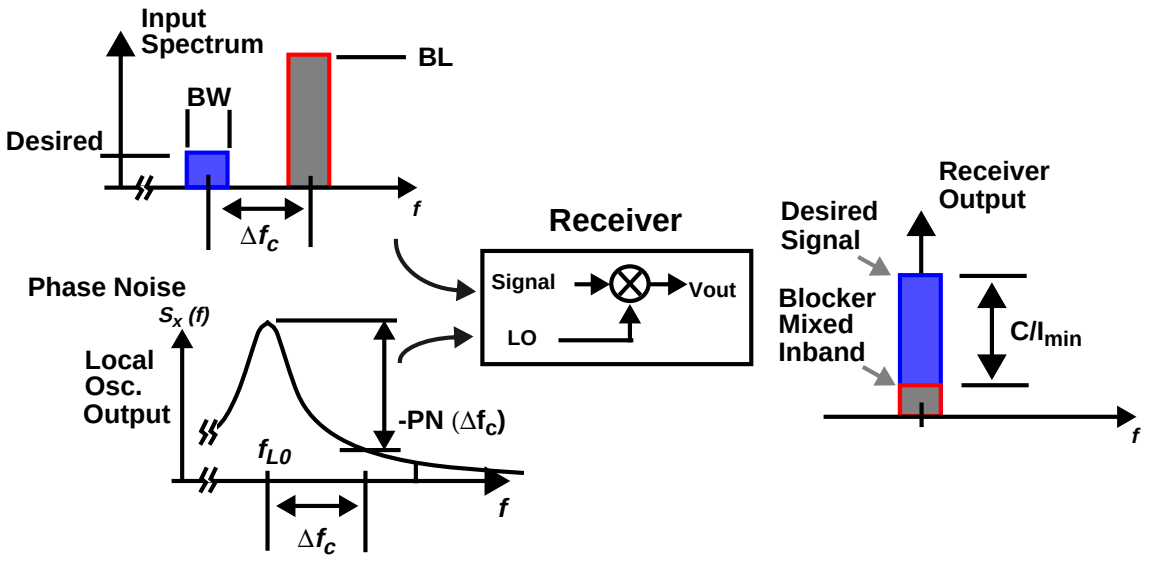

Figure 16. Simple calculation for required phase noise performance of the LO.

Based on the required C/I ratio at the output of the mixer, the blocker magnitude, along with the carrier offset and the desired signal level, the required phase noise performance in dBc/Hz may be estimated using,

$$PN(\Delta f_c)\left(\frac{dBc}{Hz}\right) = \qquad \text{(Eq 2.22)}$$

$$S_{desired}(\Delta f_c)(dBm/dBV) - S_{bl}(\Delta f_c)(dBm/dBV) - C/I_{min}(dB) - 10\log(BW))$$

Where $PN(\Delta f_c)$ is the phase noise in dBc/Hz, Δf_c away from the carrier. S_{bl} is the magnitude of the blocker in dBm or dBV while $S_{desired}$ is the magnitude of the desired carrier in dBm or dBV. C/I_{min} is the minimum required carrier-to-interference ratio and BW is bandwidth of the desired signal.

As stated before, equation 2.22 can be used to approximate the required phase noise performance of the local oscillators in the receiver, assuming there are no other sources of interference in the receiver channel. However, practically speaking this is far from the true situation and the receiver white thermal noise contribution will further degrade the overall carrier-to-interference ratio at the output. Therefore, a better picture of the true C/I ratio at the output of the receiver, should include the white noise added

to the desired signal band, as well as the effects of blockers reciprocal mixing with the phase noise and the effects of gain compression in the receiver signal path due to a large blocking signal.

The approach to determine the required receiver phase noise performance as a function of the needed blocking performance may be done as follows. All of the equivalent input noise resistances are referred to the output of the receiver including the available noise contribution at the input of the receiver (12.5Ω). Then at each mixer output, the power of the blocking signal reciprocal mixing with the LO phase noise which creates an interferer within the desired signal band, can be approximated by assuming the phase noise is flat across the band of interest. This gives the following expression,

$$10\log(\sigma^2_{\text{Mixerout}}) = [S_{bl}(\Delta f_c)(\text{dBV}) - [PN(\Delta f_c) + 10\log(BW)]](\text{dBV}) \qquad \text{(Eq 2.23)}$$

Where $\sigma^2_{Mixerout}$ is the power of interferer created inband by reciprocal mixing. This interference source can then be referred to the output of the receiver along with all other interferers in the receiver chain, including the noise contribution of the individual receiver components. This procedure is illustrated for the Wide-Band IF architecture shown in figure 17.

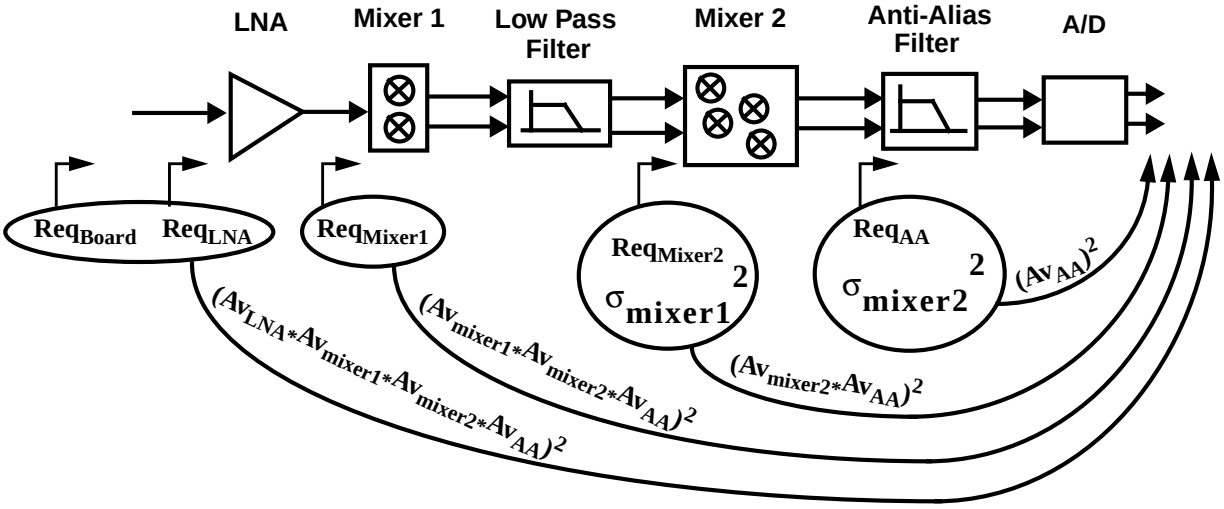

Figure 17. Sources of interference in the receiver signal path while an undesired blocker is present.

Treating the interference produced by the blocker reciprocal mixing with the phase noise of the LOs as an rms noise voltage source, one can reflect all of the interference sources, both thermal and phase noise to the output of the receiver. The total interference can be expressed in terms of the equivalent input noise resistance (R_{eq}) of each block, the individual component voltage gain and the blocking interference created by reciprocal mixing. Defining σ^2_{out} as the total inband voltage interference power (both thermal and reciprocal mixing) at the output of the receiver gives,

$$\sigma^2_{out} = (Av_{Mixer2} \cdot Av_{AA})^2 \cdot \sigma^2_{mixer1} + (Av_{AA})^2 \cdot \sigma^2_{mixer2} + \sigma^2_{thermal} \qquad \text{(Eq 2.24)}$$

Where $\sigma^2_{thermal}$ represents *all* of the thermal noise contribution referred to the output of the receiver, which can be found using equation 2.18 and scaling the equivalent output noise resistance by 4kT to get the rms noise voltage. The receiver output C/(I+N) can be expressed as,

$$C/I_{output} = \frac{Av^2 \cdot S_{Desired}}{(Av_{Mixer2} \cdot Av_{AA})^2 \cdot \sigma^2_{mixer1} + (Av_{AA})^2 \cdot \sigma^2_{mixer2} + \sigma^2_{thermal}} \qquad \text{(Eq 2.25)}$$

Where A_v is the overall receiver voltage gain and $S_{Desired}$ is the rms voltage power of the desired signal. Next, if a simplifying assumption is made that the power of the blocker reciprocal mixing with the phase noise of the individual mixers contribute equally (both mixers have the same phase noise profile) and the thermal noise contributions of each receiver component has been determined, the maximum interference allowed by the phase noise mixing with the blocker can be found. This is expressed as,

$$\sigma^2_{pn} = \frac{\left(\frac{Av^2 \cdot S_{Desired}}{C/I_{required}}\right) - \sigma^2_{thermal}}{((Av_{Mixer2} \cdot Av_{AA})^2 + (Av_{AA})^2)} \qquad \text{(Eq 2.26)}$$

The required phase noise performance of the local oscillator to meet the blocking profile for a particular standard can be determined using equation 2.26 in conjunction with equation 2.23.

2.3.1.7 Second Order Intermodulation (IM2)

One non-ideality which will affect the receiver's blocking performance is second order intermodulation (IM2) of the various components in the signal path. A second order non-linearity is particularly problematic for high selectivity applications where the carrier is downconverted to baseband without any channel filtering, as would be the case in a direct conversion receiver discussed in the next chapter. The mechanism for second order intermodulation is outlined below with an explanation of the method used to find the required equivalent input IP2 of the baseband blocks used by direct conversion systems, as a function of the required blocking performance.

The effect of IM2 is quickly understood by examining a simple expression which relates the input and output signal of a block, via a high order transfer function. First, assume looking into the baseband block that there is a non-linear transfer function relating the input and output signals by,

$$S_o(t) = a_1 S_i(t) + a_2 S_i^2(t) + a_3 S^3{}_i(t) \ldots \quad \text{(Eq 2.27)}$$

Where $S_o(t)$ is the output signal and $S_i(t)$, can represent an applied blocker (interfering signal). To understand the mechanism which creates interference in the desired signal band from second order intermodulation. One can apply a blocking signal $S_i(t)$ to the non-linear transfer function in equation 2.27. $S_i(t)$ can be represented by a sinewave where, $S_i(t) = S_i \cos(\omega_{bl} t)$ and ω_{bl} is the frequency of the blocker. Keeping in mind that in a direct conversion system, the desired band signal is center around DC at baseband. Therefore, the interference created at baseband, (DC), by a blocker passing through a second order non-linearity is of interest. If ω_{bl} represents the frequency offset relative to DC after frequency translation to baseband, then using some simple

trigonometric relationships reveals that when the input signal (or blocker) passes through a second order non-linearity, the following result is generated by the second order term in equation 2.27,

$$a_2 \cdot (S_i \cos(\omega_{bl} t))^2 = a_2 \cdot S_i^2 \left(\frac{1 + \cos(2\omega_{bl} \cdot t)}{2} \right) \quad \text{(Eq 2.28)}$$

From equation 2.28, the second order non-linearity is seen to create a DC component. This is a particular problematic when there is a weak desired signal which gets frequency translated to baseband in the presence of a strong adjacent channel blocker. The large blocker now creates an interfering component at DC, which is in the center of the desired signal spectrum at baseband. The relationship between the required equivalent input IP2, based on the targeted blocking profile of any standard or application, may be found with a little simple math. Using the relationship between the coefficients of the high order signal transfer function, and the definitions for both second order intermodulation (IM2) and second order harmonic distortion (HD2) given in [2.7]. HD2 and IM2 can be expressed as,

$$HD2 = \frac{a_2 S_i^2 / 2}{a_1 S_i} \quad \text{(Eq 2.29)}$$

$$IM2 \cong HD2 + 6dB \quad \text{(Eq 2.30)}$$

The required IP2 performance may be inferred from a knowledge of the gain which precedes the baseband and blocking test which must be performed to comply to a standard. Again, similar to the required noise figure and phase noise performance, the required IP2 performance for the GSM mode of operation is far more aggressive than what is called for by DECT. Accordingly, as an example calculation of the IP2 performance required by the baseband blocks of a direct conversion receiver, the 3MHz blocking condition in the GSM blocking profile will be used, see figure 12.

To find the required IP2, it will be first assumed that both the desired signal and the blocker are frequency translated to baseband without any filtering of the unwanted adjacent channel signal; a fair assumption for any receiver which attempts to eliminate the IF filter. In addition, both the carrier and the blocker will see an equal

gain by all components which precede the baseband. This gain will be denoted A_{vrf} which is the comprehensive gain between the antenna and the baseband blocks. In the GSM standard, under the 3MHz blocking condition, the relationship between the desired baseband signal, the 3MHz blocker, and the interference component generated by the second order intermodulation are as shown in figure 18.

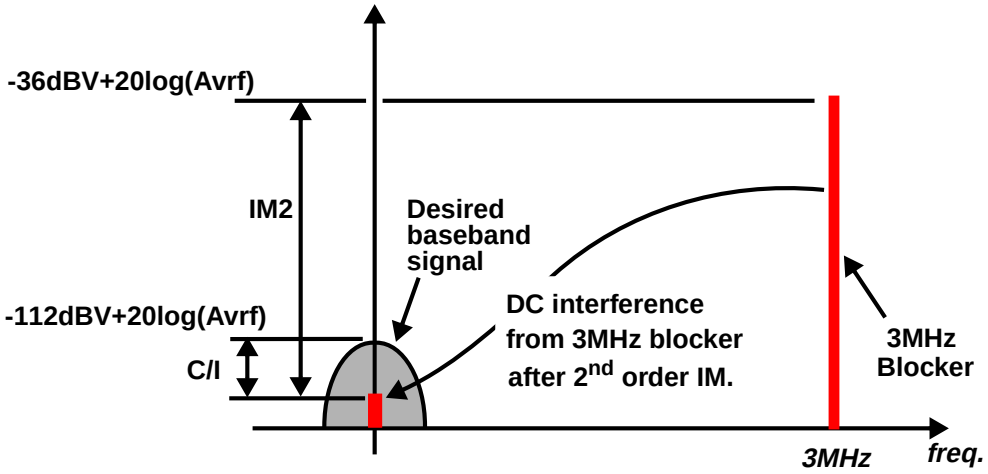

Figure 18. Signal spectrum after the mixer in a direct-conversion receiver. An interferer is created within the signal band, by the 3 MHz blocker passing through the baseband 2^{nd} order nonlinearities.

The DC interference which is generated by the second-order intermodulation of the blocker can be found from equation 2.28. In equation 2.29, the numerator of the expression for HD2 is equivalent to the magnitude of the DC component produced by blocker passing through the second-order term in equation 2.27. To ensure that the second order interference has negligible degradation to the overall receiver C/I ratio under the blocking condition (in this example the 3MHz blocker is used in the DCS1800 standard), the DC component generated by the second order intermodulation should be about 15dB below the desired baseband signal level. If S_{des} represents the power of the desired signal at the receiver input in dBV, and S_{bl} the magnitude of the blocker at the receiver input, also in dBV. To meet the condition of negligible degradation in the C/I ratio arising from the DC component created by 2^{nd} order IM we have,

$$a_2 S_i^2 / 2 \le S_{des}(\text{dBV}) + 20\log(A_{vrf})(\text{dB}) - 15\text{dB} \qquad \text{(Eq 2.31)}$$

The magnitude of the blocker at baseband is,

$$S_{bl}(dBV) + 20\log(A_{vrf})(dB) \quad \text{(Eq 2.32)}$$

A closer examination will reveal the required HD2 under the conditions outlined above is simply the difference between equation 2.31 and equation 2.32 in dB. Therefore, when the interference is required to be 15dB below the desired signal, HD2 can be expressed as,

$$HD2(dB) = S_{des}(dBV) + 20\log(A_{vrf})(dB) - 15dB - [S_{bl}(dBV) + 20\log(A_{vrf})(dB)] \quad \text{(Eq 2.33)}$$

or,

$$HD2(dB) = S_{des}(dBV) - 15(dB) - S_{bl} \quad \text{(Eq 2.34)}$$

The required IM2 performance of the baseband is,

$$IM2 = S_{des}(dBV) - 9(dB) - S_{bl}(dBV) \quad \text{(Eq 2.35)}$$

By simply examining a plot of IM2 verses the blocker input power one can quickly see that the IM2 decreases by 10 dB for every 10 dB increase in blocker power. Therefore, the required IP2 may be expressed as,

$$IP2(dBV) = S_{bl}(dBV) + [S_{bl}(dBV) + 9dB - S_{des}(dBV)] \quad \text{(Eq 2.36)}$$

Similar to the IP3 which will be discussed shortly, the IP2 number is a characterization of the second order non-linearity in the receiver components. As can be observed from equation 2.36, a high second order non-linearity performance is required of the baseband blocks when there exists a large the difference between the magnitude of the blocking signal, S_{bl}, and the desired signal, S_{des}. In addition, a high IP2 is required when just the magnitude of the blocking signal by itself is large. Thus, the IP2 performance of any block along the receiver chain is dependent on the gain which proceeds that block.

For direct conversion receivers, with essentially no front-end filtering, the required IP2 performance at baseband can be very aggressive. As an example IP2

calculation looking into the baseband, assume a direct-conversion receiver with no channel filtering between the antenna and baseband which is used in the DCS 1800 system. The required IP2 looking into the baseband will be dependent on the 3 MHz blocking condition. From figure 12, the desired signal S_{des} is -97 dBm while the blocker, S_{bl}, is - 26 dBm. It is convenient to convert the input signals from dBm to dBV. If it is assumed that there is 20 dB of voltage gain between the antenna and baseband, S_{des} at baseband is -90 dBV and S_{bl} is -19 dBV, then the required IP2 from equation 2.36 becomes,

$$IP2(dBV) = -19(dBV) + [-19(dBV) + 9dB - (-90)(dBV)] \quad \text{(Eq 2.37)}$$

This gives an IP2 of +60 dBV. This is a challenging number for any baseband block to meet. Thus, one of the reasons why integrated receivers using direct conversion are difficult to implement for high selectivity standards similar to DCS 1800.

2.3.2 Third Order Intermodulation (IM3) and Selectivity

An additional circuit impairment which may affect a receivers ability to reject signals found in other bands is the third order intermodulation (IM3) performance. The mechanism of interference to the desired signal band from third IM is slightly different than the source of interference during a blocking test described above. Interference from third order intermodulation arises from two out of band signals which pass through a third order non-linearity, and generated a new spectral component which falls directly in the band of the desired signal. Along the receive signal path the nonlinearity associated with the circuits have a high order transfer function as given in equation 2.27. Assume that there are two input signals which are applied to the receiver frontend and are represented as S_1 and S_2, at frequencies ω_1 and ω_2, respectively. The input signal, S_i, can then be described by,

$$S_i = S_1\cos(\omega_1 t) + S_2\cos(\omega_2 t) \quad \text{(Eq 2.38)}$$

After S_i passes through the third order non-linearity in equation 2.27, several new spectral components are generated. After doing a little trigonometry, the following results,

$$a_3 S_i^3 = \frac{a_3 S_1^3}{4}(\cos(3\omega_1 t) + 3\cos(\omega_1 t)) + \frac{a_3 S_2^3}{4}(\cos(3\omega_2 t) + 3\cos(\omega_2 t)) + \quad \text{(Eq 2.39)}$$

$$\frac{3}{4}a_3 S_1 S_2^2[2\cos(\omega_1 t) + \cos((2\omega_2 - \omega_1)t) + \cos((2\omega_2 + \omega_1)t)]$$

$$+ \frac{3}{4}a_3 S_1^2 S_2[2\cos(\omega_2 t) + \cos((2\omega_1 - \omega_2)t) + \cos((2\omega_2 + \omega_1)t)]$$

Of most interest in equation 2.39 are the terms which result in a spectral component at $2\omega_2$-ω_1, $2\omega_2$+ω_1, $2\omega_1$-ω_2, and $2\omega_2$+ω_1. These spectral components which arise from a third order non-linearity are of particular concern in radio receiver applications, as the situation may arise where there are two alternate band users which may be present very close in frequency to the receiver's desired channel. If the alternate band signals happen to lie at frequencies ω_2 and ω_1, while the desired signal band to receive resides at either $2\omega_2$-ω_1, $2\omega_2$+ω_1, $2\omega_1$-ω_2, and $2\omega_2$+ω_1, $2\omega_2$-ω_1. If this situation occurs, as it sometimes does, the spectral components generated from the alternate band signals passing through the receivers third order non-linearity will actually appear as interference in the desired signal band, this is illustrated in figure 19.

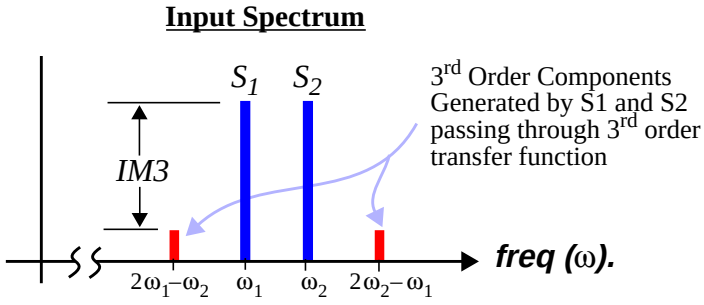

Figure 19. Third order intermodulation in the frequency domain.

A classic measure of 3rd order non-linearity in an individual component in the receiver or the entire receive path, is the third order intermodulation intercept point (IP3). This number is usual measured with a two-tone test, where the tones are applied

to a receiver input (S_1 and S_2) and the third order component generated is measured. The results are plotted on a log-log plot as shown in figure 20. The magnitude of S_1 and S_2 are increased and the 3^{rd} order component is again measured. From the log-log plot, both the linear and third order terms are extrapolated. Where the two lines intersect is the third order intermodulation intercept point.

The issue of third intermodulation is revisited in chapter 6, section 6.6 with an emphasis on the estimation of third order intermodulation performance in CMOS mixers. However, now the focus is more on the relationship between the required selectivity performance of a standard or application and the comprehensive intermodulation performance of the entire receiver. Specifically, it is desired to estimate the total intermodulation performance of the receiver based on the linearity performance of the individual blocks cascaded along the receive chain. The method of doing such an estimate for integrated receivers is reviewed. This is followed by some relationships between the physical layer specifications on intermodulation and the required third order intercept (IP3) performance of the receiver. Both the DECT and GSM standards are again used as examples.

2.3.2.1 Estimate of Receiver (IP3)

There are several methods for calculating the intermodulation performance of an individual block and of a cascaded chain of receiver components. Two methods for calculating the equivalent distortion performance of a number of cascaded receiver blocks as a function of the distortion performance of the individual components are outlined in this section.

The objective in this work, is to derive expressions for the various aspects of receiver performance with respect the voltage gain, equivalent IP2 and IP3 (written as a voltage) and a noise resistance for each block. With this in mind, a few useful relationships can be obtained by examining a simple plot of an individual receiver

component's intermodulation intercept point. Take the example of any generic component with an output 3rd intermodulation intercept point as shown in figure 20.

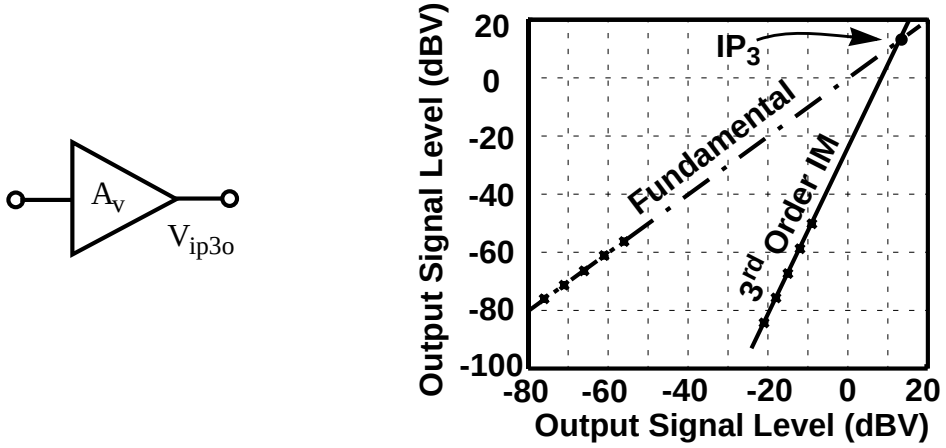

Figure 20. Simple Amplifier with voltage gain Av and Output Third order intercept V_{ip3o}

The plot in figure 20 takes a little examination to understand its meaning. The plot is of the output response both the linear and the 3rd order component as a function of the magnitude of the *output* signals which are intermodulating *at the output of the amplifier* (a two tone test). Both the x and y axis are the *output* signal levels in dBV. Therefore, given the output 3rd order intercept point, we can read both the linear component of the intermodulating signals and the 3rd order component produced by the two intermodulating signals as a *function of the output power in* dBV *of the two signals which are intermodulating*. A very useful expression that can determine the magnitude of the 3rd order response, at the output or input of a receiver block, as a function of the output or input IP3 respectively is [2.8],

$$V_{o3^{rd}} = \frac{V_{inter(o)}^{3}}{V_{IP3o}^{2}} \qquad \text{(Eq 2.40)}$$

Where V_{o3rd} is the output 3rd order component generated by two adjacent channel interfering signals at the output of the amplifier of magnitude $V_{inter(o),}$ this is illustrated in figure 21. Likewise, at the input of the same amplifier one could write,

$$V_{i3^{rd}} = \frac{V_{inter(i)}^{3}}{V_{IP3i}^{2}} \qquad \text{(Eq 2.41)}$$

Where V_{ip3i}, $V_{inter(i)}$, and V_{i3rd} are the input intercept point, the intermodulating tones, and the input referred third order component respectively, again this illustrated in figure 21.

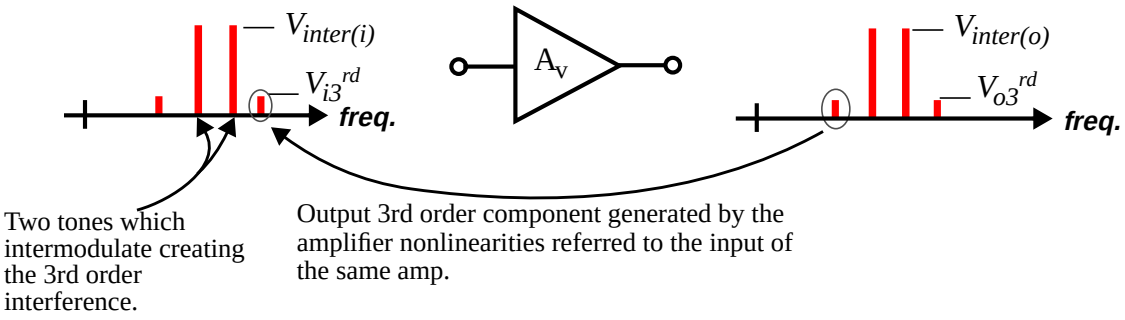

Figure 21. Representation of the adjacent channel interferers and the intermodulated 3rd order component which is created.

All variables in equation 2.40 are related to the input of the simple block shown in figure 17. Equation 2.40 and equation 2.41 can be extend to a more generalized expression to describe the distortion components generated by any order intermodulation at a given node in a receiver chain,

$$V_{dn} = \frac{(V_{inter})^n}{(V_{IPn})^{n-1}} \qquad \text{(Eq 2.42)}$$

2.3.2.2 Intermodulation for cascaded blocks

There are several methods for calculating both an intermodulation interferer at any stage in the receiver and the equivalent Intermodulation Intercept Point (IIP). Again, the example of the 3rd order IM will be used to find the equivalent IIP3 of several cascaded blocks. Although, this analysis could easily be extended to any order

of intermodulation. The equivalent input or output intercept point of a three stage

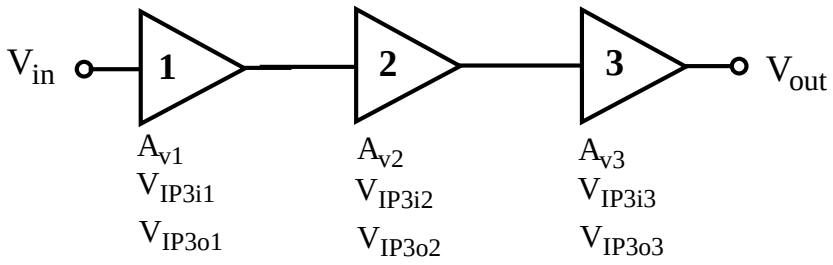

Figure 22. Intermodulation in a set of cascaded blocks.

cascaded network will be determined, figure 21, as a function of the input or output intercept points of the individual blocks in the chain. A_{vn} is the voltage gain of the n^{th} block and V_{IP3in} and V_{IP3on} are the equivalent input and output voltage intermodulation intercept points respectively of the n^{th} block. Two methods to finding the equivalent intercept point at the output or input of a cascaded network are now explored.

The first and simplest approach is to reflect each of the individual intercept points to either the input or the output of the cascaded blocks and find the minimum term and approximate this as the intermodulation intercept point for the cascaded chain [2.9].

$$V_{ip3cascade} = \min\left(V_{IP3i1}, \left(\frac{V_{IP3i2}}{A_{v1}}\right), \left(\frac{V_{IP3i3}}{A_{v1}A_{v2}}\right)\right) \qquad \text{(Eq 2.43)}$$

Equation 2.43 works well when trying to predict the intermodulation performance of a number of cascaded blocks, when there is a “weak link” in the chain and one input or output intercept point dominants (much lower in the case of IP3) the cascaded IP3. However, when the individual IP3s contribute somewhat equally to the overall chains linearity performance, then equation 2.43 is not a good approximation.

The second approach to estimating the equivalent receiver IP3, attempts to take into account the interaction of the intercept points between the cascaded blocks in the chain. In this approach, the assumption is that the distortion contribution from each of the blocks is uncorrelated, thus their distortion products are independent from block to

block. If we write the total 3rd order distortion products at the output of the cascade chain, shown in figure 5, we get [2.8],

$$V_{out}^{3rd} = A_{v3} \cdot A_{v2} \cdot V_{o1}^{3rd} + A_{v3} \cdot V_{02}^{3rd} + V_{o1}^{3rd} \quad \text{(Eq 2.44)}$$

Where V_{out}^{3rd} is the *total* 3rd order distortion of the cascaded configuration and V_{o1}^{3rd}, V_{o2}^{3rd}, and V_{o3}^{3rd} are the output distortion contributions of each of the blocks. We can now reflect the output distortion to the input, to find the equivalent input IP3 of the three cascaded blocks,

(Eq 2.45)

$$V_{in}^{3rd} = \frac{A_{v3} \cdot A_{v2} \cdot V_{o1}^{3rd} + A_{v3} \cdot V_{02}^{3rd} + V_{o3}^{3rd}}{A_{v1} \cdot A_{v2} \cdot A_{v3}}$$

Expressing each of the 3rd order distortion components using equation 2.40 gives,

$$\frac{V_{in}^3}{(V_{iIP3cas})^2} = \frac{A_{v2} \cdot A_{v3} \cdot \frac{(V_{o1})^3}{(V_{IP3o1})^2} + A_{v3} \cdot \frac{(V_{02})^3}{(V_{IP3o2})^2} + \frac{(V_{o3})^3}{(V_{IP3o3})^2}}{A_{v1} \cdot A_{v2} \cdot A_{v3}} \quad \text{(Eq 2.46)}$$

As noted previously, the assumption is that the distortion components generated from different blocks are uncorrelated which may not necessarily be true and the potential exist for cancellation of the third order distortion from stage to stage. However, within an individual block, the distortion is correlated between the input and output. Therefore, the output IP3 for an individual block may be reflected back to the input of the same block, or $V_{IP3in}=V_{IP3on}/A_{vn}$ for the n^{th} stage. Also, an expression can be given for all of the output voltages in terms of V_{in} and the voltage gain A_v of a block. Equation 2.46 now becomes,

(Eq 2.47)

$$\frac{V_{in}^3}{(V_{iIP3cas})^2} = \frac{A_{v2}\cdot A_{v3}\cdot \frac{(A_{v1}\cdot V_{in})^3}{(A_{v1}\cdot V_{IP3i1})^2} + A_{v3}\cdot \frac{(A_{v1}\cdot A_{v2}\cdot V_{in})^3}{(A_{v2}\cdot V_{IP3i2})^2} + \frac{(A_{v1}\cdot A_{v2}\cdot A_{v3}\cdot V_{in})^3}{(A_{v3}\cdot V_{IP3i3})^2}}{A_{v1}\cdot A_{v2}\cdot A_{v3}}$$

Cancelling terms we get the familiar form of,

$$\frac{1}{(V_{iIP3cas})^2} = \frac{1}{(V_{IP3i1})^2} + \frac{A_{v1}{}^2}{(V_{IP3i2})^2} + \frac{(A_{v1}\cdot A_{v2})^2}{(V_{IP3i3})^2} \quad \text{(Eq 2.48)}$$

The total input referred IP3 for the cascaded configuration shown in figure 22 is,

$$V_{iIP3cas} = \frac{1}{\sqrt{1/(V_{IP3i1})^2 + A_{v1}{}^2/(V_{IP3i2})^2 + (A_{v1}\cdot A_{v2})^2/(V_{IP3i3})^2}} \quad \text{(Eq 2.49)}$$

A similar analysis reveals that for a two stage cascaded network the equivalent output IP3 can be expressed as,

$$V_{oIP3cas} = \frac{A_2\cdot V_{IP3o1}\cdot V_{IP3o2}}{\sqrt{(V_{IP3o2})^2 + (V_{IP3o1})^2}} \quad \text{(Eq 2.50)}$$

And the equivalent input IP3 of the same two stage network is,

$$V_{iIP3cas} = \frac{V_{IP3i1}\cdot V_{IP3i2}}{\sqrt{(V_{IP3i2})^2 + (A_{v1}\cdot V_{IP3i1})^2}} \quad \text{(Eq 2.51)}$$

Both equation 2.50 and equation 2.51 can be used recursively to obtain the equivalent IP3 at any node in a cascaded chain of receiver components. Using either equation 2.50 or equation 2.51 in conjunction with equation 2.40, the equivalent 3rd order distortion component, which is seen as an interferer to the desired signal, may be found at any point in the receiver chain. The 3rd order inference can then be added with

the rms noise in the receiver chain to find the carrier-to-(noise-plus-distortion) ratio at any point in the receiver chain.

Generally speaking, from equation 2.51 the distortion performance of a receiver chain is degraded when more gain is used toward the front end. This is in contrast to the noise figure performance, where as much gain at the absolute front end of the receiver is desired. Thus, the classic trade-off between receiver noise figure and intermodulation performance becomes more apparent. As will be discussed in chapter 3, this trade-off becomes more complicated when trying to integrate all of the receiver functionality onto a single chip. Integrated receivers typically lack high-Q filtering until the signal is frequency translated to near baseband. Thus, both the blocking and intermodulating components see little, if any filtering until much later in an receive chain than would otherwise be seen in a discrete implementation of a receiver where high-Q filters are used much closer to the front-end.

2.3.2.3 Intermodulation Requirements in DECT and GSM

Both the DECT and GSM standards outline a set of requirements on the immunity of a receiver to two adjacent or alternate channels intermodulating with each other. This specification, as with most standards, is given in the form of the magnitude of two interfering signals spaced in frequency, in such a way that the third order component generated falls in the band of the desired signal. A desired modulated signal is then applied to the receiver with the two interfering tones. The performance of the receiver is then measured in terms of the bit error rate. Some specific example tests are now given for both GSM and DECT. These examples are given to illustrate how to transform the required tests associated with a standard, to an equivalent required input IP3 for the entire receiver.

In GSM, the adjacent channel immunity test is performed by applying two unmodulated carriers with a power level of -49 dBm to the input of the receiver while a

signal 3dB above the reference sensitivity is applied (-99 dBm for GSM 900, E-GSM, and PCS 1900. -97dBm for DCS 1800). The receiver must maintain a 10^{-3} BER or 9dB C/I at the output of the receiver, while performing the adjacent channel test. However, this also includes the effects of noise in the receiver channel. Therefore, the distortion components, plus the white noise in the receiver, degrade the overall C/(I+N) at the receiver output. The desired signal level is 3dB above the sensitivity requirement. If the noise floor, at the output of the receiver, is just low enough to pass the sensitivity test, than it can be assumed that the noise floor referred to the input is 9dB (to meet 9dB CNR required at the output of the receiver) below the sensitivity requirement. This implies that the maximum receiver input referred noise floor is at -111 dBm. Both the noise and 3rd order components are uncorrelated. Therefore, if the 3rd order IM is kept at or below the noise floor, then the total interference to the carrier from both noise and 3rd order intermodulation will raise the interference floor by 3dB, and the C/(I+N) ratio will be at 9dB or better; this is illustrated in figure 23.

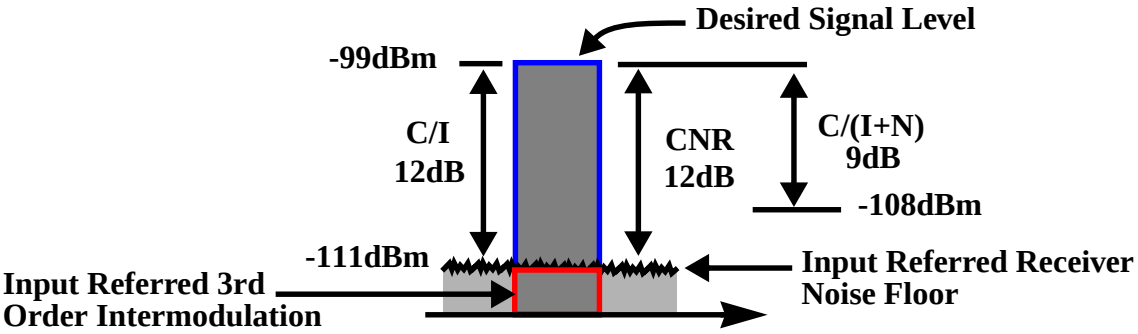

Figure 23. Maximum allowable input referred noise and distortion levels under the intermodulation test for DCS 1800.

The desired signal is at -99 dBm and it is desired to have all the distortion from the receiver to remain 12 dB below the desired signal or at -111 dBm. If the two intermodulating adjacent channels are applied to the receiver at -49 dBm, then the IM3 component must be greater than,

$$IM3 = -49\text{dBm} - (-111\text{dBm}) \qquad \text{(Eq 2.52)}$$

The IM3 component decreases at a rate of 20dB/decade for every decade increase in input power. Therefore, the input referred IP3 can be expressed as,

$$IP3 = -49\text{dBm} + \left(\frac{IM3}{2}\right)\text{dBm} \quad \text{(Eq 2.53)}$$

Which gives us a -18 dBm input referred IP3 or better required of the receiver to be compliant with the GSM standard.

Similar to GSM, the DECT standard outlines a set of conditions to test the intermodulation performance of the receiver. A desired carrier is applied to the receiver 3dB above the reference sensitivity or -80 dBm. Two adjacent channel signals are applied with a -46 dBm input power. Using the same procedure to calculate the input referred IP3 as in GSM, gives an IP3 of,

$$IP3_{DECT} \geq -22\text{dBm} \quad \text{(Eq 2.54)}$$

2.4 General comments on Receiver Design

Throughout this chapter, the emphasis was on relating some of the classic receiver non-idealities, such as noise figure, intermodulation, and phase noise to the selectivity and sensitivity figures of merit. Two key receiver characteristics which were not covered in this chapter are image rejection and filtering, both of which affect the selectivity performance. Image rejection will be discussed in detail throughout chapters 5 and 6 while filtering goes beyond the scope of this thesis.

The objective of any receiver systems is usually to provide filtering, gain and frequency translation of the received signal spectrum before the desired information is recovered through some method of detection (see figure 24(a)). The distribution of the gain, filtering and the method as well as frequencies used for frequency translation, all will have an impact on the receiver selectivity and sensitivity performance. Each of the receiver impairments will interact with one another and between various blocks along the signal path. This interaction concept is illustrated in figure 24(b), where the

relationship between receiver characteristics and performance in terms of selectivity and sensitivity are shown. As was described in this chapter, the more gain used toward the front of the receiver will improve the overall receiver noise figure. However, an increase in front-end gain will place a greater demand on the linearity performance of the subsequent receiver blocks. As will be described in chapter 3, this problem or trade-off between gain, noise figure and linearity is exacerbated by the very act of attempting to integrate all of the receiver components on to a single chip. Most of the proposed high integration architectures perform filtering much later in the receive chain, than a discrete component implementation of a receiver. Therefore, adjacent and alternate channel blockers as well as potentially intermodulating spectral components are passed through more of the receive chain in an integrated solution as compared to a discrete receiver. This makes the selection of gain distribution along the receive chain particularly challenging to accommodate a good noise figure and linearity performance. The last receiver characteristic which will ultimately affect virtually all of the receiver characteristics is the power consumption. Most receiver non-idealities in the signal path may be improved by increasing the overall power consumption of the active components used by the receiver. For portable applications, the trade-off is between providing adequate receiver performance with a minimal amount of power consumption.

Receiver system design usually takes place by modeling the receive channel with respective to linearity, noise, filtering, gain and phase noise. The distribution of the gain and filtering are usually attached to a target linearity, blocking and noise figure performance. Both the design and interaction between various receiver characteristics are addressed through the use of a “link budget”. A link budget also provides a method of book keeping to track of the required performance of individual circuit blocks along the receive chain. An example link budget for the GSM/DECT receiver presented in later chapters of this thesis is described in [2.4]. The link budget, in some respect, is similar to accounting principles making spread sheet software useful when designing a

receiver from a higher system level. The Excel spread sheet used to generate the link budget for the GSM/DECT receiver may be found at [2.10].

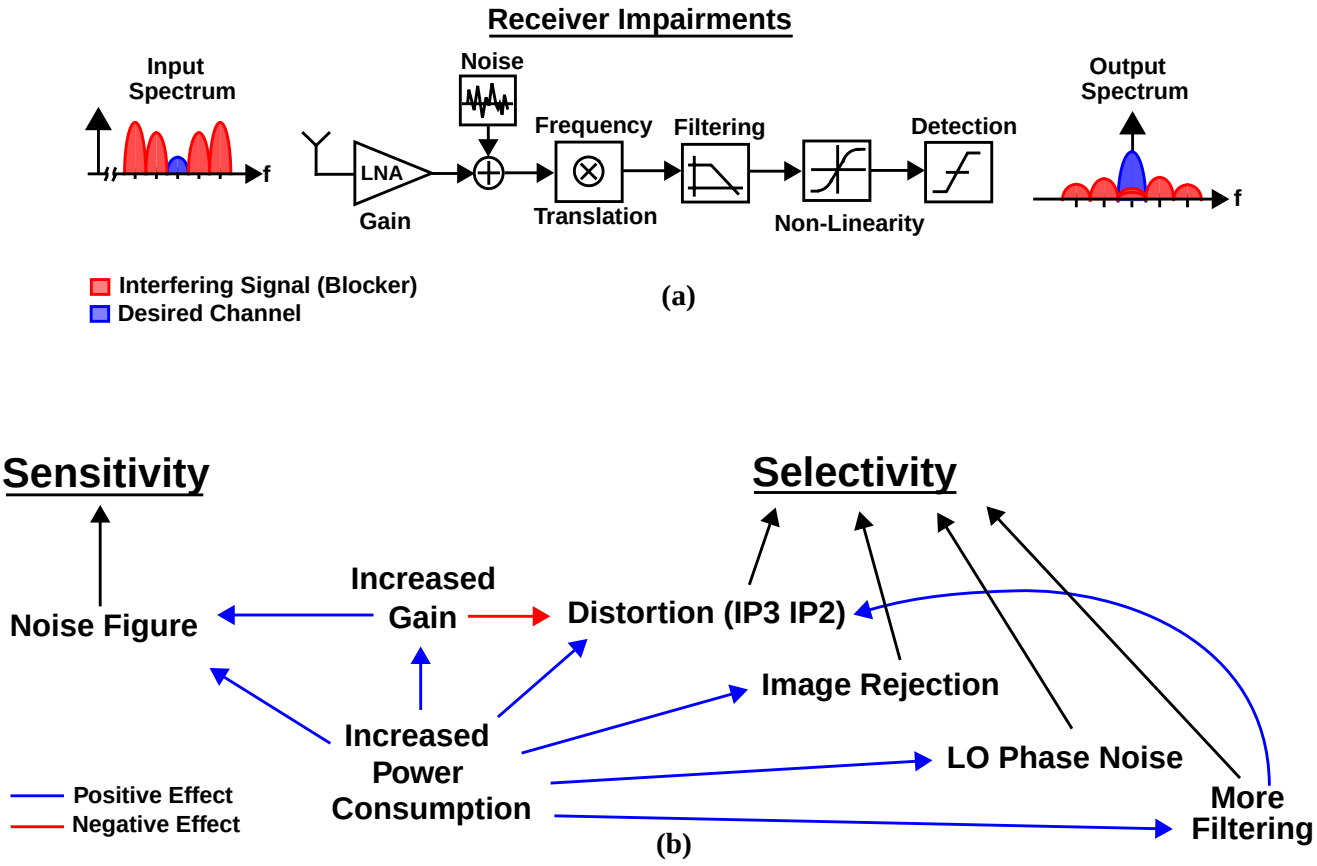

Figure 24. (a) Receiver Impairments (b) Interaction between various receiver characteristics and performance.

With an understanding of how various receiver characteristics can influence the selectivity and sensitivity performance, the discussion will now turn toward the issues associated with integration. Chapter 3 will first review the challenges of integrating a radio on to a single chip. The next chapter will then examine some recently proposed radio architectures which attempt to maintain the selectivity and sensitivity performance of a receiver and achieve high levels of front-end radio integration.

2.5 References

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Chapter 3

Integrated Receiver Architectures

3.1 Introduction

With a quick review given on some of the general issues surrounding receiver system design and implementation, the focus will now turn toward the challenges associated with the integration of a radio receiver on to a single silicon substrate. Specifically, this chapter will try to give the reader an appreciation of the difficulty indelivering comparable performance with an integrated CMOS radio as that which is achievable in more conventional discrete component receivers. The material in this section begins by examining one of the more popular implementations of a discrete radio architecture known as the superheterodyne system which is characterized by excellent performance with respect two key receiver figures of merit; mainly the selectivity and the sensitivity performance. A functional understanding of a discrete component receiver will then serve as a backdrop for a discussion on the challenges associated with integrating all of a radio receiver components, on to a single silicon die. This is followed by an evaluation of several proposed receiver architectures which attempt to overcome some of the hurdles associated with integration of radio components. This chapter will conclude with a somewhat in-depth look at a recently proposed radio receiver system called Wide-Band IF with double conversion. This

architecture attempts to facilitate receiver integration, particularly for applications which require narrow channel tuning along with a low phase noise performance synthesizer (narrow channel tuning and low phase noise typically go hand-in-hand).

3.2 Superheterodyne Receiver

Although to date there has been a heavy emphasis from the communications industry to build commercial radios which are highly integrated, most RF high performance transceivers manufactured today still utilize some variant of a conventional superheterodyne architecture. The “superhet” as it is often referred to as, was originally developed by Edwin Amstrong at the end of World War I, he patented the idea in 1917[3.1]. The contemporary version of the superheterodyne receiver, shown in figure 25, is implemented with a collection of both passive and active discrete components. Various semiconductor technologies such as gallium arsenide, silicon bipolar and CMOS are used to realize many of the active high frequency components along the receiver chain, such as the low noise amplifier, mixers, and analog baseband circuits.

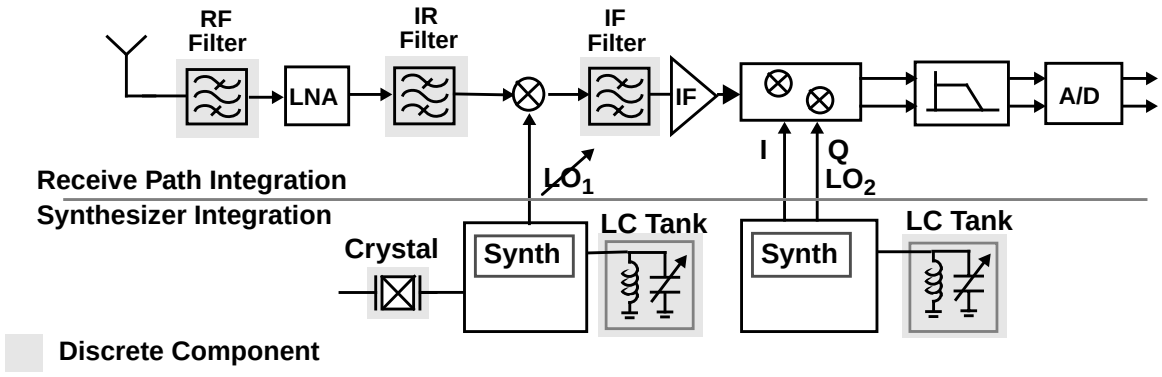

Figure 25. Dual-Conversion Conventional Super-Heterodyne Receiver.

In conventional radio design, probably two of the broadest and most comprehensive figures of merit are the sensitivity and selectivity performance of a

receiver. Both of these figures of merit were described in chapter 2. As will be described later, the selectivity performance of a receiver is typically the more difficult performance metric to address when attempting to integrate a receiver onto a single chip. The longevity of the superhet is due in part, to both the high selectivity and sensitivity performance which may be obtained utilizing this approach. A convenient starting point for the discussion of integrated receiver architectures is to first understand why a superheterodyne system affords such high performance. A quick overview of the superhet will begin at the antenna, and move down the receiver chain with a description of the functionality provided by each of the components.

In short, the typical objective of a receiver is to provide three basic forms of signal processing; discriminate the desired received signal from other users at alternate frequency bands, down-convert or frequency translate the desired signal to a low frequency and provide sufficient variable gain to both accommodate a broad range of received signal power as well as minimize the noise contribution from the entire receive signal path. Shown in figure 26, is a hypothetical spectrum as it passes through various stages of a super-het. At the antenna, the desired channel is shown in the presence of other channels found within that user's standard. All of the channels together form the "inband" spectrum which are defined both in bandwidth and power level by a radio standard. Examples of inband signals would be the entire band comprising the 75, 200kHz channels associated with DCS 1800 or the entire spectrum from 1.88GHz to 1.89GHz associated with the DECT standard in Europe. Any signal energy which is not apart of the users system is typically referred to as out-of-band signals or out-of-band blockers. The RF filter follows the antenna and is used to perform a first order attenuation of all out-of-band energy. After the RF filter, the entire spectrum including both the inband and residual out-of-band energy is gained up with an amplifier optimized to contribute a minimal amount of noise, this component is typically referred to as a low noise amplifier or LNA. At the LNA output, a sufficient amount of gain has been added to the signal to overcome the large amount of noise introduced to the

desired signal band while passing through the function of frequency translation, which is performed by a component called the mixer.

In a superheterodyne receiver, the signal applied to the RF port of the mixer is down converted, in frequency, with a tunable local oscillator which tunes to any of the channels associated with a standard or system. The entire spectrum present at the RF port of the mixer is frequency translated, either up or down, between the mixer input and output. The amount of translation in frequency is the difference between input band and the frequency of the local oscillator, this difference frequency is often described as the intermediate frequency or just IF. Both the bands above and below the frequency of the first local oscillator will translate to the same intermediate frequency. The other undesired band below the LO frequency (in the case of figure 26) is referred to as the image band. Without filtering, the image band could potentially overwhelm the desired signal at IF. Thus, some form of image attenuation must be implemented. In the case of the superheterodyne receiver, the RF filter provides an initial filtering of the image band. After the LNA, an image-rejection filter or sometimes referred to as a noise filter specifically attempts to further attenuate signals present within the image band. Although at first glance it would appear that the RF and image rejection filters have an identical role, this isn’t quite true as all of the image attenuation could be placed before the LNA. However, the image rejection filter has the additional function of suppressing noise emitted from the LNA, which resides in the image band. Thus, the reason why this filter is placed after the LNA and not before. Without the image rejection filter, the mixer would frequency translate the LNA output noise from two bands and effectively double the noise figure of the LNA. This leads to the origin of the name “noise filter” which is used interchangeably with image-rejection filter.

The excellent selectivity performance of a super-het is due in part to how the carrier is frequency translated to IF and the analog signal processing which takes place at the IF portion of the receiver. After the noise filter, the desired carrier is down-converted to IF using a mixer which has a tunable local oscillator at one of the mixer inputs. The frequency synthesizer which feeds the first mixer is variable and tunes to the frequency of the desired channel to recover. This implies that the frequency translation of the desired carrier is always to the *same* IF frequency; shown as f_{IF} in figure 26. This is an important feature of a superheterodyne receiver as the desired channel always appears at the same IF frequency independent of the carrier frequency. Therefore, at the output of the first mixer, adjacent channel energy may be filtered using what is commonly called an IF filter. Because the adjacent and alternate channel energy has been attenuated, the desired band can be considered isolated from strong alternate channel blockers, this is illustrated in figure 26. This now implies that the desired

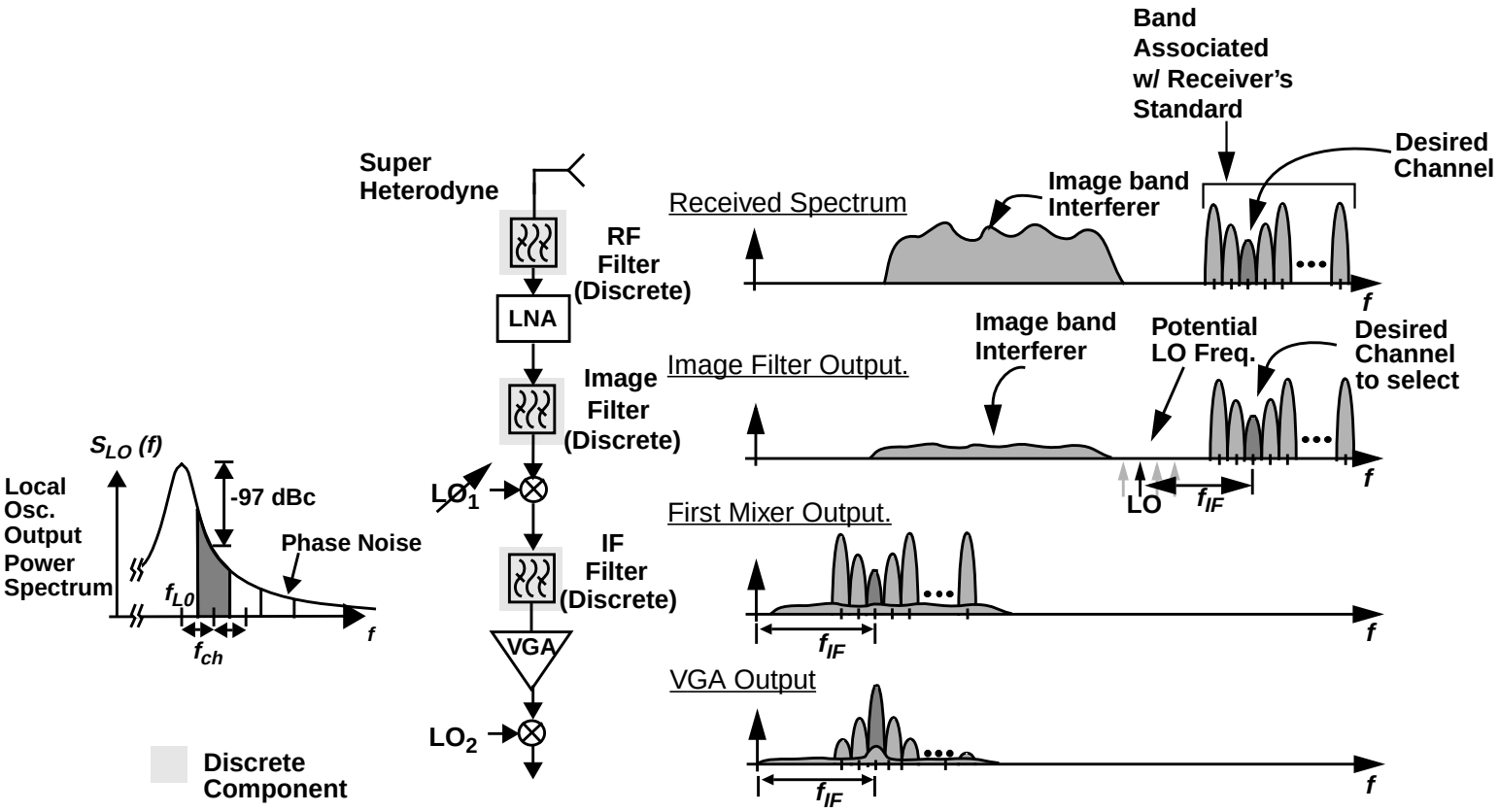

Figure 26. Basic step-by-step operation of a super-heterodyne receiver system. Excellent selectivity and sensitivity are provided by a distribution of high-Q filtering, gain and frequency conversion.

signal can have variable gain (done with a VGA) added which in turn reduces the required dynamic range and the linearity/intermodulation performance requirements of the subsequent receiver blocks. After the variable gain amplifier, the signal is then down converted to another IF stage with additional filtering, or down converted to baseband where additional channel filtering is then performed before symbol recovery (assuming the system uses some form of digital modulation) or frequency discrimination takes place.

The superior selectivity performance of a superheterodyne receiver is due primarily to the ability of this system to provide as much high Q filtering at the earliest possible point in the receive chain. In addition, the frequency synthesizers are typically realized with an external high-Q tanks which use discrete inductors and varactor diodes. A high-Q tank for the core resonant element in the frequency synthesizers results in a local oscillator with a very low-phase-noise profile, implying less degradation of the Carrier-to-Interference (C/I) ratio from reciprocal mixing of the phase noise with the alternate channel/band energy. Consequently, the increase in the receivers immunity to alternate channel signals and ultimately contributes to a better overall selectivity performance. In addition, high frequency, high Q filters in super-het as of yet are only available as a discrete component solution. Also, the discrete filters found in the signal path of a superheterodyne receiver have a frequency response which is tailored to either a standard’s band or channel bandwidth, making a receiver designed for one standard difficult or impossible to operate on another standard. Thus, when the superhet is realized using discrete components, as it typically is, the promise of developing a multi-standard implementation is relatively remote.

In summary, the superheterodyne receiver achieves excellent performance through a combination of high-Q filtering along the signal path as well as the available high-Q components used in the VCO tank circuitry. Therefore, the challenge of fully integrating a receiver is to replace the functions traditionally implemented with high-Q

discrete components with integrated on-chip solutions. Problems associated with full integration of the receiver can be separated into two categories. First, the integration of the receive signal path (see figure 25) requires the elimination or the replacement with an equivalent function of the discrete-component image-rejection and IF filters. Second, an integrated low-phase noise channel-select synthesizer must be realized using the relatively low-Q and poor phase-noise performance of on-chip VCOs or delay based elements for the core resonator. In addition, there is a desire to develop integrated receiver architectures which facilitate the implementation of programmable signal paths allowing both frequency tuning as well as variable filtering to address the requirements of multiple standards. Toward these goals, the rest of this chapter will focus on a few example implementations of high integration receivers and discuss the relative merits with respect to potential selectivity performance as well as the promise of realizing an integrated solution capable of multi-standard/mode operational.

3.3 Direct Conversion

One receiver architecture that eliminates many off-chip components in the receive signal path is the direct conversion, or homodyne architecture. This receiver system which is also sometimes referred to as a “Zero-IF receiver”, has been considered as early as 1924 [3.2], while one of the first radios to be built using direct conversion occurred in 1947 [3.3]. In the homodyne receiver, shown in figure 27, all of the in-band potential channels are frequency translated from the carrier directly to baseband using a single mixer stage. Energy from undesired channels is easily removed with on-chip filtering at baseband. In a direct conversion receiver, the IF stage is eliminated as is the need for image-rejection filtering, because the image is simply one of the sidebands about the carrier of the desired signal.

In direct conversion receivers, the channel filtering takes place at baseband, this has an advantage with respect to both integration as well as potential use in multi-

standard applications. With the desired channel modulated to baseband, this enables the implementation of integrated, high-Q filter structures capable of providing sufficient rejection of alternate channel energy before being digitized. Because the carrier is directly modulated to baseband, there exists the possibility of integrating programmable baseband signal processing either in the form of programmable filters or high-dynamic range ADCs followed by programmable digital channel filters to address variable bandwidth and frequency response requirements associated with different standards. Therefore, from the perspective of the receive signal path electronics, the direct conversion receiver holds the potential of allowing programmability between various standards as well integration of the entire receive signal path.

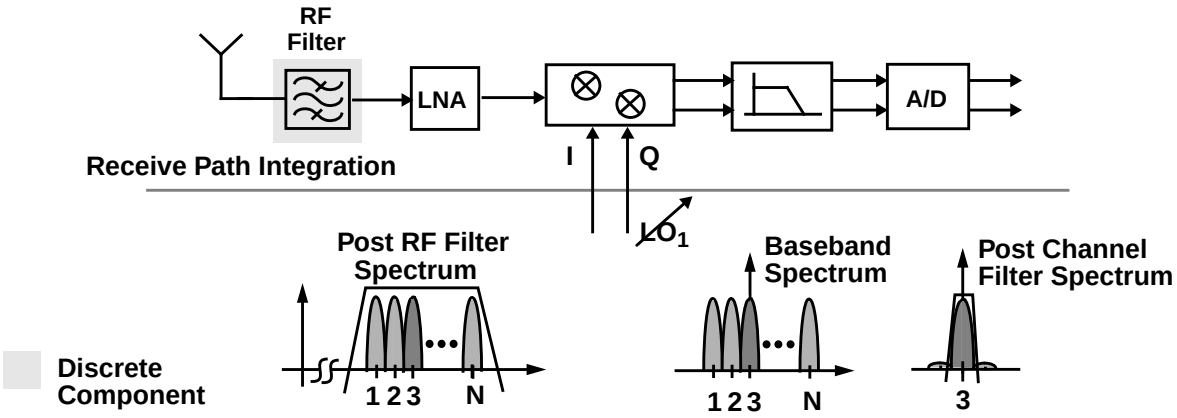

Figure 27. Direct Conversion Architecture.

With a plethora of advantages, one would think that zero-IF receivers should be prevalent in modern communication wireless receivers. However, there are several disadvantages to the direct conversion receiver which limits the performance, particularly as a fully integrated solution. For high-selectivity applications, the direct conversion receiver tends to be plagued with DC offsets which arise at the output of the mixer. This is particularly problematic as unwanted DC components appears as interference in the desired signal band. DC offsets which arise in a direct conversion receiver can be linked to a few separate mechanisms. The most well known source of DC offsets relates to an inherent feature of the direct-conversion receiver, mainly the

Local Oscillator (LO) is at the same frequency as the RF carrier. In this unique case, the potential then exists for the LO to leak to either the mixer input, or back to the antenna where radiation may occur, this is illustrated in figure 28. The unintentionally transmitted LO signal may reflect off nearby objects, which are physically moving relative to the receiver, and will be “re-received”. This re-reception of the LO is effectively modeled as the impedance of the antenna varying as a function of time. An amplitude varying component of the LO is reflected down the receiver chain and consequently self-mixes with the local oscillator resulting in a time-varying or “wandering” DC offset at the output of the mixer[3.4][3.5]. Another source of baseband DC offsets may arise from the LO coupling to the LNA or mixer input, again leading to self mixing and a DC offset. However, this offset mechanism is typically considered less severe than DC offset arising from the changing antenna impedance, as the LNA and mixer input impedance will remain relatively constant with time. Thus, the offset which is created via LO leakage through the LNA and mixer input paths will also hold constant and is easier to address with offset cancellation schemes.

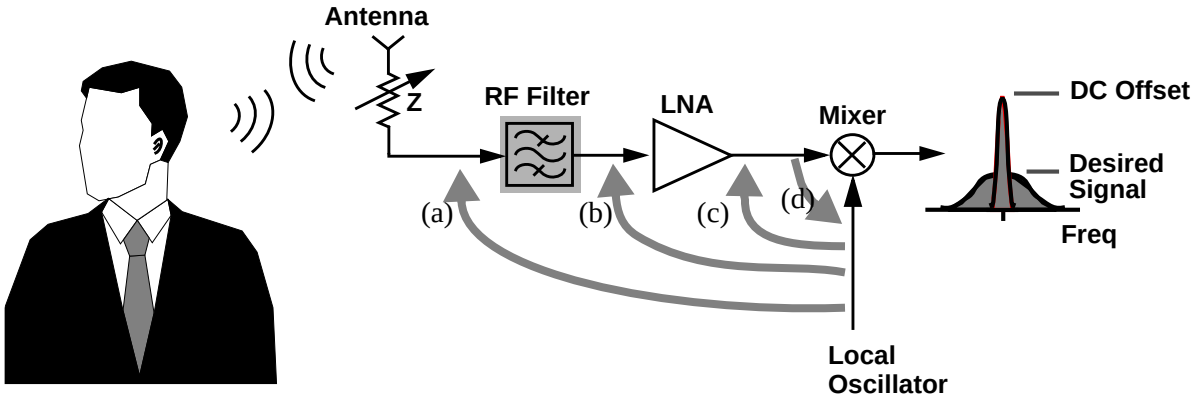

Figure 28. LO Leakage paths which lead to DC offset in Direct Conversion Receivers. (a) LO to Antenna with varying impedance (b) LO to LNA input (c) LO to Mixer input (d) Mixer Input to LO output

In addition to the well known LO leakage problem, other offsets in a direct conversion receiver will arise at the mixer output. For high selectivity applications, large adjacent and alternate channel AM blockers can potentially be received. In a

mechanism which is virtually the reverse of LO leakage, the AM blocker present at the mixer RF input can couple to the area around the mixer LO port. This again creates the situation where two identical frequency components exists at both the mixer RF and LO ports. Thus, LO self-mixing may occur, resulting in a DC component at the mixer output. Similar to the LO leakage to the antenna, the adjacent channel AM blockers may vary as a function of time, creating an offset which is potentially difficult to cancel. In addition, the same adjacent channel AM blocker when frequency translated to baseband may create an additional offset when passing through the circuit non-linearities. Specifically, the second order non-linearities associated with the baseband circuits will provide a processes by which a DC offset is created from an alternate channel blocker. Thus, the particular importance of designing baseband circuits with excellent second order intermodulation performance when intended for use in a direct conversion receivers. Both IM2 and the process by which DC offsets arise from blockers passing through the second order non-linearities were discussed with more detail in chapter 2.

The last component of interference found at baseband in the direct conversion approach, relates to low frequency 1/f noise. Although not limited to a particular semiconductor technology, 1/f tends to be more severe in CMOS processes. The contribution from 1/f noise is roughly inversely proportional to the device size and may be reduced by careful selection of larger aspect ratio devices. However, this is done at the expense of reduced performance with respect to speed and/or power consumption of the baseband components.

Much of the research and development which is aimed at realizing practical implementations of direct conversion receivers attempt to mitigate the affect of DC offsets on the receive channel. One such approach is to simply remove the DC signal component at the output of the mixer. This is typically done by utilizing an AC coupling capacitor between the mixer output and baseband filter input. The ability to realize the AC coupling capacitor on-chip is often dependent on the overall system, both the

modulation scheme and more importantly the bandwidth. For many wireless LAN standards with wide-channel bandwidths, a significant amount of energy may removed from the signal around DC without a significant bit-error-rate penalty, allowing the use of DC offset cancellation with on-chip passive components. In this situation, a small AC coupling capacitance, compatible with on-chip integration, may be used to cancel the offset. An example of DC offset cancellation using integrated coupling capacitors can be found in [3.6]. For narrower channel bandwidths or systems that utilize modulation schemes more sensitive to removing a significant amount of energy around DC, the AC coupling elements are sized such that they must be placed off chip, an example of this approach is given in [3.7].

A more sophisticated approach to removing DC offsets in direct conversion receivers, is to estimate what offset exists at the mixer output. Based on the estimation, the offset can be canceled or negated from the mixer output. Such approaches usually rely on a known sequence of bits which may be used for calibration in estimating the DC offset that exist. Recent attempts in utilizing such cancellation schemes use the header associated with a received frame to estimate the baseband offset [3.8][3.9] as illustrated in figure 29. This estimation is then used to cancel the offset for the

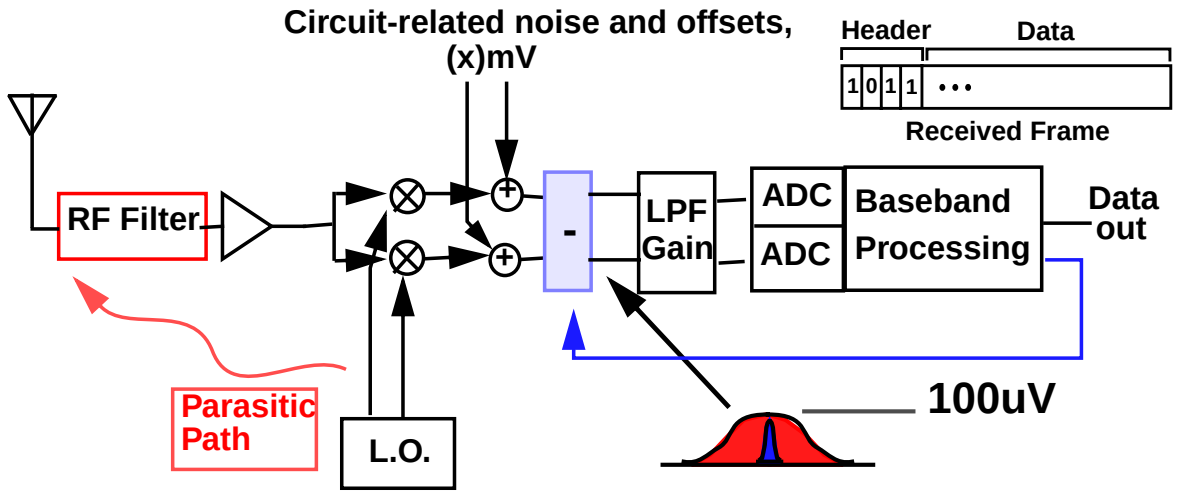

Figure 29. DC offset cancellation in Direct Conversion receivers (figure courtesy of Paul Gray).

remainder of the frame. In general, this approach assumes that the offset will remain constant for the entire portion of time a frame is received. However, standards and systems exist which require that the baseband be immune to offsets which may arise mid-frame. One example of a rapidly varying DC offset is written in the GSM standard, where a large alternate channel AM blocker may suddenly appear after the frame header and DC offset cancellation takes place. This leaves the potential situation for a new offset, created by the blocker and baseband second order non-linearity, to appear after the DC offset cancellation algorithm has been applied. In this case, the remainder of the frame could be lost from saturated baseband circuits.

Although the direct conversion receiver nicely integrates the receive signal path, there still exists some challenges with the integration of the synthesizer section of the receiver. This is particularly true for applications or standards with narrow channel spacing and aggressive phase noise requirements. This is often the case with cellular standards where the channel spacing is narrow and the blocking requirements are particularly severe. As an integrated solution, the resonant tank phase noise performance is rather weak compared to the discrete component counterpart making complete integration of the synthesizer rather challenging at high frequency with narrow channel tuning. However, for applications with wider channel spacings and less aggressive phase noise requirements on the local oscillator, as is the case in many indoor WLAN standards, complete integration of the synthesizer with the resonant tank elements is certainly attainable for a direct conversion solution; this has been demonstrated in [3.6][3.10] and [3.11].

3.4 Low-IF Architectures

An obvious alternative to address the DC offset problems introduced in a direct conversion system, is to down-convert the carrier to a very low IF, rather than directly to baseband. The Low-IF receiver[3.12][3.13], shown in figure 30, is almost identical to

a direct conversion system in the sense that only a single mixer stage is used to frequency translate the carrier to a low IF; where the IF for the desired signal is offset by one or two channel bandwidths from DC.

Similar to a direct conversion receiver, the low-IF architecture requires the use of only one discrete filter, the RF filter. The primary advantage of a low-IF receiver is the fact that the carrier is offset from DC. Therefore, Zero-IF receivers are less susceptible to the mechanisms which create DC interference which include, second order intermodulation, LO leakage and accumulated offset created by the baseband blocks. However, the low-IF system comes with certain drawbacks, the most noticeable being the requirements on image-rejection as well an increased bandwidth and dynamic range requirements on the baseband blocks. The low-IF receiver relies on the fact that most standards have a blocking profile where the strength or magnitude of the blocker increases as one moves further away from the desired carrier in frequency; one example blocking profile was given for GSM in section 2.3.1.1 of chapter 2. Thus, the reason why low-IF receivers typically frequency translate the carrier to an IF of no more than one or two channels away from DC. Here, the image-rejection required of the front-end is minimal, as it would need to be, because unlike many heterodyne systems the image-

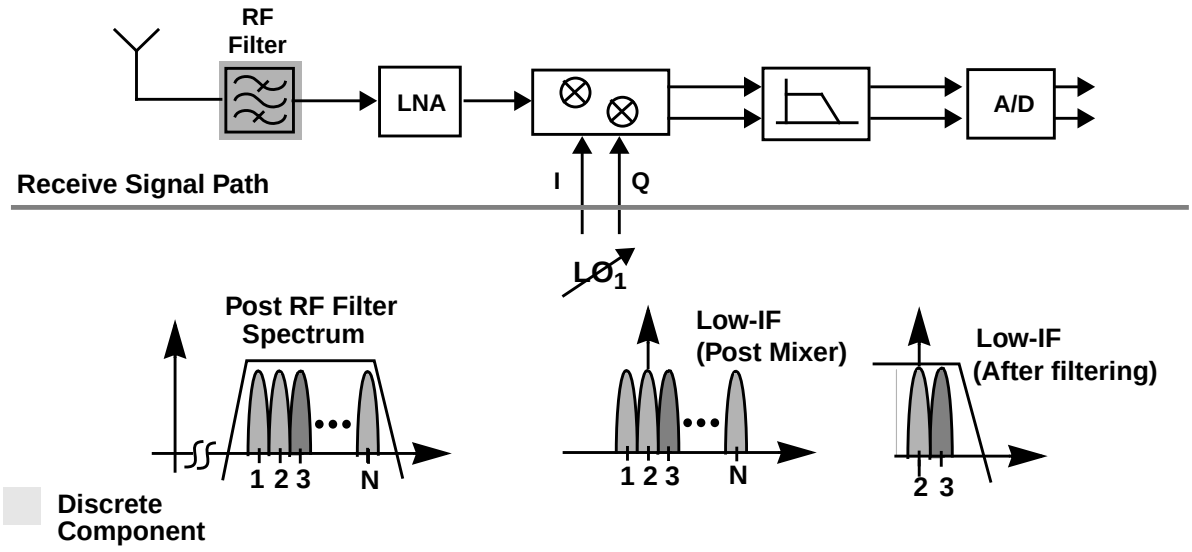

Figure 30. Conceptual diagram of a Low-IF receiver.

rejection function is not shared between multiple components; the frontend RF filter provides no benefit with respect to image rejection. All of the image rejection must be performed with some Weaver like structure, which limits the entire receiver to around 45dB of image suppression.

Dependant on the standard used, blockers on the lower sideband of the first local oscillator are frequency translated closer to the desired signal at the output of the first mixer, this is illustrated in figure 31. From the figure, it becomes obvious that the blockers on the lower sideband of the first mixer move closer to the desired signal by $2\ \omega_{IF}$. Assuming an ADC is used to digitize the signal, a higher order filter would be required at IF, to remove an equal amount of alternate channel energy as compared to a similar filter used by a direct conversion system. An alternative to using a higher order filter in the low-IF receiver, would be the use of an ADC with a higher resolution as compared to a direct conversion receiver. Such an ADC would require higher resolution as well as an increased bandwidth in a low-IF receiver. Both the higher resolution and bandwidth required in the baseband, of a low-IF receiver, would have an associated power penalty when compared to a direct conversion receiver.

As mentioned earlier, the Low-IF receiver is mainly limited to system where the signal strength of the immediate adjacent channel signal is quite relaxed, which ultimately reduces the image-rejection required by the signal path. This happens to be the case for a couple of recently demonstrated receiver systems[3.14][3.15][3.12][3.13] one for GPS, while the other prototype was built for GSM. In the case of the GSM standard, the immediate adjacent channel to carrier power ratio is no more than 9dB above the adjacent channel signal. Therefore, given that the required C/I at the output of the receiver, is 9dB, implies that only about 20dB of image-rejection is required by the Weaver like structure in a low-IF receiver. This translates to rather moderate phase and gain matching between the I and Q signal paths.

Similar to a direct conversion receiver, the synthesizer required to generate the local oscillator for the first mixer operates near the frequency of the RF carrier. Therefore, it is rather challenging to realize a low-IF architecture for applications or standards that require a synthesizer capable of generating narrow-channel spacings, with a low phase noise profile, at RF, with a fully integrated VCO.

Overall, the integrated Low-IF system presents an interesting alternative for certain applications where DC offset cancellation cannot be adequately performed using a direct conversion solution. However, low-IF receivers are only appropriate for

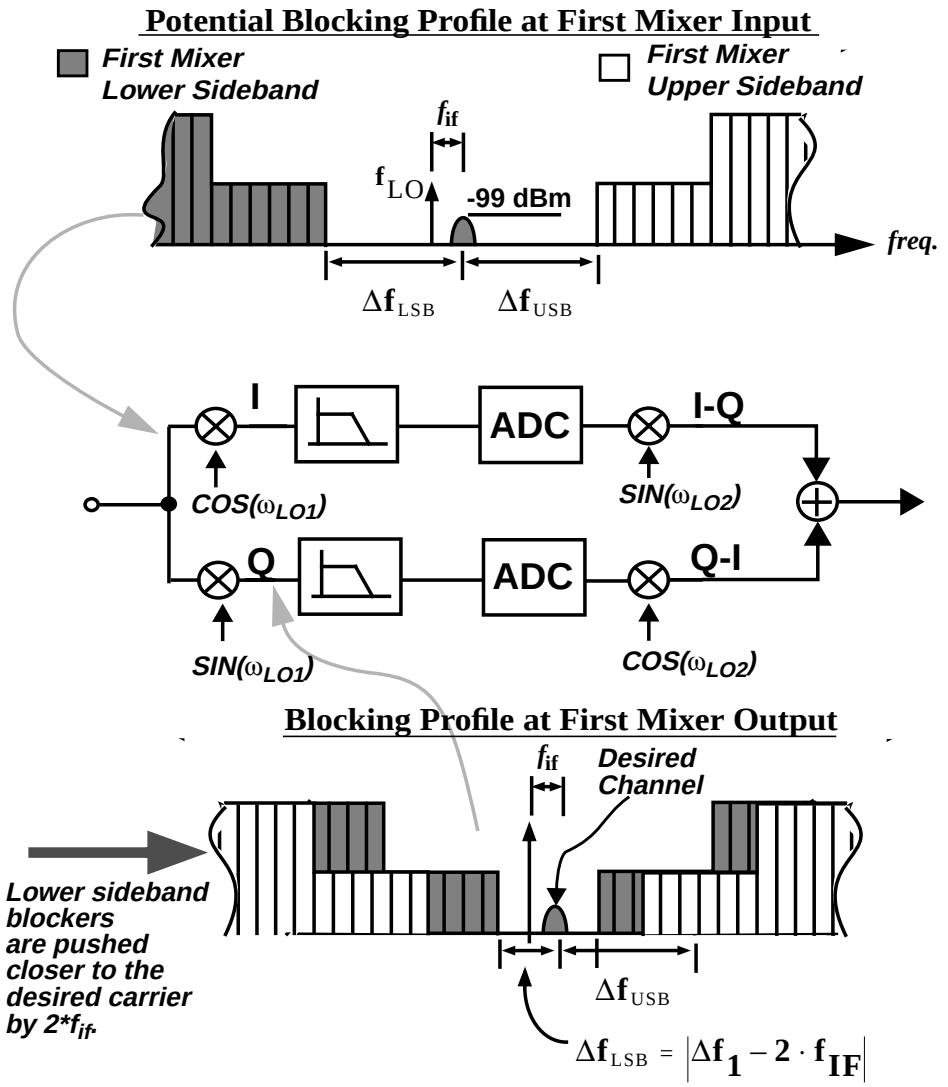

Figure 31. Blockers from one sideband about the first local oscillator move closer to the desired carrier when frequency translated by the first mixer.

standards with relaxed adjacent channel blocking requirements. In addition, the baseband implementation may be quite challenging with respect to bandwidth and dynamic range requirements. It is also not clear how a single baseband signal path could be made programmable between various standards with diverse channel bandwidth profiles.

3.5 Double Low-IF Receiver.

An additional interesting example of a proposed integrated receiver architecture is the Double-Low-IF system [3.16][3.17][3.18], shown in figure 32. As the name implies, a two step conversion approach is used based on an architecture originally proposed by Donald Weaver in 1956 [3.32]. The basic concept is to utilize quadrature mixers and a RF channel-tuning synthesizer which both tunes and down-converts the desired channel to a low IF. The I and Q channels at IF, are then up converted in frequency, to a high IF using a fixed frequency synthesizer. The signal is then feed off chip where a standard discrete IF filter may be used.

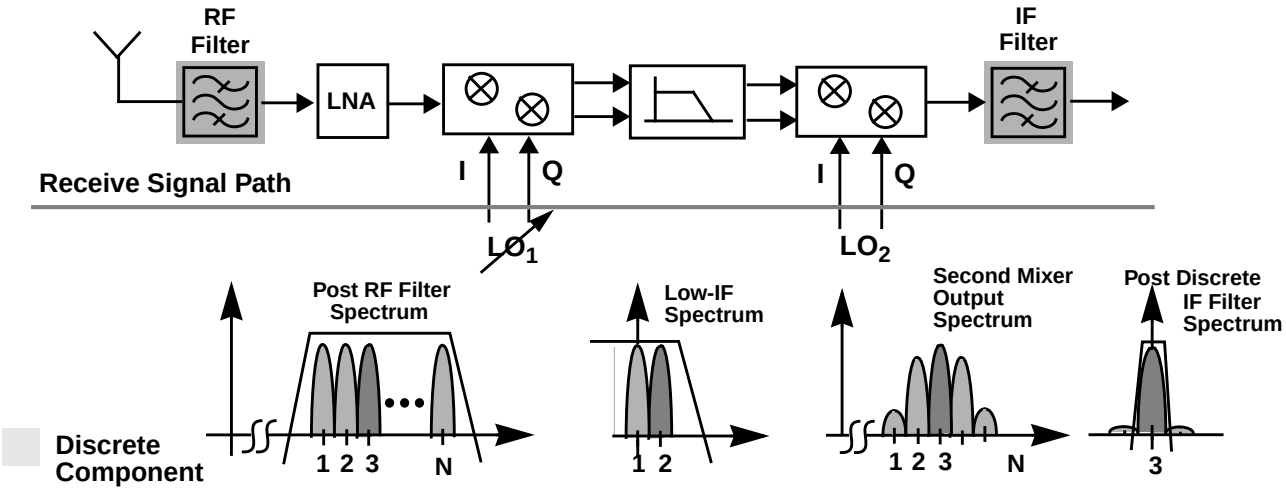

Figure 32. Conceptual diagram of a Double-Conversion Low-IF receiver.

Similar to a low-IF system, the close proximity of the image band implies that none of the image suppression will be provided by the RF filter. Thus all of the image attenuation in the double low-IF receiver must be provided by the weaver method,

again, limiting this architecture to standards with moderate adjacent and alternate channel blocking profiles.

The double low-IF receiver has the feature that it is more immune to DC offsets similar to the a low-IF system. Unlike a low-IF receiver, the entire band is up converted to a high IF were a very high-Q discrete filter may be used to remove adjacent and alternate channel energy. Assuming that enough image rejection is provided by the weaver method, the double low-IF system provides a reasonable amount of selectivity performance by virtue of the low pass filter at the first IF in conjunction with the discrete channel filter at the higher IF. Although this architecture requires an additional discrete filter, it provides a nice compromise between integration and selectivity performance. Depending on the required frequency response and characteristics, the discrete IF filter may not have a significant cost penalty. This was the case in [3.18], which used a very common and inexpensive 10.7-MHz-FM-discrete filter.

Similar to all of the previously integrated receiver systems discussed so far, the double low-IF receiver still requires an RF synthesizer. For narrow channel tuning applications with difficult phase noise requirements, this again, may be difficult to implement with a fully integrated VCO.

3.6 Sub-Sampling Receivers

Many of the proposed architectures which have been discussed so far utilize sampled data circuits to implement many of the baseband functionality including the channel filter as well as the analog-to-digital converter, this is particularly true of CMOS implementations. One proposed architecture cleverly uses some of the properties of sampling to implemented a good portion of the frontend receiver electronics using discrete-time circuits. Specifically, a sub-sampling architecture deliberately takes advantage of aliasing effects when sampling a continuous time signal. The sub-sampling receiver (figure 33) samples at a frequency which is a sub-harmonic of the

carrier frequency where $f_c=N \cdot f_s$, N being an integer while f_s and f_c are the sampling and carrier frequencies respectively. The need for a continuos time mixer and a synthesizer which operates at the carrier frequency has been obviated by a sampling circuit which aliases down in frequency the desired carrier. The sampling circuit given in [3.19] is actually the first stage of a switch-cap filter used to perform channel filtering and provide variable gain.

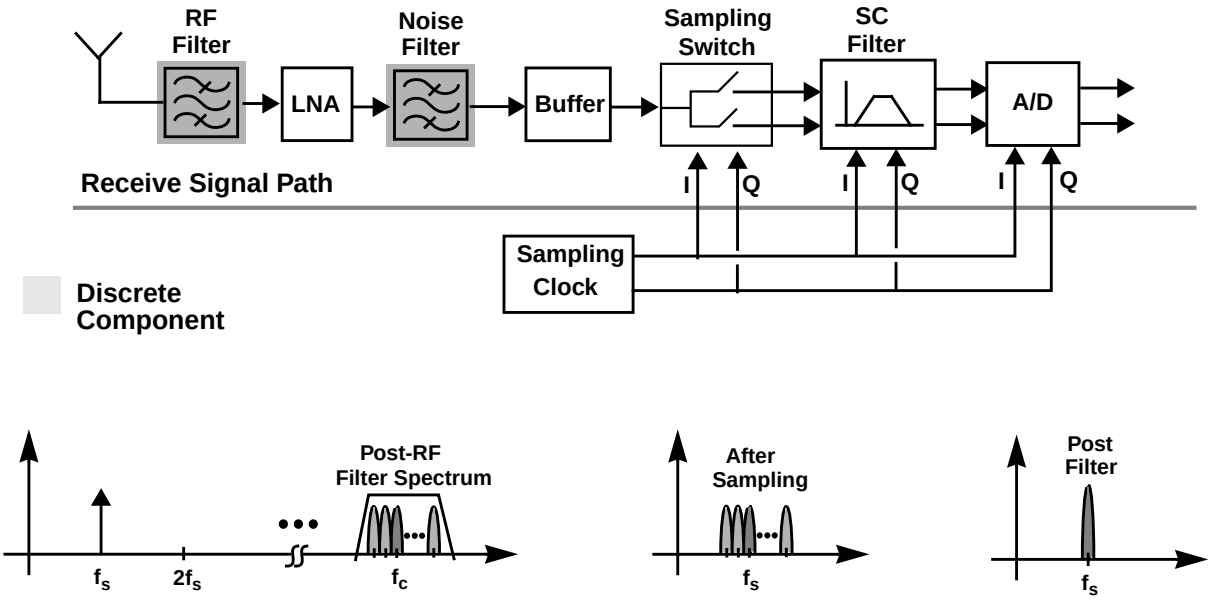

Figure 33. Sub-Sampling Receiver Architecture.

Although the sampling process associated with this architecture effectively down-converts the desired carrier, it should also be noted that energy at all of the other harmonics of f_s are also aliased into the desired signal band after sampling. This implies that a very high-Q filter, acting as an anti-alias filter, must be used before the signal is sampled to attenuate any unwanted energy and noise at the other harmonics of f_s. A filter with the needed attenuation characteristics is only practical as a discrete component and is shown as a noise filter in figure 33. The noise filter will almost invariably be followed by a buffer to drive the sampling switches. The white noise produced by the buffer and the kT/C noise from the sampling switch will still alias in

the desired signal band as the noise filter precedes the buffer and sampling circuitry. Thus, the reason sub-sampling receivers tend to be plagued by high noise figures.

There are several recently published examples of sub-sampling receivers which completely integrate all of the active front-end components in CMOS [3.19]. An additional sub-sampling systems which integrates the transceiver from the IF through the baseband is given in [3.20].

3.7 Wide-band IF with Double Conversion.

An alternative architecture well suited to integration of the entire receiver is wide-band IF with double conversion [3.21][3.22][3.23]. Shown in figure 34, this receiver system takes all of the potential channels (entire RF band) and frequency translates them from RF to IF, using a mixer with a coarse band tuning local oscillator. A simple low-pass filter is used at IF, to remove any up converted frequency components, allowing all channels to pass to the second stage of mixers. All of the channels at IF, are then frequency translated directly to baseband using a tunable, channel-select frequency synthesizer. Alternate channel energy is then removed with a baseband filtering network where variable gain may be provided. This approach is similar to a superheterodyne receiver architecture in that the frequency translation is accomplished in multiple steps. However, unlike a conventional superheterodyne receiver, the first local oscillator frequency translates all of the receive channels (the whole RF band), maintaining a large bandwidth signal at IF. The channel selection is then realized with the lower frequency channel-tunable second LO. As in the case of direct conversion, channel filtering can be performed at baseband, where digitally-

programmable filter implementations can potentially enable more multi-standard capable receiver features[3.36][3.37].

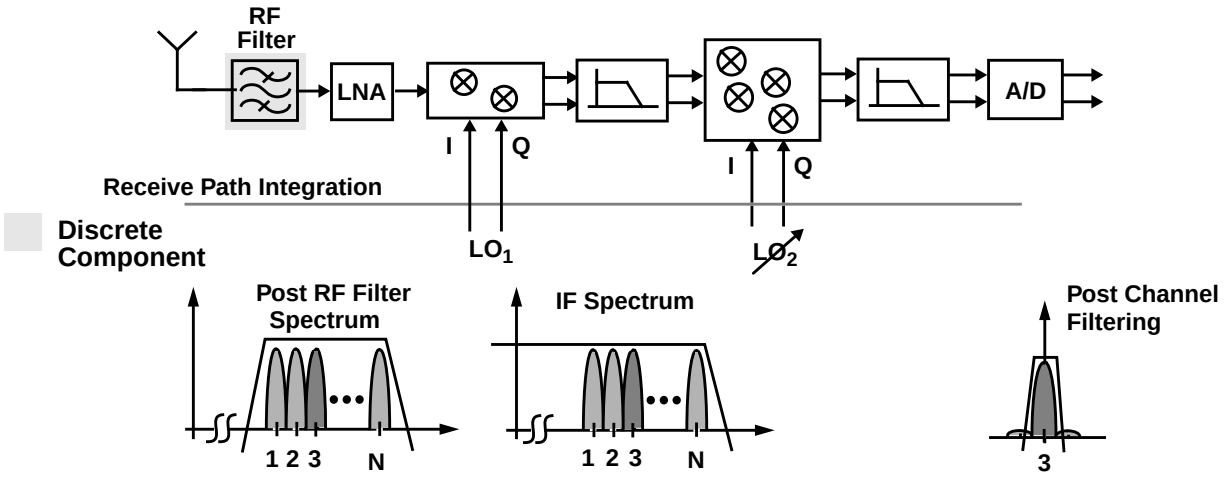

Figure 34. Conceptual operation of the Wide-band IF with Double Conversion receiver.

With a basic understanding of the wide-band IF front-end operation, some of the advantages as well as disadvantages of this architecture will be explored in depth. An extensive discussion of this architecture is provided, not because it exhibits some distinct breakthrough above and beyond the other high-integration receivers examined with respect to either facilitating integration or enabling multi-standard operation, but rather because there were some interesting features which were worth exploring and are the basis of the two prototype ICs which are reviewed in subsequent chapters of this thesis.

3.7.1 Synthesizer Integration

The wide-band IF architecture offers two potential advantages with respect to integrating the frequency synthesizer over a direct conversion approach. The primary benefit of this receiver system relates to the fact that the channel tuning is performed using the second lower-frequency, or IF local oscillator and not the first, or RF synthesizer. Consequently, the RF local oscillator can be implemented as a fixed-frequency crystal-controlled oscillator, and can be realized by several techniques which

allow the realization of low phase noise in the local oscillator output with low-Q on-chip components. One such approach is to implement the synthesizer with a wide loop bandwidth Phase-Locked Loop (PLL) which suppresses the VCO phase noise contribution near the carrier [3.25][3.26][3.27].

To better understand some of the VCO phase noise shaping properties which are capable in the wide-band IF receiver, a discussion on some of the properties of the PLL are now given. Although there are many possible implementations of a phase-locked loop that go beyond the scope of this thesis, some insight may be gained by looking at a 2^{nd} order phase-locked loop. Shown in figure 35(a), is a block diagram of a phase-locked loop utilizing an external discrete crystal which supplies a reference frequency f_R to the PLL. A phase detector (PD) is used to compared the phase of the reference frequency and a divided down version of the VCO output. The phase detector produces a voltage which is proportional to the difference in phase, between f_R and the divided down version of the PLL output frequency (also the VCO output frequency in this case). A loop filter is used to remove unwanted spurious tones produced by the phase detector as well as to ensure stability of the entire loop. The output resonant frequency is proportional to the control voltage supplied to the VCO from the Loop Filter (LF).

The thermal noise generated by each of the components in the PLL can be modeled as shown in figure 35(b). The noise from the phase detector, and the dividers is shown as "θ_1", while the noise contribution from the loop filter is "θ_2", and the noise injected from the VCO are shown as "θ_3". The transfer function from each of the noise sources to the output of the PLL can be derived and will be represented as $H_1(s)$, $H_2(s)$

and $H_3(s)$ for the transfer functions of the "θ_1", "θ_2", and "θ_3" respectively. A qualitative description of all the transfer functions is given in figure 35(c).

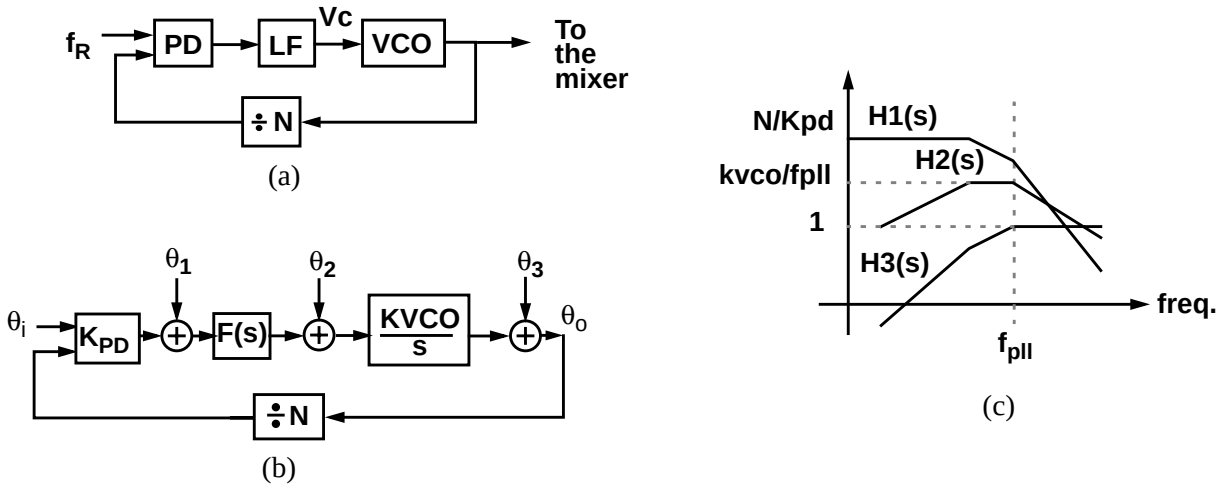

Figure 35. Concept of VCO phase noise shaping using a wideband width phase-locked loop (PLL). (a) Block diagram of a simple PLL (b) Various phase noise contributors, "θ_1" noise from the divider and phase detector, "θ_2" loop filter and "θ_3" VCO phase noise contribution. (c) Phase noise transfer functions from "θ_1", "θ_2" and "θ_3" to the output of the phase-locked loop.

A closer examination of the noise transfer function from noise injected in the VCO to the PLL output, $H_3(s)$, can be derived from the model given in figure 35(b) as,

$$\frac{\theta_o}{\theta_3} = H_3(s) = \frac{s^2}{s^2 + Ks + K\omega_2} \qquad \text{(Eq 3.1)}$$

Where the variable K represents the PLL loop bandwidth and ω_2 is a zero in the loop filter response F(s), which becomes part of a pole in both the overall PLL transfer function as well as the VCO phase noise transfer function. Fundamentally, in this simple example, the transfer function $H_3(s)$ has two zeros at the carrier frequency and a pair of poles further out from the carrier, this is illustrated in figure 35(c) for the transfer function of $H_3(s)$.

The output phase noise power spectral density produced by a stand-alone VCO, decreases as one moves away from the frequency of the carrier and is described in [3.28] as,

$$\Phi_{\theta_{VCO}}(f_m) = \frac{\Theta_o(f_m + f_a)(f_m^2 + f_b^2)f_c^2}{f_m^3(f_m^2 + f_c^2)} \quad \text{(Eq 3.2)}$$

Where f_m is the offset from the VCO resonant frequency f_o, or $f_m=f-f_o$. Θ_o is described by $\Theta_o = 2N_o/V_i^2$, $f_b=f_o/2Q$, where Q is the Q associated with resonant tank circuitry, V_i is the amplitude of the carrier in the VCO and N_o represents the thermal noise floor of the oscillator. The frequency f_a, relates to the 1/f noise corner associated with the oscillator. The phase noise power spectrum at the output of the PLL, due to noise injected by just the VCO can be described by,

$$\Phi_{\theta_o}(f) = \Phi_{\theta_{VCO}}(f)\left|H_3(j2\pi f)\right|^2 \quad \text{(Eq 3.3)}$$

Where $H_3(j2\pi f)$ is described by,

$$\left|H_3(j2\pi f)\right|^2 = \frac{(2\pi f)^4}{(2\pi f)^4 + (K^2 - 2K\omega_2)(2\pi f)^2 + K^2\omega_2^2} \quad \text{(Eq 3.4)}$$

A more detailed plot of $H_3(s)$, $\Phi_{\theta_{VCO}}(f)$ and $\Phi_{\theta_o}(f)$ is given figure 36. A couple of key observations may be made from this plot which have a profound implication on the wide-band IF architecture. Note, that the transfer function $H_3(s)$ has a high-pass frequency response relative to the carrier frequency. As mentioned before, the stand-alone VCO phase noise decreases when moving away from the carrier frequency. Overall, the shape of the PLL output phase noise contribution from the VCO can be found quantitatively by evaluating equation 3.3 with equation 3.4. Qualitatively, $\Phi_{\theta_o}(f)$ is shown in figure 36, note that the phase noise contribution increases starting from the carrier frequency and flattens out as the second pole of $H_3(s)$ has been reached, then begins to role off at the loop bandwidth frequency of the PLL. This is a significant point to observe as the amount of VCO phase noise *suppression* which can be obtained by the PLL close to the carrier, can be significantly increased by modifying the loop bandwidth.

Using the relationship observed between the VCO phase noise contribution and the PLL loop bandwidth, an opportunity for complete integration of the high-frequency PLL may be observed in the wide-band IF architecture. Typically, frequency synthesizers must realize a number of discrete frequencies and have a reference frequency applied to the phase detector which is equal to the step size in frequency between two of the desired synthesized frequencies. In a heterodyne receiver, the first synthesizer performs channel selection or tuning, thus, this

synthesizer must have a reference frequency equal to the channel spacing. For narrow-band cellular applications, this channel spacing and ultimately the reference frequency is typically on the order of 10s of kHz. An additional property of frequency synthesizers is that for both stability reasons and to reduce an inherent reference spurious tone produced by the phase detector (PD), the loop bandwidth must be anywhere from a fourth to a tenth of the reference frequency. For example, GSM uses 200 kHz channel spacing which implies that the loop bandwidth must be between 20 to 50 kHz. . This limitation on the loop bandwidth implies a boundary to the amount of VCO phase noise suppression which may be obtained from a narrow-channel-select frequency synthesizer. However, if the roles of the synthesizers are reversed compared to a superhet, as is done in the wide-band IF receiver, an opportunity to extend the PLL loop bandwidth is revealed. If now, as is done in the wide-band IF receiver, the first synthesizer purely performs band tuning between the bands of different standards, then the reference frequency associated with the first RF synthesizer may be significantly increased by as much as a couple orders of magnitude (from kHz to MHz). This implies then that the PLL loop bandwidth may also be increased by the same proportional amount (from kHz to MHz). This results in an increase of bandwidth, from the carrier, where close to carrier VCO phase noise shaping will occur, this concept is again illustrated in figure 36. Here, f_{pll} represents the loop bandwidth where $f_{pll}=K/2\pi$, and f'_{pll} represents an

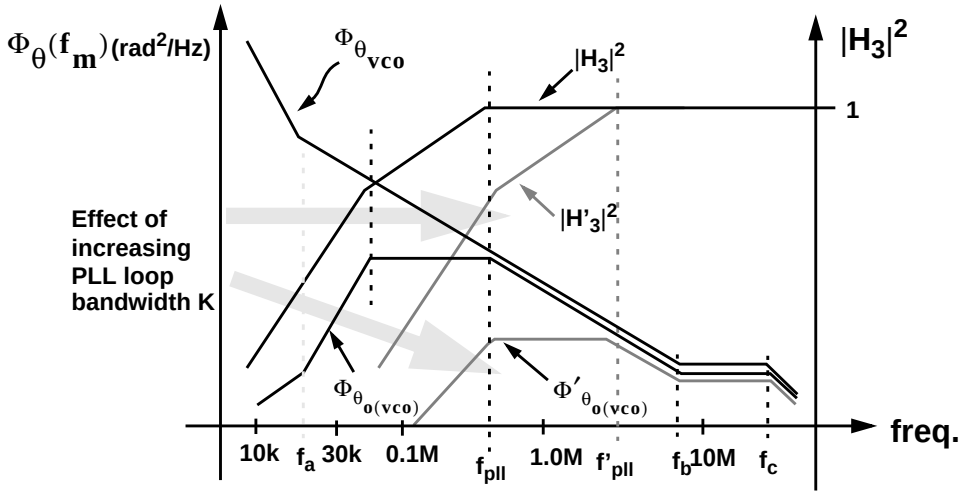

Figure 36. Effect of increasing the loop bandwidth K, on the PLL output phase contribution from the VCO.

identical PLL with a significantly increased loop bandwidth. It is also shown that the high-pass transfer function is broadbanded for the synthesizer where f'_{pll} is used. Also shown in this plot, is a hypothetical phase noise plot of a stand alone VCO represented as $\Phi_{\theta_{VCO}}(f)$. In the case of the PLL with the lower loop bandwidth f_{pll}, the synthesizer output phase noise contribution from the VCO is represented as $\Phi_{\theta_o}(f)$, while the case where loop bandwidth is increased to f'_{pll}, the VCO phase noise contribution is shown as $\Phi'_{\theta_o}(f)$. In the case of the PLL with the extended loop bandwidth, the suppression of VCO phase noise from the transfer function $H_3(s)$ is maintained further from carrier frequency.

Using the previous discussion on VCO phase noise suppression, the primary motivation for using the wide-band IF architecture can now be discussed. As was highlighted at the beginning of this chapter, current-day attempts at complete frequency synthesizer integration, with the entire receiver, have been limited to applications where low to moderate phase noise performance is acceptable. The poor phase noise performance of integrated synthesizers (particularly in standard CMOS) is attributed to the low-Q of on-chip spiral inductors which ultimately degrade the resonant tank Q. Again, because the first higher frequency synthesizer does not perform channel selection, but rather, is used for band selection, the reference frequency for the PLL can be increased by a couple orders of magnitude, allowing the same proportional increase in the loop bandwidth. In the case of the GSM/DECT prototype, discussed at the end of this thesis, the loop bandwidth was allowed to rise from approximately 2 kHz, if channel tuning were performed by the first high-frequency synthesizer, to 8MHz in the case where the first synthesizer is allowed to have an extended wide loop bandwidth, as was the case for the wideband IF GSM implementation. The implication for the wide-band IF receiver is that a wide-band PLL may be used to suppress the close-to-carrier phase noise of the VCO. Thus, relaxing the requirement on the resonant tank Q and facilitating the integration of both the VCO as well as the entire synthesizer with the rest of the receiver components.

With the first local oscillator relatively fixed in frequency, all of the channels are passed through IF, this leaves the burden of channel tuning to the second lower

frequency IF oscillator. Since the channel tuning is performed with the IF local oscillator, operating at a lower frequency, a reduction in the required divider ratio of the phase-locked loop operating at RF results. With a lower divider ratio inside the RF PLL loop, the contribution to the frequency synthesizer output phase noise from the reference oscillator, phase detector and divider circuits can be significantly reduced. Moreover, a lower divider ratio implies a reduction in spurious tones generated by the PLL [3.28].

From a more intuitive perspective, the phase noise performance of the lower frequency channel tuning synthesizer can be made inherently less than that compared to an RF channel-select synthesizer, where both are realized with low-Q, on-chip components. Assume for the moment that a synthesizer is realized which performs channel tuning at a high frequency. Then the output of the synthesizer is divided down in frequency by a divider block which is *external to the PLL* (see figure 37*)*; i.e. this is not the same divider which is a part of the PLL loop from the VCO output to the phase detector input. The integral in the frequency domain, of the power spectral density relates to the time domain RMS jitter. In short, the RMS jitter and phase noise performance are related; more phase noise implies a greater RMS jitter. Shown in the top part figure 37 is a hypothetical waveform representing the local oscillator output of a frequency synthesizer, the little shaded areas accompanying the edges represent are the RMS timing jitter associated with this waveform. Hypothetically speaking, if a noiseless divider block is used on the output of the PLL to divide the waveform shown in the top of figure 37, then the divider circuit will grab one of every N edges (where N is the divider ratio) along with the jitter associated with this edge; shown in figure 37 for N=4. Thus, the time domain jitter associated with the output waveform edges remains the same, however, the period of the divided signal has grown by a factor of 4 which can be thought of in the time domain as the desired signal increasing in power by a factor of four squared. Likewise, the same affect is observed in the frequency domain, the phase noise will be divided down by an amount proportional to the divider ratio, or

N^2. In reality, the divider circuit will contribute noise which degrades the jitter and phase noise performance. However, typically the synthesizer circuit components will dominant the noise and jitter performance, making the contribution to jitter and phase noise by the dividers negligible.

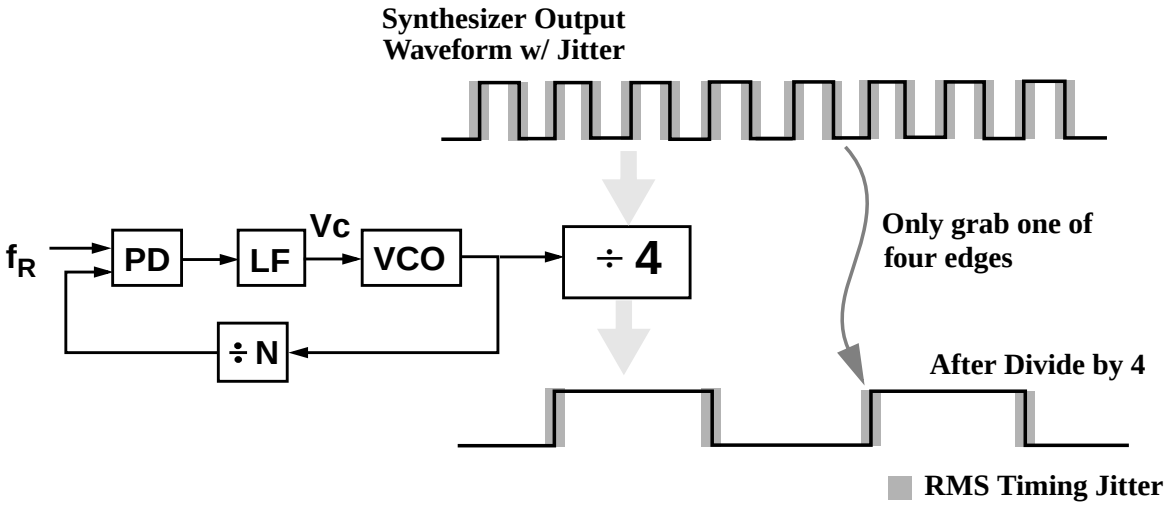

Figure 37. Jitter before and after an LO is divided down.

The high, fixed-frequency synthesizer which was used on the DECT/GSM chip was reported in [3.25] while a detailed description of the implementation can be found in [3.26]. A further discussion of the concept of VCO phase noise shaping can be found in [3.28] as well as another demonstrated PLL using these concepts is shown in [3.31]. While the discussion of band tuning high frequency synthesizes has been limited in this thesis, to phase-locked loops, it certainly does not mandate the use of these type synthesizers for block down convert architectures such as the wide-band IF receiver. An alternate approach to fixed-frequency synthesis uses a Delay-Locked Loop (DLL) and was presented in [3.29] with the implementation details given in [3.30]. An interesting feature of the DLL presented in [3.30], is that the phase noise profile remains flat close to the carrier, until the DLL's loop bandwidth has been reached. This is slightly different from similar results obtain from a PLL which has more of a high pass phase noise profile until the loop bandwidth has been reached.

The entire RF band is passed through the IF without channel filtering in the wide-band IF receiver, introducing the possibility of reciprocal mixing in both steps of the frequency conversion. Instead of having just one synthesizer which reciprocal mixes alternate channel blockers, there are now two mixer stages in the signal path. Thus, the accumulative interference which is generated by reciprocal mixing from the desired signal passing through both the first and second local oscillators in the wideband IF receiver, must be better than the desired signal band interference which is created by reciprocal mixing of just one set of mixers, as would be the case for any single frequency conversion architecture such as a direct conversion or low-IF receiver. Stated differently, the benefits of VCO phase noise shaping for both the first and second synthesizer in the wideband IF receiver, must produce at least 3dB better phase noise performance of each integrated synthesizer than those architectures using narrow loop bandwidth PLLs for tuning and down conversion.

3.7.2 DC Interference and Wide-band IF

An additional advantage associated with the wide-band IF architecture is that there are no local oscillators which operate at the same frequency, as the incoming RF carrier. This eliminates the potential for the LO re-transmission problem that plagues a direct conversion system and results in *time-varying* DC offsets. Although, the second local oscillator is at the same frequency of the IF carrier in the wide-band IF system, the offset which results at baseband, from LO self mixing is relatively constant and may be cancelled using one of the proposed methods described in [3.8][3.9].

Although, the potential for LO self mixing in the wide-band IF receiver is mitigated, there are other sources of offset which may be problematic for this architecture. Similar to direct conversion receivers, the carrier is ultimately frequency translated to baseband. Therefore, the desired signal is susceptible to 1/f noise, distortion due to 2^{nd} order intermodulation, and baseband circuit offset due to device

mismatch. In addition, like direct conversion, large adjacent channel AM blockers which are passed through the IF can potentially leak to the LO port of the mixer creating a DC offset at the output of the second set of mixers (LO2), which again, falls in the desired signal band.

3.7.3 Image-Rejection in the Wide-band IF system.

In the wide-band IF receiver, the signal is mixed to a finite IF; therefore, the image problem is re-introduced in this system. However, because the two frequency translations occur in cascade, the architecture used lends itself to easy implementation of an image-reject function using a six mixer configuration. The mixer configuration which is shown in figure 38, completes the two step down conversion by first multiplying the LNA output signal with mixers which utilize quadrature phases of the local oscillator. The second downconversion to baseband, from IF, is accomplished by using the so-called double quadrature mixer configuration. Not shown in figure 38, is a low-pass filter which provides some attenuation of the up converted terms resulting from the first down conversion.

The comprehensive configuration used to perform the frequency conversion from RF to baseband in the wide-band IF architecture, can be thought of as two independent sets of image-rejection mixers which resembles the Weaver technique original proposed in 1956 [3.32]. To understand both the function of this image-rejection mixer, as well as some of the beneficial properties it is best to start with a frequency domain interpretation of this single-sideband mixer. Shown in figure 38, at the input of the mixer configuration, is a hypothetical LNA output spectrum with both positive and negative frequencies displayed. For this example, bands 1 and 4 represent the signal above the frequency of the first local oscillator which is desired to eventual recover, while bands 2 and 3 are the undesired image-bands shown equally spaced in frequency, below the first local oscillator. The RF spectrum applied to the input of this

mixer is first multiplied by in-phase and quadrature local oscillators and converted to IF. The spectrum at IF, is the result of a convolution in the frequency domain, of the RF carrier with both a sine and cosine. At IF, there exists a known phase relationship between the image and desired frequency bands. This phase relationship is further exploited with a complex mixing from IF to baseband. If the up converted terms from the mixer are removed by low pass filtering at IF and baseband, then by properly adding the four baseband channels in pairs, the image frequencies can be made to cancel while the desired band adds constructively for both the I and Q channels. This image-rejection mixer has the property that any incoming frequency below the frequency of the first local oscillator, ideally is rejected, while any frequency above the first LO, is passed. If the IF is made high enough, additional image rejection may be obtained from the RF front-end filter.

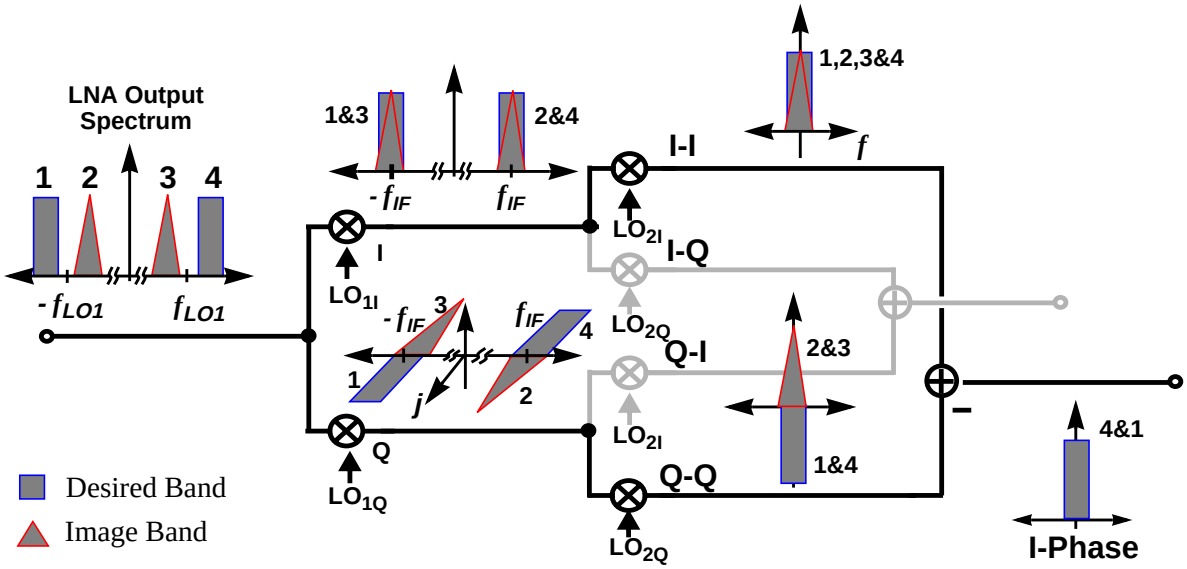

Figure 38. Frequency domain interpretation of a Weaver image-rejection mixer.

This particular image-rejection mixer topology has several advantages. First, unlike the Hartley method[3.33] or other proposed image-rejection mixers [3.12][3.35], lossy passive phase-shifting filters are not required in the receive signal path, to generate the correct phase between the image and desired bands. Second, assuming again that the up converted terms are removed, the image-rejection is very wide-band. It

can be further shown that the edge of the image-attenuation band is set by the frequency of the first local oscillator (LO1), which leads to the third advantage. If it is assumed that a multi-standard capable receiver is built where the frequency of LO1 can perform a coarse adjustment to accommodate the carrier frequency of a different standard, then the image rejection will follow the first LO, or the image rejection can be thought of as self-aligning to the frequency of LO1. To illustrate this concept, two hypothetical LO1 frequencies, labelled f_{LO1a}, and f_{LO1b} necessary to properly frequency translate the carrier of two different standards are shown in figure 39(a) & (b). Both the passband and the rejection band as a function of the frequency referenced to the input of the mixer, are aligned to LO1. Assuming that the desired band is above LO1 in frequency, the image-rejection will be self aligned with the frequency of LO1 setting the boundary between the pass and stop bands of the mixer. Further flexibility using this mixer configuration may be obtained by reversing the polarity of the four baseband channels before they are summed together at the mixer output. This has the affect of retaining the lower sideband about LO1, while rejecting the upper sideband. This concept is

illustrated in figure 39(c) and was first introduced in [3.22] and later demonstrated in [3.34].

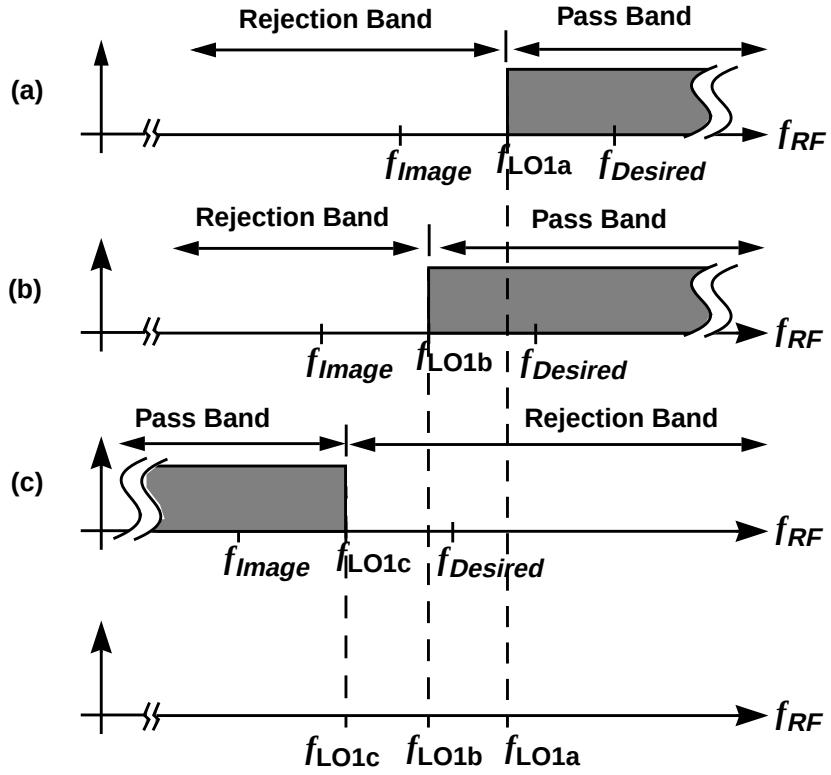

Figure 39. Self-Aligning Image-Rejection Mixer.(a) f_{LO1a}, and f_{LO1b}, two different LO1 frequencies and their relationship to the rejection and pass band of the image-rejection mixer.(c) f_{LO1c} case when the polarity of the baseband channels are reversed before the summation.

3.7.4 Non-idealities of Wide-Band IF

Although the wide-band IF system has advantages with respect to high integration, certain non-idealities limit the overall receiver performance. These are now discussed.

Because the first local oscillator is fixed in frequency, all of the channels must pass through the IF stage and the desired channel is selected with the second LO. This has two problematic implications. First, as a result of moving the channel tuning to a lower frequency, the IF synthesizers require a VCO with the capability of tuning across

a broader frequency range as a percentage of the nominal operating frequency. Second, as mentioned previously, by removing the channel select filter at IF, strong adjacent channel interferers are now a concern for the second mixer stage as well as the baseband blocks. This implies a higher dynamic range requirement of these latter receiver stages. In addition, spurious tones generated by the IF local oscillator can mix with undesired IF channels creating inband interference at the output of the second mixer stage. Additional care must be taken when developing a frequency plan to guard against digital baseband clock signals and their harmonics falling within the range of the desired IF channels.

As with virtually any single-sideband mixer which utilize a phase shifting scheme to reject a sideband or image, the magnitude of the image attenuation in the wide-band IF architecture, is a function of the phase mismatch between both the I and Q phase of the first and second local oscillators, and the gain matching between the signal paths. A detailed derivation for the image-rejection performance as a function of phase and gain mismatch is given in appendix A. The image rejection as a function of the mismatch is given by,

$$\mathrm{IRR(dB)} = 10 \cdot \log\left[\frac{1 + (1+\Delta A)^2 + 2(1+\Delta A)\cos(\phi_{\varepsilon 1} + \phi_{\varepsilon 2})}{1 + (1+\Delta A)^2 - 2(1+\Delta A)\cos(\phi_{\varepsilon 1} - \phi_{\varepsilon 2})}\right] \qquad \text{(Eq 3.5)}$$

Where $\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$ represent the deviation of the local oscillators from quadrature in the first and second LOs, respectively, while ΔA is the aggregate gain error along the I and Q signal paths. A plot of equation 3.5 is given in chapter 4, figure 50. With a sufficiently high intermediate frequency, the image-rejection may be performed with a combination of the RF front-end filter and this image-rejection mixer. Using this approach, 35dB of image-rejection can easily be obtained from the six mixer configuration.

3.8 General Comments on Receiver Architecture Selection

This chapter was presented to highlight some of the issues and challenges with respect to full receiver integration. The superheterodyne receiver was presented and contrasted to some recently proposed receiver architectures which attempt to integrated all of the components on to a single piece of silicon.

With regard to high integration radios, the choice of which architecture to use is of course, in large part, dependent on the application or required performance. Obviously, the easiest approach which is suitable for any application should be used, in most cases this is a direct conversion receiver. Moderate performance receivers are typically characterized by less aggressive selectivity and sensitivity performance. Examples might include cordless telephone, and indoor wireless LAN standards. For these applications, the cell sizes tend be rather small. Thus, reducing the possible variation in both, the desired and undesired received signal power, which relaxes the selectivity and sensitivity performance required of the receiver. For these applications, often times both direct conversion and low-IF receivers present a convenient solution for a high-integration radio.

For higher performance standards which require excellent sensitivity as well as selectivity performance, other high integration architectures may be more appropriate. In the situation where the mobile wanders far from the basestation, a large potential variation in both, the desired and undesired signal strength may occur, this is the case for most cellular standards. This translates to high performance with respect to sensitivity, selectivity as well as overall dynamic range in the signal path. Direct conversion receivers have been demonstrated for some cellular applications, such as GSM. However, while these solutions provide high integration in the signal path, the synthesizers still utilize discrete components for the tank circuitry. The Wideband IF receiver was developed to facilitate synthesizer integration, with the tank components for applications where both high selectivity performance as well as very narrow channel

spacings are required. This is often the case for narrow band cellular standards such as GSM, IS-54, and AMPS. The Double Low-IF architecture was presented as a nice compromise between receive signal path integration and selectivity performance.

Much research is still needed with respect to enabling a single chip solution which is capable of addressing multiple standards and applications. From an architectural perspective, the best hope lies with systems where the signal path may be re-used, rather than duplicated, between multiple applications/standards. In the receive signal path, this typically implies keeping the signal wideband at high frequency and performing the filtering at a very low-IF, or baseband, where integrated programmable filter structures may be implemented in either the analog or digital domain. In addition, the synthesizer must be capable of tuning to various channel spacings as well as have the ability to tune across vast portions of the spectrum to address different bands associated with the desired standards to recover. Some properties associated with programmable receive signal paths were exhibited in both the direct conversion and wideband IF architectures.

With the introduction of the wideband IF receiver, the following chapters found in this thesis will focus more on the issues associated with implementing the architecture in silicon, particularly CMOS. The emphasis will be on the components required to perform the frequency translation, mainly the mixers. The next chapter looks at various methods of performing image rejection for integrated heterodyne receivers. This is then followed with a chapter which describes a method to remove one of the non-idealities of the wideband IF receiver. Mainly, a method is presented to tune out the phase and gain mismatch in the image-rejection mixer which ultimately improves the sideband suppression. The later chapters are presented to give more specific circuit implementation details for all the blocks which realize the image-rejection mixer used by the wideband IF receiver. A recently published transmitter using the Wide-Band IF architecture has been published in [3.38].

3.9 References

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Chapter 4

Image-Rejection Mixers

4.1 Introduction

Chapter 2 was presented as an overview to some of the issues associated with receiver integration while chapter 3 reviewed a few recently proposed high integration receiver architectures. This chapter will focus on one particular problem associated with receiver integration, mainly image rejection. Virtually all receiver architectures, with the exception of direct conversion, must provide some means of suppressing undesired interference which is frequency translated to the same IF as the desired signal. This chapter will first begins with a description of the image problem. This is then followed with a review of some commonly used techniques to perform either filtering or cancellation of the image-band signals. The image-rejection mixer used by the wideband IF receiver is then described in more detail, with an analysis of the sideband suppression as a function of the phase and gain mismatch in the signal path, along with a noise analysis of this mixer system.

4.2 The Receiver Image-Band Problem

A more mathematical description of the frequency translation process using mixers is given in chapter 6. The process by which an image band interferer is

frequency translated into the same frequency as the desired band, can best be understood with a simple model for a mixer shown in figure 40. In this example, if a tone is applied to both the RF and LO ports, then the output is simply the result of the product of these two sine waves.

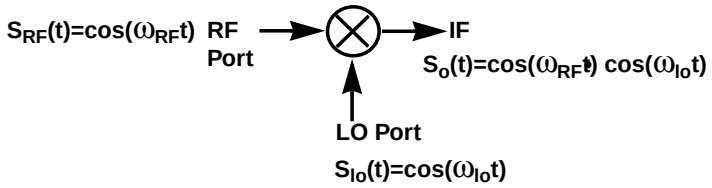

Figure 40. Simplified model of a single mixer.

Using trigonometric identities, the mixer output signal (shown in figure 40) can be expanded to reveal the frequency components associated with the output of the mixers/multipliers are,

$$S_o(t) = \cos(\omega_{RF}t)\cdot\cos(\omega_{lo}t) = \frac{1}{2}[\cos((\omega_{RF}-\omega_{lo})t) + \cos((\omega_{RF}+\omega_{lo})t)] \quad \text{(Eq 4.1)}$$

From equation 4.1, it can be seen that the mixer output signal contains a component of mixer input signal which is down converted in frequency by $(\omega_{RF}-\omega_{lo})$, while another component is upconverted in frequency by $(\omega_{RF}+\omega_{lo})$. The down converted term is usually used by radio receivers, while the up converted term is typically a desired component in the transmitter applications. In either the transmit or receive path, the resulting output spectrum is referred to as the intermediate frequency or IF. Focusing in on the down converted component $(\omega_{RF}-\omega_{lo})$, there exists two bands which can potentially be shifted to the same intermediate frequency. Imagine for the moment, that there exists two spectral components one of which resides at $\omega_{RF} = \omega_{lo}+\omega_{IF}$ and the other $\omega_{RF} = \omega_{lo}-\omega_{IF}$, both at the RF port of the mixer. From equation 4.1, one can see that both of these input spectral components will frequency translate to the same intermediate frequency at the output of the mixer, this is illustrated in figure 41. If the desired band to translate is above the frequency of the first local oscillator, ω_{lo}, then the other band which is frequency translated to the same IF, is referred to as the image frequency or image

band. It is clear to see that without proper filtering or cancellation of the signals present in the image band, this signal will appear as interference to the desired band at the output of the first mixer. The situation may arise where the desired signal in receiver applications is much weaker than undesired interferers found within the image band. Thus, a significant amount of image-suppression must be guaranteed for most receiver

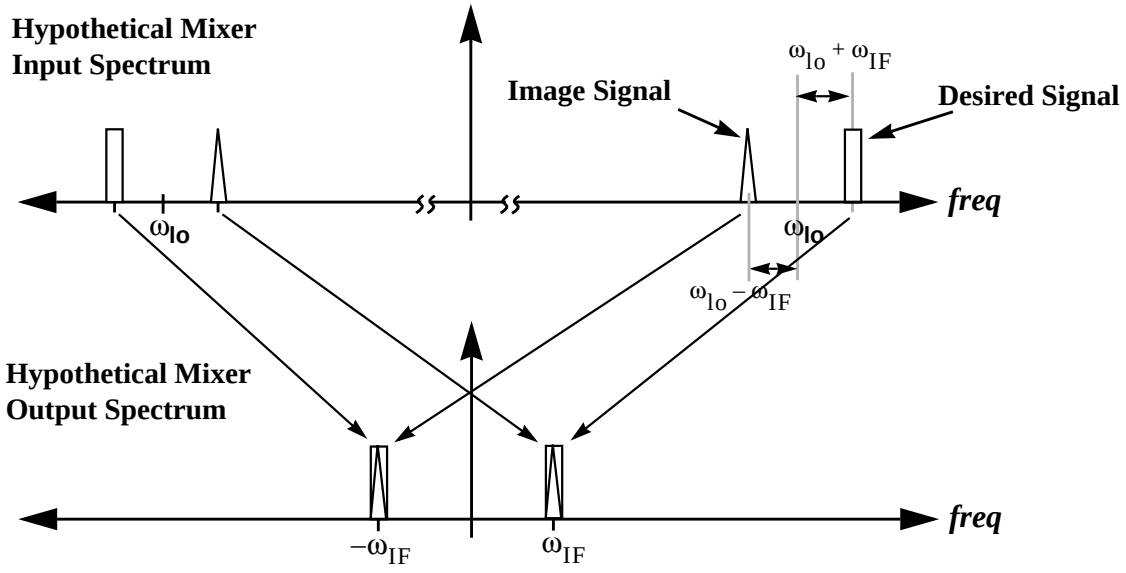

Figure 41. Hypothetical input and output spectrum of a single mixer. Frequency translation is shown for both the desired upper sideband of the mixer as well as the equivalent image band.

applications.

The amount of required image attenuation which is needed can usually be derived by either a system specification or a blocking profile which is outlined by a radio standards body. With a knowledge of both the blocking profile, the desired mixer output Carrier-to-Interference (C/I) ratio, as well as an assignment of the intermediate frequency and the minimum desired signal strength, the amount of required image attenuation may be determined. Using the blocking profiles for both GSM and DECT which were highlighted in chapter 2, along with the required sensitivity under the blocking condition, the image rejection for both the receivers used in the DECT as well as DCS1800/DECT receivers were determined with a 200MHz and 400MHz IF

respectively. The required image suppression for both GSM and DECT are summarized in Table 1.

Table 1: Summary of image rejection requirements for both DECT and DCS 1800.

Receiver Mode	IF	Maximum Required Blocking Sensitivity	Required C/I	Worst Case Image	Required Image Rejection
DCS 1800	400 MHz	-97 dBm	~ 12 dB	0 dBm	~ 110 dB
DCS 1800	200 MHz	-97 dBm	~12 dB	0 dBm	~ 110 dB
DECT	400 MHz	-73 dBm	~ 10dB	-23 dBm	~ 60 dB
DECT	200 MHz	-73 dBm	~ 10dB	-23 dBm	~ 60 dB

4.3 Methods for Receiver Image Attenuation

For virtually all receiver applications which utilize a heterodyne architecture, the image problem is addressed using one of two basic approaches; mainly, filtering or some method of image band cancellation using a serious of phase shifts between two parallel signal paths. As was discussed in the previous chapter, the super-heterodyne receiver typically accomplishes all of the image attenuation for the first down-conversion with a combination of discrete filters. Specifically, image attenuation is accomplished with both the RF and the noise/image-rejection filter which are placed both before and after the LNA. Both the RF and image-rejection filters will have anywhere from 30 to 50dB of image suppression depending on the quality of the filter and the selection of the IF frequency. Obviously, the further away from the RF carrier the imageband lies, the more attenuation of image signals may be accomplished by these filters and the easier the image problem is to address. In addition, the cost of these filters tends to be inversely proportional to both the insertion loss of the filter and proportional to the number of poles required.

Some recent research has focused on implementing the image-rejection filter as an integrated solution. One such approach attempts to utilize Micro-Electro-

Mechanical structures (MEMs) to implement the RF and image-rejection filter[4.1]. These devices are processed on the same die as the radio electronics. Although, these structures hold promise of delivering high-Q filters as an integrated solution, there are a few drawbacks to this approach. First, these filters would required a special silicon technology which tends to be more expense than main stream silicon processing such as is found with CMOS and BiPolar silicon processes. In addition, these filters suffer from other practical issues which need to be resolved to make them commercially viable. These problems included the use of a vacuum chamber to realize these filters as well as issues with respect to component tolerances, the required use of high operating voltages, as well as issues with respect to rather large input and output impedances which appear to be inherent to these structures. There have been additional attempts to address the image-band signal using a notch filter which use on-chip spiral inductors to realize an LC based filter [4.2]. The fundamental drawback to this approach, is that the notch is relatively narrowband and susceptible to component variation, making the band of image attenuation both narrow and dependent on process variation. A cleaver technique to alleviate the narrowband nature of the notch filter is through the use of a phase-locked loop in conjunction with an LC based filter where the capacitor is realized with a varactor diode. Using the control voltage from the PLL, the capacitor is tuned with the varactor diode, thus adjusting the frequency at which the notch appears[4.3][4.4][4.5]. This method of image rejection using a tunable notch filter has some shown promise for moderate image rejection with extremely low power consumption. The fundamental drawback to this approach, as with many of the integrated image rejection methods, is again the component mismatch between the varactor diode used in the PLL VCO tank and the LC filter will limit the accuracy in frequency of the notch and ultimately the amount of reliable image rejection at any given frequency.

The alternative approach to image-rejection filtering is the use of a cancellation scheme to perform image or sideband suppression. This is usually

accomplished through the use of a combination of a set of quadrature phase mixers, phase shifting filters and/or asymmetric polyphase filters. Although the name image-rejection mixer implies a single mixer, this class of device is virtually always realized through the use of several mixers which in some configurations also utilize a phase shifting filter. The basic principle of this class of mixer is to generate two channels within the receive path. Then, between the two signal paths through a combination of complex mixing and phase shift filtering, the signal at the image frequency, is rotated in phase, in such a manner, that a 180^{o} phase difference exists between the two signal paths. Although the image single has ideally an exact opposite phase difference between the two signal paths, image rejection mixers are made to create a zero phase difference between the desired signal band, found in the two channels. Thus, by simply adding the two channels together, the image band signals ideally cancel while the desired signal adds coherently. The process of creating the correct phase between image signals found between two channels is discussed with more detail in the next section followed with a few examples.

4.4 Image-Rejection Mixers

Several popular image-rejection mixers create the correct phase between the desired band and image signals by performing a complex multiplication. This is nothing more than multiplying the desired carrier using two mixers that have local oscillators which are in quadrature phase (90^{o} phase difference) applied to the mixer LO inputs. Much intuition can be gain about what is happening in the signal path, by applying a set of tones to the quadrature inputs of the mixer. This situation is illustrated in figure 42, where two sinewave inputs are applied, one of which lies above the frequency of the first local oscillator, which for the purposes of illustration will represent a desired signal, while the other sinewave at the input, resides an equal distance from the LO on the lower side of the local oscillator. If these input signals are multiplied by an in-phase and quadrature local oscillators, the signals which are shown in figure 42, will appear at

the IF output, where the upconverted terms are ignored and assumed to be removed by lowpass filtering at the output of the mixer. Between the I and Q channels at IF, the image signal has a 90^o phase difference while the desired signal has the opposite 90^o phase shift between the I and Q channels.

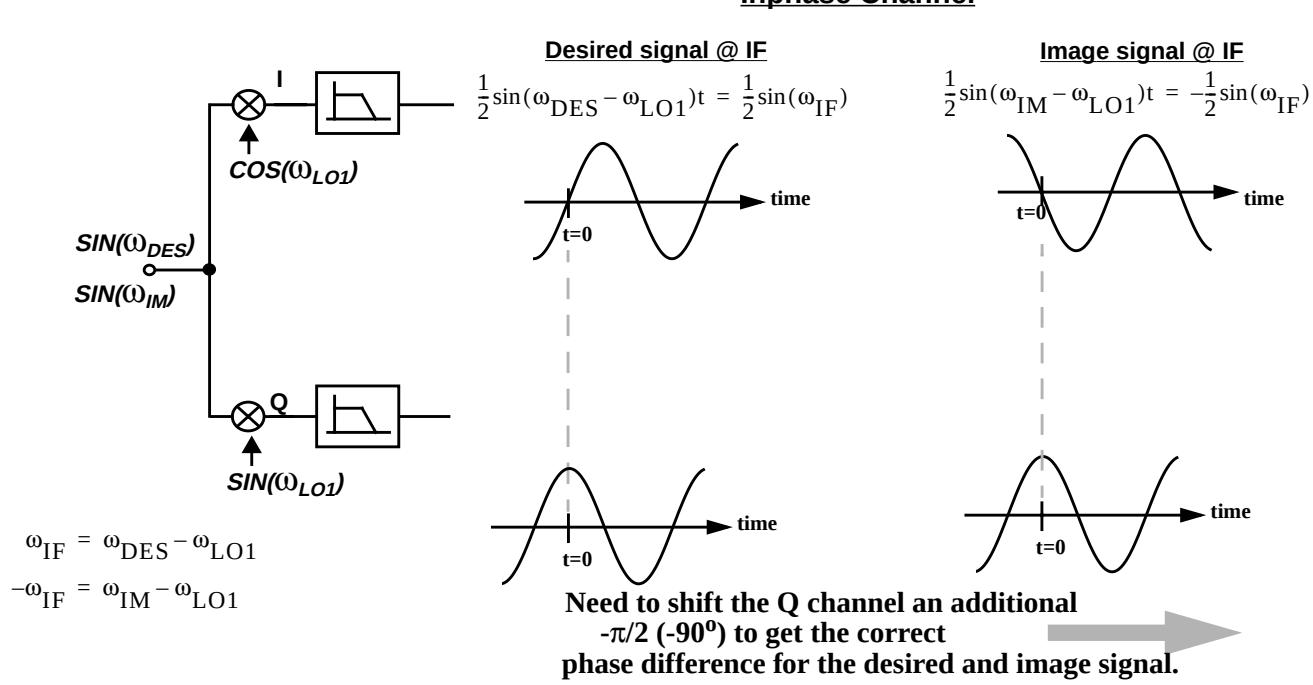

Figure 42. Result of mixing a pair of tones both above and below the frequency of the first local oscillator (LO1). The upconverted terms are ignored for simplicity. The desired signal has a 90^o phase difference between the I and Q channel while the undesired image

The difference in the phase relationship between the desired and image signals really relates to taking advantage of the odd and even properties which arise from multiplying the input signal by a local oscillator which is represented by a sine and cosine. This again is better understood by examining figure 42, where the input signal is frequency translated to an IF which is represented as $\omega_{IF} = \omega_{DES} - \omega_{LO1}$ for the desired signal, and $-\omega_{IF} = \omega_{IM} - \omega_{LO1}$ for the image signal, at IF. Because of the even property of a cosine, the phase of the signal in the quadrature channel (Q channel) will always be the same independent of whether the input signal is above or below the frequency of the first local oscillator (see figure 42). However, in the I channel, the phase of the resulting signal at IF, is dependent on whether the input signal was received above or below the

frequency of the first local oscillator. Using the relationship that sin(-x)=-sin(x), one can see that the phase of the signal at IF, in the I channel, will rotate by 180^o dependent on whether the input signal is in the upper, or lower sideband, of the local oscillator. The overall affect on the phase of the signal, when performing a complex multiplication is similar in concept, to a Hilbert transform about the frequency of the local oscillator (however, this is not a Hilbert transform as the system is non-linear). The key observation to make, which is also the basis of most image-rejection mixers, is that by shifting the phase of the Q channel IF, by an additional -90^o relative to the I channel, the desired signal will have the same phase between the two channels, while the image tone will be 180^o out of phase. Thus, in this situation, by simply combining the two channels, the desired signal adds coherently, while the image signal cancels. Ideally, in the case where a perfect 90^o phase shift is added to the signal at IF, the mixer configuration can be made to pass any signal above the frequency of the oscillator while rejecting anything below, thus giving rise to the often used name of single-sideband mixer. It is this observation which really sets the foundation for many of the single-sideband and image-rejection mixers which have been proposed, and used to date.

One approach to adding the additional $-\pi/2$ phase shift at IF, is to simply add a 90^o phase shift filter as shown in figure 43. This particular image-rejection mixer was originally proposed in 1925, with a patent by Hartley [4.6]. In the Hartley method, the additional phase shift can be implemented with a set of resistors and capacitors to implement a pole and a zero which will give a 90^o phase difference at the 3dB frequency. This approach is amenable to integration in silicon, with on-chip resistors and capacitors. The filters can be implemented with either an all-pass response, with the phase difference being 90^o only at the 3dB frequency, or the filter can be configured as a broadband 90^o phase difference, where the amplitudes only match at the 3dB frequency. A detailed discussion on the implementation of the phase shifting filters may be found in chapter 7. In the Hartley approach to image rejection, the magnitude of the sideband suppression is dependent on how far away the IF signal is from the 3dB

frequency of the phase shifting filter. Therefore, with a single set of poles and zeros to implement the phase shifting filter, the frequency range of image suppression becomes narrowband. To broad band the image rejection, additional poles and zeros need to be added to the phase shifting filter. This is usually done at the expense of attenuating the magnitude of the desired signal, resulting in either a weak noise performance and/or large power consumption.

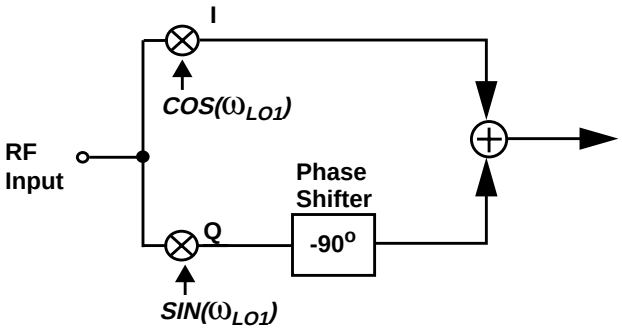

Figure 43. Hartley Image-Rejection Mixer

More than 30 years after the Hartley patent, Donald Weaver published another method to achieving the additional 90^o phase shift after the first complex mixing operation. The Weaver method, which was published in 1956 [4.7], achieves the correct phase by adding an additional complex mixing stage to the configuration shown figure 42. When two complex mixing operations are put in cascade, the input signal can be made to go through two frequency translations as well as generate a 180^o phase shift between the image signals before addition and cancellation. A block diagram of the Weaver mixer is shown in figure 44, with again two tones one above and below the frequency of the first local oscillator. One can see that, as the first IF is frequency translated a second time by quadrature mixers, the correct phase for the image and desired signal is achieved before the two channels are added together. This is shown in figure 44 for a set of tones one in the imageband (shown as a $\sin(\omega_{IM})$), while the other

resides an equal distance above the frequency of the first LO in the desired signal band (represented by $\sin(\omega_{DES})$).

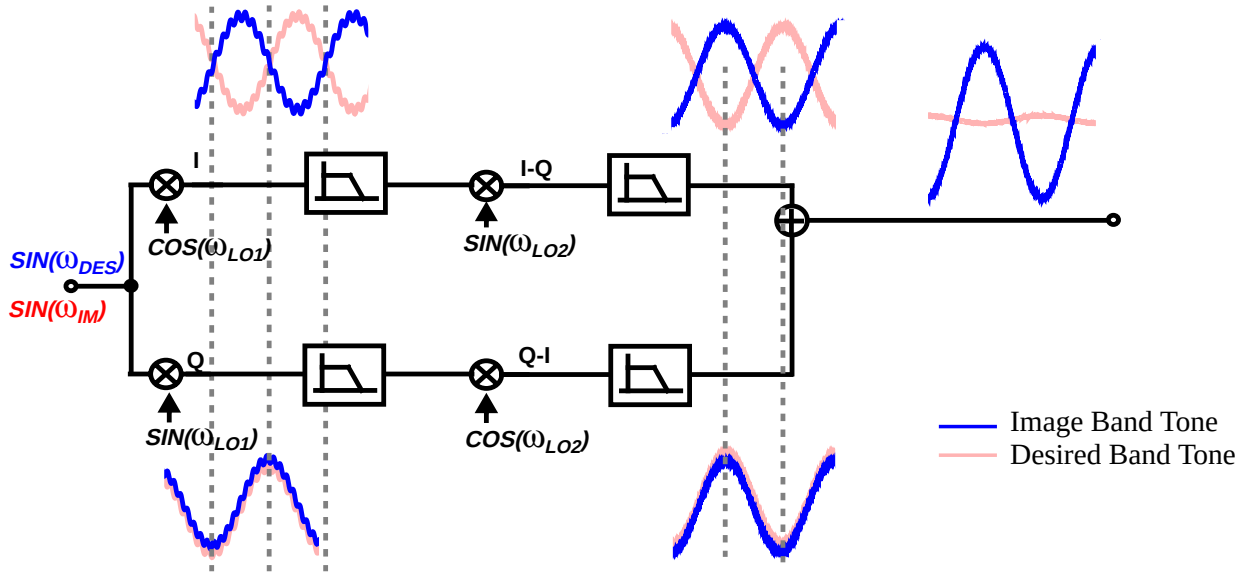

Figure 44. Time domain interpretation of the Weaver Method.

As alluded to and described in the previous chapter, the weaver method has some interesting properties with respect to the way frequency translation is performed. In essences, the edge of the rejection band is defined by the frequency of the first local oscillator. As mentioned earlier, this has some practical implications from the perspective of providing flexibility for band selection of multiple RF standards. Because the Weaver mixer is single sidebanded about the frequency of the first local oscillator, when tuning the LO1 frequency to another band of a different standard, the image-rejection will effectively by self aligned as described in chapter 3. Also, further flexibility is provided by inverting the summation of the two channels at baseband. This has the affect of sideband reversal, leaving the possibility of down converting the lower sideband about LO1 rather than the higher sideband; the sideband which is rejected would in this case, now be the high sideband about LO1.

In the next section, a discussion is given about how the weaver method was applied to the wideband IF receiver. This is followed with an estimation of the input

referred noise produced by this image-rejection mixer as a function of noise contribution from the four individual mixers used in the signal path of the weaver method. This is followed with a analysis as well as a discussion of the phase and gain mismatch of this image-rejection mixer as well as some other non-idealities of the weaver method as it applies to the special case when used in the wideband IF receiver.

4.5 Image-Rejection in the Wideband IF receiver.

A description of the frequency translation section used by the Wideband IF receiver was given in chapter 3. In short, the prototype receivers which will be discussed later essentially utilized a pair of Weaver image-rejection mixers to perform a two-step frequency conversion from RF to baseband. The comprehensive configuration (shown in figure 45), utilized six mixers which generates quadrature channels at baseband in addition to providing an image reject function. The subsequent sections of this chapter will discuss some of the non-idealities of this mixer configuration, mainly the noise performance and the affect on image rejection from phase and gain mismatch between the various signal paths.

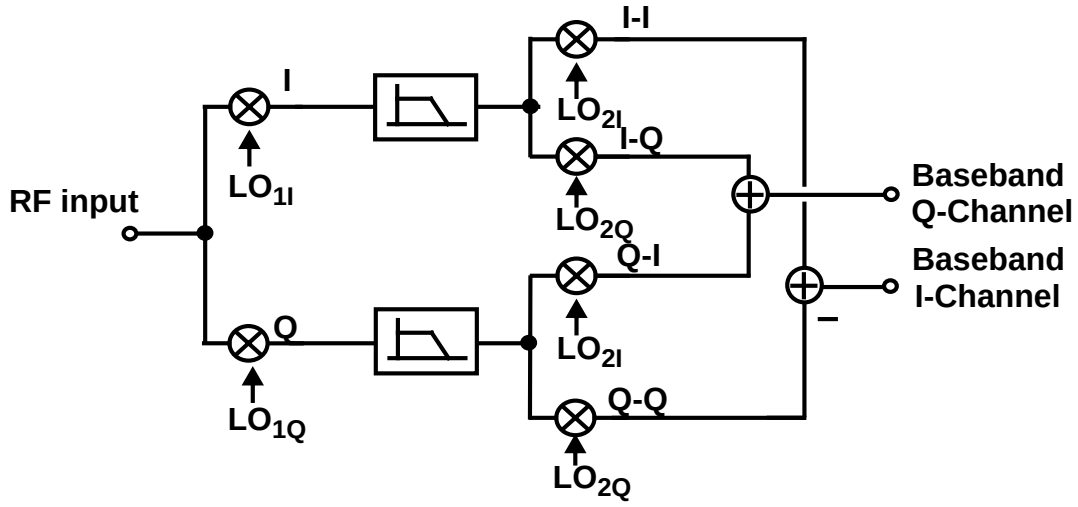

Figure 45. Block diagram of the frequency translation section used by the wideband IF receiver.

4.6 Noise Analysis for the Weaver Method

A noise analysis for the Weaver method was carried out to evaluate the additive noise to the channel and the overall impact on the receiver noise figure from the noise contribution of the mixer. The system specification for all of the receiver was written with respect to an equivalent input noise resistance on each component. This is a convenient measure of a receiver components noise performance as it can be quickly referred to the receiver input and compared to the available noise power generated by the source resistance. Therefore, this section provides a method of estimating the equivalent input noise resistance of one image-rejection mixer as a function of each of the four individual mixer cell's gain and noise resistance.

Four mixers are required to produce a single channel at baseband. Developing a specification for the individual mixers inside the four mixer configuration requires a little understanding of how the noise and signal pass through the mixers. Shown in figure 46, is the four mixer configuration used to produce one channel at baseband. The individual mixers are specified with respect to the voltage conversion gain, the equivalent input noise resistance and maximum output swing of one of the four individual mixer cells. A bit of analysis is required to translated the conversion gain and noise performance of an individual mixer cell to that of the gain and noise performance for the composite image-rejection mixer configuration.

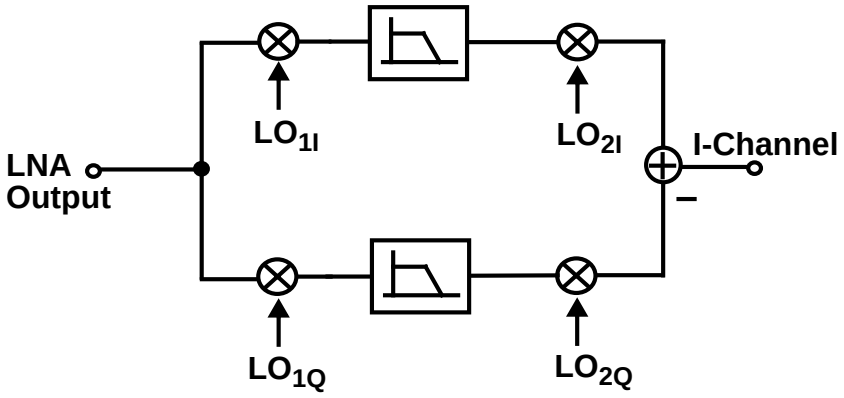

Figure 46. Single channel IR-Mixer used by the wideband IF receiver

In figure 47, a model is given for the transformation of the noise for the individual mixers to the noise produced by a single channel in the receiver. R_{eqmrf}, and R_{eqmif} are the equivalent noise resistances of the RF-to-IF mixers and the IF-to-Baseband mixers respectively. Both A_{vrf} and A_{vif} are the voltage conversion gains of the desired carrier from RF, to the output of the IF lowpass filter, and the desired signal gain from the mixer input at IF, to the mixer output just before the summation of the two signal paths taking into account the signal gain acquired when mixing from IF to baseband.

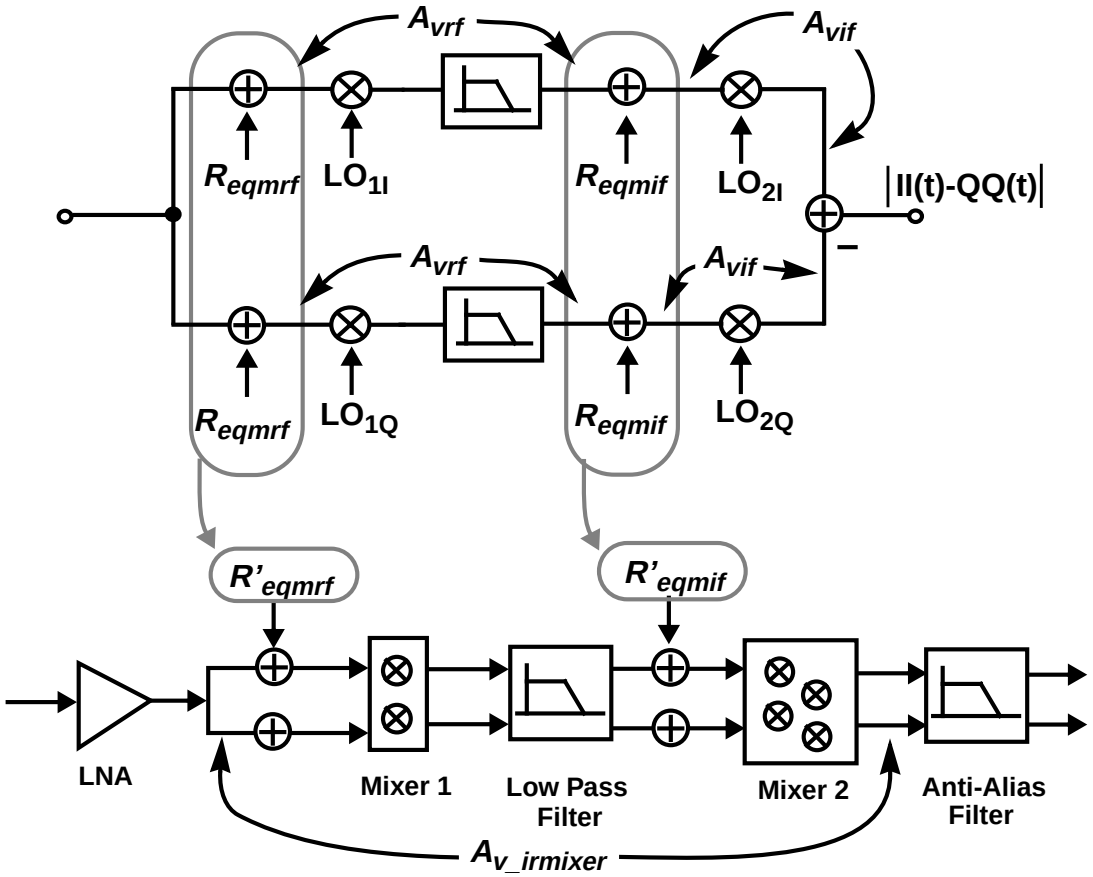

Figure 47. Model used to evaluate the noise and single gain in a single channel.

One method to understanding the relationship between the signal gain and the effective noise produced at baseband, by the mixers, can be understood by applying a test signal at the image-rejection mixer input and finding the transfer function of the signal through both mixer channels to the final mixer output at baseband. Likewise, the

noise transfer function from each mixer can be referred to the output of one channel at baseband. First, a desired signal of mean squared voltage power S_D, is applied to the input of the mixer. Before the signal in the two signal paths are summed to produce one channel, the desired signal power is,

$$S^{II}{}_D = (A_{vrf} \cdot A_{vif})^2 \cdot S_D \qquad \text{(Eq 4.2)}$$

After the summation of the channels, there is an effective gain of 2x in the signal amplitude and a 4x increase in the signal power.

$$S^{I}{}_D = (2 \cdot A_{vrf} \cdot A_{vif})^2 \cdot S_D \qquad \text{(Eq 4.3)}$$

Or,

$$S^{I}{}_D = 4 \cdot (A_{vrf} \cdot A_{vif})^2 \cdot S_D \qquad \text{(Eq 4.4)}$$

Using a similar approach, the noise produced by the mixers, at the output of one of the two channels is,

$$N^{II} = ((A_{vrf} \cdot A_{vif})^2 \cdot 4kTR_{eqmrf} + A_{vif}{}^2 \cdot 4kTR_{eqmif}) \cdot B \qquad \text{(Eq 4.5)}$$

where B is the signal bandwidth. Because the noise between the two signal paths is uncorrelated, the power of the noise adds when the two channels are added together. The total noise at the output of the mixer as a result of the noise inside the mixer is,

$$N^{I} = 2 \cdot [((A_{vrf} \cdot A_{vif})^2 \cdot 4kTR_{eqmrf} + A_{vif}{}^2 \cdot 4kTR_{eqmif}) \cdot B] \qquad \text{(Eq 4.6)}$$

Similar to the SNR argument for a differential amplifier, the desired signal before summation is correlated between the two channels. Therefore, the amplitudes add and the power of the signal is increased by 4x after the summation. However, the noise power only increases by 2x passing through the summation circuit. Therefore,

there is a net 3dB increase in the signal to noise ratio, before and after the summation. The SNR at the output of the I (or the Q channel) channel, can be expressed as,

$$SNR^{I} = \frac{4 \cdot (A_{vrf} \cdot A_{vif})^2 \cdot S_D}{2 \cdot [((A_{vrf} \cdot A_{vif})^2 \cdot 4kTR_{eqmrf} + A_{vif}^{\ 2} \cdot 4kTR_{eqmif}) \cdot B]} \qquad \text{(Eq 4.7)}$$

or,

$$SNR^{I} = \frac{2 \cdot (A_{vrf} \cdot A_{vif})^2 \cdot S_D}{[((A_{vrf} \cdot A_{vif})^2 \cdot 4kTR_{eqmrf} + A_{vif}^{\ 2} \cdot 4kTR_{eqmif}) \cdot B]} \qquad \text{(Eq 4.8)}$$

From equation 4.8, it is clear that the SNR or CNR of the desired signal increases by 3dB when the signal passes from before to after the summation of the signal paths at baseband. The question now arises of how to translate the noise produced by a single mixer to the noise of the entire radio channel. One method of translating the equivalent input noise of a single mixer to that of the entire receiver, is to simply replace the equivalent noise resistance associated with each mixer stage with that of a noise resistance half the value of a single stand alone mixer. Therefore, in the receiver R_{eqmrf} and R_{eqmif} now become, $R'_{eqmrf} = R_{eqmrf}/2$ and $R'_{eqmif} = R_{eqmif}/2$ where, R'_{eqmrf} and R_{eqmif} are the equivalent noise resistances in the receive signal path (see figure 47). Figure 48 is a more detailed model showing the equivalent noise resistance of an individual mixer cell translated to an equivalent used to estimate the noise for the comprehensive receiver channel.

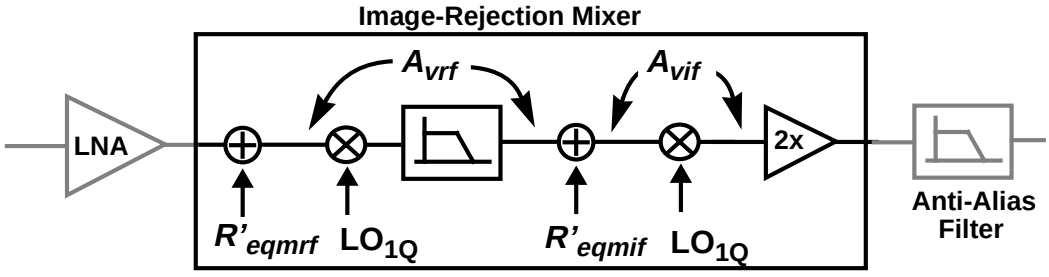

Figure 48. Model used to refer the noise of the individual mixers to the overall noise contribution in the receiver.

It is easy to verify that this noise model for the image-rejection mixer actually works by finding the signal to noise ratio at the output of the model shown in figure 48. Assuming there is a signal of power S_D at the input of the mixer, now calculate the signal to noise ratio at the baseband output. The signal power at the output of the I baseband channel is,

$$S_D^I = (2 \cdot A_{vrf} \cdot A_{vif})^2 \cdot S_D \qquad \text{(Eq 4.9)}$$

while the noise power at the mixer output is,

$$N = [(2 \cdot A_{vrf} \cdot A_{vif})^2 \cdot 4kTR'_{eqmrf} + (2 \cdot A_{vif})^2 \cdot 4kTR'_{eqmif}] \cdot B \qquad \text{(Eq 4.10)}$$

and the SNR at the baseband input is,

$$SNR^I = \frac{(4) \cdot (A_{vrf} \cdot A_{vif})^2 \cdot S_D}{(4) \cdot [(A_{vrf} \cdot A_{vif})^2 \cdot 4kTR'_{eqmrf} + (A_{vif})^2 \cdot 4kTR'_{eqmif}] \cdot B} \qquad \text{(Eq 4.11)}$$

or,

$$SNR^I = \frac{(A_{vrf} \cdot A_{vif})^2 \cdot S_D}{[(A_{vrf} \cdot A_{vif})^2 \cdot 4kTR'_{eqmrf} + (A_{vif})^2 \cdot 4kTR'_{eqmif}] \cdot B} \qquad \text{(Eq 4.12)}$$

replacing R'_{eqmrf} with $R_{eqmrf}/2$ and R'_{eqmif} with $R_{eqmif}/2$ in equation 4.12 results in,

$$SNR^I = \frac{(A_{vrf} \cdot A_{vif})^2 \cdot S_D}{[(A_{vrf} \cdot A_{vif})^2 \cdot 4kT(R_{eqmrf}/2) + (A_{vif})^2 \cdot 4kT(R_{eqmif}/2)] \cdot B} \qquad \text{(Eq 4.13)}$$

which gives,

$$SNR^I = \frac{2 \cdot (A_{vrf} \cdot A_{vif})^2 \cdot S_D}{[(A_{vrf} \cdot A_{vif})^2 \cdot 4kTR_{eqmrf} + A_{vif}^2 \cdot 4kTR_{eqmif}] \cdot B} \qquad \text{(Eq 4.14)}$$

which is identical to equation 4.8. Therefore, when estimating the noise figure of the integrated portion of the receiver using equation 4.14, $R_{mixer1} = R_{eqmrf}/2$ and $R_{mixer2} = R_{eqmif}/2$ should be used to represent the noise contribution from the first and second stage of mixing. Analysis of the CNR at the output of the receiver should also utilize half the equivalent input noise of a single mixer in the I and Q signal paths.

4.7 Image-rejection mixer phase and gain mismatch

Although single-sideband mixers have long held the promise of providing a potentially integrated solution for image rejection, there are problems which do exists with this approach. One such problem relates to matching issues between the various signal paths used by an image-rejection mixer. The magnitude of the achievable image rejection is a function of both phase and gain error between the various channels used by the mixer. This can be understood on an intuitive level, by examining figure 44. Here it is clear to see that if either of the local oscillators used by the first or second stage downconversion are not exactly in quadrature (90^o phase difference), then the image signals produced just before the summation at the output of the Weaver mixer will not be exactly 180^o degrees out of phase. This will have the affect of leaving a residual image signal after summation. Likewise, if the gain is mismatched between the two channels in figure 44, a residual image signal will be left after adding the channels together.

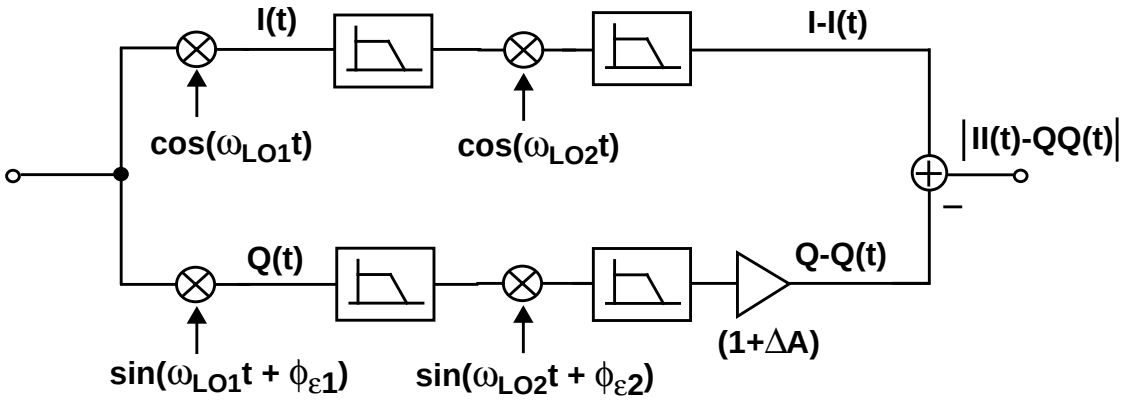

Figure 49. Model used to derive the magnitude of image-rejection as a function of the phase error in the first local oscillator ($\phi_{\varepsilon 2}$), phase error in the second local oscillator($\phi_{\varepsilon 1}$) and the gain mismatch between the two channels (ΔA).

An exact quantitative expression can be derived for the image-rejection as a function of both the phase and gain mismatch between the two received channels, using a model of which is given in figure 49. Here $\phi_{\varepsilon 1}$ defines the phase error in the first local oscillator, where $\phi_{\varepsilon 1}$ is the total deviation of the first local oscillator from quadrature. For

example, if the phase difference between the I and Q LO inputs applied to the first set of mixers is 92^o, then $\phi_{\varepsilon 1}=2^o$. Likewise, $\phi_{\varepsilon 2}$ represents the amount the phase of the second set of local oscillators deviates from 90^o. Appendix A gives a derivation for the magnitude of image-rejection as a function of the both the phase and gain mismatch of the mixer, the result of which is presented below.

$$IRR(dB) = 10 \cdot \log\left[\frac{1 + (1 + \Delta A)^2 + 2(1 + \Delta A)\cos(\phi_{\varepsilon 1} + \phi_{\varepsilon 2})}{1 + (1 + \Delta A)^2 - 2(1 + \Delta A)\cos(\phi_{\varepsilon 1} - \phi_{\varepsilon 2})}\right] \qquad \text{(Eq 4.15)}$$

There may be additional error added to the phase difference between the I and Q channel due to a mismatch in both device sizes in the mixers as well as unequal capacitive loading at IF and baseband of the two channels. These errors can be lumped in with either $\phi_{\varepsilon 1}$ or $\phi_{\varepsilon 2}$. A plot of the image rejection as a function of the phase mismatch is

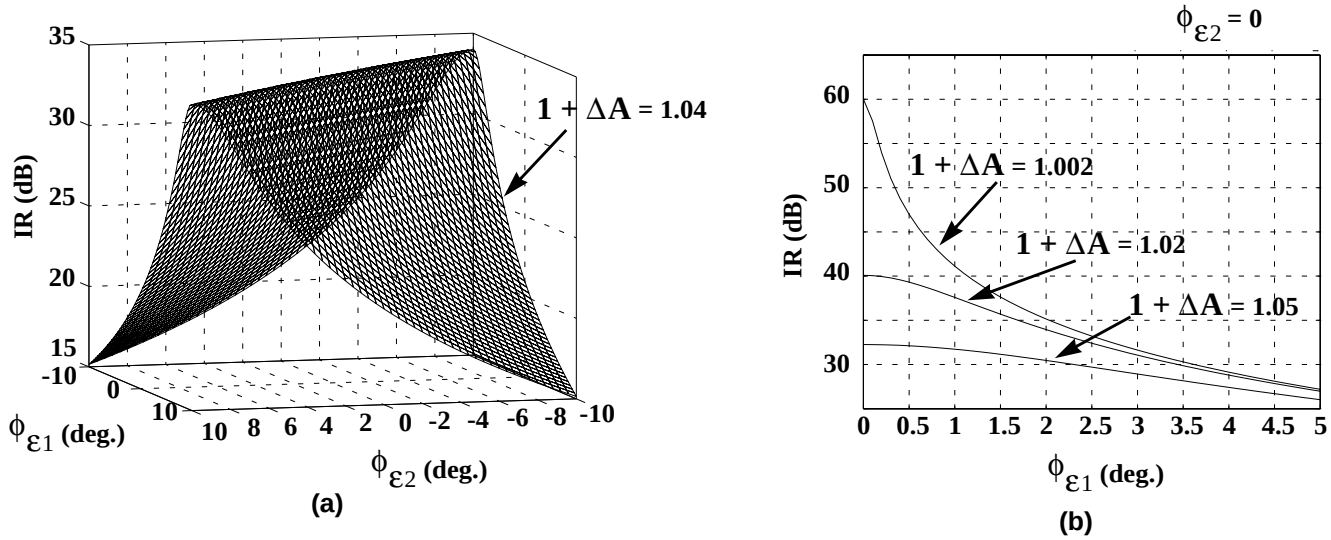

Figure 50. Image Rejection as a function of LO phase mismatch. (a) Illustrating IR dependence on $\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$. (b) IR as a function of $\phi_{\varepsilon 1}$ and gain mismatch, $\phi_{\varepsilon 2}$ = 0.

given in figure 50 for several contours of gain mismatch.

Although the mismatch between the two channels of the Weaver method can significantly limit the amount of practical image-rejection which may be obtain, there are certain techniques which can be applied to improve the matching of this image-

rejection mixer. Chapter 5 will examine some of the previous approaches to improving both the phase and gain mismatch of an image-rejection mixer.

There are other disadvantages which limit the usefulness of this class of image-rejection mixer, one of which relates to the required dynamic range of the second set of mixers. This is particularly problematic in the Wideband IF approach where the entire RF band is passed through the IF. Ideally the image signal is canceled when the two channels are added together, however, the image-rejection mixer must pass both the image and desired signal through the IF mixers (second set of mixers). Therefore, the IF mixers must have a low enough noise floor to receive a weak desired signal in the presence of a strong blocker which may be present within the image band. This situation is illustrated in figure 51.

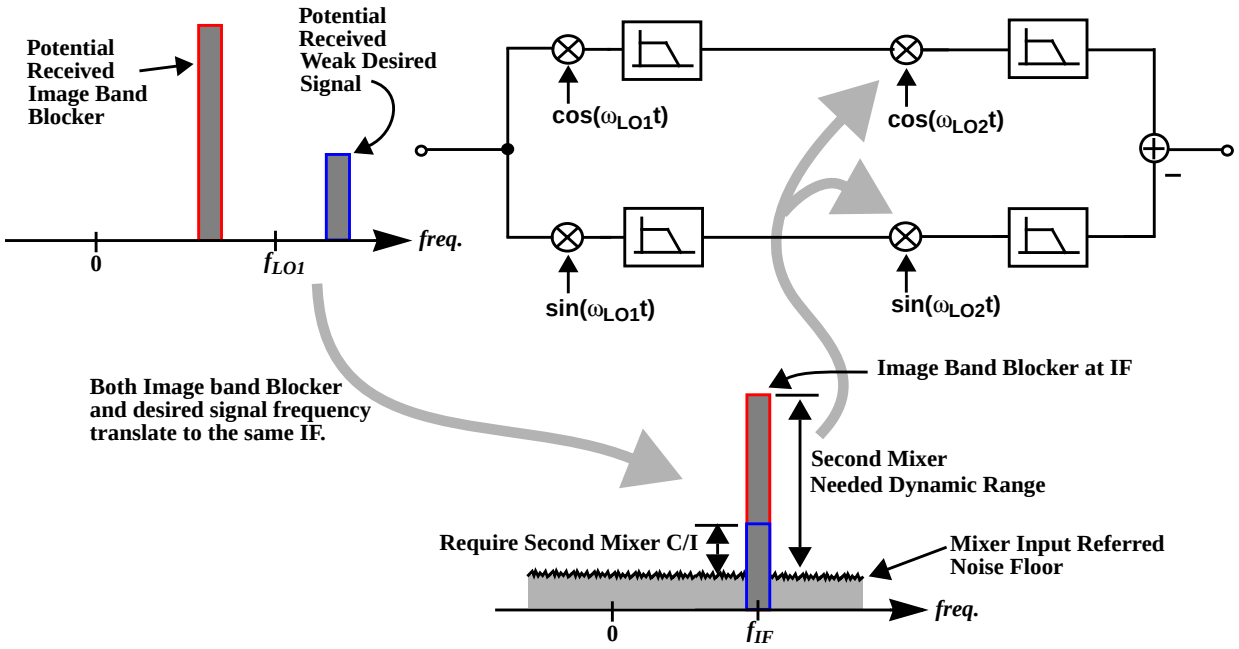

Figure 51. Illustration of an image band blocker in the presence of a weak desired band signal being passed to IF. The second set of mixers must have the dynamic range to pass both the image and desired signals, before image cancellation takes place.

4.8 References

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Chapter 5

Adaptive Image-Rejection Mixer

5.1 Introduction

The usefulness of image-rejection mixers for frequency translation in either the receiver or transmit channel of a high integration transceivers was presented in the previous chapter. The limitation of this class of single sideband mixers was also outlined with a quantitative expression given for the image-rejection performance as a function of mismatch. Specifically, it was shown in chapter 4, that the magnitude of attainable image suppression is limited predominantly by both the gain and phase mismatch between the in-phase and quadrature IF mixer channels.

This chapter will begin with a discussion of some of the techniques, which have been used in the past, to improve either the phase or gain accuracy between multiple signal paths, in an image-rejection mixer. Although many of these techniques are useful and widely used, the overall image-rejection which may be obtained is typically limited, without tuning, to about 30-35dB. While this level of sideband suppression may be adequate for short range systems with moderate required image-rejection performance, this would not be suitable for standards with higher selectivity requirements, such as is the case for many cellular networks like GSM. Therefore, this

chapter will introduce and describe a system which self-calibrates both the phase and gain settings between the two paths of a Weaver mixer, to give maximum sideband or image suppression. The self-calibrating mixer which will be described is a mixed signal system which utilizes both analog front-end components, as well as post ADC digital logic to obtain an optimal solution for maximum image rejection. A description will be given of all the analog components required of this mixer system. Although the analog portion of this mixer was included on the 2nd generation DECT/GSM receiver, the digital portion was realized only in the form of software. However, the last section of this chapter will describe some of the issues related to the digital algorithm which was intended for use with the analog portion of the self-calibrating mixer.

5.2 Methods to Improve Phase and Gain Matching

Improving the sideband suppression which is achievable within an image-rejection mixer is done through a combination of realizing circuits with excellent layout symmetry between the various signal paths and/or utilizing circuits which generate accurate quadrature phase. Techniques for good layout as well as some recently proposed methods for improving the phase accuracy are discussed in this section.

Good layout practice is always essential for any integrated circuit application where the performance is constrained by component matching. For the two prototypes receivers which utilized an image-rejection mixer, component matching was a concern, which implied generating a layout with minimal mismatch between the various signal paths.

Figure 52 is a die photo of the image-rejection mixer used by the DECT prototype receiver. This will be used as an example to highlight some of the symmetric

layout techniques, which were used, to enhance both the matching and sideband suppression performance.

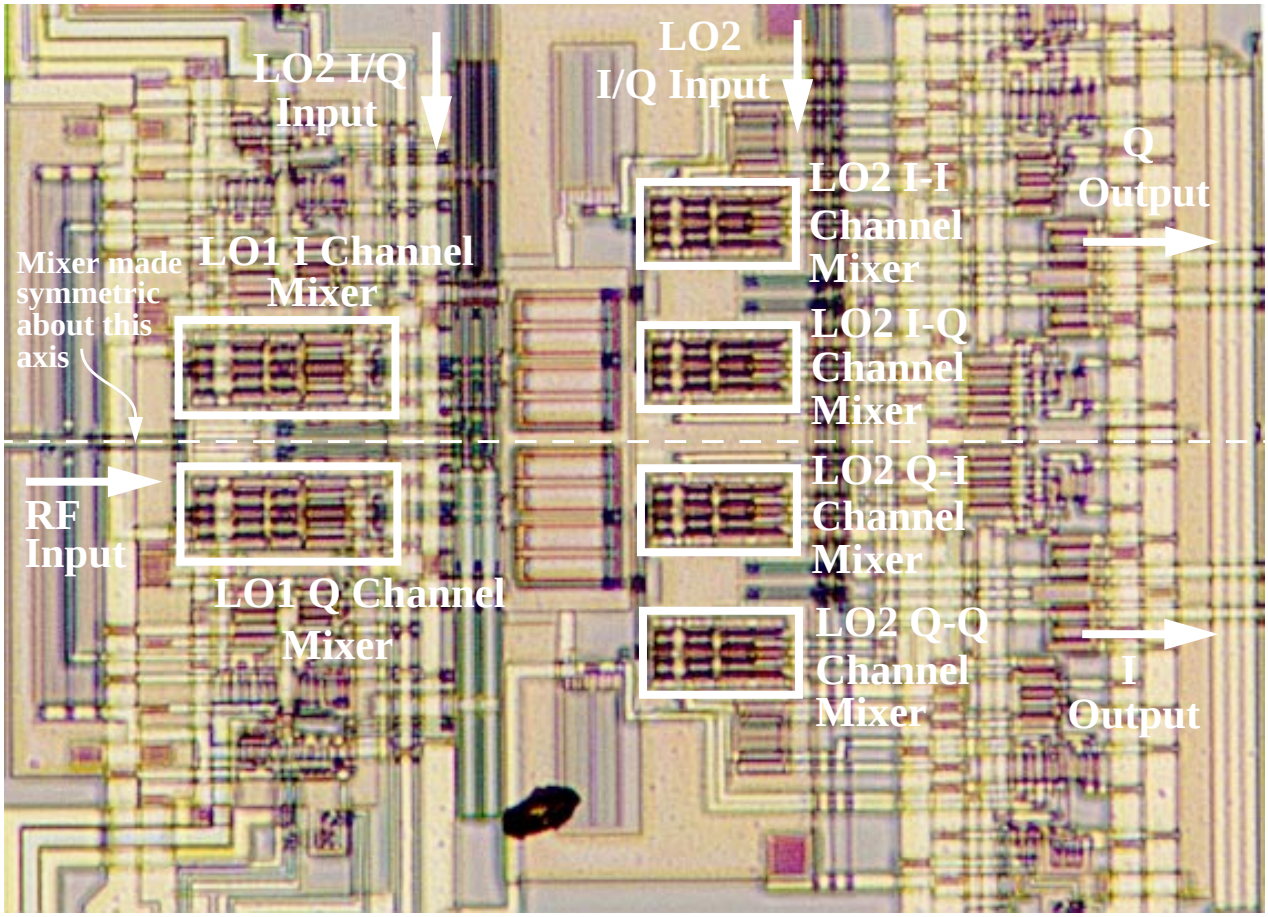

Figure 52. Die photo of the image-rejection mixer used by the DECT receiver.

Some of the layout techniques used to obtain better I and Q matching included the following:

1) Perfect mirror symmetry is applied to both the Gilbert Cell mixers which are used as well as the entire signal path. From figure 52, the RF input comes in from the left, and exists the right as I and Q baseband signals. A virtual line could be drawn horizontally between the I and Q paths of the mixer. All components on the top of this line are mirror images of every component below. In addition, the I and Q mixers as well as the II, IQ, QI and QQ paths are perfectly symmetric in layout.

2) Common centroid techniques are also useful for the switches of all the down conversion mixers. Here, the critical component to match lies between the effective input capacitance looking into the mixer LO port. Any potential

mismatch between device sizes will lead to an asymmetry between the capacitive loading of the mixer local oscillator inputs, resulting in an uneven loading of any quadrature generation circuit which is driving the mixer LO input, subsequently leading to an I/Q phase error. One technique to overcome a mismatch in device loading, is to layout the switches using common centroid techniques [5.1]. This technique was applied to the switches used by all the current commutating mixers.

3)To reduce the phase error between the inphase and quadrature local oscillator outputs, all of the signal traces must have perfect symmetry including segments which have 90 degree corners. From figure 52, the I and Q LO lines were brought in from the top side of the mixer, and run vertically to the mid-point of the image-rejection mixer. Routing was tapered off from the main line into the mixer switch in such a way that both the I and Q differential LO routing all had the same length and an equal number of corners. A similar layout philosophy was applied to the RF input to the two high frequency mixers, as well as the baseband I and Q signal paths.

Although good layout practice will lead to excellent symmetry and matching between the signal paths, additional methods for phase matching, leading to better image-suppression, may be obtained with circuit techniques which attempt to provide high phase accuracy. To date, considerable effort has been applied to circuit methods and systems which attempt to derive more accurate quadrature local oscillator signals eventually used by the mixer. One such approach cleverly adds and subtracts different phases of a quadrature local oscillator to generate an LO which produces excellent quadrature (90^o)[5.2][5.3][5.4]. Another approach is the use of an asymmetric polyphase filters to generate a local oscillator with accurate quadrature phases[5.6]. It is shown in chapter 7, that polyphase filters inherently have excellent matching characteristics and produce quadrature phase signals with less than 1.0^o phase error with components that are mismatched by as much as 10% within the filter. A third recently proposed method to generating quadrature signals, is through the use of a level-locked loop [5.5]. In the this approach, the quadrature signals are derived with a divide by two circuit which is placed inside a Level-Locked loop. Both of the quadrature outputs of the divide by four are multiplied together, the product of which is low pass filtered to produce a DC value, which is similar to a control voltage in a phase-locked loop. This DC value sets the common mode of the local oscillator which is the

clock input of the divide by 2 circuit. By modulating the common mode of the divider circuit clock input signal, the phase between the I and Q outputs of the divide-by-2, can be modulated.

While the previous mentioned techniques are extremely useful when trying to implement circuits which generate accurate quadrature signals coming out of the local oscillator, additional phase mismatch between image signals will be created within the mixer receive signal path. Therefore, methods to improve the phase accuracy of an LO signal are only useful in correcting the error introduced at the mixer LO input ports. An improved LO phase accuracy will contribute to better sideband suppression, however, additional phase error will be introduced in the receive signal path, due to both device and capacitive mismatch between the I and Q channels. This implies that the image signal at baseband, before summation, will not be exactly 180^{o} out of phase. Thus, what ultimately counts for excellent sideband suppression is generating two image signals which are 180^{o} out of phase, and not necessarily generating accurate quadrature phase LOs.

One approach to improving the image-suppression by developing image signals which are closer to 180^{o} out of phase in the two mixer channels, is through the use of polyphase filters [5.6] which are placed within the signal path. The basic idea is to utilize the core Weaver method and insert polyphase filters along the signal path at both IF, and baseband, as is shown in a figure 53. This has the affect of improving the gain and phase accuracy of the signal as it passes through the receive signal path, which ultimately accurately generates image signals which properly cancel when the channels are added back together. This technique has been demonstrated with very high sideband suppression in [5.7] and [5.8] with better than 50dB of image-suppression. As alluded to in the previous chapter, polyphase filters have excellent phase accuracy characteristics, however, the loss associated with this class of phase shifting filter is non-negligible. Therefore, the insertion of these type filters, within the signal path, can

degrade the desired carrier power which ultimately degrades the overall noise figure, or requires the use of power hungry buffers to compensate for the signal loss.

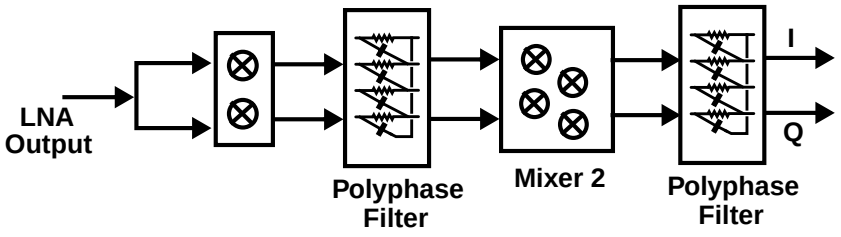

Figure 53. Weaver mixer with polyphase filters added within the signal path.

Additional means of improving sideband suppression may be obtained through laser trimming in production. This might be through modifying the resistance of a phase-shift filter to give maximum image-rejection. Although, this provides a nice alternative to using an image-rejection filter, there is a cost penalty associated with laser trimming in production, making this approach less attractive over discrete filters.

5.3 Adaptive Image-Reject Mixer

With the advent of radio receivers which are fully integrated in silicon, the possibilities of addressing traditional circuit non-idealities through new on-chip systems becomes a reality. In this theme, the second prototype receiver designed for both the DECT and DCS1800 standards, included an image-rejection mixer with the capability of tuning both the phase and gain between signal paths, such that the image-suppression is maximized. This self-calibration is accomplished by first deliberately injecting a calibration tone, at the RF input, of the image-rejection mixer (figure 54). The frequency of the calibration tone is synthesized with an on-chip PLL which

produces the tone at the image frequency of the desired received signal, the concept is illustrated in figure 54.

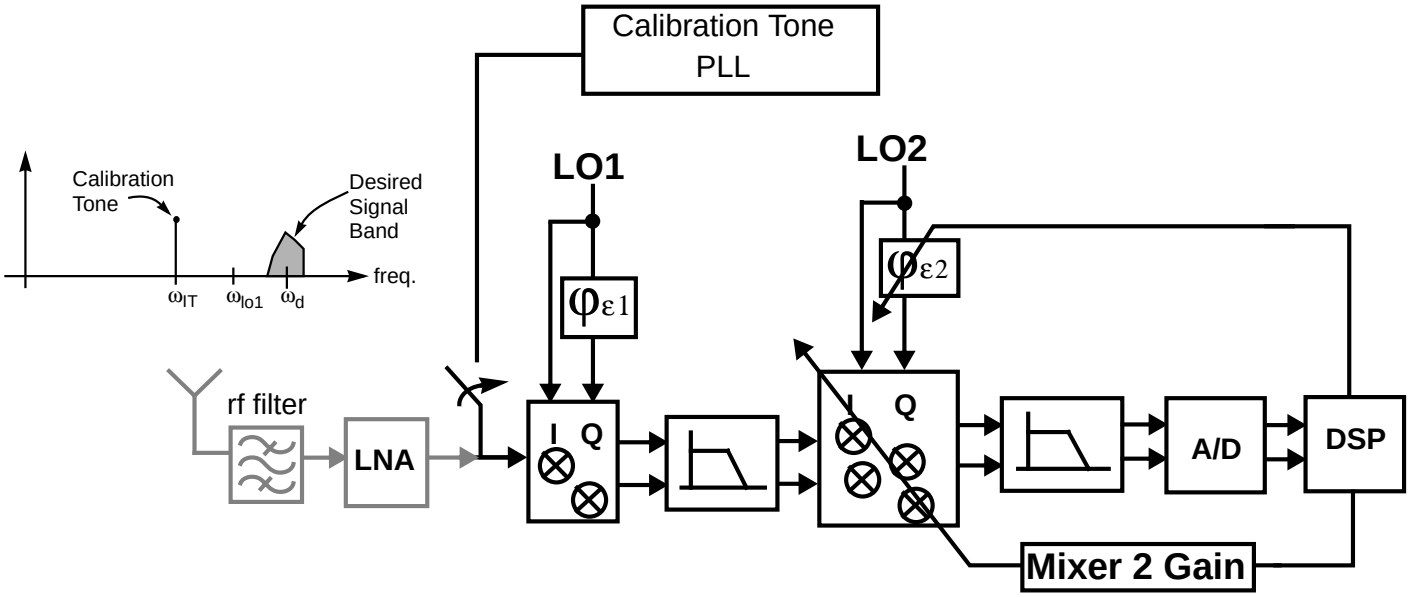

Figure 54. Block level conceptual diagram of the adaptive image rejection mixer. The total phase error is corrected using one tunable IQ phase generation circuit at the second LO input.

The basic idea behind this system is to use an on-chip PLL, which generates a tone directly in the image band, during an initial calibration period. This might be when the receiver is powered up or in the case of DCS1800, between received frames as this system is time domain duplexed (TDD). A switch is also provided on-chip, to connect the output of the calibration synthesizer, with the RF input of the image-rejection mixer. The calibration tone is then down-converted to baseband, where ideally if there were no mismatch, the image tone would be cancelled by the image-rejection mixer. However, due to mismatch there will be a residual tone which remains at baseband. The magnitude of this residual image tone is estimated using the post-ADC digital baseband. The baseband then determines how to modify the phase, as well as the gain to essentially drive the magnitude of the residual image tone at baseband, to be as close to zero as possible. A little more description of the analog electronics from a system

perspective is now given. The actual hardware which modulates the phase between the I and Q LO inputs, using a digital input computed in the baseband, is described in section 7.3.2.1 of chapter 7.

5.3.1 Requirements for the Self-Calibrating Analog Components

By reviewing from the magnitude of achievable image suppression from a a more mathematical perspective, much insight can be developed as to the requirements of this self-calibrating mixer. The equation for the magnitude of image-suppression as a function of path mismatch which was given in chapter 4, and derived in appendix A, is repeated below.

$$\mathrm{IRR(dB)} = 10 \cdot \log\left[\frac{1 + (1+\Delta A)^2 + 2(1+\Delta A)\cos(\phi_{\varepsilon 1} + \phi_{\varepsilon 2})}{1 + (1+\Delta A)^2 - 2(1+\Delta A)\cos(\phi_{\varepsilon 1} - \phi_{\varepsilon 2})}\right] \qquad \text{(Eq 5.1)}$$

From equation 5.1 an interesting observation can be made which has a practical implication which respect to realizing the circuits which actually tune the phase for maximum image-rejection performance. Equation 5.1 gives the ratio in dB of the magnitude of the desired carrier, to the magnitude of the image response, at the final mixer output (post summation of channels). To suppress the undesired image response, implies that we want to make the Image-Rejection Ratio (IRR) as large as possible. Therefore, to get the best performance out of the image-rejection mixer, it is desired to drive the dominator in equation 5.1, as close to zero as possible. The interesting observation to make with respect to tuning the phase is that the IR ratio will be at a maximum when the argument of the cosine function in the denominator is driven to zero, this will occur when the difference of $(\phi_{\varepsilon 1} - \phi_{\varepsilon 2})$ is minimized. This implies that the comprehensive phase error within the image-rejection mixer can be removed by tuning the phase of just *one* of the two local oscillators.

In the DSC1800/DECT prototype receiver, the first local oscillator operates at approximately 1.5GHz, with the second LO at 3-400MHz. Thus, the tuning of the phase for maximum image rejection is accomplished by tuning just the lower frequency local oscillator (LO2), while the first local oscillator has quadrature inputs which are fixed and not phase tunable. From an implementation perspective this has the advantage that the more complicated function of tuning the phase is pushed to a lower frequency in the form of a tunable quadrature generators used at the LO inputs, of the second stage mixers.

Intuitively, the concept of tuning the comprehensive phase error of the entire path, of the image-rejection mixer by tuning just the phase between the second LO input, can be understood by looking at figure 44 in chapter 4. Remembering that the real objective in virtually all image-rejection mixers is to create a 180^o phase shift between the image signals, in two channels, just before summation at the output of the mixer. Now, if the first quadrature local oscillator mixer input has a 2^o phase error, then the image signal between the two channels at IF, will be off by 2^o. Thus, by rotating the phase of the second local oscillator 2^o in the opposite direction, the phase error due to the first local oscillator will be compensated. Likewise, any phase error within the mixer channels can be negated by tuning the phase of just one of the two local oscillators.

A detailed block diagram of the adaptive image rejection mixer is shown in figure 55. Again the six mixer configuration is shown which implements a weaver architecture and generates I and Q baseband signal paths. Here the first higher frequency oscillator labeled as LO1 generates a a fixed 90^o of phase between the I and Q mixer local oscillator input ports. The second local oscillator which is used to frequency translate the intermediate frequency signal to baseband is then used to correct the comprehensive phase error in two of the four signal paths of this image-rejection mixer. The gain is then corrected by digitally modulating the gain in two of the four mixers, used for frequency translation. This is represented in figure 55, as a single tunable gain block, however, as will be shown in the next chapter, this tunable

gain block was implemented by modulating the gain of the second stage mixer. Each of the blocks must be tuned independent of the other. The two phase tuners are calibrated independently for the minimum image response. Likewise, the calibration is repeated on an individual basis for the two gain stages.

In keeping with the theme of pushing as much of the radio functionality as possible in to the digital domain, both the estimation of the magnitude of the image tone at baseband, as well as an update for the phase and gain is done purely in the digital domain. Thus, both the phase and gain tuners are controlled digitally. With this said, both the range and the resolution (number of bits) must be determined for both the digital words used to update the phase and gain.

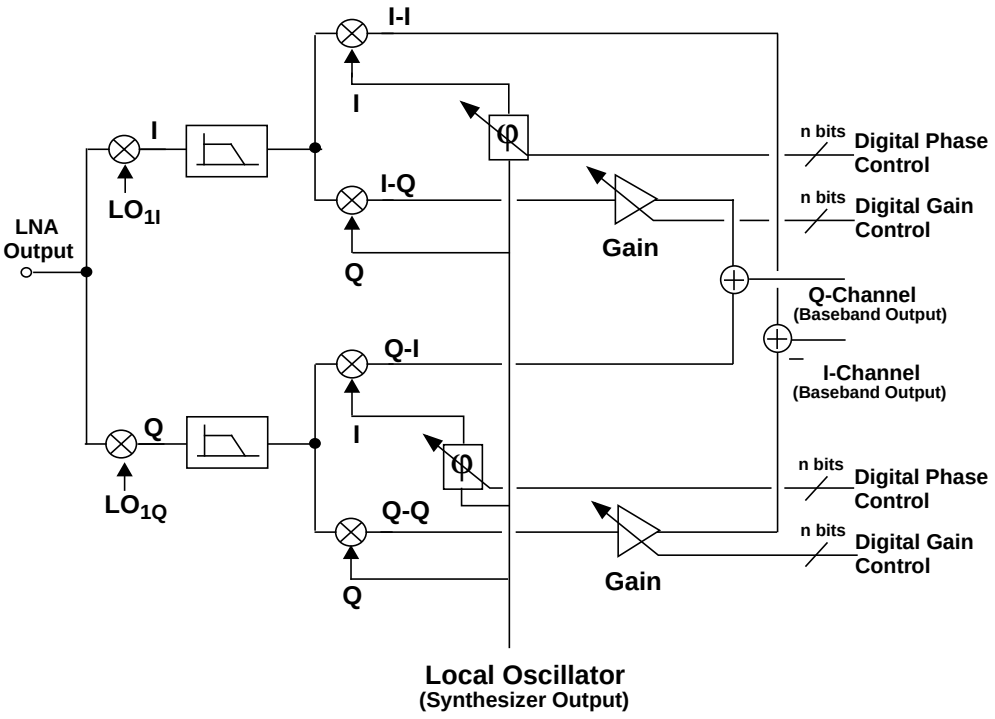

Figure 55. Digital Block Diagram illustrating the digital control (tuning) of both the phase and gain errors in the self-calibrating image-rejection mixer.

The question now arises as to what is required of the individual tuning blocks, to achieve a specified minimum image rejection. In chapter 4, it was shown that for a heterodyne system desired for DCS 1800 standard, with a 400MHz intermediate

frequency, an image suppression of 60dB is required of the six mixer configuration. With 60dB of required image suppression, the minimum resolution of the phase and tuners (shown in figure 55), can be determined. Figure 56 shows the image suppression ratio plotted in contours of gain mismatch ($\Delta\mathbf{A}$) as a function of the comprehensive phase error ($\varphi_{\varepsilon t}$) between the two mixer channels. From figure 56 and equation 5.1, it is clearly seen that the required resolution in phase tuning is dependent on the obtainable resolution in gain tuning and vice-versa.

Because of the interdependence between the phase and gain error on the image rejection, it was desired to first pick either a minimum achievable phase or gain setting. With a knowledge of the practical minimum accuracy (in either phase or gain) for one variable, the necessary resolution of the other variable (gain or phase) can be determined. This process was done through a combination of simulation and experimental data obtained from the DECT prototype image-rejection mixer[5.9]. From simulation, it was found that by modulating the tail current through the Gilbert cell mixers, a difference in the gain tunable resolution in gain of 0.001 was possible. Using data measure from the DECT receiver, it was estimated that with careful layout a worst case gain between signal paths was found to be +/- 1%. However, to ensure a sufficient range of the gain tuning, the system was specified to correct for as much as a 5% gain error between the two channels. This now defines the total range of gain tuning required as well as the minimum required resolution in gain. With this information, both the number of bits required for the gain control and the minimum resolution in phase tuning can now be determined. From the above information, the digital tuning required of the gain is,

Max. $\Delta\mathbf{A}$ required : 0.05

Min. $\Delta\mathbf{A}$ required : 0.001

Total resolution of gain control : 0.05/0.001= 50 levels or ~ 6 bits of control.

Again referring to the plot shown in figure 56, the required resolution in phase may now be determined using the minimum achievable resolution in gain. Since the specified minimum resolution in gain is 0.001 this implies that the contour which should be examined in figure 56 is the curve labeled “1+ΔA = 1.001”. The shaded area in figure 56 now defines the target performance in terms of image suppression, gain and phase accuracy which is required to achieve 60dB of image suppression. It can be seen from figure 56 that with a gain tuning resolution of 0.001 the minimum resolution in phase tuning for better than 60dB of suppression is 0.1^o. To allow a safety margin a minimum resolution in phase tuning of 0.05^o was used. In addition, it must be remember that there exist a need to tune to the optimal phase for every channel. This implies that a resolution of at least 0.1^o must be supplied across the entire range of LO2 frequencies which span from 350MHz to 420MHz.

The maximum tunable phase required of the second local oscillator is determined by the total potential phase error which can accumulate in the channel. This was previously defined as $\varphi_{\varepsilon t}$. For this mixer system, the total phase error due to mismatch is the sum of the phase error from the first quadrature local oscillator, defined as $\varphi_{\varepsilon 1}$, and is specified to be designed with less than 0.5^o deviation from quadrature. while the total error within the signal path (previously labeled as $\varphi_{\varepsilon 2}$) can be made to within 0.5^o. The total potential phase error which can accumulate in the channel is the sum of the two phase errors, approximately 1.0^o. However, an additional safety margin of 3^o was added to ensure that the phase tuner would cover a broad enough range of comprehensive phase mismatch in the mixer. Again, with the minimum and maximum range of the phase tuner, the number of bits required of the phase tuner may now be determined.

Maximum range of tuning: 3^o

Minimum resolution in phase: 0.05^o

Total number of bits required: $3^o/0.05^o$ = 60 levels or 6bits.

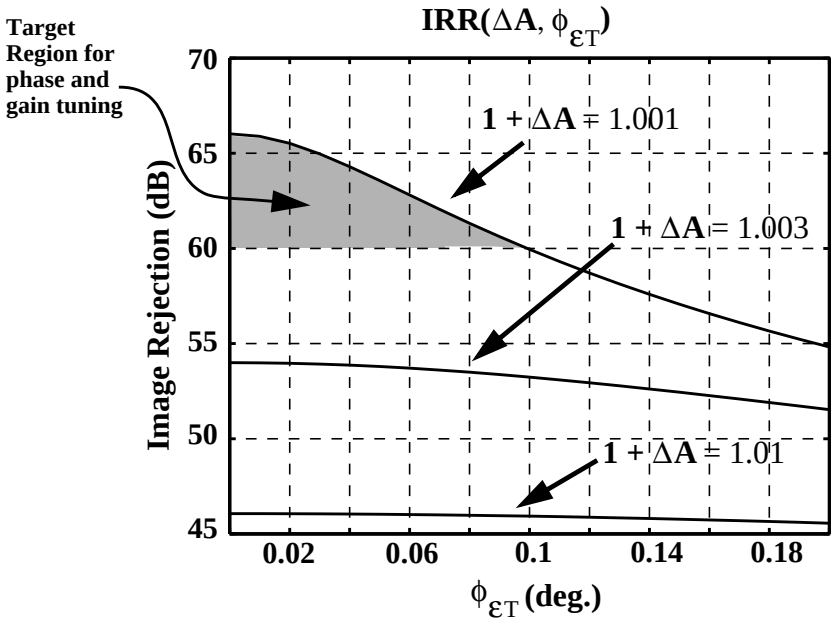

Figure 56. Image suppression as a function of the total phase mismatch a gain mismatch. To obtain a greater than image rejection a solution for the total phase and gain mismatch must lie within the shaded region.

5.3.2 Digital Image Magnitude Estimation: Digital Algorithm

With a definition of both the resolution required in phase and gain to obtain the required image-rejection for a cellular like standard such as DCS 1800, some words can be said about the digital portion of the self-calibrating mixer. A significant portion of this work was done in [5.10]. In short, this digital algorithm is done by observing the magnitude of the image (calibration tone) which is present after the ADC output. With the magnitude of the image-tone being observed at baseband, each of the tuners are swept from one end of the tuning range to the other, until the residual image tone present at baseband drops to a minimal value.

Unfortunately, it is difficult to derive information about the phase of the error signal generated at baseband (positive or negative error signal), particular when a high

image suppression ratio is required. The approach used in this work, was to monitor the magnitude of the residual image tone which appeared at baseband. Thus, unlike an LMS adaptation algorithm, or a analog feedback network, the error signal which is generated is purely a magnitude with no information in phase. Stated differently the error signal has no sign. This makes defining the direction to drive phase and gain, between the two channels difficult, and ultimately challenging to find the optimal settings in phase and gain. Therefore, both the magnitude of the image tone found in the baseband and the derivative of the magnitude with respect to either the phase or gain are both observed digitally to determine when the optimal phase and gain settings have occur, this is illustrated in figure 57.

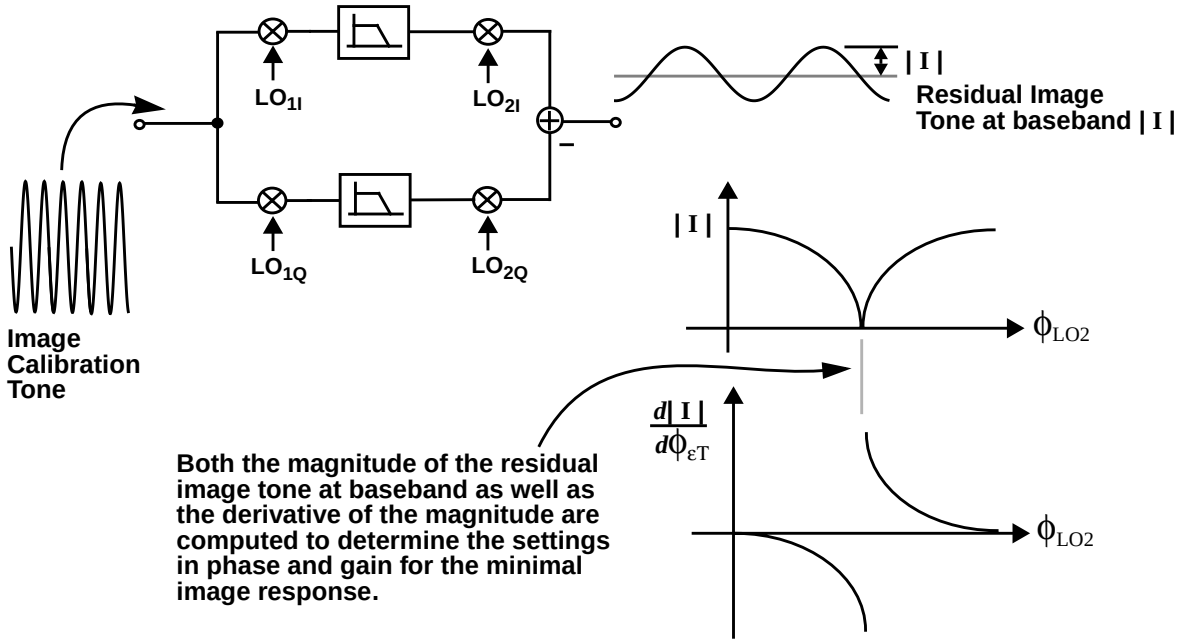

Figure 57. Information available at baseband to adapt both the phase and the gain mismatch of the image-rejection mixer. The digital portion of the radio sweeps the phase as well as gain settings, while computing the magnitude of the residual baseband image tone as well as comparing to the |I| of the previous phase/gain setting. The derivative of |I| with respect to either the phase or gain being sweep is then used to determine the settings which minimizes the magnitude of the image tone present at baseband.

When the sign of the derivative of the image tone magnitude (labeled as |I| in figure 57) changes from positive to negative or vice-versa, then it is assumed whichever variable is being modified in the mixer (be it phase or gain) has just past an optimal

point, where the magnitude of the residual image tone at baseband has been minimized. When the minimum is found for the particular variable being adjusted the process is repeated for the next tuner (again, either gain or phase adjustment). This is done until all 4 tuners have been calibrated to give the minimum image response.

The comprehensive digital algorithm described in [5.10], is shown in figure 58. During calibration, the image tone is synthesized and injected into the analog front-end at the LNA output, mixer input interface. Then, either the phase or the gain is tuned independently between two of the mixer channels. Using the variable of phase as and example, the algorithm used is described. The phase tuner is set all the way to one of end of the range of values. When the algorithm is enabled, the phase tuner begins to sweep the entire range of values using a binary search. For each trial of the binary search, 30 samples are acquired at the ADC output. The samples are then used to compute a 30 point DFT on just 100kHz (which is the frequency that the residual image tone will always lie), this effectively determines the magnitude of the image tone.

To determine the next guess in the binary search process, the existing estimate for the magnitude of the residual image tone is compared to the previous estimate and the derivative is estimated simply by computing $(1-Z^{-1})$. If the sign of the derivative changes value, then it is known that the optimal setting in phase (or in gain) has been passed. The algorithm then returns to the previous setting in phase and lowers the step size (gear shifting) used to generate a new phase setting, the binary search then continues until again the algorithm detects, via computing the magnitude and the derivative the magnitude, when a minimal image response has been passed. When again the optimal settings has been passed, the phase setting is returned to the previous value, the step size is reduced and the binary search continues. This process is repeated until the minimal step size (minimal resolution) in either phase or gain is reached. With the

phase tuned, the entire search algorithm is repeated to tune the phase between the two mixer channels.

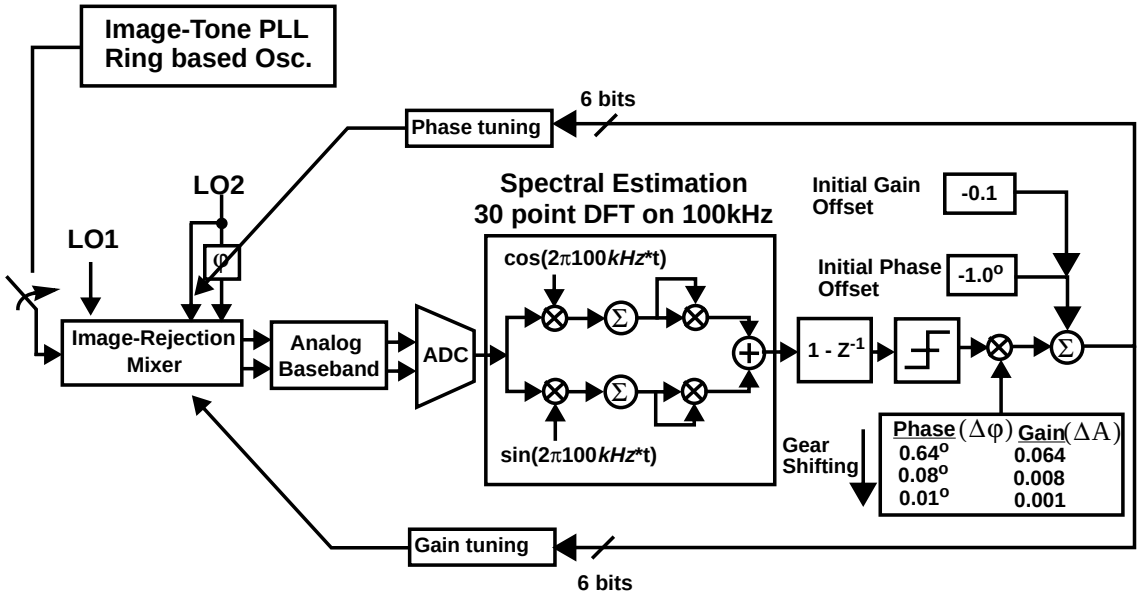

Figure 58. Digital algorithm used to adapt the analog portion of the self-calibrating image-rejection mixer

The digital algorithm described in figure 58, was modeled using a system simulator tool in matlab, called simulink. The noise as well as the expected third order distortion associated with the analog frontend were incorporated with the model of the analog frontend. The resolution in both the number of bits used by the phase and gain tuner were also modeled as well as the number of bits used for the computation of the residual image magnitude. Several simulations were run to determine whether the algorithm could adapt fast enough to allow calibration between received GSM frames, as this system is TDD. The results of one simulation are shown in figure 59. In this simulation, a phase error was deliberately introduced in LO1, of approximately 0.2^{o}. The algorithm is seen to begin the binary search hunting for the minimal response in the image-tone. Gear shifting between various step sizes can be seen as the phase is gradual tuned to the optimal setting. With the optimal phase setting in the LO2 quadrature inputs, the same procedure is then used to tune the gain for optimal image rejection, the results of which are shown in figure 59.

Although it must be qualified that the results shown in figure 59 are purely based on simulation. It is clear to see, that both the phase and the gain can be tuned within 4ms, which is approximately the time between received DCS1800 frames. Thus, the mixer has the potential of calibrating both the gain and phase to optimal settings between received frames. Although these results are purely from simulation, there does seem to be promise in building a real system which can adapt between received frames. More research is required to determine whether such a calibration system could be used by CDMA standards, which are in the receive mode, virtually operate all the time. Here the key issue is whether the desired signal, after the correlators, will be affected by a narrowband calibration tone which is injected into the front of the receiver.

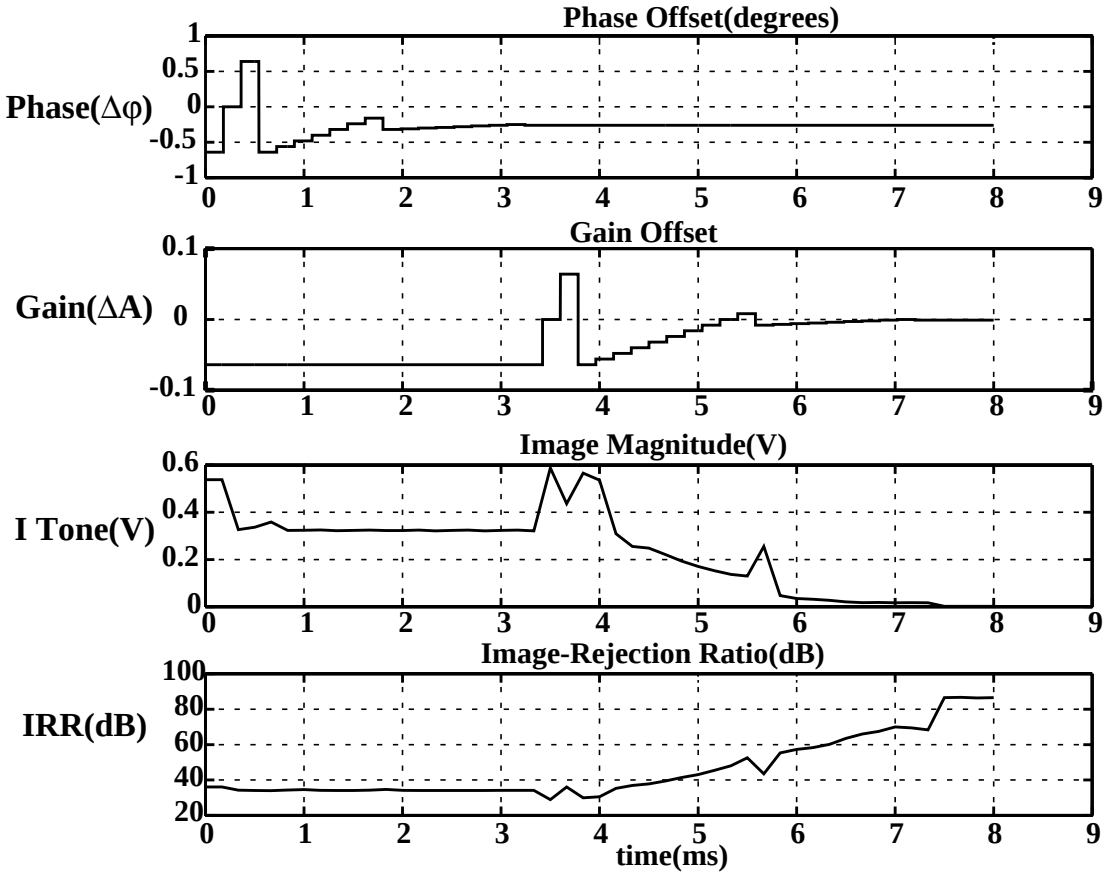

Figure 59. Simulation results of both the analog front-end and the digital algorithm used for adaptation. The top shows the phase tuner hunting for the optimal setting using a binary search algorithm. Likewise, the second plot illustrates the difference in gain between two channels of the mixer, along with convergence on the optimal gain setting. The last two plots give both magnitude of the image tone and image-rejection ratio as function of time.

Both this chapter and some of the previous material presented in chapters 3 and 4, discuss the system related aspects of the Wideband IF receiver as well as the self-calibrating image-rejection mixer. The next couple of chapters will look at more the circuit implementation details which surround the realization of both the image-rejection mixer as well as many supporting components used along the in receive chain.

5.4 References

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Chapter 6

Mixer Design

6.1 Introduction to Mixers

With a knowledge of the components used by both the Wide-Band IF system as well as the configuration used to perform image rejection, a discussion can now be given on the implementation of the circuit blocks used to realize the higher level system. Although the mixers discussed in this section are tailored for a couple prototype receivers, many of the concepts which are discussed in this chapter, can be extended to a broad class of applications which require frequency translation components utilizing only CMOS circuitry. The translation of a higher frequency signal to a lower frequency in receiver applications is typically done through the use of a mixer. Likewise, the up conversion of baseband information to a carrier frequency is also most often performed by a class of components again referred to as mixers.

Chapter 6 will provide some useful guidelines for designing active CMOS mixers which closely resemble a circuit topology originally proposed by Barrier Gilbert [6.1] and since has been known as the Gilbert Cell. This chapter begins with a description of the basic role of a mixer in both receiver and transmitter applications. This will be followed by a basic review of the frequency translation properties

associated with a mixer. A more detailed discussion will then be given on the characterization of CMOS active mixer performance with respect to the conversion gain, noise behavior and the distortion performance as well as how these figures of merit relate to the power consumption of current commutating active mixers. The approach to mixer characterization used in this work, is to provide a designer with a set of equations which characterize the mixer performance as a function of some common and intuitive variables such as the drain bias current of each mixer device (I_d), as well as the V_{GS}-V_t of each device used in the mixer. More accurate and computational efficient approaches to describing the behavior of CMOS-Gilbert-Cell-like mixers may be found in [6.2][6.3][6.4][6.5][6.6][6.7].

6.2 Mixer Basics

Mixers have long been utilized in virtually every facet of communications applications for as long as such systems have existed. They have found their place in many applications ranging from frequency up and down conversion in both wireless and wireline transceiver to the utilization as a phase detection in frequency synthesizers.

The symbol for a mixer shown in figure 60, indicates a component which actually performs a multiplication between two applied signal $S_1(t)$ and $S_2(t)$ resulting in a signal, So(t), at the output of the mixer. The symbol for a mixer implies a multiplication between two signals, this symbol often times leads to a confusion between the function of a mixer versus a multiplier. A multiplier actually performs a true multiplication between the two incoming signals $S_1(t)$ and $S_2(t)$, the output signal $S_o(t)$ is then the product of both $S_1(t)$ and $S_2(t)$. An artifact of an analog multiplication of two sinusoidal signals is the creation of an output signal which contains two spectral components one at the sum frequencies of $S_1(t)$ and $S_2(t)$ while the other component shows up at the difference between the two frequencies of the multiplied input signals. This is easily seen by using simple trigonometry on the two sinusoidal input signals as

shown in figure 60. Suppose for a minute that $S_1(t)$ is some high frequency signal received from the antenna of a receiver, while $S_2(t)$ is a signal created with a frequency synthesizer inside the receiver channel. It can be seen that the incoming signal ,$S_1(t)$, will be shifted or translated in frequency from the input to the output of the mixer by multiplying $S_1(t)$ by $S_2(t)$. In radio receivers, the difference frequency is used to typically down convert in frequency, the desired received channel and the sum frequency is filtered away. Likewise, in a transmitter system, the sum frequency is used to up convert the desired signal band before being applied to the antenna for transmission.

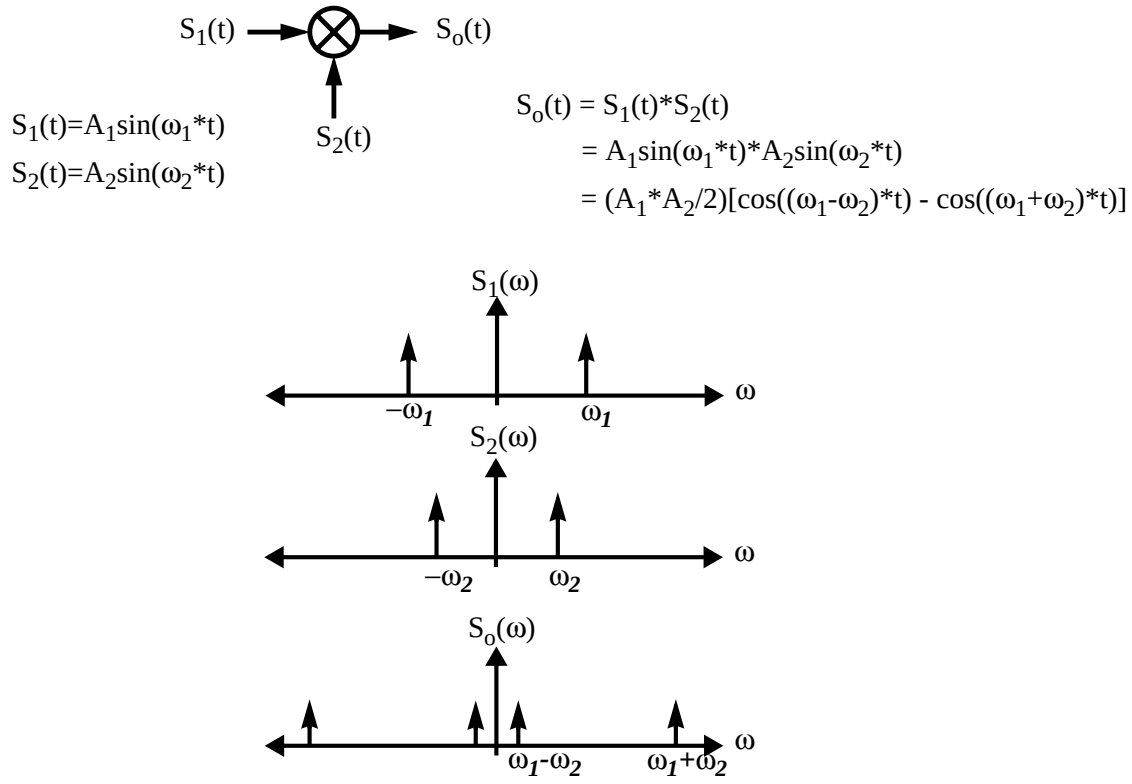


Figure 60. Analog multiplier and the affect on frequency translating sinusoidal signals.

Unlike a multiplier, mixers are a class of modulators which are designed or optimized to perform frequency translation as their primary role (frequency translation is no longer an artifact of a multiplication, but is the primary role) [6.8]. Most often a mixer is implemented with some type of switching network that is commutating at the

frequency of $S_2(t)$. The effect of switching or commutating one signal by another can be modeled as taking some desired signal, say in the case of figure 61, $S_1(t)$, and pulse modulating or multiplying by a periodic pulsed signal, here represented as $S_2(t)$ in figure 61. Remembering from basic signal processing that multiplication in the time domain is equivalent to convolution in the frequency domain, a copy of the spectrum of $S_1(t)$ will be replicated at each of the harmonics associated with the pulsed signal $S_2(t)$, this situation is illustrated in figure 61(b) where the top spectrum is shown ($S_1(f)$) represents that of the incoming signal, while P(f) represents the spectrum of the pulse which is multiplied by $S_1(t)$. The top two spectrums are convolved with each other to produce the bottom spectrum shown as $S_o(f)$ in figure 61(b).

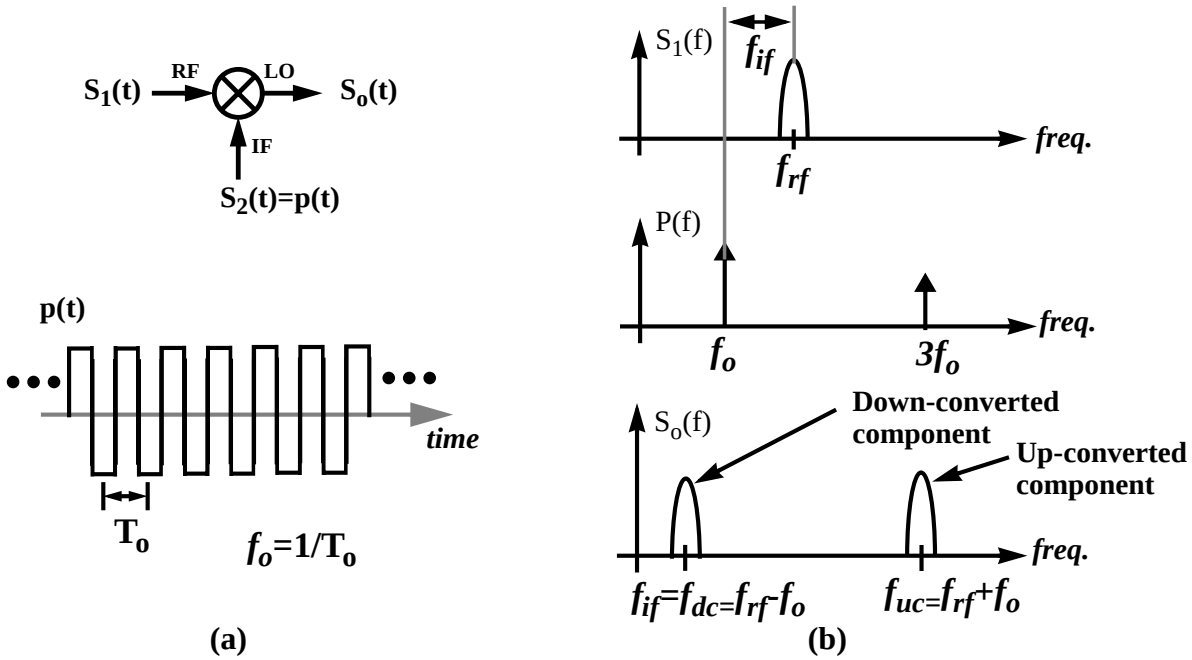


Figure 61. Operation of a simple switching mixer. (a) Switching mixer modeled in the time domain as a signal multiplied by an ideal pulse. (b) Frequency domain interpretation of various signals found at the input and output of an ideal switching mixer.

6.3 Passive vs. Active Mixers

With respect to circuit implementation, mixers can be separated into two basic classes, passive and active. As the name implies, passive mixers are realized with

components which do not dissipate standby power[1]. Most passive mixers are realized with a set of switches which are clocked by the local oscillator. This network of switches commutates the RF signal, effectively realizing a multiplication of the RF signal ,$S_1(t)$, (see figure 61), by ,p(t). In both Bipolar and MOS technologies, the switches are realized with NPN, PNP, NMOS, or PMOS transistors. Passive mixers typically commutate an input voltage from the input to the output. Unlike passive mixers, active mixers do utilize static current; thus, dissipating power. For both Bipolar and MOS active mixers, a transconductance stage is used at the mixer input to generate a current signal. This RF current signal is then passed through a network of switches which are driven by the local oscillator. The effect is again to multiply the current RF signal, S1(t), by the LO , p(t).

Passive mixers have the obvious advantage that they do not require static current with the expectation of the circuits which drive the mixer. However, without active current, the mixer will actually have a net loss in carrier power between the input and output. It will be shown in the next section, that theoretically a passive mixer can have a gain of no greater than $2/\pi$. The difficultly in realizing gain with a passive mixer, generally makes it challenging to maintain a low noise figure along the entire receive signal path. Because of the net attenuation between the mixer input and output, the linearity performance of passive mixers tends to be very good when implemented in most semiconductor technologies. However, in CMOS implementations of passive mixers, the linearity win isn't quite so clear as the switches themselves are effectively realized with a non-linear resistor. Although the passive mixer is commutating voltage, an ac current is required to pass through the switch to charge and discharge the capacitance on the other terminal of the switch. This ac current passes through the non-linear resistor resulting in a linearity degradation. Further design issue relates to the amplitude of the local oscillator which is require to drive the mixer. To ensure that the

1. The passive mixer by itself does not dissipate power. However, the circuits which drive the mixer LO and RF input ports will require power.

switch resistance is low, a large amplitude is require at the gates of the switches. Depending on the frequency of the local oscillator, this may be difficult to achieve without requiring a large amount of power from the LO driver. In CMOS, if the frequency of the local oscillator is high enough, an inductor may be used to resonant with the gate capacitance of the switches, this was shown in [6.9]. However, for some intermediate frequencies where on-chip resonance with a spiral inductor is difficult to achieve, generating a sufficient amplitude LO can be problematic. In the Wide-Band IF architecture which utilized an IF of 400 MHz, generating a large amplitude LO would require a considerable amount of power in the LO drivers.

Active mixers have the obvious advantage that signal gain may be achieved between the input and output of the mixer. With both more gain and a better control of the designated gain of the mixer, the noise figure of the entire receive signal path may be easily controlled. In addition, the voltage swing required to commutate the switches in an active mixer, usually a few hundred millivolts, is considerably less than what would be required by a passive mixer, typically more than a one volt. Therefore, the power required by the LO drives tends to be less. Although, an active mixer can provide signal gain which could be used to improve the receiver noise figure, the number of active components in the mixer itself is greater than a passive mixer. Therefore, there are actually more components within the mixer that generate noise. In particular, under certain blocking conditions noise can modulate in from the current bias and the switches may also contribute more noise when compared to the passive counterpart; particularly flicker noise.

Active mixers have one distinct advantage that there exists clear design trade-offs between gain, noise, linearity and power consumption. This makes the total design space somewhat more broad allowing flexibility in the higher level system design. This is particularly true from the perspective of allowing more controlled gain in the signal path. The rest of this chapter explores some of the characteristics of active CMOS

mixers with respect to gain, noise, and linearity. Some example designs of active mixers used by the Wide-Band IF receiver are provide at the end of this chapter.

6.4 Conversion Gain of an Active Gilbert-Cell-Like Mixers

Mixers are inherently operating as a non-linear circuit and the gain from the RF port to the IF port is called the conversion gain. The description of the mixer gain is somewhat unique compared to raw voltage gain in a linear amplifier. Here, the conversion gain of the signal gain from the input to the output of the mixer accounts for the frequency translation (or conversion in frequency) which takes place on the desired signal. Thus, the name “conversion gain”.

This section of chapter 6 will begin by providing an overview of the conversion gain of a completely idealized switching mixer. The derivation of the conversion gain for a simple mixer is then extended to the case of a CMOS current commutating mixer taking into account the finite time need for the CMOS switches to turn on and off. The results of this derivation will be useful for a later discussion on the overall noise performance of the active current commutating mixers. The reader can refer to the appendix for a more detailed derivation covering some of the equations presented in this section.

6.4.1 Switching Mixer Conversion Gain: Idealized Model

Virtually all switching mixers, or at least those considered in this thesis, commutate a signal applied to the mixer RF port shown in figure 61. Practically speaking, the signal applied to the RF port of the mixer is typically represented as a voltage or a current. Therefore, the mixers discussed in this thesis use a set of switches to commutate either the voltage or current signal represented at the RF port of the mixer. As alluded to before, the affect of commutating the input voltage or current can be modeled as an input signal $S_1(t)$ which is multiplied by an ideal periodic pulse. The

period or frequency of the pulse is controlled by the hardware (typically a frequency synthesizer) which is a part of the receiver.

The conversion gain of this idealized mixer may be found in the time domain, by multiplying each of the spectral components associated with the pulse by the input signal $S_1(t)$. Specifically, the pulse p(t) can be represented as a fourier series in the time domain. For simplicity $S_1(t)$ can be represented by a simple sinewave, where $S_1(t)=\cos(\omega_{rf}t)$. After multiplying $S_1(t)$ by p(t), the product resulting from the fundamental component of p(t) and $S_1(t)$ at the correct frequency, for a down converted component, can then be extract. The amplitude of the desired frequency component at the output of the mixer, can then be compared to the amplitude at the RF input of the mixer. Taking the ratio of the input amplitude to the amplitude of the desired mixer output spectral component will result in the conversion gain of an idealized switching mixer. A complete derivation associated with the conversion gain of a idealized switching mixer is given in appendix B and is highlight below.

First, the fourier series representation for a pulse p(t) is given by, ,

$$p(t) = \sum_{k=-\infty}^{+\infty} p_k e^{jk\omega_o t} \qquad \text{(Eq 6.1)}$$

The fourier coefficients for p(t) are given by,

$$p_k = \frac{1}{T_o}\int_{-\frac{T_o}{2}}^{\frac{T_o}{2}} p(t)e^{-jk\omega_n t}dt \qquad \text{(Eq 6.2)}$$

As shown in appendix B, the fourier series for an idea pulse with amplitude (+/-)1, given by equation 6.2, may be rewritten as,

$$p(t) = \frac{4}{k\pi}\sum_{k=1}^{\infty} \sin\left(\frac{k\pi}{2}\right)\cos(k\omega_o t) \qquad \text{(Eq 6.3)}$$

The signal at the output of the mixer can now be written as the product of,

$$S_o(t) = p(t)\cdot S_1(t) \qquad \text{(Eq 6.4)}$$

For $S_1(t)=\cos(\omega_{rf}t)$, the output signal can be described as,

$$S_o(t) = \left(\frac{4}{k\pi}\sum_{k=1}^{\infty}\sin\left(\frac{k\pi}{2}\right)\cos(k\omega_o t)\right)\cdot\cos(\omega_{rf}t) \qquad \text{(Eq 6.5)}$$

Where ωo represents the fundamental frequency of the oscillator. Expanding the result gives following form for $S_o(t)$.

$$S_o(t) = \frac{4}{\pi}\left(\frac{1}{2}[\cos((\omega_o-\omega_{rf})t)+\cos((\omega_o+\omega_{rf})t)]\right) \qquad \text{(Eq 6.6)}$$
$$-\frac{4}{3\pi}\left(\frac{1}{2}[\cos((3\omega_o-\omega_{rf})t)+\cos((3\omega_o+\omega_{rf})t)]\right)\ldots$$

For most communication transceiver applications, the important components of $S_o(t)$ result from the signal $S_1(t)$ being multiplied by the fundamental component of p(t). For receivers, the spectral component which contains (ω_o-ω_{rf}) is usually of interest. If we assume that there is an ideal brickwall filter at the output of the mixer, removing all of the components expect the one which contains (ω_o-ω_{rf}), then $S_o(t)$ can be written as,

$$S_o(t) = \frac{2}{\pi}\cos((\omega_o-\omega_{rf})t) \qquad \text{(Eq 6.7)}$$

The conversion gain of the mixer can be found be taking the ratio of the input signal amplitude at ω_{rf} to the amplitude of the signal found at (ω_o-ω_{rf}). Thus, the theoretical conversion gain of an ideal switching mixer is 2/π. For passive switching mixers, the name conversion *gain* is a bit of a misnomer as there is an inherent loss or attenuation, associated with the desired signal band passing from the input to the output. As we will see in the next section, conversion gain can be increased through the use of active components within the mixer, by adding gain either before or after the switches.

6.4.2 Conversion Gain for a Current Commutating Active Mixer

In the previous section, it was found that the conversion gain of an ideal switching mixer is 2/π, a result given in many previous publications [6.2][6.4][6.5][6.10]. In this section, a method to calculating the conversion gain of active current commutating CMOS mixers is derived.

All of the current commutating mixers discussed in this section, exhibit characteristics associated with multiplexing a desired signal by a set of switches. In most cases a voltage signal is applied to the input of the mixer, so a very high input impedance is desired. Figure 62 depicts a case where $V_{in}(t)/2$ is applied to each of a pair of transconductance stages to convert the input voltage signal to a current. This current signal is then fed through a set of double-pole, double-throw switches that are switching at the fundamental frequency of a local oscillator coming from either a clock generation or frequency synthesizer block. The current signal flows through two switches, then drives a load impedance or resistance as depicted in Figure 62.

To understand how to model the effect of the switches on the current or voltage input signal, it is useful to analyze the idealized mixer in figure 62, when the switches are set in one of the two states. First, assume the switches are set in each state for half the period of the local oscillator. Therefore, during one half of the local oscillator period, the switches will be set exactly as shown in figure 62. During this time, the mixer is operated as a resistively loaded amplifier whose voltage gain is given as $g_m R_{L.}$ When the switches move to the opposite setting during the remaining half of the local oscillator period, the gain from the input to the output of the mixer is $-g_m R_L$. Therefore, the overall circuit shown on the left of figure 62, can be simplified and modeled as shown on the right of the same figure. Essentially, the input signal $V_{in}(t)$ is attenuated

by a factor of 1/2, then applied to one of the multipliers two ports. The other signal

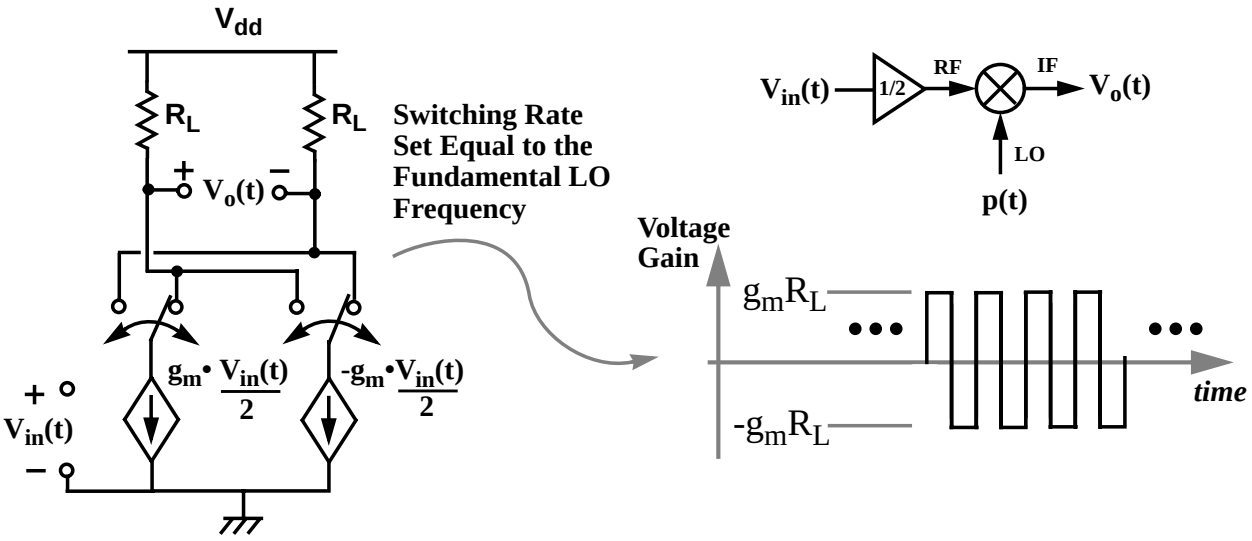


Figure 62. Conceptual schematic of a current commutating active mixer.

applied to the port of the multiplier, is again a periodic pulse with amplitude of +/- g_mR_L. Both the spectrum and the conversion gain of this mixer can be found using the identical approach given in section 6.4.1. This gives the same result for the conversion gain with the exception that the gain is scaled by g_mR_L of mixer.

$$A_{CG} = \frac{2}{\pi} g_m R_L \qquad \text{(Eq 6.8)}$$

A Bipolar implementation of a current commutating mixer is shown in figure 63(a) along with its corresponding CMOS implementation in (b). The circuit shown in figure 63(a) was reported as a four quadrant analog multiplier [6.8], and later became known as the “Gilbert Cell”. However, the original Gilbert Cell was proposed in 1968, as a four quadrant highly linear precision analog multiplier and not as a mixer. Therefore, when the circuit in figure 63(a) is used as a mixer, the term Gilbert Cell isn’t entirely accurate. By comparing the circuits of figure 63, with the circuit of figure 62, certain parallels in operation can be drawn. Because the circuit has a differential input, the input voltage $V_{in}(t)$ can be thought of as being divided by 2, as modeled by the attenuation of 0.5, shown in figure 62. Devices Q/M1 and Q/M2 are in the forward active/saturation region and act as a transconductance stage. The current signal at the

collector/drain of Q/M1 and Q/M2 are then applied to the emitter/source of a set of devices (Q/M3-Q/M6) which are over-driven to commutate the current signal from one set of differential outputs to the other. The circuit shown in figure 62, the pulse modulates the gain of the mixer from +/-$g_m R_L$ in exactly the same fashion as figure 63.

(Barrie Gilbert, JSSC Dec. 1968)

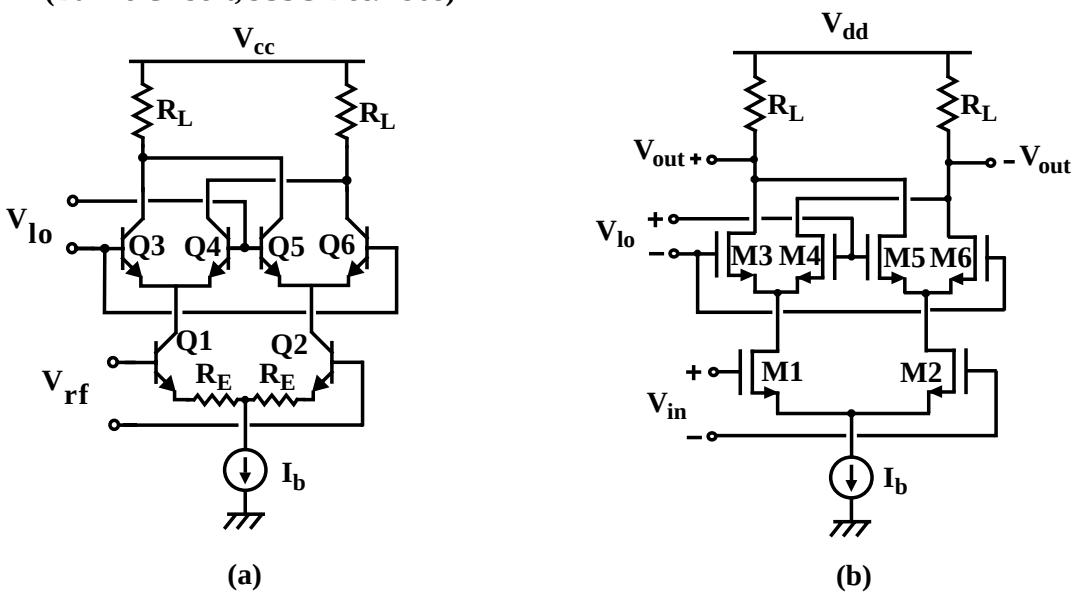


Figure 63. Current Commutating Mixers (a) Bipolar version, (b) Corresponding CMOS version.

In the ideal situation, the switches in both the Bipolar and CMOS mixers would change instantaneously. However, in reality, there will be a finite amount of time or non-negligible portion of the local oscillator period during which all of the switching devices conduct current. While all of the switches are conducting current the differential AC current signal at the output of the transconductance stage appears as a common mode signal at the output of the mixer; both positive and negative components of the current signal are added at the mixer output. This current sharing decreases the overall conversion gain of the mixer. Thus, reducing the percentage of the local oscillator period during which all of the switches are conducting current, increasing the mixer conversion gain.

To obtain a reasonable estimate of the conversion gain corresponding to the CMOS mixer in figure 63(b), a modification of the model given in figure 62 should be made. Specifically the waveform p(t) needs to be altered to account for the time that all of the switches are conducting current. The period of time during which all switches are on is referred to as the balanced state of the mixer. During the balanced state, the differential ac current applied to the switches appears as a common mode signal at the mixer output. Likewise, the period during which only two of the four switches (two devices among Q/M3, Q/M4, Q/M5, and Q/M6) are conducting current while the other two switches are in the cutoff region will be defined as the unbalanced state. While the mixer is in the unbalanced state, all of the ac current applied to the switches is differentially applied to the output load and the voltage gain of the RF input signal is instantaneously either $+/-g_mR_L$.

The periodic pulse p(t) used in the previous section to derive the conversion gain of an ideal mixer can be modified to more properly reflect what is happening in the actually implementation of a mixer circuit by taking into account the portion of the LO period during which the switches remain in the balanced state. A good approximation for p(t) while the switches are in the balanced state is to assume that the voltage transfer function follows a linear curve when moving from one unbalanced state, corresponding to when the instantaneous gain is $+g_mR_L$, to the alternate unbalanced state where the instantaneous mixer voltage gain is $-g_mR_L$. This is similar to the approach used in [6.2]. The modified waveform p(t) is shown in figure 64 where the times, T_1 and T_2 mark the instances when the switches move from an unbalanced state to a balanced state, or visa-versa. In other words, at times T_1 and T_2, the switches move from a point where current is conducted by all switches to a point where current is conducted by just two switches, or visa-versa. This leads to an easy characterization of the p(t) which will be useful in finding the conversion gain and the noise performance

of either a Bipolar or CMOS mixer with respect to device parameters such as bias currents and the V_{GS}-V_ts of the CMOS switches.

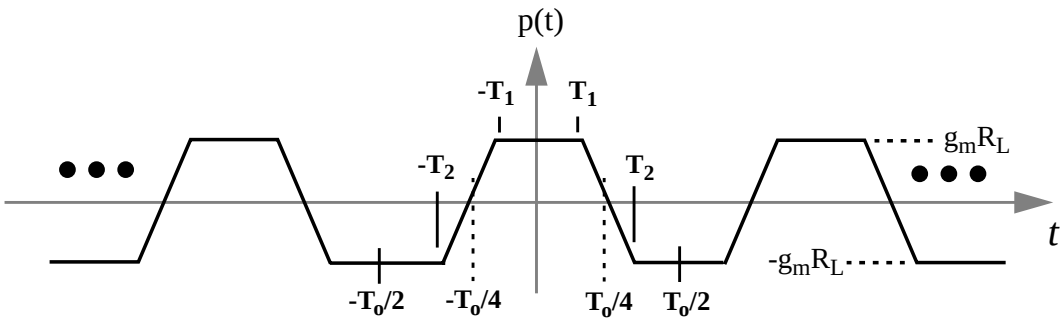


Figure 64. Pulse used to model the conversion gain and later the noise performance of a CMOS mixer.

Using the waveform p(t) shown in figure 64, the conversion gain of a CMOS mixer may be found using the i procedure outlined in section 6.4.1. First, p(t) is represented in the time domain by a fourier series. This requires finding the fourier coefficients corresponding to p(t) as shown in figure 64 so that p(t) may be represented by a fourier series. The derivation of the fourier series representation of p(t) is given in appendix C, the results of which are given below in equation 6.9.

$$p(t) = \frac{8g_mR_L}{x\pi^2}\sum_{(k=1)}^{\infty}\frac{1}{k^2}\left[\sin\left(\frac{k\pi}{2}\right)\sin\left(\frac{k\pi}{2}x\right)\right]\cdot\cos(k\omega_{LO}t) \qquad \text{(Eq 6.9)}$$

Here, the variable *x* is used to replace the variables T1 and T2. This is done by utilizing the fact that the mixers shown in figure 63, employ a doubly-balanced set of switches. Ignoring the effects of device mismatch, T_1 and T_2 are equally spaced in time from the point where zero differential voltage appears at the base/gates of the switches ($V_{LO}(t)=0$). This fact allows T_1 and T_2 to be defined with respect to the fundamental period of the local oscillator. This gives the following relationships between the variables *x*, T_1, T_2 and T_o,

$$T_1 = \frac{T_{LO}}{4} - x\frac{T_{LO}}{4} \qquad T_2 = \frac{T_{LO}}{4} + x\frac{T_{LO}}{4}$$

$$T_1 = \frac{T_{LO}}{4}(1-x) \qquad T_2 = \frac{T_{LO}}{4}(1+x)$$

$$T_2 - T_1 = 2\frac{T_{LO}}{4}x = x\frac{T_{LO}}{2}$$

Where T_o again is the period of the fundamental frequency. The value of *x* in terms of well known circuit parameters will be discussed later.

The relationship between the input and output voltage waveforms can simply be written as,

$$V_o(t) = p(t) \cdot V_{in}(t) \qquad \text{(Eq 6.10)}$$

Expressing $V_{in}(t)$ as $V_{in}(t)=\cos(\omega_{rf}t)$, $V_o(t)$ is,

$$V_o(t) = \left[\frac{8g_mR_L}{x\pi^2}\sum_{k=-\infty}^{\infty}\frac{1}{k^2}\left[\sin\left(\frac{k\pi}{2}\right)\sin\left(\frac{k\pi}{2}x\right)\right]\cdot\cos(k\omega_{LO}t)\right]\cdot\cos(\omega_{rf}t) \qquad \text{(Eq 6.11)}$$

The conversion gain can be extracted from equation 6.11 by finding the results of multiplying the input sinewave by the fundamental component of p(t), this is done by setting k=1.

$$V_o(t) = \frac{4g_mR_L}{x\pi^2}\sin\left(\frac{\pi}{2}x\right)[\cos((\omega_{RF}-\omega_{LO})t) + \cos((\omega_{RF}+\omega_{LO})t)] \qquad \text{(Eq 6.12)}$$

This result can be simplified into the following form, extracting the coefficient of the fundamental term associated with the down conversion of $V_{in}(t)=\cos(\omega_{rf}t)$ gives,

$$A_{CG} = \frac{4g_mR_L}{x\pi^2}\sin\left(\frac{\pi}{2}x\right) \qquad \text{(Eq 6.13)}$$

To confirm the accuracy of equation 6.13 a simple thought experiment can be performed. When the transition from the one peak value of the pulse to the opposite polarity occurs instantaneously, $T_1=T_2$ and x=0 and the waveform shown in figure 64, approaches the ideal squarewave. The conversion gain in this case should agree with the result obtained in section 6.4.1 for an ideal pulse modulated switching mixer. When *x* approaches zero, the approximation of $\sin(z) \approx z$ for small z may be used which gives.

$$A_{CG} = \frac{4g_mR_L}{x\pi^2}\sin\left(\frac{\pi}{2}x\right)\Bigg|_{x\to 0} = \frac{2g_mR_L}{\pi} \qquad \text{(Eq 6.14)}$$

Removing the g_mR_L component associated with the voltage in the active mixers shown in figure 63, gives the identical result for the conversion gain of an ideal switching mixer or $(2/\pi)$.

6.4.2.1 Transition time Definition for CMOS Current Switching Mixers

As will be shown later, equation 6.11 can be extremely useful for not only finding the conversion gain of an active mixer, but also to evaluate the noise contribution from the transconductance stage (the input devices). Equation 6.11 was written with respect to a variable *x* which was used to simplify some of the math required to obtain the fourier series representation of p(t). Now, it will be useful to define *x* with respect to common values used to determine when a set of CMOS switches transitions from conducting current down both legs, to a point where one device is on while the other is in the off state, or in other words a time when the switching devices move from the balanced to the unbalanced state.

The situation where the devices move from the balanced to unbalanced state is illustrated in figure 65. Again restricting ourselves to doubly-balanced mixer, when the differential local oscillator goes through the zero crossing, the four switches act as two source coupled pairs as shown in figure 65(a). As mentioned before the desired AC current shown as +/- $g_m(V_{RF}/2)$ cancels when summed at the output, in turn degrading the conversion gain. Likewise, when the amplitude of the local oscillator is sufficiently large, two of the four devices will turn off, and all of the desired AC current is passed to the output. This is shown as the unbalanced state in figure 65(b), This also, corresponds to the time when the instantaneous mixer gain will either be g_mR_L or $-g_mR_L$.

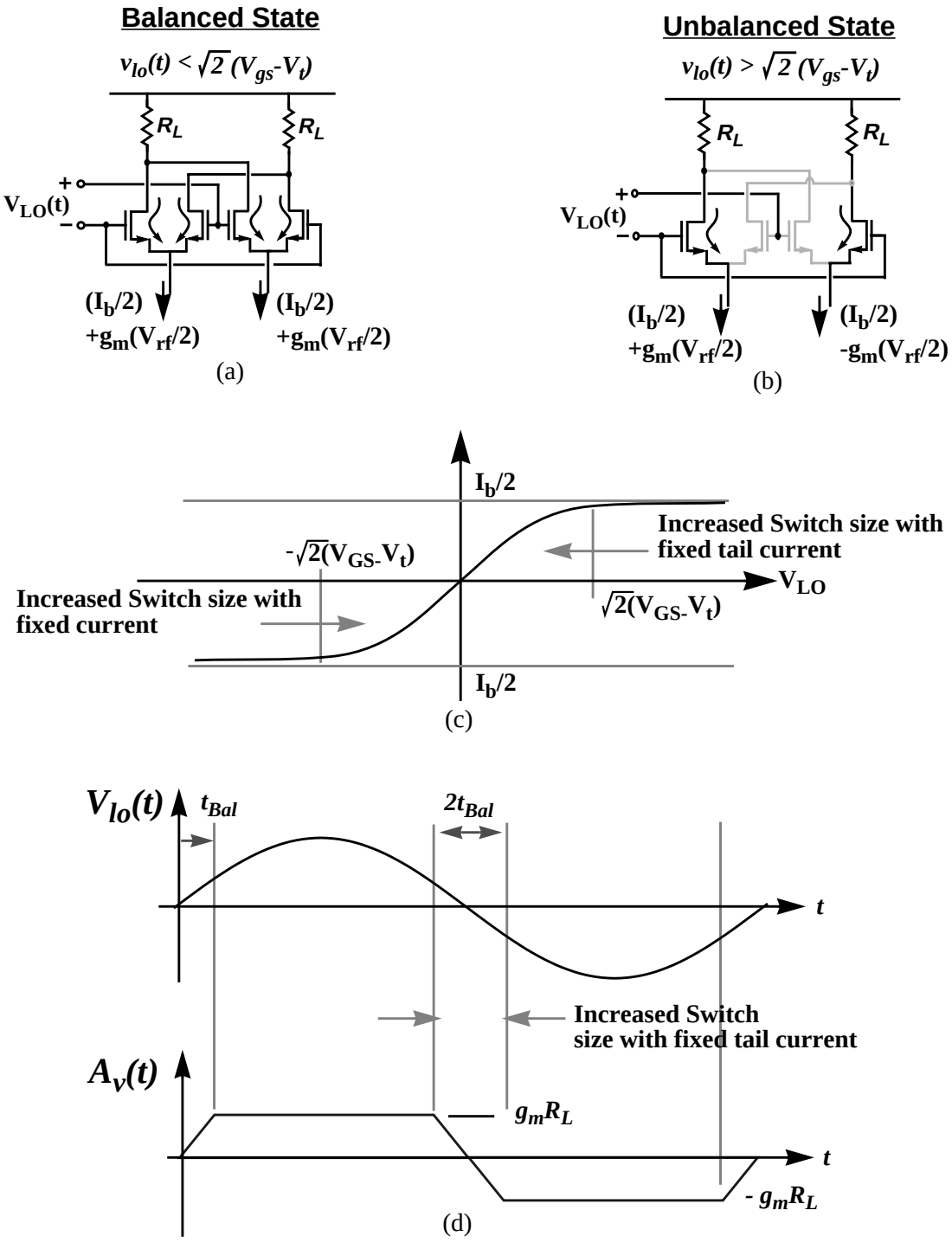


Figure 65. Mixer switch transition from the balanced state to the unbalanced state. (a) current conducted through the switches in the balanced state. (b) Current conduction through switches in the unbalanced state. (c) Differential current at the output of one set of differential switches (d) Relationship between the local oscillator amplitude and the mixer instantaneous voltage gain.

It is useful to evaluate with respect to time, when the switches of a current commutating CMOS mixer transition from the balanced state to the unbalanced state. Specifically, it is helpful to determine this time as a function of the V_{GS}-V_t of the switches as well as with respect to the amplitude and frequency of the local oscillator which is applied to the gates of the mixer switches. The time at which the switches actually transition from balanced to the unbalanced state will be defined as t_{bal}. Assume, that the local oscillator which is applied to the mixer inputs can be described by $V_{LO}(t)=V_{LO}\sin(\omega_{LO}t)$, where V_{LO} is the amplitude and ω_{LO} is the frequency of oscillation. Two of the four switches can be viewed as a source coupled pair. In this context, assuming square law devices, if the differential gate voltage becomes greater than $\sqrt{2}(V_{gs}-Vt)_{sw}$, then one device will be conducting all of the tail current while the other device goes into the cut-off region [6.11]. Using this information, one can write directly that,

$$V_{LO}(t_{bal}) = V_{LO}\sin(\omega_{LO}t) = \sqrt{2}(V_{gs}-Vt) \qquad \text{(Eq 6.15)}$$

Again, using the approximation that for small z, $\sin(z)\approx z$, t_{bal} can be solved directly from equation 6.15.

$$t_{bal} = \frac{\sqrt{2}(V_{GS}-V_t)_{sw}}{V_{LO}\omega_{LO}} \qquad \text{(Eq 6.16)}$$

Writing with respect to the period gives,

$$t_{bal} = \frac{\sqrt{2}(V_{GS}-V_t)_{sw}T_{LO}}{2V_{LO}\pi} \qquad \text{(Eq 6.17)}$$

Now from both figure 64 and figure 65, it can be seen that T_1, T_2 and t_{bal} are related such that T_2-T_1=2•t_{bal}

$$T_2 - T_1 = x\frac{T_{LO}}{2} = 2\cdot t_{bal} \qquad \text{(Eq 6.18)}$$

The variable *x* can now be solved with respect to t_{bal} and the fundamental period of the local oscillator or,

$$x = \frac{4\cdot t_{bal}}{T_{LO}} \qquad \text{(Eq 6.19)}$$

Combining equation 6.16 and equation 6.19, *x* can be now written as,

$$x = \frac{2\sqrt{2}(V_{gs} - V_t)_{sw}}{V_{LO}\pi} \quad \text{(Eq 6.20)}$$

Substituting in the value for *x* that was determined from the previous result into equation 6.13, to find the conversion gain of a CMOS current commutating mixer gives,

$$A_{CG} = \frac{\sqrt{2}(g_m R_L)V_{LO}}{(V_{gs} - V_t)_{sw}\pi}\sin\left(\frac{\sqrt{2}(V_{gs} - V_t)_{sw}}{V_{LO}}\right) \quad \text{(Eq 6.21)}$$

Any expression can be substituted in for the value of g_m to properly reflect the transconductance of the input pair, this can also include modifying g_m to reflect possible degeneration. A useful form of equation 6.21 is to utilize the following long channel expression for g_m in terms of the $(V_{gs}\text{-}V_t)_{in}$ of the input pair and tail bias current where $g_m=2I_d/(V_{gs}\text{-}V_t)_{in}$. I_d is given as the drain bias current and $V_{gs}\text{-}V_t$ is the V_{dsat} of each input device. I_d can also be expressed as half the tail current or $I_d=I_b/2$. This results in $g_m=I_b/(V_{gs}\text{-}V_t)_{in}$. Substituting the previous expression for g_m into equation 6.21 gives,

$$A_{CG} = \frac{\sqrt{2}I_b R_L V_{LO}}{(V_{gs} - V_t)_{in}(V_{gs} - V_t)_{sw}\pi}\sin\left(\frac{\sqrt{2}(V_{gs} - V_t)_{sw}}{V_{LO}}\right) \quad \text{(Eq 6.22)}$$

This equation is intuitively pleasing, as it gives the mixer conversion gain as a function of the $(V_{gs} - V_t)$ of both the input devices and switches as well as the amplitude of the local oscillator, the tail bias current I_b, and the load resistance. In this current commutating mixer, there are several tools available to the designer to increase the overall conversion gain of the mixer. The most interesting, and probably the most obvious is the relationship between the amplitude of the local oscillator (V_{LO}) relative to the nominal $V_{gs}\text{-}V_t$ of the switches. As we increase the size of the switches while holding the tail bias current constant will result in a reduction of the $V_{gs}\text{-}V_t$ of these devices, in turn reducing the differential voltage necessary to completely shut off one set of switches. Thus, reducing the value of t_{bal} or the time it takes for the switches to turn off. This is illustrated in figure 65(c) and (d), for a switch that is increased in size while the tail bias current remains constant. Alternatively, the switching time, t_{bal}, can be reduced by increasing the amplitude of the local oscillator V_{LO} relative to the $V_{gs}\text{-}V_t$

of the switches. This relationship also comes from equation 6.22. Some of the more obvious ways of increasing the conversion gain involve increasing the g_m of the input devices which may be done by decreasing the V_{gs}-V_t of the mixer input devices. However, as will be shown later, decreasing the input device V_{dsat} is done at the expense of reducing the mixer linearity performance. Likewise, the tail bias current can be increased to improve the input device g_m, however care must be taken as this will increase the switch V_{gs}-V_t when device size remains constant. A clear trade-off exists between the static power consumption of the mixer and the conversion gain. If the tail current is increased to improve gain, this has the obvious affect of increasing the mixer power consumption. However, to maintain the overdrive of the switches ($(V_{gs}-V_t)_{sw}/V_{LO}$), when increasing the mixer tail current, requires increasing the size of the switches. A larger switch size will increase the capacitance looking into the LO port of the mixer, requiring a higher power consumption of the LO buffers which drive the mixer. The method of quadrature generation and buffering are discussed in chapter 7.

The result given in equation 6.14 is intuitively practical since as the ratio of $(V_{gs}-V_t)_{sw}/V_{LO}$ goes to zero, the switches take a negligible amount of time to switch from one terminal to the other (of course this assumes the switches have infinite bandwidth), thus, driving t_{bal} to zero. In this case, the conversion gain, similar to what was shown in equation 6.14, approaches the ideal conversion gain for a switching mixer of $2/\pi$.

Shown in figure 66, is a plot of the voltage conversion gain of a current commutating mixer as a function of the LO overdrive, $V_{LO}/(V_{gs}-V_t)_{sw}$, predicted by

equation 6.21. The g_mR_L product is 6. Note, as the LO overdrive increases beyond a ratio of 2 the conversion gain begins to level off.

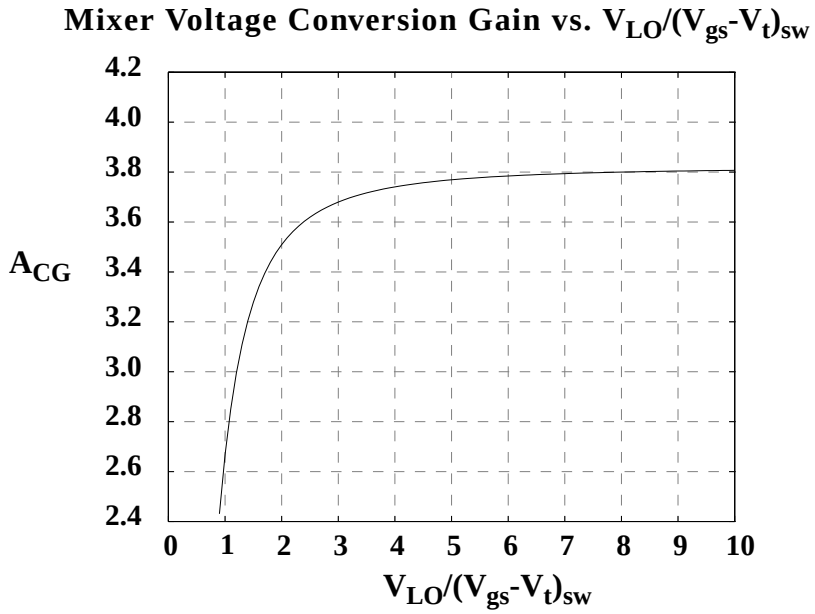


Figure 66. Conversion gain of CMOS current commutating mixer vs. $V_{LO}/(V_{gs}-V_t)_{sw}$. $g_mR_L = 6$

6.5 Mixer Noise Analysis

A natural extension to a discussion of mixer conversion gain is an analysis of the noise performance of current commutating mixers. Unlike much of the noise analysis which is carried out for lower frequency and baseband circuits , mixers as well as many RF circuits are highly non-linear. In the case of mixers, this is necessary to enable frequency translation of a desired signal. Although the non-linearity associated with mixers makes the noise analysis cumbersome, design guidelines for current commutating mixers with respect to the noise performance will be developed.

Before beginning a discussion on the noise performance of a mixer, it is particularly useful to understand the differences between a single-sideband noise figure or noise source as compared to a double-sideband noise figure or noise source. This concept has a special significance when describing the noise performance of various

mixers used by the image-rejection configuration used in the experimental prototype receivers discussed later.

6.5.1 Single-Sideband and Double-Sideband Noise

A considerable amount of confusion arises when referring to either the single sideband noise figure (SSB) or double-sideband noise figure (DSB) of either the entire receiver or an individual component along the chain. The most convenient method of determining which classification (SSB or DSB) should be used is to understand the band in which the desired signal lies, both before and after frequency translation. As was shown in previous chapters on the discussion of image-rejection, there are actually two bands which are frequency translated by a mixer block, both the desired band on one side of the local oscillator and the corresponding image-band which lies in the alternate lower sideband of the mixer. Both the upper and lower sidebands about the local oscillator are frequency translated to the same intermediate frequency. The trick to determine whether a noise source is single or double-sidebanded is to look at both how the noise and the desired signal band are being frequency translated. A more through explanation with a few examples follows.

Assume for the moment, that there is some desired spectrum which is received and lies in the frequency band above the frequency of the local oscillator used by the mixer. Further assume that one wishes to down convert the desired signal from the carrier frequency to some intermediate frequency, this situation is illustrated in figure 67. As mentioned before in several discussions, the desired signal, which in the case of figure 67, lies in the upper sideband of the mixer, is frequency translated to an intermediate frequency at the output of the mixer. Likewise, the noise in the same band is frequency translated to the same IF. The noise in the image-band is also frequency translated to the same intermediate frequency. Thus, although the noise is translated from both the upper and lower sidebands of the mixer, the desired signal is only coming

from one or a *single* sideband about the LO mixer input. Therefore, convention is to define the noise source at the input of the mixer as single-sidebanded, and the to describe the noise figure which is calculated, measured or quoted as a *single*-sideband noise figure. This definition can apply to either a single component in a receiver chain or to the entire receive path. Virtually any heterodyne receiver architecture which produces a non-zero intermediate frequency should be described in terms of a single-sideband noise figure as again, the noise is translated from both the upper and lower sidebands about the mixer while the desired signal only resides in one sideband about the mixer. Likewise, a low IF receiver architecture would as will be described by a SSB noise figure for the reasons described above.

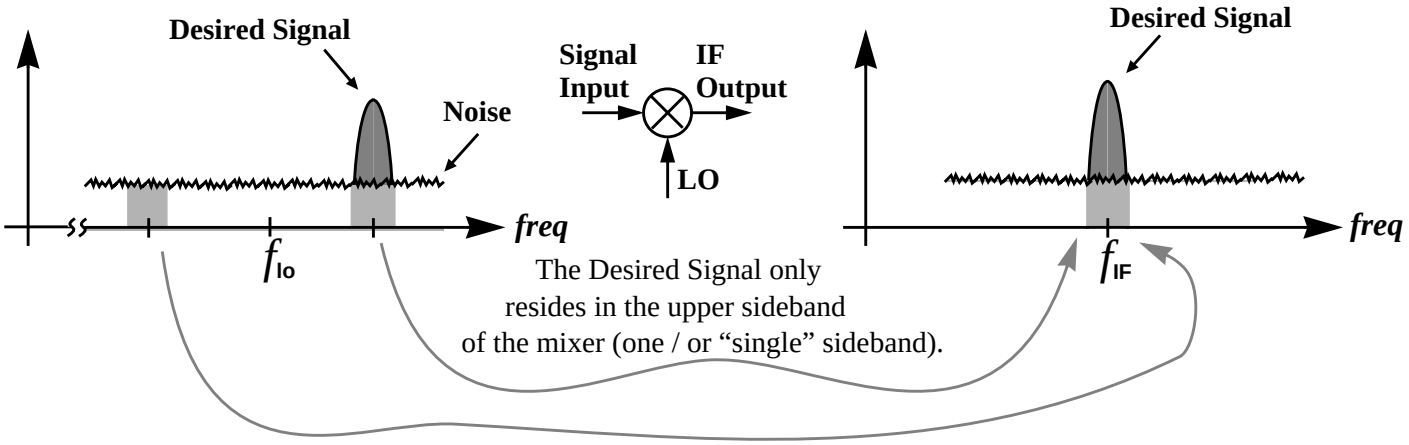
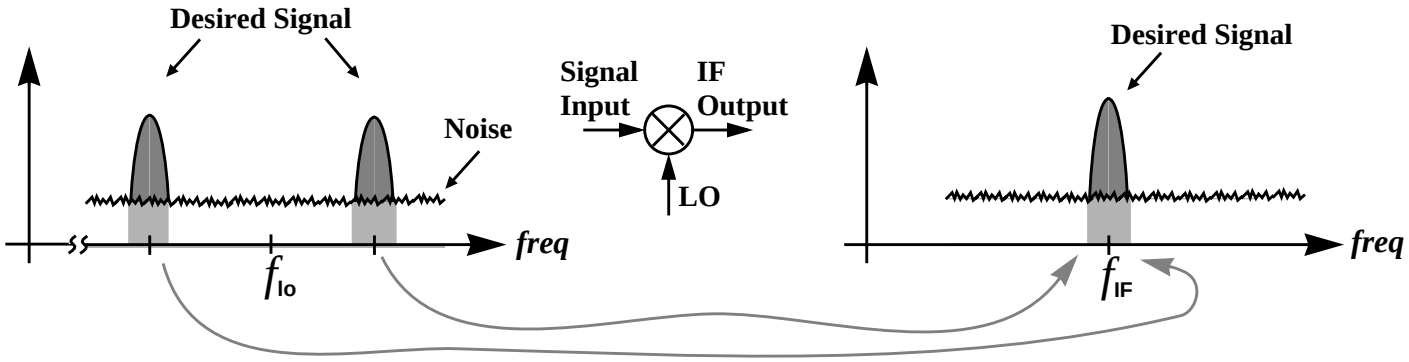


Figure 67. Simple example of double-sideband mixing and noise figure.

The other common description for the way noise folds into the desired signal band is the characterization of a double-sideband noise source or noise figure. Assume for the sake of argument that there are two identical bands which are received from above and below the frequency of the first local oscillator, i.e. both bands are 100% correlated. This unique and hypothetical case is shown in figure 68 where both the bands above and below the frequency f_{lo} are the same signal. If the frequency of the local oscillator (f_{lo}) is tuned to a frequency which is precisely between both of the received bands, then both of the bands which lie in the upper and lower sideband of the mixer will frequency translate to the same intermediate frequency. Assuming that the

local oscillator is accurate enough, both of the desired bands will add constructively at the output of the mixer. Likewise, the noise is again frequency translated from both the upper and lower sidebands about the mixer. However, unlike the single-sideband case, the desired signal is coming from both sidebands about the mixer, so that the two sidebands about the mixer add to *double* the signal energy that is translated by the single-sideband mixing operation. Thus, in this situation the noise source and the noise figure are said to be double-sidebanded (DSB) about the mixer. The noise figure which would be used to characterize either the block or the receive chain which frequency translates a signal residing in both sidebands about the mixer LO input, is referred to as the double-sideband noise figure. The situation shown in figure 68, is somewhat



Desired signal is present in both upper and lower sidebands of the mixer.
Therefore, double sideband noise figure should be used.

Figure 68. Simple example of double-sideband mixing and noise figure.

unrealistic and rarely occurs in practical applications. However, any component or receiver chain which in either one or multiple steps, frequency translates a desired band to a zero IF is virtually always described by a double-sideband noise figure. Both the mixers and the receiver of a direct conversion system would be characterized by either DSB noise sources and/or DSB noise figure. The direct conversion situation is illustrated in figure 69 where the local oscillator that is applied to the LO port of the mixer is tuned to exactly the center of the desired signal band. Therefore, the desired band which is frequency translated to a zero-IF, lies in the mixer's upper and lower

sideband. Thus, direct conversion systems are characterized with double-sideband noise figures.

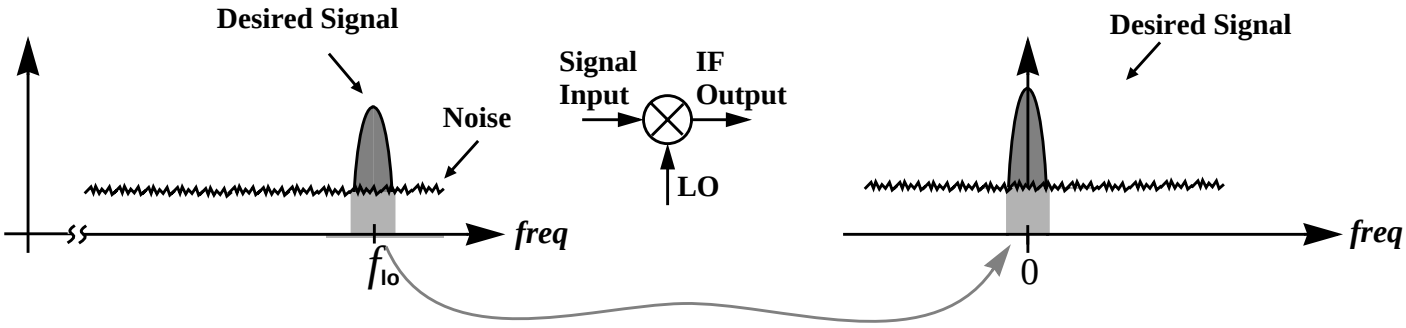


Figure 69. Translation of both the desired signal band and noise in direct translation of the carrier frequency to a zero-IF.

It might seem unusual to spend a significant amount of text describing in detail the differences between a double-sideband and single-sideband noise figure. However, the weaver mixer which was implemented in the wide-band IF double conversion receiver presents some interesting examples of the concepts surrounding SSB and DSB systems/components. Because the overall receiver is effectively performing a direct frequency conversion of the carrier from RF to baseband, albeit in two steps, the entire receiver system is characterized with a DSB noise figure measurement. However, it is interesting to note that some of the individual components used in the image-rejection mixer are actually characterized by single-sideband noise sources. Specifically, the first set of mixers which are running off of the first local oscillator would be described by a single-sideband noise figure. However, the mixers running off of the second local oscillator are defined by a double-sideband noise figure. As will be seen in the next section, a further refining of the image-rejection mixer's noise sources reveals that the only components along the entire receiver signal path which contribute noise in a single-sideband fashion are the devices associated with both the switches and the transconductance stage of the RF-IF mixers running off of LO1. All other noise sources fold into the desired signal band in a double-sideband fashion. At first glance it would appear that the noise contribution from the LNA would frequency translate to the IF

from both the upper and lower portions of the RF-IF mixers sidebands. However, the noise spectrum from the LNA falling within the image-band is actually cancelled to first order by the image-rejection mixer itself. Thus, the LNA contributes noise from one sideband.

6.5.2 Noise Analysis of a Current Commutating Mixer

Building on some of the concepts discussed in the previous two sections, the following is provided to highlight the approach to analyzing noise in current commutating CMOS active mixers. This analysis for the Gilbert Cell like circuit topology can essentially be broken down into three separate categories; the noise contribution from the transconductance stage, noise from the switches and the noise from load resistance (this is either thermal noise from resistors and or as will be illustrated later noise from active current source loads at the mixer output). Similar to the expression derived for the conversion gain, the emphasis will be on developing intuitive design relationships that can demonstrate certain trends with respect to device sizes which can be used during the development of this class of mixer. The discussion will begin with a look at the noise contribution from the transconductance stage. In addition, the convention for the noise sources discussed in this section are to reflect all of them to the mixer input, the noise is then defined with respect to a fictitious equivalent input noise resistance. This is done for convenience to allow for an easy reflection of the noise to the receiver input, where the noise may be compared to that produced by the available noise power produced by the receiver source resistance.

6.5.2.1 Transconductance Stage

As alluded to before, the expression for the conversion gain given in section 6.4.2 will prove to be useful when attempting to find the noise performance of these types of CMOS mixers. Specifically, Equation 6.9 will be useful to find the noise contribution of the transconductance stage. The noise contribution from the input pair

can be viewed as a set of source coupled devices which contribute both thermal noise and produce flicker noise. The noise then passes through the switches which frequency translates the noise power spectrum from the input devices. The noise which is produced passes through a transfer function which is periodic and the noise spectrum which appears at the output of the mixer, due to the input device noise contribution, is a cyclostationary random process described by the following expression.

$$v_{out}(t) = p(t) \cdot v_{in}(t) \qquad \text{(Eq 6.23)}$$

The overall mechanism of a white noise source which is passed through a periodic transfer function has the effect of folding several copies of the white noise spectrum in the frequency domain of the desired signal. This situation is highlighted in figure 70, where the white noise spectrum produced by the input devices actually convolves with all of the harmonics produced by the local oscillator, in turn dropping

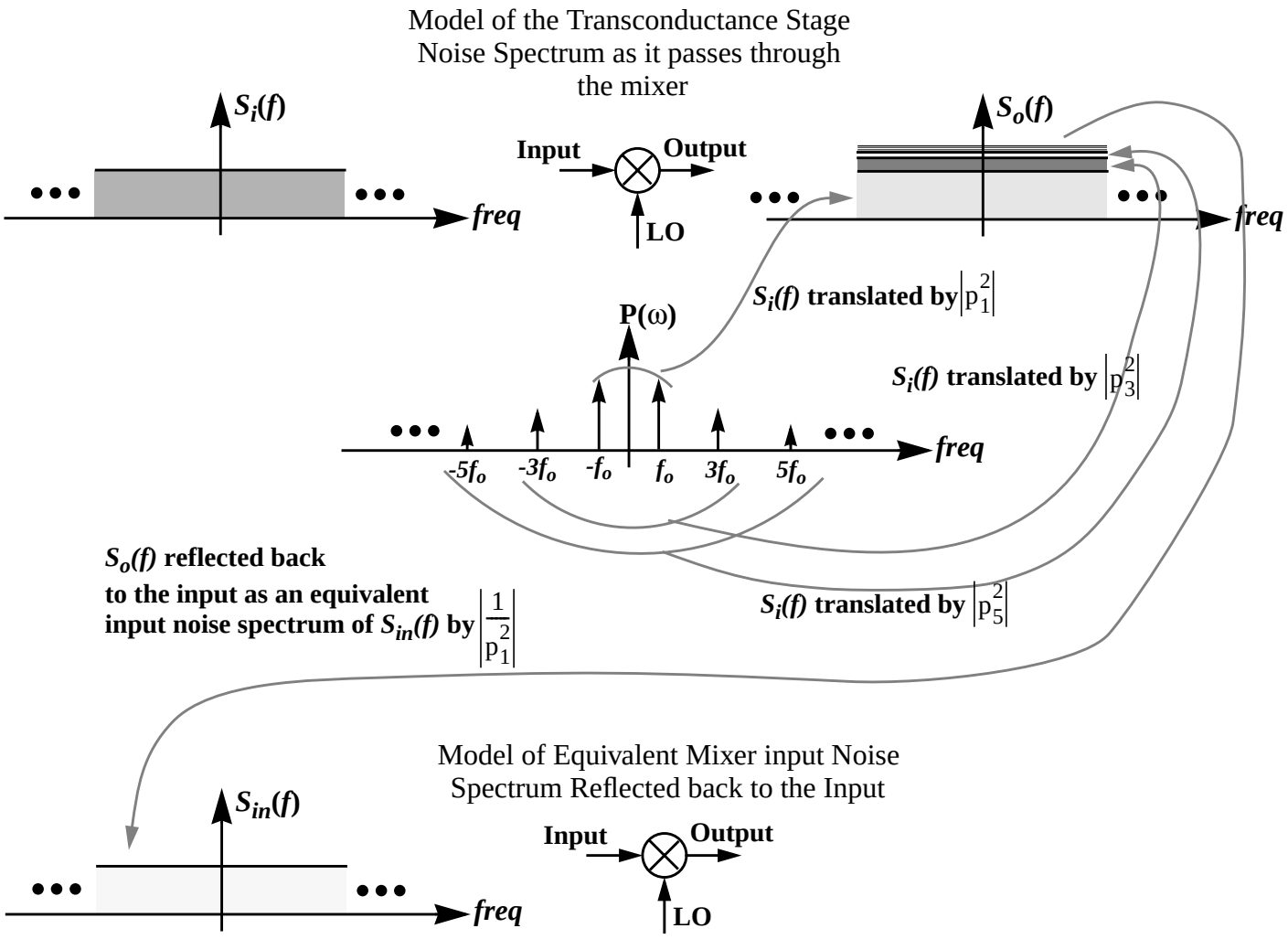


Figure 70. Noise moving from the transconductance stage to the output of the mixer. The output noise is then reflected back to the input as an equivalent input noise source.

several copies of the folded spectrum at the output of the mixer. This is the primary reason why mixers have a tendency to be extremely noisy.

The noise transfer function is computed by frequency domain techniques. Remembering that multiplication in the time domain is equivalent to convolution in the frequency domain. Therefore, the expression given in equation 6.23 can be written in the frequency domain as,

$$S_o(\omega) = \frac{1}{2\pi}(|P(\omega)|^2 \otimes S_i(\omega)) \quad \text{(Eq 6.24)}$$

Where P(ω) represents the fourier transform of the pulse p(t). Because the pulse p(t) is periodic, the fourier transform of P(ω) will be a summation of discrete Dirac delta functions in the frequency domain. Thus, intuitively the input noise produced by $S_i(\omega)$ is convolved with the discrete points associated with P(ω). This is the inherent process by which numerous copies of $S_i(\omega)$ (assuming $S_i(\omega)$ is white) are folded over in the frequency domain producing a summation of $S_i(\omega)$ with the discrete Dirac-delta functions associated with P(ω). To find the power spectral density of this cyclostationary random process can be found for $S_o(\omega)$. Mathematically, the time average of this periodic spectral density at the output can be expressed as was given in [6.2].

$$S_o(f) = \sum_{k=1}^{\infty} |p_k|^2 \cdot S_i(f - k f_{LO}) \quad \text{(Eq 6.25)}$$

This is done by extracting the energy of p(t) over one period of the LO along with using Parseval's relationship [6.12].

$$\frac{1}{T_{LO}} \int_0^{T_{LO}} (p(t))^2 dt = \sum_{k=-\infty}^{\infty} |p_k|^2 \quad \text{(Eq 6.26)}$$

Where p_k are the fourier coefficients associated with the fourier series calculation performed earlier on p(t). Equation 6.25 can be used to find the contribution of various noise components due to the harmonics associated with p(t). Assuming the noise is white, the copies of $S_i(f)$ can be represented as a constant or as will be seen later, the thermal noise contribution from the input device channel and gate resistance can be expressed as 4kTR. Therefore, $S_i(f - k f_{LO})$ can be replaced with V_n^2 which is the equivalent input noise source at the input of the transconductance stage giving,

$$S_o(f) = V^2_n \sum_{k=1}^{\infty} |p_k|^2 \quad \text{(Eq 6.27)}$$

The expression in equation 6.27 assumes infinite bandwidth for the switches. However, in reality there is a finite limitation to the speed of the switches which will dictate how many harmonics associated with p_k that must be calculated. In addition, what is of ultimate interest in the design of all mixers used by the wide-band IF receiver

is the equivalent input noise spectrum or the equivalent input noise resistance. Therefore, the expression given in equation 6.27 must be divided by the fundamental transfer function of p(t) which is nothing more than the conversion gain of the mixer. Therefore, what is of interest is the input referred version of equation 6.27 which can be written as,

$$S_{in}(f) = \frac{V^2_n}{|p_1|^2} \sum_{k=1}^{\infty} |p_k|^2 \qquad \text{(Eq 6.28)}$$

This is a rather useful form for the equivalent input referred noise contribution due to the transconductance stage. This form reveals that the equivalent input noise source can be expressed as V_n^2 commonly associated with a CMOS differential pair, multiplied by a constant which takes into account the folding of noise from the transconductance stage as it passes through the switches to the output of the mixer. Therefore, equation 6.28 can be rewritten as,

$$S_{in}(f) = V^2_n \sum_{k=1}^{\infty} \left|\frac{p_k}{p_1}\right|^2 = V^2_n \cdot \zeta \qquad \text{(Eq 6.29)}$$

Where ζ is the constant that corrects for the action of the switches folding in noise from the input to the output, this constant is similar to the α factor which is given in [6.2]. This is a convenient form for the input referred noise, and the output referred noise may be obtained by multiplying by the squared version of the expression given for the conversion gain in equation 6.22.

$$S_o(f) = V^2_n \cdot \zeta \cdot (A_{CG})^2 \qquad \text{(Eq 6.30)}$$

Next, it is of interest to evaluate the value of ζ as it relates to the CMOS mixer in figure 63. Using the expression obtained for p_k which is derived in appendix C, ζ can be written as,

$$\zeta = \sum_{k=1}^{\infty} \left|\frac{p_k}{p_1}\right|^2 = \sum_{k=1}^{\infty} \left(\frac{\left(\frac{1}{k^2}\right)\sin\left(\frac{k\pi}{2}\right)\sin\left(\frac{k\pi}{2}x\right)}{\sin\left(\frac{\pi}{2}x\right)} \right)^2 \qquad \text{(Eq 6.31)}$$

Substituting in previously determined values for *x*, equation 6.31 can be written as,

$$\zeta = \sum_{k=1}^{\infty} \left(\frac{\left(\frac{1}{k^2}\right)\sin\left(\frac{k\pi}{2}\right)\sin\left(\frac{k\sqrt{2}(V_{gs}-V_t)_{sw}}{V_{LO}}\right)}{\sin\left(\frac{\sqrt{2}(V_{gs}-V_t)_{sw}}{V_{LO}}\right)} \right)^2 \qquad \text{(Eq 6.32)}$$

This gives an interesting result, as the value of ζ is only influenced by the ratio of $V_{LO}/(V_{gs}-V_t)_{sw}$ and the number of harmonics which are actually passed to the output. The number of harmonics which should be summed is related to the frequency of the local oscillator and the overall bandwidth of the switches. For example, if the LO is running at 500MHz, and the bandwidth of the switches is 3GHz, then k should only be summed to the first 2.5GHz/500MHz or 5 harmonics in this case, therefore, the value of ζ would be summed from k=1 to 5. Figure 71 is a plot of various values of ζ for different values of overdrive as well as a several curves summing k to a finite value.

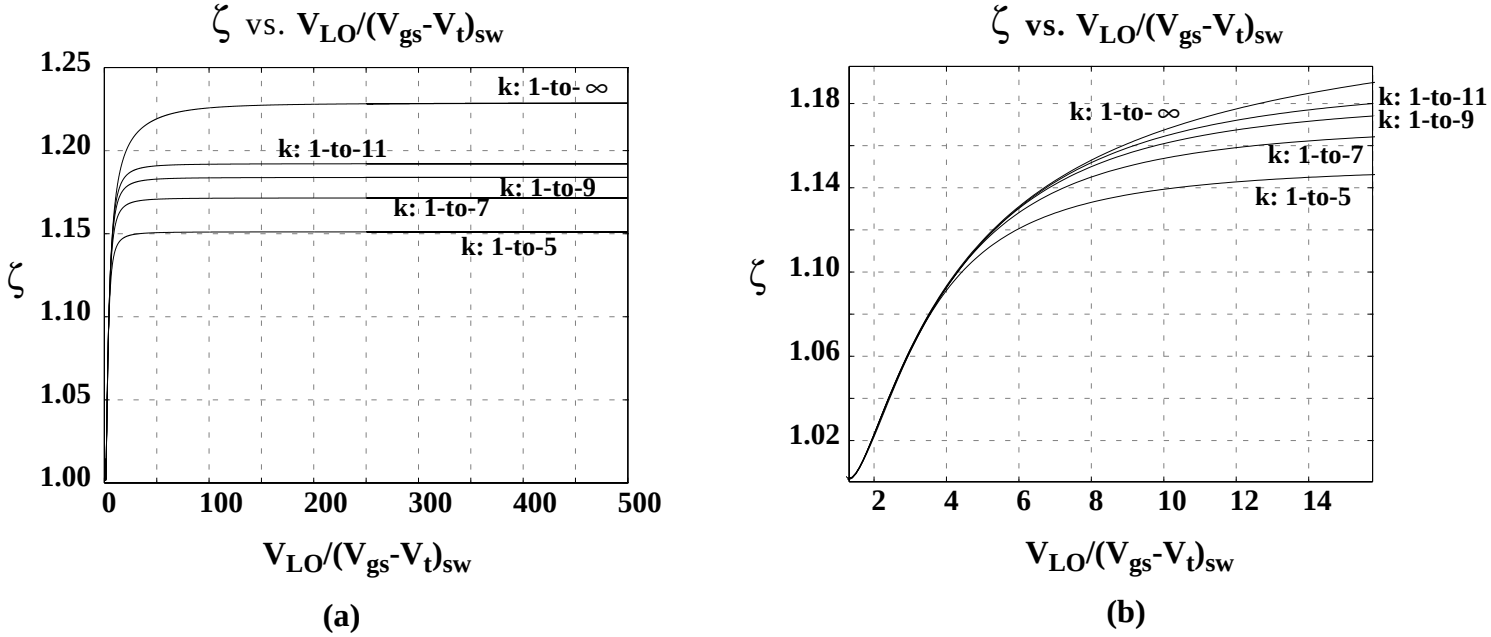


Figure 71. Plotted values of ζ as a function of $V_{LO}/(V_{gs}-V_t)$. Each curve represents a different number of harmonics which are summed in equation 6.31. (a) Illustrates ζ as p(t) approaches an ideal squarewave which is identical to $V_{LO}/(V_{gs}-V_t)$. (b) ζ for more practical values of $V_{LO}/(V_{gs}-V_t)$ which would be used by the current commutating mixer.

With a proper value of ζ the input referred noise contribution from the transconductance stage can be expressed by utilizing equation 6.29 with the correct expression for the input referred noise of a single CMOS device. Here, there is the thermal noise contribution from the channel resistance as well as the gate resistance r_g. An additional contribution to the noise produced by the transconductance stage is the source resistance from the previous stage, in this case the LNA. Overall, the total input referred noise contribution from the transconductance stage can be expressed as,

$$\overline{V_{in}^2}/(\text{Hz}) = \zeta \cdot 4kT\left(R_s + m \cdot 2\left(r_g + \gamma\frac{1}{g_m}\right)\right) \qquad m = 1, 2 \qquad \text{(Eq 6.33)}$$

Expressing equation 6.33 in the format of an equivalent input noise resistance, as is used to evaluate the overall receiver described in chapter 2 gives,

$$R_{g_m} = \zeta \cdot \left(R_s + m \cdot 2\left(r_g + \gamma\frac{1}{g_m}\right)\right) \qquad m = 1, 2 \qquad \text{(Eq 6.34)}$$

The factor *m* is an integer which is either set to 1 or 2 depending on whether the mixer is mixing noise in single-sideband or double sideband. *m* should be set to one if the down conversion mixer directly frequency translates the incoming signal to baseband or DC; again, this would be the situation when a double sideband noise figure is necessary. Likewise, if the mixer is frequency translating the incoming carrier to an IF, then a single-sideband noise figure is used and the noise from the transconductance stage is folded in from two sets of bands. In this case, *m* would be set to 2. For the Wide-band IF receiver discussed in chapter 3, the mixers running off of LO1 would have *m* set to 2, while the mixers utilizing LO2 would have *m* set to 1 in equation 6.34.

A considerable amount of effort can be placed on finding the exact value of ζ in equation 6.34 as a function of $(V_{gs}\text{-}V_t)_{sw}$. However, the maximum noise contribution from the transconductance stage will occur when the amplitude of the LO is much greater than $(V_{gs}\text{-}V_t)_{sw}$. In this case, p(t) approaches the ideal square wave and there is a maximum contribution of white noise power due to frequency translation from the harmonics of p(t). The values of ζ for large $V_{LO}/(V_{gs}\text{-}V_t)_{sw}$ are plotted in figure 71(a). Here, it can be seen, that assuming switches with an infinite bandwidth (summing all

values of k to infinity) and a very large $V_{LO}/(V_{gs}-V_t)_{sw}$ (ideal square wave p(t)) the value of ζ in the worst case is 1.2. Therefore, to determine quickly the noise contribution from the transconductance stage of a gilbert cell like mixer, the conventional noise source of a single device, due to a source coupled pair can be referred to the input and multiplied by 1.2. Practically speaking, $V_{LO}/(V_{gs}-V_t)_{sw}$ will be between 2 and 10 for most mixer designs. Thus, the additional noise contribution due to the harmonics of the switches mixing noise inband will lie between 6 and 15 percent. A few examples designs of current commutating mixers are presented at the end of this chapter along with a discussion of the ratio of V_{LO} to $(V_{gs}-V_t)_{sw}$ and with the corresponding ζ values.

6.5.2.2 Switch Noise

As was shown in the previous section, the equivalent input noise contribution from the transconductance stage is a somewhat weak function of the $V_{LO}/(V_{gs}-V_t)_{sw}$ when the LO voltage is much great then the V_{dsat}s of the switches. Conversely, the equivalent input noise contribution from the switches is a stronger function of the ratio $V_{LO}/(V_{gs}-V_t)_{sw}$ as will be seen in this section. The approach to finding the equivalent input noise contribution from the switches is similar to what was done for the transconductance stage. Again, a time varying transfer function was found from the switch input noise source to the output and then this noise spectrum was reflected back to the RF input port of the mixer. Following the approach for the transconductance stage, the noise from the switches is written in terms of an equivalent input noise resistance with a correction factor that takes into account the folding of the white noise spectrum as the noise passes through the switches.

The noise model which was used for the switches is highlighted in figure 72. Here, the equivalent input noise of all four of the switches are referred to the gates of at the input of the LO port as, $\overline{V}_{sw}$, where,

$$\overline{V^2}_{sw}/(Hz) = 4kT\left(R_{LO} + 4\left(r_g + \gamma\left(\frac{1}{g_{msw}}\right)\right)\right) \quad \text{(Eq 6.35)}$$

The input referred noise at the gate of the switches then passes through the time varying transfer function s(t) which models the voltage transfer function between the LO port to the output of the mixer. It is interesting to note that the switches will only produce noise at the output of the mixer when the mixer is in the balanced state. This corresponds to the time when the LO signal passes through the differential zero crossing. While in the unbalanced state, the switches which are in the saturation region, can be thought of as a cascode device relative to the source coupled input pair (transconductance stage). Similar to any cascode device, the noise contribution is often negligible (this isn't always true for some high frequency circuits) and will be ignored for the purposes of this analysis.

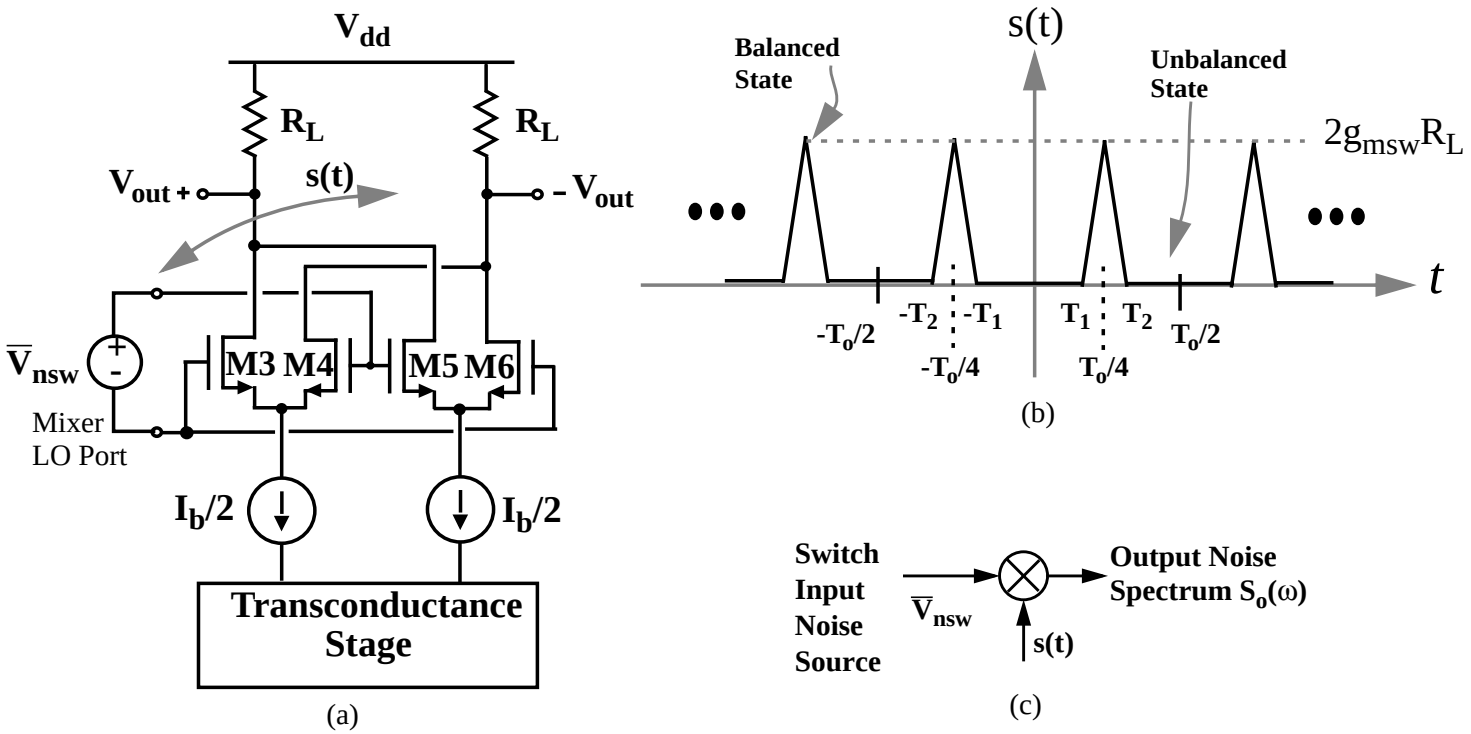


Figure 72. Model used to find the noise contribution from the switches. (a) Device input noise sources applied to the LO port of the mixer; transfer function to the output through the time varying transfer function s(t). (b) Voltage transfer function from the LO port to the mixer output, s(t). (c) Model of the noise from the switches as it passes to the

The waveform to model s(t) is shown in figure 72(b) and assumes the transfer function from the LO port to the mixer output rises linearly from the time the switches move from the unbalanced state (only two of the four devices are turned on) in to the balanced state (time when all four devices are conducting current). The voltage transfer function continues to rise and will peak at the time when the differential LO voltage is zero, this corresponds to the time when all four switches are ideally conducting an identical amount of current. At the peak of s(t), (again, when all devices are conducting equal current) the voltage transfer function from the LO port to the output of the mixer is $2g_{msw}R_L$, where g_{msw} is the transconductance associated with one of the four switches and the factor of 2 is used because the differential equivalent half circuit will have two switches between the LO port and the mixer output. In reality, the transfer function s(t) does not rise or fall linearly and can be expressed as function of time as given in [6.2].

However, by making the assumption that the transfer function s(t) is linear in the balanced state considerably simplifies the calculation of the fourier coefficients of s(t) without deviating significantly from the expected expression for s(t). In reality s(t) can be closely approximate as linear in the balanced state with minimal error from the real transfer function.

The mixer *output* noise contribution from the switches averaged over one period of the local oscillator in an identical approach, as was used to find the output referred noise of the transconductance stage in the previous section. The output referred noise due to the switches can be expressed as,

$$S_o(f) = \sum_{k=1}^{\infty} |s_k|^2 \cdot S_i(f - k f_{LO}) \qquad \text{(Eq 6.36)}$$

Where s_k are the fourier coefficients of s(t) and $S_i(f - k f_{LO})$ can be expressed as the white noise spectrum V_{nsw}/(Hz). Equation 6.36 reduces to.

$$S_o(f) = \overline{V^2}_{sw} \sum_{k=1}^{\infty} |s_k|^2 \qquad \text{(Eq 6.37)}$$

Remembering that the goal in this analysis is to reflect the output noise spectrum to the input of the mixer, and represent all of the noise sources within the mixer as an equivalent input noise resistance. Reflecting the output noise back to the input gives

$$S_{in}(f) = V^2_{nsw} \sum_{k=1}^{\infty} \left| \frac{s_k}{A_{cg}} \right|^2 = V^2_{nsw} \cdot \beta \qquad \text{(Eq 6.38)}$$

Here, β represents the amount by which the switch input noise is attenuated from the LO port to the input of the mixer. Similar to the variable ζ, β is mainly dependent on the ratio of LO amplitude to the $(V_{gs}-V_t)$ of the switches. Unlike the input referred noise from the transconductance stage, the switch noise contribution will decrease as the amount of overdrive of the mixer switches is increased (ratio of $V_{LO}/(V_{gs}-V_t)$ increases). This is expected as the switches are contributing most of the noise as the LO passes through the differential zero crossing when the mixer enters the balanced state. The value of Beta can be expressed as,

$$\beta = \sum_{k=1}^{\infty} \left| \frac{S_k}{A_{cg}} \right|^2 \qquad \text{(Eq 6.39)}$$

The fourier coefficients for s(t) are found in appendix D and repeated below.

$$s_k = (2g_{msw}R_L)\frac{4}{x}\left[\frac{\cos\left(k\frac{\pi}{2}\right)}{(k\pi)^2}\left(1 - \cos\left(\frac{k\pi}{2}x\right)\right)\right] \qquad \text{(Eq 6.40)}$$

The sum of the fourier coefficients can be expressed as,

$$\sum_{k=-\infty}^{\infty} |s_k| = (2g_{msw}R_L)\left|\frac{x}{2}\right| + (2g_{msw}R_L)\sum_{k=1}^{\infty}\left|\frac{8}{x}\frac{\cos\left(k\frac{\pi}{2}\right)}{(k\pi)^2}\left(1 - \cos\left(\frac{k\pi}{2}x\right)\right)\right| \qquad \text{(Eq 6.41)}$$

Dividing by the expression given for the conversion gain given in equation 6.13 gives,

$$\sum_{k=-\infty}^{\infty}\frac{|s_k|}{|A_{CG}|} = \frac{(2g_{msw}R_L)\left|\frac{x}{2}\right|}{\frac{4g_{mIN}R_L}{x\pi^2}\sin\left(\frac{\pi}{2}x\right)} + \frac{(2g_{msw}R_L)}{\frac{4g_{mIN}R_L}{x\pi^2}\sin\left(\frac{\pi}{2}x\right)}\sum_{k=1}^{\infty}\left|\frac{8}{x}\frac{\cos\left(k\frac{\pi}{2}\right)}{(k\pi)^2}\left(1 - \cos\left(\frac{k\pi}{2}x\right)\right)\right| \qquad \text{(Eq 6.42)}$$

Remembering that beta is the ratio of the fourier coefficients to the mixer conversion gain gives.

$$\beta = \sum_{k=-\infty}^{\infty} \frac{|s_k|^2}{|A_{CG}|^2} \qquad \text{(Eq 6.43)}$$

Substituting in the value for *x* as well as squaring the numerator and denominator of equation 6.42 an expression for β can be obtained with respect to the amplitude of the local oscillator V_{LO}, the $(V_{gs}-V_t)$ of both the switches and the input devices.

$$\beta = \sum_{k=-\infty}^{\infty} \frac{|s_k|^2}{|A_{CG}|^2} = \left| \frac{(V_{gs}-V_t)_{in}}{2(V_{gs}-V_t)_{sw}} \left(\frac{(V_{gs}-V_t)_{sw}}{V_{LO}} \right)^2 \frac{1}{\sin\left(\sqrt{2} \frac{(V_{gs}-V_t)_{sw}}{V_{LO}} \right)} \right|^2 + \qquad \text{(Eq 6.44)}$$

$$\sum_{k=1}^{\infty} \left| \frac{(V_{gs}-V_t)_{in}}{(V_{gs}-V_t)_{sw}} \frac{\cos\left(\frac{k\pi}{2}\right)}{k^2} \left(1 - \cos\left(k\sqrt{2} \frac{(V_{gs}-V_t)_{sw}}{V_{LO}} \right) \right) \frac{1}{\sin\left(\sqrt{2} \frac{(V_{gs}-V_t)_{sw}}{V_{LO}} \right)} \right|^2$$

The total input referred noise from the switches can now be expressed as an equivalent

$$R_{eq(sw)} = \beta\left(R_{LO} + 4\left(r_g + \gamma\left(\frac{1}{g_{msw}} \right) \right) \right) \qquad \text{(Eq 6.45)}$$

Several values of β are plotted in figure 73(a) summed for different several values of k. Most of the energy in s(t) is represented in the first few values of k, thus, there is negligible difference between 5 harmonics summed verses β summed from k=1 to infinity. Shown in figure 73(b) is a plot of β and ζ verses $V_{LO}/(V_{gs}-V_t)_{sw}$. Here, it is interesting to note that the value of β quickly roles off as the amplitude of the LO voltage is increased above the $(V_{gs}-V_t)$ switches. This can be explained intuitively. For lower ratios of $V_{LO}/(V_{gs}-V_t)_{sw}$ the switches are actually adding noise to the mixer for a greater percentage of time per period of the local oscillator. In addition, for a low $V_{LO}/(V_{gs}-V_t)_{sw}$, the noise from the switches reflected to the mixer input is actually being exacerbated by the loss in conversion gain from the lack of LO overdrive. A weaker dependence of ζ on $V_{LO}/(V_{gs}-V_t)_{sw}$ relates to the fact that as the LO voltage significantly increases such that the conversion gain of the mixer approaches an ideal pulse, the extra noise added from all of the

harmonics of p(t) only introduces an additional 22% noise compared to the noise relating from the fundamental. The strong dependence of the switch noise on $V_{LO}/(V_{gs}-V_t)_{sw}$ can also be explained by observing equation 6.44.

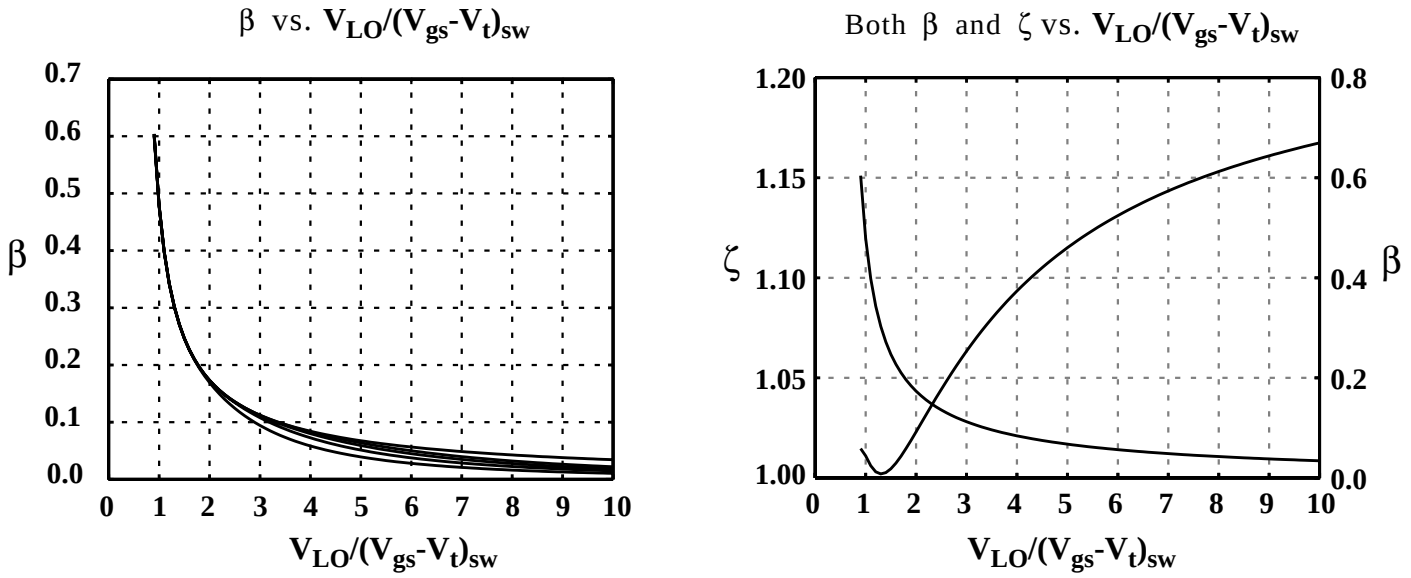


Figure 73. (a) Values of β plotted as a function of the ratio of $V_{LO}/(V_{gs}-V_t)_{sw}$ summed up to several values of k (b) Plot of both β and ζ verses $V_{LO}/(V_{gs}-V_t)_{sw}$.

6.5.2.3 Load Resistance Noise

The load resistance at the output of a CMOS Gilbert cell like mixer is the last component which contributes a significant amount of noise. The task of referring the load noise to the input is considerably more straight forward then referring the noise from either the switches or the transconductance stage. The ease of computing the input referred noise from the load devices really relates to the fact that these noise sources are not passing through the switches, therefore, the noise spectrum is not folding in the frequency domain. Stated differently, the white noise produced by the load devices is not frequency translated, making the computation of the input referred noise rather easy. The equivalent mixer input noise contribution from the load devices can be referred from the output to the input by simply dividing by the conversion gain of the mixer.

$$R_{in(load)} = \frac{R_{L(total)}}{(A_{CG})^2} \qquad \text{(Eq 6.46)}$$

The value of the load resistance is dependent on the particular implementation of the mixer. As will be seen later in this chapter, many of the mixers implemented for the experimental receiver realized for the DECT and GSM standards were done so using active current source outputs as shown in figure 74, along with PMOS triode region load resistors in a common mode feedback loop. The PMOS current source devices in figure 74, can potential be the dominant source of noise at the output of the mixer. Therefore, properly referring the noise generated by the current source devices at the output, to the input is crucial. Assuming the resistance of R_L is significantly less than the output impedance of the current source, the noise due to both the load resistance and the current source devices in figure 74, can be expressed as,

$$R_{in(load)} = 2\left(\frac{R_L + R_{CS}}{(A_{CG})^2}\right) \qquad \text{(Eq 6.47)}$$

This expression can be rewritten as,

$$R_{in(load)} = 2\left(\frac{R_L}{A_{CG}}\right)^2\left(\frac{1}{R_L} + \gamma\frac{I_b}{(V_{gs} - V_t)_{cs}}\right) \qquad \text{(Eq 6.48)}$$

Where $(V_{gs}\text{-}V_t)_{cs}$ is the V_{dsat} of the load current source devices while I_b is the mixer tail bias current. The second term in equation 6.48 can be further refined to get a relationship between the bias current and the relative V_{dsats} of the input devices as well as the switches and the current source.

(Eq 6.49)

$$R_{in(load)} = 2\left(\frac{R_L}{A_{CG}}\right)^2\left(\frac{1}{R_L} + \gamma\frac{1}{2I_b(V_{gs} - V_t)_{cs}}\left(\frac{(V_{cs} - V_t)_{in}(V_{gs} - V_t)_{sw}\pi}{R_L V_{LO}}\right)^2 \sin\left(\frac{\sqrt{2}(V_{gs} - V_t)_{sw}}{V_{LO}}\right)^2\right)$$

From equation 6.49 the relationship between the mixer bias current and the $(V_{gs}\text{-}V_t)_{cs}$ of the PMOS current source may be observed. Here the trade-off is clear between the current source noise contribution and the output swing of the mixer. The $(V_{gs}\text{-}V_t)_{cs}$ of the current should be increased as much as possible while still allowing a

desired mixer output swing. Thus, the design trade-off becomes available mixer output swing verses the noise contribution from the active current source loads.

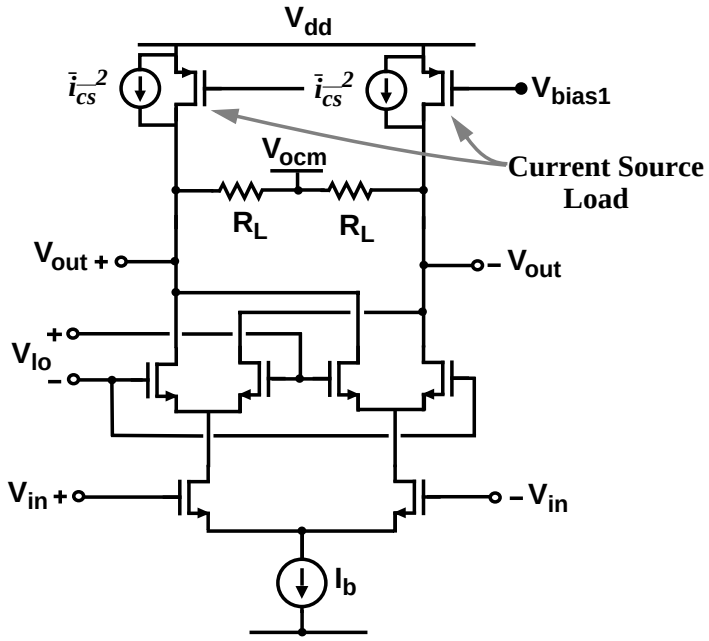


Figure 74. Noise emanating from all the output noise sources in an actively load current commutating mixer.

6.5.2.4 Total Mixer Input Referred Noise

With a description of the noise contribution from the mixer load devices referred to the input, a complete picture can now be developed for the overall mixer performance. By combining equations (Eq 6.34), (Eq 6.45), and (Eq 6.47) the following total equivalent input noise resistance of the entire mixer may be obtained.

(Eq 6.50)

$$R_{eq(total)}=\zeta\cdot\left(R_s+m\cdot 2\left(r_g+\gamma\frac{1}{g_m}\right)\right)+\beta\left(R_{LO}+4\left(r_g+\gamma\left(\frac{1}{g_{msw}}\right)\right)\right)+$$
$$2\left(\frac{R_L}{A_{CG}}\right)^2\left(\frac{1}{R_L}+\gamma\frac{I_b}{(V_{gs}-V_t)_{cs}}\right)$$

An example implementation of one mixer and the associated noise sources referred to the input and plotted as a function of $V_{LO}/(V_{gs}-V_t)_{sw}$ is shown in figure 75.

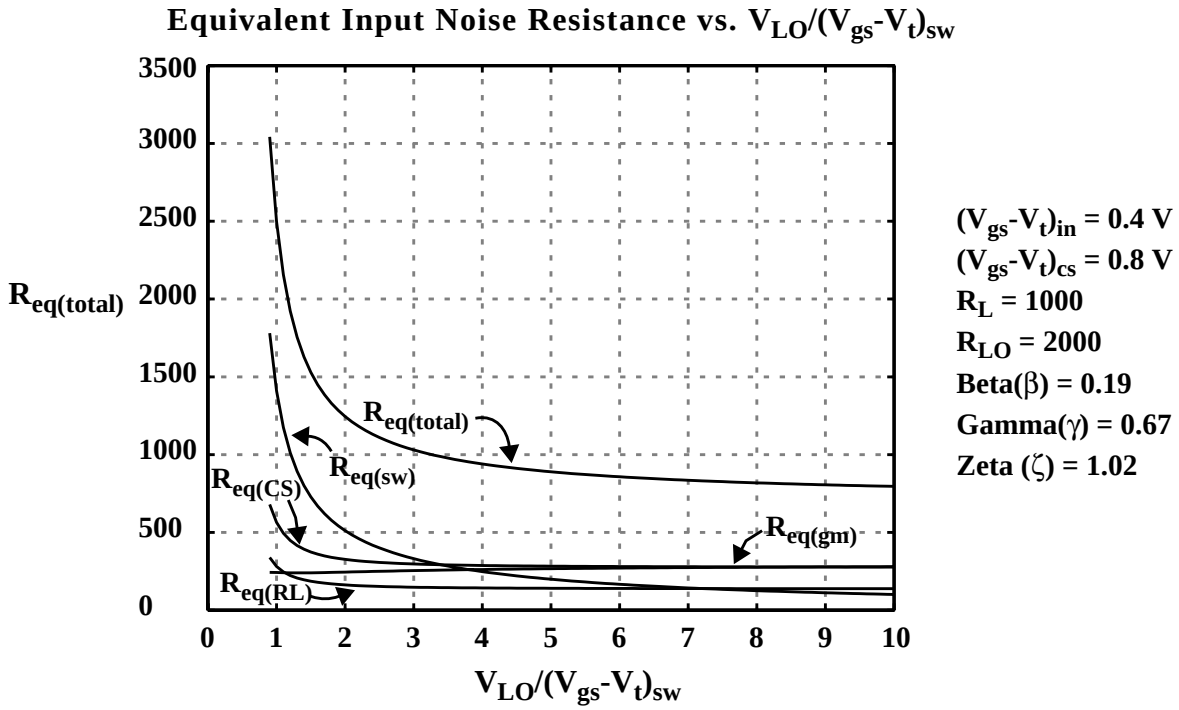


Figure 75. The total equivalent input noise resistance ($R_{eq(total)}$), as well as the individual input referred contributions from the transconductance stage ($R_{eq(gm)}$), the switches ($R_{eq(sw)}$), the load resistance R_L ($R_{eq(RL)}$), and finally the noise generated by an active current source load ($R_{eq(CS)}$).

The total equivalent input noise resistance is plotted as $R_{eq(total)}$ and described by equation 6.50. Each of the individual noise contributions referred to the input from the transconductance, the switches as well as the load resistance and current source are plotted as $R_{eq(gm)}$, $R_{eq(sw)}$, $R_{eq(RL)}$ and $R_{eq(CS)}$ respectively. As expected the equivalent input noise resistance due to the transconductance stage increases slightly as the LO overdrive is increased. The increase $R_{eq(gm)}$ with a higher overdrive relates to the fact that p(t) approaches an ideal squarewave and noise is folded over from the harmonics of p(t). However, the maximum increase in noise from the transconductance stage mixing with the harmonics has an upper bound of an additional 22%. In contrast, the switches, as well as all of the noise sources at the mixer output contribute the maximum amount

of noise for a low LO overdrive. There exists a heavier dependence of the noise contribution from the switches and the load on the amount of LO overdrive, because as the $V_{LO}/(V_{gs}-V_t)$ drops, so does the conversion gain Thus the input referred noise begins to rise significantly. In the case of the switches, the percentage of time per period that the switches add noise actually increases with a lower $V_{LO}/(V_{gs}-V_t)$ in addition to a reduction in the conversion gain. For lower values of $V_{LO}/(V_{gs}-V_t)$, the switch noise will actually dominant the overall mixer noise performance. Thus, the need to ensure that the mixer is supplied with a local oscillator which has sufficient amplitude to provide enough LO overdrive to the switches is critical.

6.6 Distortion in an Active Current Commutating Mixers

In addition to the conversion gain and mixer noise performance, the other key description of mixers for receiver applications is usually the linearity performance. The linearity of a mixer will determine how well this component can reject signals found in alternate bands which ultimately will impact the overall selectivity performance of the receiver. Because the mixers which are discussed in this section, are all differential, the second order non-linearity will tend to cancel typically making the second order intermodulation distortion negligible compared to the mixer noise floor or other sources of interference. Although, virtually all even order distortion has a tendency to be negligible for differential circuit topologies, the odd order harmonics can potential lead to a greater source of interference to the desired signal band. In particular, the third order intermodulation distortion of a single component or an entire channel can greatly influence the overall receiver's selectivity performance.

The nature of interference arising from the third order intermodulation can be understood by first looking at some of the basic issues associated with the linearity of a circuit component. In most baseband circuit applications, linear circuit analysis is assumed as this tends to be an accurate description of the needed circuit performance.

In addition, most baseband circuits are running at a low enough frequency that feedback is usually applied to linearize the circuit. However, receiver front-end components such as the LNA and mixer are typically running at too high a frequency to allow the use of feedback to linearize the circuit. Therefore, these circuits are run open loop and the non-linear nature of certain circuit elements such as junction capacitance and non-linear channel resistance will add higher order terms to the current or voltage transfer function. Thus, the relationship between the input and output signal will have the following general form [6.13].

$$S_o = a_1 S_i + a_2 S_i^2 + a_3 S_i^3 + a_4 S_i^4 \ldots \quad \text{(Eq 6.51)}$$

Where the output signal S_o is related to the input signal S_i by a high order transfer function, where a_1, a_2, a_3, etc. are the coefficients of each order of the transfer function. The particular problem related to the third order transfer function may be understood by representing the input signal, S_i, as a pair sinusoidal tones with amplitude S1 and S2 running at a set of separate but closely spaced frequencies, ω_1 and ω_2.

$$S_i = S_1 \cos(\omega_1 t) + S_2 \cos(\omega_2 t) \quad \text{(Eq 6.52)}$$

Passing the above signal through the third order term in equation 6.51 results in,

$$\begin{aligned} a_3 S_i^3 = {} & \frac{a_3 S_1^3}{4}(\cos(3\omega_1 t) + 3\cos(\omega_1 t)) + \frac{a_3 S_2^3}{4}(\cos(3\omega_2 t) + 3\cos(\omega_2 t)) + \\ & \frac{3}{4} a_3 S_1 S_2^2 [2\cos(\omega_1 t) + \cos((2\omega_2 - \omega_1)t) + \cos((2\omega_2 + \omega_1)t)] \\ & + \frac{3}{4} a_3 S_1^2 S_2 [2\cos(\omega_2 t) + \cos((2\omega_1 - \omega_2)t) + \cos((2\omega_2 + \omega_1)t)] \end{aligned} \quad \text{(Eq 6.53)}$$

Of most interest in equation 6.53 are the terms which result in a spectral component at $2\omega_2$-ω_1, $2\omega_2$+ω_1, $2\omega_1$-ω_2, and $2\omega_2$+ω_1. These spectral components which arise from a third order non-linearity are of particular concern in radio receiver applications as the situation may arise where there are two alternate band users, very close in frequency to the receiver's desired channel, may be present. If the alternate

band signals happen to lie at frequencies ω_2 and ω_1, while the desired signal band to receive resides at either $2\omega_2$-ω_1, $2\omega_2$+ω_1, $2\omega_1$-ω_2, and $2\omega_2$+ω_1, $2\omega_2$-ω_1. If this situation occurs, as it sometimes does, the spectral components generated from the alternate band signals passing through either the mixer or receivers third order non-linearity will actually appear as interference in the desired signal band, this is illustrated in figure 76.

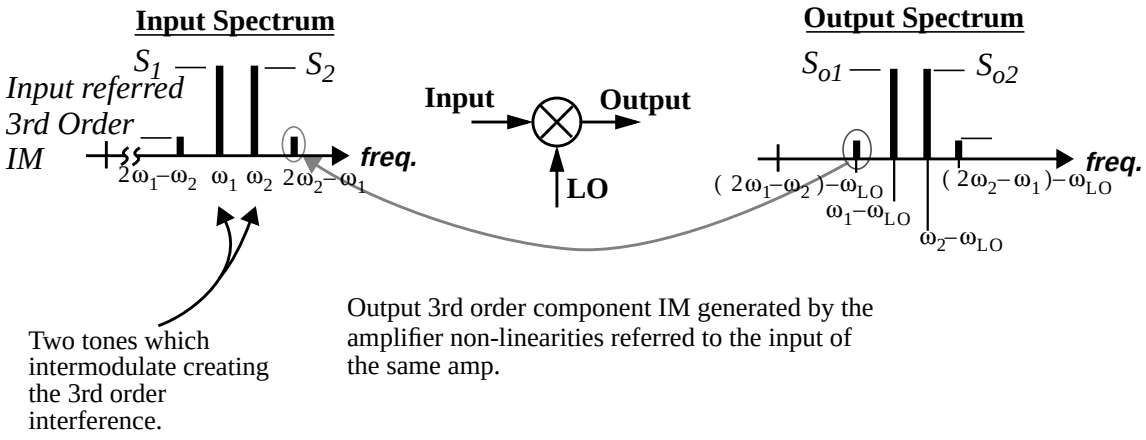


Figure 76. The third order intermodulation both output and input referred.

Two common measures which are used to describe the third order non-linearity of communication circuits or systems are the 3rd order intermodulation component (IM3) and the 3rd order intermodulation intercept point (IP3). Both measures are typically quoted when the magnitude of S1=S2. Under this assumption, the 3rd order intermodulation component or IM3 is by definition the ratio of the amplitude of third-order IM component to the amplitude of the fundamental (S_1, and S_2) either at the input or output of the component [6.13].

$$IM_3 = \frac{3}{4}\frac{a_3}{a_1}S_1^2 \qquad \text{(Eq 6.54)}$$

The plot in figure 77 is a common plot which describes both the IM3 and IP3 of a component either referenced to the input or the output of a block. The x-axis is the input/output power applied to the component which is equivalent to the power of S1 and S2 expressed in dBV in figure 77. Typically, several values for the input signal S1 are applied to the receiver in either a simulation or measurement. The linear response to the

input signal is then plotted along with the measured or simulated 3rd order IM at either $2\omega_2(-/+)\omega_1$or $2\omega_1(-/+))\omega_2$. The 3rd Order response is then recorded in dB, while a line is used to extrapolate both the linear and 3rd order response based on the simulated/ measured values. Where both of these extrapolated lines cross is defined as the 3rd order intermodulation intercept point or IP_3. This point has a special and convenient significance in defining the linearity performance of receiver communication blocks as it characterizes the amount of interference as a function of magnitude of the alternate channel/band interfering signals, and the IP_3. In addition, the IP_3 number can be used to compute the equivalent IP3 of several components in series as a function of the IP_3 of the individual components, this is discussed in chapter 2.

Although, the IP3 is useful in characterizing the amount of 3rd order distortion, it should be kept in mind that the mixer or whatever receiver component, will never actually generate signals of that magnitude as the component will go into gain compression before this point is reached. The real response due to the linear and 3rd order component will roll off before reaching the IP3, this is illustrated in figure 77.

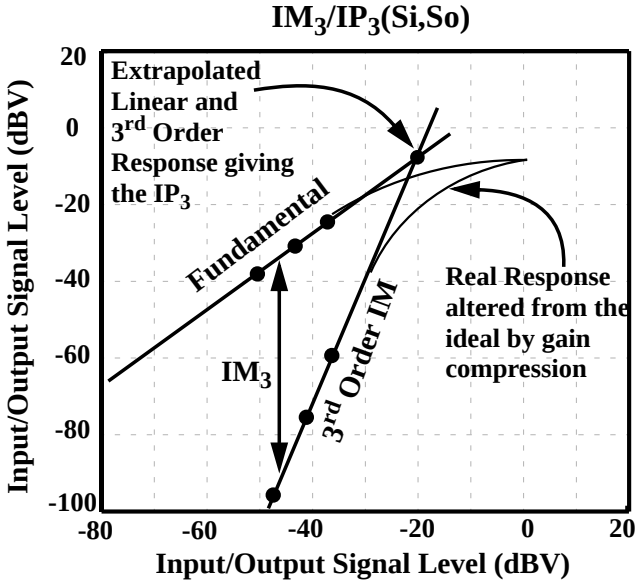


Figure 77. General plot characterizing the third order distortion of a component. Both IM3 and IP3 are illustrated on the plot.

With the previous discussion, it becomes clear that modeling the switching mixer with respect to the IP_3, quickly allows an understanding of the mixer's relative degradation of the overall receive chain's linearity. Therefore, it will now be of interest to model the linearity performance of these mixers with respect to an equivalent input referred IP3 of current switching mixers. From simulation, it was found that the degradation in the overall mixers 3rd order non-linearity was dominated by the linearity performance of the transconductance stage. Thus, the quick analysis given in this section is done so with the assumption that the transconductance stage dominates the linearity performance of CMOS switching mixers.

With the assumption that the distortion is coming from the transconductance stage a model for the equivalent IP3 of the mixer may be constructed. Part of the distortion analysis for the transconductance stage was derived from notes given in [6.13]. The input devices in fine line CMOS technologies will experience velocity saturation, which will have the affect of linearizing the device transconductance. However, a lower bound (worst case) to the 3rd order linearity performance can be given, if it is assumed that the devices in the transconductance stage, have a classical square law drain current characteristic. From figure 78, the objective now becomes finding when the 3rd order component in the drain current of the transconductance stage is equal to the differential signal produced by the fundamental. The equivalent IP3 will be found with respect to the amplitude of the differential input voltage. The differential drain current at the output of the transconductance stage can be written as,

$$I_o = I_1 - I_2 \qquad \text{(Eq 6.55)}$$

Assuming square law device the drain current can be derived as a function of the differential input voltage v_i,

$$I_o = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right) v_i \sqrt{\frac{2I_b}{\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)} - v_i^2} \qquad \text{(Eq 6.56)}$$

This can be written as,

$$I_o = \sqrt{2I_b \frac{\mu_n C_{ox}}{2}\frac{W}{L}}\, v_i \sqrt{1 - \frac{v_i^2}{\frac{2I_b}{\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)}}} \qquad \text{(Eq 6.57)}$$

Defining variables K_1 and K_2 as

$$K_1 = \frac{2I_b}{\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)} \qquad K_2 = \sqrt{2I_b \frac{\mu_n C_{ox}}{2}\frac{W}{L}}$$

Equation 6.57 can be written as,

$$I_o = K_2 v_i \sqrt{1 - \frac{v_i^2}{K_1}} \qquad \text{(Eq 6.58)}$$

Recalling the following power series expansion,

$$(1+x)^n = 1 + nx + \frac{n(n-1)}{2!}x^2 + \frac{n(n-1)(n-2)}{3!}x^3 \ldots \qquad \text{(Eq 6.59)}$$

Utilizing the above expression on equation 6.58 results in,

$$I_o = K_2 v_i \left[1 - \frac{1}{2}\frac{v_i^2}{K_1} + \frac{\frac{1}{2}\left(-\frac{1}{2}\right)}{2}\frac{v_i^4}{K_1^2} \ldots \right] \qquad \text{(Eq 6.60)}$$

Expanding out equation 6.60 similarities to equation 6.51 may be found,

$$I_o = K_2 v_i - \frac{1}{2}\frac{K_2}{K_1} v_i^3 - \frac{1}{8}\frac{K_2}{K_1^2} v_i^5 \ldots \qquad \text{(Eq 6.61)}$$

By definition the third order input referred intercept point will occur when the magnitude of the linear term generated at the output, is equal to the magnitude of the third order IM produced by the third order transfer function. Utilizing the definition given in equation 6.54 along with results from equation 6.61 gives,

$$K_2 v_{ip3} = \frac{3}{4}\left(\frac{1}{2}\right)\frac{K_2}{K_1} v_{ip3}^3 \qquad \text{(Eq 6.62)}$$

The K_2 term drops out and substituting in the definition from K1 results in,

$$v_{ip3} = 4\sqrt{\frac{2}{3}}(V_{gs} - V_t)_{in} \qquad \text{(Eq 6.63)}$$

Equation 6.63 gives a measure of the input referred IP3 with respect to the $(V_{gs}-V_t)_{in}$ of the input devices. Although the $(V_{gs}-V_t)_{in}$ devices are a variable in equation 6.63 it is assumed that the drain current is remaining constant. Assuming a constant current, the device size may be scaled to modulate the $(V_{gs}-V_t)_{in}$ and in turn change the third order intermodulation distortion performance.

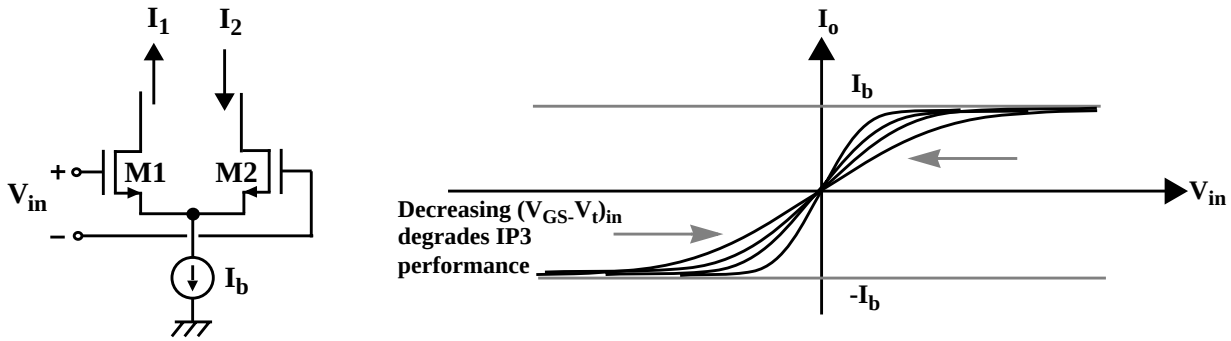


Figure 78. Source coupled stage with the corresponding curve of $I_o(V_{in})$.

Although, the analysis carried out in the previous section provides a concise result which provides a clear trade-off with the conversion gain and noise performance of the mixer, the result does not take into account the affect of filtering of both the fundamental components as well as the 3rd order intermodulation component. As long as the transconductance is operating well below the f_t of the input devices and the switches, the approximation given in equation 6.63 will produce an accurate and conservative result. However, as the speed of the mixer approaches the maximum achievable bandwidth for a particular technology, then a more appropriate approach is to utilize Volterra Series to evaluate the mixer linearity performance. In addition, the 3rd order linearity performance of the mixer is also dependent on the amount of time the switches are in the balanced state. It is shown in [6.14], that the linearity performance of the mixer will begin to degrade as the mixer spends a greater percentage of time in the balanced state. A more thorough treatment of both CMOS mixer linearity performance using volterra series as well as an in depth discussion of the linearity

dependence on the amount of time the mixer spends in the balanced state is given in [6.14].

6.7 Mixer Design Methodology

With a general description of the mixer conversion gain, noise contribution, and linearity, a review will be given of the general design methodology used to realize the mixers used in the wide-band IF receiver. A summary of the equations derived to describe the noise and linearity performance is summarized in table 2. A slight modification has been made to some of the equations such that all of the various noise sources and the conversion gain is strictly a function of the both the mixer tail bias current and the $(V_{gs}-V_t)$ of the input devices within the transconductance stage, the switches and the current source load devices.

In general, the objective is to minimize the $(V_{gs}-V_t)$ of all the devices to allow for as low a Vdd as is required by the technology. For the obvious reasons, the second objective is to minimize the static current consumed by the mixer, or minimize I_b. Alternatively, as will be discussed in detail throughout the next chapter, is to minimize the gate capacitance associated with the switches which will affect the power consumption of the LO buffers driving the mixer.

The methodology for designing all of the mixers used on both the experimental receivers described in this thesis involved first defining from a system level the required 3rd order linearity performance of the mixer. A review of the procedure used to find both the equivalent input noise resistance, 3^{rd} order linearity performance, in addition to the conversion gain of the individual mixers as well as the other receiver components used by the DECT/GSM receiver is given both in chapter 2 of this thesis, and in [6.15]. From a system level, with a definition of the required 3^{rd} order intermodulation performance of the mixer, the $(V_{gs}-V_t)$ of the input devices can be set using the first entry in table 2. This will actually give a conservative estimate for the linearity of both

the transconductance stage and the mixer, as this equation was derived using square law equations. For sub-micron technologies, the devices will experience velocity saturation, resulting in a more linear input pair and increasing the value of the V_{ip3} compared to what is defined in table 2. With the V_{dsat} of the source coupled pair defined, the next objective is to define the required conversion gain and the desired noise performance of the mixer which are now dependent on the product of I_b and R_L in addition to the ratio of $V_{LO}/(V_{gs}-V_t)_{sw}$. Again, the objective is to minimize the bias current which is used by the mixer. It would seem at first glance, that increasing the ratio of $V_{LO}/(V_{gs}-V_t)_{sw}$ could be accomplished by simply decreasing $(V_{gs}-V_t)_{sw}$ to a few millivolts. However, for a given I_b, decreasing the $(V_{gs}-V_t)_{sw}$ will obviously result in a larger switch size and corresponding large gate capacitance. This makes the design of a low power high LO amplitude buffer difficult to implement. This is particularly true if accurate quadrature is required as is in the image-rejection mixer implemented in both the receivers discussed in this thesis. The implementation of an LO buffer which generates accurate quadrature is covered in chapter 7. All of the LO buffers which were designed for both receivers were intended to have a 800mV zero-to-peak amplitude driving the mixer. With the amplitude of the LO fixed (V_{LO}), the $(V_{gs}-V_t)_{sw}$ was then selected as large as possible to meet both the noise and conversion gain requirement while minimizing the gate load capacitance on the LO buffer. From the plot shown in figure 75, it can be seen that the total input referred noise begins to role off when the $V_{LO}/(V_{gs}-V_t)_{sw}$ is approximately 2. Therefore, the V_{dsat}s of the switches were selected to be approximately half the value of the LO input amplitude, for this example, that corresponded to $(V_{gs}-V_t)_{sw}$ of approximately 400mV.

To minimize the noise contribution from the PMOS active current source, one can see from the expression given for $R_{eq(cs)}$ that maximizing the $(V_{gs}-V_t)_{cs}$ will reduce the noise contribution from the load current source. However, increasing the V_{dsats} of the load will obviously lower the output swing, in turn reducing the amount of available

headroom. Therefore, the $(V_{gs}\text{-}V_t)_{cs}$ of the load current sources should be made as large as possible allowing for the needed output swing at a given minimum supply voltage.

	Description
V_{ip3}	$4\sqrt{\frac{2}{3}}(V_{gs}-V_t)_{in}$
A_{CG}	$\frac{\sqrt{2}I_b R_L V_{LO}}{(V_{gs}-V_t)_{in}(V_{gs}-V_t)_{sw}\pi}\sin\left(\frac{\sqrt{2}(V_{gs}-V_t)_{sw}}{V_{LO}}\right)$
$R_{eq(gm)}$	$R_{eq(g_m)} = \zeta\cdot\left(R_s + m\cdot 2\left(r_g + \gamma\frac{1}{g_m}\right)\right) \quad m = 1, 2 \qquad \zeta = \sum_{k=1}^{\infty}\left\|\frac{p_k}{p_1}\right\|^2 = \sum_{k=1}^{\infty}\left(\frac{\left(\frac{1}{k^2}\right)\sin\left(\frac{k\pi}{2}\right)\sin\left(\frac{k\pi}{2}x\right)}{\sin\left(\frac{\pi}{2}x\right)}\right)^2$
$R_{eq(sw)}$	$\beta\left(R_{LO} + 4\left(r_g + \gamma\left(\frac{1}{g_{msw}}\right)\right)\right)$ $\beta = \sum_{k=-\infty}^{\infty}\frac{\|s_k\|^2}{\|A_{CG}\|^2} = \left\|\frac{(V_{gs}-V_t)_{in}}{2(V_{gs}-V_t)_{sw}}\left(\frac{(V_{gs}-V_t)_{sw}}{V_{LO}}\right)^2\frac{1}{\sin\left(\sqrt{2}\frac{(V_{gs}-V_t)_{sw}}{V_{LO}}\right)}\right\|^2 +$ $\sum_{k=1}^{\infty}\left\|\frac{(V_{gs}-V_t)_{in}}{(V_{gs}-V_t)_{sw}}\frac{\cos\left(\frac{k\pi}{2}\right)}{k^2}\left(1-\cos\left(k\sqrt{2}\frac{(V_{gs}-V_t)_{sw}}{V_{LO}}\right)\right)\frac{1}{\sin\left(\sqrt{2}\frac{(V_{gs}-V_t)_{sw}}{V_{LO}}\right)}\right\|^2$
$R_{eq(load)}$	$2\left(\frac{R_L}{A_{CG}}\right)^2\left(\frac{1}{R_L} + \gamma\frac{I_b}{(V_{gs}-V_t)_{cs}}\right)$
$R_{eq(total)}$	$R_{eq(total)}=\zeta\cdot\left(R_s + m\cdot 2\left(r_g + \gamma\frac{(V_{gs}-V_t)_{in}}{I_b}\right)\right)+\beta\left(R_{LO} + 4\left(r_g + 2\gamma\left(\frac{(V_{gs}-V_t)_{sw}}{I_b}\right)\right)\right) + 2\left(\frac{R_L}{A_{CG}}\right)^2\left(\frac{1}{R_L} + \gamma\frac{I_b}{(V_{gs}-V_t)_{cs}}\right)$

Table 2: Mixer conversion gain, noise, and linearity description.

With the $(V_{gs}\text{-}V_t)$ selected for all the mixer devices, this leaves the choice of R_L and the bias current. The product of I_b and R_L are selected to meet a particular conversion gain requirement, set on a higher system level. The choice specifically for I_b is made on the required noise performance of the mixer. From the expression given in table 2 for $R_{eq(total)}$, the relationship between bias current and the noise performance becomes clear. In short, the entire curve for $R_{eq(total)}$ can be pushed down by increasing

the value of I_b and maintaining all previously selected values for $(V_{gs}-V_t)$ of the switches, transconductance stage and the current source. An example of the noise contribution of various mixer devices on the tail bias current I_b is given in figure 79.

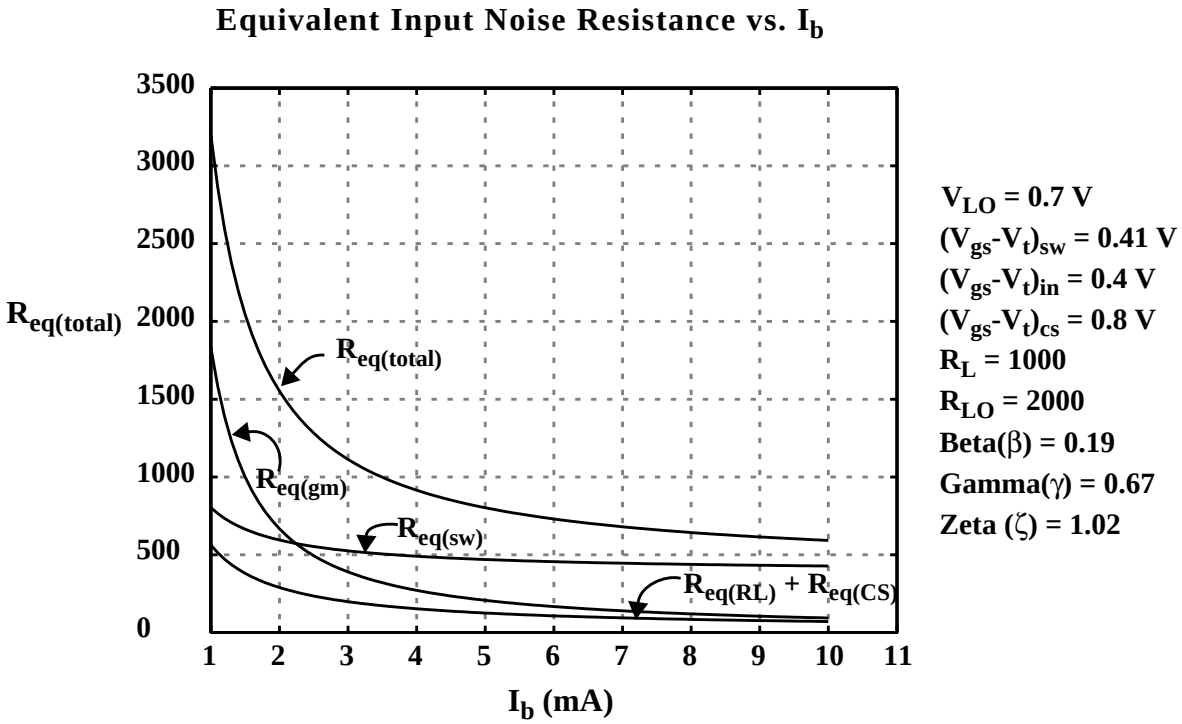


Figure 79. Current-commutating mixer noise performance as a function of the tail bias current I_b.

6.8 Example Mixer Design

With a review of the methodology used to design the mixers, a few design examples will now be provided. Not to lead to any confusion, it should be kept in mind that there were two receivers systems which were built, both of which utilized the wide-band IF architecture described in chapter 3. All of the six mixers used by both prototype receivers were implemented with some variant of the CMOS current commutating mixer shown in figure 63(b). This section will highlight some of the design features of each mixer used by both prototype receivers. For the purposes of the design examples presented in this section of the thesis, the name RF-to-BB will refer to the mixers converting the RF port signal from RF to an intermediate frequency. The RF-to-IF

mixers will always utilize the first higher frequency local oscillator referred to as LO1, the mixers themselves may sometimes use the name LO1 mixers or first stage mixers. The six mixers used in the wide-band IF architecture which convert the signal from IF to baseband will be called the IF-to-RF mixers or the LO2 mixers as these components run off of the lower frequency oscillator used in the second stage conversion, or the second local oscillator (LO2).

6.8.1 DECT Receiver Implementation

A diagram of the all the blocks included on the first DECT prototype receiver [6.15][6.16] is shown in figure 80. At the RF and LO signal ports of the receiver, a single-ended-to-differential conversion takes place with an external balun allowing the higher frequency signals to be brought on-chip differentially. To reduce the impact of coupling between blocks in the receiver, the entire signal path across the chip was made fully differential. The LNA is AC coupled to the input of the RF mixers, while the first mixer stage is AC coupled to the second set of mixers. At baseband, two offset current DACs are used to mitigate any effect due to LO self-mixing in the second mixer stage. A Sallen and Key anti-aliasing filter is used before the signal is sampled by an 8th-order switched-capacitor channel filter network. The signal is then digitized using a 10-bit, 10 MS/sec ADC. The digital output is driven off-chip using source-coupled logic to reduce the effects of digital substrate noise coupling. Quadrature LOs are realized with a 2^{nd}-order polyphase filter before being applied to the mixer input[6.17]. An indepth look into the implementation of the polyphase filter is given in chapter 7.

All circuits on this chip use a 3.3 Volt supply. All pads are ESD protected with reversed-biased PN diodes including the LNA input. To further reduce the possibility of coupling effects due to parasitic bondwire inductances, a self-biased on-chip current source is replicated throughout the RF and IF sections of the receiver. A discussion of the current source implementation is given at the end of chapter 7, section 7.4.1. The

bias circuit for the DECT prototype includes an adjustable current DAC. All bias circuits, gain control for the RF and baseband sections, as well as the ADC clocking frequency and various other options are controlled by two sets of 50-bit serial-input shift registers.

For the DECT prototype receiver, the output of the LNA is AC coupled to the input of the RF mixers (LO1), while the output of the RF-to-IF mixers is AC coupled to the input of the IF-to-BB (LO2) mixers. Finally, the output of the IF-to-BB mixers is directly coupled into the baseband anti-alias filter.

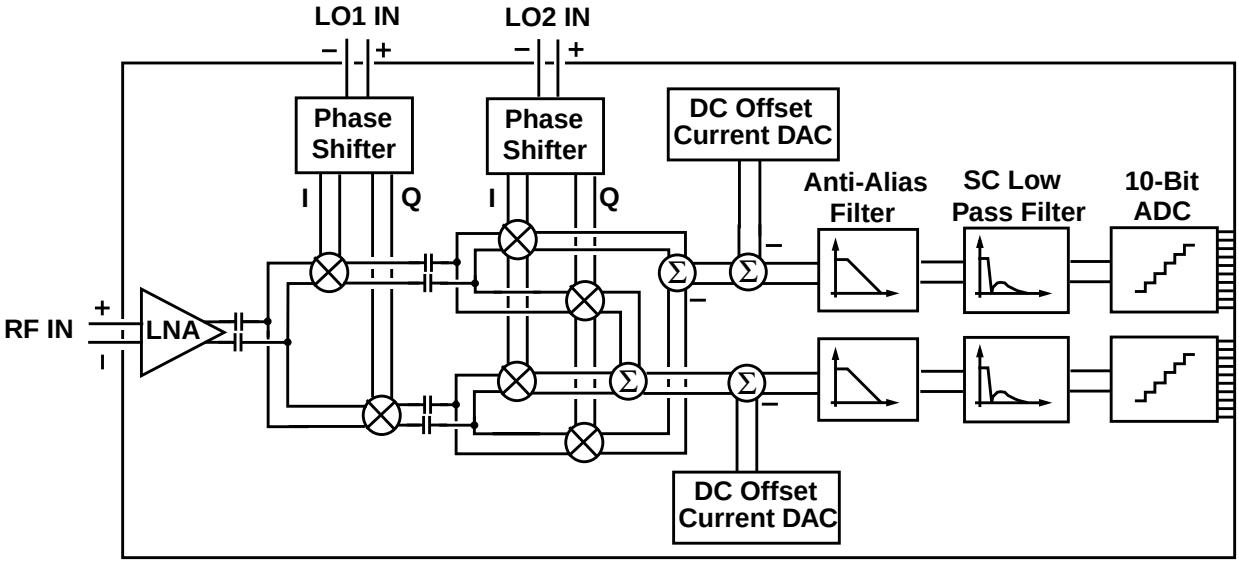


Figure 80. Block Diagram of the all the components included on the DECT receiver [6.16].

In the DECT prototype implementation, both of the local oscillators are realized off-chip. The first LO was fixed at 1.7GHz, because the DECT carrier runs from 1.88GHz to 1.89GHz, this implies that the second local oscillator must tune from approximately 190MHz to 200MHz to accommodate the direct modulation from IF to baseband.

6.8.1.1 RF-to-IF (LO1) Mixer

The basic circuit topology used by both the first and second mixer stages is shown in figure 81, with the exception that triode region devices M_9 and M_{10} are replaced with p+ diffusion resistors in the second mixer stage (LO2 mixers). The input transconductance stage consists of a simple differential pair M_1 and M_2. The cascode devices M_3 and M_4 provide better LO-to-RF isolation. M_5-M_8 act as switches in the mixer. Triode region devices M_9 and M_{10} are used to set both the load and the gain which may be modulated on-chip by varying the current through diode-connected device M_{16}. Common-mode feedback is achieved with devices M_{13}, M_{14}, M_{15} and the current source consisting of M_{11} and M_{12}. Compensation for the common-mode feedback loop is provided with C_{comp}. To remove any DC offsets from the first mixer and accommodate a level shift between the output of the first mixer stage and the input to the LO2 mixers, a 2.6pF coupling capacitor was used (see figure 82).

Selection of the local oscillator and IF frequencies involves several trade-offs. Gain and phase mismatch within the signal paths of the mixer limit the practical image attenuation to 35 dB. Therefore, to meet the image-rejection requirement of 70 dB in the DECT implementation, some filtering must be performed by the front-end RF filter. However, to make full use of this filter, the image-band must reside sufficiently far away from the desired carrier in frequency, implying a high IF. In addition, a high IF reduces the tuning range requirements of the IF synthesizer. In contrast, the output of the first mixer is a high impedance node. Therefore, the parasitic capacitance and the silicon technology used for this implementation set an upper bound on the allowable intermediate frequency. Originally, the RF mixers were designed to accompany an on-chip synthesizer where LO1 was limited to 1.7 GHz by the 0.6μm technology.

Therefore, in this implementation LO1 was set to 1.7 GHz requiring LO2 to range from 181 MHz to 197 MHz.

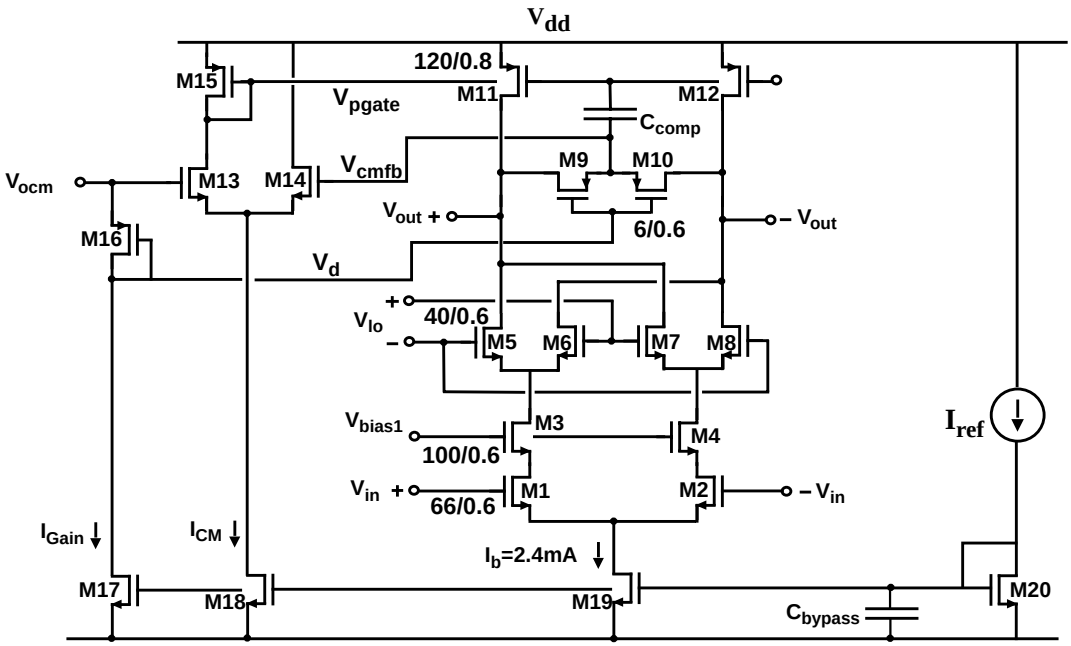


Figure 81. RF-to-IF (LO1) mixer used for the DECT receiver.

The bandwidth of the common loop is nominally 270MHz with a phase margin of 85^o. The value of C_{comp} is 8 pF. The $(V_{gs}-V_t)$ of the input devices was selected such that the IP3 of the mixer was simulated as Vip3 = 1.0 V. The size of M9 and M10 were selected to give a nominal drain to source resistance of 1 kΩ and this is the dominant load resistance of this mixer, thus, the drain-to-source resistance of M9 and M10 is represented by R_L in the model presented in section 6.5.2.3.

As mentioned earlier the amplitude of the local oscillator was designed to be 800mV zero-to-peak. To achieve minimal loading on the LO buffers while reducing the noise contribution from the switches and the load, a ratio of $V_{LO}/(V_{gs}-V_t)_{sw}$ was selected to be 2. This then set the $(V_{gs}-V_t)$ of the switches to be approximately 400mV.

The value of RL and the I_b were selected to give a voltage conversion gain of 3 with an equivalent input noise resistance of 1 kΩ.

As was mentioned in the previous section there exist a trade-off between the noise contribution from the current source devices and the available output swing of the mixer. The maximum required swing at the output of the first mixer is determined by the maximum possible received signal at the antenna as well as the total voltage gain between the antenna and the first mixer output. From the DECT standard, with 20dB of gain between the LNA input and the first mixer output this translates to a maximum differential mixer output swing of 200 mV.

The output common mode voltage was established by feeding in a single the reference current through the stack devices M1 through M6. The reference voltage set at the drain of M7 was then applied to a unity gain buffer consisting of M10, M11, M12, M19 and M20. The reference voltage at the output of the unity gain buffer, is then applied to an amplifier consisting of M13, M14, M15 and M18 which compares the desired common mode voltage at the gate of M13 with the actually common mode voltage from the output of the mixer. The error voltage generated then modulates the gate voltage of the load current source to move the output common-mode voltage in the direction of the desired common mode.

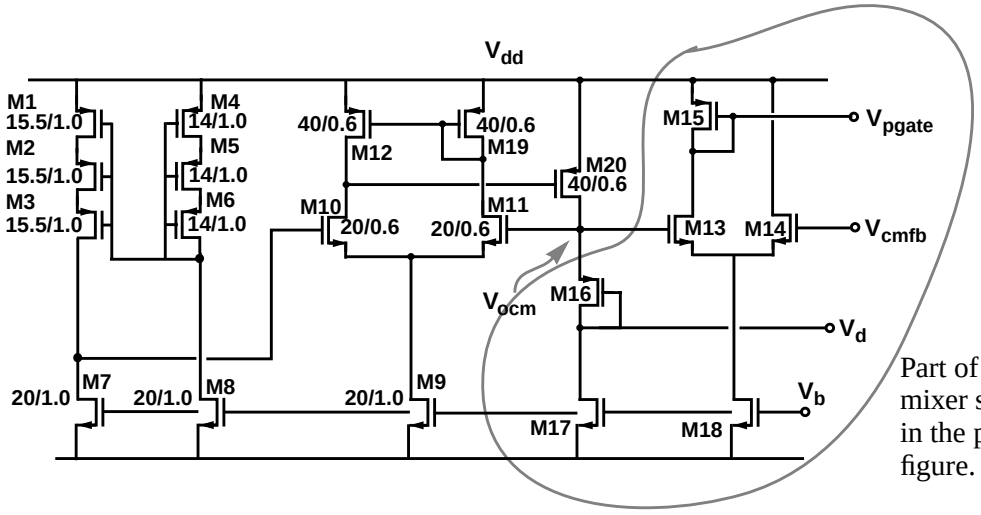


Figure 82. Circuit used to create the output common mode voltage of the LO2 DECT mixers.

6.8.1.2 IF-BB (LO2) Mixer

To remove the up converted terms, a low-pass filter is required at the IF node. The output resistance of the RF mixers in combination with the parasitic capacitance at the IF node together create the required RC time constant. Unfortunately, a problem associated with this particular implementation of the wide-band IF system is that at the first mixer output, the 3 dB frequency is 160 MHz which is much lower than desired. At IF, the desired channels range from 181 MHz to 197 MHz which implies a significant gain penalty for the RF mixers. Using a 0.6μm CMOS technology, the drain junction capacitance of the switches and the current source at the output of the first mixer, the gate capacitance of the input devices of the second mixer stage, and the parasitic capacitance of the AC coupling capacitor severely limit the bandwidth and the gain of the mixer.

The output current from two of the four IF-to-baseband mixers are added together to correctly sum the signals for image cancellation, as shown in figure 83. A pair of 6-bit DC offset current DACs are then used to mitigate the effects of any LO2 self-mixing and to compensate for DC offset in the subsequent baseband switched-capacitor filter stages. The offset current DAC on this chip can be updated with a baseband DSP using an algorithm as described in [6.18][6.19]. At the current summing node, the first pole of the anti-alias filter is created with the mixer output resistance loaded by a 28 pF capacitor. The low-pass filter created at the output of the first mixer stage in combination with the Sallen and Key filter serve a dual purpose, to remove the up converted IF mixer components and perform anti-alias filtering for the subsequent switched-capacitor blocks.

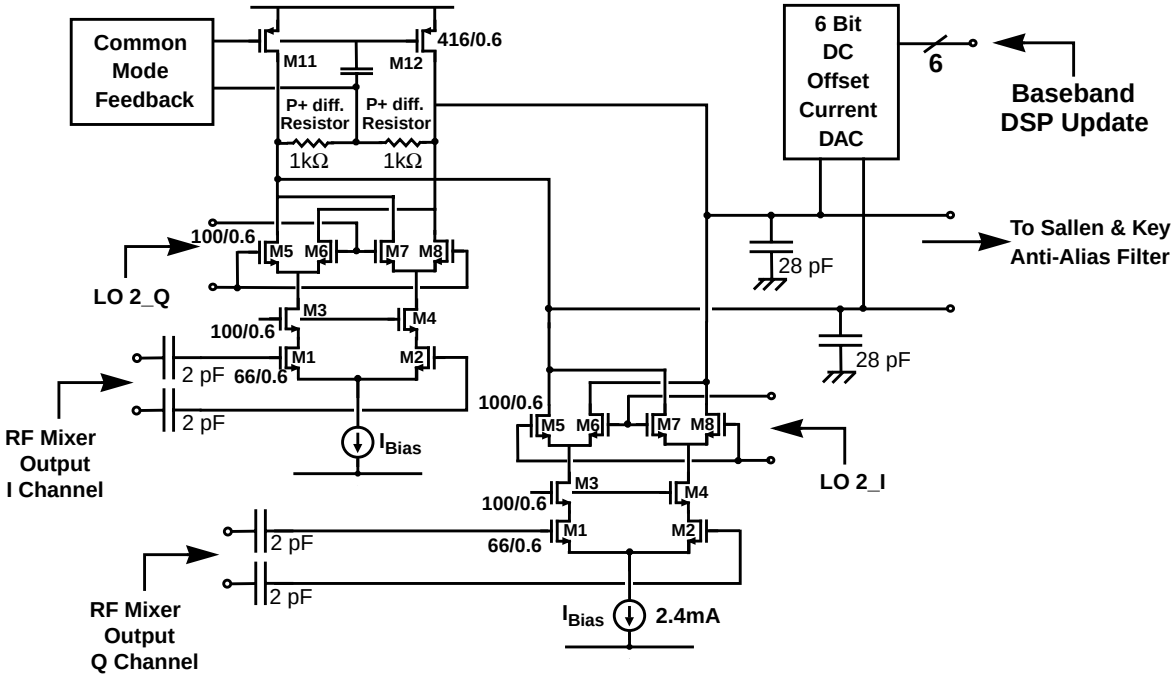


Figure 83. Two of the four mixers used by the DECT receiver to realize the frequency translation from IF to baseband.

6.9 References

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Chapter 7

IR Mixer - Supporting Circuits

7.1 Introduction.

In the previous chapters a description of the wide-band IF system was given, and a system that permits self-calibrating of the gain and phase mismatches found with in the various channels of an image-rejection mixer. In chapter 6, a discussion was given on the design of the all of the mixers used in both prototype receivers. This chapter emphazises the circuits which support the core mixer cells. In particular, the design and implementation techniques of circuits which generate quadrature signals. Both the first and second local oscillators must produce signals which have a 90^{o} phase difference. Because of the different frequencies of operation, and the requirements on tuning by the self-calibrating image-rejection mixer, the quadrature generation circuit implemented for the first local oscillator is significantly different from that used for the second local oscillator.

This chapter is broken into three sections, the first of which reviews some of the issues of generating quadrature signals at high frequency. Included in the first section, are some example implementations of high frequency quadrature phase generation circuits which have been utilized to date. This is followed by a description

of the circuit used to perform quadrature generation on the first high frequency local oscillator, shown as the LO1 phase shifter in figure 84. Specifically, a new circuit, utilized by the DECT/GSM receiver, which eliminates the loss in carrier power associated with a polyphase filter is presented. The second section of this chapter (section 7.3), looks into the issue of generating a tuneable, quadrature generation circuit, which has the ability to tune out the comprehensive phase error associated with all of the phase mismatch between two of the four image-rejection mixer channels. An example implementation of a tuneable phase shifter is presented at the end of section 7.3, along with some simulation results. The final section of this chapter (section 7.4) quickly reviews some of the standard bias circuits which were utilized by both the first and second generation prototype receivers.

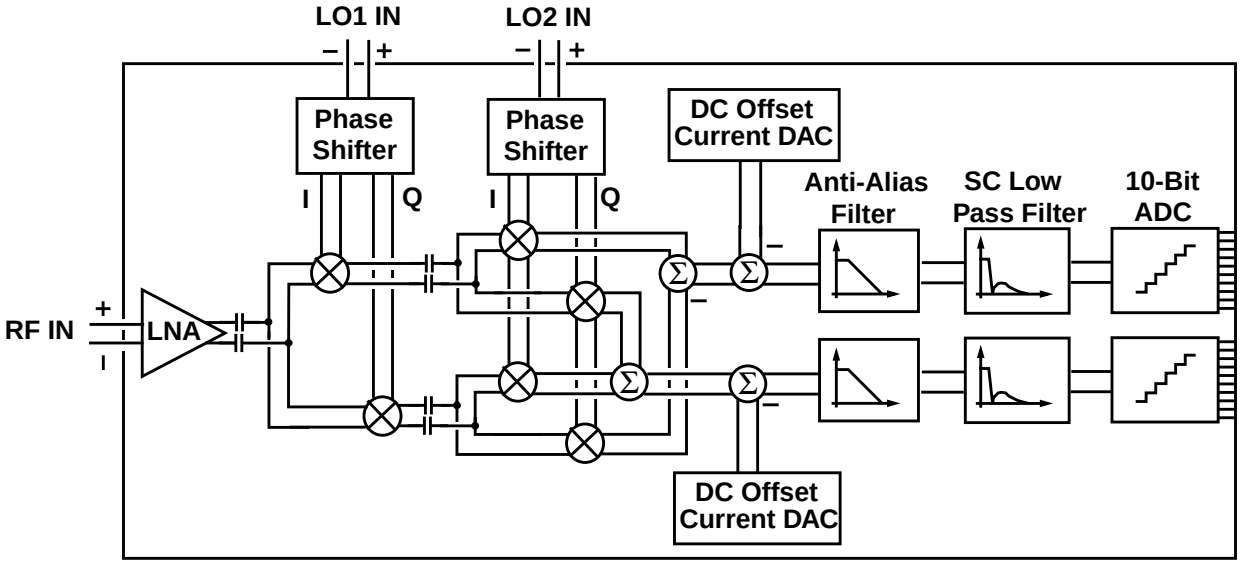


Figure 84. DECT prototype receiver block diagram.

7.2 High Frequency Quadrature Generation (LO1)

A key feature of any well designed frequency translation block used in a variety of communications applications, is the ability to generate accurate quadrature signals used by the mixers. This section will outline a block which was used for the GSM/DECT (2nd generation) receiver. An additional example is given on the

implementation of the quadrature phase shifter used by LO1 in the DECT receiver. This section begins with a brief review of the issues in designing quadrature generation circuits, as well as a comparison of some of the more common phase generation circuits used to date.

Typically in a receiver channel, quadrature signal generation begins with the output of a voltage controlled oscillator, which is inside a phase locked loop (PLL). The performance of PLLs in a radio channel is usually quoted in terms of phase noise, output carrier power (amplitude of the LO) and, for portable applications, the overall power consumption is of much interest. In conventional, discrete-component implementions of PLLs for radio channels, all of the components within the loop contribute noise fairly equally including the VCO. However, as was mentioned in chapter 3, when attempting to integrate the entire PLL, the VCO has a tendency to dominate the overall phase noise performance, as the inductor and the varactor diode used to implement the VCO have a significantly lower quality factor, than the discrete component counterpart. This is particular true of low-Q spiral inductors found on lossy CMOS substrates. Therefore, when attempting to utilize or tap the output of the phase-locked loop, it is critical to develop a circuit which not only buffers the VCO without significantly degrading the Q of the tank, but also provides buffering with minimal amount of loading to the PLL tank circuitry. In addition to generating quadrature signals, the buffer/phase shifting circuit also needs to supply sufficient carrier power for the mixer input port with a phase relationship as close to 90^o as possible.

The problem of buffering the VCO and generating quadrature signals is summarized in figure 85. Here it becomes clear from the perspective of the VCO, the input of the buffer/phase shifter should look purely reactive to prevent a reduction in the LC tank Q. Given a choice between an L or C, the choice is clear that an integrated input capacitance can be realized on-chip with a much higher Q than an inductor. This

is particularly true at 1.5GHz, which is approximately the frequency of the first local oscillator in both the GSM/DECT and DECT prototype receivers.

The VCO is typically realized with an LC tank, where the tuning frequency of the oscillator is controlled by a variable capactor, which is often nothing more than a varactor diode. Any additional parasitic capacitance added to the tank circuitry will degrade the achievable tuning range. Therefore, the capacitance looking into the VCO buffer phase shifter must be kept to a minimum. Additional issues associated with the buffer design are that the carrier power should be kept sufficiently large to ensure enough signal swing to adequately overdrive the switching devices inside the mixer. Furthermore, the phase error (defined as the deviation from the ideal 90^o) produced at the phase generator output should also be kept as small as possible, as this will influence the value of $\varphi_{\varepsilon 1}$ first described in chapter 4.

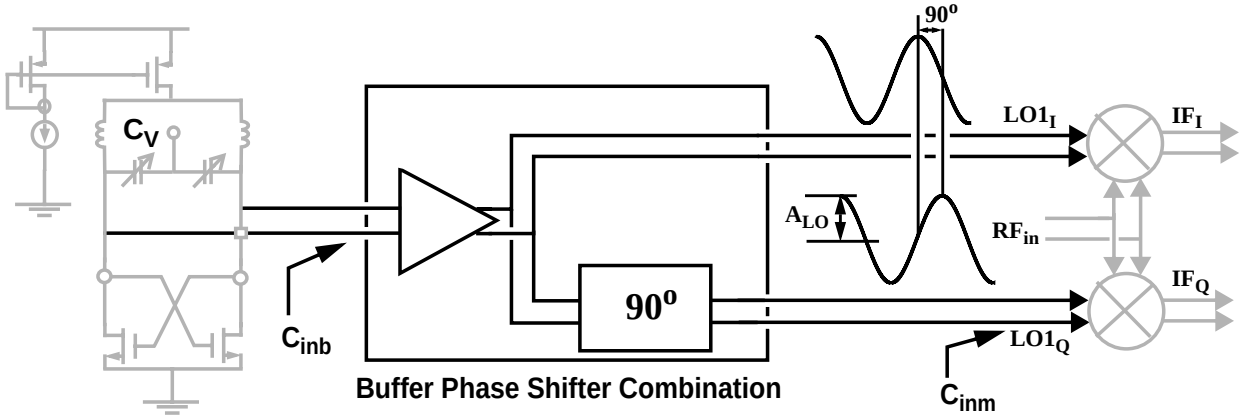


Figure 85. General block diagram of the VCO, phase shifting network and the input of the mixers.

While there are many publications and techniques introduced over the last fifty years to generate quadrature signals, only a few are highlighted here. One method for generating quadrature signals is to use a set of D flip-flops which perform a divide by 4. A desireable byproduct of this division is a set of 4 signals which are seperated equally in phase by 90^o. Although this achieves the goal of producing quadrature signals, a synthesizer is required which can realize a carrier four times higher in frequency than the signal required by the mixer. For the wideband IF system, the first local oscillator

must reside in the 1-2 GHz range for a 2 GHz input carrier. If D-latches were used to generate quadrature signals from the PLL, this would require a synthesizer capable of producing a 6 GHz output signal, which is difficult to achieve in a 0.35μm CMOS technology. In addition, achieving less than a 0.5^{o} of phase error using this method is challenging. Therefore, the divide by four method was eliminated for the first higher frequency local oscillator. However, this method was used to generate the lower frequency LO mixer input (LO2) for the DECT/GSM receiver, and is discussed more in section 7.3.

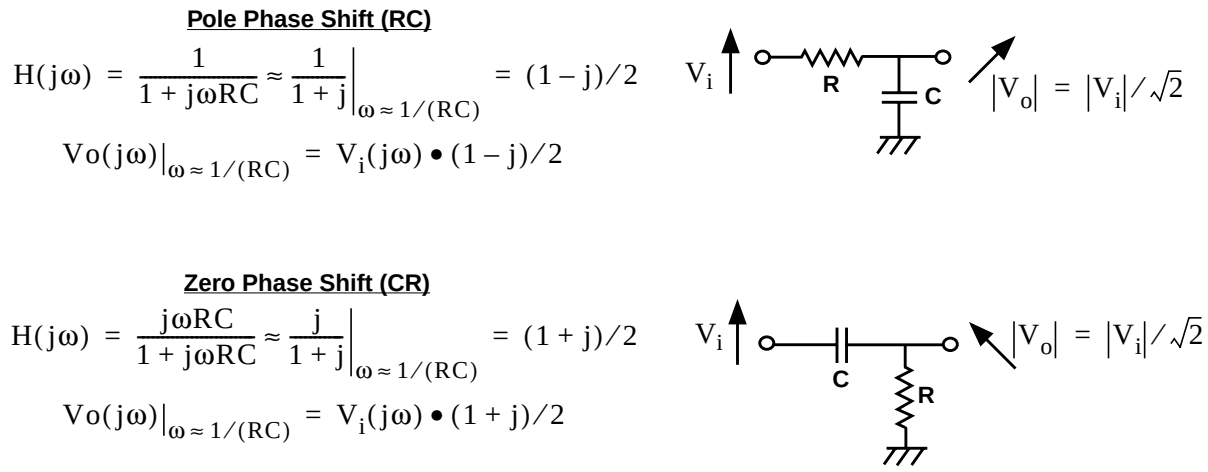


Figure 86. Vector representation of the effect of a pole and zero in the signal path.

The operation of most of the phase generation filters discussed in this section, can best be viewed or understood with a vector signal represention of the LO carrier as it passes through the filter. This is particularly true in the case of a polyphase filter which will be examined in depth, in section 7.2.5. Most of the passive phase shifting filters in the following sections utilize either a simple RC pole or zero to manipulate the phase of a signal in one path relative to the other signal path. Figure 86 contains the most intuitive vector argument, for the simplest single pole and single zero filter. The input to both the RC and CR circuits are represented with a vector of shown as V_i. The well known transfer function of both the single pole and zero are represented with H(jω). At the 3dB frequency, the input vector in the RC circuit is multiplied by the

transfer function which can be written as $(1-j)/\sqrt{2}$. This implies that the input vector is rotated by -45^o while the magnitude of the input vector magnitude is attenuated by $1/\sqrt{2}$. Likewise, in the case of a zero, the input vector is multiplied by a vector of $(1+j)/\sqrt{2}$ having the effect of advancing the phase of the input vector by 45^o, at the 3dB frequency. These simple vector concepts are reviewed in figure 86.

7.2.1 RC-CR Phase Shifter

The most basic circuit for generating a quadrature phase shift is to utilize two resistors and two capacitors to implement a pole in the in-phase path of the local oscillator, as well as a zero in the quadrature path of the carrier[7.1][7.2]. This method, which is illustrated in figure 87, simply uses the phase generated by a signal pole RC filter in one path and a zero in the other path to develop a 90^o phase difference between the two channels.

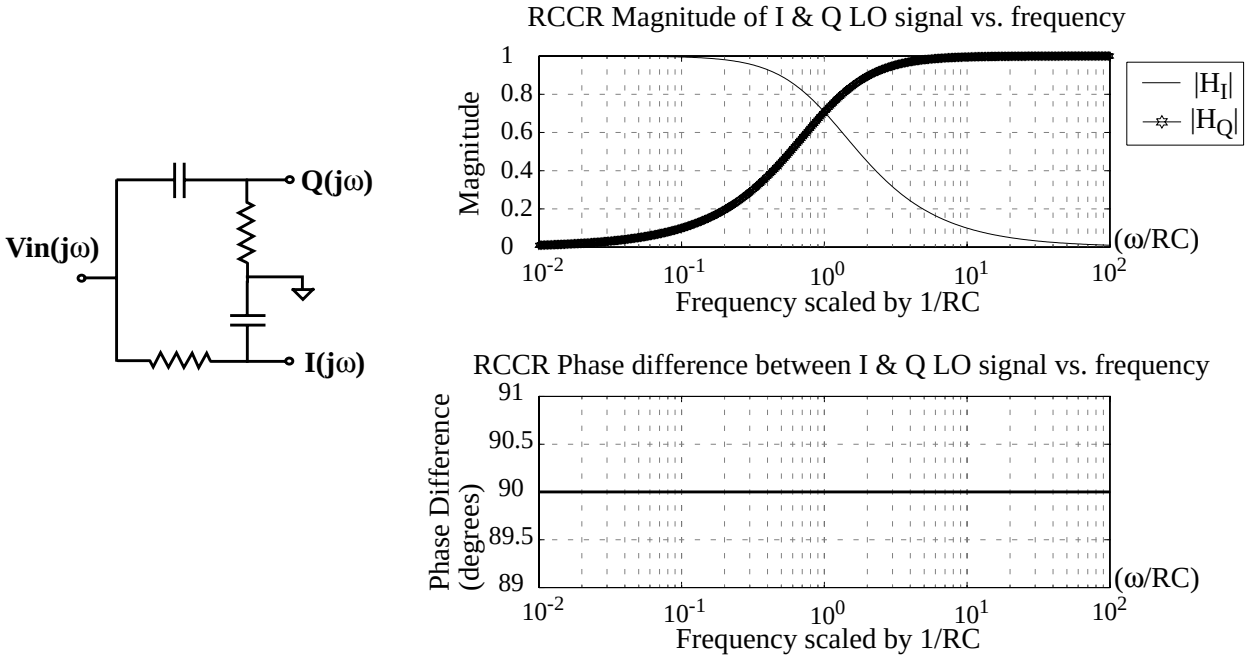


Figure 87. Simple RC-CR phase shifter used to develop a 90^o phase shift between two signal paths.

One of the most desireable characteristics of an RC-CR phase shifter is revealed when the phase difference between the I & Q output paths are derived as a function of the frequency. Assuming no mismatch between the passive components, the phase difference is a constant 90^o at all frequencies. This implies that the phase difference is immune to process variations in the resistors and capacitors (assuming no mismatch between components). However, the amplitude of the I and Q signals, in the two signal paths, vary as a function of frequency, and are only equal at the 3dB frequency. Both the magnitude and phase response of an RC-CR are plotted in figure 87, as a function of the ω normalized by the 3dB frequency. Although, the frequency is relatively constant for the first local oscillator in both the 1st and 2nd generation receivers discussed in this thesis, the amplitudes will differ considerably over resistor and capacitor process variations. This in all likelihood, would require a limiter (which is typical done) at the output of the RC-CR. Such a limiter would be difficult and relatively power hungry to design at 1.5 GHz. Additionally, the mismatch between the Rs and Cs in this filter will lead to a phase error. In appendix E, both the transfer function of the RC-CR filter is derived as well as an analysis of the phase error created by a mismatch between the passive components. The results of this analysis given in appendix E show that the deviation from ideal quadrature in an RC-CR filter as a function of component mismatch can be described as,

$$\Delta\varphi(\Delta R, \Delta C) = \operatorname{atan}\left(\frac{-\omega RC\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right)}{1 + \omega^2 (RC)^2}\right) \qquad \text{(Eq 7.1)}$$

At the 3dB frequency this may be simplified to,

$$\Delta\varphi(\Delta R, \Delta C) \approx \frac{\Delta R}{2R} + \frac{\Delta C}{2C} \qquad \text{(Eq 7.2)}$$

From equation 7.4, it can be shown that with a 5%($\Delta R/R = 0.05$ and $\Delta C/C = 0.05$) variation in both the resistor and capacitor values, the phase error will

be as large as 3^o. As will be shown shortly, the single ended version of the RC-CR filter has rather poor component matching characteristics when compared to a differential phase shifting topology.

7.2.2 Constant Magnitude Phase Shifter

One method proposed to overcome the gain mismatch between the two outputs of an RC-CR filter, was achieved through the use of a constant magnitude phase shifter [7.3]. Similar to an RC-CR phase shifter, the constant magnitude filter relies on a single RC pole and zero to obtain a 90^o phase shift. However, the primary advantage of this approach is with respect to maintaining an approximate equal amplitude between both the I and Q outputs. A schematic of the constant magnitude filter is shown in figure 88. This I/Q phase generator is inherently differential, one path of the carrier passes through a circuit with both a pole and zero, while the Q path of the filter is derived directly from the input signal, without any additional phase shift added between the input and output of the filter. For the implementation example given in [7.3], the phase shifter was used in the I and Q signal path after a downconversion mixer, however, this concept can easily be extended to generating quadrature local oscillators. In [7.3], a

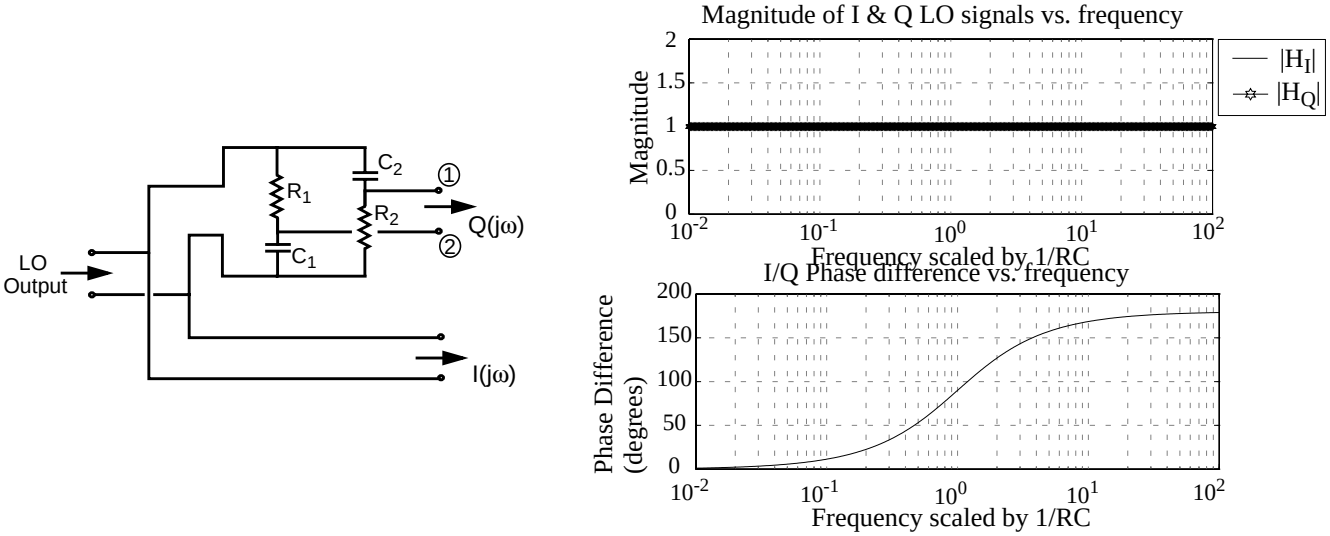


Figure 88. Constant magnitude phase shift filter.

dummy filter was placed in the Q channel, to ensure equal loading between the two signal paths.

A simple analysis of the in-phase signal path illustrates that both a pole and zero exist in the transfer function. The transfer function in the in-phase path can be expressed as,

$$H_Q(j\omega) = \frac{1 - j\omega RC}{1 + j\omega RC} \qquad \text{(Eq 7.3)}$$

Because of the allpass nature of the transfer function given in equation 7.1, the magnitude of the signal is obviously unity across the entire spectrum. From equation 7.3, the phase shift as a function of frequency can be written directly,

$$\angle H(j\omega) = \operatorname{atan}(-\omega RC) - \operatorname{atan}(\omega RC) \qquad \text{(Eq 7.4)}$$

or,

$$\angle H(j\omega) = -2\operatorname{atan}(\omega RC) \qquad \text{(Eq 7.5)}$$

From equation 7.5, it is clear to see that the phase difference between the I & Q path is 90^o, only at the 3 dB frequency. Therefore, this class of phase shifting filter has almost the opposite properties of an RC-CR filter. The gain between the two signal paths is equal at any frequency, eliminating the dependency of the signal amplitude on resistor and capacitor process variation. However, the phase is only 90^o at precisely the 3dB frequency, this can be seen in figure 88, where the magnitude response of the two channels is shown with the phase difference between the I & Q signals.

A derivation of the phase error as a function of the mismatch is given in appendix F, where the phase error as function of component mismatch can be described by,

$$\Delta\varphi(\omega, \Delta R, \Delta C) = 2\operatorname{atan}(\omega RC) - \operatorname{atan}\left(\frac{2\omega RC\left(1 + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1 - (\omega RC)^2\left(1 - \left(\frac{\Delta R}{2R}\right)^2\right)\left(1 - \left(\frac{\Delta C}{2C}\right)^2\right)}\right) \qquad \text{(Eq 7.6)}$$

The expressions for the mismatch of both the RC-CR (equation 7.4) filter as well as the constant magnitude phase shifter (equation 7.6), are plotted as a function of frequency for the case of $\Delta R/R = 0.05$, and $\Delta C/C = 0.05$ in figure 89(a), while figure 89(b) shows identical plots obtained from spice under the same condition. The phase error for an RC-CR filter peaks at the 3dB frequency, and is approximately 3^o for a 5% resistor and capacitor mismatch. Under identical circumstances, the phase error for a differential constant magnitude phase shifter is considerably less than an RC-CR filter; this is illustrated in figure 89. A 5% component mismatch results in less than a 0.1^o phase error, which is obviously considerably less than the case of an RC-CR filter.

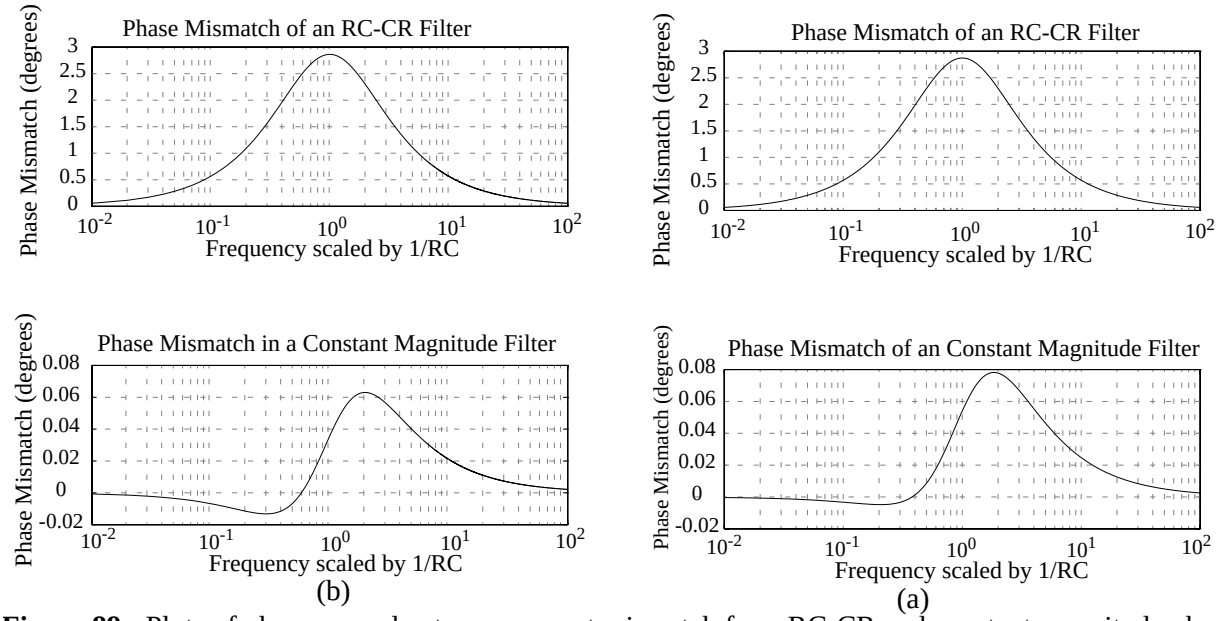


Figure 89. Plots of phase error due to component mismatch for a RC-CR and constant magnitude phase shifter vs. frequency. All examples above assume $\Delta R/R = 0.05$ and $\Delta C/C = 0.05$. (a) Results from spice simulations. (b) Plots based equation 7.2 and equation 7.6

The question of why the component mismatch has considerable less affect on a differential phase shift filter, when compared to a single ended filter, is not immediately clear. However, a vector signal diagram does aid in gaining an intuitive understanding as to why the phase error is significantly less, as a function of mismatched components, when compared to the mismatch error produced in a single-ended RC-CR filter.

Shown in figure 90(a), is a vector diagram representing the output signal of both the I and Q paths of an RC-CR filter. Near DC, the Q vector has an almost zero magnitude on the j-axis, while the I vector is at maximum magnitude, as expected, and can be represented as sitting on the real axis. As the frequency is increased and approaches the 3dB frequency of the RC combination, the Q vector rotates, and will ideally (without mismatch) sit at a 45^{o} angle with respect to the real axes, and the magnitude will increase to $1/\sqrt{2}$. Likewise, the I vector will rotate by a negative 45^{o}, and will ideally (without mismatch), reside at -45^{o}, with respect to the real axis. However, if there exist a mismatch between components in the RC filter, the vectors, at the 3dB frequency, are phase shifted; this case is represented as I' and Q' in figure 90(a). For the example mismatch case given in appendix E, R1 and C1 are slightly increased in value, thus lowering the pole frequency, and increasing the phase shift at the operating frequency, of the local oscillator, this is represented as I' in figure 90(a). Conversely, for the example given in appendix E, in the Q path of an RC-CR, a decrease in the resistor and capacitor results in an increase in the zero frequency, in turn resulting in less of a phase shift at the oscillator carrier frequency. In the RC-CR approach, the phase error due to mismatch, is then simply the sum of the phase error from the Q vector and the I vector.

A similar approach to understanding the phase error of differential constant magnitude phase shifter can be used as was done with the RC-CR filter. Figure 90(b) shows a vector signal representation of the I and Q output vectors, shown at nodes 1 and 2, in figure 88. The Q output vector is created by taking the vector represented as 1, and subtracting vector 2. Ideally, without mismatch, the resulting Q vector would lie on the j-axis. Vectors 1 and 2 will experience a similar phase shift with mismatch as was the case for the I and Q vectors in the RC-CR example. The output vectors, as a result of mismatch, are shown as 1' and 2' in figure 88(b). Now when the difference between these two vectors is taken to obtain the Q vector, it is clear, that the resulting Q vector, will still reside on the j-axis at the 3dB frequency. Thus, the phase error due to

component mismatch actually cancels, when taking the difference between the two vectors. In the RC-CR filter, the quadrature accuracy is the result of the phase

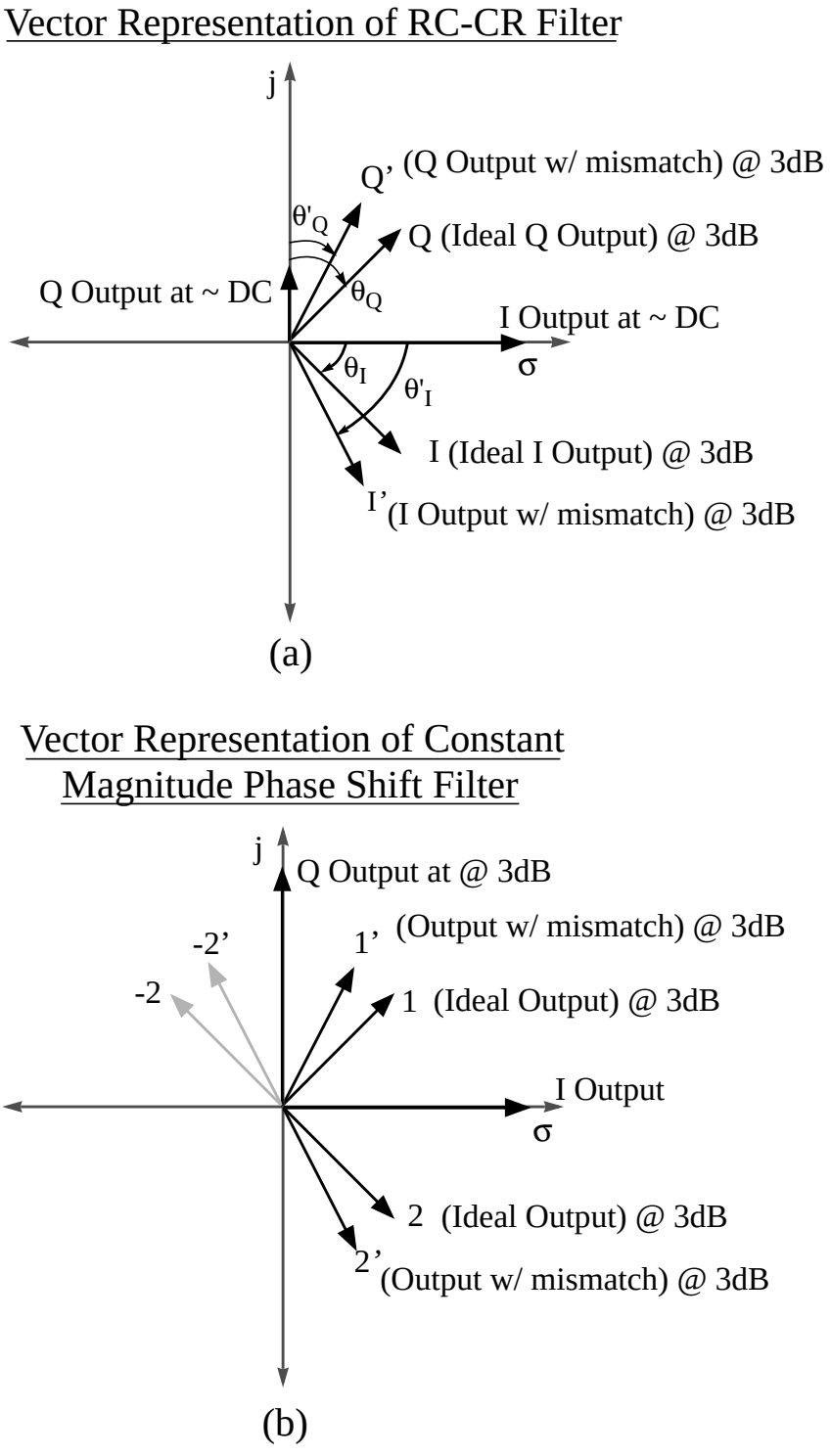


Figure 90. Vector representation of the phase error due to component mismatch (a) RC-CR filter. (b) Constant Magnitude phase shift filter.

difference between two vectors that are shifted in phase, by an amount that is roughly proportional to mismatch in R or C. However, in the case of the constant magnitude phase shifter, the Q vector is generated by taking the difference of the two vectors which are generated with a single pole and zero. To first order, the phase error generator by the pole and zero in a constant magnitude phase shifter cancels. The phase error generated as a result of component mismatch, in a constant magnitude phase shifter, is then related to higher terms resulting from subtracting vectors one and two in figure 90(b).

Generally speaking, differential phase shift circuit topologies will exhibit superior matching performance when compared to single ended quadrature generation circuits. In summary then, the RC-CR filter holds the advantage of maintaining a constant 90^o phase shift at any frequency. However, the disadvantage is with respect to matching (at least in the single ended version of this circuit) and the magnitude in each signal path is only equal at the 3dB frequency. Almost the opposite properties are observed with the constant magnitude phase shifter, which maintains an equal magnitude between the I and Q paths but has the disadvantage of only producing a 90^o phase shift at exactly the 3dB frequency, allowing for a phase error across resistor and capacitor process variation. The single ended RC-CR filter could be arranged into a differential version [7.3] to obtain superior matching properties. However, both the constant magnitude phase shifter as well as the differential version of the RC-CR filter begin to approach the form of a polyphase filter as will be discussed in section 7.2.4.

7.2.3 Miller Capacitance Phase Shifter

An alternative method to utilizing RC components in the realization of a quadrature signal generator, was introduced in [7.4], and is shown in figure 91. Here the output of the synthesizers feeds the input of two differential buffers. The output of each buffer is LC tuned with an on-chip spiral inductor. A phase shift is created between the

I and Q paths, at the buffer output, by virtue of a feed forward zero created with a capacitor between the gate and drain of the input devices of one buffer. The transfer function of the buffer with a miller compensation capacitor is shown in [7.4] to be,

$$H(j\omega) = \frac{-g_m \cdot R_L(1 - j\omega C_m/g_m)}{(1 + j\omega C_m R_L)} \qquad \text{(Eq 7.7)}$$

This expression for the voltage gain of just the input differential pair has an all pass characteristic, similar to the constant magnitude filter, in section 7.2.2. R_L is the impedance looking into the source of the cascade device (equation 7.7 is only the transconductance of the input differential pair) and can be simplified as $R_L=1/g_m$. In addition, if it is assumed that the value of C_m and g_m are selected such that $\omega = g_m/C_m$, than equation 7.7 can be expressed as,

$$H(j\omega) = \frac{-(1 - j)}{(1 + j)} \qquad \text{(Eq 7.8)}$$

This can be further simplified to,

$$H(j\omega) = -e^{-j90^o} \qquad \text{(Eq 7.9)}$$

From equation 7.9, the transconductance stage of the buffer with a Miller capacitor will create a 90^o phase shift between the input and output. The other buffer, without a Miller cap., will have a 180^o phase shift between the input and output. Thus, the total difference in phase between the two buffers outputs is ideally 90^o. This buffer configuration has a distinct advantage over the previous methods of phase shifting using passive RC components, as this circuit can actually be made to provide gain to the carrier from the VCO output to the mixer LO input. In addition, to generating quadrature, this buffer also accomplishes one of the goals previously outlined, which is to provide a capacitive input from the VCO looking into the buffer. However, it is probably worth mentioning that the impedance looking into the buffer with the feed-forward zero is not entirely capacitive and can be shown to be of the following form.

$$Z_{in}(j\omega) = \frac{(1 + j\omega C_F R_L)}{j\omega[(C_{gs} + C_F)(1 + j\omega C_F R_L) + g_m R_L C_F(1 - (j\omega C_F)/g_m)]} \qquad \text{(Eq 7.10)}$$

At $\omega = g_m/C_m$, the impedance looking into the buffer, with a miller capacitance, can be approximated as,

$$Z_{in}(j\omega)\big|_{\omega = g_m/C_m} \approx \frac{1-j}{2g_m} \qquad \text{(Eq 7.11)}$$

Equation 7.11 illustrates that there is a real part to the buffer input impedance of $1/2g_m$. Previous implementations of this phase generation scheme utilized an additional buffer between the VCO output, and the input of the two phase shifting buffers, illustrated in section 7.2.3. Depending on the use of the miller cap. phase shifter, care should be taken as the real part of the buffer input impedance could potentially degrade the Q of an LC based VCO tank.

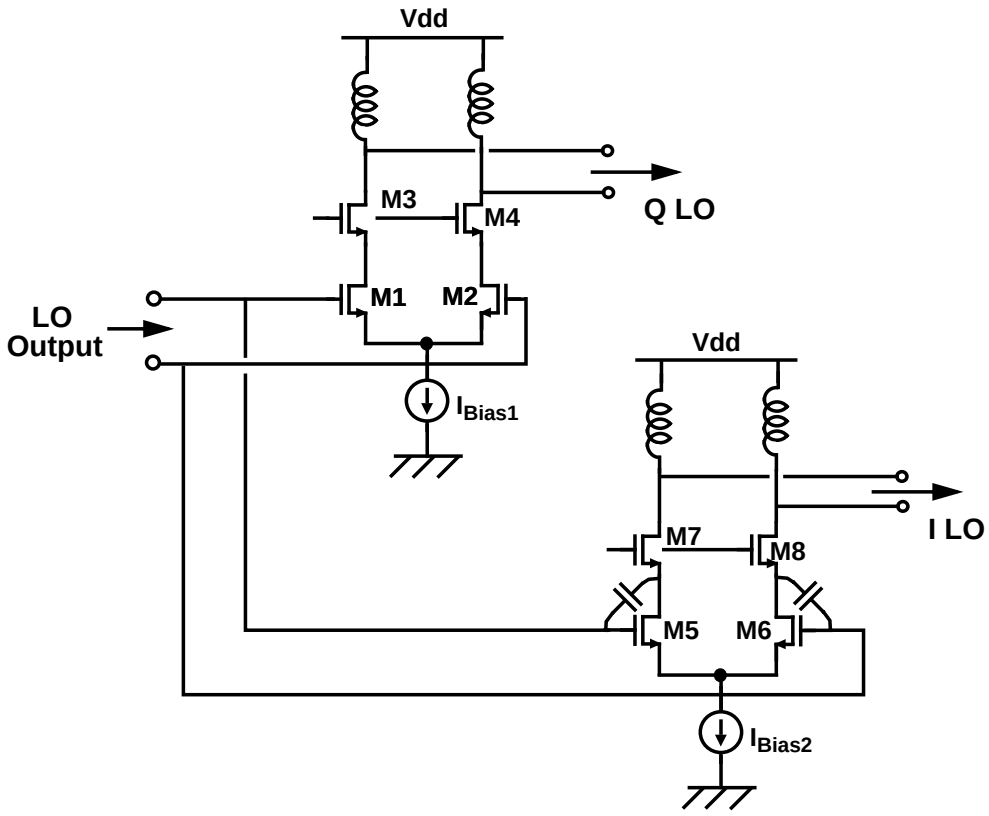


Figure 91. Miller Capacitance Phase Shifting Buffer.

The implementation given in [7.4], provided buffering of the mixer input capacitance and generate quadrature with relatively little power consumption. The phase accuracy in this approach, relies on generating a constant device g_m across

temperature and process. While this approach is suitable for applications where the requirement on phase accuracy is relaxed as it was in [7.4]. Other applications requiring a higher degree of phase accuracy may experience limitations using this method for quadrature generation.

Although, the miller phase shifting method may have limitations with respect to achievable phase accuracy, it is certainly worthy a discussion, as this concept was manipulated to realize a high phase accuracy buffer and quadrature signal generation circuit which was utilized by the first local oscillator in both the receive, and transmit paths of the GSM/DECT transceiver.

7.2.4 Asymmetric Polyphase filters

A third approach for generating quadrature signals and used in a variety of communications applications, is through the use of asymmetric polyphase filters. These filters have been used in applications ranging from quadrature signal generation to improving sideband suppression in the case of some image-rejection mixers, as discussed in chapter 5.

A polyphase filter is realized with a network of poles and zeros configured to rotated the phase of applied signals in potentially eight different directions, between the input and output of the filter. To understand how a polyphase filter may be used for various applications it is best to evaluate a single stage, again using a vector signal representation at both the input and the output of the filter.

The introduction of a phase shift for a single RC is illustrated in figure 86 and can be extended to a one stage polyphase filter shown in the center of figure 92. The filter is realized with four single ended inputs and four outputs. Four resistors and capacitors are configured to realize a network of poles and zeros. Depending on the phase relationship of the signal applied to the input of the polyphase, a number of

functions in communications channels may be realized including, quadrature signal generation, improved phase accuracy of quadrature signals and image (sideband) suppression. All of the potential input phase configurations, as well as the resulting ideal output vectors are shown in figure 92.

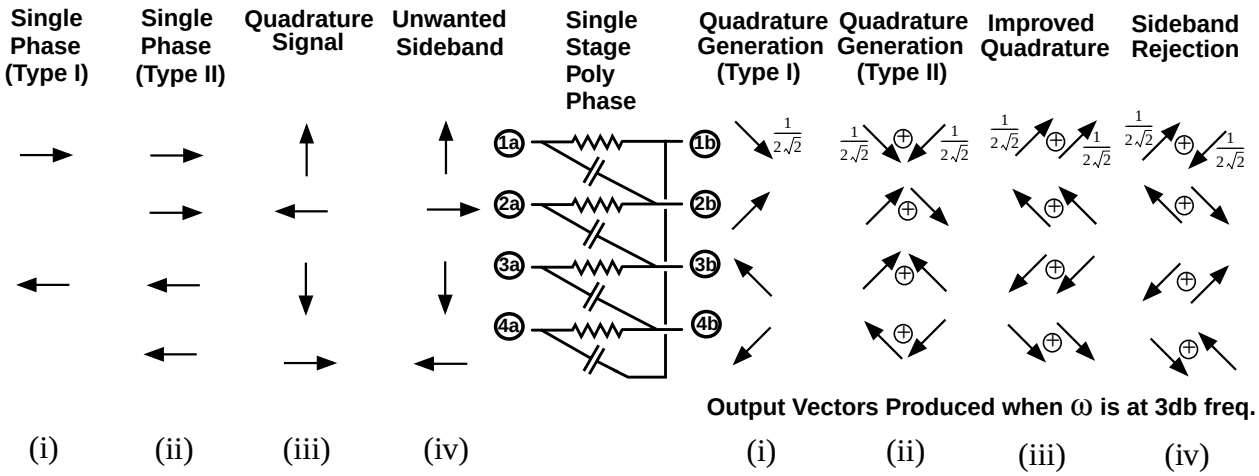


Figure 92. Potential uses for a poly phase filter. (i) Quadrature generation (type I input). (ii) Quadrature generation (type II input) (iii) Improved quadrature accuracy. (iv) Sideband (image) rejection.

Although polyphase filters may be applied in several locations within a receiver channel, of most interest in this work, is in use for quadrature signal generation. Quadrature signals are required for the local oscillator inputs of the image-rejection mixer discussed in this thesis. An accurate generation of a signal with a 90^{o} phase difference may be achieved by driving the input with a differential signal, either in what will be labeled as a single phase type I or type II input, both shown in figure 92(i) and (ii). In the type I input, one end of the differential signal is connected to terminal one while the opposite end of the differential signal is connected to terminal three, terminals two and four would then be connected to a common mode (AC gnd) voltage. For the type I input, the resulting vectors, shown on the right-hand side of figure 92 under quadrature output (Type I), will ideally result in a two differential quadrature signals by combining ports (1b) and (3b) to generate a Q signal while pairing ports (2b) and (4b) to obtain an I signal. Similarly , a polyphase filter driven

with what is labeled as a single phase (Type II) input, shown figure 92(ii), is realized by taking a single differential signal and applying one end of the signal to terminals one and two while the other end of the input differential signal is applied to terminals three and four. By applying the principle of superposition to each of the four output terminals, a set of vectors shown in figure 92(ii), at the output, would result with a type II input. Using terminal 1a under the case of quadrature output (type II), two separate vectors result at the filter output terminals 1b and 3b. However, through superposition, these two vectors when added (or subtracting 3b from 1b), results in one vector pointing along the negative j-axis. Similarly a vector pointing along the positive j-axis would result from adding two vectors shown at port 3b, in the quadrature generation (type II) example. Quadrature differential signals may be obtained by combining terminals 1b and 3b as well as the pairing 2b and 4b for both the type I and type II inputs.

Differential signals which may already be in quadrature or close to a 90^{o} phase difference may also appear at the input of a single stage polyphase filter; this is illustrated in figure 92(ii). This situation might arise when signals that are close to quadrature and need to be further refined in terms of phase accuracy are passed through either one or more stages of a polyphase filter. Another potential application for applying a signal that is already close to quadrature would be when attempting to suppress a sideband resulting from a complex mixing function [7.6]. In the case of image suppression, a differential signal in the desired frequency sideband would be applied with the phase relationship as shown in figure 92(iii) (already close to quadrature) while the undesired sideband (usually at the image frequency) would have an opposite phase relationship to the desired sideband as shown in figure 92(iv). Again, this phase relationship would exists after a complex mixing function, as is often done in receiver systems. The sideband above and below the frequency of the mixer local oscillator will have the phase relationships as shown in figure 92 (iii) and (iv). Applying the superposition principle to both sets of input vectors shown in figure 92(iii) and (iv) results in one set of output vectors which add in phase, allowing the

desired sideband to pass ideally unattenuated, while the undesired sideband (with phase as (iv)) results in a set of vectors which cancel at the filter output, thus removing the undesired sideband. The amount of sideband suppression which is attainable by a polyphase filter ultimately depends on the component matching as well as the dependence on phase to process variations. The following sections will look at these issues .

Polyphase filters are rarely implemented as a single stage. More often the polyphase filter utilizes several stages to realize either a quadrature circuit or for sideband suppression. Shown in figure 93 is again a vector diagram for a multistage polyphase filter which generates quadrature signals from a single phase type I input. This signal could be coming from the output of a synthesizer. Again, assuming that the signal passing through the filter is close to the 3dB frequency of the individual poles and zeros, the phase of signals as they pass through the filter may be tracked. This approach to studying polyphase filters was first introduced in [7.6]. At the output of the first stage of the filter, roughly quadrature signals are generated at 1b through 4b. The signal at the output of the first stage of the filter may have not be in perfect quadrature, in addition to an amplitude imbalance. The phase error resulting from the first stage is illustrated at the bottom of figure 93, where the vector labeled 4b is deviating slightly from the ideal. This error will be correct by passing the desired signal through additional stages of a polyphase filter. For quadrature generation, a phase error due to mismatch in the polyphase components is dominated by the last stage, as any phase error resulting from mismatch in all of the stages prior to the last stage, will be averaged out by the subsequent stages [7.10]. This is again illustrated at the output of the second stage of figure 93. It also worth noting that the phase of all the vectors are rotated by a positive 45^{o}, assuming the signal is near the filter 3dB frequency. Additional stages may be added to this filter to further correct the phase, as well as improve image suppression. The location of the poles and zeros in each of the stages may be staggered to increase the bandwidth of the filter, allowing quadrature phases

over a broader range of frequencies. The concept of broadbanding the phase of a polyphase filter was first introduced in [7.5][7.6]and applied in [7.7][7.8].

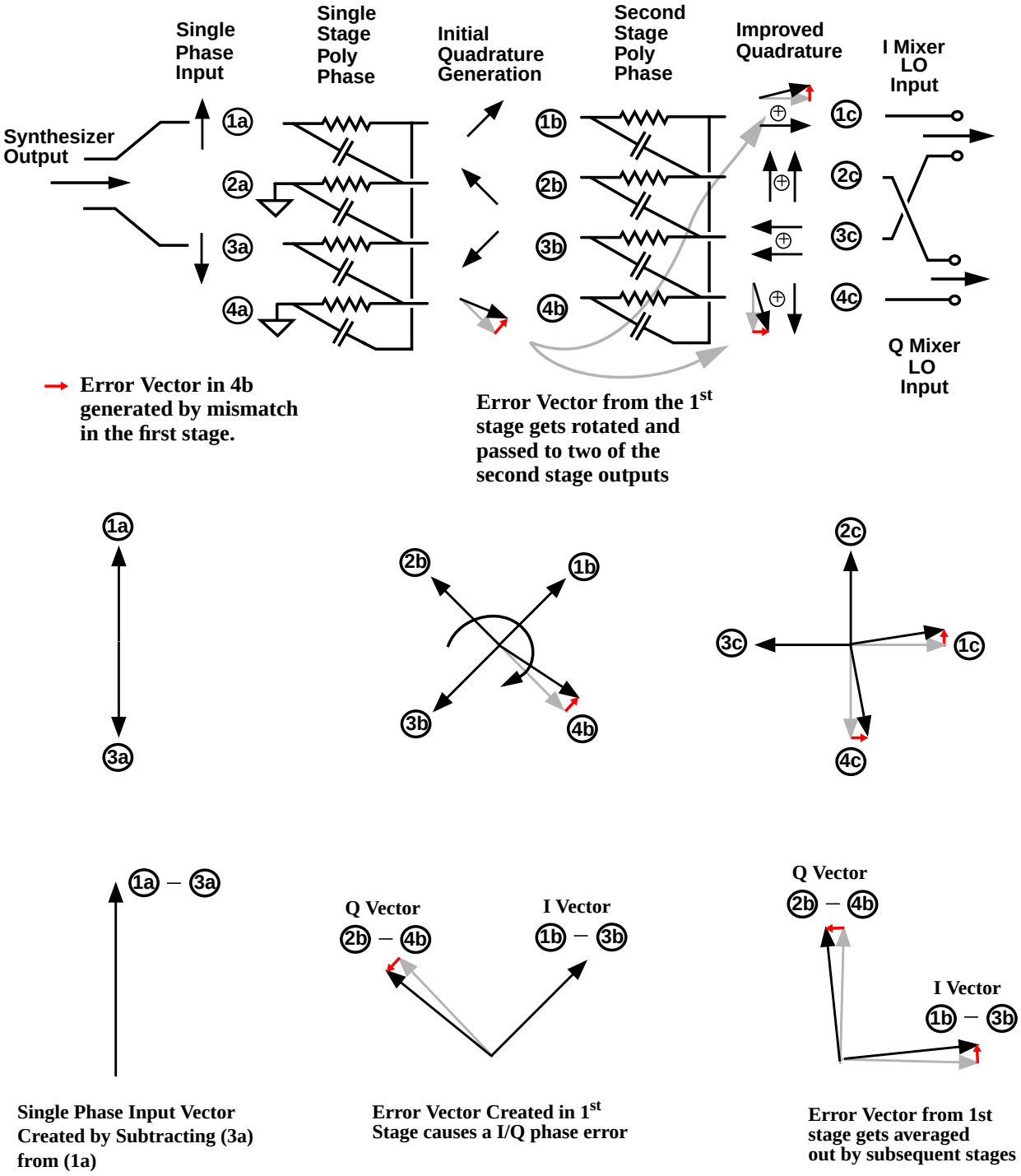


Figure 93. Mechanism of quadrature generation in an asymmetric polyphase filter. Additional stages improve quadrature accuracy.

A more quantitative description of a polyphase filter may be obtained by realizing that the output signal can be expressed in a matrix form. The relationship between the input signal and output signal can be described by,

$$V_o = P \bullet V_i \qquad \text{(Eq 7.12)}$$

Where P represents the shift in phase created by the polyphase filter and can be represented as a 4x4 matrix of the following form.

$$P = \begin{bmatrix} \frac{1}{1+j\omega RC} & 0 & 0 & \frac{j\omega RC}{1+j\omega RC} \\ \frac{j\omega RC}{1+j\omega RC} & \frac{1}{1+j\omega RC} & 0 & 0 \\ 0 & \frac{j\omega RC}{1+j\omega RC} & \frac{1}{1+j\omega RC} & 0 \\ 0 & 0 & \frac{j\omega RC}{1+j\omega RC} & \frac{1}{1+j\omega RC} \end{bmatrix} \qquad \text{(Eq 7.13)}$$

At the 3dB frequency of the individual poles and zeros, within the polyphase filter, a shift in the phase will be created where the P matrix can now be expressed as,

$$P = \begin{bmatrix} 0.5-0.5j & 0 & 0 & 0.5+0.5j \\ 0.5+0.5j & 0.5-0.5j & 0 & 0 \\ 0 & 0.5+0.5j & 0.5-0.5j & 0 \\ 0 & 0 & 0.5+0.5j & 0.5-0.5j \end{bmatrix} \qquad \text{(Eq 7.14)}$$

The input vector V_i represents the voltage at all four of the input ports of the filter. For example, a single phase differential signal with a peak voltage of unity applied to input ports 1 and 3 in figure 92(i), and figure 93, can be represented as an input vector V_i shown in equation 7.15(a). Likewise, an input signal already in quadrature may be represented as a vector in equation 7.15(c), also shown graphically in figure 92(iii). The third application of the polyphase filter is signal which has an opposing phase relationship between the I and Q inputs as the previous quadrature example and is represented as equation 7.15(c) as well as figure 92(iv).

$$V_i = \begin{bmatrix} 0.5 \\ 0 \\ -0.5 \\ 0 \end{bmatrix} \qquad V_i = \begin{bmatrix} 0.5 \\ 0.5 \\ -0.5 \\ -0.5 \end{bmatrix} \qquad V_i = \begin{bmatrix} 0.5j \\ -0.5 \\ -0.5j \\ 0.5 \end{bmatrix} \qquad V_i = \begin{bmatrix} 0.5j \\ 0.5 \\ -0.5j \\ -0.5 \end{bmatrix} \quad \text{(Eq 7.15)}$$

(a) Single Phase (type I) *(b) SinglePhase (type II)* *(c) Quadrature Input* *(d) Sideband Suppression*

Taking each of the input vectors listed above and multiplying by the P matrix results in.

$$V_o = \begin{bmatrix} 0.25 - 0.25j \\ 0.25 + 0.25j \\ -0.25 + 0.25j \\ -0.25 - 0.25j \end{bmatrix} \qquad V_o = \begin{bmatrix} -0.5j \\ 0.5 \\ 0.5j \\ -0.5 \end{bmatrix} \qquad V_o = \begin{bmatrix} 0.5 + 0.5j \\ -0.5 + 0.5j \\ -0.5 - 0.5j \\ 0.5 - 0.5j \end{bmatrix} \qquad V_o = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad \text{(Eq 7.16)}$$

(a) Single Phase (type I) *(b) SinglePhase (type II)* *(c) Quadrature Output* *(d) Sideband Suppression*

For all four cases, it is easily seen that there is an agreement with the vector argument given in figure 92. Although it becomes obvious that there are several possibilities when utilizing the polyphase filter as a quadrature generation circuit, some insight may be gained with a further investigation of the relative advantages and disadvantages in terms of the phase frequency dependence, mismatch properties as well as gain matching between the different possibilities for input phase. This will be considered in the next section.

7.2.4.1 Polyphase Properties Associated with Input Signal Phase

Upon first examination, it is not clear what the relative advantages and disadvantages associated with a single stage polyphase filter driven with a signal source which has a phase relationship classified in the previous section as either single phase type I or I input as well as a signal which is already in quadrature.

A starting point for a comparison between the different polyphase filter input signal configurations can be obtained by using equation 7.12. For a single phase type I input, equation 7.12 takes on the following form,

$$V_o = \begin{bmatrix} \frac{1}{1+j\omega RC} & 0 & 0 & \frac{j\omega RC}{1+j\omega RC} \\ \frac{j\omega RC}{1+j\omega RC} & \frac{1}{1+j\omega RC} & 0 & 0 \\ 0 & \frac{j\omega RC}{1+j\omega RC} & \frac{1}{1+j\omega RC} & 0 \\ 0 & 0 & \frac{j\omega RC}{1+j\omega RC} & \frac{1}{1+j\omega RC} \end{bmatrix} \cdot \begin{bmatrix} 0.5 \\ 0 \\ -0.5 \\ 0 \end{bmatrix} \qquad \text{(Eq 7.17)}$$

This results in an output voltage vector of,

$$V_o = \begin{bmatrix} \frac{1}{2}\left(\frac{1}{1+j\omega RC}\right) \\ \frac{1}{2}\left(\frac{j\omega RC}{1+j\omega RC}\right) \\ -\frac{1}{2}\left(\frac{1}{1+j\omega RC}\right) \\ -\frac{1}{2}\left(\frac{j\omega RC}{1+j\omega RC}\right) \end{bmatrix} \qquad \text{(Eq 7.18)}$$

Using the fact that the Q signal is created with the difference between the first and third output while the I differential signal is realized with the second and third output ports. The output vector, as a function of frequency in the I and Q outputs can be written as,

$$V_{oI} = \frac{1}{1+j\omega RC} \qquad V_{oQ} = \frac{j\omega RC}{1+j\omega RC} \qquad \text{(Eq 7.19)}$$

The phase difference between these two vectors is,

$$\angle\Delta\varphi(\omega RC) = 90^o(\text{constant}) \qquad \text{(Eq 7.20)}$$

From equation 7.19 and equation 7.20, it may be seen that type I input, shares the same properties as a RC-CR filter with respect to the phase difference between the I and Q signal maintaining a constant 90^o difference. However, similar to the RC-CR filter the amplitudes are only matched at the 3dB frequency. The one advantage of the type I input over an RC-CR filter, is again with respect to the differential nature of this

polyphase approach resulting in better matching properties. A matching analysis of a single phase type I input is provide in appendix H and is be described by,

$$\Delta\varphi(\omega, \Delta R, \Delta C)_{II} = 2\left[2\,\mathrm{atan}(\omega RC) - \mathrm{atan}\left(\frac{2\omega RC\left(1+\frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1-(\omega RC)^2\left(1-\left(\frac{\Delta R}{2R}\right)^2\right)\left(1-\left(\frac{\Delta C}{2C}\right)^2\right)}\right)\right] \quad \text{(Eq 7.21)}$$

Now looking at the case of a polyphase filter driven with a single phase type II input, and again applying equation 7.12, will result in the following response in both the I and Q output channels of the filter.

$$V_{oQ} = \frac{1-j\omega RC}{1+j\omega RC} \qquad V_{oI} = \frac{1+j\omega RC}{1+j\omega RC} \quad \text{(Eq 7.22)}$$

The phase difference between these two vectors can be described by,

$$\angle\Delta\varphi(\omega RC) = -2\,\mathrm{atan}(\omega RC) \quad \text{(Eq 7.23)}$$

From equation 7.22 and equation 7.23 it becomes obvious that a single phase type II input has identical characteristics to the constant magnitude phase shifter described in section 7.2.2. Unlike the type I input, the magnitude in the I and Q outputs are equal at any frequency. However, the phase difference between the I and Q paths becomes only 90^o at the 3 dB frequency. A closer examination of the configuration shown in figure 94 reveals that the phase of the input signal on both sides of the RC combination, comprised of R2 and C1 as well as R4 and C3 is identical. Therefore, these components do not serve any function other than providing better impedance matching for polyphase filter stages which might follow the first one. By eliminating the R_2, C_1, R_4 and C_3 from figure 94, it becomes obvious that this configuration is identical to the one shown in figure 88, the constant magnitude phase shifter. Because of the identical circuit topology between a constant magnitude phase shifter and a type II single phase input polyphase, it follows that the phase, magnitude, and matching behavior as a function of frequency are the same. The analytic result for the matching performance of a type II input polyphase is the same as given in equation 7.6. Nonetheless, the matching analysis for a type II single phase input is given in appendix

A, as the analysis was carrier out without making the observation that these two configurations are the same. The result is shown in equation 7.24.

$$\Delta\varphi(\omega, \Delta R, \Delta C)_{II} = 2\,\mathrm{atan}(\omega RC) - \mathrm{atan}\left(\frac{2\omega RC\left(1 + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1-(\omega RC)^2\left(1-\left(\frac{\Delta R}{2R}\right)^2\right)\left(1-\left(\frac{\Delta C}{2C}\right)^2\right)}\right) \qquad \text{(Eq 7.24)}$$

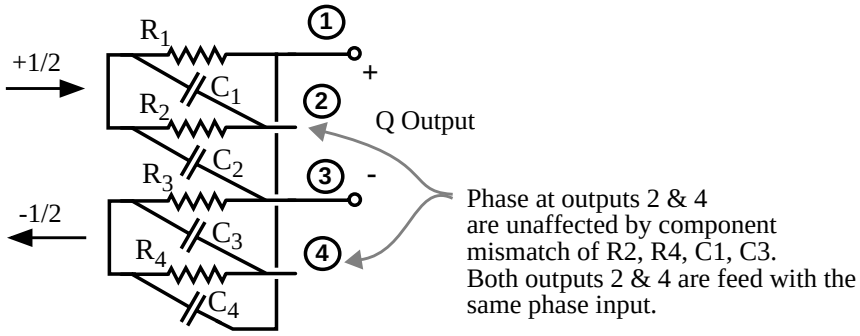


Figure 94. Type II input. Outputs 2 and 4 are immune to component mismatch as they are being driven by the same phase across an impedance divider of C_1, R_2 and C_3, R_4 combination.

The last case of interest is a single stage polyphase filter with a signal source at the input that has a phase relationship already close to quadrature. Again using equation 7.12, with an input V_i as given in equation 7.16(c), results in both an I and Q vector at the polyphase which can be written as,

$$V_{oQ} = j\frac{(1+\omega RC)}{(1+j\omega RC)} \qquad V_{oI} = -\frac{(1+\omega RC)}{(1+j\omega RC)} \qquad \text{(Eq 7.25)}$$

Here it is interesting to note that the phase difference between the I and Q paths is 90^o for any frequency. However, unlike an RC-CR type of filter, the amplitudes match for all frequencies. Admittedly, if the I and Q signal applied to the input of the filter were already in quadrature, there would be no reason to even use a polyphase filter. However, if the signal source used at the input of the filter is close to quadrature, and all that is need is a correction in phase, then there are some favorable characteristics of applying a quadrature signal, to the polyphase input as will be discussed.

The matching characteristics of a single stage polyphase filter is shown in appendix H to be,

$$\Delta\varphi(\omega, \Delta R, \Delta C)_{II} = 2\left[2\,\mathrm{atan}(\omega RC) - \mathrm{atan}\left(\frac{2\omega RC\left(1+\frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1-(\omega RC)^2\left(1-\left(\frac{\Delta R}{2R}\right)^2\right)\left(1-\left(\frac{\Delta C}{2C}\right)^2\right)}\right)\right] \quad \text{(Eq 7.26)}$$

Shown in figure 95 is a plot of the phase error due to mismatch as a function of frequency for all three of the input configurations discussed in this section. Shown in figure 95(a) are the results obtained for mismatch running spice simulations while figure 95(b) is based on the analytical expressions for mismatch presented in this section.

Shown in figure 96 are the results of SPICE simulations run on the three input phase configurations discussed in this section. The simulation results in figure 96, give identical results to all of the equations for phase and gain given in this section. From both the plots given in figure 96 and equations given in this section, some useful observations may be made with respect to the signal loss through a single stage of the filter. For the single phase type I input, a carrier loss of $1/\sqrt{2}$ at the 3dB frequency (which is where the filter should be operating to obtain the correct phase) is observed. This is intuitive, as with a type I input, the source is applied to only two of the four terminals and the power will be reduced by 1/2, in turn reducing the amplitude by $1/\sqrt{2}$. Because of the all pass nature of the constant magnitude filter shown in figure 96(b), ideally there is no signal attenuation in either the I or Q paths. The quadrature input polyphase configuration, is plotted in figure 96(c). In addition to maintaining a 90^o phase independent of frequency, there is actually a *signal gain* $\sqrt{2}$ near the 3dB frequency. The net increase in carrier power between the input and output, as compared to a polyphase driven with a type I or II input, is a significant observation that is used to realize a circuit discussed in the next section. The increase in carrier power is attributed to the fact that the filter is being driven by a signal source that adds in phase each of the four channels at the 3dB frequency. Thus, it would appear that driving a polyphase with

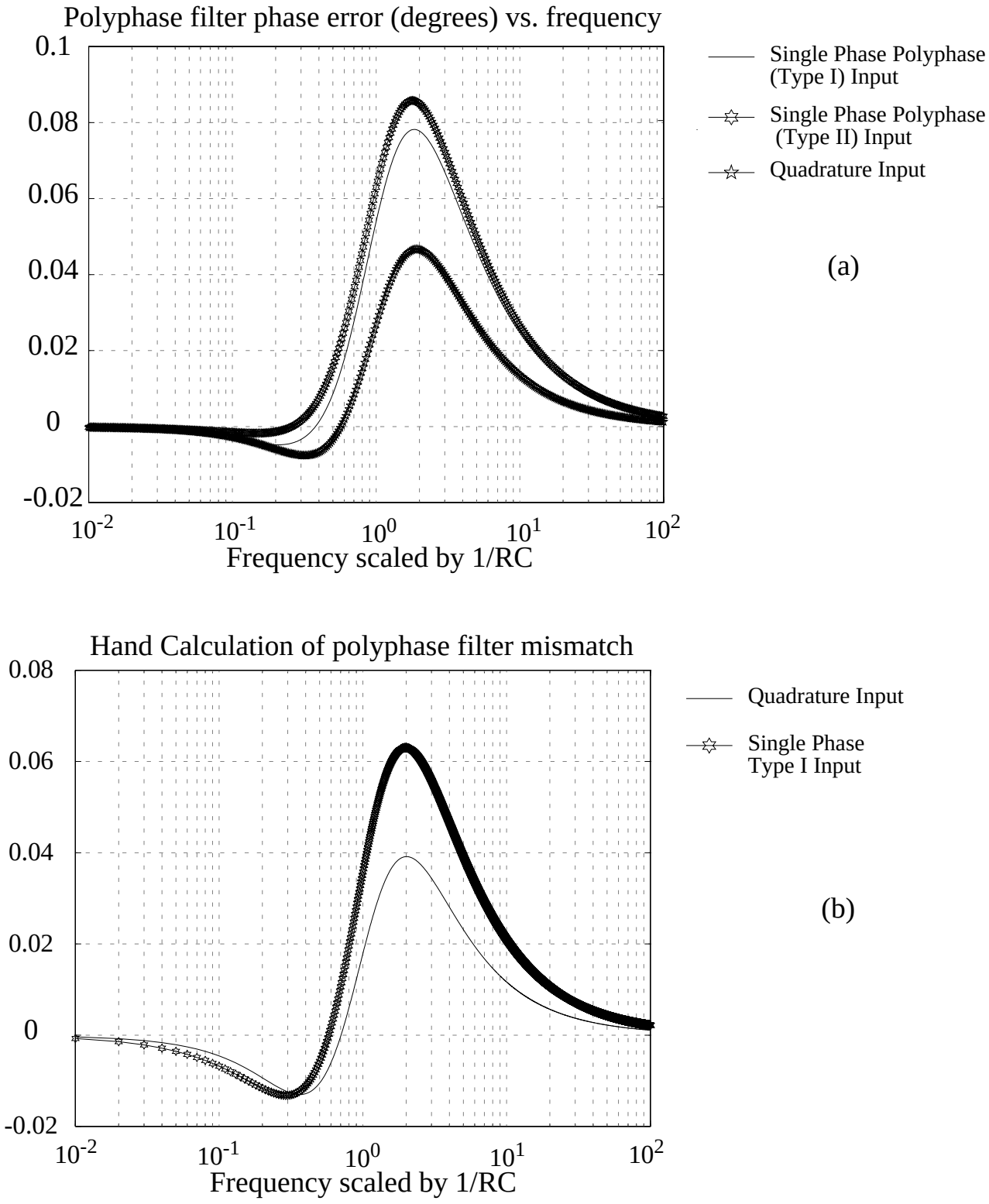


Figure 95. Phase error due to component mismatch in a single stage polyphase filter. (a) Results from SPICE simulations. (b) Phase from analytical expressions given in this section of the thesis.

a source which has a phase relationship that is at or near quadrature, has favorable characteristics in virtually ever category discussed in this section. However, the question remains as to how to generate a signal which is fairly close to quadrature to begin with, and apply this signal to the first stage of a polyphase filter. The realization of a quadrature signal source to a polyphase filter will be discussed in the section on filter implementation, section 7.2.6.

Although, polyphase filters have been demonstrated in applications where sideband suppression is required [7.7][7.8], the current discussion focus on the usefulness of polyphase filters for quadrature generation at approximately 1.5 GHz. The question at hand is how does the polyphase filter compare to the other two approaches discussed with respect to phase accuracy as a result of mismatch, gain matching, and phase sensitivity to process variations.

Table 3 gives a summary of the different characteristics of the phase shifting filters discussed in this section. It is clear that although the polyphase filter has considerable loss of carrier power, the potential advantages with respect to phase and gain accuracy become evident. A major advantage of the polyphase filter is the relative immunity that this filter has respect to component mismatch and process variation as well as the ability to broad band the quadrature phase.

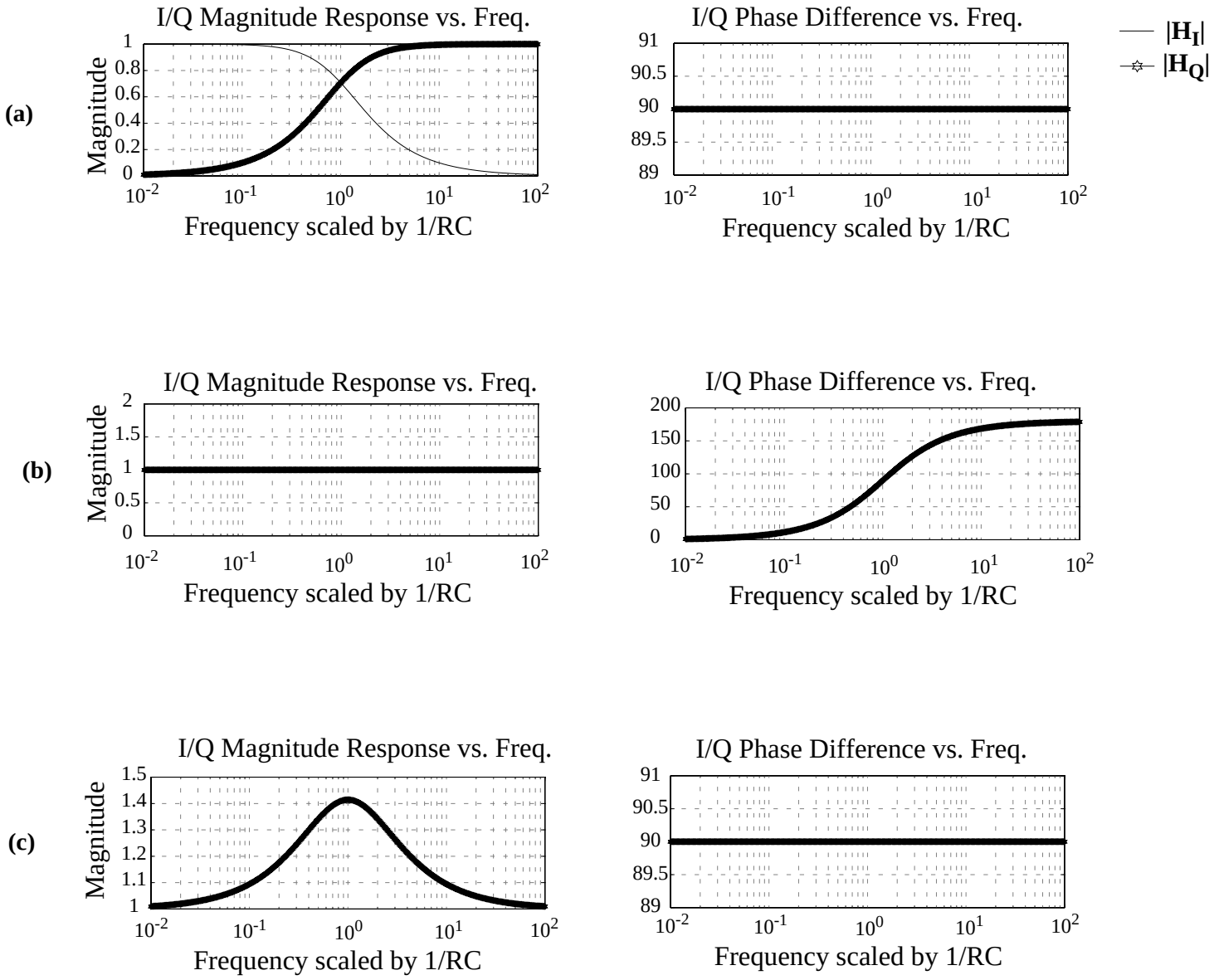


Figure 96. I / Q magnitude and phase response for a polyphase filter with various input phase configurations. (a) Single phase type I input (b) Single Phase Type II input (c) Quadrature Input

7.2.4.2 Summary of Phase Shifting filter characteristics.

Table 3 summarizes all of the characteristics of the various phase generation

	$\varphi(\omega, R, C)$	$\frac{d}{dR}\varphi(\omega, R, C)$	$\Delta A(\omega, R, C)$	$\Delta\varphi(\omega, \Delta R, \Delta C)$
RC-CR	90^{o} (Constant)	0 (Constant)	$\frac{\omega RC - 1}{\sqrt{1 + (\omega RC)^2}}$	$\operatorname{atan}\left(\frac{-\omega RC\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right)}{1 + \omega^2 (RC)^2}\right)$
Constant Magnitude	$-2\operatorname{atan}(\omega CR)$	$-2\left(\frac{\omega CR}{1 + (\omega CR)^2}\right)$	0 (Constant)	$2\operatorname{atan}(\omega RC) - \operatorname{atan}\left(\frac{2\omega RC\left(1 + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1 - (\omega RC)^2\left(1 - \left(\frac{\Delta R}{2R}\right)^2\right)\left(1 - \left(\frac{\Delta C}{2C}\right)^2\right)}\right)$
Single Phase Polyphase Filter (Type I input)	90^{o} (Constant)	0 (Constant)	$\frac{\omega RC - 1}{\sqrt{1 + (\omega RC)^2}}$	$4\operatorname{atan}(\omega RC) - 2\operatorname{atan}\left(\frac{2\omega RC\left(1 + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1 - (\omega RC)^2\left(1 - \left(\frac{\Delta R}{2R}\right)^2\right)\left(1 - \left(\frac{\Delta C}{2C}\right)^2\right)}\right)$
Single Phase Polyphase Filter (Type II input)	$-2\operatorname{atan}(\omega CR)$	$-2\left(\frac{\omega CR}{1 + (\omega CR)^2}\right)$	0 (Constant)	$2\operatorname{atan}(\omega RC) - \operatorname{atan}\left(\frac{2\omega RC\left(1 + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1 - (\omega RC)^2\left(1 - \left(\frac{\Delta R}{2R}\right)^2\right)\left(1 - \left(\frac{\Delta C}{2C}\right)^2\right)}\right)$
Polyphase Quadrature Input				$4\operatorname{atan}(\omega RC) - 2\operatorname{atan}\left(\frac{2\omega RC\left(1 + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1 - (\omega RC)^2\left(1 - \left(\frac{\Delta R}{2R}\right)^2\right)\left(1 - \left(\frac{\Delta C}{2C}\right)^2\right)}\right)$

Table 3: General frequency characteristics of three common quadrature generation filters.

filters discussed in the previous section. Each characteristic is given as a function of frequency.

Table 5 is identical to table 4 with the exception that all of the expression have been simplified to show only the particular characteristic at the 3dB frequency of the

poles and zeros with in the filter. Typically, all of the quadrature generation circuits discussed are designed to operate at or near the 3 dB frequency.

	$\varphi(\omega = 1/RC)$	$\frac{d}{dR}\varphi(\omega = 1/RC)$	$\Delta A(\omega = 1/RC)$	$\Delta\varphi(\omega = 1/RC, \Delta R, \Delta C)$(radians)
RC-CR	90^o (Constant)	0 (Constant)	0	$\approx\left(\frac{\Delta R}{2R}+\frac{\Delta C}{2C}\right)$
Constant Magnitude	$\approx 90^o$	$-1(\text{deg}/\Omega)$	0	$\pi/2 - \text{atan}\left(\frac{2\left(1+\frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1-\left(1-\left(\frac{\Delta R}{2R}\right)^2\right)\left(1-\left(\frac{\Delta C}{2C}\right)^2\right)}\right)$
Single Phase Polyphase Filter (Type I input)	$\approx 90^o$	$-1(\text{deg}/\Omega)$	0	$2\left(\pi/2 - \text{atan}\left(\frac{2\left(1+\frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1-\left(1-\left(\frac{\Delta R}{2R}\right)^2\right)\left(1-\left(\frac{\Delta C}{2C}\right)^2\right)}\right)\right)$
Single Phase Polyphase Filter (Type II input)	$\approx 90^o$	$-1(\text{deg}/\Omega)$	0	$\pi/2 - \text{atan}\left(\frac{2\left(1+\frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1-\left(1-\left(\frac{\Delta R}{2R}\right)^2\right)\left(1-\left(\frac{\Delta C}{2C}\right)^2\right)}\right)$
Polyphase Quadrature Input				$2\left(\pi/2 - \text{atan}\left(\frac{2\left(1+\frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1-\left(1-\left(\frac{\Delta R}{2R}\right)^2\right)\left(1-\left(\frac{\Delta C}{2C}\right)^2\right)}\right)\right)$

Table 4:

7.2.5 Polyphase Filter Design Issues

Once the determination has been made to use the polyphase filter for quadrature phase generation of the local oscillator, the issues associated with the implementation must then be addressed. In particular, the polyphase filter only accomplishes one of the two functions outlined at the beginning of section 7.2, the other functioning being the proper buffering of the synthesizer output. Simply connecting the polyphase filter directly to the VCO output would significantly reduce

the Q of the LC tank resulting in a degradation of the local oscillator phase noise performance. This then implies some method of buffering between the VCO output and polyphase filter input.

A simple method to shield the VCO from the polyphase is to utilize a pair of source followers at the input of the poly phase filter, this was proposed in [7.9] and is shown in figure 97. In this implementation, the loading on the VCO is almost purely capacitive. Thus, achieving one goal outlined in section 7.2, of providing the VCO with a capacitive output. However, for carriers in the 1-2 GHz range, the source followers (particular in a 0.35μm CMOS process) have a gain less than one as the C_{gs} of the source followers will act as voltage divider with the input capacitance or impedance of the filter, resulting in a net buffer gain of less than one. Depending on the selection of the Rs and Cs in this filter an additional 6 to 10 dB of signal attenuation will occur between the filter input and output. Therefore, because of the significant reduction in carrier power an additional buffer in [7.9] was required at the filter output, to drive the mixer capacitance. The composite power consumption of this buffer filter implementation was reported to be 100mW.

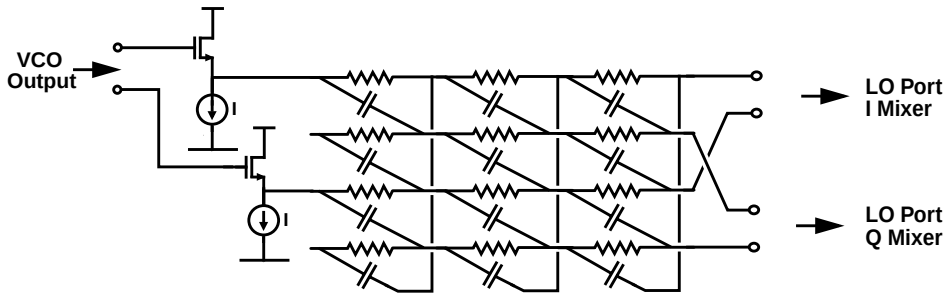


Figure 97. Source Follow with 3 stage poly-phase filter for quadrature generation. Source followers take 10mA per device.

An attempt was made to implement this filter/buffer topology illustrated in figure 97 for the GSM/DECT transceiver. However, it was found that only by consuming a prohibitively large amount of power in both the input and output buffers could attain a sufficient amplitude of the mixer LO input signal. Thus, alternative buffer/filter architectures were explored. In an attempt to reduce the power consumption

of the polyphase filter, it was desired to understand the mechanism of carrier loss in this filter topology. Either minimizing and or reducing the loss in carrier power, ultimately will reduce the need for power hungry buffers and or amplifiers.

In the section 7.2.4, simplifying assumptions were made with respect to the loading of the polyphase filter output. However, one significant contribution to the signal loss through a polyphase filter are several forms of parasitic capacitance. Although an exact analysis of the carrier loss as a function of parasitic capacitance is difficult to obtain, a more intuitive view is to simply look at the effect of loading a simple RC pole or zero with an unwanted parasitic capacitance as shown in figure 98(a). Here, it is clearly seen, that an input signal at the 3dB frequency, for either the case of a pole or a zero, will be attenuated by more than $1/\sqrt{2}$ when the output has additional undesired parasitic capacitance.

The parasitic capacitance within a polyphase filter arises from several sources. Wiring capacitance will exists between the resistors and capacitors as well as from the filter output to the mixer input. This is easily addressed with attention given to the layout. A second source of parasitic capacitance is dependent on both the method and the integrated circuit technology used to realize the individual capacitors. For the polyphase filter implemented in both the GSM/DECT and DECT receivers, the capacitors were implemented with two layers of poly. It is most obvious that an undesired parasitic bottom plate capacitance exists between the lower poly structure and the substrate of the chip, this is shown in figure 98(b). The last source of parasitic capacitance results from the output from the comprehensive capacitance at the output of filter. This capacitance is the result of wiring capacitance to the mixer as well as any gate capacitance associated with the mixer input and any capacitors used for AC

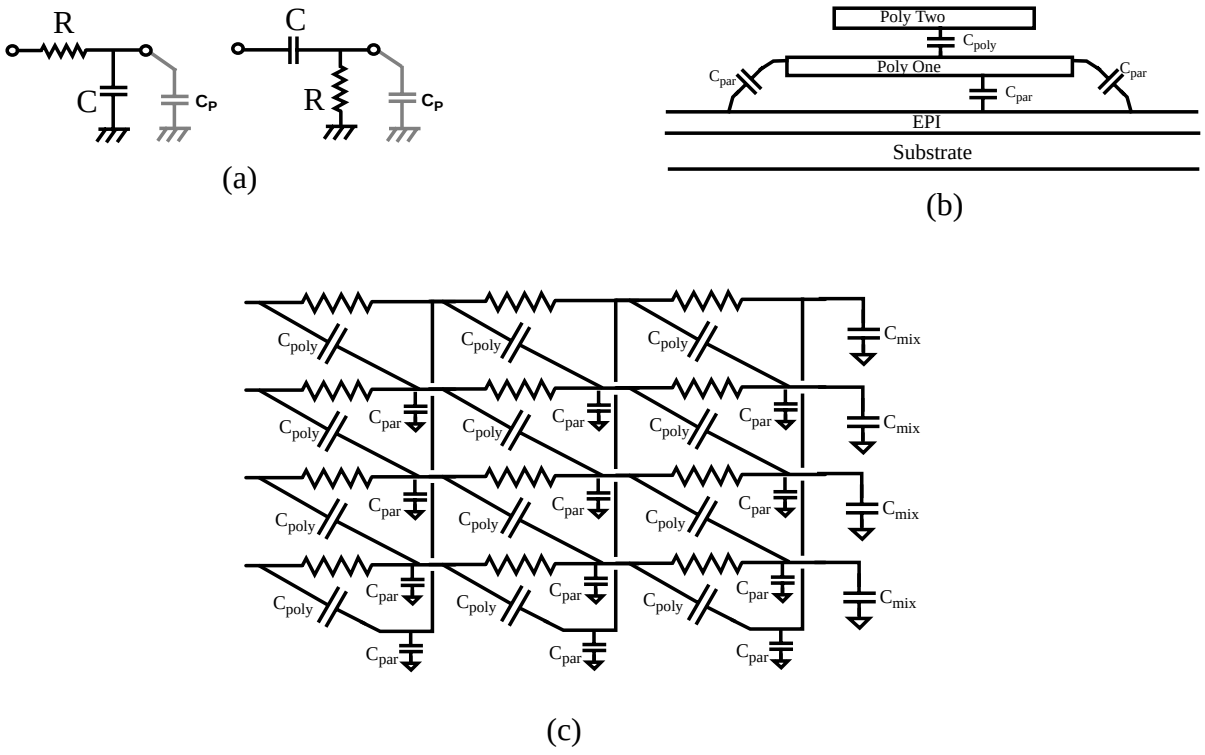


Figure 98. Non-ideal components contributing to the attenuation of the local oscillator input. (a) loading of an RC or CR by a parasitic capacitance. (b) Parasitic capacitance in a poly-poly capacitor. (c) Parasitic capacitance in a polyphase filter.

coupling. The location of each of these parasitic capacitors as they relate to a three stage polyphase filter are shown in figure 98(c).

In summary, the loss in carrier power can be attributed to three sources of parasitic capacitance. Understanding these losses will aid in the development of a buffer quadrature phase shifting circuit topology.

1) Mixer capacitive loading at the filter output, due to the mixer switching capacitance and the wiring capacitance.

2) Bottom plate parasitics of the polyphase capacitors.

3) Transition from a single phase input to quadrature phase from the filter input to the output, has a minimum loss of 3dB when operating at the filter half power point. This was discussed with the possible phases which can be applied to the polyphase in section 7.2.4.

Optimizing the mixer switching capacitance was discussed in chapter 6 and the minimizing the runner capacitance between the filter output and the mixer input, is simply a matter of good layout between the mixer LO input and the polyphase output. Also, using ac coupling capacitors between the mixer LO input and the polyphase filter output should be avoid, as this will further add parasitic bottom plate capacitance to the polyphase output. This suggests that the polyphase filter output can properly produce the common-mode required by the mixer LO mixer input port.

7.2.6 Miller Buffer Polyphase Quadrature generator

This section outlines the buffer and quadrature phase shifter that was used at the output of the first local oscillator in both the transmitter and receiver of the GSM/ DECT prototype. A similar, but less power efficient set of polyphase filters were design for quadrature generation of both LO1 and LO2 on the DECT receiver. Some guidelines for the synthesis of polyphase filters are outlined in this section.

A buffer and polyphase filter combination was developed by merging two of the previous quadrature signal generation techniques discussed in section 7.2.3 and section 7.2.4. To reduce the loss of carrier power attributed to converting a single phase input to a quadrature phase, a Miller buffer was used at the input of the polyphase filter as illustrated in figure 99. Again, using a vector signal representation for a single phase input in figure 99. The first buffer (left-hand side of figure 99), provides a 180^{o} phase shift relative to the input signal. The first buffer output is then applied to the input of a miller capacitance buffer. The output of the second buffer now has a 90^{o} phase shift relative to the output of the first buffer, thus providing roughly quadrature signals which are then applied to the polyphase filter.

The output of the first buffer drives the input impedance of the second buffer with the miller capacitance. Therefore, from the prespective of the VCO, capacitive loading is only attributed to one of the two buffers. In addition, the VCO almost sees a

pure capacitance looking in to the gates of M1 and M2 in figure 99. Both the reduced capacitance of just one buffer input as opposed to two and the elimination of the $1/(2g_m)$ component of the miller buffer input impedance described in section 7.2.3, will reduce the degradation of the LC tank Q as well as have a minimal impact on the effective reduction in tuning ranging associated with parasitic capacitances in the VCO tank.

The common mode input voltage to the mixer is provided with a common mode circuit comprised of a simple amplifier and M9 (see figure 96). A capacitor C_c is used between the gate of M9 and the supply to both provide compensation to the common mode feedback loop as well as improve the high frequency power supply rejection. This common mode feedback circuit eliminates the need for an AC coupling capacitor at the output of the polyphase filter. This again, reduces the capacitive loading at the polyphase filter output. This further reduces the loss to the carrier signal power which implies less gain and ultimately less power is required of the buffers that drive the filter input impedance.

Inductors L1 and L2 tune out both the total capacitance at the output of the first buffer, the input capacitance of the second buffer as well as the capacitance looking in to the polyphase filter. Likewise, L3 & L4 tune out the total parasitic

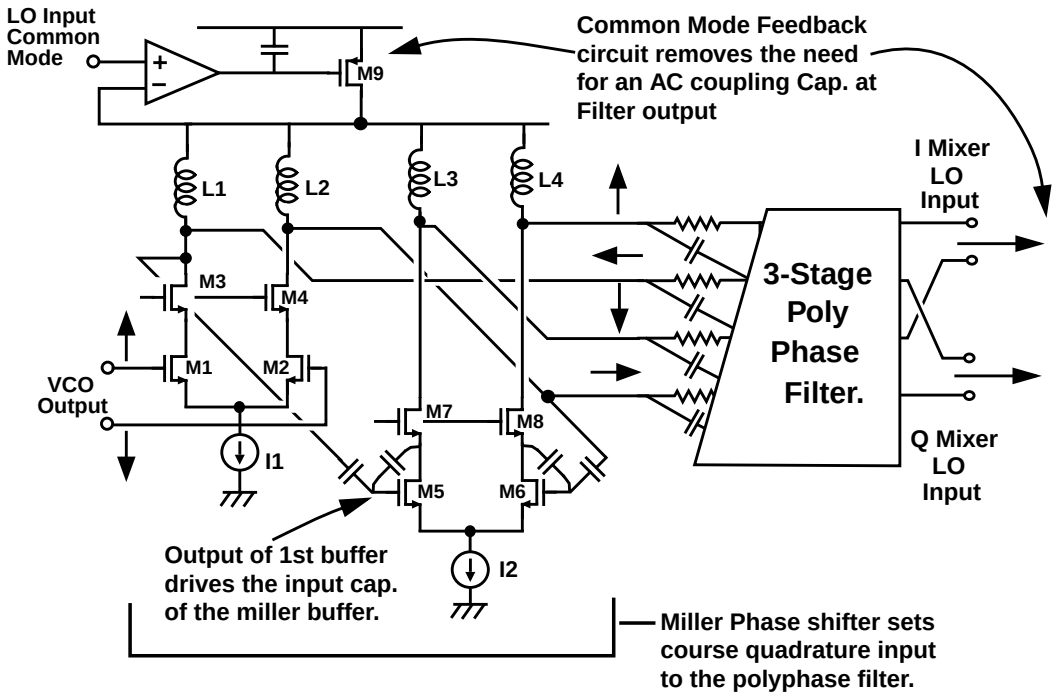


Figure 99. Buffer phase shifter combination circuit topology used for the receiver in the GSM/DECT project.

capacitance at the drains of M7 and M8, as well as the capacitance looking into the polyphase filter.

7.2.7 Device sizing.

With a definition of the buffer filter circuit topology a brief description is given for sizing some of both the passive and active components. This is followed with a few design examples which were used in the GSM/DECT prototype receiver and transmitter.

7.2.7.1 Inductor Sizing

The exact analysis of the input impedance looking into the polyphase is considerable complicated. However, if it is assumed that looking into the filter, there is a network of poles and zeros and the frequency of the carrier, and ultimately the

frequency that the inductor should resonant with the capacitance is near the 3dB frequency of the individual RC poles and zeros. Therefore the impedance looking into the filter network is relatively independent of the value of the RC components. Ultimately, to maintain the highest buffer gain with the minimum amount of power consumption it becomes obvious that developing the highest impedance possible at the buffer output is desired. The impedance looking into the filter is in parallel with the inductor impedance. This implies as high an inductance value as is possible to obtain both correct resonant frequency with the capacitance and ensure that the circuit is still operating below the self resonant frequency of the on-chip spiral inductors.

7.2.7.2 Polyphase filter R and C values.

As described earlier, a three stage polyphase filter was used in the implementation of all the polyphase filters both on the GSM/DECT transceiver as well as on the first generation DECT prototype. The value of the RC product is dependent on the frequency of operation. The first local oscillator operates at a fixed frequency and will determine the value of the RC product required to generate the proper phase. As mentioned earlier the parasitic bottom plate capacitance of the poly-poly capacitors will attenuate the carrier power. This then implies that it is desireable to have as low a C as possible while increasing the resistor value to obtain the correct 3dB frequency. However, another consideration is the additional noise contribution from the thermal resistors to the overall phase noise performance. Ideally both the polyphase filter as well as the buffer should have negligible contribution to the phase noise profile of the local oscillator. Again, an exact analysis of the contribution to phase noise from the resistors noise contribution in the polyphase, is rather involved. However, an upper bound to the resistor may be obtained by assuming that the resistors will only add white noise proportional to 4kT; although the noise will be colored by the frequency response of the filter. The sum of the three resistors in series should then add significantly less noise to the tail of the phase noise skirts. A rough estimate of the total resistance in one

of the four branches of the polyphase filter can be found by starting from the amplitude of the carrier at the output of the polyphase. This can be expressed as,

$$S_{carrier}\left(\frac{dBV}{Hz}\right) + PN(\Delta f_c)\left(\frac{dBc}{Hz}\right) = 10\log(4kT(3R)) \quad \text{(Eq 7.27)}$$

Where $S_{carrier}$ is the power spectral density of the carrier, PN the phase noise in dBc/Hz while Δf_c is the offset from the carrier. This expression is simplified as in most of the applications this circuit was designed for a carrier with a 1 volt amplitude. Therefore, equation 7.27 simplifies to,

$$PN(\Delta f_c)\left(\frac{dBc}{Hz}\right) = 10\log(4kT(3R_{max})) \quad \text{(Eq 7.28)}$$

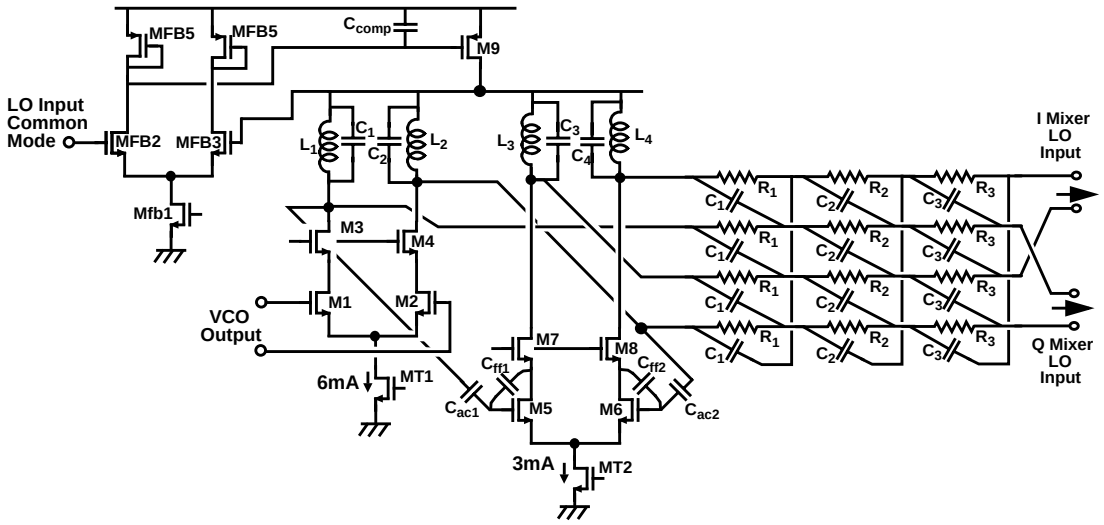
solving for R_{max},

$$R_{max} = \frac{10^{PN(\Delta f_c)/10}}{3 \cdot 1.667\times10^{-20}} \quad \text{(Eq 7.29)}$$

Using the value of R_{max} and the desired 3dB frequency the value of C is quickly found.

7.2.8 GSM/DECT LO1 Receiver Buffer Quadrature Phase Shifter.

The circuit topology shown in figure 99 was customized for the first local oscillator output of the GSM/DECT receiver. The phase noise floor required for this application is -155dBc/Hz. The value of R_{max} was then determined to be 6.32 kΩ. The operating frequency of the first local oscillator is nominally 1.5 GHz. Selecting the capacitor value of 16.7 fF would translate to a capacitance far too small for implementation by using poly-poly capacitor. Therefore, the capacitor sizes were selected such that the values were actually set slight higher then the target value. The LO common mode voltage require by the mixer switches is 1.8 volts. The bias voltage was generated using stacked diodes, designed using the relationship between voltage and the diode aspect ratio predicted in appendix K. The bias circuit was then designed to generate this voltage at the node designated “LO Input Common Mode” of 1.8 volts. From simulation the phase error between the I and Q mixer input ports was less than 1^o



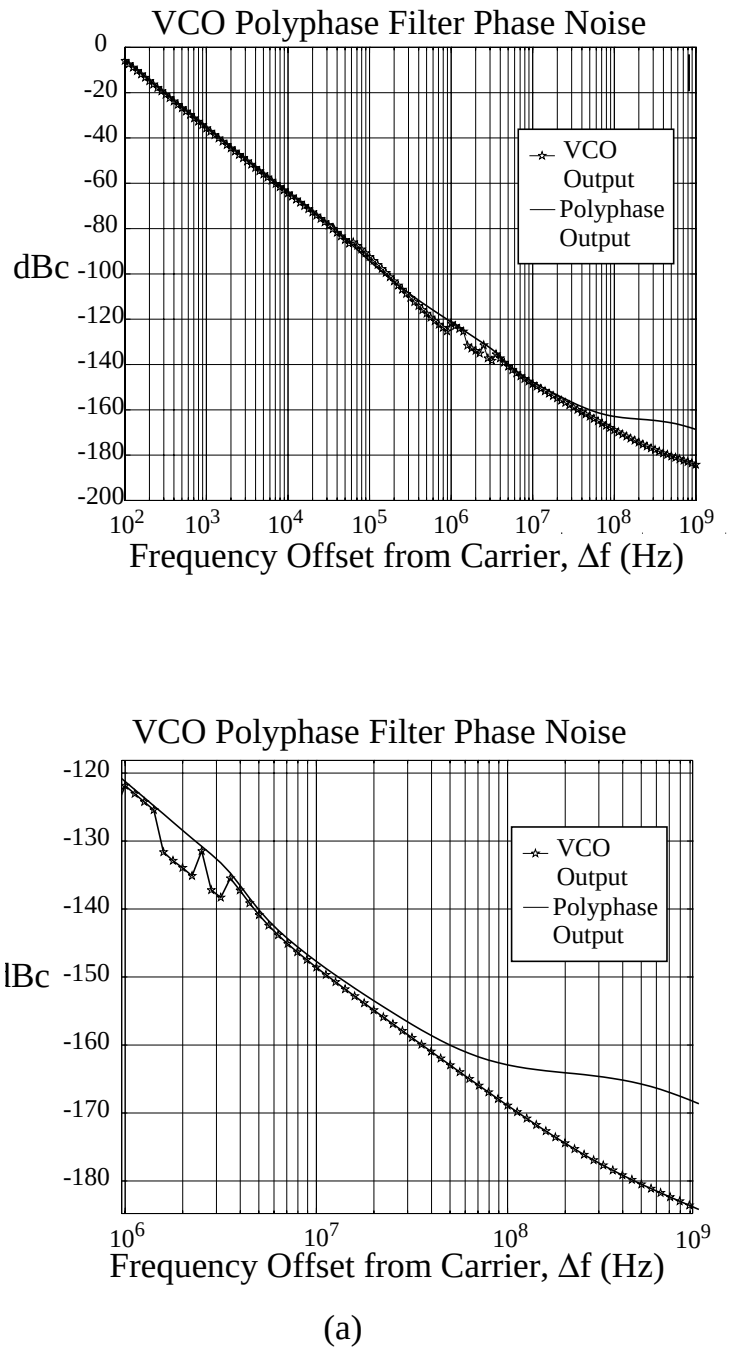
	R1	R2	R3	C1-C3	M1-M8	MFB2 MFB3	MFB5 MFB6	M9	L1 L2	L3 L4	Cac1 Cac2	Cff1 Cff2	C_{Comp}
Size	255	300	345	100fF	100(μm)/ 0.35(μm)	50(μm)/ 0.35(μm)	10(μm)/ 3(μm)	4000(μm)/ 3(μm)	8nH	11.4nH	200fF	550fF	8.3pF

Table 5: GSM/DECT LO1 receive buffer.

Figure 100. GSM/DECT LO1 receive buffer.

over process. The LO carrier amplitude variation at the mixer LO input ports ranged from 800 mV to 1 V over process.

Figure 101 shows the results of a periodic steady state analysis run using SpectraRF. This simulation was performed with all the bias circuitry along with the VCO. Note that the buffer and polyphase filter combination have a negligible contribution to the phase noise profile.



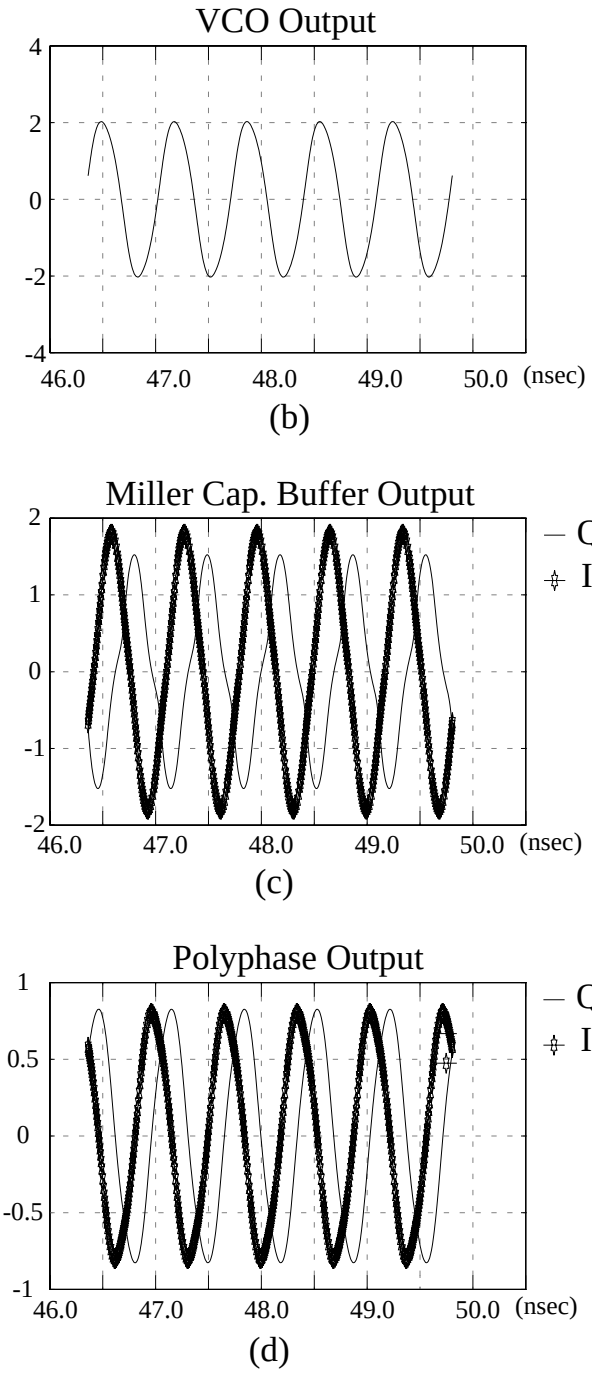
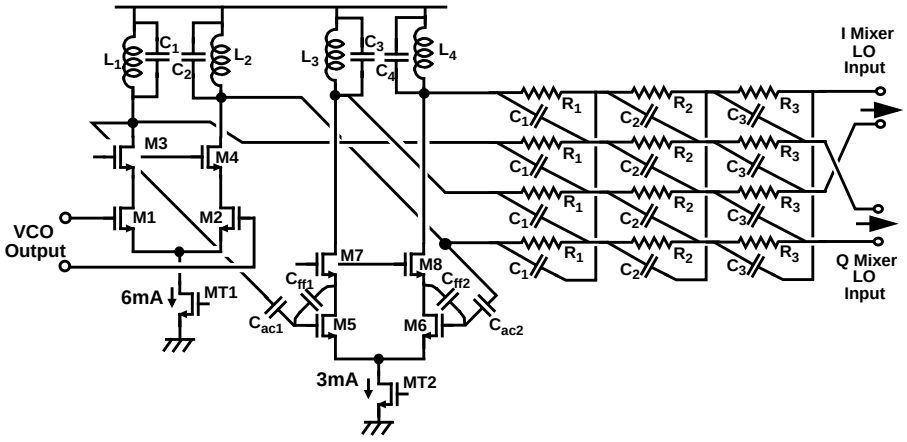


Figure 101. Results of SpectraRF simulation on the VCO and Miller-Buffer-Polyphase filter combination. (a) Phase noise power spectral density relative to the carrier frequency. Time domain waveforms shown for the (b) VCO output (c), output of the Miller Buffer, (d) output of the polyphase filter.

7.2.9 GSM/DECT LO1 Transmit Buffer Quadrature Phase Shifter.

A similar buffer filter combination was utilized for the transmitter in the GSM/ DECT prototype. Slight modifications were made to accommodate the transmit mixers. This circuit was made considerable simpler as the desired common mode input voltage at the filter output, is VDD. However, the quadrature accuracy of the I and Q filter output was much more stringent than the receiver as there is no tuning of the quadrature generator used by the second local oscillator as is the case with the self-calibrating mixer. A circuit diagram is given in figure 102, note the absence of a common mode feedback circuit. The carrier frequency of this polyphase filter is approximately 1.5 GHz and the total power consumption is 27mW from a 3.3 V supply.



	R1	R2	R3	C1-C3	M1-M8	MFB2 MFB3	MFB5 MFB6	M9	L1 L2	L3 L4	Cac1 Cac2	Cff1 Cff2
Size	255	300	345	100fF	100(µm)/ 0.35(µm)	50(µm)/ 0.35(µm)	10(µm)/ 3(µm)	4000(µm)/ 3(µm)	8nH	11.4nH	200fF	550fF

Table 6: GSM/DECT LO1 receive buffer.

Figure 102. GSM/DECT LO1 receive buffer.

7.2.10 DECT LO1 and LO2 Quadrature Phase Shifter.

In the DECT receiver, both frequency synthesizers were intended to utilize ring oscillator VCOs which inherently produce quadrature signals. This was allowed as

the image suppression required by the mixers was relatively moderate when compared to GSM. Although the intention was to integrate the DECT receiver with the synthesizer this portion of the receiver was never fully completed. Therefore, the test data which is covered in chapter 8, was realized with only the receive signal path integrated from the LNA input through the ADC output. Originally, the DECT receiver was intended to be integrated with a phase-locked-loop which utilized a ring oscillator based VCO which would also generate quadrature signals. However, some difficulty was encountered when implementing this synthesizer. Therefore, a relatively crude design was implemented on chip, to generate quadrature signals using polyphase filters and warrants some discussion. However, it must be emphasized that this design was intended for testing purposes only and little attention was paid to optimizing the power consumption of the buffers and filter combination.

In the DECT receiver, a polyphase filter was utilized to generate quadrature signals for both the first and second local oscillators. The polyphase filter topology used by the DECT receiver is shown in figure 103. The signal input in this device was brought in off chip and applied to the source follower inputs. After passing through the polyphase filter the signal was then amplified using a three stage differential pair buffer. A unique feature of this quadrature signal generate was the ability to tune the phase by varying the bias current in one set of buffers relative to the other set. By adjusting the tail current through the buffer, the delay of the buffer circuit could be

varied ultimately modifying the phase at one filter output relative to the other. This is illustrated in figure 103.

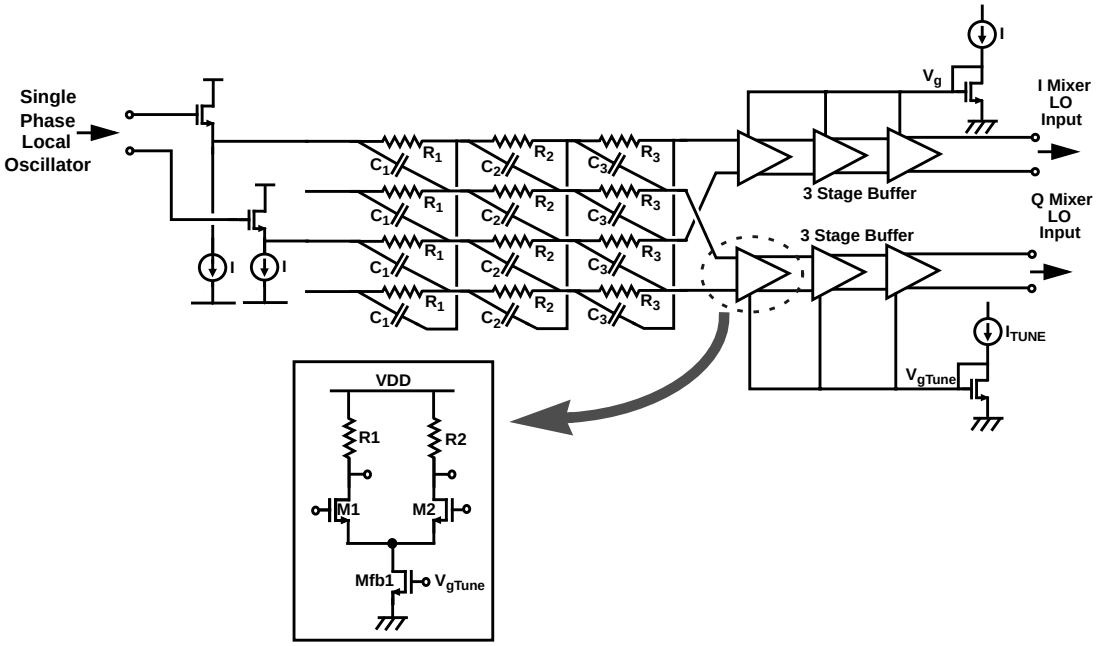


Figure 103. DECT LO1 receive buffer.

7.3 IF Quad. Generation Circuit (LO2) for Self-Calib. Mixer

In the previous section, there were some comparison of the different methods which can be used to generate quadrature signals using passive RC filters. All of the previous approaches discussed utilize a single phase signal at a particular frequency and generate quadrature signals at the same frequency. Now the focus will be on quadrature generation circuits that not only take a single phase signal at the input and produce two channels with a 90^o phase difference, but also divide down in frequency the input signal. An additional objective for this particular phase generator is with respect to the adaptive image-rejection mixer discussed in chapter 7. For this image-rejection mixer the should be close to 90^o but also have the ability to tune the phase between the I and Q local oscillator signals. The control for the tuneable phase shifter will be provided by the digital baseband. Therefore, the input to the tuner is digital implying that the circuit

which controls and generates the quadrature signals must map a digital, input to a corresponding change in phase.

Section 7.3 begins with a quick review of the adaptive image-rejection mixer and how the variable phase shifter fits into the overall mixer system. A discussion is then given on the implementation of the D-latches which were utilized to divide the synthesizer output by four and produce quadrature signals. The divide-by-four latches are followed by a set of buffers which drive the capacitance looking into the switches of the gilbert cell mixers. These buffers are were the phase tuning actually takes place. To understand how the phase is tuned with the buffers a more through discussion is given with respect to tuning the phase between two signal paths using a basic one pole RC response. Results used from this section are then applied to the design of a buffer which implements the phase tuning, a description of some of the circuits which support this buffer are given. Section 7.3 concludes with some simulation results of the phase tuning circuits. It is worth mentioning that these circuit were only utilized for the 2nd generation DECT/GSM receiver.

7.3.1 The Adaptive Image-Rejection Mixer and the LO2 Phase Shifter

Before continuing with a discussion of the implementation of the LO2 phase shifter with digital tuning, the placement of the tuneable phase shifter in the adaptive image-rejection mixer will be reviewed. Shown in figure 104 is the block diagram of the adaptive image-reject mixer system. These blocks are shown as implemented in the DECT/GSM receiver, the output of the second local oscillator is feed into a set of D-latches which performs a divide by 4 of the oscillator carrier frequency and generates quadrature signals (see figure 104). The quadrature output of the latches are then applied to a series of buffers which serve a dual function of both driving the mixer local oscillator switches and tuning the local oscillator phase for maximum image suppression. Therefore, the approach used to implement the tuneable phase shifter was

to first generate roughly quadrature signals using the D-latches, the output of these latches are then finely tuned to correct for the comprehensive phase error due to the mismatch in the quadrature generator of the first local oscillator, the potential phase error in the mixer signal path, and the quadrature phase error of the second local oscillator output (this would be the phase error from the divide by four latches and any mismatch in the mixer input switches).

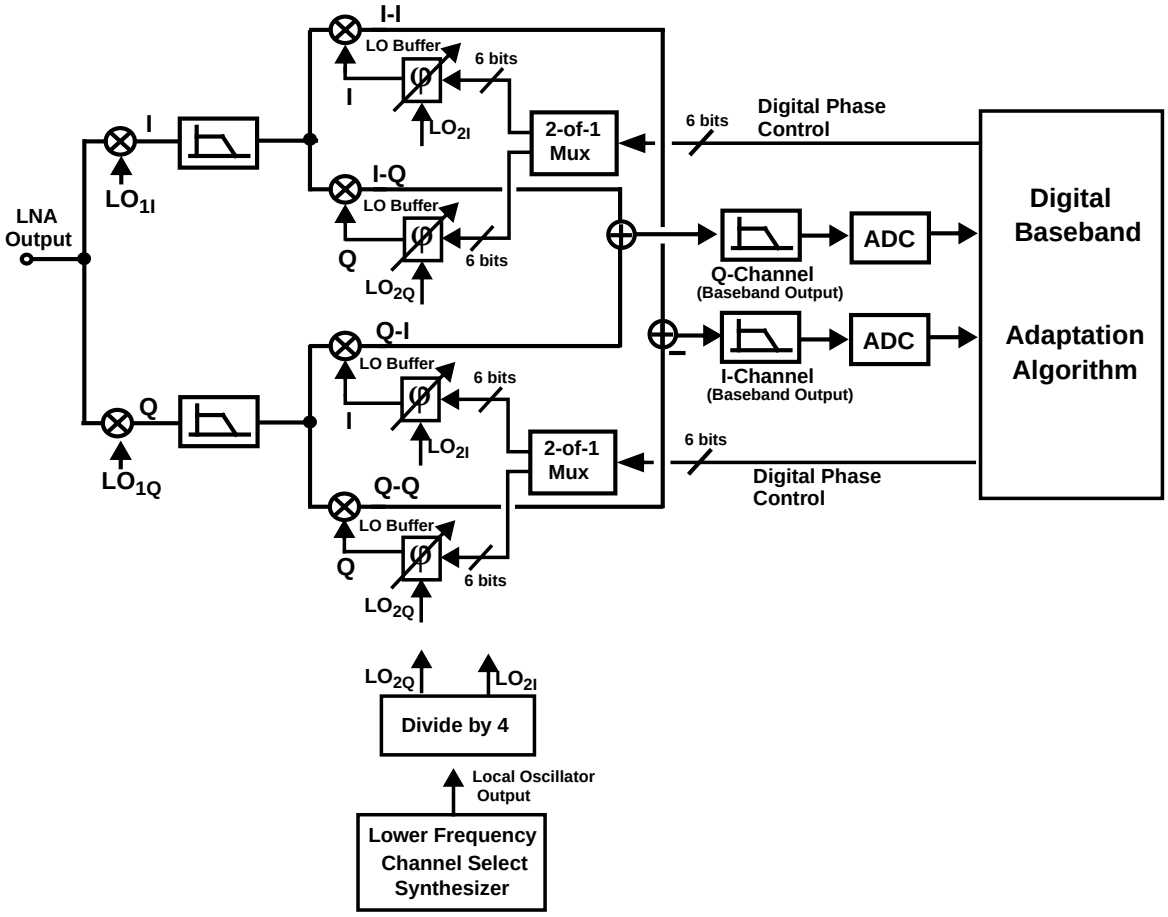


Figure 104. Adaptive Image-Rejection mixer implemented for the GSM/DECT receiver. The output of the the second local oscillator is applied to a divide by 4 block generating rough quadrature then finely tuned for maximum image suppression.

Not shown in figure 104 is the digital control for the gain tuning in two of the four mixer paths. This required an additional 12 bits of control from the digital baseband. This brings the total number of bits required from the baseband to 24. It was desired to use the digital input of the transmitters DAC to feedback the bits from the

DSP. However, the transmitter for the GSM/DECT transceiver used two 10bit DACs implying that there is only a total of 20 bits for the receiver to use for adaptation. Therefore a set of 2-1 multiplexers were used for the phase and gain tuning of the mixer. Care was taken in selecting which digital phase and gain tuners would be available at any instant; obviously access to all six bits of an individual phase tuner would be required at a given time for tuning. With the multiplexer using one set of inputs from the baseband the adaptation algorithm would be used to tune for maximum image-rejection. Once the first set of either gain or phase error has been tuned the multiplexer is then set such that the alternate set of tuners is connected to the baseband DSP and the adaptation algorithm is again used to further improve the image suppression of the mixer system.

7.3.2 Implementation of the divide by four quadrature generation circuit

The divide by four circuit show in figure 104 was implement with a pair of master-slave D-Latches configured as shown in figure 105. The output of the frequency synthesizer is used to clock two positive-edge triggered D-latches and a complementary pair of negative-edge triggered D-latches. A timing diagram of the divide by four block shown in figure 105 illustrates that the waveform at the output of each latch has 4x the period of the local oscillator input. In addition to generating four phases, each latch output ideally has a 90^{o} phase difference with the previous and subsequent latch outputs. The state diagram, also shown in figure 105, reveals that the latches will flow into the proper sequencing of states independent of the initial condition on power up.

This obviates the need for a reset circuitry to guarantee that the latch remains in one of the desired states.

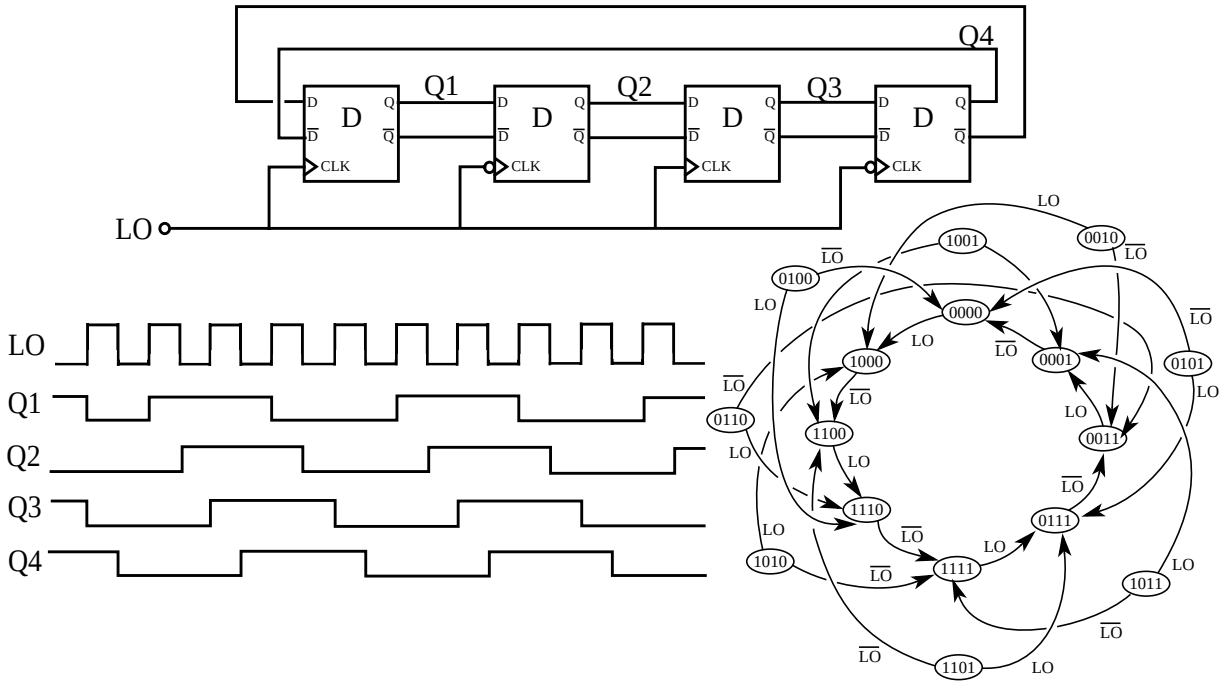


Figure 105. D-Latches configured to perform a divide by four and generate quadrature signals. Also shown, are the timing and state diagrams.

The individual latches in the divide by four were implemented using source-coupled logic. One master and one slave are shown in figure 106. In general, the individual digital components are realized with a common source differential pair with a tail current source. Although there is static power consumption associated with source coupled logic, the benefit lies in the fact that the switching current, to both the ground and from the supply are ideally zero. Generally speaking, isolating or reducing supply and substrate noise from many of the sensitive analog receiver components is essential to achieve high selectivity performance. This is particularly true for the synthesizer which can easily generate spurious components through noise or interference coupled in through the supplies and ground. The circuit shown in figure 106, has and additional

benefit of a fully differential structure which increases the rejection of undesired signal components coupled in through the supply and ground.

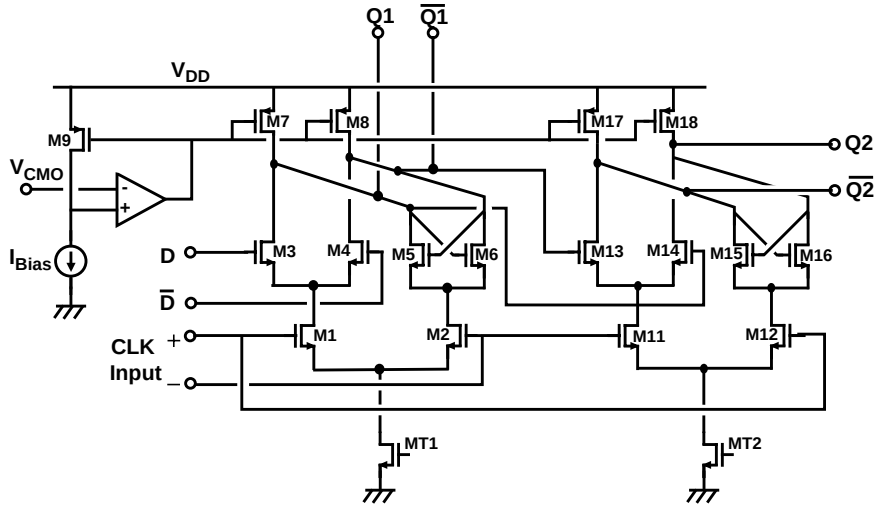


Table 7:

Device	Size
M1-M2	10µm/0.35µm
M3-M6	5µm/0.35µm
M7-M8	7.5µm/0.35µm
M11-M12	10µm/0.35µm
M13-M16	5µm/0.35µm
M17-M18	7.5µm/0.35µm
MT1-MT2	200µm/3µm
VCMO	2.3Volts

Figure 106. One of two source-coupled master slave D-Latches used to both generate quadrature signals and divide the synthesizer frequency by a factor of four.

The output of the channel select frequency synthesizer in the GSM/DECT receiver is applied to the port labeled “CLK Input” in figure 106. When the differential clock signal is high, current flows through M1 as well as M3 and M4 allowing the evaluation of D and D sets the logic value of Q1 and Q1. When the differential clock signal goes low, M1 is cutoff will M2 is turned on and current flows through the cross-coupled pair M5 and M6. The positive feedback associated with the cross coupled pair M5 and M6 ensure the value of Q1 and Q1 are latched to the output on the negative phase of the master latch input signal. Likewise, the polarity of clock input signal is reversed when applied to M11 and M12 which insures that the output of the first latch is evaluated latched to the output on the positive clock edge.

Triode region PMOS resistors are used to load the output of the latch. The swing and the bandwidth of the output signal are determined by VCMO and the current through the latch tail current. The required voltage swing of both the next latch stage and the output buffer (not shown in figure 106) will determine the value of VCMO. The

total latch load capacitance and the needed bandwidth will dictate the value of the load resistance and ultimately the required tail current.

Similar to a mixer, the low frequency noise of the tail current devices MT1 and MT2 can be upconverted or mixed in band with the desired signal. . For the circuit shown in figure 111, the input device M1 is turning on and off at the rate of the local oscillator input which will have the affect of modulating the 1/f noise from MT1 to the frequency of the latch input clock signal. However, the zero crossing of the latch output will be affect by the noise introduced by MT2.

The 1/f noise from a single device was determined through simulation and used to size the device accordingly.

7.3.2.1 Phase Tuning with a Replica Biased Buffer.

As was mentioned earlier, the tuning of the phase and the buffering of the mixer capacitance are done using the same circuit. Although there are potentially a number of different circuit implementations which could realize this tuning function, a buffer with replica biased PMOS devices was selected to perform the tuning function because of the ability to modulate the phase utilizing a current source. The basic circuit is shown in figure 110. The input to the buffer is the output of the divide by four D-Latches described in the previous section. In the replica bias buffer, the PMOS load devices are biased in the triode region with an opamp that compares a parallel transistor (shown as M3 in figure 107). The feedback of the opamp modulates the gate voltage of all the PMOS devices forcing the drain-to-source voltage of M3 to equal V_{sw}. If the input devices M1 and M2 are driven with a signal which is greater than $\sqrt{2}(V_{gs} - V_t)$ in amplitude, then one of the two devices will conduct all of the tail current while the other is in the cut-off region. In other words, the input devices are acting like switches when sufficiently over driven. With all the output current flowing through one leg of the buffer, the output voltage on corresponding side of the buffer will drop from Vdd to

V_{dd}-$I_{tail}R_{PMOS}$. The drain-to-source resistance R_{PMOS} of M3, M4, and M5 are set by forcing a current I_{TAIL}(or scaled version of the tail current) through a parallel PMOS device and comparing the VDS of the replicated PMOS device to a desired VSW via an opamp which modulates the gate voltage of all the PMOS devices, this is shown in figure 107. If all of the PMOS devices are sized such that the V_{gs}-V_t of each device is greater than the V_{DS}, then the PMOS channel resistance R_{PMOS}, can nominally be approximated as VSW/I_{tail}. In practice this estimate is accurate for M3, however, the channel resistance of M4 and M5 are only equal to V_{SW}/I_{tail} which V_{op}, V_{on} are on the low end of their swing.

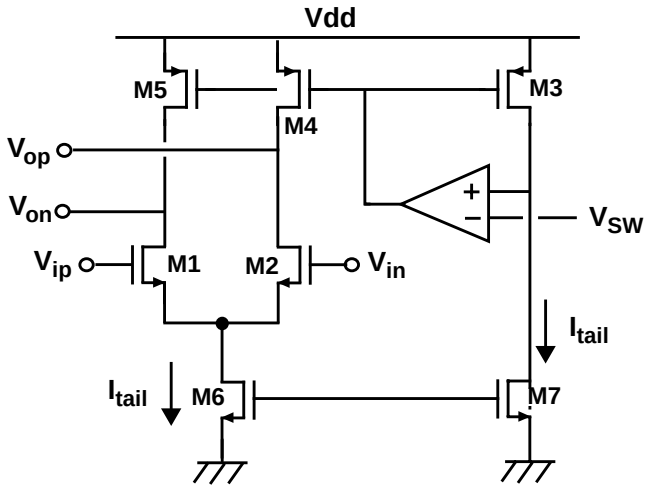


Figure 107. Buffer circuit loaded with replica biased PMOS triode region devices

If the buffer input differential pair is overdriven and assuming that the buffer is not slew rate limited at the output, the shape of the output voltage waveform is exponential. This is similar to the linear settling in a switched-capacitor integrator stage. Both the single ended and differential signals at the output exhibit an exponential characteristic in the output waveforms, this is shown in figure 108. At the output of the divide by four circuit, the signals are approximately in quadrature. These quadrature signals are passed through the replica biased buffer before being applied to the mixer input. The objective is to now finely tune the phase, at the output of one buffer, relative

to the other buffer. This is accomplished by change the drain-to-source resistance of the replica biased PMOS devices. By modulating the value of R_{PMOS}, the rise time of the exponential curve in one path maybe changed relative to the other path.

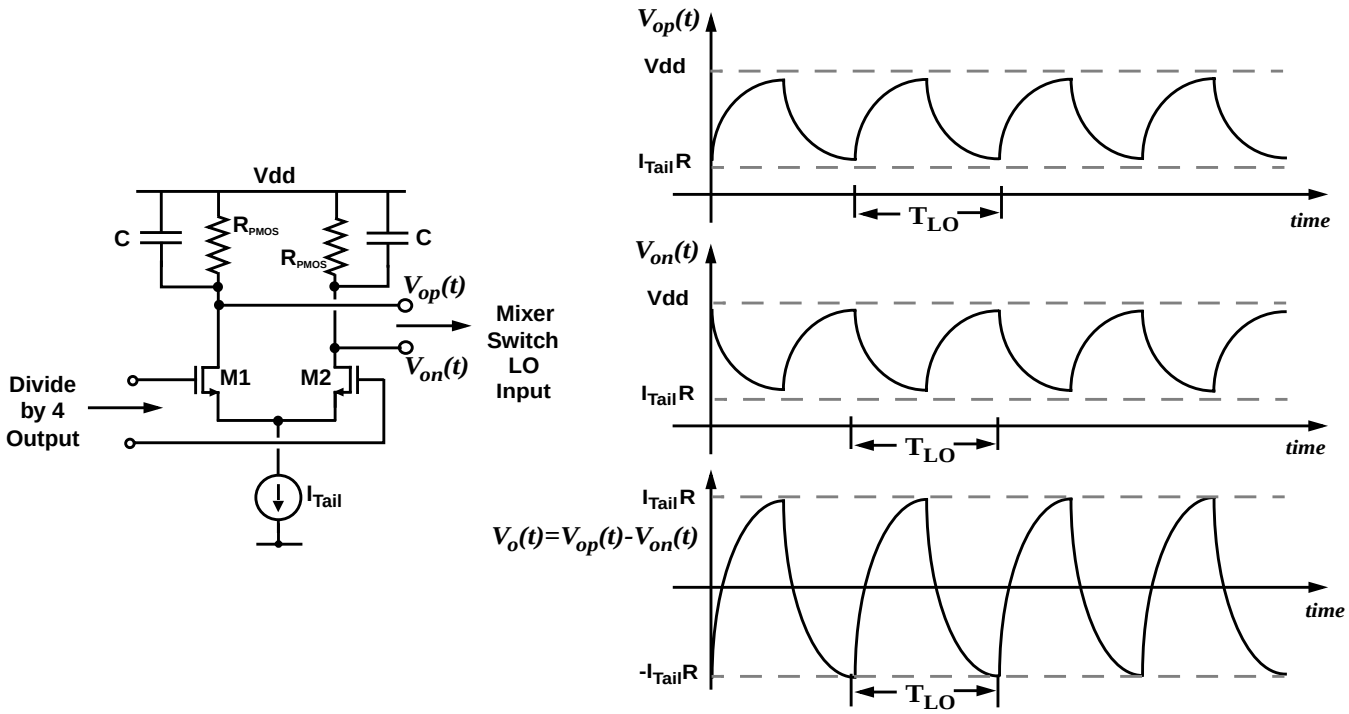


Figure 108. Resistively loaded buffer with output waveforms.

In one path (use the I path as an example), at the output of the dividers, a buffer is used with a fixed load resistance. The other path (Q output) a buffer is used with circuit where the R is modulated from its nominal value. In both buffers, assume that the output resistance is a fixed value for the entire swing (this isn't true as the resistance of both devices changes across the entire swing), an estimate may be made for the change in phase of the Q buffer, as a function of the amount that the load resistance has been modulated. It must be kept in mind that the objective is to finely tune the phase of the Q buffer such that the total phase difference between the I and Q buffers is 90^o, plus the amount needed to compensate for the total phase mismatch between two of the image-rejection mixer channels. An illustration of the desired affect

on the phase between the I and Q second local oscillator channels is illustrated in figure 109. Here, the I buffer has a fixed load resistance. However, the at the output of the Q buffer, the resistance is increased by ΔR above some nominal value. This then causes the output of the buffer to settle slightly slower than the case of the buffer with a nominal load resistance. The point of interest where the phase affects the mixer switches is when the differential output signal pass through the zero crossing. This time corresponds to the point where the single ended signal is approximately half way to its final value, where the final value will be defined as the point immediately before the single ended buffer output reaches its lowest value and begins to rise up in the direction of the rail. When the single ended signal reaches the mid-

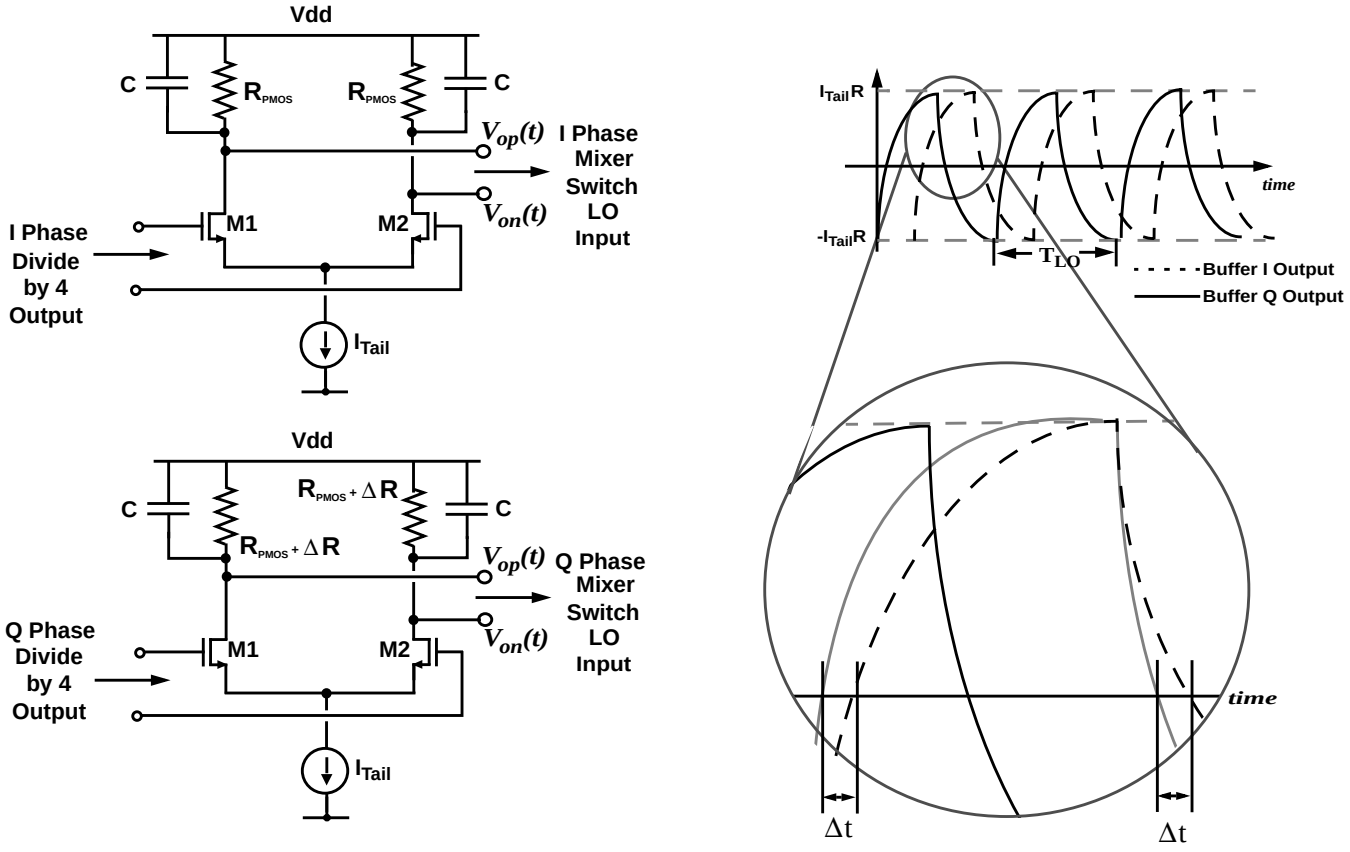


Figure 109. Conceptual illustration of incrementally modulating the zero crossing, Δt, (modulating the phase) of one buffer relative to another buffer by varying the load resistance.

point some interesting observations may be made. For the I output we can define the single ended output voltage as a simple exponential equation,

$$V_{Qo}(t) = V_{sw}\left(1 - e^{\frac{-t}{RC}}\right) \quad \text{(Eq 7.30)}$$

Now it is desired to find out what affect adding a small amount of resistance ΔR has on the both a time delay Δt at the differential zero crossing. Defining $V'Q_o(t)$ as the single sided voltage swing of a buffer with ΔR, added to the load resistance, this can be written as,

$$V'_{Qo}(t) = V_{sw}\left(1 - e^{\frac{-t + \Delta t}{(R + \Delta R)C}}\right) \quad \text{(Eq 7.31)}$$

Again, by definition Δt and ΔR are defined as the output voltage at mid-swing. To determine Δt as a function of ΔR, equation 7.30 is set equal to equation 7.31. Solving some simple algebra reveals that ΔR can be expressed as,

$$\Delta R = \frac{\Delta t \cdot R}{t_{mid}} \quad \text{(Eq 7.32)}$$

Where t_{mid} is defined as the time it takes for one side of the differential pair to go from full swing to the mid-voltage (again, corresponds to the zero crossing differentially). By solving equation 7.30 for t_{mid} results in.

$$t_{mid} = \ln\left(\frac{1}{2}\right)RC \quad \text{(Eq 7.33)}$$

Using equation 7.33 in equation 7.32 an expression can be obtained for the ΔR as function of Δt and C.

$$\Delta R = \frac{\Delta t}{\ln\left(\frac{1}{2}\right)C} \quad \text{(Eq 7.34)}$$

The objective in the design of the buffer is to understand what ΔR is require to produce the needed change in phase or resolution in phase. Δt can be expressed as a difference in phase between a nominal buffer with load resistance R and the same buffer with load resistance $R+\Delta R$ with,

$$\Delta\varphi = \frac{\Delta t}{T_{LO}}360 \quad \text{(Eq 7.35)}$$

Where TLO is the period of the local oscillator coming out of the divide by four. Substituting the above into equation 7.34 and expressing the LO period in terms of frequency gives.

$$\Delta R = \frac{\Delta\varphi}{f \cdot \ln\left(\frac{1}{2}\right) \cdot C \cdot 360} \qquad \text{(Eq 7.36)}$$

ΔR is now given as a function of the required resolution in phase, the carrier frequency and the load capacitance. The interesting observation to make is that the difference in phase between the I and Q buffers (or Δt) is independent of the absolute value of R and only depends upon the difference between the load resistance in the two output buffers. In addition, equation 7.47 reveals that the smaller the load capacitance, the larger the ΔR required to obtain a given $\Delta\varphi$. The higher the LO frequency the smaller the required ΔR. For the replica biased buffer, the ΔR is created by modulating the current through the PMOS devices. The larger the required resolution in resistance, the easier it becomes to implement the current DAC which ultimately modulates the resistance. Less load capacitance is also desireable from the perspective of burning less power. More generally speaking, this buffer is working on the synthesizer which performs the channel selection. Therefore, the worst case required resolution in R is at the highest frequency.

Although, the analysis to determine Δt assumed that the load resistance R_{PMOS} is constant across the entire output swing, in practice this isn't quite true. The resistance of the triode region PMOS load devices is a function of the drain-to-source voltage of this device. Therefore, the resistance of the output device changes throughout the entire swing of the output voltage. Assuming classic square law devices, the resistance of PMOS device can be expressed as,

$$R_{PMOS} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{gs} - V_t) - \frac{V_{ds}}{2}\right]} \qquad \text{(Eq 7.37)}$$

Where V_{ds} is obviously V_{dd}-$V_{Qo}(t)$. The expression for the single sided output voltage of the buffer is now more accurately described by.

$$V_{Qo}(t) = V_{sw}\left(1 - e^{\frac{-t}{R(V_{Qo}(t))C}}\right) \quad \text{(Eq 7.38)}$$

Equation 7.38 comes closer to equation 7.30 when the V_{gs}-V_t of the PMOS devices is made as large as possible compared to V_{ds}, which on the low end of the swing is V_{dd}-V_{sw}. With the V_{gs}-V_t of the PMOS device maximized, the modulation of the channel resistance is minimized. Although, equation 7.35 and equation 7.36 were derived assuming a constant load resistance, these estimates still come close to the actual change in phase when the channel resistance changes while the output voltage is changing.

With an understanding of the basic operation of this variable phase shifter, the question now arises as to the design of the components in this buffer. The greatest impact on the performance of this buffer is the selection of the design of the load resistance, some care must be used in selecting the value of R. Mainly, selecting the value of R ultimately has an impact on the amplitude of the LO carrier at the buffer output and the tail current power consumption. Ultimately, the lower the value of R, the faster the circuit can operate. However, this requires more tail current and power as the PMOS resistance is V_{sw}/I_{Tail}. Therefore, it is really desired to have as high a value of R as can be tolerated. The two primary considerations which define an upper limit to the value of the output resistance are the phase noise produced by the circuit and as mention the speed.

From the perspective of phase noise, the PMOS devices should be sized such that their resistance at the differential zero crossing has negligible contribution to the phase noise floor. Because the resistance of the triode region devices is changing throughout the output voltage swing, the resistance that will most influence the phase is again, when the differential voltage is zero, or the singled output voltage has reached the mid-voltage swing. A relationship between the resistance at middle of the single-sided voltage swing and the peak triode region load resistance is given in the appendix I as,

$$R_{mid} = R_{peak}\frac{(\zeta - 1)}{(\xi - 1/2)} \quad \text{(Eq 7.39)}$$

Where $\zeta = (V_{gs} - V_t)/V_{sw}$ and R_{peak} is simply the resistance at full output swing or $R_{peak}=V_{sw}/I_{Tail}$. Next, the required phase noise floor relative to a 1V carrier will be defined as PNF. To have a negligible contribution to the phase noise floor, the resistance at the zero crossing should be selected such that there is a 6dB margin between the phase noise floor and thermal noise produced by the resistor. The value of the triode region resistance at mid-swing should be no more than.

$$R_{mid} \le \frac{10^{\frac{(PNF-6)}{10}}}{4kT} \quad \text{(Eq 7.40)}$$

Using the relation given in equation 7.39 and equation 7.40 and the relationship between R_{peak} and I_{Tail}, a relationship for the minimum require tail current of the buffer may be found for a given phase noise performance.

$$I_{Tail} \ge \frac{V_{sw} \cdot 4kT}{10^{\frac{(PHF-6)}{10}}}\frac{(\zeta - 1)}{(\xi - 1/2)} \quad \text{(Eq 7.41)}$$

An additional limitation to the maximum resistance which may be used is the overall bandwidth of the buffer. As mentioned earlier, the voltage output waveform has a sawtooth shape. This is due to the exponential behavior of the output. Similar to the settling of a switched capacitor integrator stage, the less bandwidth, the more time it will take to reach the final voltage. However, unlike a switch capacitor integrator stage, the output does not need to settle with any degree of accuracy. The buffer differential output must only exceed the amplitude which is needed to drive the mixer with sufficient amplitude to maintain the required mixer conversion gain. Therefore, one side of the buffer output does not necessary need to reach V_{sw} before the buffer input switches in the opposite direction. Obviously, the fastest settling conditions will be required at the highest frequency. For this work it was assumed that the output could swing, worst case to within 15% of the final value, or within 15% of V_{sw} before swinging in the opposite direction. Using the 15% assumption, the maximum value of R_{peak} is shown in the appendix J to be roughly,

$$R_{peak} = \frac{-1}{2f \cdot \ln(0.15) \cdot C} \quad \text{(Eq 7.42)}$$

7.3.2.2 Implementation of variable phase shifter

The variable phase shifter which was described in the previous section is implemented with the circuit shown in figure 111. The phase tuning buffer shown on the right of figure 110 takes the output of the quadrature generating D-latches and drives the mixer local oscillator input. The replica bias opamp which establishes the correct gate voltage for M4 and M5 is shown on the left. The current and ultimately the output resistance of the buffer is modulated with a six bit current DAC shown in the middle of figure 110.

The variable resistors are realized with two triode region PMOS devices M4 and M5 which load the output of the buffer. The loading capacitance of the buffer provide the C of the variable RC which is used to tune the phase. The nominal value of R is selected to give the necessary bandwidth and ensure negligible contribution to the overall phase noise performance of the local oscillator at the mixer input port. With an estimate of the load resistance and the necessary amplitude of the output signal to sufficiently overdrive the mixers, the nominal tail current can then be found by simply dividing the need amplitude by the load resistance. For the GSM receiver application, the phase noise floor needs to be approximately -160dBc at 20MHz from the carrier. Keeping in mind that the channel selection is performed with this local oscillator, the highest frequency the output buffer needs to drive is 410MHz. The buffer load capacitance was estimated to be approximately 300fF. It was also found that the V_{gs}-V_t of the PMOS devices could be as high as 1.3volts. With this information the maximum load resistance was found by taking the lower of the two results obtained from equation 7.41 and equation 7.42. Equation 7.41 gives a peak load resistance of 2.2 kΩ while equation 7.42 gives an upper bound of 2.14 kΩ. Therefore, a value of 2.14 kΩ was used for the nominal PMOS output resistance. From the mixer design, it was found that the differential local oscillator input should be a minimum of 0.8 volts, therefore, V_{sw} should be at least 0.4 volts. With both the maximum resistance and the peak swing, the

nominal bias current is found to be approximately 0.2 mA which implies that each buffer output tail current should be 0.4mamps.

The replica bias opamp shown in figure 110 is used to bias the gate voltage of the PMOS load devices of the phase tuning buffer as well as the load devices of the D-latch shown in figure 106. Although the design of each buffer is identical, all of the buffers and each of the D-latches have their own independent replica bias opamp and corresponding circuitry. This is necessary particularly for the buffers as the resistance is modulated with the tail current of one buffer relative to the other. Therefore, each buffer requires an independent opamp to set the proper PMOS gate voltage. The design of the opamp used by the replica bias circuit was taken directly from [7.11] and is shown in figure 108. The V_{ds} of M6 is compared to V_{sw} with the differential to single ended converter consisting of M11, M12, M14 and M15, while M10 is used for level shifting and M7 is inserted to reduce the output load capacitance which the opamp would otherwise drive if the output were tied directly to the gates of the triode region PMOS devices. A Miller compensation capacitor is added between the gate of M10 and drain of M6. A high aspect ratio is used for M7 to reduce the V_{dsat} of this device. Increasing the size of M7, allows for a larger modulation range of current from the current DAC. Both M3 and M8 are made rather large to reduce the 1/f noise contribution which will be upconverted to the output by the switching action of the input devices M1 and M2.

The input devices to the buffer are sized to ensure that they are sufficiently overdriven. Going with the assumption that the input pair will be completely unbalanced (one device in cutoff while all of the tail current goes pass through the other device of the differential pair) when the differential input is greater than $\sqrt{2}(V_{gs} - V_t)$.

As alluded to before, the load devices M4, M5 and M6 are all sized to give as large a V_{gs}-V_t without driving M8 into triode for any of the current DAC settings.

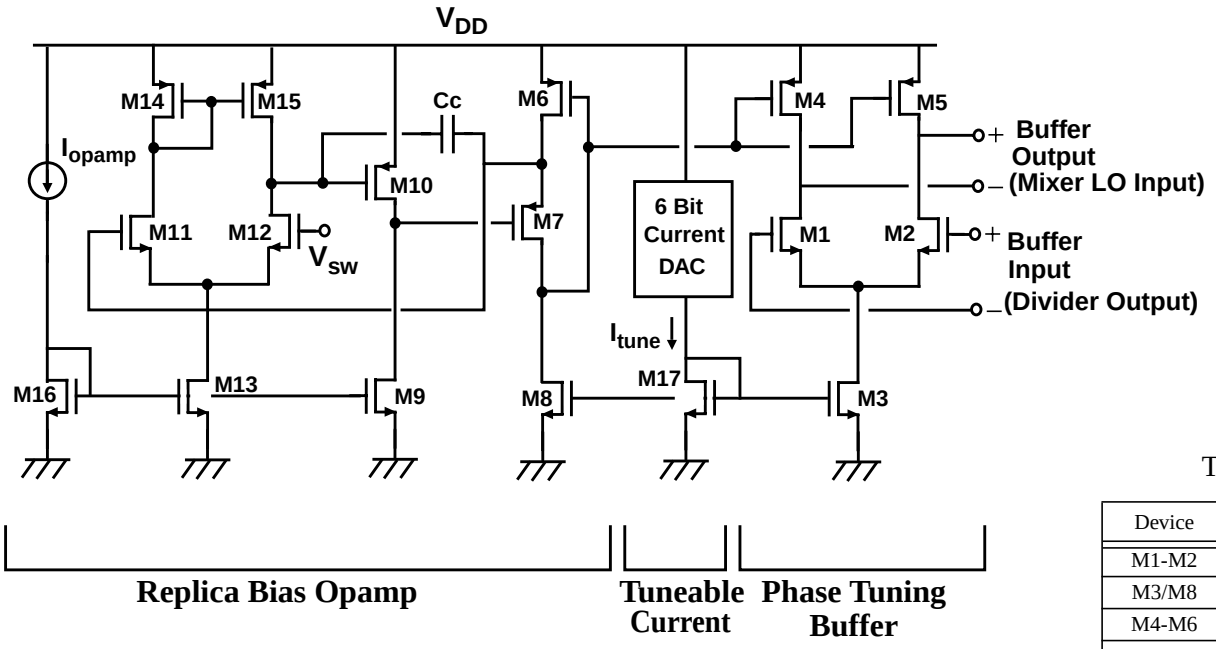


Table 7:

Device	Size(μm/μm)
M1-M2	20/0.35
M3/M8	20/3
M4-M6	15/0.35
M7	240/0.35
M9	64/1.4
M10	48/0.35
M11-M13	48/1.8
M14-M15	48/0.35
M16	64/1.4

Figure 110. Operational amplifier required by the replica biased buffer shown on the right.

A more global view of how the tuneable buffers sit in the image-rejection mixer system is shown in figure 111. Both the I and Q phases of the carrier are extracted from the divide by four block. These outputs are then buffer using the replica biased buffers shown in figure 110. Each buffer has an associated six bit current DAC to modulate the output phase of one buffer relative to the other buffer. Keeping in mind that there are two mixers which run off of the I phase of LO2 and two other mixers that run off of the Q phase of LO2, a parallel set of buffers which are not shown in figure 111 are also used for these mixers. The control bits are feed back into the chip via the transmit DAC input. In the second generation transceiver two 10bit DACs were utilized for the transmit. The bits used to control these buffers were feed in through the transmit

DACs. As there were more than a total of 20 bits to control both the gain and the phase of the mixer a multiplexer was used in this path. The multiplexer settings are set in a manor such that the phase or the gain of the mixer is controlled, both sets of bits can not be accessed at the same time. Additional reduction in the total number of bits which are feedback to the phase tuner section is accomplished by accessing only one of the two current DACs used in figure 111. Essentially an XOR decides whether the top buffer in figure 111 is accessed or the both current DAC for the Q buffer is tuned. The implementation of the current DAC which modulates the buffer output resistance is highlighted in the next section.

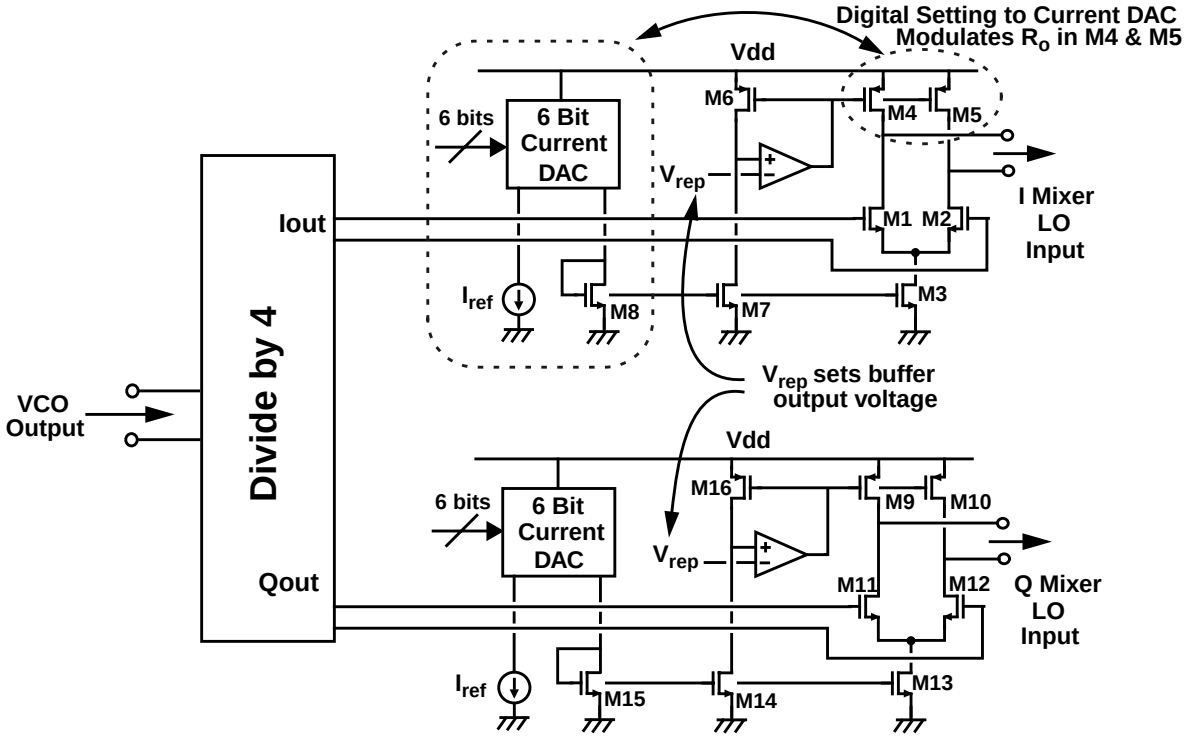


Figure 111. Digital phase shifting tuners for LO2 buffers.

7.3.2.3 Current DAC implementation

The current DAC which is used in the replica biased buffer was realized with a 6 bit binary weighted current DAC as shown in figure 112. The reference current is generated using the integrated current source described in section 7.4.1. The outputs of

the current source labeled as V_g and CASC in figure 114 are applied to the master reference current DAC. The output of the reference current DAC is then put through a 10-to-1 current mirror which then feeds the reference current of the buffers, and ultimately controls the load resistance. The output of the six bit current DAC is then put input the buffer as shown in figure 111.

The needed resolution of the current DAC can then be approximated using equation 7.36 which gives the needed change in output resistance to cause the required change in phase. The value of ΔR can be translated into a value of ΔI by solving the following relationship,

$$\Delta R = \frac{V_{SW}}{I_{Tail}} - \frac{V_{SW}}{I_{Tail} + \Delta I} \qquad \text{(Eq 7.43)}$$

Solving for ΔI and substituting in equation 7.36 for ΔR gives the following relationship between the required resolution in phase and the minimum resolution of the current DAC.

$$\Delta I = \frac{1}{\frac{1}{I_{Tail}} - \frac{\Delta\varphi}{V_{sw} \cdot f \cdot \ln\left(\frac{1}{2}\right) \cdot C \cdot 360}} - I_{Tail} \qquad \text{(Eq 7.44)}$$

In the second generation GSM transceiver, the load capacitance into the mixer was estimated to be 300fF, the highest IF frequency is 410MHz. Using equation 7.44, the required resolution in the current DAC is approximately 0.32mA. A summary of the characteristics of the replica biased buffer along with the need resolution in the current DAC is given in table 7.

Table 7: Tuning Buffer Characteristics

Variable	Value
C	300fF
f	410MHz
$\Delta\varphi$	0.05^{o}
R	2.14kΩ
ΔR	1.62Ω
I_{Tail}	0.4mA
V_{sw}	0.6
ΔI	0.32μA

The master current DAC shown in figure 112 has the MSB scaled to nominally output a current which is 10x of the desired ΔI. The master current DAC is biased off of the standard cell current source described in section 7.4.1. The current out of the master current DAC is then divided down by 10x using the NMOS current mirror. The output of the current mirror is now the reference current for the six bit current DAC. The reference current of the DAC shown in figure 112 is now ΔI and the LSB of the phase tuning DAC. Extremely low aspect ratio long channel devices were used to ensure a large V_{gs}-V_t of the devices that have a source connected to either Vdd or ground. All of these devices were scaled to give a V_{gs}-V_t of 800mV. This helps to improve both their

thermal noise contribution, improve supply immunity and reduce the effect of mismatch between the different legs of the current mirror.

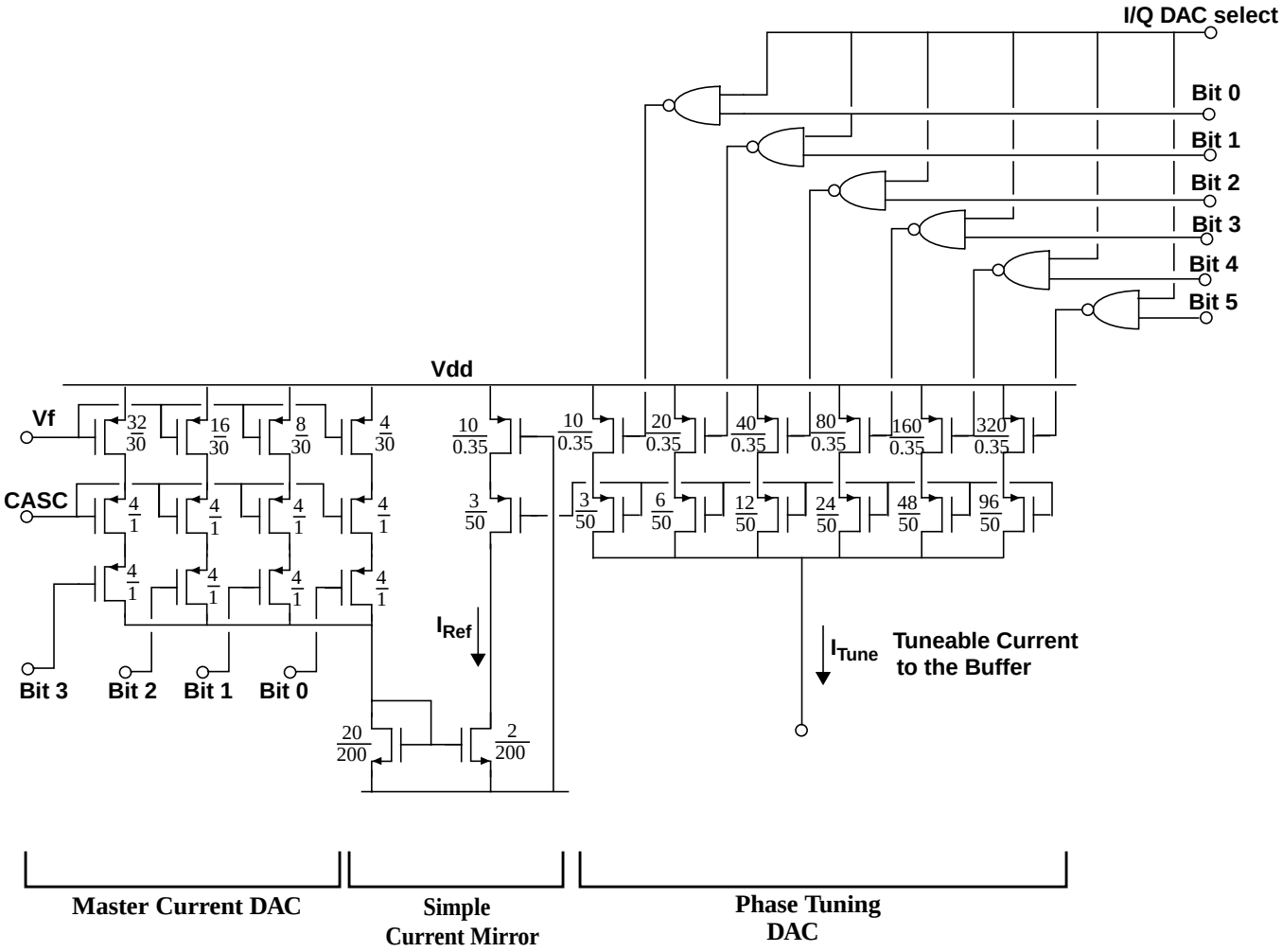


Figure 112. Current DAC utilized by the replica biased buffers. I/Q Control selects which current DAC corresponding to the output buffer is to be used. All dimensions are in micro-meters.

The terminal labeled “I/Q DAC select” in figure 112 decides whether the I current DAC or the Q current is enabled for phase tuning. Bits 0 through 5 come from a multiplexer which is between the transmitter DACs and all of the mixer tuning control.

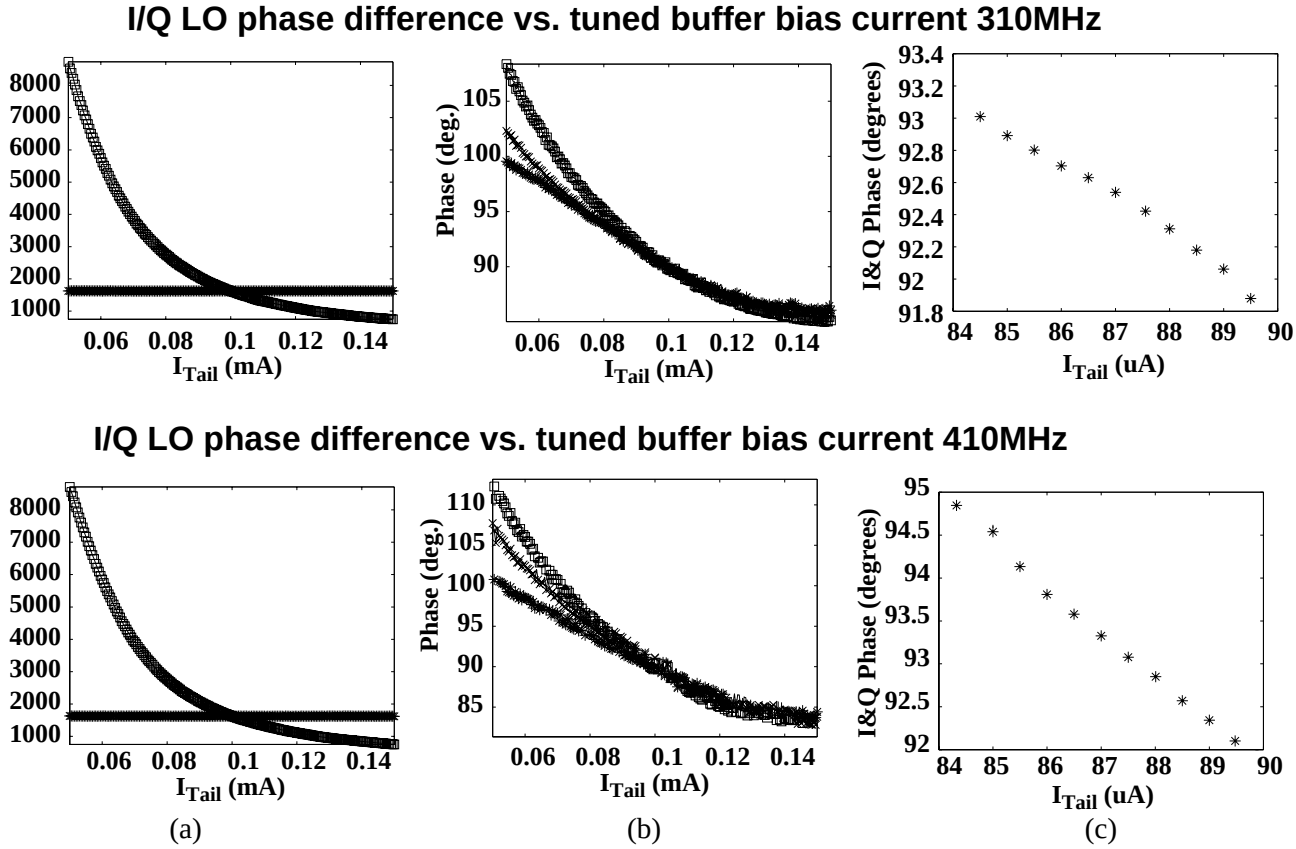
7.3.2.4 Results of phase tuner simulations

A simulation was run on the tuning buffer described in the previous section. A shell script was written to incrementally adjust the DAC settings to give a various

values of tail current in the buffer. Hspice was then run and the phase difference between the I and Q channels were measured over several hundred periods of the local oscillator. In addition, the resistance of the PMOS channel was also recorded from simulation. Using the shell script, the DAC current was automatically increased by one LSB, and the output resistance as well as the I/Q phase measurements were repeated. This process was repeated for the entire range of the DAC.

The simulation results from sweeping the buffer tail current across the entire range of the DAC are shown in figure 113. The load resistance as a function of the tail current is shown in figure 113(a). Through simulation it was found that 1.8kΩ works slightly better than the value estimated in section 7.3.2.3. A lower nominal resistance was used to accommodate any variation in load capacitance. In figure 113(b) and (c), the phase difference between the I and Q output buffers are given as a function of the output current. It is interesting to note that in figure 113(c), the minimum resolution in

phase agrees quite well with the results given by equation 7.44 when 310MHz and 410MHz are used.



(a) (b) (c)

Figure 113. Results of an iterative Spice simulation which measured the phase difference between the I and Q buffer outputs as a function of different DAC settings.

7.4 Standard Bias Cell

Because of the inductive nature of bondwires, there exists a potential to couple undesired signals from external chip components to circuit blocks found on the chip. The modulation of noise and interfering signals through the bias circuitry of RF components is a particular concern. Therefore, to reduce the likelihood that a spurious signal is coupled into the RF circuitry all of the current and voltage bias sources were generated on-chip. For both the DECT and GSM/DECT projects a standard cell current source was utilized as shown in figure 114. This particular circuit which was derived from work described in [7.12][7.13][7.14], was selected because a degree of

programmability which may be obtained by modifying some of the metal routing. Depending on the configuration, a digitally controlled current source may be used, in another configuration a PTAT voltage source may be obtained. Both of these circuits are now briefly described.

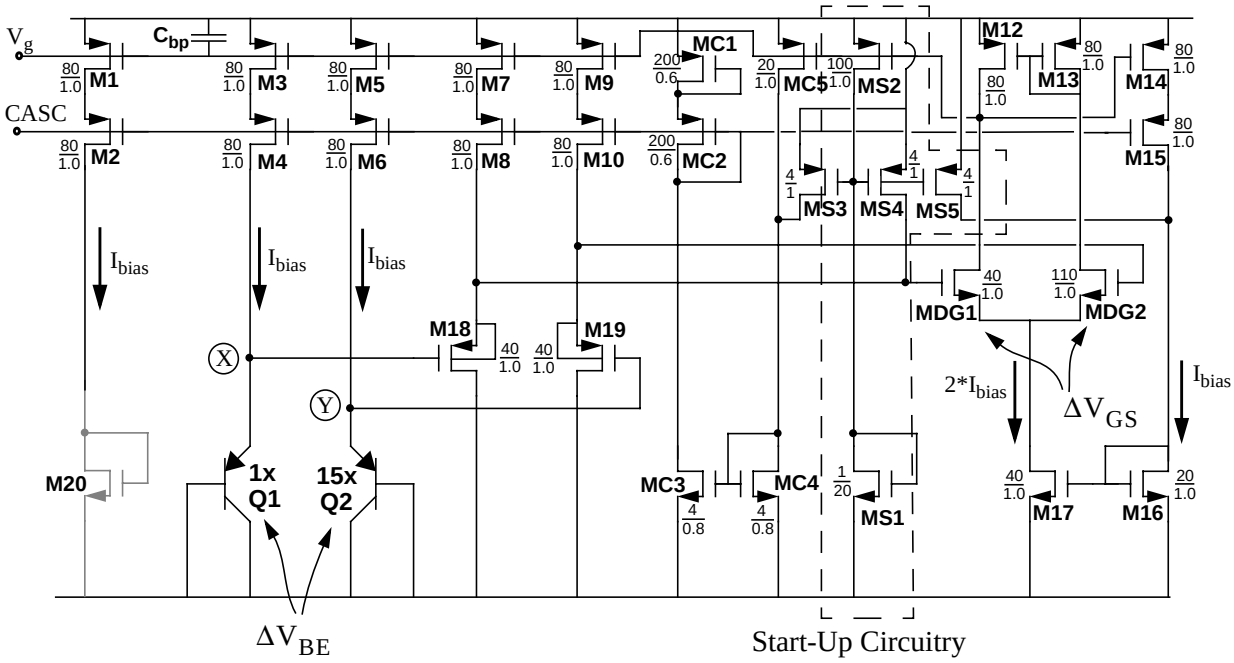


Figure 114. Standard current source used to bias all RF components on both the first and second generation receivers. Device sizes reflect those used for the DECT receiver. All device sizes are given in μm.

7.4.1 ΔV_{GS}-ΔV_{BE} Current Source

The current source version of the circuit shown in figure 114, develops a current through a pair of unequally sized substrate PNPs as well as a set of NMOS devices with different sizes. From the schematic shown in figure 114, if the PMOS cascoded legs consisting of M3-M10 and M14, as well as M15 are all given the same size, and if the aspect ratio of M16 is twice that of M17 then the current through MGD1 and MGD2 will be forced to be the same current as Q1 and Q2. Given that the current is equal in the substrate PNPs of Q1, Q2 and the MOS devices MDG1, MDG2, two operating points exist for the current through these devices. These operating points can

either be zero, this is case when the entire circuit is off. The other operating point can be described by a function which is related to the ΔV_{be} of the bipolar devices as well as the ΔV_{GS} of the MOS devices. Because the PNPs are sized differently and both have the same current, a difference in the emitter voltages of Q1 and Q2 will exist. The emitter voltages are then level shifted with the PMOS devices M18 and M19. The differential voltage is then applied to the gates of MDG1 and MDG2. Again, both of the MOS devices in the differential pair have the same current running through them. In this case the difference in gate voltages is equal to the difference in emitter voltages and we have,

$$\Delta V_{be} = \Delta V_{GS} \qquad \text{(Eq 7.45)}$$

Utilizing standard expressions for ΔV_{be} and square law equations to derive ΔV_{GS}, the current through all of the devices as well as at the output of the current source may be solved in terms of the ratio between the PNPs as well as the aspect ratios of MDG1 and MDG2. The equation describing the output current through the bias circuit is,

$$I_{bias} = \frac{u_n C_{ox}}{2}\left(\frac{W}{L}\right)_{MDG1} \frac{[V_T \ln(n)]^2}{\left(1 - \sqrt{\frac{W_{MDG1}}{W_{MDG2}}}\right)^2} \qquad \text{(Eq 7.46)}$$

7.4.1.1 Current Source Basic Operation

Although the circuit in figure 114 seems somewhat complicated, it can be simplified to the form shown in figure 112. Here again, a difference voltage is created between two unequally sized PNP devices. This difference voltage depends to first order on the size ratio between the two PNP devices. The ΔV_{be} created by the two Bipolar devices can then be thought as being applied to the inputs of an operational amplifier with a variable offset voltage $\Delta V_{GS}(I)$ which depends exclusive on the current which flows through the Bipolar devices. The dependence of the OPAMP input offset voltage ΔV_{GS} is described by the equation shown below in the figure 115. The

OPAMP will modulate the gates of M3 and M5 until an operating point is reached where $\Delta V_{be} = \Delta V_{GS}$. The operational amplifier with the built-in offset voltage ΔV_{GS} is realized with MDG1, MDG2, M12-M17 shown in the circuit of figure 114.

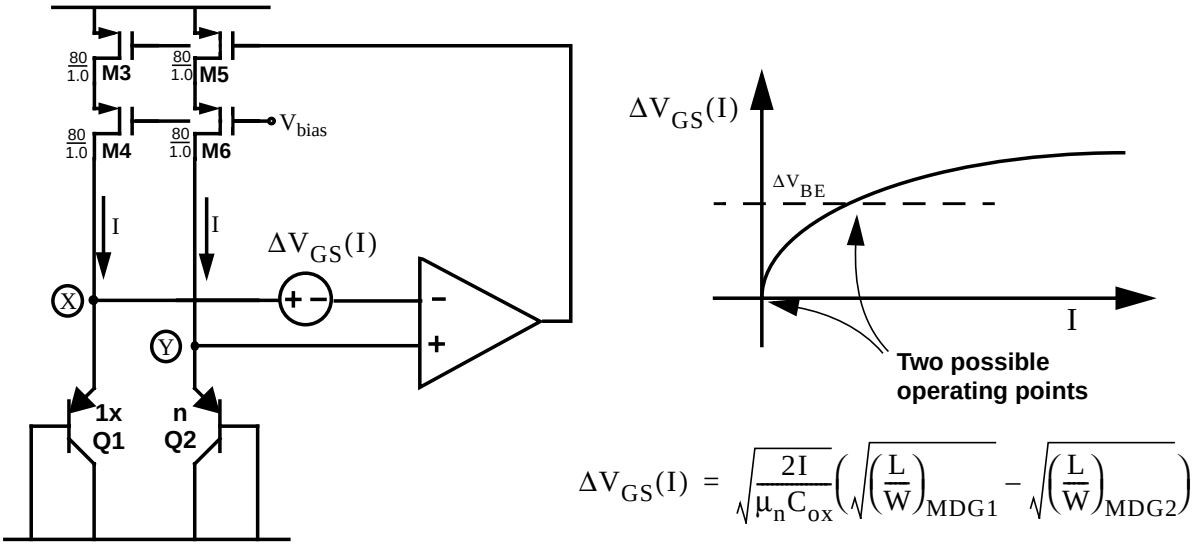


Figure 115. Conceptual diagram of the bias circuit shown in figure 114.

7.4.1.2 Start-Up Circuit

The plot of ΔV_{GS} as a function of the bias current through the PNP devices shown in figure 115, reveals an addition interesting aspect of this class of bias circuits which must be addressed during the design. From this plot, it becomes intuitively obvious that this current source has two stable operating points as described earlier. To ensure that the circuit finds the correct operating point upon power-up, start-up circuitry is required. The start-up circuitry is realized with devices MS1-MS5 shown in figure 114. Upon power-up, if the current through Q1 and Q2 is zero and the entire current source moves to a state where all of the bias circuitry is shut down then zero current will be flowing through device MS6. A diode is connected between the drain of MS6 and ground. The diode is created with a very low aspect ratio device, MS10. If there is zero current through MS6, the diode MS10 will pull the gate voltage of MS7 and MS8 toward ground. The current flowing through MS7 and MS8 will pull the voltage at the input to the feedback OPAMP (gates of MDG1 and MDG2) ensuring that

a sufficient gate voltage exists to turn on MDG1 and MDG2. In addition, current flow through MS9 will ensure that current will flow through M16, thus, ensuring that the OPAMP consisting of M12-M17 as well as MDG1 and MDG2 will eventually start-up. With the OPAMP powered up, the voltage at the gates of M1-M10 will begin to drop causing current flow through the PNP devices, eventually the current will move to the other stable operating point for this bias circuit (indicated as point 2 in figure 113). When the current source approaches a stable operating point, the VGS of MS6 is sufficient large to turn on this device and force current through MS10. Because the aspect ratio of MS10 is so small, the gate-to-source voltage is very large for a small amount of current, this results in turning off MS7-MS9, or in other words shutting down the start-up circuitry for the normal current source operation. The aspect ratio of MS10 is made sufficiently low to result in negligible drain-to-source current under normal operation.

7.4.1.3 Compensation and Supply Rejection

The capacitor C_{bp} serves in a dual role. This capacitor can compensate the feedback loop found in the current source. In addition, if the capacitor C_{bp} is placed between Vdd and the gates of all the PMOS current source devices (M1, M3, M5, M7, M9) an additional benefit will occur with respect to improving the bias circuit's supply rejection. If noise or spurious signals exists on the supply, the capacitor C_{bp} will force the gate-to-source voltage to remain constant, thus, reducing the coupling of noise from the supply to the output current. In addition, the PMOS devices were sized to give a maximum V_{GS}-Vt which again improves both the supply rejection and reduces mismatch between any of the two current legs in this bias circuit. For the DECT prototype receiver the V_{GS}-Vt was designed to be nominally 600mV.

7.4.1.4 Temperature and Process Dependence

Equation 7.46 expresses the output bias current as a function of the aspect ratios of the unequally sized MOSFET devices and the ratio of the substrate PNPs. From this expression, some useful information with respect to the current sources temperature and process dependence may be observed. To understand the relationship between, the output current, temperature and process a few simple relationships are reviewed. First, V_T is directly proportional to the temperature while the mobility of an NMOS device has the following dependence on temperature,

$$u_n \sim T^{-3/2} \qquad \text{(Eq 7.47)}$$

From equation 7.46, one can see that the output current is proportional to (V_T)^2 and V_T is obviously proportional to temperature. Therefore, the output current from the bias circuit of figure 114 has a slight temperature dependence of,

$$I_{bias} \sim T^{1/2} \qquad \text{(Eq 7.48)}$$

Although at first appearance, the temperature dependence of I_{bias} does not seem attractive as a general current source. However, a closer examination of some common circuit components which might utilize this source reveals some interesting dependences on temperature. Mainly, again assuming square law device characteristics, the g_m and the V_{dsat} of a device which utilizes this current source has the following dependencies on temperature.

$$g_m \sim T^{-1/2} \qquad V_{dsat} \sim T \qquad \text{(Eq 7.49)}$$

On there own, the temperature dependence of g_m and V_{dsat} do not seem that interesting. However, when these simple results are applied to a few specific situations some interesting results are forthcoming. Assuming the settling time is proportional to g_m/C [7.16][7.17], then it becomes clear that the settling time of an integrator stage which utilizes this current source as the main bias circuit will only have a slight

temperature dependence. An interesting utilization of the results given in equation 7.49 are found when the DVGS - DVBE current source is used to bias source coupled logic circuits like the ones described in section 7.3. For the case of a simple source-coupled buffer as shown in figure 108, the voltage gain can be expressed as,

$$A_v = g_m R_o \qquad \text{(Eq 7.50)}$$

Expressing g_m with respect to current, and the V_{dsat} of device as well as expressing R_o in terms of the voltage set across the replica bias PMOS devices. The voltage gain can be expressed as,

$$\bar{A_v} = \frac{2I}{V_{dsat}} \cdot \frac{V_o}{I} \sim \frac{V_o}{V_{dsat}}\bar{\ } \qquad \text{(Eq 7.51)}$$

Where V_o is the output swing produced by the replica biased opamps. From the relation given in equation 7.49, V_{dsat} was shown to be proportional to temperature. If V_o could also be made proportional to temperature and the current which biases the input devices comes from the current source in figure 114, then the voltage gain of these source-coupled cells are to first order, independent of temperature. A similar result for the voltage gain temperature dependence of a source coupled cell bias with the current source which utilized replica biasing for the load devices is also given in [7.15].

The question now arises as how to make V_o proportional to absolute temperature (PTAT). This was done by utilizing the core cell shown in figure 114 with a few changes to the metal routing layers. The PTAT voltage source is described in section 7.4.2.

The current source shown in figure 114 does show a temperature dependence and for the device sizes illustrated in the figure the following output currents were simulated across the four process corners, these simulation results are given in table 8.

The estimated current was verify in the lab. Most current sources for the DECT prototype had a measured output current very close to 50uA.

Table 8:

Process Corner	Output Current (I_{bias})
Typical-Typical	51.5uA
Fast-Fast	66.2uA
Fast-Slow	51uA
Slow-Fast	52uA
Slow-Slow	41uA

7.4.1.5 Adjustable Current Source

Both the first and second generation prototype receivers had a serial shift register to control all of the on-chip current and voltage biases across the chip. The previous standard cell bias circuit described had an additional option of a binary weighted current DAC which could be easily placed at the output of the current source and controlled by the shift register. This was done to allow flexibility in the lab with respect to experimenting with various bias conditions on selected receiver components. The bias current to various RF blocks could be controlled through the use of a 4 bit DAC connected to the output nodes V_g and CASC in figure 114. The current DAC used is illustrated in figure 116.

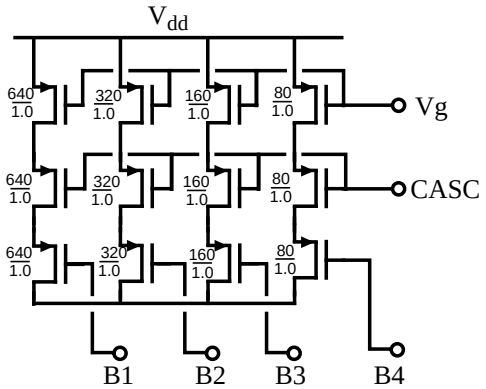


Figure 116. Binary weighted current DAC used to modulate the current source output.

7.4.2 PTAT Voltage Reference

Both the design and the layout of the ΔV_{be}-ΔV_{GS} current source was done in a fashion as to facilitate implementation of other useful circuits which utilized the base cell shown in figure 114. Mainly, a PTAT voltage reference may be realized with a slight modification to the aforementioned current source. The PTAT voltage reference option was implemented by Srenik Mehta, the details of which can be found in [7.15]. The layout of the current source was done in a way to allow the placement of a few additional devices as well as an easy resizing of MDG2.

The basic concept behind converting the current source in figure 114 to a PTAT voltage reference is illustrated in figure 117. The basic steps to converting the current source to a voltage reference is done by making the aspect ratios of MDG1 and MDG2 equal and adding an additional resistor at the emitter of Q2. By sizing both MDG1=MDG2 this has the affect of removing the current bias dependent offset to the input of the amplifier which feeds back a voltage to the gates of M3 and M5. Therefore, if M3 and M5 are equal in size, then the amplifier will force the voltage at the inputs to the opamp to be equal. The current I_{bias} through the PNPs is then easily found to be,

$$I_{bias} = \frac{V_T \ln(n)}{R_1} \qquad \text{(Eq 7.52)}$$

If the output current I_{bias} is taken from this circuit by again adding transistors to V_g and CASC as was done for the current source in figure 114, the current produced can then be applied to a resistor producing a voltage. If it is assumed that the output current is mirrored around and applied to a resistor R2, then the expression for the bias voltage produced is simply,

$$Vo = \frac{R_2 V_T \ln(n)}{R_1} \qquad \text{(Eq 7.53)}$$

Again, VT is proportional to temperature making the output voltage also proportional to absolute temperature.

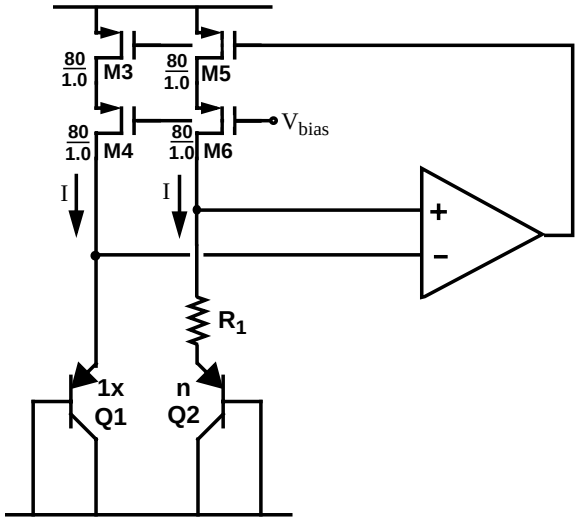


Figure 117. Simplified schematic of the PTAT option used to compliment the standard cell current source.

A more detailed circuit diagram of the implementation of the PTAT voltage source is shown in figure 118. Similar to the current source version of this circuit a binary weighted current DAC can be added to the output at V_g and CASC. This has the virtual affect of increasing the value of R2, thus changing the output voltage while still remaining proportional to absolute temperature. The exact implementation of both the

current DAC which is used to modulate the output voltage, as well as more implementation details of this PTAT reference may be found in [7.15].

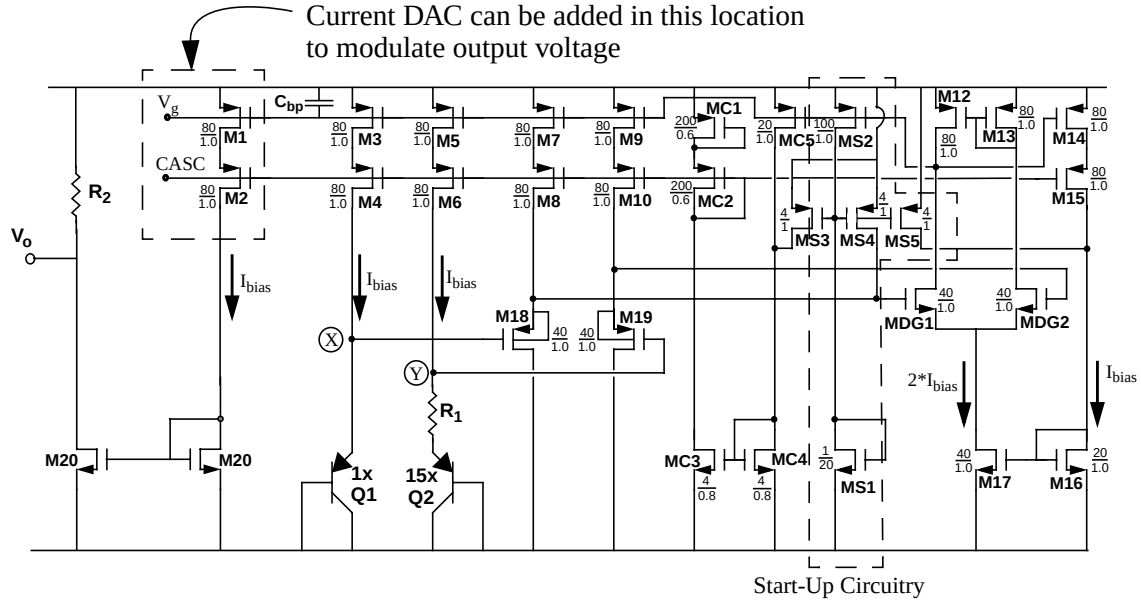


Figure 118. PTAT voltage source used in the DECT project.

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Chapter 8

Results and Conclusions

8.1 Introduction

No thesis would be complete without some description of the measured results and a comparison to the predictions presented in previous chapters. This final chapter will begin with a description, covering the measurement techniques which were used in the lab. This is followed by a discussion of the results obtained in the lab, from the DECT receiver, as well as some results from a stand alone prototype image-rejection mixer. Unfortunately, at the time of this writing, there were no results available on the second generation receiver, which included the adaptive image-rejection mixer. The DCS1800/DECT prototype will probably be published at a later time. The results obtained from the DECT prototype are compared to some of the predictions given for the image-rejection mixer. This chapter will conclude with a few comments which summarize this work in a broader context of other comparable research efforts. And finally, a discussion is given of possible future avenues of research.

8.2 Test Set-Up and Procedure

A description is given in this section, of both the test setup, as well as the procedure used to take the measured data on both the receiver and the individual image-

rejection mixer. The overall test results obtained from measurements on the DECT receiver, were taken in such a way as to compare these numbers to expected results for the image-rejection mixer in terms of noise and linearity.

The source impedance at the receiver input was assumed to be 50Ωs and all of the components on the testboard, at the input were matched a single-ended 50O source impedance. The complete characterization of the receiver was done using the setup shown in figure 119, along with some software on the PC which analyzed the digital bit stream acquired from the ADC output. To test the receiver, an RF signal generator was applied to the testboard and passed through a balun before the signal went on chip into the differential inputs of the low-noise amplifier. The output of the receive channel on the DECT chip, was driven off-chip at the output of the analog-to-digital converters using source-coupled buffers. This digital output was then read using an logic analyzer data acquisition card. The acquired bits from the ADC in the logic analyzer, were then feed to a PC were subsequent signal analysis could be done with matlab, to determine the linearity, noise, and filter response of the comprehensive channel. Two additional signal generators along with baluns were used to generator both the first and second local oscillator (known to this point as LO1 and LO2).

The performance of higher frequency receivers is highly dependent on the quality of the on-chip supply and ground. For 2-GHz receiver applications, any parasitic inductances in series with the supply can become a performance issue. Therefore, the choice of the packaging technology is important and examined in the next section. This is followed with a description of the measurement procedure, as well as a discussion of the test results.

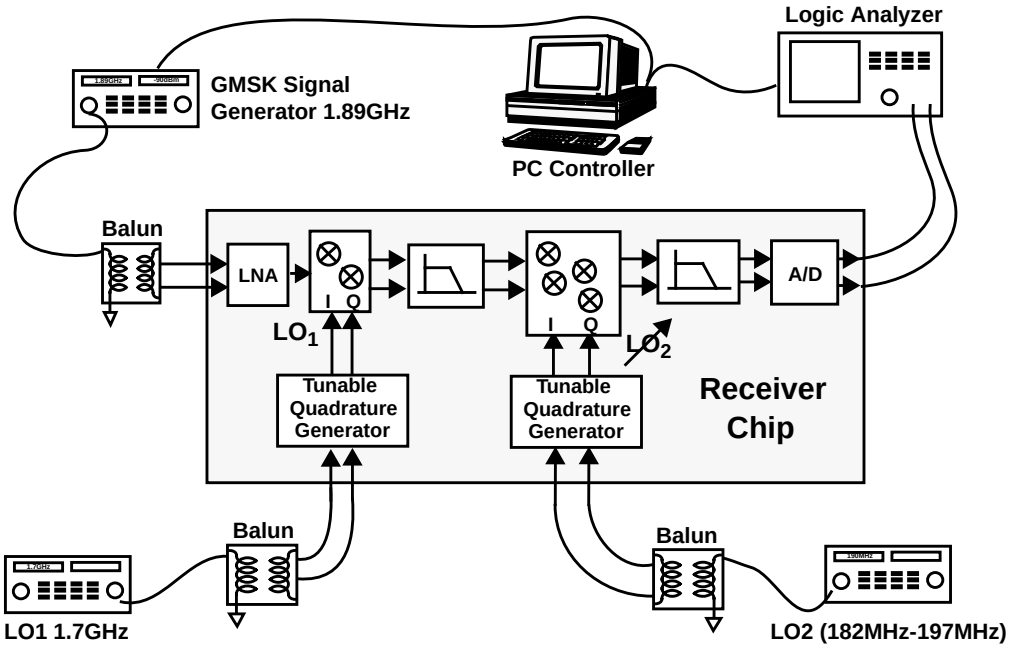

Figure 119. Block diagram of the test set-up which was utilized in the lab.

8.2.1 Packaging Considerations

All of the testchips which were evaluated for this project used Chip-On-Board (COB) packaging techniques. This basic concept is illustrated in figure 120, where the backside of the test die is attached directly to the testboard using a conductive epoxy. In this case, the area were the die is glued to the testboard has been gold plated. If elected to do so, the backside of the die can be gold plated and the substrate will have an excellent ground provide through the chip backside, after the attachment to the testboard takes place. For the experiments described in this thesis, die with and without gold plating were tested with no observable difference in performance between the plated die, verse non-gold plated die. With the backside of the die attached to the testboard, a bondwire is then run from the individual chip pads to the appropriate routing on landing zone (routing) on the testboard.

The primary advantage for packaging with COB is the reduction in parasitic lead inductance as compared to a packaged part. The situation has been illustrated in figure 120 (a) and (b). If a package were used, the total inductance from any chip pad back to the board, would include the inductance associated with the bondwire from the chip pad to the package bondwire landing zone, in series with the inductance from the package landing zone along the package lead, to the point where lead connects with the routing on the testboard. If COB is utilized in place of a package, at a minimum, the inductance associated with the package lead is removed, the bondwire inductance would still be present. However, with a proper layout of the testboard, particularly in the area of the chip landing zone, the space from the chip pads to the board landing zones can be minimized, thus reducing the length of this bondwire. In addition, the ground chip pads can be brought down directly along the side of the chip, and bonded to the chip landing zone, further minimizing the ground bondwire length and the associated inductance. Bonding of the chip ground to the die attach area, using COB is illustrated in figure 120 (c).

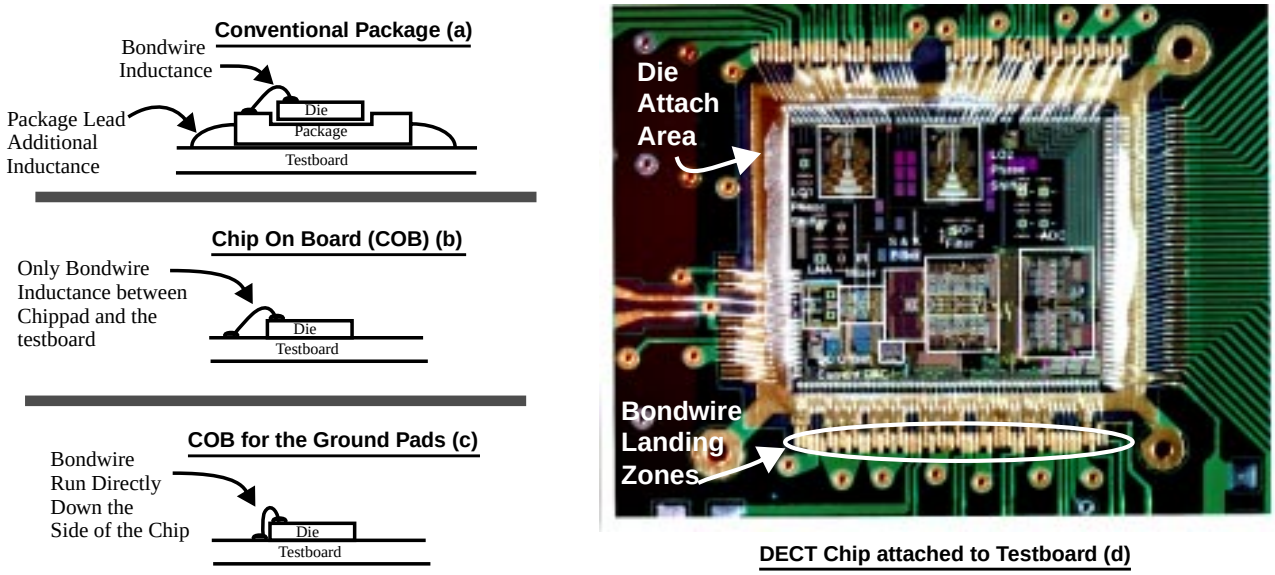

Figure 120. Chip-On-Board (COB) packaging. (a) sideview illustrating a conventional package, (b) sideview of COB packaging (c) Die photo of DECT receiver on attached to the testboard using COB.

Although there may be some advantages of reducing both supply series inductance and effects of mutual coupling of spurious signals from bondwire to bondwire, there are some practical (or maybe impractical) issues associated with COB. For experimental testboards, COB has the disadvantage that to test an individual die, an entire testboard needs to be exclusively built-up for one part. If the die on one testboard is non-functional, then an entirely new board must be built to test a second device. Testboards can be potentially recycled by reattaching new chips and rebonding. This process of recycling a board with new devices can be repeated up to three times, and can only be accomplished if the board layout is done in such a way as to allow proper movement of the bonder, in the die attach area. In other words, many of the high-profile through-hole components, must be sufficiently spaced, far enough away from the die attach area, to allow an unconstrained movement of the bonder, while a new device is being bonded. For a production part, COB might prove to be an attractive alternative to package parts as the cost of the package has been eliminated. However, the cost saving would depend on the potential penalty associated with discarding an entire board upon final test as opposed to simply eliminating a part after package testing.

Other board/chip assemble techniques which could be used to reduce the supply lead inductance, might include die attachment using flip-chip techniques. While the die is still in wafer form, solder bumps are added to each of the chip pads. After sawing the wafer, the individual die are heated to reflow the solder on the chip pads. The device is then lowered topside down (thus the name “flip-chip”), and positioned on to the board, in such a way that the solder bumps connect the chip pads to landing zones found on the board. The length of the solder bump is extremely small compared to a bondwire, giving again, the advantage of a lead parasitic which is significantly lower than even COB, and certainly better than a packaged part. However, the disadvantages relate to the fact when using flip-chip, the topside of the die (substrate) faces upward making it difficult to provide a good ground to the backside of the die. In addition, the production cost advantages of flip-chip are not immediately clear, as the reflow process

of the solder bumps can be somewhat complex requiring glass dams on the board substrate.

8.2.2 Third Order Non-Linearity (IP3)

One very common characterization of either an entire receiver or the individual components in the receive chain is the relative measure of linearity. For radio receiver applications, the overall third order intermodulation performance is critical. This measurement is done to test a receiver's immunity to a very unique situation when two very undesired signals are received, with a specific combination of frequencies, such that the relationship between the undesired interferers, and the desired received signal lead to interference with in the desired signal band. If f_{des} represents the frequency of the desired carrier while f1 and f2 are the frequencies of the undesired alternate channel interferers. Then if the relationship in frequency between the interferers and the desired signal is the following.

$$f_{des} = 2 \cdot f_1 - f_2 \text{ or } f_{des} = 2 \cdot f_2 - f_1$$

The situation may arise where the two undesired alternate channel interferers pass through a third order non-linearity and create interference in the desired signal band. The most commonly quoted figure of merit which characterize the third order distortion performance is the third order intermodulation intercept point, or IP3. This can be either referred to the input or the output of the Device Under Test (DUT). A more through treatment of IP3 is given in chapter 2.

The measurement of the IP3 number (usually quoted in dBm or dB) for the DECT receiver was done by applying two tones to the input, at frequencies such that the third order intermodulation component generated (at $2*f_2-f_1$), fell within the bandwidth of the baseband filter. The frequencies at which the two applied tones were assigned are outlined in the DECT standard [8.1]. In short, the tones were applied in various

combinations of channel spacings as shown in figure 121(a). The magnitude of the undesired tones which were applied to the receiver input, were then recorded along with the magnitude of the third order intermodulated component at the output of the ADC. To measure the magnitude of the third order component at the output of the receiver, an FFT was run on the PC shown in figure 121(b). The computed value for the third order intermodulation component was then divided by the receiver gain and recorded. The magnitude of the applied tones was then increased, and the above procedure was repeated to obtain the linear and third order response of the receiver. The results of which are shown in figure 121 (c). With this data, the linear response of the receiver was extrapolated as well as the third order response. The intersection point of the linear and third order lines is the input-referred-third-order-intermodulation-intercept point. For this receiver, the IP3 was recorded to be -7dBm.

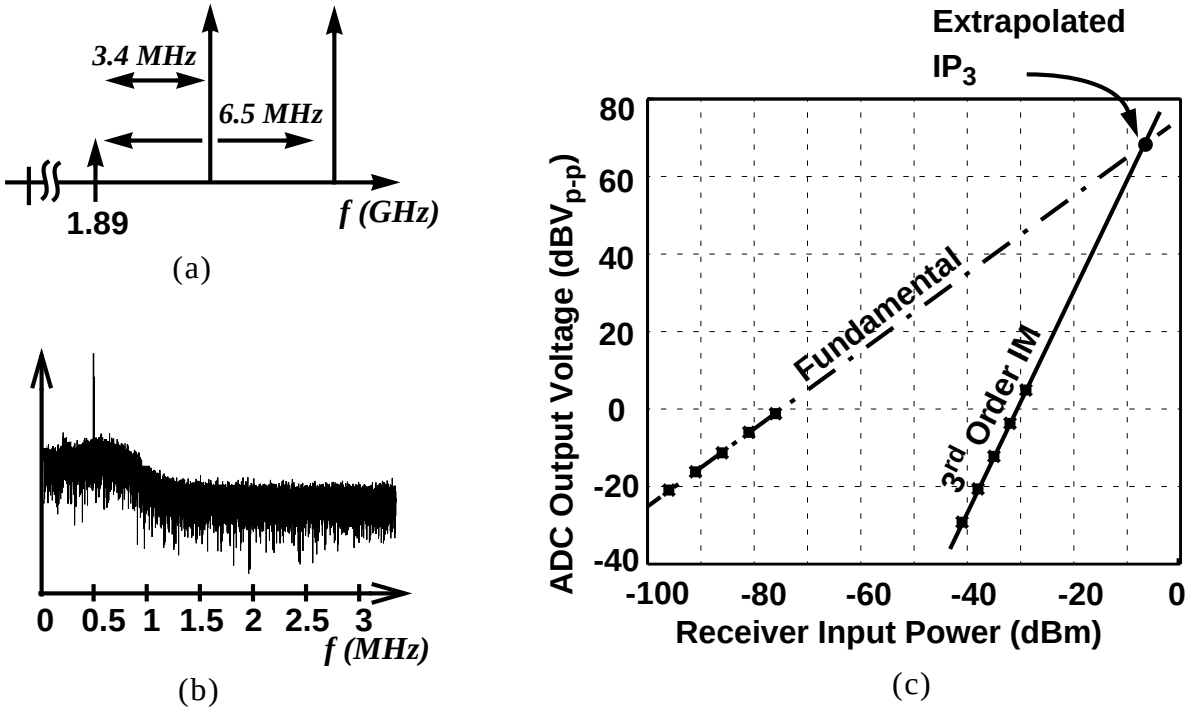

Figure 121. Two tone 3rd order intermodulation test. (a) FFT of the receiver output with a single tone input. (b) Tones applied 2 & 4 DECT channels away from the carrier. (c) 3rd Order IM plot showing intercept point.

It was determined that the linearity bottleneck for the DECT receiver, was the transconductance pair associated with the mixer running off of the first local oscillator. This was confirmed with a measurement, on a die which just included the LNA and the transconductance stage of the first mixer. Again, the IP3 was measured to be -7dBm on the LNA stand-alone chip [8.2]. An IP3 at the input of the receiver, can be converted to a peak voltage assuming a 50Ω load. The -7dBm measurement converts to 141mV at the receiver/LNA input. The LNA gain was measure to be approximately 20dB across the DECT band. Using the LNA voltage gain, the measured IP3 reflected to the mixer input is 1.41volts. Using equation 6.63 in chapter 6 the estimated IP3 is 1.31V, which was estimated with a 400mV, V_{gs}-V_t of the common source devices used by the mixer. This compares quite well to measured results. The measured IP3 is slightly higher than what is predicted by equation 6.63, this is to be expected as the hand estimate assumes square-law devices. However, even with a V_{gs}-V_t of 400mV there will still be some velocity saturation which tends to linearize the input transconductance stage.

8.2.3 Noise Performance

Obtaining noise data for an individual analog component along a receive chain, such as a standalone LNA, mixer or filter is somewhat straightforward. This is typically done using a noise figure meter which injects a noise source into the component under test. The meter then looks for the amount of noise which has been added to the output to determine the noise contribution from the device under test. Noise figure meters are made to evaluate the noise performance of purely analog components; analog input and output. The problem of measuring a receiver's noise figure becomes more complicated when an analog-to-digital converter interface has been added to the signal path, making it difficult if not virtually impossible to utilize a noise figure meter. In this work, a method was used which facilitates the noise figure measurement of a receiver without the use of a noise figure meter [8.3]. The is done by measuring the Carrier-to-Noise or Carrier-to-Interference (C/I) at both the input and the output of the device under test, in

this case the receiver. With both the C/I_{Input} and C/I_{Output}, the noise figure of the receiver can be computed directly from the definition of noise figure or,

$$NF = 10\log\left(\frac{SNR_{Input}}{SNR_{Output}}\right) = 10\log\left(\frac{C/I_{Input}}{C/I_{Output}}\right) \quad \text{(Eq 8.1)}$$

The noise figure measurement is performed by first ensuring that a good match to 50Ω has been made at the receiver input. For the DECT receiver, the S11 looking into the SMA connection was better than -14dB. A signal source was attached to the receiver input as shown in figure 119. The signal source assumes a 50Ω load and the *available power* delivered by the signal source is typically what is shown on the display of the signal generator output. To ensure that the signal source readout is calibrated properly, it is probably a good idea to check the delivered power with a spectrum analyzer, which also reads the available power of an input signal assuming a 50Ω match. Once the receiver input impedance has been matched to the source resistance (50Ω), a tone is then applied to the receiver input and the C/I ratio at the input, can be computed by using the available signal power which is read from the signal source generator display, and then taking the ratio to the available noise power delivered by a source resistance, which is simply kTB. For the DECT measurements, the signal bandwidth was assumed to be 700kHz which is the same bandwidth of the baseband filter. The C/I ratio at the receiver can be expressed as,

$$C/I_{Input}(dB) = 10\log\left(\frac{S_{tone}}{kTB}\right) \quad \text{(Eq 8.2)}$$

Where S_{tone} is the available power delivered to the receiver input (this can be taken directly from the signal generator)[1] and B is the channel bandwidth of the system, in this case 700kHz was used. The output carrier-to-noise ratio is simply found by taking an FFT of the ADC output. The bins in the FFT which correspond to the signal source applied to the receiver are found and the sum of the signal power in these bins are then used to evaluate the signal power. Next, all of the remaining bins between DC

1. If the units on the signal generator are registered in dBm, then the available signal power in Watts must be computed to use equation 8.2, or the numerator in the right-hand side of equation 8.2 must be multiplied by 1mW (inside the log expression) to obtain the correct dimensions.

and 700kHz were summed, to find the output inband noise power. The C/I ratio at the output of the receiver was then computed using these two quantities derived from the FFT.

It is worth mentioning, that the output C/I ratio estimated using an FFT is not the true C/I ratio at the output of the receiver. A fudge fact of 3dB must be subtracted from the receiver output C/I ratio, to account for the frequency conversion of the desired channel to baseband, as is the case in a direct conversion receiver or the Wideband IF receiver. To understand why 3dB has been subtracted, the following section attempts to bridge the gap between the output C/I ratio of a receiver which is measured using the above mentioned method, and what the true C/I ratio would be if a real channel signal were received.

8.2.3.1 Conversion of SSB measurement to DSB Receiver Noise Figure.

Most signals which are modulated up to the carrier frequency are double-side banded about the frequency of the carrier. Therefore, there is useful information in both the lower and the upper sidebands above and below the carrier frequency. This situation is illustrated at the top figure 122, where the desired channel (post upconversion) is shown as $F_C(f)$, and is symmetric about the carrier frequency, f_C. The objective is to then down converter the desired channel from the carrier frequency, to either a low intermediate frequency or zero IF as is the case for direct conversion or the wideband IF receiver.

As mentioned in the previous section, the noise figure of the DECT prototype was measured by finding the carrier-to-noise ratio in lab at both the input and output of the receiver. This is done by injecting a tone at a slight offset from the carrier frequency such that when down converted to the baseband, the tone is discernible and falls within the baseband filter’s bandwidth. For the purposes of the DECT receiver measurements, a tone was applied to the receiver at a 150kHz from the carrier. In other words, the

difference between the frequency of the tone applied to the frontend of the receiver, and the sum of both the local oscillators used by the receiver is 150kHz, again this difference is shown in figure 122 as Δf (Δf = f_{Tone} - f_C).

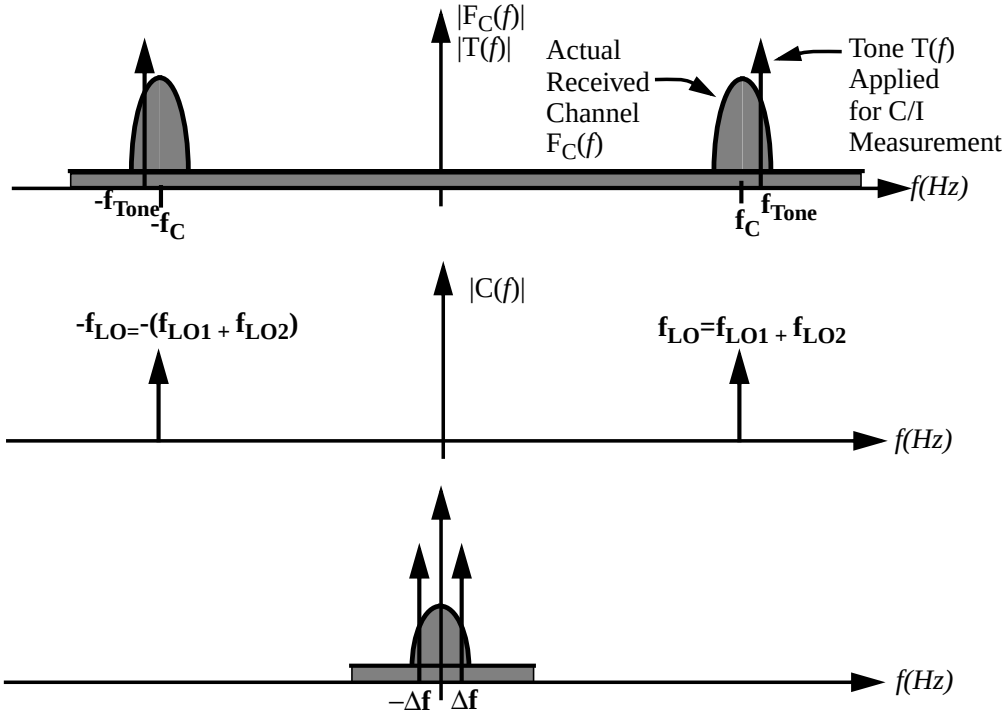

Figure 122. Illustration of the relationship between frequency translation of a real double-side banded signal and a single tone used for receiver noise figure measurement.

There is a very subtle difference between the carrier noise ratio measured at the output when a single tone is applied, and the actual carrier-to-noise ratio which would exists if a real radio channel were received. The key to understanding this difference starts by first looking at the fundamental loss in signal power when a received channel is converted to baseband. First a few definitions will be given, where it is assumed that there is a baseband channel in the transmitter which will be defined as F(f). Next, this spectrum is upconverted to the carrier frequency by multiplying with an ideal sinusoidal function. After the channel is upconverted, the spectrum can be written as F_C(f) and is shown graphically, centered about the carrier in the top part of figure 122. F_C(f) will now represent the signal which is actually received at the antenna of the receiver.

$$F_C(f) = \frac{1}{2}F(f - f_C) + \frac{1}{2}F(f + f_c) \quad \text{(Eq 8.3)}$$

The objective is to now downconvert $F_C(f)$ to either an intermediate frequency, or centered around DC. Using the DECT prototype receiver as an example, the incoming spectrum is multiplied by two cascaded local oscillators, the sum of which is shown in the frequency domain as just F_{LO}, middle of figure 122. To simplify things, the sum of the carriers will be represented by C(f) in the frequency domain. The total frequency translation of the incoming spectrum $F_C(f)$, can be modeled as the convolution in frequency between $F_C(f)$ and C(f), the result of which will be represented as $F_B(f)$.

$$F_B(f) = F_C(f) * C(f) \quad \text{(Eq 8.4)}$$

C(f) is again nothing more than the spectrum of the sum of the local oscillators in the frequency domain.

$$C(f) = \frac{1}{2}\delta(f - f_C) + \frac{1}{2}\delta(f - f_C) \quad \text{(Eq 8.5)}$$

Equation 8.4 can now be written as,

$$F_B(f) = \left[\frac{1}{2}F(f - f_C) + \frac{1}{2}F(f + f_C)\right] * \left[\frac{1}{2}\delta(f - f_C) + \frac{1}{2}\delta(f - f_C)\right] \quad \text{(Eq 8.6)}$$

The original desired channel represented as F(f) is now frequency translated, resulting in the following shift of the desired spectrum as,

$$F_B(f) = \frac{1}{4}F(f) + \frac{1}{4}F(f) + \frac{1}{4}F(f - 2f_C) + \frac{1}{4}F(f + 2f_C) \quad \text{(Eq 8.7)}$$

Because the frequency translation is a direct modulation from the carrier to DC, there is a component of $F_B(f)$ which arises from the positive frequency and also the negative frequency, these are shown as the first two terms in Equation 8.7. The baseband component of $F_B(f)$ has two spectrums which are adding together. This arises again from the fact that the frequency translation converts the desired channel to center around DC, in addition to the property of the desired channel being symmetric about the carrier. The desired channel at baseband can now be expressed as,

$$F_B(f) = \frac{1}{2}F(f) + \frac{1}{4}F(f - 2f_C) + \frac{1}{4}F(f + 2f_C) \quad \text{(Eq 8.8)}$$

The above situation of converting a radio channel to baseband is contrasted with the case where a single tone is applied to the receiver to find the input and output carrier-to-noise (C/I) ratio to estimate the receiver noise figure. As mentioned before, the tone which is applied to the receiver input needs to be offset from the carrier (or the sum of the two local oscillators), such that when the tone is frequency translated to baseband, it is easy to extract the energy of this tone using an FFT. The single tone applied to the input can be represented as $T_C(f)$, again, this situation is reflected at the top of figure 122. However, unlike the desired channel, the tone only resides on one sideband about the carrier frequency. The single tone which is applied to the receiver input ($T_C(f)$) can be written as,

$$T_C(f) = \frac{1}{2}\delta(f - (f_C + \Delta f)) + \frac{1}{2}\delta(f + (f_C + \Delta f)) \quad \text{(Eq 8.9)}$$

When the tone $T_C(f)$ is frequency translated to baseband, this can be represented with a convolution in the frequency domain. The tone which then resides will be written as $T_B(f)$, which can expressed as the convolution of a the tone around the carrier frequency, and the sum of the local oscillator frequencies or C(f).

$$T_B(f) = T_C(f) * C(f) \quad \text{(Eq 8.10)}$$

The result of this convolution at baseband is then.

$$T_B = \frac{1}{4}\delta(f-\Delta f) + \frac{1}{4}\delta(f + \Delta f) + \frac{1}{4}\delta(f + (2f_C + \Delta f)) + \frac{1}{4}\delta(f - (2f_C + \Delta f)) \quad \text{(Eq 8.11)}$$

The baseband filter will remove the higher frequency components leaving,

$$T_B = \frac{1}{4}\delta(f-\Delta f) + \frac{1}{4}\delta(f + \Delta f) \quad \text{(Eq 8.12)}$$

Note that the amplitude of the desired tone at baseband is reduced by a half when compared to the tone which is injected at the receiver input. The power of the tone which is observed at baseband, has been reduced by 3dB. This is fundamentally different from the real situation where a desired channel which occupies both sidebands about the carrier frequency. Here, energy from the down converted signal at baseband, is frequency translated from both positive and negative frequencies. So there exists a

3dB difference between the tone used for measurement of the C/I ratio at baseband, and the real situation where a desired channel is downconverted in the receiver. Thus, the reason for the 3dB fudge factor which is subtracted from NF measurement obtained using the input and output C/I ratios. Clearly again, the 3dB subtraction would only take place for radio system that frequency translate to baseband.

8.2.3.2 Noise Figure Measurement Result: Discussion

Using the procedure outlined in the previous section, the overall receiver noise figure was measured. The double-sideband noise figure from the LNA input, to the ADC output was recorded to be 14dB which corresponds to a -90 dBm sensitivity when used on a DECT channel.

The considerably high noise figure for the DECT receiver was attributed to two problematic areas. First, and certainly foremost was an error in the parasitic capacitance extraction from the layout. The value of capacitance, which was estimated and used, was as much as 30% lower than what was obtained in the lab. This had an adverse affect on the amplitude of the first local oscillator used by the RF mixers. The additional capacitance and loading of the output buffers shown in figure 103, of chapter 7, had the affect of significantly lowering the amplitude of the LO. This had a most negative affect on the conversion gain of the first set of mixers. With a lower conversion gain in the LO1 mixers, a much larger than expected noise contribution from the second set of mixers and the baseband circuits was seen and increased the receiver noise figure.

In additional, the higher than expected noise contribution from the mixers and the overall receiver was also attributed to poor device models. At the time the design was completed, little investigation had taken place into the behavior of CMOS devices at RF frequencies. In particular, it has since been found that the “gamma” factor used for the input referred channel noise associated with a single MOS device can vary as a function of frequency [8.2][8.4][8.5][8.6][8.7][8.8]. Traditional, CMOS devices have

used a value of 2/3 for γ, at low frequency. However, recently it has been suggested that γ may vary as high as 2.5 for some CMOS technologies, at high frequency. Under estimating the value of gamma for the device noise model would certainly contribute to a poor noise figure.

The noise figure of the receiver could have been also improved through a better trade off between the noise performance for an individual block, verses the power consumption. Shown in figure 123 (a) and (b), is a breakdown of the measured RMS noise power of each block referred to the receiver output, and the distribution of the receiver power consumption, respectively. One can note, that although the first mixers noise contribution to the overall receiver is almost 40%, these mixers contribute less than 10% of the overall receiver power budget. Therefore, the noise and power consumption could have been better traded off to obtain a lower receiver noise figure.

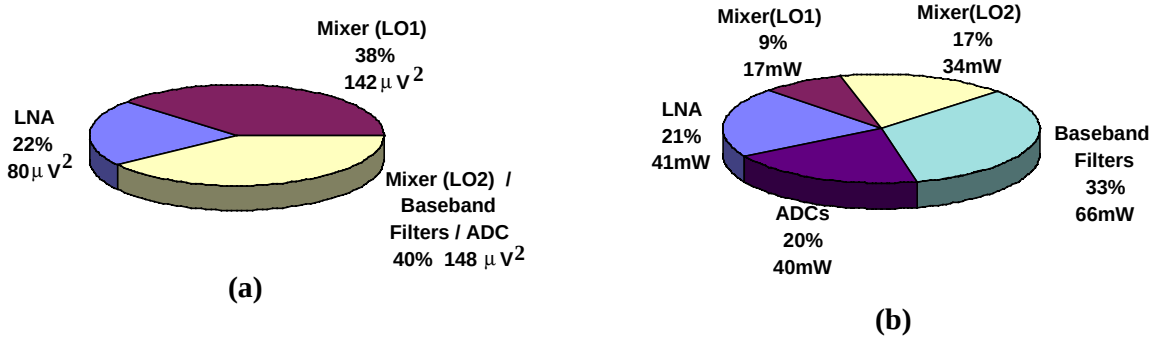

Figure 123. (a) Breakdown of the output rms noise voltage (b) breakdown of the receiver's power consumption.

8.2.4 Image-Suppression

A key component which contributes to the selectivity performance of a receiver, particularly in a heterodyne system, is the ability to reject signals found within the image-band. To test the DECT receiver's ability to reject signals found within the image-band, a series of tones were applied to the receiver sweeping the entire DECT band from 1.884GHz to 1.896GHz. The magnitude of the tones, which were feed into

the receiver, in the DECT bands, was then measure using an FFT at the ADC output. An additional set of tones were feed into the receiver, at the image frequency corresponding to each of the desired frequency tones. The ratio of the receiver's measured response at the output of the ADC, between the tone in the image band, and the corresponding tone in each of the desired bands, was recorded. The results of which are shown in figure 124.

This measurement might be better understood by looking at how one data point in figure 124 was taken and assigning some real numbers to the measurement. For the purposes of all the DECT measurements, the first local oscillator (RF LO or LO1) was set at 1.7 GHz, leaving the IF to range from approximately 190MHz to 200MHz for all the DECT channels. Given the frequency of the first local oscillator, the image band lies at approximately 200MHz below the first LO, or at 1.5 GHz to about 1.516 GHz. The first measurement point in figure 124, at 1.8838GHz was obtained by applying a single tone at this frequency, to the input of the receiver, which was set at full gain. The magnitude of the output signal was then measured. A second tone was feed into the receiver at the image frequency, of the first tone, which is at [1.7GHz - (1.8838GHz - 1.7GHz)], the magnitude of the receiver's response at baseband value was then recorded. The ratio of the receiver's response to the desired signal tone applied at 1.8838GHz was taken relative to the magnitude of the measured tone which was applied at the exact image frequency of the desired tone or [1.7 GHz -(1.8838 GHz -1.7 GHz)].

[1.7GHz -(1.8838GHz - 1.7GHz)]. The one data point under discussion has been plotted

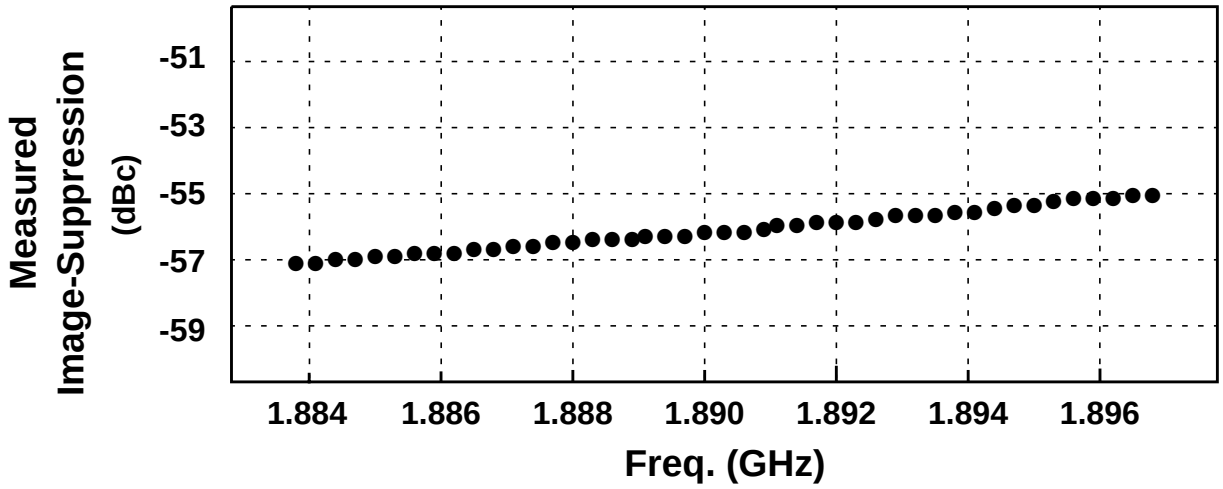

Figure 124. Image-Suppression measured for the DECT receiver. Here, the Image-Rejection is defined as $10\log(|IM|^2/|DES|^2)$.

as the left most point in figure 124.

It should be noted that the image-rejection data was taken while the phase between the I and Q LO mixer inputs were tuned for maximum image suppression. Both the circuit and process for tuning the phase on the DECT receiver were described in chapter 7, section 7.2.10.

8.2.5 Blocking performance

To test the receiver's immunity to signals found in both adjacent and alternate channels, a blocking test was performed. The conditions of this test were done in accordance with the specification outline in the ETSI document covering the physical layer of DECT [8.1]. Although there are some specific blocking conditions associated with DECT, most blocking test associated with various standards, share some commonality in the method used to evaluate the receiver's selectivity performance with respect to blocking. Specifically, blocking test are usually performed by applying a desired signal to the receiver which is 3dB above the required reference sensitivity.

Simultaneously, either a single AM or a modulated blocker is applied to the receiver, in one of the alternate channels associated with the system. The blocker is increased in power level (or amplitude) until the bit error of the desired signal increases to some unacceptable value. For the purposes of the DECT receiver testing, a desired signal of -73dBm was applied to the receiver input in accordance with [8.1]. A single sine wave was then applied to one of the adjacent DECT channels, and increased in magnitude until the C/I ratio of the desired signal, at the output of the receiver, dropped to less than 10dB. This approximately corresponds to a BER of 10-3 for a signal which is modulated using gaussian minimum shift keying (GMSK). This assumes the noise is white across the channel [8.9][8.10][8.11] which may not necessary be true. The power of the blocker in each of the adjacent channels, which resulted in the C/I ratio dropping below 10dB, was recorded and is shown in figure 125, as a star. The required DECT blocking performance has been shown in the shaded areas. As can be seen, the blocking performance of the receiver is well above what is required by DECT.

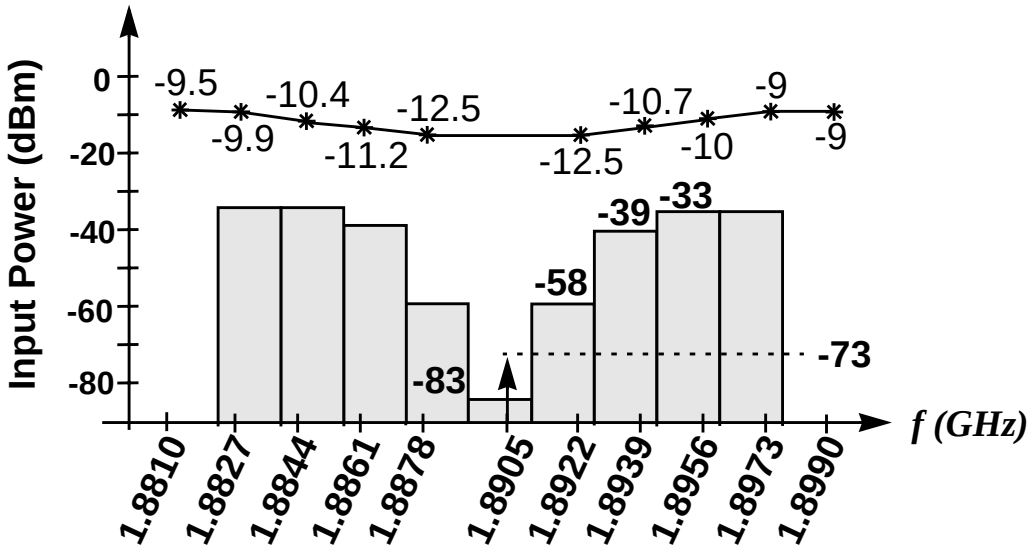

Figure 125. Blocking performance of the DECT receiver.

8.2.6 Receiver filter response

To test the comprehensive response of the entire receive channel a series of tones were recursively applied to the receiver. As shown in figure 119, a PC, the receiver input signal generator, and the logic analyzer were all networked together using HPIB connectors. A “C” program was then written [8.12] which automatically sets both the frequency and amplitude of the input signal source to some desired offset from the sum of the oscillators. With the input signal applied to the receiver, the “C” program grabs a set of data from the ADC output using the logic analyzer. Knowing the frequency of LO1 and LO2, along with the frequency of the input tone applied, the program then computes the FFT of the output signal. The bin associated with the output tone, after frequency conversion to baseband, is stored in a file. The program then slightly increments the frequency of the receiver input signal and again acquires data using the logic analyzer. Subsequently, the magnitude of the new tone at baseband is found, again using an FFT. The tone is again incremented slightly in frequency, and the process of acquiring the magnitude of the tones at baseband is done recursively, sweeping the entire range of the baseband filter output.

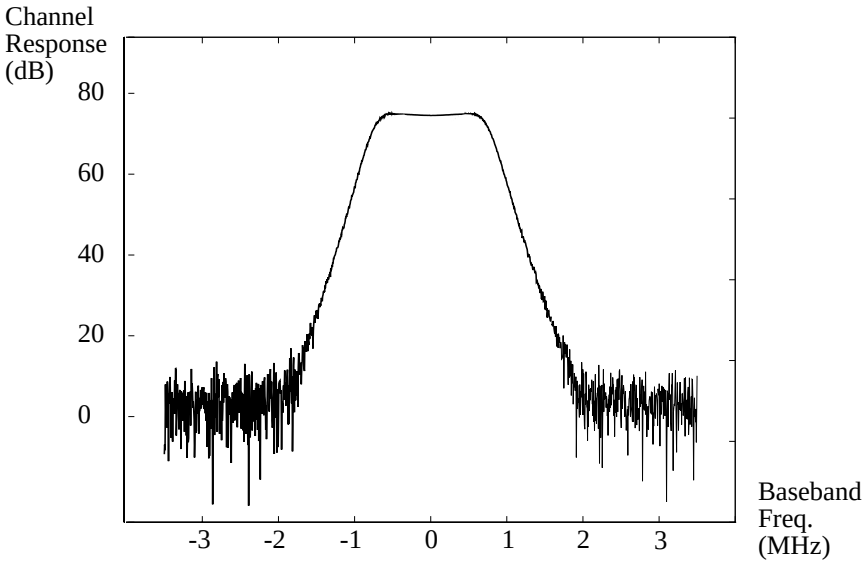

Figure 126. Frequency response of the entire receiver from the LNA to ADC output. Positive and negative frequencies are shown

Figure 126 shows the results of sweeping a series of tones from 4MHz below the carrier, to 4MHz above the input carrier frequency, notice the baseband filter bandwidth is approximately 700kHz and the receiver gain is approximately 78dB. For the DECT receiver, a 8th-order channel-select switched-capacitor filter was used which had an equiripple response.

8.2.7 Summary

As was mentioned earlier, this thesis contains data from the DECT receiver while the dual mode DECT/GSM receiver will be published at a later date. This section is provided to give a summary of the data which was obtained on the DECT receiver as well as give a relative comparison to other comparable work in the area of high integration receivers.

Table 9: Summary of results obtained from the DECT receiver

	Receiver Measurement	DECT Requirement
Sensitivity	-90dBm	-83dBm
Input IP3 (Max. gain setting)	-7dBm	-26dBm
P_{-1dB} (Min gain setting)	-24dBm	-33dBm
Receiver Image Rejection	~85dB w/ RF Filter	~70dB w/ 200MHz IF
P_{ob3dB} (Max. gain setting)	-33dBm @ 2MHz	N/A
Max. Receiver Gain	78dB	N/A
Min. Receiver Gain	26dB	N/A
Die Size	7.5mm x 6.5mm	N/A
Active Chip Area	$15mm^2$	N/A
Power Supply	3.3v	N/A
Silicon Technology	0.6μm DPTM CMOS	N/A

Many of the key measured results obtained from the DECT receiver measurements are shown in table 9. Where it is relevant, the DECT receiver measurements are compared to the physical layer specifications which are outlined in the DECT standard [8.1]. As can be seen from table 9, the DECT receiver meets each of

the significant requirements of the DECT standard. The overall receiver sensitivity is -90 dBm with a receive channel gain of 78 dB. The prototype DECT receiver was fabricated in a 0.6μm double-poly triple-metal CMOS process, at the Taiwan Silicon Manufacturing Company (TSMC). The overall receiver die size is 7.5mm by 6.5 mm and the active die area is 15 mm^2.

A relative comparison to other high integration techniques, in silicon, which have been used to perform image rejection are shown in figure 127. Various methods were used to address the image-rejection function as an integrated solution. The include, image-rejection mixers, integrated image filtering and a combination of the two methods, all of which are plotted as a function of the measured image rejection, in figure 127. The two highest reported numbers for image rejection [8.13][8.14] were obtained by manually tuning the I and Q phase error in the lab. Although, this is somewhat impractical, there does lie the hope of adaptively, auto-calibrating out the phase error and achieving a high image-rejection ratio.

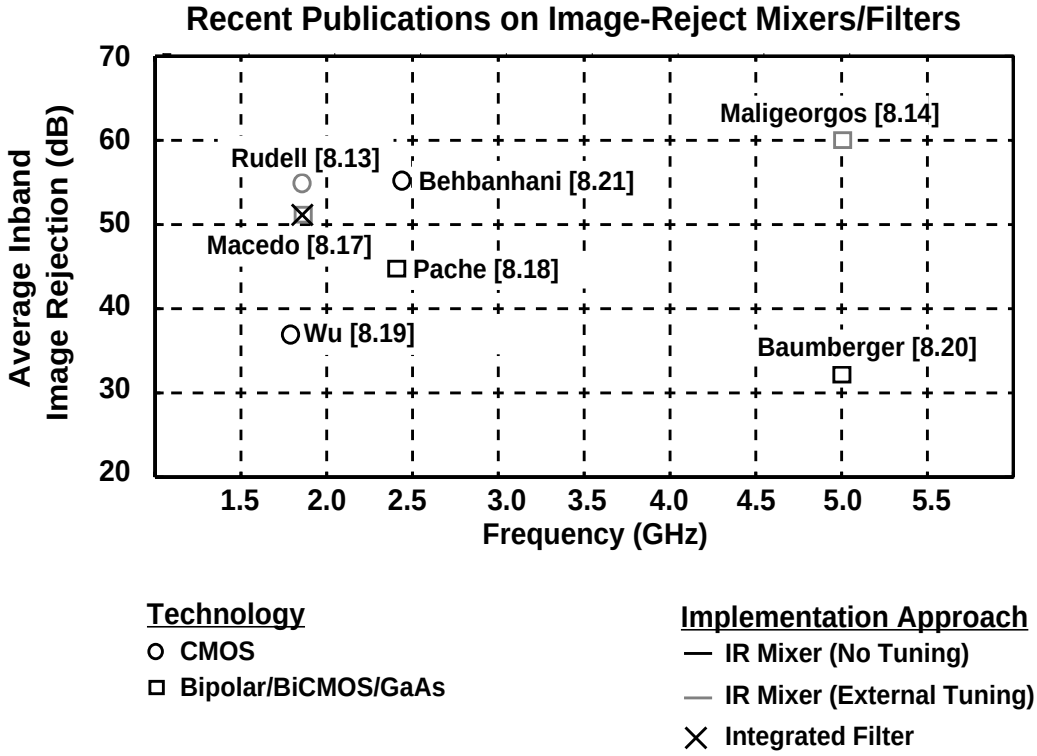

Figure 127. Relative comparison between various recently published attempts to implement an integrated image-rejection function.

In comparison to other recently reported high integration receivers, the work presented in [8.13], was one of the first complete RF radio receivers implemented in CMOS. At the time this work was presented, the prototype had the highest level of radio integration in CMOS, everything from the LNA to the ADC was all implemented on a single chip without the need for external RF and image-rejection filters. In table 10 are some other recently demonstrated high integration receivers. The various publications presented in table 10, are samples of some of the radio architectures which have been implemented as a high integration systems, and represent various silicon technologies including, CMOS, Bipolar and BiCMOS which were used to address different applications/standards.

Author	Architecture	Application	Technology	Noise Figure	IIP3	Blocking Performance	Total Power
A. Abidi et al. (ISSCC '97 [8.22])	Homodyne	ISM Band.	1.0µm CMOS	8.5dB	-8.3 dB	----------	177mW
M. Steyaert et al. (ISSCC '98 [8.23])	Low-IF	DCS 1800 upbanded	0.35µm CMOS	4.9dB	-3dBm	----------	190mW
D. Schaeffer et al. (ISSCC '98 [8.15])	Low-IF / Weaver	GPS	0.5µm CMOS	4.1dB	-16dBm	----------	115mW
S. Wu et al. (ISSCC '98 [8.19])	Weaver	GSM / DCS1800	0.6µm CMOS	4.7dB/ 4.9dB	-7dBm/ -8dBm	----------	72mW/ 75mW
M. Banu et al. (CICC '97 [8.24])	Double Low-IF	GSM	0.5µm BiCMOS	4.8 dB (SSB)	-4.5dBm	GSM	66mW
J. Rudell et al. (ISSCC '97 [8.13])	Wideband IF	DECT	0.6µm CMOS	14dB (DSB)	-7dBm	DECT	198mW
T. Cho et al. (ISSCC '99 [8.16])	Homodyne	Cordless Telephone	0.6mm CMOS	4.5dB (DSB)	-21dBm	900MHz SS	525mW
F. Banahani (ISSCC '00 [8.21])	Hetrodyne Weaver/PPF	ISM Band	0.6µm CMOS	9.8dB	-10dBm	ISM	180mW 300mW
D. Yee et al. (EESSC '00 [8.25])	Homodyne	2-GHz WLAN	0.25µm CMOS	8.5dB (DSB)	-18.3dBm	----------	106mW

Table 10: Summary of recently published high integration receivers.

The GPS receiver given in [8.15] did an excellent job of trading off the noise figure and power consumption. The cordless telephone receiver presented in [8.16] was one of the first all-CMOS integrated receivers put into production and is currently sold as a component in a Siemens telephone.

One conclusion that can be drawn from recently published work given in table 10 is that, to date, it does seem plausible and in fact, practical as well as inexpensive to implement an entire radio receiver in CMOS for moderate performance applications. These would be radios for short range standards, where the mobile does not wander to far from the basestation. In the situation where both the transmitter and receiver are relatively close together, the selectivity performance required of the receiver is somewhat relaxed. Example applications would include receivers built for cordless telephone, wireless computer peripheral components (keyboard, mouse, printer, etc.) and wireless LAN to name a few. Future research and development is needed to address many of the technical challenges still associated with full integration in CMOS, or any semiconductor technology for that matter, of an entire radio receiver intended for a high performance standard.

8.3 Contributions and Possible Future Directions

There are three distinguishable contributions in this work which come from the levels of architecture, analysis and circuit implementation. From the perspective of a radio architectures targeting high levels of receiver integration, the wide-band IF receiver was introduced and explored during the period of this work. From more of an analysis perspective, a convenient method for evaluating current commutating active mixers was also explored. Although the analysis emphasized CMOS Gilbert Cell like mixers, the design techniques are general enough to be used on any active mixer independent of the implementation technology. From more of a circuit implementation perspective, a new variable gain mixer cell was introduced. The mixer, modulates both

the load resistance and the gain of the mixer through a common mode feedback circuit. Other new circuit implementations which were introduced included a novel utilization of a polyphase filter and buffer combination. This circuit utilizes an all-pass buffer, followed by a third order polyphase filter. The buffer filter combination produces very accurate quadrature signals (less than a 0.5^{o} phase error) while maintaining the LO carrier power and reducing the overall power consumption associated with this function as compared to other polyphase filter implementations.

An additional contribution in this work, which is somewhat less proven, is the introduction of a self-calibrating image-rejection mixer. The proposed self-calibrating image-rejection mixer is really the first step in the implementation, of receiver systems which take advantage of the system aspects which are now possible and facilitated through the very act of integrating all of the radio components onto a single piece of silicon. Therefore, the implication is that not only can future radios be implemented with self-calibrating mixers, but can also overcome many traditional radio non-idealities and limitations through adaptation, or auto-calibrate as well as optimize real time performance.

Any form of research usually ends by answering a few questions while opening the door to many more new riddles. Future challenges and research associated with high integration radio systems in CMOS, lie on the device, circuit, and system level. The next wave of research will need to further explore the behavior of sub-micron CMOS devices in the 1 to 6 GHz range. The rapid implementation of all CMOS receivers will be critically linked to accurate device models for simulation, particularly a reasonable estimate of the noise performance.

The continued scaling of modern CMOS processes requires the lowering of the available supply voltage. This presents some interesting and unique challenges for the implementation of future CMOS RF circuits. Further exploration will be required to realize mixers, oscillators and power amplifiers for sub-1.5 volt CMOS processes.

From more of a system radio architecture level, a yet unexplored area where a reduction in the receiver power consumption may lie in the exploitation of high integration CMOS transceivers[8.26]. By rethinking the transceiver as a “system-on-a-chip,” radio architectures may be developed to optimize power consumption for needed performance. Most radio standards or applications outline a set of test conditions which specify the required performance of both the transmitter and receiver. A closer examination of the standards reveals that typically, high performance in terms of linearity, noise figure and dynamic range are only required during brief intervals. However, contemporary receivers and transmitters found in products are typically over-designed to meet the most difficult performance requirements even when not required. This results in higher power consumption than is really necessary. Receiving a weak desired signal in the presence of a strong alternate channel signal is an excellent example of a condition which leads to very high dynamic range requirements in the backend of integrated radio receivers; this is illustrated in figure 128. Higher required

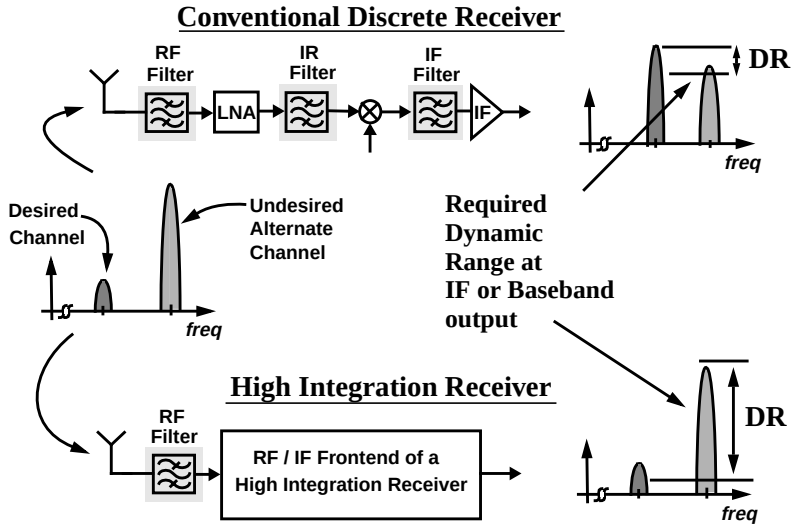

Figure 128. Effect of blockers on dynamic range in both discrete and integrated receivers.

dynamic range in both the baseband filters and/or ADC typically implies a higher receiver power consumption. The condition of an adjacent channel blocker may only occur during very brief intervals of the receiver’s operation time. However, currently

integrated radios are designed to handle high dynamic range conditions of an alternate channel blockers at all times, as shown in figure 128. A more optimal approach to handling the high dynamic range required of integrated baseband components may rest in developing transceiver systems which sense when a strong alternate channel condition exists. This would allow the receiver to fall back to a low-power, low-performance mode when high performance was not required. Then, when a strong alternate channel signal arises, the receiver would increase the dynamic range in the back-end to meet the particular condition present. Again, by monitoring the presence of the blocker, the receiver could then return to a low performance, optimal power consumption mode of operation when the blocker disappears. A parallel strategy may be applied to optimize the frequency synthesizer power consumption verses the required phase noise performance which again would be determined by the blocking condition which is sensed by an intelligent receiver system. This concept could potentially be extended to optimize the receiver power consumption versus noise figure and required sensitivity for a given received signal strength.

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Appendix

Appendix A: Image Suppression as a function of phase and gain mismatch

The following is an outline of an analysis to determine the effects of phase mismatch between the I & Q local oscillator of both LO1 and LO2 and the effects of gain mismatch between the signal paths. The matching error is modeled as shown in figure 129. The phase mismatch between both the I and Q LO mixer inputs of both the first and second local oscillators are defined as $\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$ respectively. This phase error will be defined as the deviation from ideal quadrature. For example, 91^{o} phase difference between the I and Q LO1 would be represented by $\phi_{\varepsilon 1}=1^{o}$. ΔA represents the composite gain mismatch between two of the four image-rejection channels.

The analysis is carried out by applying two complex signals denoted D(t) and IM(t) both equally spaced in the frequency domain, from the first local oscillator as shown in figure 129. Both the image and desired signal will be tracked as they move

through the mixer to the baseband II and QQ channels where they are summed. A

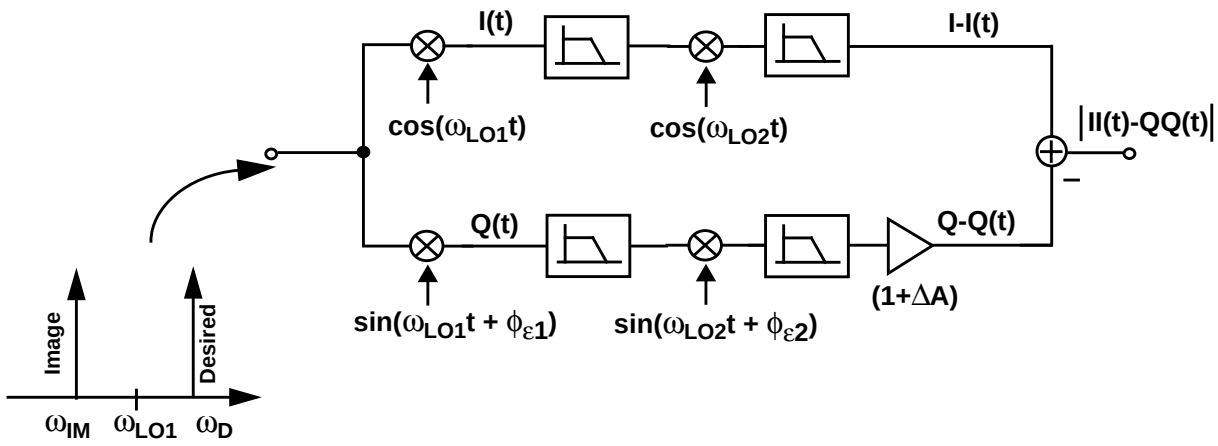

Figure 129. Model used to analyze the image-rejection performance as a function of LO phase and gain path matching.

solution for the image-rejection ratio is found with the magnitude of the desired and image signals after summation of the II and QQ channels.

$$D(t) = \cos(\omega_D t) + j\sin(\omega_D t) \quad \text{(Eq A.1)}$$

$$IM(t) = \cos(\omega_{IM} t) + j\sin(\omega_{IM} t) \quad \text{(Eq A.2)}$$

Assuming an idealized sinusoidal LO, the two input signals D(t) and IM(t) are multiplied by the I and Q local oscillators, the resulting signals at IF can be expressed as,

$$I_D(t) = \frac{1}{2}[\cos((\omega_D - \omega_{LO1})t) + \cos((\omega_D + \omega_{LO1})t)] + \frac{j}{2}[\sin((\omega_D + \omega_{LO1})t) + \sin((\omega_D - \omega_{LO1})t)] \quad \text{(Eq A.3)}$$

$$I_{IM}(t) = \frac{1}{2}[\cos((\omega_{IM} - \omega_{LO1})t) + \cos((\omega_{IM} + \omega_{LO1})t)] + \frac{j}{2}[\sin((\omega_{IM} + \omega_{LO1})t) + \sin((\omega_{IM} - \omega_{LO1})t)] \quad \text{(Eq A.4)}$$

$$Q_D(t) = \frac{1}{2}[\sin(((\omega_D + \omega_{LO1})t) + \phi_{\varepsilon 1}) - \sin((\omega_D - \omega_{LO1})t - \phi_{\varepsilon 1})] + \frac{j}{2}[\cos((\omega_D - \omega_{LO1})t - \phi_{\varepsilon 1}) - \cos(((\omega_D + \omega_{LO1})t) + \phi_{\varepsilon 1})] \quad \text{(Eq A.5)}$$

$$Q_{IM}(t) = \frac{1}{2}[\sin((\omega_{IM} + \omega_{LO1})t + \phi_{\varepsilon 1}) - \sin((\omega_{IM} - \omega_{LO1})t - \phi_{\varepsilon 1})] + \frac{j}{2}[\cos((\omega_{IM} - \omega_{LO1})t - \phi_{\varepsilon 1}) - \cos((\omega_{IM} + \omega_{LO1})t + \phi_{\varepsilon 1})] \quad \text{(Eq A.6)}$$

Assuming the upconverted terms are removed through low-pass filtering and substituting in $\omega_{IF} = \omega_D - \omega_{LO1} = \omega_{LO1} - \omega_{IM}$ results in,

$$I_D(t) = \frac{1}{2}\cos(\omega_{IF}t) + \frac{j}{2}\sin(\omega_{IF}t) \quad \text{(Eq A.7)}$$

$$I_{IM}(t) = \frac{1}{2}\cos(\omega_{IF}t) - \frac{j}{2}\sin(\omega_{IF}t) \quad \text{(Eq A.8)}$$

$$Q_D(t) = -\frac{1}{2}\sin(\omega_{IF}t - \phi_{\varepsilon 1}) + \frac{j}{2}\cos(\omega_{IF}t - \phi_{\varepsilon 1}) \quad \text{(Eq A.9)}$$

$$Q_{IM}(t) = \frac{1}{2}\sin(\omega_{IF}t + \phi_{\varepsilon 1}) + \frac{j}{2}\cos(\omega_{IF}t + \phi_{\varepsilon 1}) \quad \text{(Eq A.10)}$$

Multiplying equation A.7-10 by the second set of quadrature LOs and again removing the upconverted terms, the following expression may be obtained for the image and desired signal present in the II and QQ baseband channels.

$$II_D(t) = \frac{1}{4}[\cos((\omega_{IF} - \omega_{LO2})t) + j\sin((\omega_{IF} - \omega_{LO2})t)] \quad \text{(Eq A.11)}$$

$$II_{IM}(t) = \frac{1}{4}[\cos((\omega_{IF} - \omega_{LO2})t) - j\sin((\omega_{IF} - \omega_{LO2})t)] \quad \text{(Eq A.12)}$$

$$QQ_{Ds}(t) = \frac{1}{4}(1 + \Delta A)[-\cos((\omega_{IF} - \omega_{LO2})t - (\phi_{\varepsilon 1} + \phi_{\varepsilon 2})) \quad \text{(Eq A.13)}$$
$$-j\sin((\omega_{IF} - \omega_{LO2})t - (\phi_{\varepsilon 1} + \phi_{\varepsilon 2}))]$$

$$QQ_{IM}(t) = \frac{1}{4}(1 + \Delta A)[\cos((\omega_{IF} - \omega_{LO2})t + (\phi_{\varepsilon 1} - \phi_{\varepsilon 2})) \quad \text{(Eq A.14)}$$
$$-j\sin((\omega_{IF} - \omega_{LO2})t + (\phi_{\varepsilon 1} - \phi_{\varepsilon 2}))]$$

From equation A.11-14 the magnitude of the desired and image baseband signals may easily be found. Making the simplifying assumption that $\omega_{IF} - \omega_{LO2} \cong 0$ we get at baseband,

$$\left|II_D(t) - QQ_D(t)\right|^2 = \frac{1}{16}[(1 + (1 + \Delta A)\cos(\phi_{\varepsilon 1} + \phi_{\varepsilon 2}))^2 + ((1 + \Delta A)\sin(\phi_{\varepsilon 1} + \phi_{\varepsilon 2}))^2] \quad \text{(Eq A.15)}$$

$$\left|II_{IM}(t)-QQ_{IM}(t)\right|^2 = \frac{1}{16}[(1-(1+\Delta A)\cos(\phi_{\varepsilon 1}-\phi_{\varepsilon 2}))^2 + ((1+\Delta A)\sin(\phi_{\varepsilon 1}-\phi_{\varepsilon 2}))^2] \quad \text{(Eq A.16)}$$

By taking the ratio of equation A.15 and 16 the image-rejection ratio in (dB) is given by,

$$IRR(dB) = 10 \cdot \log\left[\frac{1+(1+\Delta A)^2+2(1+\Delta A)\cos(\phi_{\varepsilon 1}+\phi_{\varepsilon 2})}{1+(1+\Delta A)^2-2(1+\Delta A)\cos(\phi_{\varepsilon 1}-\phi_{\varepsilon 2})}\right] \quad \text{(Eq A.17)}$$

Equation A.17 is identical to the result given in [AP.1][AP.2] for the more general class of single-sideband mixers.

Appendix B: Conversion Gain of an Idea Switching Mixer

This appendix is provided to give a brief review of the conversion gain characteristics of an ideal switching mixer. The switching can take place either in the form of commutating a voltage or a current signal. This has the net affect of taking any signal and multiplying it by a pulse train, which will from this point on described by *p(t)*.

The general situation of a switching mixer is shown in figure 130 where an arbitrary signal S(t) is applied to the input port of a mixer. The signal S(t) is effectively multiplied by a pulse train with a zero mean and amplitude of unity. The period of the pulse p(t) will be defined as T_{LO} (corresponding to the frequency of the local oscillator used by the mixer). Using the fact that multiplication in the time domain, is equivalent to convolution in the frequency domain, it can be shown that the mixer output will contain several copies of the input spectrum shifted in frequency by both the fundamental and various harmonics of the local oscillator, p(t). It is now of interest to

find the gain that the input signal S(t) experiences from the input to the output of the mixer during frequency translation.

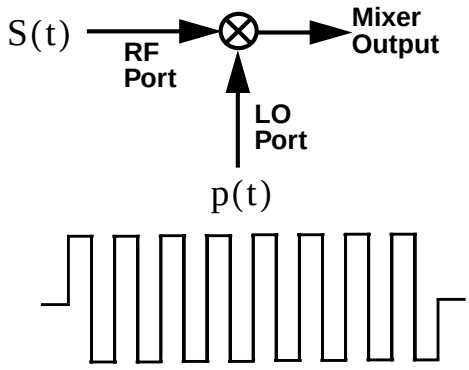

Figure 130. Model of an ideal switching mixer. S(t) represents either a voltage or current signal which will be commutated by switches, while p(t) models the pulsing action of the switches.

The best approach for finding the conversion gain of the mixer is to analyze what is going on in the frequency domain. p(t) is periodic and may be represented by the fourier series where the fourier coefficients can computed as,

$$p(t) = \sum_{k=-\infty}^{+\infty} p_k e^{jk\omega_o t} \qquad \text{(Eq A.18)}$$

The fourier coefficients p_k are given by,

$$p_k = \frac{1}{T_o} \int_{-\frac{T_o}{2}}^{\frac{T_o}{2}} p(t) e^{-jk\omega_n t} dt \qquad \text{(Eq A.19)}$$

One approach which facilitates computation of the fourier coefficients of p(t), is to offset the waveform such that the low end of the swing is zero and the high end of p(t) is twice the amplitude of the zero mean pulse; this is shown in figure 131. Once the fourier coefficients have been found, the DC component may be subtracted out to recover p(t). Although, it may be somewhat obvious to offset p(t) to get p'(t), it is worth

illustrating as this approach will be used again to find conversion of an active CMOS mixer. The offset version of p(t) will be defined as p'(t).

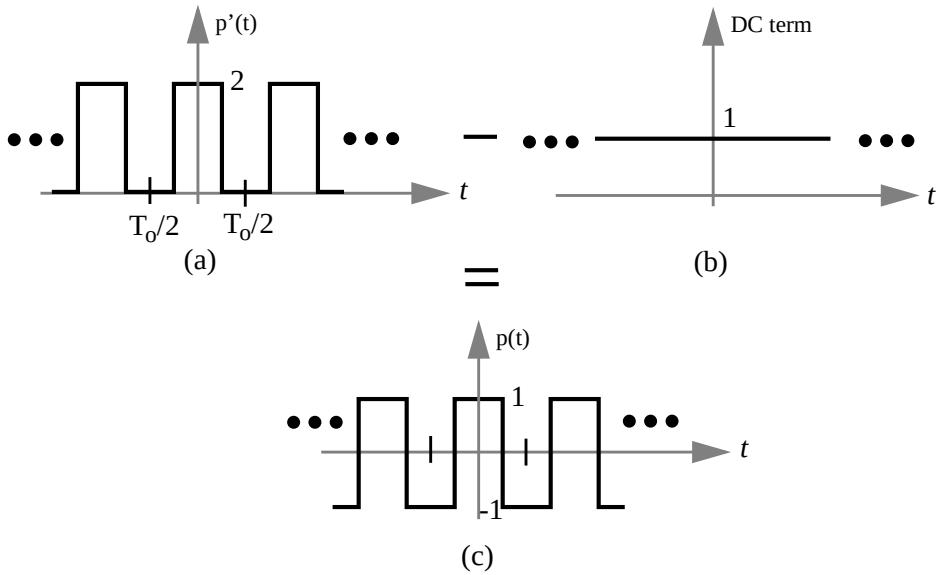

Figure 131. Offset added to p(t) which simplifies computation of the fourier series. (a) p'(t) pulse which is offset to simplify computation of the fourier coefficients. (b) The DC offset of 1 can be subtract from the fourier series representation to recover the original desired pulse p(t), shown in (c).

The fourier coefficients for the waveform p'(t) can be written as,

$$p_k = \frac{1}{T_o}\int_{-\frac{T_o}{4}}^{\frac{T_o}{4}} 2e^{-jk\omega_o t}dt \qquad \text{(Eq A.20)}$$

Solving equation A.20 results in the following expression for the fourier coefficients of p'(t),

$$p_k = \frac{2}{k\pi}\sin\left(\frac{k\pi}{2}\right) \qquad \text{(Eq A.21)}$$

The time domain expression for p(t) can be written as,

$$p'(t) = \sum_{k=-\infty}^{+\infty} \frac{2}{k\pi}\sin\left(\frac{k\pi}{2}\right)e^{jk\omega_o t} \qquad \text{(Eq A.22)}$$

It is useful to look at several values of k to notice a pattern which may be used to write a simpler and more useful expression for p(t). This is done for values of k=-3 through k=+3. Equation A.22 evaluated at k=-3 gives,

$$p'(t)\big|_{k=-3} = -\frac{2}{3\pi}e^{-j3\omega_o t} \quad \text{(Eq A.23)}$$

There is no energy in the signal at k=+/-2 as the sine function reduces to zero. For k=-1, 0, +1, +3 the fourier series representation in equation A.22 becomes,

$$p'(t)\big|_{k=-1} = -\frac{2}{\pi}e^{-j\omega_o t} \quad \text{(Eq A.24)}$$

$$p'(t)\big|_{k=1} = \frac{2}{\pi}e^{j\omega_o t} \quad \text{(Eq A.25)}$$

$$p'(t)\big|_{k=3} = \frac{2}{3\pi}e^{j3\omega_o t} \quad \text{(Eq A.26)}$$

L'Hopital's rule should be applied to get the k=0 term, which is nothing more than the DC component of p'(t). For k=0,

$$p'(t)\big|_{k=0} = 1 \quad \text{(Eq A.27)}$$

A pattern can be seen with all of the odd values of k which can be reassembled in the form of a cosine with respect to the harmonics of ω_o. p'(t) can be written as,

$$p'(t) = 1 + \frac{2}{\pi}(e^{j\omega_o t} + e^{-j\omega_o t}) + \frac{2}{3\pi}(e^{j3\omega_o t} + e^{-j3\omega_o t}) + \ldots\frac{2}{k\pi}(e^{jk\omega_o t} + e^{-jk\omega_o t}) \quad \text{(Eq A.28)}$$

$$p'(t) = 1 + \frac{4}{\pi}\sum_{k=1}^{\infty}\frac{1}{k}\sin\left(\frac{k\pi}{2}\right)\cos(k\omega_o t) \quad \text{(Eq A.29)}$$

To get p(t) from p'(t), the DC component must be subtracted out as shown in figure 131. This gives,

$$p(t) = p'(t) - 1 \quad \text{(Eq A.30)}$$

Leaving an expression of p(t) in terms of the harmonics of ω_o.

$$p(t) = \frac{4}{k\pi}\sum_{k=1}^{\infty}\sin\left(\frac{k\pi}{2}\right)\cos(k\omega_o t) \quad \text{(Eq A.31)}$$

For switching mixers, equation A.31 is probably one of the most fundamental equations describing the operation of this class of frequency translation device. Reflecting on the role of a mixer which is to frequency translate some incoming signal, in this case S(t), by another frequency either higher or lower than the frequency of S(t). To understand the frequency translation properties of the mixer, a idealized model can be constructed as a multiplication between a pulsed signal p(t) and the incoming signal S(t). This is expressed as,

$$S_o(t) = p(t) \cdot S(t) \qquad \text{(Eq A.32)}$$

Next, if it is assumed that the input signal S(t) can be described by a single tone where $S(t)=\cos(\omega_{rf}t)$, the output signal can be described as,

$$S_o(t) = \left(\frac{4}{\pi}\sum_{k=1}^{\infty}\frac{1}{k}\sin\left(\frac{k\pi}{2}\right)\cos(k\omega_o t)\right)\cdot\cos(\omega_{rf}t) \qquad \text{(Eq A.33)}$$

Expanding this results in the following form for $S_o(t)$.

$$S_o(t) = \frac{4}{\pi}\left(\frac{1}{2}[\cos((\omega_o-\omega_{rf})t)+\cos((\omega_o+\omega_{rf})t)]\right) - \frac{4}{3\pi}\left(\frac{1}{2}[\cos((3\omega_o-\omega_{rf})t)+\cos((3\omega_o+\omega_{rf})t)]\right)\ldots \qquad \text{(Eq A.34)}$$

For use in receiver applications, the term which contains the difference in frequency between ω_o and ω_{rf} ($\cos((\omega_o-\omega_{rf})t$) is of interest. The down-converted component is the useful signal which we hope to recover at the output of the mixer. Therefore, assuming that all of the other terms are removed with an ideal brickwall filter leaving just the difference frequency between the fundamental and incoming RF signal, $S_o(t)$ can now be written as,

$$S_o(t) = \frac{2}{\pi}\cos((\omega_o-\omega_{rf})t) \qquad \text{(Eq A.35)}$$

From equation A.35 the classic conversion gain which is given for an ideal switch mixer is shown to be “$2/\pi$”. In reality, as will be shown later, the non-idealities of the mixer actually reduce the value of the conversion gain to a value which is less than $2/\pi$. The result of $2/\pi$ for the conversion gain of a switching mixer is somewhat

classic and has also been shown in many other publications which include [AP.3][AP.4][AP.5][AP.6].

Appendix C: Conversion Gain of an Active Switching Mixer

A derivation of the conversion gain for a CMOS active mixer is presented in this appendix. Most of this section will focus on obtaining the fourier series coefficients of a pulse which closely models the non-idealities of a Gilbert Cell like mixer utilizing CMOS devices. In chapter 6, a more in depth discussion is given on both the topic of the conversion gain of a CMOS mixer as well as the input referred noise of this class of mixer.

The analysis begins by slightly modifying the shape of p(t) such that the switching time of the mixer is taken into account. During the time the mixer is in the balanced state (all of the switches are conducting current), the value of p(t) will be assumed to be linear. In other words, rather than a sharp transition from a low- to a high amplitude, the pulse p(t) follows a straight line from the low to high value. p'(t) can be described as shown in figure 132.

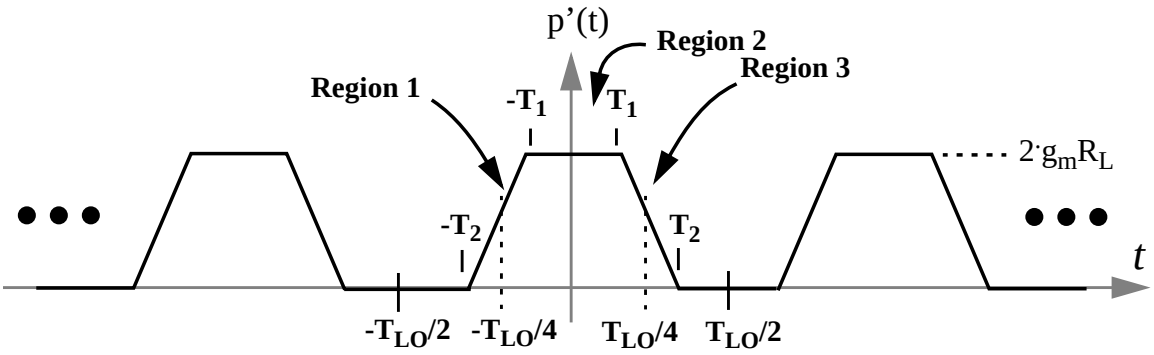

Figure 132. Waveform used to find the fourier series of the pulse which is used to compute the conversion gain of an active mixer.

The fourier coefficients for this waveform are computed in three separate cases regions which are identified as regions 1, 2 and 3 in figure 132. Region 1 is defined as the portion of the signal between $-T_2$ and $-T_1$ while region 2 is defined from $-T_1$ to T_1, and region 3 runs from T_1 to T_2. p'(t) in the region 1 can be described by,

$$p'(t) = 2g_m R_L \frac{(t + T_2)}{T_2 - T_1} \quad \text{(Eq A.36)}$$

In region 3. p'(t) can be described by,

$$p'(t) = 2g_m R_L \frac{(T_2 - t)}{T_2 - T_1} \quad \text{(Eq A.37)}$$

Again, the variables T_1 and T_2 define the begin and end of the transition time for current to completely flow from one set of mixer switches to the alternate set. It will be useful in the derivation of the fourier coefficients of the waveform given in figure 132, to define the relationship between T_1, T_2 and T_{LO}. The relationship between the three variables is easy to find when $T_{LO}/4$ is defined to be halfway between T_1 and T_2.

$T_1 = T_{LO}/4 - xT_{LO}/4$ $\qquad$ $T_2 = T_{LO}/4 + xT_{LO}/4$

The fourier coefficients of p'(t) can then be described by,

$$p_k = \frac{1}{T_{LO}} \int_{-\frac{T_{LO}}{2}}^{\frac{T_{LO}}{2}} p'(t) e^{-jk\omega_{LO}t} dt \quad \text{(Eq A.38)}$$

$$= \frac{1}{T_{LO}} \left[\int_{-T_2}^{-T_1} \left(2g_m R_L \frac{(t + T_2)}{T_2 - T_1} \right) e^{-jk\omega_{LO}t} d\,t + \int_{-T_1}^{T_1} 2g_m R_L e^{-jk\omega_{LO}t} dt + \int_{T_1}^{T_2} \left(2g_m R_L \frac{(T_2 - t)}{T_2 - T_1} \right) e^{-jk\omega_{LO}t} \right]$$

It is useful to solve each term individually in regions 1, 2, and 3, then recombine all terms and simplify at the end to obtain a final expression for p_k. The first integral in equation A.38 may be solved using integration by parts, this gives,

$$p_{k(region1)} = \frac{2g_m R_L}{T_{LO}} \left[\frac{-2te^{-jk\omega_{LO}t}}{(T_2 - T_1)jk\omega_{LO}} + \frac{2e^{-jk\omega_{LO}t}}{(T_2 - T_1)(k\omega_{LO})^2} - \frac{-2T_2 e^{-jk\omega_{LO}t}}{(T_2 - T_1)jk\omega_{LO}} \right] \Bigg|_{-T_2}^{-T_1} \quad \text{(Eq A.39)}$$

Evaluated for T_1 and T_2 gives,

$$p_{k(region1)} = \frac{2g_m R_L}{T_{LO}} \left[\frac{-e^{jk\omega_{LO}T_1}}{jk\omega_{LO}} + \frac{e^{jk\omega_{LO}T_1}}{(T_2 - T_1)(k\omega_{LO})^2} - \frac{e^{jk\omega_{LO}T_2}}{(T_2 - T_1)(k\omega_{LO})^2} \right] \quad \text{(Eq A.40)}$$

The integral for p_k in region 2 is somewhat trivial and results in,

$$p_{k(region2)} = \frac{4g_m R_L}{T_{LO}\omega_{LO}k}\sin(\omega_{LO}kT_1) \qquad \text{(Eq A.41)}$$

And finally the integral in region 3 gives,

$$p_{k(region3)} = \frac{2g_m R_L}{T_{LO}}\left[\frac{-2T_2 e^{-jk\omega_{LO}t}}{(T_2-T_1)jk\omega_{LO}} - \frac{2e^{-jk\omega_{LO}t}}{(T_2-T_1)(k\omega_{LO})^2} + \frac{-2te^{-jk\omega_{LO}t}}{(T_2-T_1)jk\omega_{LO}}\right]\Bigg|_{T_1}^{T_2} \qquad \text{(Eq A.42)}$$

Evaluated from T_1 to T_2 gives,

$$p_{k(region3)} = \frac{2g_m R_L}{T_{LO}}\left[\frac{-e^{-jk\omega_{LO}T_1}}{jk\omega_{LO}} - \frac{e^{-jk\omega_{LO}T_2}}{(T_2-T_1)(k\omega_{LO})^2} + \frac{e^{-jk\omega_{LO}T_1}}{(T_2-T_1)(k\omega_{LO})^2}\right] \qquad \text{(Eq A.43)}$$

Combining equations A.40, A.41, and A.43 as well as simplifying results in,

$$p_k = \frac{4g_m R_L}{T_{LO}}\left[\frac{\cos(k\omega_{LO}T_1)}{(T_2-T_1)(k\omega_{LO})^2} - \frac{\cos(k\omega_{LO}T_2)}{(T_2-T_1)(k\omega_{LO})^2}\right] \qquad \text{(Eq A.44)}$$

Again, the variables T_1 and T_2 define the beginning and end of the transition time for current to completely flow from one set of mixer switches to the alternate set. It will be useful in the derivation of the fourier coefficients of the waveform shown in figure 132, to define the relationship between T_1, T_2 and T_{LO}. The relationship between the three variables is easy to find if $T_{LO}/4$ is defined to be halfway between T_1 and T_2.

$$T_1 = \frac{T_{LO}}{4} - x\frac{T_{LO}}{4} \qquad T_2 = \frac{T_{LO}}{4} + x\frac{T_{LO}}{4}$$

$$T_1 = \frac{T_{LO}}{4}(1-x) \qquad T_2 = \frac{T_{LO}}{4}(1+x)$$

$$T_2 - T_1 = 2\frac{T_{LO}}{4}x = x\frac{T_{LO}}{2}$$

Substituting the above relations into equation A.19 gives,

$$p_k = \frac{4g_m R_L}{T_{LO}}\left[\frac{\cos\left(k\omega_{LO}\frac{T_{LO}}{4}(1-x)\right)}{x\frac{T_{LO}}{2}(k\omega_{LO})^2} - \frac{\cos\left(k\omega_{LO}\frac{T_{LO}}{4}(1+x)\right)}{x\frac{T_{LO}}{2}(k\omega_{LO})^2}\right] \qquad \text{(Eq A.45)}$$

This expression can be simplified to,

$$p_k = \frac{2g_m R_L}{x(k\pi)^2}\left[\cos\left(\frac{k\pi}{2}(1-x)\right) - \cos\left(\frac{k\pi}{2}(1+x)\right)\right] \qquad \text{(Eq A.46)}$$

And to obtain a simplified version of p_k after working through a little trig. gives,

$$p_k = \frac{4g_m R_L}{x(k\pi)^2}\left[\sin\left(\frac{k\pi}{2}\right)\sin\left(\frac{k\pi}{2}x\right)\right] \quad \text{(Eq A.47)}$$

Writing the general expression for p'(t) gives,

$$p'(t) = \frac{4g_m R_L}{x\pi^2}\sum_{k=-\infty}^{\infty}\frac{1}{k^2}\left[\sin\left(\frac{k\pi}{2}\right)\sin\left(\frac{k\pi}{2}x\right)\right]\cdot e^{jk\omega_{LO}t} \quad \text{(Eq A.48)}$$

Expanding out equation A.48 with respect to k, similar to what was done at the end of appendix B, a pattern can be observed which allows the simplification in the above expression for p'(t); this is given below as,

$$p'(t) = \frac{4g_m R_L}{x\pi^2}\sum_{k=-\infty}^{\infty}\frac{1}{k^2}\left[\sin\left(\frac{k\pi}{2}\right)\sin\left(\frac{k\pi}{2}x\right)\right]\cdot \cos(k\omega_{LO}t) - 1 \quad \text{(Eq A.49)}$$

p'(t) is obtained from p(t) by subtracting the DC component of 1 giving,

$$p(t) = \frac{4g_m R_L}{x\pi^2}\sum_{k=-\infty}^{\infty}\frac{1}{k^2}\left[\sin\left(\frac{k\pi}{2}\right)\sin\left(\frac{k\pi}{2}x\right)\right]\cdot \cos(k\omega_{LO}t) \quad \text{(Eq A.50)}$$

Appendix D: Fourier Coefficients for the Switch Transfer Function

Both the fourier coefficient and series, of the time varying transfer function from the switch input (LO input) to the output of mixer, are derived in appendix D. The waveform used to model the gain from the LO port mixer input port to the mixer output, is shown in figure 133, while the behavior is described in chapter 6 of this thesis. Similar to the approach used to find the fourier coefficients of the p(t) in the previous appendix, the waveform s(t) will be broken into four separate regions. The fourier

coefficients for each region are computed then combined at the end to get the comprehensive for coefficients for s(t).

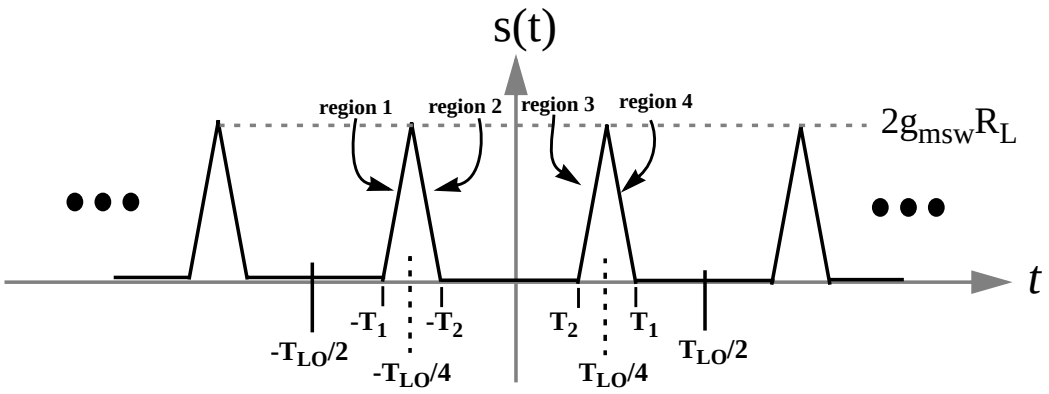

Figure 133. Periodic Pulse s(t) used to model the switch noise voltage transfer function from the LO port to the mixer output.

The mechanics for obtaining the fourier coefficients for a waveform is briefly reviewed in appendix B. Assuming s(t) is linear in regions 1,2,3, and 4 t, s_k can be found in all four regions. In region 1, s(t) is described by,

$$s(t)_{(region1)} = 2g_{msw}R_L\frac{(t+T_1)}{\left(T_1-\frac{T_{LO}}{4}\right)} \qquad \text{(Eq A.51)}$$

Using equation A.51 the fourier coefficients in region 1 are,

$$s_{k(region1)} = \frac{2g_{msw}R_L}{T_{LO}\left(T_1-\frac{T_{LO}}{4}\right)}\left[\frac{T_{LO}}{4}\frac{e^{jk\omega_{LO}\frac{T_{LO}}{4}}}{jk\omega_{LO}}+\frac{e^{jk\omega_{LO}\frac{T_{LO}}{4}}}{(k\omega_{LO})^2}-\frac{e^{jk\omega_{LO}T_1}}{(k\omega_{LO})^2}-T_1\frac{e^{jk\omega_{LO}\frac{T_{LO}}{4}}}{jk\omega_{LO}}\right] \qquad \text{(Eq A.52)}$$

In region 2 s(t) and s_k are described by,

$$s(t)_{(region2)} = 2g_{msw}R_L\frac{(t+T_2)}{\left(T_2-\frac{T_{LO}}{4}\right)} \qquad \text{(Eq A.53)}$$

$$s_{k(region2)} = \frac{2g_{msw}R_L}{T_{LO}\left(T_2-\frac{T_{LO}}{4}\right)}\left[-\frac{T_{LO}}{4}\frac{e^{jk\omega_{LO}\frac{T_{LO}}{4}}}{jk\omega_{LO}}-\frac{e^{jk\omega_{LO}\frac{T_{LO}}{4}}}{(k\omega_{LO})^2}+\frac{e^{jk\omega_{LO}T_2}}{(k\omega_{LO})^2}-T_2\frac{e^{jk\omega_{LO}\frac{T_{LO}}{4}}}{jk\omega_{LO}}\right]$$

Region 3 s(t) and s_k are respectively,

$$s(t)_{(region3)} = 2g_{msw}R_L\frac{(t-T_2)}{\left(\frac{T_{LO}}{4}-T_2\right)} \quad \text{(Eq A.54)}$$

(Eq A.55)

$$s_{k(region3)} = \frac{2g_{msw}R_L}{T_{LO}\left(T_2-\frac{T_{LO}}{4}\right)}\left[\frac{T_{LO}}{4}\frac{e^{-jk\omega_{LO}\frac{T_{LO}}{4}}}{jk\omega_{LO}}-\frac{e^{-jk\omega_{LO}\frac{T_{LO}}{4}}}{(k\omega_{LO})^2}+\frac{e^{-jk\omega_{LO}T_2}}{(k\omega_{LO})^2}-T_2\frac{e^{-jk\omega_{LO}\frac{T_{LO}}{4}}}{jk\omega_{LO}}\right]$$

And finally both s(t) and sk in region 4.

$$s(t)_{(region4)} = 2g_{msw}R_L\frac{(t-T_1)}{\left(\frac{T_{LO}}{4}-T_1\right)} \quad \text{(Eq A.56)}$$

(Eq A.57)

$$s_{k(region4)} = \frac{2g_{msw}R_L}{T_{LO}\left(T_1-\frac{T_{LO}}{4}\right)}\left[-\frac{T_{LO}}{4}\frac{e^{-jk\omega_{LO}\frac{T_{LO}}{4}}}{jk\omega_{LO}}+\frac{e^{-jk\omega_{LO}\frac{T_{LO}}{4}}}{(k\omega_{LO})^2}-\frac{e^{-jk\omega_{LO}T_1}}{(k\omega_{LO})^2}+T_1\frac{e^{-jk\omega_{LO}\frac{T_{LO}}{4}}}{jk\omega_{LO}}\right]$$

Now defining both T_1 and T_2 in terms of T_{LO} as.

$T_1=T_{LO}/4+xT_{LO}/4$ $\qquad$ $T_2=T_{LO}/4-xT_{LO}/4$

Note: The definitions of T_1 and T_2 are the opposite of what was given in appendix C. This was done unintentionally and not meant to confuse any reader.

Combining $s_{k(region1)}$, $s_{k(region2)}$, $s_{k(region3)}$, and $s_{k(region4)}$ with the above substitutions for T_1 and T_2 results in.

$$s_k = (2g_{msw}R_L)\frac{4}{x}\left[\frac{\sin\left(k\frac{\pi}{2}\right)}{4k\pi}+\frac{\cos\left(k\frac{\pi}{2}\right)}{2(k\pi)^2}-\frac{\cos\left(k\frac{\pi}{2}\right)}{2(k\pi)^2}-\frac{(1+x)\sin\left(k\frac{\pi}{2}\right)}{4k\pi}\right] \quad \text{(Eq A.58)}$$

$$-\quad (2g_{msw}R_L)\frac{4}{x}\left[-\frac{\sin\left(k\frac{\pi}{2}\right)}{4k\pi}+\frac{\cos\left(k\frac{\pi}{2}\right)}{2(k\pi)^2}-\frac{\cos\left(k\frac{\pi}{2}\right)}{2(k\pi)^2}+\frac{(1+x)\sin\left(k\frac{\pi}{2}\right)}{4k\pi}\right]$$

This reduces to,

$$s_k = (2g_{msw}R_L)\frac{4}{x}\left[\frac{\cos\left(k\frac{\pi}{2}\right)}{(k\pi)^2}\left(1-\cos\left(\frac{k\pi}{2}x\right)\right)\right] \quad \text{(Eq A.59)}$$

To obtain an expression for s(t) the fourier coefficients were used in conjunction with the definition of a signal represented as a fourier series.

$$s(t) = \sum_{k=-\infty}^{+\infty} s_k e^{jk\omega_{LO}t} \quad \text{(Eq A.60)}$$

Next, finding s(t) for a few values of k, a pattern can be observed which simplifies the final form of s(t). Starting with k=-4.

$$s(t)_{k=-4} = (2g_{msw}R_L)\frac{4}{x}\left[\frac{1-\cos(2\pi x)}{16\pi^2}\right]e^{-j4\omega_{LO}t} \quad \text{(Eq A.61)}$$

The case of k=-3, $s(t)_{k=-3} = 0$ and the for k=-2 gives,

$$s(t)_{k=-2} = (2g_{msw}R_L)\frac{4}{x}\left[\frac{1-\cos(\pi x)}{4\pi^2}\right]e^{-j2\omega_{LO}t} \quad \text{(Eq A.62)}$$

For k=-1, $s_{-1} = 0$ while for k=0 results in a solution of 0/0. Therefore, for k=0, L'Hopital's rule must be applied twice on $s(t)_{k=0}$ which results in,

$$s(t)_{k=0} = (2g_{msw}R_L)\frac{x}{2} \quad \text{(Eq A.63)}$$

The pattern can now be observed that for k odd, S(t) is zero while for k=2 and 4, gives s(t) as respectively,

$$s(t)_{k=2} = (2g_{msw}R_L)\frac{4}{x}\left[\frac{1-\cos(\pi x)}{4\pi^2}\right]e^{j2\omega_{LO}t} \quad \text{(Eq A.64)}$$

$$s(t)_{k=4} = (2g_{msw}R_L)\frac{4}{x}\left[\frac{1-\cos(2\pi x)}{16\pi^2}\right]e^{j4\omega_{LO}t} \quad \text{(Eq A.65)}$$

Observing a pattern s(t) can be written as,

$$s(t) = (2g_{msw}R_L)\left[\frac{x}{2} + \sum_{k=1}^{\infty}\frac{8}{x}\frac{\cos\left(k\frac{\pi}{2}\right)}{(k\pi)^2}\left(1-\cos\left(\frac{k\pi}{2}x\right)\right)\cos(k\omega_{LO}t)\right] \quad \text{(Eq A.66)}$$

Appendix E: Phase Mismatch Analysis for a simple RC-CR phase shifter

The following is a derivation of the phase and gain error, as a function of mismatch in both the value of R and C for a single-ended RC-CR filter. From chapter 7,

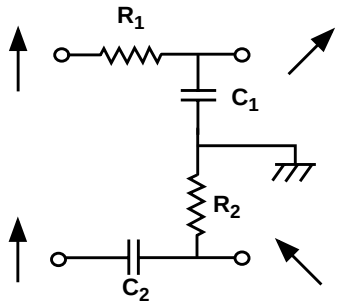

Figure 134. Simple RC-CR phase shifter.

it was shown that the difference in phase between both the input and output, of the simple phase shifting filter, can be expressed as,

$$\varphi(R, C) = -\pi/2 + (\tan(\omega R_2 C_2) - \tan(\omega R_1 C_1)) \qquad \text{(Eq A.67)}$$

As mention in chapter 7, when R1 = R2 and C1 = C2, the phase in this idealized situation is simply 90^o. Next, it will be assumed that a mismatch exists between the Rs and Cs in this filter. The mismatch between R1, R2, C1, and C2, for the purposes of analysis on the all three phase shifting configurations, will be represented as the following.

$$\Delta R = R_1 - R_2 \qquad \Delta C = C_1 - C_2$$

$$R_1 = R + \frac{\Delta R}{2} \qquad C_1 = C + \frac{\Delta C}{2}$$

$$R_2 = R - \frac{\Delta R}{2} \qquad C_2 = C - \frac{\Delta C}{2}$$

Substituting the above equations into equation A.67, the following is obtained.

$$\Delta\varphi(R, C) = (\tan(\omega R_2 C_2) - \tan(\omega R_1 C_1)) \qquad \text{(Eq A.68)}$$

or,

$$\Delta\varphi(R, C) = \left(\tan\left(\omega\left(R - \frac{\Delta R}{2}\right)\left(C - \frac{\Delta C}{2}\right)\right) - \tan\left(\omega\left(R + \frac{\Delta R}{2}\right)\left(C + \frac{\Delta C}{2}\right)\right)\right) \quad \text{(Eq A.69)}$$

expanding and removing higher order terms, the following is obtained,

$$\Delta\varphi(\Delta R, \Delta C) = \left(\operatorname{atan}\left(\omega\left(RC - C\frac{\Delta R}{2} - R\frac{\Delta C}{2} + \frac{\Delta R\Delta C}{4}\right)\right) - \operatorname{atan}\left(\omega\left(RC + C\frac{\Delta R}{2} + R\frac{\Delta C}{2} + \frac{\Delta R\Delta C}{4}\right)\right)\right) \quad \text{(Eq A.70)}$$

$$\Delta\varphi(\Delta R, \Delta C) = \left(\operatorname{atan}\left(\omega\left(RC - C\frac{\Delta R}{2} - R\frac{\Delta C}{2}\right)\right) - \operatorname{atan}\left(\omega\left(RC + C\frac{\Delta R}{2} + R\frac{\Delta C}{2}\right)\right)\right) \quad \text{(Eq A.71)}$$

Using the trigonometric identity,

$$\operatorname{atan}(x) - \operatorname{atan}(y) = \operatorname{atan}\left(\frac{x - y}{1 + xy}\right) \quad \text{(Eq A.72)}$$

setting,

$$x = \left(RC - C\frac{\Delta R}{2} - R\frac{\Delta C}{2}\right) \text{ and } \quad y = \left(RC + C\frac{\Delta R}{2} + R\frac{\Delta C}{2}\right)$$

rewriting equation A.71, substituting for both x and y results in the following,

$$\Delta\varphi(\Delta R, \Delta C) = \operatorname{atan}\left(\frac{-\omega RC\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right)}{1 + \left(RC - C\frac{\Delta R}{2} - R\frac{\Delta C}{2}\right)\omega\left(RC + C\frac{\Delta R}{2} + R\frac{\Delta C}{2}\right)\omega}\right) \quad \text{(Eq A.73)}$$

or

$$\Delta\varphi(\Delta R, \Delta C) = \operatorname{atan}\left(\frac{-\omega RC\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right)}{1 + \omega^2(RC)^2\left(1 + \frac{\Delta R}{2R} + \frac{\Delta C}{2C} - \frac{\Delta R}{2R} - \frac{\Delta C}{2C} - \frac{1}{4}\left(\frac{\Delta R}{R}\right)^2 - \frac{\Delta R\Delta C}{2RC} - \frac{1}{4}\left(\frac{\Delta C}{C}\right)^2\right)}\right) \quad \text{(Eq A.74)}$$

Assuming the mismatch is small, all of the higher order terms in the denominator of equation A.74, can be ignored. This results in,

$$\Delta\varphi(\Delta R, \Delta C) = \operatorname{atan}\left(\frac{-\omega RC\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right)}{1 + \omega^2(RC)^2}\right) \quad \text{(Eq A.75)}$$

Equation A.75 can be further simplified assuming that the filter is operating at or near the 3dB frequency of the RC filter, which it would need to be to ensure gain matching between the quadrature outputs. For $\omega \approx \omega_{3dB}$ and $\Delta R, \Delta C \ll 1$,

$$\Delta\varphi(\Delta R, \Delta C) \approx \frac{\Delta R}{2R} + \frac{\Delta C}{2C} \qquad \text{(Eq A.76)}$$

Appendix F: Constant Magnitude Phase Shifting Filter.

The following is a mismatch analysis of the constant magnitude quadrature phase generator. A description, as well as discussion of this phase shifter are given in chapter 7. For the purposes of this analysis, the configuration in figure 135 will be used

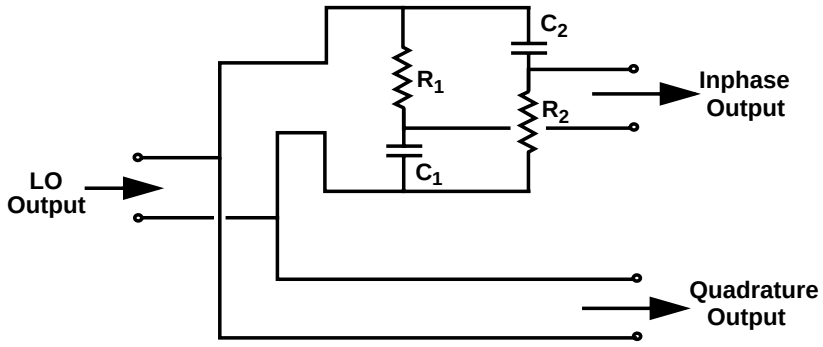

Figure 135. Constant Magnitude Phase shifting output.

along with the same definitions for ΔR, ΔC, R1, C1, R2, and C2 from the analysis given in appendix A.

In section 7.2.2, it was shown that without a mismatch, the phase difference between the I and Q outputs can be written as,

$$\varphi(R, C) = -2\,\mathrm{atan}(\omega RC) \qquad \text{(Eq A.77)}$$

Again, assuming that a mismatch exists in both the R and C of the above filter network, the transfer function between the LO Output and the In-phase Output can be described by,

$$H(j\omega) = \frac{1}{1 + j\omega R_1 C_1} - \frac{j\omega R_2 C_2}{1 + j\omega R_2 C_2} \qquad \text{(Eq A.78)}$$

Again, substituting in values for R1 R2, C1, and C2 and expanding we have,

$$H(j\omega) = \frac{1 + \omega^2\left(C - \frac{\Delta C}{2}\right)\left(C + \frac{\Delta C}{2}\right)\left(R - \frac{\Delta R}{2}\right)\left(R + \frac{\Delta R}{2}\right)}{1 + j\omega\left(R + \frac{\Delta R}{2}\right)\left(C + \frac{\Delta C}{2}\right) + j\omega\left(R - \frac{\Delta R}{2}\right)\left(C - \frac{\Delta C}{2}\right) - \omega^2\left(C^2 - \left(\frac{\Delta C}{2}\right)^2\right)\left(R^2 - \left(\frac{\Delta R}{2}\right)^2\right)} \quad \text{(Eq A.79)}$$

This then can be written as,

$$H(j\omega) = \frac{1 + \omega^2\left(C - \frac{\Delta C}{2}\right)\left(C + \frac{\Delta C}{2}\right)\left(R - \frac{\Delta R}{2}\right)\left(R + \frac{\Delta R}{2}\right)}{\left(1 + j\omega RC\left(1 + \frac{\Delta R}{2R}\right)\left(1 + \frac{\Delta C}{2C}\right)\right)\left(1 + j\omega RC\left(\left(1 - \frac{\Delta R}{2R}\right)\left(1 - \frac{\Delta C}{2C}\right)\right)\right)} \quad \text{(Eq A.80)}$$

This can finally be written as.

$$I(j\omega) = \frac{\left(1 + j\omega RC\sqrt{\left(1 - \left(\frac{\Delta C}{2C}\right)^2\right)\left(1 - \left(\frac{\Delta R}{2R}\right)^2\right)}\right)\left(1 - j\omega RC\sqrt{\left(1 - \left(\frac{\Delta C}{2C}\right)^2\right)\left(1 - \left(\frac{\Delta R}{2R}\right)^2\right)}\right)}{\left(1 + j\omega RC\left(1 + \frac{\Delta R}{2R}\right)\left(1 + \frac{\Delta C}{2C}\right)\right)\left(1 + j\omega RC\left(\left(1 - \frac{\Delta R}{2R}\right)\left(1 - \frac{\Delta C}{2C}\right)\right)\right)} \quad \text{(Eq A.81)}$$

Extracting the phase from H(jω) gives,

$$\angle H(j\omega) = -\operatorname{atan}\left(\omega RC\left(1 + \frac{\Delta R}{2R}\right)\left(1 + \frac{\Delta C}{2C}\right)\right) - \operatorname{atan}\left(\omega RC\left(\left(1 - \frac{\Delta R}{2R}\right)\left(1 - \frac{\Delta C}{2C}\right)\right)\right) \quad \text{(Eq A.82)}$$

Using the trigonometric identity.

$$\operatorname{atan}(x) + \operatorname{atan}(y) = \operatorname{atan}\left(\frac{x + y}{1 - xy}\right) \quad \text{(Eq A.83)}$$

Equation A.82 can now be written as,

$$\angle H(j\omega) = -\operatorname{atan}\left(\frac{2\omega RC\left(1 + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1 - (\omega RC)^2\left(1 - \left(\frac{\Delta R}{2R}\right)^2\right)\left(1 - \left(\frac{\Delta C}{2C}\right)^2\right)}\right) \quad \text{(Eq A.84)}$$

Taking the phase difference of a filter with no mismatch, equation A.77, and subtracting equation A.84, gives the total phase error as a function of the mismatch in resistors and capacitors.

$$\Delta\varphi(\omega, \Delta R, \Delta C) = 2\operatorname{atan}(\omega RC) - \operatorname{atan}\left(\frac{2\omega RC\left(1 + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1 - (\omega RC)^2\left(1 - \left(\frac{\Delta R}{2R}\right)^2\right)\left(1 - \left(\frac{\Delta C}{2C}\right)^2\right)}\right) \quad \text{(Eq A.85)}$$

Appendix G: Miller Capacitance Phase Shifter Transfer Function

The 90^o phase shift which is created in the buffer is done so with a Miller capacitor placed from the drain to the source of the input source coupled pair. This capacitor is shown as C_F in figure 136. The phase relationship between the input and

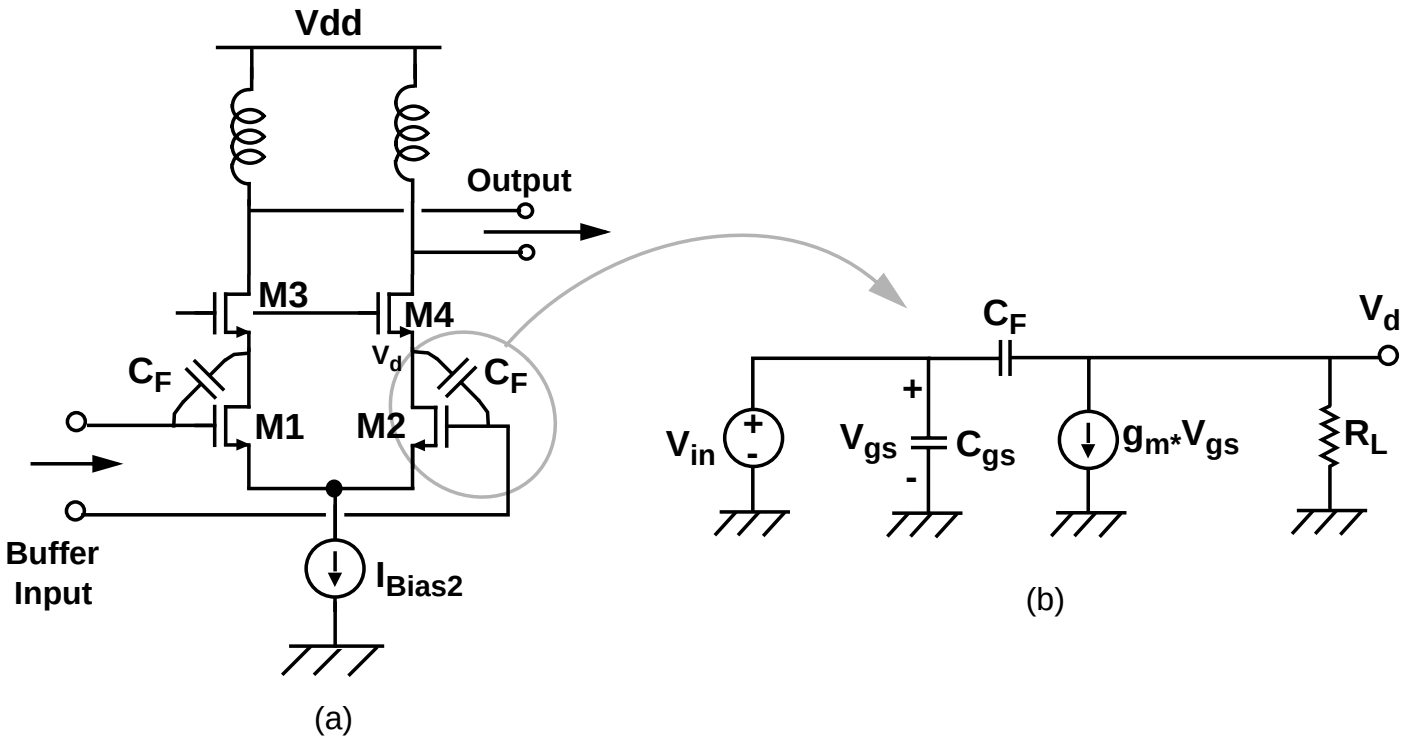

Figure 136. (a) Buffer with feed forward capacitor (b) equivalent half-circuit for just the source coupled pair.

output of the buffer can be understood finding the transfer function from the buffer input to the drain of the device M2. Although, this will not give the voltage transfer function of the buffer, it does provide insight into the phase relationship which is created between the buffer input and output; the phase difference between V_d and the buffer output will be the same. Using the small-signal model given in figure 136(b) while applying a test source V_{IN}. Noticing that $V_{IN}=V_{gs}$ and using Kirchoff's current law on the input node gives,

$$(V_d - V_{IN})sC_F + g_m V_{IN} + \frac{V_d}{R_L} = 0 \qquad \text{(Eq A.86)}$$

With a little algebra, the following transfer function between the drain and gate of the input device can be obtained.

$$\frac{V_d}{V_{IN}}(s) = \frac{-g_m R_L\left(1 - \frac{sC_F}{g_m}\right)}{(1 + sC_F R_L)} \quad \text{(Eq A.87)}$$

Substituting s=jω gives,

$$\frac{V_d}{V_{IN}}(j\omega) = \frac{-g_m R_L\left(1 - \frac{j\omega C_F}{g_m}\right)}{(1 + j\omega C_F R_L)} \quad \text{(Eq A.88)}$$

Using the assumption that the impedance at the drain of the input device can be approximated as $R_L=1/g_m$ results in,

$$\frac{V_d}{V_{IN}}(j\omega) = \frac{-g_m R_L\left(1 - \frac{j\omega C_F}{g_m}\right)}{\left(1 + j\omega\frac{C_F}{g_m}\right)} \quad \text{(Eq A.89)}$$

When the frequency of the input signal is equal to g_m/C_F, the transfer function can be simplified to,

$$\frac{V_d}{V_{IN}}(j\omega) = \frac{-g_m R_L(1 - j)}{(1 + j)} \quad \text{(Eq A.90)}$$

Further simplifying gives,

$$\frac{V_d}{V_{IN}}(j\omega) = j \cdot g_m R_L \quad \text{(Eq A.91)}$$

Note the “j” left in the transfer function, this gives rise to the 90^o phase shift between the input and output voltage of the source coupled pair.

Appendix H: Polyphase filter mismatch and phase change

The analysis of the effect on phase error due to the mismatch in a polyphase filter is given in this section. The analysis is carrier out on a single stage of a polyphase filter. The analysis is first applied to the case of a single phase type II input. These results are then extended to the both the cases of mismatch with a single phase type I and quadrature inputs applied to the polyphase filter .

While the exact analysis of the phase error created as a function of the mismatch in both the resistors and capacitors is considerable involved, insight may be obtained by decomposing the polyphase filter into an I and Q signal paths. Then analyze the affect of mismatch on one of the two paths. The situation is illustrated in figure 137(a) with a vector signal diagram for a single phase type II input. In this example, a single phase signal (shown on the x-axis of figure 137(a)) is applied to two of the four polyphase filter inputs in figure 137 (b), as discussed in section 7.2.4 on page 207. At the output of the first stage polyphase filter, channels 1 and 3 may be taken differentially to obtain the Q phase signal, while 2 and 4 may be used for the I phase signal. The differential input signal in figure 137(a), is ideally rotated with a positive

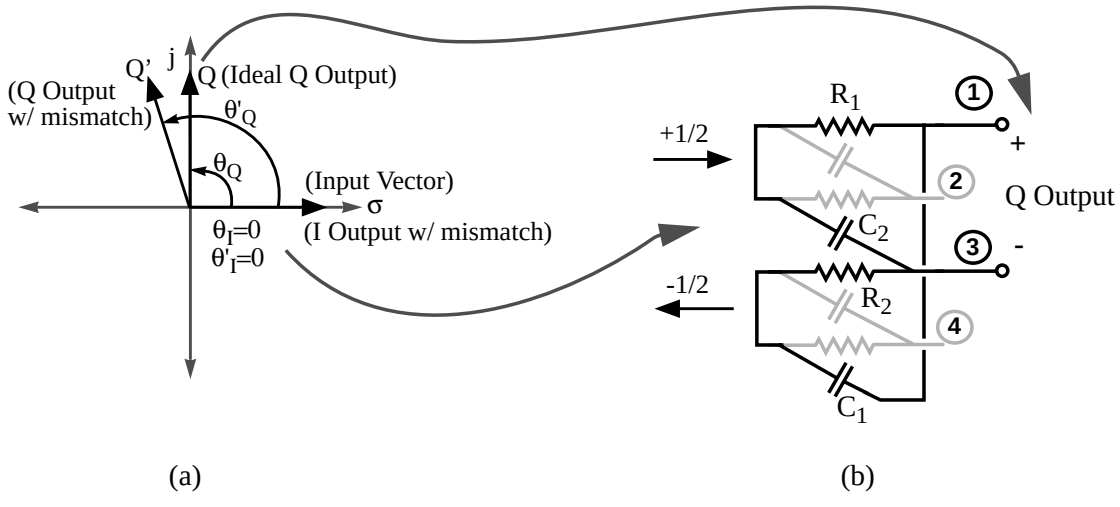

Figure 137. A mismatch analysis on a single stage of a polyphase filter. This filter has been decomposed into a mismatch analysis on just one of the two signal paths.

phase of θ_Q. However, for the case of mismatch in both the resistors and capacitors of the polyphase filter, the resulting phase will be altered to give the vector θ'_Q. The total

phase error for just the Q signal path can be expressed as $\Delta\varphi_{II} = \theta'_Q - \theta_Q$. The phase at the output, in the I path, will be identical to the input phase applied to the filter. Thus, there will be no phase error generated by component mismatch in the I path. The total phase error generated between the I and Q signal paths can be found by evaluating $\Delta\varphi_{II} = \theta'_Q - \theta_Q$ as a function of the mismatch in R and C values, along the Q path only.

First, a an expression is given for outputs of one and three in figure 137(b) as function of ω, R_1, R_2, C_1, and C_2. The output labeled as 1 can be expressed as,

$$\frac{1}{2}\left(\frac{(1 - j\omega R_1 C_1)}{(1 + j\omega R_1 C_1)}\right) \qquad \text{(Eq A.92)}$$

The output of channel 3 is,

$$\frac{1}{2}\left(\frac{(-1 + j\omega R_2 C_2)}{(1 + j\omega R_2 C_2)}\right) \qquad \text{(Eq A.93)}$$

Taking the difference of the channel 1 and 3 and working through some math gives.

$$Q(j\omega) = \frac{(1 + \omega^2 R_1 C_1 R_2 C_2)}{(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2)} \qquad \text{(Eq A.94)}$$

Using the following definitions for R_1, R_2, C_1, and C_2.

$$R_1 = R + \frac{\Delta R}{2} \qquad C_1 = C + \frac{\Delta C}{2}$$

$$R_2 = R - \frac{\Delta R}{2} \qquad C_2 = C - \frac{\Delta C}{2}$$

Substituting the above values for resistor and capacitor offset results in,

$$Q(j\omega) = \frac{\left(1 + \omega^2\left(R + \frac{\Delta R}{2}\right)\left(C + \frac{\Delta C}{2}\right)\left(R - \frac{\Delta R}{2}\right)\left(C - \frac{\Delta C}{2}\right)\right)}{\left(1 + j\omega\left(R + \frac{\Delta R}{2}\right)\left(C + \frac{\Delta C}{2}\right)\right)\left(1 + j\omega\left(R - \frac{\Delta R}{2}\right)\left(C - \frac{\Delta C}{2}\right)\right)} \qquad \text{(Eq A.95)}$$

Working through the math on equation A.95 gives,

$$Q(j\omega) = \left[\frac{1 + \omega^2 R^2 C^2\left(1 - \left(\frac{\Delta R}{2R}\right)^2\right)\left(1 - \left(\frac{\Delta C}{2C}\right)^2\right)}{\left(1 + j\omega RC\left(1 + \frac{\Delta R}{2R} + \frac{\Delta C}{2C} + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)\right)\left(1 + j\omega RC\left(1 - \frac{\Delta R}{2R} - \frac{\Delta C}{2C} + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)\right)}\right] \qquad \text{(Eq A.96)}$$

Extracting the phase from Q(jω) and adding the ideal phase without mismatch, similar to what was done in appendix F gives,

$$\Delta\varphi(\omega, \Delta R, \Delta C) = 2\,\mathrm{atan}(\omega RC) - \mathrm{atan}\left(\omega RC\left(1 + \frac{\Delta R}{2R} + \frac{\Delta C}{2C} + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)\right) \qquad \text{(Eq A.97)}$$
$$- \mathrm{atan}\,\omega RC\left(1 - \frac{\Delta R}{2R} - \frac{\Delta C}{2C} + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)$$

Again using the trigonometric identity of,

$$\mathrm{atan}(x) + \mathrm{atan}(y) = \mathrm{atan}\left(\frac{x + y}{1 - xy}\right) \qquad \text{(Eq A.98)}$$

Using the above identity with equation A.97 results in,

$$\Delta\varphi(\omega, \Delta R, \Delta C)_{II} = 2\,\mathrm{atan}(\omega RC) - \mathrm{atan}\left(\frac{2\omega RC\left(1 + \frac{\Delta R}{2R}\frac{\Delta C}{2C}\right)}{1 - (\omega RC)^2\left(1 - \left(\frac{\Delta R}{2R}\right)^2\right)\left(1 - \left(\frac{\Delta C}{2C}\right)^2\right)}\right) \qquad \text{(Eq A.99)}$$

Note the result is identical to that given for the mismatch in a constant magnitude phase shifter. This to be expect as the phase in the I path of the polyphase is not altered between the input and the output; thus, the polyphase filter with a single phase type II input is effectively identical to the constant magnitude phase shifter. However, it is worth rederiving this result using the phase relationship given for a single phase type II input polyphase filter.

The result given in equation A.99 can easily be extended by inspection, to the two other cases of the polyphase filter input discussed in chapter 7. For a polyphase filter with both single phase type II and Quadrature phase relationships applied to the input, the error which is generated is now twice the phase error given in equation A.99. This can be seen by looking at how a mismatch between component values will affect the output phase error. In the type II input, a component mismatch will only generate a phase error in one of the two possible output signal paths. This can be understood by simply looking at the I output path in figure 137. Here the components which generate the I path output (these are the lightly shaded Rs and Cs) are being feed with the same phase signal on both ends of the resistor and capacitor which make up a pole or zero. The phase at the input and output will obviously be identical. Therefore, a mismatch in

component values for the single phase type II input, *will have no affect on the phase at the output of the I path*. In contrast, when a single phase type I input or quadrature input is applied to a polyphase, a component mismatch in both the I and Q paths will generate a phase error. This is illustrated in figure 138 for a polyphase filter with a single phase type I input.

An approximation for the phase error due to component mismatch in the case of either the single phase type I or quadrature input phases is simply twice the phase error generated by a single phase type II input. The worst case phase error due to mismatch in both the type I and quadrature inputs can be written as,

$$\Delta\varphi(\omega, \Delta R, \Delta C)_I = 2\Delta\varphi(\omega, \Delta R, \Delta C)_Q = 2\Delta\varphi(\omega, \Delta R, \Delta C)_{II} \quad \text{(Eq A.100)}$$

Where $\Delta\varphi(\omega, \Delta R, \Delta C)_I$ and $\Delta\varphi(\omega, \Delta R, \Delta C)_Q$ designate the phase error as a function of frequency and component mismatch for the single phase type I and quadrature inputs respectively.

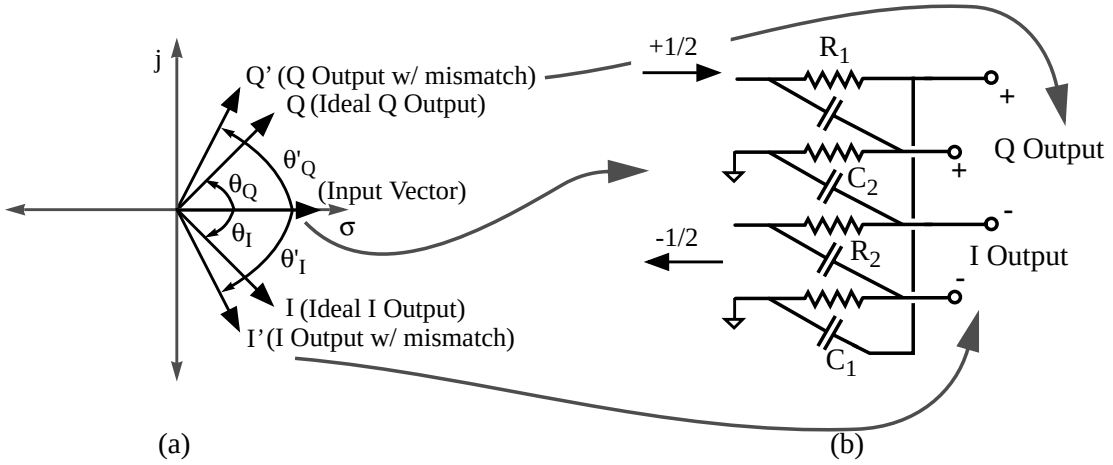

Figure 138. (a) Vector description of the phase error which is generated with a single phase type I input (b) Polyphase filter with input and output phase relationships.

Appendix I: Relation between Peak and Mid-Swing Triode Resistance

In chapter 7, of this thesis some approximations were made to find the required channel resistance of a PMOS device in the triode region of operation using a replica

biased circuit. The resistance of a PMOS device which is in triode, is easily estimated by taking the derivative with respect to V_{ds} of the well known drain-source current equation for a MOS device in triode, this results in,

$$R_{PMOS} = \frac{1}{\frac{\partial I_{ds}}{\partial V_{ds}}} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)((V_{gs} - V_t) - V_{ds})} \quad \text{(Eq A.101)}$$

When the single-sided output of the replica biased buffer is at the minimum voltage, the drain to source voltage is equal to V_{sw}. At the minimum output voltage, the drain-to-source resistance of the PMOS devices will be at a maximum, and can be defined as,

$$R_{peak} = \frac{1}{\frac{\partial I_{ds}}{\partial V_{ds}}} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)((V_{gs} - V_t) - V_{sw})} \quad \text{(Eq A.102)}$$

When the device is in the mid. swing, the resistance can be expressed as,

$$R_{mid} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)\left((V_{gs} - V_t) - \frac{V_{sw}}{2}\right)} \quad \text{(Eq A.103)}$$

Taking the ratio of the equation A.102 to equation A.103 and assuming the (Vgs-Vt) of the device remains constant for the entire buffer output swing, the relationship between R_{peak} and R_{mid} can be expressed as,

$$\frac{R_{peak}}{R_{mid}} = \frac{(V_{gs} - V_t) - \frac{V_{sw}}{2}}{(V_{gs} - V_t) - V_{sw}} \quad \text{(Eq A.104)}$$

Expressing $(V_{gs}-V_t)$ as a fraction of V_{sw} with the following relation $\zeta = (V_{gs} - V_t)/V_{sw}$. Equation A.104 can now be expressed as,

$$\frac{R_{peak}}{R_{mid}} = \frac{\zeta - \frac{1}{2}}{\zeta - 1} \quad \text{(Eq A.105)}$$

Appendix J: Peak Resistance verses Required Buffer Bandwidth

The following is a quick derivation of the maximum resistance which can be used at the output of a replica biased buffer, running at any frequency. The derivation assume that the buffer output will settle to within 15% of the desired voltage swing set by the replica biased circuit. Assuming a fixed resistance for the entire output swing and defining the time before switching as, t_{max}, the following expression can be written.

$$0.85V_{sw} = V_{sw}\left(1 - e^{\frac{-t_{max}}{R_{peak}C}}\right) \quad \text{(Eq A.106)}$$

Solving R_{peak} gives,

$$R_{peak} = \frac{-t_{max}}{\ln(0.15)C} \quad \text{(Eq A.107)}$$

t_{max} is equivalent to half the period of the buffer output signal. This then allows writing equation A.107 with respect to frequency.

$$R_{peak} = \frac{-1}{2f \cdot \ln(0.15) \cdot C} \quad \text{(Eq A.108)}$$

Appendix K: Derivation of stacked device MOS battery voltage

All of the reference bias voltages and currents used in both the DECT and GSM/DECT projects, were generated on chip. A standard bandgap reference circuit was replicated in several strategic locations of both receivers described in this thesis. The bias was generated exclusively on-chip to reduce the possibility of unwanted noise or spurious signals coupling in through the bondwires. In chapter 7, section 7.4.1, the ΔVgs/ΔVbe standard bias circuit was described which produced a reference current. The output of this current source, often times feed a set of stacked diodes which generated some of the bias voltages used throughout the receiver. One simple method to convert a reference current to a DC bias voltage is the use of a series of stacked CMOS devices. The circuit shown in figure 139, consists of two devices stacked and feed with the reference current source into the drain, of the top device. The bottom transistor (M1) is forced into the triode region by the gate-to-source voltage of M2. All of the devices above M1 are in saturation.

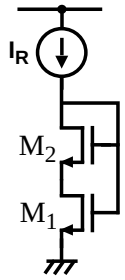

Figure 139. CMOS battery created with stacked devices.

Below is an estimate of the bias voltage generated at the drain of the top stacked transistor as a function of the reference current and the device sizes. The analysis is carried out on two stacked NMOS devices, shown in figure 139. The key to finding $V_{BIAS}(I_R, W/L_{M1}, W/L_{M2})$ is to observe that M1 is in fact in the triode region, while M2 is in saturation and all the drain currents are equal $I_R = I_D = I_{D1} = I_{D2}$. Using the drain current expression for a triode device.

$$I_D = k_p\left(\frac{W}{L}\right)_{M1}[(V_{GS_{M1}} - V_t)\cdot V_{DS_{M1}} - V_{DS_{M1}}^2/2] \qquad \text{(Eq A.109)}$$

Substituting $V_{GS_{M1}} = V_{BIAS}$ and $V_{DS_{M1}} = V_{BIAS} - V_{GS_{M2}}$ in to equation A.109 gives,

$$I_D = k_p\left(\frac{W}{L}\right)_{M1}[(V_{BIAS} - V_t)(V_{BIAS} - V_{GS_{M2}}) - (V_{BIAS} - V_t)^2/2] \qquad \text{(Eq A.110)}$$

Expanding and eliminating terms results in,

$$I_D = k_p\left(\frac{W}{L}\right)_{M1}[V_{BIAS}^2/2 - V_t\cdot(V_{BIAS} - V_{GS_{M2}}) - V_{GS_{M2}}^2/2] \qquad \text{(Eq A.111)}$$

Setting equation A.111 equal to zero then gives,

$$0 = V^2_{BIAS} - 2V_t\cdot V_{BIAS} + 2V_t\cdot V_{GS_{M2}} - V_{GS_{M2}}^2 - \frac{2I_D}{\left(k_p\left(\frac{W}{L}\right)_{M1}\right)} \qquad \text{(Eq A.112)}$$

Solving for V_{BIAS}, where the coefficients to the quadratic equation are,

$$a = 1$$

$$b = -2V_t$$

$$c = 2V_t\cdot V_{GS_{M2}} - V_{GS_{M2}}^2 - \frac{2I_D}{\left(k_p\left(\frac{W}{L}\right)_{M1}\right)}$$

Using a, b, and c in the quadratic equation gives.

$$V_{BIAS} = V_t \pm \sqrt{V_t^2 - 2V_t\cdot V_{GS_{M2}} + V_{GS_{M2}}^2 + \frac{2I_D}{k_p\left(\frac{W}{L}\right)_{M1}}} \qquad \text{(Eq A.113)}$$

Next, substituting $V_{GS_{M2}} = \sqrt{k_p\left(\frac{W}{L}\right)_{M2}} + V_t$ into equation A.113 and simplifying results in,

$$V_{BIAS} = V_t + \sqrt{\frac{2I_D}{k_p}\left(\frac{L}{W_{M2}} + \frac{L}{W_{M1}}\right)} \qquad \text{(Eq A.114)}$$

Equation A.114 ignores the body effect and assumes that the threshold voltage of both devices is identical. Although, V_t will be significantly different (a few hundred millivolts), equation A.114 gives a reasonable first order estimate for the bias voltage as a function of the reference current and the aspect ratios of M1 and M2. Equation A.114 can easily be extended to the case of N transistors stacked in series.

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