Design Techniques for High Performance Intgrated Frequency Synthesizers for Multi-standard Wireless Communication Applications

by

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B.S. (Portland State University, Portland) 1994
M.S. (University of California, Berkeley) 1996

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering-Electrical Engineering
and Computer Sciences

in the

GRADUATE DIVISION

of the

UNIVERSITY OF CALIFORNIA, BERKELEY

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Fall 2000

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University of California, Berkeley

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Abstract

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Professor Paul R. Gray, Chair

The growing importance of wireless media for voice and data communications is driving a need for higher integration in personal communications transceivers in order to achieve lower cost, smaller form factor, and lower power dissipation. One approach to this problem is to integrate the RF functionality in low-cost CMOS technology together with the baseband transceiver functions. This in turn requires integration of the frequency synthesizer with enough isolation from supply noise to allow the synthesizer to coexist with other on-chip transceiver circuitry and still meet the phase noise performance requirements of the application.

This research proposes a differential synthesizer for block-down-convert receivers that achieves improved levels of phase noise and supply rejection performance through the use of fully differential architecture and a wide-

bandwidth PLL. Analytical relationships for such a system relating output phase noise to system design parameters and internal noise sources are developed. A prototype systems embodying the design principles, and also embodying new differential circuit configurations which minimize supply coupling is designed, laid out and fabricated. The performance of the prototype synthesizer as a stand alone device is evaluated. The synthesizer is embodied in a complete integrated radio system and the performance of the synthesizer in the complete radio system is also evaluated.

Paul R. Gray, Chairman of Committee

Acknowledgments

It has been a great privilege to be a graduate student in the EECS department at the University of California, Berkeley and work closely with my advisor Professor Paul R. Gray. His keen insight into system and integrated circuit design is the key factor in the success of this research. Professor Gray will always be my role model as a person who has the highest degree of professionalism and integrity.

I would also like to thank Professor Robert G. Meyer for the numerous technical discussions. Professor Meyer's invaluable guidance was especially important in the absence of Professor Paul R. Gray due to his administrative responsibilities. I also thank Professor Joseph M. Khan and Professor Kjell Doksum for serving on my qualifying examination committee and reviewing this thesis.

I greatly appreciate the help from my colleagues in Professor Gray's group as well as peers from other research groups. I would like to thank Luns Tee who has worked closely with me in the past five years. He is a person who would never run out of ideas. Many thanks to Chris Rudell for his leadership in both technical and managerial aspects of this immense transceiver project that involved more than fifteen people and lasted more than four years. Without him, we would not have pulled the project through. My cubical-mates, George Chien and Martin Tsai have made the working environment a lot more enjoyable. I also

thank other colleagues Jeff Ou, Keith Onodera, Sekhar Narayanaswami, Andrew Abo, Jeff Weldon, Todd Weigandt, Arnold Feldman and David Cline for their support and friendship.

I am deeply grateful to my parents Jiade Lin and Biru Wang for their love and support in my whole life. Their confidence in me and their high expectation of me are the driving forces of my completion of one of the best and toughest graduate programs in the world. I am also grateful to my husband Dr. Minggui Pan who can always lift up my spirit even in the worst time. Being a busy doctor himself, he helps out as much as possible in taking care of our baby daughter Judy and the house chores. I also thank my sister Lan Lin who is always an inspiration and comfort to me.

I would like to thank my colleagues at Broadcom, Haideh Khorramabadi and Arya Behzad for their support while I was finishing my testing and thesis.

I would like to thank National Semiconductor Wireless Communication Group for providing testing equipment. Specifically, I thank Steve Lo, Wai Lau, Edwin Chan and Catsten Anderson for their support.

This project was supported by the National Science Foundation # CCR-9732550.

Chapter 1

Introduction

1.1 Motivation

The wireless personal communication market has been growing explosively due to ever emerging new applications and dropping prices. A low-cost, small, long-battery-life solution has been the dream for decades. Many efforts have been devoted to the integration of such circuits in low-cost technology in order to reach the goal.

The applications of wireless communication devices include pagers, cordless phones, cellular phones, global positioning systems and wireless local area networks, transmitting either voice or data. A standard tells how devices talk to each other. Numerous standards exist which are optimized for different implementations. For voice, examples include DECT, AMPS, GSM, DCS, PCS, CDMA, and so on. For data, there are 802.11 WLAN, Bluetooth, Home RF and so on. Costs have been driven down by technology improvement and better

design. What was previously available only in military applications is now available for the mass market. The rapidly growing market and ever emerging new applications create a high demand for a low cost, low power, high portability transceiver solution.

Current commercial approaches utilize several high quality discrete components to provide high performance required by transceiver. Each discrete component can cost from $1 to $5. High component counts and multiple chips in various technologies increase the cost and form factor. A higher integration level is required to lower the cost and form factor.

Many efforts are underway to increase the integration level of the transceiver. The ultimate goal would be a single chip transceiver in a single technology with a minimum number of off-chip components, that is, an antenna to receive or transmit the RF signal, a power supply, and a crystal reference to provide a clean frequency reference. This single chip would act as an interface between the analog RF world and the digital baseband world. With high integration level, cost and form factor is reduced.

However, many difficulties remain in the process of integration due to the lack of high quality components on chip. In a conventional double conversion receiver, the received signal spectrum is shifted down to the baseband in two steps. During the first step, a local oscillator signal at RF is mixed with the RF signal, shifting the signal to a fixed IF frequency. To achieve this, the RF LO

needs to be tunable and the minimum frequency step must be smaller or equal to the channel spacing of the standard. Then a fixed local oscillator at IF is used to shift the mixed down version of the received signal to baseband. The RF LO utilizes a low-phase-noise VCO which is coupled to a reference oscillator by a synthesizer loop of low bandwidth. The low bandwidth is desirable in order to minimize the spurious tones in the output frequency spectrum that result from the frequency comparison process. One consequence of the low synthesizer control bandwidth is that the phase noise of the overall synthesizer is dominated by the phase noise of the VCO. This makes the narrow loop bandwidth approach suitable for the implementation with discrete high Q components that is needed by the low phase noise VCO. The need for the external components is not amenable to integration of the synthesizer.

A major challenge is to find ways to realize low-phase-noise synthesizers with low-Q components. One approach is to use a wide synthesizer control bandwidth to couple a noisy on-chip oscillator to a very-low-phase-noise crystal more closely than a conventional narrow-band PLL so that the output is more dependent on the clean reference. The phase noise contribution from the on-chip oscillator to the output close to the carrier within the synthesizer control bandwidth is thus suppressed. Because a wide PLL bandwidth requires a high comparison frequency, this type of synthesizer is most amenable to the synthesis of a few widely spaced frequencies, and is thus most compatible with block-

down-convert receiver architectures such as the wideband IF double conversion architecture [1]. In this architecture, the entire signal band at RF is mixed down to the IF with a fixed RF frequency synthesizer and a variable frequency synthesizer at IF is used to tune the desired channel from IF to the baseband. The fact that high Q discrete components are not needed is amenable to integration of the synthesizer.

The IF frequency synthesizer in the wideband IF architecture is used to tune the individual channels. Because this second synthesizer is at a much lower frequency, minimization of its phase noise contributions is much easier. But the spurious tone specification is much harder because the reference frequency to the PLL is now at the channel spacing. One approach is to use a narrowband PLL which suppresses the tones outside the PLL bandwidth. By doing the channel selection at IF, the divider ratio required is RF/IF times smaller than doing it at RF. The smaller divider ratio not only reduces the tones generated by the PLL assuming a fixed PLL bandwidth, but also reduces the phase noise contribution to the output from the frequency reference, the phase detector and the divider.

For many applications transceiver integration levels will be such that the receiver path, transmit path, the complete synthesizer, and perhaps the RF power amplifier will coexist on a single integrated circuit, along with a significant amount of A/D conversion and baseband processing. This in turn requires the synthesizer maintain its phase noise and spurious tone performance in the

presence of components which deliver significant current and voltage perturbations to both the substrate GND and supply. Fully differential implementation of the complete PLL path is important for this reason.

1.2 Summary of Research Results

This research focuses on the utilization of the wide-band PLL concept and fully differential approach to realize an integrated RF synthesizer that is capable of the extremely demanding performance required in cellular telephone applications.

Fundamental performance limits of a wide-band PLL based synthesizer are investigated. Because noise from the VCO is suppressed in wideband PLL architectures, other noise sources become more important in the overall synthesizer performance. Noise from the crystal oscillator reference, phase/ frequency detector become the most important contributors within the loop bandwidth and are referred to the output enhanced in effect by the divider ratio N. Noise from charge pump and loop filter is amplified by the VCO gain around the loop bandwidth. For an integrated wideband PLL, the VCO gain is usually large because of the limited control voltage range and large frequency range required by the application. Thus the charge pump and loop filter are significant noise contributors at the offset frequency around the loop bandwidth.

Various circuit techniques to reduce the phase noise and spurious tones and to improve the power supply rejection ratio are explored. To verify the effectiveness of the techniques, a 1.4GHz differential low-noise CMOS frequency synthesizer using a wideband PLL architecture was designed and fabricated in a 0.35μm CMOS 5-metal, 2-poly technology. The prototype produces three RF frequencies, namely, 1.3824GHz, 1.4688GHz, and 1.5552GHz corresponding to the frequency plan of the dual-mode transceiver application, while achieving a phase noise of -118dBc/Hz at 100kHz, a spurious tone of -56dBc at 86.4MHz. When a 0.8MHz 200mV peak-to-peak sinewave is added to the supply, the synthesizer generates a spurious tone of -42dBc. When the 200mV tone is present the synthesizer phase noise at 100kHz degrades to -116dBc/Hz. The complete synthesizer dissipates 84mW from a 3.3V supply. A 400MHz IF frequency synthesizer was also designed, laid out, and fabricated in the same technology, providing tuning capability for a complete radio system. The RF synthesizer and IF synthesizer are embodied in a complete integrated radio system and the performance of the synthesizers in the complete radio system were evaluated.

1.3 Thesis Organization

In Chapter 2, the fundamentals of frequency synthesizer including the synthesizer role and its key parameters are reviewed. Various synthesizer architectures and their advantages and disadvantages are discussed.

In Chapter 3, the fundamental limitations of the wideband PLL architecture is examined.

In Chapter 4, low-noise design techniques for each synthesizer block are presented, including a low-noise differentially-controlled VCO, a low noise charge pump with active loop filter, and a low noise buffer.

In Chapter 5, the design of an experimental prototype and the measurement results are presented.

Chapter 6 concludes the thesis with a summary.

Chapter 2

Fundamentals of Frequency Synthesis

2.1 Role of Frequency Synthesizer

The role of a frequency synthesizer is to provide the reference frequency for frequency translation. Fig. 2.1 shows the typical block diagram of a cellular phone RF section. An RF synthesizer and an IF synthesizer are used for the frequency translation.

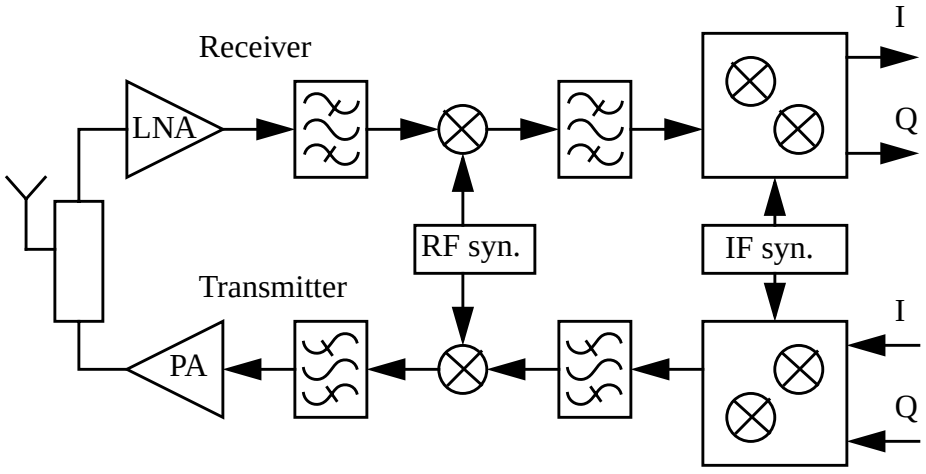


Fig. 2.1: Synthesizer in cellular application

As shown in Fig. 2.2, an ideal frequency synthesizer generates a single frequency tone. In the receiver case, it mixes with the received RF signal spectrum and shifts it down to baseband. In the transmitter case, it mixes with the modulated baseband signal and shifts it up to RF. In both cases, the output spectrum is the convolution result of the synthesizer tone with the received signal spectrum or the modulated baseband signal spectrum, e.g.,

$$S_z = S_x \otimes S_y \qquad \text{(Eq 2-1)}$$

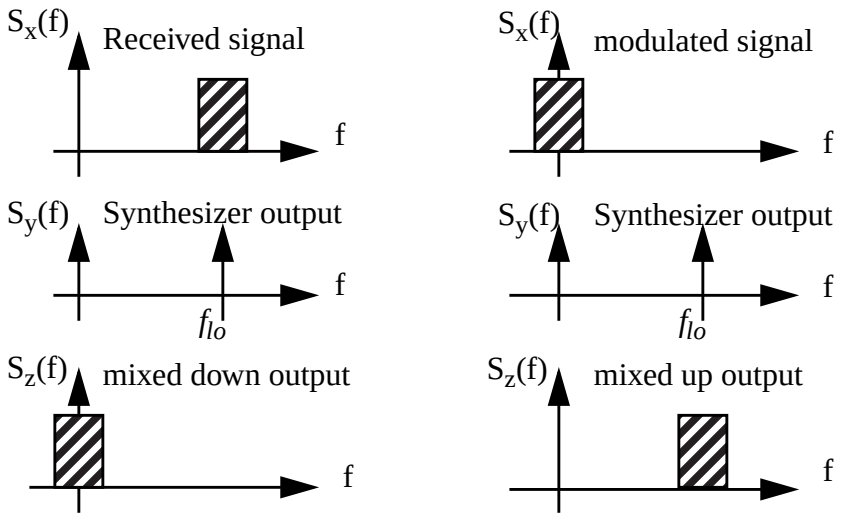


Fig. 2.2: Role of frequency synthesizer

2.2 Key Parameters in Frequency Synthesizer's Performance

2.2.1 Introduction

In the previous section we showed that the ideal output spectrum of a frequency synthesizer should be a single tone at the desired frequency in order to provide the reference frequency for frequency translation. A single tone in the frequency domain is equivalent to a pure sinusoidal waveform in the time domain. The random and systematic amplitude and phase deviations from the desired values produce energy in the frequencies other than the desired frequency. When this energy is mixed with the received RF signal or modulated baseband signal, undesired sidebands are created. Phase noise and spurious tones are the two key parameters to measure the quality of a frequency synthesizer. In the next two sections, we will discuss the mathematical model of phase noise and spurious tones and their effects on a transceiver.

2.2.2 Mathematical Model of Phase Noise and Spurious Tones

The ideal synthesizer has a pure sinusoidal waveform

$$v(t) = V_0 \cos(2\pi f_0 t) \qquad \text{(Eq 2-2)}$$

When amplitude and phase fluctuations are included, the waveform becomes

$$v(t) = [V_0 + \varepsilon(t)]\cos[2\pi f_0 + \phi(t)] \qquad \text{(Eq 2-3)}$$

where $\varepsilon(t)$ represents amplitude fluctuations and $\phi(t)$ represents phase fluctuations. Because amplitude fluctuations can be removed or greatly reduced by a limiter, we concentrate on phase fluctuations in a frequency synthesizer design.

There are three types of phase fluctuations:

- Systematic variations, due to the aging of the resonator material for example, reflects the long term stability.
- Deterministic periodic variations due to unwanted frequency or phase modulations.
- Random variations due to noise sources such as thermal, shot, flicker noise in electronic components.

In mathematical form, $\phi(t)$ can be written as:

$$\phi(t) = at^2 + \sin(2\pi f_m t) + \varphi(t) \qquad \text{(Eq 2-4)}$$

The first term represents a linear frequency drift since instantaneous frequency is the time rate of change of phase divided by 2π. This term is usually small enough to be negligible.

The second term represents the periodic phase modulation and it produces a spurious tone at an offset frequency of f_m from the carrier frequency f_0. The magnitude of the spurious tone can be derived as follows:

$$v(t) = V_0 \cos(2\pi f_0 + \Delta\phi \sin 2\pi f_m t) \qquad \text{(Eq 2-5)}$$

$$v(t) = V_0[\cos 2\pi f_0 t \cos(\Delta\phi \sin 2\pi f_m t) - \sin 2\pi f_0 t \sin(\Delta\phi \sin 2\pi f_m t)] \qquad \text{(Eq 2-6)}$$

For small phase modulation, e.g., $\Delta\phi \ll \pi/2$

$$\cos(\Delta\phi \sin 2\pi f_m t) \approx 1 \qquad \text{(Eq 2-7)}$$

$$\sin(\Delta\phi \sin 2\pi f_m t) \approx \Delta\phi \sin 2\pi f_m t \qquad \text{(Eq 2-8)}$$

$$v(t) \approx V_0[\cos 2\pi f_0 t - \Delta\phi \sin 2\pi f_0 t \sin 2\pi f_m t] \qquad \text{(Eq 2-9)}$$

$$v(t) \approx V_0\left[\cos 2\pi f_0 t - \frac{\Delta\phi}{2}\cos 2\pi(f_0 - f_m)t + \frac{\Delta\phi}{2}\cos 2\pi(f_0 + f_m)t\right] \qquad \text{(Eq 2-10)}$$

From (Eq 2-9) we can tell there are two spurious tones generated by this phase modulation, one at f_m above carrier f_0, the other at f_m below f_0. The power ratio of the spurious tone to the carrier is $-10\log(\Delta\phi/2)^2$. The unit for the spurious tone is dBc, meaning the spurious is $-10\log(\Delta\phi/2)^2$ dB below carrier.

The third term represents the random phase fluctuations. The spectral density of phase noise is

$$S_\varphi(f) = \int_{-\infty}^{\infty} R_\varphi(\tau) e^{-j2\pi f\tau} d\tau \qquad \text{(Eq 2-11)}$$

where

$$R_\varphi(\tau) = E[\varphi(\tau)\varphi(t-\tau)] \qquad \text{(Eq 2-12)}$$

When amplitude fluctuations are negligible and the root-mean-square (rms) value of $\varphi(t)$ is much smaller than 1 radian, the spectral purity of $v(t)$ can be approximated as

$$S_v(f) \approx \frac{V_0^2}{2} \cdot [\delta(f - f_0) + S_\varphi(f - f_0)] \quad \text{(Eq 2-13)}$$

Phase noise is specified as the ratio of noise power in 1Hz bandwidth at a certain offset frequency from carrier to the carrier power. The unit is dBc/Hz.

$$\Phi(f) = 10\log\frac{P_{noise}}{P_{carrier}}(dBc/Hz) \quad \text{(Eq 2-14)}$$

2.2.3 Effect of Phase Noise and Spurious Tones on Transceiver Performance

Any noise in the circuit or environment will create phase disturbance. In Fig. 2.3, a nonideal frequency synthesizer spectrum is shown. It is no longer a single frequency tone but rather a smeared version. The energy under the skirt is phase noise. Sometimes the energy is concentrated at frequencies other than the desired frequency, appearing as a spike above the skirt. This energy is due to a spurious tone. Phase noise and spurious tones are the two key performance parameters of a frequency synthesizer.

In a receiver, the spurious tones and phase noise of the frequency synthesizer can mix with the undesired signal and produce noise in the desired channel. This reduces the sensitivity and selectivity of a receiver.

Similarly, in a transmitter, the spurious tones and the phase noise of the frequency synthesizer can mix with the modulated baseband signal and produce

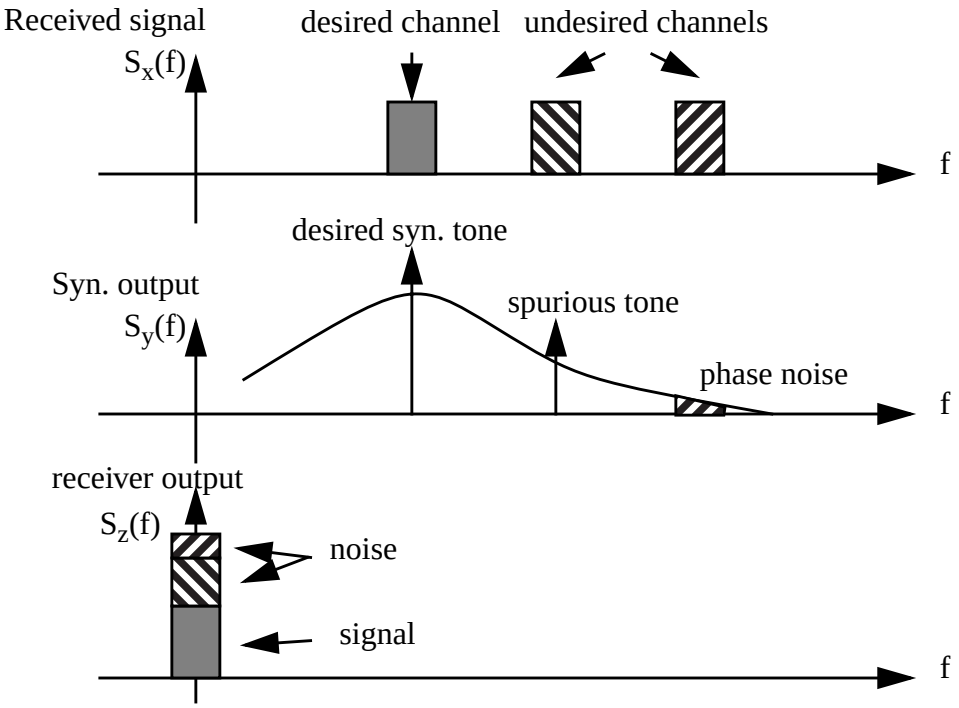


Fig. 2.3: Effect of phase noise and spurious tones in a receiver

undesired spectral emissions, increase adjancent channel interference, and reduce the modulation accuracy.

2.3 Synthesizer Alternatives

2.3.1 Introduction

There are many ways to implement a frequency synthesizer. For an integrated multi-standard radio transceiver, we want the synthesizer to be able to generate a tunable frequency in the gigahertz range with low phase noise and low spurious tones using minimum power. A direct digital frequency synthesizer is best known for its fast switching and very fine frequency resolution. It can

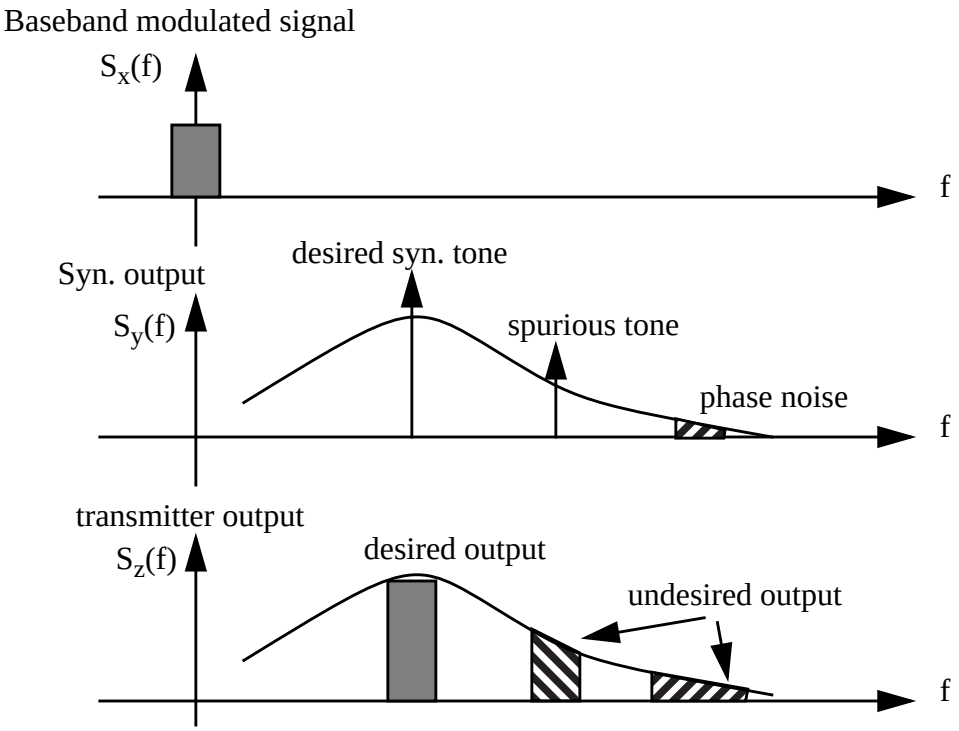


Fig. 2.4: Effect of phase noise and spurious tones in a transmitter

also easily be integrated because no off chip components are required. But due to technology limitations, it takes large power consumption to synthesize very high frequencies directly. Usually a second frequency translation is needed to shift the center frequency to the GHz range. A phase-locked-loop-based frequency synthesizer with narrow loop bandwidth is the most commonly used technique due to its high performance, namely, low phase noise and low spurious tones. But the need for off chip high-Q components is not amenable to the integration of the synthesizer. In addition, the narrow loop bandwidth makes it unsuitable in an agile system where fast frequency switching is needed. A Fractional-N synthesizer is a modified version of the narrow band PLL. It greatly relieves the constraint on the loop bandwidth so that faster frequency

switching can be achieved. But it generates large spurious tones due to the periodic switching of the divider mode. The automatic phase interpolation technique is used to reduce the spurious tones but the requisite complexity makes the technique only suitable for very high performance applications such as testing instruments.

2.3.2 Direct Digital Frequency Synthesizer

Fig. 2.5 shows the basic block diagram of a Direct Digital Frequency Synthesizer. The phase accumulator accumulates its output with the frequency setting word at every clock cycle. The output increases linearly until the accumulator maximum count is reached and the accumulation starts from zero again. Hence the phase accumulator output follows a periodical sawtooth pattern. The frequency of this sawtooth pattern is the synthesizer output frequency f_{out}. It is determined by the frequency setting word length L_{set}, the accumulator length L_{acc}, and the clock frequency f_{clk}, as in .

$$f_{out} = f_{clk} \cdot \frac{L_{set}}{L_{acc}} \qquad \text{(Eq 2-15)}$$

A ROM converts the digital phase value at the output of the phase accumulator to a digital amplitude value according to the lookup table stored in the ROM. In a typical case, the conversion is cosine. A DAC then converts the digital amplitude value into an analog waveform. The waveform goes through a low-pass filter so that the output spectral purity is improved.

Because the DDFS is an open-loop structure, output frequency

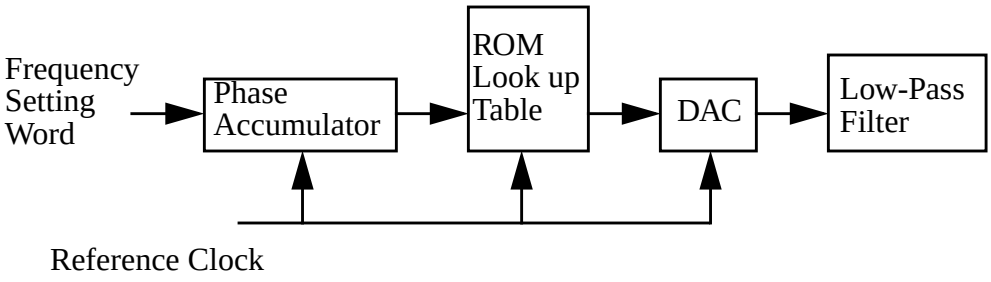


Fig. 2.5: DDFS block diagram

switching can be done in a few clock cycles. This fast switching capability is one of the reasons that DDFS is preferred in an extremely agile system, such as a frequency-hopped spread- spectrum system. Both frequency and phase modulation can be implemented by simply modulating L_{set} in digital domain. Very small frequency increments can be achieved. In fact, the minimum frequency increment is the clock frequency divided by the accumulator length. Fractional Hz can easily be achieved. DDFS is also amenable to integration because no off chip components are required.

However, the spectral purity of the DDFS is limited by the DAC speed and resolution because the finite resolution in quantization leads to inaccurate representation of the sinusoid and hence spurious outputs. If the output frequency is a subharmonic of the clock frequency, then the output is free of spurious tones. Otherwise, spurious tones are about 6dB per bit of DAC. For cellular applications, typical spurious tones levels of -56dBc or lower are

desired and a 9-bit DAC would be required. However, it is difficult to build a 9-bit DAC in the GHz range with current technology. High power consumption is needed for high frequency operation.

2.3.3 Phase-Locked-Loop Frequency Synthesizer

A Phase-Locked-Loop is a loop which locks the output phase or frequency to an accurate reference. Fig. 2.6 shows the block diagram of a typical PLL. A voltage-controlled oscillator (VCO) generates an output waveform at a frequency set by the control voltage V_{ctrl}. The Phase/Frequency Detector (PFD) compares the phase/frequency of a divided reference frequency f_{ref} with the divided output phase/frequency f_2 . When the loop is locked, the PFD sees two identical waveforms at its inputs and f_o equals to Nf_{ref}. As shown in the waveform, if for some reason $f_{ref} > f_1$, $Vctrl$ goes down and the VCO output frequency decreases. Vice versa, if $f_{ref} < f_1$, V_{ctrl} goes up and the VCO output frequency increases. A loop filter (LPF) is used to stabilize the loop by introducing zeros and poles into the loop.

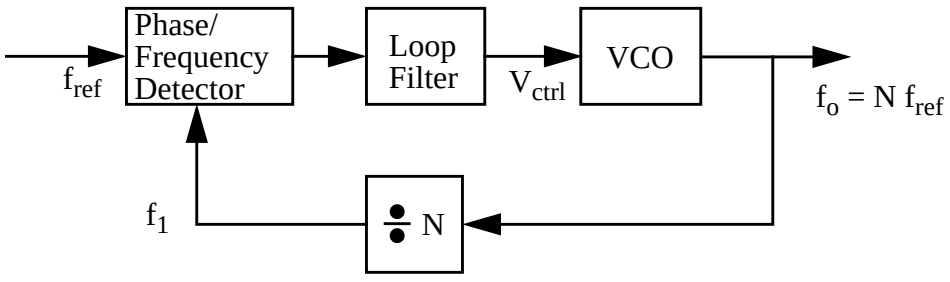


Fig. 2.6: Phase-Locked-Loop block diagram

There are many different ways to implement the circuit blocks of a PLL. Generally, a linearized model can be used to get more insight into the PLL design. Fig. 2.7 shows the linear model of a typical PLL.

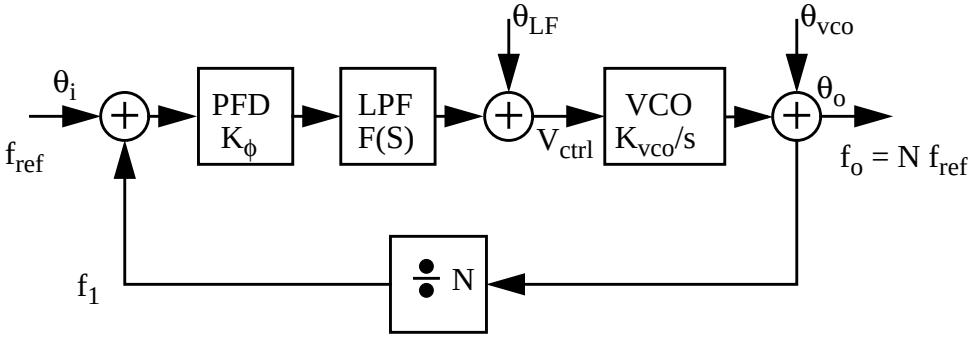


Fig. 2.7: Phase-Locked-Loop linear model

In the linear model, the PFD has a gain of K_ϕ, the loop filter has a transfer function *F(s)*, and the VCO has a gain of K_{vco}*(Hz/V)*. Because phase is the integrated value of frequency, an integrator *1/s* is included into the VCO block so that the VCO block has a gain of K_{vco}/s. The open loop gain *G(s)* can be written as

$$G(s) = \frac{K_\phi F(s) K_{vco}}{Ns} \qquad \text{(Eq 2-16)}$$

The PLL bandwidth f_{PLL} is defined as the frequency when the open-loop gain drops to unity.

The sum of phase noise from the reference, phase detector and the frequency divider is represented by θ_i. The noise transfer function from θ_i to output is

$$\frac{\theta_o}{\theta_i} = N\frac{G(s)}{1+G(s)} \qquad \text{(Eq 2-17)}$$

Notice that the transfer function is a low-pass transfer function with a gain of N at frequencies below the loop bandwidth. This means the noise contribution from the reference, phase detector, and divider is referred to the output enhanced in effect by *N* at low offset frequencies from the carrier, and suppressed at high offset frequencies from the carrier. Intuitively, for the low-frequency part of the noise, it can be seen that the loop is fast enough to modulate the VCO so that the output follows the input. The enhancement factor N comes from the fact that the PFD only compares one out of every *N* cycles of the VCO output. But for the high-frequency part of the noise, the loop is not fast enough to follow and suppress the noise from the input.

The noise from the loop filter is represented by θ_{LF}. The transfer function from loop filter output to synthesizer output is

$$\frac{\theta_o}{\theta_{LF}} = \frac{K_{VCO}}{s}\frac{1}{1+G(s)} \qquad \text{(Eq 2-18)}$$

The response from the loop filter to the output depends on the loop filter. For example, the 2nd-order PLL has a loop filter with one zero and two poles, which gives the above transfer function a bandpass characteristics. Notice the noise is multiplied by the VCO gain at the output. Intuitively, for the low frequency part of the noise, it can be seen that the loop is fast enough to follow the reference rather than letting the output be affected by the loop filter noise.

But for the high frequency part of the noise, the loop is not fast enough to correct the noise.

The noise from the VCO is represented by θ_{VCO}. The transfer function from the VCO output to the synthesizer output is

$$\frac{\theta_o}{\theta_{VCO}} = \frac{1}{1 + G(s)} \qquad \text{(Eq 2-19)}$$

This has a high-pass characteristic. Intuitively, the lower-frequency part of the noise from the VCO can be corrected by the relatively fast PLL. But for the higher-frequency part of the noise from VCO, the loop is not fast enough and is essentially an open loop.

In cellular applications, low loop bandwidth is desired in order to minimize the spectral components due to spurious tones in the output spectrum, which result from the frequency comparison process. One consequence of the low synthesizer control bandwidth is that the phase noise of the overall synthesizer is dominated by the phase noise of the VCO. This makes the narrow loop bandwidth approach suitable for the implementation with a discrete high Q component that is needed by the low-phase-noise VCO. The need for external components is not amenable to integration of the synthesizer.

A major challenge is to find ways to realize low-phase-noise synthesizers with low-Q components. One approach is to use a wide synthesizer

control bandwidth to couple a noisy on-chip oscillator to a very-low-phase-noise crystal more closely than a conventional narrow-band PLL so that the output is more dependent on the clean reference. The phase noise contribution from the on-chip oscillator to the output spectrum close to the carrier within the synthesizer control bandwidth is thus suppressed. A wideband IF double conversion receiver architecture is proposed to facilitate the utilization of the wideband synthesizer. In this architecture, the entire signal band at RF is mixed down to the IF with a fixed RF frequency synthesizer. A variable frequency synthesizer at IF is used to tune the desired channel from IF to the baseband. Because the RF LO is a fixed or coarsely tuned frequency, a high-frequency reference is allowed and hence a wide synthesizer control bandwidth is allowed. This approach is amenable to integration of the synthesizer because that relatively low Q on-chip components can be tolerated. We will discuss the wide band PLL in detail in the next chapter.

The narrow loop bandwidth also implies slow frequency switching. A PLL based synthesizer has a frequency resolution of f_{ref}. When very fine frequency resolution is needed, the loop bandwidth is even lower in order to maintain the stability of the loop. Usually, loop bandwidth f_{PLL} should be *10* times less than f_{ref}. This makes the PLL-based synthesizer not suitable in an agile system where fast switching is needed. However, a narrow band PLL based frequency synthesizer is most commonly used in applications where extremely

high performance (very low spurious tones and very low phase noise) are required.

2.3.4 Fractional-N Frequency Synthesizer

The fractional N frequency synthesizer is a modified version of the PLL based synthesizer where the integer frequency divider is replaced by a fractional frequency divider. Fig. 2.8 shows the simplified block diagram of a fractional N synthesizer. The only difference from the PLL based synthesizer is that the frequency divider has a choice between two integers, *N* and *N+1*.

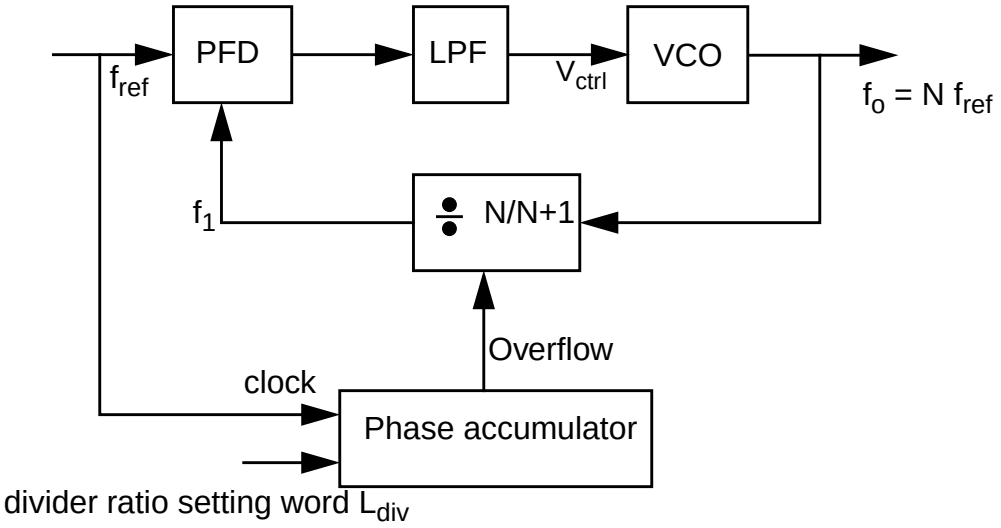


Fig. 2.8: Fractional N frequency synthesizer block diagram

The reference clock also provides the clock signal for the phase accumulator. The phase accumulator accumulates its output with a divider ratio setting the word of length L_{div} at each clock cycle. The dual-mode divider

divides its input by *N* when the phase accumulator is not overflowed. When an overflow signal from the phase accumulator appears, the dual-mode divider divides its input by *N+1*. On average, the divider divides its input by a fractional value between *N* and *N+1*. To calculate the exact divider ratio, we assume the accumulator length to be L_{acc}. For every L_{acc} clock cycles, the accumulator overflows L_{div} times. That means for every L_{acc} clock cycles, the divider divides its input by *N+1* L_{div} times, and divides by *N* for the rest of the times. If N_{avg} is the average dividing ratio, then

$$N_{avg} \cdot L_{acc} = N(L_{acc} - L_{div}) + (N + 1) \cdot L_{acc} \quad \text{(Eq 2-20)}$$

and

$$N_{avg} = N + \frac{L_{div}}{L_{acc}} \quad \text{(Eq 2-21)}$$

The fractional divider ratio makes it possible to have a much smaller frequency step with the same reference frequency comparing to the PLL based synthesizer. In other words, the fractional N synthesizer can have a higher reference frequency and hence higher loop bandwidth without compromising the stability of the loop. But the fractional divider ratio is achieved through an averaging process. The alternating *N, N+1* divide numbers cause the output frequency to vary between $N*f_{ref}$ and $(N+1)*f_{ref}$. This periodically alternating process generates spurious tones at the fractional offset frequency. If the fractional frequency falls inside the loop bandwidth, a very large spurious tone appears. Since the alternating process is deterministic, it is possible to

compensate for the phase error generated by this alternating process. The compensating scheme is known as Automatic Phase Interpolation, or API.

Another form of fractional N synthesizer uses the Sigma-Delta technique to randomize the choice of $N/N+1$ divider ratio. In fact, the phase accumulator can be viewed as the first order Sigma-Delta. When higher order Sigma-Delta is used, noise can be shaped and pushed outside the loop bandwidth and hence suppressed at the output of the synthesizer. Arbitrarily fine frequency resolution can be achieved limited only by the size of the digital adders.

2.3.5 Delay-Locked Loop Frequency Synthesizer

Recently a new approach to a frequency synthesizer using a Delay-Locked Loop (DLL) has been proposed [29]. A DLL is a PLL with the voltage controlled oscillator replaced by a voltage controlled delay line. Fig. 2.9 shows the block diagram of a frequency synthesizer with a DLL core. When the loop is locked, the output of the delay line is a one reference period T_{ref} delayed version of the input of the delay line. For a total of N delay stages, each delay stage has a delay of T_{ref}/N. An edge combiner generates a transition for each delay stage output transition. The output frequency of the edge combiner is N times the reference frequency f_{ref}.

The advantage of the DLL based frequency synthesizer is that the jitter does not accumulate from cycle to cycle as in the ring oscillator (one example of

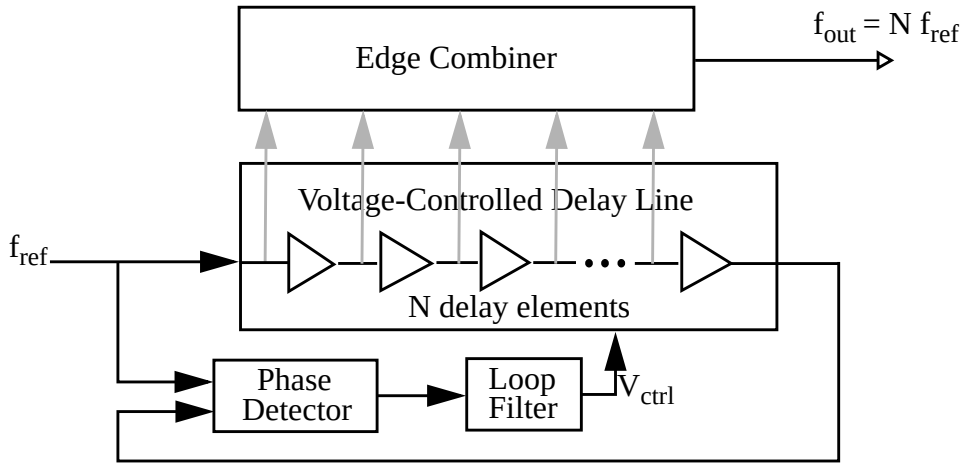


Fig. 2.9: Block diagram of a Delay-Locked Loop frequency synthesizer

voltage controlled oscillators) and thus lower phase noise at close-in frequencies can be achieved. This approach is amenable to the integration of the frequency synthesizer because no high Q tank is needed.

The major disadvantage of the DLL approach is that the output frequency is fixed by the number of delay stages in the delay line. Hence it is not suitable in applications where frequency tuning is required.

Chapter 3

Wideband PLL Frequency Synthesizer

3.1 Introduction

The growing importance of wireless media for voice and data communications is driving a need for higher integration in personal communications transceivers in order to achieve lower cost, smaller form factor, and lower power dissipation. One approach to this problem is to integrate the RF functionality in low-cost CMOS technology together with the baseband transceiver functions. This in turn requires integration of the frequency synthesizer with enough isolation from supply noise to allow the synthesizer to coexist with other on-chip transceiver circuitry and still meet the phase noise performance requirements of the application.

In the previous chapter we discussed several alternative ways to implement a frequency synthesizer. Direct digital frequency synthesis is most amenable to the integration of the frequency synthesizer because no off-chip

component is required. But due to technology limitations, it takes large power consumption to synthesize very high frequencies directly. Usually a second frequency translation is needed to shift the center frequency to the GHz range. Conventional phase-locked-loop based frequency synthesis with narrow loop bandwidth requires off-chip high-Q components to achieve low phase noise and spurious tone levels. In addition, the narrow loop bandwidth makes it unsuitable in an agile system where fast frequency switching is needed. The Fractional-N synthesis greatly relieves the constraint on the loop bandwidth so that faster frequency switching can be achieved. But it generates large spurious tones due to the periodic switching of the divider mode. The automatic phase interpolation technique can be used to reduce the spurious tones but the requisite complexity makes the technique only suitable for very high performance applications such as testing instruments.

In this chapter, we will explore a new architecture that facilitates the integration of the frequency synthesizer and is capable of high performance required in a typical cellular application. This architecture is called wideband PLL. In this architecture, the noise contributed by the resonator can be suppressed at the synthesizer output. Because a wide PLL bandwidth requires a high comparison frequency, this type of synthesizer is most amenable to the synthesis of a few widely spaced frequencies, and is thus most compatible with

block-down-convert receiver architectures such as the wideband IF double conversion architecture [1].

In the next section, we will describe the wideband PLL architecture and the noise shaping in this architecture. Then we will discuss how to optimize the loop bandwidth to achieve the minimum phase noise at a certain offset frequency. Finally, we will discuss the effect of the wideband PLL architecture on the receiver architecture.

3.2 Noise Shaping of the Wideband PLL

As discussed in chapter 2, noise from different blocks of a PLL goes through different transfer functions to the output of the PLL. By selecting a different loop bandwidth, their magnitude at the output can be varied. The three transfer functions from the three noise sources to the output are:

$$H_1(s) = \frac{\theta_o}{\theta_i} = N\frac{G(s)}{1+G(s)} \qquad \text{(Eq 3-1)}$$

$$H_2(s) = \frac{\theta_o}{\theta_{LF}} = \frac{K_{VCO}}{s}\frac{1}{1+G(s)} \qquad \text{(Eq 3-2)}$$

$$H_3(s) = \frac{\theta_o}{\theta_{VCO}} = \frac{1}{1+G(s)} \qquad \text{(Eq 3-3)}$$

where *G(s)* is the open-loop gain

$$G(s) = \frac{K_\phi F(s) K_{VCO}}{Ns} \qquad \text{(Eq 3-4)}$$

and K_ϕ, *F(s)*, K_{VCO}, *N* are the phase-detector gain, the loop-filter transfer function, the VCO gain, and the divider ratio respectively. Note that (Eq 3-1) is a low-pass function and (Eq 3-3) is a high-pass function. The shape of (Eq 3-2) depends on the loop filter. The most commonly used loop filter is the second-order RC low-pass filter, as shown in Figure 3.1.

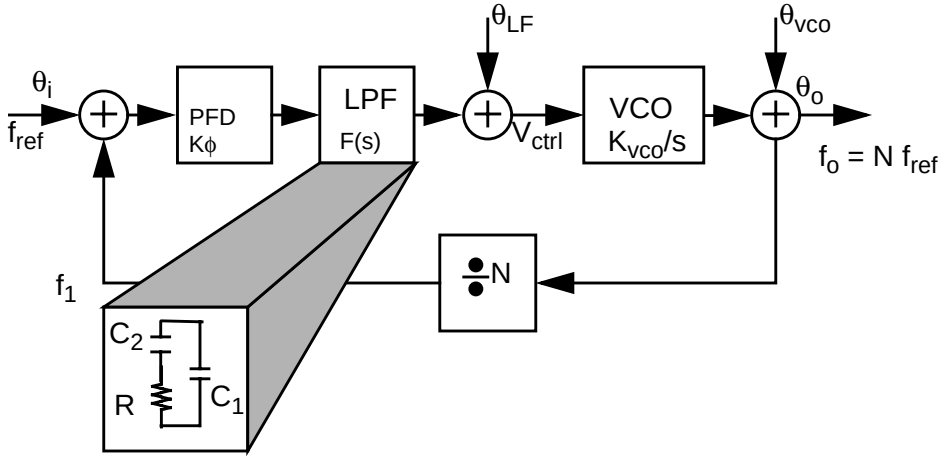


Fig. 3.1: Second Order Phase-Locked Loop linear model

Because in the VCO the input variable is frequency and not phase, the VCO always has a 1/s term in the transfer function. The loop filter introduces another pole at DC in order to have enough suppression on the spurious tones from the frequency comparison process. These two poles at DC introduce a phase shift of 180 degrees per decade. Without compensation, the loop will have a phase shift of 180 degree before the unity-gain bandwidth, which makes the

loop unstable. A zero is introduced before the loop bandwidth to provide enough phase margin. A third pole above the loop bandwidth is introduced to provide more suppression. To quantify this, we can write

$$F(s) = \frac{1}{sC_1} + \frac{1}{\frac{1}{R} + sC_2} = \frac{1 + sR(C_1 + C_2)}{sC_1(1 + sRC_2)} \quad \text{(Eq 3-5)}$$

Let $P_3 = \frac{1}{RC_2}$ and $Z_1 = \frac{1}{R(C_1 + C_2)}$, then

$$F(s) = \frac{1 + s/Z_1}{sC_1(1 + s/P_3)} \quad \text{(Eq 3-6)}$$

and

$$G(s) = K_\phi \cdot \frac{1 + s/Z_1}{sC_1(1 + s/P_3)} \frac{K_{VCO}}{Ns} \quad \text{(Eq 3-7)}$$

The PLL loop bandwidth f_{PLL} is defined as the frequency when the open loop gain equals unity, i.e.,

$$\left|G(j2\pi f_{PLL})\right| = 1 \quad \text{(Eq 3-8)}$$

Figure 3.2 shows the plot of the open-loop gain and the three transfer functions. It is clear from the plot that the noise from input, loop filter, and VCO goes through low-pass, band-pass, and high-pass filtering separately. Section 2.3.3 gives an intuitive analysis of the three transfer functions.

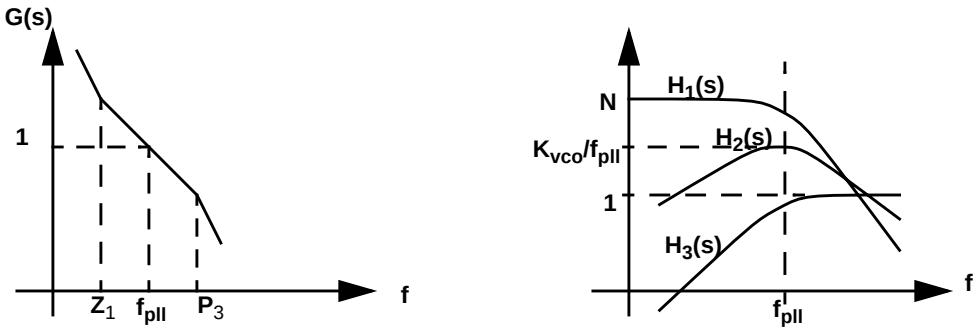


Fig. 3.2: Transfer functions of the 2nd-order PLL a) open-loop gain b) transfer functions

The periodic frequency comparison at the PFD produces spurious tones at the PLL output. The magnitude of the tones is suppressed by the loop according to the transfer function $H_1(s)$. In a conventional PLL used in cellular applications, the loop bandwidth f_{PLL} is chosen to be very small in order to obtain good spectral purity. The transfer function from the VCO to the PLL output approaches unity at frequencies above loop bandwidth, i.e., noise from the VCO goes to the PLL output without much suppression at offset frequencies above the loop bandwidth. Fig. 3.3 (a) shows a plot of a typical VCO noise and its contribution at the narrow-loop-bandwidth PLL output. In order to preserve good spectral purity, an off-chip high-Q resonator is needed in the conventional PLL implementation for cellular applications.

To completely integrate the frequency synthesizer, the off-chip high-Q resonator must be replaced with on-chip components, such as on-chip spiral

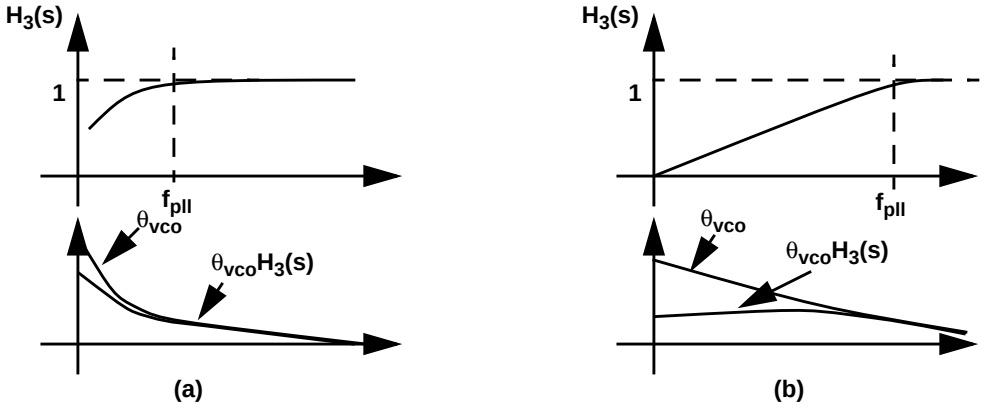


Fig. 3.3: Noise shaping of VCO phase noise in (a) narrow band PLL (b) wideband

inductors and varactors using P+/Nwell junction or MOSCAP. Due to the substrate loss and the relatively high resistivity of aluminum compared to other metals such as copper or gold that are readily available off chip, the Q of the on-chip components are usually an order of magnitude smaller than their off-chip counterparts. As a result, circuits using the low-Q on-chip components tend to have higher noise levels. In order to obtain good spectral purity, we must find an architecture that gives good spectral purity at the frequencies of interest using noisy on-chip components. One possible solution is a PLL with a wide loop bandwidth. In this architecture, the VCO noise is suppressed at frequencies below the wide loop bandwidth so that good spectral purity at frequencies below the loop bandwidth can be obtained. Fig. 3.3(b) shows the plot of typical VCO noise and its contribution at the wideband PLL output. Usually the noise from the reference and loop filter are less than the noise contributed by the noisy on-chip resonator. The wideband PLL architecture can achieve a better signal

spectral purity than the narrow-band PLL architecture if an on-chip resonator is used.

3.3 Loop Bandwidth Optimization

If VCO noise is the only noise source in a PLL, then a very large loop bandwidth can potentially be used to obtain an output signal with very high spectral purity. However the reference, usually a crystal oscillator, has some noise generated by its active circuits. The loop filter also generates noise. This goes through low-pass and band-pass filtering which is different from the VCO noise which goes through the high-pass filtering. This difference suggests an optimal loop bandwidth exists for a specific application. Depending on the level of the different noise sources and the location of the frequency of interest, the optimal loop bandwidth can be different. The goal is to find the optimal loop bandwidth so that the total noise contributed by all noise sources is minimum at the output of the PLL at the frequency of interest.

For example, the second-order PLL discussed in the previous section has three transfer functions that are low-pass, band-pass, and high-pass separately. Assuming the three noise sources have spectrums as plotted in Fig. 3.4, and the frequency of interest is *3MHz*, then the optimal loop bandwidth is chosen to be slightly above *3MHz* so that the total noise at the output of PLL is minimum at *3MHz*.

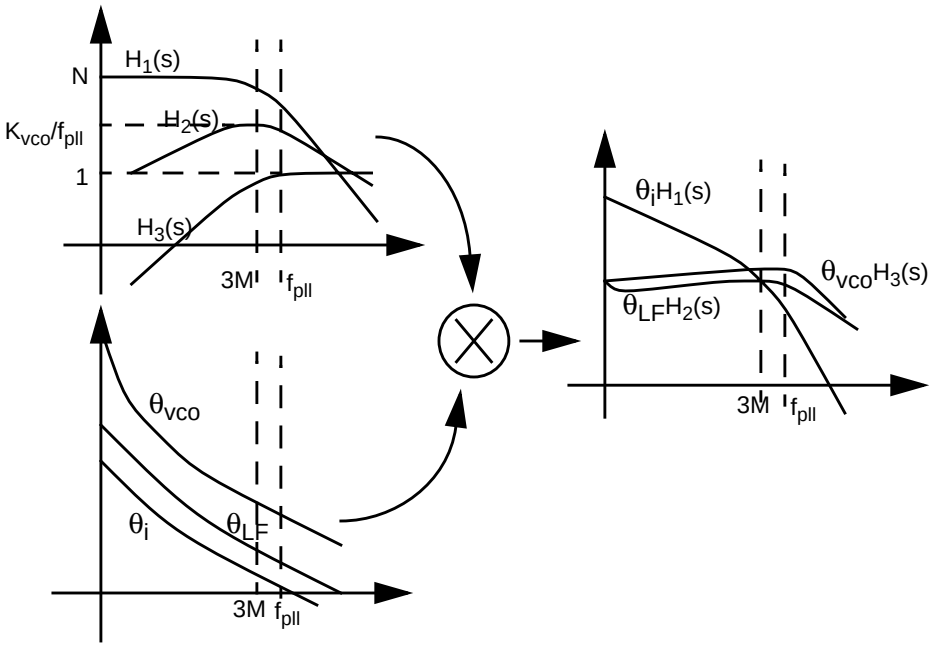


Fig. 3.4: Loop bandwidth optimization example for a second order PLL

To quantify the optimization process, the loop bandwidth f_{PLL} can be written as a function of R, C_1, C_2, N, K_{VCO}, and K_ϕ by combining (Eq 3-7) and (Eq 3-8). We can choose an optimal loop bandwidth by varying those parameters. Enough phase margin should be designed in to guarantee the stability of the loop. The actual optimization requires a knowledge of the noise spectrum from each individual noise source. This noise spectrum sometimes also depends on the choice of those parameters. Thus the optimization is an iterative process.

3.4 Effect of the Wideband PLL on Receiver Architecture

In a conventional superheterodyne receiver architecture, the received signal spectrum is mixed down to baseband in two steps. During the first step, a HF synthesizer signal is mixed with the RF signal, shifting the information signal to a fixed IF frequency. To do this, the RF synthesizer needs to be tunable and the minimum frequency step must be smaller or equal to the channel spacing of the standard. Then a fixed-frequency synthesizer at IF is mixed with the mixed-down version of the received signal and finally shifts it to baseband. Fig. 3.5 shows the spectrum translation in this architecture.

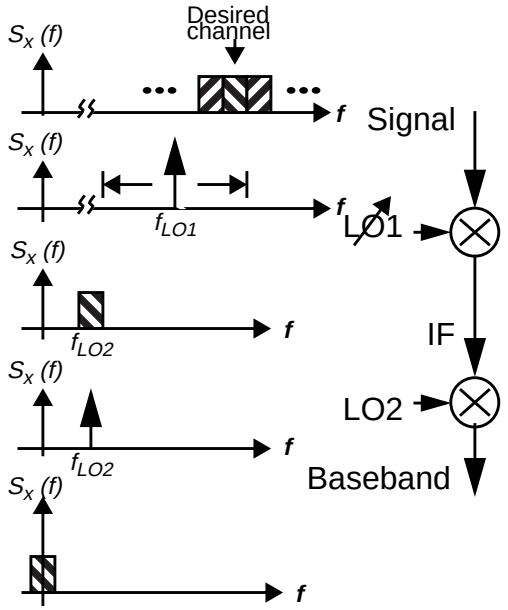


Fig. 3.5: Spectrum translation in Superheterodyne receiver architecture

With the wideband PLL architecture, it is possible to obtain a good spectral purity with a noisy on-chip resonator as the VCO. But in order to have a

stable loop, the reference frequency must be larger than the loop bandwidth if integer frequency division is assumed. This means the frequency step of a wideband PLL is large. In cellular applications, the required frequency step is usually very small. For example, GSM has channel spacing of *200kHz*. The wideband PLL based frequency synthesizer cannot produce frequencies with a step of *200kHz* because the loop bandwidth may be in the MHz range and the reference frequency may be in tens of MHz range.

To solve this problem, a Wideband IF Double Conversion receiver architecture[1] is proposed. In this architecture, the entire signal band at RF is mixed down to the IF with a fixed RF frequency synthesizer, and a variable frequency synthesizer at IF is used to tune the desired channel from IF to the baseband. Fig. 3.6 shows the spectrum translation. The IF synthesizer can tune the channels and still achieve low phase noise because it is generating outputs at lower frequencies.

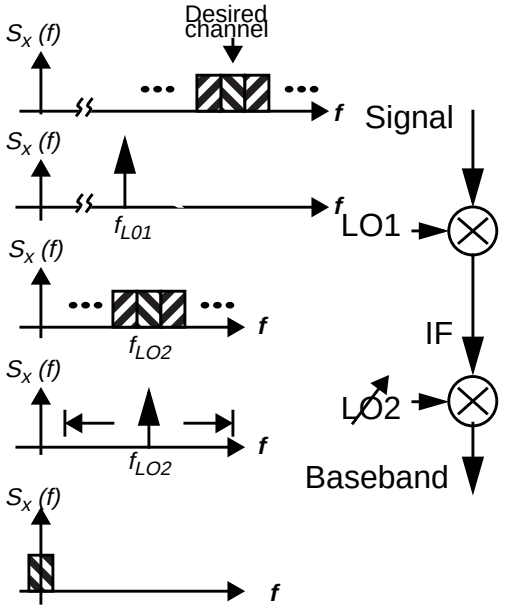


Fig. 3.6: Spectrum translation in the Wideband IF Double Conversion Receiver Architecture

Chapter 4

Design Techniques for Low Noise Synthesizers

4.1 Introduction

In the previous chapter we proposed a wideband PLL architecture to implement a high performance frequency synthesizer with noisy on-chip components. We also discussed the optimization of the loop bandwidth. We pointed out that the optimization of the loop bandwidth depends on the noise spectrum of each individual noise source. In this chapter, we will discuss the low-noise design of each block in a PLL. The most important block is the integrated VCO. Even though the wideband loop can suppress the noise from the VCO, the suppression may not be enough because the integrated VCO is noisy, and the loop bandwidth cannot go arbitrarily high. A low-noise VCO is crucial in achieving a high performance frequency synthesizer. The phase/frequency detector, loop filter, and frequency divider are also important in realizing a high performance frequency synthesizer. The noise from the PFD and frequency

divider is multiplied by the divider ratio at the output of the PLL. When a wideband PLL is used, the divider ratio may be reduced. However, because the loop bandwidth is very wide, noise is not suppressed until the frequency is above the loop bandwidth, which is usually above the frequency of interest. A low-noise latch clocked by the VCO can be placed at the divider output so that the noise from the divider does not contribute at the output of the PLL. The noise from loop filter also has a peak gain depending on the VCO gain and loop bandwidth. Careful design of the loop filter is required to maintain good spectral purity at frequencies around the loop bandwidth. Fig. 4.1 shows the block diagram of a PLL with a low-noise buffer at the output of the frequency divider.

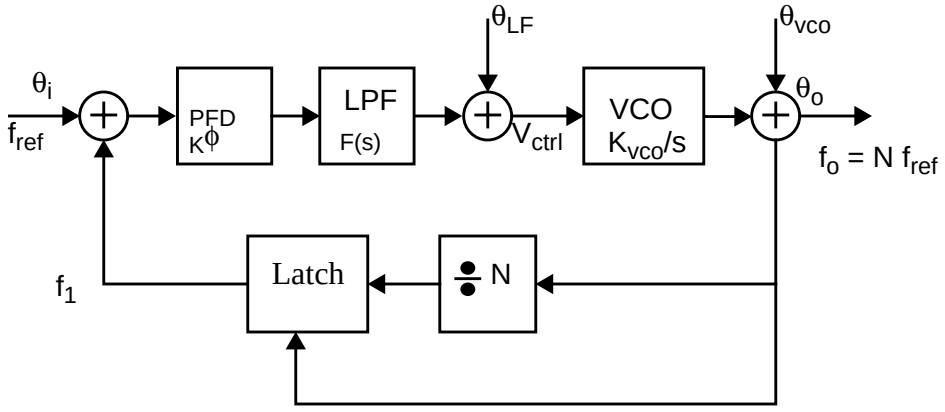


Fig. 4.1: PLL block diagram

4.2 Low-Noise Integrated VCO Design

There are basically two types of VCO, tuned and untuned. Untuned oscillators have inferior spectral purity compared to tuned oscillator for the

same power consumption. The performance of a tuned oscillator depends on the quality factor Q of the tuned element.

A typical example of an untuned oscillator is a ring oscillator. It consists of *n* inverters in a ring as shown in Fig. 4.2. The end of the ring is 180^o

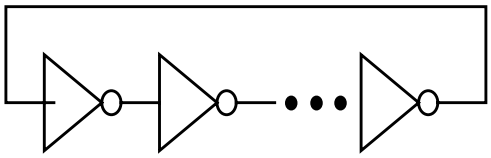


Fig. 4.2: Block diagram of a ring oscillator

out of phase from the beginning of the ring. The logic level propagates through the ring and there are no stable DC points. If each inverter stage has a delay of t_p, then the oscillation period is $2Nt_p$ and the oscillation frequency is $1/2Nt_p$. The most attractive feature of a ring oscillator is that it is fully integrable because of its digital-like building blocks. It also has a wide tuning range. A frequency tuning range of 2:1 is easy to obtain. But for a given level of power consumption, it has worse spectral purity than the tuned oscillator.

A tuned oscillator can be modeled as a gain stage with a bandpass filter in the feedback path as shown in Fig. 4.3. It has lower phase noise because of the bandpass characteristics of the feedback loop. In this context, we interpret the Q factor as the ratio of the carrier frequency to the 3-dB bandwidth of the bandpass filter. The larger the Q is, the better the output spectral purity.

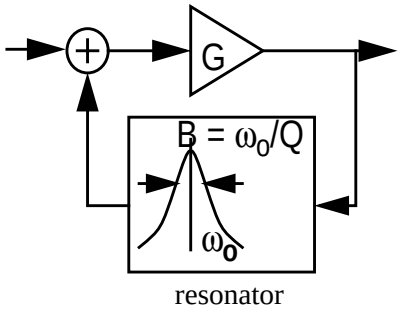


Fig. 4.3: Tuned oscillator model

The tuned element is usually a passive resonator, such as an LC tank, a crystal, SAW and so on. These discrete components usually have a large Q value. For example, a crystal can have a Q of 100,000. But these resonators are not integrable. Recently, on-chip inductors have been the focus of many research efforts. The simplest way to realize such elements is the planar spiral inductor, implemented with the metal layers available in any standard process. A suspended inductor is a spiral inductor with its underlying substrate etched away [2]. Bond wires have also been used as inductors[21]. The Q factor of the spiral inductor has been reported to be from 3 to 20, while bond wires have a Q factor of about 50. An on-chip varactor can be implemented with the p+/nwell junction also available in standard process. The series resistance of the junction can be minimized by minimizing the distance between the junctions, which is limited by the available technology. In 0.35μm CMOS technology, the minimum distance is 0.35μm and the quality factor ranges from 10 to 20 at GHz frequencies.

4.2.1 On-chip Inductors

In a standard process, metal layers can be used to construct on-chip spiral inductors. Fig. 4.4 shows a square and an octagonal spiral inductor.

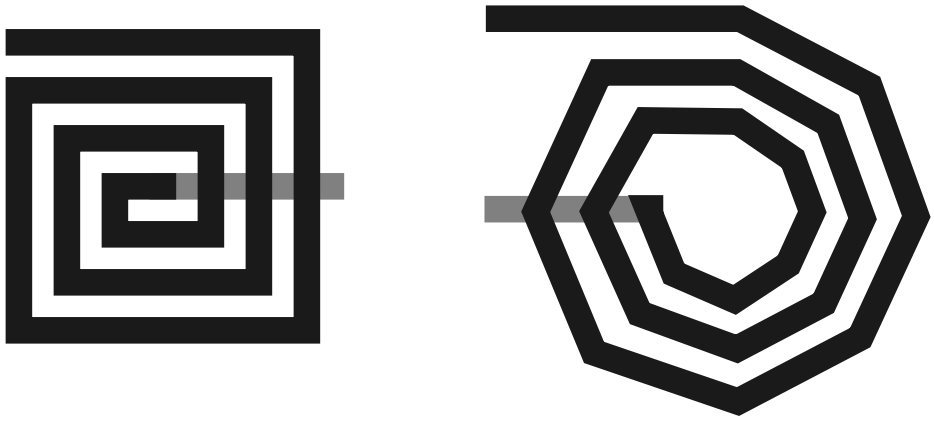


Fig. 4.4: Square and octagonal spiral inductors

Several issues associated with the on-chip inductor need to be mentioned. First, there is series resistance in the metal layers which reduces the quality factor of the inductor. Second, there is capacitive coupling from the metal to substrate which reduces the self-resonant frequency of the inductor. Third, there is resistance in the conducting substrate which also reduces the quality factor of the inductor. These nonidealities are modeled in the lumped π model as shown in Fig. 4.5. L_s models the series inductance and R_s models the series resistance of the metal. C_{p1} and C_{p2} model the capacitive coupling of the metal and the substrate. R_1 and R_2 model the resistive path in the substrate. Many research efforts have been devoted to developing an accurate model for the spiral inductor. Some software can be used to optimize the layout of the

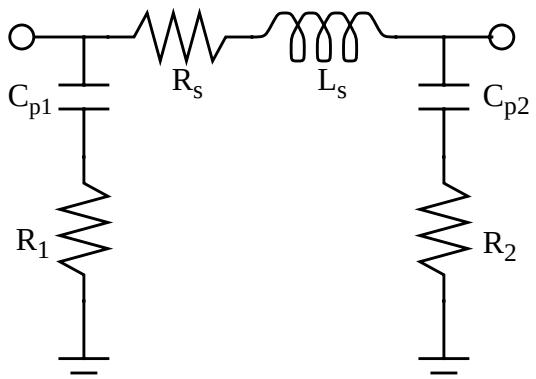


Fig. 4.5: Spiral inductor model

inductor[17][18]. These programs take two effects into account. One, the eddy currents induced by the changing magnetic field from the oscillating current in the inductor which flow in the opposite direction in the substrate. This effect reduces the effective inductance and increase the effective series resistance so that the quality factor is reduced. The other is the skin effect which forces the current in the inductor to flow on the outside of the spiral. This makes the inner turns of the spiral less effective than the outer turns and the effective series resistance higher. The optimal layout of an inductor depends on the inductance value, the particular process (epi or non epi, available metal layers and their thickness, doping level of the substrate, etc.), and the frequency of operation. At RF, quality factors of 3-20 have been reported in recent publications.

Another way to implement an on-chip inductor is a gyrator-based active inductor as shown in Fig. 4.6.

The equivalent inductance is

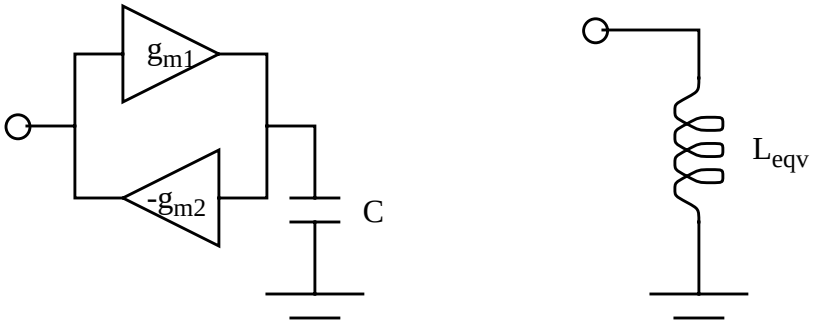


Fig. 4.6: On-chip active inductor

$$L_{eqv} = \frac{C}{g_{m1} \cdot g_{m2}} \qquad \text{(Eq 4-1)}$$

The active inductance has the advantage of easiness for tuning and small area comparing to spiral inductors. However, the active devices generate more noise than the passive implementation. For a high performance VCO, this is not a suitable solution.

4.2.2 On-chip Varactor

In a standard process, the p+/nwell junction can be used as a varactor. Less attention is paid to the optimization of the layout of the junction because the quality factor of such a junction can easily reach 20. The Q of the tank thus is dominated by the Q of inductor rather than the Q of varactor. But when the operating frequency is high, the Q of varactor is reduced because the Q of varactor is inversely proportional to the operating frequency. In the mean time, the Q of the inductor is proportional to the operating frequency. That is, at higher frequencies, the Q of the varactor is more important. Currently, at RF, the

Q of a varactor is about 10-20 for pF capacitance. Fig. 4.7 shows the cross

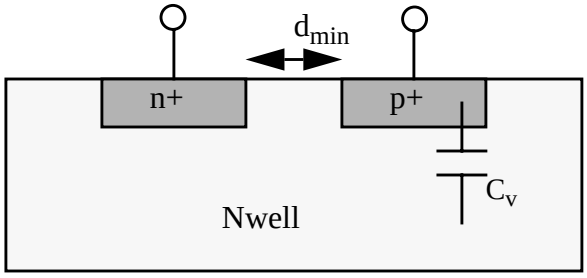


Fig. 4.7: Cross section of the p+/Nwell junction

section of the p+/Nwell junction. The distance between the p+ and n+ region is the current path and it should be kept minimum for minimum series resistance associated with the varactor. Sidewall capacitance has a larger Q and less tuning range because of the higher doping profile. Bottom-plate capacitance has a lower Q and larger tuning range because of the lower doping profile. For maximum Q, the varactor should be laid out in an array of minimum units, e.g., draw the p+ and n+ region in minimum area and place them in the minimum distance allowed by the technology so that for a given area the sidewall capacitance is maximum. But this will reduce the tuning range. For maximum tuning range, one big piece of the p+ region with a ring of n+ around it should be the layout choice. Depending on the application, one can choose a compromise between the two layout styles. Fig. 4.8 shows the array layout of four-unit varactor.

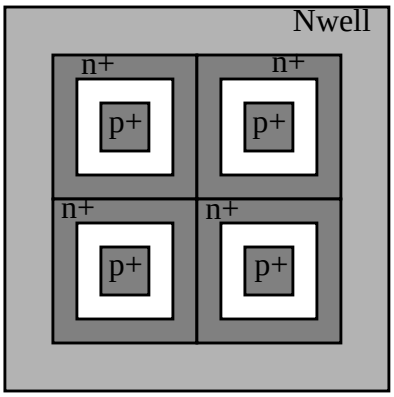


Fig. 4.8: An array of the varactor

Another way to construct a varactor using the standard process is to use the MOS capacitor in depletion and deep depletion regions as shown in Fig. 4.9. To maximize the Q of the varactor, the minimum gate width should be used. This

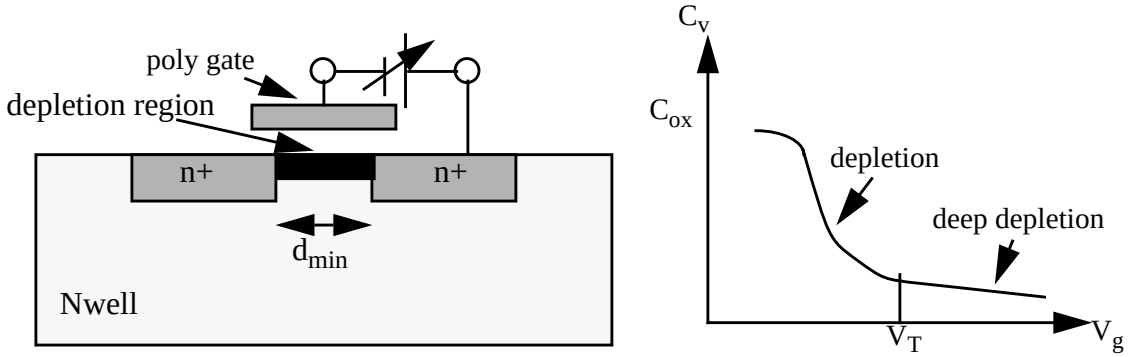


Fig. 4.9: Cross section of a MOS capacitor and its C-V curve

suggests that the Q is scalable with technology.

4.2.3 Fully-Integrated VCO with Tuned Element

There are many ways to connect a gain stage (one transistor or two) and a bandpass filter (tuned element or resonator) together to form an oscillator. The configuration which gives the best spectral purity is not an easy question to answer [7][8][9][23]. However, there is no question that the integrated VCO performance strongly depends on the quality of the on-chip tank, which is dominated by the Q of the spiral inductor. No matter which configuration is chosen, the Q of the inductor needs to be optimized in order to achieve the best performance.

The basic feedback oscillator is the Colpitts oscillator as shown in Fig. 4.10. The capacitive positive feedback provides negative resistance to cancel the

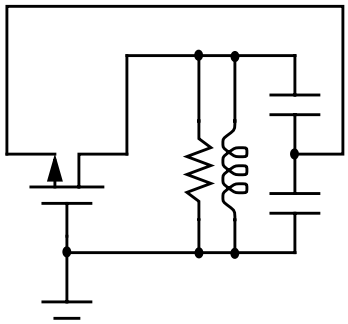


Fig. 4.10: Colpitts oscillator

positive resistance in the tank.

Variations of the Colpitts oscillator are also commonly used. For example, a Clapp oscillator is a Colpitts with an additional tap on the capacitor divider chain which allows the voltage swing across the inductor to exceed the

supply voltage. Larger signal swing improves the spectral purity of the

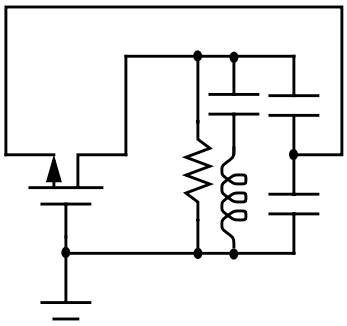


Fig. 4.11: Clapp oscillator

oscillator.

The major difference between oscillator noise and amplifier noise is that the active device in the oscillator is overdriven, resulting in signal mixing. Phase noise analysis of the basic feedback oscillator can start from the analysis of the amplifier noise and then calculate the additional noise by the mixing process. Fig. 4.12 shows the noise model of a basic feedback amplifier with

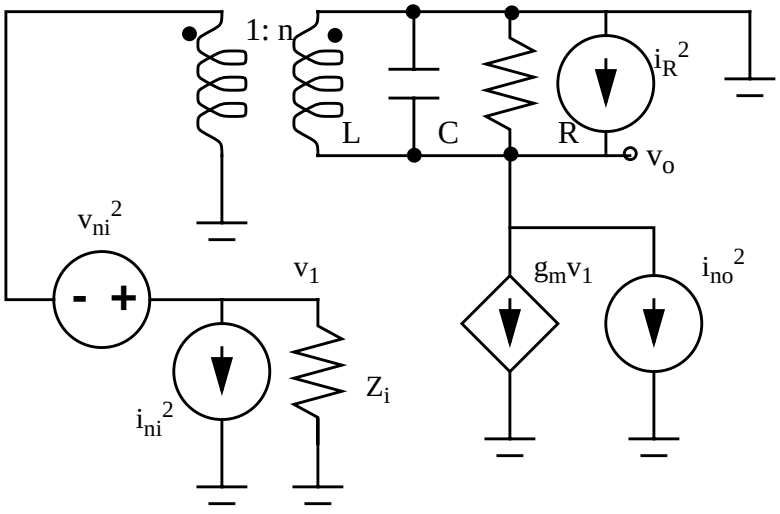


Fig. 4.12: Noise model of a basic positive feedback amplifier with loop gain < 1

positive feedback loop gain less than one.The active device can be either a bipolar transistor or a MOSFET. The equivalent noise model is shown in Fig. 4.13, where

$$i_n^2 = i_{no}^2 + \frac{i_{ni}^2}{n^2} + v_{ni}^2 \cdot \left(g_m - \frac{1}{nZ_i}\right)^2 + \frac{4kTdf}{R} \qquad \text{(Eq 4-2)}$$

and

$$v_o = -\frac{i_n Z_T}{1 - \frac{g_m Z_T}{n}} \qquad \text{(Eq 4-3)}$$

where the total tank impedance Z_T is $\frac{1}{\frac{1}{R_1} + j\omega C + \frac{1}{j\omega L}}$ and R is total shunt resistance $\frac{1}{\frac{1}{R_1} + \frac{1}{n^2 Z_i}}$.

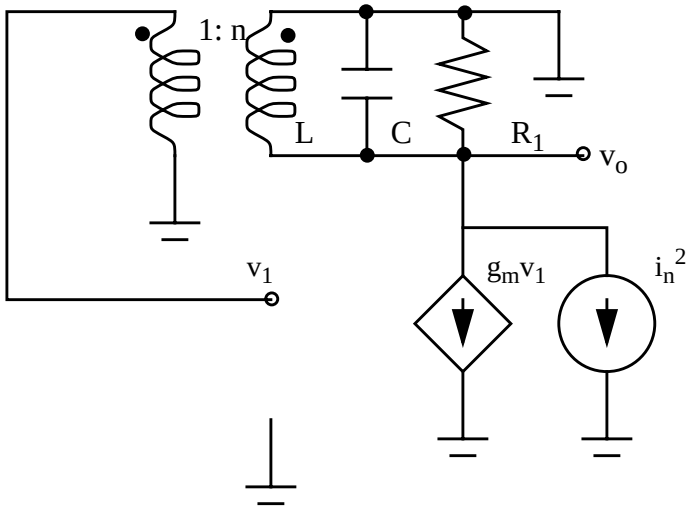


Fig. 4.13: Equivalent noise model

If the loaded tank quality factor Q is

$$Q = \frac{R_1}{\omega_o L} = \omega_o C R_1 \qquad \text{(Eq 4-4)}$$

then the total tank impedance is

$$Z_T = \frac{R_1}{1 + jQ\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)} \approx \frac{R_1}{1 + 2jQ \cdot \frac{\omega - \omega_o}{\omega_o}} \qquad \text{(Eq 4-5)}$$

The noise spectral density is

$$v_o^2 = i_n^2 - \frac{R_1^2}{\left(1 - \frac{g_m R_1}{n}\right)^2 + 4Q^2\left(\frac{\omega - \omega_o}{\omega_o}\right)^2} \qquad \text{(Eq 4-6)}$$

At the offset frequency of interest, $4Q^2\left(\frac{\omega - \omega_o}{\omega_o}\right)^2 \gg \left(1 - \frac{g_m R_1}{n}\right)^2$, so the noise density of the positive-feedback amplifier with loop gain less than one is

$$\left(\frac{v_o}{V_{rms}}\right)^2 = i_n^2 \cdot \frac{1}{V_{rms}^2}\left(\frac{f_o}{2Q}\right)^2 \cdot \frac{R_1^2}{(f - f_o)^2} \qquad \text{(Eq 4-7)}$$

For the oscillator, the initial loop gain is greater than one and the output signal grows exponentially until the active devices begin to limit the large signal loop gain to one. The device noise sources are time varying. (Eq 4-7) is still valid except that i_n^2 must be reevaluated. Low-frequency noise such as 1/f noise will be mixed up to oscillation frequency and appears as sideband phase noise.

Using a cross-coupled pair in Fig. 4.14 as example, we can write

$$i_n^2 = 4kT \times 2 \times \left(\frac{2}{3} \cdot g_m D + \frac{1}{R_1}\right) \qquad \text{(Eq 4-8)}$$

where *D* is the duty cycle of the output waveform. When the low frequency noise such as 1/f noise *K/f* is considered,

$$i_n^2 = 4kT \times 2 \times \left(\frac{2}{3} \cdot g_m D + \frac{1}{R_1} + \frac{1}{\pi} \cdot \frac{K}{f - f_o} \right) \qquad \text{(Eq 4-9)}$$

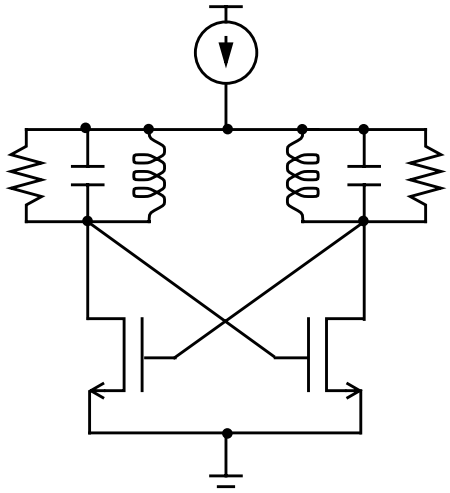


Fig. 4.14: Differential VCO with cross coupled pair

4.2.4 Differentially-Controlled VCO

When the VCO is integrated with other circuits, noise can be coupled through the substrate. The supply line might not be as clean as the supply in the stand-alone VCO. The Power Supply Rejection Ratio (PSRR) becomes very important. If the output is differential, any variation in the control voltage or supply will result in variation in the effective capacitance in the tank. Hence the oscillation frequency will also fluctuate with the control voltage or supply. If,

however, the oscillation frequency is a function of the differential control-voltage rather than the absolute control voltage level, then the PSRR will improve greatly.

Fig. 4.15 shows the possible implementation of such a function. Four

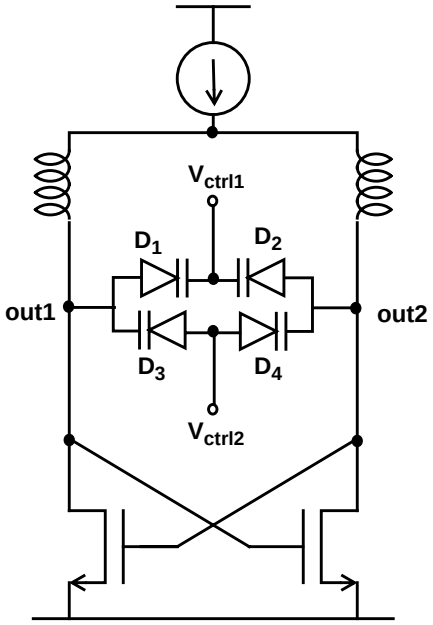


Fig. 4.15: Differentially-controlled VCO with differential output

varactors are connected as shown with differential controls. The change in D1 value is to the first order compensated by the change in D3. D2 is likewise compensated by D4. The frequency of the output to the first order depends only on the differential controls rather than the absolute control voltage. Notice that voltage across D1 is the same as across D3, the voltage across D2 is the same as across D4. In this way, the nonlinear dependence of the junction capacitance on voltage is cancelled to first order when the output is taken differentially.

4.3 Low-Noise Loop Filter and Phase/Frequency Detector

The control voltage of the VCO comes from the output of a loop filter, which contains the information of how much the VCO phase leads or lags that of the reference. The phase detector and loop filter are connected in order to generate the control voltage. Fig. 4.16 shows the functionality of one of the most common ways to generate the control voltage. This configuration is used because of its large frequency comparison range and ideally zero static phase error.

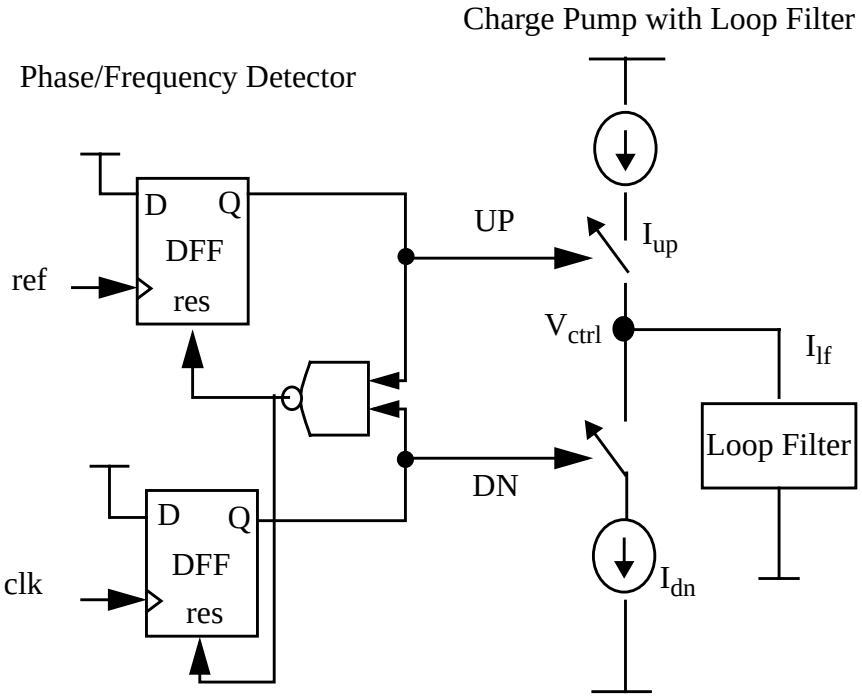


Fig. 4.16: Functional block diagram of the loop filter and PFD

The top DFF generates a high signal when an edge from reference is received. This high signal will turn on the top switch and allow the current to

flow into node V_{ctrl}. The same occurs with the bottom DFF and the bottom switch which allows the current to flow away from node V_{ctrl}. The net current flow into node V_{ctrl} is the net current flow into the loop filter. This will change the voltage level of the V_{ctrl}. When both outputs of the DFF are high, the NAND gate outputs a low signal which resets two DFF outputs to low and both switches are opened. When the PLL is locked, the net charge flowing in or out of the loop filter in one comparison period must be zero. Ideally the static phase error should be zero because any phase difference between reference and VCO output will lead to some net current flow in or out of the loop filter in one comparison period, resulting in a change in control voltage until the phase difference is zero and the PLL is locked.

4.3.1 Loop Filter Design

A simple implementation of the charge pump based on the current steering concept is shown in Fig. 4.17. Differential UP and DN signals from the phase/frequency detector are used to steer the current one way or the other in the differential pair in the charge pump.

There are several nonidealities resulting in a non-zero static phase error and creation of spurious tones. Fig. 4.18 shows the waveforms of the loop filter with non idealities. This assumes that the reference frequency and the VCO frequency are the same but their phases do not match. During the time when both switches are off, i.e., both UP and DN are low, there is some leakage

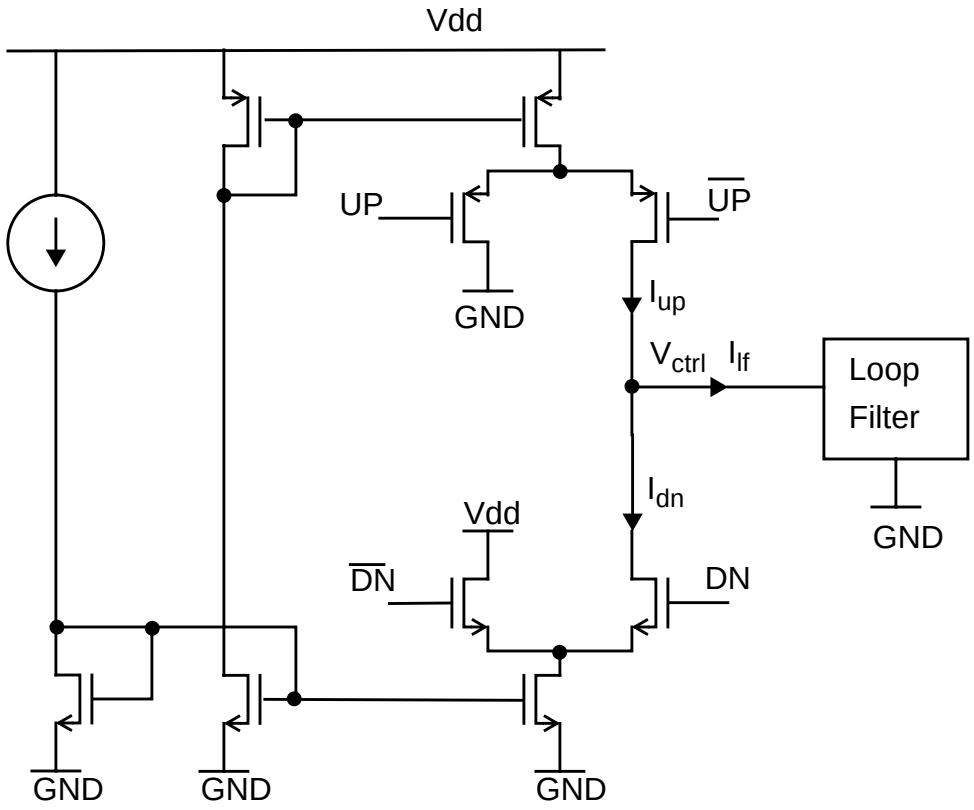


Fig. 4.17: Current steering charge pump

current flowing in and out of the control node. The top leakage current may not equal the bottom leakage current, resulting a net charge flowing in or out of the loop filter in one comparison period. In the PLL locking condition, the net charge must compensated by a different on-time of the two switches. For example, if I_{up} leakage is smaller than I_{dn} leakage, the UP signal must occur slightly earlier than the DN signal to compensate for the net charge flow out of the loop filter. This means the reference edge should come slightly earlier than VCO edge if we assume the PD is ideal. The mismatch between the leakage is one form of static mismatch. Another form of the static mismatch is the DC

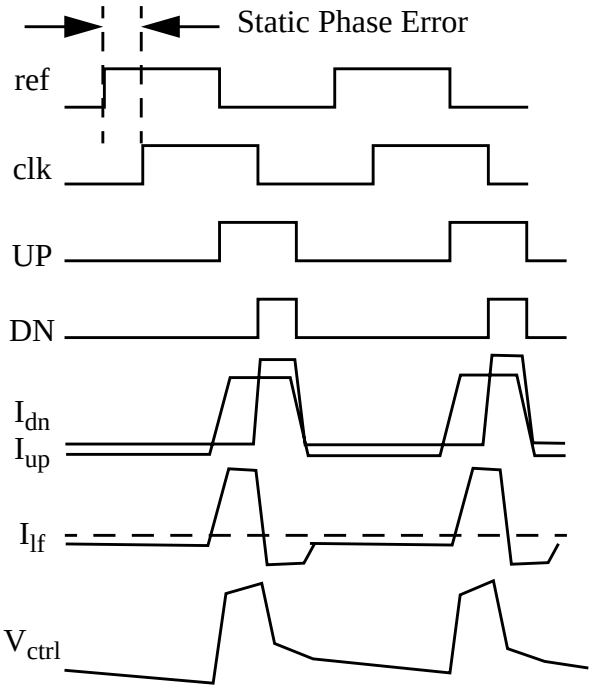


Fig. 4.18: Waveforms of the loop filter with nonidealities

current level difference when both switches are on. The effect is the same as in the case of leakage current mismatch. Dynamic mismatch occurs when the switch has different finite switching on or off time. Both dynamic and static mismatch result in net charge flows in or out of the loop filter periodically, at the rate of the comparison frequency. As a result, the control voltage has a ripple at the comparison frequency, which modulates the VCO frequency and generates spurious tones at multiples of the comparison frequency away from the carrier.

Cascoded current sources can be used to reduce the DC current level mismatch between the top and bottom current sources. Full swing UP and DN signals can be used to hard switch off the switches in order to minimize the

leakage current, hence minimizing the mismatch of the leakage current. Minimum length devices can be used as switches to reduce the switching on or off time, hence reducing the dynamic mismatch. But the static or dynamic mismatches cannot be completely eliminated. The fully differential approach minimizes the effect such that the ripple of one control voltage does not matter but the difference between two control voltages is the control voltage of VCO. As we mentioned before, the VCO is designed to have differential control and differential output. This makes it possible to utilize a fully-differential charge pump to minimize the effect of static and dynamic mismatch. Fig. 4.19 shows the circuit diagram of the fully differential charge pump with cascoded current sources and switches with a full-swing differential switching signal.

The waveform of this differential charge pump with nonidealities is shown in Fig. 4.20. The I_{up} and I_{dn} on one side of the differential charge pump and loop filter still have static and dynamic mismatch and there is still ripple on each control voltage. But when the difference of the control voltages is taken, the ripple is cancelled. Mismatch between the two top current sources and mismatch between the two bottom current sources create nonideal cancellation of the two sources of control voltage ripple, but the ripple is much smaller than in the single-ended case.

Noise on voltage V_{ctrl1} and V_{ctrl2} modulates the oscillation frequency of the VCO. Assuming the input-referred noise of the opamp is much smaller than

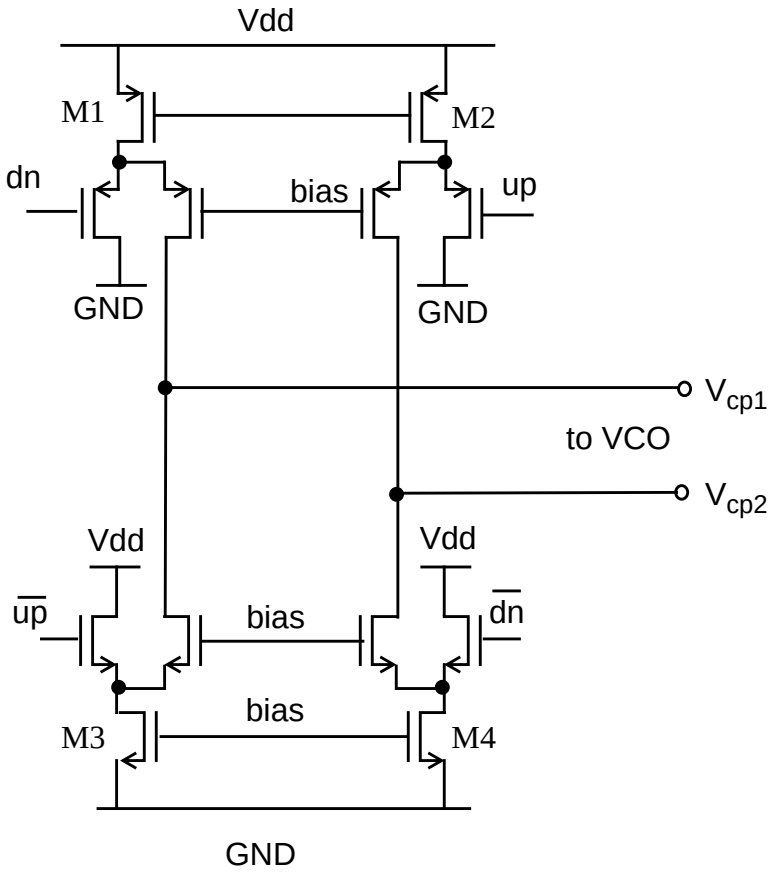


Fig. 4.19: Fully-differential charge pump

the charge-pump output noise, and the duty cycle of the UP or DN signal when the loop is locked is *D*, we can write the total noise as

$$v_o^2 = (i_{n1}^2 + i_{n2}^2 + i_{n3}^2 + i_{n4}^2)Z_f^2 D \qquad \text{(Eq 4-10)}$$

In order to reduce the noise from the cascoded current source, vd_{sat} of the devices M1, M2, M3, M4 should be large. Large vd_{sat} reduces the valid range of the control voltages V_{cp1} and V_{cp2}, hence reducing the VCO tuning range. Mismatch between the two top current sources and mismatch between the two bottom current sources is increased when a larger differential control voltage is

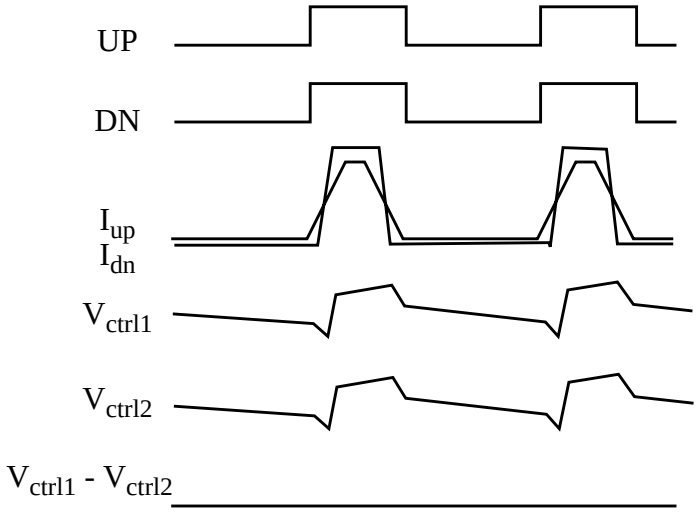


Fig. 4.20: Waveforms of differential charge pump with nonidealities

required to drive the VCO. These mismatches cannot be cancelled through the fully differential approach.

An active loop filter can be used so that the steady-state charge pump differential output is always zero, even when a large control voltage is required to drive the VCO. A CMFB can set the voltage of V_{cp1} and V_{cp2} to be the same as the bias circuit so that current I_{up} and I_{dn} match very well. The tuning range of the VCO is only limited by the output stage of the active loop filter (opamp output stage) where small vd_{sat} can be used and matching between the top and bottom current sources is not an issue. The only drawback of the fully differential approach is the complexity of the design. Common-mode feedback at the output of the opamp and input of the opamp must be designed carefully so that it does not affect the settling and stability of the full PLL. Fig. 4.21 shows the circuit diagram of a fully-differential charge pump with an active loop filter.

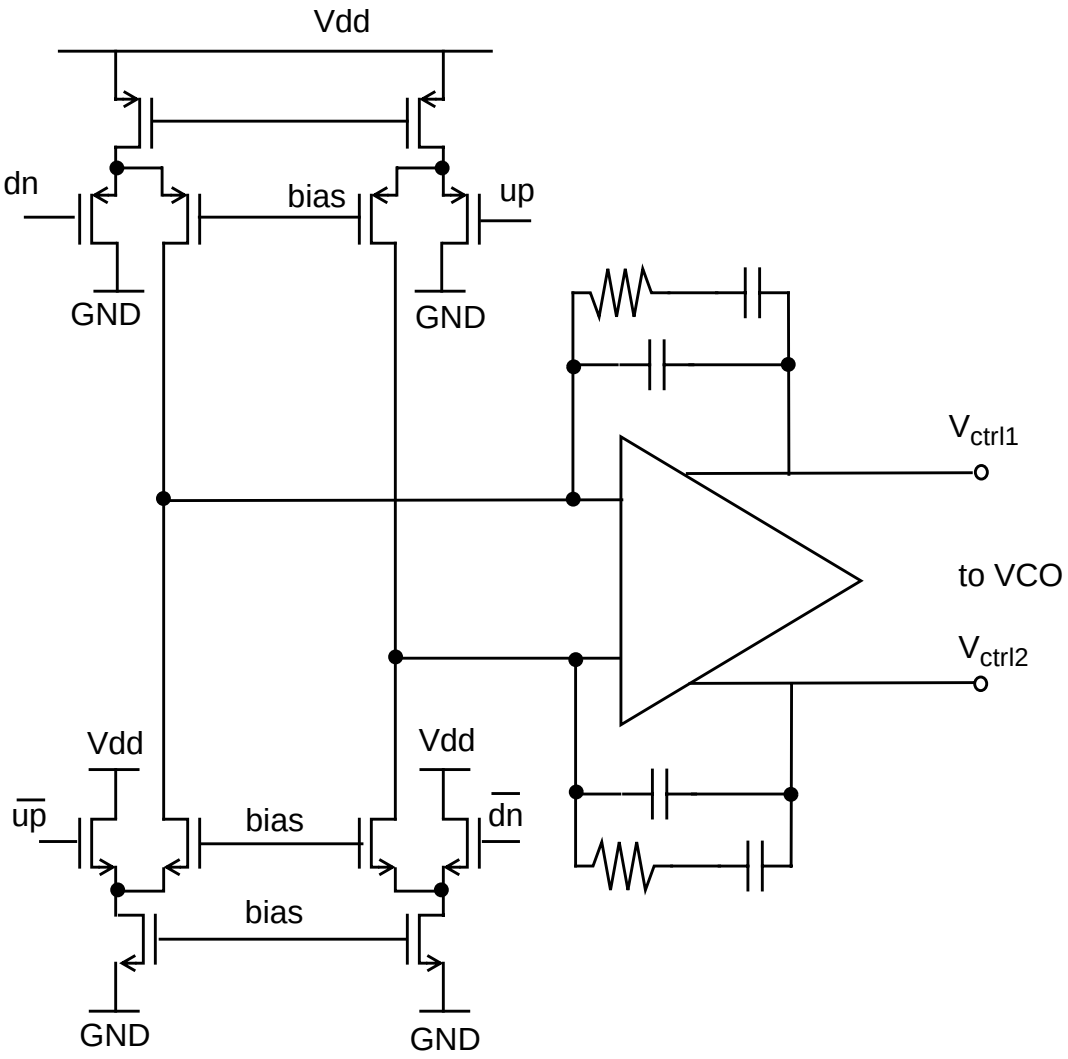


Fig. 4.21: Differential charge pump with active loop filter

4.3.2 Phase/Frequency Detector Design

The most common implementation of the Phase/Frequency Detector is shown in Fig. 4.22. As we mentioned before, the UP and DN signal are full swing signals in order to minimize the leakage current in the switches in the

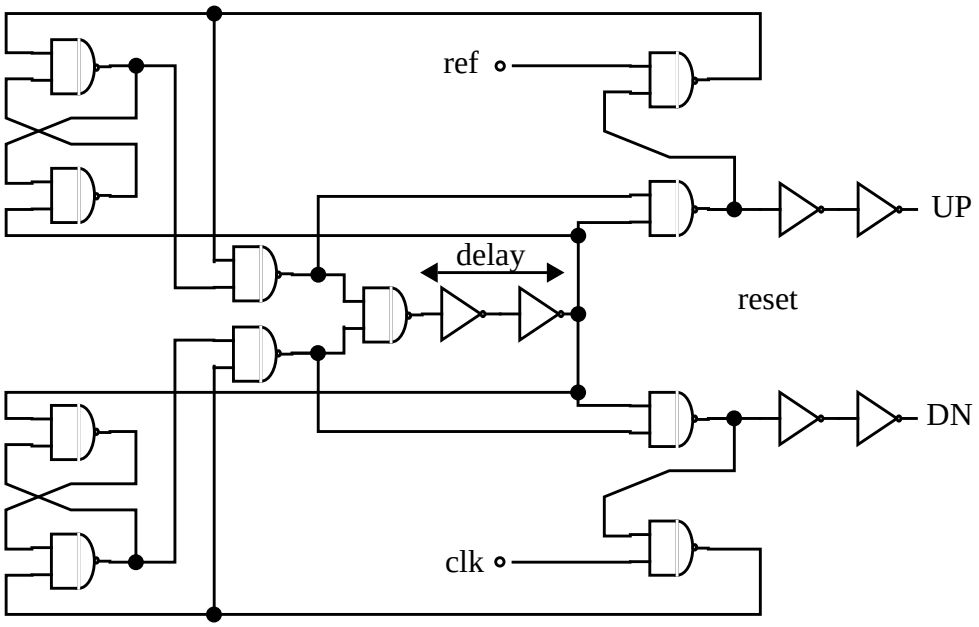


Fig. 4.22: Phase/frequency detector circuit diagram

charge pump. Because the charge pump also needs differential UP and DN signals for the four switches, the PFD should also uses a differential topology. DCVSL seems to be the best choice to implement the logic in the PFD. Fig. 4.23 shows a two input AND/NAND DCVSL gate.

In order to minimize the noise generated by the gate, the ratio of PMOS size to NMOS size should be designed properly so that the output rising or falling edge is sufficiently fast. Assuming the rising slope is *k(V/sec)* and the waveform period is *T*, any voltage variation or noise v_n at the zero crossing is translated to phase variation or noise ϕ_n as

$$\phi_n = \frac{2\pi}{T} \cdot \frac{v_n}{k} \qquad \text{(Eq 4-11)}$$

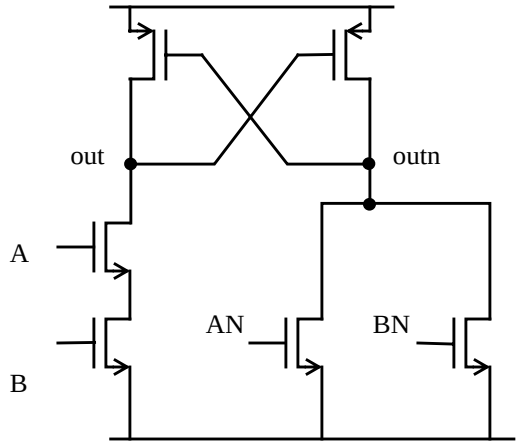


Fig. 4.23: Two input AND/NAND DCVSL gate

The larger k is, the less sensitive ϕ_n is to v_n. Minimum length device should be used for largest k.

4.4 Low-Noise Latch

The function of the low-noise latch at the output of the frequency divider is to bypass the noise in the divider chain. It is clocked by the VCO which is at RF and takes the divider output as its input. The divider output should be ready before the VCO clock arrives in order to bypass the noise in the divider.

Fig. 4.24 shows the differential design of the buffer. It functions as a DFF. The difficulty of the design is that the clock signal is at RF and it is close to a sinusoidal waveform rather than a square wave. The differential pair M1/M2

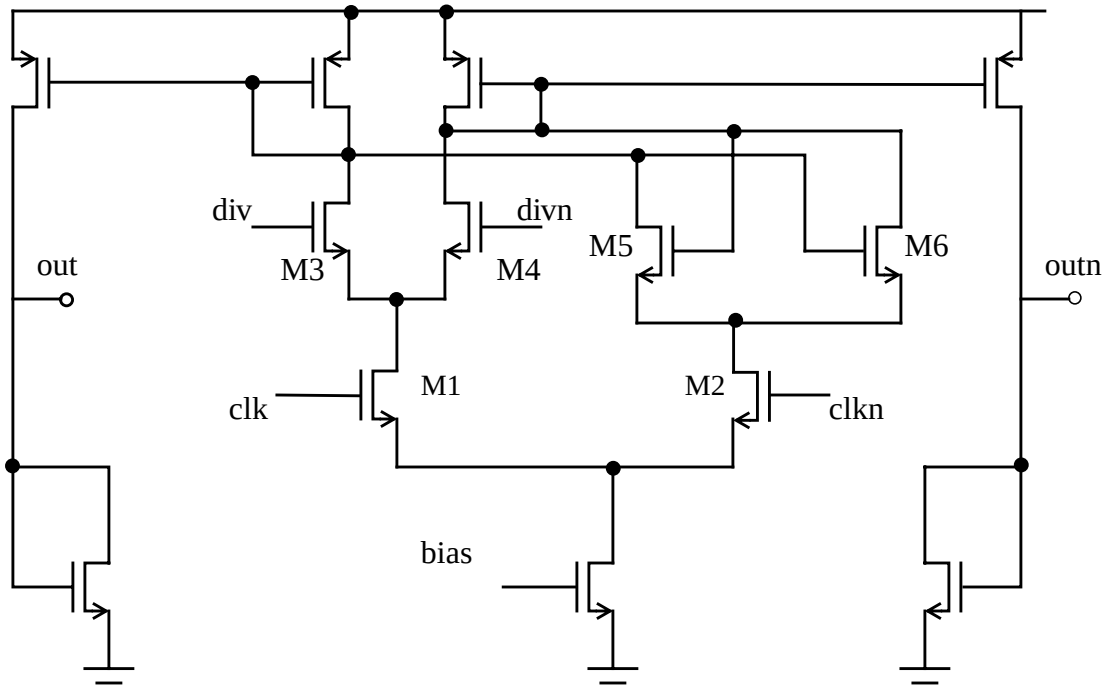


Fig. 4.24: Low-noise latch clocked by VCO

should have a large aspect ratio so that the switching threshold of the differential pair is low enough to ensure complete current steering. Otherwise M3, M4, M5, M6 will be on at the same time and all four transistors contribute noise at the output nodes. Small loading should be ensured at the output nodes so that the transition can be fast enough and the timing error or phase noise according to (Eq 4-11) is small.

4.5 Frequency Divider

A programmable frequency divider usually consists of a prescaler and two counters in a pulse swallow architecture as shown in Fig. 4.25. The

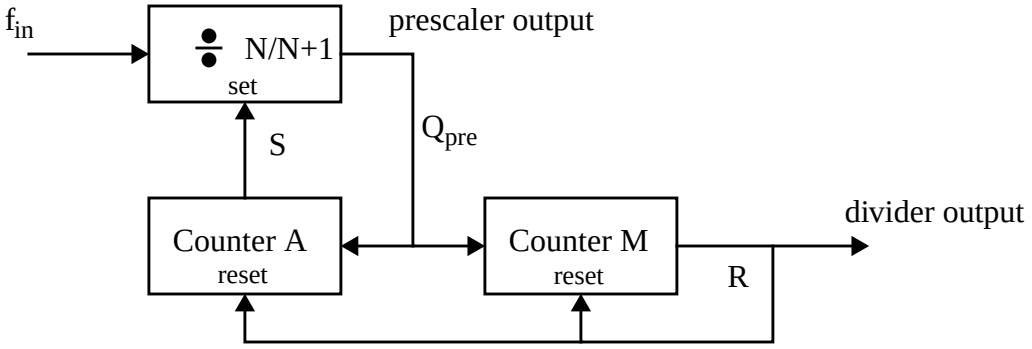


Fig. 4.25: Block diagram of a programmable divider

prescaler divides the input frequency by either N or $N+1$ depending on the setting signal S. The output of the prescaler serves as the input of counter A and counter M. At the beginning of the state, the prescaler is in the divide by $N+1$ mode. When counter A reaches zero count, the setting signal S sets the prescaler in the divide by N mode. This mode continues until counter M reaches zero count. For a complete cycle, it takes $A(N+1)+(M-A)N$ edges of the input to generate one edge at the divider output. This means that the divider divides the input by $MN+A$. Counter M is required to be larger than counter A in order to achieve continuous dividing ratio from $N(N-1)$ to $M(N+1)$.

The prescaler sees the full bandwidth of the input signal and is the most difficult block to design in the programmable divider. Counter A and counter M operate at a frequency N times lower than the prescaler. When a low-noise latch clocked by the VCO is inserted at the output of the divider to bypass the noise

generated by the divider itself, significant power can be saved in the two counters.

Although the low-noise latch at the output of the frequency divider relieves the constraint on the noise performance of the divider, the total current flows in or out of the divider should be kept relatively constant to minimize the noise coupling from substrate injection. Differential logic keeps the current at a constant level much better than the single-ended case.

Chapter 5

Experimental Prototype

5.1 Design Specifications

There are numerous wireless standards located at various frequency bands. Fig. 5.1 shows some of the most commonly used around the world. GSM, Enhanced GSM, DCS1800, and PCS1900 are for mobile applications. Their channel spacing is *200kHz* wide. DECT is for indoor cordless application and has 10 channels with a channel spacing of *1.728MHz*. The single GPS channel for the Coarse Acquisition (C/A) code is *2MHz* wide. The role of a frequency synthesizer is to provide a reference frequency for frequency translation in a transceiver. This means that the frequency synthesizer needs to generate a set of frequencies at the frequency bands of the standard with a frequency step equal to the channel spacing. DCS1800 is selected as the target standard to implement for a demonstration prototype.

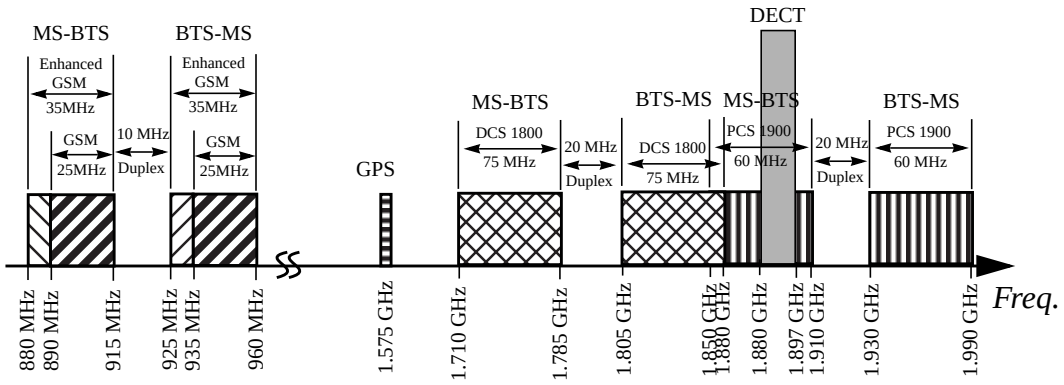


Fig. 5.1: Band allocation of various standards

5.1.1 Blocking Characteristics

If a receiver is used in close proximity to a base station but is receiving signals from a different base station which is far away, or when another user is transmitting signals close nearby, the desired signal will be much smaller than the undesired signal in the neighboring channel. This situation can result in overload of the receiver and impaired reception, a process called blocking. The blocking performance of a receiver is tested by applying a GMSK *BT=0.3* modulated desired signal and a single unmodulated tone simultaneously at the input of the receiver. The desired signal is set *3dB* above the required receiver reference sensitivity. The undesired tone is set at discrete increments of the channel spacing (*200kHz* for DCS1800) from the desired signal with a magnitude as shown in the specific blocking requirements. Note, the following blocking requirements are given for the mobile station(MS) only, a separate set of specifications exist for the base station.

Fig. 5.2 shows the blocking characteristics of DCS1800. The desired inband signal is set to be *-97dBm*. The two power levels for the out-of-band blockers are *-12dBm* and *0dBm*. The three power levels for the inband blockers are *-43dBm*, *-33dBm*, and *-26dBm*.

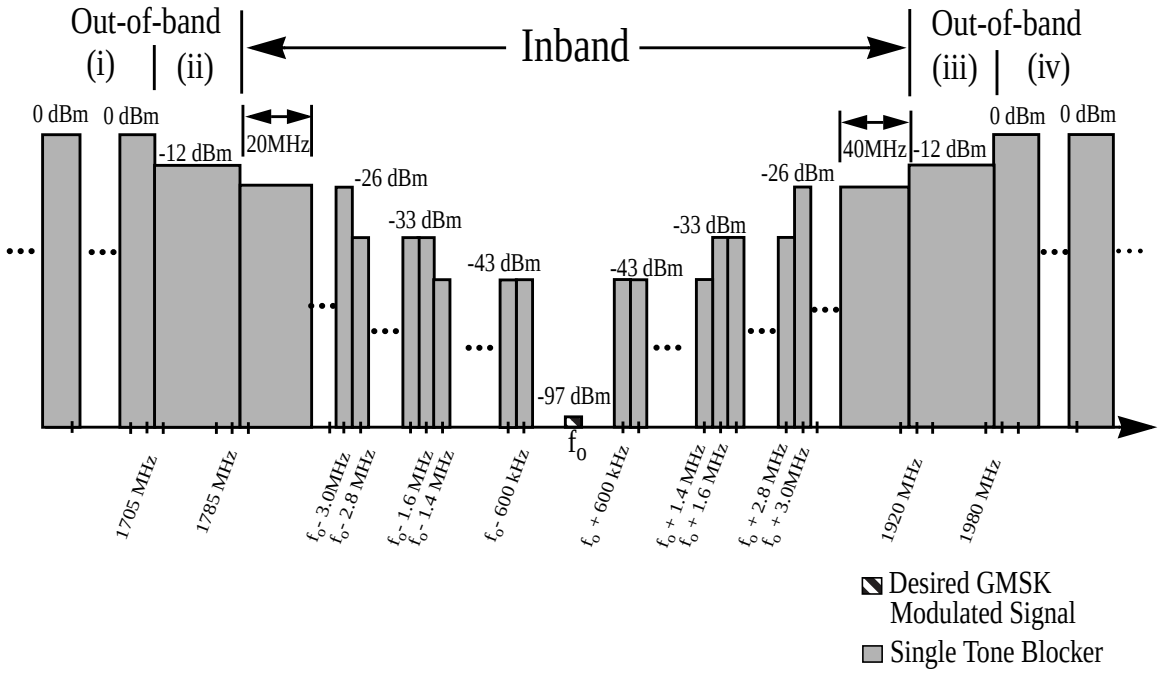


Fig. 5.2: Blocking characteristics of DCS1800

5.1.2 Spurious Response Characteristics

Spurious response frequencies are those frequencies at which the blocking requirement of Sec 5.1.1 is relaxed. For example, DCS1800 allows the blocking requirement to be relaxed to *-49dBm* at the frequency where the blocker is applied. As many as *12* inband frequencies may be selected with a maximum of three adjacent spurious response exceptions. As many as *24* out-of-band

spurious response frequencies are allowed with a maximum of three adjacent frequencies assigned to be spurious response exceptions. The frequencies at which the blocking requirement can be relaxed are selected by the user. Each channel is allowed a different set of spurious response frequencies.

5.1.3 Phase Noise Specification

Energy from the frequency synthesizer at frequencies other than the desired frequency is contributed by the phase noise and spurious tones of the frequency synthesizer. When the synthesizer signal is mixed with the received signal, the undesired signal will mix with the phase noise or the spurious tones of the synthesizer output creating interference within the desired signal band. This interference degrades the C/I (carrier-to-interference ratio) at the receiver output and thus degrades the selectivity of the receiver. Fig. 5.3 shows the reciprocal mixing of phase noise and undesired signals. Blocking requirements set the phase noise and spurious tone specifications for a frequency synthesizer for a particular application. The synthesizer must be designed such that under the worst case blocking condition, the reciprocal mixing of the blocker with the phase noise of the oscillator will produce an interference component far below the desired signal level, so that the receiver output C/I ratio is above the minimum value set by the standard.

Assuming that the receiver channel is noiseless and the only interference produced within the signal band moving through the receiver chain

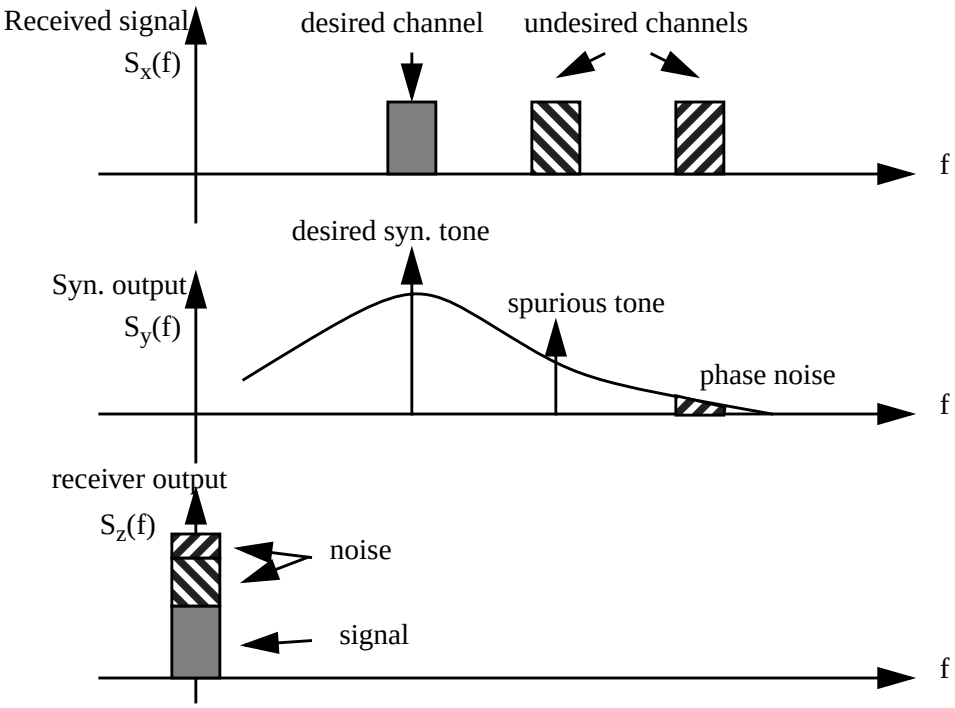


Fig. 5.3: Effect of phase noise and spurious tones in a receiver

is due to the phase noise reciprocal mixing with out-of-signal band blockers, in order to maintain the C/I ratio at the mixer output, the phase noise $\Phi(f)$ should satisfy the following equation:

$$\Phi(f)(\mathrm{dBc/Hz}) \le P_{signal}(\mathrm{dBm}) - P_{blocker}(\mathrm{dBm}) - C/I(\mathrm{dB}) - 10\log(BW_{noise}) \quad \text{(Eq 5-1)}$$

where P_{signal} is the desired signal power, $P_{blocker}$ is the blocker signal power, and BW_{noise} is the noise bandwidth. For example, from Fig. 5.2 we know that the blocker at *3MHz* can be as high as *-26dBm* while the desired signal can be as low as *-97dBm*. The noise bandwidth or the channel spacing of DCS1800 is *200kHz*. Assuming a *9dB* C/I ratio is required, the phase noise specification at *3MHz* offset frequency is then

$$\Phi(3\text{MHz}) \leq -97-(-26)-9-10\log(200000) = -133\text{dBc/Hz} \quad \text{(Eq 5-2)}$$

However, white noise added to the desired signal band and gain compression in the receiver signal path further degrades the overall C/I ratio at the output [2]. A lower phase noise specification is required than the number calculated in (Eq 5-2) in order to achieve the same C/I ratio or BER. Fig. 5.4 shows the phase noise mask for DCS1800.

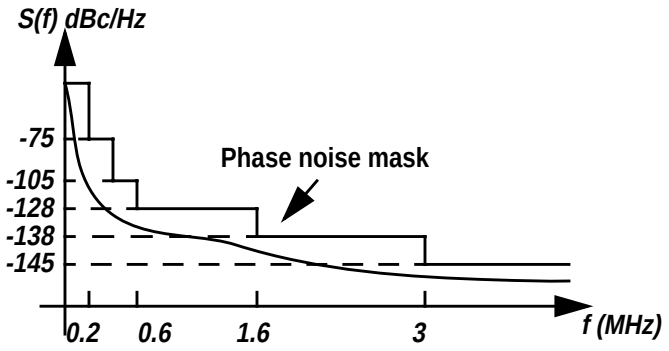


Fig. 5.4: Phase noise specifications for DCS1800

The specification for the spurious tone can be simply calculated as the difference between the desired signal power and the blocker power. For DCS1800, it is

$$-97\text{dBm}-(-49\text{dBm}) = -48\text{dBc} \quad \text{(Eq 5-3)}$$

5.2 Prototype Design

A prototype based on the wideband PLL architecture was fabricated in a 0.35μm 2-poly 5-metal CMOS process, intended as the RF synthesizer or LO1 in

a 1.8GHz DCS1800/DECT transceiver using a wideband IF double-conversion architecture.

For many applications transceiver integration levels will be such that the receiver path, transmit path, the complete synthesizer, and perhaps the RF power amplifier will coexist on a single integrated circuit, along with a significant amount of A/D conversion and baseband processing. This in turn requires the synthesizer maintain its phase noise and spurious tone performance in the presence of components which deliver significant current and voltage perturbations to both the substrate GND and supply. Fully differential implementation of the complete PLL path is important for this reason. This prototype is implemented as a wideband PLL based frequency synthesizer that is fully differential and fully integrated.

Fig. 5.5 shows the block diagram of the prototype. Each block has differential input and differential output. The VCO is differentially controlled and the low-noise buffer is differentially clocked.

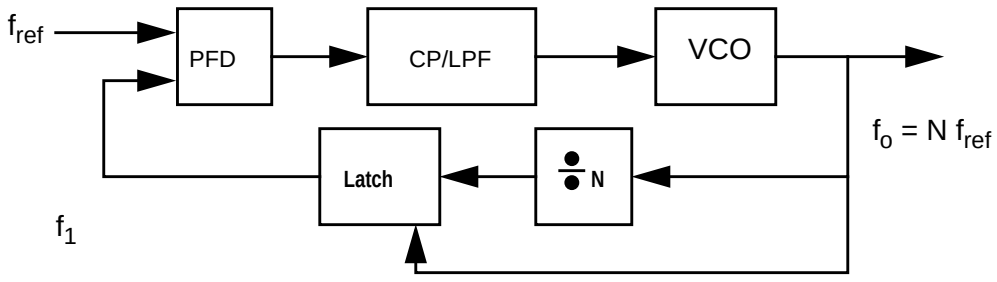


Fig. 5.5: PLL block diagram

5.2.1 Frequency Plan

A good frequency plan is crucial to achieving all the specifications of different standards, with a minimal amount of hardware and power consumption. The frequency plan determines how the frequency translation of the carrier is performed in both the receive and transmit paths. Therefore, the frequency plan determines the amount of hardware and power it takes to generate the reference frequency with the frequency synthesizer and has a significant impact on the overall synthesizer performance, namely, phase noise, spurious tones and the required power consumption.

The first design choice is the reference frequency. It is desirable to develop a frequency plan where only one external crystal reference oscillator is used. The phase noise performance of the external crystal oscillator also influences the choice of the reference frequency. Currently, the available crystal oscillators on the market below 200MHz typically have a phase noise level below -145dBc/Hz at 50kHz offset frequency. With a low phase noise option added to the crystal oscillator a phase noise performance of -160dBc/Hz at 50kHz offset frequency may be obtained.

When DECT and DCS1800 are the target applications, a reference frequency that is a multiple of *1.728MHz* (channel spacing of DECT) and a multiple of *0.2MHz* (channel spacing of DCS1800) is needed. The minimum value of such frequencies is *43.2MHz*. If a *43.2MHz* reference is used, the

frequency step of the RF synthesizer or LO1 is *43.2MHz* and the minimum IF range that LO2 must be able to generate is *43.2MHz*. To improve the image-rejection from the front-end filter, the IF should be at least *200MHz* with a 1.9GHz carrier. This implies that the divider ratio *N* to implement the LO1 is about *36 (1.6GHz/43.2MHz)*. The phase noise of the crystal oscillator and phase detector and the divider is amplified by *N*, e.g., *31dB*. With a *31dB* noise enhancement from the divider it is virtually impossible to meet the phase noise requirement for cellular applications using a wideband PLL with an integrated VCO. Therefore, the crystal reference frequency is chosen as *86.4MHz*. With an *86.4MHz* crystal reference frequency, the divider ratio *N* is significantly reduced from *36* to *16* with a *400MHz* IF. If the divider ratio is reduced to *16*, the noise amplification of the crystal oscillator, phase detector, and dividers are reduced to *24dB*, making it possible to implement a wide band PLL for the first local oscillator (LO1) using an external low phase noise crystal oscillator.

The narrow-band PLL approach is used for the IF synthesizer or LO2 to suppress the spurious tones generated by the loop. Therefore, with a narrow loop bandwidth, the phase noise from the crystal oscillator, the phase detector and the divider will also be suppressed by the loop filter at the output of the LO2 PLL. The overall phase noise profile of LO2 outside the loop bandwidth is dominated by the VCO. However, the phase noise requirements of the VCO for LO2 is relaxed by *12dB* because the VCO output is divided by *4* to obtain the IF

frequency. The required tuning range of LO2 can be approximated as the crystal reference frequency divided by the IF frequency. For an *80MHz* crystal reference frequency and a *400MHz* IF frequency, the tuning range is about *20%*.

The frequency plan implemented by the PLL is shown in Fig. 5.6. Only one external crystal reference is needed. The overlap of the IF range for both

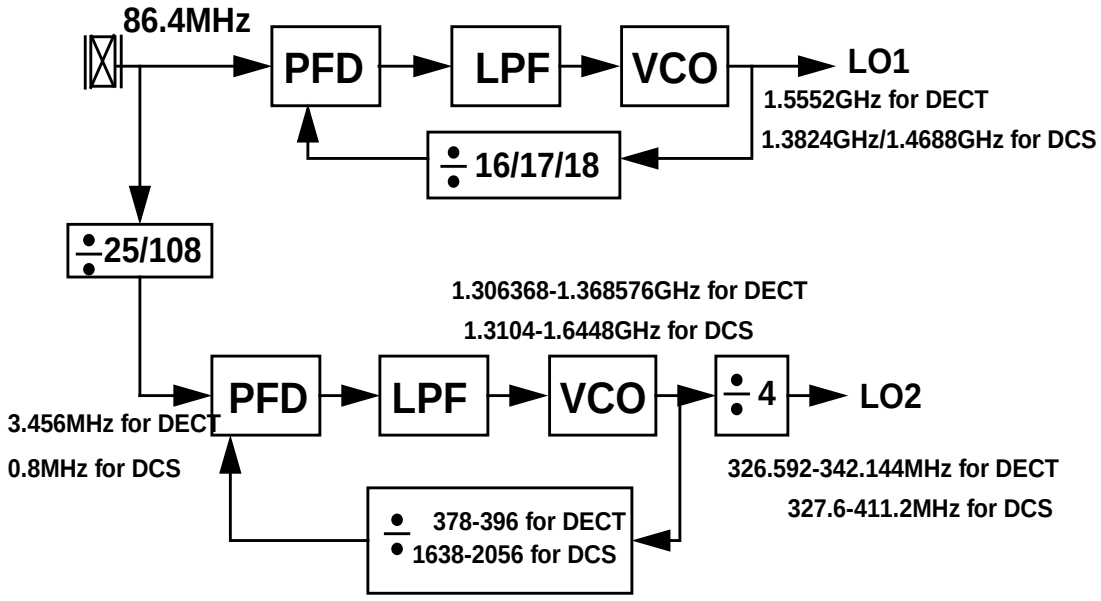


Fig. 5.6: PLL implementation of the frequency plan

standards makes it possible to have only one LO1 and one LO2 to generate all frequencies for both DCS1800 and DECT.

5.2.2 Loop Parameter Design

The loop bandwidth of the wideband PLL needs to be optimized in order to achieve minimum overall phase noise at a the offset frequency where the performance is most critical. DECT has a much more relaxed specification to

meet than DCS1800. For DCS1800, the specification at *3MHz* offset frequency is the most difficult to meet, which is *-145dBc/Hz*. So the optimization of the loop bandwidth is to minimize the overall phase noise at *3MHz*.

An *86.4MHz* reference frequency is chosen for the reason mentioned above. The loop bandwidth of LO1 should be less than *1/10* of the reference frequency for the stability of the loop. For this design, the loop bandwidth is chosen to be about *8MHz* for maximum suppression of the VCO noise while maintaining low noise at *3MHz* from the reference, loop filter and PFD.

Fig. 5.7 shows one way to implement the loop filter based on an RC network. Knowing the desired loop bandwidth, we can determine the RC parameters of the loop filter by leaving enough phase margin for the loop.

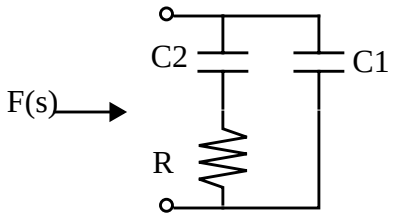


Fig. 5.7: Loop filter based on RC

We know the open-loop gain is

$$G(s) = \frac{K_\phi F(s) K_{vco}}{Ns} \qquad \text{(Eq 5-4)}$$

where F(s) is

$$F(s) = \frac{1}{sC_1} + \frac{1}{\frac{1}{R} + sC_2} = \frac{1 + sR(C_1 + C_2)}{sC_1(1 + sRC_2)} \qquad \text{(Eq 5-5)}$$

Let $P_3 = \frac{1}{RC_2}$ and $Z_1 = \frac{1}{R(C_1 + C_2)}$, then

$$F(s) = \frac{1 + s/Z_1}{sC_1(1 + s/P_3)} \quad \text{(Eq 5-6)}$$

and

$$G(s) = K_\phi \cdot \frac{1 + s/Z_1}{sC_1(1 + s/P_3)} \frac{K_{VCO}}{Ns} \quad \text{(Eq 5-7)}$$

The value of R, C1, C2 should be chosen so that G(s) has enough phase margin. For LO1, the value of R is 20kΩ, the value of C1 is 0.2pF and the value of C2 is 8pF. The phase margin is 75 degree.

For LO2, the loop bandwidth is chosen to be 40kHz. The value of R is 40kΩ, the value of C1 is 10pF and the value of C2 is 400pF.

5.2.3 VCO Design

The PLL will not be fully differential if the VCO is not differentially controlled. Fig. 5.8 shows the circuit diagram of a differentially controlled VCO with differential outputs. A cascode current source is used to improve the power supply rejection ratio. PMOS devices with *1μm* channel length are used to reduce the 1/f noise. To maximize the frequency control range, the output common mode level is set to the midpoint between the V_{dd} and *GND* by choosing the appropriate ratio of the current and the size of the cross coupled NMOS

devices. A common-mode feedback circuit in the loop filter sets the common-mode level of the control voltage to be the same as the common-mode level of the VCO outputs. This way the differential-mode signal of the control voltage has the largest effective control range.

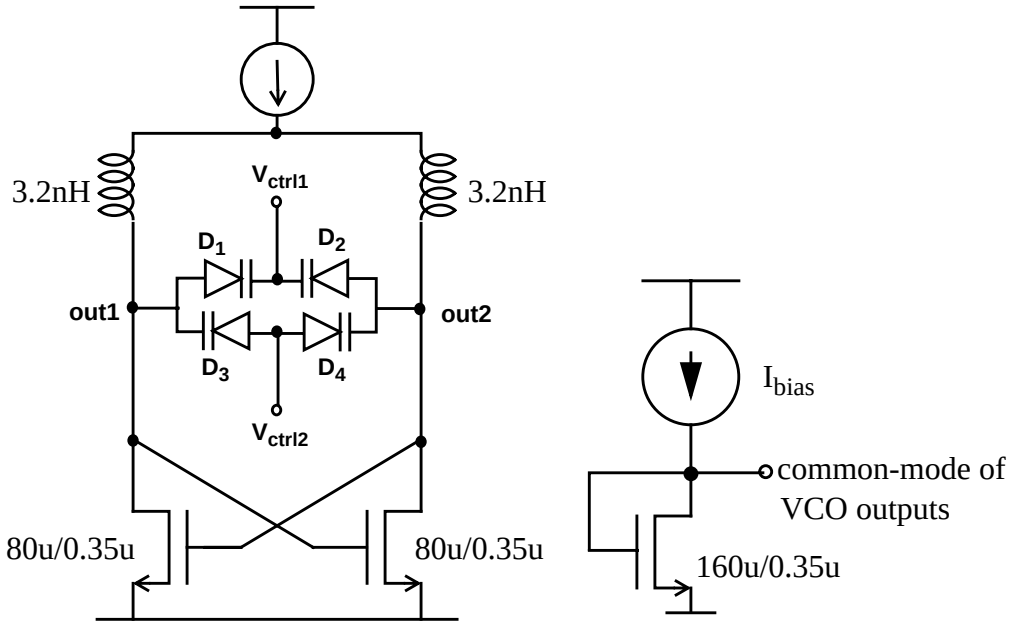


Fig. 5.8: Differentially controlled VCO with differential outputs

5.2.4 Charge Pump Design

The bias circuit for the charge pump is shown in Fig. 5.9. The vd_{sat} of the devices are set to be about 400mV to minimize the noise.

The charge pump circuit is shown in Fig. 5.10. Because the vd_{sat} of the cascode current source is about *400mV*, the headroom of the charge pump v_{cp1} and v_{cp2} is reduced to $vdd - 2 \times vd_{sat} = 3.3V - 4 \times 0.4 = 1.7V$. There are two

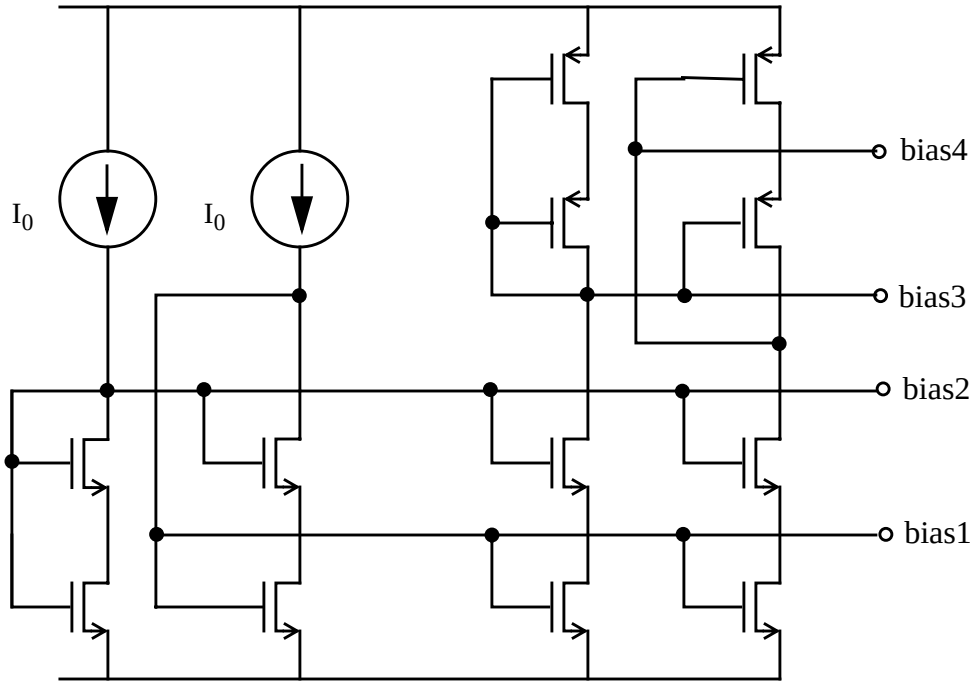


Fig. 5.9: Bias circuit for charge pump

disadvantages if the charge pump outputs are used directly to control the VCO. First, the VCO will not have enough tuning range because of the limited control voltage range. Second, the need for different control voltages for different frequencies creates a static current mismatch between the I_{up} and I_{dn}, which creates a spurious tone at the comparison frequency.

To avoid these two disadvantages, an active loop filter is used. The opamp OP_3 is used to set the differential mode level of the charge pump outputs, which are the same as the opamp inputs while any current difference between I_{up} and I_{dn} goes through the RC network and creates a voltage difference at the loop filter output V_{ctrl1} and V_{ctrl2}. Two 200k resistors are used to sense the common-

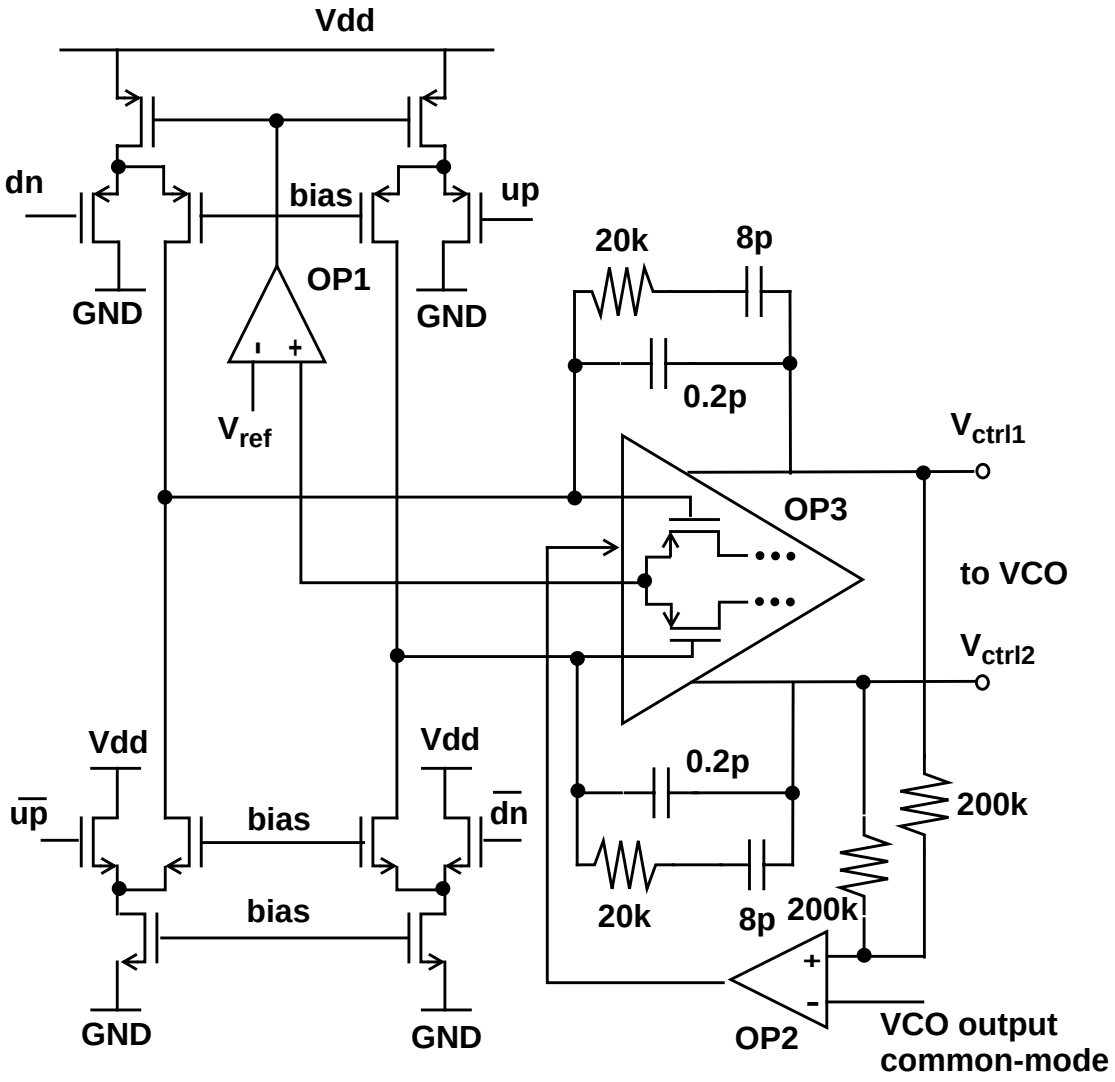


Fig. 5.10: Charge pump with active loop filter for LO1

mode level of V_{ctrl1} and V_{ctrl2}. The opamp OP2 is used to set the common-mode level of V_{ctrl1} and V_{ctrl2} to be the same as the common-mode level of the VCO outputs. This is a continuous CMFB loop. The common-mode level of V_{cp1} and V_{cp2} is sensed through the source of the differential pair at the input of OP_3 without loading down the output resistance at the charge pump output. The opamp OP_1 compares this common-mode voltage with a desired reference and

sets the gate of the PMOS current source so that the common-mode level of the charge pump output is the same as bias4 in the bias circuit. In this way the I_{up} and I_{dn} match ideally. The detailed circuit of the OP3 in the active loop filter and the two CMFB circuits are shown in Fig. 5.11.

Because this CMFB loop includes the charge-pump current source which is only on for a portion of the frequency comparison period, it is actually a sampled-data CMFB loop. Assuming the feedback loop bandwidth is f_0 if the charge pump is always on, and the duty cycle of the charge-pump current source is D, then the actual loop bandwidth is Df_0 if the comparison frequency is much higher than Df_0 and it can be viewed as a continuous CMFB loop. The loop bandwidth of the two CMFB loop must be either much greater or smaller than the PLL loop bandwidth and the unity-gain bandwidth of OP3 must be much greater than the PLL loop bandwidth with the loading of VCO to ensure the stability of the PLL.

5.2.5 Frequency Divider Design

When a low noise latch clocked by the VCO is added at the output of the frequency divider, the noise generated by the divider itself is bypassed and a significant amount of power can be saved in the divider. Because the latch is clocked by the VCO running at GHz frequencies, the divider output must be ready within one period of the VCO output. This can be hard to achieve. One way to reduce the uncertainty in the logic delay is to reclock the low-noise latch

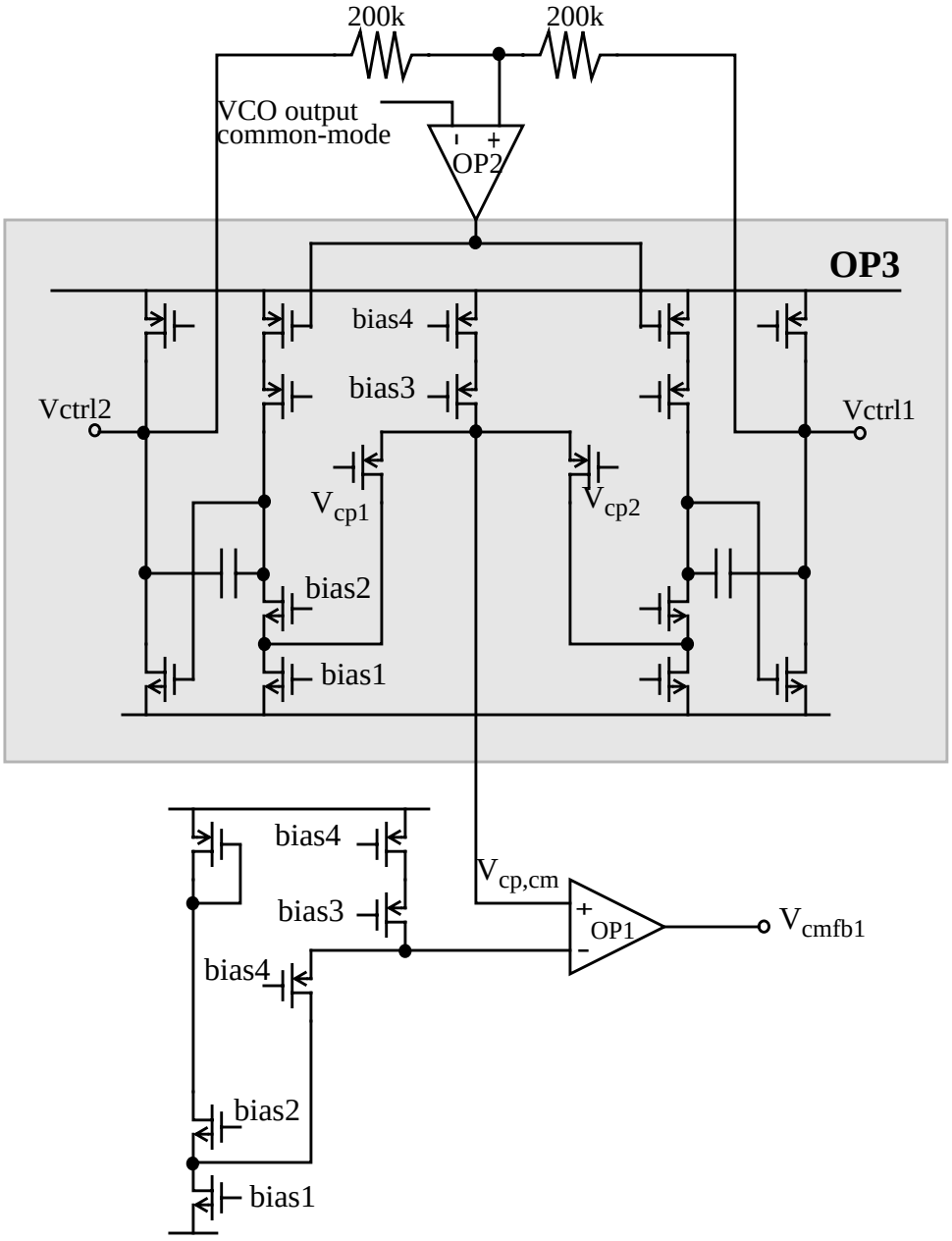


Fig. 5.11: Detailed circuit of OP3 and its input/output CMFB

input by the prescaler output. Fig. 5.12 shows the scheme. With this scheme, the low-noise-latch input is only one gate delay after the prescaler output and can be

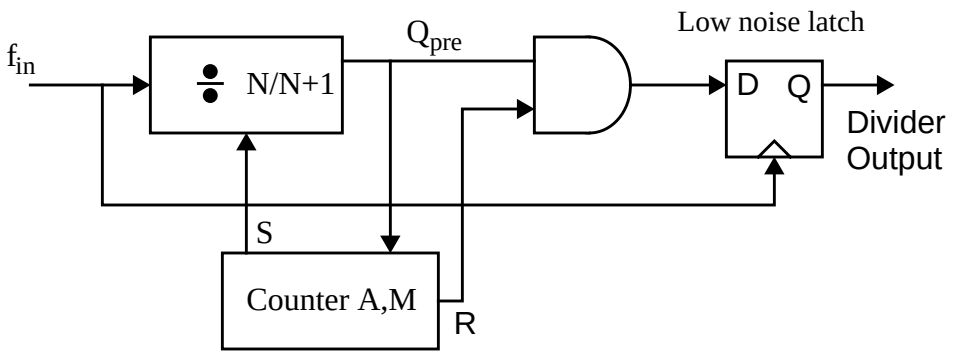


Fig. 5.12: Low noise latch input re-clocked by prescaler output

latched immediately. Counter A,M output R should be ready within half the period of the prescaler output.

Fig. 5.13 shows the counter outputs can also be re-clocked by the prescaler output to reduce the uncertainty in the logic delay.

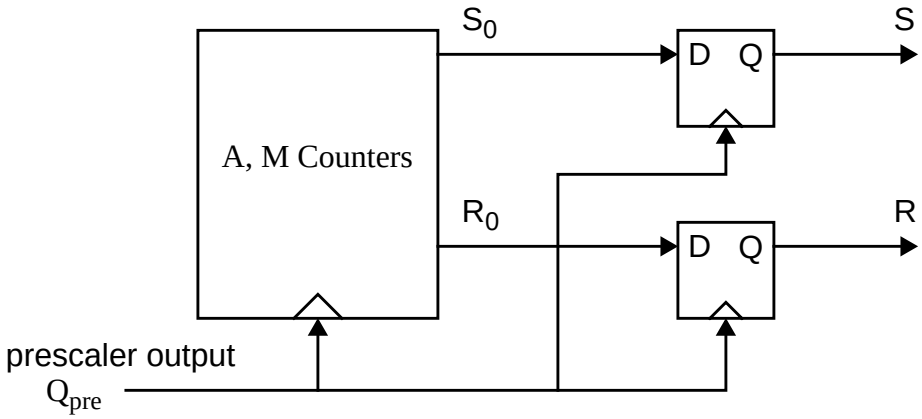
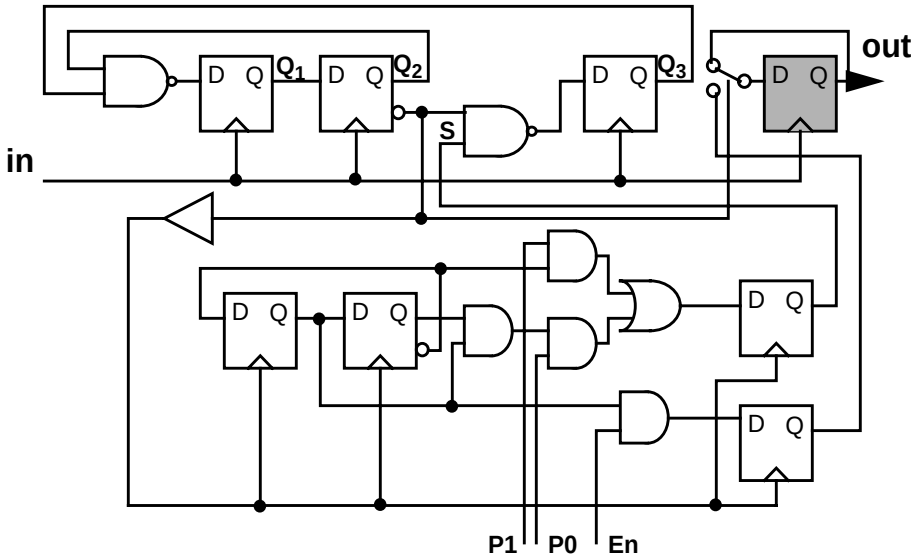


Fig. 5.13: Counter outputs re-clocking

The complete block diagram of a prescaler with divider ratio of *16, 17,* and *18* is shown in Fig. 5.14. The shaded block is the low noise latch clocked by the VCO output.



divider ratio = 16 + 2P1 + P0

Fig. 5.14: Block diagram of a prescaler with dividing ratio 16/17/18

5.3 Simulations Results

Full-loop simulation results using HSPICE are shown in Fig. 5.15. The first spectrum shows the spurious tone is *-56dBc* at multiples of *86.4MHz* away from the carrier frequency. When a *200mV* peak-to-peak sinewave at *5.4MHz* is applied to the power supply of the PLL, a tone of *-35dBc* appears at *5.4MHz* away from carrier, as shown in the second spectrum. The third spectrum is the

difference of the Up and Dn signals at the PFD outputs. This is a measure of the static phase error of the PLL. A *-80dB* tone at DC translates a static phase error of 0.01 degree.

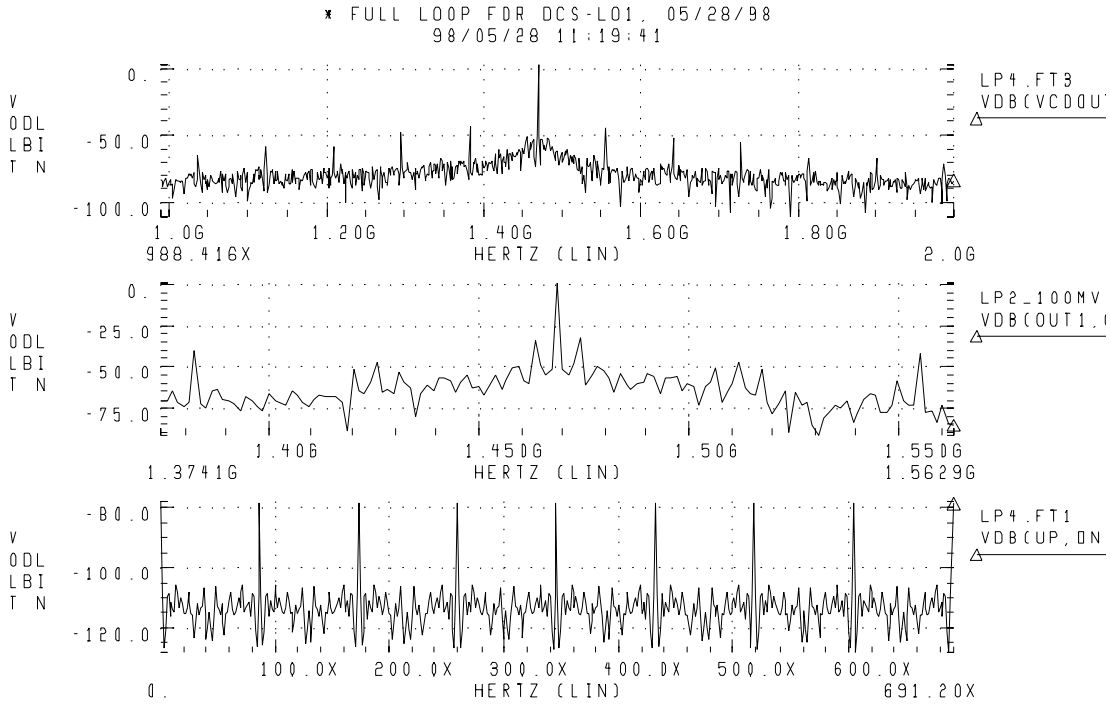


Fig. 5.15: Full loop simulation results using HSPICE

5.4 Measurement Results

The concepts describes above were embodied in two prototypes. The first prototype was fabricated in a 0.35mm 2-poly 5-metal CMOS process,

intended as the LO1 in a DECT/DCS1800 dual-mode transceiver, shown in Figure 5.16.

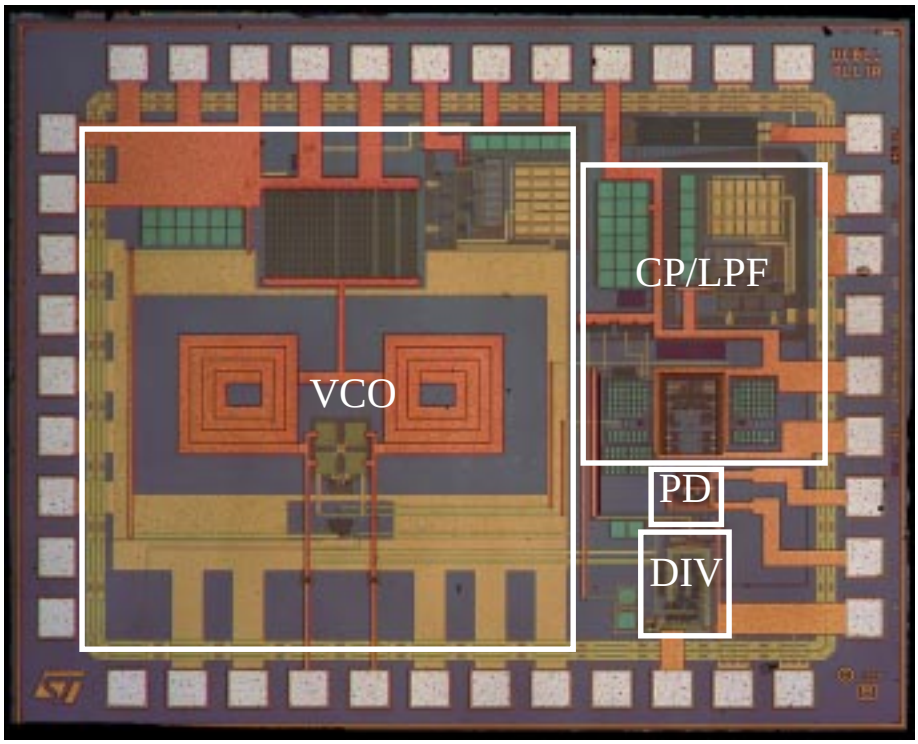


Fig. 5.16: Die micrograph of LO1

The second prototype contains both LO1 and LO2 that are integrated in the transceiver.

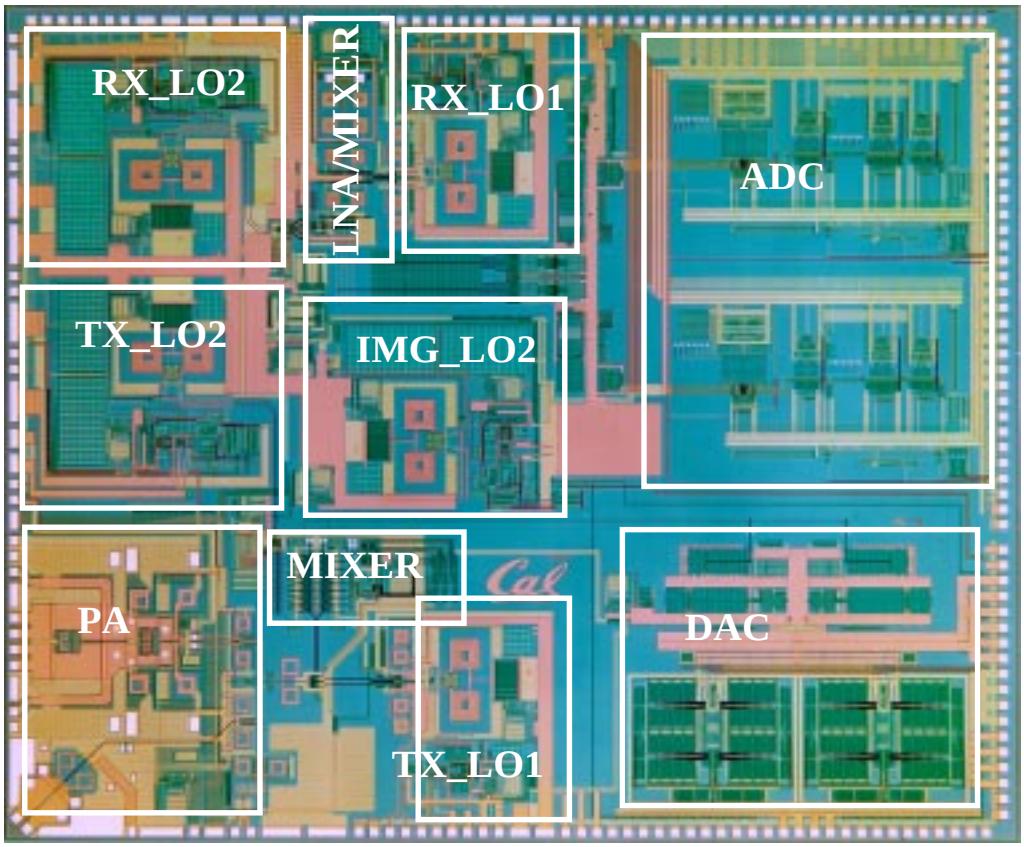


Fig. 5.17: Die Micrograph of complete transceiver including LO1 and LO2 for both transmitter and receiver

The first prototype, which is the stand-alone LO1, produces three RF frequencies, e.g., *1.3824GHz, 1.4688GHz,* and *1.5552GHz* corresponding to the frequency plan of the dual-mode transceiver application, while achieving a

phase noise of *-118dBc/Hz* at *100kHz*, shown in Figure 5.18, and a spurious tone of *-56dBc* at *86.4Mhz*.

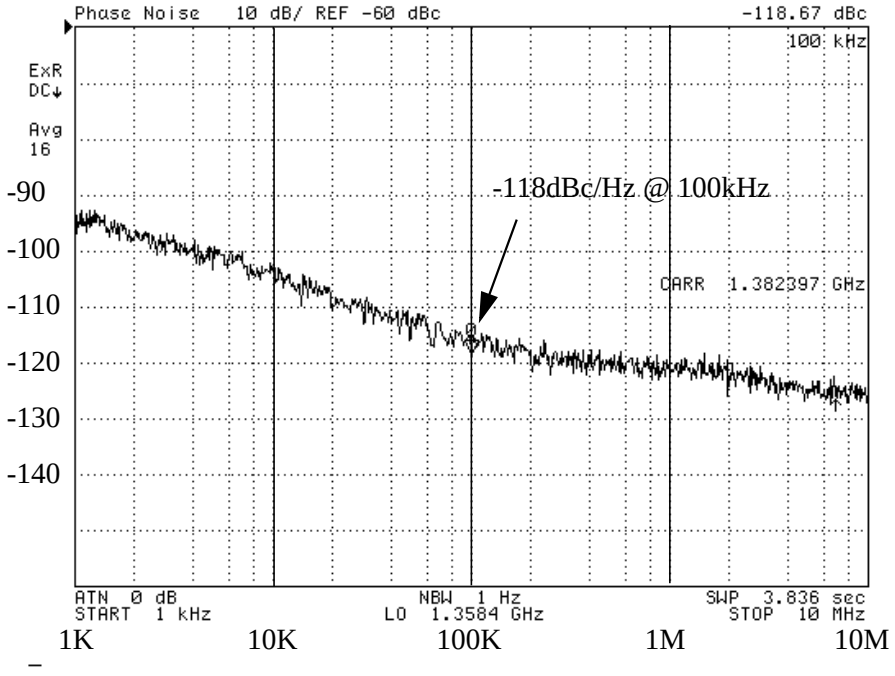


Fig. 5.18: Measured phase noise performance

When a *0.8MHz 100mV* 0-to-peak sinewave is added to the supply, the synthesizer phase noise at *100kHz* degrades to *-116dBc/Hz*, shown in Figure 5.19. A spurious tone of *-42dBc* is produced at *0.8MHz* due to the supply ripple.

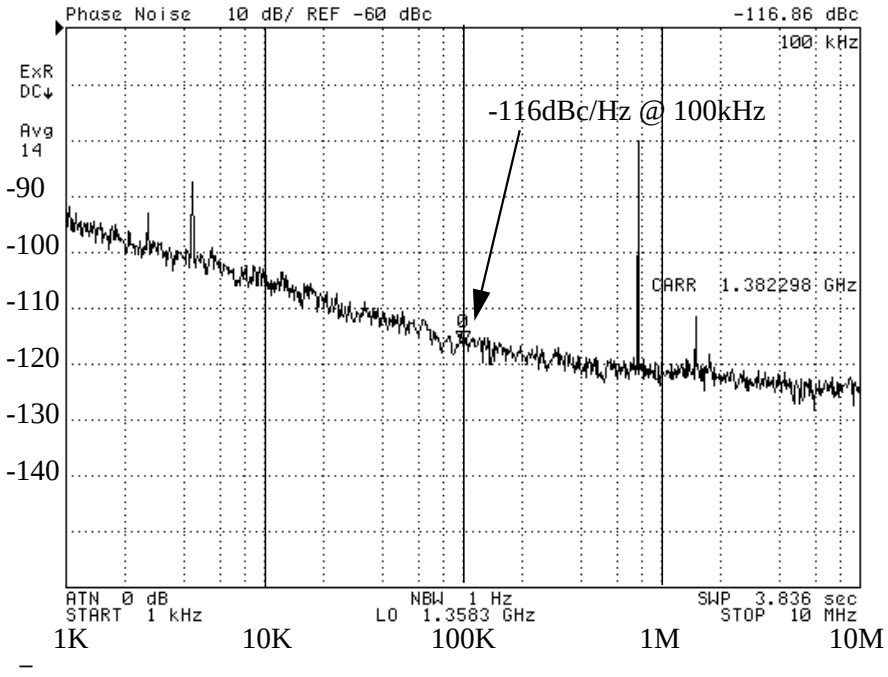


Fig. 5.19: Measured phase noise when a 100mv 0-to-peak sinewave at 0.8MHz is applied to power supply

More data points were taken to check the supply rejection performance across the frequency range from *200kHz* to 10*MHz*. Spurious tones produced by the supply ripple were measured and plotted in Figure 5.20. It can be used to deduce the allowed supply perturbation for a given spurious specification. For example, the worst case spurious tone when a *100mV* 0-to-peak ripple is applied to the supply is *-39dBc*. If we assume the

spurious tone and supply ripple amplitude has a linear relationship, then for a spurious tone specification of *-49dBc*, the maximum allowed supply ripple is about *30mV*.

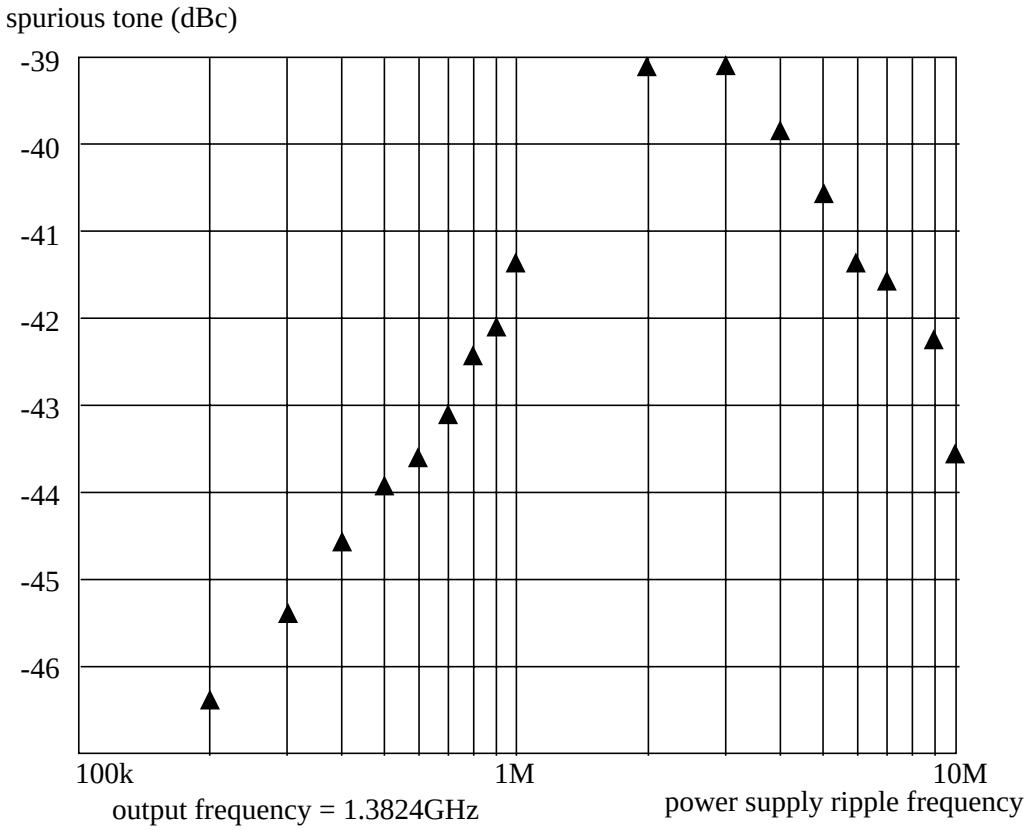


Fig. 5.20: Supply sensitivity vs. power supply ripple frequency

The complete synthesizer dissipates *84mW* from a *3.3V* supply. Table 5.1 shows the summary of the chip performance and Fig. 5.21 shows a comparison with other recently published work.

VDD	3.3V	
Power	VCO	39.55mW
	the rest of PLL	44.5mW
	Total	84.05mW
Output Frequency	1.3824GHz 1.4688GHz 1.5552GHz	
Phase Noise	-118dBc/Hz @ 100kHz	
	-120dBc/Hz @ 1MHz	
	-123dBc/Hz @ 3MHz	
Spurious Tones	-56dBc @ 86.4MHz	
Spurious Tones due to 100mV supply ripple	-46dBc ~ -39dBc	
Die Size	2260µm x 1860µm	
Technology	0.35µm CMOS, 5 metal layers, 2 poly	

Table 5.1: Performance summary of LO1

The performance of the second prototype which contains both LO1 and LO2 integrated in a full transceiver was evaluated[38]. While LO1 produces the same three frequencies as the first prototype, LO2 produces frequencies from 327.6MHz to 367.6MHz in 0.2MHz step. When applying a modulated GSM digital baseband signal, less than 1.5 degree rms and 4 degree peak phase error is achieved. The complete LO1, LO2 and the IQ generating VCO buffer draws 95mA from a 3.3V supply.

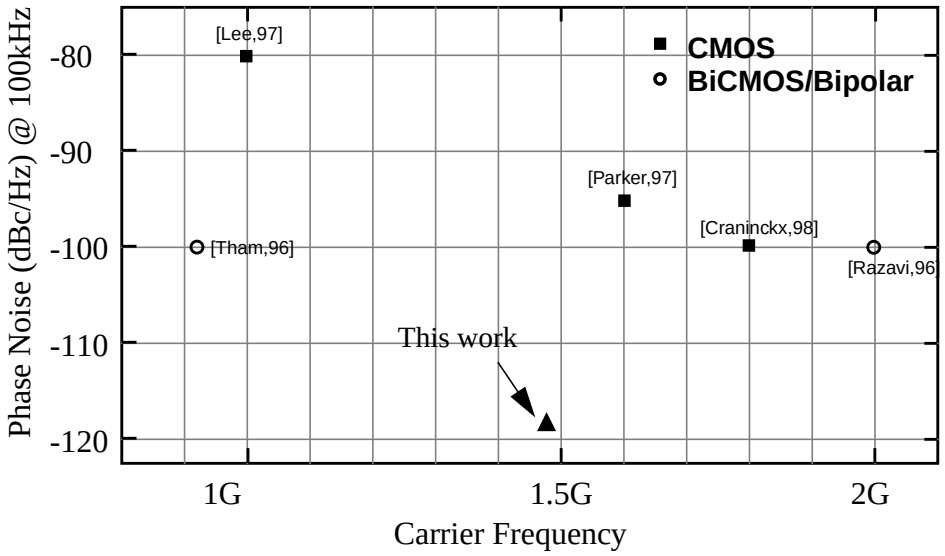


Fig. 5.21: Comparison of recently published work on integrated synthesizer

Chapter 6

Conclusion

In this thesis, the fundamental limitations on high-performance frequency synthesizer specifications are examined. A wide-bandwidth-PLL-based frequency synthesizer architecture is proposed. Various circuit techniques to minimize phase noise and spurious tones are explored. A fully-integrated wide-band high-performance RF frequency synthesizer using low-Q on-chip components for a multi-standard CMOS RF transceiver is demonstrated in a prototype. Both the wide-band RF synthesizer and the narrow-band IF synthesizers were integrated in a fully integrated DECT/DCS1800 dual-mode transceiver. The performance of the two synthesizers were evaluated in the context of the fully integrated transceiver.

The main points of note are:

- Among several frequency synthesizer architectures, e.g., DDFS, narrow band PLL, Fractional-N PLL, and wideband PLL, the wideband PLL is the most amenable to integration while still capable of high performance. In this architecture, the noise contribution from the VCO is suppressed within the loop bandwidth. This allows a relative noisy on-chip VCO to be used.

- Because noise from the VCO is suppressed in wideband PLL architectures, other noise sources become more important in the overall synthesizer performance. Noise from the crystal oscillator reference, buffer, and phase/frequency detector become the most important contributors within the loop bandwidth and are referred to the output enhanced in effect by the divider ratio N.

- Noise from the charge pump and loop filter is amplified by the VCO gain around the loop bandwidth. For an integrated wideband PLL, the VCO gain is usually large because of the limited control voltage range and large frequency range required by the application. Thus the charge pump and loop filter are significant noise contributors at the offset frequency around the loop bandwidth.

- For many applications, transceiver integration levels will be such that the receiver path, transmit path, the complete synthesizer, and perhaps the RF power amplifier will coexist on a single integrated circuit, along with a significant amount of A/D conversion and base-band processing. This in turn requires the synthesizer maintain its phase noise and spurious tone performance in the presence of components which deliver significant current and voltage perturbations to both the substrate GND and supply. Fully differential implementation of the complete PLL path is important for this reason.

- A differentially-controlled VCO with differential outputs is proposed to realize the fully differential PLL.

- A low-noise charge pump with active loop filter is proposed to minimize spurious tones due to the frequency comparison process and to maximize the frequency tuning range of VCO.

- A low-noise buffer clocked by the VCO is proposed to remove noise from the frequency divider.

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