High-Performance Pipeline A/D Converter
Design in Deep-Submicron CMOS

by

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Abstract

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Analog-to-digital converters (ADCs) are key design blocks in modern microelectronic digital communication systems. With the fast advancement of CMOS fabrication technology, more and more signal-processing functions are implemented in the digital domain for a lower cost, lower power consumption, higher yield, and higher re-configurability. This has recently generated a great demand for low-power, low-voltage ADCs that can be realized in a mainstream deep-submicron CMOS technology.

Intended for embedded communication applications, specifications of these converters emphasize high dynamic range and low spurious spectral performance. For example, the worst-case blocking specs of some wireless standards, such as GSM, dictate a conversion linearity of 14-16 bits to avoid losing a weak received signal due to distortion artifacts. It is nontrivial to achieve this level of linearity in

a monolithic environment where post-fabrication component trimming or calibration is cumbersome to implement for certain applications or/and for cost and manufacturability reasons.

Another hurdle to achieve full system integration stems from the power efficiency of the A/D interface circuits supplied by a low voltage dictated by the gate-oxide reliability of the deeply scaled digital CMOS devices. It has been observed recently that these interface analog/mixed-signal circuits are gobbling a larger chunk of the chip area as well as total power consumption; hence it becomes essential to accomplish an optimized design from both the architecture and the circuit standpoints. To achieve high linearity, high dynamic range, and high sampling speed simultaneously under low supply voltages in deep-submicron CMOS technology with low power consumption has thus far been conceived of as extremely challenging.

This thesis addresses these challenges using the pipeline ADC as a demonstration platform. Specific new design techniques/algorithms include (1) a power-efficient, capacitor ratio-independent conversion scheme, (2) a pipeline stage-scaling algorithm, (3) a nested CMOS gain-boosting technique, (4) a $\Delta\Sigma$ common-mode voltage regulation circuit, (5) an amplifier and comparator sharing technique, and the use of minimum channel-length, thin oxide transistors with clock bootstrapping and in-line switch techniques. The prototype design of a 14-

bit pipeline ADC fabricated in a 0.18-μm CMOS technology that achieves an over 100-dB spurious-free dynamic range (SFDR) demonstrates the effectiveness of these techniques.

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Professor Paul R. Gray, Chair

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Chapter 1 _____

INTRODUCTION

1.1 WIRELESS COMMUNICATION

The rapid evolution of the silicon integrated circuits (IC) during the last two decades has enabled the miniaturization of narrow-band mobile phones that can operate on batteries for reasonable lifetimes. The aggregation of the research results of the radio-frequency (RF) microelectronics – carried out in both universities and industry – has spurred an exponential growth in the market of personal wireless communications, especially when the CMOS technology was demonstrated to be a good contender to achieve an integrated RF, intermediate-

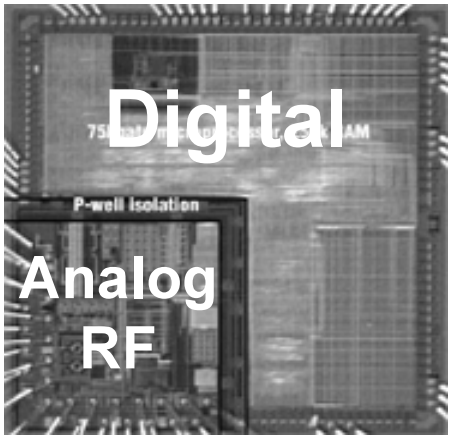

Figure 1.1 Ericsson single-chip 0.18-μm CMOS Bluetooth radio (2001).

frequency (IF), and baseband analog/mixed signal front-end in conjunction with the back-end digital signal-processing (DSP) circuits. The economics has thus far been the major driving force to accomplish a higher level of integration with potential requital of lower power dissipation, smaller form factor, and ultimately lower cost. One example of this genre is the all-CMOS Bluetooth transceiver from Ericsson that has achieved the RF-analog-digital integrated wireless system on a chip (SoC).[1] A die photo of this chip is shown in Figure 1.1.

With the proliferation of wireless communication products and standards, broadband radios are rapidly emerging as the dominant technology to provide users with high data-rate connections in limited geographical areas where a traditional wired infrastructure may incur high installation and maintenance costs. Among these endeavors, the wireless local area network (LAN) standards – the

Table 1.1 Overview of broadband wireless technologies

Technology	Data Rate (Mb/s)	Range (m)	Multi-Access Technique	Bandwidth (MHz)	Carrier Frequency
Bluetooth	1	10	FHSS	1	2.4-GHz ISM
IEEE 802.11a	54	20	OFDM	20	5-GHz UNII
IEEE 802.11b	11	50	DSSS	22	2.4-GHz ISM
IEEE 802.11g	54		DSSS, OFDM		
DVB-T	5-32	80,000	OFDM	8	130-160 MHz, 430-862 MHz
UWB	100-500	10	DSSS, OFDM	≥ 500	3.1-10.6 GHz

IEEE 802.11a/b/g – are the most noteworthy. Commercial products in this category can now be purchased in retail electronic stores worldwide. The Bluetooth radio, intended for short-range applications such as computer peripherals, PDAs, consumer electronics, and smart home appliances, is also gaining a wider deployment. Most recently, the ultra-wideband (UWB) radio and the cognitive radio are directing the spotlight of wireless communications industry. The UWB radio envisions a transmission rate of 100-500 Mb/s for short-range applications with a nearly undetectable transmission power level that seamlessly hides its operation in the background noise. The cognitive radio is promoting a concept similar to that of the software-defined radio (SDR) where the ability to adapt to the environment is the prominent feature as well as the major technical challenge. Table 1.1 provides an overview of these wireless technologies.

1.2 CHALLENGES OF BROADBAND RADIO

The exponentially growing demand of wireless data-rate coupled with the increasingly crowded usage of the incumbent RF spectrum directs the radio research on the physical layer communications engineering. Although the data-rate and the bandwidth required for transmission are not identical, they are closely related by the law of information theory, known as the Shannon limit

$$C = W \cdot \log_2(1 + \frac{P_{av}}{W \cdot N_0}), \tag{1.1}$$

where, C is the channel capacity in bits/s, W is the channel bandwidth in hertz, P_{av} is the average signal power in watts, and N_0 is the power spectral density (PSD) of the additive white Gaussian noise (AWGN) in watts/Hz.[2]

It is deduced from (1.1) that a higher transmission data-rate can be achieved by increasing either the channel bandwidth or the signal-to-noise ratio (SNR). Although this observation is drawn from the simple hypothesis of an AWGN channel, the underlying principle is ubiquitous even when sophisticated wireless channel models are assumed, be it a multi-path propagation or with advanced time-frequency-space coding. The implication is that a broadband radio is technically more challenging than its narrowband counterparts in that the information to be processed by the transceiver potentially occupies more bandwidth, exhibits a higher sensitivity to noise, or both.

In addition to the principal hurdles, the cost and mobility of a broadband radio are also adversely affected by the following factors that have been challenging the wireless communications system engineers all along:

Fading. The non-stationary nature of the mobiles or the environment dictates the wireless channel to be time-varying. The channel response may be quite different from the start of transmission to the end. Ideally, a flat frequency response is desired but often very difficult to come across for broadband channels. Narrowband channels are benign in the sense that the channel response hardly

exhibits variations for a very narrow RF bandwidth – a phenomenon termed "flat fading".

Multi-User. The users of the wireless medium are geographically separated and often uncoordinated. To achieve spectral efficiency in a cellular multipoint-to-point or point-to-multipoint communication is significantly more challenging than in a single-user environment, particularly when the data-rate requirements are heterogeneous. The transmission of one user may also be completely "blocked" when his/her desired signal is overwhelmed by a strong nearby interference signal, often unintentionally exerted by another user.

Power Limitation. Since the majority of mobile users are battery operated, power efficiency, in addition to spectral efficiency, is crucial. This applies not only to the transmitted power but also to the circuit-dissipated power. Sophisticated designs required to approach the capacity limit, e.g., certain coding algorithms, may not be advisable for a battery-operated terminal.

1.3 CMOS TECHNOLOGY SCALING

Propelling the great venture and unprecedented success of digital techniques, the CMOS technology has emerged and dominated the mainstream silicon IC industry in the last few decades. As the lithography technology improved, the MOS device has kept shrinking its minimum feature size over the last forty years and greatly impacted the performance of digital integrated circuits – the

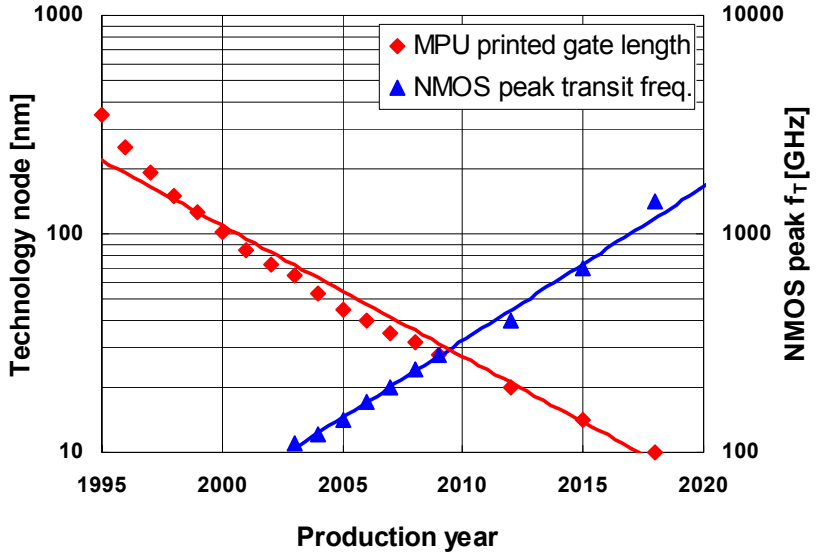

Figure 1.2 Scaling trend of silicon CMOS according to the 2003 edition international technology roadmap of semiconductor (ITRS).[3]

computing power that can be packed into a single chip has been constantly doubled every 18-24 months, known as the Moore's law (Figure 1.2).

During the course of pursuing a higher level of system integration and lower cost, the economics has driven technology to seek solutions to integrate analog and digital functionalities on a single die using the same or compatible fabrication processes. With the inexorable scaling of the MOS transistors, the raw device speed takes great leaps over time, measured by the exponential increase of the *transit frequency* f_T – the frequency where a transistor still yields a current gain of unity (Figure 1.2). The advancement of technology culminated in a dramatic performance improvement of CMOS analog circuits, opening an avenue to

Table 1.2 Impact of technology scaling on analog circuit design

CMOS Technology Scaling		Design Constraints			
		Channel length	Oxide	V_{DSAT}	Circuit Complexity
Intrinsic Speed	$f_T \uparrow$	Short	Thin	Large	Low
Power Supply	$V_{DD} \downarrow$	/	/	Small	Low
Thermal Noise	$4kT(\gamma \cdot g_m) \uparrow$	Long	Thick	/	Low
Intrinsic Gain	$g_m \cdot r_{out} \downarrow$	Long	Thick	Small	High
Device Matching	$W, L \downarrow$	Long	/	/	Low
Device Modeling	SCE	Long	Thick	/	/

achieve system integration using a pure CMOS technology. Process enhancements, such as the triple-well option, even helped to reduce the noise crosstalk problem – one of the major practical limitations of sharing the substrate of precision analog circuits with noisy digital logic gates.

As CMOS integrated circuits are moving into unprecedented operating frequencies and accomplishing unprecedented integration levels, potential problems associated with device scaling – the short-channel effects (SCE) – are also looming large as technology strides into the deep-submicron regime. Besides that it is costly to add sophisticated process options to control these side effects, the compact device modeling of short-channel transistors has become a major challenge for device physicists. In addition, the loss of certain device characteristics, such as the square-law I-V relationship, adversely affects the

portability of the circuits designed in an older generation of technology. Smaller transistors also exhibit relatively larger statistical variations of many device parameters (i.e., doping density, oxide thickness, threshold voltage and etc.). The resultant large spread of the device characteristics also causes severe yield problems for both analog and digital circuits.

Table 1.2 summarizes the offerings of technology scaling alongside with the desired features from an analog design standpoint. In general, a short channel length gives rise to a short carrier transit time, hence a high f_T. However, the accompanying reduction of the supply voltage due to the reliability issue of thin oxide and the degradation of some fundamental device characteristics – e.g., intrinsic gain $g_m r_{out}$ – substantially limit the choice of analog circuit architectures and the achievable power efficiency. The conflicting design constraints shown in the right half of Table 1.2 also indicate that no unique set of process options can meet all the expectations for a specific analog/mixed-signal design. In other words, to achieve the optimal trade-offs given a set of design constraints seems to be a sensible target for good analog/mixed-signal designs.

1.4 A/D INTERFACE

One critical functional block in highly integrated CMOS wireless transceivers that exhibits keen sensitivity to technology scaling is the analog-to-digital interface circuit. Influenced by the advancement of the fabrication technology, the

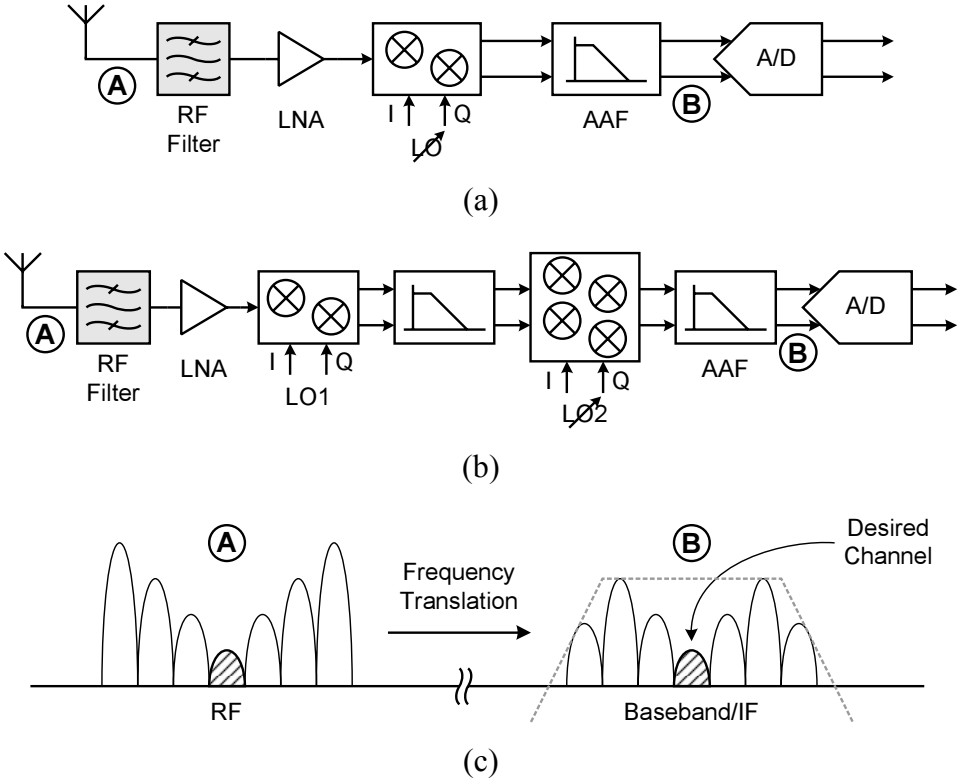

Figure 1.3 (a) Simplified block diagram of a direct-conversion RF receiver. Shaded blocks are off-chip components. (b) Simplified block diagram of a double-conversion receiver. (c) Signal spectrum at point A (after antenna) and B (before ADC).

boundary between analog and digital functionalities in these transceivers is constantly redefined. The trend toward more digital signal-processing for multi-standard agility in receiver designs has recently created a great demand for low-power, low-voltage analog-to-digital converters (ADCs) that can be realized in a mainstream deep-submicron CMOS technology.

Intended for embedded applications, the specifications of such converters

emphasize high dynamic range and low spurious spectral performance. In a CMOS radio SoC, regardless of whether frequency translation is accomplished with a single conversion, e.g., the direct-conversion (Figure 1.3a) and low-IF architecture, or a wideband-IF double conversion (Figure 1.3b), the lack of high-Q on-chip IF channel-select filters inevitably leads to a large dynamic range imposed on the baseband circuits in the presence of in-band blockers (strong adjacent channel interference signals as shown in Figure 1.3c). For example, the worst-case blocking specs of some wireless standards, such as GSM, dictate a conversion linearity of 14-16 bits to avoid losing a weak received signal due to distortion artifacts.[4, 5, 6] Recent works also underline the trend toward the IF-digitizing architecture to enhance programmability and to achieve a more "digital" receiver.[7, 8, 9] However, advancing the digitizing interface toward the antenna exacerbates the existing dynamic range problem, as it also requires a high oversampling ratio. To achieve high linearity, high dynamic range, and high sampling speed simultaneously under low supply voltages in deep-submicron CMOS technology with low power consumption has thus far been conceived of as extremely challenging.

1.5 RESEARCH CONTRIBUTION

Among various ADC architectures, the pipeline converter is widely used in Nyquist sampling applications that require a combination of high resolution and

high throughput. This dissertation describes the prototype design of a 14-bit pipeline ADC fabricated in a 0.18-μm digital CMOS technology. Specific research contributions of this work include:

- A power-efficient passive capacitor error-averaging technique, which achieves a ratio-independent A/D conversion scheme;
- Identifying a precise breakdown of the circuit noise contribution in a switched-capacitor pipeline converter. A pipeline stage-scaling algorithm that addresses the capacitor taper factor and the per-stage resolution simultaneously is introduced;
- A nested CMOS gain-boosting technique that achieves a minimum of 130-dB DC-gain with 0.2-μm thin oxide transistors;
- A $\Delta\Sigma$ common-mode voltage regulation circuit is introduced to facilitate the control of the common-mode levels in pseudo-differential amplifiers;
- An amplifier and comparator sharing technique that reduces the total number of the amplifiers and comparators by half. A 14-b pipeline ADC is realized with six amplifiers and seven sub-ADCs.

1.6 THESIS ORGANIZATION

Chapter 2 of this thesis reviews the pipeline ADC architecture and discusses the design challenges for switched-capacitor circuits in deep-submicron CMOS

technology. To alleviate the prominent issue of power efficiency under low supply voltages, a pipeline ADC stage-scaling analysis is then introduced that determines the optimum stage resolution and scaling factor simultaneously. Following this, Chapter 3 highlights the key linearity technique of this design – the passive capacitor error-averaging technique. In Chapter 4, the details of the circuit implementation issues are presented. The experimental results of the prototype chip are summarized in Chapter 5 with the conclusion and future works following in Chapter 6.

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Chapter 2 _____

PIPELINE ARCHITECTURE POWER EFFICIENCY

2.1 PIPELINE ADC ARCHITECTURE

A pipeline A/D converter is inherently a multi-step amplitude quantizer in which the digitization is performed by a cascade of many topologically similar or identical stages of low-resolution analog-to-digital encoders. Pipelining enables high conversion throughput by inserting analog registers, i.e., sample-and-hold amplifiers (SHAs), in between stages that allow a concurrent operation of all stages. This is done at the cost of an increased latency. The block diagram of a pipeline ADC is shown in Figure 2.1.

A pipeline stage takes two actions when an input signal arrives (signaled by a master clock) – a snapshot of the input by the sample-and-hold (S/H) and a coarse quantization by the sub-ADC. These two operations are often performed simultaneously or in tandem. The resolution of a typical pipeline stage is usually

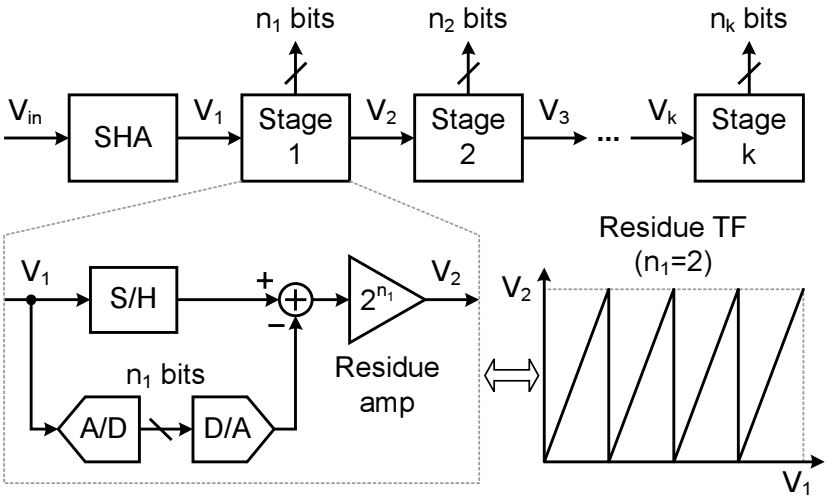

Figure 2.1 Block diagram of a pipeline A/D converter.

no more than four bits. The resolution of the conversion is enhanced by passing a residue signal – the unconverted part of the input signal – to the later stages where it is further quantized (Figure 2.1). The conversion residue is created by a digital-to-analog converter (DAC) and a subtraction circuit. The maximum swing of this residue signal is often brought back to the full-scale reference level with a precision amplifier – the residue amplifier in Figure 2.1. This keeps the signal level constant and allows the sharing of an identical reference throughout the pipeline stages.

Breaking a high-resolution conversion into multiple steps greatly reduces the total number of comparators required in contrast to a flash converter. In the limiting case, a 1-bit/stage (b/s) pipeline ADC only needs N comparators to resolve an N-bit code as opposed to 2^N comparators required by a flash converter.

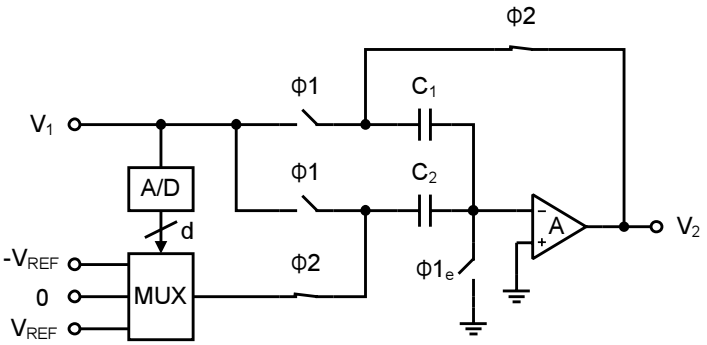

Figure 2.2 Circuit diagram of the 1.5-b/s MDAC.

The large accumulative inter-stage gain also relaxes the impact of circuit non-idealities, such as noise, nonlinearity, and offset, of later stages on the overall conversion accuracy. For medium- to high-resolution Nyquist applications, pipeline ADCs have been demonstrated to achieve the lowest power consumption at relatively high conversion rates.[1-10]

In CMOS circuit technology, a typical pipeline ADC stage usually consists of a coarse comparator and a compact switched-capacitor circuit termed the multiplier DAC (MDAC), which integrates the sample-and-hold, the DAC, the subtraction, and the residue-gain functions.[3] The circuit diagram of a single-ended 1.5-b/s MDAC is shown in Figure 2.2. This architecture is also known to tolerate large comparator offsets due to the built-in decision level overlaps between successive stages, usually referred to as digital redundancy or digital error-correction (DEC).[3] The conversion accuracy thus solely relies on the precision of the residue signals; the conversion speed, on the other hand, is largely determined by the settling speed of the residue amplifier.

2.2 POWER EFFICIENCY UNDER LOW SUPPLY VOLTAGE

As mentioned in Chapter 1, while the scaling of CMOS technology offers a potential for improvement on the operating speed of mixed-signal circuits, the accompanying reduction in the supply voltage and various short-channel effects create both fundamental and practical limitations on the achievable gain, signal swing, and noise level of these circuits, particularly under a low power constraint.

2.2.1 $\frac{kT}{C}$ NOISE

For noise-limited analog designs, the circuit fidelity relies on the relative contrast of the signal strength to that of the noise, measured by the signal-to-noise ratio (SNR) in decibels. Although the final calculation should have all man-made noise sources included, the scope of discussion in this chapter will be limited to those that are fundamental – the thermal noise, the Flicker noise, and etc.

For discrete-time analog signal-processing circuits, especially those using the switched-capacitor technology, analog signals are usually acquired and processed in a batched fashion where a snapshot of the signal is taken periodically controlled by a clock signal – a process termed sampling. As the sampling circuit cannot differentiate the noise from the signal, part of that snapshot corresponds to the instantaneous value of the noise at the moment the sampling takes place. In the context of switched-capacitor circuits where the sample is stored as charge on

a capacitor, the root-mean-square (rms) total integrated thermal noise voltage is

$$\sqrt{\overline{V_N^2}} = \sqrt{\int_0^\infty \frac{4kTR}{1+(2\pi f \cdot RC)^2} df} = \sqrt{\frac{kT}{C}}, \tag{2.1}$$

where kT is the thermal energy, R is the switch resistance, C is the sampling capacitance. This is often referred to as the $\frac{kT}{C}$ noise.

Note that (2.1) indicates that the integrated noise is independent of the switch resistance R (cancelled after integration). This is not surprising as when R is increased, hence higher noise floor, the bandwidth of the circuit is reduced and the total integrated noise stays constant.

2.2.2 Power Consumption of Pipeline ADC

For noise-limited designs, it can be derived that the power consumption of a switched-capacitor circuit is inversely proportional to the supply voltage for a fixed dynamic range (DR),

$$P \propto kT \cdot DR \cdot \left(\frac{V_{gs} - V_{th}}{V_{dd}} \right) \cdot f_s, \tag{2.2}$$

where kT is the thermal energy, f_s is the sampling rate, $V_{gs} - V_{th}$ is the overdrive voltage of the amplifier input transistors, and V_{dd} is the supply voltage.[12]

In pipeline ADCs, the sampling process inherent in switched-capacitor circuits

introduces the $\frac{kT}{C}$ noise at each pipeline stage when a residue voltage is captured. This noise usually comprises two major contributions – the channel noise of the switches and the amplifier noise. Since no direct current is conducted by the switch right before a sampling takes place (the bandwidth of the switch-capacitor network is assumed large and the circuit is assumed settled), the 1/*f* noise is not of concern here; only the thermal noise contributes, which is a function of the channel resistance that is weakly affected by the technology scaling.[13] On the other hand, the amplifier output noise is in most cases dominated by the channel noise of the input transistors, where the thermal noise and the 1/*f* noise both contribute.

Because the input transistors of the amplifier are usually biased in saturation region to derive large transconductance (g_m), impact ionization and hot carrier effect tend to enhance their thermal noise level;[14, 15] the 1/*f* noise increases as well due to the reduced gate capacitance resulted from finer lithography and therefore shorter minimum gate length. It follows that, as CMOS technology scaling continues, amplifier increasingly becomes the dominant noise source for switched-capacitor circuits. An accurate consideration of the intrinsic noise sources in such a circuit should have the thermal noise of switches, all amplifier noises readily included.

Interestingly, the total integrated output noise (the input-referred noise as well)

still takes the form of $\frac{kT}{C}$ with some correction factor, as those will be shown in the next section. Thus a fundamental technique to reduce the noise level, or to increase the signal-to-noise ratio of a switched-capacitor circuit, is to increase the size of the sampling capacitors. The penalty associated with this technique is the increased power consumption as larger capacitors demand larger charging/discharging current to keep up the sampling speed.

2.3 Stage-Scaling Analysis of Pipeline ADC

Exploiting the fact that later stages contribute a diminishing input-referred noise because of the accumulative inter-stage gain, one architectural approach to maximize the signal-to-noise ratio with a given power budget is to determine an optimum way of distributing the biasing current to each pipeline stage. The optimization involves choosing an optimum per-stage resolution and reducing the sampling capacitor sizes along the pipeline.

Both of the techniques are commonly encountered in the literature.[4, 11] Although it increases the design and layout time dramatically, tapering capacitor sizes can often greatly reduce the overall power consumption of a high-resolution pipeline ADC. But to choose the right per-stage resolution is not as straightforward – it often involves other architectural considerations such as the component matching accuracy in the front-end stages. The following discussion

will assume that to maximize the SNR is the sole constraint of the design.

Intuitively, a too low per-stage resolution (hence more stages) increases the number of residue resampling events. Coupled with a low inter-stage gain, this leads to larger capacitors and more biasing current. Conversely, although a high per-stage resolution (hence fewer stages) minimizes the number of resampling events and allows a rapid tapering of the capacitor size, the per-stage power increases exponentially due to the reduction of the feedback factor of residue amplifiers. This is clearly not power efficient as well. It follows that the optimum stage resolution has to be somewhere in between, but the exact answer depends on the conversion speed, the technology used, the circuit topology, and a specific layout. Due to the complexity of this problem, simple hand analyses, albeit lacking in numerical accuracy, are commonly used to reveal qualitative parametric trade-offs and to offer insight to circuit designers.

2.3.1 CLINE-GRAY MODEL

The first such analysis was introduced by Cline and Gray.[11] Analytical results were shown attempting to optimize both the per-stage resolution and the taper factor of the sampling capacitors. The noise model readily confirms the existence of an optimum taper factor, which is determined to be approximately the inter-stage voltage gain. A prototype 13-b, 5-MS/s pipeline ADC that achieved an SNDR of 80.1 dB was demonstrated dissipating only 166 mW on a 5-V supply.

As the analytical model predicted a monotonic decrease of the overall conversion power when the per-stage resolution is increased, a 2.5-b/s architecture was chosen based on inspection.[11]

It was pointed out that the analysis leading to the counterintuitive observation neglected the loading effect of parasitic capacitances on the amplifier, the interconnect capacitances, and the capacitive loading of the comparators on the output. In the next section, the parasitic-loading effects are considered as the analytical model is revisited. We will prove that for high-speed conversions, a 2-3-b/s architecture is indeed optimum from a power standpoint.

2.3.2 PARASITIC-LOADED AMPLIFIER MODEL

It was mentioned before that amplifier is increasingly becoming the dominant noise source in switched-capacitor circuits implemented in deep-submicron CMOS technology. It is therefore essential for a noise model intended to optimize

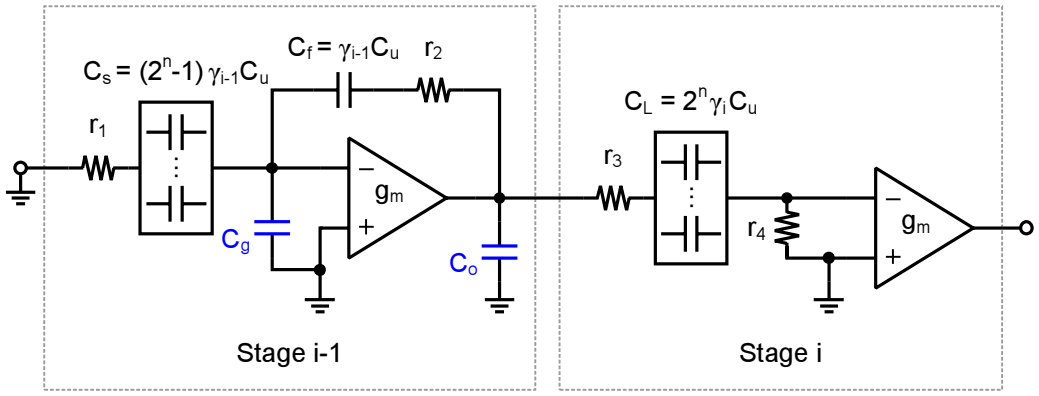

Figure 2.3 Noise model of MDAC including parasitic loading effects.

the SNR of a pipeline ADC to accurately account for all noise sources that ultimately contribute to the $\frac{kT}{C}$ noise. In addition, the noise transfer functions must be individually sorted as they originate from different components at different parts of the circuit.

Figure 2.3 shows the single-ended circuit diagram of two consecutive multiplier DAC stages of a typical switched-capacitor pipeline ADC, with all noise sources included – the g_m blocks that model the amplifier and r_1 through r_4 that model the switch on-resistance. Here, stage *i*-1 is assumed in phase $\phi 2$ (amplifying mode) and stage *i* is assumed in phase $\phi 1$ (sampling mode).

To begin the calculation, we assume that the per-stage resolution *n* is constant. The unit sampling capacitor for stage *i* is $\gamma_i C_u$, where C_u is the first stage unit sampling capacitor and the capacitor scaling factor for stage *i* is γ_i. The prominent feature of this model is the inclusion of the loading from the amplifier, the comparators, the switches, and the wiring, modeled by two capacitors – C_o at the output node and C_g at the summing node of the residue amplifier, respectively (Figure 2.3). An accurate account of the parasitics requires a post-layout extraction that is design specific.

At the architectural level, two observations are noteworthy in modeling these parasitics. First, to keep up the conversion speed, the transconductance of the

amplifier (hence its size and biasing current) must increase exponentially as a function of the stage resolution due to the exponential decrease of the feedback factor. Meanwhile the number of comparators and sampling switches, the wiring complexity of layout exhibit the same dependence. Second, the parasitic-loading effects worsen as the conversion rate increases. In a high-speed converter, the parasitic capacitance can be comparable to the total sampling capacitance. The model $C_o \approx C_g \approx \eta\left(2^n \gamma_i C_u\right)$ captures these dependences, where a technology independent "speed factor" η is introduced to model the loading effects as a function of the conversion speed.† The value of this "speed factor" varies between 0 and 1 in this analysis by observing the following facts:

- When conversion speed is low, the loading due to parasitics is insignificant and the residue amplifier is mainly loaded by the sampling capacitors. This indicates a small "speed factor", hence η is set to 0 for this scenario;
- When conversion speed is high, the parasitic-loading effect is severe. If a specific technology is given, an exact relationship between η and the sampling rate can be derived. To make this analysis more general and technology independent, the maximum parasitic capacitance is set to equal

† This "speed factor" essentially stands for the ratio of the total parasitic capacitance to the total sampling capacitance ($2^n \gamma_i C_u$) of a certain pipeline stage.

the total sampling capacitance, i.e., $C_o \approx C_g \approx 2^n \gamma_i C_u$ or $\eta = 1$.

Note that we assumed $C_o \approx C_g$ in this analysis, which is approximate to make the algebra simpler. A full-length treatment would of course introduce two speed factors, one for C_o and one for C_g.

2.3.3 STAGE-SCALING ANALYSIS REVISITED

In Figure 2.3, a feedforward factor can be defined as

$$\alpha = \frac{C_s}{C_s + C_f + C_g} = \frac{1}{1+\eta}\left(1 - \frac{1}{2^n}\right), \tag{2.3}$$

and a feedback factor as

$$\beta = \frac{C_f}{C_s + C_f + C_g} = \frac{1}{1+\eta} \cdot \frac{1}{2^n}. \tag{2.4}$$

Assuming a first-order frequency response, the g_m noise floor at the output of the stage *i*-1 is $\left(\frac{1}{\beta}\right)^2 4kT\frac{N_{op}}{g_m}$, where N_{op} is the "noise factor" of the amplifier. In a single-ended amplifier, if the input transistor is the only noise contributor, then $N_{op} = 2/3$ holds for long-channel devices. However, for short-channel devices, the "noise factor" can be substantially greater than $2/3$.[14, 15] Furthermore, other devices in a complicated amplifier also contribute noise. E.g., in a one-stage folded-cascode amplifier, the current sources generate noise at the output equally

as the input devices do; the cascode devices' noise, albeit suppressed at low frequencies, contribute substantially at high frequencies. In a two-stage amplifier, the input devices of the second stage also produce noise at the output. In this analysis, we assume $N_{op} = 3$ for single-ended amplifiers.

The noise transfer functions of the switches r_1 through r_4 can be calculated individually. As the switch noises are band-limited by the amplifier, their contribution is reduced compared to the scenario where the circuit bandwidth is only determined by the lowpass filter formed by the switch and the sampling capacitors. The exact solution, taking into account the effect of the switch resistance on the frequency response, is quite involved. Instead of an accurate account of these second-order effects, the total noise floor at the output of the stage *i*-1 is approximated as

$$N_i(f) = 4kT \cdot \left[\left(\frac{1}{\beta} \right)^2 \frac{N_{op}}{g_m} + \left(\frac{\alpha}{\beta} \right)^2 r_1 + r_2 + (r_3 + r_4) \right], \tag{2.5}$$

where the first term stems from the amplifier noise and the rest from the switches. The frequency response is assumed first-order, band-limited by the closed-loop bandwidth (ω_{-3dB}) of the residue amplifier. In addition, the switches are sized such that they will not limit the settling speed of the amplifier. For this reason, assume

$$r_1 C_s, r_2 C_f, (r_3 + r_4) C_L \le \frac{1}{5} \frac{1}{\omega_{-3dB}} = \frac{1}{5} \frac{C_T}{\beta \cdot g_m}, \tag{2.6}$$

where C_T is the total output load capacitance of the residue amplifier given by

$$C_T = \left[1 - \frac{1}{(1+\eta) \cdot 2^n} + \eta \cdot 2^n \right] \gamma_{i-1} C_u + 2^n \gamma_i C_u. \tag{2.7}$$

Combining (2.5) and (2.6), we have

$$N_i(f) = \frac{4kT}{5g_m} \cdot \left[\frac{5N_{op}}{\beta^2} + \left(\frac{\alpha}{\beta} \right)^2 \frac{C_T}{\beta C_s} + \frac{C_T}{\beta C_f} + \frac{C_T}{\beta C_L} \right]. \tag{2.8}$$

The input-referred integrated noise sampled by the stage *i* is

$$N_i = \frac{1}{\left(4^n\right)^{i-1}} \left[\frac{\pi}{2} N_i(f) BW \right] = \frac{1}{\left(4^n\right)^{i-1}} \frac{kT}{5C_u} \cdot \left[\frac{(1+\eta) 2^n 5N_{op}}{C_T / C_u} + \frac{2^n}{\gamma_{i-1}} + \frac{1}{2^n \gamma_i} \right]. \tag{2.9}$$

If a uniform scaling is assumed, i.e., $\gamma_i = \gamma^{i-1}$ for $i = 1, \cdots, \infty$, $\sum_i N_i$ is summable for $\gamma > 1/4^n$ and is given by

$$\sum_{i=1}^{\infty} N_i = \frac{kT}{2^n C_u} + \frac{kT}{5C_u} \left(\frac{1}{4^n \gamma - 1} \right) \left[\frac{(1+\eta) \cdot 2^n \gamma \cdot 5N_{op}}{1 - \frac{1}{(1+\eta) \cdot 2^n} + \eta \cdot 2^n + 2^n \gamma} + 2^n \gamma + \frac{1}{2^n} \right], \tag{2.10}$$

where the first term $\frac{kT}{2^n C_u}$ represents the noise of the front-end S/H circuit as no SHA is assumed.

In addition, if slewing is ignored, the settling speed is determined by the small-signal closed-loop bandwidth (ω_{-3dB}) of the residue amplifier. The total conversion power can be derived as

$$P \propto SNR \cdot kT \cdot f_s \cdot \left(\frac{V_{gs} - V_{th}}{V_{dd}} \right) \cdot g(n, \gamma, \eta), \tag{2.11}$$

where f_s is the sampling rate, $V_{gs} - V_{th}$ is the overdrive voltage of the amplifier input transistor, and V_{dd} is the supply voltage. Function $g(.)$ is given by

$$g(n,\gamma,\eta) = \left(\frac{1+\eta}{1-\gamma} \right) \left(2^n - \frac{1}{1+\eta} + \eta \cdot 4^n + 4^n \gamma \right) \cdot \left\{ \frac{1}{2^n} + \frac{1/5}{4^n \gamma - 1} \left[\frac{(1+\eta) \cdot 4^n \gamma \cdot 5N_{op}}{2^n - \frac{1}{1+\eta} + \eta \cdot 4^n + 4^n \gamma} + 2^n \gamma + \frac{1}{2^n} \right] \right\}. \tag{2.12}$$

2.3.4 SUMMARY

Equation (2.11) supports the widely known result of (2.2) with an addition of the new $g(n,\gamma,\eta)$ function, which captures the dependence of the overall power consumption of a pipeline ADC on the per-stage resolution *n*, the scaling factor γ, and the speed factor η. For a given speed factor, minimizing this function yields the optimum stage resolution and scaling factor at the same time.

2.3.4.1 SPEED FACTOR

In Figure 2.4, the function $g(.)$ is plotted against the scaling factor γ for a per-stage resolution $n = 1\ldots5$ and a speed factor $\eta = 0$, 0.5, and 1. The plot indicates a significant impact of the speed factor on the optimum stage resolution and the minimum power consumption.

For a small η, or a low conversion speed, the model predicts the same dependency between the stage resolution and the power consumption as the Cline-Gray model does – a higher per-stage resolution always results in a lower total power consumption for a fixed resolution (the leftmost plot of Figure 2.4).

When η approaches one, i.e., for high conversion speeds, the amplifier is

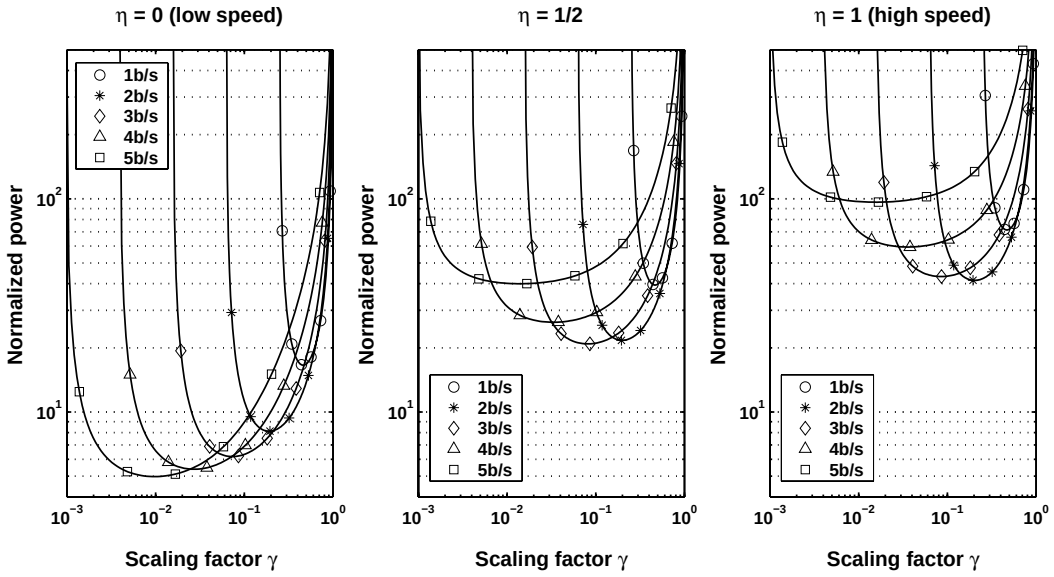

Figure 2.4 Evaluation of $g(n,\gamma,\eta)$ versus the scaling factor γ.

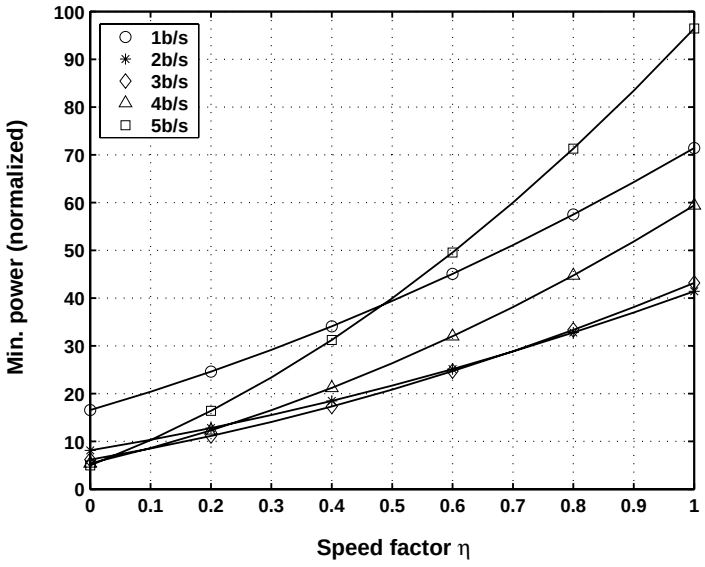

Figure 2.5 Evaluation of $g(n,\gamma,\eta)$ versus the speed factor η.

increasingly loaded by parasitics. The total power consumption rises collectively regardless of the stage resolution as expected. However, high per-stage resolution architectures exhibit a higher sensitivity to the speed factor in that their minimum power rises much faster when n exceeds 3-b/s (the middle and the right plots of Figure 2.4). The optimum resolution is 2- or 3-b/s for a pipeline converter operating at these speeds. This is the typical scenario encountered in a practical design.

The above conclusion is better observed in Figure 2.5, where the minimum power consumption is plotted against the speed factor for $n = 1\ldots5$.

2.3.4.2 TAPER FACTOR

A "taper factor" x was defined in the Cline-Gray model, which relates to the

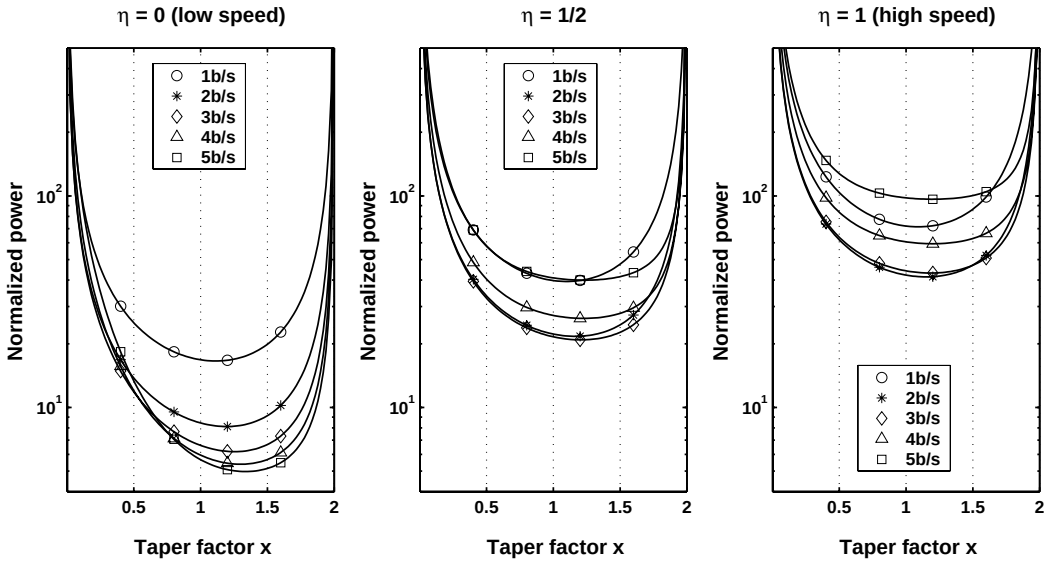

Figure 2.6 Evaluation of $g(n,\gamma,\eta)$ versus the taper factor x.

scaling factor by the equation $\gamma = \frac{1}{2^{nx}}$. One important observation drawn by the Cline-Gray model was that the optimum scaling factor γ_{opt} is approximately equal to the inter-stage voltage gain of the pipeline.[11] In other words, the optimum taper factor x_{opt} is approximately one.

This observation is confirmed by Figure 2.6, where the power is plotted against the taper factor x. The optimum taper factor for any per-stage resolution is slightly greater than one regardless of the speed factor (varying from 0 to 1). To better observe this, x_{opt} is plotted against the stage-resolution for different speed factors in Figure 2.7.

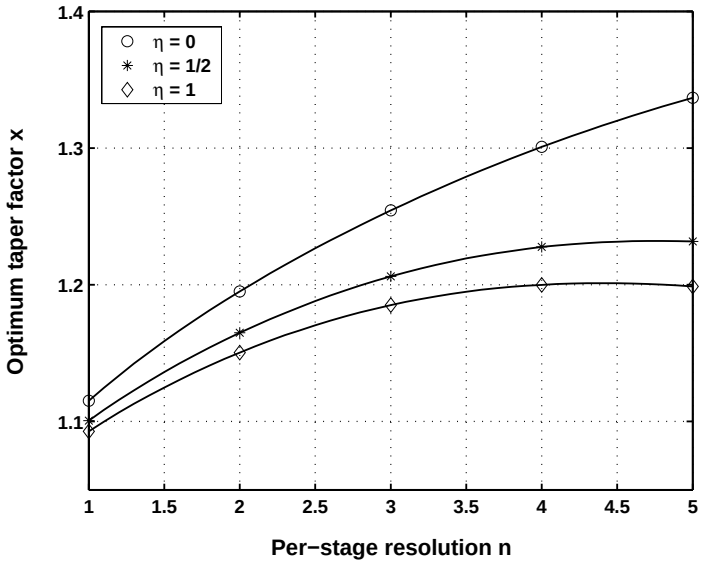

Figure 2.7 Evaluation of γ_{opt} versus the stage resolution n.

The optimum taper factor is a weak function of the stage resolution, and this statement is increasingly accurate for higher conversion speeds (indicated by the flat right half of the curves in Figure 2.7. The plot also points out that the optimum taper factor is neither a strong function of the speed factor. These observations are probably justified by the fact that the speed factor influences all stages uniformly and the inter-stage gain remains constant for a given n.

The summary serves as guideline for pipeline ADC designs when the trade-off between SNR and power consumption is critical. Note that the derivation does not include the SHA noise if one is used. The uniform scaling factor throughout the pipeline may not be practical due to an increased layout effort. In addition, scaling of the last few pipeline stages may be difficult when they become too small. Lastly, although a uniform per-stage resolution helps to keep a design modular,

increasing the resolution of the backend stages (a non-uniform scaling essentially) may result in more power savings.

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Chapter 3 _____

CAPACITOR ERROR-AVERAGING

In Chapter 2, we discussed the fundamental trade-off between the achievable $\frac{kT}{C}$ noise level and the power consumption of a pipeline ADC. A revised pipeline stage-scaling algorithm was introduced that optimizes the conversion power given the target SNR specification.

In practice, however, the performance of a high-speed, high-accuracy pipeline ADC is also limited by other device or circuit non-idealities that degrade the fidelity of the digitization process – often manifested as nonlinearities and memory effects. Depending on application, the distortion artifact can sometimes be more harmful than an additive white noise.

In this chapter, a discussion of the pipeline ADC error mechanism is presented, followed by a brief review of the previous precision conversion techniques. Upon analyzing the pros and cons of these prior arts, the discussion gradually develops

a focus on the capacitor error-averaging technique – an inherently linear pipeline A/D conversion scheme. The shortcomings of an earlier averaging approach are discussed in details, and then a new technique – the passive capacitor error-averaging – is introduced. Quantitative comparisons using both analytical methods and a Monte Carlo computer simulation are included toward the end of the chapter.

3.1 PIPELINE ADC ERROR MECHANISM

Although a pipeline ADC makes use of considerable amount of digital logic, most of its signal-processing functions are executed in the analog domain. The conversion process therefore is susceptible to analog circuit and device impairments. As pointed out in Chapter 2, as the quantization takes a divide-and-conquer approach, the requirements on the comparators are greatly relaxed compared to that of a flash-type converter. The conversion accuracy is solely determined by the residue transfer accuracy.

Static non-idealities that affect the residue accuracy include the sampling capacitor mismatch, finite amplifier gain, and switch-induced charge injection errors. The capacitor mismatch and finite amplifier gain effect can be readily evaluated by inspecting the voltage transfer characteristic obtained for the circuit shown in Figure 2.2 of a 1.5-b/s pipeline ADC:

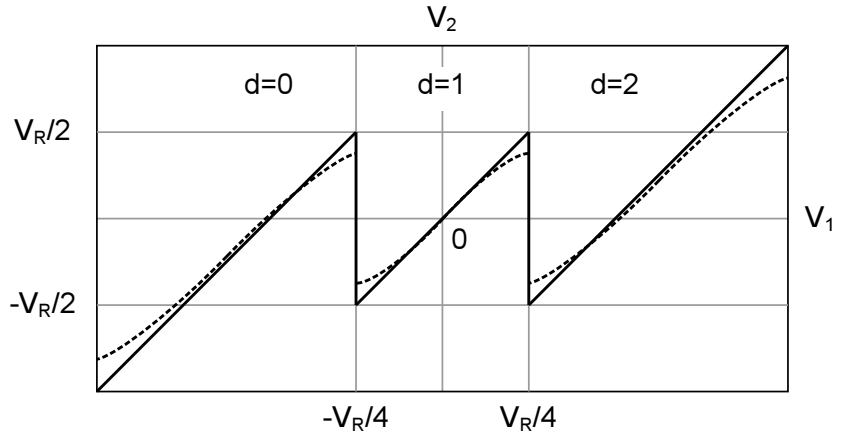

Figure 3.1 Voltage transfer characteristic of a 1.5-b/s residue gain stage. The solid curve shows the ideal transfer function and the dashed one exhibits static nonlinearity due to analog circuit non-idealities.

$$V_2 = \frac{V_1(C_1 + C_2) - (d-1)\cdot V_{REF} C_2 + V_{os}(C_1 + C_2)}{C_1 + \dfrac{C_1 + C_2}{A(V_2)}}, \tag{3.1}$$

where V_{os} is the offset voltage of the amplifier. These errors effect a nonlinear residue transfer function as indicated in Figure 3.1.

In addition to static errors, finite circuit bandwidth limits the tracking speed hence the accuracy of the front-end track-and-hold (T/H) circuit. The same issue exists for the residue amplifier as well. On the other hand, the dynamic errors of the comparators include hysteresis and metastability, although neither affects the conversion accuracy of a pipeline converter as harmfully as they do to a flash converter.[1, 2]

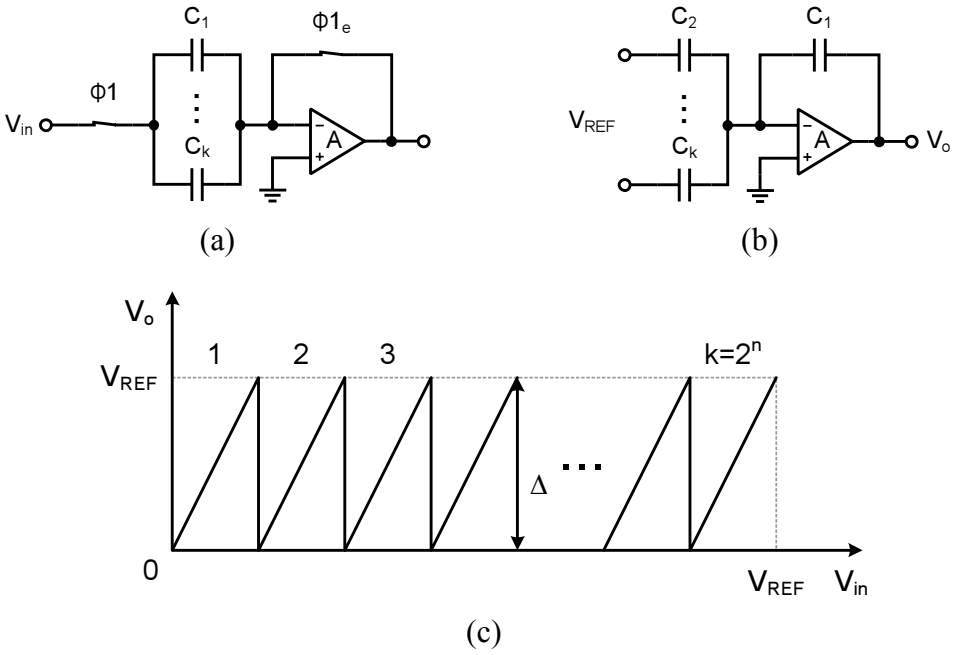

Figure 3.2 Circuit diagram of an *n*-b/s pipeline ADC and its residue transfer characteristic. (a) Sampling mode. (b) Amplification mode.

3.2 CAPACITOR MATCHING ACCURACY

Among the static conversion nonlinearities, the capacitor mismatch – a random error due to the imperfection of the manufacture process – is the one mostly discussed in the literature. In a fully optimized pipeline ADC, random capacitor mismatch is often the most important error source of nonlinearity. In the absence of a post-fabrication component trimming or calibration, the conversion accuracy is usually limited to approximately 10-12 bits.

To understand how exactly the capacitor mismatch affects the conversion linearity, specifically DNL and INL, we consider the *n*-b/s, *N*-bit pipeline ADC

shown in Figure 3.2. A single-ended circuit diagram is shown for simplicity.

The circuit operates on a two-phase clock. In $\phi 1$, all k ($=2^n$) capacitors are connected together to the input; in $\phi 2$, C_1 is switched to the feedback path and the rest of the capacitors act as an n-bit DAC by switching the top plates to either ground or V_{REF} according to the comparison outcome. The transfer characteristic of the stage consists of k segments spanning between 0 and V_{REF}. Ideally, the end points of each segment should precisely land at 0 and V_{REF} if all circuit elements are ideal and all segmental transitions (Δ's in Figure 3.2) should be exactly V_{REF}.

Now let's study the capacitor mismatch effect alone by setting the amplifier gain to infinite and nullifying all offset errors. In the Appendix, the matching accuracy required to achieve N-bit linearity is calculated. The important conclusions are as follows:

- DNL is a direct result of the mismatch error between adjacent capacitors in the MDAC. This error is not carried over from segment to segment;
- INL is the result of the cumulative mismatch error of all sampling capacitors, albeit the first i capacitors have a more severe impact on the linearity for the i^{th} segment. Therefore the INL is more susceptible to the mismatch errors among the capacitors.

In Figure 3.3, the MDAC capacitor matching accuracy as a function of the stage resolution of a 14-b pipeline ADC is plotted as an example. Indeed, the

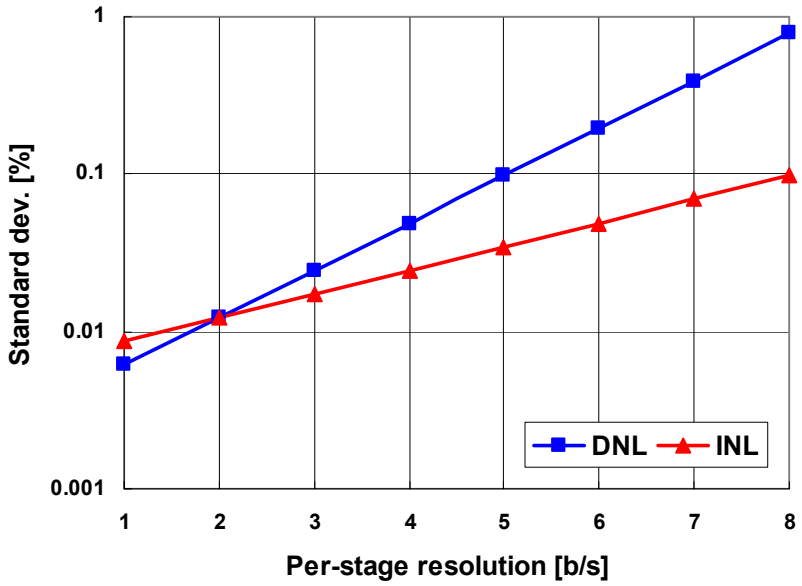

Figure 3.3 Capacitor matching accuracy versus stage resolution for a 14-bit pipeline ADC. A half LSB maximum DNL and INL error is assumed.

matching accuracy is gradually relaxed by placing more bits in the front-end stage. Quite a few works in the literature exploit this fact.[3-8] As studied in Chapter 2, the penalty of this approach, however, is a much degraded power efficiency when the stage resolution is pushed over 3-4-b/s. In the next section, conversion techniques that do not require matched capacitors will be discussed.

3.3 Precision Conversion Techniques

To combat the mismatch error, ratio-independent voltage multiplication techniques were invented in the 80's and 90's. Although most of these techniques are discussed in the context of an algorithmic (also called cyclic) A/D converter,

they often can be applied to the pipeline architecture with little modification.[9-12]

Most of the ratio-independent techniques rely on sampling an input or residue voltage on the same capacitor multiple times to achieve an accurate multiply-by-*n* function that is immune to capacitor matching errors. The techniques often involve a second capacitor acting as the temporary storage of the intermediate charge. The penalty associated with this is the extra time required to process the signal, which inevitably impacts the conversion speed.

A few techniques that reduce this timing overhead deserve to be mentioned here. The first implements an exact multiplication by four with two clock cycles in a 1.5-b/cycle algorithmic ADC.[11] The scheme takes advantage of the fact that an algorithmic ADC makes use of the same circuit cyclically. By alternating the roles of two capacitors as the sampling and feedback capacitors, the residue gain error is inverted every other iteration, which results in a complete error cancellation for every two consecutive bits. However, this two-cycle error cancellation is only possible with an algorithmic ADC, where the gain error is constant each time the residue voltage circulates around the loop. The second is a capacitor error-averaging (CEA) technique that is well suited for a pipelined implementation.[13, 14, 15] This scheme exhibits inherent linearity even in the presence of large capacitor mismatch errors, and will be discussed in more details in the following sections. The third technique implements a mismatch-

independent DNL architecture, which in essence is a decision code-weighted capacitor ratio selection algorithm. However, the INL of this architecture still relies on the capacitor matching accuracy.[16, 17, 18]

In the late 80's and 90's, the pipeline ADCs using a power-on or background digital capacitor trimming or calibration technique have become increasingly popular. Since the conversion linearity is not inherent, the performance sensitivity to temperature and supply voltage drift, component aging has been problematic for these types of converters. The power consumption and silicon area of the logic circuitry have been important metrics in evaluating the performance and complexity of the digital techniques until recently, when the advancement of the CMOS technology scaling made the digital transistors abundantly available to circuit designers in a cost-effective way. Many sophisticated digital signal-processing algorithms now can be assembled in a small silicon area in these deep-submicron processes with relatively small power overhead. This is especially advantageous in a system-on-a-chip (SoC) design, where large amount of digital circuits share the same die with the front-end analog circuits.

3.3.1 ACTIVE CAPACITOR ERROR-AVERAGING

As mentioned in the last section, one approach to treat mismatch error is the capacitor error-averaging. For a 1-b/s pipeline architecture, the error correction is performed by interchanging the roles of two sampling capacitors during the

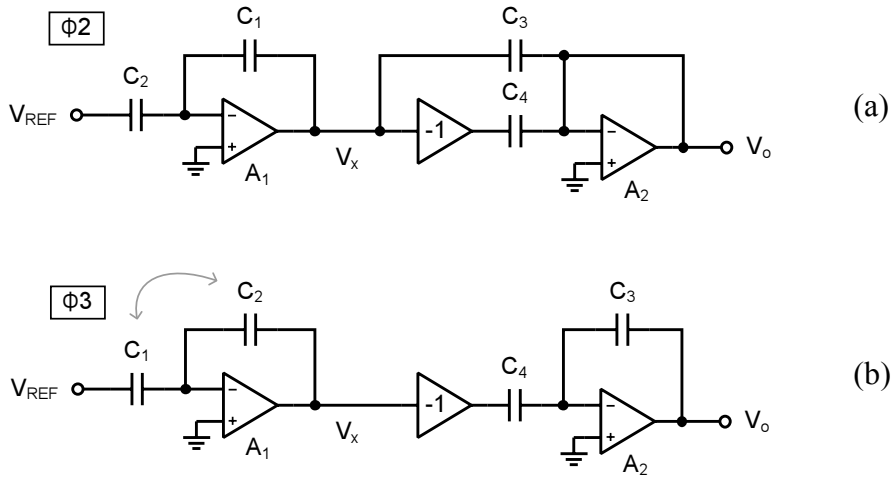

Figure 3.4 Circuit diagram of the active CEA technique. The stage operates on a three-phase clock. $\phi 1$ is the sampling phase (not shown). $\phi 2$ and $\phi 3$ are the amplification phases shown in (a) and (b), respectively.

amplification phases (Figure 3.4). Two residue voltages that contain complementary errors are generated consecutively. A second amplifier and two extra capacitors are used to obtain the average of the residue voltage pair (hence the name "active"). The gain-of-minus one block is implemented by simply cross-connecting the differential signals. It has been shown that the first order gain error resulted from capacitor mismatch is removed by averaging.[13, 15]

The active CEA technique is capable of realizing an excellent linearity with poorly matched capacitors. However, this is achieved at the cost of an added circuit complexity and more power consumption due to the residue resampling process. Assuming the averaging amplifier generates an equal amount of noise while draining the same current as the residue amplifier, the approach leads to a

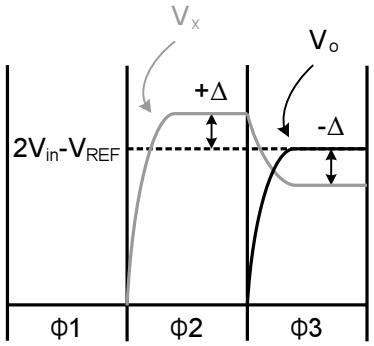

Figure 3.5 Voltage waveforms of the active CEA gain stage of Figure 3.4.

four times power and area increase for the same SNR compared to the conventional architecture. Moreover, the averaging amplifier and the residue resampling process impose additional nonlinearities on the signal path, compromising the overall linearity of the converter.

3.3.2 PASSIVE CAPACITOR ERROR-AVERAGING – PART I

The essence of the CEA technique is to generate a residue voltage pair that contain complementary gain errors, and then average them to obtain an accurate multiply-by-two function. However, the averaging operation using an additional amplifier is extravagant. The pipeline nature of the conversion renders the opportunity to exploit the sampling capacitors from the trailing stages to realize the averaging function without the resampling of the residue voltages.[14] This section describes the first realization of this technique.

The new approach is illustrated in Figure 3.6. The sampling capacitors C_1 and C_2 are split in half into C_1' and C_1'', C_2' and C_2''. The stage operates on a four-phase clock. $\phi 1$ and $\phi 2$ are the sampling phases (not shown in the figure). $\phi 3$ and $\phi 4$ are

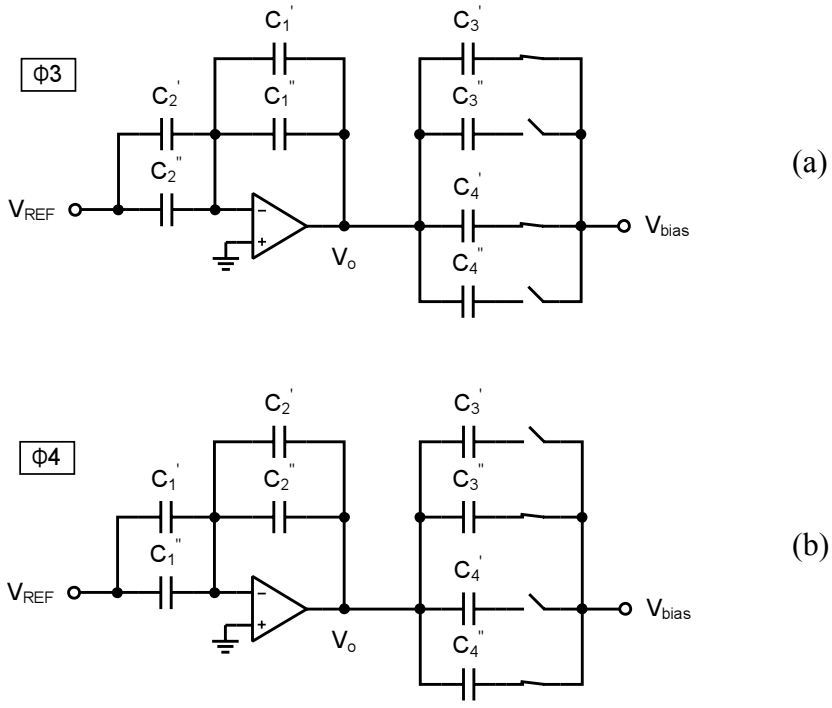

Figure 3.6 Circuit diagram of the passive CEA technique (I). C_1 and C_2 are the sampling capacitors of the current pipeline stage, while C_3 and C_4 are from the trailing stage.

the amplification phases.

Assuming that the previous pipeline stage produces a residue voltage pair $V_{in}^{'}$ and $V_{in}^{"}$, $C_1^{'}$ and $C_2^{'}$ are used to sample the first residue voltage ($V_{in}^{'}$) in $\phi 1$, and then $C_1^{"}$ and $C_2^{"}$ are used to sample the second one ($V_{in}^{"}$) in $\phi 2$. The two samples acquired in tandem are then merged by the two split capacitors in the following amplification phases ($\phi 3$ and $\phi 4$). The charge sharing between the half capacitors therefore performs the error-averaging function on the fly while the output residue is produced. No extra amplifier is required to explicitly produce an averaged

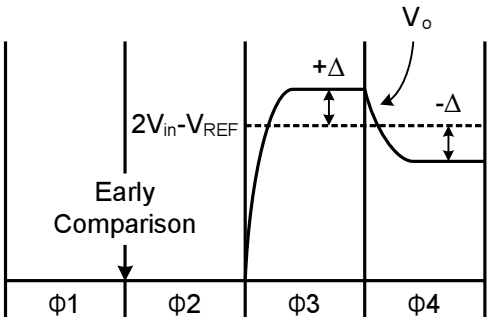

Figure 3.7 Voltage waveforms of the passive CEA gain stages of Figure 3.6 and Figure 3.8.

output voltage as compared to the active CEA approach – hence the name "passive" CEA. The operation of double sampling and double amplification is repeated by each stage of the pipeline ADC. The double sampling of the input voltage is not required in the first stage.

Assuming that the input residues are complementary, the output residues produced in $\phi 3$ and $\phi 4$ are calculated in the Appendix. Equation (3.24) shows that all of the first-order gain error terms in the output residue expression stem from the current stage; the mismatch errors from the previous stage are reduced to the second order after averaging. Interestingly, the first-order gain error terms remain complementary.

One side advantage of producing two residue voltages instead one is that it allows more comparator settling time if an early comparison approach is used.[14, 15] This is indicated in Figure 3.7 by the arrow in between $\phi 1$ and $\phi 2$, where the first residue is compared against the reference thresholds. With this approach, the comparator settling time is as long as one quarter of the clock period as opposed

to just the non-overlapping time between the two phases (ϕ1 and ϕ2) for the conventional architecture.

3.3.3 PASSIVE CAPACITOR ERROR-AVERAGING – PART II

Another circuit architecture that equally performs the passive averaging technique is shown in Figure 3.8. Each residue gain stage consists of one amplifier and two capacitors similar to that of a conventional 1.5-b/s architecture. The timing diagram of this approach is shown in Figure 3.7. The circuit operates as follows. In ϕ1 and ϕ2, the complementary input voltage pair ($V_{in}^{'}$ and $V_{in}^{''}$) produced by the previous stage is sampled by C_1 and C_2, respectively. During ϕ3 and ϕ4, two output residue voltages ($V_o^{'}$ and $V_o^{''}$) are generated by swapping the positions of C_1 and C_2, followed by the sampling by C_3 and C_4 from the trailing stage, respectively.[14] The charge averaging is performed on the fly in this circuit, which

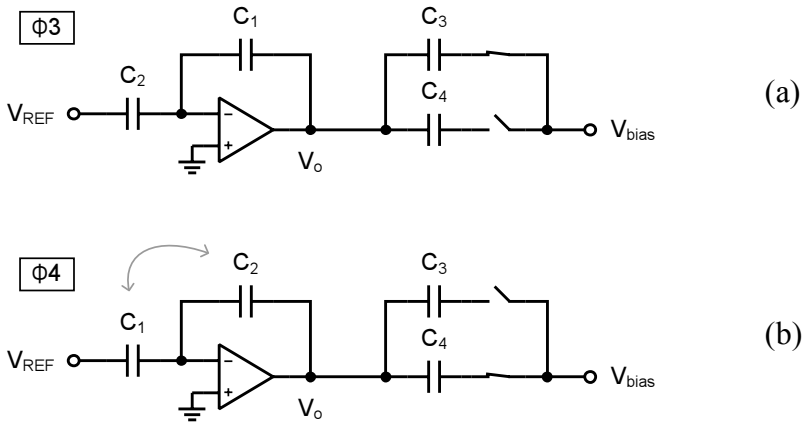

Figure 3.8 Circuit diagram of the passive CEA technique (II). Here C_3 and C_4 are also the sampling capacitors from the trailing stage.

Table 3.1 Averaging effects of CEA techniques

Architecture (1.5-b/s)	Conventional	Active CEA	Passive CEA (I)	Passive CEA (II)
E(ε)	0	σ^2	$0.5\sigma^2$	σ^2
Var(ε)	σ^2	$3.75\sigma^4$	σ^4	$3\sigma^4$

is identical to the first approach. Again, no explicitly averaged residue voltage is produced and no averaging amplifier and capacitors are required.

The comparison between the averaging effects of the passive and active CEA techniques are calculated in the Appendix and summarized in Table 3.1.

3.3.4 POWER EFFICIENCY

Both of the passive CEA techniques discussed in the previous two sections are more power-efficient averaging approaches compared to the active one. Avoiding the residue resampling process reduces the total conversion power by a factor of four. In addition, the uncorrelated noise in two separately acquired residue samples further increases the SNR by three decibels. Furthermore, the loading of the residue amplifier is reduced because only half of the sampling capacitance switches on during either one of the sampling phases.

A limitation of the passive CEA technique is that it takes four clock phases to complete the sampling-comparison-amplification process, in contrast to two for a conventional implementation with no averaging, or three for the active CEA.

Table 3.2 ADC architecture power efficiency

Architecture (1.5-b/s)	Conventional	Active CEA	Passive CEA
Averaging	No	Yes	Yes
Power	1	4	1/2
Speed	1	2/3	1/2
Power/speed	1	6	1

Table 3.2 summarizes the power-saving results of the new approaches. For the same target SNR, the power efficiency is defined by normalizing the total conversion power to the sampling rate. It follows that the passive CEA approach is as efficient as the conventional technique, and six times more efficient than the active approach.

3.3.5 MONTE CARLO SIMULATION

A MATLAB behavioral model of the new averaging technique was constructed. A 1.5-b/s, 14-b pipeline ADC using the passive CEA (II) approach was evaluated. Various circuit non-idealities –sampling capacitor mismatch, amplifier finite gain effect, comparator and amplifier offset – were considered in the simulation. As the averaging reduces the matching requirement quadratically, it is expected that an n-bit capacitor matching accuracy is adequate to achieve a $2n$-bit INL.

The results of the Monte Carlo yield simulation are summarized in Table 3.3. A Gaussian distribution is assumed for all circuit parameters except the amplifier

Table 3.3 Monte Carlo simulation results of a 14-b pipeline ADC

Simulation results	$INL_{p\text{-}p}$ (median)	$DNL_{p\text{-}p}$ (median)	ENOB (median)	Yield (|INL| ≤0.5LSB)
Case I	0.501 LSB	0.500 LSB	13.92 bits	96%
Case II	0.891 LSB	0.625 LSB	13.89 bits	66%

Table 3.4 Circuit parameters used in Monte Carlo simulation

Circuit parameters	Capacitor matching (3σ)	Comparator offset (3σ)	Amplifier DC-gain (fixed)
Case I	6 bits	0.1 V_{FS}	100 dB
Case II	7 bits	0.1 V_{FS}	90 dB

gain that is fixed (Table 3.4). The INL and the DNL results were obtained using a code density simulation and the effective-number-of-bits (ENOB) figure was calculated from the signal-to-noise plus distortion ratio (SNDR) value obtained through a fast Fourier transform.

Note that two scenarios were compared in the simulation. In the first case, a 6-bit capacitor matching accuracy was assumed with a large amplifier gain (100 dB). The capacitor mismatch error is expected to be the dominant source of nonlinearity. The results of a total of 96 runs (out of 100) exhibited an INL less or equal to ±0.5 LSB. A lower amplifier gain of 90 dB was assumed in the second case, which is about the minimum value typically required by a 14-bit ADC. A 66% yield (|INL| ≤0.5LSB) was obtained with a 7-bit capacitor matching accuracy.

The INL and DNL histograms of the first scenario are shown in Figure 3.9.

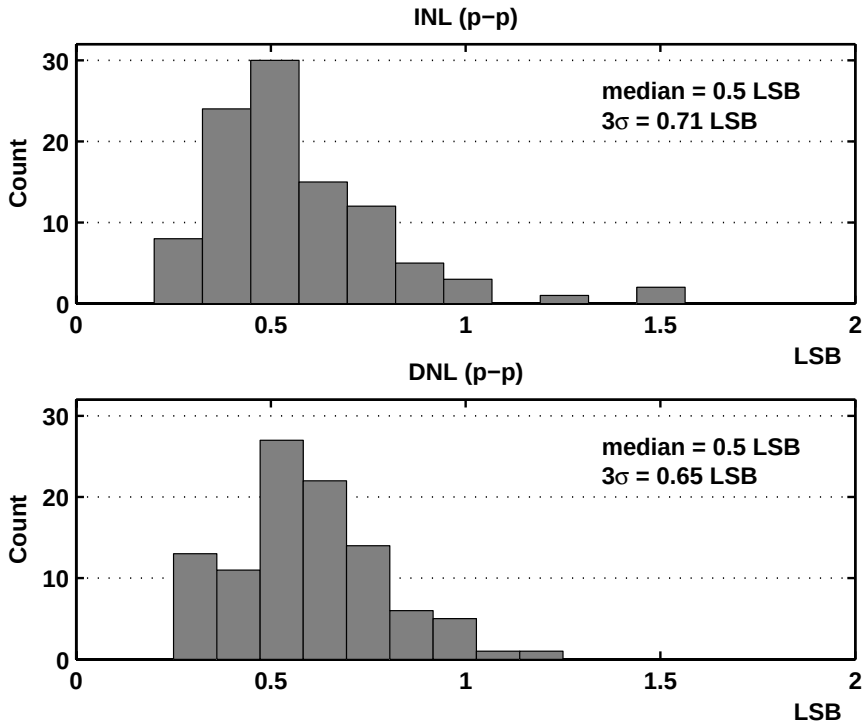

Figure 3.9 Results of the Monte Carlo yield simulation. 14-bit INL and DNL are achieved with a 6-bit capacitor matching accuracy (3σ). Amplifier gain is assumed to be large (100 dB).

APPENDIX

A3.1 MDAC Capacitor Matching

In the transfer curve of the *n*-b/s MDAC shown in Figure 3.3, assume the input resides in the i^{th} segment, balance the charge transfer and we have

$$V_o = V_{in} \cdot \left(\frac{C_1 + C_2 + ... + C_k}{C_1} \right) - V_{REF} \cdot \left(\frac{C_2 + ... + C_i}{C_1} \right). \tag{3.2}$$

When matching is perfect, (3.2) becomes

$$V_o = V_{in} \cdot 2^n - V_{REF} \cdot (i-1). \tag{3.3}$$

Now we inspect the segmental transition between the i-1^{th} and the i^{th} segment, i.e., let $V_{in} = \frac{i-1}{k} \cdot V_{REF}$, we have

$$\begin{aligned} V_o^{\,i-1} &= V_{REF} \cdot \left(\frac{i-1}{k} \cdot \frac{C_1 + C_2 + ... + C_k}{C_1} - \frac{C_2 + ... + C_{i-1}}{C_1} \right), \\ V_o^{\,i} &= V_{REF} \cdot \left(\frac{i-1}{k} \cdot \frac{C_1 + C_2 + ... + C_k}{C_1} - \frac{C_2 + ... + C_{i-1} + C_i}{C_1} \right). \end{aligned} \tag{3.4}$$

The difference between $V_o^{\,i-1}$ and $V_o^{\,i}$ should ideally be V_{REF}. The relative deviation is a measure of the differential nonlinearity:

$$\begin{aligned} V_o^{\,i-1} - V_o^{\,i} &= V_{REF} \cdot \frac{C_i}{C_1} \\ &= V_{REF} \cdot (1 + \Delta_i), \end{aligned} \tag{3.5}$$

where we assumed $C_i = C_1 \cdot (1 + \Delta_i)$. For an *N*-bit resolution, this deviation should be no larger than one half LSB, i.e., $\frac{V_o^{i-1} - V_o^{i}}{V_{REF}} \le \frac{1}{2^{N-n+1}}$, so we have

$$\Delta_i \le 1/2^{N-n+1}. \tag{3.6}$$

The derivation of the INL is more involved as the absolute voltage deviation from the ideal value needs to be considered. Let $V_{in} = \frac{i}{k} \cdot V_{REF}$, we have:

$$\begin{aligned} \frac{V_o^{i} - V_{REF}}{V_{REF}} &= \frac{i}{k} \cdot \frac{C_1 + C_2 + \ldots + C_k}{C_1} - \frac{C_2 + \ldots + C_i}{C_1} - 1 \\ &= \frac{i}{k} \cdot \left(k + \sum_{j=2}^{k} \Delta_j \right) - (i-1) - \sum_{j=2}^{i} \Delta_j - 1 \\ &= \frac{i}{2^n} \cdot \sum_{j=2}^{2^n} \Delta_j - \sum_{j=2}^{i} \Delta_j . \end{aligned} \tag{3.7}$$

Note that the INL is determined by the cumulative mismatch of all capacitors in the MDAC, with the first *i* capacitors – the second term in (3.7) – heavily weighted for the i^{th} segment. When *i* is small, not many Δ's contribute so the INL error is not great; interestingly, when *i* approaches $k = 2^n$, the correlation between the first and the second term in (3.7) dramatically increases, which also leads to a small INL when the input is close to the full scale. To derive the maximum INL as a function of *i*, we first need to obtain the mean and the variance of the cumulative error of (3.7). Assume that all Δ's are uncorrelated and

exhibit the same statistics with zero mean and variance σ^2, we have

$$E\left(\frac{V_o^{\,i}-V_{REF}}{V_{REF}}\right)=0,\quad Var\left(\frac{V_o^{\,i}-V_{REF}}{V_{REF}}\right)=\sigma^2\left(i-\frac{i^2}{2^n}\right). \tag{3.8}$$

Now set the derivative of the variance with respect to i to zero, solve for i:

$$i_{\max}=2^{n-1},\quad Var\left(INL_{\max}\right)=2^{n-2}\sigma^2. \tag{3.9}$$

So the maximum INL error occurs at the midpoint of the transfer curve. To achieve a half LSB maximum INL, we need

$$\sigma \le {}^{1}\!\Big/\!_{2^{N-\frac{n}{2}}}. \tag{3.10}$$

A3.2 Active CEA

In Figure 3.4, assume the following matching conditions:

$$C_1=C(1+\delta_1),\quad C_2=C(1+\delta_2),\quad C_3=2C(1+\delta_3),\quad C_4=C(1+\delta_4), \tag{3.11}$$

where δ_1, δ_2, δ_3, δ_4 are independent Gaussian random variables of the relative mismatch errors with zero mean and variance σ^2, C is the nominal capacitance.

During ϕ_2, balance the charge sampled on C_3 and C_4, we have

$$\sum Q_2=\frac{(C_1+C_2)\cdot V_{in}-C_2\cdot V_{REF}}{C_1}\cdot(C_3-C_4), \tag{3.12}$$

where $\sum Q_2$ is the total charge sampled on the top plates of C_3 and C_4, V_{in} is the

input voltage sampled on C_1 and C_2 in ϕ_1. Repeat this for ϕ_3, we have

$$\sum Q_3 = V_o \cdot C_3 - \frac{(C_1 + C_2)\cdot V_{in} - C_1 \cdot V_{REF}}{C_2} \cdot C_4, \tag{3.13}$$

where V_o is the output residue voltage produced by the averaging amplifier in ϕ_3. Apply the charge conservation law, let $\sum Q_2 = \sum Q_3$, solve for V_o :

$$V_o = V_{in}\left[1 + \frac{C_2}{C_1} + \left(\frac{C_1}{C_2} - \frac{C_2}{C_1}\right)\cdot\frac{C_4}{C_3}\right] - V_{REF}\left[\frac{C_2}{C_1} + \left(\frac{C_1}{C_2} - \frac{C_2}{C_1}\right)\cdot\frac{C_4}{C_3}\right]. \tag{3.14}$$

Now we approximate the capacitor ratios by a power series, keeping terms up to the second order:

$$\begin{aligned}
\frac{C_2}{C_1} &= 1 - \delta_1 + \delta_2 + \delta_1^{\,2} - \delta_1 \cdot \delta_2, \\
\frac{C_1}{C_2} &= 1 - \delta_2 + \delta_1 + \delta_2^{\,2} - \delta_1 \cdot \delta_2, \\
\frac{C_4}{C_3} &= \frac{1}{2}(1 - \delta_3 + \delta_4 + \delta_3^{\,2} - \delta_3 \cdot \delta_4),
\end{aligned} \tag{3.15}$$

Substitute into (3.14), we obtain the final output residue with the mismatch error:

$$V_o = (2V_{in} - V_{REF}) + \varepsilon \cdot (V_{in} - V_{REF}), \tag{3.16}$$

where $\varepsilon = \frac{1}{2}(\delta_1 - \delta_2)(\delta_1 - \delta_2 - 2\delta_3 + 2\delta_4)$. Finally, we have

$$E(\varepsilon) = \sigma^2, \quad Var(\varepsilon) = \frac{15}{4}\sigma^4. \tag{3.17}$$

A3.3 Passive CEA (I)

In Figure 3.6, assume the following matching conditions:

$$\begin{aligned} C_1^{'} &= \frac{C}{2}(1+\delta_1), \quad C_2^{'} = \frac{C}{2}(1+\delta_2), \\ C_1^{''} &= \frac{C}{2}(1+\delta_3), \quad C_2^{''} = \frac{C}{2}(1+\delta_4), \end{aligned} \tag{3.18}$$

where δ_1, δ_2, δ_3, δ_4 are defined the same way as in the active CEA case. In addition, assume the input residue voltage pair is complementary:

$$V_{in}^{'} = V_{in}(1+\Delta), \quad V_{in}^{''} = V_{in}(1-\Delta), \tag{3.19}$$

where Δ is a small quantity determined by the accuracy of the previous stage.

During ϕ_1 and ϕ_2, the total charge sampled on $C_1^{'}$ and $C_1^{''}$ is

$$\begin{aligned} \sum Q &= V_{in}^{'} \cdot C_1^{'} + V_{in}^{''} \cdot C_1^{''} \\ &= \frac{V_{in}C}{2} \cdot [2 + (\delta_1 + \delta_3) + \Delta(\delta_1 - \delta_3)]. \end{aligned} \tag{3.20}$$

The total charge sampled on $C_2^{'}$ and $C_2^{''}$ is

$$\sum Q_2 = \frac{V_{in}C}{2} \cdot [2 + (\delta_2 + \delta_4) + \Delta(\delta_2 - \delta_4)]. \tag{3.21}$$

Summing up the total charge on the four capacitors gives

$$\begin{aligned} \sum Q &= \sum Q_1 + \sum Q_2 \\ &= \frac{V_{in}C}{2} \cdot [4 + (\delta_1 + \delta_2 + \delta_3 + \delta_4) + \Delta(\delta_1 + \delta_2 - \delta_3 - \delta_4)]. \end{aligned} \tag{3.22}$$

Balance the charge transfer in ϕ_3 and ϕ_4, solve for $V_o^{'}$ and $V_o^{"}$:

$$\begin{aligned} V_o^{'} &= \frac{\sum Q - V_{REF} \cdot \left(C_2^{'} + C_2^{"}\right)}{C_1^{'} + C_1^{"}}, \\ V_o^{"} &= \frac{\sum Q - V_{REF} \cdot \left(C_1^{'} + C_1^{"}\right)}{C_2^{'} + C_2^{"}}. \end{aligned} \tag{3.23}$$

We have

$$\begin{aligned} V_o^{'} &= \left(2V_{in} - V_{REF}\right) - \lambda_1 \cdot \left(V_{in} - V_{REF}\right) + \lambda_2^{'} \cdot \left(V_{in} - V_{REF}\right) + \lambda_3 \cdot \Delta \cdot V_{in}, \\ V_o^{"} &= \left(2V_{in} - V_{REF}\right) + \lambda_1 \cdot \left(V_{in} - V_{REF}\right) + \lambda_2^{"} \cdot \left(V_{in} - V_{REF}\right) + \lambda_3 \cdot \Delta \cdot V_{in}, \end{aligned} \tag{3.24}$$

where

$$\begin{aligned} \lambda_1 &= \frac{1}{2}\left(\delta_1 + \delta_3 - \delta_2 - \delta_4\right), \\ \lambda_2^{'} &= \frac{1}{2}\left(\delta_1 + \delta_3\right) \cdot \left(\delta_1 + \delta_3 - \delta_2 - \delta_4\right), \\ \lambda_2^{"} &= \frac{1}{2}\left(\delta_2 + \delta_4\right) \cdot \left(\delta_2 + \delta_4 - \delta_1 - \delta_3\right), \\ \lambda_3 &= \frac{1}{2}\left(\delta_1 + \delta_2 - \delta_3 - \delta_4\right). \end{aligned} \tag{3.25}$$

Assume that $V_{in}^{'} = V_{in}^{"} = V_{in}$, which holds true for the first pipeline stage. Also assume the following matching conditions for the second stage:

$$C_3^{'} = \frac{C}{2}\left(1 + \delta_5\right), \quad C_3^{"} = \frac{C}{2}\left(1 + \delta_6\right), \tag{3.26}$$

where δ_5 and δ_6 are assumed to have the same statistics as that of δ_1, δ_2, δ_3, δ_4. When $V_o^{'}$ and $V_o^{"}$ are sampled by $C_3^{'}$ and $C_3^{"}$, respectively, an effective residue

voltage can be defined as

$$\begin{aligned} V_{o,eff} &= \frac{V_o^{'} \cdot C_3^{'} + V_0^{''} \cdot C_3^{''}}{C_3^{'} + C_3^{''}} \\ &= \left(2V_{in} - V_{REF}\right) + \varepsilon \cdot \left(V_{in} - V_{REF}\right), \end{aligned} \tag{3.27}$$

where $\varepsilon = \frac{1}{8}\left(\delta_1 + \delta_3 - \delta_2 - \delta_4\right) \cdot \left(\delta_1 + \delta_3 - \delta_2 - \delta_4 - 2\delta_5 + 2\delta_6\right)$. Finally, we have

$$E\left(\varepsilon\right) = \frac{\sigma^2}{2}, \quad Var\left(\varepsilon\right) = \sigma^4. \tag{3.28}$$

A3.4 Passive CEA (II)

In Figure 3.8, assume the following matching conditions:

$$C_1 = C\left(1 + \delta_1\right), \quad C_2 = C\left(1 + \delta_2\right), \quad C_3 = C\left(1 + \delta_3\right), \quad C_4 = C\left(1 + \delta_4\right), \tag{3.29}$$

where δ_1, δ_2, δ_3, δ_4 are defined the same way as in the previous cases. Again, assume the input residue voltage pair is complementary.

At the end of ϕ_2, the total charge sampled on C_1 and C_2 is

$$\begin{aligned} \sum Q &= V_{in}^{'} \cdot C_1 + V_{in}^{''} \cdot C_2 \\ &= V_{in} C \cdot \left[2 + \left(\delta_1 + \delta_2\right) + \Delta\left(\delta_1 - \delta_2\right)\right]. \end{aligned} \tag{3.30}$$

Solve for $V_o^{'}$ and $V_o^{''}$ in ϕ_3 and ϕ_4, we have

$$\begin{aligned} V_o^{'} &= \left(2V_{in} - V_{REF}\right) - \lambda_1 \cdot \left(V_{in} - V_{REF}\right) + \lambda_2^{'} \cdot \left(V_{in} - V_{REF}\right) + \lambda_1 \cdot \Delta \cdot V_{in}, \\ V_o^{''} &= \left(2V_{in} - V_{REF}\right) + \lambda_1 \cdot \left(V_{in} - V_{REF}\right) + \lambda_2^{''} \cdot \left(V_{in} - V_{REF}\right) + \lambda_1 \cdot \Delta \cdot V_{in}, \end{aligned} \tag{3.31}$$

where

$$\begin{aligned} \lambda_1 &= \delta_1 - \delta_2, \\ \lambda_2^{'} &= \delta_1 \cdot (\delta_1 - \delta_2), \\ \lambda_2^{''} &= \delta_2 \cdot (\delta_2 - \delta_1). \end{aligned} \tag{3.32}$$

Again assume that $V_{in}^{'} = V_{in}^{''} = V_{in}$; when $V_o^{'}$ and $V_o^{''}$ are sampled by C_3 and C_4, the effective residue voltage is given by

$$\begin{aligned} V_{o,eff} &= \frac{V_o^{'} \cdot C_3 + V_0^{''} \cdot C_4}{C_3 + C_4} \\ &= (2V_{in} - V_{REF}) + \varepsilon \cdot (V_{in} - V_{REF}), \end{aligned} \tag{3.33}$$

where $\varepsilon = \frac{1}{2}(\delta_1 - \delta_2) \cdot (\delta_1 - \delta_2 - \delta_3 + \delta_4)$. Finally, we have

$$E(\varepsilon) = \sigma^2, \quad Var(\varepsilon) = 3\sigma^4. \tag{3.34}$$

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Chapter 4 _____

PROTOTYPE DESIGN

This chapter describes the prototype design of a 14-b pipeline ADC that employs the passive capacitor error-averaging technique (II). The stage scaling is applied to this converter using the analysis presented in Chapter 2. A few practical issues in the design of a high-resolution pipeline ADC will be addressed and the measurement results of the prototype will be presented in the next chapter.

4.1 SAMPLING CLOCK SKEW

In a typical pipeline ADC implementation, a dedicated sample-and-hold amplifier (SHA) at the front-end is often used to enhance the dynamic performance of the converter. It mitigates the effect of the timing skew between the passive switched-capacitor sampler and the sub-ADC of the first stage. As indicated in Figure 4.1,

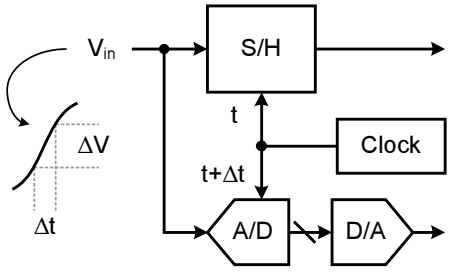


Figure 4.1 Sampling clock skew in the front-end pipeline stage.

this aperture error effectively creates a dynamic offset between the two paths when the input signal exhibits a large slew-rate. The offset ultimately results in a hard clipping error when the digital error-correction range of the subsequent stages is exceeded.

Nonetheless, the dedicated SHA is accompanied by a substantial power penalty; as it usually acts as a unity-gain buffer, the SHA provides no attenuation to the ADC noise referred to the input, meanwhile adding its own contribution. Assuming the SHA and the ADC contribute an equal amount of noise and consume an equal amount of power, then for the same target SNR, having a dedicated SHA translates into a fourfold increase in the total conversion power. This is too high a price for low-voltage designs that are SNR-limited. Notwithstanding, alternative solutions exist to remedy this problem. One approach is to use digital techniques to monitor the skew and adaptively compensate for it with a variable delay circuit. In this prototype, a simpler approach is adopted that exploits the large built-in digital redundancy of a 1.5-b/s architecture.[1] For example, it is straightforward to calculate that for a 40-MHz full-scale sinusoidal input, the maximum clock skew tolerable to this architecture is one nanosecond. It is believed that the choice of a 1.5-b/s topology achieves a judicious architectural tradeoff and the best power efficiency in this prototype when the stage resolution and scaling, the SHA power penalty, the clock skew, and the averaging overhead are all taken into account. With this choice, the

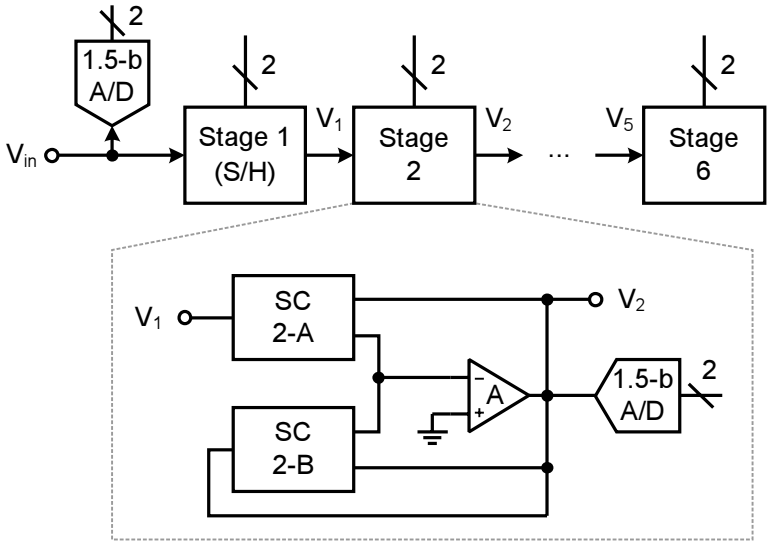


Figure 4.2 Block diagram of the 14-b pipeline ADC.

optimum stage-scaling factor is determined to be 1/2.

4.2 AMPLIFIER AND SUB-ADC SHARING

Figure 4.2 shows the equivalent single-ended block diagram of the prototype ADC. The actual implementation is fully differential. The amplifiers and sub-ADCs are interleaved between the successive switched-capacitor stages to save more power (e.g., SC 2-*A* and 2-*B* in Figure 4.2). The 14-bit ADC is partitioned into six pipeline stages with a total of six amplifiers and fourteen comparators. Three bits are resolved by each stage effectively.

The amplifier sharing technique was previously used in pipeline ADCs with an 8- to 10-bit resolution.[2, 3] The challenge of this technique is to maintain the charge fidelity at the summing node, which is particularly difficult at the accuracy

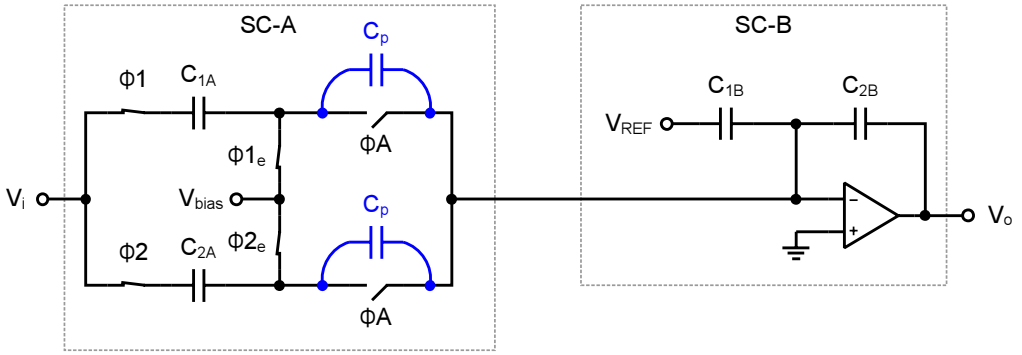
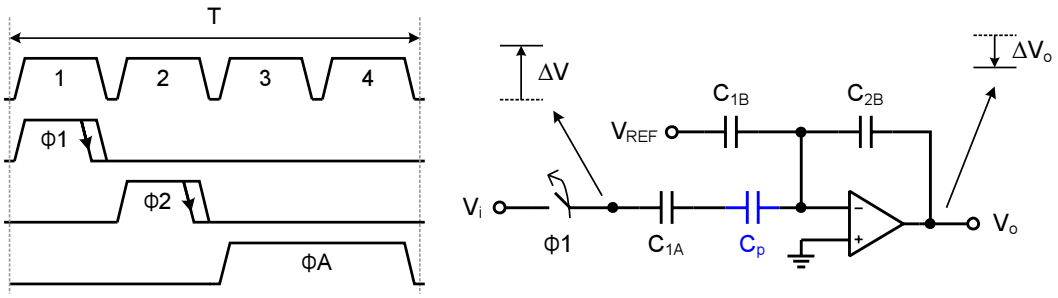


Figure 4.3 Potential summing node crosstalk through the parasitic capacitance of off switches.

level of 14 bits. A potential crosstalk path between SC-*A* and SC-*B* (Figure 4.3 and Figure 4.4b) arises due to a drain-to-source stray capacitor C_p of the off-switch ϕA (the same problem exists for ϕB, which is not shown).

At the moment $\phi 1$ switches off, a signal-dependent charge injection induces an error voltage ΔV on the top-plate of the capacitor C_{1A}; through the series connection of C_{1A}, C_p, and C_{2B}, it produces a small error voltage ΔV_o in the output



(a) (b)

Figure 4.4 (a) Timing diagram. (b) Summing node crosstalk path during the falling edge of $\phi 1$.

residue, destroying the accuracy of SC-*B*. The effect of C_p, albeit small, can be significant at the 14-bit level. The effect of this crosstalk can be gauged by the voltage gain through the coupling path, which is essentially the capacitor ratio C_p/C_{2B}.

A simple remedy to this problem is to tie the bottom-plates of C_{1A} and C_{2A} (C_{1B} and C_{2B} as well) to an AC ground at all time, such that the coupling through C_p only results in a fixed offset error. This is accomplished for C_{2A} by simply advancing the rising edge of $\phi 2_e$ (the early phase of $\phi 2$) to the rising edge of $\phi 1$ as shown in Figure 4.5a. However, the same operation for C_{1A} is not possible because it has to take a sample at the end of $\phi 1$ and its bottom-plate becomes floating afterwards. An alternative solution is to postpone the trailing edge of $\phi 1$ to the end of $\phi 2$. Since the switch-off of $\phi 1$ is delayed, no charge is injected onto

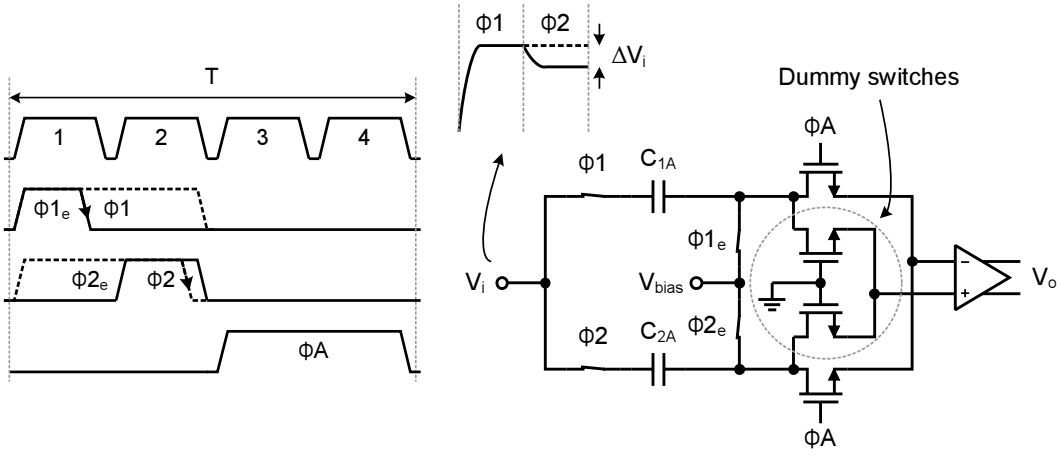


Figure 4.5 (a) Modified timing diagram. (b) Dummy switches.

the top-plate of C_{1A} at the first place. Thus, the crosstalk is eliminated.

Nonetheless, a careful examination of this solution still reveals a problem – it relies on the fact that V_i remains constant between $\phi 1$ and $\phi 2$, which is hardly guaranteed. In practice, V_i can be different between $\phi 1$ and $\phi 2$ due to a capacitor mismatch error in the previous pipeline stage. The difference between the dual residues, ΔV_i, albeit considerably smaller than the charge injection error, can still generate a significant error at the output. To mitigate this problem, gate-grounded dummy switches are introduced at the summing nodes (Figure 4.5b). Cross-coupled between the p- and n-sides of the virtual ground, they convert the residual crosstalk into a common-mode signal, which is rejected by the differential architecture. Combining all these techniques, the magnitude of the resultant crosstalk can be estimated by the following equation

$$\frac{\Delta V_o}{V_{FS}} \approx \frac{\Delta C}{C} \cdot \frac{C_p}{C_{2B}} \cdot \frac{\Delta C_p}{C_p} \approx \frac{1}{2^7} \cdot \frac{1}{2^8} \cdot 10\% << \frac{1}{2^{14}} \tag{4.1}$$

where $\frac{\Delta C}{C}$ represents the capacitor mismatch error of the previous stage, $\frac{\Delta C_p}{C_p}$ corresponds to the cancellation accuracy of the cross-coupled dummy switches, and V_{FS} is the full-scale reference voltage. Even with the conservative estimates of (4.1), the aggregated attenuation of the crosstalk is large enough to ensure a 14-bit accuracy at the summing node.

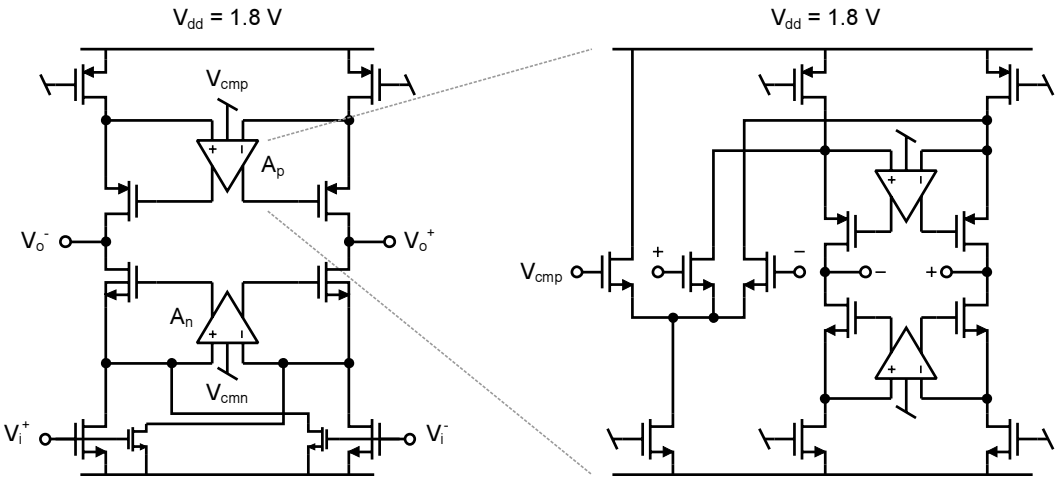


Figure 4.6 Nested CMOS gain-boosted amplifier.

4.3 NESTED CMOS GAIN BOOSTING

Delivering sufficient DC-gain at a high sampling rate with low power dissipation is a difficult challenge for amplifier design at a low supply voltage. Although a multi-stage architecture offers high open-loop gain, the necessity of frequency compensation makes it power inefficient. Single-stage architectures, on the other hand, offer large gain-bandwidth products with limited DC-gain due to the low output resistance of short-channel devices. The CMOS gain-boosting technique was previously introduced to enhance the output resistance of a single-stage operational transconductance amplifier (OTA).[4]

In this design, a nested gain-boosting technique is used. As illustrated in Figure 4.6, a two-level recursive boosting with devices of 0.2-μm gate-length

results in a minimum open-loop gain of 130 dB across the process corners in simulation, exceeding the accuracy requirement of a 14-bit converter. A manual analysis of the dynamics of the nested feedback loop is difficult; computer simulation was used instead to verify the stability.[5]

To maintain high current efficiency and large output swing simultaneously, the main amplifier uses a pseudo-differential architecture as shown in Figure 4.6. With four transistors in a stack, the peak-to-peak output swing of the amplifier exceeds 2 volts with a supply voltage of 1.8 volts. The boosting amplifiers all use a folded-cascode structure with a p- or n-type input differential pair to allow a flexible input common-mode range. The nested boosters are the scaled version of the main boosters. The current ratios among the main amplifier, the gain boosters, and the nested boosters are 64:8:1. The later two also share a common bias circuit.

4.4 Discrete-Time Common-Mode Regulation

The amplifier and switch-induced offset voltages are problematic in pseudo-differential pipeline architectures. Without compensation, the offset will quickly accumulate and saturate the usable signal swing due to the large inter-stage gain of the pipeline. Reverting to a fully differential topology with instantaneous common-mode feedback (CMFB) every a few stages was suggested to break the offset propagation, resulting in a compromised hybrid design.[6]

In this prototype, an analog delta-sigma loop that facilitates the common-

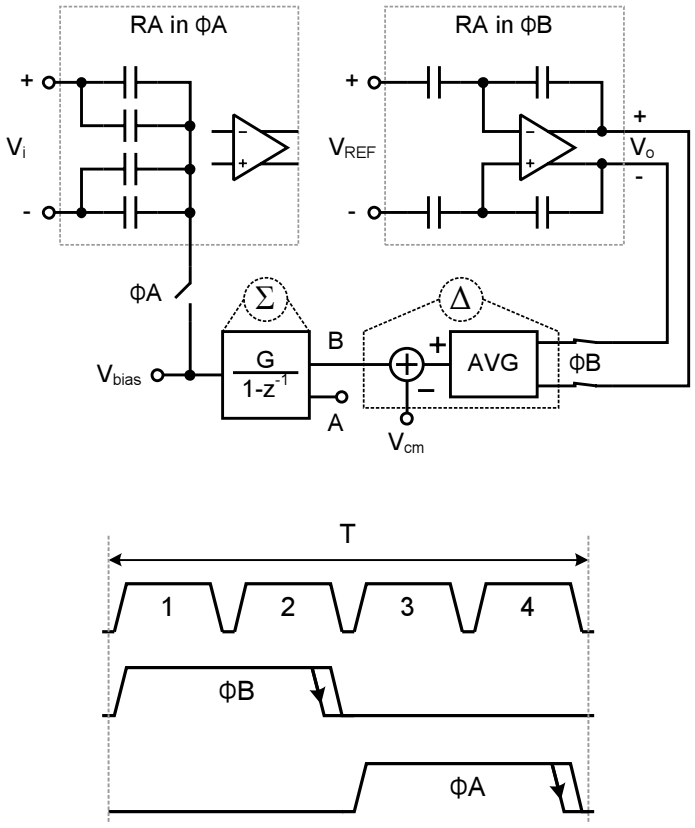


Figure 4.7 (a) ΔΣ common-mode regulation circuit. (b) Timing diagram.

mode control is introduced. Shown in Figure 4.7, an averaging circuit derives the output common-mode voltage and compares it to the desired reference (Δ); the resultant error voltage is then accumulated with a discrete-time integrator (Σ) and fed-back to be the bottom-plate bias for the S/H circuit. When the loop settles, the long-term average of the integrator input has to be zero, which forces the output common-mode to equal the reference voltage. The switched-capacitor circuits realizing the Δ and Σ blocks are also shown in Figure 4.8.

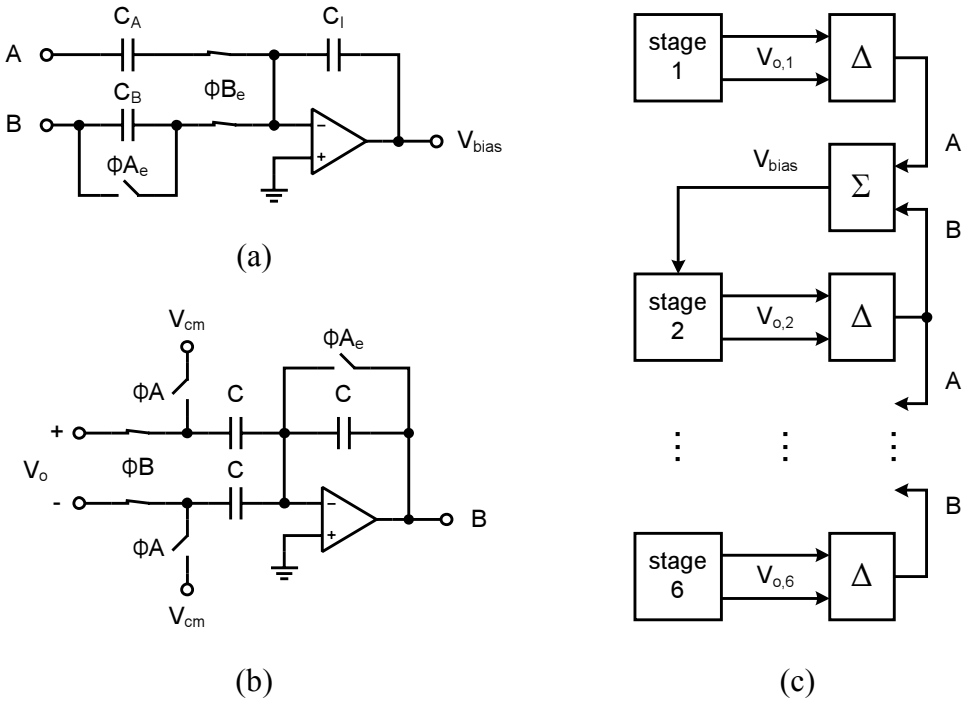


Figure 4.8 (a) Discrete-time integrator with look-ahead capacitor C_A. (b) Averaging and differencing amplifier. (c) Common-mode feedback and feedforward connections of the six pipeline stages.

One key design aspect of the common-mode regulation loop is to ensure its stability. Assuming an ideal integrator and ignoring parasitic capacitance, the z-domain closed-loop common-mode voltage transfer function can be derived as

$$H_{cm}(z) = \frac{V_{o,cm}}{V_{i,cm}} = \frac{1}{\beta} \cdot \frac{1 - z^{-1}}{1 - (1 - 2G/\beta) \cdot z^{-1}} \tag{4.2}$$

where β is the feedback factor of the main amplifier and $G = C_B/C_I$ is the integrator gain. The pole-zero location and the frequency response of this function

are plotted in Figure 4.9. The highpass nature resembles the characteristic noise-shaping function of a sigma-delta modulator. To ensure stability, the condition $0 \le G/\beta \le 1$ must be satisfied. Because G and β are determined by capacitor ratios, stability can be guaranteed over process corners.

However, stability is not sufficient to make this scheme fully functional. For a small integrator gain G, the magnitude of the closed-loop transfer function near the Nyquist frequency is approximately $1/\beta$, which is typically greater than one. It follows that a high-frequency common-mode variation will still be amplified. The desired closed-loop gain should be as close to zero as possible at all frequencies. This is accomplished by introducing a look-ahead path in the integrator as shown in Figure 4.8a. The modified transfer function becomes

$$H_{cm}(z) = \frac{1}{\beta} \cdot \frac{\left(1 - 2\beta \cdot \frac{C_A}{C_I}\right) \cdot \left(1 - z^{-1}\right)}{1 - \left(1 - \frac{2}{\beta} \cdot \frac{C_B}{C_I}\right) \cdot z^{-1}} \tag{4.3}$$

The condition $2\beta \cdot \frac{C_A}{C_I} = 1$ sets $H_{cm}(z) = 0$ identically for all frequencies. Again, this is determined by capacitor ratios and insensitive to process variations.

It is well known that the finite open-loop gain leads to a leakage problem in discrete-time integrators. This however is not of concern in this design as it

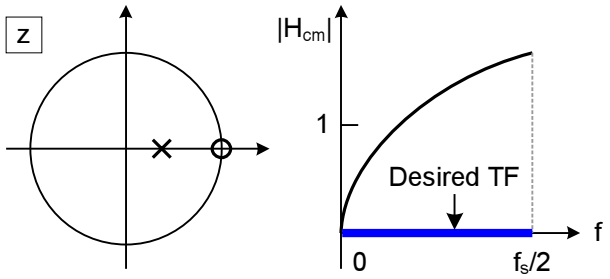


Figure 4.9 Pole-zero and frequency response plots of the CMFB loop.

effectively only introduces a small offset in setting the output common-mode. As a result, single-transistor amplifiers are used in the integrator and the averaging circuit. Computer simulation reveals a systematic offset of approximately 10 mV resulted from the finite-gain effect, which is small compared to the full-scale output swing.

4.5 Dynamic Comparator

The 1.5-b/s pipeline architecture greatly relaxes the offset tolerance of the comparators. In addition, an early comparison is performed that exploits the dual residue feature of the CEA technique. This allows the comparators a complete quarter clock cycle to resolve the digital code. As a result, the comparator design is quite relaxed; dynamic comparators with minimum size devices are used. The schematic diagram of the comparator is shown in Figure 4.10. The comparison threshold is determined by the size ratio of the sampling capacitors, which is 4:1 in this design. In addition, to maximize the architectural tolerance to the front-end sampling clock skew, autozeroed inverters are used as preamps to further reduce the first stage comparator offsets.

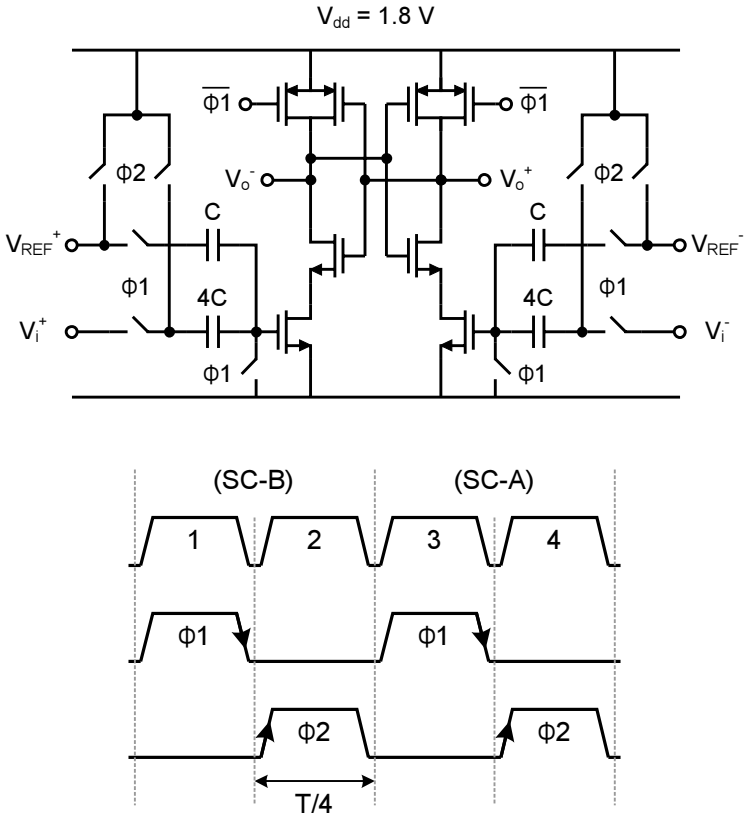


Figure 4.10 (a) Dynamic comparator. (b) Timing diagram.

4.6 SAMPLING SWITCH

The signal-dependent charge injection and on-resistance variation of switches pose fundamental limits to the achievable distortion levels of switched-capacitor circuits. The increased f_T through technology scaling improves the switch performance. In this prototype, the use of minimum channel-length devices combined with clock bootstrapping and in-line switch techniques[7, 8] resulted in an outstanding SFDR of 97 dB with a full-scale, 40-MHz input.[9]

APPENDIX

A4.1 Discrete-Time Common-Mode Regulation

The ΔΣ discrete-time common-mode feedback circuit utilizes an integrator in the feedback path to set the long-term DC bias of the sampling capacitor bottom-plate reference. The high-frequency common-mode gain is cancelled by the differentiator (C_A) that receives the common-mode output voltage from the previous pipeline stage (essentially the future common-mode input of the current stage). Redraw the integrator during ϕA and ϕB respectively in Figure 4.11.

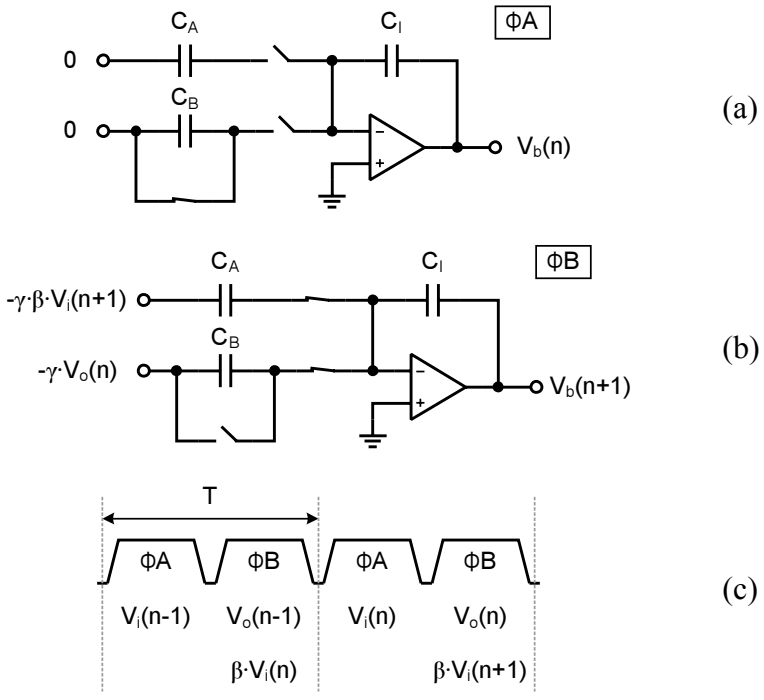


Figure 4.11 (a) Integrator in ϕA (sampling). (b) Integrator in ϕB (integration). (c) Timing diagram.

Assume that the closed-loop gain of the Δ-amplifier is γ.[†] The total charge on the top plates of C_A, $C_{B,}$ and C_I at the end of ϕA is

$$\sum Q_A = -\gamma\beta \cdot V_i(n)C_A + V_b(n)C_I, \tag{4.4}$$

and at the end of ϕB:

$$\sum Q_B = -\gamma\beta \cdot V_i(n+1)C_A - \gamma \cdot V_o(n)C_B + V_b(n+1)C_I. \tag{4.5}$$

Also, the common-mode voltage gain of the main amplifier is

$$V_o(n) = \frac{1}{\beta} \cdot \left[V_i(n) - V_b(n)\right]. \tag{4.6}$$

Combine (4.4)-(4.6), solve for V_o, we have

$$\frac{V_o}{V_i}(z) = \frac{1}{\beta} \cdot \frac{\left(1 - \gamma\beta \cdot \frac{C_A}{C_I}\right) \cdot \left(1 - z^{-1}\right)}{1 - \left(1 - \frac{\gamma}{\beta} \cdot \frac{C_B}{C_I}\right) \cdot z^{-1}}. \tag{4.7}$$

Set $C_A = 0$ in (4.7), we obtain the effect of the integrator only:

$$\frac{V_o}{V_i}(z) = \frac{1}{\beta} \cdot \frac{1 - z^{-1}}{1 - \left(1 - \frac{\gamma}{\beta} \cdot \frac{C_B}{C_I}\right) \cdot z^{-1}}. \tag{4.8}$$

If we set $\gamma = 2$ in (4.7) and (4.8), we obtain the expressions of (4.3) and (4.2).

[†] The closed-loop gain of the Δ-amplifier is not assumed simply determined by the capacitor ratio because of the finite-gain effect of the single-transistor amplifier.

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Chapter 5 _____

EXPERIMENTAL RESULTS

Chapter 4 described the design of a 14-b pipeline ADC that employs the passive capacitor error-averaging technique (II). The prototype ADC was fabricated in a

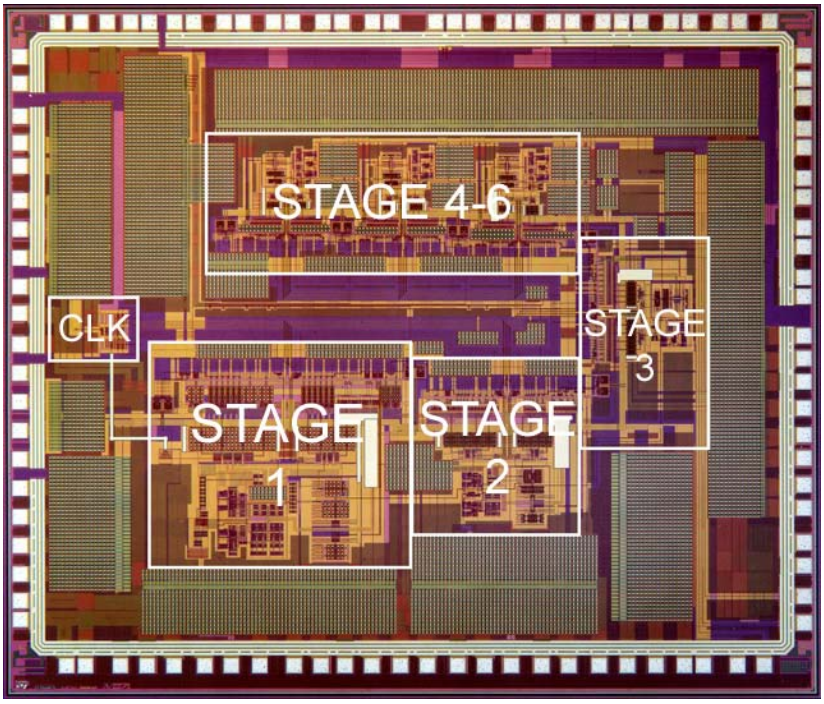


Figure 5.1 Die photo of the prototype 14-b pipeline ADC.

1.8-V, 0.18-μm, 6M-1P digital CMOS process. Capacitors were implemented using metal-insulator-metal (MIM) structures with no special attention paid in layout to match them. The die photo is shown in Figure 5.1. The size of the chip measures 4.3×3.5 mm^2 with the ADC occupying approximately 10 mm^2. The measurement results of the prototype are presented in this chapter.

5.1 STATIC LINEARITY

A code-density test was used to measure the differential nonlinearity (DNL) and the integral nonlinearity (INL) with a 1-MHz full-scale sinusoidal input. At 12 MS/s, eight million samples were collected. The measured DNL and INL profiles are shown in Figure 5.2. The maximum DNL is 0.47 LSB and the maximum INL is 0.54 LSB.

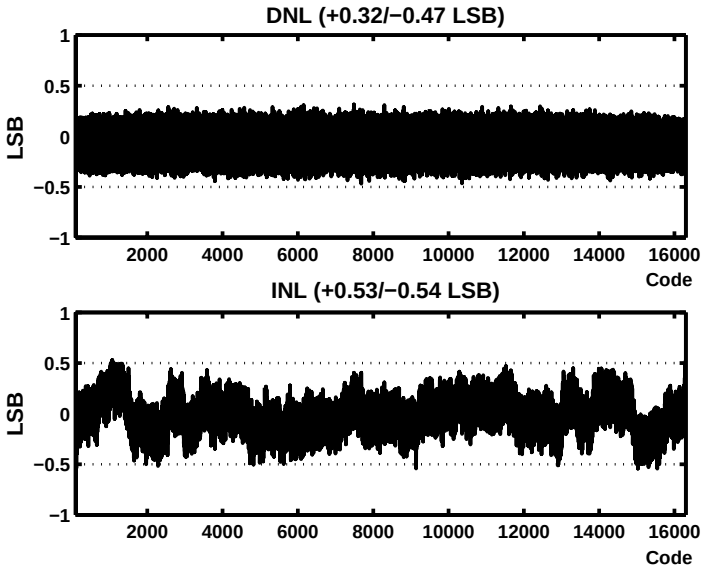
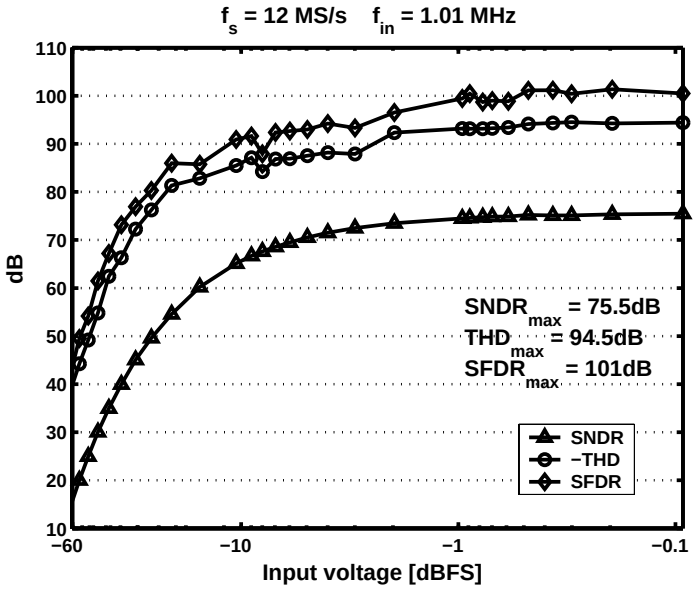
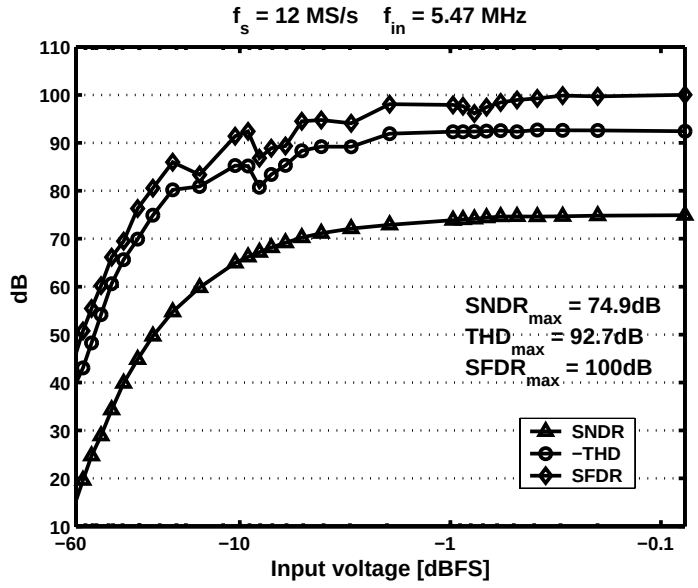


Figure 5.2 Measured DNL and INL (f_s = 12 MS/s, f_{in} = 1 MHz).



(a)



(b)

Figure 5.3 Measured ADC performance versus input signal level. (a) f_s = 12 MS/s, f_{in} = 1.01 MHz. (b) f_s = 12 MS/s, f_{in} = 5.47 MHz.

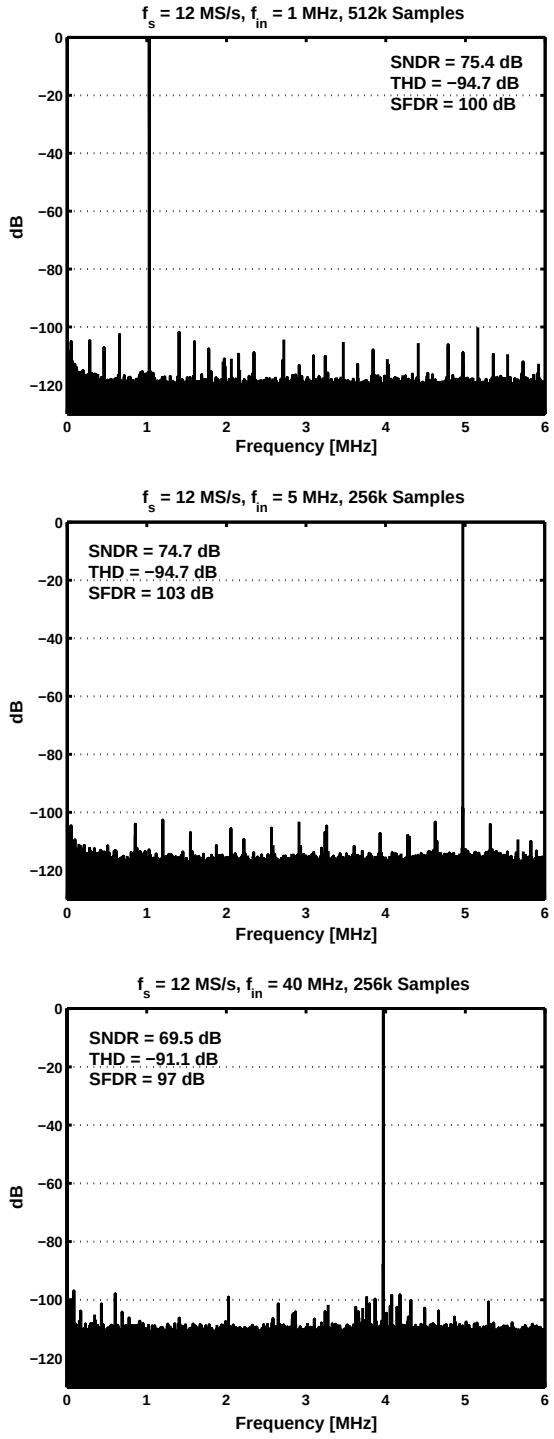
5.2 DYNAMIC LINEARITY

The dynamic linearity of the ADC was characterized by analyzing a fast Fourier transform (FFT) of the output codes with a single-tone input.

5.2.1 SNDR, THD, AND SFDR

Shown in Figure 5.3a, the measured peak SNDR reaches 75.5 dB with a 1.01-MHz input, equivalent to 12.25 effective-number-of-bits (ENOB). Under the same condition, the peak total harmonic distortion (THD) and the peak spurious-free dynamic range (SFDR) are -94.5 dB and 101 dB respectively (the THD figure corresponds to the power sum of the first fifteen harmonics). The same measurement performed with a 5.47-MHz input reveals a fraction of dB degradation in SNDR figures (Figure 5.3b).

The measured FFT spectrums with -0.4-dBFS, 1-MHz and 5-MHz inputs are shown in Figure 5.4a and Figure 5.4b, respectively. The SFDR in these cases reaches the value of 100 dB and 103 dB, and the SNDR is 75.4 dB and 74.7 dB, respectively. To measure the input analog bandwidth and to verify the architecture choice without a dedicated sample-and-hold amplifier, the ADC was also tested with a -0.4-dBFS, 40-MHz sine-wave sub-sampled at 12 MS/s. Figure 5.4c shows the digital spectrum of the output. In this case, the measured SNDR and SFDR are 69.5 dB and 97 dB, respectively.



(a)

(b)

(c)

Figure 5.4 FFT spectrum at f_{in} = (a) 1 MHz, (b) 5 MHz, and (c) 40 MHz.

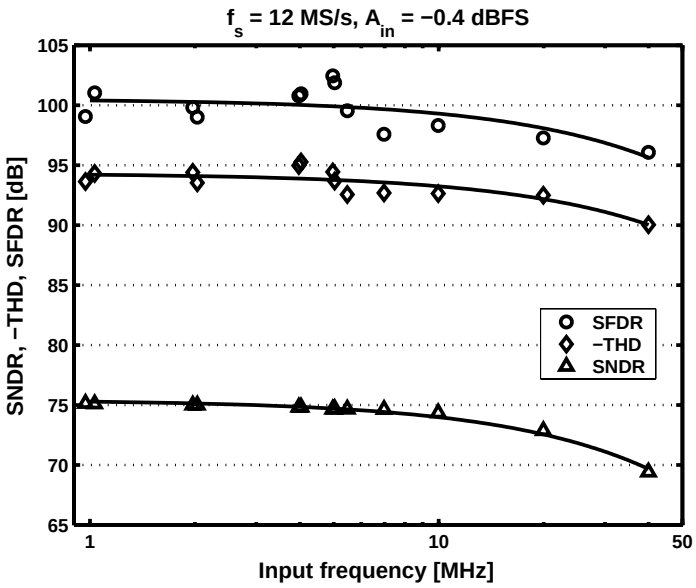


Figure 5.5 Measured dynamic performance.

5.2.2 ADC PERFORMANCE SENSITIVITY

Figure 5.5 summarizes the measured dynamic performance of this 14-bit ADC with an input frequency span from 1 MHz to 40 MHz. The random jitter

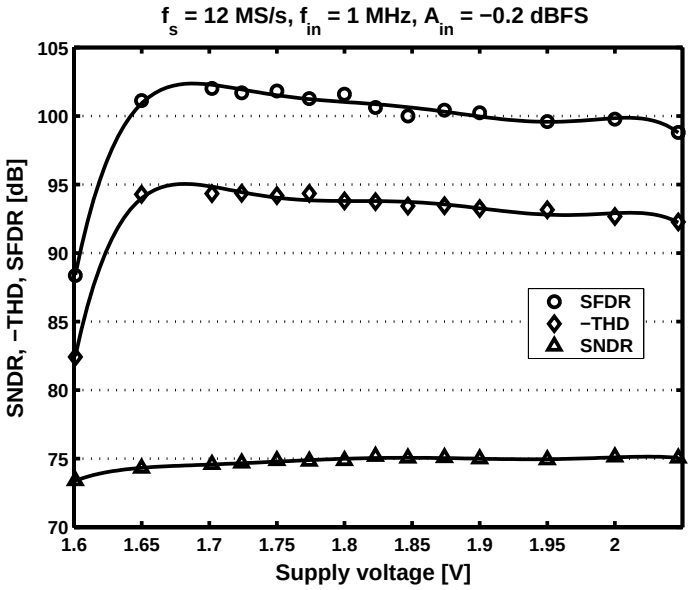


Figure 5.6 Measured performance versus V_{dd}.

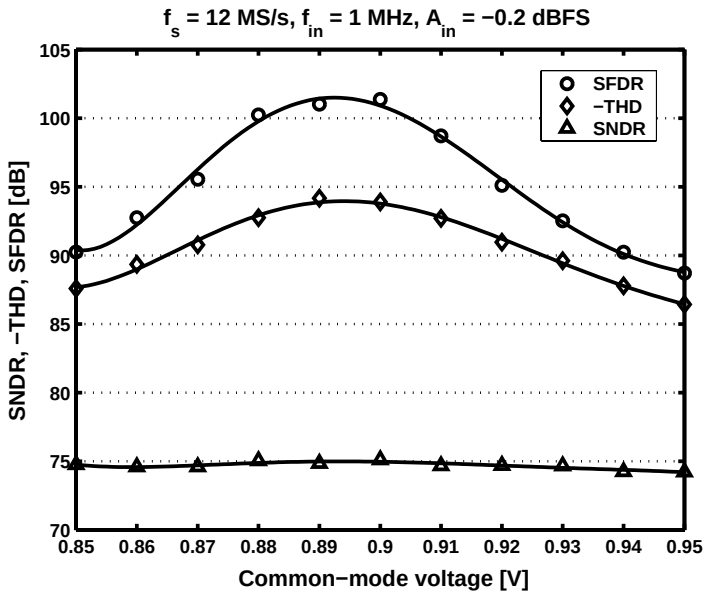


Figure 5.7 Measured performance versus V_{cm}.

accumulated during the generation and distribution of the clock signal limits the SNR performance at high frequencies. A locked histogram test revealed a 1.5-ps rms jitter in the system including the clock generator, the synthesizer, the ADC chip, and the board, which translates to a 70-dB SNR at 40 MHz approximately.[1] This confirms the observation that the performance of this converter is limited by the clock jitter at high input frequencies.

The performance sensitivity against the supply and common-mode voltages was also verified. The measurement results are summarized in Figure 5.6 and Figure 5.7. The minimum supply voltage at which this ADC still works without noticeable performance degradation is 1.65 volts. The total power consumption of the chip is 97.7 mW excluding the low-voltage-differential-swing (LVDS) digital output drivers. Out of this, 95.4 mW is consumed by the analog circuits, 1.4 mW

Table 5.1 Measured ADC Performance (1.8 V, 25 °C)

Resolution	14 bits	
Reference voltage	0.4 V and 1.4 V	
Packaging	QFP100	COB
Sampling rate	10 MS/s	12 MS/s
DNL @ 1 MHz	-0.31/0.31 LSB	-0.47/0.32 LSB
INL @ 1 MHz	-0.58/0.53 LSB	-0.54/0.53 LSB
Peak SNDR	73.6 dB	75.5 dB
Peak SFDR	99 dB	103 dB
SFDR @ 40 MHz	84 dB	97 dB
Power	112 mW	98 mW
Technology	0.18-μm 6M-1P CMOS	

is consumed by the digital circuits, and 0.9 mW goes to the clock buffer.

All measurements were performed with a 1.8-V supply at room temperature (25 ºC). Table 5.1 summarizes the measurement results of the prototype ADC.

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Chapter 6

CONCLUSION

A 14-bit pipeline ADC in 0.18-μm CMOS technology using exclusively thin oxide transistors and a low supply voltage of 1.8 volts is demonstrated. The prototype design achieves a true 14-bit linearity and a 12.25 ENOB in experiments without trimming, calibration, or dithering. This work demonstrates the feasibility of sustained scaling of high-resolution CMOS ADCs in the deep-submicron regime and the potential improvement on performance harvestable through technology scaling.

As a reference, Figure 6.1 shows the comparison of this design (marked by a square) and the previously reported high-resolution ADCs (marked by lozenges) with a 12-bit and higher resolution dated from 1988 to 2004. For SNR-limited designs, a more appropriate figure-of-merit (FOM) used in this comparison is defined as

$$FOM = \frac{Power}{2^{ENOB} \cdot f_s} \cdot V_{dd} \tag{6.1}$$

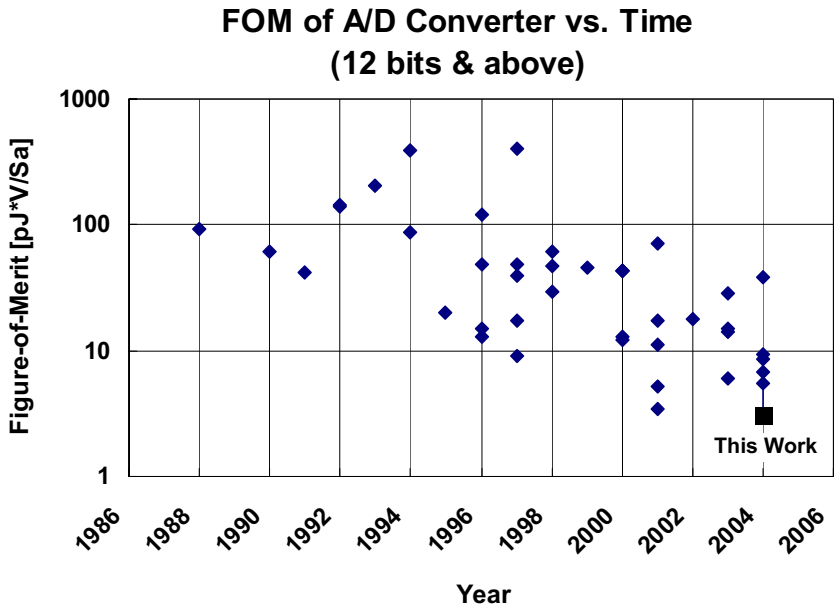

Figure 6.1 Comparison of this design (square) and previously published high-resolution ADCs (diamonds).

This is in accordance with (2.11) that the conversion power is inversely proportional to the supply voltage, as manifested by the normalization to the supply voltage in (6.1). This 14-bit pipeline ADC has achieved the lowest FOM in this category of Nyquist converters.