SYNTHESIS OF NONLINEAR DC CIRCUIT MODELS FOR THREE-TERMINAL DEVICES

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ABSTRACT

A unified black box approach is presented for synthesizing nonlinear dc circuit models of 3-terminal devices characterized by two families of characteristic curves in piecewise-linear form. The model building blocks consist of linear and nonlinear 2-terminal resistors, independent and linear controlled sources, as well as five generic forms of nonlinear controlled sources; namely, nonlinear controlled-linear resistors,-concave resistors, - convex resistors, -bi-concave resistors, and -bi-convex resistors. The circuit parameters and functions characterizing each of these elements in the models can be determined easily from the slopes and breakpoints associated with the segments of the prescribed characteristic curves. The paper concludes with the presentation of several nonlinear dc circuit models for 4 widely used devices; namely, bipolar transistors, field effect transistors, unijunction transistors, and triacs.

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1. INTRODUCTION

Device modeling is probably the weakest link in the area of computer-aided circuit design. Indeed, unless one has realistic circuit models for the devices used in a given circuit, no amount of computer analysis, let alone design, would be meaningful. In view of its crucial importance to computer-aided circuit design, much research is currently being conducted in the area of device modeling. There are basically two distinct approaches to device modeling: the physics-oriented approach [1-4] and the black box approach [5-9]. The first approach is based on the physical mechanisms which led to the device's operating characteristics. The second approach is based on the data measured from the device's terminals. In contrast to the heavy reliance on physical principles in the first approach, only system and circuit-theoretic principles are invoked in the black box approach.

The physics-oriented approach would appear to be more logical and reliable if indeed the physical operating mechanisms of the device are well-understood, and if the subsequent evolution from physical concepts to circuit model is carried out accurately. Unfortunately, this last step is usually achieved through various simplifying assumptions and approximations. The end result of which could lead to a highly idealized model. Another objection to the physics-oriented approach is that it is difficult to formulate a systematic modeling procedure that would apply to a large variety of devices. For example, the physical principles used to derive the pentode model are quite different from those used to derive the transistor model.

The black box approach would overcome some of the objections inherent in the physics-oriented approach. However, the absence of an identification theorem for general nonlinear systems precludes the possibility of verifying the validity of a black box model under arbitrary excitations.[1] In view of this basic problem, the black box approach has so far been used successfully only in the synthesis of linear incremental circuit models. Our objective in this paper is to extend the scope of application of the black box approach to the synthesis of nonlinear dc circuit models of 3-terminal devices. This class of circuit models is essential to the analysis of equilibrium states of dynamic nonlinear networks [10], as well as in the design of biasing circuits [11-12]. Fortunately, the validity of a nonlinear dc black box circuit model can be easily verified by comparing the family of simulated input and output characteristic curves with those actually measured from the device.[2] For convenience, we will assume throughout this paper that the two families of input and output characteristic curves are represented in piecewise-linear form.[3]

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[1] Unlike linear systems [6], a nonlinear circuit model which correctly simulates a nonlinear system under some prescribed excitation may not respond correctly when the system is driven by other excitations.

[2] Referring to the symbols and notations defined in Figs. 1(a), (b), and (c), the dc characteristics of a 3 terminal device is completely specified by two families of characteristic curves [8]; namely, a family of input characteristic curves $i_1=g_1(v_1,x_1)$, where the controlling parameter x_1 may be either i_2 on v_2; and a family of output characteristic curves $i_2=g_2(v_2,x_2)$, where the controlling parameter x_2 may be either i_1 or v_1. We will assume throughout this paper that each family of characteristic curves is either voltage-controlled or current-controlled. In the latter case, we will use the same notations even though $g_1(v_1,x_1)$ and $g_2(v_2,x_2)$ are no longer single-valued functions of v_1 and v_2.

[3] With some increased computational efforts, the modeling procedure to be presented in this paper could be generalized to handle smooth characteristic curves. However, this generalization is seldom necessary since more piecewise-linear segments could always be added to improve the model's accuracy.

Using the model decomposition technique to be presented in Sec. 2 and the model building blocks to be presented in Sec. 3, a unified black box approach to dc nonlinear circuit modeling of 3-terminal devices will be presented in Sec. 4. This approach is quite simple and is rather precise in the sense that a circuit model can always be synthesized to simulate exactly the prescribed families of piecewise-linear characteristic curves. The parameters associated with the model can be determined directly from the prescribed characteristic curves. Moreover, the same procedure applies to any 3-terminal device, be it a vacuum tube or a transistor.

2. THE MODEL DECOMPOSITION PREAMBLE

The problem of synthesizing a nonlinear dc circuit model for a 3-terminal device is equivalent to that of synthesizing a controlled resistor R_1 characterized by $i_1=g_1(v_1,x_1)$ and a controlled resistor R_2 characterized by $i_2=g_2(v_2,x_2)$.[4] The complete model is realized by interconnecting these two controlled resistors as shown in Fig. 1(d) [8]. Since the characteristic curves of most existing 3-terminal devices are located only in the first and the third quadrants, we will simplify matters by assuming both families of input and output characteristic curves to lie only within the shaded regions shown in Figs. 1(b) and (c), respectively. Under this assumption, each controlled resistor R_j

[4] A controlled resistor is a 2-terminal black box whose v-i curve is controlled by a third parameter x [8]. For example, a photo-diode is a controlled resistor with light intensity as the controlling parameter. In this paper, the controlling parameter will always be a voltage or a current.

may be synthesized by interconnecting two appropriate controlled resistors R_j' and R_j'' (j=1,2), with two ideal diodes either in the parallel mode shown in Fig. 1(e), or in the series mode shown in Fig. 1(h). In both cases, R_j' is designed to simulate the characteristic curves in the first quadrant only, while R_j'' is designed to simulate the characteristic curves in the third quadrant only. The characteristic curves of R_j' and R_j'' in the remaining regions are irrelevant since they are effectively "clipped" by the ideal diodes.

For the parallel mode in Fig. 1(e), the two diodes are used to introduce the constraint $i_j' = 0$ for $v_j' \leq 0$ in Fig. 1(f), and the constraint $i_j'' = 0$ for $v_j'' \geq 0$ in Fig. 1(g). The resulting characteristic curves of the composite 1-port shown in Fig. 1(e) would then be characterized by a family of curves whose first quadrant characteristics are identical to those of Fig. 1(f), and whose third quadrant characteristics are identical to those of Fig. 1(g). For the series mode in Fig. 1(h), the two diodes are used to introduce the constraint $v_j' = 0$ for $i_j' \leq 0$ in Fig. 1(i), and the constraint $v_j'' = 0$ for $i_j'' \geq 0$ in Fig. 1(j). Again, the composite 1-port shown in Fig. 1(h) would correctly simulate the prescribed characteristic curves in both the first and the third quadrants.

In view of this decomposition technique and the observation that the characteristic curves of controlled resistors are rotated by 180° upon interchanging the two terminals of the resistor, it follows that henceforth, we may restrict our attention to the synthesis of models for simulating characteristic curves in the first quadrant only.

It will be clear in the sequel that for certain devices exhibiting odd symmetry or other special properties, it may be superflous to apply

the decomposition technique. Indeed, since the dynamic range of operation of most practical devices invariably covers only portions of the first or the third quadrant, no decomposition would be needed in such cases. However, for the sake of generality, the decomposition preamble must be considered as an integral part of the unified approach to be presented in Sec. 4.

3. MODEL BUILDING BLOCKS

We will now introduce the building blocks to be used in our models. These building blocks constitute a "complete set" in the sense that no other elements will be needed. This set is listed in Table 1 under 4 separate categories. Category I consists of linear resistors and four types of linear controlled sources. For convenience in the determination of circuit parameters, the linear resistors will be represented either by its resistance R, or by its conductance G. Category II consists of independent sources and 2-terminal nonlinear resistors. The ideal diode, the concave resistor, and the convex resistor are three specific nonlinear resistors frequently used in our models. The concave resistor is characterized by [8]:

$$\begin{aligned} i &= G(v-E) \quad , v \geq E \\ &= 0 \qquad , v < E \end{aligned} \tag{1}$$

It is completely specified by two parameters, the conductance (slope) G and the voltage intercept E. The convex resistor is characterized by:

$$\begin{aligned} v &= R(i-I) \quad , i \geq I \\ &= 0 \qquad , i < I \end{aligned} \tag{2}$$

It is completely specified by two parameters, the resistance (reciprocal slope) R and the current intercept I.

Category III consists of nonlinear controlled sources and nonlinear controlled linear resistors. There are 4 types of nonlinear controlled sources; namely, a voltage-controlled voltage source characterized by $v_j = E_j(v_k)$, a current-controlled voltage source characterized by $v_j = E_j(i_k)$, a voltage-controlled current source characterized by $i_j = I_j(v_k)$, and a current-controlled current source characterized by $i_j = I_j(i_k)$, where $E_j(\cdot)$ and $I_j(\cdot)$ are arbitrary nonlinear functions and where $j \neq k$. The nonlinear controlled linear resistor may be represented either as a controlled resistance $v_j = R_j(x_j)i_j$, or a controlled conductance $i_j = G_j(x_j)v_j$, where the controlling parameter x_j may be either v_k or i_k, $k \neq j$, and where $R_j(\cdot)$ and $G_j(\cdot)$ are arbitrary nonlinear functions [10]. From the theoretical point of view, the elements listed in Category III are redundant in the sense that they all could be synthesized by using only elements belonging to Categories I and II. Indeed, Table 2 shows two distinct realizations for each of the four elements in Category III using only linear controlled sources and nonlinear resistors. These equivalent circuits will be useful for those computer programs which do not accept elements from Category III.

Category IV consists of four generic families of x-controlled 2-terminal nonlinear resistors; namely, an x-controlled concave resistor, an x-controlled convex resistor, an x-controlled bi-concave resistor, and an x-controlled bi-convex resistor. An x-controlled concave resistor is characterized by

$$i_j = G_j(x_j)u\circ(v_j - E_j(x_j)) \tag{3}$$

where "$\circ$" denotes the usual composition operation, and where

$$\begin{aligned} u(z) &= z \quad , z \geq 0 \\ &= 0 \quad , \quad > 0 \end{aligned} \tag{4}$$

and where $G_j(\cdot)$ and $E_j(\cdot)$ are arbitrary nonlinear functions of the parameter x_j, which may be either v_k or i_k, $j \neq k$. For a given value of x_j, an x-controlled concave resistor reduces to a concave resistor as defined in (1). Hence, an x-controlled concave resistor is completely specified by two functions, the conductance function $G_j(\cdot)$ and the voltage-intercept function $E_j(\cdot)$.

An x-controlled convex resistor is characterized by

$$v_j = R_j(x_j)u\circ(i_j - I_j(x_j)) \tag{5}$$

where $u(\cdot)$ is as defined in (4), $R_j(\cdot)$ and $I_j(\cdot)$ are arbitrary nonlinear functions of the parameter x_j, which may be either v_k or i_k, $j \neq k$. For a given value of x_k, an x-controlled convex resistor reduces to a convex resistor as defined in (2). Hence, an x-controlled convex resistor is completely specified by two functions, the resistance function $R_j(\cdot)$ and the current-intercept function $I_j(\cdot)$.

An x-controlled bi-concave resistor is characterized by

$$i_j = G_j(x_j)u\circ(v_j - E_j(x_j)) + G_j^*(x_j)u^*\circ(v_j + E_j^*(x_j)) \tag{6}$$

where $u(\cdot)$ is as defined in (4), and

$$u^*(z) = - u(-z) \tag{7}$$

and where $G_j(\cdot)$, $E_j(\cdot)$, $G_j^*(\cdot)$, and $E_j^*(\cdot)$ are arbitrary nonlinear functions of the parameter x_j, which may be either v_k or i_k, $j \neq k$. An x-controlled bi-concave resistor is completely specified by 4 functions; namely, the two conductance functions $G_j(\cdot)$ and $G_j^*(\cdot)$ and the two voltage-intercept functions $E_j(\cdot)$ and $E_j^*(\cdot)$.

An <u>x-controlled bi-convex resistor</u> is characterized by

$$v_j = R_j(x_j)u\circ(i_j - I_j(x_j)) + R_j^*(x_j)u^*\circ(i_j + I_J^*(x_j)) \tag{8}$$

where $u(\cdot)$ and $u^*(\cdot)$ are defined in (4) and (7), and where $R_j(\cdot)$, $I_j(\cdot)$, $R_j^*(\cdot)$, and $I_j^*(\cdot)$ are arbitrary nonlinear functions of the parameter x_j, which may be either v_k or i_k, $j \neq k$. An x-controlled bi-convex resistor is completely characterized by 4 functions; namely, the two resistance functions $R_j(\cdot)$ and $R_j^*(\cdot)$ and the two current-intercept functions $I_j(\cdot)$ and $I_j^*(\cdot)$.

The v-i curve associated with each element in Category IV for a given value of the parameter x is given in Table 3 along with an equivalent circuit model made up of only elements from categories I, II, and III. Since the elements from Category III were shown earlier to be made up of only elements in Categories I and II, it follows that the elements in Categories III and IV are introduced only for the purpose of obtaining simpler models. With the help of the equivalent models given in Tables 2 and 3, only the elements listed in Categories I and II are absolutely

necessary. In spite of this redundancy, however, it would still be advantageous for us to include the elements in Categories III and IV in our repertoire of model building blocks because these elements will generally be needed in the models of many practical devices. Replacing these elements by their equivalent circuits from Tables 2 and 3 would greatly increase the complexity of the resulting circuit model.

4. A UNIFIED BLACK BOX MODELING APPROACH

Our unified approach is a generalization of the segment-by-segment method presented in Chapter 8 of [8] for synthesizing a 2-terminal black box with a prescribed v-i curve. Using only concave and convex resistors as building blocks, the v-i curve is realized one segment at a time. The crux of the segment-by-segment method is based on the observation that a concave (convex) resistor, when connected in parallel (series) with another 2-terminal black box N, changes the v-i curve of N only in the region $v > E$ ($i > I$). This property is a direct consequence of the characteristic constraint $i = 0$ for $v \leq E$ ($v = 0$ for $i \leq I$) of a concave (convex) resistor. Since the v-i curve of N remains unchanged in the region $v \leq E$ ($i \leq I$) upon connecting a concave (convex) resistor in parallel (series) with it, it is possible to add a new segment with any prescribed slope and breakpoint to the v-i curve without affecting the remaining segments. In other words, the addition of an appropriate concave or convex resistor will not introduce any "loading effect" on that part of the v-i curve previously synthesized. Consequently, a v-i curve with n breakpoints can be realized by using a total combination of n concave and convex resistors. In general, a linear resistor and an

independent voltage or current source is used to realize the first (left-most) segment. The next segment is realized by connecting either a concave resistor in parallel, or a convex resistor in series, depending on the relative slope and break point between the first two segments. This procedure is repeated until the last (right-most) segment is realized.

The segment-by-segment method can be generalized to realize an arbitrary family of prescribed v-i curves provided x-controlled concave resistors and x-controlled convex resistors are used as building blocks. The procedure consists of realizing one v-i curve at a time, via the segment-by-segment method. This generalization is possible because each v-i curve is controlled by the value of the parameter x. By fixing the value of x, we automatically fix the v-i curve to be synthesized. In order to guarantee that each v-i curve in the family is realized by the same circuit topology, we must assume that each v-i curve in the family of prescribed characteristic curves has the same number of breakpoints. There is no loss of generality in this assumption because additional breakpoints can always be inserted along the v-i curve, if necessary, without changing the original specification.

Example. To illustrate the above synthesis procedure, let us consider synthesizing a dc nonlinear circuit model for simulating exactly the family of prescribed piecewise-linear input characteristic curves $i_1 = g_1(v_1,v_2)$ in Fig. 2(a) and the family of prescribed piecewise-linear

output characteristic curves $i_2 = g_2(v_2,i_1)$ in Fig. 2(b).[5]

(a) Modeling the input characteristic curves $i_1 = g_1(v_1,v_2)$. Since each v_1-i_1 curve has 4 breakpoints, it would be necessary to use a combination of "4" v_2-controlled concave and convex resistors. The resulting model is shown in the left-half portion of Fig. 2(c). The v_2-controlled linear resistor is used to realize the 4 leftmost segments (through the origin) in Fig. 2(a). Its conductance function $G_1(\cdot)$ is shown in Fig. 3(a). An inspection of this function shows that $G_1(0) = 2.0$ m℧, $G_1(2) = 0.5$ m℧, $G_1(4) = 0.3$ m℧, and $G_1(6) = 0.2$ m℧. These values are taken directly from the slopes of the 4 leftmost segments in Fig. 2(a). The function $G_1(\cdot)$ in Fig. 3(a) is obtained by connecting these 4 data points by straight lines. This is equivalent to assumming the slope varies uniformly between each pair of segments in Fig. 2(a). Clearly, a non-uniform variation could also be simulated by drawing an appropriate smooth curve through the 4 data points.

The second segment associated with each of the 4 v_1-i_1 curves in Fig. 2(a) is realized next by connecting a v_2-controlled concave resistor in parallel with the v_2-controlled linear resistor $G_1(v_2)$. The conductance function $G_2(\cdot)$ and the voltage intercept function $E_2(\cdot)$ for this

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[5] We pick a hypothetical device here in order to illustrate the generality of our present approach. Unlike the modeling procedure presented in Chapter 11 of [8], the family of v-i curves to be modeled may now be prescribed arbitrarily. Indeed, corresponding breakpoints are no longer required to lie along a straight line, and segments with both positive and negative slopes are now allowed. Moreover, two or more v-i curves in the family may even intersect one another, as is the case in Fig. 2(a).

a combination of "5" i_1-controlled concave and convex resistors. The resulting model is shown in the right-half portion of Fig. 2(c). Again, the 4 leftmost segments through the origin in Fig. 2(b) are realized by the i_1-controlled linear resistor with a resistance function $R_6(\cdot)$ as shown in Fig. 3(j). The next two segments can be realized by connecting two i_1-controlled convex resistors in series with this resistor as shown in Fig. 2(c). The resistance function $R_7(\cdot)$ and current-intercept function $I_7(\cdot)$ are obtained from the slope and intercept of the second segment relative to the first segment, and are shown in Figs. 3(k) and (ℓ). similarly, the resistance function $R_8(\cdot)$ and current-intercept function $I_8(\cdot)$ are obtained from the slope and intercept of the third segment relative to the second segment, and are shown in Figs. 3(m) and (n).

The remaining 3 segments in each of the 4 v_2-i_2 curves in Fig. 2(b) can be realized by connecting three appropriate i_1-controlled concave resistors in parallel with the 3-element network realized so far, as shown in Fig. 2(c). The characterizing conductance and voltage-intercept functions $G_9(\cdot)$, $E_9(\cdot)$; $G_{10}(\cdot)$, $E_{10}(\cdot)$; and $G_{11}(\cdot)$, $E_{11}(\cdot)$ are easily computed from the prescribed curves in Fig. 2(b) and are shown in Figs. 3(o) to (t), respectively.

The complete model shown in Fig. 2(c) clearly simulates the prescribed characteristic curves in Figs. 2(a) and (b) exactly. Since no restriction has so far been imposed, it follows that our synthesis procedure is indeed a unified approach for modeling 3-terminal devices. In general, a total combination of "n" x-controlled concave and convex resistors will be required to realize each family of characteristic curves,

element are shown in Figs. 3(b) and (c). The value of $G_2(v_2)$ for v_2 = 0,2,4, and 6 is obtained by subtracting the corresponding slope of the second segment from the slope of the first segment. The value of $E_2(v_2)$ for v_2 = 0,2,4, and 6 is equal to the voltage coordinate v_1 at each of the 4 breakpoints connecting the first two segments.

The third segment of each of the 4 prescribed v_1-i_1 curves is characterized by a negative slope and can be realized next by connecting a v_2-controlled convex resistor with a <u>negative</u> resistance function in series with the 2-element network realized so far. The resistance function $R_3(\cdot)$ and current-intercept function $I_3(\cdot)$ for this element are shown in Figs. 3(d) and (e). The value of $R_3(v_2)$ for v_2 = 0,2,4, and 6 is obtained by subtracting the reciprocal slope of the third segment associated with each v_1-i_1 curve from the reciprocal slope associated with the second segment. The value of $I_3(v_2)$ for v_2 = 0,2,4, and 6 is equal to the current coordinate i_1 at each of the 4 breakpoints connecting the second and the third segments.

The last two segments associated with each of the 4 v_1-i_1 curves can be realized in the same manner upon connecting two v_2-controlled convex resistors in series with the preceding 3-element network. The resistance function $R_4(\cdot)$ and current-intercept function $I_4(\cdot)$ are easily computed as before and are given in Figs. 3(f) and (g). Similarly, the resistance function $R_5(\cdot)$ and current intercept function $I_5(\cdot)$ are shown in Figs. 3(h) and (i).

(b) <u>Modeling the output characteristic curves $i_2 = g_2(v_2,i_1)$</u>. Since each v_2-i_2 curve has 5 breakpoints, it would be necessary to use

where n is the total number of breakpoints in each v_j-i_j curve in the family. Observe that the number of elements in the model does not depend on the number of v_j-i_j curves prescribed for each family of characteristic curves. Of course, it is up to the circuit designer to specify a sufficient number of curves since the unspecified continuum of curves will be generated automatically by the model on the basis of a linear interpolation between each pair of prescribed curves and a linear extrapolation beyond the first and last prescribed curves. The piecewise-linear functions characterizing each of the x-controlled concave and convex resistors will contain the same number of segments as the number of curves prescribed in each family of characteristic curves.

So far we have not yet discussed the family of x-controlled bi-concave and bi-convex resistors since they are used in more specialized applications, such as in the modeling of the Triac in Sec. 5, where the characteristic curves exhibit odd symmetries. On such occasions, the use of bi-concave and bi-convex resistors will obviate the need to implement the decomposition technique described in Sec. 2, while at the same time obtain a model containing half as many elements.

5. NONLINEAR DC CIRCUIT MODELS OF SEMI-CONDUCTOR DEVICES

We will now apply the black box approach presented in the preceding section to synthesize nonlinear dc circuit models of several widely used devices; namely, the bipolar transistor, the FET, the unijunction transistor, and the Triac or SCR. Due to the limitation of space, the models will be presented without much detailed discussion since the same procedure is applied in each case. The characteristic curves of each device

to be modeled will be given at the outset in piecewise-linear form. Each curve is represented by a sufficient number of segments adequate for most practical applications. If better accuracy is desired, the models presented in this section could be easily refined by adding additional x-controlled concave and convex resistors.

(a) Bipolar transistor model. Only npn transistors will be considered here since the same models would apply to pnp transistors under minor modifications [8]. The most versatile model to be proposed for the npn transistor in Fig. 4(a) is the Model A shown in Fig. 4(b). The relationship between the slope and breakpoint of each segment and the characteristic functions associated with the building blocks are indicated directly on top of the prescribed characteristic curves in Fig. 4(c) and (d). Observe that Model A is capable of simulating not only the nonlinear current gain in the active region, but also various high injection nonlinear effects such as the variation of collector output conductance in different regions of the I_C-vs.-V_{CE} plane. Among other things, Model A is capable of simulating all features possessed by the dc version of the Gummel and Poon model [13]. However, the parameters associated with Model A can be determined much more easily than that required by Gummel and Poon [13-14].

Since the dynamic range of operation of most bipolar transistors in practice usually covers only a small portion of the first quadrant, Model A may be further simplified under certain assumptions. For example, Model A reduces to Model B in Fig. 5(a) if we approximate the saturation region of the output characteristic curves in Fig. 4(d) by

a single straight line with slope G_C, as shown in Fig. 5(c), and if we delete the third segments which normally are needed only in the region of high collector voltage.

A further reduction from Model B to Model C in Fig. 5(d) is possible provided the family of input characteristic curves in Fig. 5(b) is approximated by a single curve as shown in Fig. 5(e), and provided the collector output conductance in the active region is assumed to be a constant as shown in Fig. 5(f). Model C still contains a nonlinear current-controlled current source. This element, which belongs to Category IV, may be replaced by a linear voltage-controlled current source upon decomposing the concave resistor R_1 in Fig. 5(d) into two nonlinear resistors R'_B and R''_B in the equivalent Model D shown in Fig. 5(g). The v'_B-i'_B curve for R'_B is characterized by the relation $v'_B = \frac{1}{k} I_C(i'_B)$, where k is any convenient scaling constant (Fig. 5(h)). The v''_B-i''_B curve for R''_B is chosen to take up the "slack" (Fig. 5(i)) in order that the composite v_1-i_1 curve (Fig. 5(j)) is identical to that shown in Fig. 5(e).

Another variant of Model C is the Model E shown in Fig. 5(k). The validity of this model is based on a very special observation by Gummel and Poon [13]; namely, for a large class of bipolar transistors, the collector curves in the active region when projected backwards, would all meet at a focal point as shown in Fig. 5(ℓ). This observation has been verified experimentally by this author to be approximately true for most bipolar transistors. Model E takes advantage of this property and consequently requires only the evaluation of $R_C(I_B)$ and E_C. The remaining parameters G_B, E_B, and G_C are known for various types of transistors.

With the help of a curve tracer and a straight edge, it has been found that $R_C(I_B)$ and E_C could be determined almost by inspection! Hence, Model E seems to be an excellent compromise between accuracy and simplicity in the determination of the model parameters.

(b) Field effect transistor model. Only n-channel FET will be considered here since the p-channel model would follow trivially. The most flexible model for the n-channel FET in Fig. 6(a) is the FET Model A shown in Fig. 6(b). This model is designed to simulate the prescribed characteristic curves in Figs. 6(c) and (d) exactly. It bears a strong resemblence to the npn transistor Model A of Fig. 4(b). However, a nonlinear resistor R_1 is used instead of a controlled concave resistor since the FET input characteristic curves can be approximated accurately by a single I_G-vs.-V_{GS} curve.

Model A can be simplified to Model B in Fig. 6(e) provided we approximate the first and the third segments of the family of I_D-vs.-V_{DS} curves by a single straight line each. In this case, the linear resistor $\hat{R}_{D_0}$ of Model B is used to simulate the first segment and the concave resistor R_3 of Model B is used to simulate the third segment. By a precedure dual to that used in deriving the npn transistor Model D, we can replace the nonlinear controlled source in the FET Model B by a linear controlled source to obtain the equivalent FET Model C shown in Fig. 6(f).

(c) Unijunction transistor model. This device is probably one of the more difficult ones to model since no realistic unijunction transistor model has yet existed. Using our unified approach, we obtain the unijunction transistor Model A shown in Fig. 7(b). The V_{BB}-controlled linear resistor and the nonlinear controlled source $E_B(V_{BB})$ are used to simulate

the negative resistance segment of the input characteristic curves in Fig. 7(c). The corresponding v-i curves in the fourth quadrant are clipped by the ideal diode R_2. Finally, the family of near vertical segments in Fig. 7(c) are realized by the V_{BB}-controlled convex resistor R_1. In the output portion of this model, the I_E-controlled linear resistor $\hat{R}_B$ and the I_E-controlled convex resistor R_3 are used to realize the first and the second segment, respectively, of the I_{B2}-vs.-V_{BB} output characteristic curves in Fig. 7(d).

(d) Triac model. The Triac Model A shown in Fig. 8(b) was designed to simulate the input and output characteristic curves shown in Figs. 8(c) and (d). The input portion of this model consists of a single nonlinear resistor R_1 characterized by the V_G-I_G curve shown in Fig. 8(c). The output portion of the model consists of a linear resistor $\hat{G}_A$ for simulating the segment through the origin, and an I_G-controlled bi-concave resistor R_2(in parallel with it) for simulating the odd symmetric second segments associated with the output characteristic curves in Fig. 8(d). The remaining two odd-symmetric segments are realized by connecting two I_G-controlled bi-convex resistors R_3 and R_4 in series with the parallel combination of $\hat{G}_A$ and R_2.

Since a Triac may be modeled by two SCR's connected back-to-back in parallel, the Triac Model A in Fig. 8(b) can be transformed into an SCR model upon replacing the controlled bi-concave and bi-convex resistors by controlled concave and convex resistors having identical first quadrant characteristic curves.

6. CONCLUDING REMARKS

The unified procedure described in this paper can be used to synthesize a nonlinear dc circuit model for simulating the prescribed family of input and output characteristic curves of any 3-terminal device. The only assumption we made is that each curve belonging to the family of input or output characteristic curves must be prescribed in piecewise-linear form with the same number of breakpoints. The number of circuit elements in our model is proportional to the number of breakpoints and is independent of the number of curves prescribed for each family. Our model will simulate each prescribed characteristic curve exactly. It will also simulate the continuum of characteristic curves lying between each pair of prescribed curves by assuming a uniform variation from one prescribed curve to the next. In other words, a linear interpolation between curves is automatically implemented by our model.

Some of the desirable features of our approach are: (1) our approach is applicable to the modeling of any 3-terminal device. Since the prescribed characteristic curves are simulated exactly, the only inaccuracy lies in the initial approximation used in specifying the characteristic curves, and not in the model itself. (2) Since each element in our model is responsible for realizing a specific portion of the prescribed characteristic curves, it is often possible to simplify a given model by deleting those elements which do not affect the region of the characteristic curves covered by the dynamic range of operation. (3) The characteristic functions and circuit parameters associated with the circuit model could be determined directly from the slope and breakpoint of

the characteristic curves. No involved calculation or computer optimization techniques are needed.

Some of the undesirable features of our approach are: (1) the elements in the model do not bear any physical or geometrical relationship with the device. This is a distinct disadvantage in the design of integrated circuits when the effect of doping and other manufacturing parameters must be carefully controlled through computer simulation. (2) Ours is strictly a dc model. The extension to include high frequency characteristics does not seem to be feasible at this time. (3) In order to use our model efficiently, new computer programs must be developed to allow the building blocks listed in Table 1. This objection is not serious, however, since the simplicity and accuracy of our model should justify the inclusion of these building blocks in future circuit analysis programs.

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10. L. O. Hill, D. O. Pederson, and R. S. Pepper, "Synthesis of electronic bistable circuits," IEEE Trans. on Circuit Theory, vol. 10, March 1963, pp. 25-35.

11. W. J. McCalla and W. G. Howard, Jr., "BIAS-3 - A program for the non-linear dc analysis of bipolar transistor circuits," IEEE J. Solid State Circuits, vol. 6, February 1971, pp. 14-19.

12. T. E. Idleman, F. S. Jenkins, W. J. McCalla and D. O. Pederson, "SLIC - A simulator for linear integrated circuits," IEEE J. Solid State Circuits, vol. 6, August 1971, pp. 188-203.

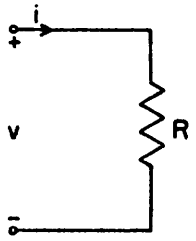
13. A. K. Gummel and H. C. Poon, "An integral charge control model of bipolar transistors," Bell System Tech. J., May-June 1970, pp. 827-852.

14. R. Rohrer, S. P. Fan and L. Claudio, "Automated bipolar junction transistor dc model parameter determination, IEEE J. of Solid State Circuits, vol. 6, August 1971, pp. 260-262.

LIST OF TABLE AND FIGURE CAPTIONS

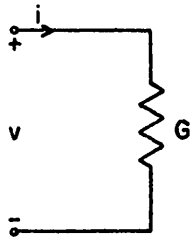
I. Linear Resistors and Controlled Sources

(a) linear resistor



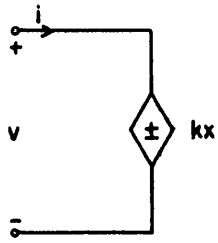
$v = Ri$

(b) linear conductor



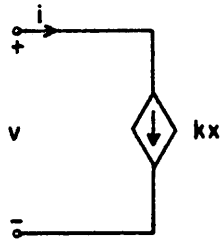
$i = Gv$

(c) linear controlled voltage source



$v = kx$

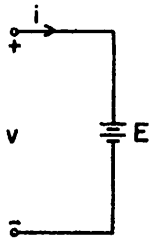
(d) linear controlled current source



$i = kx$

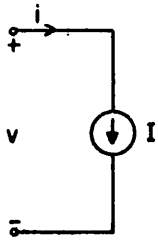
II. Independent Sources and Nonlinear Resistors

(a) voltage source



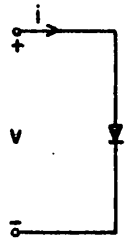
$v = E$

(b) current source



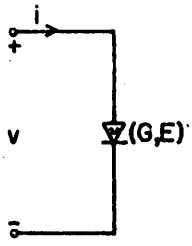
$i = I$

(c) ideal diode



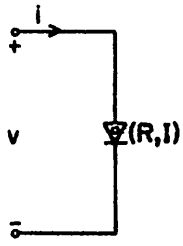
$v = 0, i \geq 0$
$i = 0, v < 0$

(d) concave resistor



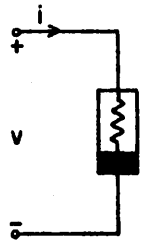
$i = G(v-E), v \geq E$
$= 0, v < E$

(e) convex resistor



$v = R(i-I), i \geq I$
$= 0, i < I$

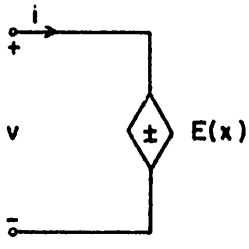
(f) nonlinear resistor



$f(v,i) = 0$

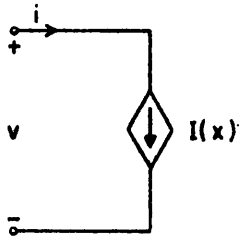
III. Nonlinear Controlled Sources and Controlled Linear Resistors

(a) x-controlled voltage source



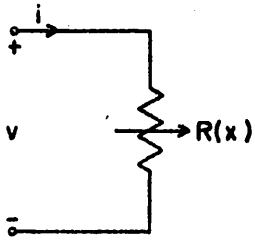
$v = E(x)$

(b) x-controlled current source



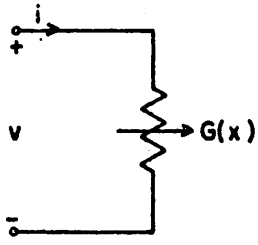
$i = I(x)$

(c) x-controlled linear resistor



$v = R(x)i$

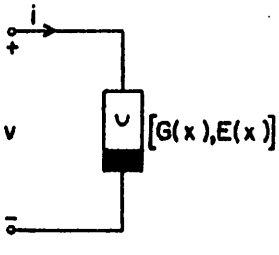
(d) x-controlled linear conductor



$i = G(x)v$

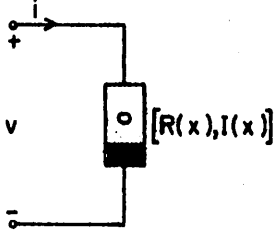
IV. Controlled Nonlinear Resistors

(a) x-controlled concave resistor



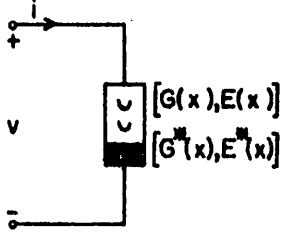
$i = G(x)u_{\circ}(v-E(x))$

(b) x-controlled convex resistor



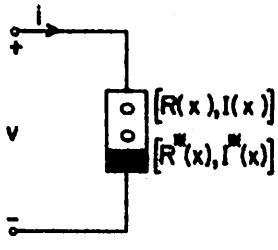
$v = R(x)u_{\circ}(i-I(x))$

(c) x-controlled bi-concave resistor



$i = G(x)u_{\circ}(v-E(x))$
$+ G^{*}(x)u^{*}{}_{\circ}(v+E^{*}(x))$

(d) x-controlled bi-convex resistor



$v = R(x)u_{\circ}(i-I(x))$
$+ R^{*}(x)u^{*}{}_{\circ}(i+I^{*}(x))$

TABLE I

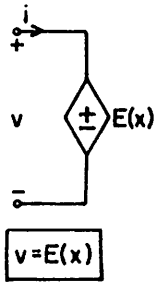
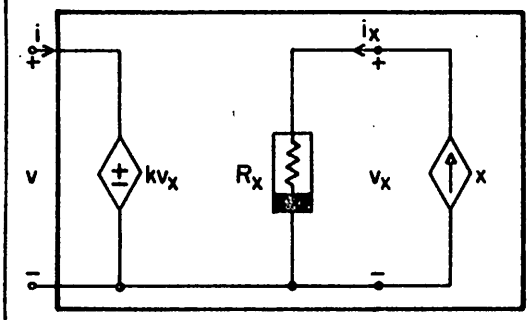
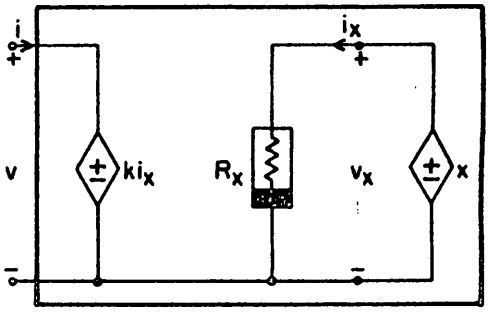
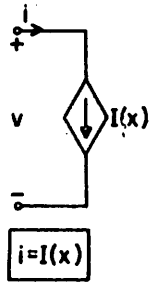
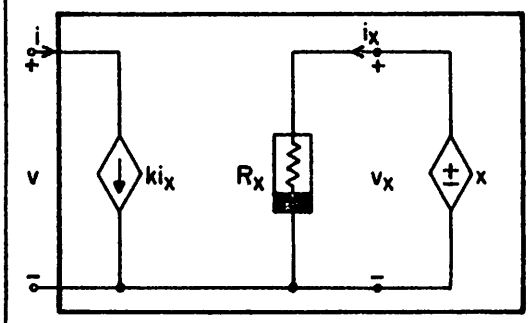
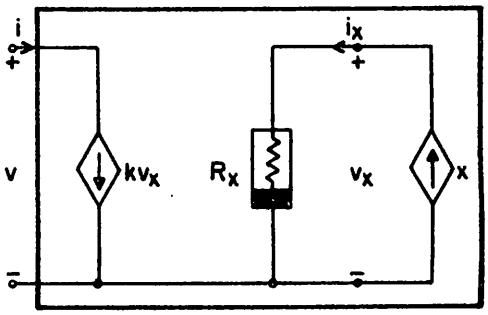
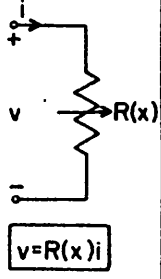
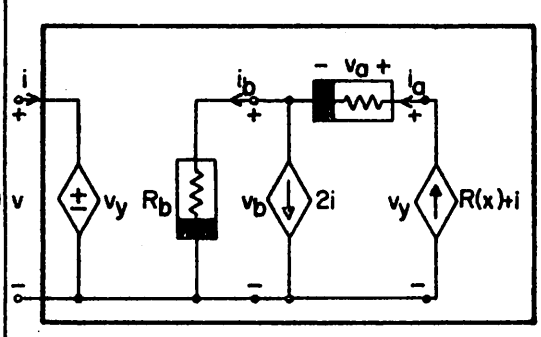
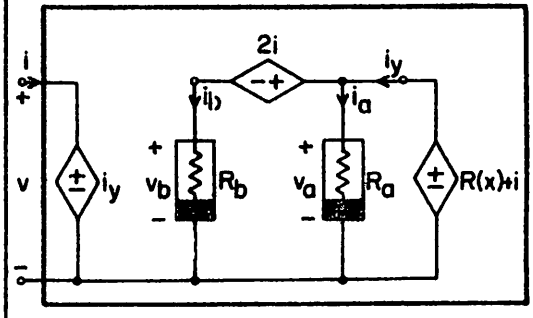
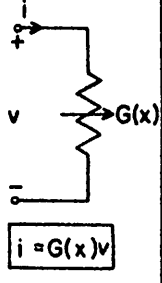
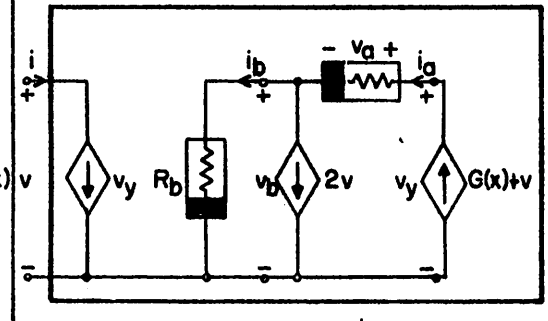
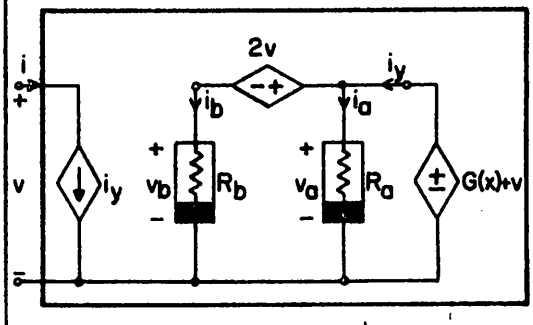
NAME AND SYMBOL	CIRCUIT MODEL 1	CIRCUIT MODEL 2
1. x-controlled voltage source  	 v_x-i_x curve for R_x: $v_x = \frac{1}{k} E(i_x)$	 v_x-i_x curve for R_x: $i_x = \frac{1}{k} E(v_x)$
2. x-controlled current source  	 v_x-i_x curve for R_x: $i_x = \frac{1}{k} I(v_x)$	 v_x-i_x curve for R_x: $v_x = \frac{1}{k} I(i_x)$
3. x-controlled linear resistor  	 v_a-i_a curve for R_a: $v_a = \frac{1}{4} i_a^2$ v_b-i_b curve for R_b: $v_b = -\frac{1}{4} i_b^2$	 v_a-i_a curve for R_a: $i_a = \frac{1}{4} v_a^2$ v_b-i_b curve for R_b: $i_b = -\frac{1}{4} v_b^2$
4. x-controlled linear conductor  	 v_a-i_a curve for R_a: $v_a = \frac{1}{4} i_a^2$ v_b-i_b curve for R_b: $v_b = -\frac{1}{4} i_b^2$	 v_a-i_a curve for R_a: $i_a = \frac{1}{4} v_a^2$ v_b-i_b curve for R_b: $i_b = -\frac{1}{4} v_b^2$

TABLE 2

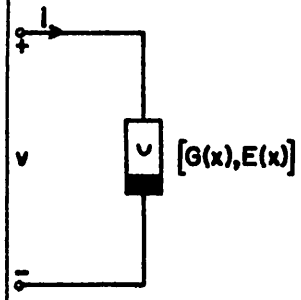
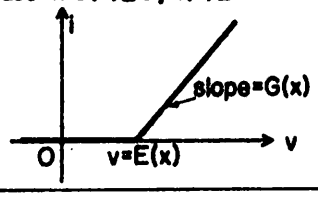
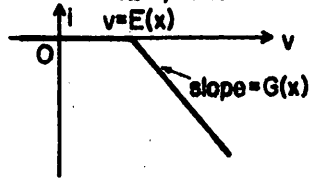
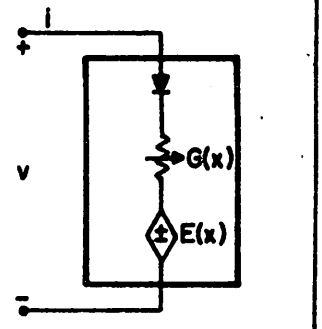
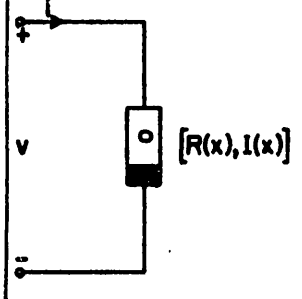
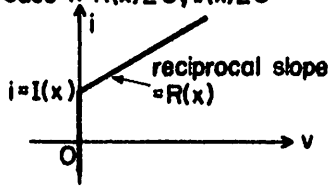
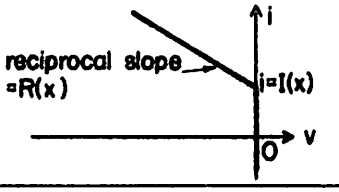
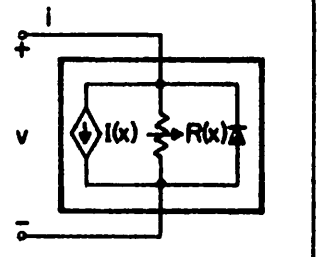
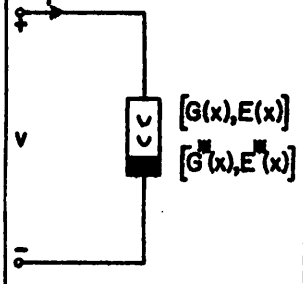
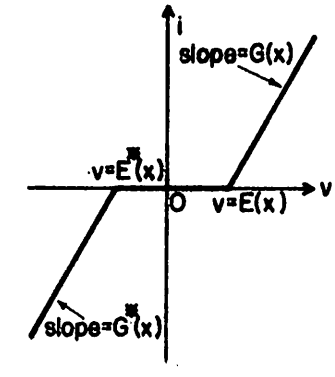
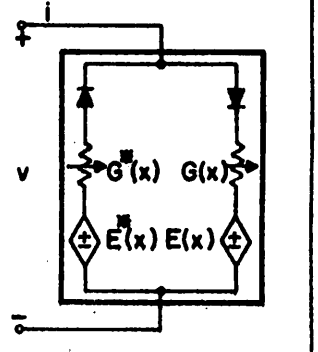
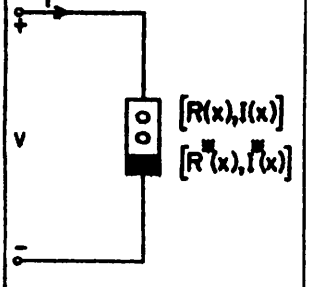
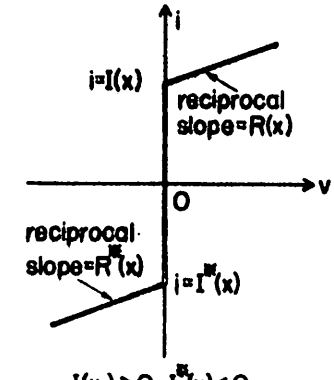
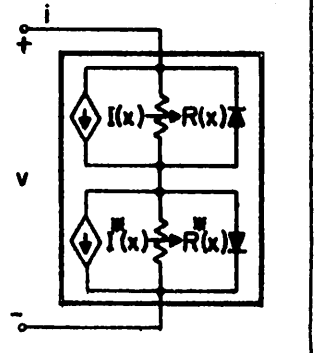
Name and Symbol	v-i Curves as Function of Parameter x	Mathematical Model	Circuit Model
1. x-controlled concave resistor 	Case 1: G(x)≥0, E(x)≥0  Case 2: G(x)≤0, E(x)≥0 	$i=G(x)u_{\bullet}(v-E(x))$ where $u(\bullet)$ is the unit ramp function: $u(z)=z, z\geq 0$ $=0, z<0$	 $G(x)\geq 0, E(x)\geq 0$
2. x-controlled convex resistor 	Case 1: R(x)≥0, I(x)≥0  Case 2: R(x)≤0, I(x)≥0 	$v=R(x)u_{\bullet}(i-I(x))$ where $u(\bullet)$ is the unit ramp function: $u(z)=z, z\geq 0$ $=0, z<0$	 $R(x)\geq 0, I(x)\geq 0$
3. x-controlled bi-concave resistor 	 $E(x)\geq 0, E^{*}(x)\leq 0$	$i=G(x)u_{\bullet}(v-E(x))+G^{*}(x)u^{*}_{\bullet}(v+E^{*}(x))$ where $u(\bullet)$ is the unit ramp function: $u(z)=z, z\geq 0$ $=0, z<0$ and where: $u^{*}(z)=-u(-z)$	 $E(x)\geq 0, E^{*}(x)\leq 0$
4. x-controlled bi-convex resistor 	 $I(x)\geq 0, I^{*}(x)\leq 0$	$v=R(x)u_{\bullet}(i-I(x))+R^{*}(x)u^{*}_{\bullet}(i+I^{*}(x))$ where $u(\bullet)$ is the unit ramp function: $u(z)=z, z\geq 0$ $=0, z<0$ and where: $u^{*}(z)=-u(-z)$	 $I(x)\geq 0, I^{*}(x)\leq 0$

TABLE 3

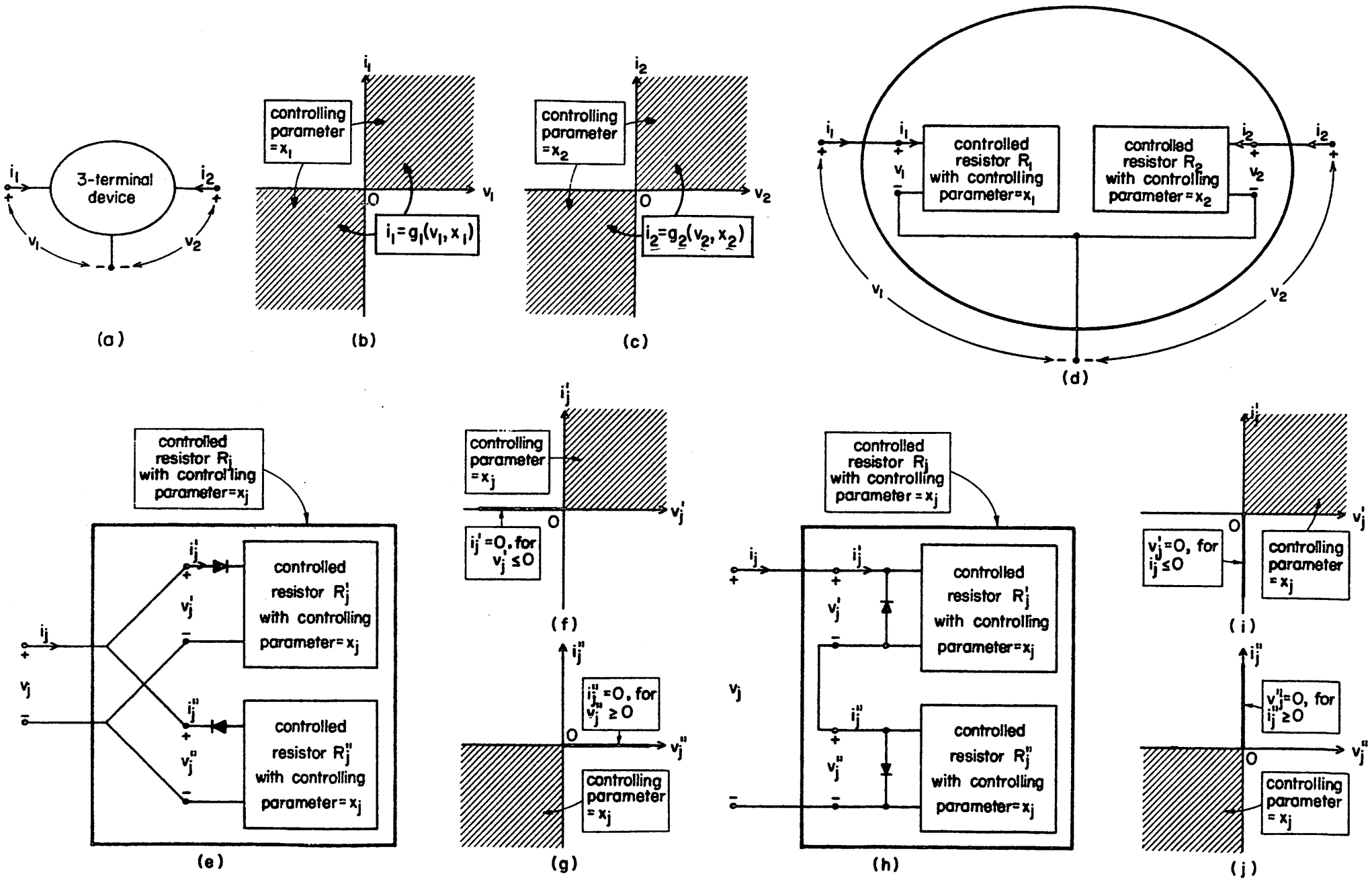
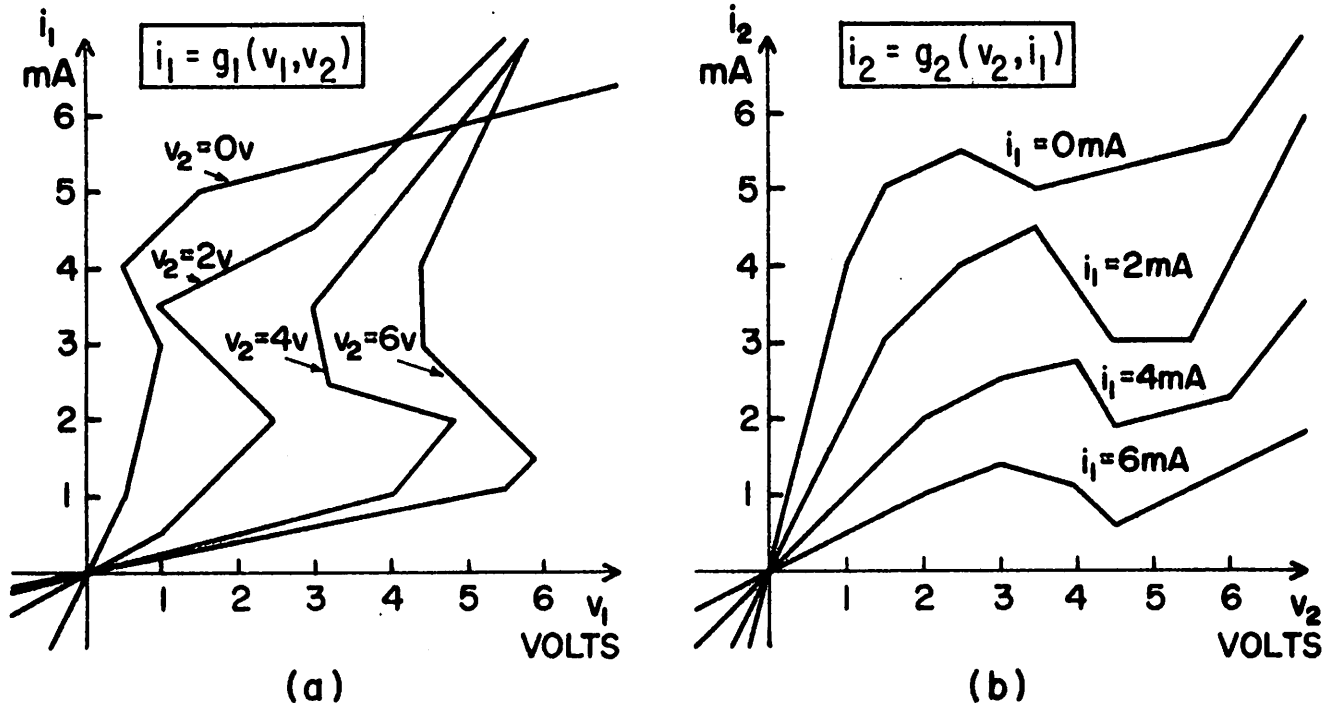

3-terminal device
controlling parameter = x1
controlling parameter = x2
i1 = g1(v1, x1)
i2 = g2(v2, x2)
controlled resistor R1 with controlling parameter = x1
controlled resistor R2 with controlling parameter = x2
controlled resistor Rj with controlling parameter = xj
controlled resistor R'j with controlling parameter = xj
controlled resistor R''j with controlling parameter = xj
i'j = 0, for v'j ≤ 0
i''j = 0, for v''j ≥ 0
v'j = 0, for i'j ≤ 0
v''j = 0, for i''j ≥ 0
(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
(i)
(j)

FIGURE 1


i_1
mA
$i_1 = g_1(v_1, v_2)$
v_2=0v
v_2=2v
v_2=4v
v_2=6v
v_1
VOLTS
(a)
i_2
mA
$i_2 = g_2(v_2, i_1)$
i_1=0mA
i_1=2mA
i_1=4mA
i_1=6mA
v_2
VOLTS
(b)

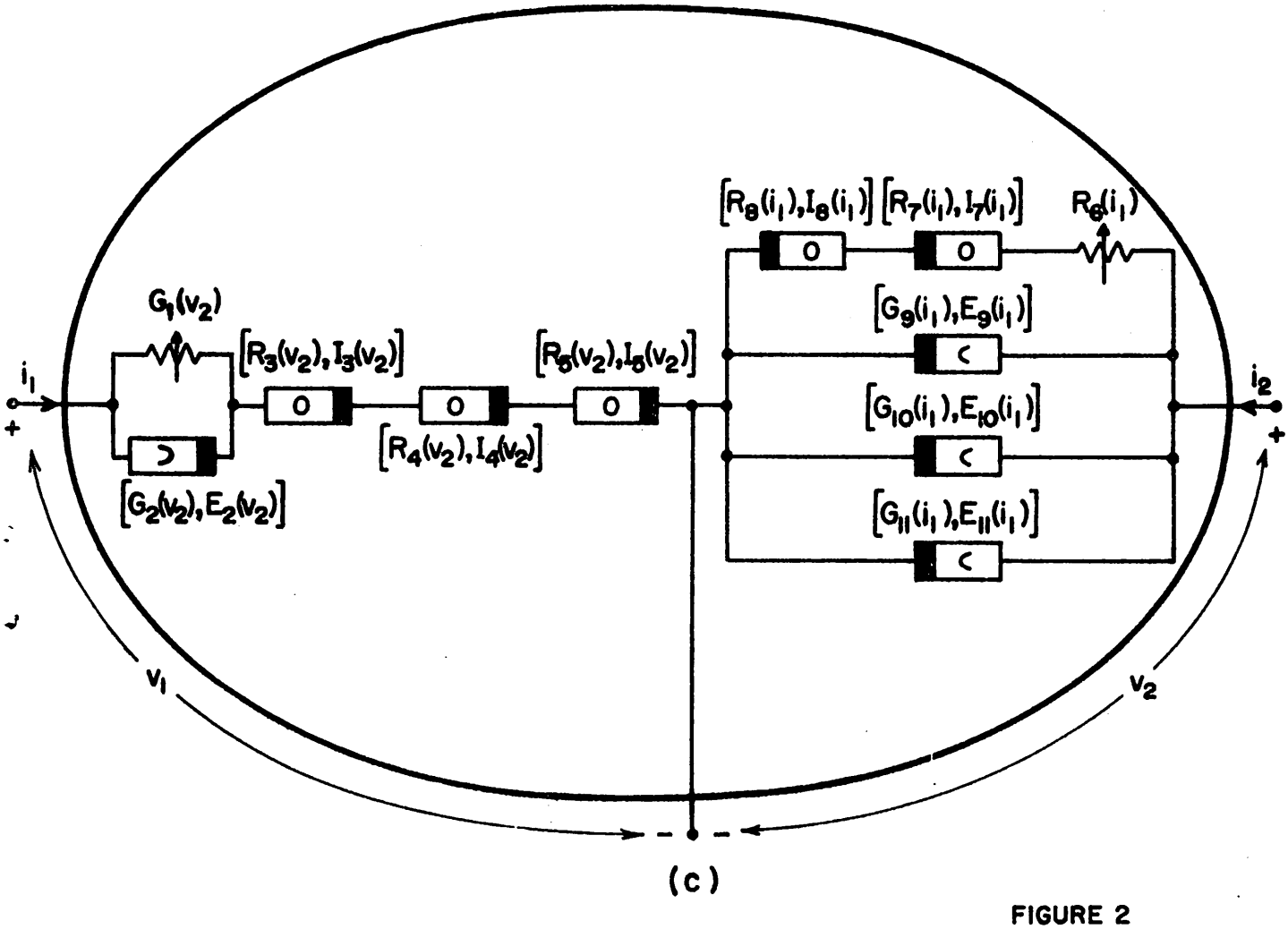

$G_1(v_2)$
$[R_3(v_2), I_3(v_2)]$
$[R_5(v_2), I_5(v_2)]$
$[R_8(i_1), I_8(i_1)]$
$[R_7(i_1), I_7(i_1)]$
$R_6(i_1)$
$[G_9(i_1), E_9(i_1)]$
$[G_{10}(i_1), E_{10}(i_1)]$
$[G_{11}(i_1), E_{11}(i_1)]$
i_1
i_2
$[R_4(v_2), I_4(v_2)]$
$[G_2(v_2), E_2(v_2)]$
v_1
v_2
(c)

FIGURE 2

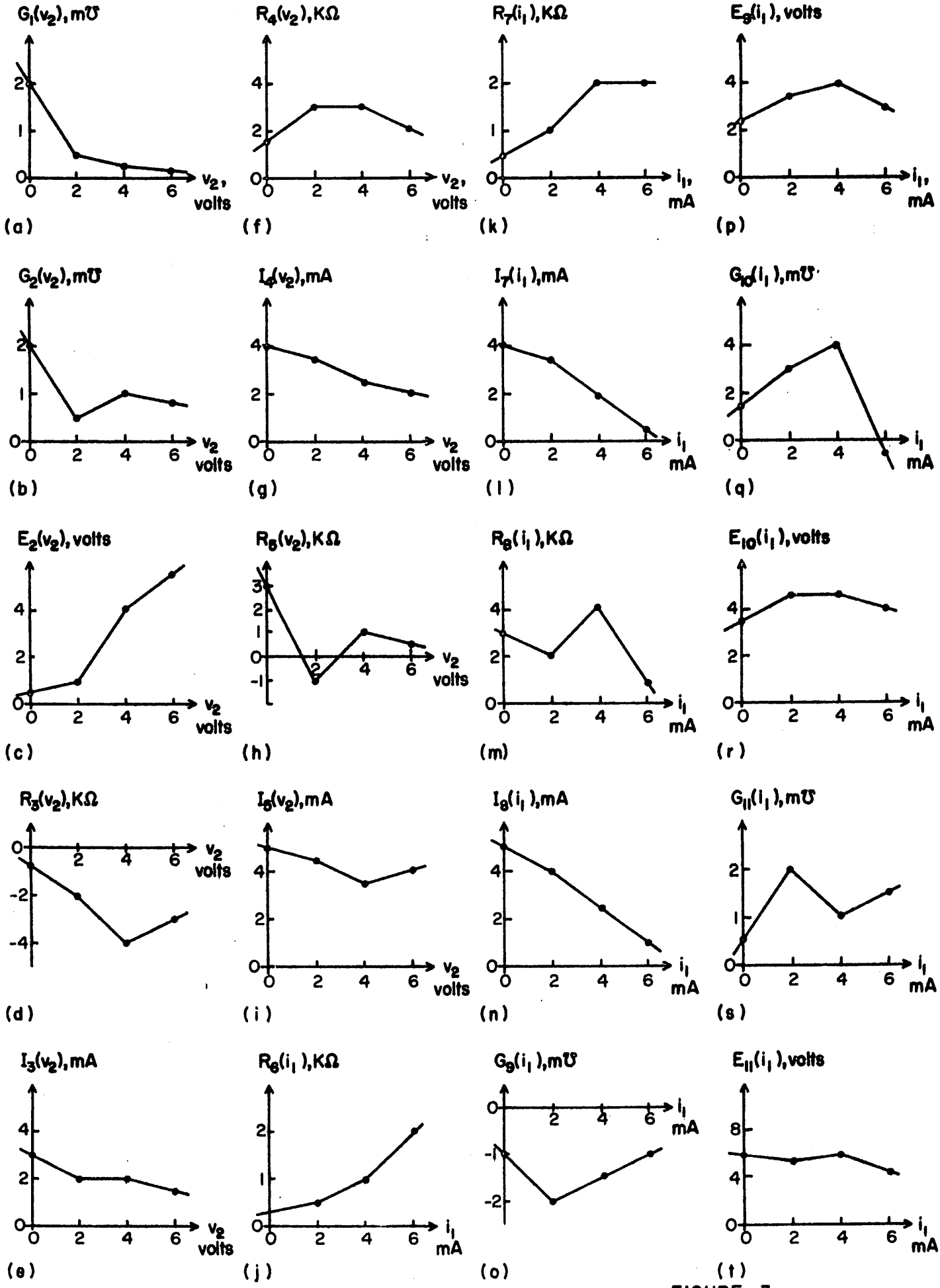
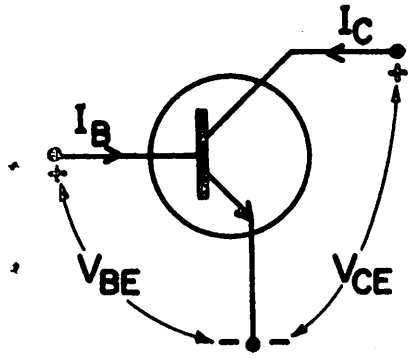
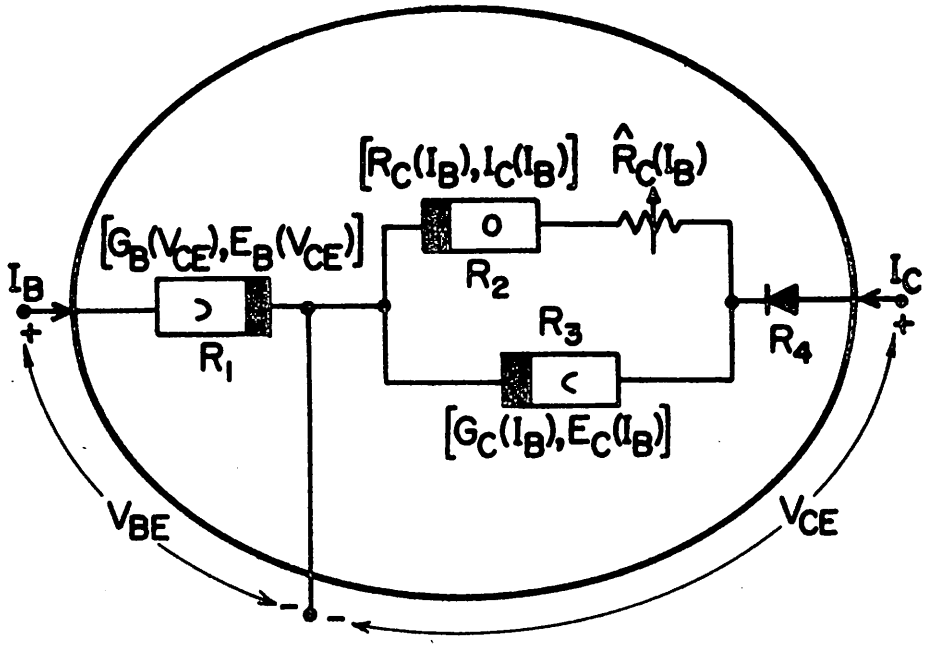

$G_1(v_2)$, m℧
v_2, volts
(a)
$R_4(v_2)$, KΩ
v_2, volts
(f)
$R_7(i_1)$, KΩ
i_1, mA
(k)
$E_9(i_1)$, volts
i_1, mA
(p)
$G_2(v_2)$, m℧
v_2 volts
(b)
$I_4(v_2)$, mA
v_2 volts
(g)
$I_7(i_1)$, mA
i_1 mA
(l)
$G_{10}(i_1)$, m℧
i_1 mA
(q)
$E_2(v_2)$, volts
v_2 volts
(c)
$R_5(v_2)$, KΩ
v_2 volts
(h)
$R_8(i_1)$, KΩ
i_1 mA
(m)
$E_{10}(i_1)$, volts
i_1 mA
(r)
$R_3(v_2)$, KΩ
v_2 volts
(d)
$I_5(v_2)$, mA
v_2 volts
(i)
$I_8(i_1)$, mA
i_1 mA
(n)
$G_{11}(i_1)$, m℧
i_1 mA
(s)
$I_3(v_2)$, mA
v_2 volts
(e)
$R_6(i_1)$, KΩ
i_1 mA
(j)
$G_9(i_1)$, m℧
i_1 mA
(o)
$E_{11}(i_1)$, volts
i_1 mA
(t)

FIGURE 3

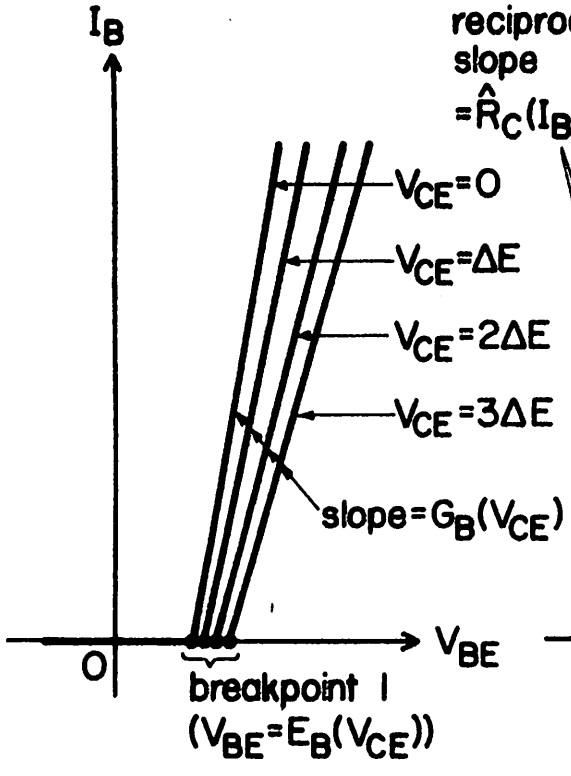


(a)

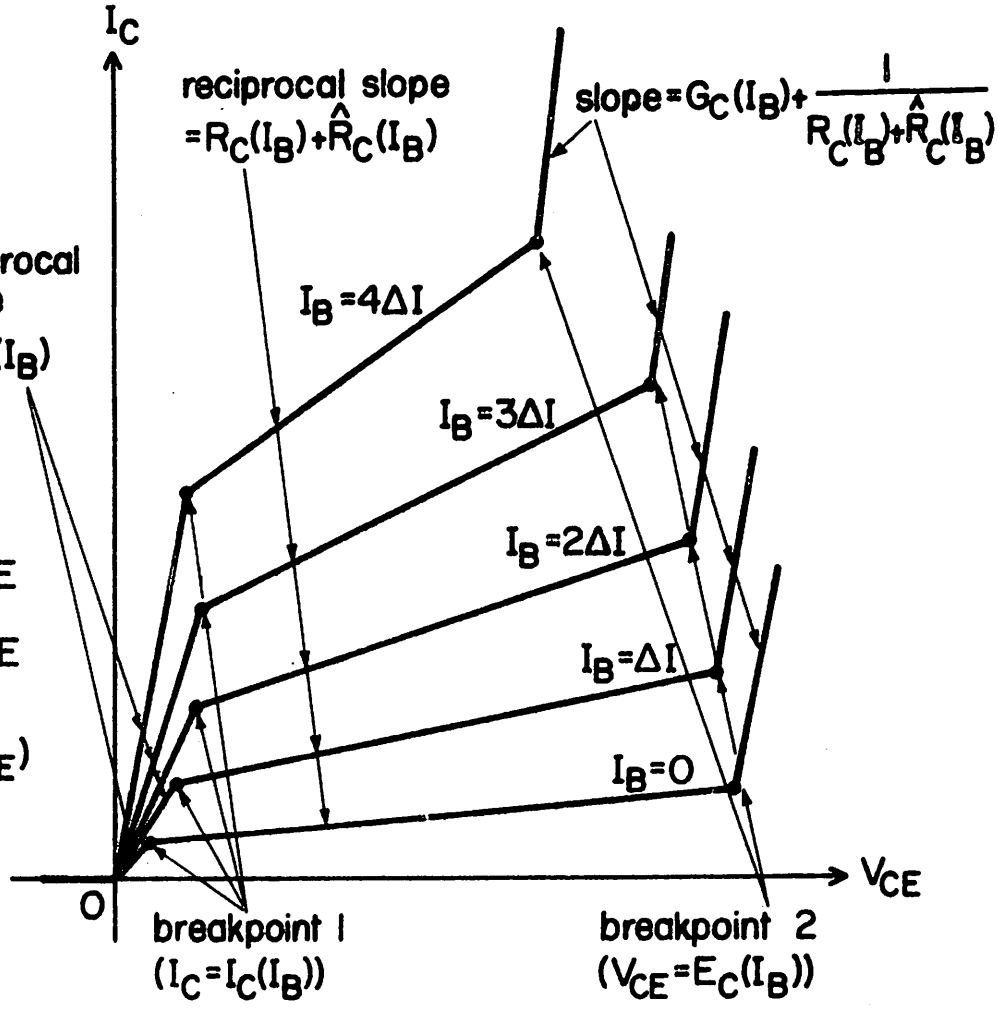
npn TRANSISTOR



(b) MODEL A



(c)



(d)

FIGURE 4

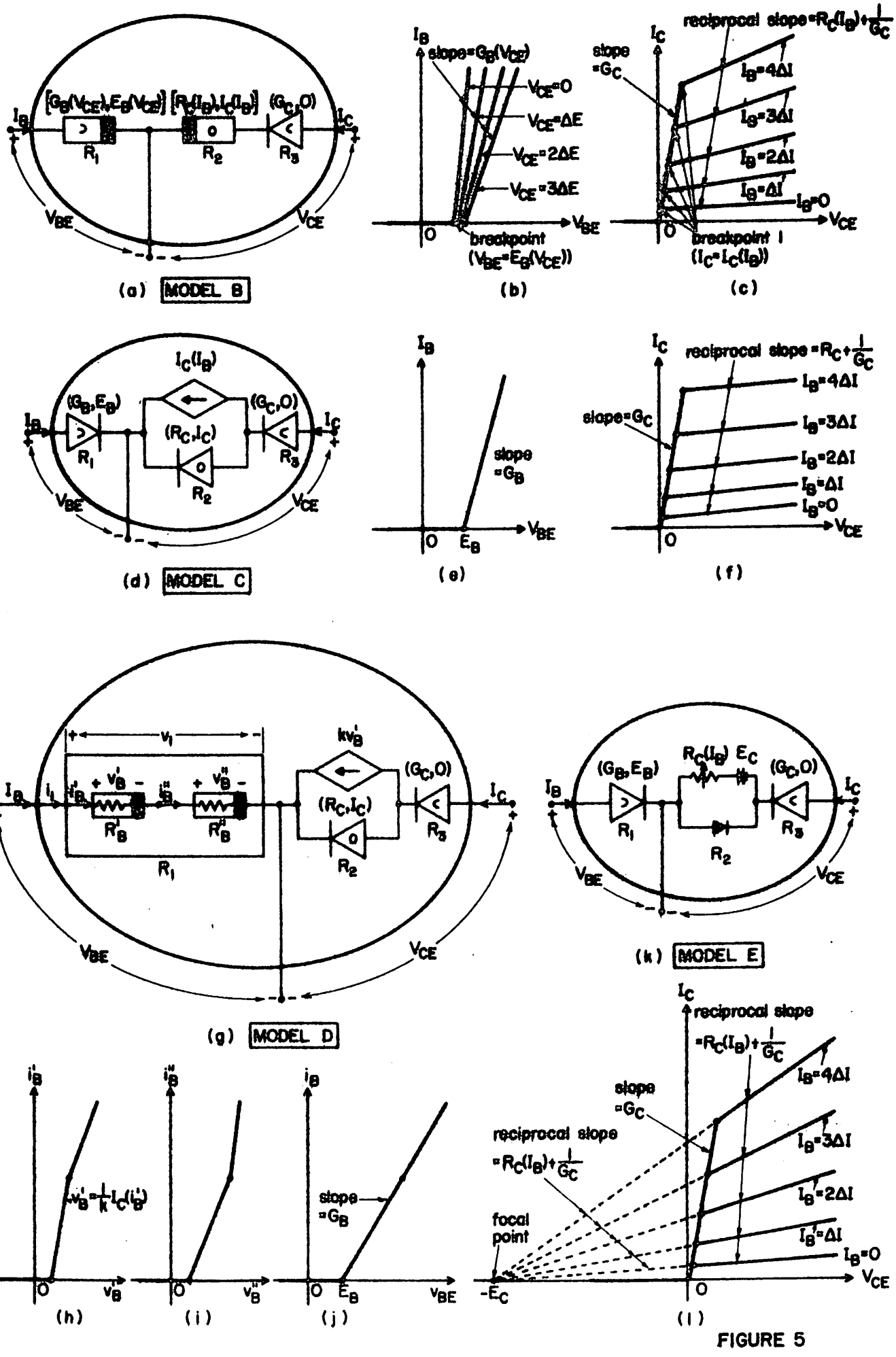
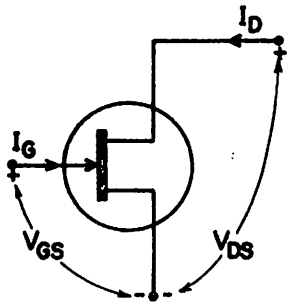
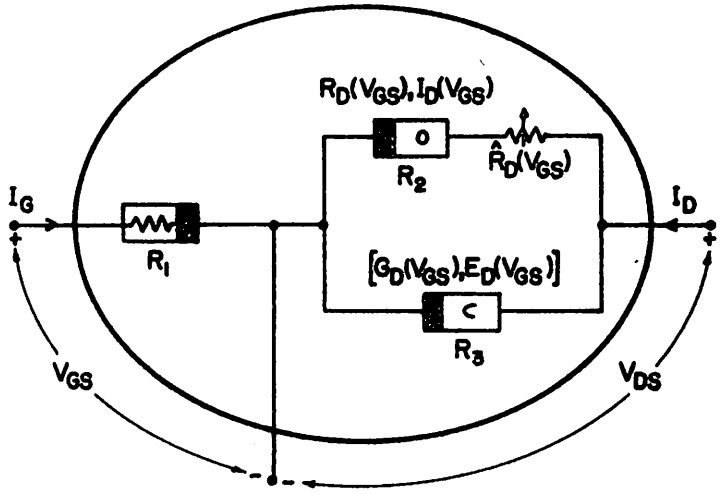


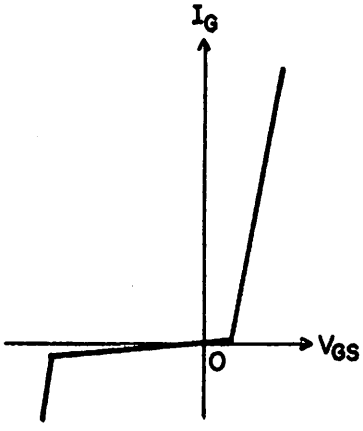
FIGURE 5



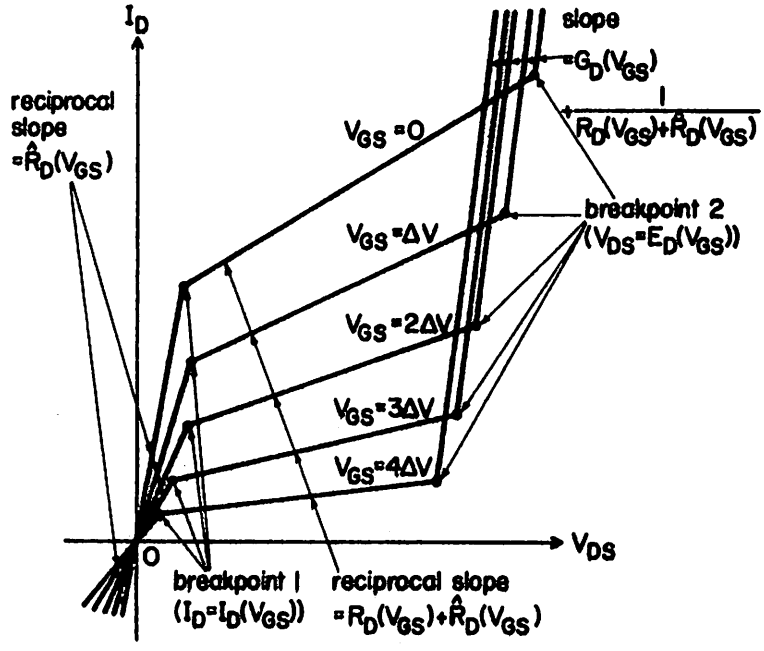
(a)
n-CHANNEL
FET



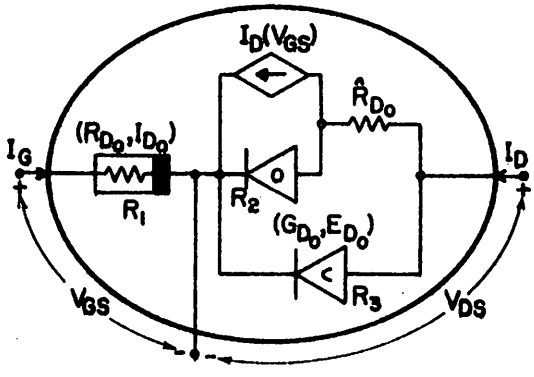
(b) MODEL A



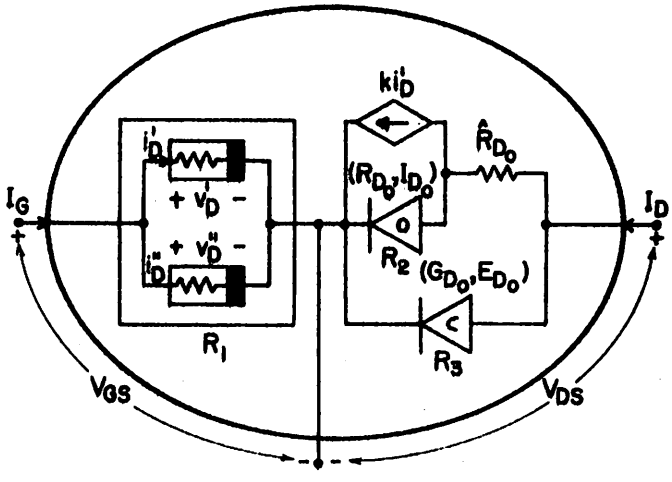
(c)



(d)

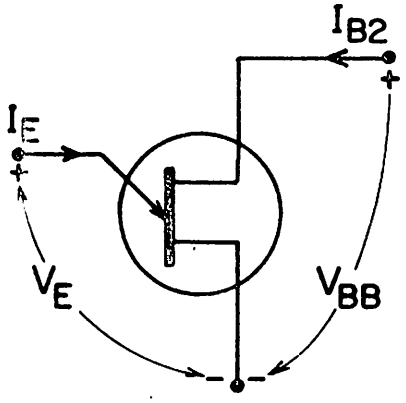


(e) MODEL B

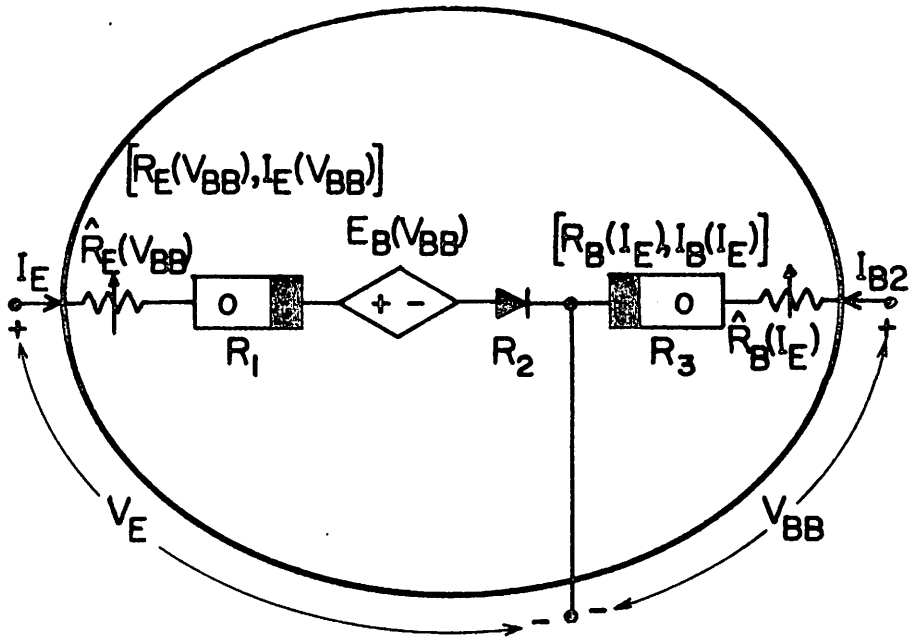


(f) MODEL C

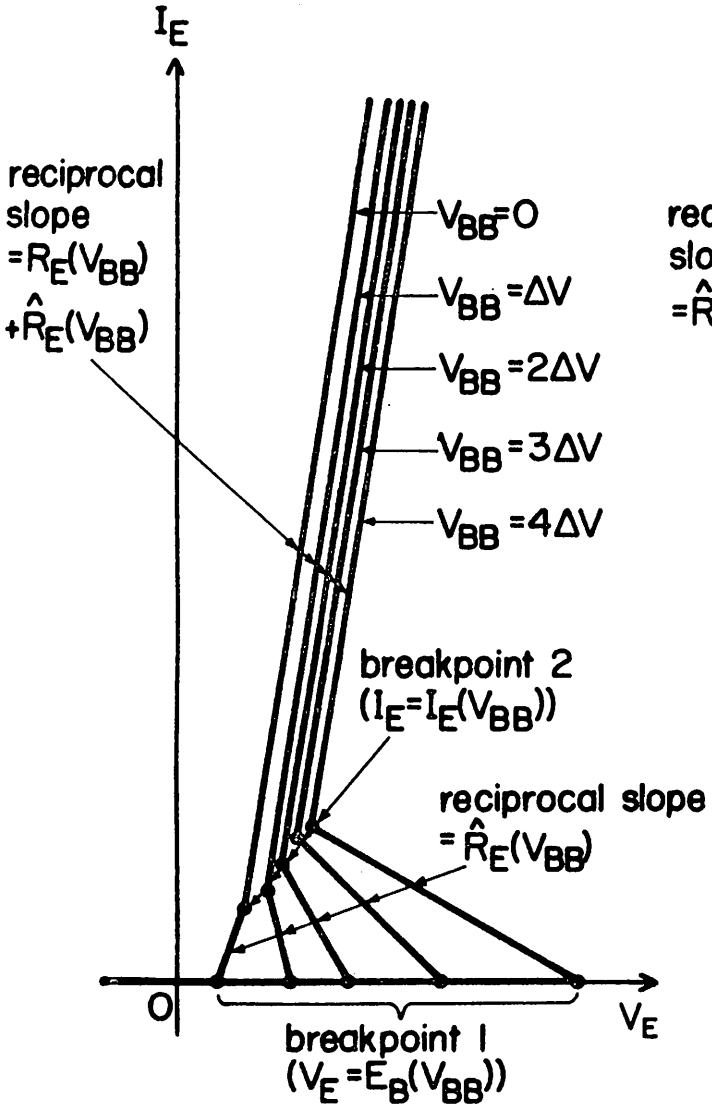
FIGURE 6



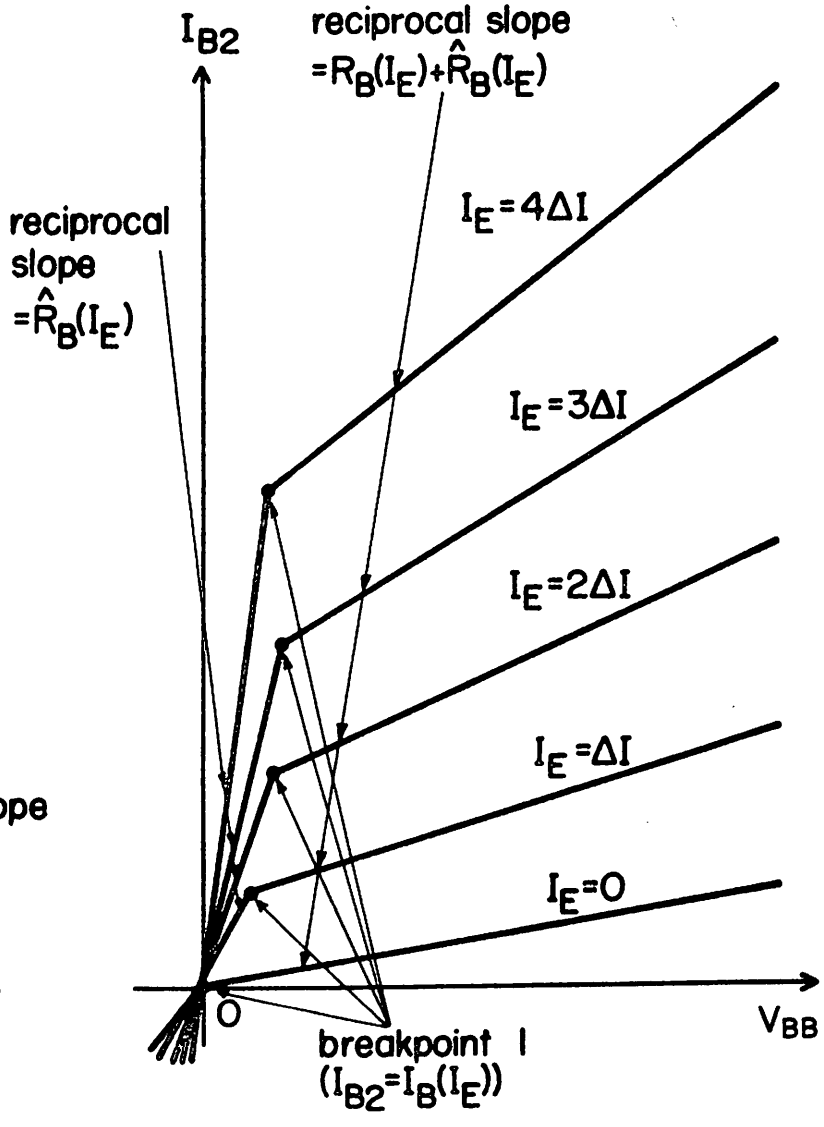
(a)
UNIJUNCTION
TRANSISTOR



(b) MODEL A

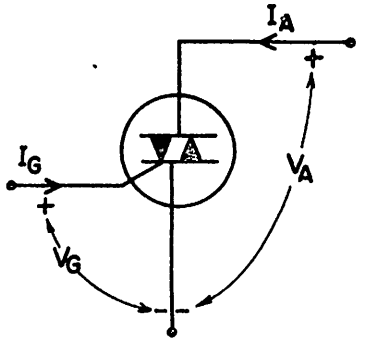


(c)

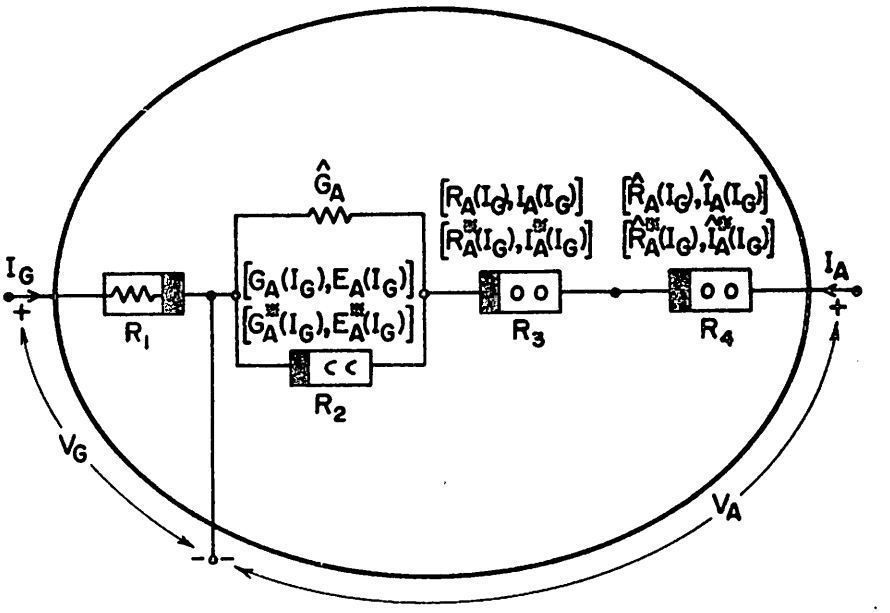


(d)

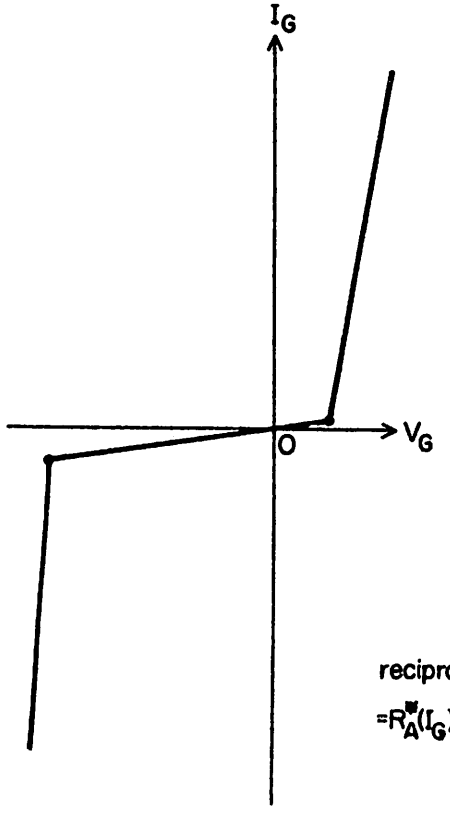
FIGURE 7



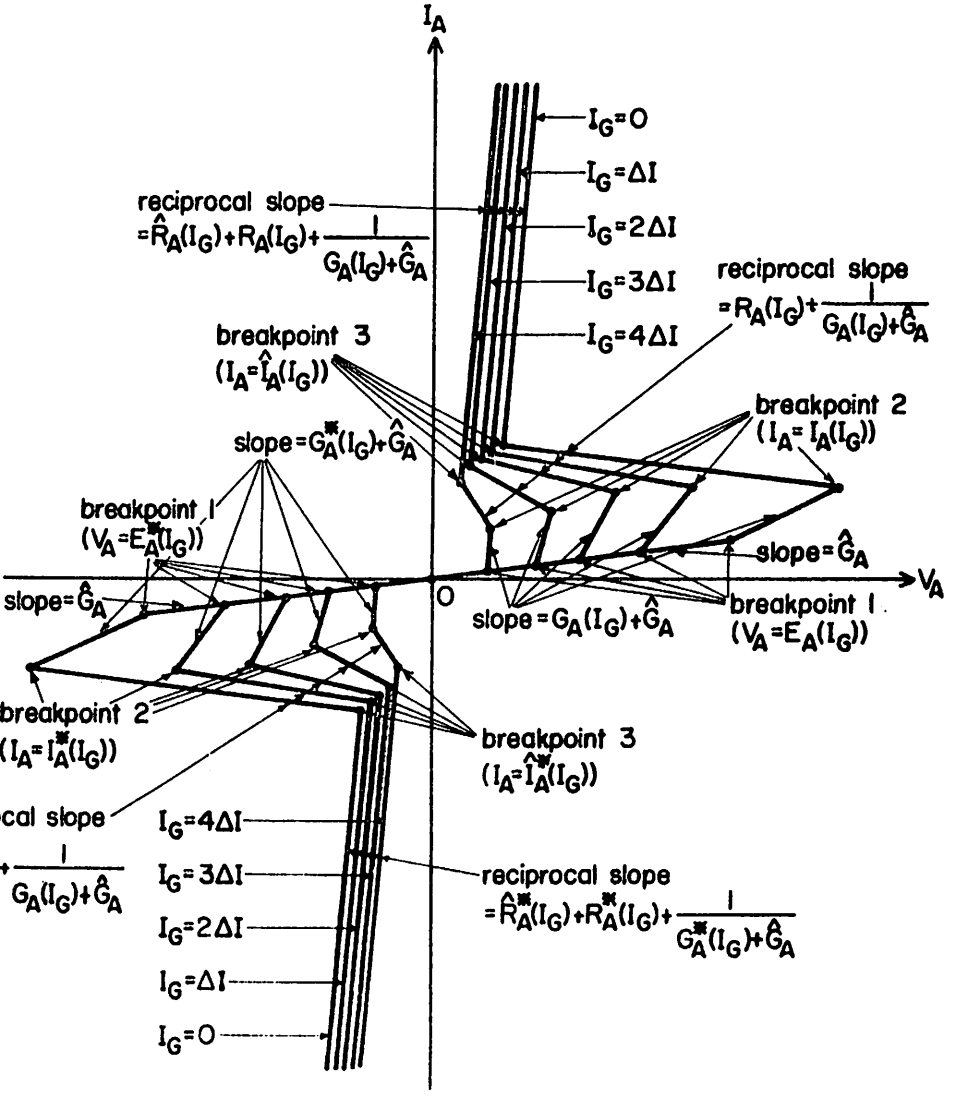
(a) TRIAC



(b) MODEL A



(c)



(d)

FIGURE 8