OPTIMUM DESIGN OF INTEGRATED VARIABLE-GAIN AMPLIFIERS

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ABSTRACT

The design of an integrated wideband variable-gain amplifier with maximum dynamic range is approached by considering all possible bipolar transistor configurations that realize this function. Three configurations are shown to be basic in that all others can be derived from them, and these three are analysed for distortion and noise performance. A generalized analysis shows the importance of transistor base resistance in determining distortion and noise in all three circuits.

On the basis of these analyses, one configuration is shown to yield maximum dynamic range and this configuration is then used as the basis for the development of a new circuit called the improved agc amplifier. This circuit gives the highest dynamic range that can be achieved with bipolar transistors if given limits of distortion and noise are not to be exceeded over the whole dynamic range. The circuit consists of a quadruple of transistors driven by an input pair. A unique biasing scheme allows a considerable reduction in distortion and noise together with a significant increase in bandwidth compared with conventional circuits. In addition, high frequency feedthrough is minimized.

Using transistors with base resistances of 105Ω and 65Ω (double base) and unity-gain frequency of 210 MHz, the improved

agc amplifier is shown to yield a dynamic range of 33 dB at 70 MHz for a signal-to-noise ratio of 40 dB (Δf = 4.5 MHz). This is only 1.5 dB below the calculated value but approximately 20 dB better than the performance that can be achieved using existing circuits and the same devices. The bandwidth obtained is 120 MHz and is limited by feedthrough at 31 dB attenuation.

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TABLE OF CONTENTS.

CHAPTER 1.

INTRODUCTION.

Variable-gain amplifiers are used as automatic-gain-control amplifiers or as electronically programmable attenuators. In the former case, the dc signal that controls the gain of the amplifier is derived from the output signal such that for any input signal level the amplitude of the output signal is kept constant. In the latter case, the amplitude of the output signal is set directly by the dc control signal.

A useful figure of merit for a variable-gain amplifier is its dynamic range over a given frequency range. This is defined as the ratio of the maximum to minimum signal that can be handled within specific limits of distortion and noise. Distortion is thus examined for most variable-gain circuits at low frequencies in Chapter 2 and at high frequencies in Chapter 3. Approximative expressions are presented that describe distortion well under low-distortion conditions. They are derived from power-series expansions at low frequencies and from Volterra-series expansions at high frequencies. Ample computational and experimental justification is included. Noise is studied in Chapter 4. The noise exhibited by the variable-gain circuits is represented by analytical expressions which have been verified by means of computer-aided analysis programs. This study has thus made possible the prediction of the distortion and noise performance of most variable-gain amplifiers at both low and high frequencies.

The analyses described above have made possible the optimum design of an integrated variable-gain amplifier. Considerations are restricted to balanced circuit configurations because of the resulting cancellation of even-order distortion. Input and output ports are differential. Input and output impedances are independent of amplifier gain. In order to reduce the noise contribution from following stages, the maximum gain is larger than unity and is typically about 15 dB. This automatically excludes varioloss circuits. No additional pre or post amplifiers are included since they only shift the gain range without affecting the dynamic range. Finally the circuit realization performs over a wide frequency range and is integrated by standard six-mask processing. No lateral-pnp transistors appear in the signal path.

Three basic variable-gain configurations are first identified and investigated. They are designated by the agc amplifier [3], the multiplier [2] and Gilbert's quad [1]. Applying the results of Chapters 2,3 and 4, they are optimized for dynamic range and compared with one another in Chapter 5. This results in the design and realization of an improved variable-gain amplifier in integrated form. Its performance is predicted and verified experimentally by means of two different integrated circuit realizations.

In Chapter 6, the integration process is presented in

detail. The improved variable-gain amplifier is biased such that its performance can be optimized depending on its application. Special attention is paid to the layout and characterization of the integrated transistors. Accurate measurement of base resistance, unity-gain frequency and junction capacitances has been investigated. In particular, the circle-diagram method used to estimate the value of base resistance has been revised and a new technique, the phase-cancellation method, has been developed [8] .

Finally, a summary of the results and conclusions is given in Chapter 7.

CHAPTER 2.

ANALYSIS OF DISTORTION IN VARIABLE-GAIN AMPLIFIERS AT LOW FREQUENCIES.

2.1 INTRODUCTION

In this chapter, all possible variable-gain amplifiers within the specifications already given, are analyzed and compared for low frequency distortion. The simplest circuit consists of a single transistor. This is followed by a discussion of the various configurations possible, using a differential pair. Finally, using the results, the three most useful configurations are discussed. These consist of transistor quads and are designated as the age amplifier [3], the multiplier [2] and Gilbert's variable-gain quad [1].

Before discussing these circuits in detail, the definitions of distortion are first reviewed and the relationships between the various kinds of distortion are shown.

2.2 INTRODUCTION TO DISTORTION

At low frequencies the output $y(t)$ of an amplifier can be expressed in terms of its input $u(t)$ by a power series

$$y(t) = a_1 \; u(t) + a_2 \, (u(t))^2 + a_3 \; (u(t))^3 + \ldots \qquad \ldots (2.1)$$

Coefficient a_1 represents the linear gain of the amplifier, whereas coefficients a_2 , a_3 ... represent its distortion.

Applying a cosine wave of frequency ω and amplitude V at the input of that amplifier yields output components at all multiples

of ω. The nth harmonic distortion (HD_n) is defined as the ratio of the component at frequency $n\omega$ to the one at the fundamental ω. It is obtained by trigonometric manipulation [5]. Under low-distortion conditions only second and third-order distortion components are considered. Expression (2.1) becomes then

$$y(t) = (a_1 + \frac{3}{4} a_3 V^2) V \cos \omega t + \frac{a_2}{2} V^2 \cos 2\omega t + \frac{a_3}{4} V^3 \cos 3 \omega t + \ldots \quad \ldots (2.2)$$

Odd-order distortion thus modifies the signal component at the fundamental frequency. This can be neglected however under low-distortion conditions. Harmonic distortion is then specified by

$$HD_2 = \frac{1}{2} \frac{a_2}{a_1} V \quad \ldots (2.3)$$

and

$$HD_3 = \frac{1}{4} \frac{a_3}{a_1} V^2 \quad \ldots (2.4)$$

It is very important to note that HD_2 is proportional to V and HD_3 to V^2. Low-distortion conditions apply for values of V where this holds true.

Phase inversion of the input signal changes the sign of the fundamental and third-order component but not of the second-order component. This is exploited in a balanced circuit, to which two input signals of opposite phase but equal amplitude are applied. The difference of the output signals does not contain even-order distortion if no imbalance is caused by mismatch.

If coefficients a_3 and a_1 have the same sign, the third-harmonic component adds in phase with the fundamental such that the resultant waveform looks expanded [5]. If a_3 and a_1 have opposite signs, the output waveform appears to be compressed. Obviously compression and expansion can cancel each other, which gives rise to a null in third-order distortion.

Applying the sum of two cosine waves of frequencies ω_1 and ω_2 and both of amplitude V at the input, gives rise to output signal components at all combinations of ω_1, ω_2 and their multiples. Under low-distortion conditions, the number of terms [5] can be reduced to the ones caused by coefficients a_2 and a_3 only. They are mapped versus frequency in Fig. 2.1. Second-order intermodulation distortion (IM_2) is then defined by the ratio of the component at frequency $\omega_1 \pm \omega_2$ to the one at ω_1 or ω_2. Under low-distortion conditions

$$IM_2 = \frac{a_2}{a_1} V \qquad \ldots (2.5)$$

and by comparison with (2.3)

$$IM_2 = 2\, HD_2 . \qquad \ldots (2.6)$$

Third-order intermodulation distortion (IM_3) can be detected at the frequencies $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ and is given by

$$IM_3 = \frac{3}{4} \frac{a_3}{a_1} V^2 \qquad \ldots (2.7)$$

such that

$$IM_3 = 3\, HD_3 . \qquad \ldots (2.8)$$

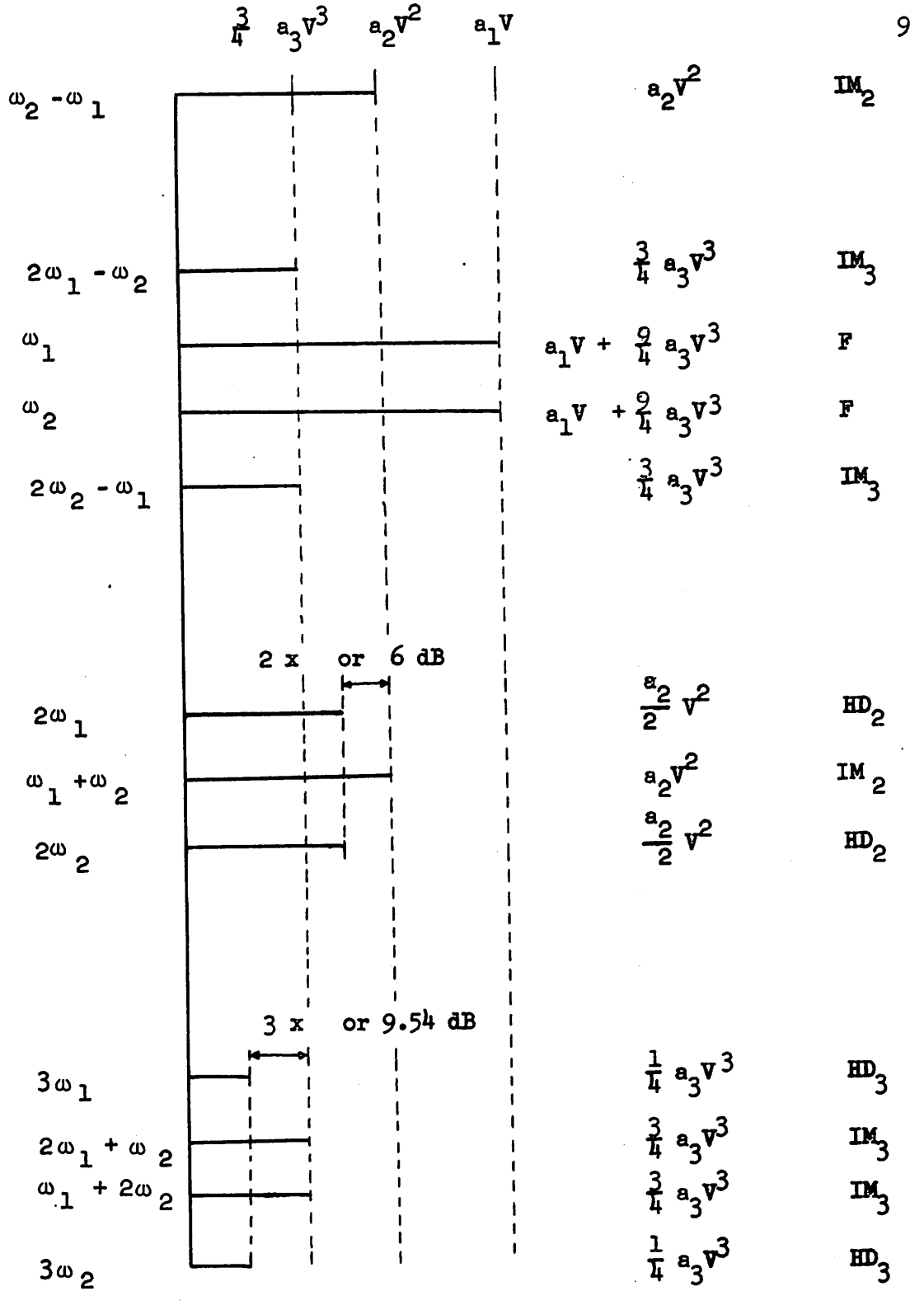


FIGURE 2.1

Intermodulation components in the output signal caused by coefficients a_1, a_2 and a_3 in the power series expansion. The input signals have frequencies ω_1 and ω_2 and amplitude V.

At low frequencies, there is thus one to one correspondence between harmonic and intermodulation distortion [5].

There are several other ways to describe the distortion caused by coefficients a_2, a_3, ... , such as cross-modulation distortion, triple beat, etc. There is nevertheless always a constant relationship of type (2.6) and (2.8) among them [5, 18].

2.3 GAIN CONTROL IN A SINGLE TRANSISTOR

In a bipolar transistor, the ac collector current i_C depends on the ac base emitter voltage v_i by an exponential relationship of the form

$$I_C + i_C = I_{CS} \exp\left(\frac{V_{BE} + v_i}{V_T}\right) \qquad \ldots (2.9)$$

in which I_C is the dc collector current,

I_{CS} is the collector saturation current,

V_{BE} is the dc base emitter voltage,

and $V_T = kT/q \simeq 26$ mV at 302° K.

For small v_i, the exponential can be expanded in v_i and (2.9) becomes

$$i_C = g_m v_i \left[1 + \frac{1}{2}\frac{v_i}{V_T} + \frac{1}{6}\left(\frac{v_i}{V_T}\right)^2 + \ldots\right] \qquad \ldots (2.10)$$

The first-order coefficient g_m, given by

$$g_m = \frac{I_C}{V_T} \qquad \ldots (2.11)$$

is the small-signal transconductance of the transistor. Consequently, gain can be varied by changing I_C.

Comparison of (2.10) with (2.1) shows that the distortion is given by (2.5) and (2.7)

$$IM_2 = \frac{1}{2} \frac{v_{ip}}{V_T} \qquad \ldots (2.12)$$

and

$$IM_3 = \frac{1}{8} \left(\frac{v_{ip}}{V_T} \right)^2 \qquad \ldots (2.13)$$

in which v_{ip} is the peak value of input signal v_i. As an example, one percent IM_2 is reached for 0.37 mV_{RMS} input voltage; one percent IM_3 for 5.2 mV_{RMS}.

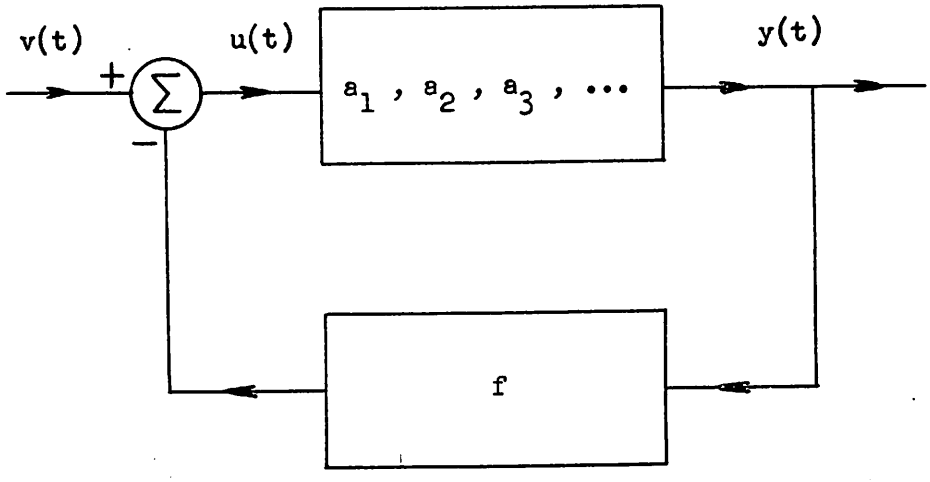
Series base and emitter resistances in the transistor linearize the exponential I_C - V_{BE} relationship and thus reduce the distortion [13, 14] as shown in the next Section. This corresponds however with a reduction in available gain-variation. In the limit of very high series resistance, the transistor is current-driven and gain variation is possible only as far as current gain β depends on collector current I_C. The distortion given by (2.12) and (2.13) is then negligible with respect to distortion caused by the dependence of β on I_C [6].

2.4 THE EFFECT OF NEGATIVE FEEDBACK ON DISTORTION

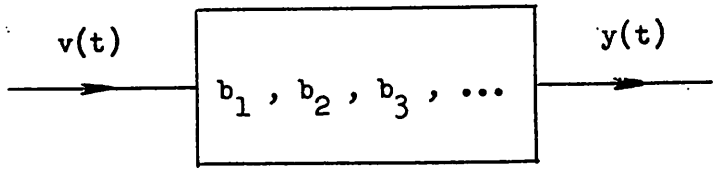
The application of negative feedback around the amplifier characterized by transfer coefficient a_i (Figure 2.2.a) gives rise to a new power series of the form of (2.1) in which

$$u(t) = v(t) - fy(t) \qquad \ldots (2.14)$$

where f represents the transfer function of the feedback network. This is equivalent to the amplifier represented in Figure 2.2.b; its output $y(t)$ is related to its input $v(t)$ by a power series expansion similar to (2.1) with coefficients



(a)



(b)

Figure 2.2.

Application of Negative Feedback with Transfer Function f around an Amplifier with Power Series Coefficients a_i (a) Equivalent to an Amplifier with an Input $v(t) = u(t) + fy(t)$ and with Coefficients b_i instead of a_i (b).

b_i instead of a_i and

$$b_i = \frac{1}{i!} \left. \frac{\delta^{(i)} y(t)}{\delta v(t)^{(i)}} \right|_{v(t) = 0} \qquad \ldots (2.15)$$

The application of (2.15) on (2.1) with (2.14) yields

$$b_i = \frac{a_1}{1 + T} \qquad \ldots (2.16)$$

$$b_2 = \frac{a_2}{(1 + T)^3} \qquad \ldots (2.17)$$

$$b_3 = \frac{a_3 (1 + T) - 2f a_2^2}{(1 + T)^5} \qquad \ldots (2.18)$$

in which the loopgain T is given by

$$T = fa_1 \qquad \ldots (2.19)$$

The third-order distortion is again given by (2.4) after replacing a_3 and a_1 respectively by b_3 and b_1. The output signal given by (2.16) is $(1 + fa_1)$ times smaller than without feedback. For the same output signal amplitude, IM_{3f} is thus given by

$$IM_{3f} = \frac{3}{4} \left[\frac{a_3}{a_1} (1 + T) - 2\left(\frac{a_2}{a_1} \right)^2 T \right] \left(\frac{V}{1 + T} \right)^2 \qquad \ldots (2.20)$$

In a similar way, for equal output signal amplitude as without feedback

$$IM_{2f} = \frac{a_2}{a_1} \frac{V}{1 + T} \qquad \ldots (2.21)$$

The first term in (2.20) represents third-order distortion, which is also present without feedback. The second one is due to second-order interaction around the feedback loop. Third-order distortion cancels completely for specific conditions of a_1, a_2, a_3 and f. This null has been studied and observed abundantly [13, 14, 17] but is too sharp to be of great practical interest. It is important to note, however, that for high loopgain, IM_{3f} is negative and thus always represents compression distortion. For negligible a_2 or low T, the type of distortion depends on the relative signs of a_3 and a_1.

At low frequencies, base and emitter resistance can always be lumped together in one single base or emitter resistance [2, 8]. Inserting emitter resistance R_E in one single transistor gives as loopgain

$$T = g_m R_E \qquad \ldots (2.22)$$

with g_m given by (2.11). The distortion is then found from (2.10) and (2.20) and is given by

$$IM_{3f} = \frac{1}{8} \left(\frac{v_{ip}}{(1 + T) V_T} \right)^2 (1 - 2T) \qquad \ldots (2.23)$$

and

$$IM_{2f} = \frac{1}{2} \frac{v_{ip}}{(1 + T) V_T} \qquad \ldots (2.24)$$

As an example, a transistor with $\beta = 100$ and having a base resistance of 120 Ω is biased at 5 mA collector current; its loopgain is thus 0.23. One percent IM_{3f} is reached for 8.7 mV_{RMS} input signal and the output signal current is the same as without base resistance. Adding 1.4 Ω emitter resistance cancels IM_{3f} completely. Adding another 1 Ω or more causes IM_{3f} to be one percent or less.

2.5 GAIN CONTROL IN A BASE-DRIVEN PAIR

Even-order distortion generated in a single transistor can be balanced out completely by applying input signal v_i between the bases of a matched pair (Figure 2.3). The gain is then varied by changing common emitter current I_E.

Assuming beta much larger than unity, the signal output current is given by

$$i_{C2} = I_E \left(\frac{1}{1 + \exp \frac{v_i}{V_T}} - \frac{1}{2} \right) \qquad \ldots (2.25.a)$$

or also,

$$i_{C2} = -\frac{1}{2} I_E \tanh \left(\frac{1}{2} \frac{v_i}{V_T} \right) . \qquad \ldots (2.25.b)$$

The expressions for i_{C1} are the same as for i_{C2}, but with a minus sign in front of v_i. Under low-distortion conditions (2.25) can be expanded as a power series in v_i and becomes

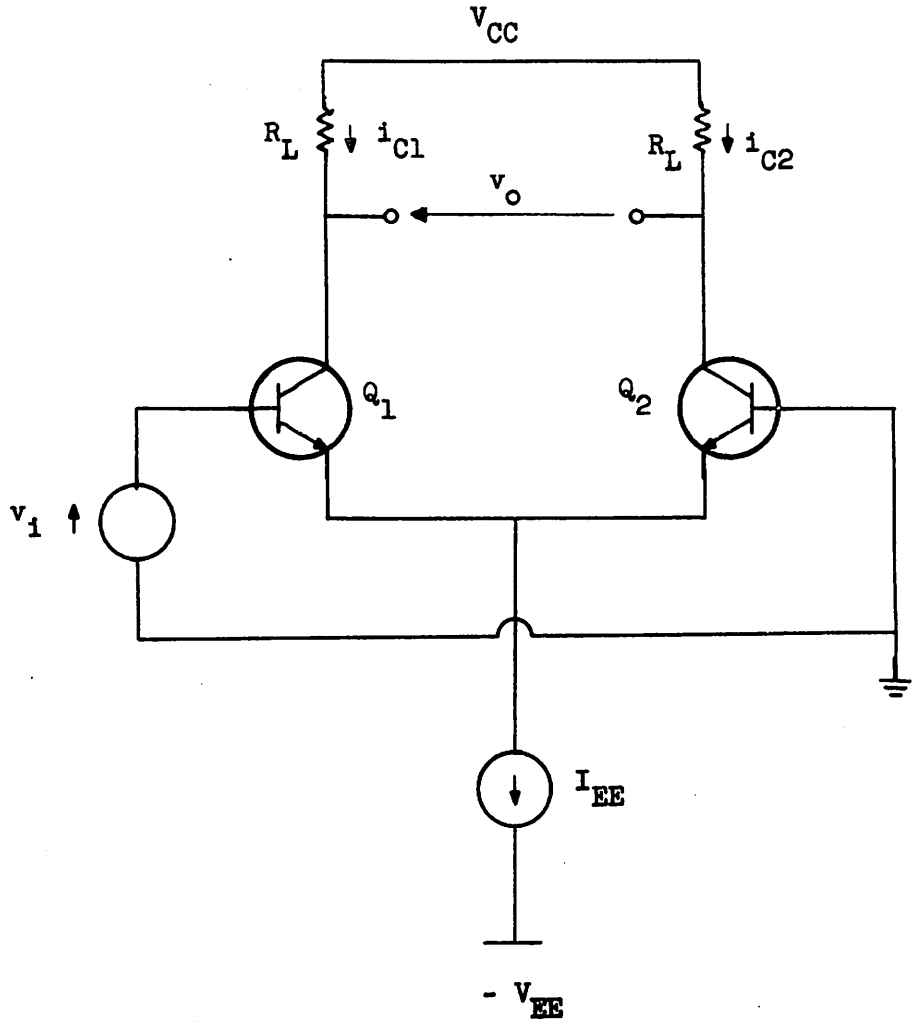


Figure 2.3

Base-Driven Variable-Gain Pair.

$$i_{C2} = -\frac{1}{2} g_m v_i \left[1 - \frac{1}{12} \left(\frac{v_i}{V_T}\right)^2 + \ldots \right] \quad \ldots (2.26)$$

in which

$$g_m = \frac{I_E}{2V_T} \quad \ldots (2.27)$$

No second-order distortion is present. Third-order distortion is compression distortion and is given by

$$IM_3 = \frac{1}{16} \left(\frac{v_{ip}}{V_T}\right)^2 \quad \ldots (2.28)$$

As an example, one percent IM_3 is reached at 7.4 mV_{RMS} input signal, which is $\sqrt{2}$ times higher than for a single transistor.

In practice, mismatch between both transistors causes some IM_2. Therefore, a differential output (Figure 2.3) is usually preferred for its improved rejection of even-order distortion.

As for a single transistor, the presence of base and emitter resistance causes negative feedback, which reduces output distortion in exchange for available gain variation. For emitter resistances R_E in each transistor, the residual distortion is derived from (2.20) and (2.26) and is given by

$$IM_{3f} = \frac{1}{4} i_p^2 \frac{1}{1 + g_m R_E} \quad \ldots (2.29)$$

in which i_p is the fractional current swing, which is given by $i_p = \frac{1}{2} \frac{v_i}{V_T} \frac{1}{1 + g_m R_E}$; g_m is given by (2.27). Note that for the same current swing as without feedback, the input signal voltage is increased by factor $(1 + g_m R_E)$.

The base-driven pair is thus able to suppress even-order distortion, but merely decreases the odd-order distortion present in a single transistor. Better performance can be achieved by applying the signal input as a current via the current source of the differential pair.

2.6 GAIN CONTROL IN AN EMITTER-DRIVEN PAIR

Interchanging the positions of the ac input signal and the dc gain-control signal in the pair of Figure 2.3 results in the emitter-driven pair shown in Figure 2.4. Input current $I_E (1 + i)$, in which i represents the fractional signal level, feeds both transistors in parallel. Control voltage V_B determines what fraction of the input current flows in each transistor.

The signal output current i_{C2} is derived from (2.25) for $\beta \gg 1$ and no series emitter resistance, and is given by

$$i_{C2} = \frac{i\, I_E}{1 + \exp b} \quad \text{or} \quad \frac{i\, I_E}{2} \left(1 - \tanh \frac{b}{2}\right) \qquad \ldots (2.30)$$

in which

$$b = \frac{V_B}{V_T} \qquad \ldots (2.31)$$

The normalized attenuation $\frac{i_{C2}}{iI_E}$ is plotted versus b in Figure 2.5. For large negative b, all current flows in

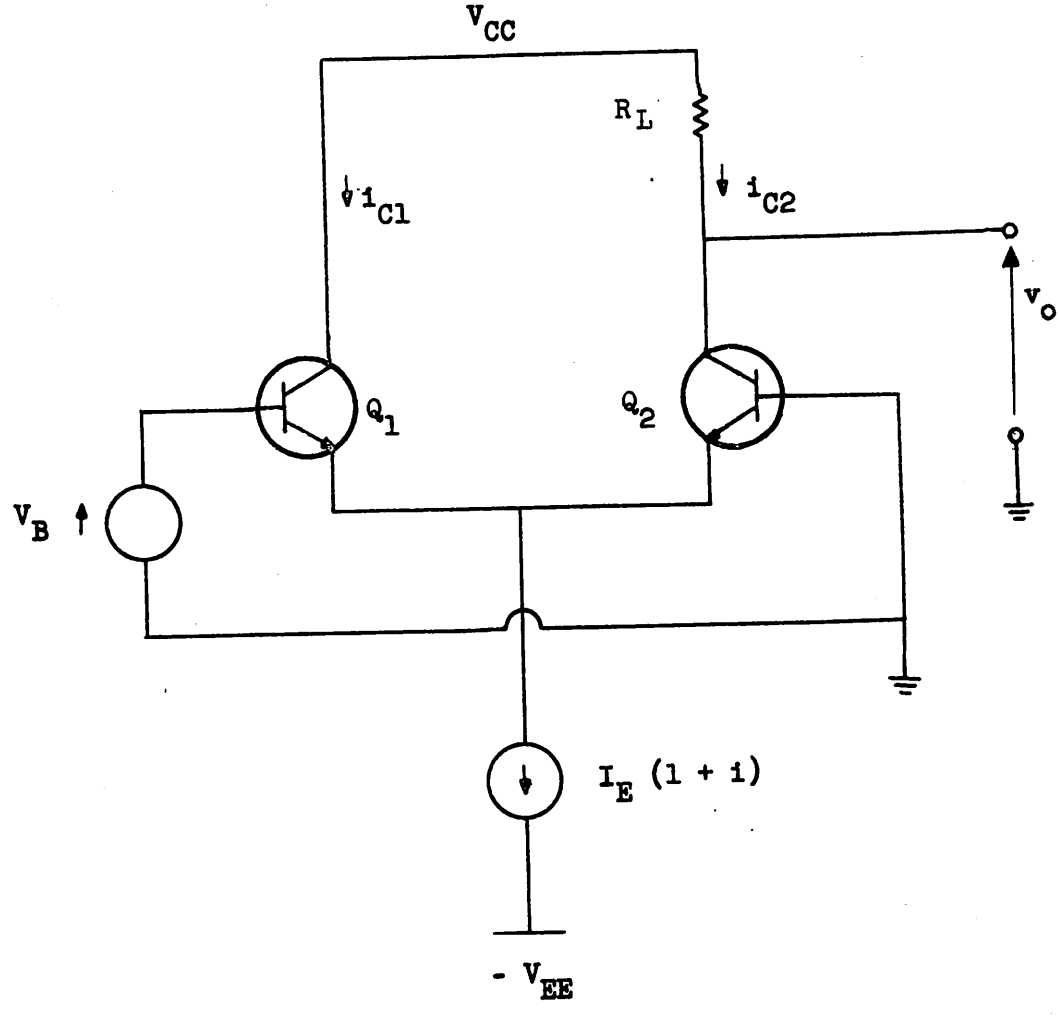


Figure 2.4

Emitter-Driven Variable-Gain Pair

Q_2 and thus maximum gain is achieved. For zero control voltage, the input is divided equally over both transistors and the current gain drops 6 dB. For large positive b , the relative attenuation in dB increases linearly with a slope of 8.7 dB per unit b (i_{C2} decreases by a decade for an increment of 60 mV in V_B) until the output signal is lost in noise.

Since the signal output current i_{C2} in (2.30) is linear in the input current i , no distortion occurs. The emitter driven pair is thus by far superior to the base driven pair in this respect. However, the input signal needs to be available as a current. The required voltage-current conversion is usually achieved by transistors with large emitter degeneration. As a result, the distortion actually present in i_{C2} is never zero, but can be made very low at the expense of circuit gain. This trade-off will be illustrated in the design of an age amplifier in Chapter 5.

Whereas the presence of base and emitter resistance improves the distortion performance of a single transistor and of a base-driven pair, it has a deteriorating effect for the emitter-driven pair [3] . Inclusion of base resistances r_{B1} and r_{B2} in the transistors of Figure 2.4 gives the circuit equations

$$I_{C1} \left(1 + \frac{1}{\beta_1}\right) + I_{C2} \left(1 + \frac{1}{\beta_2}\right) = I_E (1 + i) \qquad \ldots (2.32.a)$$

$$\frac{I_{C1}}{I_{C2}} = \exp\left[b - \frac{1}{V_T} \left(\frac{r_{B1} I_{C1}}{\beta_1} - \frac{r_{B2} I_{C2}}{\beta_2} \right) \right] \qquad \ldots (2.32.b)$$

in which I_{C1} and I_{C2} represent total collector current.

Equation (2.32.b) is nonlinear if the voltage drops across the base resistances are different.

Elimination of I_{C1} in (2.32.a) and (2.32.b) gives

$$I_{C2} = \frac{I_E (1 + i)}{1 + \exp\left[b - r_1 (1 + i) - \frac{I_{C2}}{I_E} (r_1 + r_2)\right]} \quad \ldots (2.33)$$

in which

$$r_j = \frac{r_{Bj} I_E}{\beta_j V_T} \text{ or } \frac{r_{Bj}}{r_{\pi j}} \text{ for } j = 1,2 \quad \ldots (2.34)$$

if $\beta_j \gg 1$.

Equation (2.33) is nonlinear in i . This equation is solved point by point for a sinusoidal input and a Fourier analysis is taken of the output waveform. This is executed by program NOLIBE given in Appendix A.1. The first-order ac component $|a_1|\ (i_{C2})$ is plotted versus b in Figure 2.5. The shape of the curve is the same as without base resistance . However, at high values of b, the curve is shifted in horizontal direction over a distance which equals r_1 .

The absolute value of the third order component a_3 is the same for both collector currents and is represented in Figure 2.5. The relative third-order intermodulation distortion for the emitter-driven pair is then given by

$$IM_{3p} = \frac{3}{4} \frac{|a_3|}{|a_1|\ (i_{C2})} , \quad \ldots (2.35)$$

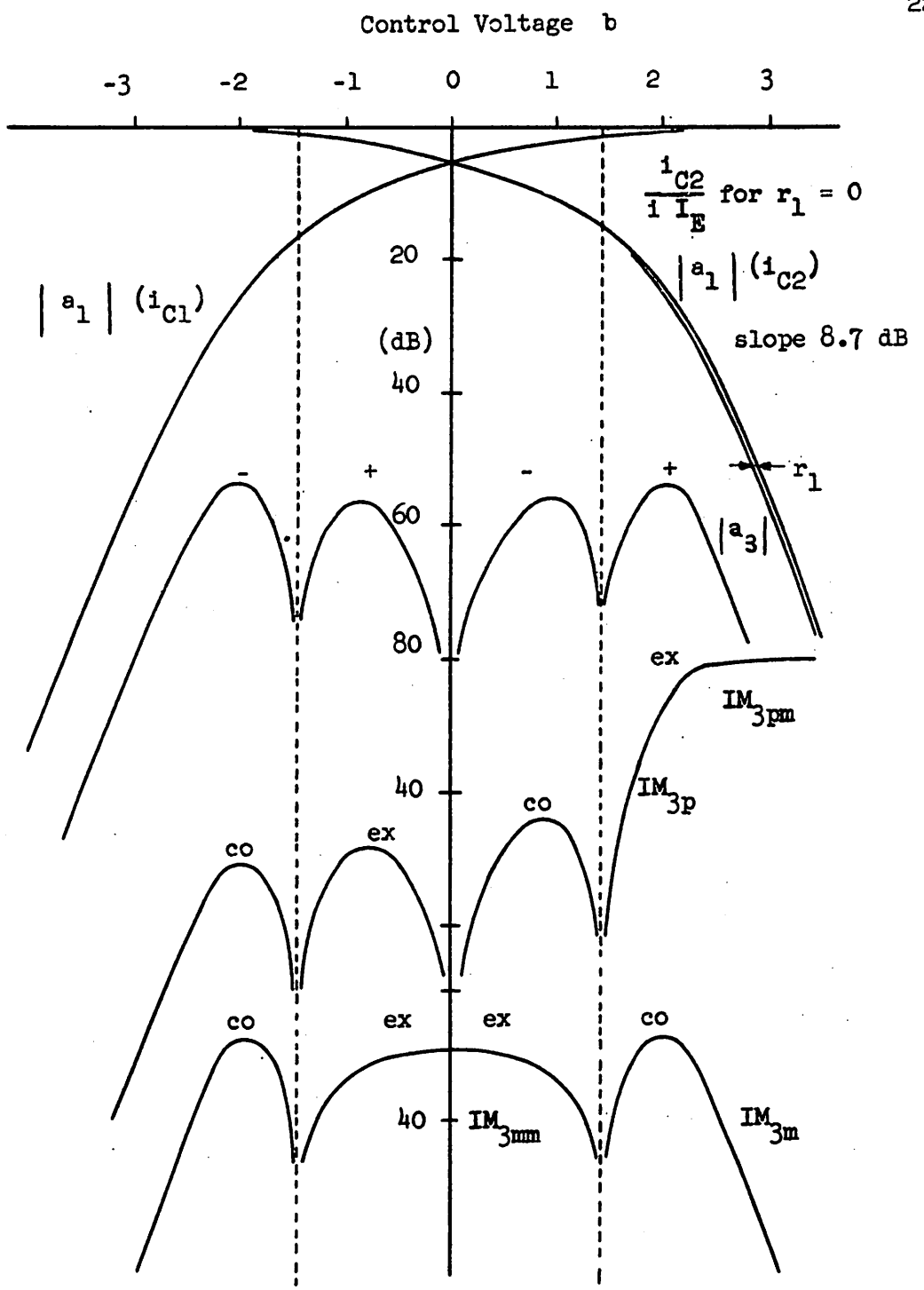


Figure 2.5.

Relative attenuation $\frac{i_{C2}}{iI_E}$ versus normalized Control Voltage b for the Emitter-driven Pair without base-or emitter resistances; the absolute values of the linear components of the collector signal currents are $|a_1|(i_{C1})$ and $|a_1|(i_{C2})$; the absolute value of the third-order component is $|a_3|$.

and is also plotted versus b in Figure 2.5. Both IM_{3p} and IM_{2p} are plotted versus relative attenuation in Figure 2.6.

At maximum gain, transistor Q_1 (Figure 2.4) is off and Q_2 behaves as a current-driven common-base stage. Because of the assumption that β is approximately independent of current, no distortion occurs. Indeed, in (2.33) the exponential term is negligible and I_{C2} is linear in i.

When both transistors carry the same currents, the exponential term in (2.33) equals unity. The relative attenuation is 6 dB and no distortion is present. For high attenuation, I_{C2} is very small, whereas b is positive and large compared with V_T. Expression (2.35) can then be simplified to

$$I_{C2} = I_E (1 + i) \exp (-b + r_1) \exp (r_1 i) \qquad \ldots (2.36)$$

The distortion in the attenuated output current is thus caused by the ac voltage drop across the base resistance of the current carrying transistor, which is represented by $\exp (r_1 i)$ in (2.36). Expanding $\exp (r_1 i)$ in a power series in i yields the upper limits of the distortion.

$$IM_{2pm} = r_1 i_p \frac{1 + \frac{r_1}{2}}{1 + r_1} \qquad \ldots (2.37)$$

and

$$IM_{3pm} = \frac{3}{8} (r_1 i_p)^2 \frac{1 + \frac{r_1}{3}}{1 + r_1} \qquad \ldots (2.38)$$

in which i_p is the peak value of i. The values given in (2.37) and (2.38) are represented also in Figure 2.6. They

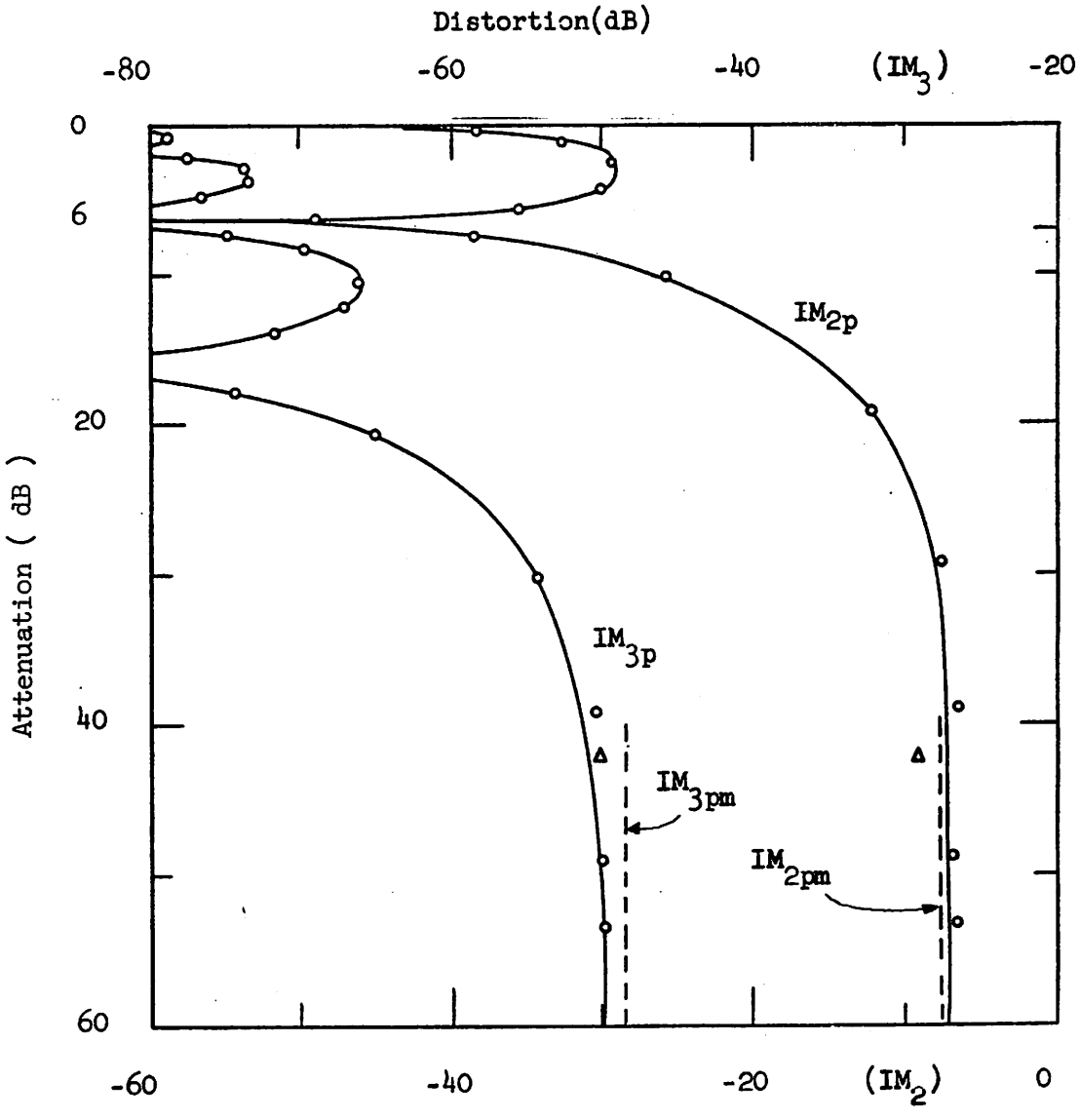


Figure 2.6.

IM_2 and IM_3 distortion for the Emitter-driven Pair (Appendix B.1); $r_1 = 0.385$ and $i_p = 0.25$; ——— computed; - - - approximated (2.37, 2.38); 0 measured; given by TIME and CANCER.

agree very well with the ones obtained by numerical computation.

Experiments have been performed on an emitter-driven pair using CA 3018 as matched transistors. The experimental set-up is described in Appendix B.1. The transistor model is obtained by the procedure given in Chapter 6. In particular, an accurate value for the base resistance is required. This had lead to a review and comparison of several existing methods such as the circle-diagram method. Also, fast estimation of base resistance has been made possible by a new method : the phase-cancellation method [8] .

All experimental work is initiated by determining under what values of i_p low-distortion conditions apply. This is done by verifying the slope of IM_2 and IM_3 versus i_p as shown in Figure 2.7. Deviation from a straight line indicates high level distortion. For a given value of r_1 this verification is carried out at high attenuation and thus at maximum distortion. Under the conditions of Figure 2.7 nearly full current swing is allowed. Another characteristic of low level distortion is the strict validity of (2.6) and (2.8). This has been verified extensively.

The experimental data are also represented in Figure 2.6. They agree well with the results from exact computations and the values predicted by (2.37) and (2.38).

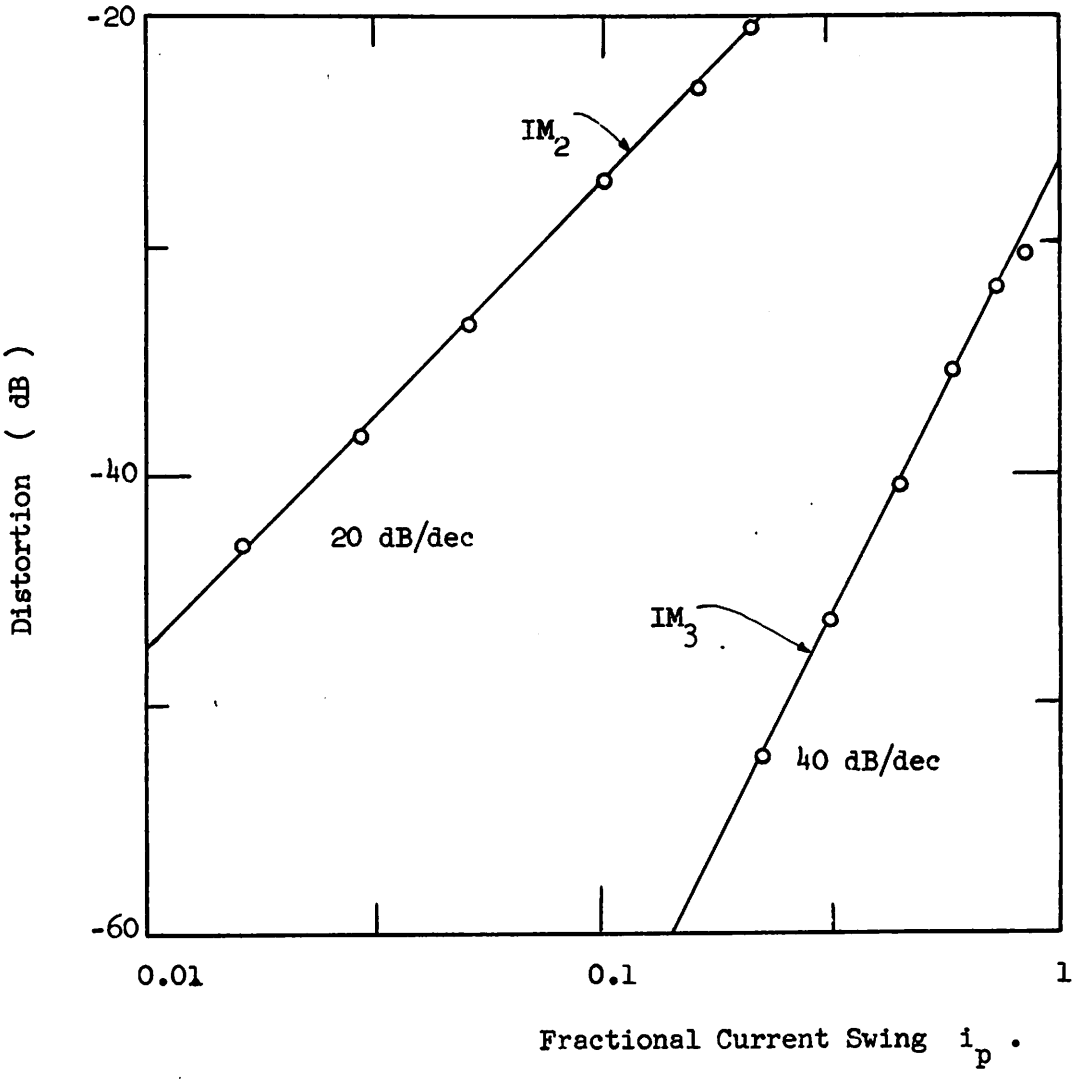


Figure 2.7

High Attenuation Distortion of Emitter-driven Pair (r_1 = 0.385) versus Fract. Current Swing i_p ; —— computed; O measured.

Finally, the results given by the computer-aided circuit analysis programs TIME [10] and CANCER [11] are added in Figure 2.6. They are obtained by performing a Fourier analysis on the transient solution for a sinusoidal input waveform.

The base resistances r_{Bj} are equivalent to emitter resistances with value $r_{Bj}/(1+\beta_j)$ and thus cause negative feedback. As pointed out in Section 2.4, third-order distortion cancels for specific amounts of feedback. This is clearly illustrated in Figure 2.5. The absolute distortion components $|a_3|$ are labeled with the sign that they have in the power series expansion of i_{C2} in i ; a_1 is assumed to be positive. For large positive b, a_3 is positive and thus IM_{3p} is expansion distortion. Expansion distortion is converted to compression distortion by a null and vice-versa. Since nulls in third-order distortion correspond with inflection points in the transfer characterictic, they can be predicted by applying

$$\left.\frac{d^3 I_{C2}}{d\, i^3}\right|_{i=0} = 0 \qquad \ldots (2.39)$$

on (2.33). The solution of (2.39) then gives the values of b at which a null occurs. This problem can be simplified by dropping 1 out of the denominator and using $1 - 2\frac{I_{C2}}{I_E} r_1$ instead of $\exp\left[-\frac{I_{C2}}{I_E}(r_1 + r_2)\right]$. This gives about

$b \approx \pm 2.45$ which is quite close to the experimental result $b \approx \pm 2.3$. For practical purposes, however, and especially in variable-gain amplifiers, these nulls are too sharp and thus not considered further.

It is possible to compensate for base resistance distortion by making the resistive voltage drops in (2.32.b) equal. Thus, if base (or emitter) resistances or beta's can be provided such that

$$\frac{r_{B1}}{r_{B2}} \frac{\beta_2}{\beta_1} = \frac{I_{C2}}{I_{C1}} \qquad \ldots (2.40)$$

no distortion occurs. Although this is quite feasible for fixed collector currents by scaling the emitter areas or by adding resistance on the low current side, it is impractical for variable current circuits and thus not further explored. Any reduction of β at low currents causes a reduction in maximum distortion however.

The excellent properties of an emitter-driven pair are realized in three commonly known transistor-quads : the automatic-gain-control (agc) amplifier [3], the multiplier [2] and Gilbert's variable-gain quad [1].

2.7 THE AGC AMPLIFIER

The agc amplifier consists of two emitter-driven pairs in parallel (Figure 2.8), such that an output can be taken in differential mode. As explained in Section 2.2, even-order

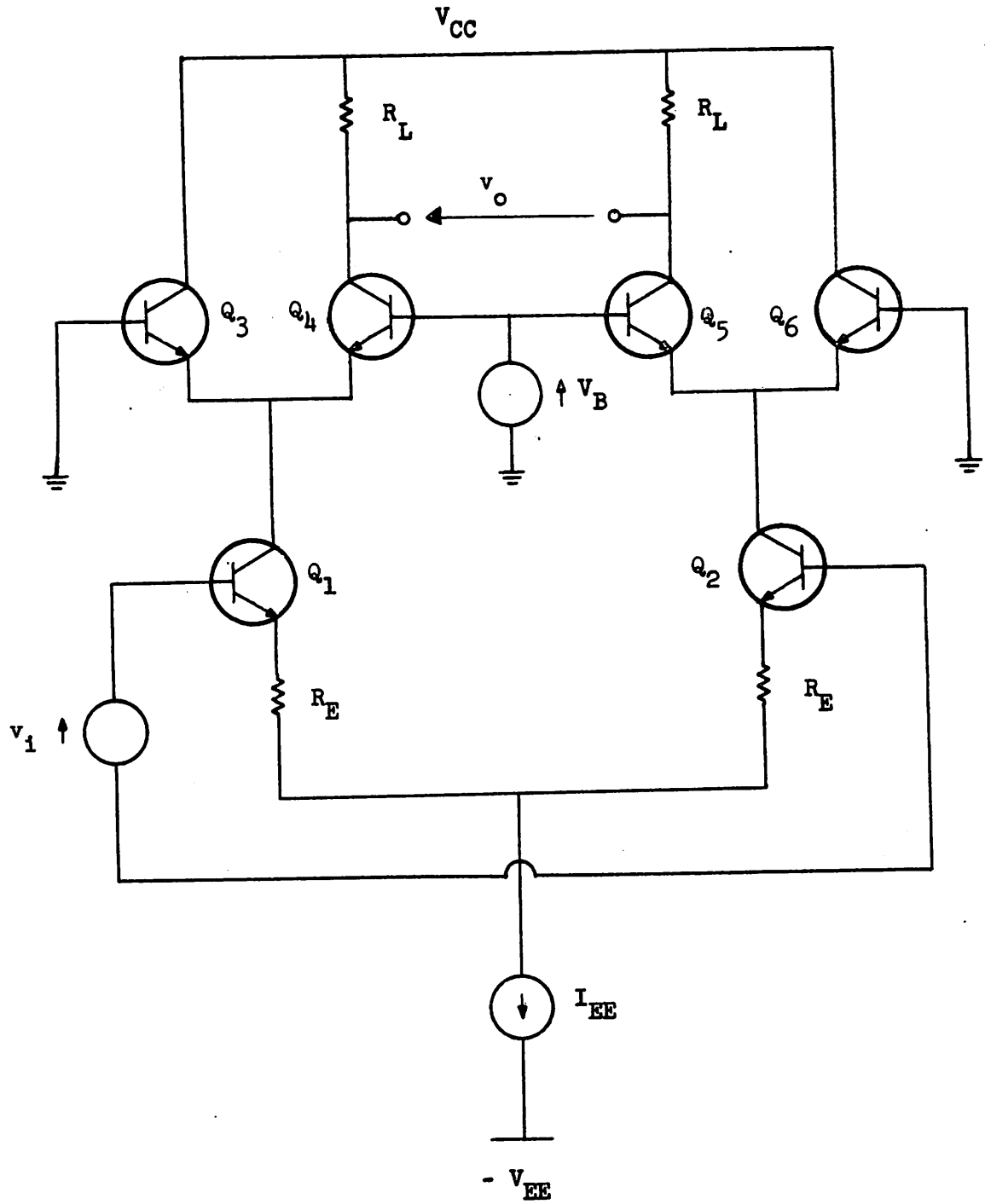


Figure 2.8

Variable-Gain Quad based on Signal Summation (AGC Amplifier).

distortion is cancelled, but the fundamental and odd-order components add. The maximum value of expansion distortion caused by the quad Q_3 , Q_4 , Q_5 and Q_6 is thus given by (2.38) with r_3 instead of r_1 where

$$r_3 = \frac{r_{B3}\, I_{EE}}{2\, \beta_3\, V_T} \qquad \ldots (2.41)$$

Actually, transistors Q_3 and Q_6 are matched and are designed for low values of r_B/β ; Q_4 and Q_5 form a matched pair also.

The input signal is differential in order to improve the common mode rejection if current source I_{EE} is non-ideal. A base-driven pair with emitter resistors R_E is used as a differential current source. The compression distortion caused in pair Q_1 , Q_2 is thus given by (2.29) with I_{EE} instead of I_E . Arbitrary increasing of R_E decreases the distortion, but also the maximum differential voltage gain, which is given by

$$A_{v,\,max} = \frac{R_L}{R_E + \frac{2V_T}{I_{EE}}} \qquad \ldots (2.42)$$

Consequently, a trade-off is to be made in the choice of emitter resistance R_E . Also note that the signal expansion in the quad can be compensated by the compression in the pair. All this is examined further with respect to the design of an agc amplifier in Chapter 5.

On the other hand, there is an additional source of signal compression which has not been mentioned hitherto. The differential current source may be non-ideal such that its output resistance only has a finite value R_S. The distortion caused by R_S is calculated for an emitter-driven pair (Figure 2.4) under high attenuation conditions. Nearly all the current of the pair flows then in transistor Q_1 which thus acts as a current-driven common-base stage. As a result, the emitter voltage and the impedance level at the common emitter point are only determined by Q_1. Transistor Q_2 acts then as a voltage-driven common-base stage.

The ac model for the emitter-driven pair with shunt resistance R_S is shown in Figure 2.9. The transfer functions of both transistors are described by power series which are similar to (2.10) and given by

$$i_{C1} = I_E \left[\frac{v}{V_T} - \frac{1}{2} \left(\frac{v}{V_T}\right)^2 + \frac{1}{6} \left(\frac{v}{V_T}\right)^3 + \ldots \right] \qquad \ldots (2.43)$$

and

$$i_{C2} = \epsilon I_E \left[\frac{v}{V_T} - \frac{1}{2} \left(\frac{v}{V_T}\right)^2 + \frac{1}{6} \left(\frac{v}{V_T}\right)^3 + \ldots \right] \qquad \ldots (2.44)$$

Signal currents i_{C1} and i_S are related by

$$i_S = i_{C1} + \frac{v}{R_S} \quad . \qquad \ldots (2.45)$$

Replacing i_{C1} in (2.45) by (2.43) allows us to expand v in i_{C1} as given by

$$v = \rho_1 i_S + \rho_2 i_S^2 + \rho_3 i_S^3 \qquad \ldots (2.46)$$

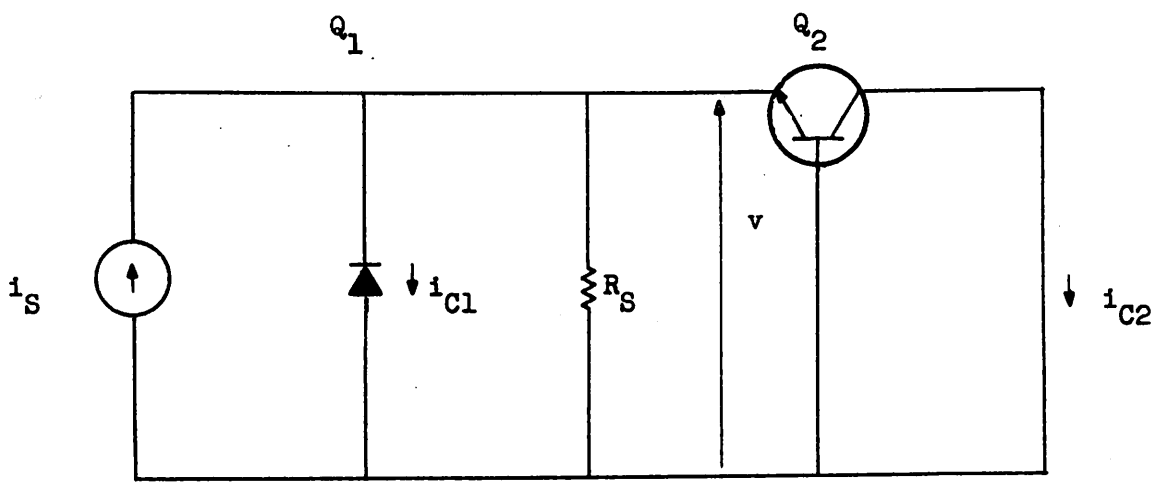


Figure 2.9.

Ac Model of Emitter-Driven Pair (Figure 2.4) with Non-ideal Current Source.

which, after substitution in (2.44) yields the power series expansion

$$i_{C2} = b_1 i_S + b_2 i_S^2 + b_3 i_S^3 \qquad \ldots (2.47)$$

with $b_1 = \frac{1}{I_E}$

$$b_2 = -\frac{V_T}{R_S I_E} \frac{1}{I_E^2}$$

$$b_3 = -\frac{1}{3} \frac{V_T}{R_S I_E} \frac{1}{I_E^3} \qquad \text{if } R_S \gg \frac{V_T}{I_E}$$

For the agc amplifier (Figure 2.8) the additional third-order distortion is then found by replacing I_E by $I_{EE}/2$, and is given by

$$IM_3 = \frac{2 V_T}{R_S I_{EE}} i_p^2 \qquad \ldots (2.48)$$

An experimental set-up of an agc amplifier is described in Appendix B.2. The experimental data for IM_3 are identical to the data for the emitter-driven pair and therefore not repeated. Matching was sufficient to reduce IM_2 at least to 20 dB below IM_3 under all circumstances.

The additional compression distortion given by (2.48) has been verified experimentally by connecting resistors of 100 Ω from the common emitter points to ac ground. Since I_{EE} is 10 mA (2.48) predicts 1.3% for $i_p = 0.5$. This value agrees well with the measured reduction (1.4%) in expansion distortion.

2.8 THE MULTIPLIER

In the agc amplifier of Figure 2.8 the collector currents of Q_3 and Q_6 are not used. On the contrary, in the agc quad of Figure 2.10, the collectors of Q_3 and Q_6 are joined to the ones of the complementary transistor in the other pair. For zero control voltage V_B all collector signal currents are equal and the signal output voltage v_o is thus zero. For a large value of V_B the amplifier reaches its maximum gain, which is given by (2.42). When control voltage V_B is replaced by an ac signal voltage, the quad is the well-known multiplier [2].

The mechanisms of distortion in the multiplier are exactly the same as in the agc amplifier. However, the components are combined in a different way and thus the results for relative distortion are different. This is illustrated in Figure 2.5. The linear components of Q_3 and Q_4 are represented by the curves denoted by $|a_1|(i_{C2})$ and $|a_1|(i_{C1})$ respectively. The current components of pair $Q_{5,6}$ behave in the same way as the ones of pair $Q_{4,3}$ but they all have opposite polarity. The relative distortion level for the multiplier IM_{3m} is then proportional to the ratio $|a_3|/|a_1|$ and is plotted versus b in Figure 2.5 and versus relative attenuation in Figure 2.11. Maximum gain is achieved for high V_B; $|a_1|$ is constant but $|a_3|$ decreases with V_B and thus

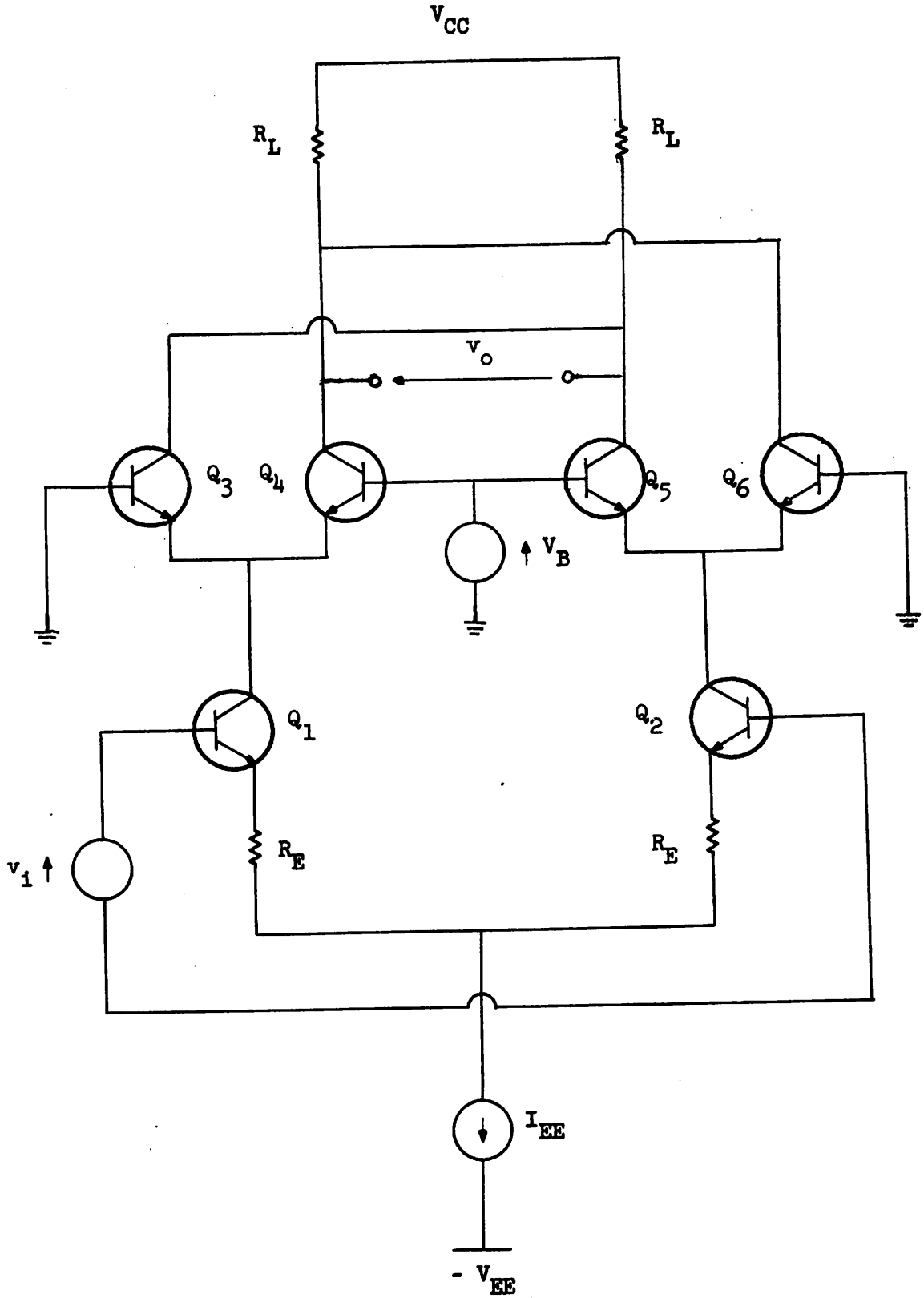


Figure 2.10

Variable-Gain Quad based on Signal Subtraction (Multiplier).

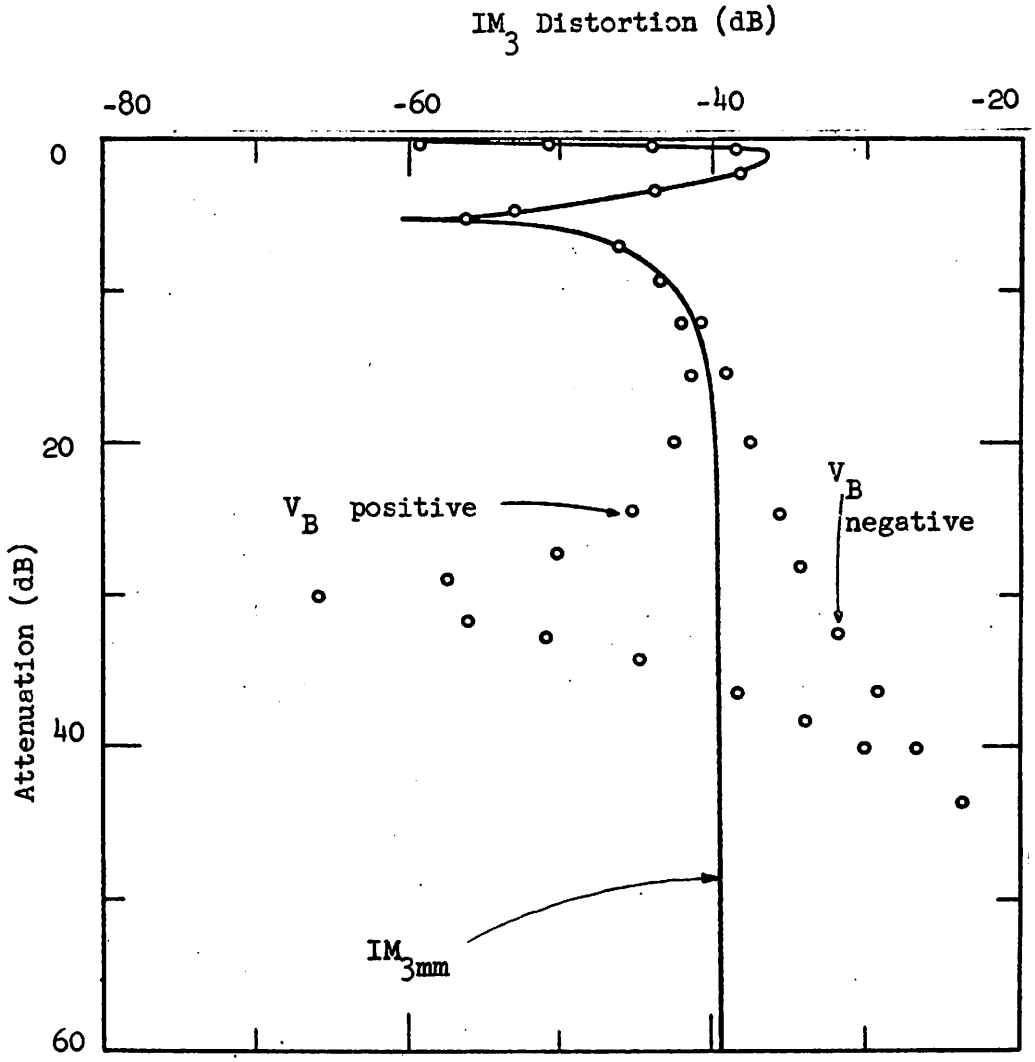


Figure 2.11.

IM_3 Distortion versus Attenuation for the Multiplier with $r_1 = 0.35$ and $i_p = 0.5$; —— computed for matched transistors; O measured.

IM_{3m} decreases with the same slope as $|a_3|$ does. Attenuation is obtained by direct cancellation of $|a_1|$ (i_{C1}) and $|a_1|$ (i_{C2}) but $|a_3|$ cancels in the same way such that around zero V_B IM_{3m} reaches a constant value IM_{3mm}. This distortion is expansion distortion and has a lower value than the peak of compression distortion (Figure 2.11) that occurs at lower attenuation levels. However, this constant amount of distortion IM_{3mm} extends over a wider attenuation range and is therefore predicted by power series considerations. Second-order distortion is cancelled by taking a differential output and therefore not mentioned further.

Assuming a very small value of b in (2.33) yields a power series expansion of I_{C2} in i with coefficients

$$c_1 = -\frac{b}{4}$$

$$c_2 = -\frac{b}{8} r_1 i_p \qquad \ldots (2.49)$$

and $c_3 = -\frac{b}{24} r_1^2 i_p^2$

from which, after comparison with (2.38)

$$IM_{3mm} = \frac{1}{3} IM_{3pm} . \qquad \ldots (2.50)$$

A multiplier used as an agc amplifier thus exhibits actually 10 dB less distortion than the so-called agc amplifier itself. However, if the multiplier is not fully compensated [2] for offset voltages and mismatch in beta and base resistance, then $|a_3|$ cancels at a different value of V_B than $|a_1|$ does. This results in an infinite value for IM_{3m} (Figure 2.12) at an attenuation level determined by the degree of mismatch. This is illustrated in Figure 2.11 for a multiplier using

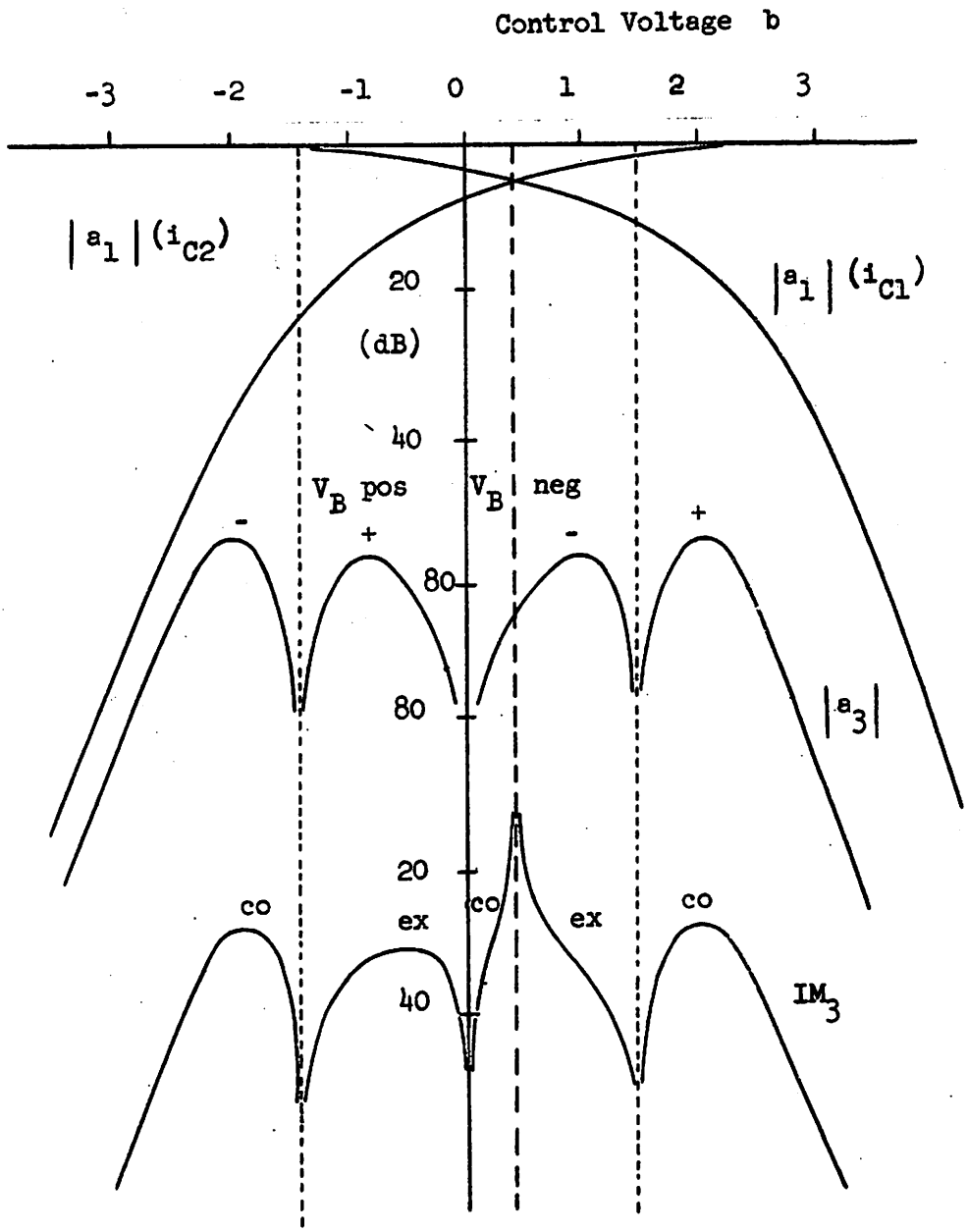


Figure 2.12.

The effect of mismatch on IM_{3m} distortion in a Multiplier.

CA 3045 as quad. Base resistance is added to make distortion measurement easier. The experimental set-up is described in Appendix B.3. Without compensation only 25 dB attenuation is available. Thus a multiplier has superior distortion performance compared with the agc amplifier, provided full four potentiometer compensation [2] is applied.

2.9 GILBERT'S VARIABLE-GAIN QUAD

The variable-gain quad shown in Figure 2.13 is based on Gilbert's wide band amplifier technique [1]. The input signal is converted into a current and predistorted by transistors Q_3 and Q_4 in order to cancel the distortion generated in base-driven pair $Q_{5,6}$. This predistortion principle is also applied in high-performance multipliers [2].

The gain A_v is controlled by the ratio of pair currents I_{E1} and I_{E2} as shown in Figure 2.14. However, distortion is absent only if [1]

$$r_i - r_o = 0 \qquad \ldots (2.51)$$

in which r_i and r_o are defined as in (2.34) for pair $Q_{3,4}$ and $Q_{5,6}$ respectively. Condition (2.51) is fulfilled for only one value of gain A_v. Thus for lower and higher gain values, distortion occurs (Figure 2.14). This is found from the nonlinear equation describing the quad [2], which is given by

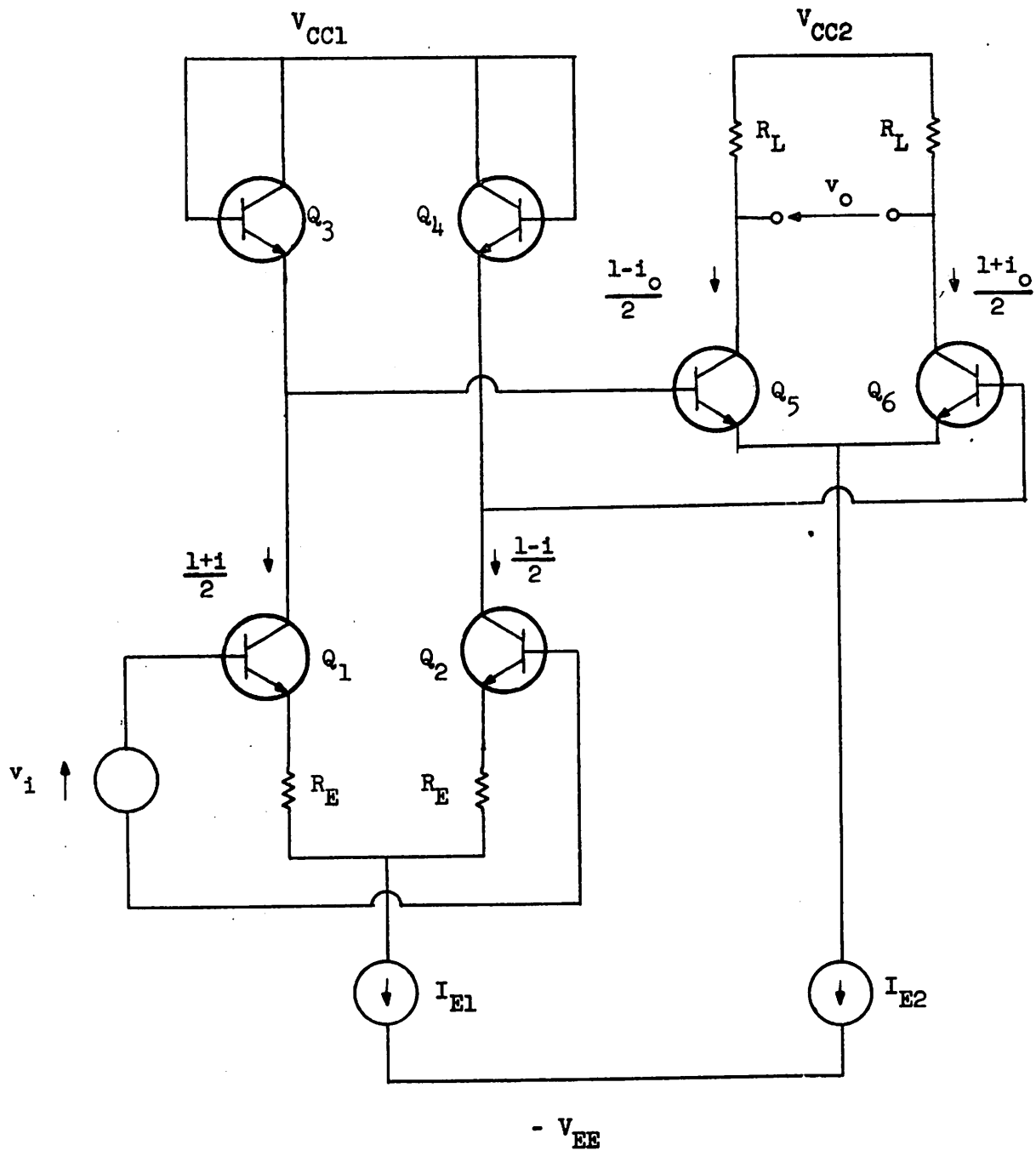


Figure 2.13

Variable-Gain Quad based on Predistortion (Gilbert's Quad).

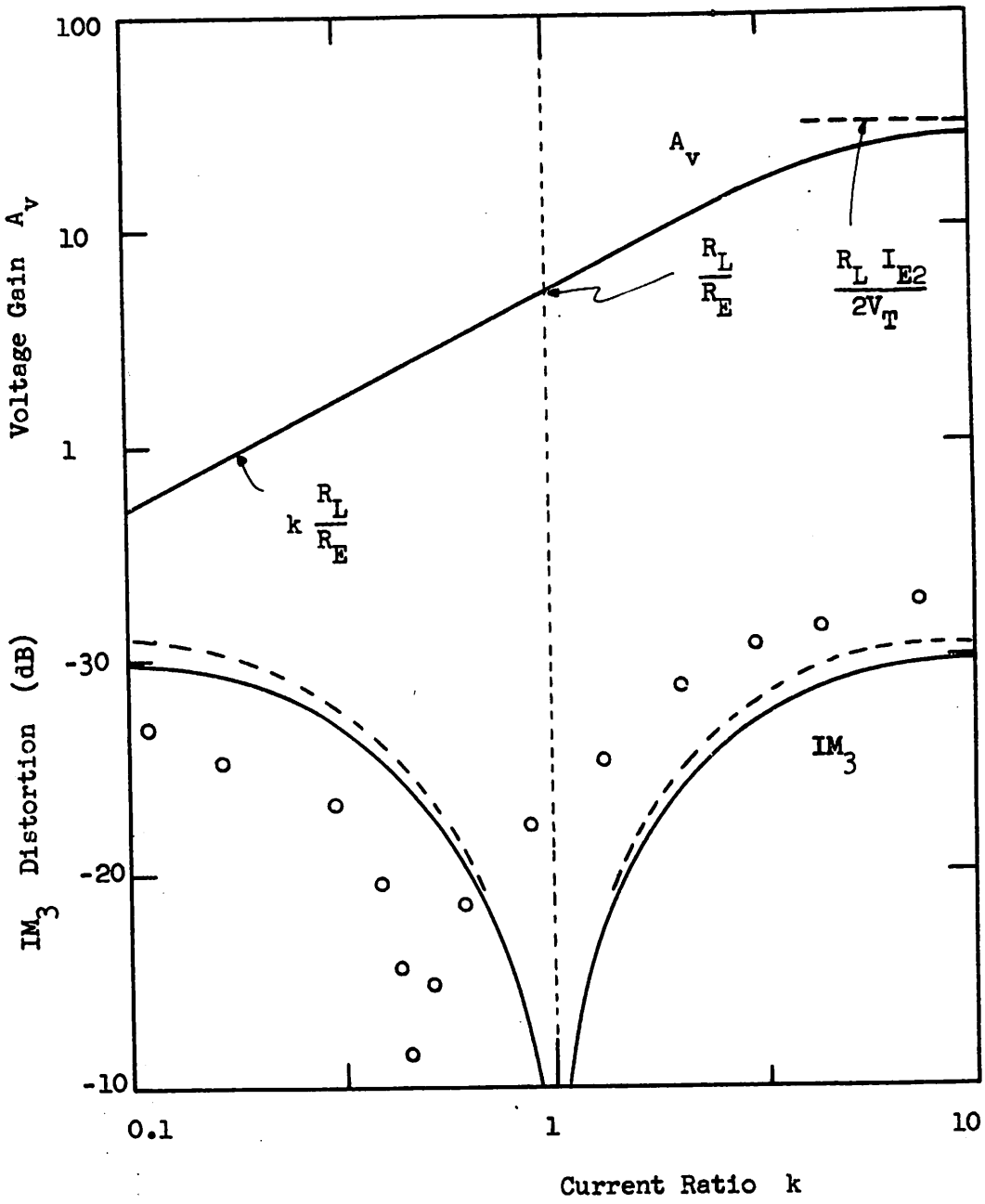


Figure 2.14.

Voltage Gain A_v and IM_3 Distortion versus Pair Current Ratio $k = I_{E2}/I_{E1}$ for Gilbert's variable-gain quad using CA 3045; —— computed; - - - approximated (2.54); O measured.

$$1 + i_o = (1 + i) \frac{\exp F}{1 + \frac{1 + i}{2} (\exp F - 1)} \qquad \ldots (2.52)$$

with $F = i\, r_i - i_o\, r_o$. Using (2.52) output current swing i_o can be expressed in terms of input current swing i as given by

$$i_o = i + \frac{r_1 - r_o}{2} i^3 \ . \qquad \ldots (2.53)$$

Ideally, no second-order distortion is present, even from a single-ended output. Residual second-order distortion, due to device imbalances, can be further reduced by taking a differential output (Figure 2.13). The third-order distortion is given by

$$IM_3 = \frac{3}{8} (r_i - r_o)\, i_p^2 \qquad \ldots (2.54)$$

Values from (2.54) together with results obtained by direct computations with (2.52) by means of program NOLIBE (Appendix A1), are represented in Figure 2.14 and Figure 2.15. Experimental data using CA 3045 are taken with the circuit described in Appendix B.4 and are added in Figure 2.15. For high gain I_{E2} is larger than I_{E1} and IM_3 is negative. Thus the output signal exhibits compression distortion. For low gain, expansion distortion prevails. For a matched quad with ideal current sources $Q_{1,2}$ distortion cancels when I_{E1} exactly equals I_{E2} . However, due to mismatch and additional compression distortion in $Q_{1,2}$, the zero distortion point is usually observed at a value of I_{E1} which is higher

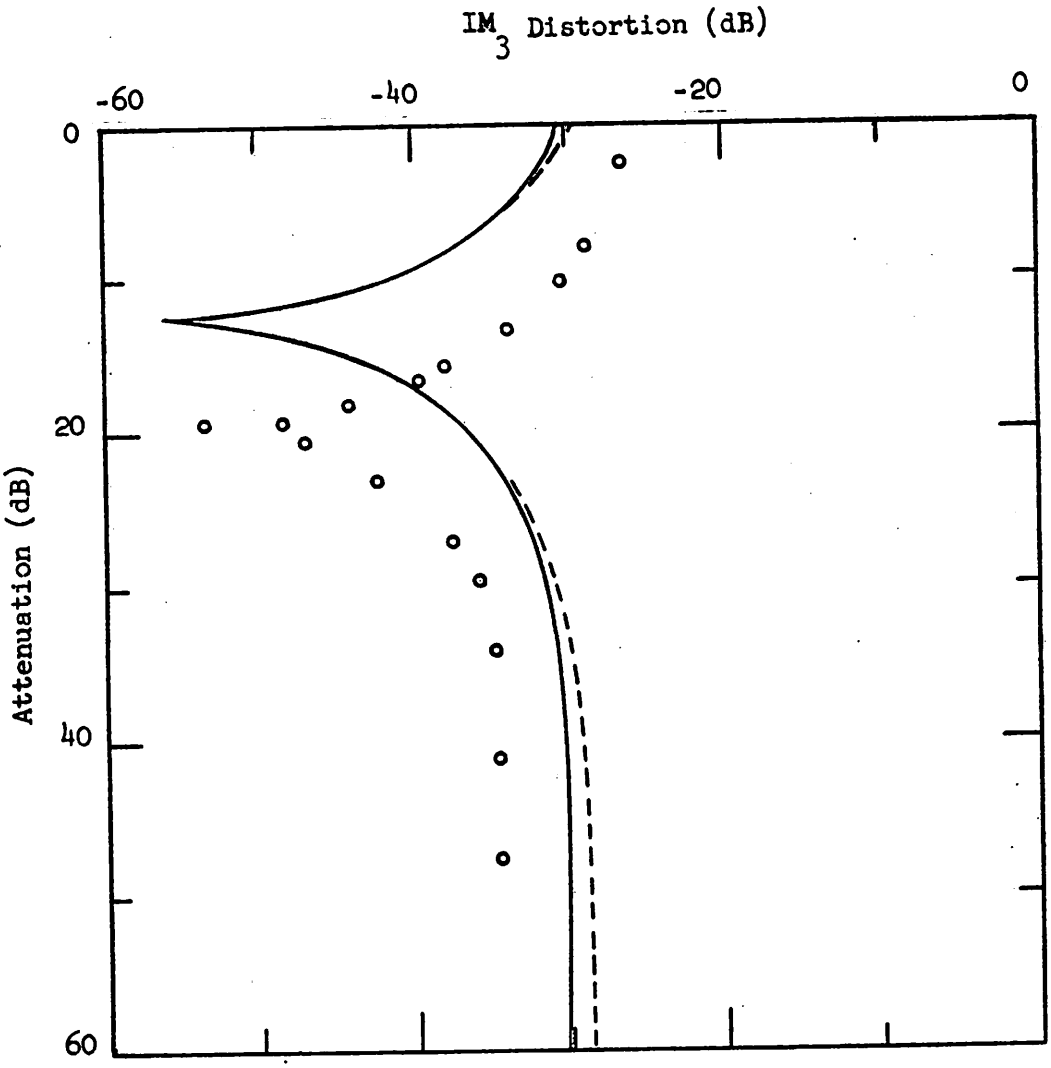


Figure 2.15.

IM_3 Distortion versus Attenuation for Gilbert's variable-gain quad using CA 3045; $r_{1,2\ max} = 0.35$ and $i_p = 0.5$; —— computed; - - - approximated (2.54); o measured.

than the one of I_{E2}. This is illustrated in Figure 2.15. The null in distortion occurs at a lower gain than predicted. Also the measured distortion levels deviate from the predicted ones in opposite sense.

Another source of extra compression distortion is the presence of shunt resistances R_S at the inter-connection lines between both pairs. The amount of distortion is obtained by a similar technique as the one leading to (2.48). It is given by

$$IM_3 = \frac{4\ V_T}{R_S\ I_{E1}} \qquad \ldots (2.55)$$

for high R_S under low gain conditions.

The comparison of (2.54) and (2.38) shows that the maximum distortion in Gilbert's quad is usually higher than in the agc amplifier. The null in the distortion of Gilbert's quad is wider however, because (2.54) is linear in voltage drop r, whereas (2.38) is quadratic. Gilbert's quad is thus quite attractive for a moderate attenuation range around the distortion null.

CHAPTER 3.

ANALYSIS OF DISTORTION IN HIGH-PERFORMANCE VARIABLE-GAIN AMPLIFIERS AT HIGH FREQUENCIES.

3.1 INTRODUCTION

From Chapter 2, three variable-gain amplifiers have evolved which are superior in performance to other configurations in the class of amplifiers considered here. However, the analysis was restricted to low frequencies where charge storage is unimportant. In this chapter, the high-frequency distortion is analyzed and compared for the three high-performance variable-gain amplifiers. The agc amplifier is shown to provide a higher dynamic range, but Gilbert's quad is superior if a small attenuation range is acceptable.

Frequency dependent distortion can be calculated by solving the differential equations that describe the nonlinearity. However, little insight is provided as to the relative contributions of transistor and circuit parameters. In this study, Volterra-series expansions [7] are used to indicate the dominant distortion parameters. These parameters are shown to be invaluable in the comparison of high-frequency distortion for all quads considered.

The high-frequency attenuation in all quads is limited by direct signal feedthrough along the junction capacitances. An estimate is given of the value of this attenuation limit, followed by computational and experimental verification.

3.2 HIGH FREQUENCY DISTORTION IN THE AGC AMPLIFIER AND MULTIPLIER.

3.2.1 HIGH FREQUENCY DISTORTION IN THE EMITTER-DRIVEN PAIR AT HIGH COLLECTOR CURRENTS (f_T constant)

At high frequencies, charge storage becomes important. Initially, the collector current is assumed to be high such that the device f_T is constant and given by

$$f_T = \frac{1}{2\pi\tau} \qquad \ldots (3.1)$$

where τ is the base transit time. Also, the frequency is high enough to neglect recombination current in the base. Then

$$I_B = \tau \frac{dI_C}{dt} \qquad \ldots (3.2.a)$$

$$I_C = I_{CS} \exp\left(\frac{V_{BE}}{V_T}\right) \qquad \ldots (3.2.b)$$

where I_B, I_C and V_{BE} are total values for base current, collector current and base-emitter voltage respectively.

The circuit equations for the emitter-driven pair (Figure 2.4) are then given by

$$(1 + \tau_1 \frac{d}{dt}) I_{C1} + (1 + \tau_2 \frac{d}{dt}) I_{C2} = I_E (1 + i) \qquad \ldots (3.3.a)$$

$$\frac{I_{C1}}{I_{C2}} = \exp\left[b - \frac{1}{V_T} (r_{B1} \tau_1 \frac{dI_{C1}}{dt} - r_{B2} \tau_2 \frac{dI_{C2}}{dt}) \right] \qquad \ldots (3.3.b)$$

Equation (3.3.a) shows that both collector currents roll off at their common-base cut-off frequency, which is about f_T. Equation (3.3.b) describes the nonlinearity. As for low frequencies, this is caused by the difference in voltage drop across the

base resistances. However, these voltage drops are now time differentials so that the distortion is frequency dependent.

Eliminating I_{C1} in (3.3.a) and (3.3.b) gives a nonlinear differential equation of the first order. This equation has been solved directly by a fourth-order Runge-Kutta method and a Fourier analysis has been taken of the output waveform. This is executed by computer program NONLIN given in Appendix A.2. The amount of distortion at one specific frequency is plotted in Figure 3.1. Frequency is normalized as given by

$$B = \omega\tau_1 \frac{r_{B1} I_E}{V_T} \text{ or } r_1 \frac{f}{f_\beta} \text{ with } f_\beta = \frac{f_T}{\beta} . \qquad \ldots (3.4)$$

As for low frequencies, distortion due to the presence of base resistance is zero at full gain and at half that gain. For high attenuation, distortion becomes maximum. This maximum value can be predicted by an analytical expression derived as follows.

In (3.3.a) and (3.3.b) I_{C2} is neglected with respect to I_{C1}. The ac part of I_{C1} is then found from (3.3.a) and given in the frequency domain by

$$i_{C1} = I_E \frac{i}{1 + j\gamma B} \qquad \ldots (3.5)$$

in which $\gamma = \frac{V_T}{r_{B1} I_E}$ and thus $\gamma B = \omega\tau_1$ or $\frac{f}{f_T}$. The ac part of collector current I_{C2} can then be represented by a Volterra series of the form [7]

$$i_{C2} = I_E \exp(-b) \left[H_1(B_1)oi + H_2(B_1,B_2)oi^2 + H_3(B_1,B_2,B_3)oi^3 + \ldots \right] \qquad \ldots (3.6)$$

in which $H_i\ (B_1, B_2, \ldots, B_i)$ are the i th-order Volterra Kernels operating on input signal i . The first factor in (3.6) is common to all Kernels and therefore taken out. The Kernels are obtained by substituting (3.5) and (3.6) in (3.3.b) and they are given by

$$H_1\ (B_1) = \frac{1 + jB_1}{1 + j\gamma B_1}$$

$$H_2\ (B_1, B_2) = \frac{jB_1\ (1 + \frac{jB_2}{2})}{(1 + j\gamma B_1)\ (1 + j\gamma B_2)} \qquad \ldots (3.7)$$

$$H_3\ (B_1, B_2, B_3) = \frac{jB_1\ jB_2\ (1 + \frac{jB_3}{3})}{2(1 + j\gamma B_1)\ (1 + j\gamma B_2)\ (1 + j\gamma B_3)} .$$

The harmonic distortion components (which at high frequencies are not necessarily related to the intermodulation products by a constant ratio as given by (2.6) and (2.8) are derived from (3.7) and given by

$$HD_2 = \frac{i_p}{2} \frac{B}{(1 + \gamma^2 B^2)^{1/2}} \left(\frac{1 + (B/2)^2}{1 + B^2}\right)^{1/2} \qquad \ldots (3.8)$$

$$HD_3 = \frac{i_p^2}{8} \frac{B^2}{1 + \gamma^2 B^2} \left(\frac{1 + (B/3)^2}{1 + B^2}\right)^{1/2} . \qquad \ldots (3.9)$$

Harmonic distortion as predicted by the above equation is plotted versus frequency in Figure 3.2 and as asymptotes in Figure 3.1. Experimental results taken again with the circuit configuration described in Appendix B.1 are represented in Figure 3.1 and Figure 3.2.

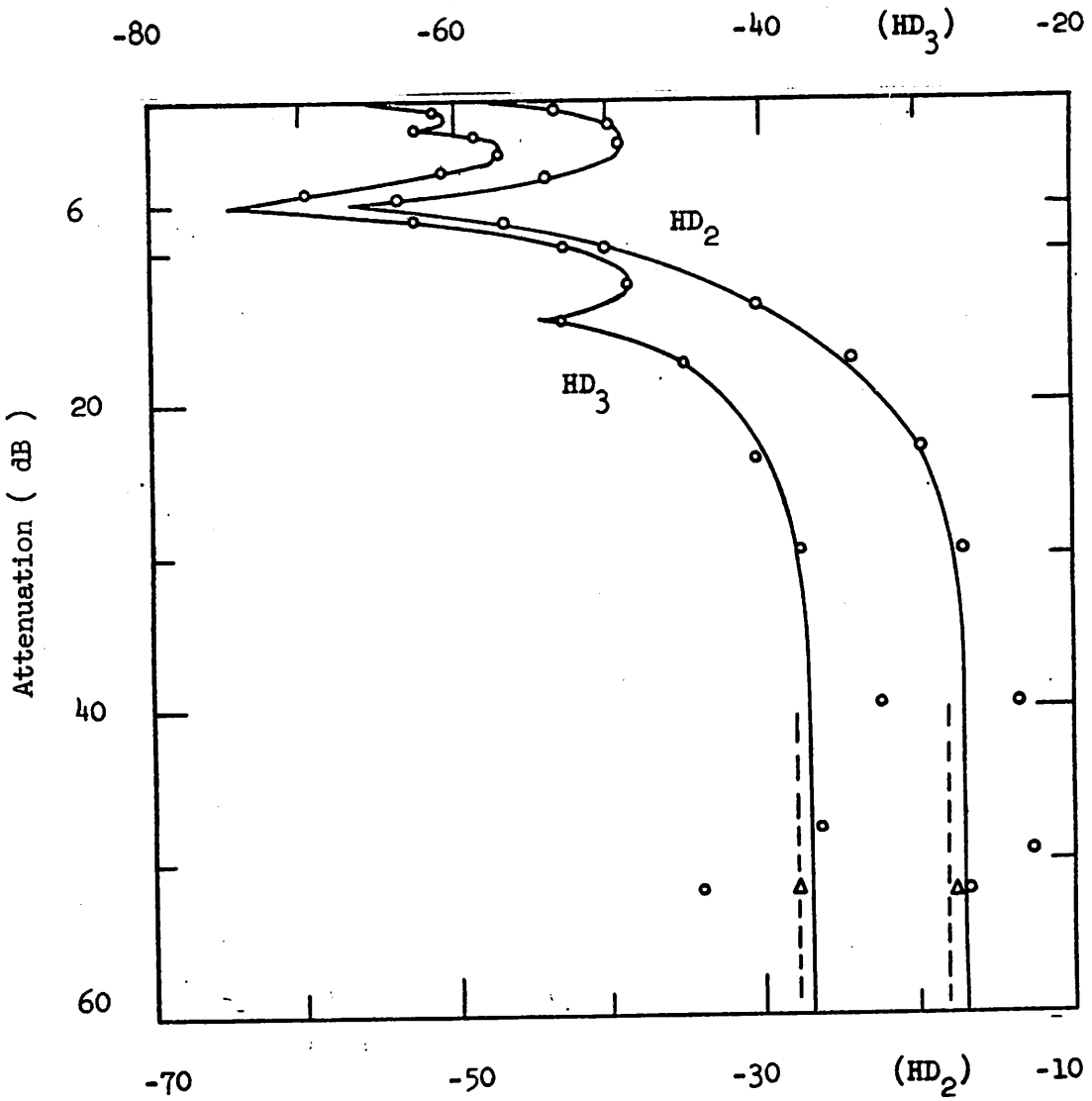


Figure 3.1.

HD_2 and HD_3 distortion for the Emitter-driven Pair (Appendix B.1); B = 4 (60 MHz) and i_p = 0.25 ; —— computed ; - - - approximated

O measured ; given by TIME and CANCER.

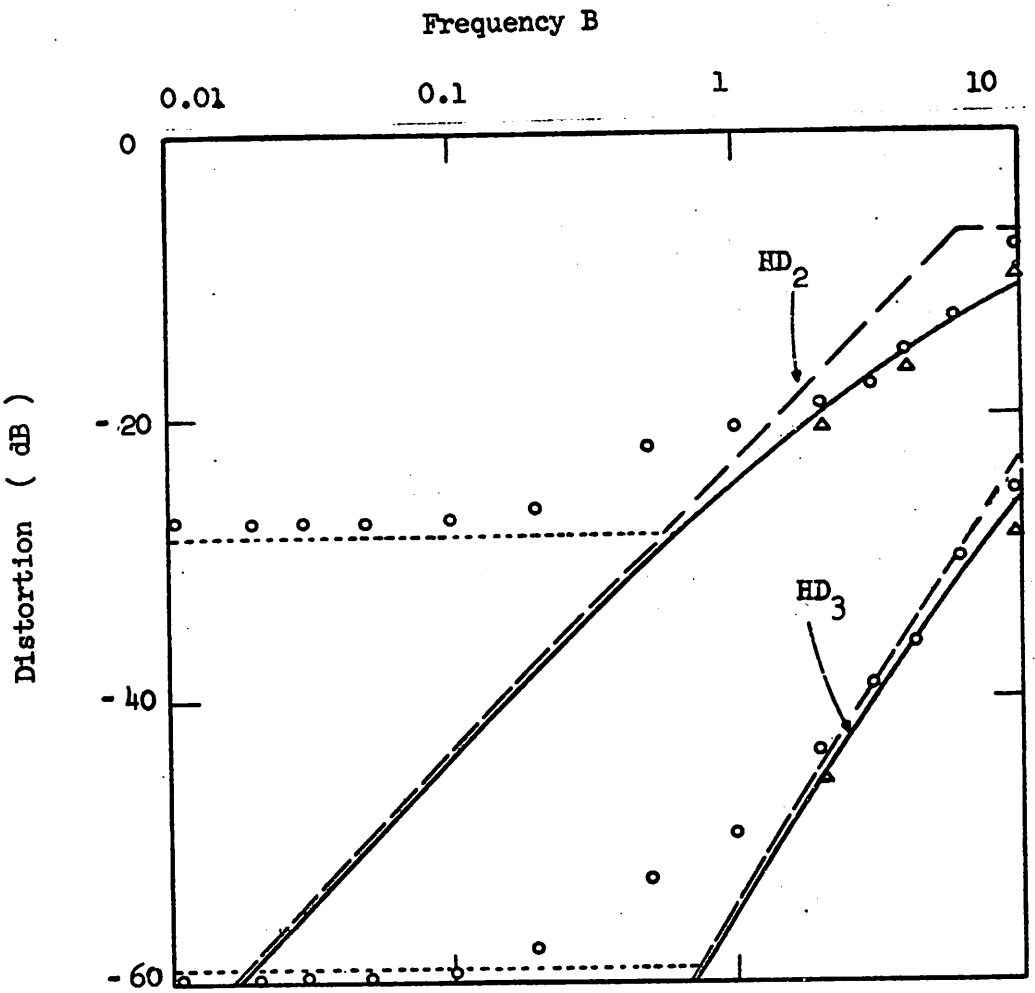


Figure 3.2.

Maximum HD_2 and HD_3 distortion versus frequency for the Emitter-driven Pair (Appendix B.1); $i_p = 0.25$ and $\gamma = 0.06$. —— computed; - - - approximated by asymptotes (3.8,3.9) at high frequencies; ..... approximated at low frequencies (2.37, 2.38); 0 measured; ▵ given by TIME and CANCER.

In Figure 3.1, the agreement is satisfactory except at high attenuation, where the distortion becomes excessively large and the attenuation itself reaches a limited value. Both effects are caused by signal feedthrough along the junction capacitances C_{jE2} and C_{jC2} of output transistor Q_2 (Figure 2.4). A detailed analysis is given in Section 3.5.

The measured values of the maximum distortion plotted versus frequency in Figure 3.2 agree well with the computed ones and the values obtained by Volterra-series approximation. At low frequencies, however, the experimental data deviates from the other values because base recombination has been neglected. The measurements thus follow the low-frequency approximations given by (2.37) and (2.38). The cross-over frequency is found by comparison of (3.9) and (2.38) and equals f_β given by (3.4).

Data given by the computer simulation programs TIME [10] and CANCER [11] are represented in Figure 3.1 and Figure 3.2. They compare favorably with the other data.

3.2.2 HIGH FREQUENCY DISTORTION IN THE EMITTER-DRIVEN PAIR AT LOW COLLECTOR CURRENTS.

At low collector currents, emitter base junction capacitance becomes non-negligible. This capacitance can be modelled by assuming a current dependent base transit time τ for the

pair transistors. Expression (3.2.a) then becomes

$$I_B = \tau \frac{dI_C}{dt} + C_{jE} \frac{dV_{BE}}{dt} \qquad \ldots (3.10)$$

if C_{jE} is voltage independent. From (3.2.b) $\frac{dV_{BE}}{dt} = \frac{V_T}{I_C} \frac{dI_C}{dt}$ and i_B, the ac portion of I_B is then given by

$$i_B = \left(\tau + C_{jE} \frac{V_T}{I_Q} \frac{1}{1 + i_C/I_Q} \right) \frac{di_C}{dt} \qquad \ldots (3.11)$$

where i_C and I_Q are respectively the ac and quiescent components of I_C. Expanding $(1 + i_C/I_Q)^{-1}$ in a power series yields

$$i_B = \tau_0 \frac{d\, i_C}{dt} + \frac{\tau_1}{2} \frac{d\, i_C^2}{dt} + \frac{\tau_2}{3} \frac{d\, i_C^2}{dt} + \ldots \qquad \ldots (3.12)$$

in which

$$\tau_0 = \tau + \tau_j$$

$$\tau_1 = - \frac{\tau_j}{I_E}$$

$$\tau_2 = \frac{\tau_j V_T}{I_E^2}$$

and $\tau_j = \frac{C_{jE} V_T}{I_E}$.

Initially, base resistance is neglected and C_{jE} is still voltage independent. Both collector currents in the emitter-driven pair then contain the same amount of fractional distortion. The same amount of distortion is also present in the collector

current of one single emitter-driven transistor. As a consequence, the distortion caused by the presence of constant junction capacitances in an emitter-driven pair is independent of the attenuation level and can easily be calculated by considering only one single emitter-driven transistor.

Take thus a transistor with constant base-emitter capacitance C_{jE}. This capacitance actually represents the base emitter junction capacitance of two transistors plus any parasitic capacitance C_E shunting the current source of the pair. The ac part of collector current i_C can be represented by a Volterra-series expansion. The Kernels are obtained using (3.2.b) and (3.12) and are given by

$$H_1(s_1) = \frac{1}{1 + \tau_0 s_1}$$

$$H_2(s_1,s_2) = -\frac{\tau_1 s_1}{(1 + \tau_0 s)^2 (1 + \tau_0 (s_1 + s_2))} \qquad \ldots (3.13)$$

$$H_3(s_1,s_2,s_3) = \frac{\tau_1 (s_1 s_2 + s_1 s_3 + s_2 s_3)}{(1 + \tau_0 s)^4 (1 + \tau_0 (s_1 + s_2)) (1 + \tau_0 (s_1 + s_2 + s_3))}$$

$$- \frac{\tau_2 s_1}{(1 + \tau_0 s)^3 (1 + \tau_0 (s_1 + s_2 + s_3))} .$$

The third-order harmonic distortion is then given by

$$HD_3 = \frac{i_p^2}{4} \left[\frac{3 \tau_j^2 s^2}{(1 + \tau_0 s)(1 + 2\tau_0 s)(1 + 3\tau_0 s)} - \frac{\tau_j s}{1 + 3\tau_0 s} \right] \ldots (3.14)$$

in which i_p is the fractional current swing. The second term in (3.14), which is due to second-order interaction, is always dominant. Thus the distortion is compression distortion, although the phase shift between fundamental and third-order component is not zero. The distortion is given by

$$HD_3 = \frac{i_p^2}{4} \frac{V_T}{I_E} (2 C_{jE} + C_E) \omega \qquad \ldots (3.15)$$

for frequencies below $f_T/3$. This has been verified for the agc amplifier (Figure 2.8) as presented in the next section.

3.2.3 HIGH FREQUENCY DISTORTION FOR THE AGC AMPLIFIER AND THE MULTIPLIER.

The HD_3 distortion for the agc amplifier (Figure 2.8) is the same as for the emitter-driven pair and the calculation is therefore not repeated. For a matched transistor pair, HD_2 distortion is reduced to a value which is usually less than HD_3 . HD_2 distortion is thus of little importance.

The effect of constant capacitance has been examined by connecting capacities of 33 pF at the common emitter points of the quad built with CA 3045 (Appendix B.2). For I_E = 4 mA, i_p = 0.7 and a total constant capacitance of about 46 pF, expression (3.15) predicts a reduction in distortion of 0.7% at 30 MHz. Actually, the HD_3 distortion decreased from 4.9% to 4.5%. This shows that the distortion caused by base resistance and constant capacitance is not exactly opposite in

phase so that a vector difference has to be taken. Also, the distortion introduced by the presence of constant capacitance is small and thus only important under very low distortion conditions.

The addition of base resistance in series with C_{jE} reduces slightly the effective value of C_{jE} and thus decreases the value given in (3.15). It is shown now that the voltage dependence of C_{jE} also reduces this distortion value. Capacitance C_{jE} depends on the ac base emitter voltage v as given by

$$C_{jE} = \frac{C_{jEO}}{(1 - \frac{V_{BE}}{\mathbb{O}_E} + \frac{v}{\mathbb{O}_E})^{1/n}} \qquad \ldots (3.16)$$

where $\mathbb{O}_E$ is the base-emitter junction potential. Coefficient n equals 3 for a linearly graded junction. Expression (3.16) can be expanded in a power series in v as given by

$$C_{jE}(v) = c_0 \ (1 - c_1 v + c_2 v^2 - c_3 v^3 + \ldots) \qquad \ldots (3.17)$$

in which $c_0 = C_{jEO}(\frac{\mathbb{O}_E}{\mathbb{O}_E - V_{BE}})^{1/n}$

$$c_1 = \frac{1}{n} \frac{1}{\mathbb{O}_E - V_{BE}}$$

$$c_2 = \frac{n+1}{2n^2} \frac{1}{(\mathbb{O}_E - V_{BE})^2}$$

and $$c_3 = \frac{(n+1)(n+2)}{6n^3} \frac{1}{(\mathbb{O}_E - V_{BE})^3} .$$

As mentioned before, the amount of distortion in the pair due to C_{jE} is the same as that in a single transistor with emitter drive current i. This current is related to the collector current i_C and base current i_B as given by

$$i_C = i - i_B \qquad \ldots (3.18)$$

where

$$i_B = \left[\tau g_m e^{\frac{v}{V_T}} + C_{jE}(v) \right] \frac{dv}{dt} . \qquad \ldots (3.19)$$

Current i_B can be expanded as a Volterra-series in v. Current i_C is expanded in v as given by (2.10). As a result (3.18) yields a Volterra-series expansion of i_C in i with the Kernels given by

$$H_1(s_1) = \frac{1}{1 + \frac{g_1}{g_m} s_1} \qquad \ldots (3.20)$$

$$H_2(s_1, s_2) = \frac{\left[\frac{g_1}{2 V_T} s_1 - g_2 (s_1 + s_2) \right] g_m}{(g_m + g_1 s_1)^3}$$

$$H_3(s_1, s_2, s_3) = \left\{ \frac{g_m}{6 V_T^2} - H_1 \left[\frac{g_m}{6 V_T^2} + g_3 (s_1 + s_2 + s_3) \right] \right.$$

$$- H_2 \left[\frac{g_m^2}{V_T} + 2 g_1 g_2 (s_1 s_2 + s_2 s_3 + s_1 s_3) \right.$$

$$\left. \left. + g_1 \frac{g_m}{V_T} s_1 + 2 g_2 g_m (s_1 + s_2) \right] \right\} / (g_m + g_1 s_1)^3$$

in which $g_1 = \tau g_m + c_0$

$$g_2 = \frac{1}{2}\left(\frac{\tau g_m}{V_T} - c_1 c_0\right)$$

$$g_3 = \frac{1}{3}\left(\frac{\tau g_m}{2V_T^2} + c_2 c_0\right)$$

For moderately high frequencies the third-order distortion is approximately given by (n = 3)

$$HD_3 \approx \frac{1}{12}\,\frac{c_0\omega}{g_m}\left(1 + \frac{V_T}{\mathbb{D}_E - V_{BE}}\right) \qquad \ldots (3.21)$$

if C_{jE} is dominant with respect to the charge storage capacitance (i.e. low I_C). This distortion is compression distortion caused by the voltage dependence of C_{jE} whereas the first one is due to the presence of C_{jE} itself. The voltage dependence of C_{jE} has thus usually a negligible effect on the distortion.

In a multiplier, matching at high frequencies is usually sufficient to make HD_2 distortion smaller than HD_3 distortion but, as at low frequencies, mismatch causes excessive distortion even at moderate attenuation levels (Figure 2.11). Since mismatch becomes worse at high frequencies, the useful attenuation range is even lower. A multiplier is thus not attractive at all as a low distortion agc quad at high frequencies.

3.3 HIGH FREQUENCY DISTORTION IN GILBERT'S QUAD

In Gilbert's variable-gain quad (Figure 2.13) the high

frequency output current is given by the same equation (2.52) as at low frequencies but now with

$$F = B_i \frac{di}{dt} - B_o \frac{di_o}{dt} \qquad \ldots (3.22)$$

where B_i and B_o are defined as in (3.4) for pair $Q_{3,4}$ and $Q_{5,6}$ respectively; it is assumed that f_T is constant and given by (3.1). This nonlinear differential equation can be solved using the same computer program NONLIN (Appendix A.2) as in Section 3.2.1. The results obtained are shown in Figure 3.3. This graph has the same shape as the one at low frequencies (Figure 2.15) but now the distortion values are higher.

An approximative value of HD_3 distortion can also be found by means of a Volterra-series expansion. Signal output current i_o is then represented by a Volterra-series. Its Kernels are found from the nonlinear equation and are given by

$$H_1 (B_{1i}, B_{1o}) = \frac{1 + \frac{B_{1i}}{4}}{1 + \frac{B_{1o}}{4}}$$

$$H_2 (B_{1i}, B_{1o}, B_{2i}, B_{2o}) = 0 \qquad \ldots (3.23)$$

and

$$H_3(B_{1i},B_{1o},B_{2i},B_{2o},B_{3i},B_{3o}) = \frac{1}{6} (B_{1i},B_{2i} B_{3i} - H_1^3 B_{1o} B_{2o} B_{3o}) - H_1 (B_{1i} - H_1 B_{1o})$$

The third-order distortion is thus approximately given by

$$HD_3 = \frac{i^2}{8} (B_i - B_o) \qquad \ldots (3.24)$$

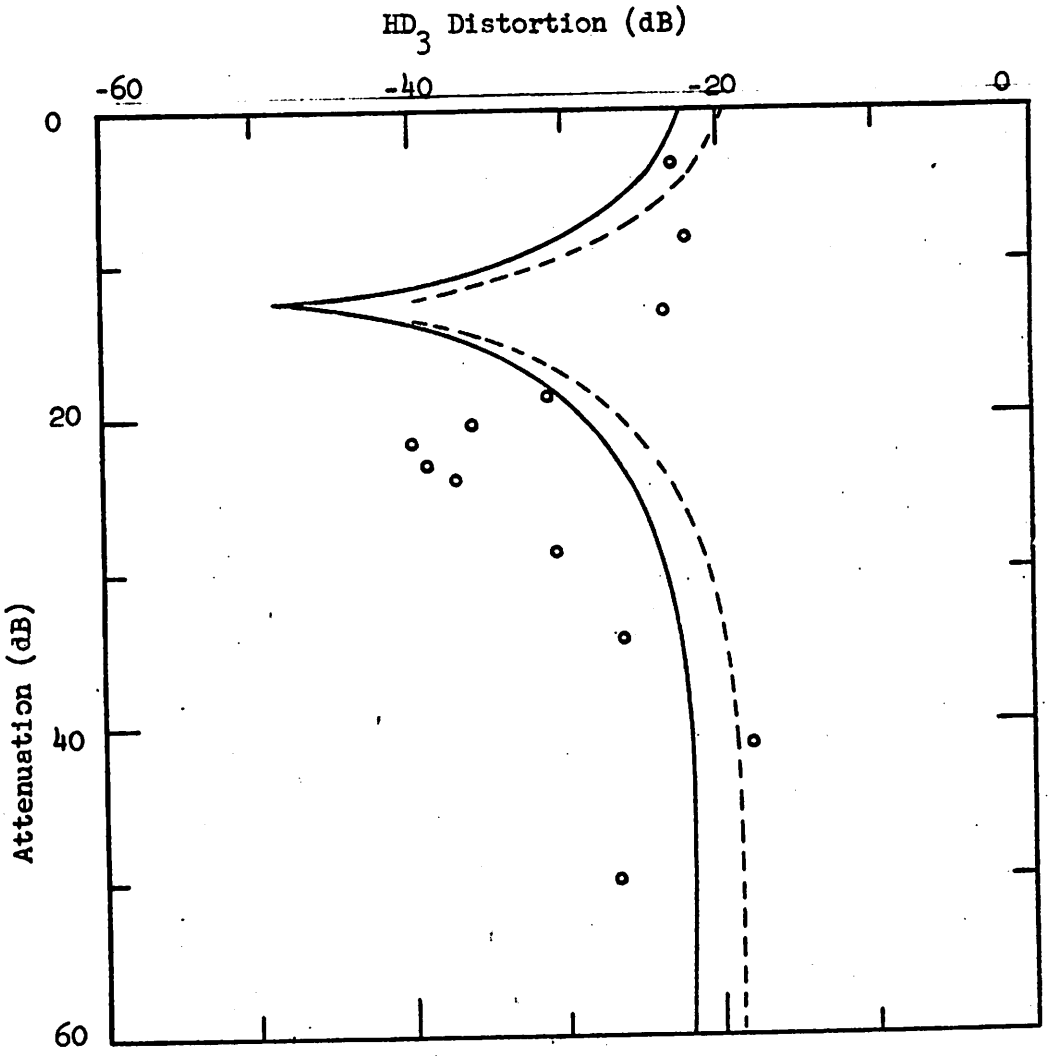


Figure 3.3.

High frequency HD_3 Distortion versus Attenuation for Gilbert's quad using CA 3045 (Appendix B4); $B_i + B_o = 4$ (49 MHz) and $i_p = 0.5$; —— computed; approximated (3.24); 0 measured.

for moderately high frequencies. This result is also represented in Figure 3.3.

Experimental data are taken with the circuit described in Appendix B.4. The compression distortion generated in the current sources causes a shift downwards in the attenuation level at which the null occurs. Thus, for low attenuation, this additional compression distortion adds to the compression distortion due to ohmic base resistance; at high attenuation it subtracts.

The presence of constant junction-capacitance C_{jE} and parasitic capacitance at the emitters of pair $Q_{5,6}$ has a similar effect as in the agc amplifier. A small amount of compression distortion, which causes the shift in the null (Figure 3.3) is thus due to this effect.

3.4 THE ATTENUATION LIMIT AT HIGH FREQUENCIES

For the emitter-driven pair (Figure 2.4) under high attenuation conditions, the g_m current generator of transistor Q_2 is nearly zero. At high frequencies, two sources of signal feedthrough to the input can then be distinguished. Assume that the collectors of both transistors are fed from the same power supply line, having a finite impedance Z_S. The lowest output signal level v_o that can be reached is then $Z_S i$, where i is the ac input current. Using separate supply lines

usually solves this feedthrough problem. The other one is treated next.

At high attenuation, input current i flows entirely in transistor Q_1 (Figure 2.4) and develops voltage v_i at the emitter. This voltage is applied to transistor Q_2 which can be modelled by a second-order high-pass filter as shown in Figure 3.4. The output current i_L then determines the maximum attenuation range AR, which is defined by

$$AR = \left| \frac{i}{i_L} \right| \qquad \ldots (3.25)$$

Emitter voltage v_i is generated by driving current i into the common-base stage formed by transistor Q_1. Thus v_i is given by

$$v_i = i\, r_D \, \frac{1 + j \frac{r_B}{r_D} \frac{f}{f_T}}{1 + j \frac{f}{f_T}} \qquad \ldots (3.26)$$

in which $r_D = \frac{1}{g_m} + \frac{r_B}{1 + \beta}$. Parasitic capacitance C_p is initially neglected. For high frequencies below f_T, (3.25) can be approximated by

$$\left| v_i \right| \simeq i\, r_B \frac{f}{f_T} \quad \text{and} \quad \arg (v_i) \simeq 90^\circ - p_1 \qquad \ldots (3.27)$$

where p_1 is a small phase shift to represent the fact that $\arg (v_i)$ becomes smaller than 90° at lower frequencies.

Output current i_L is generated by voltage source v_i and is given by

$$i_L = \frac{v_i}{R_L} \frac{s^2}{s^2 + \frac{\omega_2^2}{\omega_1} + \omega_2^2} \qquad \ldots (3.28)$$

where $\omega_1 = (r_B C_{jE} + r_B C_\mu + R_L C_\mu)^{-1}$

and $\omega_2^2 = (r_B R_L C_{jE} C_\mu)^{-1}$. For frequencies lower than $\omega_1/2$ expression (3.28) can be simplified to approximately

$$|i_L| \approx v_i \omega^2 r_B C_{jE} C_\mu \text{ and } \arg(i_L) \approx 180^\circ - p_2 \qquad \ldots (3.29)$$

where p_2 indicates that $\arg(i_L)$ becomes smaller than 180° at higher frequencies.

The attenuation range is found from (3.25), (3.27) and (3.29) and is given by

$$|AR_p| \approx \frac{\omega_T}{r_B^2 C_{jE} C_\mu \omega^3} \text{ and } \arg(AR_p) \approx -270^\circ + p_1 + p_2 \,. \qquad \ldots (3.30)$$

Consequently, the product $r_B^2 C_{jE} C_\mu$ rather than only C_μ has to be minimized, if a high attenuation range is required. Capacitance C_μ represents the collector-base junction capacitance and any other parasitic capacitance shunting base and collector.

Expression (3.30) has been verified by means of measurements on the agc amplifier (circuit in Appendix B.2) and by use of circuit analysis program TIME [10] . This is shown in Figure 3.5. In the appropriate frequency range (3.30) predicts the maximum attenuation fairly well. At higher frequencies, the

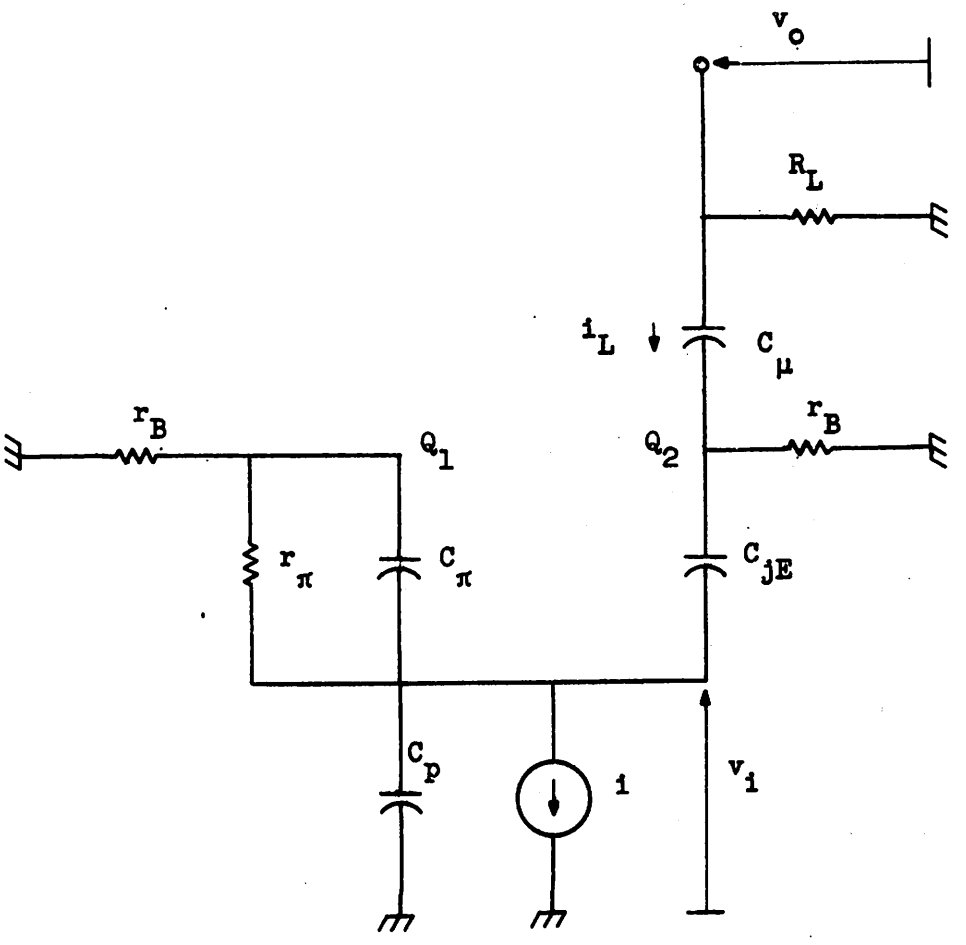


Figure 3.4

Incremental Model of Emitter-Driven Pair at High Attenuation.

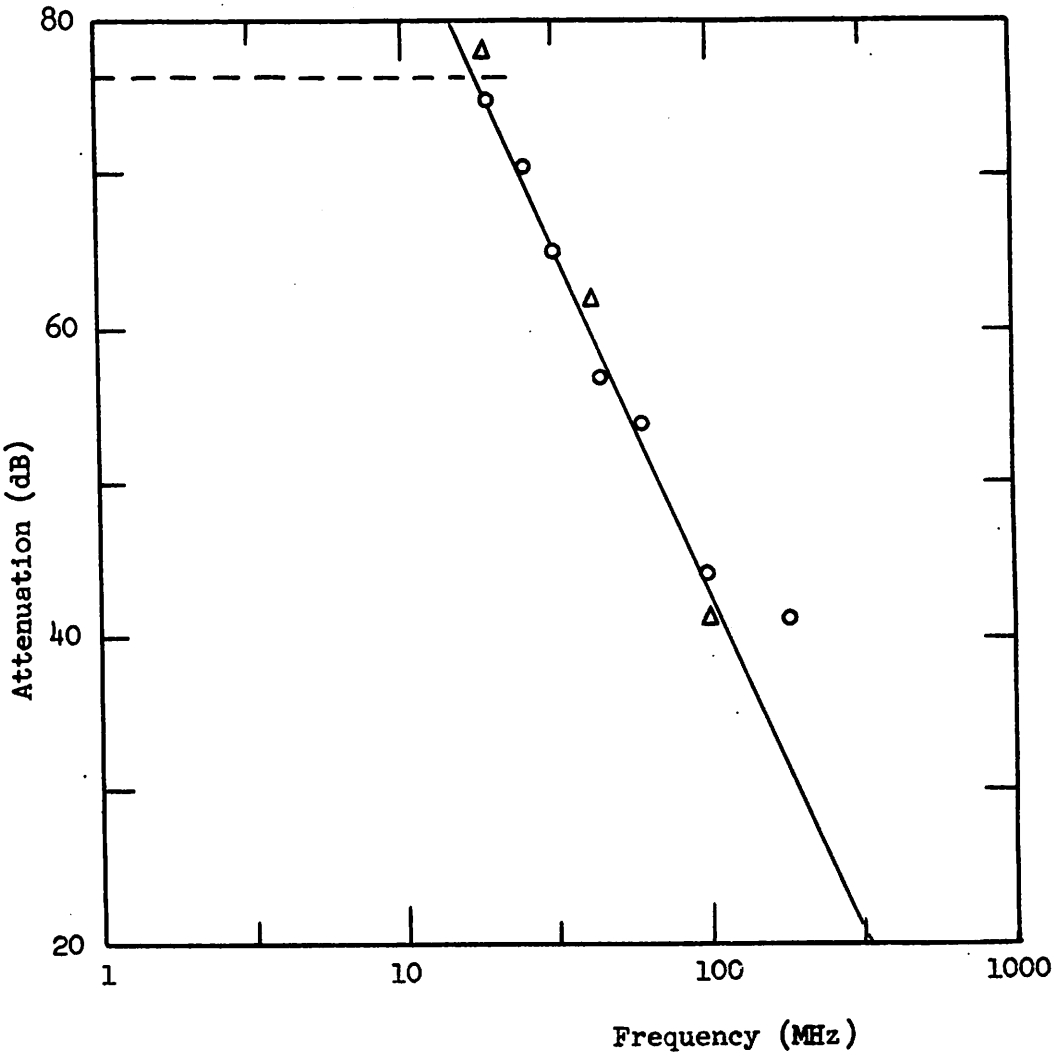


Figure 3.5.

Attenuation limit versus Frequency for the Agc Amplifier (Appendix B.2); - - - limited by noise; —— approximated (3.30); O measured ; ▲ given by TIME.

transistors Q_1 and Q_2 cannot be treated independently. Also, parasitic capacitances such as C_p and other phase effects become important. At lower frequencies (3.30) becomes very high and signal detection is limited by noise.

In order to illustrate the effect of signal feedthrough on distortion, consider the emitter-driven pair at high attenuation levels (Figure 3.4). At moderately high attenuation levels feedthrough signal i_L is negligible with respect to signal i_m from the g_m current generator of Q_2. The distortion caused by base resistance thus prevails.

For a higher attenuation i_L becomes comparable in magnitude with i_m but is excessively distorted due to the exponential $I_C - V_{BE}$ relationship of Q_1 and also because i_L is obtained from a high-pass filter. Signals i_m and i_L are represented in Figure 3.6 for $p_1 + p_2 = 45^\circ$. If $p_1 + p_2 = 90^\circ$, i_m and i_L would have opposite polarity. The fundamental components in i_m and i_L would cancel and cause infinite relative distortion. For $p_1 + p_2 = 45^\circ$ only partial cancellation occurs and thus the distortion is higher than expected. This is also true for the agc quad. Only odd-order distortion occurs (Figure 3.6) but with higher magnitude than expected. In Figure 3.6, both the resultant waveforms for the pair and the quad have been computed by TIME $\lceil 10 \rceil$, but have also been observed on the scope screen as shown in Figure 3.7. This data is taken for the pair and the quad described respectively in

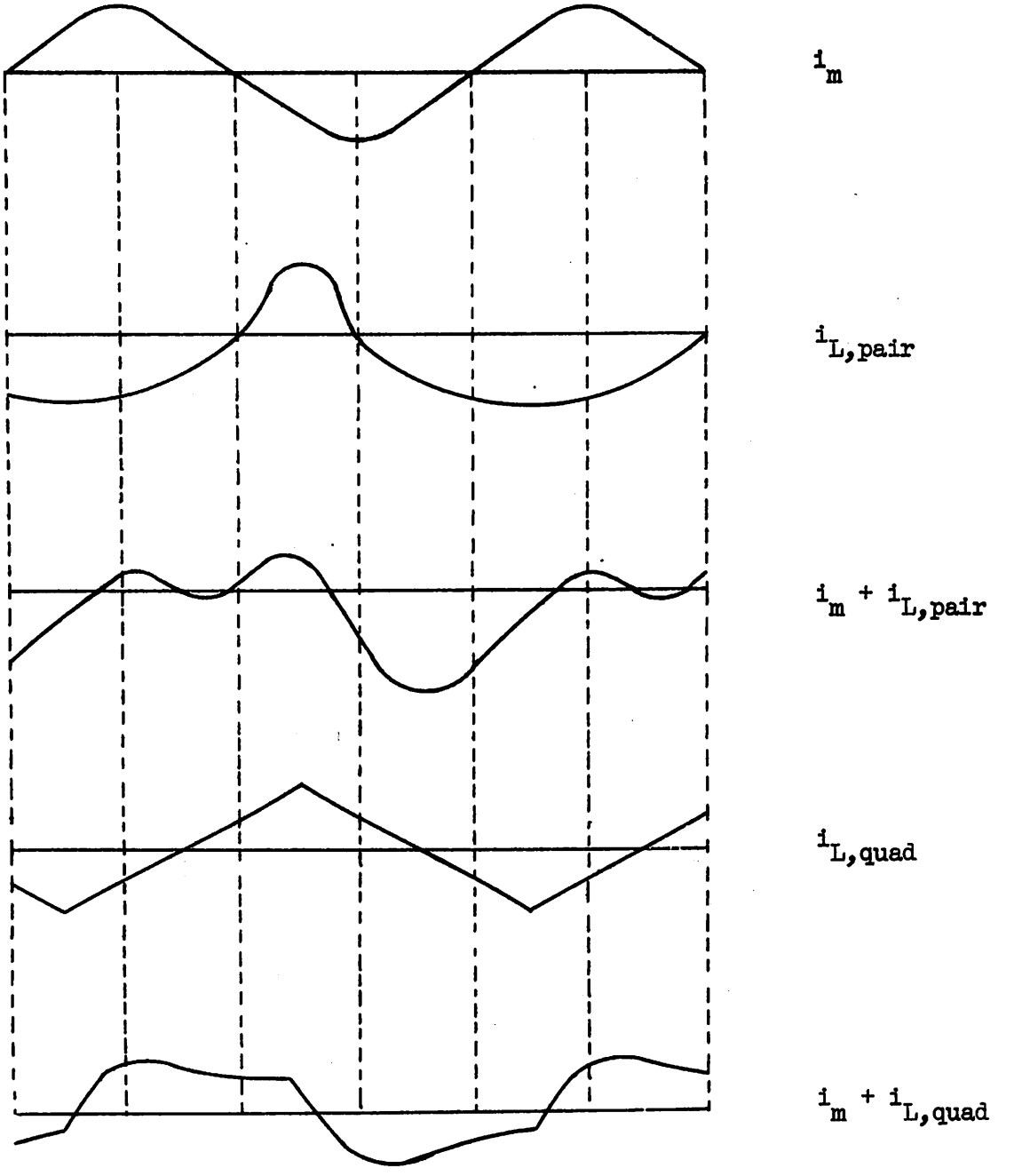
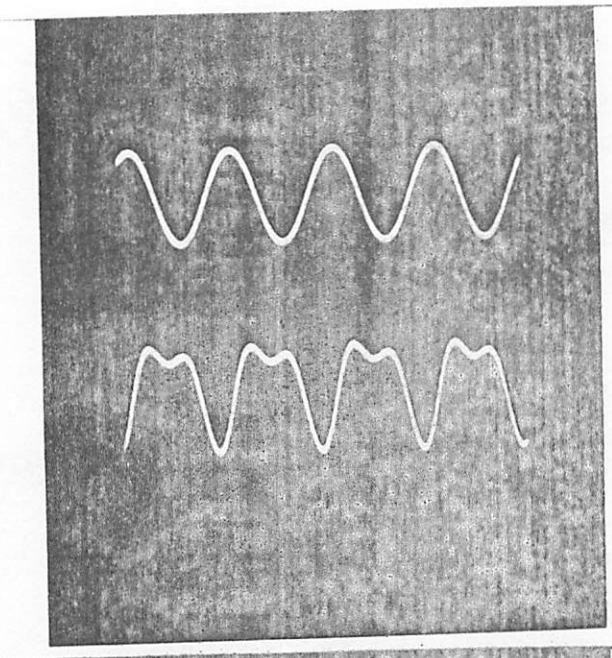


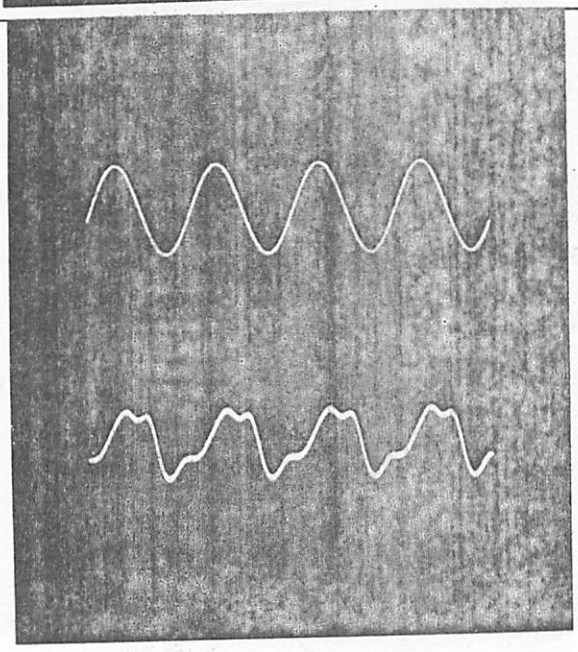
Figure 3.6.

Output waveforms of Pair and Agc Quad when Current Source Signal i_m and Feedthrough Signal i_L are of equal amplitude, computed by TIME [10] for $p_1 + p_2 = 45^\circ$.



PAIR

upper trace : 100 mV/div
lower trace : 5 mV/div



QUAD

upper trace : 100 mV/div
lower trace : 2 mV/div

Figure 3.7

Photographs of Input (upper trace) and Output (lower trace)Waveforms of Pair and Agc Quad observed on scope screen for the circuits of Appendix B.1 and Appendix B.2 at 180 MHz.

Appendix B.1 and B.2 at 60 MHz.

When Q_2 is turned off completely, the output signal consists uniquely of i_L and differs in phase from i_m as given by (3.30). The distortion is now lower (no cancellation in fundamental components can occur) and entirely due to the exponential input characteristic of the conducting transistors.

For Gilbert's quad (Figure 2.13) the ac half circuit model under high attenuation is obtained by interchanging the position of r_B and C_{jE} in Q_2 (Figure 3.4). For moderately high frequencies, (3.29) can be replaced by

$$|i_L| \simeq v_i C_\mu \omega \quad \arg(i_L) \simeq 90^\circ - p_2 \qquad \ldots (3.31)$$

Using (3.25), (3.27) and (3.31) the attenuation range is then given by

$$|AR_G| \simeq \frac{\omega_T}{C_\mu r_B \omega^2} \quad \arg(AR_G) \simeq -180 + p_1 + p_2 \ldots (3.32)$$

This is less than in the agc amplifier for frequencies below $\frac{1}{C_{jE} r_B}$. As pointed out before however, Gilbert's quad is not suitable for high attenuation ranges due to its excessive distortion caused by base resistance.

CHAPTER 4.

ANALYSIS OF NOISE IN HIGH-PERFORMANCE VARIABLE-GAIN AMPLIFIERS

4.1 INTRODUCTION

For a given output signal level, the gain of a variable-gain amplifier is maximum when the amplitude of the input signal is minimum. The lower limit of the amplitude of the input signal is thus established by the noise generated in the amplifier.

At low frequencies, the amount of noise is predicted by hand calculations for the agc amplifier, the multiplier and Gilbert's quad. For each case, the dominant noise sources are isolated and their noise contribution at the output is given by a simple expression. It has thus become possible to predict the noise performance of all variable-gain amplifiers considered in this study. These results, obtained for low frequencies, are verified by means of the circuit analysis program CANCER [11]. First-order approximations aided by extensive use of the same program extend the noise analysis towards high frequencies.

This chapter is initiated by a review of the noise model of a transistor and the definitions of noise temperature, noise resistance and noise figure. The effect of bias resistors and of emitter degeneration on noise performance is examined next. This is followed by the noise analysis of an emitter follower with noisy load, the common base stage, base-driven pair, the cascode amplifier and finally the emitter-driven pair at several attenuation levels. This leads directly to the analysis and comparison of the noise behavior of the agc

amplifier, the multiplier and Gilbert's quad.

4.2 CHARACTERIZATION OF NOISE IN A SINGLE TRANSISTOR

In a transistor the following two types of noise are considered : the thermal noise power $d(v_B^2)$ generated in the base resistance r_B , and the shot noise powers $d(i_B^2)$ and $d(i_C^2)$ caused by the dc current flow in the base (I_B) and collector (I_C) respectively. They are given by [15]

$$d(v_B^2) = 4kT\, r_B\, df \qquad \ldots (4.1)$$

$$d(i_B^2) = 2q\, I_B\, df \qquad \ldots (4.2)$$

and $$d(i_C^2) = 2q\, I_C\, df \; ; \qquad \ldots (4.3)$$

kT/q = 26 mV at $302^{\circ}K$ and $q = 1.610^{-19}$ C; df is the frequency band over which the noise power is to be taken. Flicker noise is not considered, since only higher frequencies are of interest.

These noise sources can be lumped into an equivalent noise voltage source $d(v_i^2)$ and an equivalent noise current source $d(i_i^2)$ at the input of the transistor model (Figure 4.1). They are given by

$$d(v_i^2) = d(v_B^2) + \frac{d(i_C^2)}{g_m^{\,2}} \qquad \ldots (4.4)$$

$$\text{and} \quad d(i_i^2) = d(i_B^2) + \frac{d(i_C^2)}{|\beta(j\omega)|^2} \qquad \ldots (4.5)$$

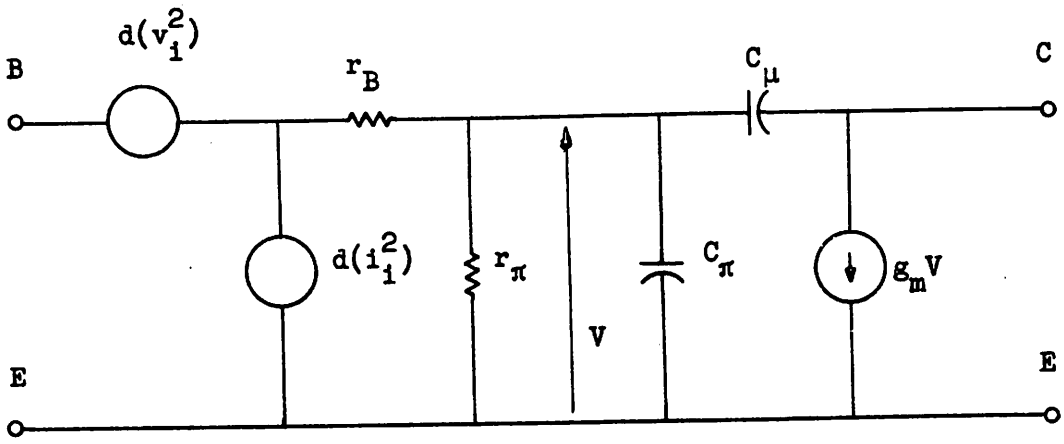


Figure 4.1.

Equivalent Noise Model of Transistor in Common-Emitter Configuration.

in which $\beta(j\omega) = \dfrac{\beta}{1 + j\omega/\omega_\beta}$. The equivalent noise sources are correlated because $d(i_C^2)$ contributes to both of them. Interaction of the two sources will thus yield a non-negligible noise component.

When a signal source with source resistance R_S is connected to an amplifier with power gain G (Figure 4.2.a) then the output signal power S_o is related to the input signal power S_i by

$$S_o = G S_i \qquad \ldots (4.6)$$

This is also true for the source noise power N_i if the amplifier is noiseless and thus

$$N_o' = G N_i \ . \qquad \ldots (4.7)$$

However, taking into account the equivalent input noise power of the amplifier N_G (Figure 4.2.b), the total output noise power becomes

$$N_o = N_o' + G N_G \quad \text{or} \quad G(N_i + N_G) \qquad \ldots (4.8)$$

The noise figure of an amplifier is the ratio of the input signal-to-noise ratio to the output signal-to-noise ratio. It is thus given by

$$F = \frac{\frac{S_i}{N_i}}{\frac{S_o}{N_o}} = 1 + \frac{N_G}{N_i} \qquad \ldots (4.9)$$

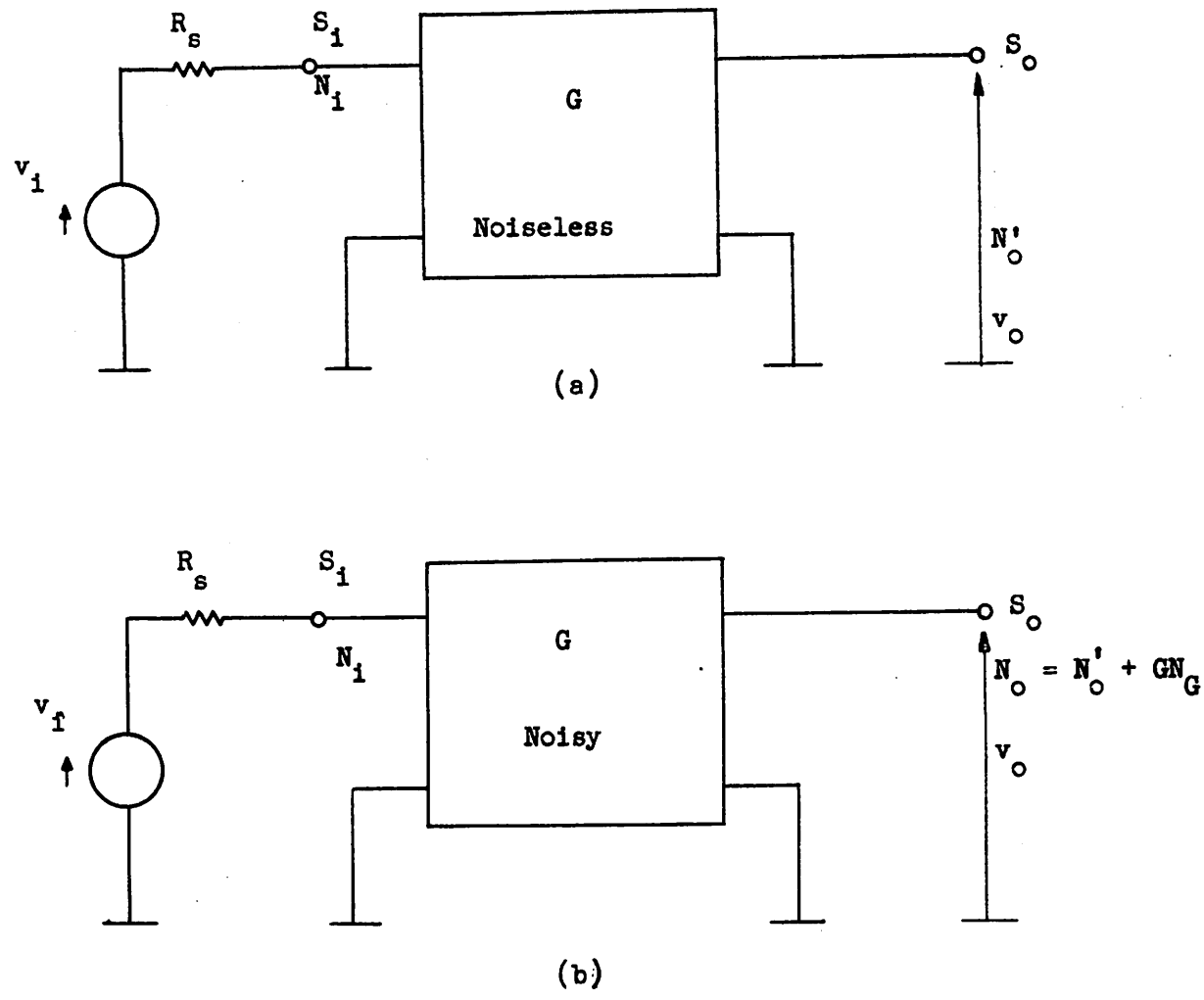


Figure 4.2.

The Definitions of Input Signal and Noise Power S_i and N_i and Output Signal and Noise Power S_o and N_o when an Input Signal with Source-resistance R_s is amplified by an Amplifier with Power Gain G and Equivalent Input Noise Power Contribution N_G.

It indicates how much the signal-to-noise ratio of a signal source with resistance R_S has been lowered by amplifying this signal with a noisy amplifier. The noise temperature T_N is defined as the absolute temperature that the source R_S would have to take in order to generate the same N_o with a noiseless amplifier. Therefore, T_N is given by

$$T_N = T_S \frac{N_G}{N_i} \qquad \ldots (4.10)$$

where T_S is the absolute temperature of the source resistance. The noise resistance R_N is defined as the value for R_S that would generate the same N_o again with a noisless amplifier:

$$R_N = R_S \frac{N_G}{N_i} \quad . \qquad \ldots (4.11)$$

The noise contribution of the amplifier N_G can thus be described by any of these three parameters since they are inter-related by

$$F - 1 = \frac{R_N}{R_S} = \frac{T_N}{T_S} \qquad \ldots (4.12)$$

For a variable-gain amplifier, the noise figure is not a useful measure because N_G in (4.9) depends on the gain of the amplifier. Therefore, the output signal-to-noise ratio S_o/N_o is used for a given source resistance. For a wide-band amplifier, noise is usually specified as spot noise. This means that the noise is measured over a narrow bandwidth Δf to which the amount of noise is directly proportional. Variation of noise power with frequency is thus easily dealt with

if Δf is small.

4.3 NOISE PERFORMANCE OF ELEMENTARY TRANSISTOR CONFIGURATIONS

To obtain a better insight into the noise behavior of the emitter-driven pair and the quads, the noise analysis is reviewed for several single-transistor configurations, the base-driven pair and the cascode. In all cases, the equivalent input noise sources are calculated. This is done by consecutively open and short circuiting the input terminals and calculating the output noise power.

4.3.1 SINGLE TRANSISTOR WITH BIAS RESISTORS [15]

All bias resistors of a transistor in the common emitter configuration can be lumped into one resistance R_S in series with the base lead or into one shunt resistance R_H from base to ground. Series resistance R_S adds a noise voltage source $d(v_{R_S}^2)$ of the form (4.1). Thus the equivalent noise sources can be taken out in front of R_S by modifying (4.4) into

$$d(v_{iS}^2) = d(v_i^2) + d(v_{R_S}^2) + R_S^2\, d(i_i^2) \qquad \ldots(4.13)$$

whereas (4.5) remains unchanged. Shunt resistance R_H adds a current noise source $d(i_{R_H}^2)$ which is derived from (4.1) and given by

$$d(i_{R_H}^2) = \frac{d(v_{R_H}^2)}{R_H^2} \quad \text{or} \quad \frac{4\,kT\,df}{R_H} \qquad \ldots (4.14)$$

In order to move the equivalent noise source in front of the bias resistor R_H, (4.4) remains unchanged but (4.5) changes into

$$d(i_{iH}^2) = d(i_i^2) + d(i_{R_H}^2) + \frac{d(v_i^2)}{R_H^2} \qquad \ldots (4.15)$$

As can be seen from the above equations, low series resistance (R_S in (4.13)) and high shunt resistance (R_H in (4.15)) hardly affect the noise performance of a transistor.

4.3.2 EMITTER DEGENERATION

For the equivalent input noise sources, a resistance R_E in the emitter lead has the same effect as a series resistance R_S in the base lead. The equivalent noise voltage source $d(v_{iE}^2)$ is thus given by (4.13) with R_E replacing R_S :

$$d(v_{iE}^2) = d(v_i^2) + d(v_{R_E}^2) + R_E^2\, d(i_i^2) \; . \qquad \ldots (4.16)$$

The equivalent noise current source is still given by (4.5).

The noise figure for a transistor ($\beta \gg 1$) in the common-emitter configuration with emitter resistor R_E is thus found from (4.9) and given by

$$F = 1 + \frac{4\,kT(R_E + R_B)\,df + (\frac{r_\pi^2}{\beta} + R_S^2)\,(2q\,I_B\,df)}{4\,kT\,R_S\,df} \; . \qquad \ldots (4.17)$$

If source resistance R_S is smaller than about $\left[2\beta r_\pi\,(R_E + r_B)\right]^{1/2}$ (4.17) can be simplified to

$$F = 1 + \frac{R_E + r_B}{R_S} \; . \qquad \ldots (4.18)$$

An emitter follower with emitter resistor R_E and source resistance R_S has the same noise figure as given by (4.18). However, the emitter follower only has a voltage gain of about unity such that the equivalent input noise voltage of the next stage is referred back unattenuated to the input of the emitter follower. In Figure 4.3, an emitter follower is shown with a "noisy load." This means that at the emitter of the emitter follower, noise is contributed by R_L and also by the next stage. This noise power is given by $d(v_L^2)$ in Figure 4.3.a or by $d(i_L^2)$ in Figure 4.3.b such that $d(v_L^2) = R_L^2\, d(i_L^2)$. However, this noise power can be referred back to the input (Figure 4.3.c) so that the equivalent input noise voltage source becomes

$$d(v_{NL}^2) = d(v_{iE}^2) + \left(\frac{R_E}{R_E + R_L}\right)^2 \left[d(v_L^2) + R_L^2 \left(d(i_i^2) + d(i_L^2)\right) \right] \quad \ldots (4.19)$$

instead of only $d(v_{iE}^2)$ given by (4.16). Usually the terms in R_L^2 are negligible, but the contribution of $d(v_L^2)$ can be quite significant.

4.3.3 COMMON BASE STAGE

It is readily shown that the equivalent input noise generators for a transistor in common emitter and in common base configuration are the same and thus given by (4.4) and (4.5). In 4.3.2, it has been shown that the equivalent noise voltage is greatly

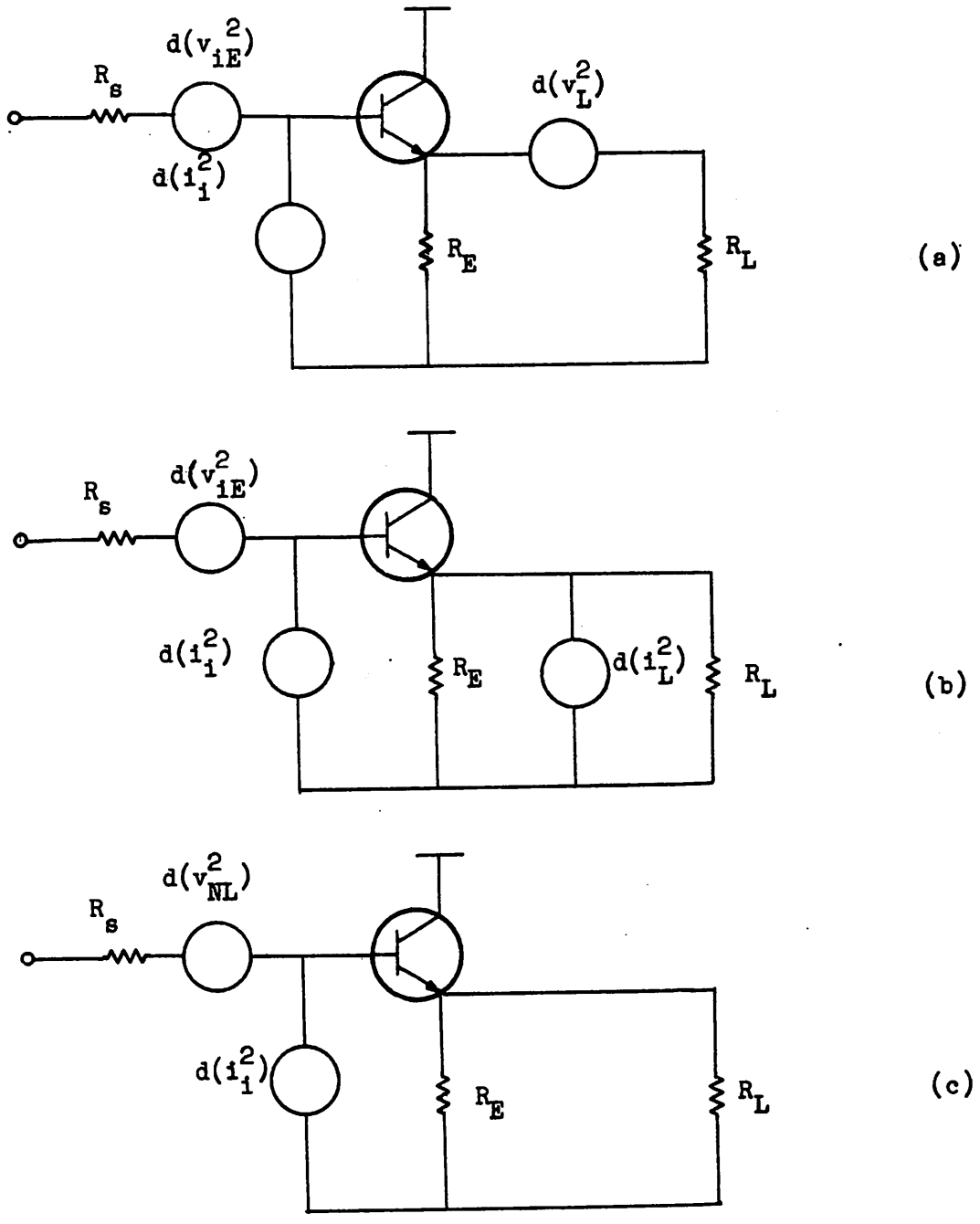


Figure 4.3.

Emitter Follower with Load R_L. Noise Contributed by R_L and Following Stages (not shown) is represented by Equivalent Noise Voltage Source $d(i_L^2)$ in (a) or by Equivalent Noise Current Source $d(i_L^2)$ in (b) or can be taken into account by the Equivalent Input Noise Voltage Source $d(v_{NL}^2)$.

increased when the voltage gain is unity. In a common base amplifier, the current gain is unity. Thus the noise current $d(i_L^2)$ due to the load and the next stage adds to the equivalent input noise sources, which are then given by ($\beta \gg 1$)

$$\begin{cases} d(i_{CB}^2) = d(i_i^2) + d(i_L^2) \\ d(v_{CB}^2) = d(v_i^2) + \dfrac{d(i_L^2)}{g_m^2} \end{cases} \quad \ldots (4.20)$$

Thus the emitter follower and the common base stage have in common that they are unable to shield the noise of their load from their input.

4.3.4 BASE-DRIVEN PAIR (FIGURE 2.3)

Initially assume that the current source is noiseless. Since the noise currents in both pair transistors are the same (if $\beta \gg 1$) and both caused by the noise sources in both transistors, the noise output from a differential output is twice that from a single-ended output. Taking a differential input or a single-ended input does not change the result as long as the source resistance from one base to the other is the same. Thus, changing from a balanced to an unbalanced output configuration without modifying R_L reduces both the gain and also the RMS noise voltage by a factor of two. The output signal-to-noise ratio thus remains the same and so does the noise figure.

For a single-ended input and output, the equivalent input noise sources are readily obtained from Section 4.3.2. One pair transistor is assumed to have as emitter resistance the noisy common-base input resistance of the other transistor. If noise contributions from the collector loads and following stages are neglected, then the equivalent input noise generators are obtained from (4.5) and (4.19) in which resistors R_E and R_L are noiseless and given by

$$R_E = \infty$$

$$\text{and } R_L = \frac{2\,V_T}{I_E} \quad .$$

The noise generators are then given by (4.5) and

$$d(v_{BP}^2) = 2\ d(v_i^2) + \left(\frac{2\,V_T}{I_E}\right)^2 d(i_i^2) \qquad \ldots (4.21)$$

In general, the current source itself delivers noise power $d(i_{CS}^2)$ to the pair. This does not affect the noise from a differential output, but for a single-ended output one fourth of $d(i_{CS}^2)$ is to be added to the output noise power. The equivalent input noise generators are then given by

$$\begin{cases} d(v_{BD}^2) = 2\left\{ d(v_i^2) + \left(\frac{2V_T}{I_E}\right)^2 \left[d(i_i^2) + \tfrac{1}{2}\, d(i_{CS}^2) \right] \right\} \\ d(i_{BD}^2) = d(i_i^2) + \dfrac{d(i_{CS}^2)}{4\beta^2} \end{cases} \qquad \ldots (4.22)$$

4.3.5 CASCODE AMPLIFIER

The equivalent input noise generators for transistor Q_1 in the cascode (Figure 4.4.a) are denoted by $d(v_1^2)$ and $d(i_1^2)$ and are given by (4.4) and (4.5); $d(v_2^2)$ and $d(i_2^2)$ are the ones for Q_2. The equivalent input noise generators for the cascode are then given by

$$\begin{aligned} d(v_C^2) &= d(v_1^2) + R_1^2\, d(i_2^2) \\ d(i_C^2) &= d(i_1^2) + \frac{d(i_2^2)}{\beta 2} \end{aligned} \qquad \ldots (4.23)$$

where $R_1 = \dfrac{2V_T}{I_E} + \dfrac{r_{B1}}{1+\beta_1}$.

Noise generator $d(v_2^2)$ does not contribute significantly and the contribution of $d(i_2^2)$ in (4.23) is usually negligible. A cascode thus has about the same noise performance as a single transistor.

To introduce the noise analysis of an emitter-driven pair, the equivalent input noise generators are calculated for a cascode with a noisy load R_C shunting Q_2 (Figure 4.4.b). They are given by

$$\begin{cases} d(v_{CR}^2) = d(v_1^2) + R_1^2 \left(1 + \dfrac{R_2}{R_C}\right)^2 \left[\dfrac{d(v_2^2) + d(v_R^2)}{R_C^2} + d(i_2^2) \right] \\ d(i_{CR}^2) = d(i_1^2) + \left(1 + \dfrac{R_2}{R_C}\right)^2 \left[\dfrac{d(v_2^2) + d(v_R^2)}{R_C^2} + d(i_2^2) \right] \end{cases} \qquad \ldots (4.24)$$

where $R_2 = \dfrac{1}{g_{m2}} + \dfrac{r_{B2}}{1+\beta_2}$ and $d(v_R^2)$ represents the

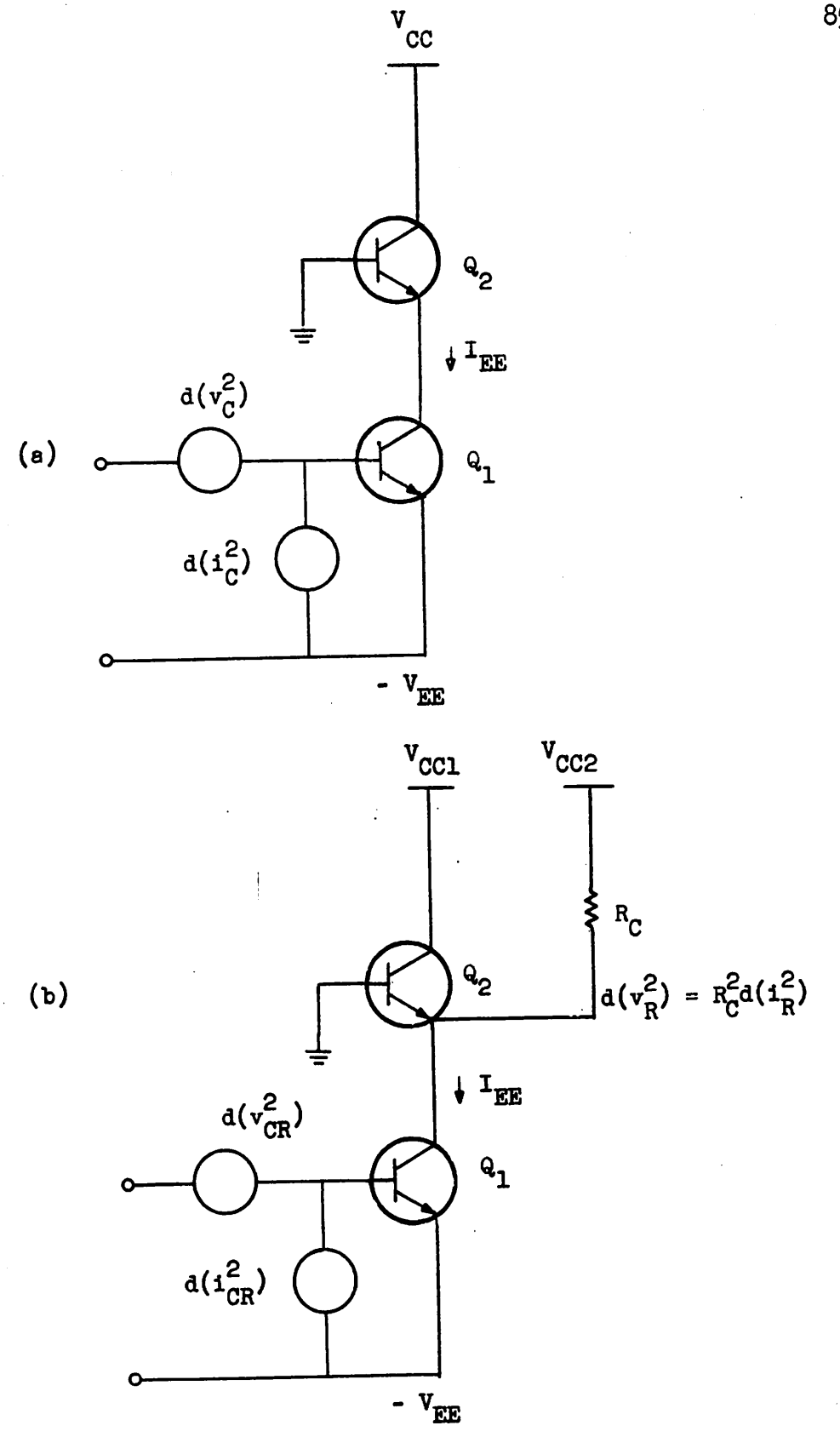


Figure 4.4.

(a) Cascode; (b) Cascode with Noisy Shunt Load R_C.

noise power associated with resistance R_C . If $R_2 \gg R_C$ the contributions from $d(i_2^2)$ and $d(v_2^2)$ are usually negligible so that (4.24) can be approximated by

$$\begin{cases} d(v_{CR}^2) \simeq d(v_1^2) + \left(\frac{R_1}{R_C}\right)^2 dv_R^2 \\ d(i_{CR}^2) \simeq d(i_1^2) + \frac{dv_R^2}{R_C^2} \end{cases} \quad \ldots (4.25)$$

The contribution of the noise sources of Q_2 increases when R_C becomes smaller and for $R_C = R_1$, both Q_1 and Q_2 add equal noise powers. This is the case of an emitter-driven pair (Figure 4.5) with zero control voltage V_A .

4.4 NOISE PERFORMANCE OF THE EMITTER-DRIVEN PAIR, THE AGC AMPLIFIER AND THE MULTIPLIER

The equivalent input noise sources of the emitter-driven pair, represented in Figure 4.5, depend on the circuit gain and are thus not a useful measure of noise. Therefore, the output noise power N_o and the output signal-to-noise ratio S_o/N_o are used instead. In Chapter 5, it is shown that this choice of noise parameters is most suitable for the design of low-noise variable-gain amplifiers.

At maximum gain, transistors Q_3 and Q_1 (Figure 4.5) form a cascode. The output noise power $d(i_o^2)$ is thus entirely due to transistor Q_1 . It is calculated in Section

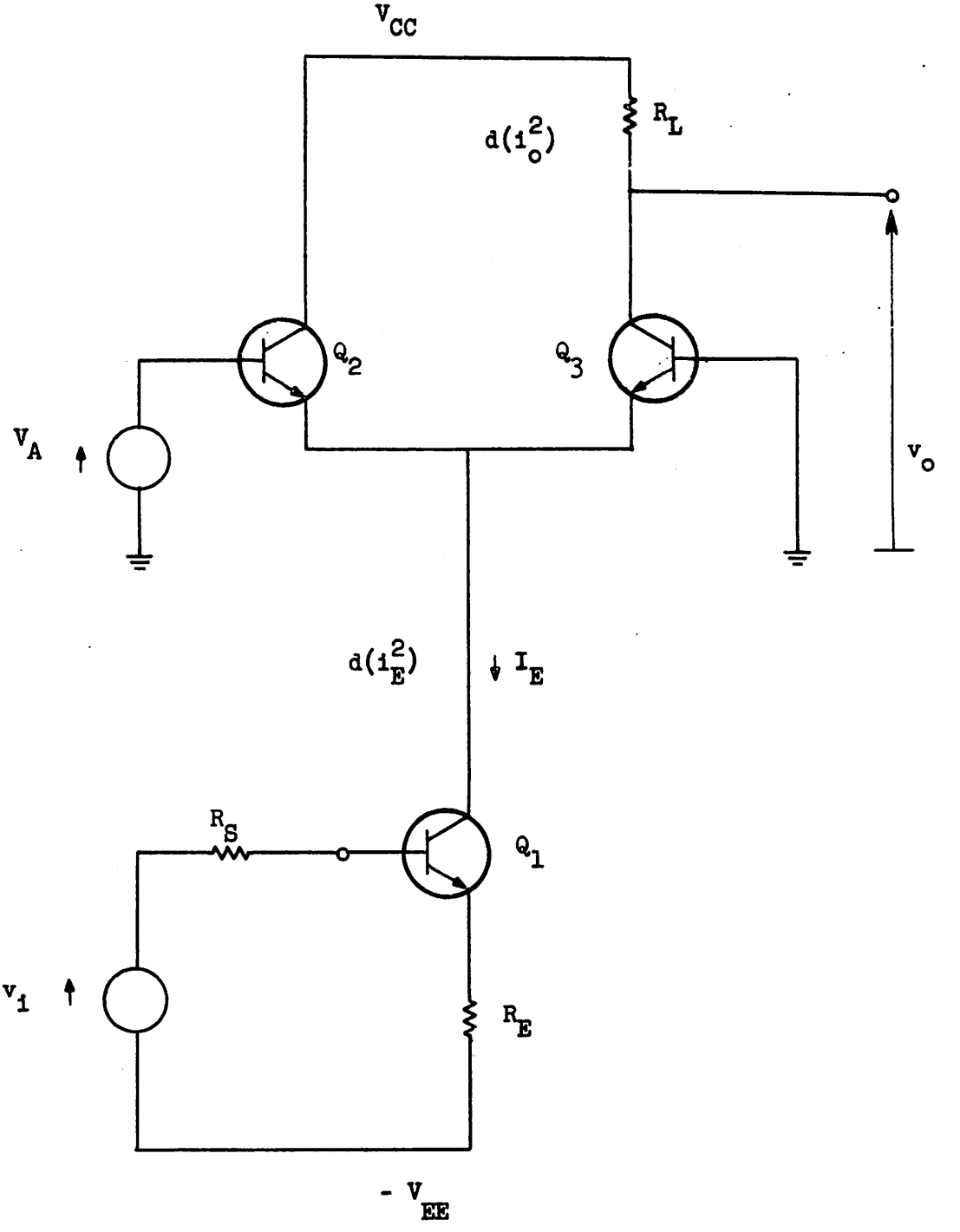


Figure 4.5.

Emitter-Driven Pair.

4.3.2 and given by

$$d(i_o^2) = d(i_E^2) = \frac{d(v_E^2)}{\left(R_E + \frac{V_T}{I_E}\right)^2} \qquad \ldots (4.26)$$

with $d(v_E^2) = d(v_i^2) + d(v_{R_E}^2) + d(v_{R_S}^2) + (R_E^2 + R_S^2)\, d(i_i^2)$;

$d(v_i^2)$ and $d(i_i^2)$ are given by (4.4) and (4.5) respectively;

$d(v_{R_E}^2)$ and $d(v_{R_S}^2)$ represent the thermal noise in resistors R_E and R_S. In most cases (4.26) can be simplified to

$$d(i_o^2) = \frac{4\,kT\,(r_B + R_E + R_S)\,df}{\left(R_E + \frac{V_T}{I_E}\right)^2} \; . \qquad \ldots (4.27)$$

When the gain is reduced, only a fraction of the noise power given by (4.27) reaches the output. If the relative voltage gain is denoted by x then the noise contribution at the output due to Q_1 is given by

$$d(i_o)_1^2 = x^2\, d(i_o^2) \qquad \ldots (4.28)$$

and is plotted versus x in Figure 4.6. However, the pair transistors Q_2 and Q_3 themselves now also contribute output noise power. This is obtained by considering Q_3 as an emitter follower with a noisy load consisting of the common-base input resistance of Q_2. The output noise generated by the pair is then given by

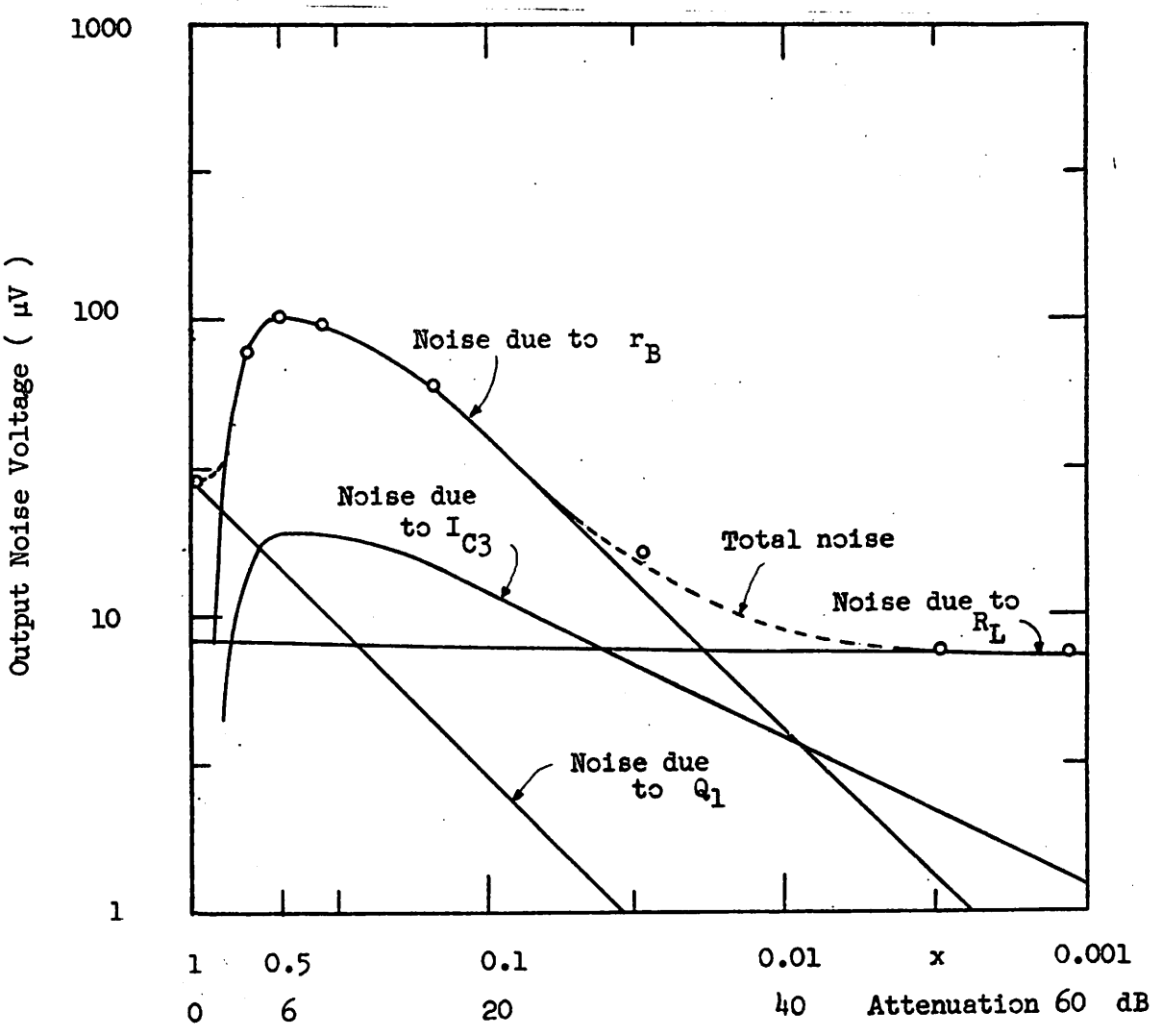


Figure 4.6.

Noise contributions of the dominant noise source in the Agc Amplifier, plotted versus Signal Attenuation x . For the Emitter-driven Pair, the curves have to be shifted down by 3 dB, —— computed; O measured for transistors CA 3045 (Appendix B.2).

$$d(i_o^2)_p = \frac{d(v_{i2}^2) + d(v_{i3})^2 + R_3^2 \left(d(i_{i2}^2) + d(i_{i3}^2) \right)}{(R_2 + R_3)^2} \qquad \ldots (4.29)$$

with $d(v_{i2}^2)$, $d(v_{i3})^2$, $d(i_{i2})^2$ and $d(i_{i3})^2$ given by (4.4) and (4.5) for Q_2 and Q_3 as indicated and $R_j = \frac{V_T}{I_{Ej}} + \frac{r_{Bj}}{1 + \beta_j}$ for $j = 2,3$. This can be written explicitly in terms of the attenuation level x by taking

$$I_{E3} = x\, I_E$$

and $$I_{E2} = (1 - x)\, I_E \,. \qquad \ldots (4.30)$$

For high attenuation ($x < \frac{1}{2}$),(4.29) can be simplified to

$$d(i_o^2)_{px} = 2\, q\, I_E\, x \left(\frac{4\, r_B}{V_T} I_E\, x + 1\right) df \qquad \ldots (4.31)$$

if $\frac{V_T}{r_B} < I_E < \frac{2\beta\, V_T}{r_B}$. For $x = \frac{1}{2}$ itself the output noise is given by

$$d(i_o^2)_{p\frac{1}{2}} = \frac{kT\, r_B}{2} \left(\frac{I_E}{V_T}\right)^2 \qquad \ldots (4.32)$$

which is about 6 dB lower than predicted by (4.31). The two terms of $d(i_o^2)$ are plotted versus attenuation x in Figure 4.6. At low attenuation, the first term of (4.31) which represents the thermal noise generated in both base resistances r_B is dominant. At high attenuation, the collector current I_{C3} shot noise of Q_3 dominates. The curves are obtained from noise computations by CANCER [11] for the pair described in Appendix B.1. For high attenuation, however, they correspond precisely with the asymptotic expressions given above.

The last component in output noise power is contributed by load resistance R_L and is given by

$$d(i_o)^2_L = \frac{4\ kT\ df}{R_L} \qquad \ldots (4.33)$$

which is also represented in Figure 4.6. The total output noise power is the sum of the noise powers given in (4.28), (4.31) and (4.33) and is represented in Figure 4.6 by a dotted line. At any given attenuation level x the relative values of I_E, r_B and R_L mainly determine which noise sources are dominant. The noise output power caused by r_B depends on the value of the quad current I_E given by (4.32), whereas the noise output power due to R_L is constant. They are equal for I_E given by

$$I_{EBL} = 2\sqrt{2}\ \frac{V_T}{\sqrt{R_L\ r_B}} \ . \qquad \ldots (4.34)$$

Thus in the case of Figure 4.6 $I_E > I_{EBL}$. The shot noise due to I_{C3} is negligible, except for very low I_E.

The noise output power of the agc quad is twice that of the emitter-driven pair and is thus also represented in Figure 4.6 by shifting the curves up by 3 dB.

If the pair is used as an automatic-gain control circuit with constant output signal, then the S_o/N_o characteristic is exactly the inverse of the N_o characteristic shown in Figure 4.6. For the agc quad, the output signal-to-noise ratio is 3 dB better than for the pair if the amplitude of the signal

current is the same in all pairs.

For the multiplier, used as a variable-gain circuit, the contributions from the dominant noise sources are plotted versus attenuation in Figure 4.7. Factor x which represents the current division in the pair, is included to illustrate how the graphs of Figure 4.7 are derived from those in Figure 4.6. As for the agc quad, the multiplier at maximum gain makes use of the excellent noise behavior of a cascode. However, whereas for the agc quad the r_B noise peaks only for $x = \frac{1}{2}$ (Figure 4.6), the r_B noise for the multiplier extends over nearly the whole attenuation range (Figure 4.7). For $I_E < I_{EBL}$ given by (4.34), r_B noise is dominated by R_L noise. The agc quad and the multiplier then exhibit the same output noise level independent of attenuation level.

The multiplier used as an agc amplifier delivers a constant output signal. The output signal-to-noise ratio is then obtained by inverting the graph of Figure 4.7. This leads to the surprising result that S_o/N_o is minimum at high attenuation and thus at high input signal levels, which is the inverse of the result for the agc quad.

It can thus be concluded that in noise performance the multiplier is inferior to the agc quad since the noise peak due to base resistance in the quad extends over all high attenuation levels in the multiplier.

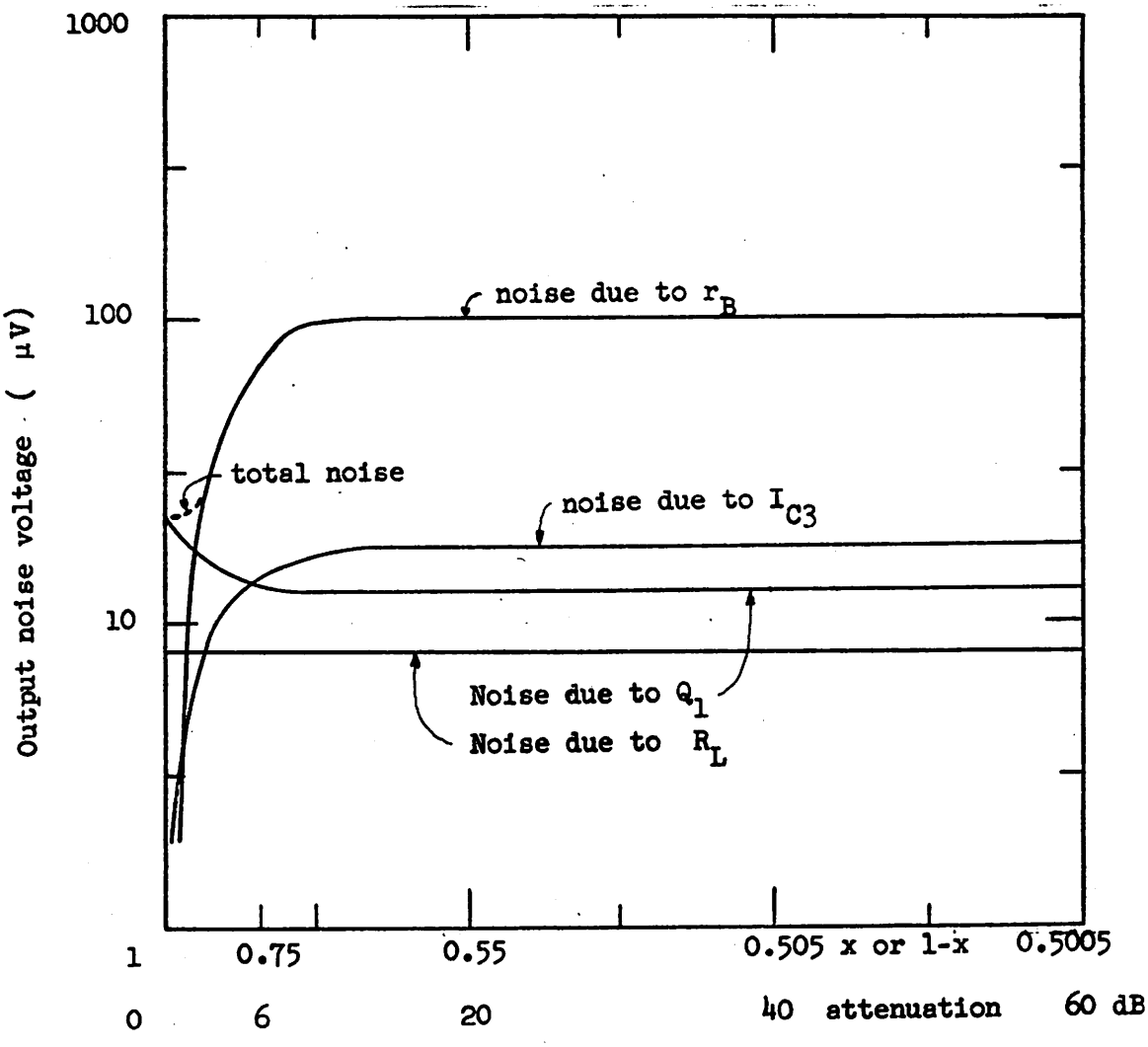


Figure 4.7.

Noise contributions from the Dominant Noise Sources in the Multiplier used as a Variable-gain Circuit (derived from Figure 4.6.)

At high frequencies, the noise contributions from R_L, Q_1 and I_{C3} in Figure 4.6 and 4.7 remain constant, but the noise output voltage due to r_B decreases with a slope of 20 dB/dec above the -3 dB frequency defined by $B = 1$. This is illustrated in Figure 4.8. The noise contributions from R_L, r_B and I_{C3} are plotted versus attenuation at low frequencies and at one high frequency. The noise from r_B has decreased significantly, except at high frequencies. The noise due to R_L and I_{C3} remain approximately unchanged. The curves were computed by CANCER [11] for the agc pair described in Appendix B.1.

It can be concluded that in a first-order analysis, noise generation at high frequencies is less import than at low frequencies and therefore need not be considered further.

4.5 GILBERT'S VARIABLE-GAIN QUAD

The currents I_{E1} and I_{E2} in Gilbert's quad (Figure 2.13) are usually [4] provided by a pair with total current I_{EE}, delivered by transistor Q_E, such that

$$I_{EE} = I_{E1} + I_{E2} . \qquad \ldots (4.35)$$

The circuit gain is then determined by the current ratio $k = I_{E2}/I_{E1}$ as shown in Figure 2.14.

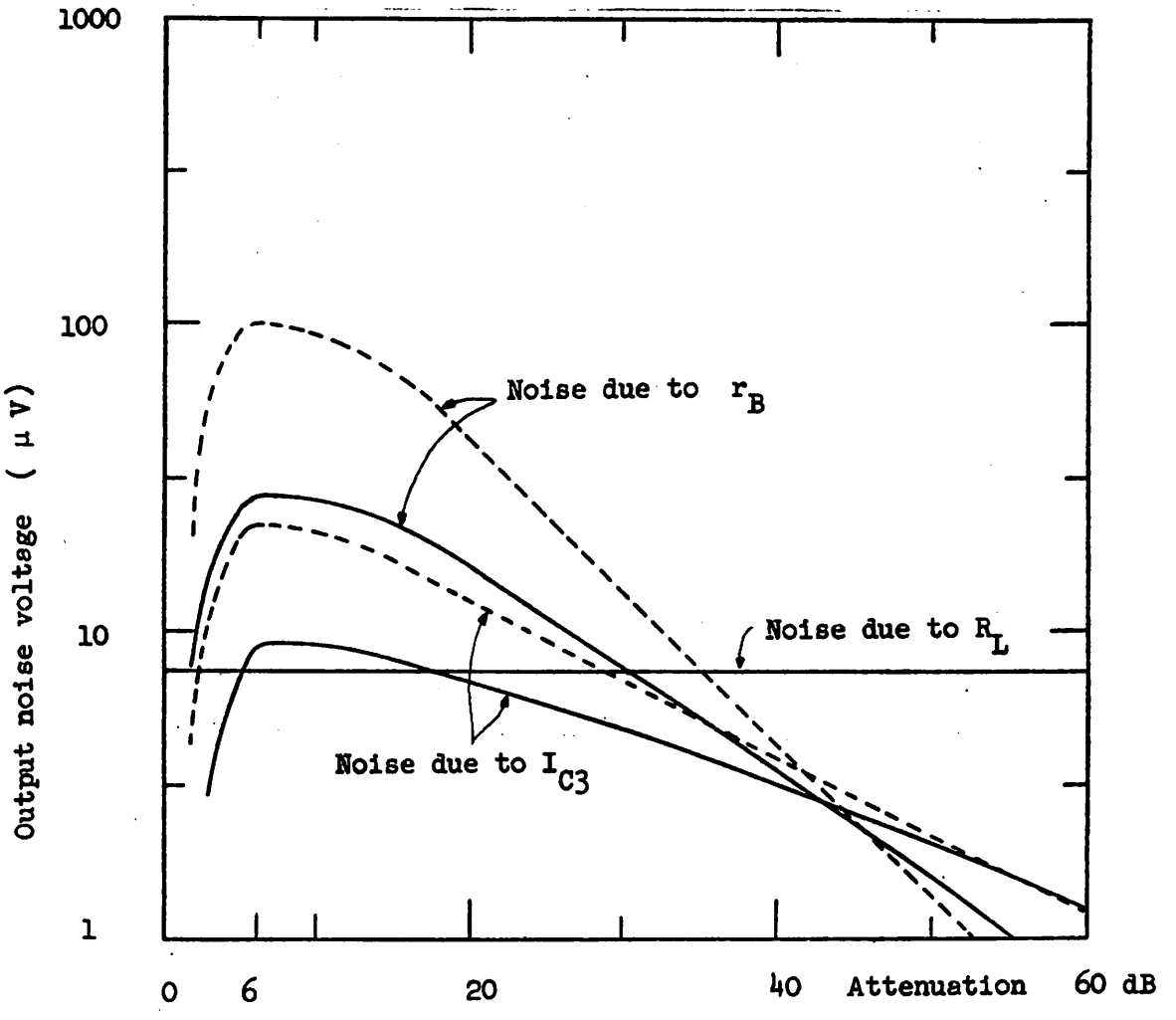


Figure 4.8.

Noise contribution of the Dominant Noise Sources versus Attenuation for the Agc Amplifier (Appendix B.2), computed at low frequencies (- - -) and at the -3 dB frequency (——) at which B = 7.

For a differential output no noise is contributed from the current source transistors carrying I_{E1}, I_{E2} and I_{EE}. However, if a single-ended output is taken, transistor Q_E, which carries the total current I_{EE}, does contribute noise to the output. If $d(i_o^2)_E$ represents the output noise of Q_E, the noise contribution at the load R_L is given by

$$d(v_o^2)_E = \tfrac{1}{2} \left(\frac{k}{k+1}\right)^2 R_L^2 \, d(i_o^2)_E \quad . \qquad \ldots (4.36)$$

The output noise power of the quad is twice that of the differential circuit, which then consists of transistors Q_1, Q_3 and Q_5. The output noise component due to Q_1 including R_E is given by

$$d(v_o^2)_1 = k^2 \frac{d(v_i^2)_1 + (R_{S/2})^2 \, d(i_i)_1^2}{\left(R_E + \frac{2V_T}{I_{E1}}\right)^2} R_L^2 \qquad \ldots (4.37)$$

in which $d(v_i^2)_1$ includes the effect of R_E as given by (4.16). The output noise components due to Q_3 and Q_5 are given by

$$d(v_o^2)_{3,5} = \left[\left(\frac{I_{E2}}{2V_T}\right)^2 \left(d(v_i^2)_3 + d(v_i^2)_5 \right) + k^2 \, d(i_i^2)_5 \right] R_L^2 \quad .. (4.38)$$

For (4.37) and (4.38) it is assumed that $k < \beta$. Comparison of (4.36), (4.37) and(4.38) shows that the noise source given by the first term in (4.38) is dominant if

$$k < \sqrt{\frac{2 \, r_B \, I_{E2}}{V_T}} \quad . \qquad \ldots (4.39)$$

Since $I_{E2} = I_{EE} \frac{k}{1+k}$, this dominant component for the complete quad can be written as

$$d(v_o^2) = \left(\frac{k}{1+k}\right)^2 \left(\frac{R_L I_{EE}}{2 V_T}\right)^2 16\,kT\,(r_{B3} + r_{B5})\,df \qquad \ldots (4.40)$$

and is plotted versus k in Figure 4.9. Also, since current division k is related to attenuation x by

$$x = \frac{k}{k+1}, \qquad \ldots (4.41)$$

the values of the dominant output noise components can also be plotted versus attenuation as shown in Figure 4.10. The output noise due to collector current shot noise in transistors Q_3 and Q_5 is also shown in Figure 4.9 and 4.10. However, for moderate current levels, they are less important than the thermal noise generated by the base resistances of the four quad transistors. The output noise voltage due to r_B reaches its peak value for high values of k or for $x = 1$ as given by (4.40). It is $2\sqrt{2}$ times higher than the r_B noise peak for the agc quad (obtained from (4.32)), if the base resistances r_B and the quad current I_{EE} are assumed to be equal. However, the noise peak for the agc quad occurs at 6 dB attenuation and for Gilbert's quad at 0 dB so that r_B noise for Gilbert's quad is only $\sqrt{2}$ times higher than for the agc quad, if the relative attenuation is high and the same in both quads. Also, the absolute voltage gain in Gilbert's quad is $R_E\, I_{EE}/V_T$ times higher than in the agc quad.

As for the agc quad, the relative importance of the noise due to r_B and R_L depends on the value of the quad current I_{EE}. Since the r_B noise peak in Gilbert's quad equals $2\sqrt{2}$ times the noise peak in the agc quad, the current I_{EE} at which

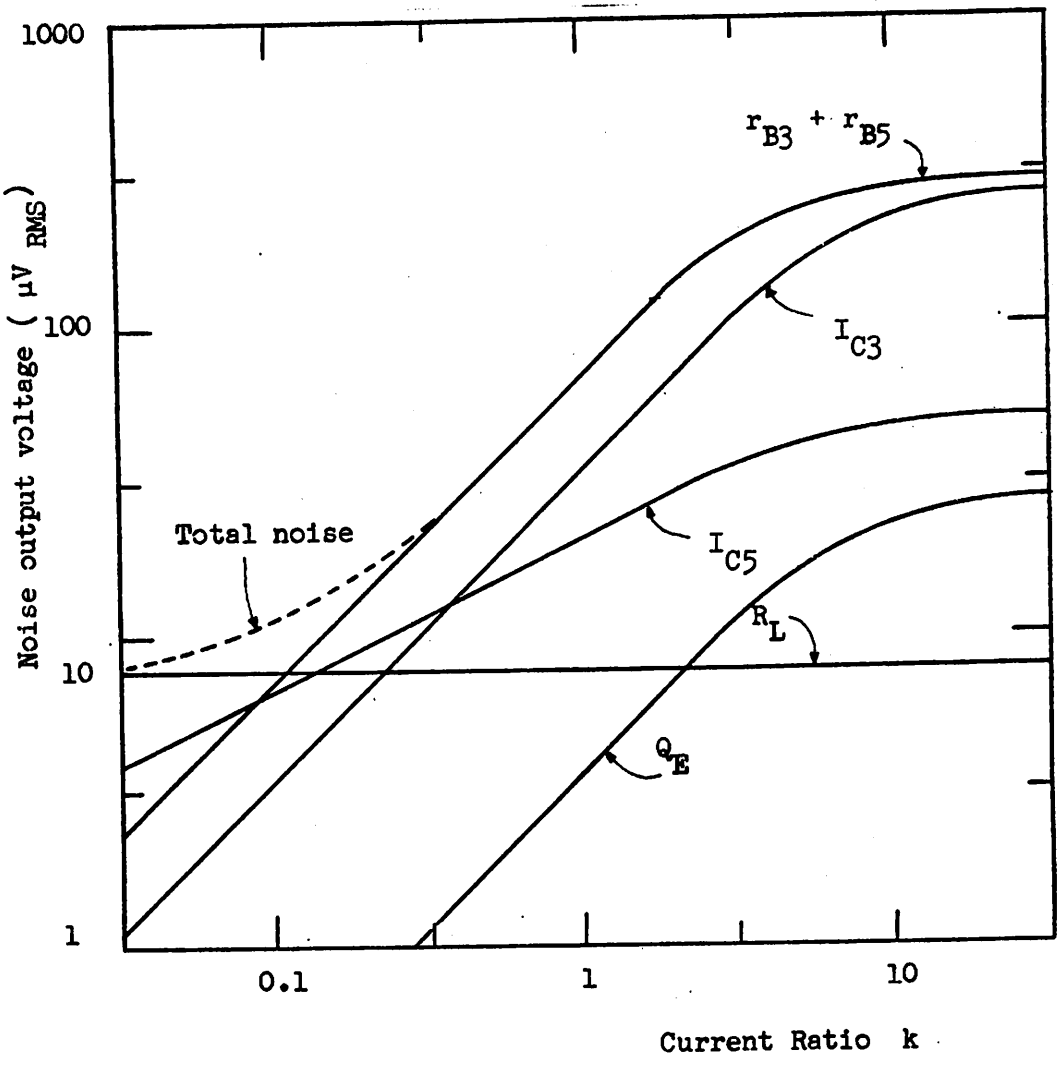


Figure 4.9.

Dominant output noise components in Gilbert's variable-gain quad versus current division k , computed by CANCER [11] for the circuit described in Appendix B.4.

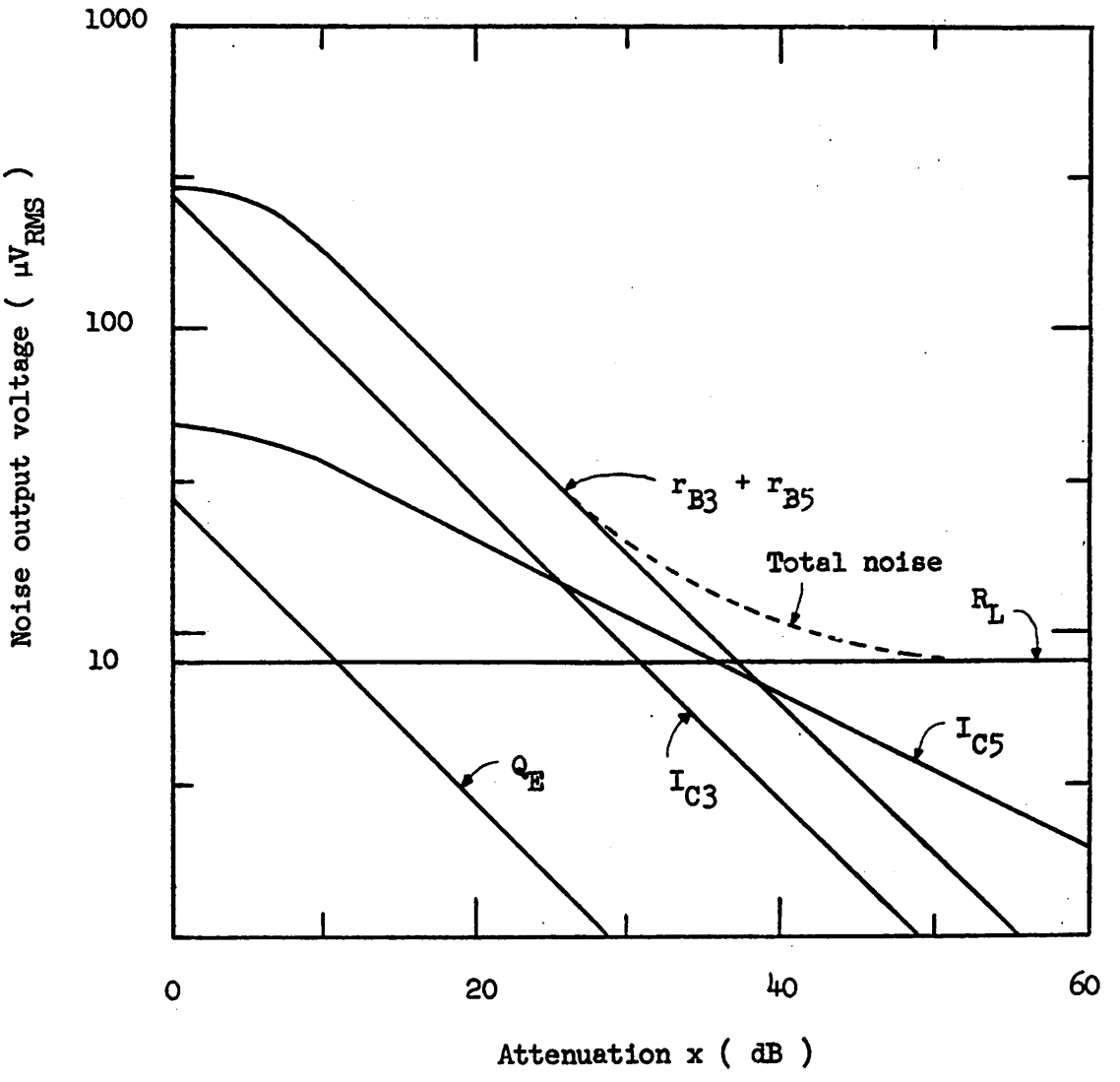


Figure 4.10.

Dominant output noise components versus attenuation for Gilbert's quad, derived from the curves of Figure 4.9.

maximum r_B noise equals R_L noise, is thus $2\sqrt{2}$ times lower for Gilbert's quad than for the agc quad (given by (4.34)).

At high frequencies, the noise contribution of the base resistances decreases so that the collector current shot noise becomes relatively more important. The change of noise level at high frequencies for Gilbert's quad is thus very similar to the agc quad and therefore not considered.

CHAPTER 5.

THE IMPROVED AGC AMPLIFIER

5.1 INTRODUCTION

The aim of this study is the realization of a variable-gain quad with maximum dynamic range-bandwidth product for a given type of transistor. In order to compare the three basic quads (i.e. the agc amplifier, the multiplier and Gilbert's quad) the dynamic range is optimized for each of these in turn. The dynamic range of an agc circuit is completely characterized if its dynamic range is known for all values of v_o. Thus, the amplitude of the signal output voltage v_o and the quad current I_{EE} are selected for maximum dynamic range (DR). The corresponding values of v_o, I_{EE} and DR are then expressed in terms of transistor parameters and collector load R_L.

In order to achieve a flat transfer characteristic over a wide frequency range, the quad current I_{EE} should be such that the quad presents a constant resistance to the input signal current. Since this is usually different from the optimum current for dynamic range, a compromise is to be made between the value of I_{EE} that gives the highest dynamic range and the value that gives the widest bandwidth.

All basic quads employ a base-driven pair with emitter degeneration as the input stage. In order not to degrade the performance of the quad, the input pair should thus exhibit an even wider frequency range than the quad itself.

Also, noise and distortion caused by the input pair should be lower than that contributed by the quad. It is shown that the current in the input pair I_P and the emitter resistor R_E can be chosen such that these conditions are fulfilled. Moreover, at low frequencies, the distortion of the pair can cancel the distortion of the quad under some conditions.

The agc amplifier is selected as the most suitable variable-gain quad for a high dynamic range over a wide frequency band. For optimum performance, the quad is biased at current I_{EE} and the pair at I_P which is usually higher than I_{EE}. The improved agc amplifier thus employs bleeder resistances R_B to make up for the difference I_Q between I_P and I_{EE}. One discrete and two integrated circuits have been realized to illustrate the advantages of optimum operating point operation.

5.2 OPTIMUM DYNAMIC RANGE OF THE AGC AMPLIFIER

In the agc amplifier, represented in Figure 2.8, the amplitude of the output signal voltage is determined by the voltage gain A_v, which is controlled by dc voltage V_B, and by the fractional current swing i_p, which is caused by input voltage v_i. The amplitude of the output voltage which is obtained for maximum A_v and unity current swing i_p is the highest encountered. It is given by

$$v_{oM} = \frac{I_{EE} R_L}{\sqrt{2}} \text{ Volt}_{RMS} \quad \ldots (5.1)$$

and is represented by point A in Figure 5.1. Any output voltage lower than v_{oM} can be obtained by reducing either A_v or i_p or both. In Figure 5.1, all combinations of A_v and i_p that yield identical v_o are represented by the straight line BC . At point B, A_v is maximum, whereas at point C, i_p equals unity. For all points on line BC , product $A_v i_p$ is thus constant and given by

$$A_v i_p = A_{v,\,max} \frac{v_o}{v_{oM}} \quad \ldots (5.2)$$

where $A_{v,\,max}$ is given by (2.42) and v_{oM} by (5.1). Maximum gain $A_{v,\,max}$ is achieved for all points on line AB . Lines parallel to AB thus represent constant - A_v lines, where the value of A_v is decreasing towards point C.

The potential dynamic range DR_P is then defined as the ratio of maximum to minimum current swing i_p or voltage gain A_v over line segment BC . It is thus given by

$$DR_P = 20 \log_{10} \frac{v_{oM}}{v_o} \text{ dB} \quad \ldots (5.3)$$

where v_{oM} is given by (5.1).

Distortion and noise limit the potential dynamic range by the dB quantities DRD and DRN respectively. The resultant dynamic range is then given by

$$DR = DR_P - DRD - DRN \quad \ldots (5.4)$$

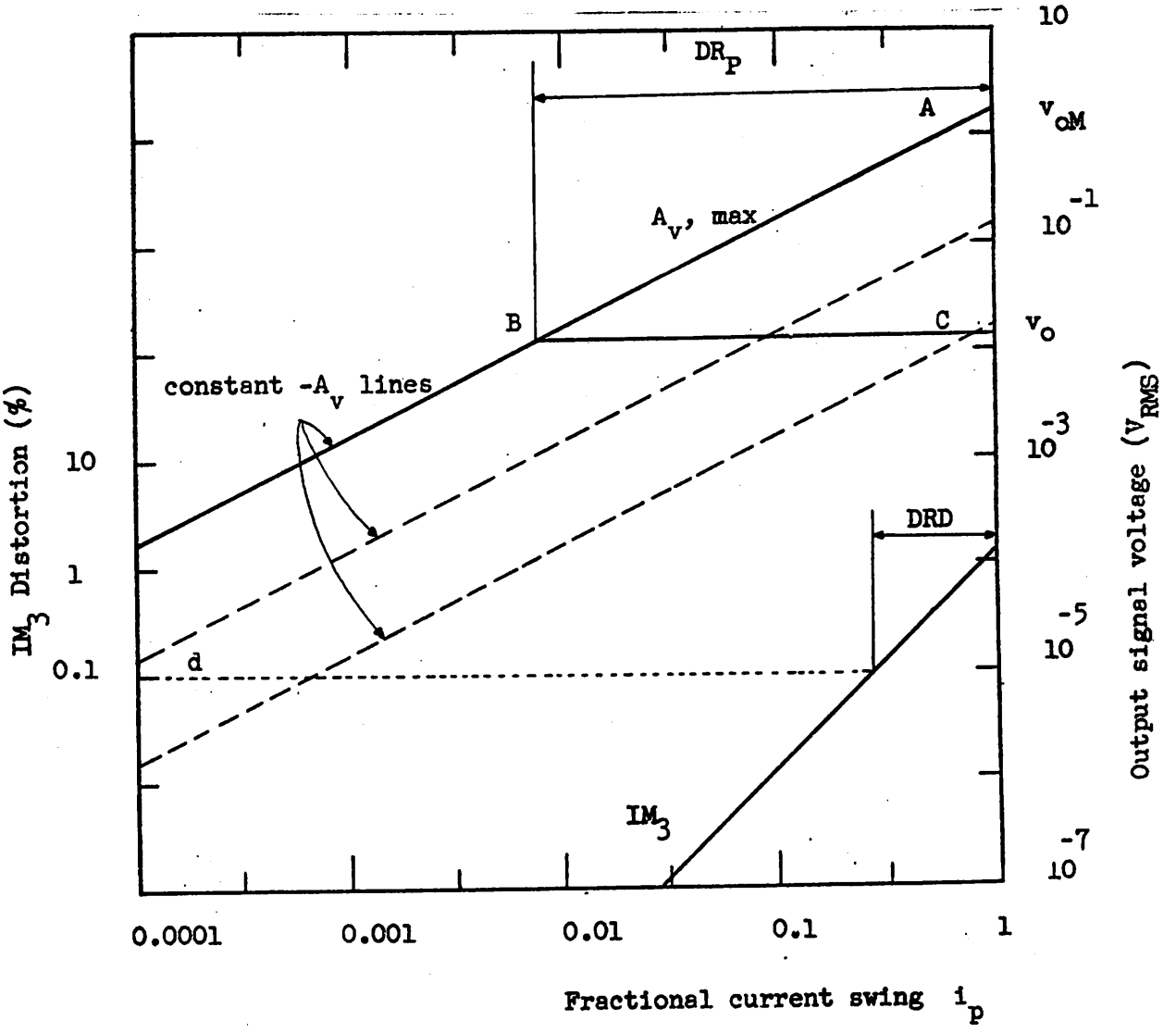


Figure 5.1.

Output Signal Voltage v_o and IM_3 Distortion versus Fractional Current Swing i_p.

At low frequencies, the distortion in the agc amplifier consists mainly of third-order distortion given by (2.38) which is also plotted versus i_p in Figure 5.1. It is assumed that the attenuation is high enough to reach the maximum distortion region. For a given maximum distortion d, the reduction in dynamic range DRD is read directly on the graph of Figure 5.1 or is calculated from (2.38) and given by

$$DRD = 20 \log_{10} \sqrt{\frac{3}{8d}} \frac{r_B I_{EE}}{2 \beta V_T} \qquad \ldots (5.5)$$

As an example, take I_{EE} = 10 mA, r_B = 100 Ω and β = 100. For 1% IM_3 at low frequencies, the reduction in dynamic range DRD only equals 1.4 dB, and 11.4 dB for 0.1% IM_3 .

The noise output of the agc amplifier consists mainly of noise due to the four base resistances r_B of the quad and the two collector loads R_L . In Section 4.4, it is shown that the noise generated by R_L is dominant if the quad current I_{EE} is lower than I_{EBL} , which is given by (4.34). The noise output voltage is then constant with respect to A_v and is given by

$$v_{oR_L} = \sqrt{8 \, kT \, R_L \, \Delta f} \; . \qquad \ldots (5.6)$$

For a required signal to noise ratio n , the minimum output voltage that can be chosen is thus given by

$$v_{o\,m} = n \, v_{oR_L} \; . \qquad \ldots (5.7)$$

However, since the potential dynamic range decreases with increasing v_o as given by (5.3), the resultant dynamic range is maximum when v_o equals v_{om} itself. This maximum dynamic range DR_M then equals the potential dynamic range DR_P and is found by substituting (5.1) in (5.3). It is given by

$$DR_M = 20 \log_{10} \frac{1}{\sqrt{2}} \frac{I_{EE} R_L}{v_{om}} \quad \ldots (5.8)$$

The substitution of v_{om}, given by (5.7) in (5.8) yields

$$DR_M = 20 \log_{10} \frac{I_{EE}}{4n \sqrt{kT R_L \Delta f}} \quad \ldots (5.9)$$

Expression (5.8) shows that the product of DR_M and v_{om} is only dependent on R_L and I_{EE}. Dynamic range can thus be exchanged for output voltage v_o and thus also for output signal-to-noise ratio n. For the resultant dynamic range, the value of DRD still has to be subtracted from (5.9).

For a given value of n, (5.7) yields the value of v_o at which DR is maximum. For lower values of v_o, the specification of n cannot be met. For higher values of v_o, the dynamic range decreases because the potential dynamic range decreases.

Usually, quad current I_{EE} is larger than I_{EBL} so that the noise peak caused by the base resistance r_B is greater than the noise due to R_L. The noise curves of Figure 4.6 can then be approximated as follows. For $x \geq 0.5$, the noise

due to r_B is constant and equal to the peak noise found from (4.32) and given by

$$v_{oB} = \frac{I_{EE} R_L}{V_T} \sqrt{kT\, r_B\, \Delta f} \quad . \qquad \ldots (5.10)$$

This approximation ignores the low-noise behavior of the quad at maximum gain. However, this low-noise region is of no practical use if a wide range of gain values is considered. For $x < 0.5$ the output noise voltage can be approximated by

$$v_{o\, r_B} = 4 \times v_{oB} \qquad \ldots (5.11)$$

where v_{oB} is given by (5.10). These asymptotic approximations are derived from Figure 4.6, and are represented in Figure 5.2. The axis of relative attenuation x is shown in line BC in Figure 5.2. Since $x = A_v/A_{v,max}$ the relation between x and i_p is found from (5.2) and given by

$$x.i_p = \frac{v_o}{v_{oM}} \qquad \ldots (5.12)$$

which also equals the inverse of the potential dynamic range (not in dB). Thus point B always coincides with $x = 1$ and for different values of v_o, point B shifts over the i_p axis. The noise curves are related directly to the x-axis and move accordingly as point B moves. This is illustrated in Figure 5.3 for two different values of v_o. Besides r_B and R_L noise, the noise curves in Figure 5.2 also represent noise due to I_{C3} (see Figure 4.6), which can be important at low current levels.

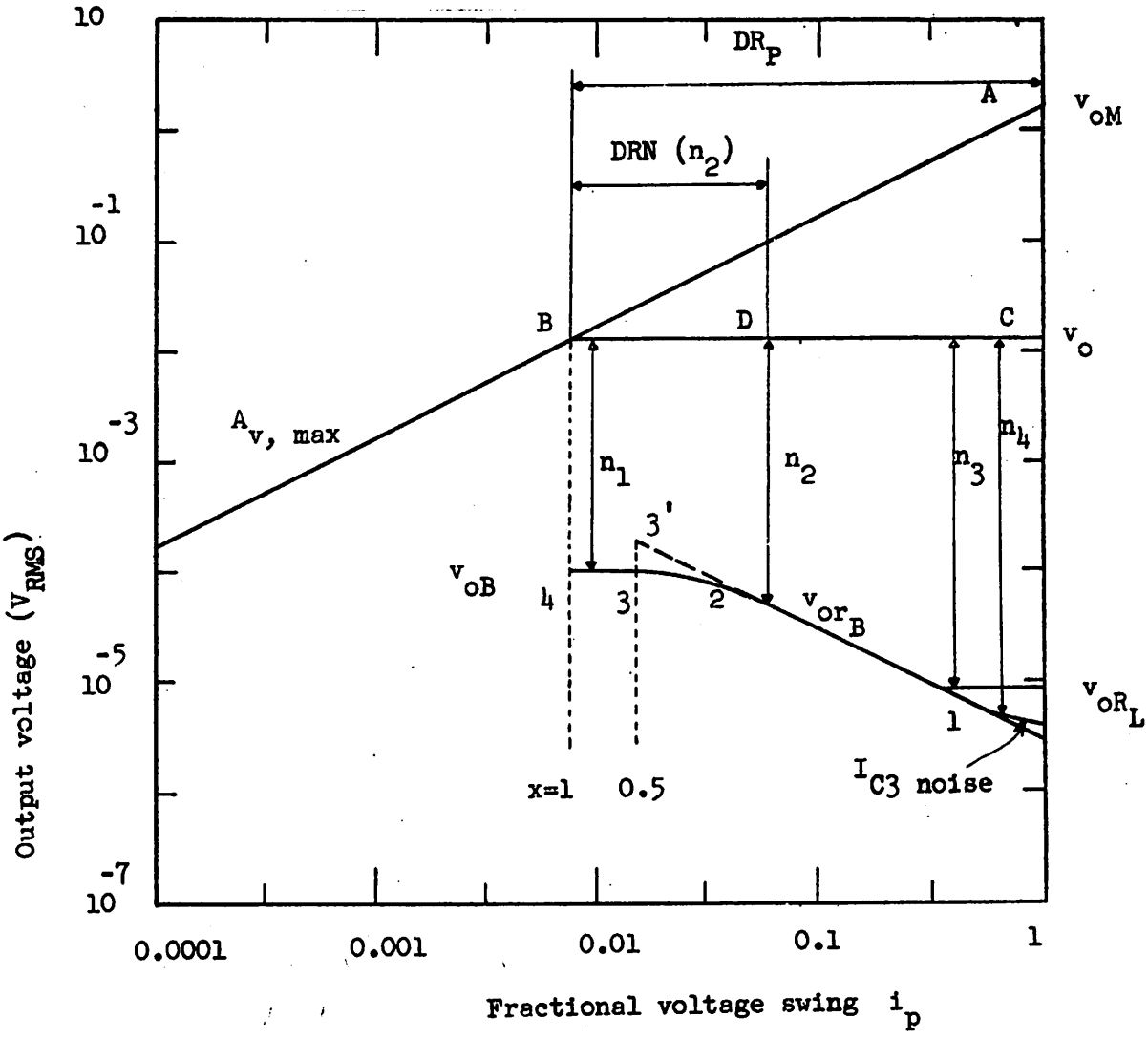


Figure 5.2.

Output Signal Voltage v_o and Output Noise Voltage (Figure 4.6) versus Fractional Current Swing i_p, for a given Quad Current I_{EE} and Signal-to-noise ratio n.

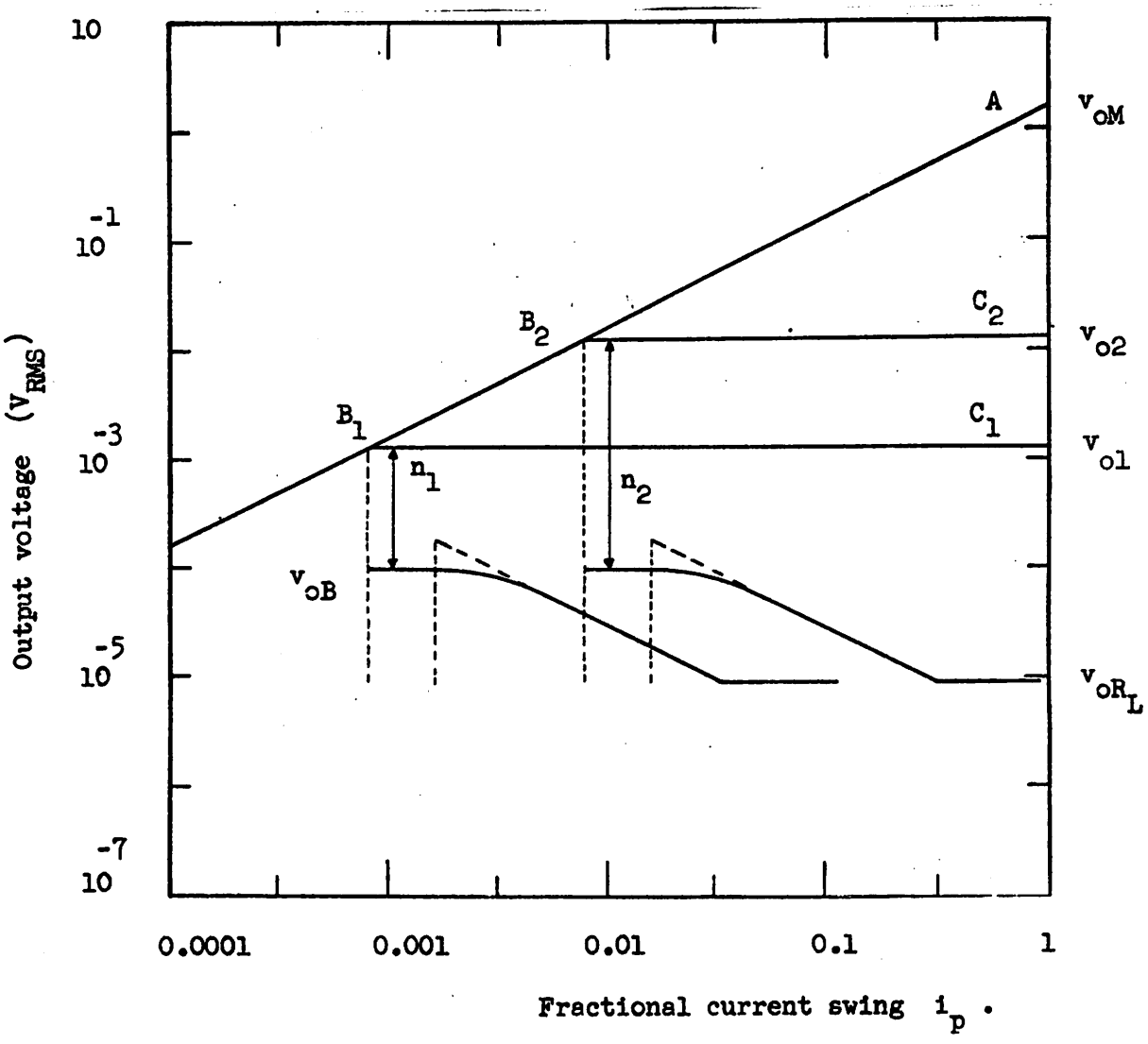


Figure 5.3.

Output Signal Voltage v_o and Output Noise Voltage due to r_B and R_L versus Fractional Current Swing i_p for two different values of v_o . The maximum signal-to-noise ratio in each case is indicated.

For $x \geqslant 0.5$ the output noise v_{oB} is constant. Consequently, all conclusions stated for a constant noise level are still valid. For a given output signal-to-noise ratio n (n_1 in Figure 5.2), the minimum value of output signal v_{om} (v_o in Figure 5.2) is given by (5.7) with v_{oB} instead of v_{oR_L}. However, for higher values of v_o the dynamic range decreases because DR_P, given by (5.3), decreases and the signal-to-noise ratio becomes larger than n_1. As a result, the maximum dynamic range DR_M occurs at v_{om} itself. For $v_o \geqslant v_{om}$ the dynamic range DR is plotted versus v_o in Figure 5.4. In this region DR is limited by the potential dynamic range, except at $v_o = v_{om}$, where DR_M is also limited by the peak r_B noise v_{oB}.

The value of DR_M is again equal to DR_P and is thus found by replacing v_{om} by $n\, v_{oB}$ in (5.8). It is given by

$$DR_M = 20 \log_{10} \frac{V_T}{n \sqrt{2kT\, r_B\, \Delta f}} \qquad \ldots (5.13)$$

This value of DR_M is independent of I_{EE} because both v_{oM} and v_{oB} are proportional to I_{EE}. Also, DR_M is independent of R_L. For a given type of transistor, the maximum dynamic range is thus unambiguously determined by (5.13).

If the amplitude of the output signal v_o is now reduced to values below v_{om}, the dynamic range is limited again by

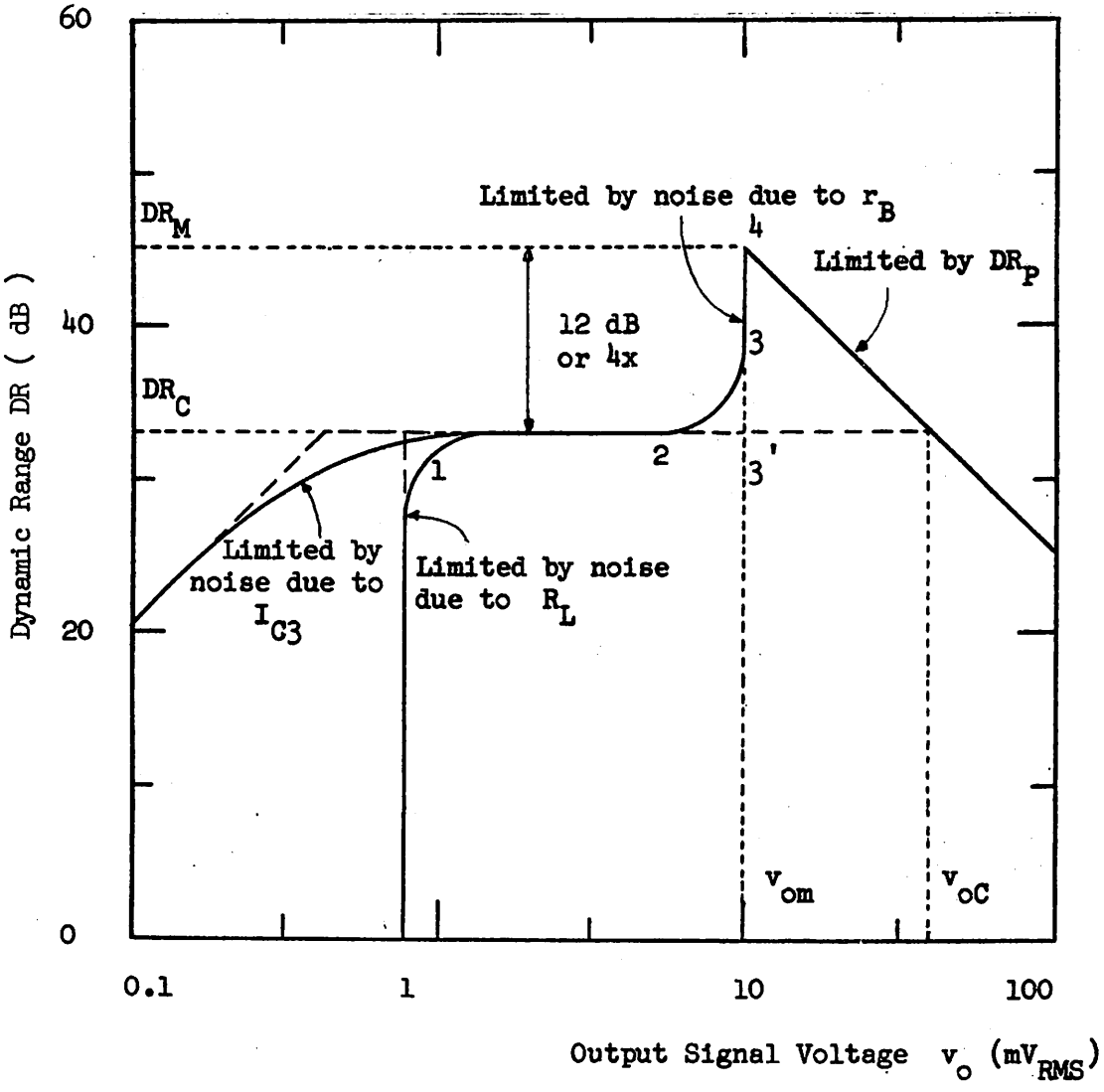


Figure 5.4.

Dynamic Range DR versus Output Signal Voltage v_o for a given Quad Current I_{EE} and Signal-to-noise Ratio n . The labels correspond with the noise levels (Figure 5.2) which limit the dynamic range. The reduction in DR due to distortion is not taken into account.

r_B noise but now this noise is dependent on i_p as given by (5.11) and (5.12). This is shown in Figure 5.2 for signal-to noise ratio n_2, which is the same as before (but v_o is lower than before). For this value of n, the conditions represented by line segment BD on line BC are thus too noisy and an amount of DRN of the potential dynamic range DR_P is lost. The value of DRN is given by the value of i_p at which the noise limit is exceeded. It is found by substitution of x out of (5.11) in (5.12), after replacing v_{or_B} by v_o/n_2, and is given by

$$DRN = 20 \log_{10} 4n_2 \frac{v_{oB}}{v_o} \quad \ldots (5.14)$$

The substitution of (5.14) and (5.3) in (5.4) yields a value of dynamic range DR_C which is independent of v_o (Figure 5.4) because both DR_P and DRN decrease with v_o. Also, DR_C is always 12 dB (factor 4) lower than DR_M given by (5.13).

If the amplitude of output signal voltage is reduced further, the dynamic range is limited by noise due to R_L or I_{C3}, whichever is higher. In Figure 5.2 noise due to R_L is assumed to be higher. For the same value of n as before, (n_3 in Figure 5.2), the minimum value of v_o that meets this specification is again given by (5.7). At this point, the curve in Figure 5.4 falls to zero because v_o cannot be reduced without changing n.

However, if noise due to I_{C3} is higher than R_L noise, v_o can be reduced still further for the same value of n (n_4 in Figure 5.2) as before. Since noise due to I_{C3} only decreases with a slope of 10 dB/decade, the dynamic range decreases with a slope of 20 dB/decade (Figure 5.4). This is found from the same expressions (5.11) and (5.12). In this region, both the values of DR and v_o have become low and thus no more attention is paid to I_{C3} noise.

From Figure 5.4, it can thus be concluded that for output voltages lower than v_{oC}, which is four times larger than v_{om}, a dynamic range of at least DR_C can be obtained. However, the maximum dynamic range is 12 dB higher and is reached at v_{om} itself. The values of DR_M at different current levels I_{EE} are plotted in Figure 5.5. For values of I_{EE} lower than I_{EBL} (4.34), R_L noise is dominant and DR_M increases with I_{EE} as given by (5.9). For high values of I_{EE}, however, r_B noise dominates and DR_M is independent of I_{EE}. Also, this value of DR_M, which is given by (5.13) is the highest value that can be obtained for the given type of transistors and a specific value of n and is therefore designated by DR_{MM}. In the above example $r_B = 100\ \Omega$ and for $\Delta f = 4.5$ MHz, the product $n\ DR_{MM}$ equals 82.5 dB. Thus, for an output signal-to-noise ratio n = 40 dB, the maximum dynamic range is 42.5 dB. The value of v_{om}, at

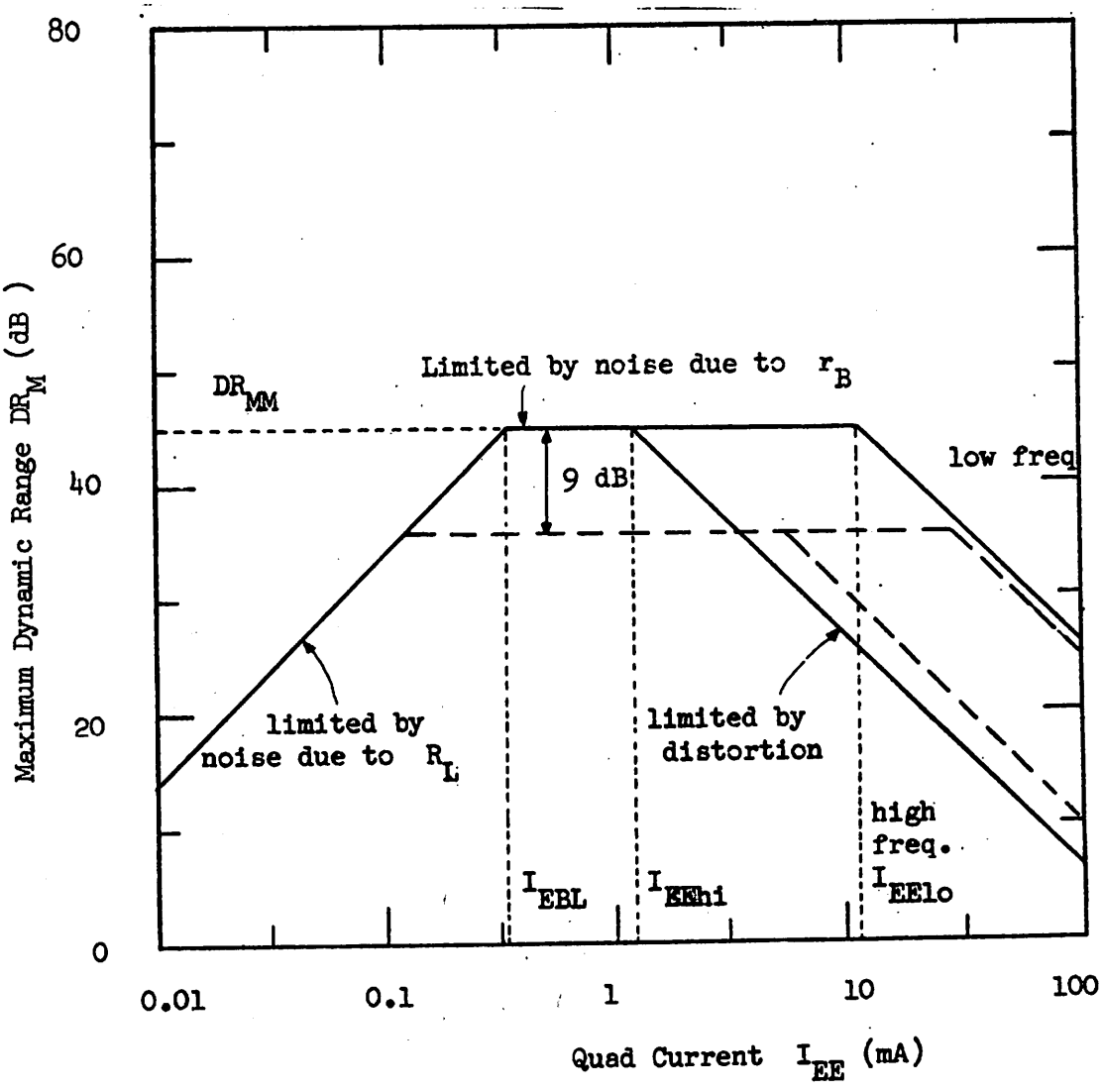


Figure 5.5.

Asymptotic values of Maximum Dynamic Range DR_M of the Agc Amplifier (——) and Gilbert's Quad (- - -) versus Quad Current I_{EE} for a given Signal-to-noise Ratio n and a given value of Collector Load R_L.

which DR_{MM} is available, does depend on I_{EE} and R_L. For example, if $R_L = 500\,\Omega$ and $I_{EE} = 4$ mA, the maximum noise due to r_B is given by (5.10) and equals $v_{oB} = 0.105\ mV_{RMS}$; and thus for $n = 100$, $v_{om} = 10.5\ mV_{RMS}$.

For high values of I_{EE}, the optimum output voltage v_{om} becomes large, but distortion begins to limit the dynamic range as given by (5.5). This is also shown in Figure 5.5. The optimum value of I_{EE} is thus obtained at the edge of the noise limited region, which is designated by I_{EElo} at low frequencies. This value of I_{EE} is found from (5.5) by equating DRD to 3 dB. For example, I_{EElo} equals 12 mA for $d = 0.01$ (1% IM_3) and $r_B/\beta = 1\,\Omega$.

At high frequencies, the reduction in dynamic range due to distortion DRD increases. Comparison of (2-38) and (3-9) suggests an increment of $20 \log_{10} \frac{f}{f_\beta}$ to (5.5) which results in a reduction of either the resultant dynamic range DR_M or the optimum value of I_{EE} by the same amount (see Figure 5.5). For example, if $f_\beta = 6$ MHz, DR_M decreases by 20 dB at 60 MHz, but the DR_M of 42.5 dB can be maintained if the quad current becomes $I_{EE\,hi} = 0.1\ I_{EElo}$ or 1.2 mA.

In a first-order analysis, the noise output at high frequencies remains constant over the frequency range of interest. Therefore, the reduction in dynamic range due to noise is not changed for high frequencies.

Finally, the small-signal bandwidth over which the agc quad maintains its dynamic range is examined. At high gain (point B in Figure 5.1) the output transistors behave as current driven common base stages at currents close to $I_{EE}/2$. The cut-off frequency is thus about f_T . However, under maximum attenuation conditions, the output transistors exhibit a capacitive input impedance consisting mainly of their junction capacitances C_{jE} and C_{jC} . They are driven however by a current source shunted by the inductive input impedances of the other pair transistors. Peaking can thus occur. In the limit at very high frequencies, the input resistance approaches r_B and the upper limit of the dominant time constant is given by

$$\tau_i = r_B (C_{jE} + C_{jC}) \quad . \qquad \ldots (5.15)$$

The bandwidth is also limited by the output time constant

$$\tau_o = R_L C_{CS} \quad . \qquad \ldots (5.16)$$

The higher value of (5.15) and (5.16) thus determines the bandwidth of the quad. For a given dynamic range, however, this bandwidth can be severely reduced by direct signal feedthrough, as indicated in Chapter 3.

5.3 OPTIMUM DYNAMIC RANGE OF THE MULTIPLIER

For dynamic range considerations, the multiplier behaves very much in the same way as the agc amplifier. The dynamic range is limited by distortion when the attenuation is high. As given by (2.50), the maximum distortion is found to be only

one third of the maximum distortion exhibited by the agc amplifier. If the reduction in dynamic range due to distortion DRD for the agc amplifier is larger than 2.4 dB, the value of DRD for the multiplier is thus 2.4 dB less. Otherwise, the dynamic range of the multiplier is not limited by distortion. In the above example, DRD = 1.4 dB for the agc amplifier and zero for the multiplier if d = 1% ; however, if d = 0.1% , these numbers become 11.4 dB and 9.0 dB.

The dynamic range of the multiplier is also limited by noise, which is due mainly to the base resistances r_B and the collector loads R_L . It is assumed that the r_B noise versus attenuation (Figure 4.7) is constant and given by its maximum value. This holds true only if the dynamic range is higher than about 20 dB. The constant noise level is thus given by v_{oB} in (5.10) or v_{oR_L} in (5.6), whichever is larger. The maximum dynamic range DR_M is then obtained for an output signal voltage v_{om} , which is n times higher than the maximum noise level. The value of DR_M is given by (5.8). The dynamic range of both the multiplier and the agc amplifier are thus limited by noise in exactly the same way. In the example, the dynamic range of the multiplier is thus 1.4 dB larger than for the agc amplifier, because the multiplier has lower distortion.

The dynamic range of the multiplier, however, is most severely limited by the high distortion due to mismatch (Section

2-8). It is thus quite possible that, instead of reducing DRD , a significant increase in DRD is obtained. The agc amplifier is thus definitely superior to the multiplier if low distortion is required over a large dynamic range. The multiplier nevertheless exhibits a unique property, which makes it quite attractivefor use in dc-coupled circuitry. Its dc output level is constant and independent of the ac gain of the circuit. This is not true for the agc amplifier and Gilbert's quad, which thus require a differential output amplifier to achieve this property.

The multiplier is also superior to the agc amplifier with respect to the small-signal frequency response. At high gain, both circuits have the same wide bandwidth. At low gain, the bandwidth of the agc amplifier has decreased significantly, whereas for the multiplier, the bandwidth is about the same as at high gain, because the dc current is still one half of its value under high gain conditions.

5.4 OPTIMUM DYNAMIC RANGE OF GILBERT'S VARIABLE-GAIN QUAD

The dynamic range of Gilbert's quad shown in Figure 2.13 is optimized in a similar way as for the agc amplifier. The distortion and the noise characteristics versus attenuation have the same shape as the curves for the agc amplifier.

Again it is assumed that quad current I_{EE}, which is the sum of pair currents I_{E1} and I_{E2}, is constant. The circuit gain A_v is then controlled by the ratio k of current I_{E2} to I_{E1}, as it is shown in Figure 2.14.

For a given output voltage v_o, the values of the maximum output voltage v_{oM} and the potential dynamic range DR_P are the same as for the agc amplifier and are thus given by (5.1) and (5.3) respectively. As shown in Figure 2.15, the maximum distortion is encountered at both high attenuation and also at high gain. Under high gain conditions, however, the noise output voltage is maximum also (Figure 4.10) such that the reduction in dynamic range due to noise (DNR) will probably mask the reduction in dynamic range due to distortion(DND). This may not be true at high frequencies where DRD increases without an increase in DRN. In this analysis, however, it is assumed that noise only limits the dynamic range at low attenuation and distortion at high attenuation.

The maximum IM_3 distortion at low frequencies is given by (2.54). For a given upper limit in distortion d, the reduction in dynamic range due to distortion DRD is then given by

$$DRD = 20 \log_{10} \sqrt{\frac{3}{8d}} \sqrt{\frac{r_B I_{EE}}{2\beta V_T}} \qquad \ldots (5.17)$$

which is usually larger than the value of DRD for the agc amplifier, which is given by (5.5). In the above example, DRD equals 8.6 dB for 1% IM_3 and 18.6 dB for 0.1% IM_3.

As for the two other quads, the noise output of Gilbert's quad consists mainly of noise due to the four quad base resistances r_B and the two collector loads R_L. Using the output noise characteristic of Figure 4.10, the graph of dynamic range DR versus output voltage v_o is obtained using exactly the same procedure as for the agc amplifier and is represented in Figure 5.6. For purposes of comparison, the DR-v_o characteristic of the agc amplifier which is given in Figure 5.3, is also represented in Figure 5.6.

For high values of output voltage v_o, the dynamic range DR of the both circuits is limited by the potential dynamic range DR_P and is thus the same. At v_{om} the DR is also limited by the maximum r_B noise. Since for Gilbert's quad the maximum r_B noise voltage is 9 dB higher, the value of v_o at which this noise level is reached is thus $2\sqrt{2}$ times higher than v_{om} and is designated by v_{omG}. For lower values of v_o, the potential dynamic range DR_P decreases at the same rate as the reduction in dynamic range due to noise DRN decreases and thus the resultant DR remains constant. However, DR for the agc amplifier is 3 dB higher than for Gilbert's quad. If v_o is reduced further, noise due to R_L makes the realization of signal-to-noise ratio n impossible and DR goes to zero. It can thus be concluded that for the same values of I_{EE}, r_B and n, the maximum dynamic range DR_M in Gilbert's quad is 9 dB lower than in the

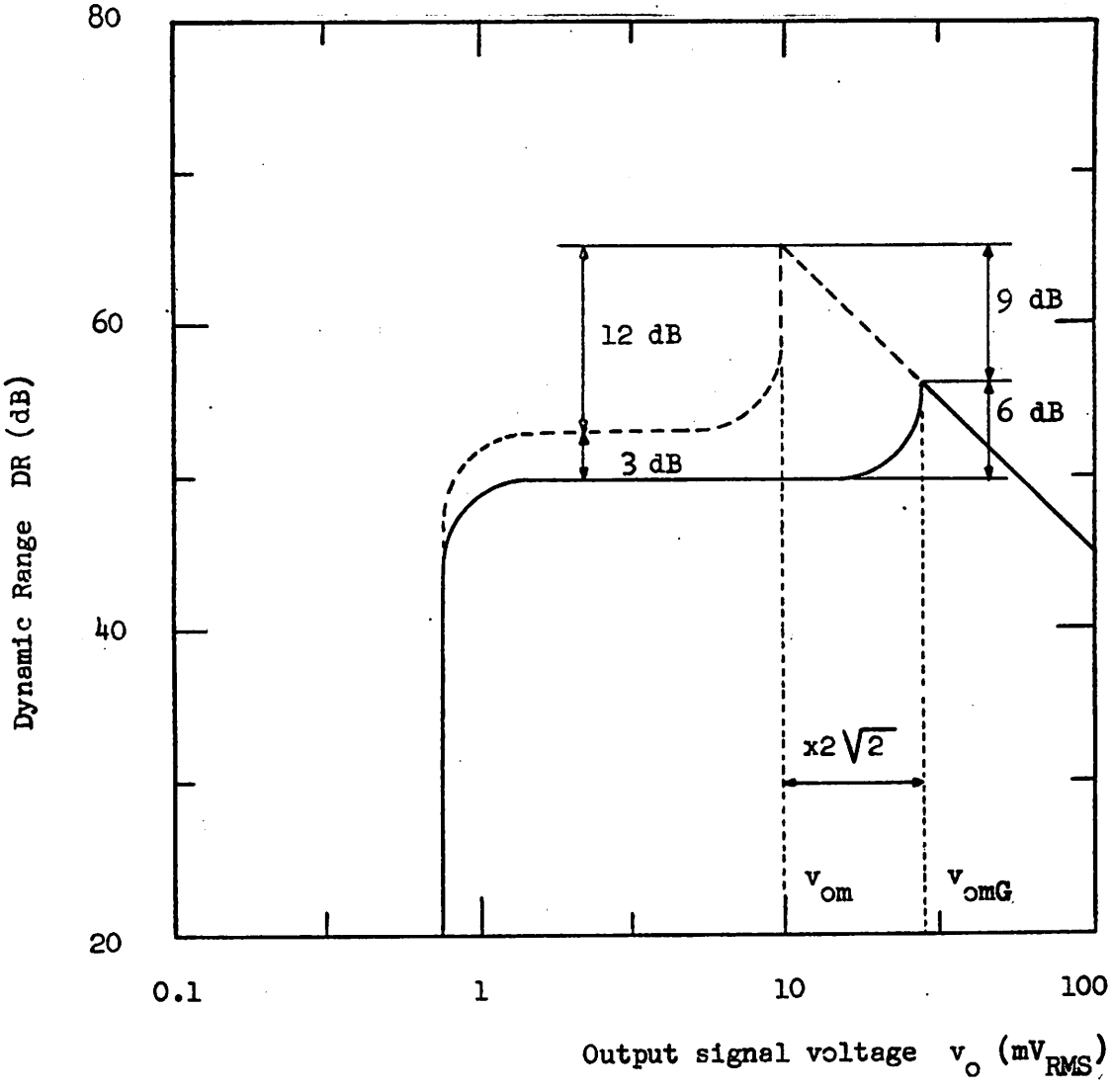


Figure 5.6.

Dynamic Range DR versus Output Signal Voltage v_o for the Agc Amplifier (- - -) and Gilbert's Quad (——).

agc amplifier. Also, it occurs at v_{omG} which is $2\sqrt{2}$ times higher than v_{om}.

As for the agc amplifier, the maximum dynamic range DR_M of Gilbert's quad is independent of I_{EE} and R_L (Figure 5.5). At low values of I_{EE} however, the value of DR_M decreases because R_L noise becomes important at a value of $I_E = I_{EBL}/2\sqrt{2}$. At values of I_{EE} above I_{EElo}, distortion reduces DR_M. The value I_{EElo} is obtained from (5.17) by equating DRD to 3 dB. For the data of the example I_{EElo} = 25 mA. For this example, the DR_M of the agc quad is thus always higher than for Gilbert's quad.

At high frequencies, the distortion generated by Gilbert's quad increases with frequency, but at a lower rate than in the agc amplifier. Since at low frequencies the distortion in Gilbert's quad is higher than in the agc amplifier, there exists a cross-over frequency above which Gilbert's quad presents less distortion. However, this cross-over point may be masked by signal feedthrough which is more severe in Gilbert's quad (Section 3.5).

The small-signal bandwidth of Gilbert's quad under high-attenuation conditions is determined by the frequency response of the output transistors Q_5 and Q_6 in Figure 2.13. The collector current in these transistors is low and their input impedance consists mainly of junction capacitances C_{jE} and C_{jC}.

The dominant time constant is then given by

$$\tau_i \quad (\frac{1}{2}\ \frac{V_T}{I_{EE}} + r_B)\ (C_{jE} + C_{jC}) \qquad \ldots (5.18)$$

where r_B, C_{jE} and C_{jC} all refer to the output transistors. Under high-gain conditions, the collector current in the input transistors is low and the -3 dB frequency of the output pair is only f_β. The maximum bandwidth for the quad is obtained when pair currents I_{E1} and I_{E2} are comparable in magnitude. The -3 dB frequency is then given by

$$f_o = (\frac{I_{E1}}{I_{E2}} + \frac{r_B I_{E1}}{V_T})\ f_T \qquad \ldots (5.19)$$

which can be quite close to f_T itself. As for both other quads however, the output time constant given by (5.16) may be dominant.

5.5 THE CHOICE OF QUAD CURRENT I_{EE}.

For a given type of transistor, only the values of R_L and I_{EE} affect the optimum performance of a quad. The required bandwidth determines the value of R_L so that I_{EE} is the only design parameter.

As it is shown in Sections 5.2 and 5.3, the maximum dynamic range is obtained for a whole range of values of I_{EE} and output voltage v_o. However, signal feedthrough limits the dynamic range that can be reached at high frequencies. Also,

when I_{EE} is low at high frequencies, the distortion in the quad is no longer due only to base resistance r_B but rather to junction capacitance C_{jE} and my tend to cancel at a specific value of I_{EE}. Very low values of I_{EE} also reduce the small-signal bandwidth. On the other hand, high values of I_{EE} cause peaking in the transfer characteristic. The choice of the value of I_{EE} thus depends on many factors which are now described in more detail.

At high frequencies and for low value of I_{EE}, the distortion due to base resistance becomes small compared with the distortion caused by junction capacitance C_{jE}. Comparison of (3.9) and (3.15) shows that both amounts of third-order distortion are equal at the value of I_{EE} given by

$$I_{EJ} = \sqrt{2g}\,\frac{V_T}{r_B} \qquad \ldots (5.20)$$

at frequency f_T/g for $g \geq 3$. Actually, since these types of distortion have opposite polarity, they cancel at current I_{EJ}. This null is sharp however, and disappears at higher frequencies due to changing phase conditions. Using values of I_{EE} higher than I_{EJ} and taking into account only the distortion due to r_B will give a worst-case result. As an example, take $g = 3$; (5.20) gives $I_{EJ} = 0.8$ mA for $r_B = 80\,\Omega$.

When the quad is biased at the current I_{EE} given by [8]

$$I_{EG} = \frac{2\,V_T}{r_B} \qquad \ldots (5.21)$$

then the pairs present resistive input impedances (with value r_B) to the signal currents. The transfer characteristic versus frequency is thus flat with frequency to f_T, which then equals the frequency given by (5.15). For values of I_{EE} which are much higher than I_{EG}, the current carrying transistors have an inductive input impedance and the transfer characteristic exhibits peaking. This is illustrated in Figure 5.7 for an agc amplifier using CA 3045 as quad transistors. The input transistors Q_1 and Q_2 (Figure 2.8) are high frequency transistors with large emitter resistors R_E in order to isolate the performance of the quad from that of the input pair. The curves are taken for constant control voltage V_B. For a high value of I_{EE}, peaking occurs (Figure 5.7.a) which is not present for low I_{EE} (Figure 5.7.b). However, the direct signal feedthrough, which to a first-order is independent of the amplitude of the ac input current, limits the dynamic range more at the low current than at the high current. This reduction is mainly due to the difference in the value of r_B for these two currents and the second-order effects indicated in Section 3.4. If values of I_{EE} higher than I_{EG} are selected, parasitic capacitances such as collector-substrate capacitance C_{CS} and and the input capacitance of the following output amplifier always compensate the resultant peaking to some extent. Note that the value of I_{EG}, which equals 0.65 mA for $r_B = 80\,\Omega$, is always smaller than the value of I_{EJ}.

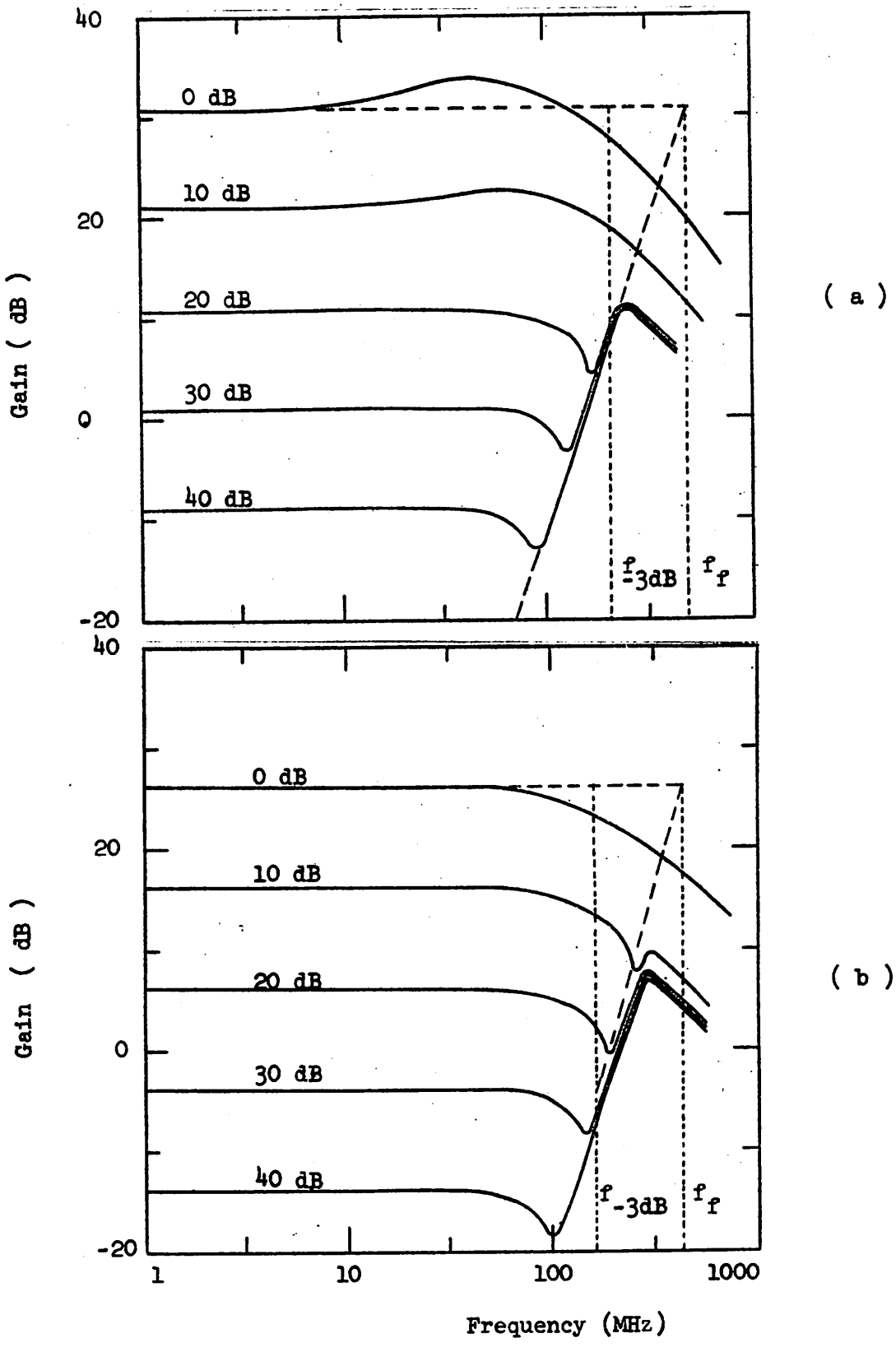


Figure 5.7.

Attenuation versus Frequency for the Agc Amplifier (Appendix B.2) at (a) $I_{EE} = 10\ I_{EG}$ and (b) $I_{EE} = I_{EG}$.

For the agc amplifier, a lower limit to the value of I_{EE} is thus provided by I_{EBL} and I_{EJ}. An upper limit is reached when base resistance distortion starts reducing the dynamic range (I_{EEhi} in Figure 5.5) and when peaking becomes too great to be compensated by parasitic capacitances.

5.6 THE INPUT VOLTAGE-CURRENT CONVERSION

Both the agc amplifier and the multiplier employ an input pair with emitter-degeneration in order to convert the input signal voltage to a differential current drive. Gilbert's quad also uses this voltage-current conversion but the current in the pair is not necessarily constant. For a given type of transistor, the pair current I_P and resistances R_E completely characterize the performance of the input pair. In order not to degrade the dynamic range of the quad over any portion of the bandwidth, the values of I_P and R_E have to satisfy certain conditions which are now investigated.

The input pair is actually a base-driven pair with degeneration resistors R_E. At low frequencies the feedback caused by R_E reduces the distortion as given by (2.29). However, since the distortion in the input pair and the quad have opposite polarity, distortion cancellation can occur. If the current in the pair is the same as in the quad ($I_P = I_{EE}$), the conditions for the values of I_P and R_E are found by comparison of (2.29)

with (2.38). For the transistor parameters of the above example and $I_P = 8$ mA, the distortion nulls for $R_E \simeq 40\,\Omega$. Since this null is very sharp, and also disappears at high frequencies, it is not of great practical use. Therefore, the currents I_{EE} and I_P are selected independently. This is a significant deviation from the usual biasing of differential pairs. In Chapter 6 a biasing technique is described that allows a different current in the quad from that in the input pair. The performance of the quad can then be optimized without interfering with the optimum current level in the input pair. The values of I_P and I_{EE} are selected such that the maximum distortion d is not exceeded in the quad or the input pair independently. For the above example, it is found from (2.38) that I_{EE} has to be lower than 10.6 mA to limit the low frequency distortion to 1% IM_3 ($i_p = 1$). Since the fractional current swing in the pair is then given by $i_p = I_{EE}/I_P$ (if $I_{EE} < I_P$), it is found from (2.38) and (2.29) that I_P has to be larger than I_{PE} given by

$$I_{PE} = V_T \left(\frac{16\,\beta^2}{3R_E r_B^2}\right)^{1/3}, \qquad \ldots (5.22)$$

which equals 12 mA for $R_E = 70\,\Omega$. Note that I_{PE} is independent of d because I_{EE} and thus also the current swing in the pair both decrease with smaller values of maximum distortion d.

The output noise of the quad is mainly due to base resistances r_{B1} and r_{B2} and is maximum when the currents in all quad transistors

are equal. In Section 5.2 and Section 5.3, the dynamic range has been optimized for this source of noise. The output noise which is contributed by the input pair will not affect the above analysis as long as the noise generated in the quad is dominant. This holds true if I_{EE} is larger than I_{EN}, given by

$$I_{EN} = \left(\frac{2}{I_P} + \frac{R_E}{V_T}\right)^{-1} \sqrt{\frac{r_{B3} + R_E}{r_{B1} + r_{B2}}} \qquad \ldots (5.23)$$

where r_{B3} is the base resistance of the input pair transistors. Source resistances are included in the corresponding base resistances. For $I_P = 2.8$ mA, $R_E = 70\,\Omega$, $r_{B1,3} = 80\,\Omega$ and $r_{B2} = 120\,\Omega$, (5.23) yields $I_{EN} = 0.26$ mA. Since the value of R_E is usually smaller than any of the base resistances, (5.23) gives as worst-case-value $I_{EN} = V_T/R_E$ which equals 0.37 mA in this example. The value of I_{EN} thus establishes another lower limit to the value of I_{EE} or an upper limit to the value of I_P.

For high emitter degeneration ($I_P R_E > 2\,V_T$), the -3 dB frequency of the input pair transfer characteristic is controlled by the time constant

$$\tau_p = (R_S/2 + r_{B3})\,\frac{\tau_3 + C_{\mu 3} R_C}{R_E} \qquad \ldots (5.24)$$

where τ_3 is the base transit time and $C_{\mu 3}$ the collector-base capacitance of the pair transistors; R_C represents the load of the input pair and R_S its total source resistance. Expression (5.24) is valid if the pair current I_P is higher than I_{PC}, given by

$$I_{PC} = \frac{2\,V_T\,C_{jE3}}{\tau_3 + C_{\mu 3} R_C} \qquad \ldots (5.25)$$

where C_{jE} is the emitter-base junction capacitance of the pair transistors. Since the voltage gain of the total circuit is proportional to R_L/R_E, the gain-bandwidth product is independent of the current level. As a consequence, gain can be exchanged for bandwidth by selecting the value of R_E. At current levels below I_{PC} the cut-off frequency drops with a slope of 20 dB/dec. For very low I_P, as in Gilbert's quad under high gain conditions, R_E no longer produces broadbanding. The dominant time constant for the input pair is then approximately given by

$$\tau_{pj} = (R_S/2 + r_{B3})(C_{jE3} + C_{\mu 3}) \qquad \ldots (5.25)$$

which may considerably degrade the bandwidth of Gilbert's pair. For best performance, (5.25) thus establishes a lower limit to the value of I_P. As an example, take $\tau_3 = 0.3$ ns, $C_{jE3} = 4$ pF. The worst-case value for R_C is assumed to be zero. The widest bandwidth is then obtained for I_P larger than 0.69 mA.

5.7 THE IMPROVED AGC AMPLIFIER.

The above analysis has shown that for optimum performance the bias current for the quad itself has to be lower than that for the input pair. Indeed, the distortion in the quad due to base resistance is reduced by decreasing the current levels, whereas the distortion performance of the input pair improves by increasing its bias current. Also, a smaller value of emitter resistance can then be used to maintain a high value of voltage gain.

The same trade-off exists for noise and bandwidth considerations. The current level in the input pair can only be increased as long as its noise does not become comparable in magnitude to the noise of the quad. However, the bandwidth of the input pair significantly improves for high current levels, whereas lower currents cause less peaking in the transfer characteristic.

The aim of this study is to achieve a maximum product of bandwidth with dynamic range. For that purpose, the agc amplifier is selected among the quads discussed above. It has been shown that the optimum dynamic range over its total bandwidth can be obtained provided the input current source is biased at a high current level. The agc amplifier built in this way is called the improved agc amplifier and is shown in Figure 5.8. The resistances R_B carry current I_Q, which is the difference between the pair current I_P and the quad current I_{EE}. The biasing scheme is such that resistance R_B is always much larger than the input impedance of $Q_3(Q_5)$ or $Q_4(Q_6)$. The voltage gain is then approximately given by

$$A_v = \frac{R_L}{R_E} \qquad \ldots (5.27)$$

if $R_E I_P > 2 V_T$. The value of R_L is limited by the output time constant given by (5.16). However, an output amplifier is used with very low input impedance. Its transresistance is 700 Ω and its configuration is given in Appendix C. Thus capacitance C_{CS} is no longer the dominant bandwidth limitation. In order to achieve a voltage gain of 15 to 20 dB, the value of R_E is obtained from

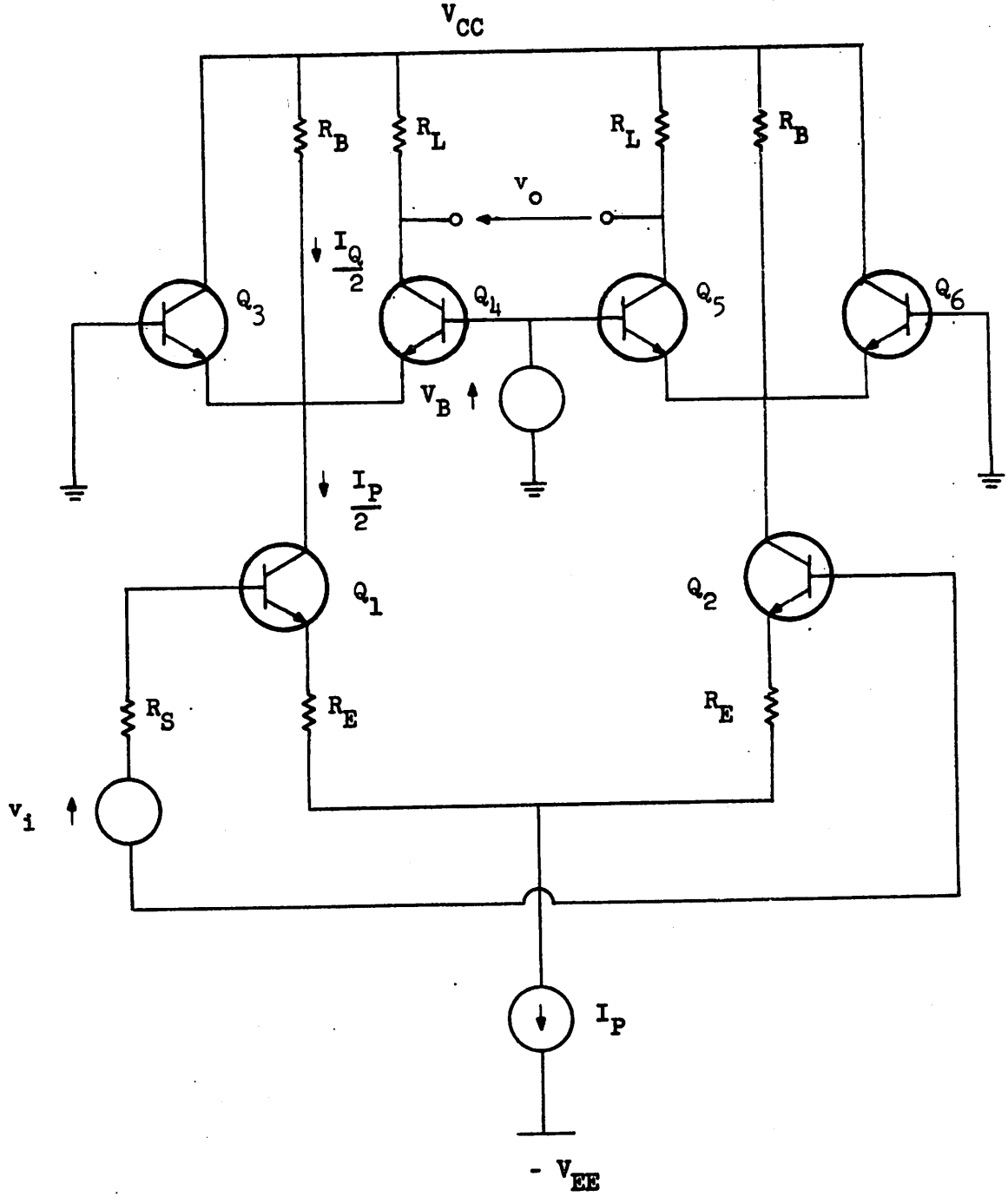


Figure 5.8.

Improved AGC Amplifier with $I_P = I_{EE} + I_Q$.

(5.27). For $R_L = 700\,\Omega$, (5.27) yields $R_E = 70\,\Omega$ for $A_v \simeq 10$ or 20 dB. For the amplifier of Figure 5.8, the values of the pair current I_P, the quad current I_{EE} and the output voltage v_o have to be found so that the product of dynamic range DR and bandwidth is maximum. The maximum allowable distortion over the whole bandwidth is 1% IM_3 and the signal-to-noise ratio n should be at least 40 dB for $\Delta f = 4.5$ MHz under all circumstances.

The improved agc amplifier has been realized with discrete components (CA 3045) and in integrated form (process P1 and P2). The values of the transistor parameters, which are used in the selection of I_{EE} and I_P, and which are obtained by the procedures given in Chapter 6, are listed in Table 5.1. The parameters which have been used for the example throughout this Chapter are included. For each type of transistor, the maximum dynamic range is calculated and also all current values that are pertinent to the choice of I_{EE} and I_P.

Since transistors with single (1B) and double (2B) base strings are used, two different values of r_B are listed. For noise calculations, their average is taken. Since $n = 100$, the maximum dynamic range that can ever be obtained is 43.6 dB for P1. At low frequencies, any value of I_{EE} between 0.37 mA and 2.9 mA allows that maximum to be achieved. For instance, if $I_{EE} = 1$ mA, the value of v_{om} is given by $\frac{100 \times 1}{42.4} = 2.35$ mV. However, at high frequencies (70 MHz) this maximum dynamic range of 43.6 can only be achieved if $I_{EE} < 0.4$ mA and thus 0.4 mA

			P1	P2	CA 3045	Example
r_{Blo}	(2B)		65	580	180	80
r_{Bhi}	(1B)		105	710	180	120
r_{Bno}	$\frac{1}{2}(r_{Blo}+r_{Bhi})$		85	645	180	100
f_T	at high I_C	MHz	210	620	400	530
C_{CS}	at -5 V	pF	3.1	3	3	3
C_μ	at -5 V	pF	2.1	2.2	1.5	0.7
C_{jE}		pF	8	7	5	4
β			22	800	100	100
n. DR_{MM}	(5.13)	dB	83.6	74.5	80	82.6
I_{EElo}	(5.5)	mA	2.9	11.8	4.75	10.6
$I_{EEhi}(f_T/3)$		mA	0.40	0.044	0.14	0.30
n I_{EE}/v_{om}	(5.10)	S	42.4	14.2	25.5	38
I_{EBL}	(4.34)	mA	0.37	0.13	0.245	0.33
$f_f(\lvert AR_P\rvert = 1)$	(3.30)	MHz	430	144	350	850
I_{EG}	(5.21)	mA	0.80	0.09	0.29	0.65
$I_{EJ}(g=3)$	(5.20)	mA	0.98	1.10	0.35	0.80
I_{PC}	(5.25)	mA	0.60	1.42	0.65	0.69
I_{PE}	(5.22)	mA	21.5	13.6	7.5	12.8

Table 5.1.

The values of Quad Current I_{EE} and Input Pair Current I_P which are instrumental in the choice of I_{EE} and I_P for the Improved Variable-gain Amplifier.

seems to be the best choice for I_{EE}. This dynamic range is not yet limited by feedthrough since at 70 MHz 48 dB attenuation can be obtained (the dynamic range is zero dB at 430 MHz but increases at a rate of 60 dB/decade). For I_{EE} = 0.4 mA, the bandwidth of the quad is rather low. A value of 0.8 mA or higher would be better. Also, at 0.4 mA, distortion due to junction capacitance is dominant and may reduce resultant dynamic range. A value of 0.98 mA or higher is suggested. Choosing 1 mA solves both latter problems but 42.5 dB dynamic range will be available only up to 70/2.5 = 28 MHz and the optimum output voltage is now 5.9 mV. If the bandwidth of 70 MHz is required, only 34.5 dB dynamic range is obtained.

For the input pair, four times 0.6 mA will provide a wide bandwidth. Since this is larger than 0.37 mA, given by (5.23), the noise from the input pair is negligible. However, in order to reduce the distortion in the input pair to less than 1%, the value of I_P has to be at least 21.5 mA. This value can be lowered by increasing R_E.

Experimentally (P1), the maximum dynamic range was found to be 33 dB at 70 MHz (Δf = 4.5 MHz), which occurred at output signal v_{om} = 3.5 mV_{RMS}. The current levels were I_{EE} = 1 mA and I_P = 6 mA. The deviation of v_{om} from the predicted value can be explained by noting that the output noise is reduced

at high frequencies and thus also v_{om}. However, the corresponding increase in dynamic range is partially cancelled by the relatively large amount of distortion generated in the input pair. Therefore the value of resultant dynamic range is close to the predicted one.

Whereas the value of v_{om} is experimentally easy to determine (n times maximum noise level), the value of I_{EE} for optimum dynamic range is much more cumbersome to find. Fortunately, experiments have shown that the optimum value of I_{EE} is less critical than it is suggested by the calculated values given in Table 5.1. The maximum dynamic range of 35 dB, obtained at I_{EE} = 1 mA, decreased by 3 dB at the current values I_{EE} = 0.4 mA and 1.5 mA. As a consequence, an acceptable value of I_{EE} can be estimated directly from Table 5.1 and need not be further refined by experiments.

The -3 dB frequency at full gain is limited by the frequency response of the input pair. Although (5.24) yields only 90 MHz, the experimental (P1) value was approximately 120 MHz. This discrepancy is probably due to inaccurate knowledge of the values of f_T and r_B for which average values have been used. At 120 MHz, the feedthrough line (Figure 5.7) was reached at 32 dB attenuation. Thus frequency f_f = 410 MHz, which compares favorably with the predicted value of 430 MHz.

The performance of the circuits of processes P1 and P2 are compared under the same conditions of quad current I_{EE} (1 mA) and frequency (70 MHz). The total pair current I_P however, equals 4.5 mA for P2. The maximum dynamic range was then obtained at 11 mV_{RMS} output signal and was only 27 dB. This is much less than for process P1, because the base resistance is much higher. However, the value of f_T is also higher such that this difference is somewhat compensated.

The -3 dB frequency was 160 MHz. This is more than P1 because of the higher values of f_T and R_E in the input pair. Approximately 1 dB peaking was found under high gain conditions, which is due to the relatively high quad current I_{EE} (Figure 5.7). Frequency f_f was found to be 380 MHz, which is much higher than the value given in Table 5.1. This is probably due to the over-estimation of base resistances. This would also explain why the dynamic range for process P2 is not very much lower than for P1 as suggested by the ratio of the base resistances in Table 5.1.

Finally, the improved agc amplifier has been realized using a matched transistor quad CA 3045. The main purpose of this circuit was to study the small-signal frequency response and the signal feedthrough. Since a high frequency transistor pair (2N 3423) has been used for the input stage, the dominant time constant is caused by the f_T of the output transistors. In this way, a bandwidth of 220 MHz has been achieved, which is

more than $f_T/2$ of that device.

Although feedthrough is affected by several transistor parameters (see (3.30)), it is mainly determined by the base resistances and the total collector-base capacitance. For discrete devices, a considerable amount of parasitic capacitance is included which affects the feedthrough quite significantly. This is illustrated by comparison of f_f obtained with CA 3045 and f_f obtained in the example (Table 5.1). A low value of C_μ leads to a high value of frequency f_f and thus to a high dynamic range at high frequencies.

Finally, it is interesting to compare the performance of the improved agc amplifier and the agc amplifier with equal total currents. In the agc amplifier, the quad current I_{EE} equals the pair current I_P so that noise and distortion are greatly enhanced. For process P1, the worst case reduction in dynamic range that can occur is then 15.5 dB due to distortion and 15.5 dB due to noise. The actual reduction depends on the specifications of maximum distortion and output signal-to-noise ratio. For P1 and $d = 1\%$ and $n = 40$ dB, the dynamic range decreases by approximately 21 dB, which is quite significant. Of this amount, 12 dB is due to noise and 9 dB due to distortion. At low frequencies, the decrease is only 17 dB, but is entirely due to noise.

CHAPTER 6.

THE INTEGRATED-CIRCUIT REALIZATION OF THE IMPROVED VARIABLE-GAIN AMPLIFIER.

6.1 INTRODUCTION

The improved variable-gain quad is implemented in an integrated circuit fabricated using regular six-mask processing. Two types of npn transistor are used in the signal path. The first is a small-size transistor and is designed to keep signal-feedthrough as low as possible. The other transistor has a multiple-base stripe for the purpose of low circuit noise and distortion. One lateral pnp transistor is used for biasing.

The improved agc amplifier is embedded in a dc feedback loop which allows the adjustment of the current level in the signal transistors. Since performance is closely related to this current level, it is thus possible to bias the circuit for optimum performance in any type of application. Precautions are taken to avoid voltage supply feedthrough when the output signal level is low. Gain variation with temperature has been minimized to a first order.

Due to the importance of base resistance in determining the distortion, noise and frequency performance of variable-gain amplifiers, considerable effort was made to characterize base resistance in bipolar transistors. The circle-diagram method has been found to be the most suitable technique to estimate base resistance as a function of collector current. Also, a new technique has evolved, called the phase-cancellation

method, which gives an estimate of base resistance from one single measurement.

The parasitic capacitance of package and aluminum paths must be accounted for in the determination of the common-emitter unity-gain frequency f_T and the junction capacitances. This was accomplished by calibrating the measurement equipment by means of an identical integrated transistor with closed contact windows.

6.2 TRANSISTOR DESIGN

The ac part of the improved agc amplifier contains two types of npn transistors with specific requirements. The output transistors Q_4 and Q_5 (Figure 5.8) have minimum size in order to keep the collector junction capacitances small. On the other hand, the collector series resistances also have to be restricted to low values in order to reduce the loss in gain by voltage division with the load R_L. For a minimum linewidth $l_u = 10\ \mu$ the layout chosen for this type of transistor is shown in Figure 6.1.a. The junction depths and resistivities for two different processing procedures P1 and P2 are given in Table 6.1. The resistivity of the epitaxial layer is chosen for best trade-off between collector-base and collector-substrate capacitance, collector series resistance and collector-base breakdown voltage [19]. The thickness of the epitaxial layer x_{EPI} is determined by the

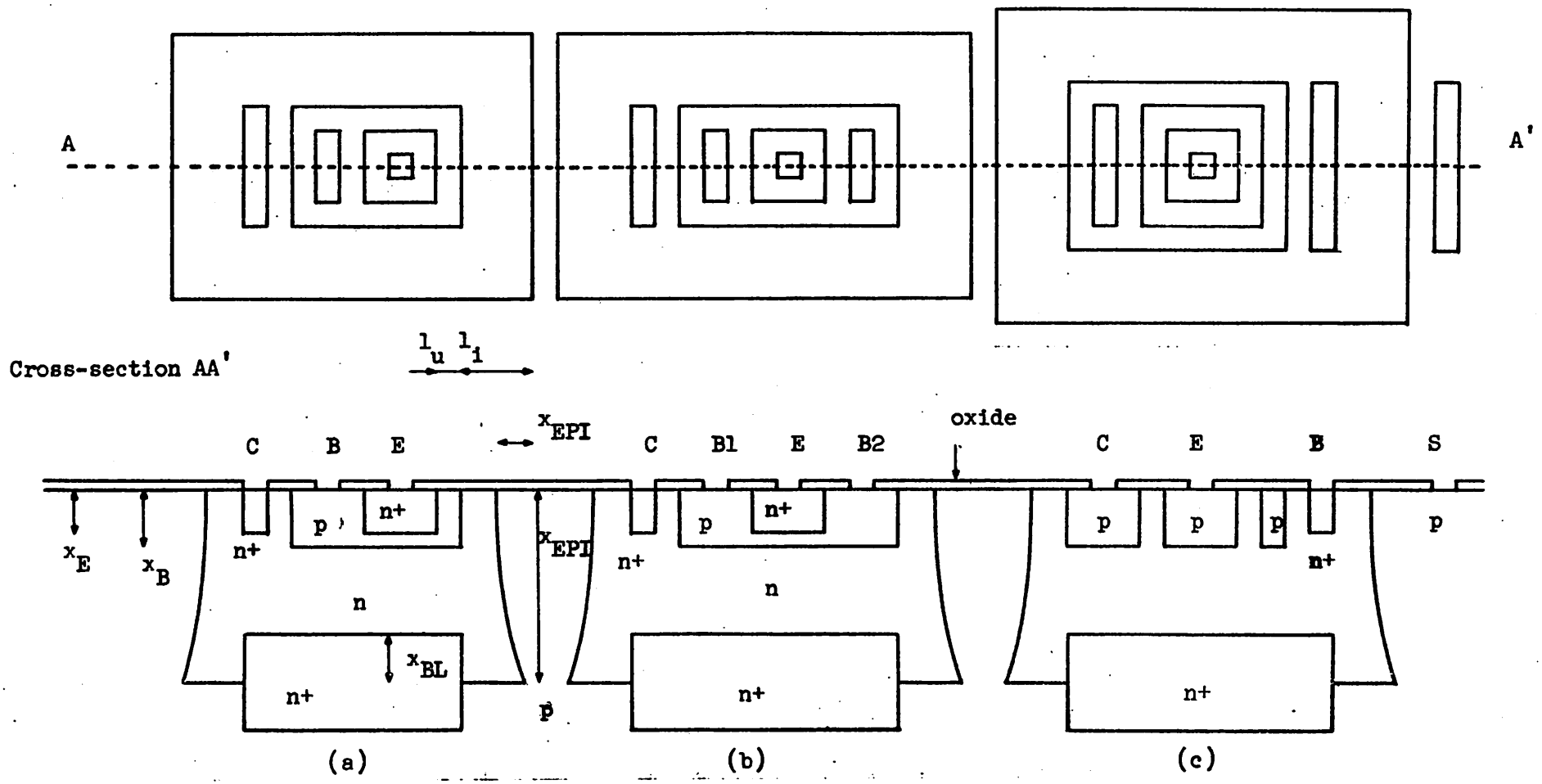


Figure 6.1.

Surface geometry and cross-section of integrated-circuit transistors : (a) small-size npn (B1); (b) double-base npn (B2); (c) lateral pnp. Minimum line width $l_u = 10$; isolation distance $l_i = 30$.

		P1	P2
ρ_{SUB}	Ω cm	8	10
ρ_{EPI}	Ω cm	1	1
ρ_{BL}	Ω/sq	8	12
ρ_{B}	Ω/sq	70	135
ρ_{E}	Ω/sq	2	2.2
x_{SUB}	μ	250	250
x_{EPI}	μ	12	10
x_{BL}	μ	3	2.5
x_{B}	μ	3.5	1.6
x_{E}	μ	2.7	1.2

Table 6.1

Processing Details For Procedures At E.R.L. U.C. Berkeley (P1)

And At Signetics Corporation, Sunnyvale (P2)

base diffusion depth x_B (3.5 μ in P1), the base-collector space-charge region (2 μ at -16 V in 1 Ω cm epi) and the outdiffusion of the Arsenic buried layer into the epitaxial layer x_{BL} . This outdiffusion mainly occurs during the isolation diffusion of Boron and is approximately given by [20]

$$x_{BL} = x_{EPI} \sqrt{\frac{D_{As}}{D_B}} \qquad \ldots (6.1)$$

where D_{As} and D_B are the diffusion constants for As and B respectively. At 1200°C it is found that approximately $x_{BL} = x_{EPI}/4$. An epitaxial layer thickness of about 10 μ is thus sufficient but in P1 a thickness of 12 μ has been chosen to allow for thickness uncertainties. During the isolation diffusion, the Boron also diffuses laterally underneath the oxide. As a rule of thumb, lateral diffusion proceeds as fast as vertical diffusion. The distance between the buried layer and the isolation wall l_i thus has to be larger than the sum of the side-diffusion lengths of the isolation wall (12μ) and the buried layer (3μ). If misalignment up to 5 μ is allowed, a safe value is obtained for $l_i = 30\mu$.

The outer transistors of the pair Q_3 and Q_6 (Figure 5.8) are designed for low base resistance r_B and especially for a low product of base resistance and emitter-base junction capacitance C_{jE} . This product does not decrease significantly if more than two base stripes and one emitter are used because

C_{jE} then increases by the same ratio as r_B decreases. The surface geometry of this transistor is shown in Figure 6.1.b. Decreasing the base resistivity also decreases the value of r_B but increases the value of C_{jE}. The product $r_B C_{jE}$ is reduced [19, 23] but a considerable reduction in β is then experienced. This is clearly illustrated by the values of β and r_B for both processes P1 and P2 listed in Table 6.2. The values of C_{jE} are listed in Table 6.3. For a higher base doping (P1), β and r_B are both lower but C_{jE} is higher than for process P2 with higher base sheet resistivity. Product $r_B C_{jE}$ is lower for P1 whereas ratio r_B/β, which is important at low frequencies, is lower for P2.

For biasing purposes, lateral pnp transistors are also used. Because of their low f_T, they cannot be used in the signal path. For a standard six-mask process, the emitter of the pnp and the base of the npn are diffused simultaneously. Thus a p diffusion with high sheet resistivity will cause a high value of β for the npn but a low emitter efficiency and thus a low value of β for the pnp. Also a narrow lateral base width and the presence of a buried layer improve the efficiency of the carrier transport from emitter to collector and thus improve β. However, decreasing the basewidth is limited by side-diffusion and punch-through. Also the Early voltage V_E becomes very small. For these reasons, the value of the basewidth has been chosen to be 10μ. The layout of the pnp transistor is shown

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* The symbol V_E has been chosen because V_A refers to the dc control voltage of the agc amplifier.

		P1			P2		
		1B	2B	pnp	1B	2B	pnp
I_S	fA	0.60	0.60	6.2	4.1	4.0	1.25
n		1.00	1.00	1.11	1.10	1.10	1.11
V_E	V	100	100	60	20	20	70
β(1mA)		22	24	5.5	800	800	0.6
(0.1mA)		10	12	19	800	800	1.7
f_T(5mA)	MHz	210	210	-	625	660	-
f_T(0.5mA)	MHz	135	140	4	210	210	1.1
C_f	pF	9.6	10.2	-	8.3	10.8	-
τ_C	ms	0.70	0.81	-	0.22	0.20	-
r_B(5mA)	Ω	74	44	-	580	440	-
r_{Bph}	Ω	105	65	-	710	580	-
r_C	Ω	48	47	-	50	42	-

Table 6.2

Transistor Parameters For Processes P1 And P2.

		P1		P2	
		1B	2B	1B	2B
C_μ (0V)	pF	2.12	3.17	2.25	3.07
C_μ (-5V)	pF	1.34	2.18	1.25	1.90
Φ_C	V	0.56	0.56	0.50	0.48
C_{jE}(0V)	pF	2.25	3.29	1.61	2.05
Φ_E	V	0.76	0.74	0.84	0.83
C_{CS}(0V)	pF	4.10	4.50	3.73	3.78
C_{CS}(-5V)	pF	3.14	3.41	3.04	3.10

Table 6.3

Capacitance Values Of The Transistors of Processes P1 And P2

in Figure 6.1.c.

6.3 DESIGN OF THE INTEGRATED CIRCUIT

The improved agc amplifier of Figure 5.8 is embedded in the integrated circuit represented in Figure 6.2. A microphotograph of the circuit is given in Figure 6.3.

The biasing scheme has to satisfy two specific requirements. The total quad current I_{EE}, which is the sum of the emitter currents of Q_4, Q_5, Q_6 and Q_7, must be stabilized with respect to transistor parameters. This must be achieved even when I_{EE} is small compared with the total pair current I_P which flows through Q_1. Also, the output terminals at the collectors of Q_6 and Q_7 must be isolated from the collectors of Q_4 and Q_5 in order to prevent feedthrough along the power supply lines. The design of a bias network to achieve these objectives is now discussed in detail.

Transistor Q_1, which carries current I_P, delivers the quad current I_{EE} and also current I_Q, which flows through resistances R_{B1} and R_{B2}. If I_{EE} is only a fraction of I_Q, any inaccuracy in the determination of I_P would cause considerable variation in the amplitude of current I_{EE}. Therefore, current I_{EE} is sensed by diode-connected transistor Q_8, which drives Q_9, Q_{10} and finally Q_1. This feedback loop stabilizes I_{EE} at the value given by

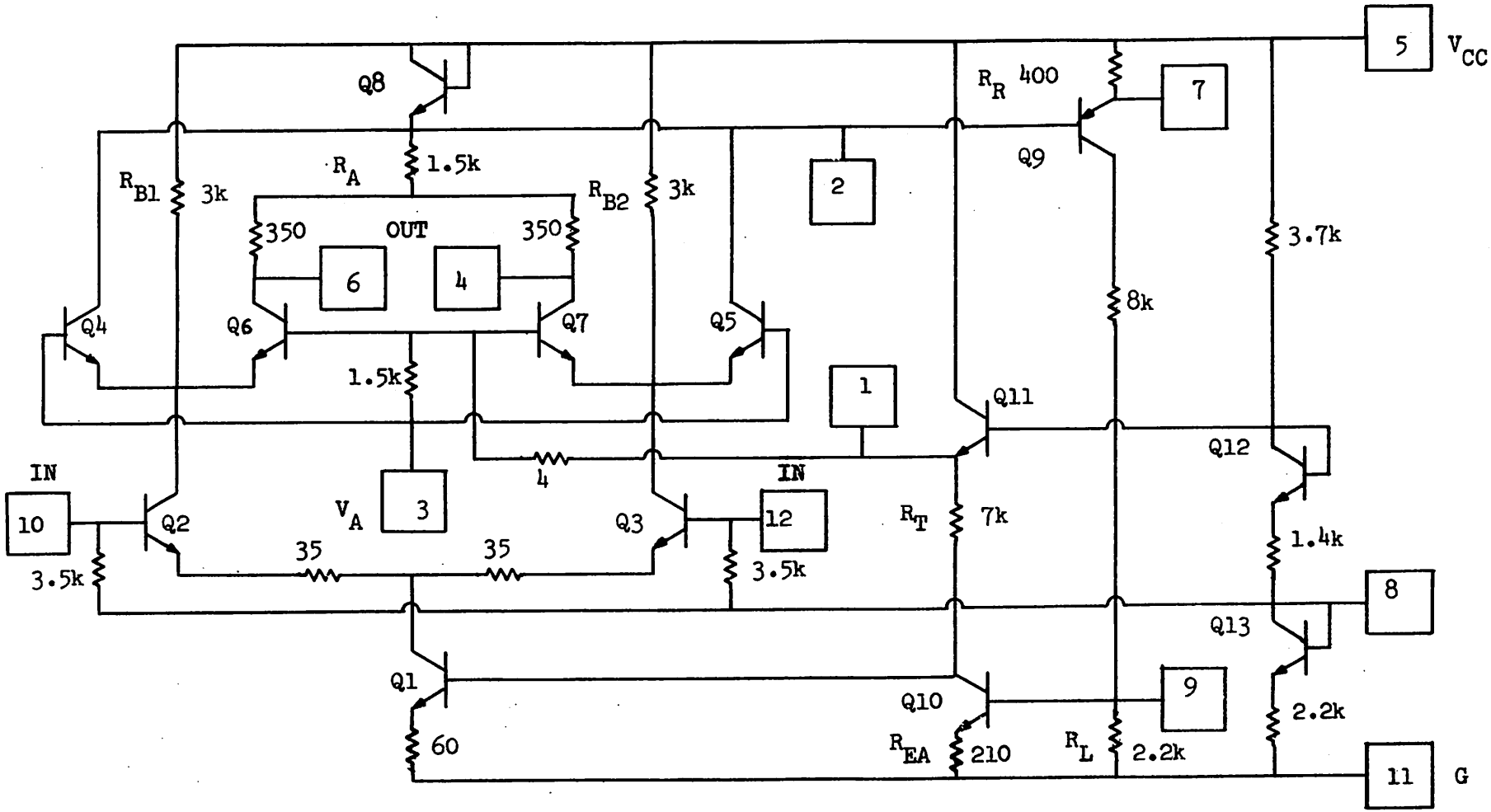

Figure 6.2.

Integrated circuit realization of the Improved Agc Amplifier. The resistor values are given for process P1. For process P2, the resistor values are twice as large.

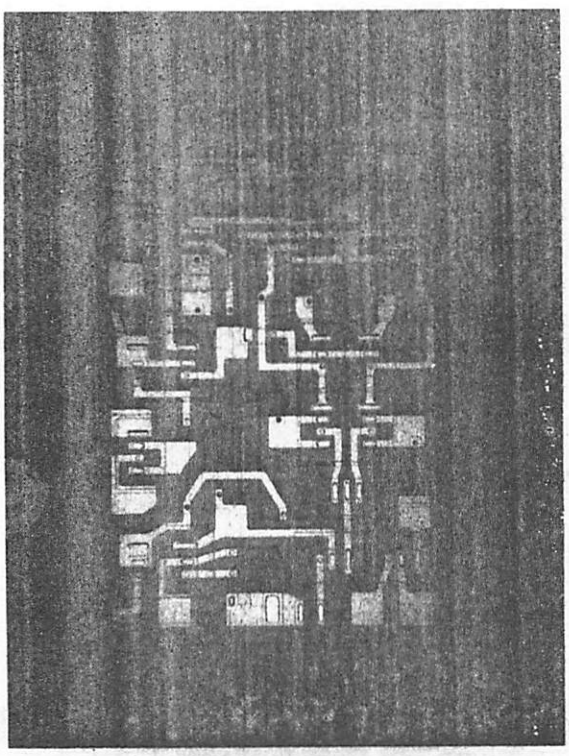

Figure 6.3.

Microphotograph Of The Improved AGC Amplifier In Integrated Form; The Circuit Dimensions Are 1.18 x 1.48 mm, And The Reduction 43x.

$$I_{EE} = \frac{I_Q}{T - 1} \qquad \ldots (6.1)$$

where T is the dc loop gain, approximately given by

$$T \simeq h \frac{R_L}{R_{EA}} \frac{R_T}{R_E} \quad . \qquad \ldots (6.2)$$

Factor h is the current gain realized by transistors Q_8 and Q_9 with emitter resistor R_R, and is thus given by the ratio of I_{C9} to I_{EE} or

$$\frac{1}{h} = \frac{1}{\beta_P} + \frac{I_{SN}}{I_{SP}} \exp\left(\frac{h R_R I_{EE}}{\alpha_P V_T}\right) \qquad \ldots (6.3)$$

in which I_{SN} and I_{SP} are the saturation currents for Q_8 and Q_9 respectively; α and β are the common-base and common-emitter current gain of pnp transistor Q_9. The value of I_{EE} is thus determined by current I_Q and resistor R_R. The value of current I_Q is given by

$$I_Q = \frac{V_{CC} - V_A + V_{BEon}}{R_{B1,2}} \qquad \ldots (6.4)$$

where V_{BEon} equals about 0.7V and V_A is the voltage at the bases of Q_6 and Q_7. For the resistance values shown in Figure 6.2, it is given by

$$V_A \simeq \frac{V_{CC}}{2} \quad . \qquad \ldots (6.5)$$

As it is seen from (6.1), (6.2) and (6.3), the value of I_{EE} is a decreasing function of the value of resistance R_R. When R_R is shorted out externally, I_{C9} reaches its highest

value and I_{EE} its lowest value. Current I_{EE} can be reduced further by connecting in parallel with Q_9 an external pnp transistor with higher I_{SP}, or by raising the voltage level at the base of Q_{10} by means of external resistors. However, this latter method de-activates the stabilization of the feedback loop and is thus less attractive than the first method.

Large values of I_{EE} can be achieved for high values of R_R. Since R_R is limited to the value used in the integrated circuit, I_{EE} can also be increased by lowering the voltage level at the base of Q_{10}. This can be done conveniently by connecting external resistance from this point to ground.

As an example, consider process P1. For this process, $T = 1200$ h and for $V_{CC} = 10$ V and $I_Q = 3.8$ mA, $I_{EE} = 12.5$ mA if no external resistors are used and less than 0.1 mA if R_R is shorted out. In process P_2, $T = 1230$ h and for $V_{CC} = 12$ V and $I_Q = 2.3$ mA, $I_{EE} = 1.67$ mA but 1.06 mA if R_R is shorted out. The connection of a 2N4249 in parallel with Q_9 changed these currents respectively to 7.4 mA and less than 0.1 mA. An external resistance of 19.7k between the collector of Q_{13} and the base of Q_{10} also causes $I_{EE} = 0.1$ mA without shunting R_R or Q_9.

The feedback loop is decoupled at high frequencies by bypassing the base of either Q_9 or Q_{10} or Q_1 with a high

and is added in the collector lead of Q_9 . The other resistance (4 Ω) was diffused together with the emitter n-diffusion and connects the bases of Q_6 and Q_7 (voltage level V_A) with the emitter of Q_{11} .

The output transistors Q_6 and Q_7 are small-size transistors, whereas the other transistors of the quad Q_4 and Q_5 and also the input transistors have a double base stripe to minimize base resistance. All other npn transistors only serve bias purposes and are thus small-size transistors. Care was taken to lay out the quad and input pair in as symetrical and compact a way as possible. Also, the input and output paths are bonded to leads on opposite sides of the TO-5 package. The input leads are separated by the ground (and substrate) lead and the output leads are separated by the power supply lead.

6.4 TRANSISTOR CHARACTERIZATION

As shown before, the performance of the improved agc amplifier is mainly limited by transistor parameters such as base-transit time τ , both junction capacitances C_{jE} and C_{jC} , the collector-substrate capacitance C_{CS} and also base and collector series resistances r_B and r_C . Therefore, special effort was taken to characterize these parameters. The small signal current gain β is included for its effect

quality capacitance. However, bypassing the base of Q_9 has the additional advantage that common mode signals caused by the signal currents in Q_4 and Q_5 are prevented from reaching the output terminals. Also, the inclusion of resistance R_A improves the isolation significantly. If the input signal drive is not differential but applied only to one input terminal, another bypass capacitor to ground is required at the other input terminal.

In order to avoid excessive circuit complexity, no effort was made to make the current levels independent of supply voltage V_{CC}. However, as it is shown by (6.5), arrangements were made to keep the voltage level V_A approximately constant with temperature, because the dc control voltage is applied to this point. Actually, the control voltage is applied to the bases of the outer transistors Q_4 and Q_5 because this point can then be bypassed to avoid additional effective base resistance. A low resistance to ground for the bases of Q_6 and Q_7 is less important. On the contrary, additional base resistance tends to compensate the distortion at high attenuation (see Section 2.6). Nevertheless, the output resistance of Q_{11}, which provides V_A, is never high because Q_{11} also delivers the collector current of Q_{10}.

In order to make the circuit planar, two cross-unders have been used. The first (8 kΩ) is made from the p-diffusion

on low frequency distortion. For bias considerations, dc parameters such as the saturation current I_S , the emission coefficient n and the Early voltage V_E are also characterized. The collector-base reverse bias for all transistors is 5 V unless stated otherwise. The results are listed in Tables 6.2 and 6.3.

6.4.1 SATURATION CURRENT I_S AND EMISSION COEFFICIENT n .

The dc collector current I_C is related to the base-emitter voltage V_{BE} by

$$I_C = I_S \exp\left(\frac{V_{BE}}{nV_T}\right) \qquad \ldots (6.4)$$

where I_S is the saturation current and V_T equals 26 mV at 27.6° C (obtained in mV by dividing the absolute temperature in °K by 11.60); n is the emission coefficient. The results are obtained for collector currents between 1 μA and 100 μA where $\ln I_C$ is linear in V_{BE} and temperature effects are negligible.

6.4.2 EARLY VOLTAGE V_E AND AC CURRENT GAIN β .

The Early voltage V_E is the ratio of the collector current to the slope of the I_C - V_{CE} characteristic at that current. For moderate currents, it is independent of current [12] and measured on the curve tracer. The ac current gain is

also measured on the curve tracer. As expected, the β of the pnp transistor peaks at a much lower current than for the npn transistor.

6.4.3 COMMON-EMITTER UNITY-GAIN FREQUENCY f_T .

This frequency is obtained by measuring β at 100 MHz. However, the value of f_T for a transistor packaged in a TO-5 can is lower than for the same transistor used in the actual integrated circuit. In order to obtain the real device f_T , these parasistic capacitances are resonated out by a parallel LC circuit across the input terminals, which is tuned at 100 MHz. For this purpose a transistor is used with exactly the same bonding and package as the transistor for which f_T has to be measured, except that the contact windows are not opened and thus no electrical contact is made.

Plotting $1/f_T$ versus $1/I_C$ gives a straight line for low values of I_C [16] . Its slope is given by

$$\frac{I_C}{f_T} = 2\pi V_T C_f \qquad \ldots (6.5)$$

where $C_f = C_{jE} + C_{jC}$. Extrapolation to the $1/f_T$ axis yields the effective base transit time τ_C which is related to the base transit time τ by

$$\tau_C = \tau + r_C C_\mu \qquad \ldots (6.6)$$

Other components in f_T [16] are unimportant if f_T is not very large. The results obtained are listed in Table 6.2. The value of C_f is mainly determined by surface geometries and is thus about the same in both processes. Process P2 makes use of shallower diffusion depths however, and thus yields a lower value of τ_C .

6.4.4 BASE RESISTANCE.

Throughout this study it has been shown that the base resistance has a dominant effect on the noise and distortion performance of variable-gain amplifiers. Also, it has been found that the optimum choice of current level in the amplifier mainly depends on the value of the base resistance. For this reason, an accurate method of estimating this value is of crucial importance.

Several methods have been surveyed, but two methods have been found to be most useful [8] . The first one is called the circle-diagram method. It yields an estimate of base resistance from the measurement of the common-emitter input impedance as a function of frequency. This method has the advantage of averaging a number of data points (at different frequencies) for better accuracy. It allows high frequency deviations to be easily detected. Also an estimate of base resistance can be obtained over a range of collector currents.

This method also yields a good estimate of the -3 dB frequency for the common-emitter gain f_β .

The other method is called the phase-cancellation method. It gives an estimate of base resistance from the measurement of the common-base input impedance at the collector current where this impedance is real. It involves only one measurement at one arbitrary high frequency. Both methods are now briefly examined. Only the aspects which are important for this study are retained from the general treatment [8] .

The hybrid-π model of a bipolar transistor is represented in Figure 6.4.a. The common-emitter input impedance is measured with a Wayne-Kerr RC bridge at several high frequencies. Each time, all parasitic capacitances of package and paths are included to null the bridge. They are thus not represented in the model of Figure 6.4.a. The measured values of input impedance are plotted in the complex phase and a circle of best fit is drawn (Figure 6.4.b). The low frequency real axis value $R_{i,lo}$ is then given by

$$R_{i,lo} = r_\pi + r_B + (1 + \beta)\, r_E \qquad \ldots (6.7)$$

and the high frequency real axis extrapolation of this circle is approximately given by

$$R_{i,\,hi} \simeq r_B \left[1 - \frac{C_\mu}{2C_T} (1 + g_m r_C) \right] \qquad \ldots (6.8)$$

with $C_T = C_\pi + C_\mu (1 + g_m r_C)$. The lower point of the

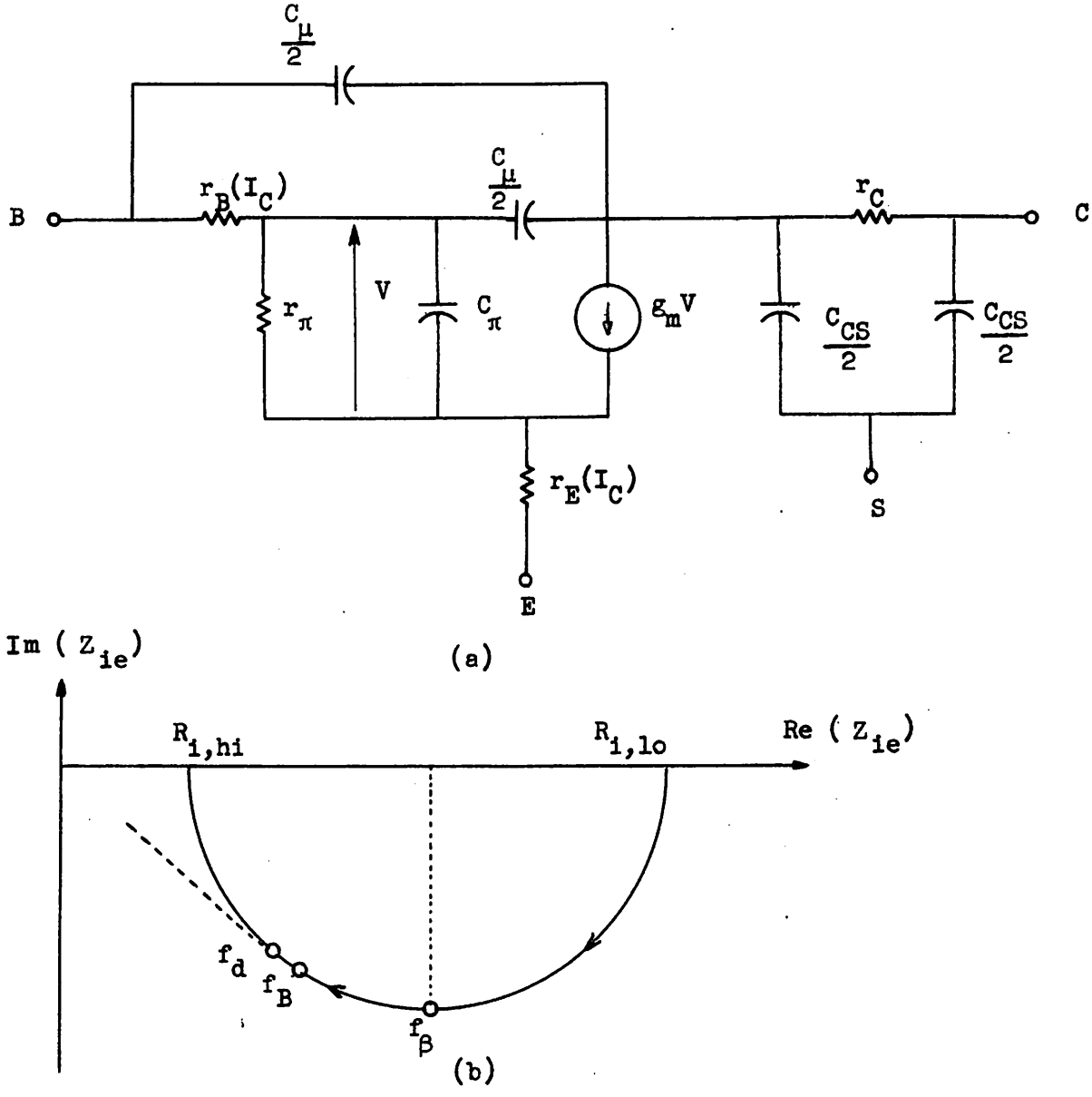

Figure 6.4.

(a) Small signal transistor model. (b)— Circle diagram; --- deviation from circle diagram for a distributed base.

circle coincides with frequency f_β which is given by

$$f_\beta = \frac{1}{2\pi r_\pi C_T} \quad . \qquad \ldots (6.9)$$

Emitter lead inductance and excess phase are not taken into account.

From the above results the values of r_B and r_E are obtained as follows. After calculation of g_m and measurement of β, C_μ and r_C, the value of r_B is found from (6.8) and the value of r_E is found from (6.7). Scaling the circle in frequency gives the value of f_β. For all npn transistors, the values of r_B are given in table 6.2 for $I_C = 5$ mA.

At high frequencies, the distributed nature of the base resistance causes deviation from the circle (Figure 6.4.b) This starts about at frequency f_d which has been found to be usually higher than frequency f_B defined by

$$f_B = \frac{f_T}{g_m r_B} \quad . \qquad \ldots (6.10)$$

For this reason, the circle is fitted to the data only for frequencies below f_B. However, the value of r_B obtained in this way is useful up to frequencies much higher than f_B.

The circle-diagram method becomes increasingly difficult to use at lower collector currents unless β is quite low, because the diameter of the circle becomes large compared to the high frequency asymptote. For low currents, the other method is used.

The phase-cancellation method gives the value of base resistance at one low collector current and proceeds as follows. The common-base input impedance is measured at one arbitrary high frequency. The collector current is then varied until this impedance has become real. It can be shown that this occurs at

$$I_{CB} = \frac{V_T}{r_B} \quad \ldots (6.11)$$

at which current the input resistance is given by

$$R_{in} = r_B + r_E \quad \ldots (6.12)$$

This can be understood by examining the model in Figure 6.4. The impedance consisting of r_π and C_π is always capacitive so that the presence of r_B causes the current generator to look inductive. For high current levels, the current generator dominates and the input impedance is inductive. For very low current levels, the current generator has negligible effect and the input impedance is capacitive. As a result, a current exists at which the input impedance is purely resistive. This current is given by (6.11).

The effect of small capacitances is negligible as long as they do not appear at the emitter lead. For the npn transistors, the values obtained by the phase-cancellation method are denoted by r_{Bph} and are listed in Table 6.2. Since these values are obtained at lower currents than the ones given by

the circle-diagram method, they are higher in value because r_B decreases as collector current increases.

6.4.5 JUNCTION CAPACITANCES C_{jE} , C_{jC} AND C_{CS}.

The bandwidth at low quad currents and the signal feed-through are dominated by the junction capacitances. Prediction of circuit performance thus relies directly on accurate knowledge of these capacitance values.

These capacitances have been measured by means of a Boorton capacitance bridge at 100 kHz. The bridge is nulled with the parasitic capacitances of package and paths corrected. The results are listed in Table 6.3. It has been found that the capacitances C_{jE} and C_{jC} depend on their bias voltage by a one-third law. Capacitance C_{CS} obeys a one-half law. Also, an aluminum path of 50 x 50 μ represents about 0.4 pF. Adjacent leads of a TO-5 add about 0.3 pF parasitic capacitance or about 0.1 pF if the leads are not adjacent. These values illustrate the importance of accounting for parasitic capacitances in the measurement of transistor junction capacitances.

CHAPTER 7.

SUMMARY AND CONCLUSIONS.

The optimization of the dynamic range and the bandwidth of integrated variable-gain amplifiers is illustrated by the design of three basic amplifiers which consist of a quadruple of transistors driven by an input pair. The circuits examined are the agc amplifier [3] , the multiplier [2] and Gilbert's variable-gain quad [1] . An extensive analysis of distortion and noise in these quads has shown that the agc amplifier is most suitable for the realization of a high dynamic range. Mismatch of the transistors limits the performance of the multiplier and the dynamic range of Gilbert's quad is mainly limited by distortion.

The maximum product of output signal-to-noise ratio and maximum dynamic range n. DR_M that can be achieved with a given bipolar transistor depends only on its base resistance. As a consequence a practical upper limit for this product is found by assuming very small base resistances (20 Ω). For a frequency band of 4.5 MHz, the product then equals 95 dB. If one thus requires 40 dB signal-to-noise ratio, 55 dB dynamic range is about the best that can be expected from bipolar transistors.

In order to achieve this maximum dynamic range in an integrated agc amplifier, the current level in the quadruple has to be sufficiently low so that distortion and noise fall within the required limits. However, to obtain low distortion over a

wide bandwidth in the input stage, the current in the input pair has to be high. In the improved agc amplifier a dc feedback loop stabilizes the quad current at a much lower value than the pair current. Only in this way can the maximum dynamic range be reached for given transistor parameters.

The maximum dynamic range is obtained only for a very specific value of output signal amplitude. In some applications however, a larger output signal is more important than the maximum dynamic range. The current in the quad then has to be increased which causes a reduction in dynamic range due to base resistance noise in the quad. Also, if the current level in the input stage is judged to be too high for power considerations, the current can be decreased at the expense of reduced dynamic range due to distortion in the input pair.

The input pair also limits the frequency response of the agc amplifier. This is only true however if the effect of the output capacitance can be made negligible by the output amplifier, as was the case in this work. The current in the quad itself is usually not so low that it affects the time constant of the input stage.

The improved agc amplifier has been realized in integrated form using two different processes. For the first one, the maximum dynamic range was found to be 33 dB at 70 MHz (Δf = 4.5 MHz) and was obtained at 3.5 mV_{RMS} output signal. This is only 1.5 dB

less than the theoretical value for at least 40 dB output signal-to-noise ratio and less than 1% third-order intermodulation distortion. At this frequency, the dynamic range is mainly limited by feedthrough and not by distortion. At full gain, the bandwidth was 120 MHz but for 32 dB attenuation and more, the bandwidth decreased again due to signal feedthrough.

For the second process, the base resistance is much higher so that only 27 dB dynamic range was obtained. Bandwidth and signal feedthrough were similar to the values obtained for the first process.

For previous circuits, the total current in the pair was the same as in the quad so that large amounts of distortion and noise were generated in the quad. For the same total current as in the improved agc amplifier, the agc amplifier shows 12 dB less dynamic range due to noise and another 9 dB less due to distortion. It can thus be concluded that different current levels are needed in quad and pair to achieve the maximum dynamic range possible with the given transistor parameters.

APPENDIX A.

A.1 PROGRAM "NOLIBE."

For a non-linear transfer function F(X) = 0 with derivative DERF(X) = 0 , program NOLIBE calculates the harmonic output components for a sinusoidal input waveform. The non-linear equation is solved over NPO points by SUBROUTINE RTNI. The tabulated output waveform FST(NPO) is then Fourier analysed (NHAR harmonics) by SUBROUTINE FORIT. The listing is included for equation (2.32).

A.2 PROGRAM "NONLIN."

Program NONLIN is similar to program NOLIBE, but solves a first-order non-linear differential equation instead. The number of points is again NPO. For each point Z the function value VALUE at the next point (i.e. at Z + DT) is calculated by a fourth-order Runge-Kutta method described in SUBROUTINE RKGA (VALUE, Z, DT). Therefore the derivative of the function VALUE with respect to Z is calculated in SUBROUTINE DUM (VALUE,Z). The Fourier Analysis is performed by SUBROUTINE FOURAN.

The listing is given for Equation (3.3). Parameter b in (3.3) is represented by B , B in (3.4) by A and B in (3.5) by CURI. Also I_{C2} in (3.3) is transformed into F by

$$I_{C2} = I_E \frac{1 + VK(B,Z,CURI)}{1 + \exp F} \qquad \ldots (A1)$$

in order to avoid ln functions in the equations.

Another example for solving a non-linear differential equation of the first order is given in program ECURC. This program yields i as a function of t for the equation

$$\exp\ (V \cos t - B \frac{di}{dt} - Ti) = 1 + i \qquad \ldots (A2)$$

using the transformation

$$1 + i = \exp (f) . \qquad \ldots (A3)$$

This program is given because of an additional feature which is not present in NONLIN. The computational stability of the solution is verified by comparison of the first and last function values of one period. Only if they differ less than a given limit is the Fourier analysis performed. Otherwise the computation is extended for another period. This continues for a limited number of iterations until stability is obtained.

```
                PROGRAM NOLIBE(INPUT,OUTPUT)
)0003           COMMON RS,BE,SIV,B1,B2,AIN1,AIN2
)0003           DIMENSION FNT(500),FST(500),SIF(11),COF(11),ACS(11)
)0003           EXTERNAL FCT
)0003           EXTERNAL FCS
)0003           DO 150 NKA=1,30
)0005           READ 201,NPO,NHAR,NR,RS,BE,VE,KBE1,KBE2
)0030           IF(NPO.EQ.0) STOP
)0033           PRINT 240,NPO,NHAR,NR,RS,BE,VE,KBE1,KBE2,NKA
)0061           NE=(NPO-1)/2
)0064           PRINT 204
)0067           IEND=20
)0070           TPO=NPO
)0071           B1=KBE1
)0073           B2=KBE2
)0074           AIN1=(1.+B1)/B1
)0077           AIN2=(1.+B2)/B2
)0101           DO 112 I=1,NPO
)0103           FNT(I)=SIN(6.2831853*I/TPO)
)0111           SIV=1.+VE*FNT(I)
          C        INITIAL GUESS ROOT X
)0114           XST=2.*SIV/(1.+EXP(BE))
)0121           EPS=1.E-4*XST
          C        SUBR RTNI
)0123           IF(BE)107,107,108
)0125       107 CALL RTNI(Y,F,DERG,FCS,XST,EPS,IEND,IER,IT)
)0136           FST(I)=Y
)0140           GO TO 109
)0141       108 CALL RTNI(X,F,DERF,FCT,XST,EPS,IEND,IER,IT)
)0152           FST(I)=X
)0154       109 PRINT 205,I,FNT(I),FST(I),F,XST,EPS,IER,IT
)0200       112 CONTINUE
          C        FOURIER ANALYSIS
)0203           CALL FORIT(FST,NE,NHAR,COF,SIF,IER)
)0207           PRINT 210,NPO,NHAR,IER
)0221           NHAS=NHAR+1
)0223           DO 120 I=1,NHAS
)0225       120 ACS(I)=SQRT(COF(I)*COF(I)+SIF(I)*SIF(I))
)0240           DO 130 I=1,NHAS
)0241           KI=I-1
)0242           ACSR=100.*ACS(I)/ACS(NR+1)
)0246       130 PRINT 230,KI,SIF(I),COF(I),ACS(I),ACSR
)0266       150 CONTINUE
)0270       201 FORMAT(I3,I2,I1,3F6.3,2I3)
)0270       204 FORMAT(5X,≠POINT  INPUTSINUS OUTPUTSINUS    RESULT FUNCT        INI
              1T ROOT ERROR LESS THAN ERRORCODE      ITER≠/)
)0270       205 FORMAT(5X,I5,2F12.8,3E16.8,2I10)
)0270       210 FORMAT(1H1,≠FOURIER ANALYSIS WITH≠,I6,≠ POINTS≠,I6,≠ HARMONICS
              1    ERRORCODE≠,I4)
)0270       230 FORMAT(5X,I2,≠ HARM SIN=≠,E14.5,≠ COS=≠,E14.5,≠ MAG= ≠,E14.5,F12.5
              1,≠ PERCENT≠)
)0270       240 FORMAT(1H1,≠M=≠,I4,≠ NHAR=≠,I3,≠ NR=≠,I2,≠ RS=≠,F8.4,≠ BE=≠,F8.4,≠
              1 VE=≠,F8.4,≠ BETA1=≠,I4,≠ BETA2=≠,I4,20X,≠ NUMBER CARD=≠,I4/)
)0270           END
```

```
                SUBROUTINE RTNI(X,F,DERF,FCT,XST,EPS,IEND,IER,IT)
C               SUBROUTINE RTNI
C               X          RESULTANT ROOT OF EQUATION F(X)=0
C               F          RESULTANT FUNCTION VALUE AT ROOT X
C               DERF       RESUTANT VALUE OF DERIVATJVE AT ROOT X
C               FCT        EXTERNAL SUBROUTINE USED. IT COMPUTES TO GIVEN
C                          ARGUMENT X FUNCTION VALUE F AND DERIVATIVE DERF
C               XST        INITIAL GUESS OF ROOT X
C               EPS        UPPER BOUND ERROR OF X
C               IEND       MAX NUMBER OF ITERATION STEPS
C               IER        =0  NO ERROR
C               IER        =1  NO CONVERGENCE AFTER IEND ITERATION STEPS
C               IER        =2  DERF WAS ZERO AT ANY ITERATION STEP
000014             IER=0
000014             X=XST
000016             TOL=X
000017             CALL FCT(TOL,F,DERF)
000027             TOLF=100.*EPS
000030             DO 6 I=1,IEND
000032             IF(F)1,7,1
000033          1  IF(DERF)2,8,2
000034          2  DX=F/DERF
000035             X=X-DX
000037             TOL=X
000040             CALL FCT(TOL,F,DERF)
000050             TOL=EPS
000050             A=ABS(X)
000052             IF(A-1.)4,4,3
000055          3  TOL=TOL*A
000057          4  IF(ABS(DX)-TOL)5,5,6
000063          5  IF(ABS(F)-TOLF)7,7,6
000066          6  CONTINUE
000071             IER=1
000072          7  IT=I
000074             RETURN
000075          8  IER=2
000077             RETURN
000077             END
```

RUN FORTRAN COMPILER VERSION 2.3 B.1

```
                SUBROUTINE FCT(X,F,DERT)
000006          COMMON RS,BE,SIV,B1,B2,AIN1,AIN2
000006          BEA=(AIN2+(1.+B1)/B2)/2.
000012          RSB1=RS/(1.+B1)
000015          EXE=EXP(BE+RSB1*(BEA*X-SIV))
000025          F=X*(AIN2+AIN1*EXE)-2.*SIV
000033          DERT=AIN1*EXE*(1.+X*BEA*RSB1)+AIN2
000041          RETURN
000041          END
```

RUN FORTRAN COMPILER VERSION 2.3 B.1

```
                SUBROUTINE FCS(Y,G,DERG)
000006          COMMON RS,BE,SIV,B1,B2,AIN1,AIN2
000006          RSB2=RS/(1.+B2)
000010          BEAY=(AIN1+(1.+B2)/B1)/2.
000015          EXYI=EXP(BE+RSB2*(BEAY*Y-SIV))
000025          G=Y*(AIN1+AIN2*EXYI)-2.*SIV
000033          DERG=AIN2*EXYI*(1.+Y*BEAY*RSB2)+AIN1
000041          RETURN
000041          END
```

RUN FORTRAN COMPILER VERSION 2.3 B.1

```
                SUBROUTINE FORIT(FNT,N,M,A,B,IER)
        C          SUBROUTINE FORIT
        C          FNT  VECTOR OF TABULATED FUNCTION VALUES OF LENGTH 2N+1
        C          N    DEFINES THE INTERVAL
        C          M    MAXIMUM ORDER OF HARMONICS TO BE FITTED
        C          A    RESULTANT VECTOR OF FOURIER COSINE COEFF OF LENGTH M+1
        C          B    RESULTANT VECTOR OF FOURIER SINE   COEFF OF LENGTH M+1
        C          IER  0  NO ERROR
        C          IER  1  N NOT EQUAL OR GREATER THAN M
        C          IER  2  M LESS THAN 0
000011             DIMENSION A(1),B(1),FNT(1)
000011             IER=0
000011          20 IF(M)30,40,40
000013          30 IER=2
000014             RETURN
000015          40 IF(M-N)60,60,50
000017          50 IER=1
000020             RETURN
000021          60 AN=N
000022             COEF=2./(2.*AN+1.)
000026             CONST=3.1415926*COEF
000027             S1=SIN(CONST)
000031             C1=COS(CONST)
000033             C=1.0
000035             S=0.
000035             J=1
000036             FNTZ=FNT(1)
000043          70 U2=0.
000044             U1=0.
000044             I=2*N+1
000047          75 U0=FNT(I)+2.*C*U1-U2
000055             U2=U1
000056             U1=U0
000057             I=I-1
000061             IF(I-1)80,80,75
000063          80 A(J)=COEF*(FNTZ+C*U1-U2)
000071             B(J)=COEF*S*U1
000073             IF(J-(M+1))90,100,100
000076          90 Q=C1*C-S1*S
000102             S=C1*S+S1*C
000104             C=Q
000105             J=J+1
000107             GO TO 70
000110         100 A(1)=A(1)*.5
000112             RETURN
000112             END
```

```
                PROGRAM NONLIN (INPUT,OUTPUT,TAPE6=OUTPUT)
        C       DIFF. PAIR  NC F.B
000003      100 FORMAT (1H0,10HFACTOR A =,E11.4,10X,17HDRIVE VOLTAGE B =,F10.5,10X
                   1,10HFACTOR B =,E11.4,10X,11HAV. VALUE =,E12.5/)
000003      101 FORMAT (1X,3H N ,8X,9HMAGNITUDE/)
000003      102 FORMAT (1X,I3,F16.6)
000003      103 FORMAT (1X,15HINITIAL VALUE =,E13.6,10X,13HFINAL VALUE =,E13.6/)
000003      104 FORMAT (1X,18HFEEDBACK FACTOR H=,F8.3/)
000003      105 FORMAT (1X,21HINPUT CURRENT AMPL. =,F8.3,5X,6HF/FT =,F9.4/)
000003          COMMON A(10),B(10),I,J
000003          DIMENSION F(1000),C(500),FI(500),BB(500),AA(500),DB(500)
000003          COMMON H
000003          B(1)=-10.
000004          B(2)=-50.
000006          A(1)=10.
000007          A(2)=16.66
000011          A(3)=32.
000012          A(4)=100.
000014          A(5)=166.66
000015          A(6)=-2.
000017          H=0.
000017          CURI=.01
000021          DT=0.012566371*2.
000023          DO 201 J=1,10
000024          IF (B(J).LT.(-30.)) STOP
000031          DO 200 I=1,10
000033          IF (A(I).LT.(-1.)) GO TO 201
000036          X=0.06*A(I)
000037          Z=0.
000040          VALUE=0.5
000042          L=1
000043          DO 202 K=1,750
000045          CALL RKGA(VALUE,Z,DT)
000047          Z=FLOAT(K)*DT
000051          VK=(CURI*(SIN(Z)-X*COS(Z)))/(1.+X**2)
000064          IF(K.EQ.500) XI=(1.+VK)*1./(1.+EXP(VALUE))
000074          IF (K.LE.500) GO TO 202
000077          F(L)=(1.+VK)/(1.+EXP(VALUE))
000104          L=L+1
000106      202 CONTINUE
000110          XF=F(250)
000111          KEY=4
000113          CALL FOURAN(250,250,1,05,KEY,F,C,FI,BB,AA,DB,A0,CMAX)
000127          BBB=A(I)
000131          PRINT 100,A(I),B(J),BBB,A0
000145          PRINT 103,XI,XF
000155          PRINT 105,CURI,X
000165          PRINT 101
000171          DO 203 IJK=1,5
000173          C(IJK)=C(IJK)*CMAX
000175      203 PRINT 102,IJK,C(IJK)
000207      200 CONTINUE
000211      201 CONTINUE

000213          END
```

RUN FORTRAN COMPILER VERSION 2.3 B.1

```
                FUNCTION DUM(VALUE,Z)
000005          COMMON A(10),B(10),I,J
000005          COMMON H
000005          X=0.06*A(I)
000007          CURI=.01
000010          VK=(CURI*(SIN(Z)-X*COS(Z)))/(1.+X**2)
000024          VJ=(A(I)*CURI*(X*SIN(Z)+COS(Z)))/(2.*(1.+X**2))
000043          VJ=VJ+VJ
000044          VD=(A(I)*(1.+VK)*EXP(VALUE))/(1.+EXP(VALUE))**2
000060          VD=VD+VD
000061          RR=(A(I)*CURI*(COS(Z)+X*SIN(Z)))/((1.+EXP(VALUE))*(1.+X**2))
000104          RR=RR+RR
000105          IF (VD.LE.0.01) VD=0.01
000111          DUM=-(B(J)+VALUE+VJ-RR)/VD
000117          RETURN
000117          END
```

RUN FORTRAN COMPILER VERSION 2.3 B.1

```
                SUBROUTINE RKGA(VALUE,Z,DT)
          C     SUBROUTINE TO SOLVE FIRST ORDER D.E BY RUNGE KUTTA METHOD
000006          DVA=DUM(VALUE,Z)*DT
000012          VALUEA=VALUE+DVA/2.
000014          Z=Z+DT/2.
000016          DVB=DUM(VALUEA,Z)*DT
000023          VALUEA=VALUE+DVB/2.
000025          DVC=DUM(VALUEA,Z)*DT
000032          VALUEA=VALUE+DVC
000033          Z=Z+DT/2.
000036          DVD=DUM(VALUEA,Z)*DT
000043          VALUE=VALUE+(DVA+2.*DVB+2.*DVC+DVD)/6.
000052          RETURN
000053          END
```

RUN FORTRAN COMPILER VERSION 2.3 B.1

```
                      SUBROUTINE FOURAN(N,M,MIN,MAX,KEY,A,AMP,ANG,ASIN,ACOS,DB,SUM,CONST
                     1)
000020               10 FORMAT (1H1, 41HFOURIER ANALYSIS OF THE WAVEFORM GIVEN BY,I4,
                       27H VALUES//(1X,1P10E13.5))
000020               11 FORMAT (1X, I4, F15.7, F10.2, 3F15.7)
000020               13 FORMAT (21H NORMALISING CONSTANT, E16.8, 10X, 12HDC COMPONENT, E16
                       2.8/)
000020               14 FORMAT (4H-  N,6X, 9HMAGNITUDE, 8X, 2HDB, 10X, 5HANGLE, 10X,
                       2 4HSINE, 10X, 6HCOSINE/)
000020               15 FORMAT (1H1)
000020                      DIMENSION A(1000), AMP(500), ANG(500), ASIN(500), ACOS(500),
                       2 DB(500)
000020                      DOUBLE PRECISION ASIND, ACOSD
000020                      IS = 1
000020                      P = 3.14159265 / FLOAT(N)*2.
000023                      IF (KEY .LE. (-1))  IS = 2
000027                      KEY = IABS(KEY)
000030                      IF (KEY .EQ. 2.OR. KEY .EQ. 4) WRITE (6,10) N,(A(I), I=1,M)
000065                      SUM = 0.
000066                      DO 100 I=1,M
000070               100    SUM = SUM + A(I)
000075                      SUM = SUM / FLOAT(N)
000077                      CONST = 0.
000100                      DO 101 I=MIN,MAX
000102                      ASIND = 0.D0
000105                      ACOSD = 0.D0
000107                      DO 102 J=1,M
000111                      Y = P*FLOAT(MOD(I*J,N))
000120                      ASIND = ASIND + DBLE(A(J)*SIN(Y))
000145               102    ACOSD = ACOSD + DBLE(A(J)*COS(Y))
000175                      ASIN(I) = ASIND
000201                      ACOS(I) = ACOSD
000205                      AMP(I) = SQRT(ASIN(I)**2+ ACOS(I)**2)
000216               101    IF (ABS(AMP(I)) .GT. CONST) CONST = ABS(AMP(I))
000235                      IF (KEY .EQ. 0) CONST = FLOAT(N)/2.
000240                      IF (IS .EQ. 2) CONST = SUM*FLOAT(N)/2.
000245                      IF (KEY .EQ. 3) WRITE(6,15)
000256                      IF (KEY .GT. 2) WRITE(6,14)
000270                      DO 104 I=MIN,MAX
000272                      AMP(I) = AMP(I) / CONST
000275                      DB(I) = ALOG10(ABS(AMP(I)))*20.
000305                      ANG(I) = ATAN2(-ASIN(I),ACOS(I))
000320                      ASIN(I) = ASIN(I) / CONST
000323                      ACOS(I) = ACOS(I) / CONST
000325                      IF (KEY .LT. 3)  GO TO 104
000333                      WRITE(6,11) I, AMP(I), DB(I), ANG(I), ASIN(I), ACOS(I)
000360               104    CONTINUE
000365                      CONST = CONST / FLOAT(N)*2.
000370                      IF (KEY .EQ. 0) CONST = 1.
000372                      IF (KEY .LT. 3) GO TO 103
000374                      WRITE(6,13) CONST, SUM
000404               103    RETURN
000405                      END
```

```
                PROGRAM FOURIER(OUTPUT)
000003          COMMON A(10),B(10),V(15),I,J,ILS
000003          DIMENSION F(260),FA(11),FB(11),FFA(11),FC(11),FCR(11)
000003          A(1)=1.
000004          A(2)=10.
000006          A(3)=1.
000006          A(4)=2.
000010          A(5)=5.
000011          A(6)=-5.
000013          B(1)=2.
000013          B(2)=11.
000015          B(3)=3.
000016          B(4)=4.
000020          B(5)=9.
000021          V(1)=0.1
000023          V(2)=.5
000024          V(3)=1.
000026          V(4)=2.
000027          V(5)=3.
000031          V(6)=5.
000032          V(7)=7.
000034          V(8)=-2.
000035          A(2)=-3
000037          NC=5
000040          NPO=49
000041          NT=NPO*NC
000043          NK=NT-NPO
000045          DT=6.2831852/(NPO*1.)
000051          DO 101 I=1,10
000052          IF(A(I).LT.0.) STOP
000056          DO 102 J=1,15
000060          IF(V(J).LT.0.) GO TO 101
000062          Z=0.
000062          VALUE=1.
000064          LU=0
000064          ILS=0
000066          DO 103 K=1,NT
000067          Z=K*DT
000072          CALL FKGA(VALUE,Z,DT)
000074          IF(K.EQ.NK) XI=EXP(VALUE)-1.
000102          IF(K.LE.NK) GO TO 103
000105          LU=LU+1
000106          F(LU)=EXP(VALUE)-1.
000113          IF(ILS.GT.1) GO TO 104
000117      103 CONTINUE
000122          IF(ABS(F(LU)-XI).GT.XI/200.) GO TO 104
C               PREPARE FOURIER ANALYSIS
000130          N=(NPO-1)/2
000132          NHAR=5
000133          CALL FORIT(F,N,NHAR,FA,FB,IER)
000137          LU=N+N+1
000141          PRINT 81,LU,(F(IL),IL=1,LU)
000156      81  FORMAT (1H1, 41HFOURIER ANALYSIS OF THE WAVEFORM GIVEN BY,I4,
```

```
                27H VALUES//(1X,1P10E13.5))
000156          PRINT 84,X1,IER
000166      84  FORMAT(1X/,≠ INIT VALUE = ≠,1PE13.5,≠ ERRORCODE= ≠,I6)
000166          PRINT 83,B(I),A(I),V(J)
000200      83  FORMAT(1X//,≠ B= ≠,F10.3,9H          ,≠ A= ≠,F11.4,10X,≠ DRIVE
                *VOLTAGE = ≠,F10.3//)
000200          PRINT 504
000204          NHAS=NHAR+1
000206          DO 510 L=1,NHAS
000210          FC(L)=SQRT(FA(L)*FA(L)+FB(L)*FB(L))
000220      510 FFA(L)=ATAN2(-FB(L),FA(L))*180./3.1415926
000231          DO 520 L=1,NHAS
000232          IPOR=L-1
000233          FCR(L)=100.*FC(L)/FC(2)
000237      520 PRINT 506,IPOR,FB(L),FA(L),FC(L),FCR(L),FFA(L)
000261      504 FORMAT(1X,≠ORDER HARM≠,3X,≠SINE≠,8X,≠COSINE≠,15X,≠MAGNITUDE  RELAT
                1 MAG   PHASE≠/)
000261      506 FORMAT(7X,I2,3X,2E12.4,9X,1E11.4,2F11.4)
000261          GO TO 102
000261      104 PRINT 110,B(I),A(I),V(J),XI,F(LU),K,LU,ILS
000305      110 FORMAT(1H1,3F10.3,2E12.4,3I6)
000305      102 CONTINUE
000307      101 CONTINUE
000311          END
```

```
                FUNCTION DUM(VALUE,Z)
000005          COMMON A(10),B(10),V(15),I,J,ILS
000005          IF (VALUE.GT.46.) VALUE=46.
000010          IF(VALUE.LT.-46.) VALUE=-46.
000013          IF(ABS(VALUE).GT.45.)  ILS=ILS+1
000020          DUM=((V(J)*COS(Z)+A(I)-VALUE)/EXP(VALUE)-A(I))/B(I)
000037          RETURN
000037          END
```

```
                SUBROUTINE RKGA(VALUE,Z,DT)
          C     SUBROUTINE TO SOLVE FIRST ORDER D.E BY RUNGE KUTTA METHOD
000006          DVA=DUM(VALUE,Z)*DT
000012          VALUEA=VALUE+DVA/2.
000014          Z=Z+DT/2.
000016          DVB=DUM(VALUEA,Z)*DT
000023          VALUEA=VALUE+DVB/2.
000025          DVC=DUM(VALUEA,Z)*DT
000032          VALUEA=VALUE+DVC
000033          Z=Z+DT/2.
000036          DVD=DUM(VALUEA,Z)*DT
000043          VALUE=VALUE+(DVA+2.*DVB+2.*DVC+DVD)/6.
000052          RETURN
000053          END
```

APPENDIX B.

TEST CONFIGURATIONS.

In this Appendix, details are given on the measurements performed on the different circuits described in this work.

B.1 THE EMITTER-DRIVEN PAIR.

The data for the emitter-driven pair (Figure 2.4) has been taken with the transistors CA 3018. The collector has a dc load of 50 Ω and is dc coupled to a 50 Ω line. The collector currents are provided by two separate power supplies in order to avoid feedthrough along the supply line. A high frequency transistor MT 1061A with large emitter resistor (Figure B.1) is used as a current source.

The circuit is built on copper clad board to avoid parasitic inductances, and the input and output 50 Ω lines are connected directly to the circuit without intermediate connectors. The voltage supplies are provided by double-lead shielded wire, which is grounded only on the copper clad. High quality 0.05 μF capacitors bypass the supply voltages.

As input generators, only Hewlett Packard (H.P.) oscillators 651 B and 608 C have been used for their low output distortion. For measurement of intermodulation distortion two identical oscillators are connected together via 10 dB paths to a 50 Ω power divider. The output is detected by a wave analyser

H.P. - WA 310 A at low frequencies, or at high frequencies by a vector voltmeter (H.P. - 8405 A), of which the IF output is connected to the wave analyser. For measurement of intermodulation distortion at high frequencies, a receiver (Communication Electronics Type 901) is connected to the output via a calibrated attenuation. In this way, the receiver always operates at the same input signal level and need only be calibrated once at each frequency.

B.2 THE AGC AMPLIFIER.

The agc amplifier, represented in Figure 2.8, employs matched transistors (CA 3045) in the quad and a high frequency transistor pair (2N 3423) in the input stage. Large emitter resistance ($R_E = 250\,\Omega$) are used to isolate the distortion due to the quad only. The total current I_{EE} equals 10.2 mA and is provided by the same type of circuit as in Figure B.1. The values of the voltage supplies are $V_{CC} = 8$ V and $V_{EE} = 12$ V.

Since both input and output parts are differential, an ac coupled balanced-unbalanced transformer is used in both positions (Figure B.2). The resistances of $100\,\Omega$ then act respectively as source or load resistances and V_L is the ground or the dc voltage level in the circuit.

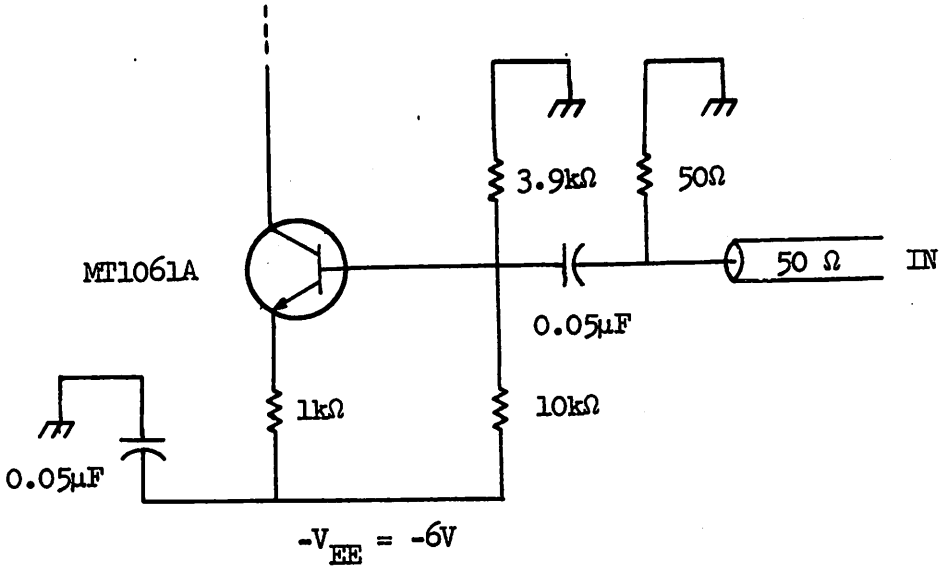

Figure B.1

Circuit realization of the Current Source Input Stage for the Emitter-driven Pair.

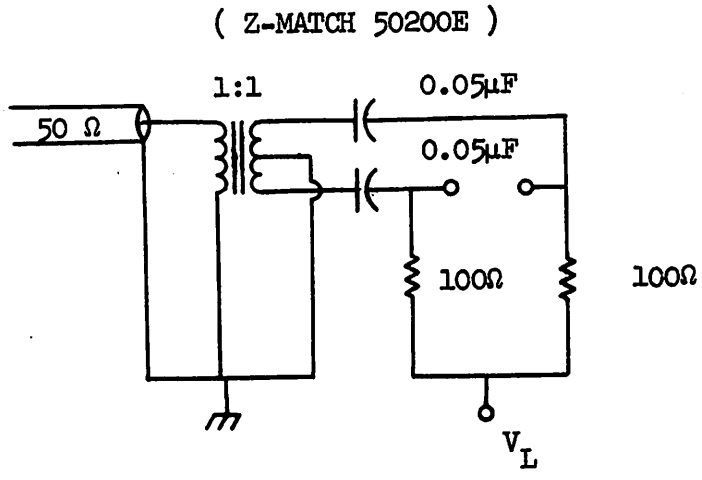

Figure B.2.

Balance-unbalance Conversion Circuit.

B.3 THE MULTIPLIER.

Since the multiplier, shown in Figure 2.10, is obtained by merely cross-connecting the collectors of Q_3 and Q_6 to the collector loads, the test circuit described in Appendix B.2 has been modified accordingly to obtain data for the multiplier.

B.4 GILBERT'S VARIABLE-GAIN QUAD.

Gilbert's variable-gain quad (Figure 2.13) also uses CA 3045 as the quad and 2N 3423 as input pair. The currents I_{E1} and I_{E2} are provided by independent current sources of the type shown in Figure B.1. Both currents can be varied between 0 and 4 mA. In all other aspects this circuit is set up as described in Appendix B.2.

B.5 THE IMPROVED AGC AMPLIFIER.

This amplifier, represented in Figure 6.2, is mounted in a TO-5 can and set up for measurements as it is shown in Figure B.3. All capacitances have a value of 0.05 μ F. The balanced-unbalanced conversion is provided by transformers which are terminated into 50 Ω . They consist of bifilar windings on two permalloy cores.

For each output terminal a separate output amplifier

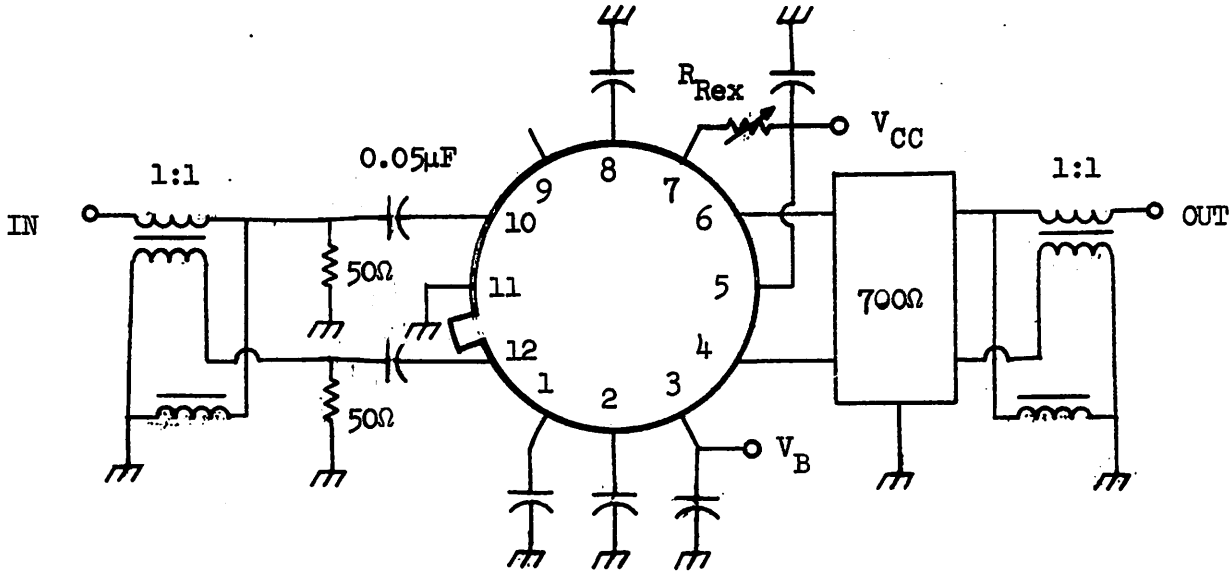

Figure B.3.

Measurement set-ups for the Improved Agc Amplifier (Figure 6.2)

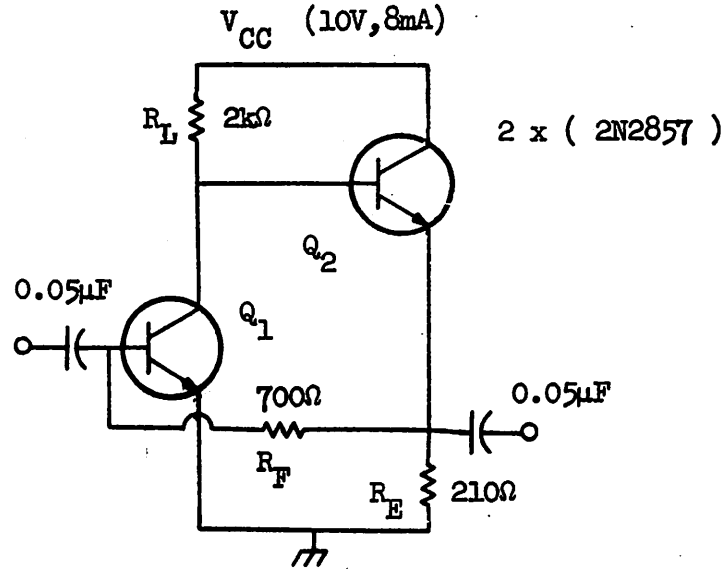

Figure C.1.

Circuit configuration for the 700 Ω Transresistance Amplifier.

(700 Ω transresistance) is used. The performance of this amplifier, which is represented in Figure B.4, is given in Appendix C.

The output signal of the output amplifier is analysed by a spectrum analyser (H.P. - 141 T, 8552 B, 8553 B). For measurement of intermodulation distortion, a hybrid junction (ANZAC H-8) is used instead of a power divider to combine the two input signals without intermodulation distortion.

APPENDIX C.

THE TRANSRESISTANCE AMPLIFIER.

The output amplifier (Figure C.1) used with the improved agc amplifier has the following properties. Its input and output impedances are very low because shunt-shunt feedback is employed. The output capacitance of the improved agc amplifier, which consists mainly of collector-substrate capacitance, then gives a very low time constant which is not dominant.

Shunt-shunt feedback stabilizes a transresistance with value approximately R_F if the loop gain T is high. The loop gain is given by

$$T = \frac{R_L}{r_\pi + R_F} \frac{1}{1 + R_e C_\pi s} \qquad \ldots (C1)$$

where

$$R_C = \frac{r_\pi R_F}{r_\pi + R_F} .$$

For the actual circuit of Figure C.1, the current in both transistors is about 4 mA and for $\beta = 100$, $T = 130$ at low frequencies. For $f_T = 2$ GHz, the break frequency is approximately 40 MHz. The input impedance is given by

$$Z_{in} = \frac{R_e}{T} (1 + R_e C_\pi s) \qquad \ldots (C2)$$

which equals 3.3 Ω at low frequencies and approximately 33 Ω at 400 MHz. This is sufficient to neutralize the effect of the output capacitance of the improved agc amplifier.

The bandwidth of the amplifier is limited by the time constant $C_\mu R_F$, where C_μ is the total collector-base capacitance of Q1 ($\simeq$ 0.85 pF). This yields 267 MHz for $R_F = 700\,\Omega$ but only 210 MHz was obtained experimentally.

REFERENCES.

1. B. Gilbert, " A New Wide-Band Amplifier Technique," IEEE J. Solid-State Circuits, Vol. SC-3, December 1968, pp. 353-365.

2. B. Gilbert, IEEE J. Solid State Circuits, Vol. SC-3, December, 1968, pp. 365-373.

3. W. R. Davis and J. E. Solomon, "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control," IEEE J. Solid-State Circuits, Vol. SC-3, December 1968, pp.408-416.

4. T. B. Mills and D. Bray, "An Integrated Circuit AGC IF Amplifier," Fairchild Semiconductor, TP-58, April 1970.

5. K. A. Simons, "The Decibel Relationships Between Amplifier Distortion Products," Proc. IEEE, Vol. 58, July 1970, pp. 1071-1086.

6. M. Riva, P. J. Beneteau and E. Dalla Volta, "Amplitude Distortion in Transistor Amplifiers," Proc. IEEE, Vol.3, No3, March 1964, pp. 481-490.

7. S. Narayanan, "Transistor Distortion Analysis Using Volterra Series Representation," Bell System Tech., J., Vol. 46, May-June 1967, pp. 991-1024.

8. W. M. C. Sansen and R. G. Meyer, "Characterization And Measurement Of The Base And Emitter Resistances Of Bipolar Transistors," IEEE J. Solid-State Circuits, Vol. SC-7, December 1972 (to be published).

9. J. L. Blue, "Three-Dimensional Small-Signal Analysis Of Bipolar Transistors," Bell Systems Tech., J., Vol. 51, No.4, April 1972, pp. 889-902.

10. F. S. Jenkins and S.-P. Fan, "TIME - A Nonlinear DC And Time-Domain Circuit-Simulation Program," IEEE J. Solid-State Circuits, Vol. SC-6, August 1971, pp. 182-188.

11. L. Nagel and R. Rohrer, "Computer Analysis Of Nonlinear Circuits, Excluding Radiation (CANCER)," IEEE J. Solid-State Circuits, Vol. SC-6, August 1971, pp. 166-182.

12. T.E.Idleman, F.S. Jenkins, W.J.McCalla and D.O.Pederson, "SLIC - A Simulator For Linear Integrated Circuits," IEEE J. Solid-State Circuits, Vol. SC-6, August 1971, pp. 188-203.

13. H.K.V. Lotsch, "Theory Of Nonlinear Distortion Produced In A Semiconductor Diode," IEEE Trans. Electron Devices, Vol. ED-15, May 1968, pp.294-307.

14. L. C. Thomas, "Eliminating Broadband Distortion In Transistor Amplifiers," Bell Syst. Tech., J., Vol. 47, March 1968, pp. 315-342.

15. E. M. Cherry and D. E. Hooper, "Amplifying Devices And Lowpass Amplifier Design," Wiley, 1968, Ch.8.

16. L. P. Hunter, "Handbook Of Semiconductor Electronics," McGraw-Hill, 1970; Section 19.

17. A. T. Starr, "Radio And Radar Techniques," Pitman, London, 1953, p. 416.

18. R. G. Meyer, M. J. Shensa and R. Eschenbach, "Cross Modulation And Intermodulation In Amplifiers At High Frequencies," IEEE J. Solid-State Circuits, Vol. SC-7, February 1972, pp. 16-23.

19. H. F. Cooke, "Microwave Transistors : Theory And Design," Proc. IEEE, Vol. 59, No. 8, August 1971, pp. 1163-1181.

20. R. M. Warner, J. N. Fordemwalt, "Integrated Circuits," New York: McGraw-Hill, 1965, Ch.3.

21. J. Addis, "Three Technologies On One Chip Make A Broadband Amplifier," Electronics, June 5, 1972, pp. 103-107.

22. E. M. Cherry and D. E. Hooper, "The Design Of Wide-band Transistor Feedback Amplifiers," Proc. IEEE, Vol. 110, No.2, February 1963, pp. 375-389.

23. D. A. Conrad, E. T. Yon and W. H. Ko, "A Micropower Monolithic Transmitter For Single-Or Multichannel Biomedical Telemetry," IEEE J. Solid-State Circuits, Vol. SC-7, April 1972, pp.120-124.