N-MOS OPERATIONAL AMPLIFIER STUDY

by

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Abstract

An all N-channel MOS operational amplifier has been designed and simulated using the integrated circuit simulation program ISPICE. The open loop gain is 86.3 db using only enhancement load devices, the amplifier is internally compensated and settles within 0.1% in 4.75 μsec loaded by 20 pF.

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Introduction

An all N-channel MOS operational amplifier has been designed and simulated using the integrated circuit simulation program ISPICE. The open loop gain is 86.3 db using only enhancement load devices, the amplifier is internally compensated and settles within 0.1% in 4.75 μsec loaded by 20 pF.

Design Philosophy

Considering only enhancement load devices the gain of an amplifying MOS stage is limited by low MOSFET transconductance.[1] One way to realize a high gain amplifier would be to use a positive feedback with a voltage transfer function $A_v = A_1/(1-A_2)$ where A_2 is close to one. This would of course result in undesired large gain variations and stability problems as a consequence of device mismatch, threshold voltage stability, carrier mobility dependence on temperature, etc.

Another way to achieve a high gain amplifier is cascading of several gain stages. Then the crucial problem is phase compensation of the amplifier. For high gain a very low dominant pole is necessary and therefore a pole splitting capacitor should be employed, otherwise a large external capacitor must be used.[2] The required pole splitting capacitor applied over one single stage would be still too large because of low gain. Besides it creates a dominant right-half plane zero due to the feedthrough and the low MOSFET transconductance.

The problem of phase compensation has been solved by applying the pole splitting capacitor over three stages and using a feedforward phase compensation to ensure the local stability. The feedforward amplifier provides a low-phase shift path at high frequencies to maintain frequency

stability.[3] The feedthrough has been prevented by feeding the signal back through a voltage follower.

Circuit Description

The transistors M25, M26, and M27 are connected as a voltage divider for circuit biasing. The scaling of the W/L ratios M25/M26/M27 is the same as M13/M14/M16 so that the ratios of voltage drops across these transistors are the same. Thus the power supply voltage sensitivity and the influence of threshold voltage stability have been minimized. By selecting the $\frac{W}{L}$ ratios M2/M1 and M3/M4 the same as M26/M27 the need for another voltage divider has been eliminated and the scaling has been preserved.

The transistors M10, M11, M12, M13, and M15 form a conventional differential input stage. The gain of this stage should be large to minimize the input offset voltage, the input stage should have large common-mode input voltage range, large common-mode rejection ratio, large bandwidth and low input capacitance. Since some of these requirements are contradictory, a compromise was necessary. M12 is a long channel device (22.5 mil/1.5 mil) to achieve high CMRR.

The following level shift stage M14, M16 is loaded by a large effective capacitance and so the positive transient is different from the negative one due to assymetrical loading of the input stage.

The next three stages M1, M2, M3, M4, M5, and M6 produce high gain. The pole splitting capacitor over these three stages has shifted the dominant pole to 100 Hz. The feedforward discussed above is provided by the transistor M7. The voltage follower M8, and M9 prevents the signal feedthrough.

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The output stage requires a different DC operating point for its linear operation. This is done by M23, M24, M17, and M18. The capacitor C_H cancells the left-half plane zero which occurs owing to the output impedance of the voltage follower M8 and M9.

A low output impedance and a large output swing are the main requirements for the output stage. Considering that such a MOS operational amplifier would be mainly used in large MOS circuits only a large capacitive load can be assumed. The shunt-shunt feedback gain block M19, M20, M21, and M22 satisfies both requirements mentioned above. The feedback transistor M20 lowers the output impedance by a factor $(\sqrt{50} + 1)$ and so the bandwidth is larger for capacitive loading. The positive output voltage swing is limited by V_T of M21, the negative is limited by V_T of M20 plus V_T of M22.

The MOS capacitors C_C, C_N, and C_H should have max. tolerance 2%.

Offset Voltage

The large offset voltage is the main problem of the MOS operational amplifier unless an offset cancellation scheme can be employed.

The input offset voltage due to the design is 1.5 mV. An estimation of the input offset voltage caused by the 2% device mismatch yields the standard deviation 75 mV.

The sensitivity of the input offset voltage to the threshold voltage V_{TO} is 12.6 mV/V.

Computer Simulation

The circuit was simulated using the NCSS program ISPICE, an interactive version of the SPICE 1 simulation program. The ISPICE program uses the NCSS MOSFET model, which is based on the Frohman-Bentchkowsky equations[4]

but with different effective mobility and channel-length modulation relations.[4] The effective mobility equation does not allow direct measurement of accurate parameters for the devices and hence these parameters were chosen for best-fit of the drain characteristics over the operating range of a particular transistor.

For modeling of MOS transistors in the MOS operational amplifier, the following parameters were determined empirically for the N-channel, metal gate process which is currently used in the Integrated Circuits Laboratory, Electronics Research Laboratory, U.C. Berkeley:

Parameter		Value	Measurement Unit
VTO	Zero-bias threshold voltage	0.2	V
PHI	Surface potential	0.7	V
RD	Drain ohmic resistance multiplied by unit channel width	0	Ω-cm
RS	Source ohmic resistance multiplied by unit channel width	0	Ω-cm
CO	Oxide capacitance	3.46×10^{-8}	F/cm
C1	Gate-source overlap capacitance/ unit channel width	15	pF
C2	Gate-drain overlap capacitance/ unit channel width	15	pF
CBD	Bulk-drain zero-bias capacitance/ unit channel width	45	pF
CBS	Bulk-source zero-bias capacitance/ unit channel width	45	pF
PB	Bulk junction potential	0.85	V
VMO	Field-dependent mobility parameters	∞	V
M	Field-dependent mobility exponent	1	
GAMMA	Bulk threshold parameter	0.91	$V^{1/2}$
LAMBDA	Channel length modulation parameter	3.3×10^{-5}	$cm/V^{1/2}$

The transconductance parameter BETA was varied according to estimated DC operating point:

V_{GS}	Model	BETA[$\mu A/V^2$]
less than 4.5 V	N1	13.55
4.5 V - 8 V	N2	11.8
8 V - 12.5 V	N3	10.3
12.5 V - 17.5 V	N4	9.7
more than 17.5 V	N5	8.35

Conclusion

The results of the simulation have shown that it is possible to realize a high gain all-MOS operational amplifier with enhancement loads only and internal compensation. However it is necessary to pay attention to high input offset voltage and low output driving capabilites for resistive loads.

A use of a N-channel silicon gate would represent one possible improvement because of smaller overlap capacitances.

A depletion load would increase the gain of a single stage so that less stages would be needed for a high gain amplifier. The input offset voltage would decrease if a high gain input stage were used. The output voltage swing would increase.

MOS Operational Amplifier: Electrical Characteristics

($V_{Supply} = \pm 15$ V, $V_{Body} = -20$ V, $R_{Load} = 0$

$R_{Source} \leq 1k\ \Omega$, $T_A = 25°C$)

Parameter	Conditions	Typ	Units
Open-loop voltage gain		86.3	dB
Unity gain bandwidth		1.8	MHz
Phase Margin	C_{Load}=0	50	degrees
Output Impedance	f=100Hz	500	Ω
Slew rate at unity gain	C_{Load}=20pF	6	V/μsec
Settling time 0.1% (unity gain)	$V_{IN\ STEP}=\pm 5V$, C_{Load}=0	4.5	μsec
	C_{Load}=20pF	4.75	μsec
	C_{Load}=50pF	6	μsec
Common-Mode rejection ratio		66.5	dB
Common-Mode input range		+10.5, -13.3	V
Output voltage swing		+10.5, -8.5	V
Power supply current		2.8	mA
Power consumption		84	mW
Power supply voltage rejection ratio		52.5	dB

References

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2. P.W. Fry, A MOST Integrated Differential Amplifier, IEEE JSSC, June 1969.

3. J. G. Graeme, G. E. Tobey and L. P. Muelsmann, Operational Amplifiers, Design and Applications, McGraw-Hill, New York, 1971, Chapter 5, pp.

4. ISPICE MOSFET Model Note, National CSS, Norwalk, Conn., June 1975.

CIRCUIT DIAGRAM OF MOS OPERATIONAL AMPLIFIER