MOS SAMPLED DATA RECURSIVE FILTERS

USING STATE VARIABLE TECHNIQUES

by

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ABSTRACT

A new technique to analog sampled data filtering is presented which can be fully integrated using MOS technology. Advantages of this new approach are reduced circuit complexity, low sensitivity to coefficient variations and efficient utilization of silicon area. Performance of monolithic low Q (Q=1) and high Q (Q=73) filters are presented which were implemented using NMOS technology. In implementing the high Q filter a new operational amplifier design was used which had a 14 V output range, rms noise voltage of 45 μV, an open loop gain of 6000 and a unity gain bandwidth of 2 MHz.

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CHAPTER 1

INTRODUCTION

One of the most common circuits in electronic systems are filters for frequency selective filtering. As large scale integration techniques are being used to integrate systems, it is becoming increasingly important to develop techniques to efficiently implement these filters. Since these applications often require a large number of filters on a single integrated circuit (IC) as well as circuitry to implement other system functions; it is desirable that the filters be fully integrated, require no trimming and use as little silicon circuit area as possible.

Conventional active filters which use a thin film or other hybrid technology, while being a significant advance over discrete component passive filters, do not meet any of the above requirements and are therefore not appropriate for the system LSI applications.

A more promising approach is the use of charge transfer devices (CTD) to implement analog sampled data transversal filters [1]. However, since CTD transversal filters have only zeros of transmission (no poles) in their transfer function, they are relatively inefficient in their use of silicon area in implementing simple frequency response functions: e.g., a narrow band pass response with a Q of 90, which can be implemented with a two pole recursive filter, requires five hundred CTD stages [2]. In addition, the large insertion loss experienced in CTD transversal filters, which is usually greater than 20 dB with non-destructive capacitive sensing, requires that a low noise output amplifier be used in order to obtain filter dynamic ranges in excess of 70 dB [3]. It is difficult to achieve the required level of noise performance with integrated MOS operational amplifiers.

Monolithic recursive filters have been implemented using analog sampled data techniques which do not have the above disadvantages. The output signal voltage in a recursive filter can be sensed directly (instead of capacitively) resulting in a larger signal and thus significantly relaxing the requirements on the noise performance of the amplifiers. Previous implementations of MOS analog sampled data recursive filters have used the conventional direct form of a second order section and even though this organization is widely used in digital filtering, the sensitivity of the filter frequency response to the values of the filter coefficients can be very high [4]. In general this is not an important disadvantage for a digital filter since it is only necessary to increase the number of bits used in quantization of the filter coefficients until adequate performance is achieved. However, it is important in an analog sampled data implementation, because there are physical limits to the achievable coefficient accuracy.

In this work new configurations of analog sampled data recursive filters will be presented which yield frequency responses that have a low sensitivity to the values of the filter coefficients [5,6]. In addition these new filters will be shown to need only a small amount of silicon area and require relatively low performance amplifiers.

These filters, which are based on conventional state variable filter design techniques, make use of switches, capacitors and operational amplifiers in a manner related to the "switched" filters that were investigated using discrete components in the late 1960's [7]. In this paper we will refer to these filters as switched capacitor filters. It will be found that the MOS technology is particularly well suited for implementing these filters for the following reasons: the high density

of MOS components (e.g., MOS operational amplifiers are 3-5 times smaller than their bipolar counterparts); the high precision and stability with which filter coefficients can be derived using ratios of capacitor values; and the essentially ideal characteristics of MOSFET switches.

CHAPTER 2

PRINCIPLES OF ANALOG SAMPLED DATA FILTERS

2.1. Sampled Data Systems

There is a wide variety of active filter techniques available to the linear active filter designer. Unfortunately most of these techniques have several disadvantages: (1) cost: typically four precision components (two resistors and two capacitors) are required for each complex pole pair, (2) sensitivity: the center frequency and bandwidth are often very sensitive functions of active gains or absolute values of feedback components, (3) complexity: these components can only be fabricated in integrated form using thin film or hybrid technology [8].

As shown in Chapter 1, one solution to this problem has been the use of sampled data techniques and digital filtering concepts (transversal and direct form recursive filters).

The basic difference between an analog and sampled data system is that the analog system processes a continuous time-varying physical quantity, e.g. voltage, while the sampled data system utilizes time samples of such a signal. The outputs of both systems are identical at the sampling points [9]. In a digital system these samples would have to be converted to a digital word by an analog-to-digital converter. Figure 2.1 illustrates the difference between these three systems.

The sampled data system consists of a sampler and an analog processor. As a result of the sampling process a set of time samples is obtained from a continuous input signal $x(t)$. The sample $x_s = x(mT_c)$ can be obtained by multiplying $x(t)$ by the appropriate unit impulse function, $\delta(t-mT_c)$. The sampled signal is then represented by the sample set,

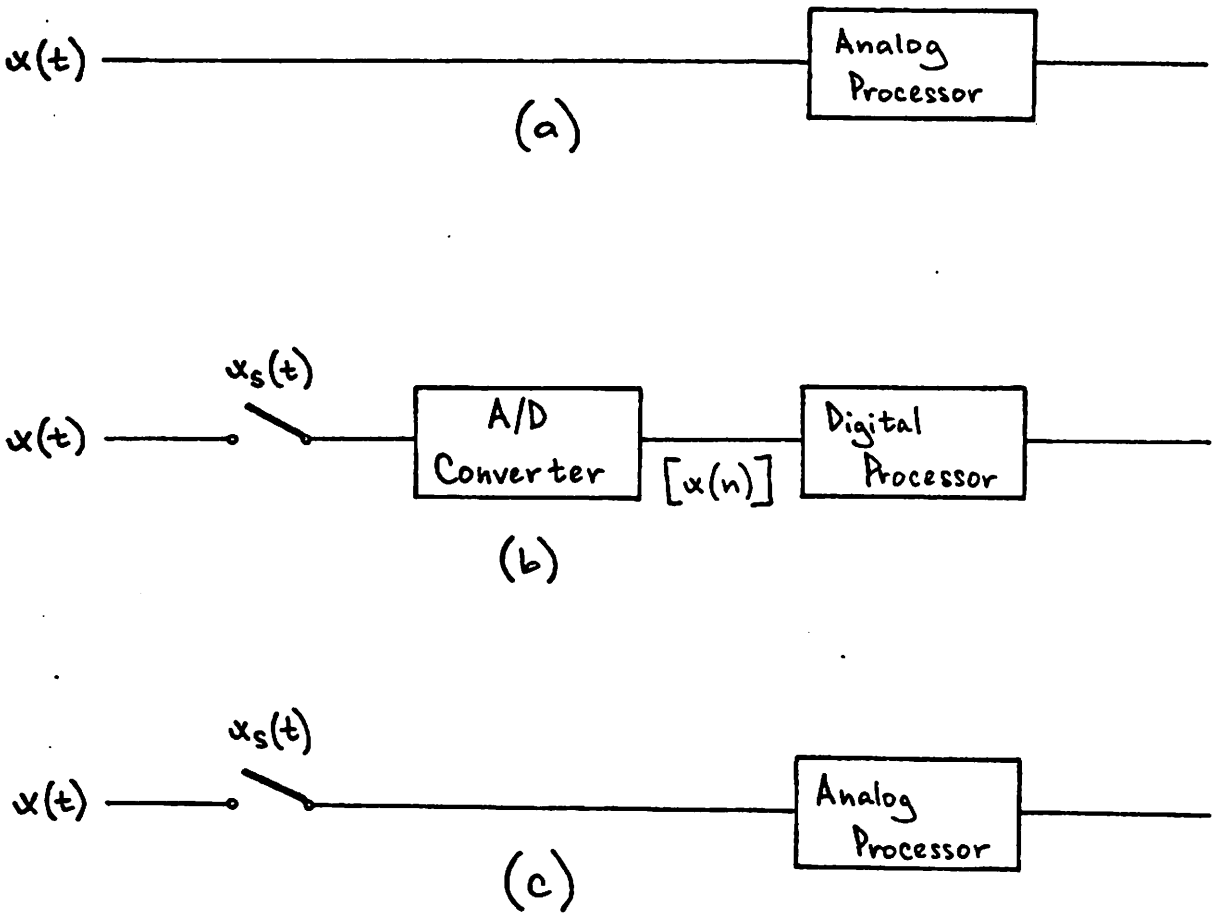


Figure 2.1: (a) Analog system
(b) Digital system
(c) Analog sampled data system

$$x_s(t) = \sum_{m=-\infty}^{\infty} x(t)\delta(t-mT_C) \tag{2.1}$$

in a continuous-time notation. In discrete-time notation this will look as follows:

$$x_s(nT_C) = \sum_{m=-\infty}^{\infty} x(mT_C)\ \delta[(n-m)T_C] \tag{2.2}$$

This can be written as

$$x(n) = \sum_{m=-\infty}^{\infty} x(m)\ \delta(n-m) \tag{2.3}$$

It is interesting to compare the Fourier transforms of x(t) and $x_s(nT_C)$:

$$X(\omega) = \int_{-\infty}^{\infty} x(t)e^{-j\omega t}\, dt \tag{2.4}$$

$$X_s(\omega) = \sum_{n=-\infty}^{\infty} x(nT_C)e^{-j\omega nT_C} \tag{2.5}$$

The latter can be written as follows:

$$X_s(\omega) = \frac{1}{T_C} \sum_{n=-\infty}^{\infty} X(\omega + \frac{2\pi n}{T_C}) \tag{2.6}$$

where $\frac{2\pi}{T_C} = \omega_c = 2\pi f_c$.

It can be seen from Eq. (2.4) and (2.6) that the discrete Fourier transform $X_S(\omega)$ is a superposition of an infinite number of shifted Fourier transforms $X(\omega)$ [9]. The result is shown in Fig. 2 for a case where X(f) is bandlimited at f_N. If the sampling rate f_c is greater than $2f_N$ then it is possible to recover the continuous signal x(t) from the sampled one simply by filtering out the shifted spectra (see Fig. 2.2b).

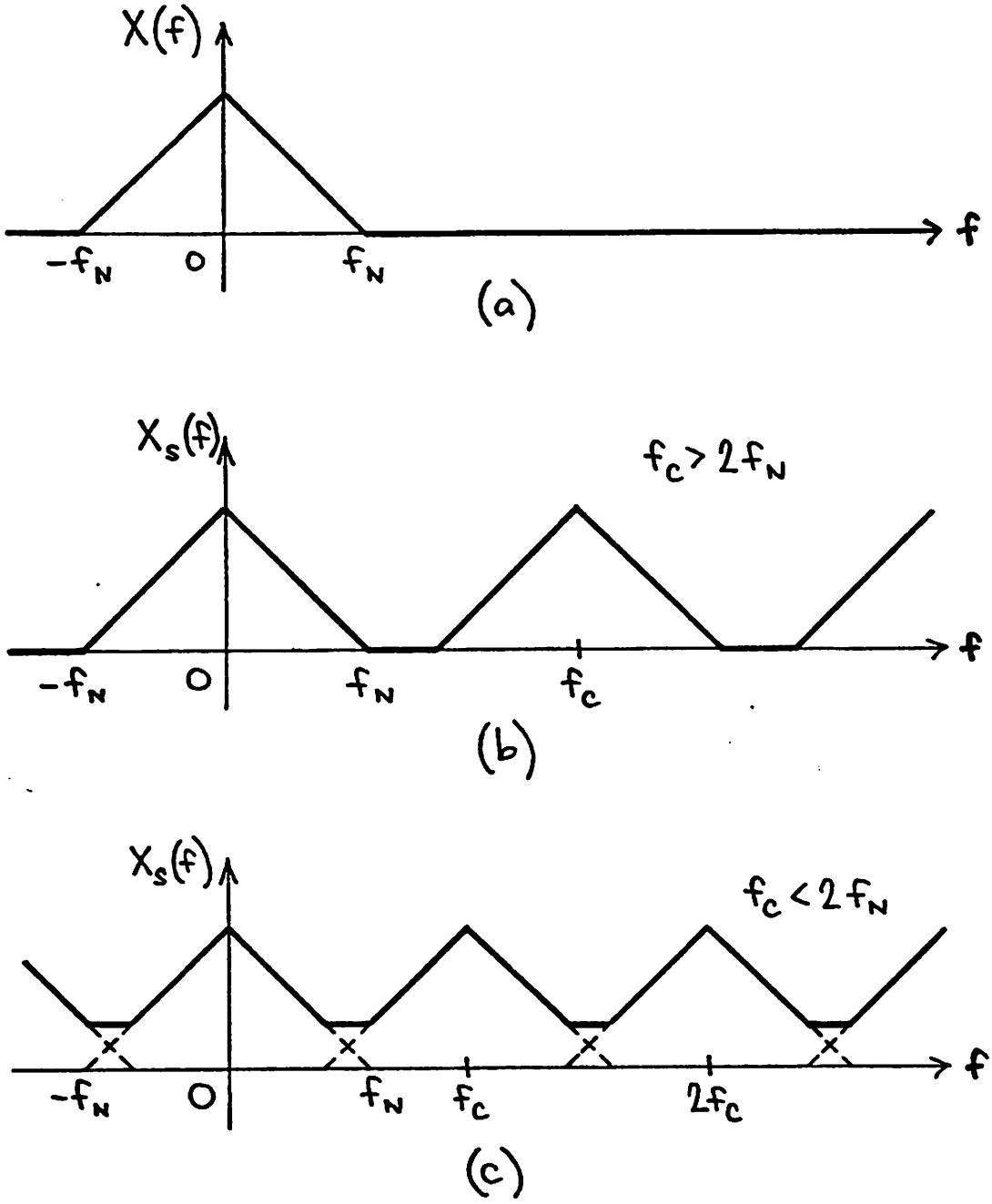


Figure 2.2: (a) The Fourier spectrum of a continuous signal
(b) The Fourier spectrum of a sampled signal with a sample rate of $f_C > 2f_N$
(c) The Fourier spectrum for a sample rate of $f_C < 2f_N$

If the sample rate is lower than $2f_N$ as shown in Fig. 2.2.c, then the shifted spectra overlap and x(t) cannot be recovered without distortion. This effect is called aliasing.

A suitable prefilter which limits the bandwidth of the input signal to half the sampling rate (so that $f_N = f_C/2$ is needed to avoid aliasing (so called antialiasing filter).

2.2. The z-Transform

A common representation of the sample set is so called z-transform, defined as follows: The z-transform of any complete set [x(n)] of regular samples of a function x(t) is

$$X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-1} \tag{2.7}$$

From Eq. (2.5) we see that if the z-transform is evaluated on a unit circle $z = e^{j\omega T_C}$ we find

$$X(z)\Big|_{z=e^{j\omega T_C}} = X(e^{j\omega T_C}) = \sum_{n=-\infty}^{\infty} x(n)e^{-j\omega n T_C} \tag{2.8}$$

which is the Fourier transform of the sequence x(n). An ample discussion of the basic properties of the z-transform can be found in literature [9,10,11,12]. Three important properties that are going to be used in this work will be briefly discussed in the next three sections.

2.2.1. Linearity

The z-transform is linear: the z-transform of $ax_1(n) + bx_2(n)$ is $aX_1(z) + bX_2(z)$ for all real a and b. $X_1(z)$ is the z-transform of $x_1(n)$ and $X_2(z)$ is the z-transform of $x_2(n)$.

2.2.2. Delays

If x(n) has z-transform X(z), then x(n-k) has the z-transform $z^{-k}X(z)$ for all k. Thus a difference equation can be easily converted into the z-transform domain. E.g., the difference equation

$$y(n) = x(n) - ay(n-1) - by(n-2) \tag{2.9}$$

has a z-transform representation

$$Y(z) = X(z) - az^{-1}Y(z) - bz^{-2}Y(z) \tag{2.10}$$

where Y(z) is the z-transform of y(n).

2.2.3. Convolution

If x(n) is the input to a discrete-time linear system with unit impulse response h(n) and y(n) is the output [see Fig. 2.3a], then

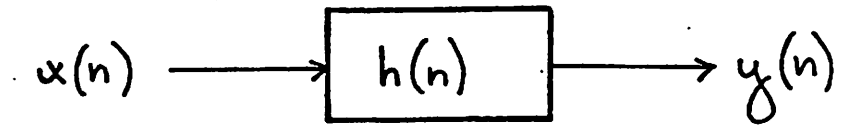
$$Y(z) = X(z)\ H(z) \tag{2.11}$$

where X(z), H(z), and Y(z) are the respective z-transforms of x(n), h(n), and y(n). We have assumed that the system is time-invariant, i.e., if the input sequence x(n) produces an output sequence y(n), then the input sequence x(n-k) produces the output sequence y(n-k) for all k. From Eq. (2.10) and (2.11) we can write

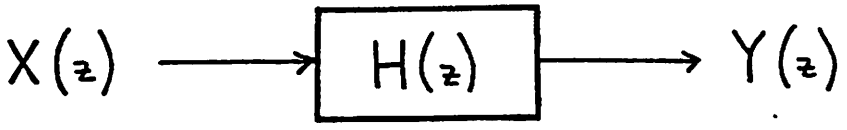
$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{1+az^{-1}+bz^{-2}} \tag{2.12}$$

2.3. Principles of Discrete Time Filtering

Our discussion in Section 2.1 indicates that both concepts of discrete time filtering, i.e. analog sampled data technique and digital



(a)



(b)

Figure 2.3: (a) Linear time-invariant system
(b) z-transform representation of a

filters, are related because they work with discrete time signals. The difference is the processor implementation which is analog in the case of analog sampled data filters and digital in the case of digital filters. Thus as far as we do not discuss the implementation, the discrete time filter theory applies to both concepts.

As an introduction to discrete time filtering, a discrete time version of a continuous time single pole, RC filter will be analyzed [13]. Figure 2.4a shows such a filter. The relation between the continuous time input and output voltages is given by

$$V_{out}(t) = V_{in}(t) - RC \frac{dV_{out}(t)}{dt} \tag{2.13}$$

For the discrete time version of this filter it is necessary to replace the continuous time derivative in Eq. (2.13) with the finite difference form of a derivative, i.e.

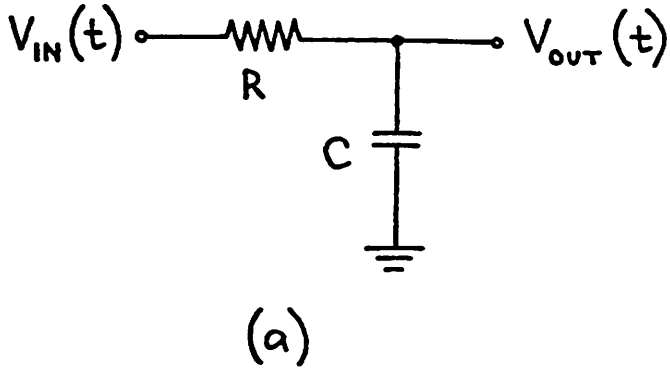
$$\frac{dV_{out}(t)}{dt} \Rightarrow \frac{V_{out}[nT_C]-V_{out}[(n-1)T_C]}{T_C} \tag{2.14}$$

where $V_{out}[(n-1)T_C]$ and $V_{out}[nT_C]$ are two adjacent time samples of the output voltage. When this substitution is carried out the original differential equation (2.13) is converted into the difference equation:

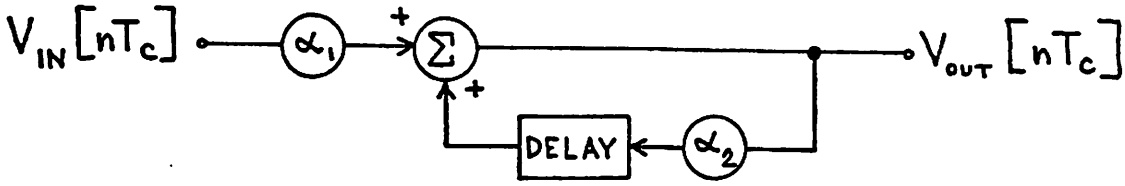
$$V_{out}[nT_C] = \frac{T_C}{T_C+RC} V_{in}[nT_C] + \frac{RC}{T_C+RC} V_{out}[(n-1)T_C] \tag{2.15}$$

Using $\alpha_1 = \frac{T_C}{T_C+RC}$ and $\alpha_2 = \frac{RC}{T_C+RC}$ the Eq. (2.15) simplifies to

$$V_{out}[nT_C] = \alpha_1 V_{in}[nT_C] + \alpha_2 V_{out}[(n-1)T_C] \tag{2.16}$$



(a)



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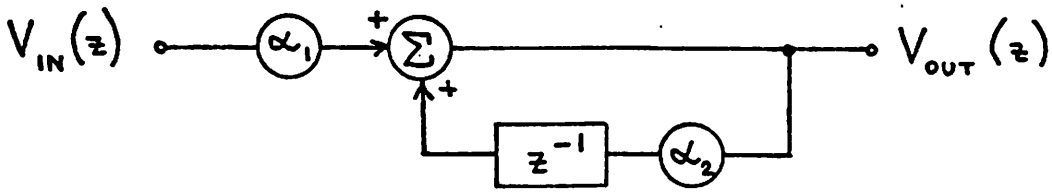


(c)

Figure 2.4: (a) Continuous time single pole RC lowpass filter
(b) Discrete time version of a
(c) z-transform representation of b

Figure 2.4b shows the implementation of Eq. (2.16). It has been shown in the Section 2.2.2 how a difference equation can be converted into a z-transform:

$$V_{out}(z) = \alpha_1 V_{in}(z) + \alpha_2 z^{-1} V_{out}(z) \tag{2.17}$$

Similarly as in Eq. (2.12), the z-transform of this filter can be expressed as a rational polynomial in z^{-1}; i.e.,

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{\alpha_1}{1-\alpha_2 z^{-1}} \tag{2.18}$$

As noted in Section 2.2, the substitution $z = e^{j\omega T_C}$ will lead to the discrete time filter transfer function

$$H_s(\omega) = \frac{\alpha_1}{1-\alpha_2 e^{-j\omega T_C}} = \frac{1}{1 + \frac{RC}{T_C}(1-e^{-j\omega T_C}} \tag{2.19}$$

For comparison the transfer function for the continuous time filter is

$$H(\omega) = \frac{1}{1+j\omega RC} \tag{2.20}$$

For very high sampling rate $f_c >> 1$, i.e. $T_C << 1$, $e^{-j\omega T_C}$ can be replaced by $(1-j\omega T_C)$. Then equations (2.19) and (2.20) are identical and therefore at low frequencies, $f << f_c$, the two filters yield the same response. However, at higher frequencies there is a significant deviation in the two responses since the discrete time filter response is periodic with a period equal to the sampling period $T_C = 1/f_c$.

This can be seen when we analyze the mapping from the z-plane into the s-plane. By definition

$$z = e^{sT_C} \tag{2.21}$$

where $s = \sigma+j\omega$. Then s can be expressed as

$$s = \frac{1}{T_C} \ln(z) = \frac{1}{T_C} \ln(Re^{j(\theta\pm 2\pi n)}) = \frac{1}{T_C} \ln(R) + \frac{j}{T_C} (\theta\pm 2\pi n) \qquad (2.22)$$

From here we obtain

$$\omega = \frac{1}{T_C} (\theta\pm 2\pi n) \qquad (2.23)$$

or

$$f = \frac{1}{T_C} (\frac{\theta}{2\pi} \pm n) \qquad (2.24)$$

where n = 0,1,2,3,... . This periodicity is characteristic for all discrete time filters.

2.4. Discrete Time Filter Structures

As discussed in the last chapter, the z-transform of a discrete time filter can be expressed as a rational polynomial in z^{-1}. A general expression is

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{\sum_{m=0}^{N} a_m z^{-m}}{\sum_{m=0}^{N} b_m z^{-m}} \qquad (2.24)$$

where $b_o = 1$. The corresponding difference equation is

$$V_{out}(n) = \sum_{m=0}^{N} a_m V_{in}(n-m) - \sum_{m=1}^{N} b_m V_{out}(n-m) \qquad (2.25)$$

A simple realization of this difference equation is shown in Fig. 2.5a. This represents the most general linear discrete time filter which can be realized using summers, multipliers and delay elements according to our difference equation. The Eq. (2.25) contains two kinds of terms: feedback terms determined by coefficients b_m and feed forward term

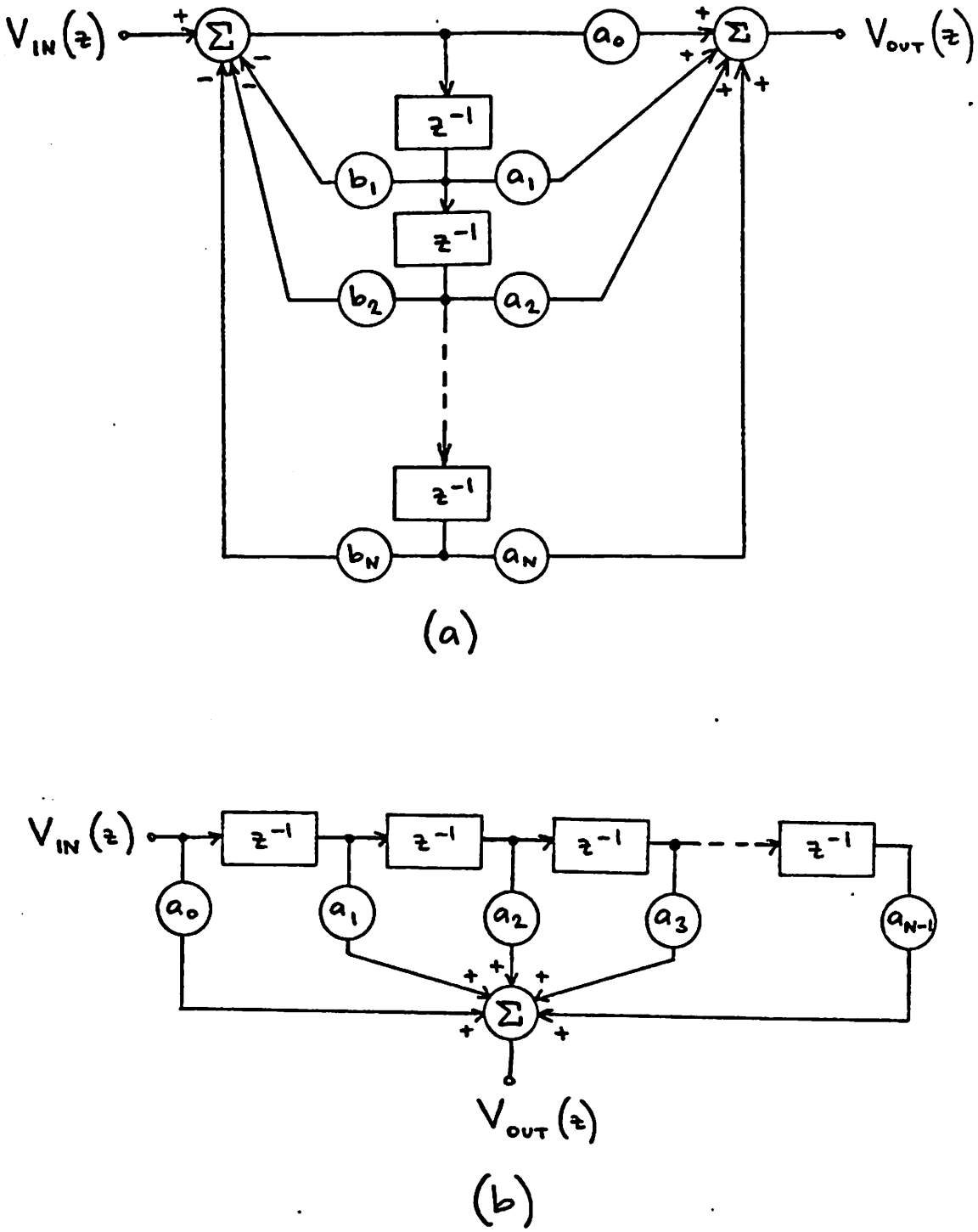


Figure 2.5: (a) Recursive (IIR) filter
(b) Transversal (FIR) filter

determined by a_m. A filter which contains any feedback terms is called a recursive or infinite impulse response (IIR) filter.

If the difference equations contains only feedforward coefficients a_m, then we obtain a transversal or finite impulse response (FIR) filter (Fig. 2.5b). Similarly to the recursive filter the z-transform and the difference equations are

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \sum_{m=0}^{N} a_m z^{-m} \tag{2.26}$$

$$V_{out}(n) = \sum_{m=0}^{N} a_m V_{in}(n-m) \tag{2.27}$$

The impulse response of a transversal filter is [14]:

$$V_{out}(t) = \sum_{m=0}^{N} h_m \delta(t-mT_C) \tag{2.28}$$

From Eq. (2.27) and (2.28) it can be seen that $h_m = a_m$, i.e. the impulse response h_m is equal to the weighting coefficients a_m. FIR filter can be very easily implemented using CTD technology. Some advantages and disadvantages of these filters are discussed in Chapter 1.

More discussion on comparison of IIR and FIR filters can be found in literature [10,12].

2.5. Relationship between s-plane and z-plane Poles

We have discussed a first-order discrete time filter in Section 2.3 the transfer function of which is given by Eq. (2.18). The pole of this function in the z-plane is

$$z = \alpha_2 \tag{2.29}$$

The question arises as to how the corresponding pole in the s-plane can be found. Using Eq. (2.21) we find

$$\alpha_2 = e^{pT_C} \tag{2.30}$$

where p is the pole in the p-plane. The position of the pole is determined by the sampling rate f_c and the coefficient α_2:

$$p = f_c \ln(\alpha_2) \tag{2.31}$$

Let us recall for a moment the original continuous time filter discussed in Section 2.3, from which our discrete time filter was derived. The analogy between these two filters was based on $\alpha_2 = RC/(T_C+RC)$. If this is substituted in Eq. (2.31) we get

$$p = \frac{1}{T_C} \ln\left(\frac{RC}{T_C+RC}\right) \tag{2.32}$$

For high sampling rate, i.e. $T_C << RC$, it can be shown that

$$\ln\left(\frac{RC}{T_C+RC}\right) \approx \frac{RC}{T_C+RC} - 1 \approx -\frac{T_C}{RC} \tag{2.33}$$

Thus we obtain

$$p \approx -\frac{1}{RC} \tag{2.34}$$

which is the pole of the continuous time filter (see Eq. (2.20)). Figure 2.6 shows the pole in both planes.

Let us focus our attention on a second-order system. This will be useful later on when we will be investigating second-order lowpass filters. A second-order continuous time transfer function that realizes a lowpass characteristic is

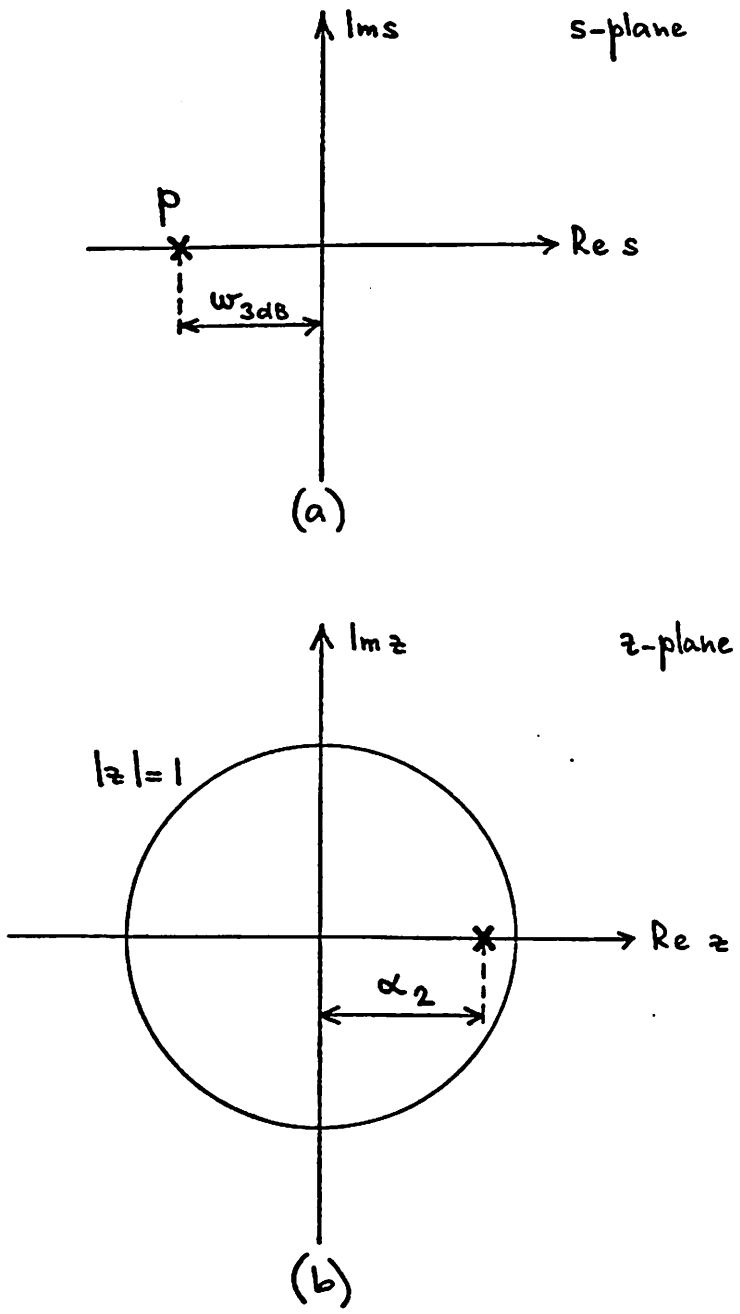


Figure 2.6: (a) Pole of a 1st-order system in the s-plane
(b) Pole of a 1st-order system in the z-plane

$$H(s) = \frac{K_1}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \tag{2.35}$$

The poles are complex conjugate roots of the denominator which are given by

$$s_{1,2} = \omega_o\left[-\frac{1}{2Q} \pm j\sqrt{1-\left(\frac{1}{2Q}\right)^2}\right] \tag{2.36}$$

where ω_o and Q are the center frequency and selectivity of the filter respectively. The 3 dB bandwidth is given by

$$\Delta f = \frac{f_o}{Q} \tag{2.37}$$

The complex conjugate poles of Eq. (2.35) in the s-plane are shown in Fig. 2.7a.

Complex poles can be realized either using passive RLC networks or active RC networks. The latter ones contain an active element, usually an operational amplifier. If the input signal to such an active filter is increased, the output continues to increase until eventually the output waveform becomes clipped because the amplifier saturates. On the other hand, the minimum input signal level should be large enough to maintain all signal levels above the noise voltage. Thus we define the dynamic range as the ratio of the maximum usable output voltage to the noise output voltage [20]. Since the output voltage depends on the filter transfer function, the dynamic range depends on the noise voltage, the output swing of the operational amplifier and the frequency characteristics of the active filter.

Let us consider the magnitude of the function given by Eq. (2.35):

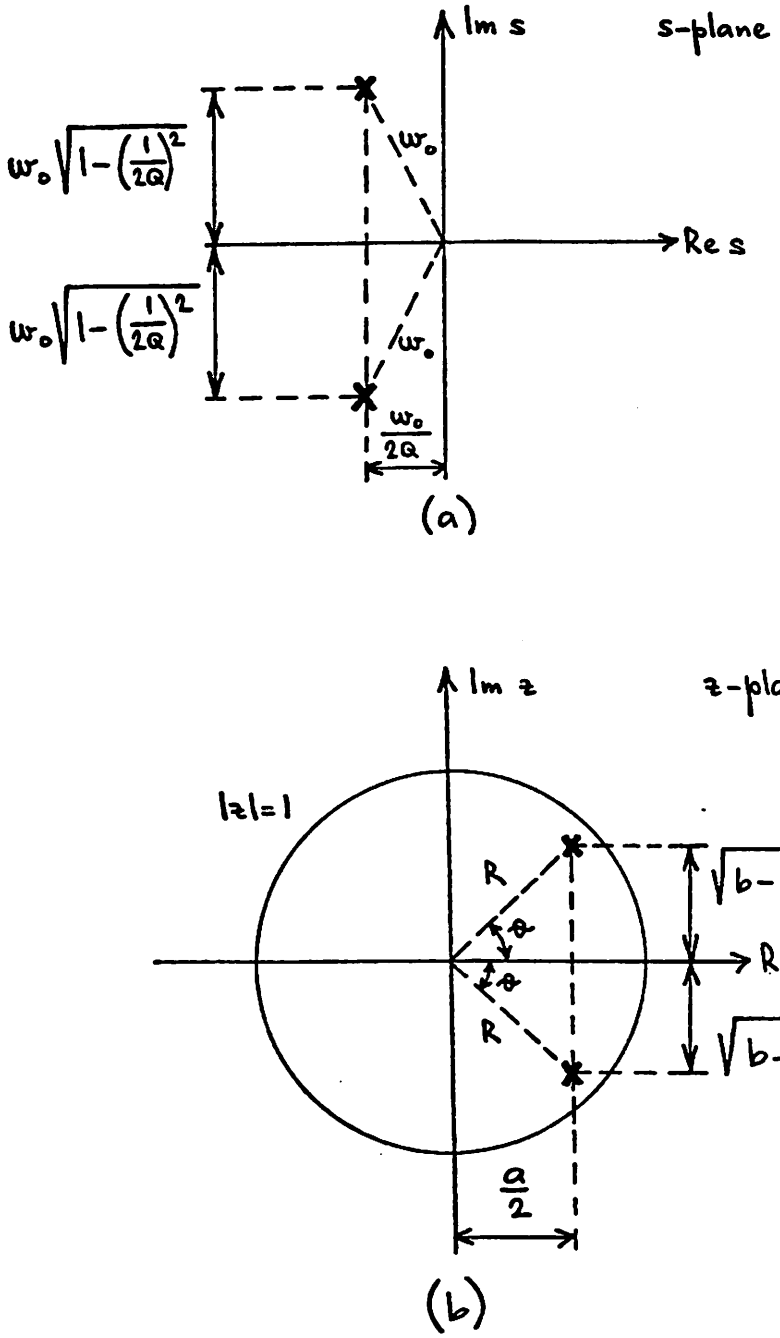


Figure 2.7: (a) Complex conjugate poles of a 2nd-order system in the s-plane

(b) Complex conjugate poles in the z-plane

$$|H(\omega)| = \frac{K_1}{\sqrt{(\omega_o^2-\omega^2)^2+(\frac{\omega\omega_o}{Q})^2}} \tag{2.38}$$

The peak frequency, i.e. the frequency at which the magnitude achieves a maximum is obtained by equating the derivative of $|H(w)|$ to zero:

$$\frac{d|H(\omega)|}{d\omega} = 0 \tag{2.39a}$$

Solving this equation we obtain

$$\omega_p = \omega_o\sqrt{1 - \frac{1}{2Q^2}} \tag{2.39b}$$

and the magnitude is

$$H_{max} = |H(\omega=\omega_p)| = \frac{2K_1Q}{\omega_o^2\sqrt{4 - \frac{1}{Q^2}}} \tag{2.39c}$$

Note that for high Q filters

$$\omega_p \simeq \omega_o \tag{2.40a}$$

and

$$|H(\omega=\omega_p)| \cong |H(\omega=\omega_o)| \tag{2.40b}$$

where

$$|H(\omega=\omega_o)| = \frac{K_1Q}{\omega_o^2} \tag{2.41a}$$

It can be seen from Eq. (2.39) and (2.41) that the dynamic range can be a problem for high Q filters since the max. magnitude of the signal is proportional to Q. Furthermore it can be seen that the max. magnitude

appears approximately at the center frequency ω_0 for high Q.

For low Q filters, ω_p will more towards $\omega=0$ and the max. magnitude will be close to

$$|H(\omega=0)| = \frac{k_1}{\omega_0^2} \tag{2.41b}$$

We shall now turn our attention to sampled data filters. The z-transform of a second-order lowpass filter would be

$$H(z) = \frac{K_2}{z^2-az+b} \tag{2.42}$$

The poles of this polynomial are

$$z_{1,2} = \frac{a}{2} \pm j\sqrt{b-(\frac{a}{2})^2} \tag{2.43}$$

If R is the distance of the poles from the origin of the z plane and θ is the angle of the poles it can be readily shown that (see Fig. 2.7b)

$$a = 2R \cos \theta \tag{2.44}$$

and

$$b = R^2 \tag{2.45}$$

Thus we obtain the canonical equation for a second order lowpass filter

$$H(z) = \frac{K_2}{z^2-2zR \cos \theta+R^2} \tag{2.46}$$

Referring to Eq. (2.21) and (2.36) it can be found that

$$z = \exp\{\omega_0 T_c[-\frac{1}{2Q} \pm j\sqrt{1-(\frac{1}{2Q})^2}]\} = [\exp(-\frac{\omega_0 T_c}{2Q})]$$

$$[\cos(\omega_0 T_c\sqrt{1-(\frac{1}{2Q})^2}) \pm j \sin(\omega_0 T_c\sqrt{1-(\frac{1}{2Q})^2})] \tag{2.47}$$

A comparison of R from Eq. (2.45) and (2.47) yields

$$|z| = e^{-\frac{\omega_o T_C}{2Q}} = R = \sqrt{b} \tag{2.48}$$

The selectivity is then

$$Q = -\frac{\omega_o T_C}{\ln(b)} = -\frac{2\pi f_o}{f_c \ln(b)} \tag{2.49}$$

Similarly the comparison of R cos θ (Eq. (2.44) and (2.47)) gives

$$\text{Re } z = \frac{a}{2} = e^{-\frac{\omega_o T_C}{2Q}} \cos\left(\omega_o T_C \sqrt{1-\left(\frac{1}{2Q}\right)^2}\right) = \sqrt{b} \cos\left(\omega_o T_C \sqrt{1-\left(\frac{1}{2Q}\right)^2}\right) \tag{2.50}$$

After some manipulation we get

$$\omega_o = \frac{1}{T_C}\sqrt{\left(\frac{1}{2}\ln(b)\right)^2 + \left(\arccos\frac{a}{2\sqrt{b}}\right)^2} \tag{2.51}$$

The center frequency is

$$f_o = \frac{\omega_o}{2\pi} = \frac{f_c}{2\pi}\sqrt{\left(\frac{1}{2}\ln(b)\right)^2 + \left(\arccos\frac{a}{2\sqrt{b}}\right)^2} \tag{2.52}$$

Using the polar coordinates for the selectivity and center frequency we obtain following expressions:

$$Q = -\frac{\pi f_o}{f_c \ln(R)} \tag{2.53a}$$

$$f_o = \frac{f_c}{2\pi}\sqrt{\theta^2 + (\ln(R))^2} \tag{2.53b}$$

When Eq. (2.53b) is substituted in Eq. (2.53a), it becomes clear, that Q is independent of the clock rate:

$$Q = -\frac{\sqrt{\theta^2 + (\ln(R))^2}}{2\ln(R)} \tag{2.54}$$

while f_o scales with the clock rate. For poles close to the unit circle (i.e. for $f_o << f_c$ and $Q >> 1$) R will be close to 1 and log R will be very small. Then the Eq. (2.53b) can be written as

$$f_o \approx \frac{\theta f_c}{2\pi} \tag{2.55}$$

and the Eq. (2.54) is reduced to

$$Q \approx -\frac{\theta}{2\ \ln(R)} \tag{2.56a}$$

Because R is close to 1 the approximation $\ln(R) \approx R-1$ can be used and thus

$$Q \approx \frac{\theta}{2(1-R)} \tag{2.56b}$$

When looking for the dynamic range of the sampled data filter (Eq. (2.42)), we are going to assume that the max. magnitude again appears at the center frequency f_o as was the case of the continuous time filter. Furthermore we assume that the poles are close to the unit circle. Then

$$z\Big|_{\omega=\omega_o} = e^{j\omega_o T_C} = e^{j\theta} \tag{2.57}$$

and the max. magnitude is given approximately by

$$|H(e^{j\theta})| = \frac{K_2}{|e^{2j\theta}-2e^{j\theta}R\cos\theta+R^2|} \tag{2.58a}$$

Using

$$R \approx 1 - \frac{\theta}{2Q} \tag{2.58b}$$

from Eq. (2.56) and

$$R^2 \approx 1 - \frac{\theta}{Q} \tag{2.58c}$$

we find that

$$|H(e^{j\theta})| = \frac{QK_2}{\theta \sin \theta} \tag{2.58d}$$

Because sin $\theta \approx \theta$ for high sampling rate our final result is

$$H_{max} \approx \frac{QK_2}{\theta^2} \tag{2.58e}$$

For low Q filters, the max. magnitude will be close to the DC value:

$$|H(e^{j\theta=1})| = K_2 \tag{2.59}$$

CHAPTER 3

ANALOG SAMPLED DATA RECURSIVE FILTERS USING STATE VARIABLE TECHNIQUES

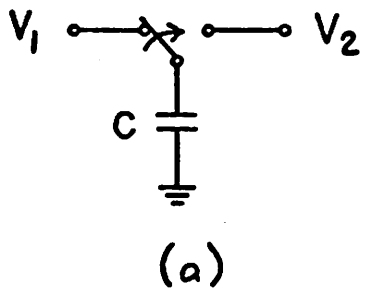
3.1. Switched Capacitor "Resistors"

A major reason that active filters have not previously been fully integrated in MOS technology is the necessity of accurately defining resistance-capacitance products, which requires that the absolute value of the resistors and capacitors be well controlled. In addition, integrated (diffused) resistors have poor temperature and linearity characteristics as well as requiring a large amount of silicon area.

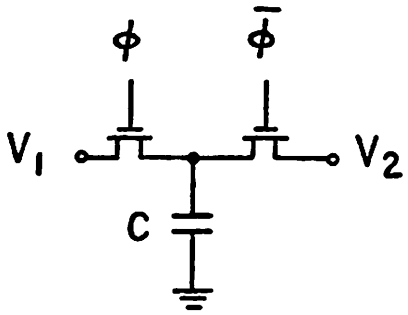
A circuit that performs the function of a resistor which does not have these disadvantages has been investigated independently by several workers [5, 15] and is shown in Fig. 3.1a. The operation of this "resistor" is as follows: the switch is initially in the left hand position so that the capacitor C is charged to the voltage, V_1. The switch is then thrown to the right and the capacitor is discharged to the voltage, V_2. The amount of charge which flows into (or from) V_2 is thus $Q = C(V_2-V_1)$. If the switch is thrown back and forth every T_c seconds, then the current flow, i, into V_2 will be

$$i = \frac{C(V_2-V_1)}{T_c} \tag{3.1}$$

Thus the size of an equivalent resistor which would perform the same function as this circuit is $R = T_c/C$. If the switching rate, $f_c = 1/T_c$, is much larger than the signal frequencies of interest then the time sampling of the signal which occurs in this circuit can be ignored and the switched capacitors can then be considered as a direct replacement for a conventional resistor. If, however, the switch rate and signal frequencies



(a)



(b)

Figure 3.1: (a) A "resistor" implemented using a switched capacitor
(b) MOS implementation of a

are of the same order then sampled data techniques are required for analysis and, as for any sampled data system, the input signal should be band-limited below $f_c/2$ as dictated by the sampling theorem.

The MOS realization of the circuit of Fig. 3.1a is shown in Fig. 3.1b. The two MOSFETs are operated as switches which are pulsed with a two phase non-overlapping clock (ϕ and $\bar{\phi}$) at a frequency f_c. The stability and linearity of the resistance value, $R = 1/(f_c C)$, is much better than that obtained from diffused resistors, since the insulator in a properly fabricated MOS capacitor has essentially ideal characteristics. For example, typical temperature coefficients for these capacitors are less than 10 ppm [16]. Another important advantage of the switched capacitor resistors is the high accuracy of RC time constants that can be obtained with their use. If a capacitor, C_1, which is switched at a clock rate of f_c is connected to a capacitor, C_2, the resultant time constant of this RC network, τ_{RC}, is

$$\tau_{RC} = \left(\frac{1}{f_c C_1}\right) C_2 = \frac{1}{f_c}\left(\frac{C_2}{C_1}\right) \tag{3.2}$$

For a given clock rate the value of τ_{RC} is therefore determined by a ratio of capacitor values which makes it insensitive to most processing variations.

The relative values of the capacitors C_1 and C_2 are determined by photolithographic definition of their area. Since the capacitance per unit area is uniform across an IC it is possible to achieve high precision in the capacitor ratio. It has been shown that the error in such ratios can be less than 0.1% using standard MOS processing techniques [16]. In addition the stability of this ratio is extremely high since to first order there is no temperature dependence in the capacitance ratio. It is thus apparent that the switched capacitor resistor of Fig. 3.1 makes

it possible to design precise stable RC active filters which can be fully integrated using MOS technology.

3.2. State Variable Technique

The problem of implemehting active filters in MOS technology has thus been reduced to a question of what kind of an active filter should be used. The state variable synthesis method [17] has the dual advantages of a very low sensitivity to coefficient values as well as only requiring relatively low performance operational amplifiers.

State variable filters are derived from analog simulation techniques used in analog computers. The basic building block of these computers is an operational amplifier connected as an integrator [18]. A state-variable network configuration is illustrated in Fig. 3.2a. The voltage transfer function has the form

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a_0+a_1s+\ldots+a_{N-2}s^{N-2}+a_{N-1}s^{N-1}+a_Ns^N}{b_0+b_1s+\ldots+b_{N-2}s^{N-2}+b_{N-1}s^{N-1}+6_Ns^N} \tag{3.3}$$

A slightly different configuration for a second-order lowpass filter is shown in Fig. 3.2b. The transfer function is

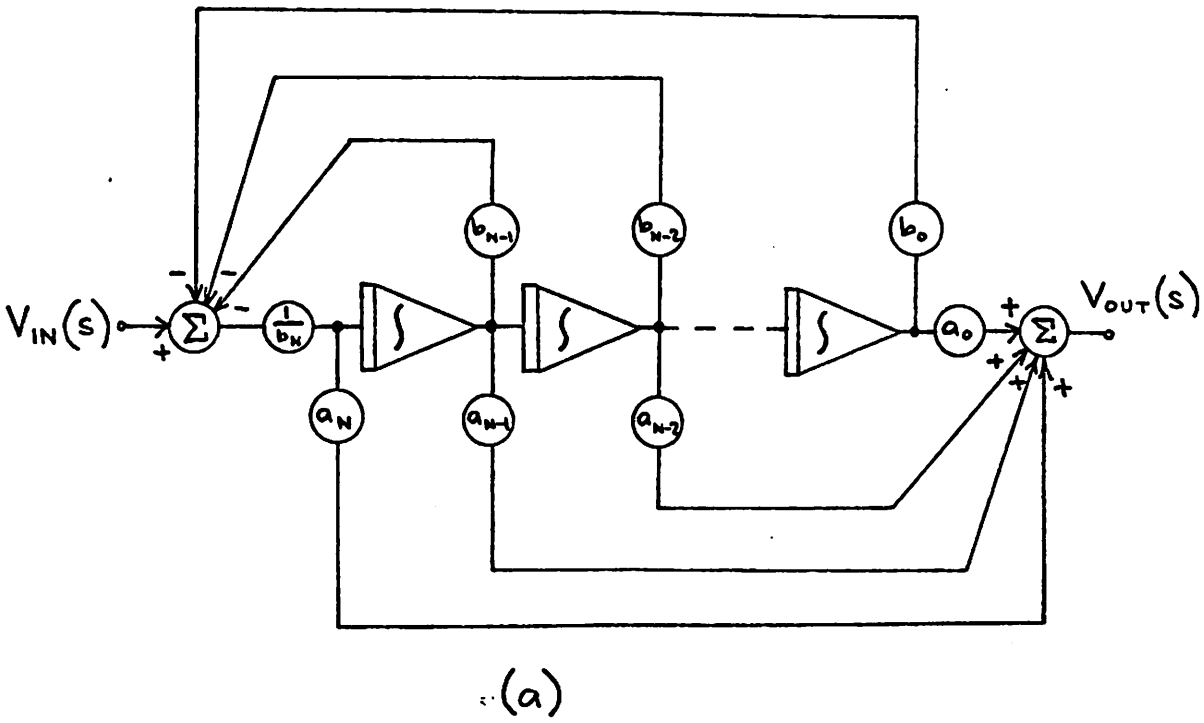
$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a_0b_1b_2}{s^2+sb_1+b_1b_2} \tag{3.4}$$

Comparison with Eq. (2.35) yields the following filter characteristics:

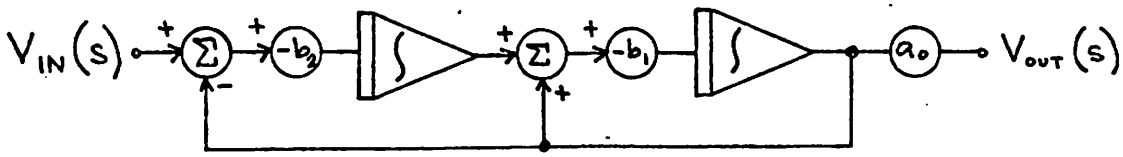
$$\omega_0 = \sqrt{b_1b_2} \tag{3.5}$$

$$Q = \sqrt{\frac{b_2}{b_1}} \tag{3.6}$$

$$K_1 = a_0b_1b_2 \tag{3.7}$$



(a)



(b)

Figure 3.2: (a) State variable network configuration
(b) Second-order lowpass filter in state variable technique

3.3. Filter Sensitivity

Now we will turn our attention to sensitivity of the transfer function parameters to filter element changes. E.g., the fractional change in the center frequency w_0 for a given fractional change in b_1 is given by

$$\left|\frac{\Delta\omega_0}{\omega_0}\right| = S_{b_1}^{\omega_0} \left|\frac{\Delta b_1}{b_1}\right| \tag{3.8}$$

The sensitivity of w_0 with respect to b_1 is then

$$S_{b_1}^{\omega_0} = \left|\frac{\partial\omega_0}{\partial b_1}\right| \left|\frac{b_1}{\omega_0}\right| \tag{3.9}$$

For the case of the filter from Fig. 3.2b described in the last section:

$$S_{b_1}^{\omega_0} = S_{b_2}^{\omega_0} = \frac{1}{2} \tag{3.10}$$

$$S_{b_1}^{Q} = \frac{1}{2} \tag{3.11}$$

$$S_{b_2}^{Q} = \frac{1}{2} \tag{3.12}$$

Equations (3.11) and (3.12) suggest that it is possible to achieve low sensitivity even for high Q state-variable filters.

Let us investigate sensitivity of first-order sampled data systems. Consider again the circuit from Fig. 3.3a. It has been shown (Eq. (2.31)) that the 3 dB cut-off frequency for this filter was

$$\omega_{3dB} = -f_c \ln(\alpha_2) \tag{3.13}$$

The sensitivity of ω_{3dB} with respect to α_2 is then

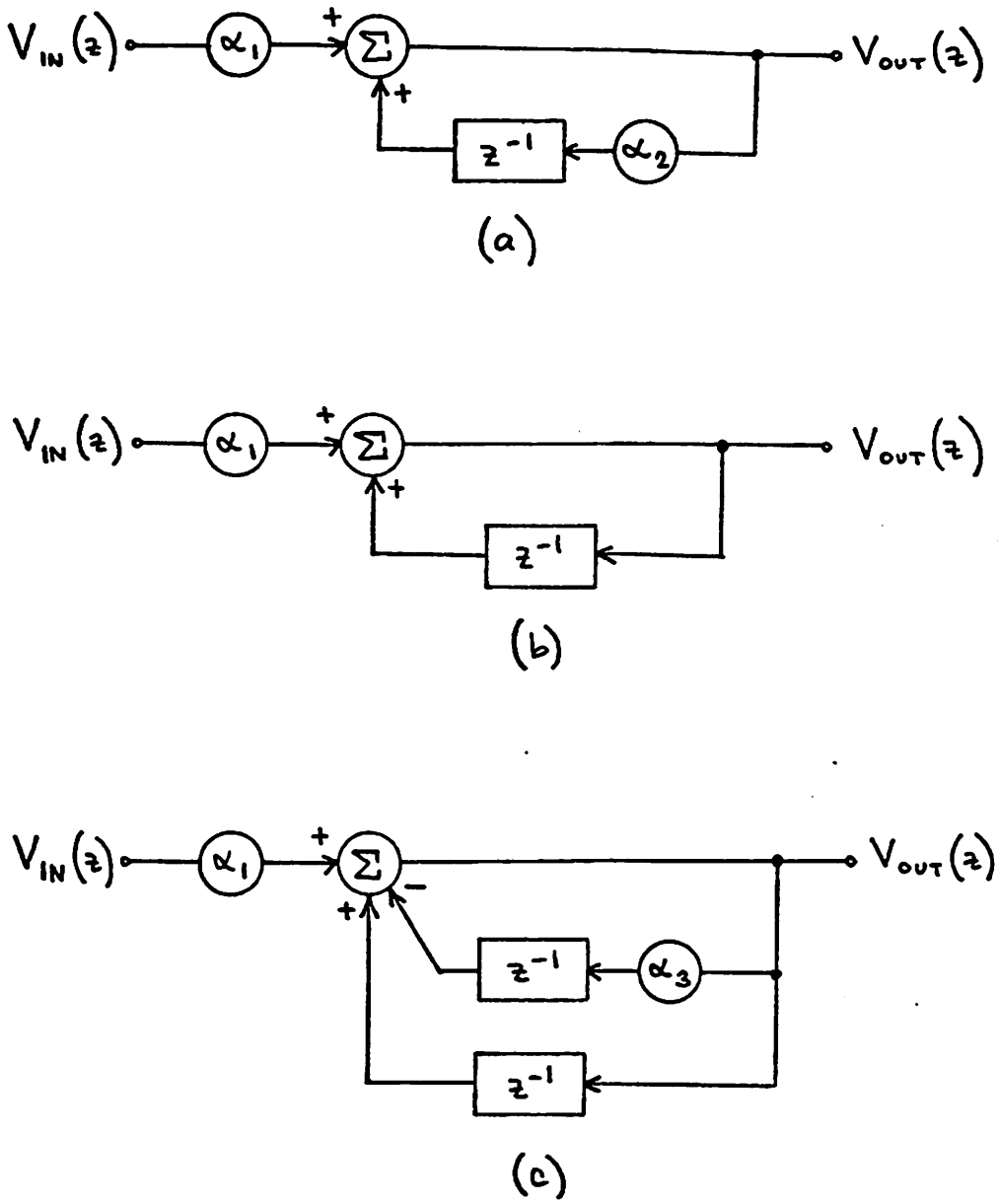


Figure 3.3: (a) Sampled data 1st-order lowpass filter
(b) Sampled data integrator
(c) 1st-order lowpass filter using sampled data integrator

$$S_{\alpha_2}^{\omega_{3dB}} = \left| \frac{1}{\ln(\alpha_2)} \right| \tag{3.14}$$

This expression shows what can be obviously extended to higher order recursive sampled-data filters as well: the higher clock rate f_c is chosen when designing the filter the higher the sensitivity of filter parameters will be: from Eqs. (3.13) and (3.14) we obtain for a first-order system

$$S_2^{\omega_{3dB}} = \left| \frac{f_c}{\omega_{3dB}} \right| \tag{3.15}$$

The sensitivity $S_2^{\omega_{3dB}}$ will be large for a pole close to the unit circle. To minimize sensitivity, the designer would have to select sufficiently low clock rate f_c; the roll-off of the antialiasing prefilter (see Chapter 2.1) should be then very sharp. In the next part we are going to show that the sensitivity is inversely proportional to the clock rate for sampled-data recursive filters in state-variable technique and thus it is decreasing for increasing f_c. This relaxes requirements on the antialiasing prefilter: the prefilter can be then very simple with only a gradual roll-off and it can be realized with a small number of external low-precision elements.

The basic element of state-variable filters is an integrator as noted before. Figure 3.3.b shows a block diagram of a sampled data integrator. The integrator performs two basic functions: it multiplies samples of the input voltage by a constant factor α_1 and stores all samples with delay T_c. Mathematically expressed in z-transform this looks as follows:

$$V_{out}(z) = \alpha_1[1 + z^{-1} + z^{-2} + z^{-3} + \ldots]V_{in}(z) \tag{3.16}$$

The transfer function is then

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{\alpha_1}{1-z^{-1}} \tag{3.17}$$

A first-order recursive lowpass filter using the sampled data integrator (Fig. 3.3c) has then the z-transform

$$H(z) = \frac{\alpha_1}{1-(1-\alpha_3)z^{-1}} \tag{3.18}$$

This filter which we will now call a recursive state-variable filter has the z-transform similar to the one for the filter discussed above (Eq. (2.18)) however α_2 has been replaced by $(1-\alpha_3)$. To illustrate the advantage of the state-variable technique we shall calculate the 3 dB cut-off frequency which is now

$$\omega_{3dB} = -f_c \ln(1-\alpha_3) \tag{3.19}$$

and the sensitivity of ω_{3dB} with respect to α_3 is

$$S_{\alpha_3}^{\omega_{3dB}} = \frac{\alpha_3}{1-\alpha_3} \left| \frac{1}{\ln(1-\alpha_3)} \right| \tag{3.20}$$

For a pole close to the unit circle α_3 will be very small. When the original design equation (3.19) is substituted back into Eq. (3.20) we find

$$S_{\alpha_3}^{3dB} = (e^{\frac{\omega_{3dB}}{f_c}} - 1) \frac{f_c}{\omega_{3dB}} \tag{3.21}$$

For high clock rate we approximate

$$e^{\frac{\omega_{3dB}}{f_c}} \approx 1 + \frac{\omega_{3dB}}{f_c} \tag{3.22}$$

and we find

$$S_{3}^{\omega_{3dB}} \approx 1 \tag{3.23}$$

Figure 3.4 shows filter coefficients and sensitivities as functions of $\frac{\omega_{3dB}}{f_c}$ for filters we have just discussed. We can conclude that for high clock rate ($\frac{\omega_{3dB}}{f_c} << 1$)

$$S_{\alpha_3}^{\omega_{3dB}} << S_{\alpha_2}^{\omega_{3dB}} \tag{3.24}$$

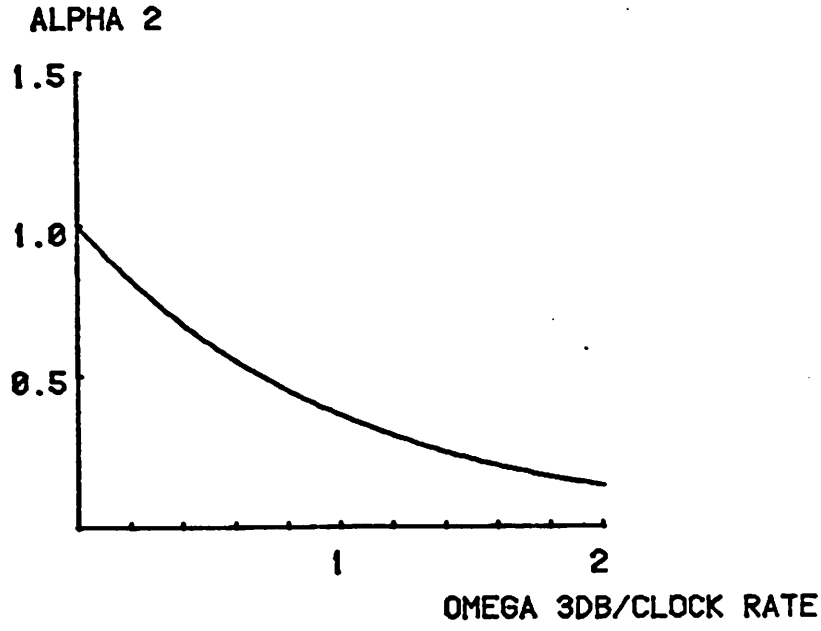
and therefore the state-variable recursive filter (Fig. 3.3c) is a better choice for a system with high f_c.

3.4. Sampled Data Integrators

As mentioned above the basic building block of state variable filters is an operational amplifier connected as an integrator as shown in Fig. 3.5a. The transfer function of this integrator is

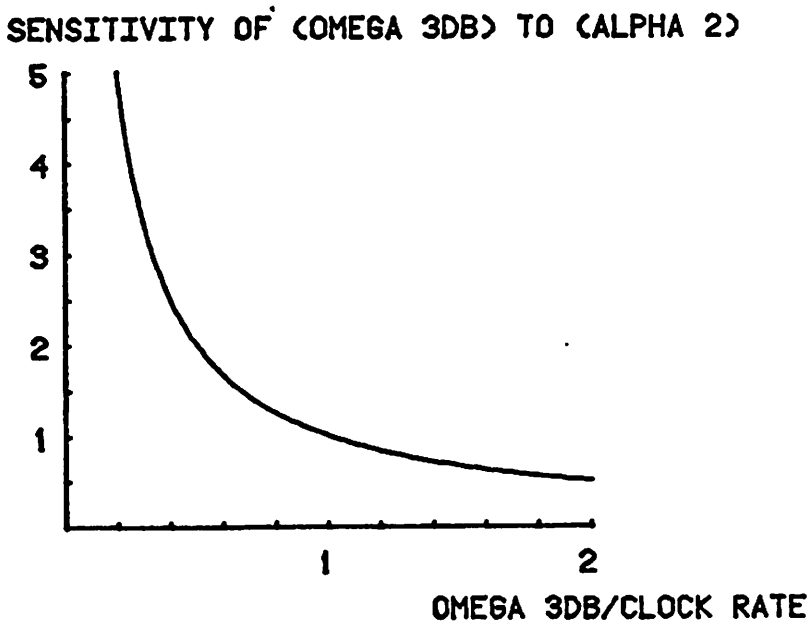
$$H(\omega) = -\frac{1}{j\omega R_1 C_2} \tag{3.25}$$

In Fig. 3.5.b the resistor, R_1, in the integrator has been replaced by the switched capacitor circuit of Fig. 3.1a with $C_1 = 1/f_c R_1$. In the n^{th} clock period, the capacitor C_1 is charged to the voltage $V_{in}(nT_c)$ and then after the switch is thrown to the right, is discharged by the operational amplifier. The charge $C_1 V_{in}(nT_c)$ is thus effectively transferred from C_1 to the feedback capacitor C_2. Taking into account the delay of one clock



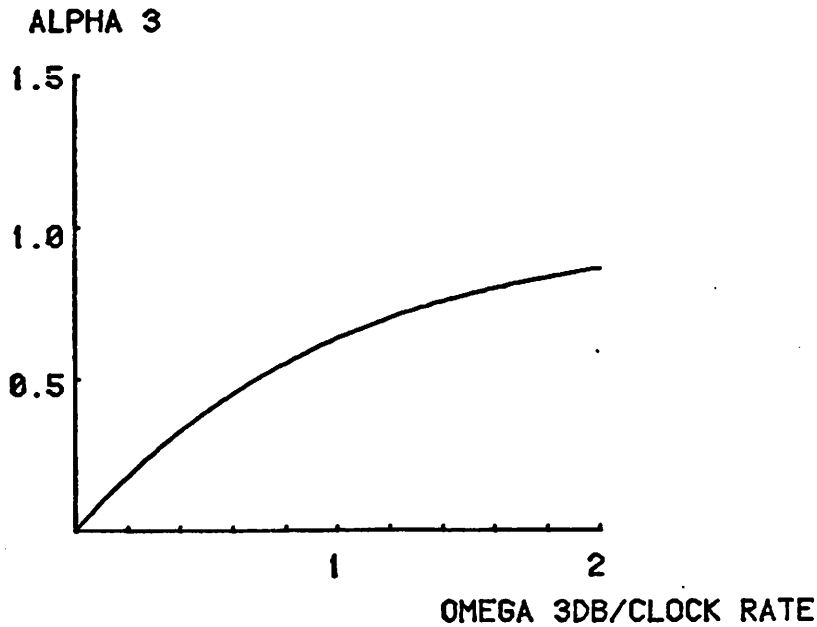
(a)

Figure 3.4.a: Coefficient α_2 as a function of ω_{3dB}/f_C for filter from Fig.3.3.a



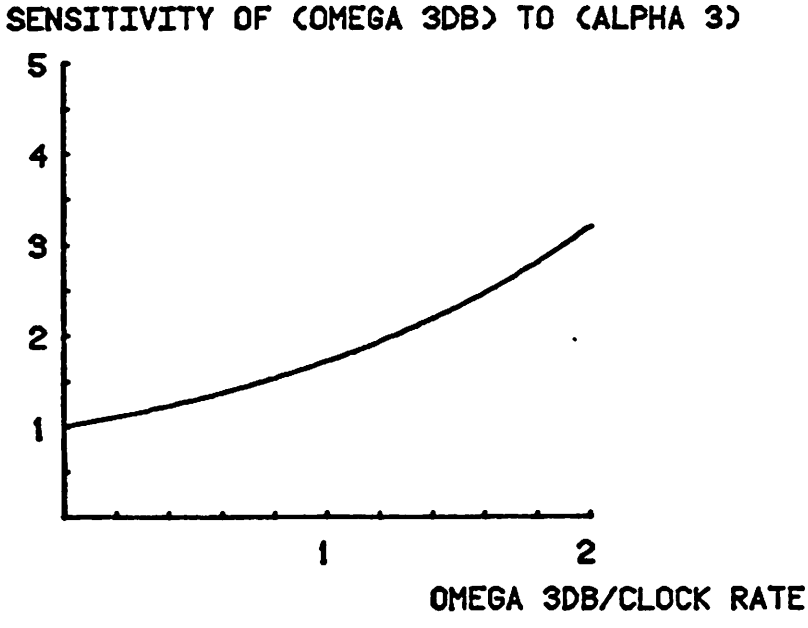
(b)

Figure 3.4.b: Sensitivity $S_{\alpha_2}^{\omega_{3dB}}$ as a function of ω_{3dB}/f_C for filter from Fig.3.3.a



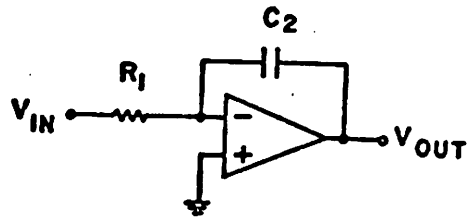
(c)

Figure 3.4.c: Coefficient α_3 as a function of ω_{3dB}/f_C for filter from Fig.3.3.c

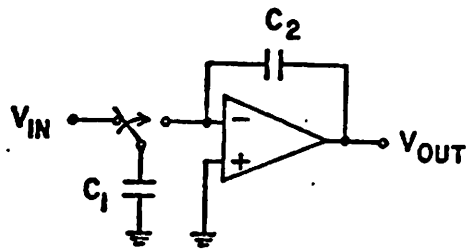


(d)

Figure 3.4.d: Sensitivity $S_{\alpha_3}^{\omega_{3dB}}$ as a function of ω_{3dB}/f_C for filter from Fig.3.3.c



(a)



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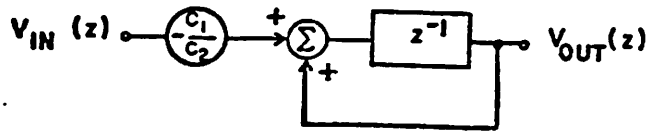


(c)

Figure 3.5: (a) A conventional integrator
(b) A sampled data integrator
(c) z-transform block diagram of integrator in b

period introduced by the switching process results in the following charge conservation equation:

$$C_2V_{out}[nT_c] = C_2V_{out}[(n-1)T_c] - C_1V_{in}[(n-1)T_c] \tag{3.26}$$

Since this is a sampled data system, the z-transform technique should be used, which yields the transfer function

$$H(z) = \frac{-(C_1/C_2)z^{-1}}{1-z^{-1}} \tag{3.27}$$

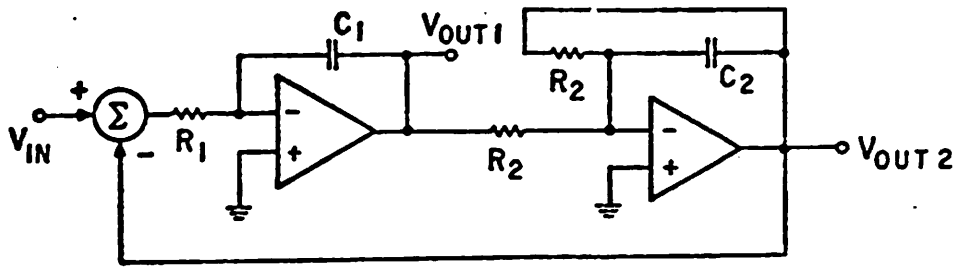
A block diagram of the z-transform interpretation of this integrator is shown in Fig. 3.5c. If a high clock rate ($f_c \gg \frac{\omega}{2\pi}$) is assumed then z can be approximated by $1 + j\omega T_c$ which when substituted into Eq. (3.27) yields Eq. (3.25) as exprected, i.e., if the capacitor, C_1, is switched fast enough then it is equivalent to a resistor.

3.5. Second Order Filters

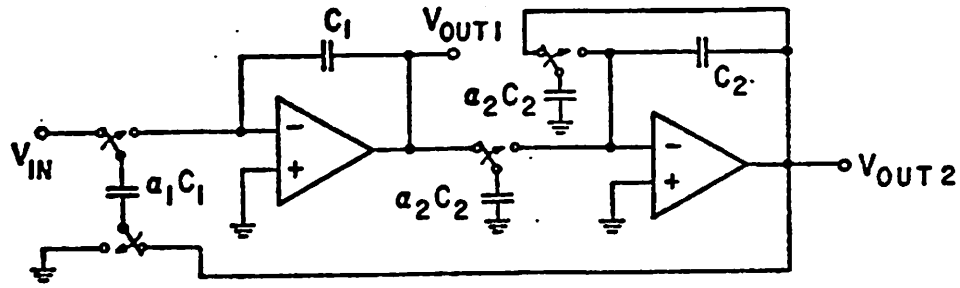
There are many possible circuit organizations using state variable design techniques which can be used to implement two poles. In this section four different versions will be presented and the advantages and disadvantages of each with respect to sensitivity, the size of the capacitor ratios and circuit complexity will be discussed.

3.5.1. Version 1

The conventional circuit for realizing a pair of complex poles using state variables filters is shown in Fig. 3.6a. This is the realization of the circuit from Fig. 3.2b. A straightforward replacement of the resistors in this circuit with switched capacitors yields the circuit shown in Fig. 3.6b. Since each integrator is inverting, the negative feedback around both integrators requires an additional inversion. In



(a)



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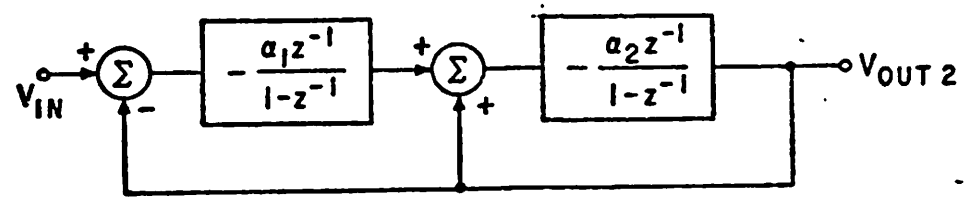


(c)

Figure 3.6: (a) A conventional state variable filter
(b) Sampled data version of a
(c) z-transform block diagram of b

Fig. 3.6b this is achieved by feeding the output back into the bottom plate of the $\alpha_1 C_1$ capacitor. The charge introduced into the first integrator is thus $(V_{in}-V_{out})\alpha_1 C_1$ and the necessary sign inversion has been accomplished. The second integrator has a local feedback obtained through the switched capacitor $\alpha_2 C_2$. As in conventional state variable filters both bandpass (i.e., the transfer function has a zero near zero frequency) and lowpass filter characteristics are available at the outputs V_{out1} and V_{out2}, respectively. The z-transform block diagram of this filter is shown in Fig. 3.6c. It is interesting to note that this block diagram is the same as a digital filter structure which was developed for low coefficient sensitivity [19]. The transfer function for the bandpass filter output at V_{out1} is

$$\frac{V_{out1}(z)}{V_{in}(z)} = \frac{\alpha_1[(1-\alpha_2)-z]}{z^2-(2-\alpha_2)z+(1+\alpha_1\alpha_2-\alpha_2)} \tag{3.28}$$

where α_1 and α_2 are the capacitor ratios defined in Fig. 3.6b. The lowpass filter output at V_{out2} has the transfer function

$$\frac{V_{out2}(z)}{V_{in}(z)} = \frac{\alpha_1\alpha_2}{z^2-(2-\alpha_2)z+(1+\alpha_1\alpha_2-\alpha_2)} \tag{3.29}$$

The position of the poles in the z-plane can be determined by comparing to the canonical equation for a second order filter (see Eq. (2.46))

$$H(z) = \frac{1}{z^2-2zR\cos\theta+R^2} \tag{3.30}$$

where R and θ are the polar coordinates in the z-plane of the two poles. Then the following formulas are valid (see Eq. (2.53))

$$f_0 = \frac{f_c}{2\pi}\sqrt{\theta^2+\ln^2(R)} \tag{3.31a}$$

$$Q = -\frac{\pi f_0}{f_c \ln(R)} \tag{3.31b}$$

where f_0 and Q are the center frequency and selectivity respectively. From Eqs. (3.28), (3.29), (3.30) and (3.31) the following design formulas can be derived

$$\alpha_2 = 2[1-e^{-\frac{\pi f_0}{Qf_c}}\cos(\frac{\pi f_0}{f_c}\sqrt{4-\frac{1}{Q^2}})] \tag{3.32}$$

$$\alpha_1 = 1 + \frac{1}{\alpha_2}(e^{-\frac{2\pi f_0}{Qf_c}} - 1) \tag{3.33}$$

Since it is assumed that no trimming of component values will be performed it is necessary to investigate the sensitivity of f_0 and Q to variations in α_1 and α_2 to determine the required accuracy of these ratios. For $f_0 << f_c$ and $Q >> 1$, the sensitivity of the center frequency, f_0, to α_2 is approximately

$$S^{f_0}_{\alpha_2} = \left|\frac{\partial f_0}{\partial \alpha_2}\right| \frac{\alpha_2}{f_0} \cong (\frac{f_c}{2\pi f_0})\sin(\frac{\pi f_0}{f_c}) \tag{3.34}$$

The sensitivity thus can be reduced to 0.5 (i.e., $\pm$1% tolerance in α_2 yields $\pm$0.5% variation in f_0) by increasing the clock rate so that $f_0 << f_c$. Similar sensitivity results are found to hold for Q. The highest sensitivity is the Q sensitivity of α_1 which is approximately given by

$$S^{Q}_{\alpha_1} = 2\pi\frac{f_0 Q}{f_c} \tag{3.35}$$

Therefore for high Q filters the clock rate required to obtain low

sensitivity may be very high.

To find the dynamic range of this filter, first we simplify Eq. (3.32) and (3.33) for poles close to the unit circle:

$$\alpha_2 \approx \theta(\theta + \frac{1}{Q}) \tag{3.36a}$$

$$\alpha_1 \approx 1 - \frac{1}{\theta Q} \tag{3.36b}$$

and then use Eq.

$$\left|\frac{V_{out2}}{V_{in}}\right|\Bigg|_{z=e^{j\theta}} = \frac{\alpha_1\alpha_2 Q}{\theta \sin \theta} \approx Q[1 - \frac{1}{(\theta Q)^2}] \tag{3.37}$$

This is the max. magnitude of the signal at the lowpass filter output. We should check the bandpass output as well:

$$\left|\frac{V_{out1}}{V_{in}}\right|\Bigg|_{z=e^{j\theta}} = \frac{Q\alpha_1[(1-\alpha_2)-e^{j\theta}]}{\theta \sin \theta} \tag{3.38a}$$

Because $\cos \theta \approx 1 - \frac{\theta^2}{2}$ and $\sin \theta \approx \theta$ for small θ it can be written

$$|(1-\alpha_2)-e^{j\theta}| \approx \theta \tag{3.38b}$$

and thus

$$\left|\frac{V_{out1}}{V_{in}}\right|\Bigg|_{z=e^{j\theta}} = \frac{\alpha_1\theta Q}{\theta \sin \theta} \approx \frac{Q}{\theta}(1 - \frac{1}{\theta Q}) \tag{3.38c}$$

An interesting concept which could lead to programmable filters is shown in Fig. 3.7a. It is similar to the filter from Fig. 3.6b, but the capacitor $\alpha_1 C_1$ is being switched at a clock rate f_{c1} and $\alpha_2 C_2$ are switched at a different clock rate f_{c2}. The lowpass output at V_{out2} has the

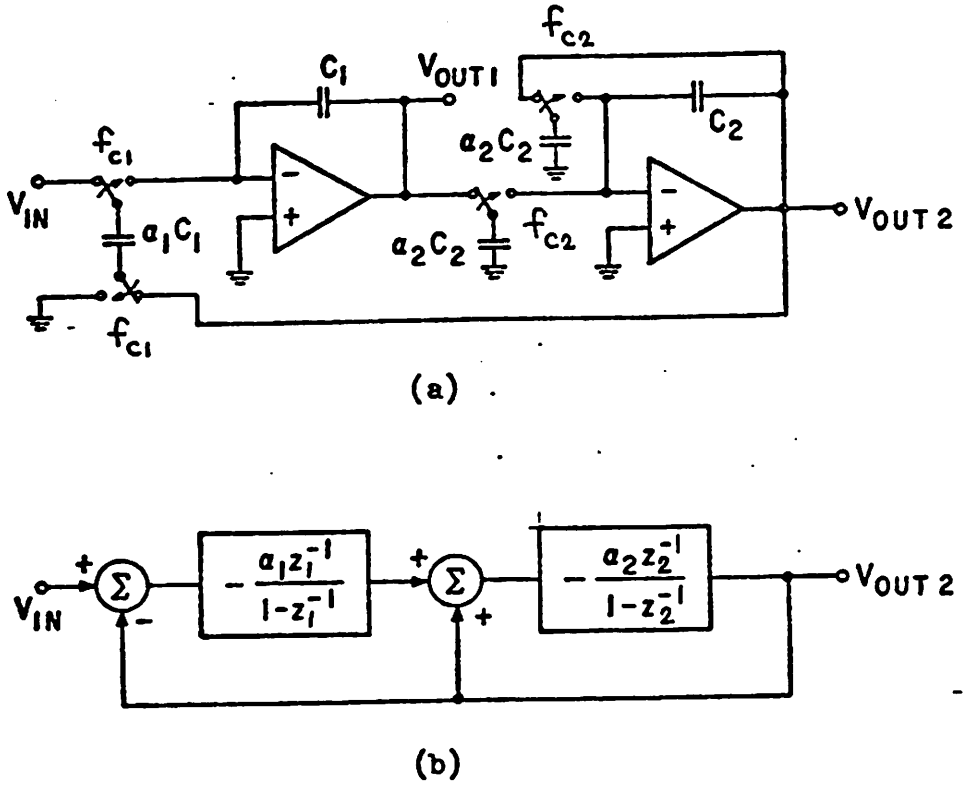


Figure 3.7: (a) Version 1 filter with 2 different clock rates
(b) z-transform block diagram of a

transfer function (see Fig. 3.7b):

$$\frac{V_{out2}(z)}{V_{in}(z)} = \frac{\alpha_1\alpha_2}{z_1z_2-z_2-z_1(1-\alpha_2)+(1+\alpha_1\alpha_2-\alpha_2)} \tag{3.39}$$

where $z_1 = e^{sT_{c1}}$ and $z_2 = e^{sT_{c2}}$. Let us assume that

$$f_{c2} = kf_{c1} \tag{3.40a}$$

which is equivalent to

$$T_{c2} = \frac{T_{c1}}{k} \tag{3.40b}$$

and further that the poles are close to the unit circle. Then the following approximation is valid:

$$z_2 \approx 1 + \frac{z_1-1}{k} \tag{3.41}$$

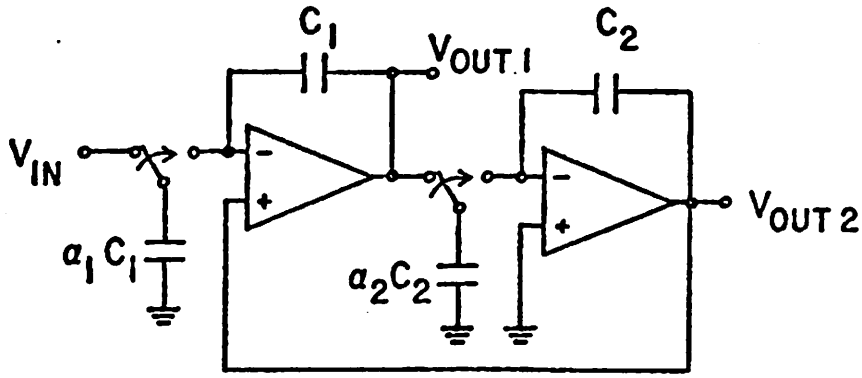
and the transfer function can be written as

$$\frac{V_{out2}(z)}{V_{in}(z)} = \frac{\alpha_1 k\alpha_2}{z_1^2-z_1(2-k\alpha_2)+(1+\alpha_1 k\alpha_2-k\alpha_2)} \tag{3.42}$$

This equation is identical to the Eq. (3.29) with the difference that α_2 has been replaced by $k\alpha_2$. In this way α_2 can be changed by changing the ratio f_{c2}/f_{c1}.

3.5.2. Version 2

The filter shown in Fig. 3.8a does not have high sensitivity to Q. With this filter the sensivities remain at 0.5 even for high Q filters. The single feedback line through the non-inverting input of the first



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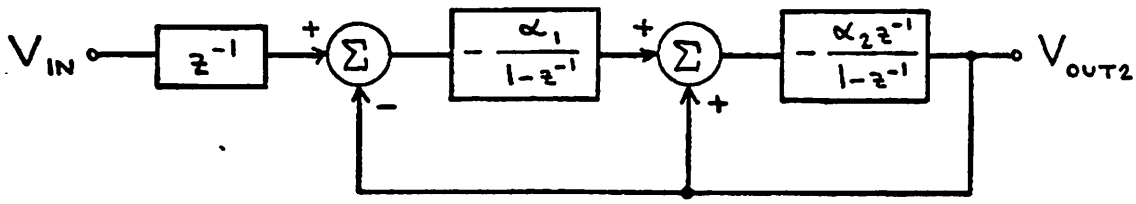


(b)

Figure 3.8: (a) The version 2 filter which has low sensitivity to the capacitor ratios α_1 and α_2
(b) z-transform block diagram of a

integrator simultaneously performs the overall negative feedback around both integrators as well as the local feedback around the second integrator. This makes possible a reduction in circuit complexity in comparison to version 1. The z-transform block diagram of this filter is shown in Fig. 3.8b. The transfer function at the bandpass output, V_{out1}, of the version 2 filter is

$$\frac{V_{out1}(z)}{V_{in}(z)} = \frac{-\alpha_1(z-1)}{z^2-(2-\alpha_1\alpha_2-\alpha_2)z+(1-\alpha_2)} \tag{3.43}$$

The lowpass output, V_{out2}, has the transfer function,

$$\frac{V_{out2}(z)}{V_{in}(z)} = \frac{\alpha_1\alpha_2}{z^2-(2-\alpha_1\alpha_2-\alpha_2)z+(1-\alpha_2)} \tag{3.44}$$

The design formulas for this filter are,

$$\alpha_2 = 1 - e^{-\frac{2\pi f_0}{Qf_c}} \tag{3.45a}$$

$$\alpha_1 = \frac{2[1-e^{-\frac{\pi f_0}{Qf_c}}\cos(\frac{\pi f_0}{f_c}\sqrt{4-\frac{1}{Q^2}})]}{1-e^{-\frac{2\pi f_0}{Qf_c}}} - 1 \tag{3.45b}$$

Similarly as in the case of the version 1 filter, it can be shown, that for poles close to the unit circle:

$$\alpha_2 \simeq \frac{\theta}{Q} \tag{3.46a}$$

$$\alpha_1 \simeq Q\theta \tag{3.46b}$$

The max. magnitude of the signal at the lowpass output is

$$\left|\frac{V_{out2}}{V_{in}}\right|_{z=e^{j\theta}} = \frac{\alpha_1\alpha_2 Q}{\theta \sin \theta} \simeq Q \qquad (3.47a)$$

and the max. magnitude at the bandpass output will be

$$\left|\frac{V_{out1}}{V_{in}}\right|_{z=e^{j\theta}} = \frac{\alpha_1 |e^{j\theta}-1| Q}{\theta \sin \theta} \simeq Q^2 \qquad (3.47b)$$

where $|e^{j\theta}-1| \simeq \theta$ for small θ. The Eq. (3.47b) suggests that there will be a problem concerning the dynamic range of this filter. We would have to attenuate the input signal for high Q filters in order to avoid the output swing limitation of the amplifier and this would decrease the dynamic range of the filter.

A disadvantage of this low sensitivity filter is that in order to obtain a high value of Q (greater than 100) the capacitor ratios can become quite large (also greater than 100) which requires a large amount of silicon area. This tradeoff between the size of the capacitor ratio and sensitivity appears to be a basic property of the sampled data state variable filter approach.

This becomes clearer when the transfer function of all versions presented are compared. Starting with the transfer function of a general second-order lowpass filter (Eq. (2.42)

$$H(z) = \frac{K_2}{z^2-az+b} \qquad (3.48a)$$

where $a = 2R \cos \theta$ and $b = R^2$ (from Eq. (2.44) and (2.45)) we can conclude that for poles close to the unit circle a will be close to 2 and b will be close to 1. Therefore it is more advantageous from the point of view of the state variable technique to realize a as $a = (2-c)$ and b as $b = (1-d)$

where c and d are both positive and very small. The Eq. (3.48a) changes to

$$H(z) = \frac{K_2}{z^2-(2-c)z+(1-d)} \tag{3.48b}$$

and the sensitivity can be easily calculated, e.g. S_c^Q, if we know the sensitivity S_a^Q:

$$S_c^Q = \left|\frac{c}{a}\right| S_a^Q \tag{3.48c}$$

Similarly

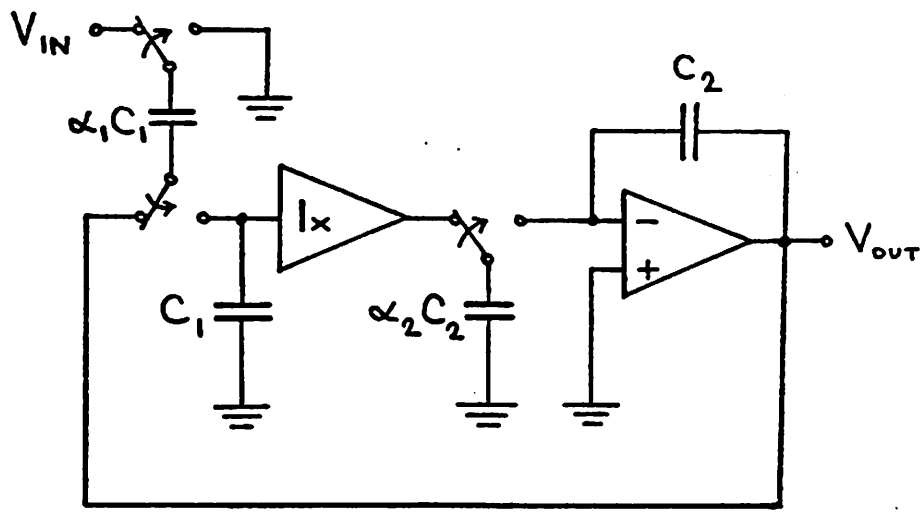
$$S_d^Q = \left|\frac{d}{b}\right| S_b^Q \tag{3.48d}$$

Since c and d are very small, both S_c^Q and S_d^Q will be much smaller than S_a^Q and S_b^Q, respectively. However the realization of very small coefficients will require very large capacitor ratios. When the transfer functions of all filters analyzed in this chapter are compared this particular version 2 is the best as far as the sensitivity is concerned and corresponds most closely to the analog state variable filter.

3.5.3. Version 3a

Both versions 1 and 2 use two operational amplifier integrators to realize two poles. One of these amplifiers can be replaced by a capacitor (unswitched) to yield the single amplifier lowpass filter shown in Fig. 3.9a. However a unity-gain buffer is needed between the two stages.

The unswitched capacitor C acts as an integrating capacitor when it is charged from a small capacitor αC (see Fig. 3.9b). The charge conservation equation yields



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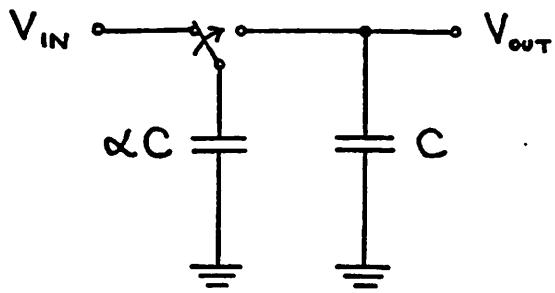
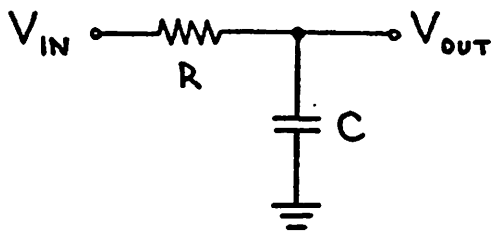


(b)

Figure 3.9: (a) The version 3a filter
(b) A passive sampled data integrator



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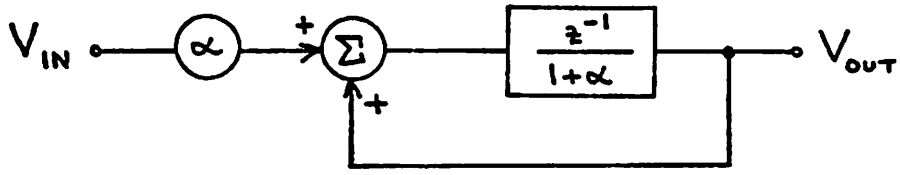

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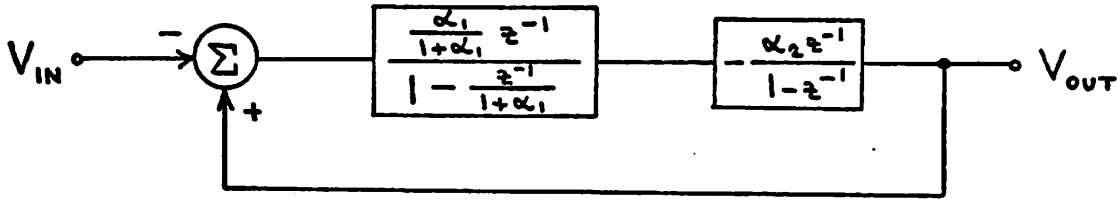


(e)

Figure 3.9: (c) A passive RC integrator
(d) z-transform block diagram of b
(e) z-transform block diagram of a

$$(1+\alpha)CV_{out}[nT_c] = CV_{out}[(n-1)T_c] + \alpha CV_{in}[(n-1)T_c] \tag{3.49}$$

Thus we have obtained a passive sampled data integrator with the transfer function

$$H(z) = \frac{\frac{\alpha}{1+\alpha} z^{-1}}{1 - \frac{z^{-1}}{1+\alpha}} \tag{3.50}$$

A block diagram of the z-transform of this integrator is shown in Fig. 3.9d. For a high clock rate ($f_c >> \omega/2\pi$) z can be approximated by $1 + j\omega T_c$ which when substituted into Eq. (3.50) yields

$$H(\omega) = \frac{1}{1+j\omega T_c(1+\frac{1}{\alpha})} \tag{3.51}$$

For very small α this function is the transfer function of an integrator. This is similar to an RC lowpass filter (Fig. 3.9c) with very large RC product.

The z-transform block diagram of the filter version 3a can be found in Fig. 3.9e.

The transfer function at the lowpass output is

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{\frac{\alpha_1\alpha_2}{1+\alpha_1}}{z^2 - z\frac{2+\alpha_1}{1+\alpha_1} + \frac{1+\alpha_1\alpha_2}{1+\alpha_1}} \tag{3.52a}$$

The design equations for this filter are:

$$\alpha_1 = 2\frac{1-e^{-\frac{\pi f_0}{Qf_c}}\cos\left(\frac{\pi f_0}{f_c}\sqrt{4-\frac{1}{Q^2}}\right)}{2e^{-\frac{\pi f_0}{Qf_c}}\cos\left(\frac{\pi f_0}{f_c}\sqrt{4-\frac{1}{Q^2}}\right)-1} \tag{3.52b}$$

$$\alpha_2 = \frac{1}{\alpha_1}\left[(1+\alpha_1)e^{-\frac{2\pi f_0}{Qf_c}} - 1\right] \tag{3.52c}$$

As mentioned above the disadvantage is that a unity-gain buffer is needed. If this buffer is removed then there will be a charge sharing between the capacitors C_1 and $\alpha_2 C_2$ as well. We will call such filter version 3.

3.5.4. Version 3

The circuit diagram of this filter is shown in Fig. 3.10a. In order to derive the transfer function we have to write the charge conservation equations first. The equation for the first stage has to include the charge sharing between all three capacitors: $\alpha_1 C$, C and $\alpha_2 AC$:

$$(1+\alpha_1)(1+A\alpha_2)V_c[(n-1)T_c] = \alpha_1\{V_{out}[(n-2)T_c] - V_{in}[(n-2)T_c]\} + V_c[(n-2)T_c] \tag{3.53a}$$

where V_c is the voltage across the capacitor C. The second stage is the integrator:

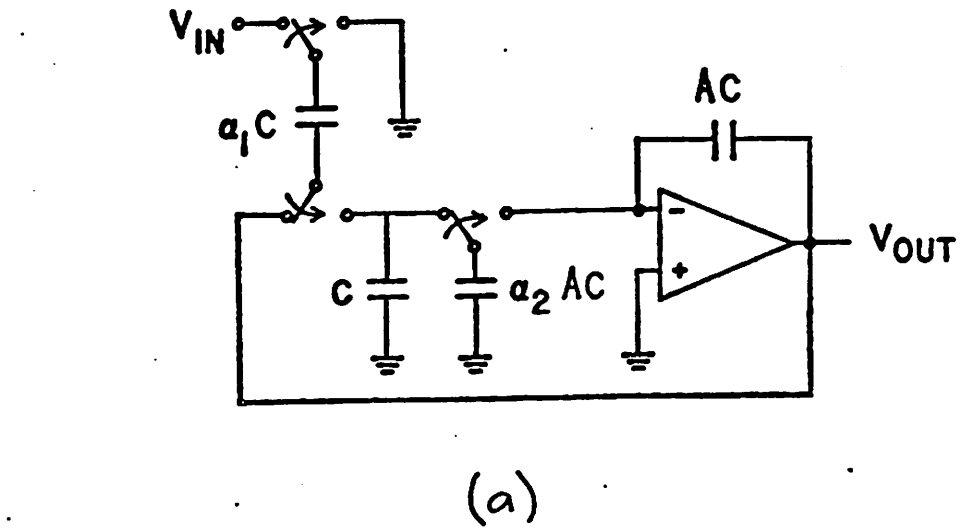
$$V_{out}[nT_c] = V_{out}[(n-1)T_c] - \alpha_2 V_c[(n-1)T_c] \tag{3.53b}$$

The z-transform block diagram of the whole filter is shown in Fig. 3.10b. The transfer function is

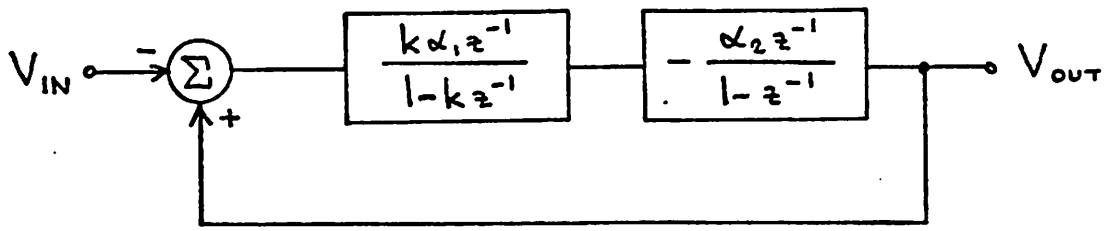
$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{k\alpha_1\alpha_2}{z^2 - z(k+1) + k(1+\alpha_1\alpha_2)} \tag{3.54a}$$

where

$$k = \frac{1}{(1+\alpha_1)(1+A\alpha_2)} \tag{3.54b}$$



(a)



(b)

Figure 3.10: (a) The version 3 filter which only requires a single amplifier

(b) z-transform block diagram of a

This filter has sensitivity characteristics which are similar to version 1. Since there are three design variables α_1, α_2 and A, there is an extra degree of freedom in this second order filter which can be resolved by requiring the filter design to have the lowest possible sensitivity.

A design procedure for this filter is as follows: first, choose a value of α_2; then calculate the value of k from the expression,

$$k = 2 \exp[-\frac{\pi f_0}{Q f_c}] \cos[\frac{\pi f_0}{f_c}\sqrt{4-\frac{1}{Q^2}}] - 1; \tag{3.55a}$$

finally, using the above values of k and α_2, calculate α_1 and A,

$$\alpha_1 = \frac{1}{\alpha_2}\left(\frac{1}{k}\exp[-\frac{2\pi f_0}{Q f_c}] - 1\right) \tag{3.55b}$$

$$A = \frac{1}{\alpha_2}\left(k^{-1}(1+\alpha_1)^{-1}-1\right) \tag{3.55c}$$

The sensitivity calculation is quite involved and after some manipulation we will find that for $f_0 << f_c$ and $Q >> 1$ the filter sensitivities are approximately given by ($\theta \cong 2\pi f_0/f_c$)

$$S_{\alpha_1}^{f_0} = \frac{1}{2\alpha_2}\left[1 - \theta^2(1+\frac{1}{\alpha_2})\right] \tag{3.56a}$$

$$S_{\alpha_2}^{f_0} = S_A^{f_0} = \frac{1}{2}\left(1-\frac{1}{\alpha_2}\right)(1-\theta^2) \tag{3.56b}$$

$$S_{\alpha_1}^{Q} = Q\,\frac{\theta(1-\theta^2)(\alpha_2-1)}{\alpha_2(1-\theta^2)+\theta^2} \tag{3.56c}$$

$$S_{\alpha_2}^{Q} = \frac{Q\theta}{\alpha_2} \tag{3.56d}$$

$$S_A^Q = Q\theta\left(1 - \frac{1}{\alpha_2}\right) \tag{3.56e}$$

Let us plot $S_{\alpha_2}^Q$ and S_A^Q as a function of α_2 (Fig. 3.11). The optimal case is $S_{\alpha_2}^Q = S_A^Q$ which yields $\alpha_2 \approx 2$. Then the sensitivities are approximately:

$$S_{\alpha_1}^{f_0} = \frac{1}{4}\left(1 - \frac{3\theta^2}{2}\right) \tag{3.57a}$$

$$S_{\alpha_2}^{f_0} = S_A^{f_0} = \frac{1}{4}\left(1 - \theta^2\right) \tag{3.57b}$$

$$S_{\alpha_1}^Q = Q\theta\left(\frac{1-\theta^2}{2-\theta^2}\right) \tag{3.57c}$$

$$S_{\alpha_2}^Q = S_A^Q = \frac{Q\theta}{2} \tag{3.57d}$$

The reader will note that for very small θ:

$$S_{\alpha_1}^Q \approx \frac{Q\theta}{2} \tag{3.58}$$

and so it is equal to $S_{\alpha_2}^Q$ and S_A^Q.

Before we check the dynamic range of the filter we express k and α_1 for poles close to the unit circle as

$$k \approx 1 - \theta\left(\theta + \frac{1}{Q}\right) \tag{3.59a}$$

$$\alpha_1 \approx \frac{1}{\alpha_2}\left[\frac{1}{k}\left(1 - \frac{\theta}{Q}\right) - 1\right] \tag{3.59b}$$

The max. magnitude of the signal at the filter output is

$$\left|\frac{V_{out}}{V_{in}}\right|\Bigg|_{z=e^{j\theta}} = \frac{k\alpha_1\alpha_2 Q}{\theta \sin \theta} \approx Q \tag{3.60}$$

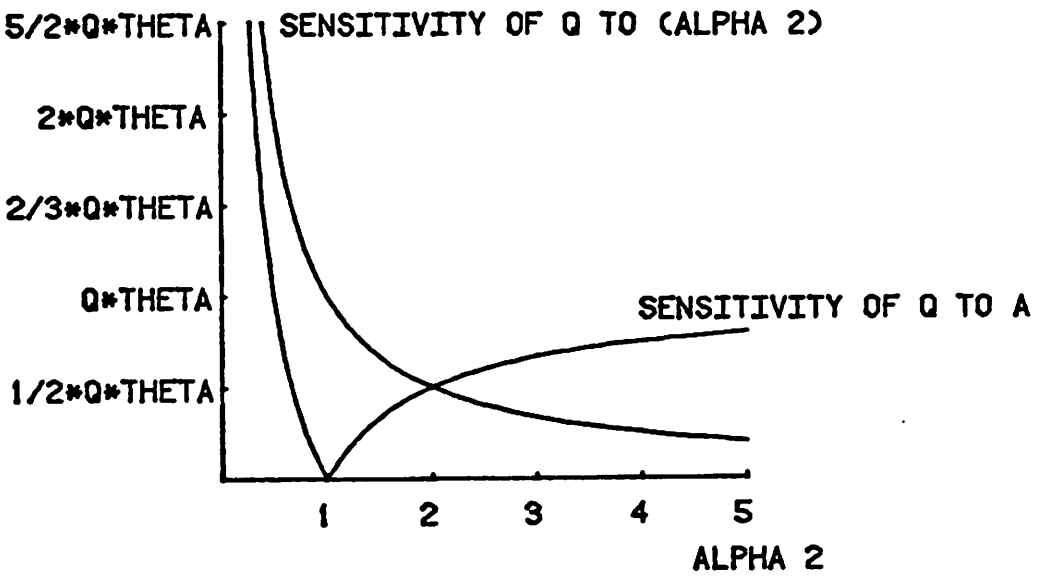


Figure 3.11: The sensitivities $S^{Q}_{\alpha_2}$ and S^{Q}_{A} as a function of α_2

So far the capacitors used in the filters described here have been considered linear. However in reality there will be some nonlinearity which will make the capacitor value dependent on the signal level as it will be explained later on. Therefore we should check how large would the signal be on the integrating capacitor C (Fig. 3.10a). Using the z-transform block diagram from Fig. 3.10b the voltage across this capacitor is given by

$$\frac{V_c(z)}{V_{in}(z)} = -\frac{k\alpha_1(z-1)}{z^2-z(k+1)+k(1+\alpha_1\alpha_2)} \tag{3.61}$$

Then

$$\left.\frac{V_c}{V_{in}}\right|_{z=e^{j\theta}} \approx \frac{k\alpha_1(e^{j\theta}-1)Q}{\sin} \approx \frac{\theta Q}{\alpha_2} \tag{3.62}$$

which is the max. magnitude of the signal level across C (with reference to the input).

CHAPTER 4

ANALOG AMPLIFIERS IN MOS TECHNOLOGY

4.1. Introduction

The inherent need to implement analog functions in large MOS-LSI systems has already led to design of all-MOS analog functional blocks, such as A/D converters and operational amplifiers [4,16,21-29,36]. In this chapter basic analog building blocks suitable for MOS amplifiers including discussion on multistage amplifiers will be presented.

We will concentrate on three types of technology: 1) single channel technology using enhancement devices only, 2) single channel MOS technology using enhancement and depletion devices, 3) CMOS technology. The discussion of single channel MOS technology will be limited to NMOS technology because transformation from an NMOS circuit to an analogous PMOS circuit is straightforward.

4.2. MOSFET DC Characteristics and Small-Signal Parameters

Despite the existence of more accurate and sophisticated MOSFET models [30-32] we will use the simple MOSFET model developed by Schichman and Hodges which is the most convenient one for physical understanding [33].

Figure 4.1 shows the cross section of a N-channel MOSFET in metal gate technology. Two N-regions are diffused into the P-substrate. A gate electrode is positioned between these two regions and it is insulated from the substrate by a thin layer of silicon dioxide. Figure 4.2 shows symbol and notation for an N-channel MOSFET. Figure 4.3 illustrates three areas of operation

a) cut-off region,

b) nonsaturation or linear region and

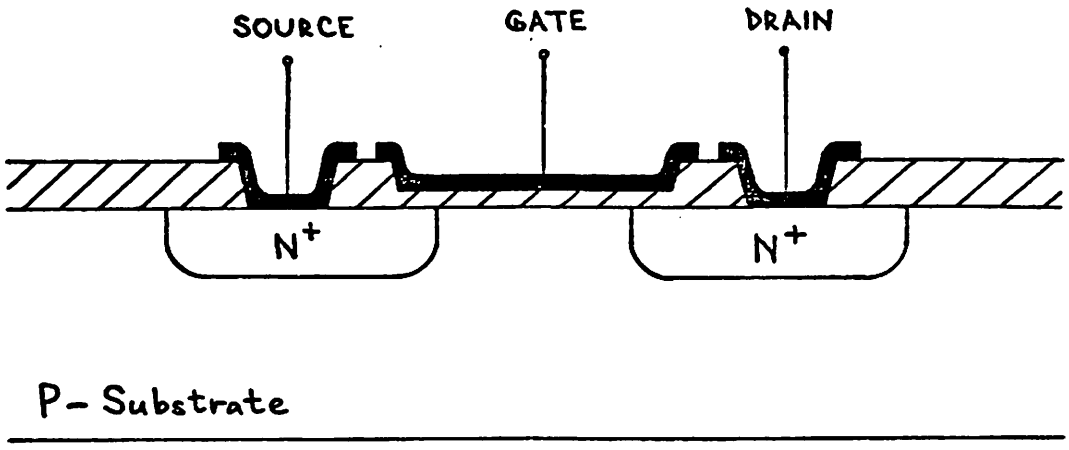


Figure 4.1: Crossection of an N-channel MOSFET

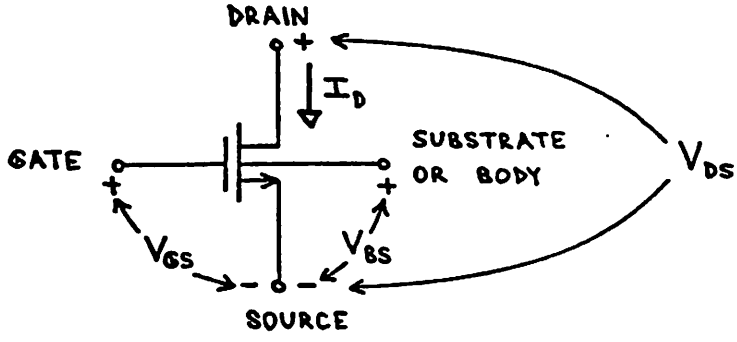


Figure 4.2: Symbol of an N-channel MOSFET and voltage and current notation

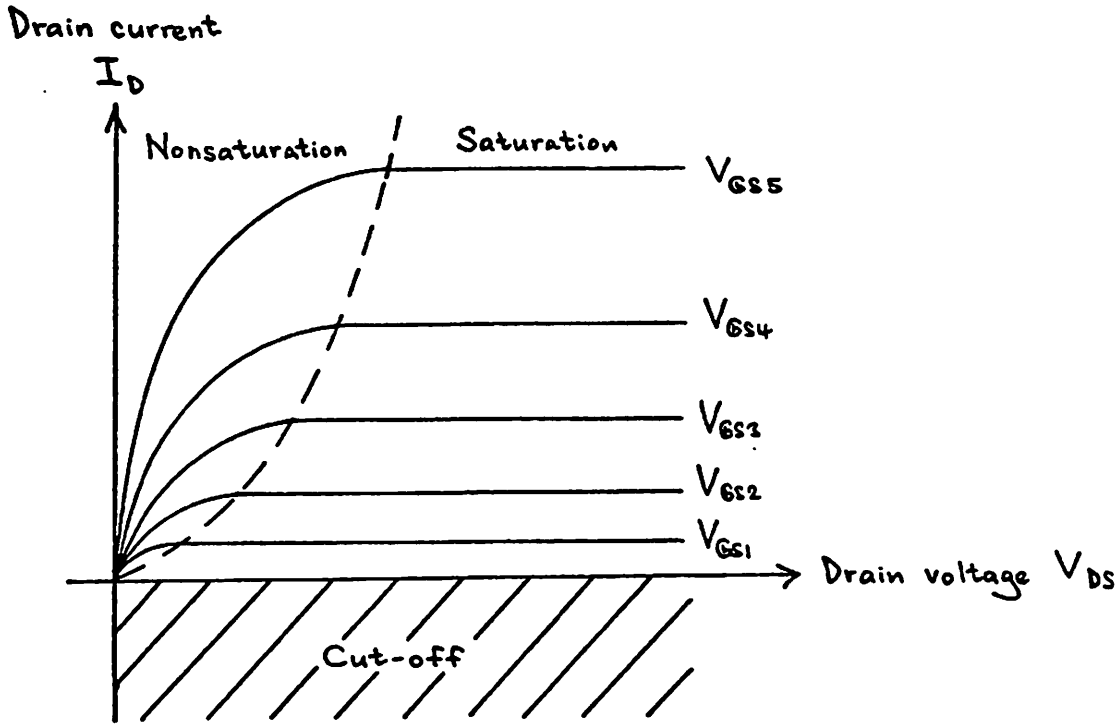


Figure 4.3: Drain characteristics of an MOSFET

c) saturation region.

The equation for the Schichman-Hodges model are as follows:

1. Nonsaturation region ($V_{GS}-V_T>V_{DS}$):

$$I_D = k[2(V_{GS}-V_T)V_{DS}-V_{DS}^2] \tag{4.1}$$

2. Saturation region ($V_{GS}-V_T \leq V_{DS}$):

$$I_D = k(V_{GS}-V_T)^2 \tag{4.2}$$

The parameter k is called the conduction factor:

$$k = k'(\frac{w}{\ell}) = \frac{\mu C_{ox}}{2}(\frac{w}{\ell}) = \frac{\mu \varepsilon_{ox}}{2t_{ox}}(\frac{w}{\ell}) \tag{4.3}$$

where μ = average surface mobility of electrons in the channel,

t_{ox} = thickness of the oxide over the channel,

ε_{ox} = permittivity of the oxide,

ℓ = length of the channel,

w = width of the channel.

The threshold voltage V_T is dependent upon the source-substrate voltage V_{BS}:

$$V_T = V_{TO} + \gamma(\sqrt{\phi_B-V_{BS}} - \sqrt{\phi_B}) \tag{4.4}$$

where V_{TO} = threshold voltage for V_{BS} = 0V,

ϕ_B = equilibrium junction potential,

γ = body effect coefficient.

For some applications it is important to express that I_D is dependent on V_{DS} in saturation region, i.e. that the drain characteristic curve has some finite slope even if this slope is rather small. The equation in

saturation region can be then modified to

$$I_D = k(V_{GS}-V_T)^2(1+\lambda V_{DS}) \tag{4.5}$$

where λ = channel length modulation parameter. The small signal MOSFET parameters are defined in terms of partial derivatives of the terminal voltages and currents:

1. Nonsaturation region

- transconductance $$g_m = \frac{\partial I_D}{\partial V_{GS}} = 2kV_{DS} \tag{4.6}$$

- output conductance $$\frac{1}{r_0} = \frac{\partial I_D}{\partial V_{DS}} = 2k(V_{GS}-V_T-V_{DS}) \tag{4.7}$$

2. Saturation region

- transconductance $$g_m = 2\sqrt{kI_D(1+\lambda V_{DS})} \tag{4.8}$$

- output conductance $$\frac{1}{r_0} = \frac{\lambda_{ID}}{1+\lambda I_D} \tag{4.9}$$

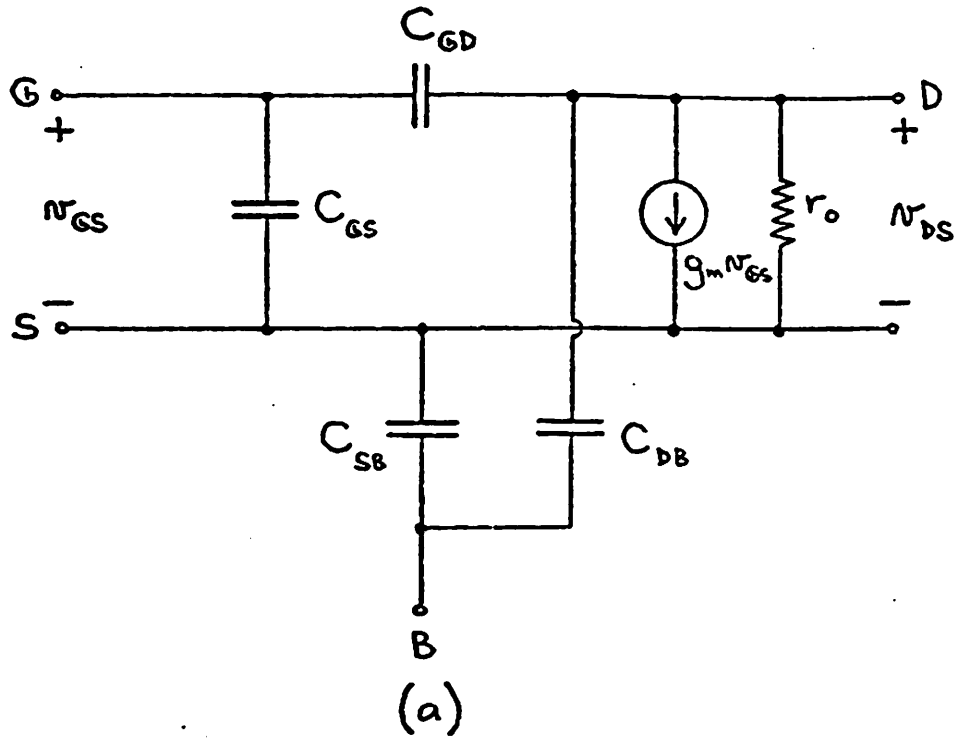
Because usually $\lambda V_{DS} << 1$ the last two expressions can be written as

$$g_m \approx 2\sqrt{kI_D} \tag{4.10}$$

and

$$\frac{1}{r_0} \approx \lambda I_D \tag{4.11}$$

Now we can draw a small-signal equivalent circuit for a MOSFET valid for both regions (Fig. 4.4a) that has to include intrinsic MOS and parasitic capacitances as well (from Fig. 4.4 b). The output resistance is much larger in the saturation region than in the nonsaturation region. Thus in general, we try to operate MOSFETs in analog circuits in the saturation region.



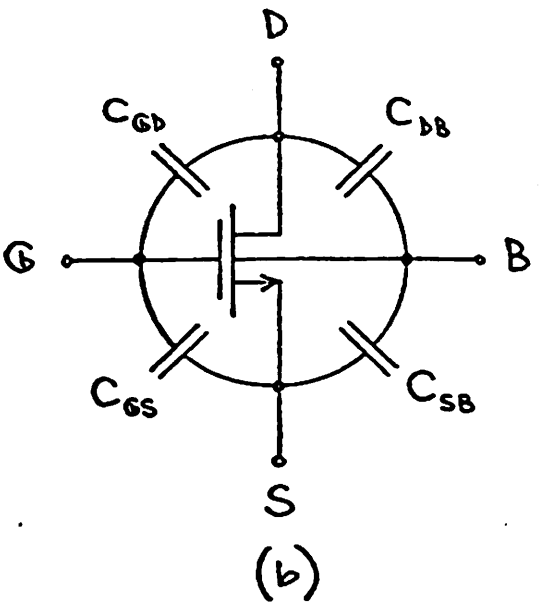


Figure 4.4: (a) Small-signal equivalent circuit for a MOSFET
(b) Intrinsic and parasitic MOSFET capacitances

The MOSFET capacitances in saturation region are given by following formulas:

$$C_{GD} = C_{\text{OVERLAP/UNIT CHANNEL WIDTH}} \times (\text{CHANNEL WIDTH}) \tag{4.12}$$

$$C_{GS} = [C_{\text{OVERLAP/UNIT CHANNEL WIDTH}} \times (\text{CHANNEL WIDTH})] + [(\tfrac{2}{3}) \times (C_{\text{OXIDE/UNIT OXIDE AREA}}) \times (\text{OXIDE AREA})] \tag{4.13}$$

$$C_{SB} = C_{\text{JUNCTION}} \times \left(1 + \frac{|V_{SB}|^{-1/2}}{\phi_B}\right) \times (\text{JUNCTION AREA}) \tag{4.14}$$

$$C_{DB} = C_{\text{JUNCTION}} \times \left(1 + \frac{|V_{DB}|^{-1/2}}{\phi_B}\right) \times (\text{JUNCTION AREA}) \tag{4.15}$$

where $C_{OVERLAP}$ = overlap capacitance, occurs where the thin gate oxide overlaps drain N-regions,

C_{OXIDE} = thin gate oxide capacitance,

$C_{JUNCTION}$ = PN junction capacitance at zero bias voltage.

Figure 4.5 shows the dependence of g_m and r_0 on the quiescent current I_D.

4.3. Basic MOS Analog Building Blocks

4.3.1. Inverters

The basic MOS inverter circuit with a passive linear load resistor is shown in Fig. 4.6a. The small-signal voltage gain can be readily obtained from Fig. 4.6b:

$$A_V = \frac{v_{out}}{v_{in}} = -g_m(R_L \| r_0) \cong -2\sqrt{kI_D}\,(R_L \| \frac{1}{\lambda I_D}) \tag{4.16}$$

Assuming that $R_L << \frac{1}{\lambda I_D}$, $k' = 6.25\ \mu A/V^2$, $\frac{W}{\ell} = 10$, $I_D = 1mA$, we obtain that for $A_V = 10$ a resistor $R_L = 20\ k\Omega$ is needed. A typical value of sheet resistance for a standard conventional diffused resistor is

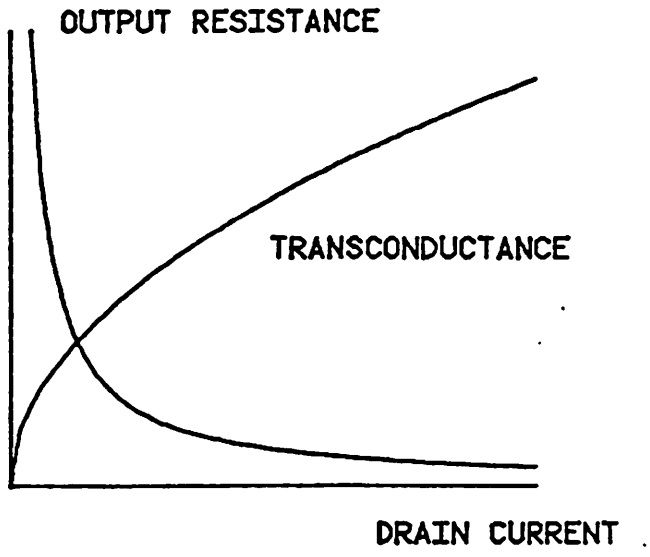
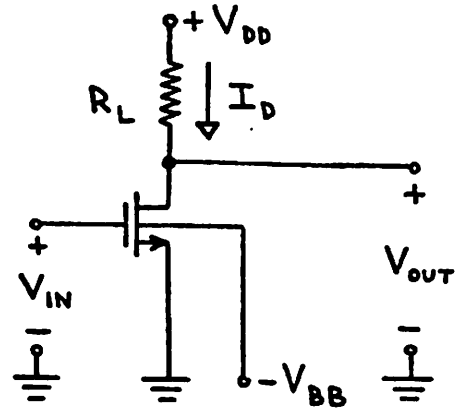
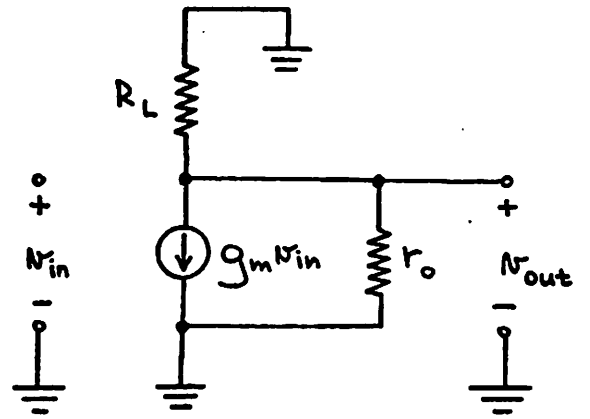


Figure 4.5: Small-signal parameters of a MOSFET as a function of the quiescent current I_D



(a)



(b)

Figure 4.6: (a) Circuit diagram of an MOS inverter with a passive load resistor

(b) Small-signal equivalent circuit of a

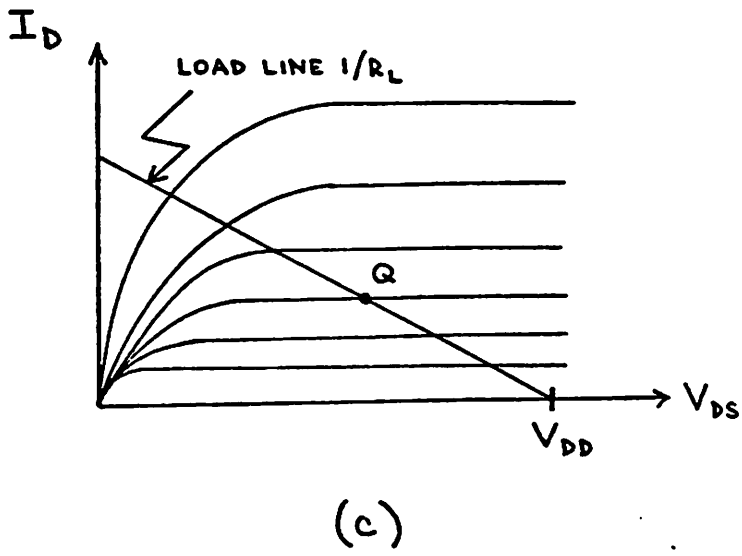


Figure 4.6.c: Drain characteristics of an MOS inverter with a passive load resistor

approximately 100 Ω/□. As a result, a 20 kΩ resistor would be typically 0.3 mil wide and 60 mil long and it would occupy an area approximately 18 mil^2. The MOS driver would occupy only about 1 mil^2. Thus a MOS load device is preferred to a diffused load resistor [34].

A simpliest MOS driver-load pair is an enhancement driver-enhancement load pair (Fig. 4.7a). A simple calculation based on small signal equivalent circuit for the enhancement load will show that the load represents an impedance $[(1/g_{m2})\|r_{02}]$ (Fig. 4.7b). Because $r_{02} >> 1/g_{m2}$ and $r_{01} >> 1/g_{m1}$ for practical purposes we can write

$$A_V = \frac{v_{out}}{v_{in}} \cong -\frac{g_{m1}}{g_{m2}} = -\frac{2\sqrt{k_1 I_{D1}}}{2\sqrt{k_2 I_{D2}}} \tag{4.17}$$

Knowing that

$$I_{D1} = I_{D2} = I_D,\ k_1 = k'(\tfrac{W}{\ell})_1,\ k_2 = k'(\tfrac{W}{\ell})_2$$

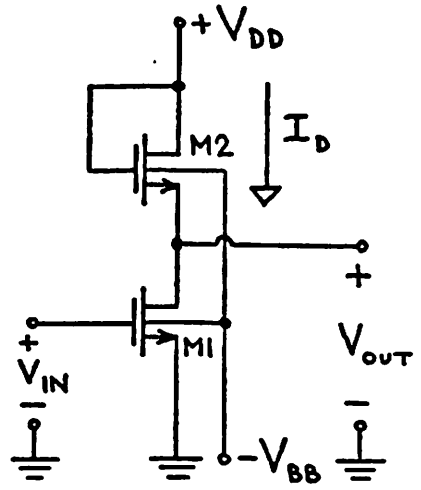
the voltage gain is

$$A_V = -\sqrt{\frac{(\frac{W}{\ell})_1}{(\frac{W}{\ell})_2}} \tag{4.18}$$

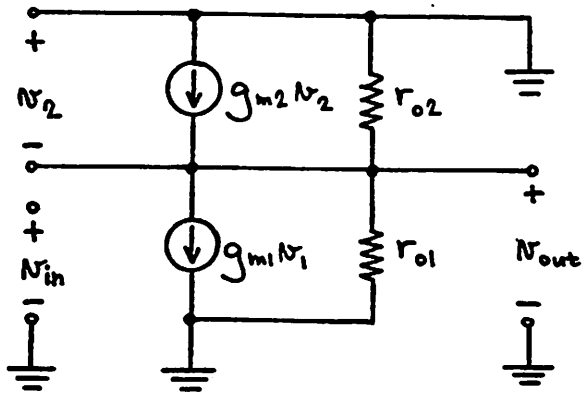
Thus the voltage gain is determined solely by MOS device geometries. Figure 4.7d shows that as we try to achieve high gain the driver device is getting impractically wide and the load device impractically long. Neglecting the channel length modulation of both devices we can write for the DC transfer curve

$$V_{OUT} = V_{DD} - \sqrt{\frac{(\frac{W}{\ell})_1}{(\frac{W}{\ell})_2}}\ (V_{IN}-V_{T1}) - V_{T2} \tag{4.19}$$

assuming M1 is in saturation. Figure 4.7e shows the transfer characteristics. When the substrate bias is $-V_{BB}$ then the threshold voltages are

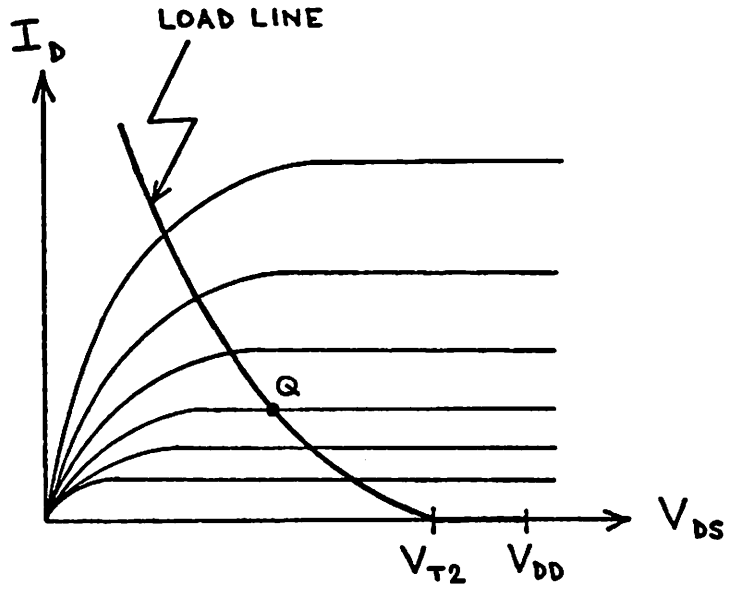


(a)



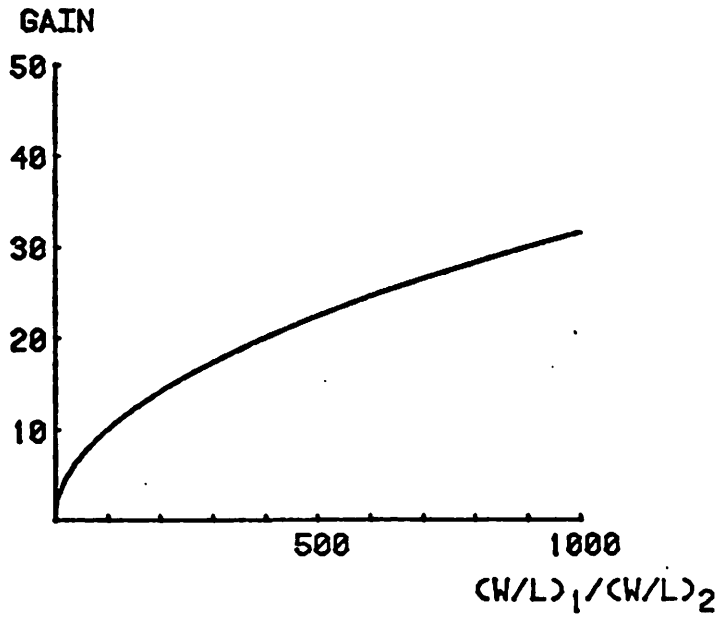
(b)

Figure 4.7: (a) MOS inverter with an MOS enhancement load device
(b) Small-signal equivalent circuit of a



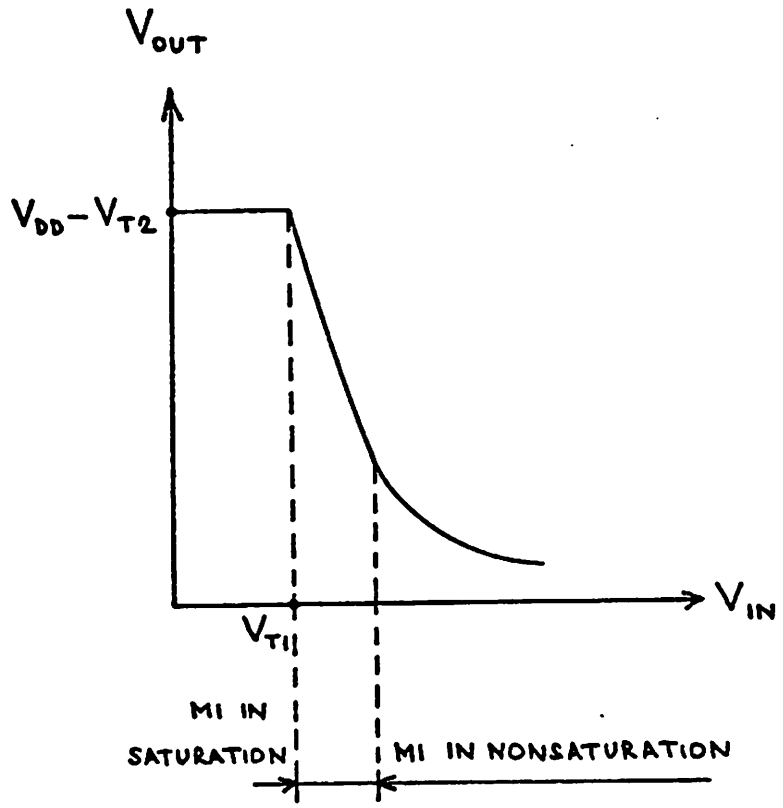
(c)

Figure 4.7.c: Drain characteristics of a



(d)

Figure 4.7.d: Voltage gain of a vs. ratio of device geometries



(e)

Figure 4.7.e: DC transfer curve of a

$$V_{T1} = V_{TO1} + \gamma(\sqrt{\phi_B - V_{BS1}} - \sqrt{\phi_B}) \tag{4.20}$$

$$V_{T2} = V_{TO2} + \gamma(\sqrt{\phi_B - V_{BS2}} - \sqrt{\phi_B}) \tag{4.21}$$

where

$V_{BS1} = -V_{BB}$ and $V_{BS2} = -V_{BB} - V_{OUT}$.

The DC transfer curve will be somewhat nonlinear due to the body effect:

$$V_{OUT} = V_{DD} - \sqrt{\frac{(\frac{W}{\ell})_1}{(\frac{W}{\ell})_2}}\,[V_{IN} - V_{TO1} - \gamma(\sqrt{\phi_B + V_{BB}} - \sqrt{\phi_B})] -$$

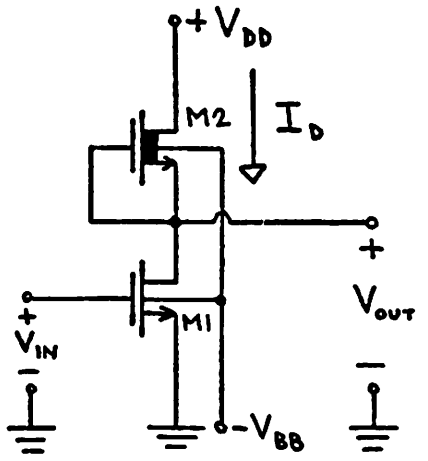
$$- V_{TO2} - \gamma(\sqrt{\phi_B + V_{BB} + V_{OUT}} - \sqrt{\phi_B}) \tag{4.22}$$

Rearrangement and differentiation yield

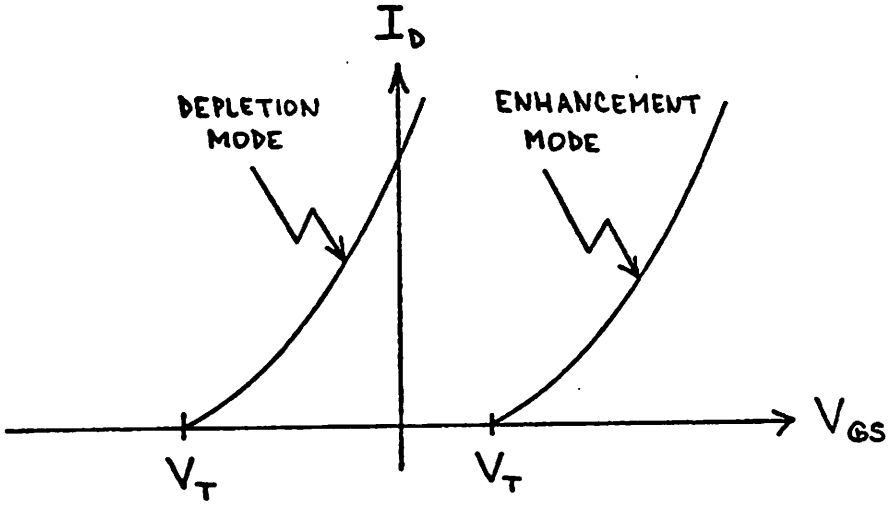
$$A_V = \frac{dV_{OUT}}{dV_{IN}} = -\frac{\sqrt{\frac{(\frac{W}{\ell})_1}{(\frac{W}{\ell})_2}}}{1 + \frac{\gamma}{2}\frac{1}{\sqrt{\phi_B + V_{BB} + V_{OUT,DC}}}} \tag{4.23}$$

Thus the small signal voltage gain is smaller due to the body effect.

Another MOS driver-load pair is an enhancement driver-depletion load pair (Fig. 4.8a). So far we have considered only enhancement MOSFETs. Figure 4.8b illustrates the difference between an enhancement MOSFET ($V_T>0$) and a depletion MOSFET ($V_T<0$). For the depletion MOSFET a following configuration is possible: the gate bias is kept constant at zero volts by connecting the gate and source terminal together. In a discrete version the substrate of the depletion MOSFET can be returned to the source and thus the device will function as a constant current source if the quiescent point is properly established [35]. The output impedance is then given by the channel length modulation.

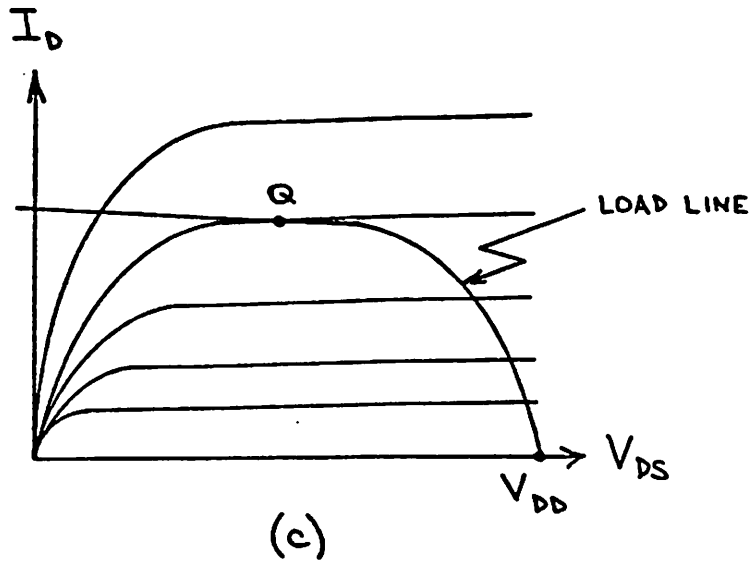


(a)

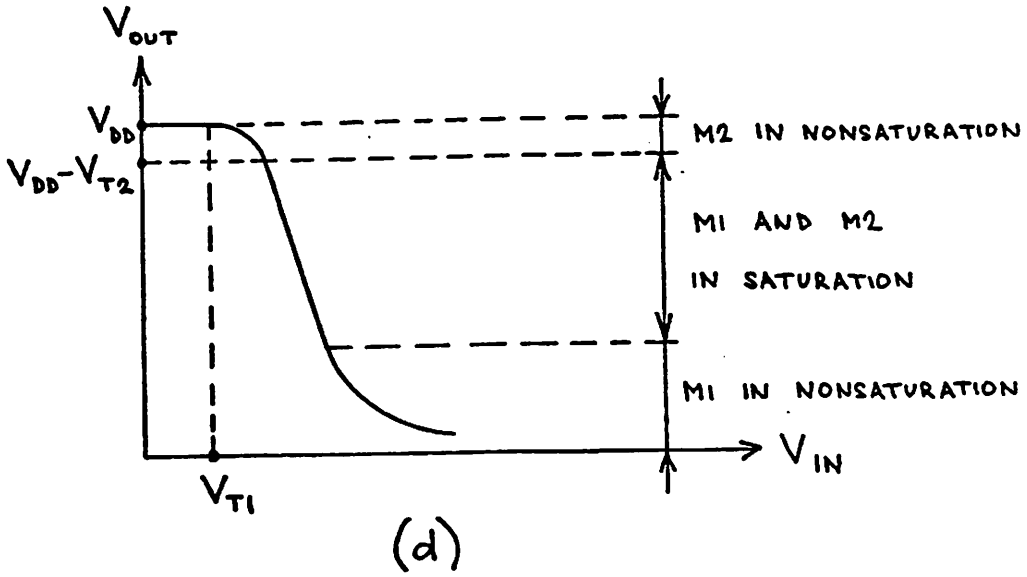


(b)

Figure 4.8: (a) MOS inverter with an MOS depletion load device
(b) I_D-V_{GS} characteristics of enhancement and depletion mode devices



(c)



(d)

Figure 4.8: (c) Drain characteristics of a
(d) DC transfer curve of a

In the integrated version the substrate will be connected to the substrate bias voltage V_{BB} and therefore the body effect will reduce the output impedance. The output impedance for the depletion device M2 is

$$\frac{1}{r_{O2}} = \frac{\partial I_{D2}}{\partial V_{DS2}} = \frac{\partial}{\partial V_{DS2}} [k_2(V_{GS2}-V_{T2})^2(1+\lambda_2 V_{DS2})] \tag{4.24a}$$

where $$V_{T2} = V_{TO2} + \gamma_2(\sqrt{\phi_{B2}-V_{BS2}} - \sqrt{\phi_{B2}})$$

$$V_{BS2} = - V_{BB} - V_{OUT}$$

$$V_{DS2} = V_{DD} - V_{OUT}$$

The result

$$\frac{1}{r_{O2}} = \frac{I_{D2}\lambda_2}{1+\lambda_2(V_{DD}-V_{OUT,DC})} + \frac{\gamma_2}{\sqrt{\phi_{B2}+V_{BB}+V_{OUT,DC}}} \sqrt{k_2 I_{D2}[1+\lambda_2(V_{DD}-V_{OUT,DC})]} \tag{4.24b}$$

suggests that the output impedance will be significantly lower than for the discrete device. If we make assumptions $\lambda_1 V_{DS1} << 1$ and $\lambda_2 V_{DS2} << 1$ we can write for the small signal gain

$$A_V = -g_{m1}(r_{O1} \| r_{O2}) \approx - 2\sqrt{k_1 I_{D1}} \frac{1}{\gamma_2} \sqrt{\frac{\phi_{B2}+V_{BB}+V_{OUT,DC}}{k_2 I_{D2}}}$$

$$= -\sqrt{\frac{(\frac{W}{\ell})_1}{(\frac{W}{\ell})_2}} \frac{2}{\gamma_2} \sqrt{\phi_{B2}+V_{BB}+V_{OUT,DC}} \tag{4.25}$$

From this expression and from Fig. 4.8d it can be seen that a depletion load offers two advantages over an enhancement load: higher voltage gain and larger output voltage swing.

Neglecting again the channel length modulation in both transistors

the DC transfer curve for the inverter from Fig. 4.8a is given by

$$V_{OUT} = \{\sqrt{\phi_{B2}} - \frac{1}{\gamma_2}\left[\sqrt{\frac{(\frac{W}{\ell})1}{(\frac{W}{\ell})_2}}(V_{IN}-V_{T1}) + V_{TO2}\right]\}^2 - (\phi_{B2}+V_{BB}) \qquad (4.26)$$

where $V_{T1} = V_{TO1} + \gamma_1(\sqrt{\phi_{B1}+V_{BB}} - \sqrt{\phi_{B1}})$. Equation (4.26) assumes that both devices are in saturation.

Last MOS driver-load pair to be examined here is a CMOS driver-load pair (Fig. 4.9a). The advantage is that substrates of both devices are separated and can be connected to their sources. The body effect is thus eliminated. The voltage gain is

$$A_V = \frac{v_{out}}{v_{in}} = -(g_{m1}+g_{m2})(r_{01}\|r_{02}) = -2\frac{\sqrt{k_1}+\sqrt{k_2}}{\sqrt{I_D}(\lambda_1+\lambda_2)} \qquad (4.27)$$

4.3.2. Current sources

MOS current sources are very similar to their bipolar counterparts. A current source that is analogous to Widlar's bipolar current source is shown in Fig. 4.10a. The current ratio is (when M2 in saturation)

$$\frac{I_{D2}}{I_{D1}} = \frac{(\frac{W}{\ell})_2}{(\frac{W}{\ell})_1}\frac{1+\lambda_2 V_{DS2}}{1+\lambda_1 V_{DS1}} \qquad (4.28)$$

and the output impedance is given by r_{02}. The output impedance of this source can be increased by a negative feedback (Fig. 4.10b). The output impedance will be then equal to the output impedance of the output transistor M3 times the loop gain ($g_{m3}r_{02}$):

$$Z_{OUT} \cong g_{m3}r_{02}r_{03} \qquad (4.29)$$

Output impedance of Wilson's MOS current source (Fig. 4.10c) would be

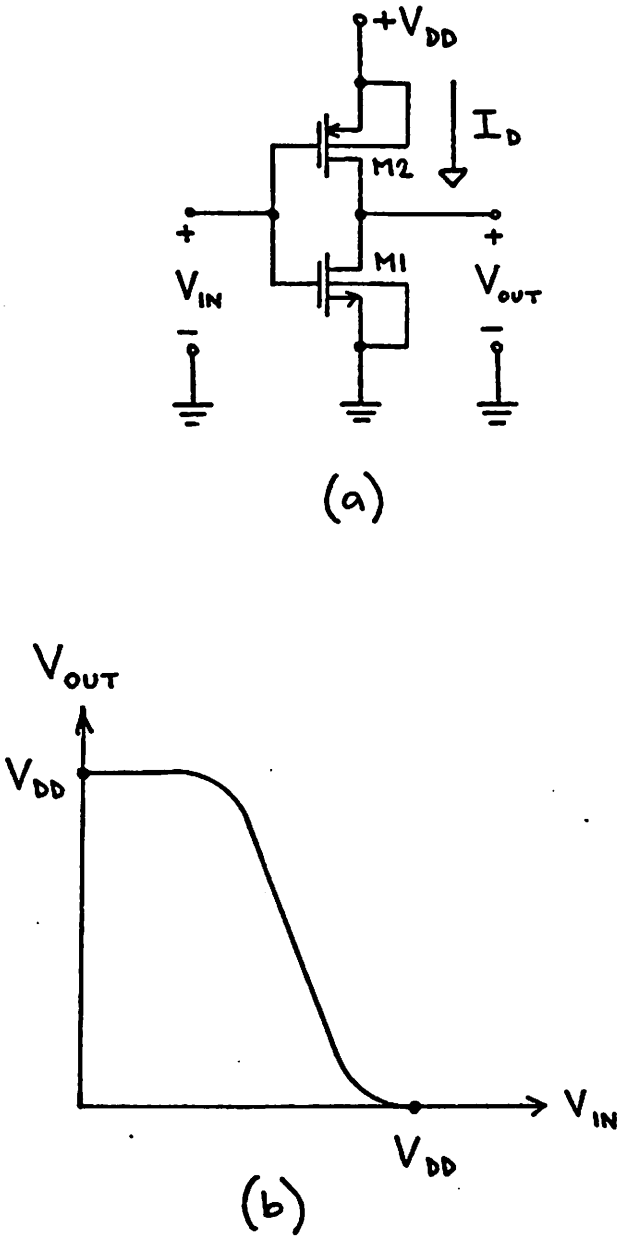


Figure 4.9: (a) CMOS inverter
(b) DC transfer curve of a

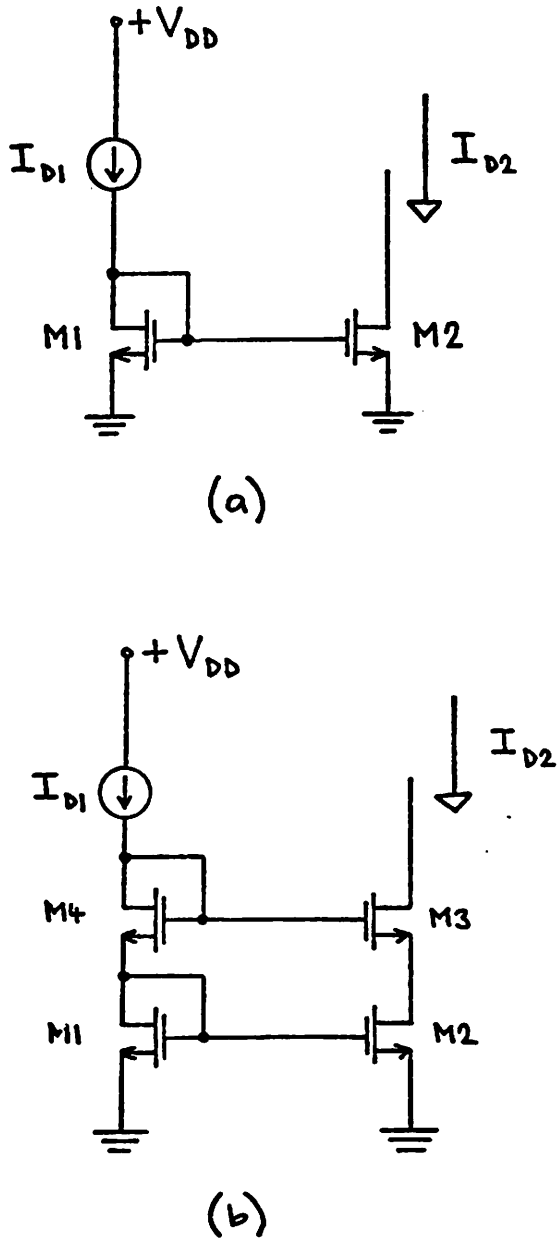
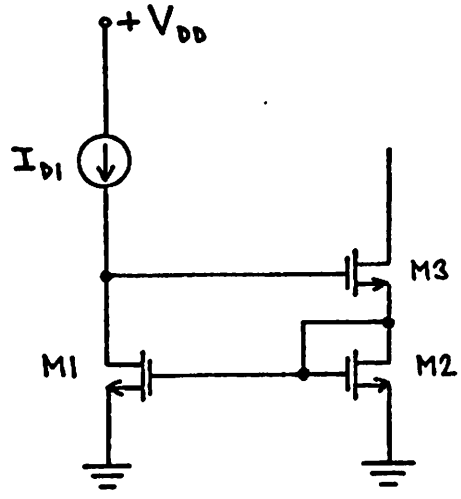


Figure 4.10: (a) MOS Widlar current source
(b) Improved MOS Widlar current source



(c)

(d)

Figure 4.10: (c) MOS Wilson current source
(d) Depletion MOSFET as a current source

$$Z_{OUT} \cong \frac{g_{m1}g_{m3}}{g_{m2}} r_{03} \; (r_{01} \| r_{04}) \tag{4.30}$$

It has been shown in section 4.3.1 that a depletion MOSFET can be used as a current source if the gate and source terminals are connected together (Fig. 4.10d). The current is

$$I_{D1} \cong k_1[V_{T01} + \gamma(\sqrt{\phi_B - V_{BS1}} - \phi_B)]^2 \tag{4.31}$$

The output impedance is

$$r_{01} \cong (\frac{1}{I_{D1}\lambda_1}) \| (\frac{1}{\gamma}\sqrt{\frac{\phi_B - V_{BS1}}{k_1 I_{D1}}}) \tag{4.32}$$

If B is kept at constant voltage then the impedance seen from A is only $1/(I_{D1}\lambda_1)$.

4.3.3. Source followers

A basic MOS source follower (Fig. 4.11a) has voltage gain

$$A_V = \frac{v_{out}}{v_{in}} = \frac{g_{m1}(r_{01} \| r_{02})}{1+g_{m1}(r_{01} \| r_{02})} \tag{4.33}$$

The output impedance is given by

$$R_{OUT} = \frac{1}{g_{m1}} \| r_{01} \| r_{02} \tag{4.34}$$

The max. output voltage is $(V_{DD}-V_{T1})$. However the source follower must be driven from a previous stage, i.e. with a top device M3. Then the practically available max. output voltage is only $(V_{DD}-V_{T1}-V_{T3})$.

Figure 4.11b shows another type of a source follower. The formulas above are valid in this case if we replace r_{02} by $[(1/g_{m2}) \| r_{02}]$.

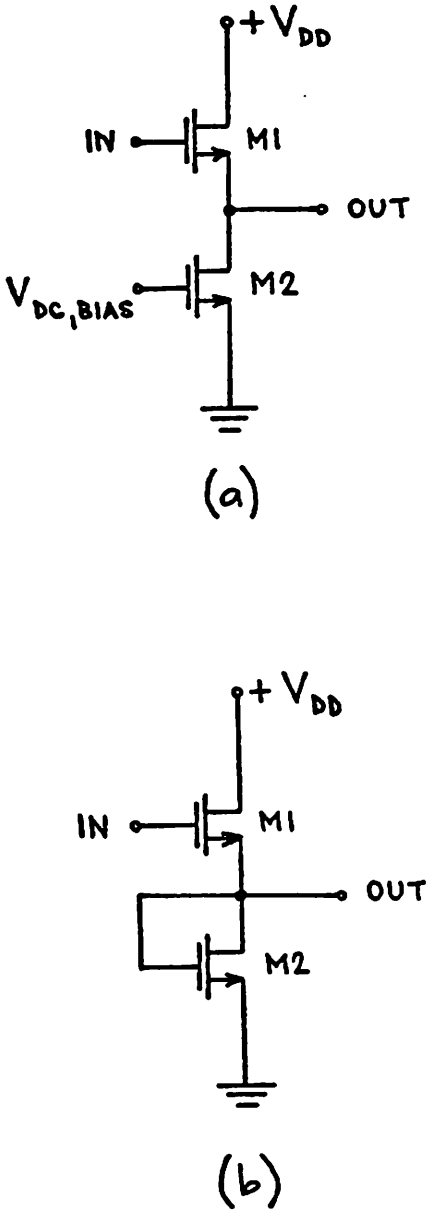
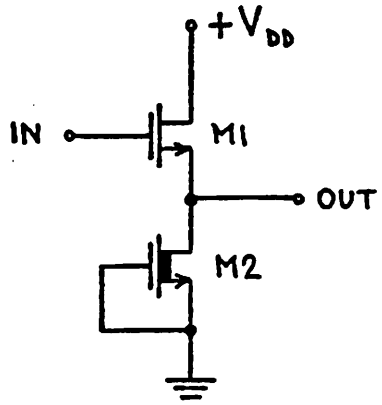
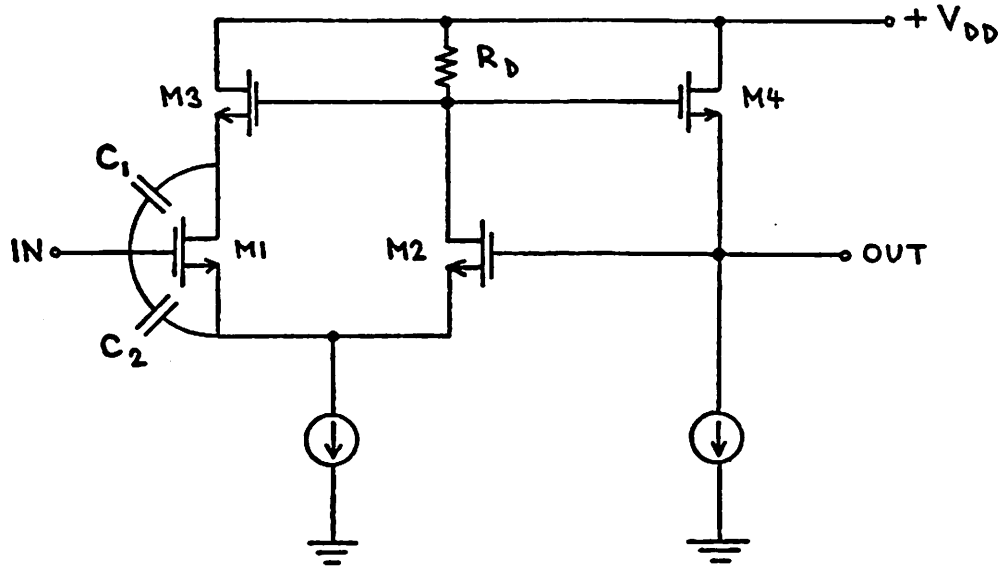


Figure 4.11: (a) Basic MOS source follower
(b) Bottom device has its gate connected to drain terminal



(c)



(d)

Figure 4.11: (c) Bottom device is a depletion MOSFET
(d) Voltage follower with very low input capacitance

The top device M1 can be a depletion MOSFET. This gives a higher output voltage swing. The bottom device M2 should be an enhancement MOSFET if we want higher output voltage swing in linear region. It is necessary for a MOSFET to be in saturation to keep

$$V_{DS} \geq V_{GS} - V_T$$

This gives lower range for depletion devices since $V_T < 0$. Despite this we may use a depletion MOSFET as a bottom device for some source followers (Fig. 4.11c) because it does not require any DC bias. The disadvantage of these source followers is that the top device has to be very large for low output impedance. Then of course the input capacitance which scales with the device geometry will be large as well. The voltage follower from Fig. 4.11d does not have this disadvantage. The output impedance is lowered by the loop gain:

$$R_{OUT} \approx \frac{1}{g_{m4}} \frac{1}{1 + \frac{1}{2} g_{m1} R_D} \tag{4.35}$$

and the input capacitance as well:

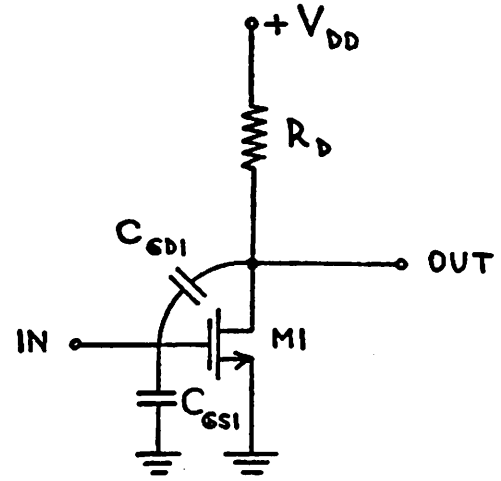
$$C_{IN} = \frac{\frac{1}{2} C_1 + C_2 (1 + \frac{g_{m1}}{2g_{m3}})}{1 + \frac{g_{m1} R_D}{2}} \tag{4.36}$$

We have assumed $g_{m1} = g_{m2}$. R_D can be a resistor or enhancement or depletion MOSFET.

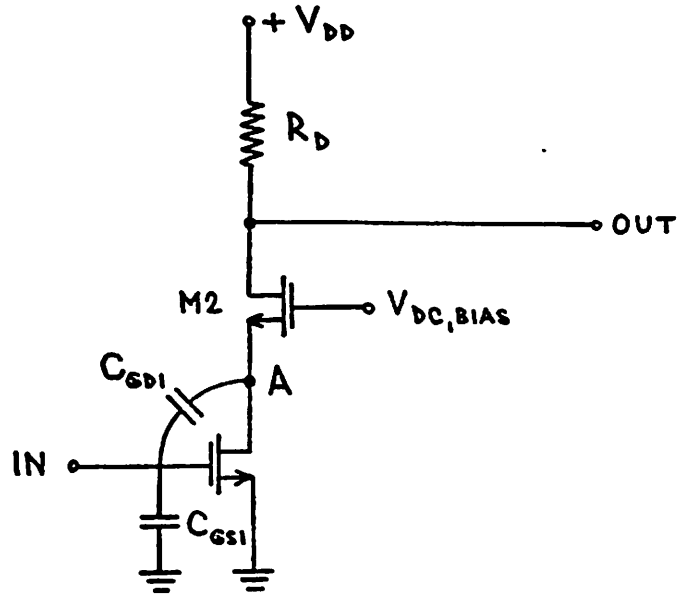
4.3.4. CASCODE

An inverter (Fig. 4.12a) delivers an output voltage

$$v_{out} = - g_{m1} (R_D \| r_{01}) v_{in} \tag{4.37}$$



(a)



(b)

Figure 4.12: (a) Inverter
(b) Cascode

where R_D can be any load we have discussed in Section 4.3.1. Thus the input capacitance due to Miller effect is

$$C_{IN} = [1 + g_{m1}(R_D \| r_{01})]\, C_{GD1} + C_{GS1} \tag{4.38}$$

This represents a large capacitive load to stage driving it. When a transistor M2 is inserted between the load R_D and the transistor M1 (Fig. 4.12b) the voltage at the node A is

$$v_A \simeq -\frac{g_{m1}}{g_{m2}} v_{in} \tag{4.39}$$

and the input capacitance is only

$$C_{IN} = (1 + \frac{g_{m1}}{g_{m2}})\, C_{GD1} + C_{GS1} \tag{4.40}$$

The small signal voltage gain is

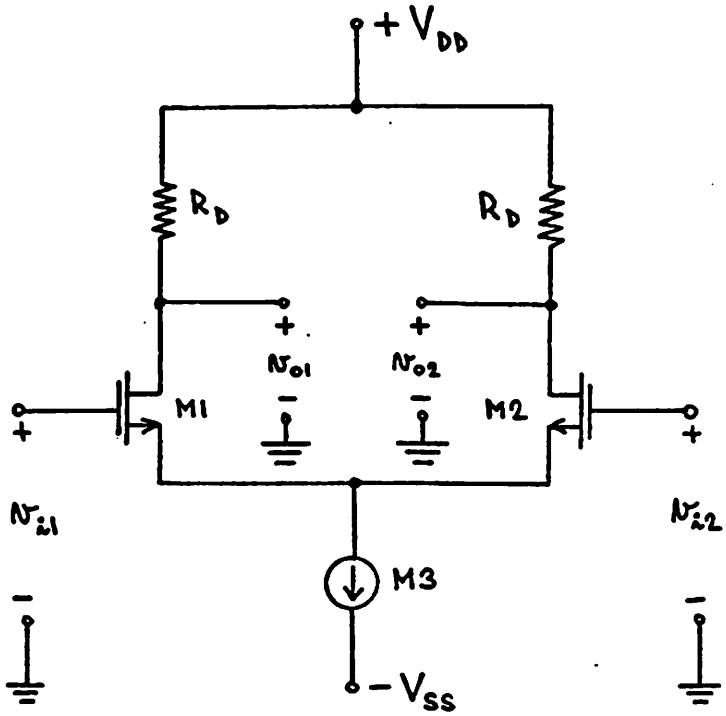
$$A_V \cong \frac{v_{out}}{v_{in}} \simeq -g_{m1}[R_D \| (1+g_{m2}r_{01})r_{02}] \tag{4.41}$$

This is the second benefit we obtain by using cascode: the shunting effect of r_{01} is by factor approximately $g_{m2}r_{02}$ smaller because the impedance when looking into the drain of M2 is $(1+g_{m2}r_{01})r_{02}$ due to the feedback loop M1, M2.

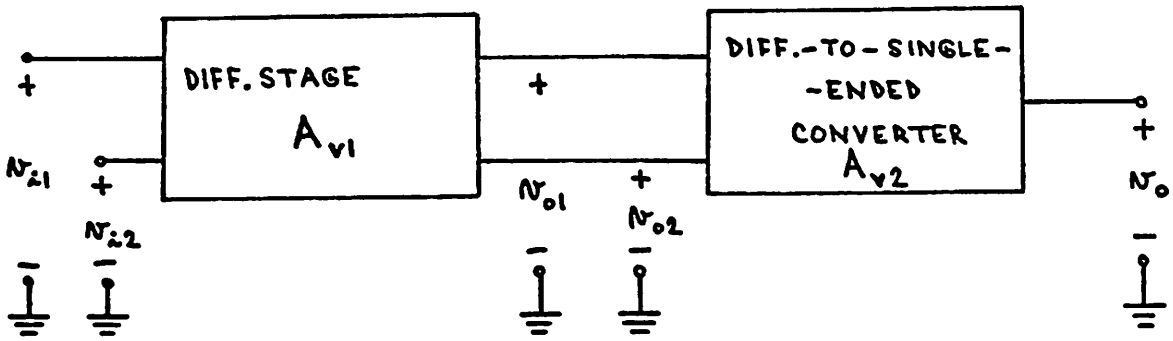
4.3.5. Differential stages

A basic MOS differential stage is shown in Fig. 4.13a. We define the differential-mode (DM) output voltage

$$v_{0d} = v_{01} - v_{02} \tag{4.42}$$

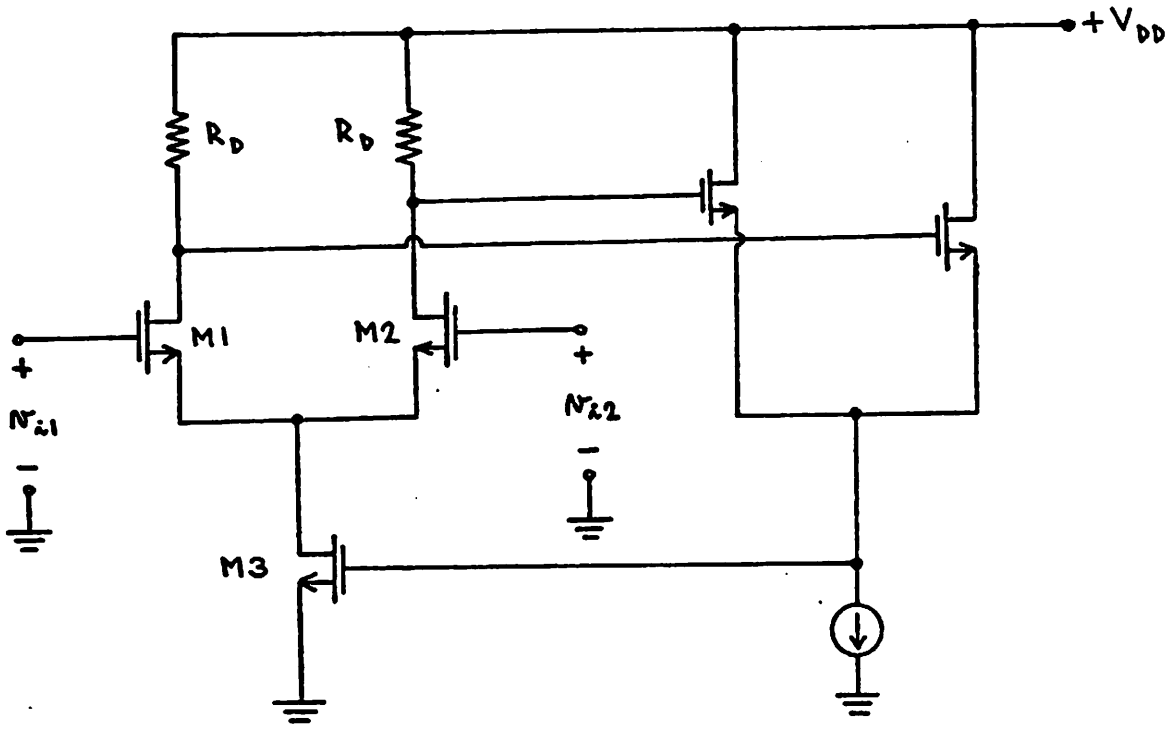


(a)



(b)

Figure 4.13: (a) MOS differential stage
(b) Block diagram of a diff.stage and a diff.-to--single-ended converter



(c)

Figure 4.13.c: Differential stage with common-mode feedback

and the common-mode output voltage

$$v_{0c} = \frac{v_{01}+v_{02}}{2} \tag{4.43}$$

From Fig. 4.13a it can be found that

$$v_{0d} = R_D \frac{g_{m2}v_{i2}(1+2g_{m1}r_{03})-g_{m1}v_{i1}(1+2g_{m2}r_{03})}{1+(g_{m1}+g_{m2})r_{03}} \tag{4.44}$$

and

$$v_{0c} = \frac{R_D}{2} \frac{g_{m2}v_{i2}+g_{m1}v_{i1}}{1+(g_{m1}+g_{m2})r_{03}} \tag{4.45}$$

if we assume that $r_{01} = \infty$ and $r_{02} = \infty$. Introducing

$$g_m = \frac{g_{m2}+g_{m1}}{2} \tag{4.46}$$

and

$$\Delta g_m = g_{m2} - g_{m1} \tag{4.47}$$

we can simplify our output voltages to

$$v_{0d} = -(v_{i1}-v_{i2})\left(g_m R_D - \frac{(\Delta g_m)^2 R_D r_{03}}{2(1+2g_m r_{03})}\right) + \frac{v_{i1}+v_{i2}}{2} \frac{\Delta g_m R_D}{1+2g_m r_{03}} \tag{4.48}$$

and

$$v_{0c} = \frac{v_{i1}+v_{i2}}{2} \frac{g_m R_D}{1+2g_m r_{03}} - (v_{i1}-v_{i2}) \frac{\Delta g_m R_D}{4(1+2g_m r_{03})} \tag{4.49}$$

We will find it convenient to define a DM input voltage

$$v_{id} = v_{i1} - v_{i2} \tag{4.50}$$

and a CM input voltage

$$v_{ic} = \frac{v_{i1}+v_{i2}}{2} \tag{4.51}$$

as well. This allows us to write the relation between the input and output voltages in the following form:

$$v_{0d} = A_{dm}v_{id} + \frac{A_{dm}}{CMRR_{CD}} v_{ic} \tag{4.52}$$

$$v_{0c} = \frac{A_{dm}}{CMRR_{CC}} v_{ic} + \frac{A_{dm}}{CMRR_{DC}} v_{id} \tag{4.53}$$

where $CMRR_{CD}$ is CM-to-DC rejection factor,

$CMRR_{DC}$ is DM-to-CM rejection factor,

$CMRR_{CC}$ is CM-to-CM rejection factor

of the differential stage.

A_{dm} is the DM voltage gain and for $(\Delta g_m/g_m) << 1$:

$$A_{dm} \approx - g_m R_D \tag{4.54}$$

Then the rejection factors are :

$$\frac{1}{CMRR_{CD}} = \frac{\Delta g_m}{g_m} \frac{1}{1+2g_m r_{03}} \approx \frac{\Delta g_m}{2g_m^2 r_{03}} \tag{4.55}$$

$$\frac{1}{CMRR_{CC}} = \frac{1}{1+2g_m r_{03}} \approx \frac{1}{2g_m r_{03}} \tag{4.56}$$

$$\frac{1}{CMRR_{DC}} = \frac{\Delta g_m}{g_m} \frac{1}{4(1+2g_m r_{03})} \approx \frac{\Delta g_m}{8g_m^2 r_{03}} \tag{4.57}$$

Very often a differential stage is followed by a differential-to-single-ended converter (Fig. 4.13b) and we are primarily interested in single-ended output v_0:

$$v_0 = A_{dmtot} + \frac{A_{dmtot}}{CMRR} v_{ic} = A_{1dm}A_{2dm}[(1 + \frac{1}{CMRR_{DC1}CMRR_{CD2}}) v_{id} +$$

$$+ \left(\frac{1}{CMRR_{CD1}} + \frac{1}{CMRR_{CC1}CMRR_{CD2}}\right)v_{ic}]$$

$$\approx A_{1dm}A_{2dm}\left(v_{id} + \frac{1}{CMRR}\, v_{ic}\right)$$

because

$$\frac{1}{CMRR_{DC1}CMRR_{CD2}} << 1 \qquad (4.58)$$

and

$$\frac{1}{CMRR} = \frac{1}{CMRR_{CD1}} + \frac{1}{CMRR_{CC1}CMRR_{CD2}} \qquad (4.59)$$

This expression for the common-mode rejection ratio shows very clearly (4.60)

limits that can be reached with differential stages: when we increase $CMRR_{CC1}$ (as in the case of Fig. 4.13c where

$$CMRR_{CC1} \approx g_m g_{m3} r_{03} R_D)$$

the term $CMRR_{CD1}$, which is due to mismatch of M1 and M2, will become (4.61)

dominant. For $1/g_{01,2} = r_{01,2} \neq \infty$ we obtain

$$\frac{1}{CMRR_{CD1}} \approx \frac{\Delta g_m}{g_m^2}\left(g_0 + \frac{1+R_D g_0}{2r_{03}}\right) + \frac{\Delta g_0}{g_m}\left(1 + \frac{R_D}{2r_{03}}\right) \qquad (4.62)$$

simpler way to increase CMRR is to make the channel length of M3 longer hich increases r_{03}.

4.3.6. Differential-to-Single Ended Converters

Figure 4.14a shows an example of a differential-to-single ended erter. It can be found that

$$v_0 \approx v_{i2} - \frac{g_{m2}}{g_{m1}+g_{m2}}\, v_{i1} \qquad (4.63)$$

$= g_{m3}$ and $g_{m2} = g_{m4}$. Using relationship

$= v_{i1} - v_{i2}$ (4.64)

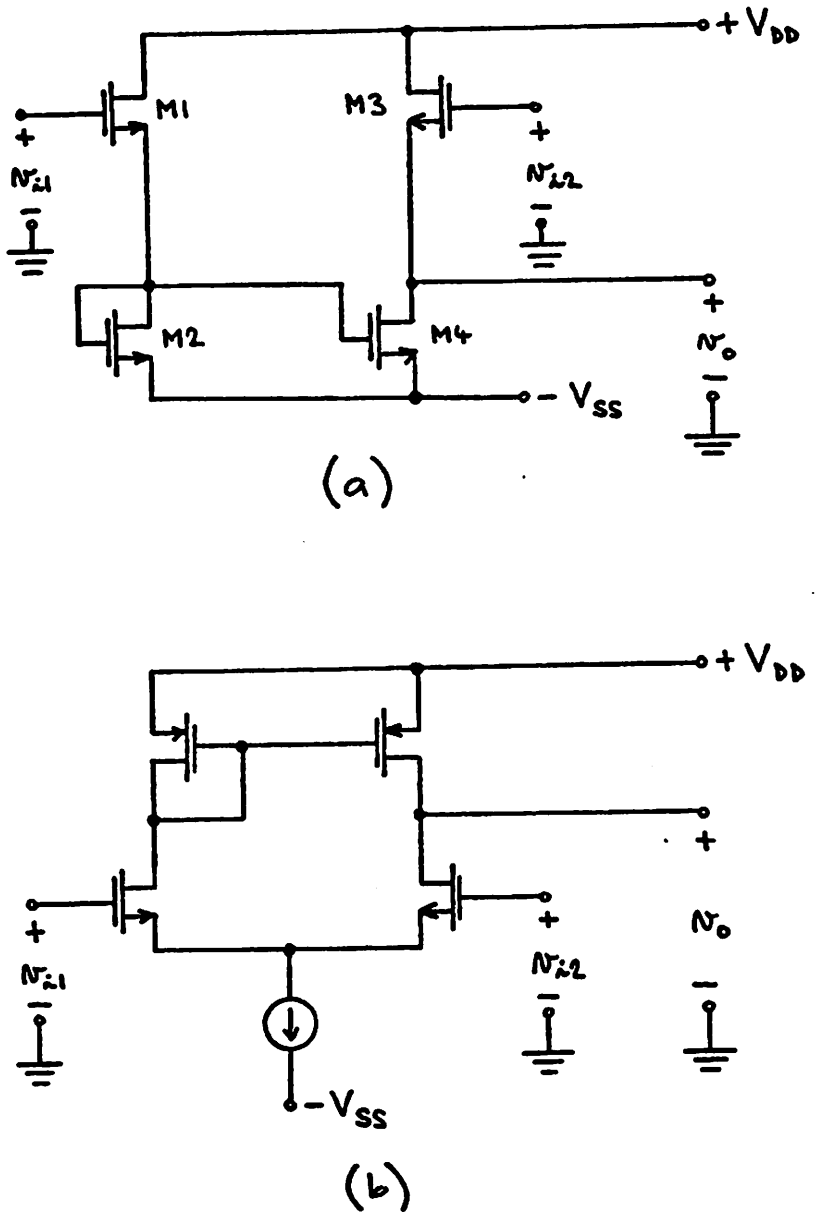


Figure 4.14: (a) Differential-to-single-ended converter
(b) CMOS differential stage with active loads

and

$$v_{ic} = \frac{v_{i1}+v_{i2}}{2} \tag{4.65}$$

we can write:

$$v_0 = v_{ic}\left(1 - \frac{g_{m2}}{g_{m1}+g_{m2}}\right) - \frac{v_{id}}{2}\left(1 + \frac{g_{m2}}{g_{m1}+g_{m2}}\right) \tag{4.66}$$

Thus for this converter

$$A_{dm} = -\frac{1}{2}\left(1 + \frac{g_{m2}}{g_{m1}+g_{m2}}\right) \tag{4.67}$$

and

$$CMRR = \frac{1}{2} + \frac{g_{m2}}{g_{m1}} \tag{4.68}$$

Clearly $g_{m2} >> g_{m1}$ is required for good design and consequently the following has to be fulfilled:

$$\left(\frac{W}{\ell}\right)_2 = \left(\frac{W}{\ell}\right)_4 >> \left(\frac{W}{\ell}\right)_1 = \left(\frac{W}{\ell}\right)_3 \tag{4.69}$$

A CMOS differential stage with active loads (Fig. 4.14b) has the advantage that it does not need any differential-to-single-ended converter because it automatically provides single ended output signal.

4.4. Special MOS Analog Building Blocks

4.4.1. High Gain Stages

Discussion in Section 4.3.1 has shown very clearly that max. available gain from basic MOS inverters is limited, depending on particular case, by max. and min. device geometries, processing parameters and power consumption. In this chapter we will investigate whether we can increase max. available gain by using more sophisticated circuit configurations.

Starting with an enhancement driver-enhancement load pair (Fig. 4.7a) the max. available gain is limited only by max. and min. device geometries:

$$A_{V1} \approx -\sqrt{\frac{(\frac{W}{\ell})_1}{(\frac{W}{\ell})_2}} \tag{4.70}$$

In practice usually $A_{Vmax} \simeq$ 10-15. It has been shown that the body effect reduces somewhat the voltage gain A_V.

One way to realize a high gain MOS inverter would be to use a positive feedback (Fig. 4.15) with a voltage transfer function

$$A_{Vtot} = -\frac{A_{V1}}{1-A_{V2}} \tag{4.71}$$

where A_{V2} is close to one. This would result however in undesired large voltage gain variations and stability problems as a consequence of device mismatch:

$$\left|\frac{\Delta A_{Vtot}}{A_{Vtot}}\right| = \left|\frac{\Delta A_{V1}}{A_{V1}}\right| + \left|\frac{A_{V2}}{1-A_{V2}}\right|\left|\frac{\Delta A_{V2}}{A_{V2}}\right| \tag{4.72}$$

The only way to obtain a high gain amplifier with enhancement load devices seems to be cascading of several gain stages. However this solution creates some problems which will be discussed later (see Section 4.5.1).

Voltage gain of the enhancement driver-depletion load pair can be increased by inserting a diffused resistor R_S between the source of M2 and the drain of M1 (Fig. 4.16a). The load impedance is then increased for r_{02} to

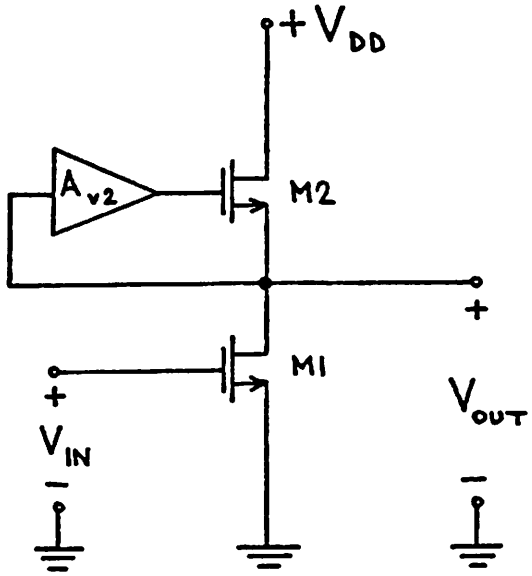


Figure 4.15: MOS gain stage with positive feedback

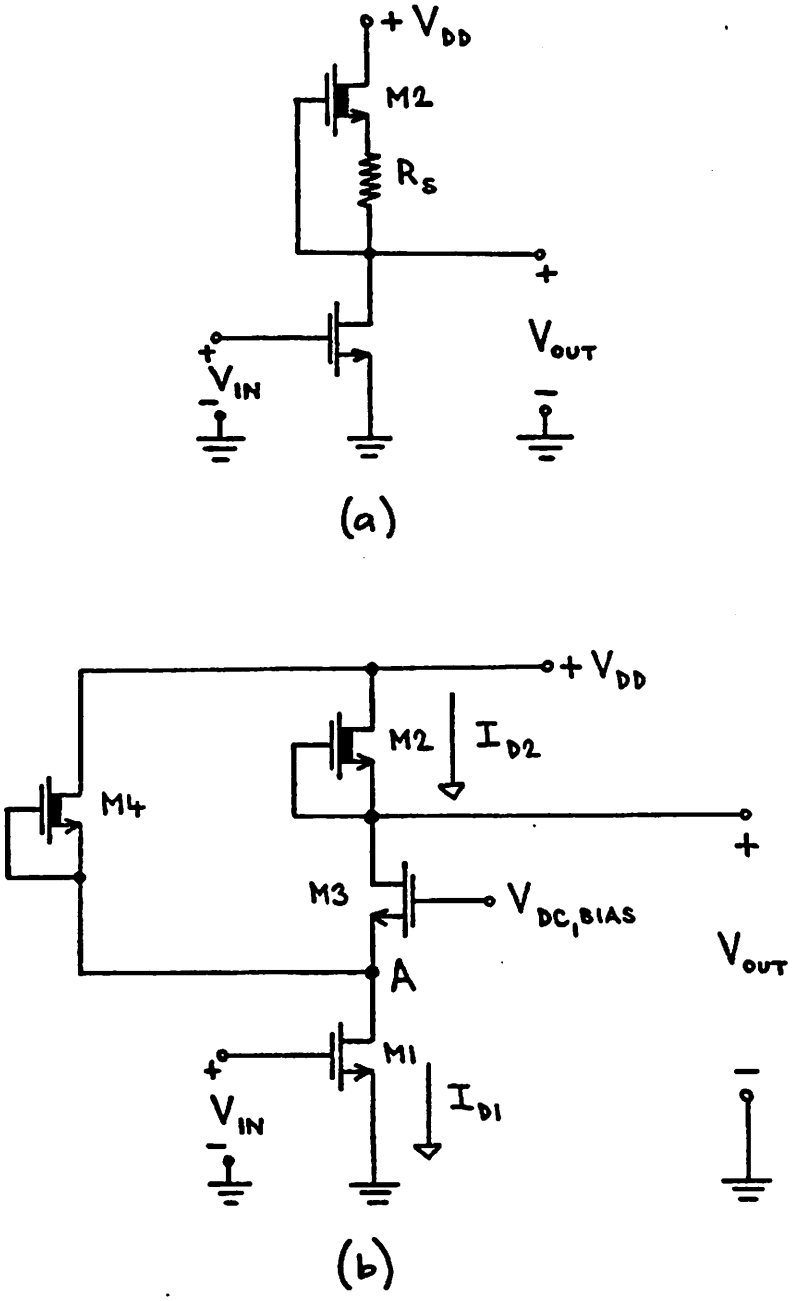
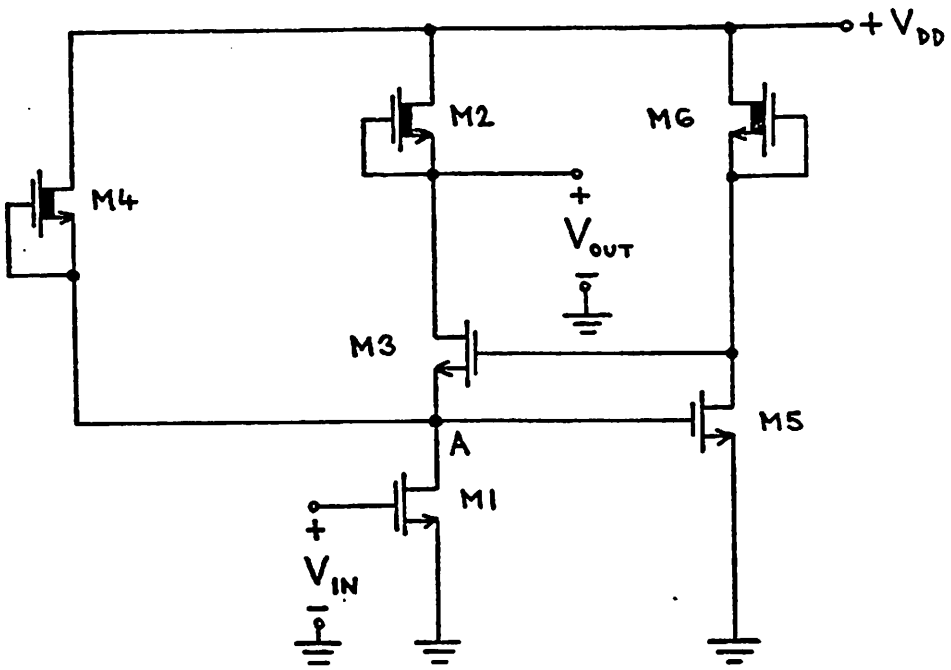


Figure 4.16: (a) MOS inverter with depletion load and diffused resistor

(b) MOS inverter with depletion load and current splitting



(c)

Figure 4.16.c: MOS inverter with depletion load and improved current splitting

$$R_{LOAD} = r_{02}(1+g_{m2}R_S) \tag{4.73}$$

and the gain increases to

$$A_V = - g_{m1}(r_{01} \| R_{LOAD}) \tag{4.74}$$

Figure 4.16b shows an enhancement driver-depletion bad gain stage where a current source (M4) has been added in order to increase the DC current of the driver M1. This will increase the transconductance g_{m1} and consequently total gain of the stage:

$$A_V \approx - g_{m1}r_{02} \approx - \frac{2}{\gamma_2}\sqrt{\frac{(\frac{W}{\ell})_1}{(\frac{W}{\ell})_2}}\sqrt{\frac{I_{D1}}{I_{D2}}}\sqrt{\phi_{B2}+V_{BB}+V_{OUT,DC}} \tag{4.75}$$

when r_{01}, r_{03} and r_{04} neglected. The practical gain will be smaller because of the shunting effect of r_{01}, r_{03} and r_{04}. The transistor M3 (common gate configuration) isolates the load device M2. The disadvantage is that one more pole has been introduced; its location will be determined mainly by the transconductance of M3 and total capacitance at node A. The transconductance of M3 will be small if I_{D2} is small. Thus smaller bandwidth will result if large gain is desired.

Figure 4.16c suggests an improved circuit. The feedback stage M5, M6 will lower the impedance at node A by factor

$$1 + \frac{2}{\gamma_6}\sqrt{\frac{(\frac{W}{\ell})_5}{(\frac{W}{\ell})_6}}\sqrt{\phi_{B6}-V_{BS6}} \tag{4.76}$$

This will increase total gain of the stage (shunting effects of r_{01}, r_{03} and r_{04} decrease) and the bandwidth.

CMOS technology is certainly the most attractive for an analog circuit designer because it offers greater flexibility than single channel MOS technology. New CMOS processes allow analog CMOS circuits being capable of operation with a 30 V power supply [36].

A simple CMOS high gain stage is shown in Fig 4.17a. Advantages of a cascode stage (see Section 4.3.4) can be fully utilized. Two complementary cascodes create a very high impedance node. The gain is given by this impedance and the transconductance of the stage. Assuming full symmetry, i.e.

$$g_{m5} = g_{m8},\ r_{05} = r_{08} \tag{4.77}$$

$$g_{m6} = g_{m7},\ r_{06} = r_{07} \tag{4.78}$$

the voltage gain is

$$A_V = \frac{v_{out}}{v_{in}} = - g_{m5} r_{05} (1+g_{m6} r_{06}) \tag{4.79}$$

Adding a feedback stage which has been used in the MOS inverter with depletion load and improved current splitting (Fig. 4.16c) will increase the gain even more (see Fig. 4.17b). The new voltage gain is

$$A_v = - g_{m5} r_{05} [1 + g_{m6} r_{06} (1+g_{m10} (r_{09} \| r_{010}))] \tag{4.80}$$

Again a full symmetry is assumed:

$$g_{m5} = g_{m8},\ r_{05} = r_{08} \tag{4.81}$$

$$g_{m6} = g_{m7},\ r_{06} = r_{07} \tag{4.82}$$

$$g_{m10} = g_{m11},\ r_{010} = r_{011} \tag{4.83}$$

$$r_{09} = r_{012} \tag{4.84}$$

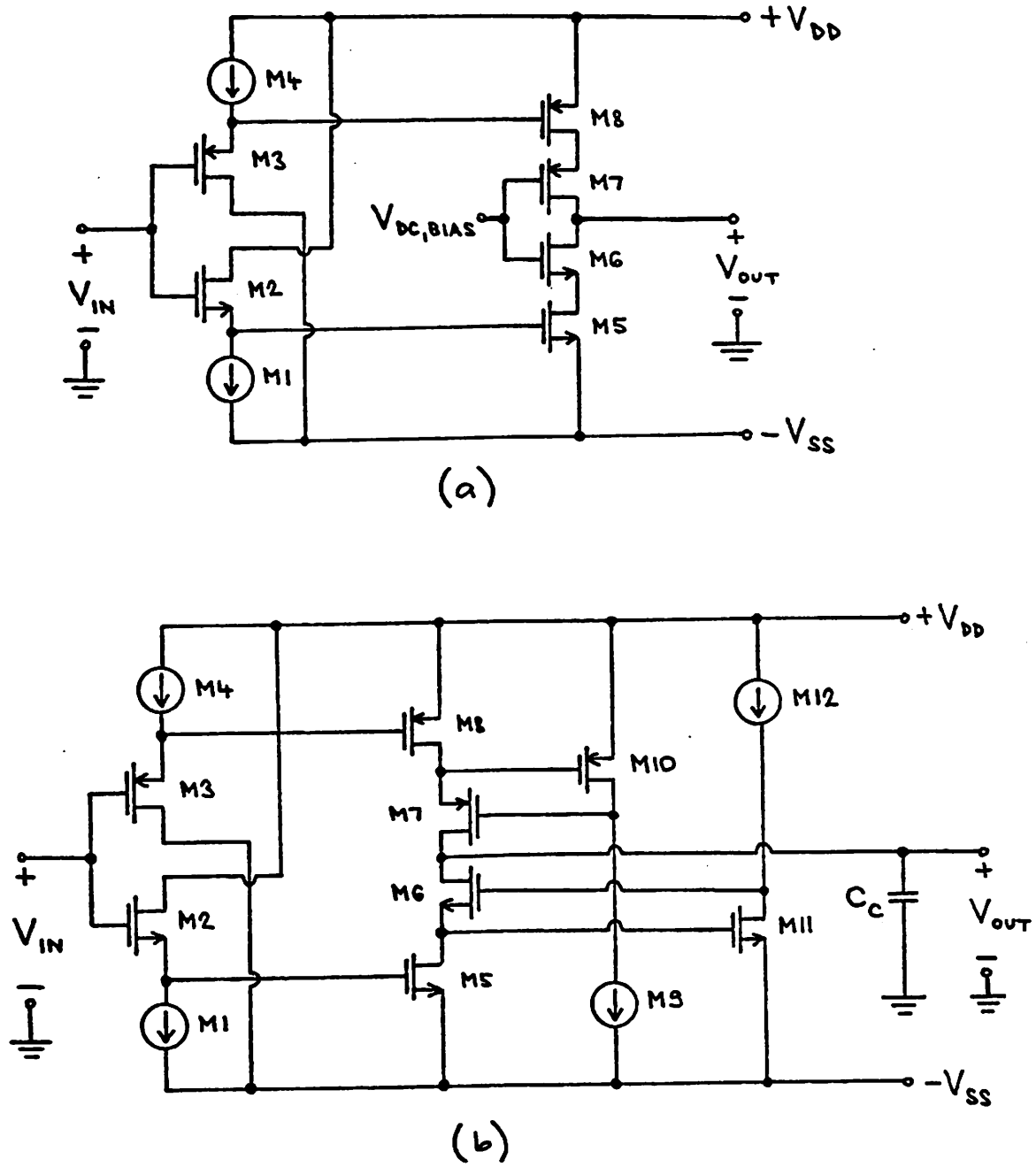
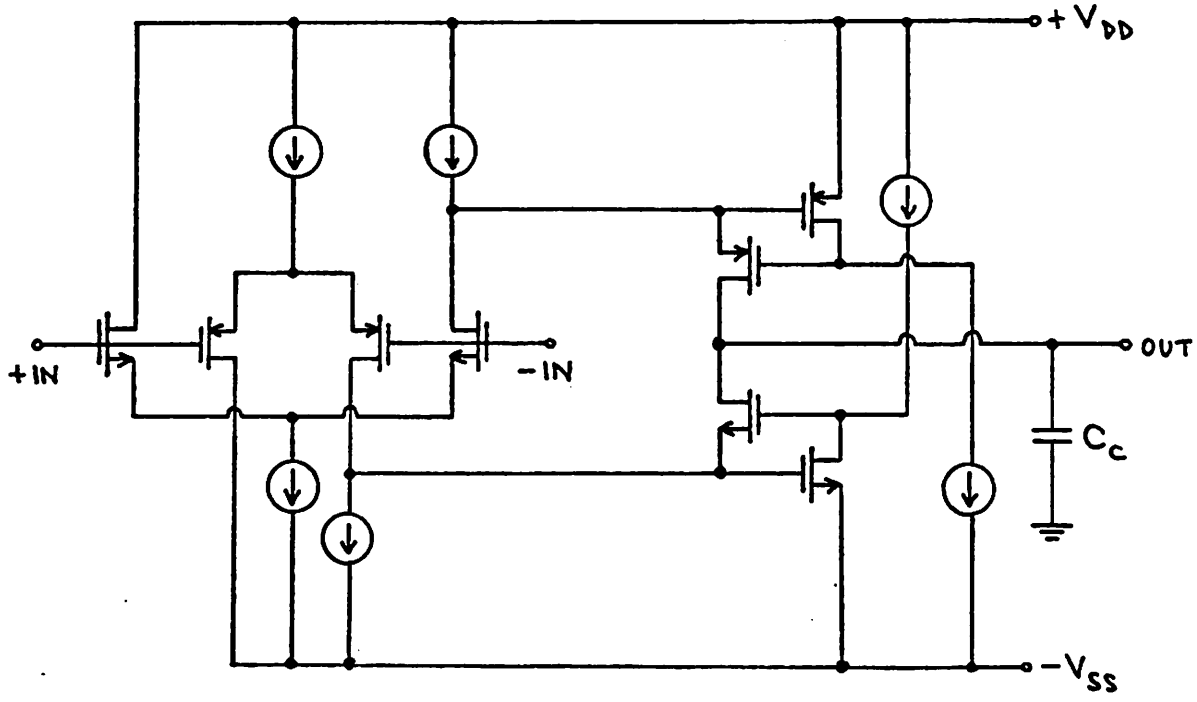


Figure 4.17: (a) CMOS high gain stage with complementary cascode
(b) Improved CMOS high gain stage



(c)

Figure 4.17.c: Improved CMOS high gain stage with diff.input

If the channel length modulation parameters λ for all transistors in the circuit are identical then the gain is approximately

$$A_v \simeq -4k'\sqrt{k'\left(\frac{W}{L}\right)_5\left(\frac{W}{L}\right)_6\left(\frac{W}{L}\right)_{10}}\;\frac{1}{\lambda^3 I_{D1}\sqrt{I_{D2}}} \tag{4.85}$$

The unity-gain bandwidth is given by the transconductance of the stage and the total capacitance at the output node:

$$GBW = \frac{g_{m5}}{2\pi C_C} \tag{4.86}$$

Figure 4.17c shows the same circuit as above but with a differential input.

4.4.2. Output stages

The simplest output stage for a MOS amplifier is a source follower (see Section 4.3.3). The output impedance of such output stage is usually gain by the transconductance of the top device, which will be low if (W/L) and the quiescent current are large.

An inverter can be used as the output stage as well if the output impedance is lowered by negative feedback. Figure 4.18a illustrates an example of a shunt-shunt feedback. The transresistance of the circuit is

$$R_{trans} = \frac{v_{out}}{i_{in}} = -\frac{g_{m1}(R_D \| r_{01})R_F}{1+g_{m1}(R_D \| r_{01})} \tag{4.87}$$

and the output impedance is

$$R_{out} = \frac{R_D \| r_{01}}{1+g_{m1}(R_D \| r_{01})} \tag{4.88}$$

Figure 4.18b shows a MOS realization of this circuit. The feedback resistor R_F has been replaced by the transistor M2 and the current source

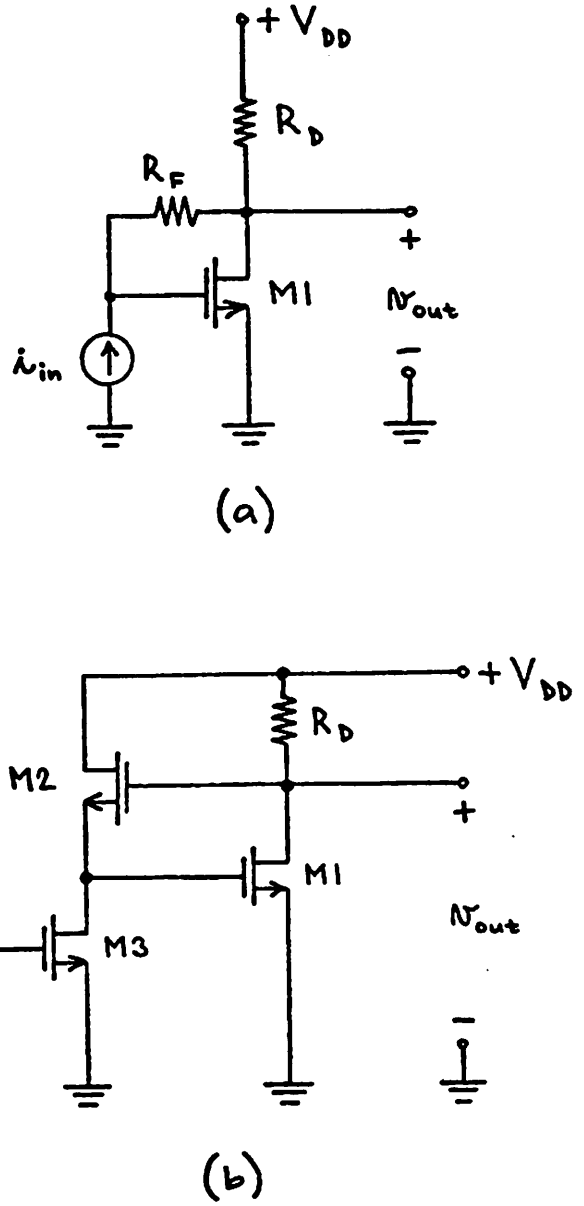


Figure 4.18: (a) Gain stage with resistor shunt-shunt feedback
(b) Gain stage with MOSFET shunt-shunt feedback

by the device M3. The voltage gain can be expressed as

$$A_V \cong \frac{g_{m3}}{g_{m2}} \frac{g_{m1}(R_D \| r_{01})}{1+g_{m1}(R_D \| r_{01})} \tag{4.89}$$

and the output impedance is again

$$R_{out} \cong \frac{R_D \| r_{01}}{1+g_{m1}(R_D \| r_{01})} \tag{4.90}$$

R_D can be any MOS load device or resistor. For large gain of the forward amplifier $[g_m(R_D \| r_{01}) >> 1]$ the relationships simplify to

$$A_V \approx \frac{g_{m3}}{g_{m2}} \tag{4.91}$$

and

$$R_{out} \approx \frac{1}{g_{m1}} \tag{4.92}$$

As far as CMOS output stages are concerned, the only commercially available operational amplifier which uses a CMOS output stage is CA3130 [54]. It is a simple CMOS inverter (Fig. 4.9) so that such an output stage has high output impedance and its gain is dependent on the load. Further the class A biasing depends on the power supply voltage.

Figure 4.19a shows a CMOS stage with series-shunt feedback. The calculation yields

$$A_V = \frac{v_{out}}{v_{in}} \approx 1 \tag{4.93}$$

and

$$R_{out} \approx \frac{g_{m3}}{g_{m5}} \left(\frac{1}{g_{m2}} + \frac{1}{g_{m4}}\right) \tag{4.94}$$

This stage does not give symmetrical linear voltage transfer curve

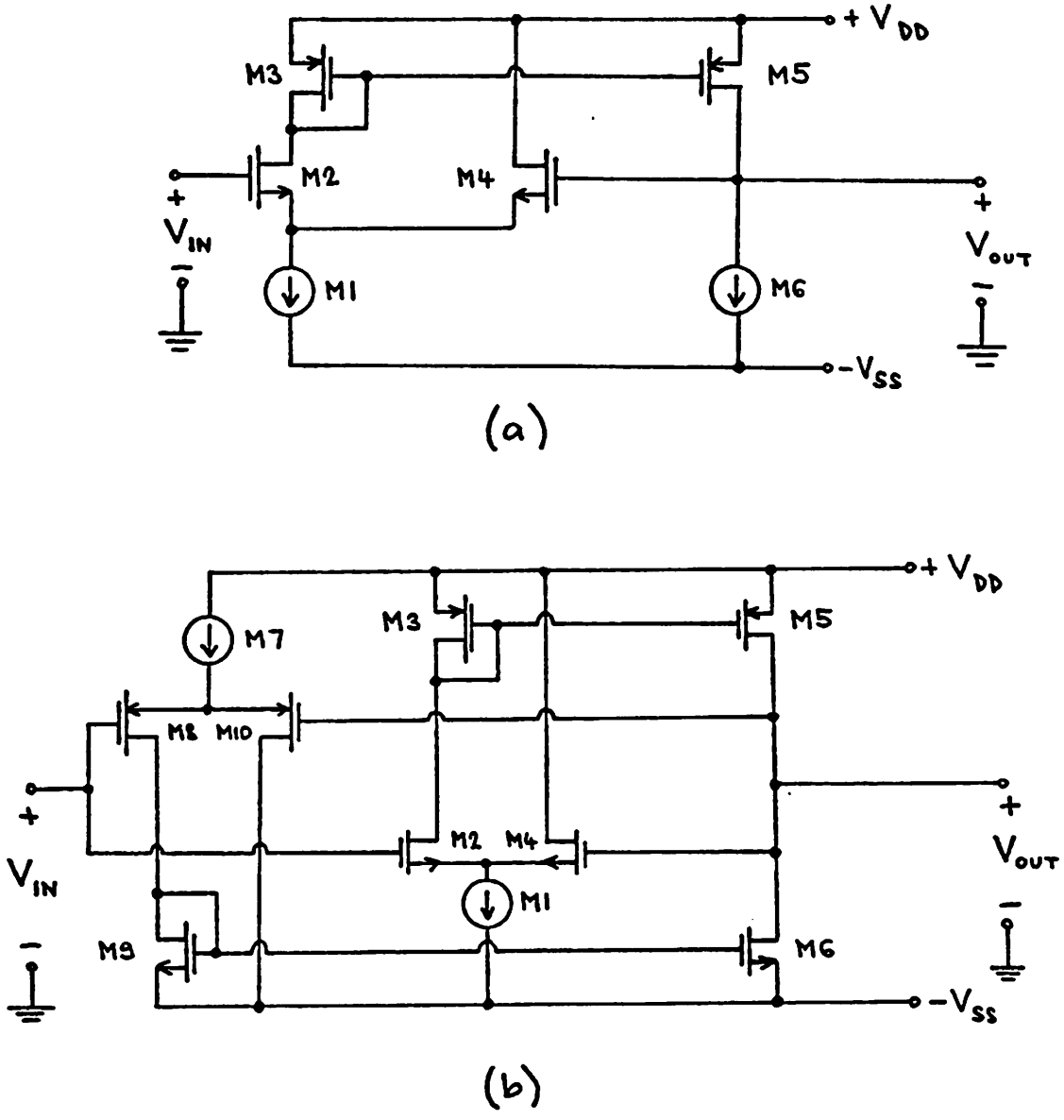


Figure 4.19: (a) CMOS output stage
(b) Complementary CMOS output stage

for positive and negative input signals. This can be solved by a complementary stage (see Fig. 4.19b). Computer simulations confirmed that such a stage has large bandwidth, large output swing and low output impedance.

4.5. Operational Amplifiers

In the preceding section some of the basic analog building blocks in MOS technology have been described. These blocks can be combined in different ways to realize a circuit with required performance characteristics. It has been shown in Chapter 3 that an operational amplifier connected as an integrator is needed as a building block for sampled data state variable filters.

An "ideal" operational amplifier could be defined as a voltage-controlled voltage source which offers infinite voltage gain, infinite input impedance and zero output impedance [8]. In this section we will analyze the overall performance and practical limitations of operational amplifiers that use stages we have discussed.

4.5.1. Gain and Frequency Response

In its most usual form an operational amplifier consists of several stages, such as differential input stage, gain stage, output stage etc. (Fig. 4.20a) [18]. When all intrinsic and parasitic MOSFET capacitances (see Fig. 4.4) are considered, then we obtain at least one pole for any stage discussed in Sections 4.3 and 4.4. This becomes clear from Fig. 4.20b: if R_T is the total impedance at the node A (including the loading of the following stage if any) and G_m is the total transconductance of the stage, then the voltage gain is

$$-A_V = \frac{V_{OUT}}{V_{IN}} = - G_m Z_T = - \frac{G_m R_T}{1+sC_T R_T} \qquad (4.95a)$$

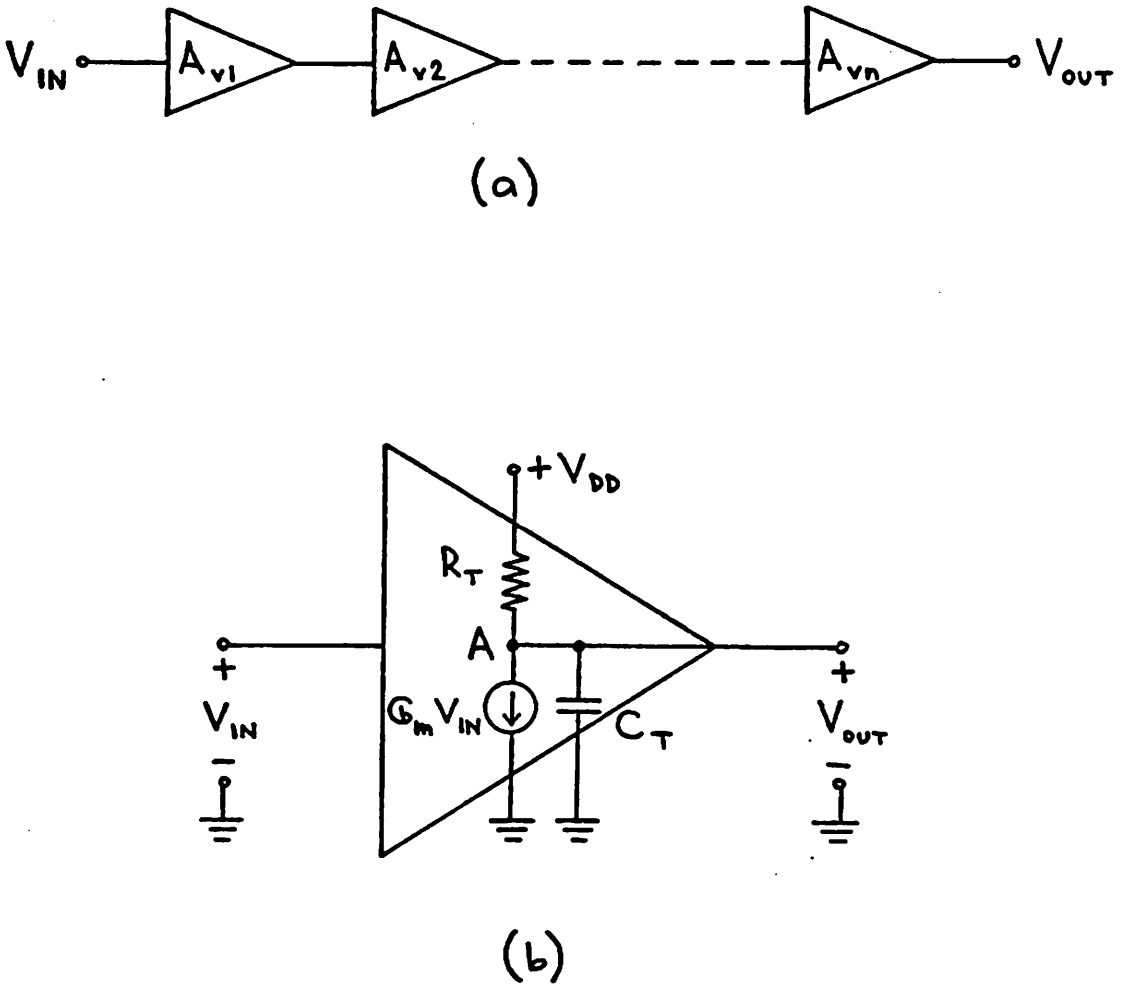


Figure 4.20: (a) Block diagram of a multistage amplifier
(b) Model of a gain stage

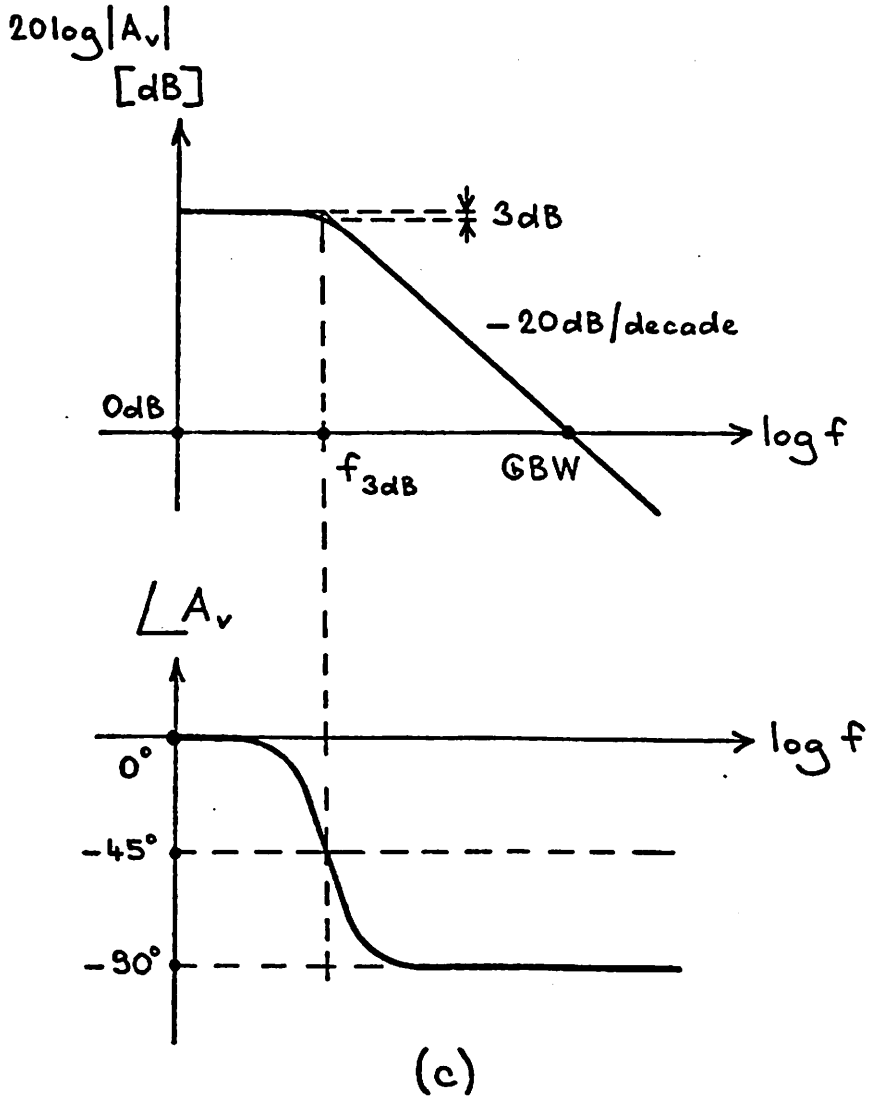


Figure 4.20.c: Bode diagram of the stage in b

The pole associated with this stage is given by

$$p = -\frac{1}{C_T R_T} \tag{4.95b}$$

Figure 4.20c shows the magnitude and phase response for the transfer function given by Eq. (4.95a) (so called Bode diagram). It can be seen that this function corresponds to a -20 dB/decade roll-off for frequencies in excess of f_{3dB} where f_{3dB} is

$$f_{3dB} = \left|\frac{p}{2\pi}\right| = \frac{1}{2\pi C_T R_T} \tag{4.96}$$

When we introduce DC voltage gain A_{vo}

$$|A_{VO}| = G_m R_T \tag{4.97}$$

and unity-gain bandwidth GBW, which is frequency for $|A_V| = 1$:

$$|A_V| = 1 = \left|\frac{A_{VO}}{1+j2\pi(GBW)C_T R_T}\right| \tag{4.98}$$

we can derive for the latter:

$$GBW \cong f_{3dB}|A_{VO}| = \frac{G_m}{2\pi C_T} \tag{4.99}$$

Based on the discussion in the Chapter 4.2, our conclusion is: the max. achievable unity-gain bandwidth is dependent on processing parameters, device geometry and power consumption.

The total voltage gain of the amplifier from Fig. 4.20a is

$$A_{vtot} = A_{v1}A_{v2}\cdots A_{vn} = \frac{A_{vo1}A_{vo2}\cdots A_{von}}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})\cdots(1+\frac{s}{p_n})} \tag{4.100}$$

It should be noted that one stage can have more poles than one. Generally it can be said that every node in the signal path will contribute one pole. However in practice some of these poles are at much higher frequency than the frequency of interest and therefore need not be considered. This becomes clear from Fig. 4.21 which shows the Bode diagram of a multistage amplifier. The range of frequencies we are interested in is usually only roughly up to GBW which is now of course not given by Eq. (4.99) any more.

4.5.2. Frequency Compensation

Consider an operational amplifier with open-loop total voltage gain $A_{vtot}(s)$ in a feedback configuration (Fig. 4.22) where the amount of feedback is represented by the feedback factor $\beta(s)$. The closed-loop gain is

$$A_{CL}(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = - \frac{A_{vtot}(s)}{1+\beta(s)A_{vtot}(s)} \tag{4.101}$$

Instability will result if the denominator of Eq. (4.101) becomes zero, as happens when

$$\beta(s)A_{vtot}(s) = 1\underline{/}\ 180° = -1 \tag{4.102}$$

Under this condition $A_{CL}(s)$ is infinite, indicating that an output results for no input signal and that this would produce self-sustaining oscillations. The instability can be avoided by limiting the phase shift of the feedback loop $\beta(s)A_{vtot}(s)$ to less than 180° when the loop gain $|\beta(s)A_{vtot}(s)| = 1$. This is usually accomplished by introducing a dominant pole low enough so that the frequency response has a roll-off -20dB per decade down to frequency, where $|\beta(s)A_{vtot}(s)| = 1$.

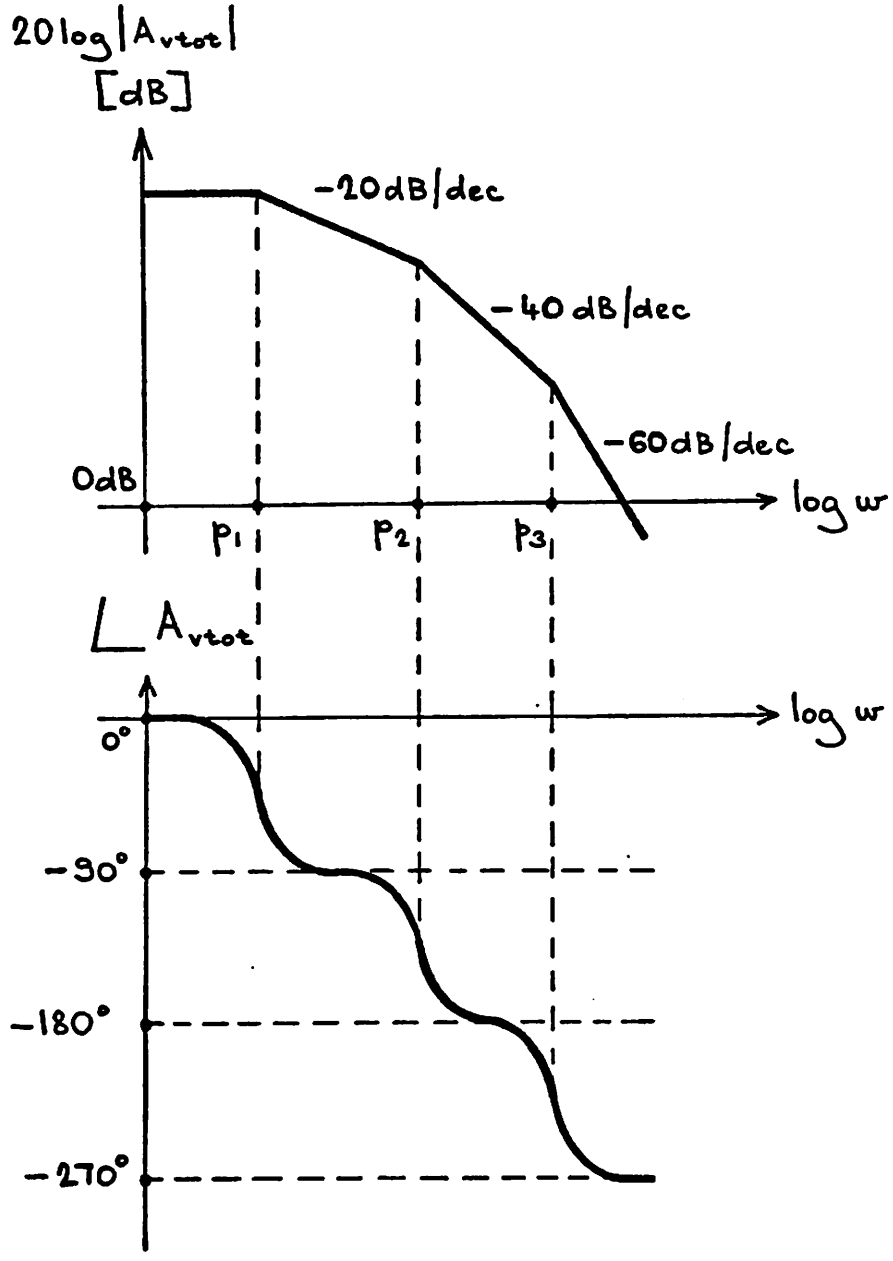


Figure 4.21: Bode diagram of a multistage amplifier

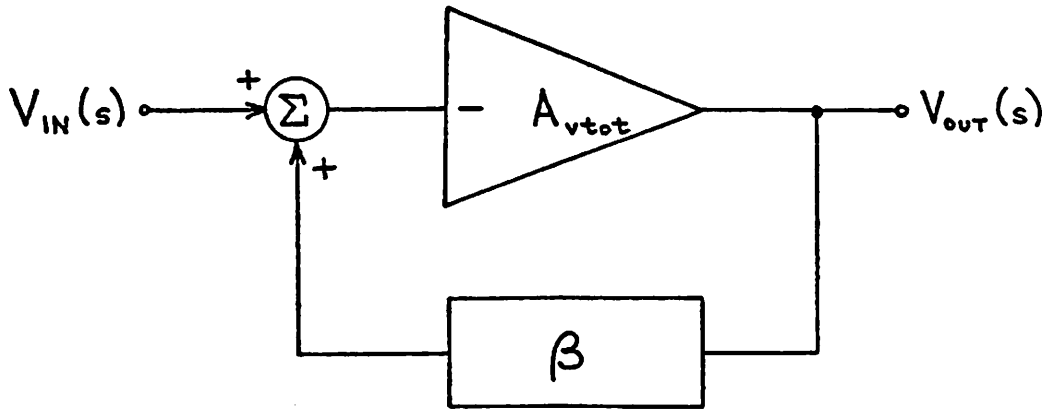


Figure 4.22: Operational amplifier with negative feedback

Because the realization of a low pole requires a large capacitance the most effective method used in monolithic bipolar operational amplifiers is the "pole-splitting" [37].

Consider Fig. 4.23a, where a general MOS amplifying stage with the transconductance G_m, the output impedance $R_0/(1+sC_0R_0)$ and the input capacitance C_{IN} is shown. The stage is driven from a voltage source with the source resistance R_{IN}. The voltage gain is

$$-A_V(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{-G_mR_0(1-\frac{sC_C}{G_m})}{s^2R_0R_{IN}(C_CC_0+C_{IN}C_0+C_{IN}C_C)+s[C_c((G_mR_0+1)R_{IN}+R_0)+R_{IN}C_{IN}+R_0C_0]+1} \tag{4.103}$$

The transfer function contains two poles which are given for $G_mR_0 >> 1$ approximately by

$$p_1 \simeq -\frac{1}{C_CR_{IN}G_mR_0} \tag{4.104a}$$

$$p_2 \simeq -\frac{C_CG_m}{C_CC_0+C_CC_{IN}+C_{IN}C_0} \tag{4.104b}$$

We note that p_1 is the dominant pole of the stage and it is due to the Miller effect. p_1 is inversely proportional to G_m and C_C, while p_2 is directly proportional to G_m and C_C. Thus the poles p_1 and p_2 are being "split-apart" by the increase capacitive feedback (Fig. 4.23b).

The transfer function contains a zero

$$z = \frac{G_m}{C_C} \tag{4.104c}$$

which, according to its sign, lies in the right half plane. The Bode diagram of the Eq. (4.103) suggests that it will be difficult to compensate this stage for use in feedback configurations (Fig. 4.23c).

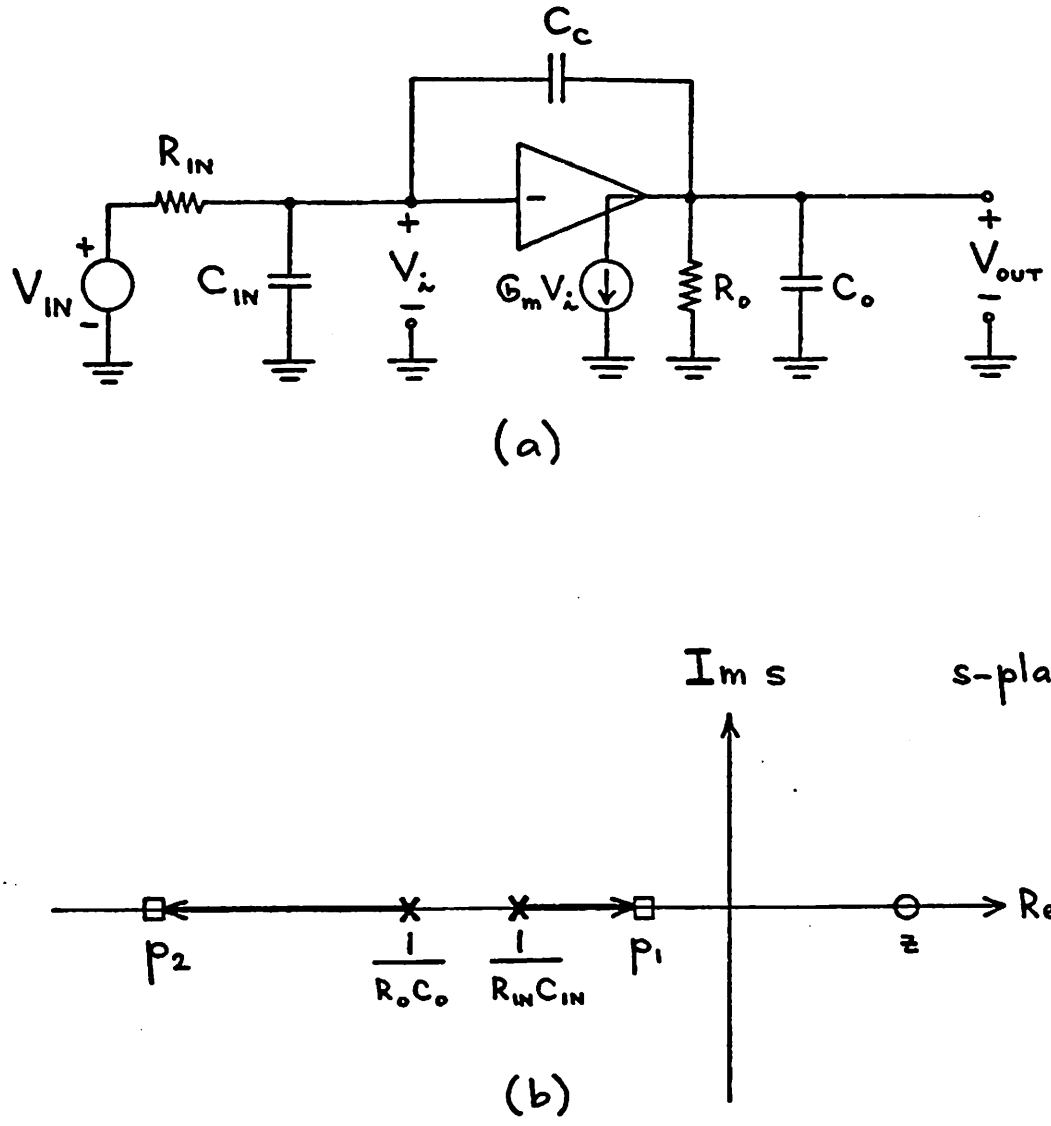


Figure 4.23: (a) General MOS amplifying stage with "pole-splitting" capacitor

(b) Root locus of the voltage gain for the circuit in a

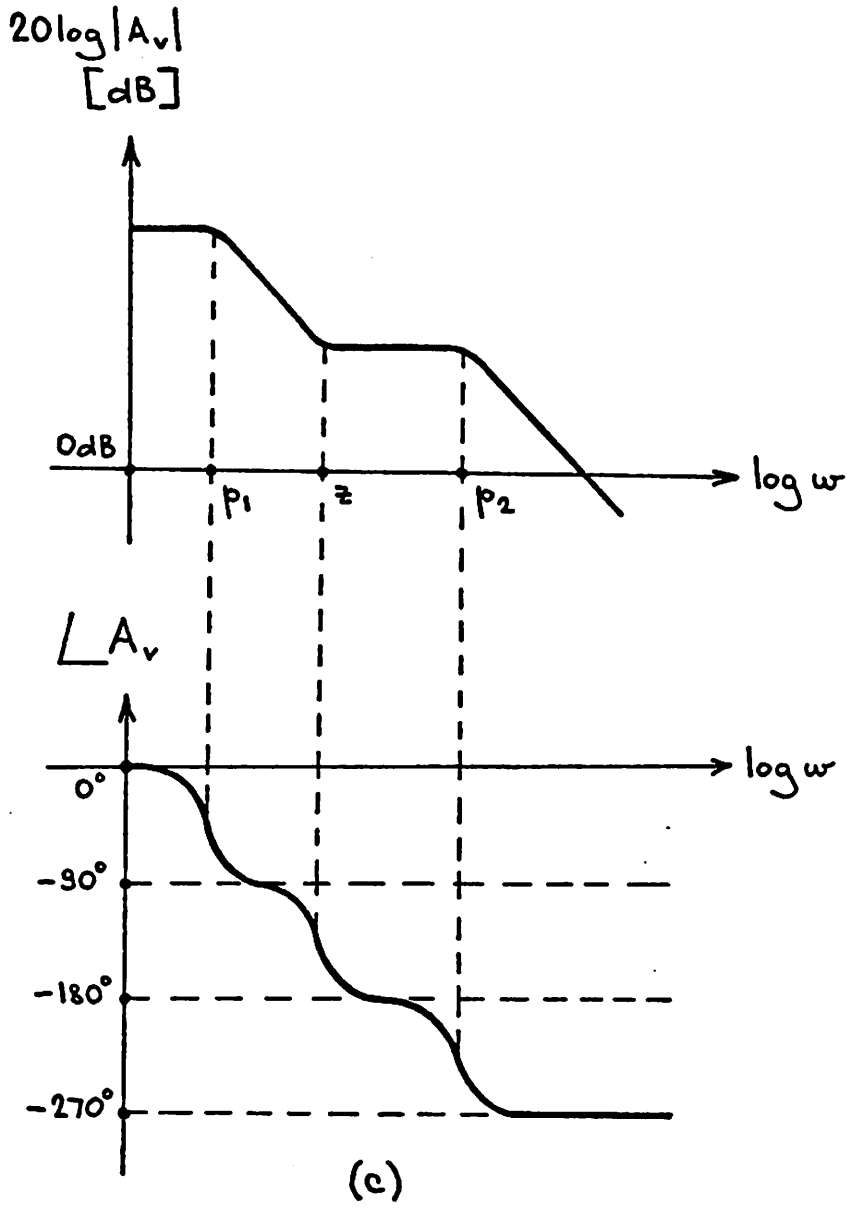


Figure 4.23.c: Bode diagram of the voltage gain for the circuit in a

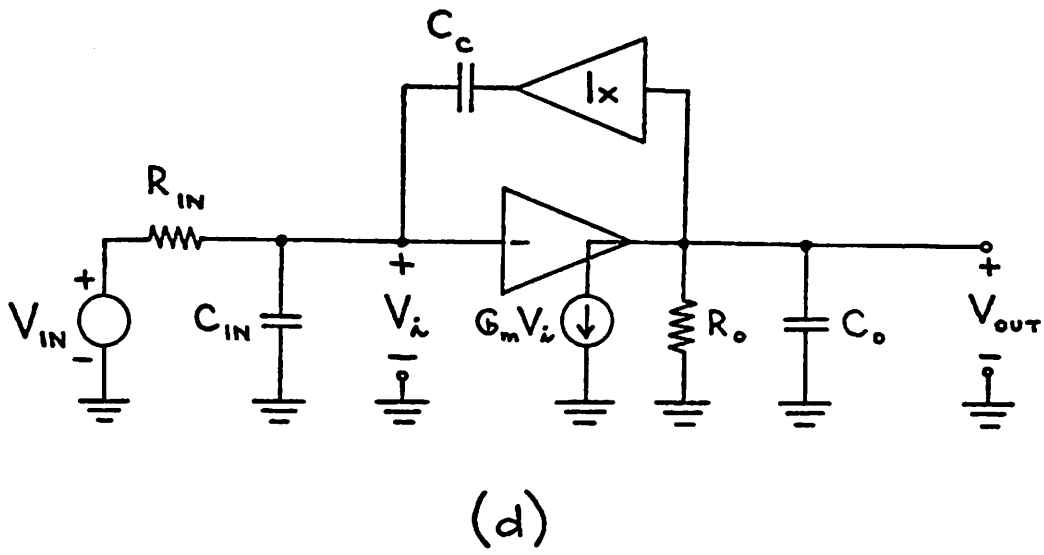


Figure 4.23.d: Circuit from a using a buffer to prevent signal feedthrough

A remedy to this is a unity-gain buffer in series with the compensation capacitor C_C which prevents the signal feedthrough and thus eliminates the right-half plane zero (see Fig. 4.23d) [23]. The new voltage transfer function is

$$-A_V(s) \simeq \frac{-G_m R_O}{s^2 R_O R_{IN}(C_O C_C + C_O C_{IN}) + s[C_C (G_m R_O + 1) R_{IN} + R_{IN} C_{IN} + R_O C_O] + 1} \qquad (4.105)$$

The poles have hardly changed:

$$p_1 \simeq -\frac{1}{C_C R_{IN} G_m R_O} \qquad (4.106a)$$

$$p_2 \simeq -\frac{C_C G_m}{C_C C_O + C_{IN} C_O} \qquad (4.106b)$$

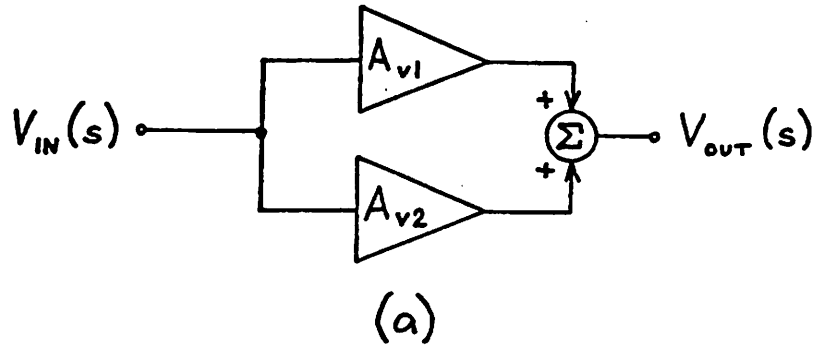
Another interesting way of phase compensation is the "feedforward compensation" which can be easily implemented in MOS amplifiers [38]. Figure 4.24a illustrates the principle of the feedforward compensation. Let us assume that A_{v1} is a high-gain, low-frequency amplifier with two poles and A_{v2} is a low-gain, high-frequency amplifier with one pole, so that

$$A_{v1} \simeq \frac{A_{v10}}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})} \qquad (4.107a)$$

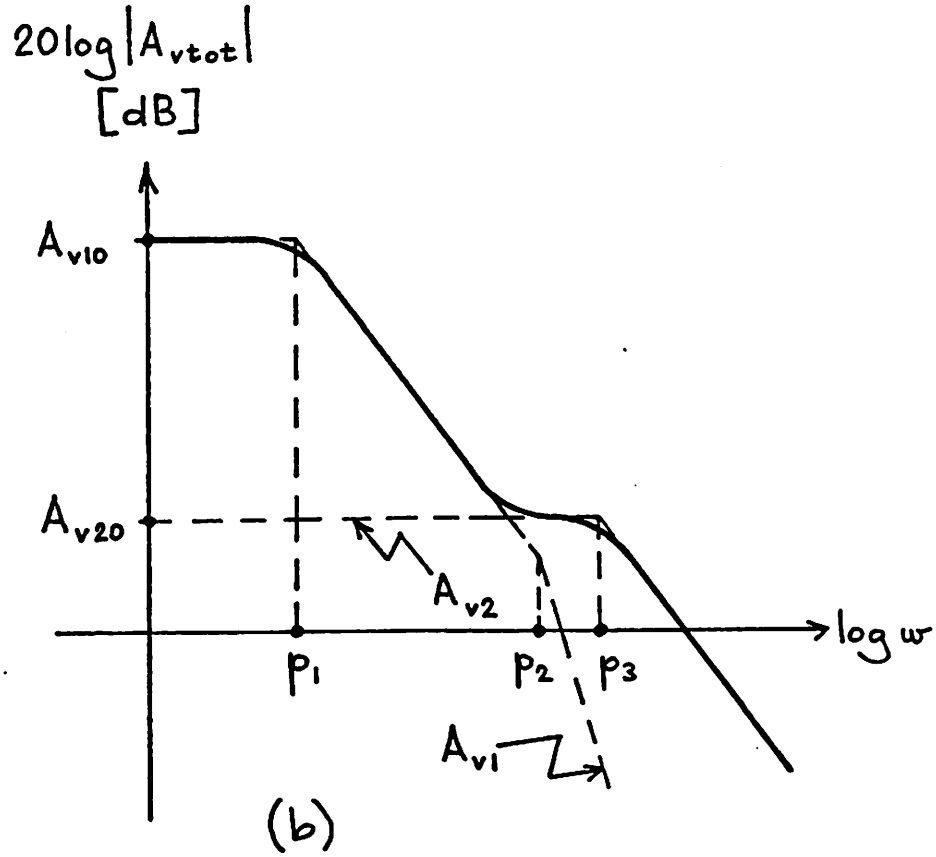
and

$$A_{v2} \simeq \frac{A_{v20}}{(1+\frac{s}{p_3})} \qquad (4.107b)$$

The feedforward amplifier A_{v2} provides a low-phase-shift path at high frequencies to maintain frequency stability (see Fig. 4.24b). The overall



(a)



(b)

Figure 4.24: (a) Block diagram of the feedforward compensation
(b) Bode diagram of a

amplifier gain is

$$A_{vtot} = A_{V10} + A_{V20}$$

$$= (A_{V10}+A_{V20}) \frac{\frac{s^2}{p_1p_2}\left(\frac{A_{V20}}{A_{V10}+A_{V20}}\right)+ \frac{s}{A_{V10}+A_{V20}}\left(\frac{A_{V10}}{p_3} + \frac{A_{V20}}{p_1} + \frac{A_{V20}}{p_2}\right) + 1}{\left(1+ \frac{s}{p_1}\right)\left(1+ \frac{s}{p_2}\right)\left(1+ \frac{s}{p_3}\right)}$$

$$= (A_{V10}+A_{V20}) \frac{\left(1+ \frac{s}{z_1}\right)\left(1+ \frac{s}{z_2}\right)}{\left(1+ \frac{s}{p_1}\right)\left(1+ \frac{s}{p_2}\right)\left(1+ \frac{s}{p_3}\right)} \qquad (4.108)$$

where

$$z_{1,2} = - \frac{1}{2}\left(\frac{A_{V10}}{A_{V20}} \frac{p_1p_2}{p_3} + p_1+p_2\right)$$

$$\pm \sqrt{\frac{1}{4}\left(\frac{A_{V10}}{A_{V20}} \frac{p_1p_2}{p_3} + p_1+p_2\right)^2 - p_1p_2\left(\frac{A_{V10}}{A_{V20}} +1\right)} \qquad (4.109a)$$

The feedforward amplifier A_{V2} has introduced two new zeros which help to compensate the whole amplifier. However if the phase shift in the high-gain amplifier A_{V1} approaches -180° at the transition from one response to the other, the two signals can be of opposite phase and the overall response would have a notch.

4.5.3. Input Offset Voltage

The input offset voltage is the DC input voltage which must be applied across the input terminals of an operational amplifier to obtain zero output voltage [8]. In the same way we can define an input offset voltage for each individual stage. Thus V_{os1} is the input offset voltage of the 1st stage, V_{os2} of the 2nd state, etc.

When cascading these stages to realize a multistage amplifier (Fig. 4.25a), we are interested in the input offset voltage of the whole amplifier. From Fig. 4.25a we will find that the output voltage due to offset voltage contribution of each individual stage is

$$V_{OUT} = ((V_{os1}A_{V1}+V_{os2})A_{V2}+V_{os3})A_{V3} + \ldots \tag{4.110a}$$

where A_{V1} is the voltage gain of the 1st stage, A_{V2} is the gain of the 2nd stage, etc. The voltage referred to the amplifier input yields the total input offset voltage of the operational amplifier:

$$V_{os,tot} = \frac{V_{OUT}}{A_{vtot}} = V_{os1} + \frac{V_{os2}}{A_{V1}} + \frac{V_{os3}}{A_{V1}A_{V2}} + \ldots \tag{4.110b}$$

where $A_{vtot} = A_{V1}A_{V2}A_{V3} \ldots$. Figure 4.25b shows $V_{os,tot}$ as the total input offset voltage of the amplifier.

The input stage obviously contributes most of the total input offset voltage because it is not reduced by any voltage gain.

Figure 4.26a shows a typical differential input stage with depletion load devices. First consider a mismatch of the input driver transistors M1 and M2. Then an offset voltage has to be applied to the input so that the currents in M1 and M2 are equal:

$$V_{os} = V_{Gs1} - V_{Gs2} \tag{4.111a}$$

where

$$V_{Gs1} \approx V_{T1} + \sqrt{\frac{I_D}{k_1}} \tag{4.111b}$$

and

$$V_{Gs2} \approx V_{T2} + \sqrt{\frac{I_D}{k_2}} \tag{4.111c}$$

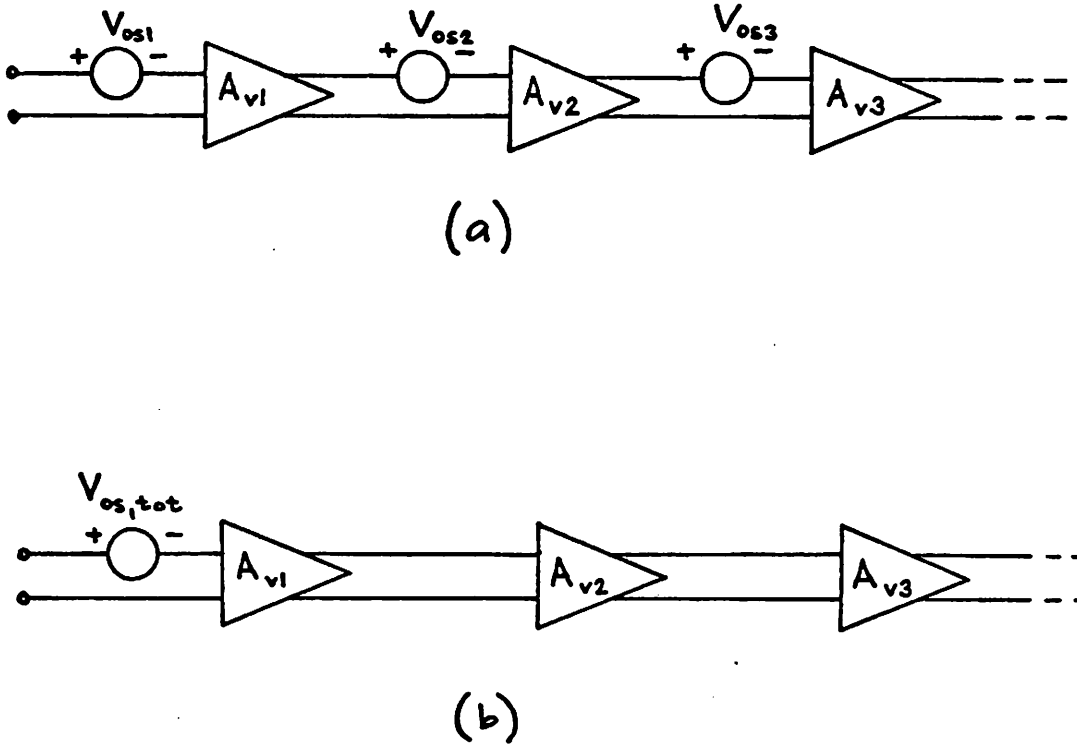


Figure 4.25: (a) The input offset voltages of individual stages in an operational amplifier
(b) The total input offset voltage of an operational amplifier

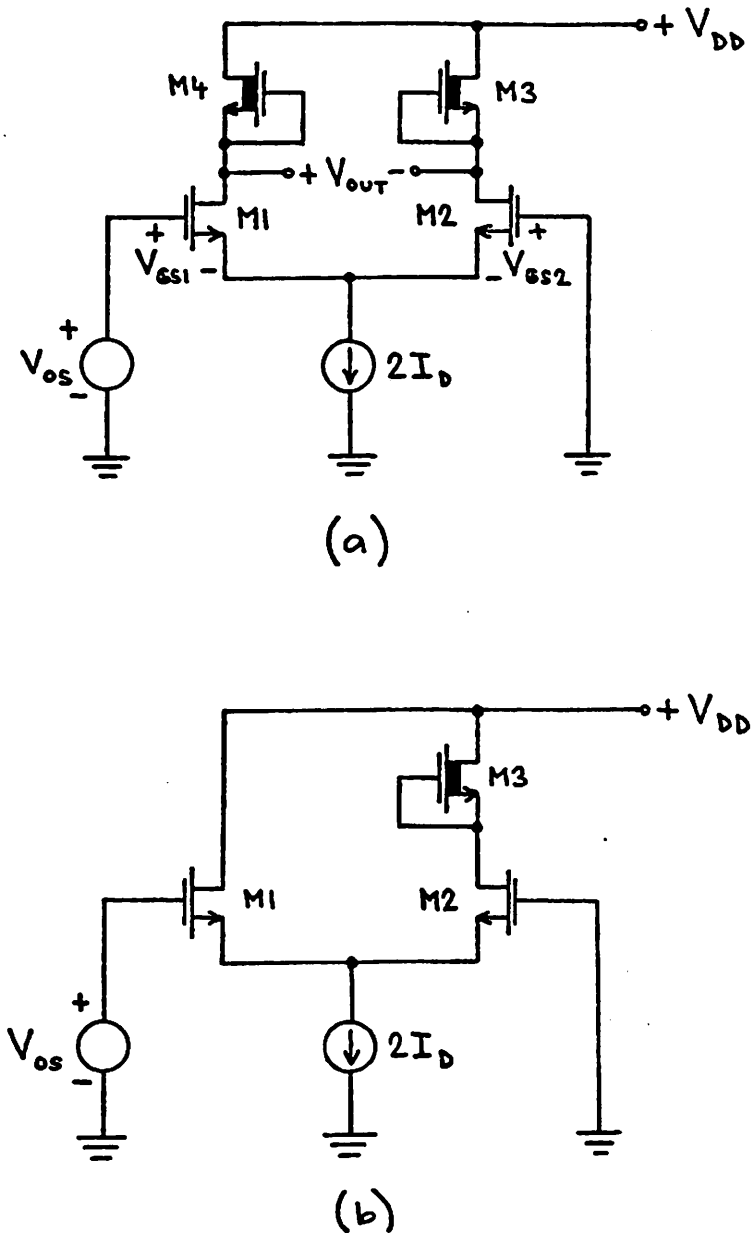


Figure 4.26: (a) A differential input stage with depletion loads
(b) A differential input stage with assymetrical load

when neglecting the channel length modulation. Let us assume that the mismatch is very small. Then the conduction factors k can be expressed as

$$k_1 = k_{driver} \tag{4.112a}$$

$$k_2 = k_{driver} + \Delta k_{driver} \tag{4.112b}$$

where $\frac{\Delta k_{driver}}{k_{driver}} << 1$. The input offset voltage due to the threshold voltage mismatch is

$$V_{os1} = V_{T1} - V_{T2} = \Delta V_T \tag{4.113}$$

The input offset voltage due to the conduction factor mismatch can be calculated using Eq. (4.111) and (4.112) as

$$V_{os2} = \sqrt{\frac{I_D}{k_1}} - \sqrt{\frac{I_D}{k_2}} \simeq \frac{1}{2}\sqrt{\frac{I_D}{k_{driver}}}\left|\frac{\Delta k_{driver}}{k_{driver}}\right| \tag{4.114}$$

The typical input offset voltage of MOS matched pairs is of the order of 10 to 20 mV [39]. This is about an order of magnitude higher than offset voltage of bipolar matched pairs.

The load mismatch is given by the mismatch of the load transistors M3 and M4 which will cause unbalanced currents in M1 and M2:

$$\left|\frac{\Delta I_D}{I_D}\right| = \left|\frac{\Delta k_{load}}{k_{load}}\right| + 2\left|\frac{\Delta V_{Tload}}{V_{Tload}}\right| \tag{4.115}$$

The input offset voltage V_{os3} has to make V_{OUT} equal to zero:

$$V_{os3} = \sqrt{\frac{I_D+\Delta I_D}{k_{driver}}} - \sqrt{\frac{I_D}{k_{driver}}} \approx \frac{1}{2}\sqrt{\frac{I_D}{k_{driver}}}\left|\frac{\Delta I_D}{I_D}\right|$$

$$= \sqrt{\frac{I_D}{k_{driver}}}\left(\frac{1}{2}\left|\frac{\Delta k_{load}}{k_{load}}\right| + \left|\frac{\Delta V_{Tload}}{V_{Tload}}\right|\right) \qquad (4.116)$$

It is necessary to realize that the offset voltages we have derived are random quantities, that is to say, there will be some statistical distribution of these offset voltages. Unless there is a systematic component in the input offset voltage due to the design, the mean of V_{os} will be zero and the standard derivation can be estimated as

$$V_{os} = \sqrt{V_{os1}^2+V_{os2}^2+V_{os}^3} \qquad (4.117)$$

A systematic component of the input offset voltage could be caused for example by assymetrical loading of the input drivers M1 and M2 (Fig. 4.26b). Assuming that the input driver pair M1, M2 is ideally matched we can write

$$V_{os4} = \sqrt{\frac{I_D}{k_{driver}}}\left(\frac{1}{\sqrt{1+\lambda V_{DS2}}} - \frac{1}{\sqrt{1+\lambda V_{DS1}}}\right) \approx \sqrt{\frac{I_D}{k_{driver}}}\frac{\lambda}{2}(V_{DS1}-V_{DS2}) \qquad (4.118)$$

4.5.4. Equivalent Input Noise Voltage

Compared to bipolar transistors, MOSFET equivalent input noise can be much higher, particularly the 1/f component. The noise current at the drain of the MOSFET is comprised of thermal noise and 1/f (or "flicker") noise. The noise model of the MOSFET is shown in Fig. 4.27a [40] where

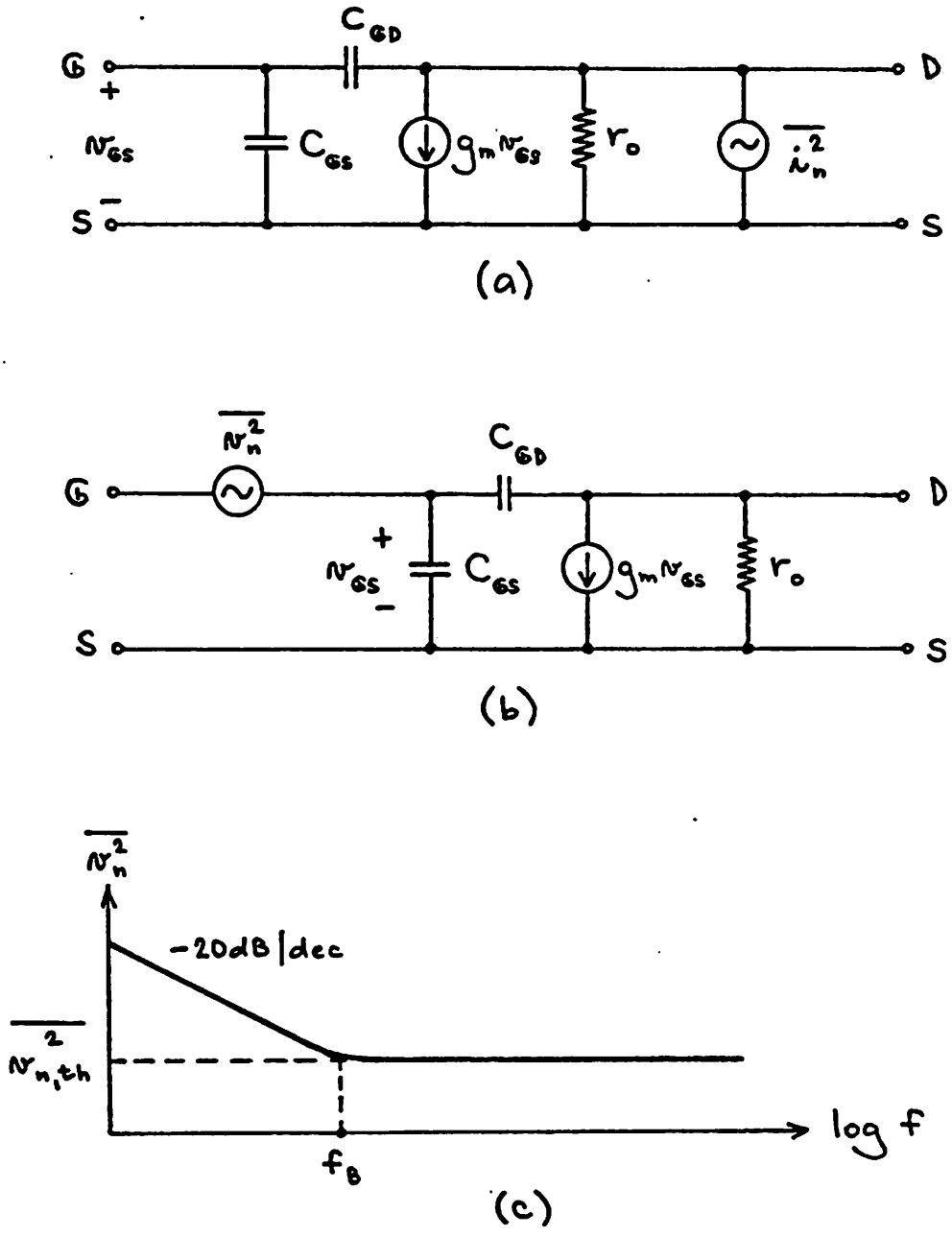
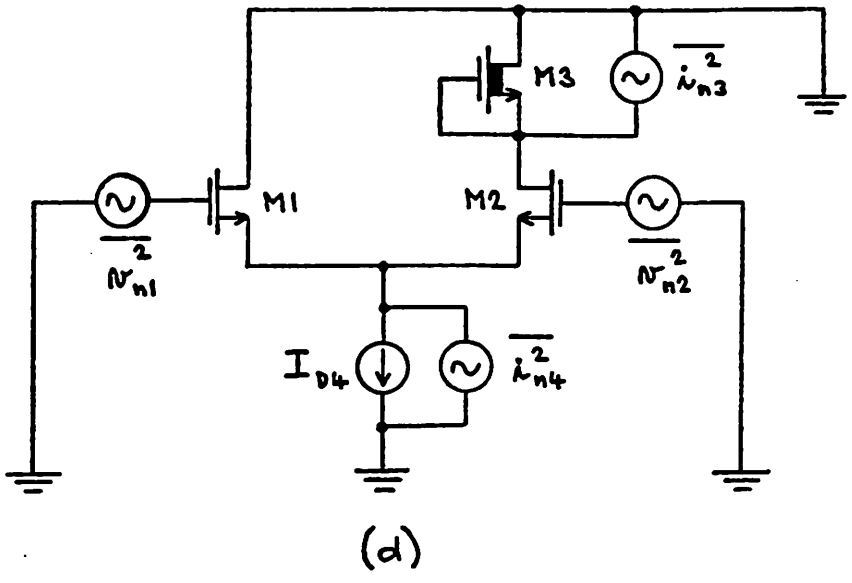
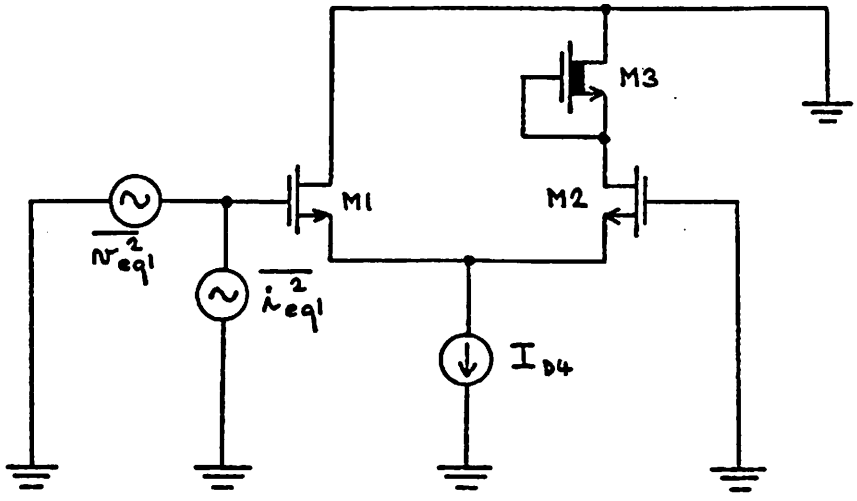


Figure 4.27: (a) Noise model for a MOSFET
(b) Equivalent input noise voltage model of a
(c) Equivalent input noise voltage of a MOSFET vs. frequency



(d)



(e)

Figure 4.27: (d) Noise model of a differential input stage
(e) Equivalent input noise voltage model of d

$$\overline{i_n^2} = 4kT\left(\frac{2}{3} g_m\right) df + \frac{KI_D^a}{f^b} df \tag{4.119a}$$

where k is Boltzmann's constant

T temperature

g_m transconductance

df bandwidth

K device constant

I_D quiescent current

a device constant

b device constant

We are very often interested in the equivalent input noise voltage at the gate of the MOS transistor. Such a model is shown in Fig. 4.27b where

$$\overline{v_n^2} = 4kT\left(\frac{2}{3g_m}\right) df + \frac{KI_D^a}{f^b g_m^2} df \tag{4.119b}$$

To simplify our noise calculations we approximate Eq. (4.119b) by a following expression:

$$\overline{v_n^2} = \overline{v_{n,th}^2}\left(1+\frac{f_B}{f}\right) \tag{4.120}$$

where $\overline{v_{n,th}^2}$ is the thermal noise and f_B is the flicker noise corner frequency (Fig. 4.27c). f_B ranges between 10 kHz for low current levels to 100 kHz at high current levels [41].

A useful technique for the estimation of circuit noise performance is the referral of all noise to the circuit input. An example of calculation of the equivalent input noise of a circuit can be shown for

a differential stage of Fig. 4.27d. The equivalent input noise voltage of this differential stage is

$$\overline{v_{eq1}^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2} + \frac{\overline{i_{n3}^2}}{g_{m2}^2} \tag{4.121a}$$

and the equivalent input noise current is

$$\overline{i_{eq1}^2} = 0 \tag{4.121b}$$

The equivalent circuit is shown in Fig. 4.27e.

If each stage is modelled with its own equivalent input noise voltage (similarly to input offset voltage (see Section 4.5.3) then the total equivalent input noise voltage of a multistage amplifier is given by

$$\overline{v_{eq,tot}^2} = \overline{v_{eq1}^2} + \frac{\overline{v_{eq2}^2}}{A_1^2(\omega)} + \frac{\overline{v_{eq3}^2}}{[A_1(\omega)A_2(\omega)]^2} + \ldots \tag{4.122}$$

where $\overline{v_{eq1}^2}$ is the equivalent input noise voltage of the 1st stage, $\overline{v_{eq2}^2}$ of the 2nd stage, etc.

Note that while the equivalent input noise voltage of the input stage is dominant at low frequencies other noise sources can become dominant at high frequencies if the gain falls off with frequency. For this reason frequency compensation should be placed as close to the output of a multistage amplifier as possible.

4.5.5. Harmonic Distortion

An MOS transistor in the saturation region has ideally a square law transfer characteristic given by Eq. (4.2). Thus, all third order

distortion is ideally zero (neglecting body effect).

Consider MOS enhancement driver-depletion load pair of Fig. 4.8a. The DC transfer characteristic given by Eq. (4.26) is nonlinear. If $V_{IN,DC}$ is a DC bias voltage and v_{in} is the signal input, the output voltage is $V_{OUT} = V_{OUT,DC} + v_{out}$. $V_{OUT,DC}$ is the DC component of the output voltage and v_{out} is the signal output. This allows us to simplify Eq. (4.26) and express it as a part of power series:

$$v_{out} = a_1 v_{in} + a_2 v_{in}^2 \tag{4.123}$$

where

$$a_1 = \left(-\frac{2}{\gamma_2}\right)\sqrt{\frac{\left(\frac{W}{\ell}\right)_1}{\left(\frac{W}{\ell}\right)_2}}\sqrt{\phi_{B2}+V_{BB}+V_{OUT,DC}} \tag{4.124a}$$

$$a_2 = \frac{1}{\gamma_2}\frac{\left(\frac{W}{\ell}\right)_1}{\left(\frac{W}{\ell}\right)_2} \tag{4.124b}$$

The a_1 term can be recognized as the small signal voltage gain used in linear analysis (see Eq. (4.25)).

If a single sinusoidal input signal is applied to the circuit

$$v_{in} = V_1 \cos \omega_1 t \tag{4.125}$$

the output signal is

$$v_{out} = a_1 V_1 \cos \omega_1 t + \frac{1}{2} a_2 V_1^2 (\cos 2\omega_1 t + 1)$$

Fractional second harmonic distortion is defined as

$$HD_2 = \frac{\text{amplitude of second harmonic distortion signal}}{\text{amplitude of fundamental}}$$

For small distortion, this can be expressed as

$$HD_2 = \frac{1}{2}\frac{a_2}{a_1} V_1 \tag{4.126}$$

The distortion is usually referred to the output signal level. If $V_{out,pp}$ is the peak-to-peak value of the fundamental signal (at frequency ω_1) in the output then

$$V_{out,pp} \simeq 2a_1 V_1 \tag{4.127}$$

Using Eq. (4.127) in Eq. (4.126) gives

$$HD_2 = \frac{1}{4}\frac{a_2}{a_1^2} V_{out,pp} \tag{4.128}$$

Hence

$$HD_2 = \frac{1}{16}\frac{V_{out,pp}}{\phi_{B2}+V_{BB}+V_{OUT,DC}} \tag{4.129}$$

Since there is not any other harmonic distortion, HD_2 represents the total harmonic distortion.

When one of the devices enters the linear region, the harmonic distortion will substantially above the value given by Eq. (4.129).

4.6. Conclusions

The main problem encountered in single channel MOS analog circuit design is the limited voltage gain per stage. Further, designer's choice is restrained by the lack of availability of complementary devices. The single channel MOS process (NMOS or PMOS), however, is a very simple one: It requires only four masking steps unless channel stops are necessary (the channel stop technique requires an extra masking step). Maximum practical voltage gain per stage is about 10-15 if only enhancement load devices are used.

This gain can be increased substantially through use of depletion load devices or CMOS stages. Two cascaded MOS gain stages can provide voltage gains of 1000 to 10000 [39].

The implantation of boron in P-channel, or phosphorous in N-channel, is the usual way to create depletion type devices. It is a noncritical step and requires very simple masking [44]. CMOS processes, on the other hand, are one of the most sophisticated of MOS processes. It requires at least six masking steps, including the critical "well" diffusion [34]. These deep, low doping concentration diffusions are necessary for opposite polarity transistors. The output resistance of these devices will be low due to low doping concentration of the well. In addition, the density is rather poor because double guarding rings are usually necessary to prevent field inversion.

Thus, unless a high performance CMOS process combining high breakdown voltage with high output resistance is used [36], a CMOS process does not offer any significant advantage, which would justify use of such complex technology.

CHAPTER 5

PRACTICAL DESIGN OF ANALOG SAMPLED DATA RECURSIVE FILTERS

5.1. Practical Design Considerations

In this section we investigate second order effects, such as operational amplifier limitations, parasitic capacitances, etc. Furthermore we will evaluate the role these effects play in the design and performance of analog sampled data recursive filters.

The first part will be devoted to operational amplifier limitations, such as open-loop gain, offset, output swing, noise and distortion. Since our discussion is limited to all-MOS amplifiers we will not consider any input-bias or input-offset currents.

The second part will examine limitations imposed by use of MOSFET switches. We will study and evaluate effects of "on" resistance of the switches, clock feedthrough, junction capacitance and leakage and MOSFET noise.

In the third part, errors due to MOS capacitor mismatch, thin oxide gradients, metal interconnect, package parasitics and voltage dependence of MOS capacitors will be investigated.

5.1.1. Amplifier Open-Loop Gain

By and large, the most important property of real operational amplifiers used in analog filters is its finite, frequency-dependent gain. Our discussion will be of course limited to the operational amplifiers connected as integrators due to our specific topic.

Consider the integrator shown in Fig. 5.1a. If the finite gain and bandwidth of the amplifier are taken into account, their effects

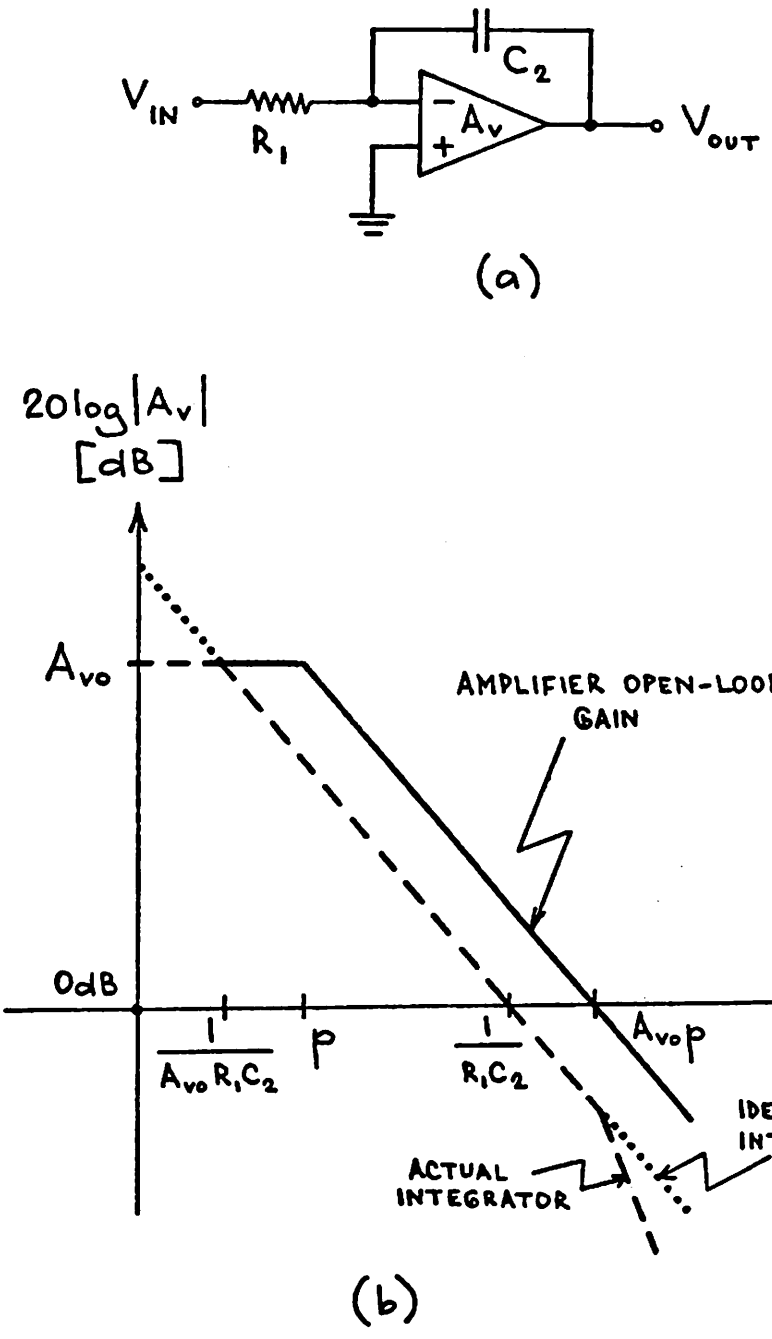
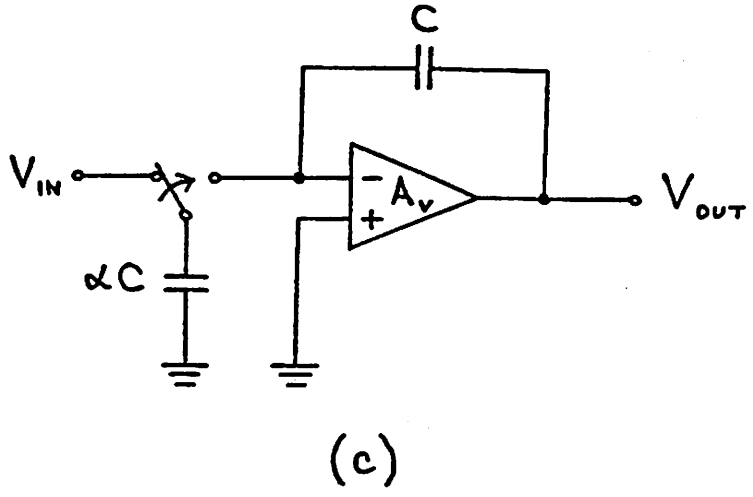


Figure 5.1: (a) A conventional integrator
(b) Bode diagram of b



(c)

Figure 5.1.c: A sampled data integrator

on the integrator response may be evaluated [18]. The open-loop frequency response of the amplifier is approximated by a single pole p and a low-frequency gain of A_{V0}:

$$A_V = \frac{A_{V0}}{1+\frac{s}{p}} \tag{5.1}$$

The resulting integrator response function is approximately

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} \approx -\frac{A_{V0}}{(1+\frac{s}{A_{V0}p})(1+sA_{V0}R_1C_2)} \tag{5.2}$$

if $A_{V0} >> 1$ and $(A_{V0}R_1C_2) >> 1/p$. This function has two poles on the real axis while the ideal integrator has a single pole at the origin. In Fig. 5.1b the frequency response of this actual integrator is compared with the response of an ideal integrator which is given by

$$H(s) = -\frac{1}{sR_1C_2} \tag{5.3}$$

At the low frequencies the response of the real integrator departs from the ideal one due to the finite gain A_{V0}. At high frequencies the departure is due to the finite amplifier bandwidth.

In Fig. 5.1c the resistor, R_1, in the integrator has been replaced by the switched capacitor circuit of Fig. 3.1a with $\alpha C = 1/(f_c R_1)$. It is the same integrator as in Fig. 3.5b but with a finite gain A_V, $C_1 = \alpha C$ and $C_2 = C$. We will assume an amplifier with an infinite bandwidth ($p=\infty$) first. The charge conservation equation can be derived similarly to Eq. (3.26):

$$C(1+\frac{1}{A_V})\, V_{out}[nT_c] + \frac{\alpha C}{A_V} V_{out}[nT_c) = C(1+\frac{1}{A_V})V_{out}[(n-1)T_c] - \alpha C V_{in}[(n-1)T_c] \tag{5.3}$$

The z-transform technique yields the transfer function

$$H(z) = - \frac{\frac{A_V}{A_V+1+\alpha} z^{-1}}{1- \frac{A_V+1}{A_V+1+\alpha} z^{-1}} \tag{5.4}$$

To simplify this equation we introduce

$$\gamma = \frac{A_V}{A_V+1+\alpha} \tag{5.5a}$$

and

$$\eta = \frac{A_V+1}{A_V+1+\alpha} \tag{5.5b}$$

and write

$$H(z) = - \frac{\alpha\gamma z^{-1}}{1-\eta z^{-1}} \tag{5.6}$$

Thus the Eq. (3.27) is not valid any more and filter transfer functions and design equations have to be modified when a finite amplifier gain is included.

The transfer function of an ideal sampled data integrator given by Eq. (3.27) is for $\alpha = C_1/C_2$

$$H(z) = - \frac{\alpha z^{-1}}{1-z^{-1}} \tag{5.7}$$

The magnitude is then

$$|H(\omega)| = \frac{\alpha}{\sqrt{2(1-\cos \omega T_c)}} \tag{5.8}$$

The magnitude of the transfer function given by Eq. (5.6) is

$$|H(\omega)| = \frac{\alpha\gamma}{\sqrt{(1+\eta^2)-2\eta \cos \omega T_c}} \tag{5.9}$$

The pole of this real sampled data integrator is not at the origin but is approximately at $\alpha f_c/A_V$. The max. magnitude is A_V, i.e. the amplifier gain.

So far we have considered the gain indpendent of frequency. The frequency dependent gain will raise question of stability. Figure 5.2a shows the Bode diagram of a operational amplifier connected as a sampled data integrator. The feedback factor β is determined by capacitor ratio seen in Fig. 5.2b (see Eq. 5.14):

$$\beta = \frac{C}{\alpha C+C} = \frac{1}{\alpha+1} \tag{5.10}$$

The worst case will occur, however, when the switch is thrown to the left, as shown in Fig. 5.2c. The feedback factor is then

$$\beta' = \frac{C}{C_{par}+C} \tag{5.11}$$

and it is determined by the parasitic capacitance at the inverting input of the amplifier C_{par} and the feedback capacitor C. Usually $\beta' > \beta$.

It is known from Section 4.5.2 that a feedback configuration is stable if the phase shift of the feedback loop is less than 180° at the frequency where $|\beta A_V| = 1$. This can be found by plotting $|1/\beta|$ in the Bode diagram of $|A_V|$ as shown in Fig. 5.2a. The derivation of this procedure is very simple:

$$20 \log |\beta A_V| = 20 \log |A_V| - 20 \log \left|\frac{1}{\beta}\right| \tag{51.2}$$

The difference between 180° and the phase shift at $|\beta A_V| = 1$ mentioned

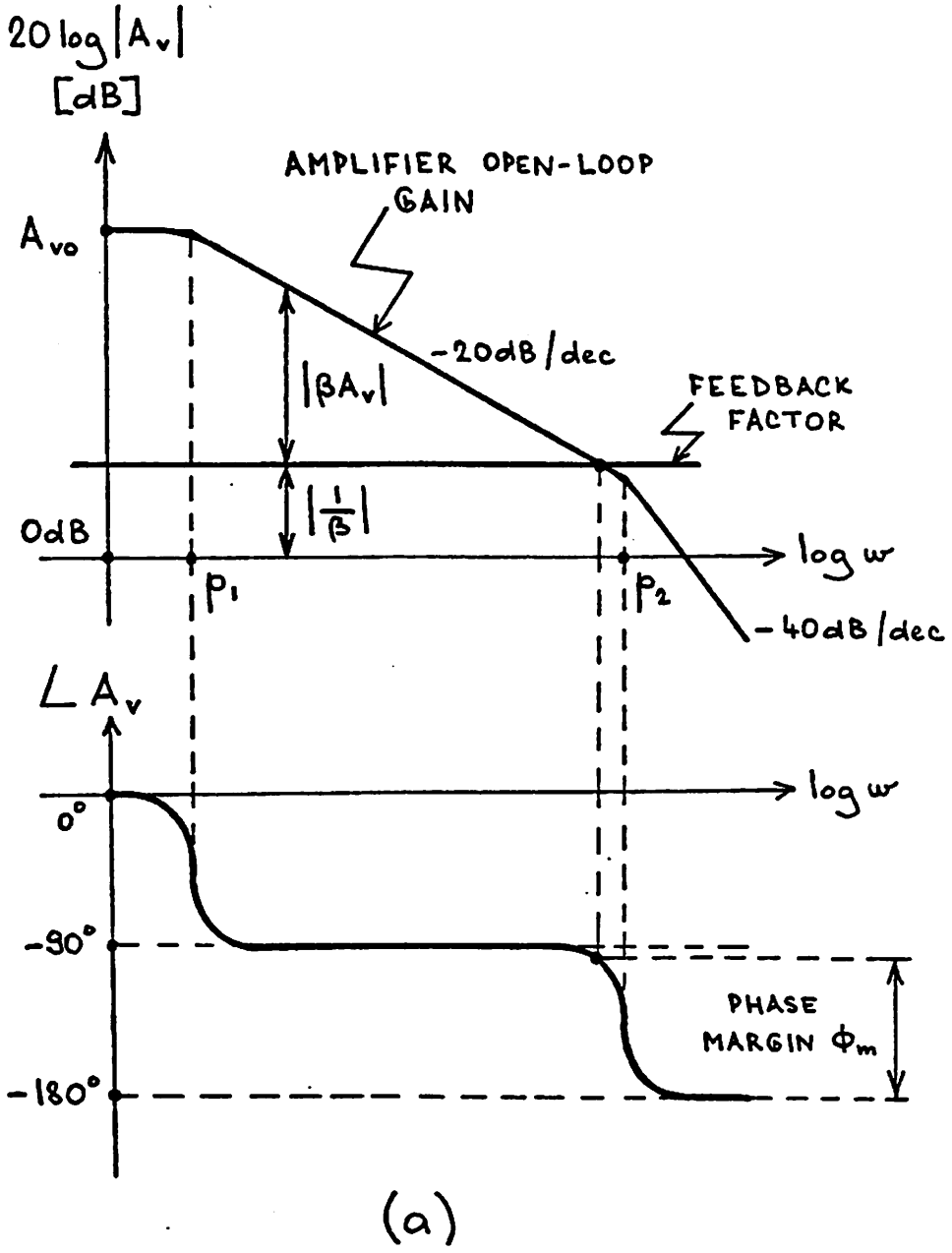
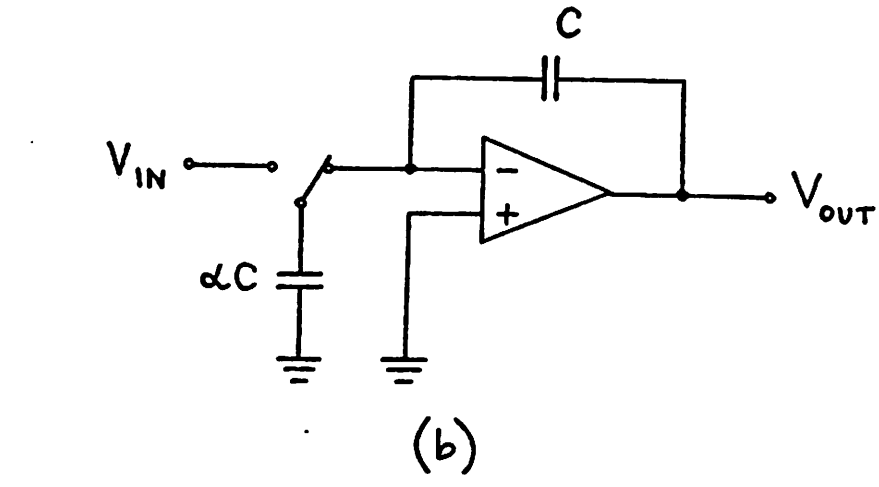


Figure 5.2.a: Bode diagram of a feedback amplifier



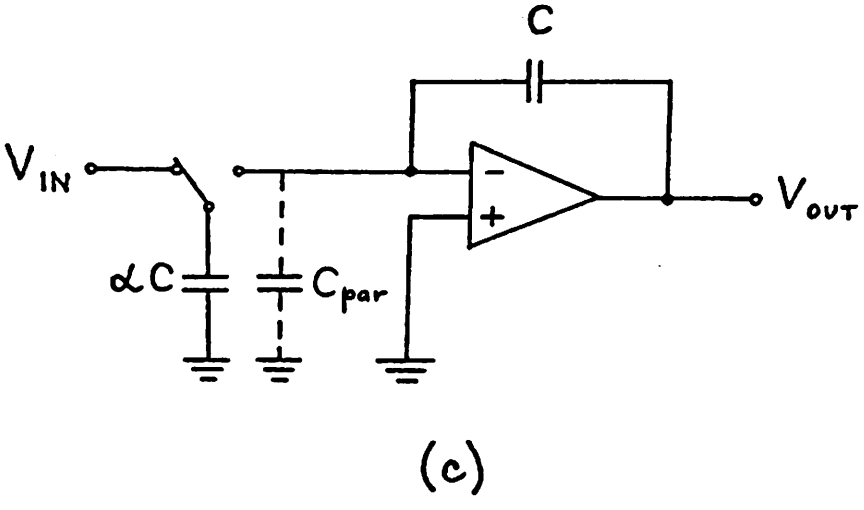


Figure 5.2: (b) A sampled data integrator:
the switch is thrown to the right
(c) A sampled data integrator:
the switch is thrown to the left

above is called phase margin (ϕ_m):

$$\phi_m > 0° \tag{5.13}$$

for stable circuit.

Since the operational amplifier is connected as an integrator, the amplifier only needs to respond to the change in signal which occurs each clock cycle. If the sample rate is high compared to the filter passband frequency then this change in voltage will be small. The slew rate requirement of the amplifier is therefore primarily dependent on the rate of change of the output signal at the passband frequencies. For related reasons, the settling time of the integrators will in general be much shorter than the large signal settling time of the amplifier connected in unity gain (which is the number usually quoted in amplifier specifications).

To estimate the required value of settling time consider that every period the output voltage of the integrator changes by

$$\Delta V_{out} = -\left(\frac{\alpha}{1+\alpha}\right) \frac{A_{V0}}{1+A_{V0}\frac{1}{1+\alpha}} V_{in} \approx -\alpha V_{in} \tag{5.14}$$

For small voltage changes, when the amplifier does not slew, we can treat the integrator as a linear second-order system. The two-pole open-loop gain response from Fig. 5.2a is described by

$$A_V = \frac{A_{V0}}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)} \tag{5.15}$$

The Eq. (5.14) corresponds to a step response of the feedback configuration $A_V/(1+\beta A_V)$. The settling time can be determined from the ringing of the step repsonse. The settling time is commonly specified as the time

required for response settling to within a certain percent of final value. For small signal, the first peak within the error band approximately defines settling time. For an error band of x percent the appropriate peak is that for the smallest value of n satisfying [18]

$$100\% \exp\left(-\frac{\xi n\pi}{\sqrt{1-\xi^2}}\right) \leq x\% \tag{5.16}$$

With the value of n found this way, the settling time is approximately

$$t_s = \frac{n\pi}{\omega_n\sqrt{1-\xi^2}} \tag{5.17}$$

where ω_n is the natural frequency of oscillation and ξ is the damping ratio. According to [18] they are defined as follows:

$$\omega_n = \sqrt{A_{V0}\beta p_1 p_2} \tag{5.18a}$$

$$\xi = \frac{p_1+p_2}{2\sqrt{A_{V0}\beta p_1 p_2}} \tag{5.18b}$$

For large voltage changes, the output response speed is bounded by the slewing rate limit imposed by amplifier capacitances. Slewing rate is limited by ability of the amplifer to provide charging current to such capacitances. The dominant limit is usually the phase compensation capacitance. When the phase compensation is connected to a differential stage, the stage will have to charge or discharge the compensation capacitor.

5.1.2. Amplifier Input Offset Voltage

The input offset voltage of the operational amplifier of the

sampled data integrator of Fig. 5.3a will now be considered. The output of the integrator is

$$V_{out} = -\alpha \frac{z^{-1}V_{in} - V_{OS}}{1-z^{-1}} + V_{OS} \qquad (5.20)$$

The output contains a DC error term which consists of two components: one is the integrated input offset voltage and second is a DC output offset voltage equal to the input offset voltage.

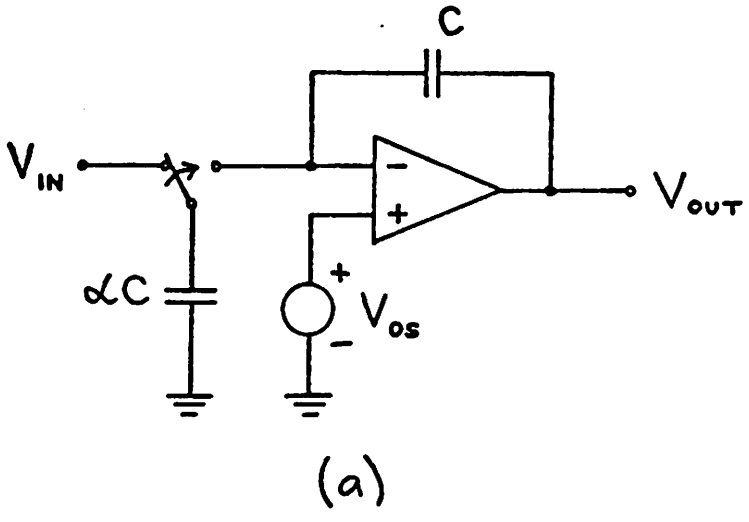
5.1.3. Amplifier Output Swing

Since the dynamic range is defined as the ratio of the maximum usable output voltage to the noise output voltage (see Section 2.5), it is desirable, among others to obtain a large output swing and low noise voltage of the operational amplifier.

The maximum output voltage swing depends on the technology used. If only enhancement devices are used, the voltage swing to the positive supply rail (for NMOS) is inferior to a technology which uses depletion or CMOS devices. Typical numbers are: 16 V output swing for 30 V power supply and technology with enhancement devices only [53], 14 V output swing for 15 V power supply and technology which used depletion devices (Table III), 15 V output swing for 15 V power supply and CMOS technology (CA 3130, [54]). No load was assumed in all three cases.

5.1.4. Amplifier Input Noise Voltage

If the amplifier noise is modeled as a noise source at the positive input to the integrator amplifier (Fig. 5.3b) it is apparent that, in addition to a direct feedthrough, the noise voltage will be sampled and stored on the integrating capacitor:



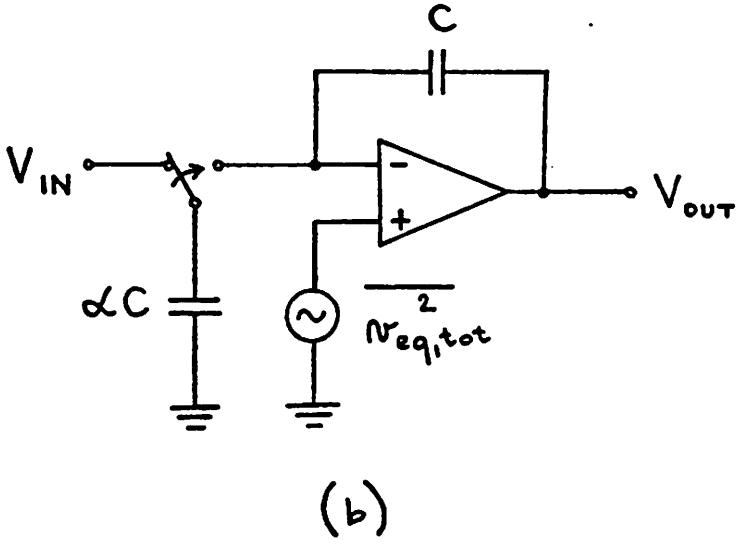


Figure 5.3: (a) Sampled data integrator model including input offset voltage of the amplifier
(b) Sampled data integrator model including equivalent input noise voltage of the amplifier

$$V_{out} = -\alpha \frac{z^{-1}V_{in} - \sqrt{\overline{v^2_{eq,tot}}}}{1-z^{-1}} + \sqrt{\overline{v^2_{eq,tot}}} \qquad (5.21)$$

The estimate of the dynamic range of the integrator involves calculation of the total rms output noise voltage. Let us assume that the equivalent input noise voltage of the amplifier can be expressed as (see Section 4.5.4)

$$\overline{v^2_{eq,tot}} = \overline{v^2_{eq,th}} \left(1 + \frac{f_{Beq}}{f}\right) \qquad (5.22)$$

Let us calculate separately the integrated noise and the noise fed directly through. The integrating part of the transfer function which can be approximated for the frequencies between 0 and f_c by

$$|H(\omega)| \approx \frac{\alpha f_c}{2\pi} \left(\frac{1}{f} + \frac{1}{f_c - f}\right) \qquad (5.23)$$

since it is known that the approximation $\alpha f_c/(2\pi f)$ is valid for $f \ll f_c$ and that the frequency response is periodic with period $T_c = 1/f_c$. Using Eq. (5.22) and (5.23), we calculate the noise [42]:

$$\overline{v^2_{n1}} = \int_{f_{low}}^{f_{Beq}} \overline{v^2_{eq,th}} \left(\frac{f_{Beq}}{f}\right)\left(\frac{\alpha f_c}{2\pi f}\right)^2 df = \overline{v^2_{eq,th}} \left(\frac{\alpha f_c}{2\pi}\right)^2 \left(\frac{f_{Beq}}{2f^2_{low}} - \frac{1}{2f_{Beq}}\right) \qquad (5.24a)$$

It turns out that other noise components are much smaller, i.e., $\overline{v^2_{n2}}, \overline{v^2_{n3}}, \overline{v^2_{n4}} \ll \overline{v^2_{n1}}$, where

$$\overline{v^2_{n2}} = \int_{f_{Beq}}^{f_c - f_{low}} \overline{v^2_{eq,th}} \left(\frac{\alpha f_c}{2\pi f}\right)^2 df \qquad (5.24b)$$

$$\overline{v_{n3}^2} = \int_{f_{low}}^{f_{Beq}} \overline{v_{eq,th}^2} \left(\frac{f_{Beq}}{f}\right)\left[\frac{\alpha f_c}{2\pi(f_c-f)}\right]^2 df \tag{5.24c}$$

$$\overline{v_{n4}^2} = \int_{f_{Beq}}^{f_c-f_{low}} \overline{v_{eq,th}^2} \left[\frac{\alpha f_c}{2\pi(f_c-f)}\right]^2 df \tag{5.24d}$$

The same applies to the noise that comes directly through:

$$v_{n5}^2 = \int_{f_{low}}^{f_{Beq}} \overline{v_{eq,th}^2} \left(\frac{f_{Beq}}{f}\right) df \tag{5.24e}$$

$$v_{n6}^2 = \int_{f_{Beq}}^{f_c-f_{low}} \overline{v_{eq,th}^2} \, df \tag{5.24f}$$

The total rms output noise voltage, integrated over a band from f_{low} to (f_c-f_{low}) is

$$\overline{v_{n,tot}^2} = \sum_{i=1}^{6} \overline{v_{ni}^2} \tag{5.25a}$$

The first term in v_{n1}^2 is certainly dominant. Hence

$$\overline{v_{n,tot}^2} \approx \overline{v_{eq,th}^2} \left(\frac{\alpha f_c}{2\pi f_{low}}\right)^2 \frac{f_{Beq}}{2} \tag{5.25b}$$

5.1.5. Amplifier Harmonic Distortion

Any MOS gain stage will produce some nonlinearity. Section 4.5.5 shows an example for a stage with the depletion load. Especially when the signal input voltage level becomes very large the signal waveform at the output of a MOS transistor pair becomes very distorted because

one of the transistors is eventually driven out of the saturation region.

The same will basically apply to an all-MOS amplifier. The nonlinear transfer characteristic of an amplifier can be expressed as a power series

$$v_{out} = a_1 v_{in} + a_2 v_{in}^2 + \ldots \tag{5.26}$$

where the coefficients $a_1, a_2, \ldots, a_n$ are constants. The a_1 term is the small signal voltage gain used in linear analysis. It is known that for a given output signal level in an amplifier, and assuming ideal feedback, the harmonic distortion can be reduced by the application of negative feedback [43]. E.g., the second harmonic distortion (as defined in Section 4.5.5) will be reduced by a factor (1+loop gain):

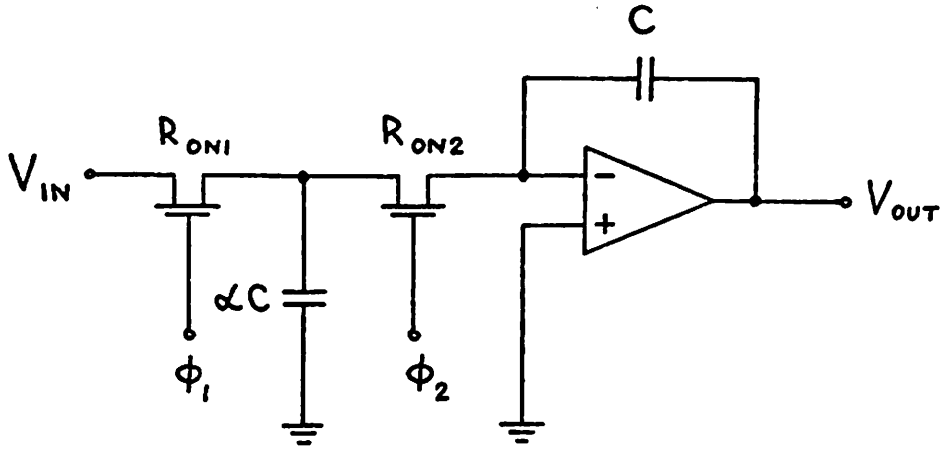
$$HD_2 = \frac{1}{4} \frac{a_2}{a_1^2} \frac{V_{out,pp}}{1+a_1\beta} \tag{5.27}$$

where β is the feedback factor (see Eq. (5.14) and Fig. 5.2a)).

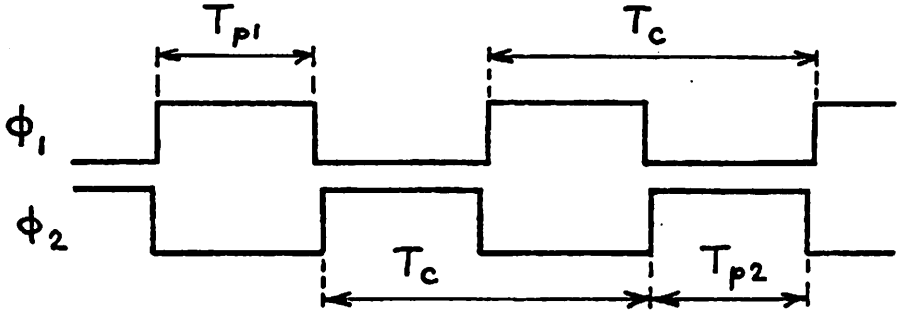
5.1.6. "On" Resistance of the Switches

At very high sample rates (higher than most amplifiers would allow) the time constant of the switched capacitors will become important. This time constant is determined by the "on" resistance of the switches (typically several kilohms) and the value of the switched capacitances (tens of picofarads) which yields a time constant on the order of tens of nanoseconds

The charge conservation equation can be derived from Fig. 5.4a similarly to Eq. (3.26):



(a)



(b)

Figure 5.4: (a) Sampled data integrator with MOSFET switches
(b) Timing diagram for switching of a

$$CV_{out}[nT_c] = CV_{out}[(n-1)T_c] - \alpha C(1-e^{-\frac{T_{p1}}{\alpha CR_{ON1}}})(1-e^{-\frac{T_{p2}}{\alpha CR_{ON2}}})V_{in}[(n-1)T_c] \tag{5.28}$$

The transfer function is

$$H(z) = -\frac{\alpha_{actual} z^{-1}}{1-z^{-1}} \tag{5.29}$$

where

$$\alpha_{actual} = \alpha(1-e^{-\frac{T_{p1}}{\alpha CR_{ON1}}})(1-e^{-\frac{T_{p2}}{\alpha CR_{ON2}}}) \tag{5.30}$$

5.1.7. Clock Feedthrough

Most MOSFET switches exhibit some degree of clock feedthrough, due to capacitive coupling between the gate and the channel (see Fig. 4.4b). This is a difficult parameter to define in quantitative terms since the MOSFET capacitances are not linear. The negative falltime feedthrough should cancel the positive risetime feedthrough, but an exact cancellation is not achieved due to the nonlienarities mentioned above.

The clock feedthrough may be expressed as

$$Q_{clock} = \int C_{gate} dV_{clock} \tag{5.31}$$

one clock period (see Fig. 5.5), then the charge conservation equation yields following transfer function:

$$V_{out} = -\frac{\alpha z^{-1} V_{in} + \frac{\Delta Q_{clock,tot}}{C}}{1-z^{-1}} \tag{5.32}$$

Compare Eq. (5.32) with Eq. (5.20). Clearly, the clock feedthrough has similar effect as a DC offset voltage.

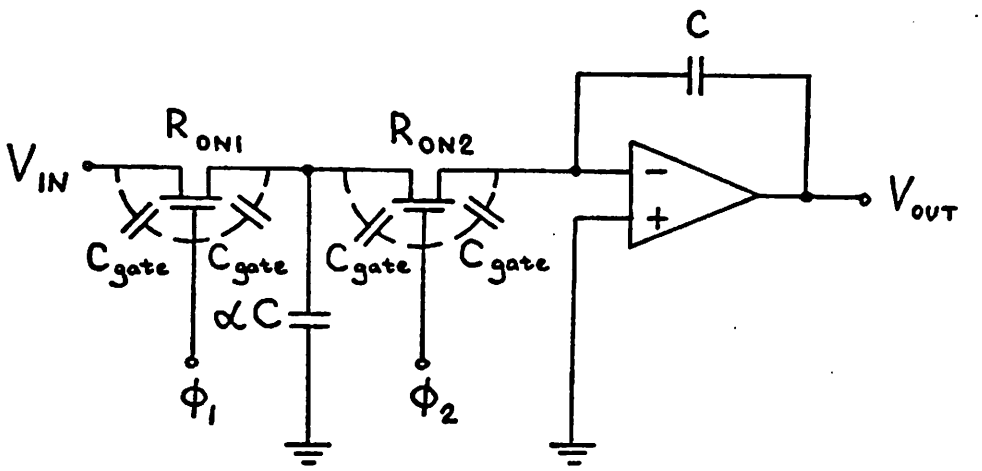


Figure 5.5: Clock feedthrough

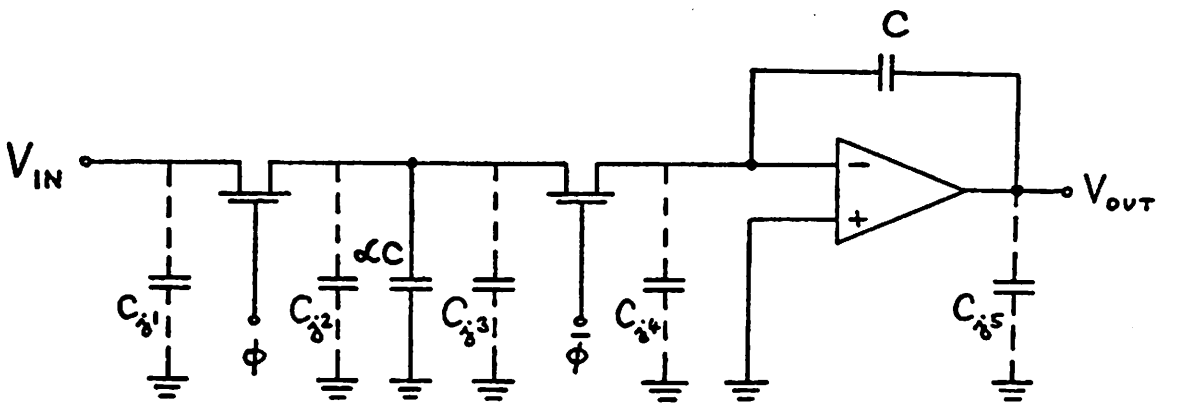


Figure 5.6: Junction capacitances

The clock feedthrough can be decreased by lowering the clock voltage and by using smaller gate-channel overlap (this will decrease the overlap capacitance). Especially MOSFET switches fabricated by self-aligned gate techniques are attractive because of elimination of gate overlap capacitance. Another method of clock feedthrough reduction is use of charge-cancelling circuit techniques [16,25].

5.1.8. Junction Capacitances

Figure 4.1 shows the cross section of a typical N-channel MOSFET in metal gate technology. In normal operation, the N-region is reverse biased (positive with respect to the P-substrate). The junction capacitance that appears across the depletion region is given by Eq. (4.14) and (4.15) for the junction capacitance between source and substrate and drain and substrate, respectively.

Figure 5.6 illustrates the effect of the junction capacitances C_j. But only C_{j2} and C_{j3} have to be considered because the remaining three junction capacitances have no effect. The capacitance C_{j1} is merely shunting the input voltage source, C_{j4} is at virtual ground and C_{j5} is voltage driven.

Hence

$$\alpha_{actual} = \frac{\alpha C + C_{j2} + C_{j3}}{C} = \alpha + \frac{C_{j2} + C_{j3}}{C} \tag{5.33}$$

Let us assume that C_{j2} and C_{j3} are equal, i.e.

$$C_{j2} = C_{j3} = \frac{C_{JUNCTION} \times (\text{JUNCTION AREA})}{\sqrt{1 + \frac{V}{\phi_B}}} \tag{5.34}$$

Further, let us assume that the junction voltage V has a large DC component V_{DC} and a small signal voltage which is equal to the input

signal voltage v_{in}:

$$V = V_{DC} + v_{in} \tag{5.35}$$

Substituting Eq. (5.35) in Eq. (5.34) gives

$$C_{j2} = C_{j3} = \frac{C_{JUNCTION}x(\text{JUNCTION AREA})}{\sqrt{(1+\frac{V_{DC}}{\phi_B})(1+\frac{v_{in}}{\phi_B(1+\frac{V_{DC}}{B})})}} \approx C_{PN}[1-\frac{v_{in}}{2(\phi_B+V_{DC})} \tag{5.36}$$

for $v_{in} << (\phi_B+V_{DC})$. The capacitance C_{PN} is

$$C_{PN} = \frac{C_{JUNCTION}x(\text{JUNCTION AREA})}{\sqrt{1+\frac{V_{DC}}{\phi_B}}} \tag{5.37}$$

Using Eq. (5.33) and (5.36), we find

$$\alpha_{actual} = \alpha + \frac{C_{PN}}{C}[2 - \frac{v_{in}}{\phi_B+V_{DC}}] \tag{5.38}$$

If the last term is neglected, the α coefficient error is

$$\frac{\Delta\alpha}{\alpha} = \frac{\alpha_{actual}-\alpha}{\alpha} \cong \frac{2C_{PN}}{\alpha C} \tag{5.39}$$

The dependence of on v_{in} will give rise to second harmonic distortion. Substituting Eq. (5.38) in Eq. (5.14) and subsequent solving of Eq. (4.128) give

$$HD_2 = \frac{1}{4}\frac{C_{PN}}{C(\alpha+\frac{2C_{PN}}{C})}\frac{1}{2}\frac{1}{(\phi_B+V_{DC})}V_{out,pp} \tag{5.40}$$

Both Eq. (5.39) and (5.40) indicate that an effort should be made to decrease the junction capacitance, i.e., to keep junction area as small

as possible and to use large body bias and lightly doped substrate material.

To estimate $\Delta\alpha/\alpha$ and HD_2 consider typical numbers, e.g., C_{PN} = 0.01 pF, C = 1 pF, V_{DC} = 7.5 V, ϕ_B = 0.542 V, α = 1 and $V_{out,pp}$ = 1 V. Then we obtain $\Delta\alpha/\alpha$ = 2% and HD_2 = -70.5 dB from Eq. (5.39) and (5.40).

5.1.9. Junction Leakage

A large leakage current from a reversed biased PN junction connected to a capacitor plate can cause an error in capacitor voltage (see Fig. 5.7). The transfer function of the integrator suggests that the leakage currents will cause a DC offset:

$$V_{out} = -\frac{\alpha z^{-1} V_{in} + \frac{Q_2-Q_1}{C} z^{-1} + \frac{Q_2}{C}}{1-z^{-1}} \tag{5.41}$$

where:

$$Q_1 = \frac{T_c}{2}\left(I_{leakage\ 2}+I_{leakage\ 3}\right) \tag{5.42a}$$

$$Q_2 = \frac{T_c}{2}\left(I_{leakage\ 5}-I_{leakage\ 4}\right) \tag{5.42b}$$

Typical leakage currents in MOS circuits are in the order of 10 pA/mil^2 at the room temperature [25] which implies 1 mil^2 yields 10 mV offset on an 1 pF capacitance at 1 kHz clock rate.

5.1.10. Noise of the MOSFET Switches

The other noise contribution is due to the thermal noise of the MOSFET switches which is sampled onto the switched capacitors. This results in an rms noise contribution from each switching operation of $\left(\frac{kT}{C}\right)^{1/2}$, where C is the switched capacitance and kT is the thermal voltage [45]. This noise can be minimized by increasing the size of the

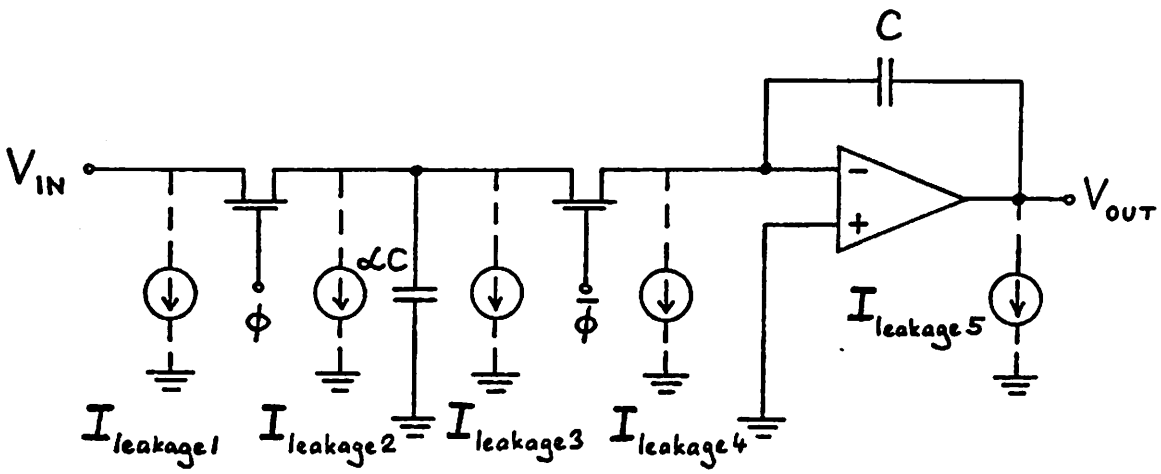


Figure 5.7: Junction leakage

switched capacitors.

5.1.11. MOS Capacitor Mismatch

Figure 5.8a shows the implementation of MOS precision capacitors for a sampled data integrator in N-channel Al-gate MOS technology. The capacitor areas are defined by the metal pattern. Since the capacitance per unit area is uniform across an IC it is possible to achieve high recision in the capacitor ratio. It has been shown that the error in such ratios can be less than 0.1% using standard MOS processing techniques [16].

The capacitance for MOS capacitors is given by

$$C = C_{ox}A \tag{5.43}$$

where C_{ox} is the capacitance per area and A is the area. $C_{ox} = \varepsilon_{ox}/t_{ox}$, for a dielectric permitivity ε_{ox} and oxide thickness t_{ox}.

The flexibility of capacitor geometry allows them to be made square or even circular so as to optimize matching accuracy. If σ_x is the random uncertainty in edge definition due to the photolithography, the fractional variation in the capacitor value is

$$\frac{\sigma_{C_1}}{C_1} = \sqrt{\frac{1}{a^2} + \frac{1}{b^2}}\ \sigma_x \tag{5.44}$$

because $\Delta C_1/C_1 = \Delta a/a + \Delta b/b$ for a capacitor C_1 defined by the area $A_1 = ab$ (Fig. 5.8b). For rectangular geometries this quantity is minimized for a square area $A_1 = a^2$. Then

$$\frac{\sigma_{C_1}}{C_1} = \frac{\sqrt{2}}{a}\sigma_x \tag{5.45}$$

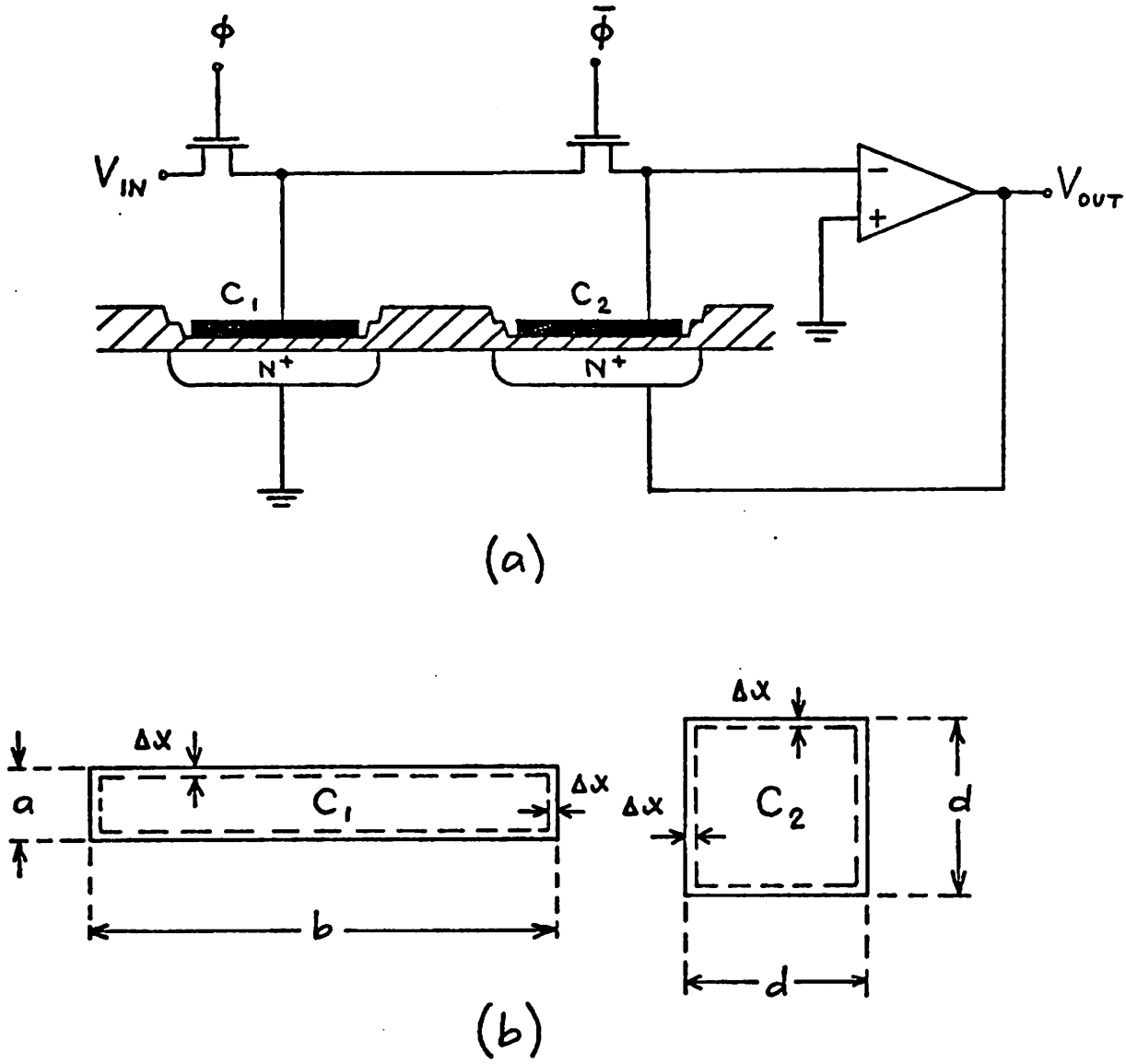


Figure 5.8: (a) MOS capacitor implementation for a sampled data integrator
(b) Capacitor geometry for a

Measured data on MOS capacitors suggest a standard derivation edge uncertainty of approximately 0.1 μm [25].

Consider a capacitor ratio $\alpha = C_1/C_2$. Neglecting any oxide gradients this ratio can be written as $\alpha = A_1/A_2$ (see Eq. (5.43)). During the etching phase of the photomask process a poorly controlled lateral etch occurs called undercut [16]. Let Δx be the undercut length and A_i and P_i be the area and the perimeter length of a capacitor C_i, respectively. The actual ratio is different from the nominal ratio $\alpha = A_1/A_2$:

$$\alpha = \frac{A_1 - P_1\Delta x}{A_2 - P_2\Delta x} \approx \alpha - \frac{\Delta x}{A_2}(P_1 - \alpha P_2) \tag{5.46}$$

for very small Δx. The ratio error is proportional to the undercut length:

$$\frac{\Delta\alpha}{\alpha} = \left|\frac{\alpha_{actual} - \alpha}{\alpha}\right| \approx \frac{\Delta x}{A_2}\left(\frac{P_1}{\alpha} - P_2\right) \tag{5.47}$$

This problem can be obviously solved by a geometry such that the perimeter lengths are ratioed as well, i.e. $\alpha = A_1/A_2 = P_1/P_2$.

Consider two capacitors C_1 and C_2, shown in Fig. 5.8b. To eliminate the undercut problem, the following equation has to be solved:

$$\alpha = \frac{ab}{d^2} = \frac{2(a+b)}{4d} \tag{5.48}$$

For a given side length d, the solution is

$$\sqrt{\frac{a}{b}} = \sqrt{\alpha} \pm \sqrt{\alpha - 1} \tag{5.49}$$

Clearly $C_1 \geq C_2$ for $\alpha \geq 1$, i.e., the square area capacitor must be the smaller one.

$$\frac{\sigma_\alpha}{\alpha} = \sqrt{\left(\frac{\sigma_{C_1}}{C_1}\right)^2 + \left(\frac{\sigma_{C_2}}{C_2}\right)^2} \tag{5.50}$$

where $\left(\frac{\sigma_{C_1}}{C_1}\right)$ is given by Eq. (5.44) and

$$\left(\frac{\sigma_{C_2}}{C_2}\right) = \frac{\sqrt{2}}{d}\,\sigma_x.$$

Hence

$$\frac{\sigma_\alpha}{\alpha} = \frac{\sigma_x}{d}\sqrt{2 + \frac{1}{\alpha}\left(\frac{a}{b} + \frac{b}{a}\right)} \tag{5.51}$$

If $\alpha = 1$, then

$$\frac{\sigma_\alpha}{\alpha} = 2\,\frac{\sigma_x}{d} \tag{5.52}$$

For large α and $P_1 = \alpha P_2$, the Eq. (5.51) gives

$$\frac{\sigma_\alpha}{\alpha} \approx \sqrt{6}\,\frac{\sigma_x}{d} \tag{5.53}$$

When both capacitors, C_1 and C_2, have a square geometry (a=b) so that $P_1 \neq \alpha P_2$, we get

(5.53)

$$\frac{\sigma_\alpha}{\alpha} = \frac{\sigma_x}{d}\sqrt{2\left(1 + \frac{1}{\alpha}\right)} \tag{5.54}$$

Thus, for large α, the square capacitors would have $\sqrt{3}$ times smaller mismatch error due to the edge uncertainty than the contiguration shown in Fig. 5.8b. The error due to the undercut, however, would be

$$\frac{\Delta\alpha}{\alpha} \approx \frac{4\Delta x}{d}\left(\sqrt{\alpha} - 1\right) \tag{5.55}$$

Since the expected undercut length is about 1 μm [46], it presents more serious problem than the edge uncertainty.

Other undercut-insensitive geometries include common-centroids with nearly constant area/perimeter ratios [4] and paralleling identical size plates to form different size capacitors [16].

5.1.12. Voltage Dependence of MOS Capacitors

To characterize the capacitor ratio error due to capacitor linearities, let [25]

$$\psi = \gamma_V^C = \frac{1}{C}\frac{\partial C}{\partial V} \tag{5.56}$$

where γ_V^C is the effective voltage coefficient of the MOS capacitors. The capacitors of Fig. 5.8a then have the form:

$$C_{1actual} = C_1(1+\psi V_1) \tag{5.57a}$$

$$C_{2actual} = C_2(1+\psi V_2) \tag{5.57b}$$

Here it is assumed that the nonlinearity is small enough that the higher order terms in C(V) can be neglected. Consider one charge transfer described by Eq. (5.14):

$$\Delta V_{out} = -\alpha_{actual} V_{in} \tag{5.58}$$

in which $\alpha_{actual} = C_{1actual}/C_{2actual}$. Hence

$$\alpha_{actual} = \frac{C_1(1+\psi V_{in})}{C_2(1-\psi V_{out})} \tag{5.59}$$

For small voltages and small ψ, it can be shown that ($\alpha=C_1/C_2$):

$$\alpha_{actual} \approx \alpha(1+\psi V_{in})(1+\psi V_{out}) \tag{5.60}$$

Using Eq. (4.128), (5.58) and (5.60), we can derive the second harmonic distortion for small voltages and small coefficient :

$$HD_2 \approx \frac{(1+\alpha)}{4\alpha} V_{out,pp} \tag{5.61}$$

Similarly the third harmonic distortion is

$$HD_3 \approx \frac{\psi^2}{8\alpha} V^2_{out,pp} \tag{5.62}$$

The voltage coefficient ψ depends on bias voltage and doping of the bottom plate. For MOS capacitors on heavily doped N back plates voltage coefficients of less than 24 ppm/V have been observed [16]. Hence $HD_2 = -94.8$ dB for $\alpha = 1$ and $V_{out,pp} = 1$ V.

5.1.13. Thin Oxide Gradients

Another contribution to ratio errors are gradients in the thin capacitor oxide. These gradients arise from nonuniform oxide growth conditions. If this variation in oxide thickness is approximated as first-order gradient, then the resulting capacitance is a function of distance α:

$$C(x) = A \frac{\varepsilon_{ox}}{t_{ox}} (1+gx) \tag{5.63}$$

in which g is the thin oxide gradient divided by the nominal thin oxide thickness t_{ox}. The ratio error is proportional to the fractional variation in oxide thickness:

$$\alpha_{actual} = \frac{C_1(x_1)}{C_2(x_2)} = \frac{A_1}{A_2}\frac{1+gx_1}{1+gx_2} \approx \alpha[1+g(x_1-x_2)] \qquad (5.64a)$$

for small g. Experimentally, values of 10-100 ppm/mil have been observed for the factor g [16].

The coefficient error due to thin oxide gradient is then

$$\frac{\Delta\alpha}{\alpha} = \frac{\alpha_{actual}-\alpha}{\alpha} = g(x_1-x_2) \qquad (5.64b)$$

This yields error 1% for α if g = 100 ppm/mil.

5.1.14. Capacitor Ratio Error Due to Interconnect

The metal over field oxide capacitance C_M is similar to MOS capacitance but, because field oxide is approximately 10 times the thickness of thin oxide, C_M is given by

$$C_M \approx A_M \frac{\varepsilon_{ox}}{10t_{ox}} \qquad (5.65)$$

where A_M is the area of metal interconnections. It can be modelled as a parasitic capacitance to substrate or ground, similarly to junction capacitances (see Section 5.1.8 and Fig. 5.6). C_M is not significantly voltage dependent for voltages less than the field threshold voltage [34].

5.1.15. Package Parasitics

Package parasitic effects result from lead inductance, pin capacitance, and mutual coupling between bonding leads. Especially the pin capacitance can be quite large, in the order of pF. Therefore the signal nodes that are electrically connected to package pins should always be either voltage driven or at virtual ground.

5.1.16. Conclusions

Table I summarizes the results of our discussion on second order effects.

DC offsets are caused by input offset voltage of the amplifier, clock feedthrough and junction leakage currents. The DC offsets can be considered negligible, if they are small compared to signal amplitude. Large DC offsets, however, would reduce the dynamic range available for signals.

Harmonic distortion of the filter is effected by the distortion of the amplifier, voltage dependence of MOS capacitors and junction capacitances.

Gain of the amplifier, "on"-resistance of the switches, junction capacitances, MOS capacitor mismatch, thin oxide gradients and capacitances due to metal interconnect effect the capacitor ratio α.

5.2. Filter Version 3 Design

5.2.1. Optimal Design Procedure

It is desirable to have the clock (sample) rate as high as possible relative to the filter passband frequencies in order to reduce the aliasing of the input signal (and to reduce the requirements on any anti-aliasing filter that may be required). The filters which have been described in Chapter 3 are particularly amenable to high sample rate operation, because their sensitivity to parameter variations decreases as the clock rate is increased. However, the size of the capacitor ratio α required for a given frequency response also increases with clock rate, which increases the silicon area requirements.

TABLE I

Second Order Effects

Section	Effect	Typical Numbers
5.1.1.	Low-frequency gain	100-10000 [39]
	Unity-gain frequency	2-5 MHz [39]
5.1.2.	Input offset voltage	tens of milivolts [39]
5.1.3.	Output swing	see section 5.1.3
5.1.4.	Input noise voltage	30-100 microvolts, integrated over a band from 20 Hz to 50 kHz [39]
5.1.5.	Harmonic distortion	usually negligible because reduced by the loop gain
5.1.6.	"on"-resistance of the switches	several kiloohms
5.1.7.	Clock feedthrough	tens or hundreds of milivolts, depending on technology and circuit design
5.1.8.	Junction capacitance	tens of femtofarads for each terminal pair [39]
5.1.9.	Junction leakage	10 pA/mil^2 [25]
5.1.10.	Noise of MOSFET switches	wideband rms noise 64.5 μV for C = 1 pF
5.1.11.	MOS capacitor mismatch	0.02-0.3% [39]
5.1.12.	Voltage dependence of MOS capacitors	24 ppm/V [16]
5.1.13.	Thin oxide gradients	10-100 ppm/mil [16]
5.1.14	Meal interconnect	10x smaller than the thin oxide capacitance (per area)
5.1.15.	Package parasitics	pin capacitance 1.5 pF

For medium to low Q filters (i.e., Q < 50) the low Q sensitivity of version 2 is not required and thus the reduction in circuit complexity achieved with version 3 gives it a distinct advantage over the other versions.

As mentioned in Section 5.1.1, the finite open-loop gain A_v of the amplifier should be included in design equations of the filter. The required value for this gain is very dependent on the frequency response of the filter and is to be determined from the sensitivity of filter parameters to A_v. The transfer function for the version 3 filter, including A_v, is

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{k\alpha_1\alpha_2\gamma}{z^2 - z(k+\eta-\varepsilon\gamma\alpha_2) + k(\eta+\gamma\alpha_1\alpha_2)} \tag{5.66}$$

where

$$k = \frac{1}{(1+\alpha_1)(1+A\alpha_2)} \tag{5.67}$$

$$\gamma = 1 - \frac{1+\alpha_2}{A_v} \tag{5.68a}$$

$$\eta = 1 - \frac{\alpha_2}{A_v} \tag{6.58b}$$

$$\varepsilon = k(1+\alpha_1)\ \frac{A\alpha_2}{A_v} \tag{5.69}$$

The sensitivity equations (3.56a), (3.56b), (3.56c), (3.56d) and (3.56e), derived under conditions that $f_0 << f_c$ and $Q >> 1$, are valid if an additional condition is fulfilled: $A_v >> Q$. Since A_v has become a new filter variable, it is necessary to calculate the sensitivity of filter parameters to A_v. Under conditions mentioned above, we obtain after some manipulation:

$$S_{A_v}^{f_0} = \frac{1}{2A_v}\left[\alpha_2\left(1+\frac{1}{\theta^2}\right)-1\right] \tag{5.70a}$$

$$S_{A_v}^{Q} = \frac{Q}{A_v}\left(\theta + \frac{\alpha_2}{\theta}\right) \tag{5.70b}$$

While the sensitivity of f_0 is certainly small, the sensitivity of Q will be less than 1 only if $A_v > Q\left(\theta + \frac{\alpha_2}{\theta}\right)$.

Thus, the optimal design procedure for the version 3 filter, given f_0 and Q_1 is as follows: first, choose a clock rate f_c, a value of α_2 (see Fig. 3.11) and a gain A_v; then calculate the value of k from the expression:

$$k = \frac{2A_v \exp\left[-\frac{\pi f_0}{Qf_c}\right]\cos\left[\frac{\pi f_0}{f_c}\left(4 - \frac{1}{Q^2}\right)^{1/2}\right] - A_v\eta + \alpha_2\gamma - \exp\left[-\frac{2\pi f_0}{Qf_c}\right]}{A_v + \gamma\alpha_2 - \eta} \tag{5.71a}$$

and finally, calculate α_1 and A:

$$\alpha_1 = \frac{1}{\gamma\alpha_2}\left(\frac{1}{k}\exp\left[-\frac{2\pi f_0}{Qf_c}\right] - \eta\right) \tag{5.71b}$$

$$A = \frac{1}{\alpha_2}\left[\frac{1}{k(1+\alpha_1)} - 1\right] \tag{5.71c}$$

where,

$$\gamma = 1 - \frac{1+\alpha_2}{A_v} \tag{5.72a}$$

$$\eta = 1 - \frac{\alpha_2}{A_v} \tag{5.72b}$$

5.2.2. Design Example

Two version 3 lowpass filters (Fig. 3.10a) are to be designed. One should be a high Q filter with Q = 73 at a center frequency of

$f_0 = 0.0366\ f_c$ (filter I), while the second should have the relatively low Q = 1 at a center frequency of $0.0165\ f_c$ (filter II).

The sensitivity equations (3.56c), (3.56d) and (3.56e) show that the Q sensitivities increase for increasing Q. Therefore we are going to choose the optimal value of α_2 from Fig. 3.11: $\alpha_2 = 2$ for the high Q filter. Next step is calculation of gain A_v. If not more than 1% Q variation due to 10% gain variation is desired, then $S^Q_{A_v}$ should be less than 0.1:

$$S^Q_{A_v} = \frac{\Delta Q/Q}{\Delta A_v/A_v} = \frac{1}{10} \tag{5.73}$$

When Eq. (5.73) is substituted in Eq. (5.70b), we obtain $A_v = 6000$. From Eq. (5.71) and (5.72) remaining coefficients α_1 and A can be found. Since the coefficients have to be rounded off in order to be realizable, it is necessary to find a suitable combination. For our case it has been found:

Filter I: $\alpha_1 = 0.028$, $\alpha_2 = 1.99$, $A = 0.015$

This combination gives Q = 73.14. Equations 93.56) adn (5.70a) yield all sensitivities:

$$S^{f_0}_{\alpha_1} = 0.23 \tag{5.74a}$$

$$S^{f_0}_{\alpha_2} = S^{f_0}_{A} = 0.24 \tag{5.74b}$$

$$S^Q_{\alpha_1} = 8.2 \tag{5.74c}$$

$$S^Q_{\alpha_2} = S^Q_A = 8.43 \tag{5.74d}$$

$$S^{f_0}_{A_v} = 0.003 \tag{5.74e}$$

We shall choose a different design approach for the low Q filter II. In this case, we are not concerned about high Q sensitivities so we can try to minimize the capacitor area. We choose our coefficients so that $\alpha_1 \approx A\alpha_2$ and rather arbitrarily $A_v = 40$:

Filter II: $\alpha_1 = .06$, $\alpha_2 = .182$, $A = .295$

The resulting Q is 0.99. The sensitivities can be again calculated based on Eq. (3.56) and (5.70):

$$S_{\alpha_1}^{f_0} = 2.5 \tag{5.75a}$$

$$S_{\alpha_2}^{f_0} = S_A^{f_0} = 2.22 \tag{5.75b}$$

$$S_{\alpha_1}^{Q} = 0.44 \tag{5.75c}$$

$$S_{\alpha_2}^{Q} = 0.57 \tag{5.75d}$$

$$S_A^{Q} = 0.47 \tag{5.75e}$$

$$S_{A_v}^{f_0} = 0.2 \tag{5.75f}$$

$$S_{A_v}^{Q} = 0.05 \tag{5.75g}$$

5.2.3. Conclusions

As expected, the Q sensitivity for filter I is relatively high and therefore serious attention should be paid when designing the lay-out of this filter.

5.3. MOS Amplifier Design

5.3.1. Design Description

Since the amplifier requirements for low and high Q filters are quite different, two amplifier designs were performed. The first is a new operational amplifier design with a gain of 6000, while the second is a simple differential pair with a gain of 40. The advantage of using a simple amplifier for low Q filters is the savings achieved in circuit area (which was about a factor of 2.5).

The main problem of single channel MOS amplifiers is the low gain per gain stage. For this reason depletion type loads were used which inherently offer more gain than enhancement loads (see Chapter 4.3.1). A single channel NMOS operational amplifier with depletion loads is shown in Fig. 5.9. The input stage M1, M2, M3 and M4 is a single-ended differential amplifier. This is followed by the level shifter M8, M9 which drives the main gain stage. The transconductance of the driver transistor M10 has been increased by adding the current source M11, M12, which provides more DC bias current for M16 and thus increases the total gain of this state (similarly as in Fig. 4.16b). The transistor M13 (common gate configuration) isolates the load device M14. The output stage M17, M18 is connected as a push-pull driver but the main gain stage has so much gain that M18 basically operates as a source follower with M17 as the load.

Frequency compensation is accomplished by an on-chip Miller capacitor C_c = 6 pF. This compensation capacitor has not been connected directly to the output of the main gain stage because this would introduce a right-half plane zero due to signal feedthrough, as we have seen in Chapter 4.5.2. Instead C_c has been connected to another push-pull

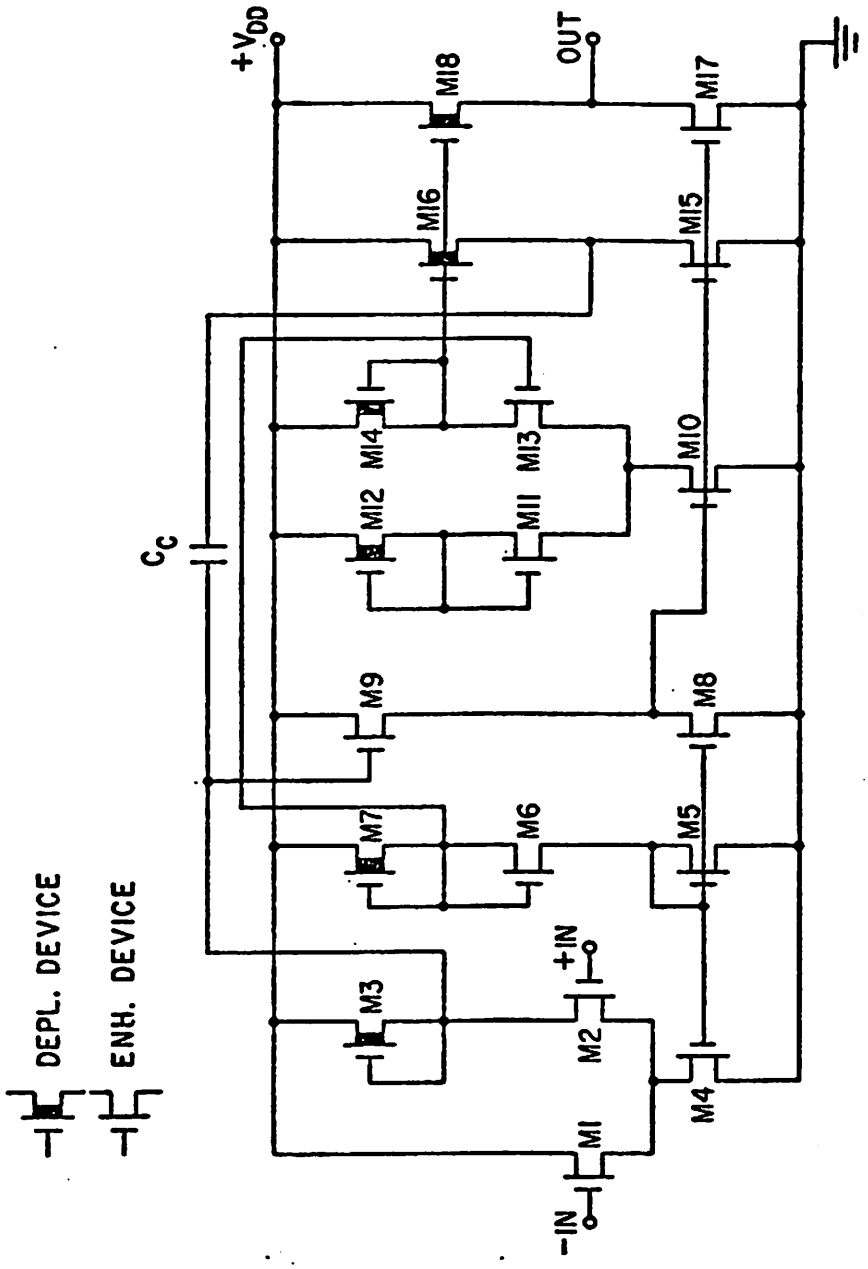


Figure 5.9: A single channel NMOS operational amplifier with depletion loads

driver (M15, M16) following the main gain stage. This configuration has the advantage that the main gain stage is essentially bypassed at high frequencies; otherwise the Miller capacitor C_c would have been applied over too many poles. This is practically the feedforward compensation from the Chapter 4.5.2. The dominant pole of the amplifier is then determined by C_c multiplied by the gain of the main stage and load impedance of the input stage (M3).

The circuit has been designed so that its operation is largely independent of the threshold voltage variations. Configurations and geometries were selected in such way that all quiescent voltages through the amplifier track the quiescent voltages of the bias string M5, M6, M7 [23]. This assures that all devices will be in saturation even for large threshold voltage variations.

As mentioned above for low Q filters an amplifier with only moderate gain is needed. For such filters a relatively simple differential amplifer which is shown in Fig. 5.10 has been designed. The amplifier consists of the differential input stage M19, M20, M21 and M22, the output stage M26, M27 and the bias string M23, M24, M25. This amplifier is the same design as the input stage to the operational amplifier of Fig. 5.9.

Table II contains the w/ℓ ratios for all the MOSFETs in the two amplifiers.

5.3.2. MOSFET parameters

The process used in this work is an N-channel Al-gate technology. The starting material is lightly doped (C_B=5x10^{14}cm^{-3}) p-type silicon.

The threshold voltage equation used in this calculation uses the basic threshold equation [47]:

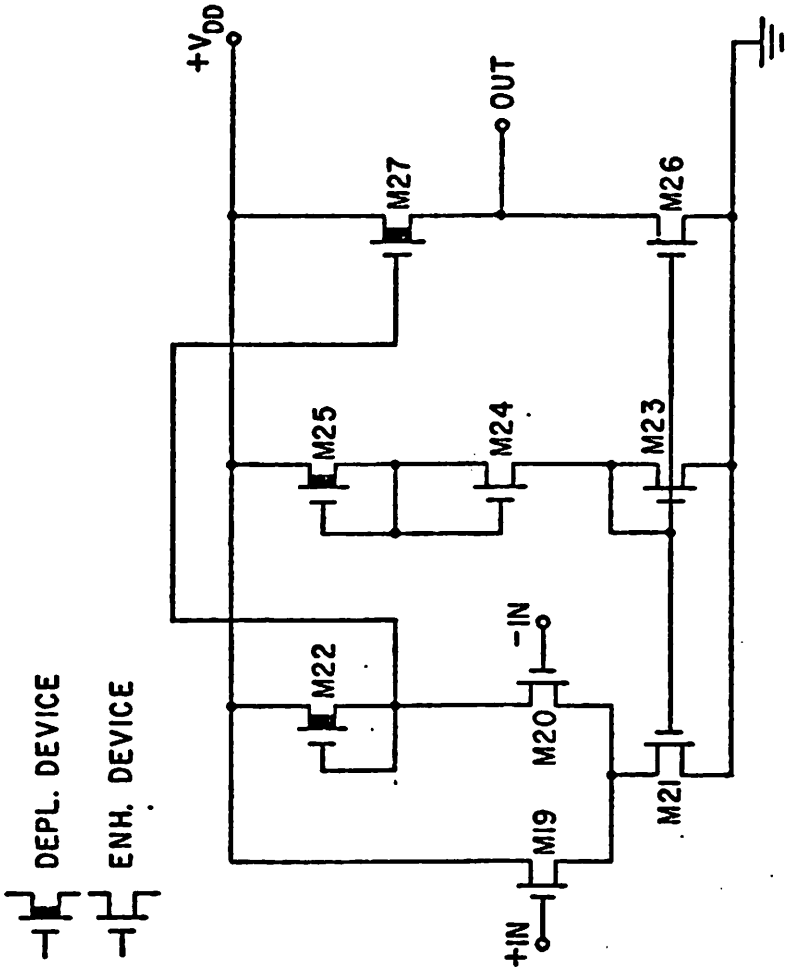


Figure 5.10: A single channel NMOS differential pair with depletion loads

TABLE II

Mask Device Dimensions

Device	w(μm)	ℓ(μm)
M1	250	20
M2	250	20
M3	10	30
M4	35	20
M5	15	20
M6	10	25
M7	10	30
M8	15	20
M9	10	25
M10	165	20
M11	107.05	25
M12	107.05	30
M13	10	25
M14	10	30
M15	165	20
M16	122.5	30
M17	165	20
M18	122.5	30
M19	250	20
M20	250	20
M21	35	20
M22	10	30
M23	15	20
M24	10	25
M25	10	30
M26	165	20
M27	122.5	30

$$V_T = V_{FB} + \phi_B + V_{bulk} \tag{5.76}$$

The flat-band voltage, V_{FB}, is given by [34]

$$V_{FB} = \phi_{MS} - \frac{Q_{ox}}{C_{ox}} \tag{5.77}$$

Since we estimate for our process t_{ox} = 700 Å and $Q_{ox}/q \cong 10^{11}cm^{-2}$ [49], we calculate $V_T = -0.645V + V_{bulk}$. For a nonimplanted wafer (C_B=5x10^{-14}), the body effect coefficient is $\gamma = 0.258\ \sqrt{V}$, so that body bias -6V would be necessary for $V_T = 0$.

The threshold voltage can be raised by implanting boron so that the threshold voltages of all enhancement devices would be near 0V with zero body bias. A boron dose $7.8x10^{11}cm^{-2}$, energy 50 keV, raises the threshold voltage by about $F_B Q_{IB}/C_{ox}$, where Q_{IB} is the ion-implanted charge and F_B is the activation parameter. Based on previous experiments F_B = 1/3 [48], and Q_{IB} can be calculated from the dose. The resulting threshold voltage shift is $\Delta V_T = 0.823$ V. To first order, a step function of depth D can be used to approximate the actual implanation profile. If D is small or equal to the depletion layer width w_α, then the body effect coefficient changes: the substrate doping concentration, C_B, is replaced by the step doping concentration, N_S [47]:

$$N_S \cong C_B + F_B \frac{Q_{IB}}{qD} \tag{5.78}$$

An estimate for our case, based on curves for projected range [44], is $N_S \cong 10^{16}cm^{-2}$. The body effect coefficient γ is then 1.153 $\sqrt{V}$. The threshold voltage equation for enhancement mode devices is

$$V_T = 0.178\ V + 1.153\ \sqrt{V}\ \sqrt{0.542V - V_{BS}} \tag{5.79}$$

A second ion implantation has to be performed for depletion devices. As we plan to implant the whole wafer with boron, the final threshold voltage shift of the depletion devices will be given by the difference of both threshold votlage shift

$$\Delta V_T = F_B \frac{Q_{IB}}{C_{ox}} - F_p \frac{Q_{IP}}{C_{ox}} \tag{5.80}$$

Phosphorous dose of $2.1\text{x}10^{12}\text{cm}^{-2}$, energy 150 keV and $F_p = 1/2$ [48], yield $\Delta V_T = -2.5$ V. An estimate of the step doping concentration which considers both implants gives $N_S \approx 2.7\text{x}10^{16}\text{cm}^{-2}$. Because this is mainly phosphorous, w_d will increase so that $w_d > D$. Assuming a linear tail of the implanted profile, we take $N_S(x=w_d) \approx N_S D/w_d$ $= 2.7\text{x}10^{16}\text{x}0.3\ \mu\text{m}/5\ \mu\text{m}$ and use this value for γ calculation: $\gamma \approx 0.463\ \sqrt{V}$. The threshold voltage equation for depletion devices is then given by

$$V_T = -3.145\ \text{V} + 0.463\ \sqrt{V}\ \sqrt{0.542V - V_{BS}} \tag{5.81}$$

The conduction factor k used in this work is given by Eq. (4.3):

$$k = k' \left(\frac{W}{\ell}\right) = \frac{1}{2}\mu C_{ox}\left(\frac{W}{\ell}\right) \tag{5.82}$$

Previous investigations for a similar process and substrate material have yielded following data: $t_{ox} = 700$ Å, $\mu = 868\ \text{cm}^2/\text{V sec}$ [49]. Hence $k' = 22\ \mu\text{A/V}^2$.

The dimension ℓ in Eq. (5.82) is the electrical effective channel length, which is the distance between the source and drain N-regions. This distance is less than the masking dimension by the amount of lateral N-region diffusion:

$$\ell = \ell_{mask} - 2L_D X_j \tag{5.83}$$

in which X_j is the junction depth and L_D is the lateral diffusion coefficient. From Ref. [49] we take $2L_D X_j = 0.2$ mil.

5.3.3. Bias Current Calculations

The next step in our design is to determine bias currents in the operational amplifier. All bias currents are set by the bias string M5, M6, M7 (Fig. 5.11a). Its quiescent current is 22 μA when Eq. (4.2) and parameters derived in Section 5.3.2 are employed. Power supply +15V and substrate bias -2.5V are assumed. The quiescent voltages are $V_A = 3.2$ V and $V_B = 7.67$ V.

All other bias currents will be scaled according to the (W/ℓ) ratio of each current source, as described in Section 4.3.2. The values of all bias currents are given in Fig. 5.11b. Since all the quiescent voltages track the quiescent voltages of the bias string V_A and V_B, all DC voltage level in the amplifier are known.

The predicted power supply current is then 0.82 mA, which results in a power dissipation of 12.3 mW.

Similar design considerations are valid for the differential pair. The power supply current should be about 0.32 mA and power dissipation 4.8 mW.

5.3.4. Gain Calculations

Let us proceed to calculate the voltage gain. Substituting the quiescent currents and voltages derived in Section 5.3.3 in small-signal MOSFET parameters (Eq. (4.10), (4.11) and (4.24b)) gives the transconductance and the output impedance of device of interest. E.g.:

$$g_{m1} = 2\sqrt{k'\left(\frac{W}{\ell}\right)_1 I_{D1}} = 2\sqrt{22\mu A/V^2 \times \frac{10\ \text{mil}}{(0.8-0.2)\text{mil}} \times 25.67\ \mu A} = 1/(5.154k\Omega) \tag{5.84}$$

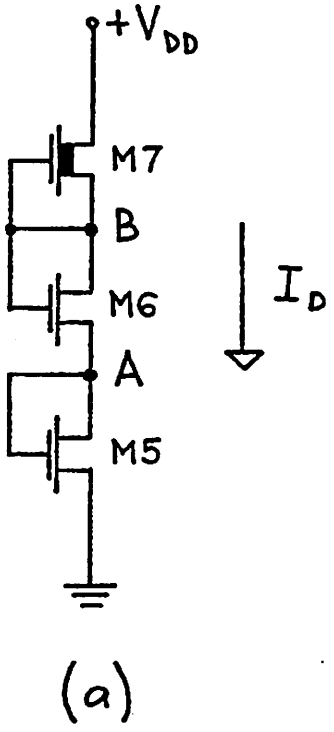


Figure 5.11.a: The bias string

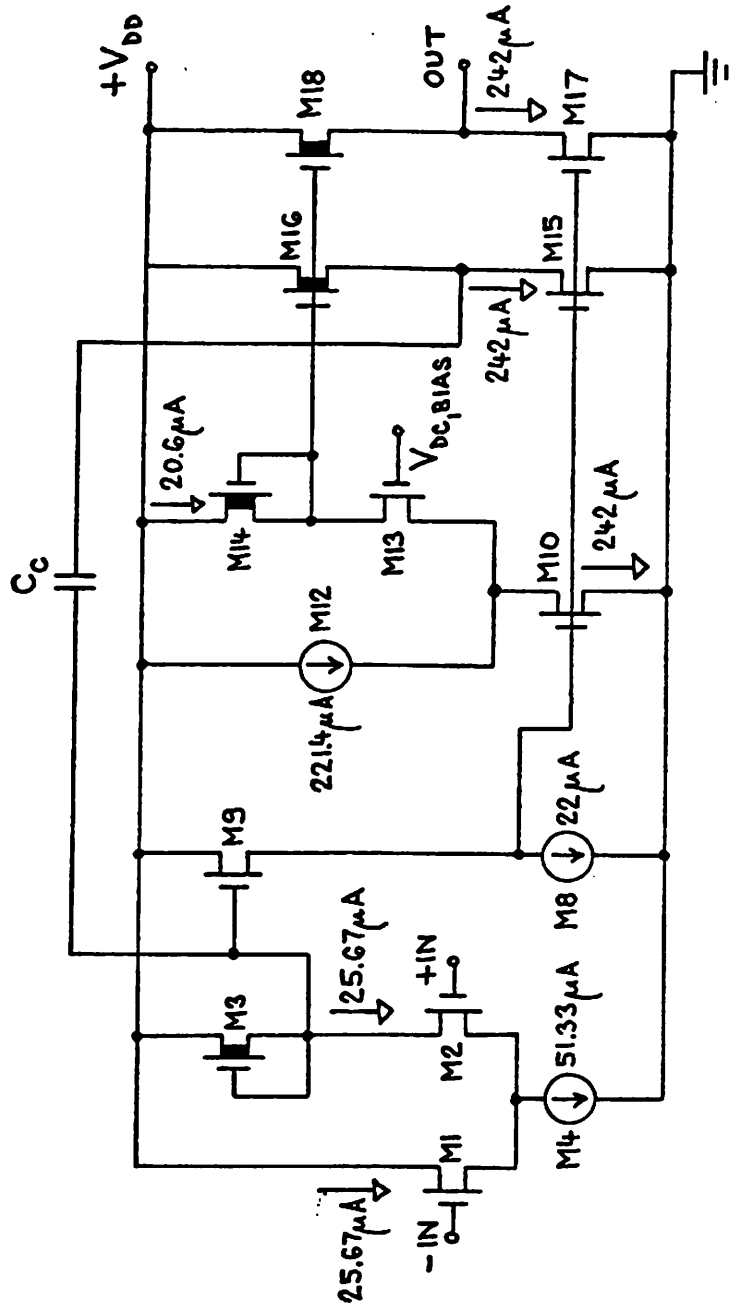


Figure 5.11.b: Bias currents in the NMOS operational amplifier

If the channel length modulation is neglected, the output impedance of device M3 is primarily determined by the body effect (λ=0):

$$r_{03} = \frac{1}{\gamma_3}\sqrt{\frac{\phi_{B3}+V_{BB}+V_B}{k'(\frac{W}{\ell})_3 I_{D3}}} = \frac{1}{0.463\sqrt{V}}\sqrt{\frac{0.542V+2.5V+7.67V}{22\mu A/V^2 \times \frac{0.4\ mil}{(1.2-0.2)mil} \times 25.67\mu A}}$$

$$= 470.8\ k\Omega \qquad (5.85)$$

The differential-mode voltage gain of the input stage M1, M2, M3 and M4 is given by

$$|A_{v1}| = \frac{g_{m1}(r_{01}\|r_{04})+g_{m2}r_{02}}{r_{03}+r_{02}+(r_{01}\|r_{04})}\frac{r_{03}}{2} \qquad (5.86)$$

Assume $\lambda = 0$. Hence $r_{01} = r_{02} = r_{04} = \infty$. Equation (5.86) then yields

$$|A_{v1}| = (g_{m1}+g_{m2})\frac{r_{03}}{2} = 45.67 \qquad (5.87)$$

for $g_{m1} = g_{m2}$.

The input stage is followed by the level shifter M8, M9 which has the voltage gain

$$|A_{v2}| = \frac{g_{m9}(r_{08}\|r_{09})}{1+g_{m9}(r_{08}\|r_{09})} \qquad (5.88)$$

Again we can proceed as above; assume $r_{08} = \infty$ and r_{09} is finite due to body effect. The final calculation gives $|A_{v2}| = 0.8125$.

The voltage gain of the main gain stage (M10, M11, M12, M13 and M14) can be calculated as

$$|A_{v3}| = \frac{g_{m10}r_{014}}{\frac{r_{013}+r_{014}}{(g_{m13}r_{013}+1)(r_{010}\|r_{012})} + 1} \tag{5.89}$$

This becomes for $r_{010} = r_{013} = \infty$

$$|A_{v3}| = \frac{g_{m10}r_{014}}{\frac{1}{g_{m13}r_{012}} + 1} = 151.5 \tag{5.90}$$

Finally, the output stage M17, M18 has a voltage gain of

$$|A_{v5}| = \frac{g_{m18}(r_{017}\|r_{018})}{1+g_{m18}(r_{017}\|r_{018})} \tag{5.91}$$

For $r_{017} = \infty$, the gain is $|A_{v5}| = 0.934$. The voltage gain of the feedthrough path (see Fig. 5.12a) is

$$|A_{v4}| = \frac{g_{m17}}{g_{m18}} = 1.5 \tag{5.92}$$

The gains A_{v4} and A_{v3} are added at the output of the output stage so that the voltage gain of this part of the amplifier is given by $(A_{v3}+A_{v4})A_{v5}$. This is shown in Fig. 5.12b.

The block diagram of the operational amplifier is shown in Fig. 5.12c in which the frequency compensation path is included. The total open-loop voltage gain is

$$A_{vtot} = A_{v1}A_{v2}(A_{v3}+A_{v4})\,A_{v5} = 5303 \tag{5.93}$$

The block diagram of the differential pair is illustrated in Fig. 5.12d.

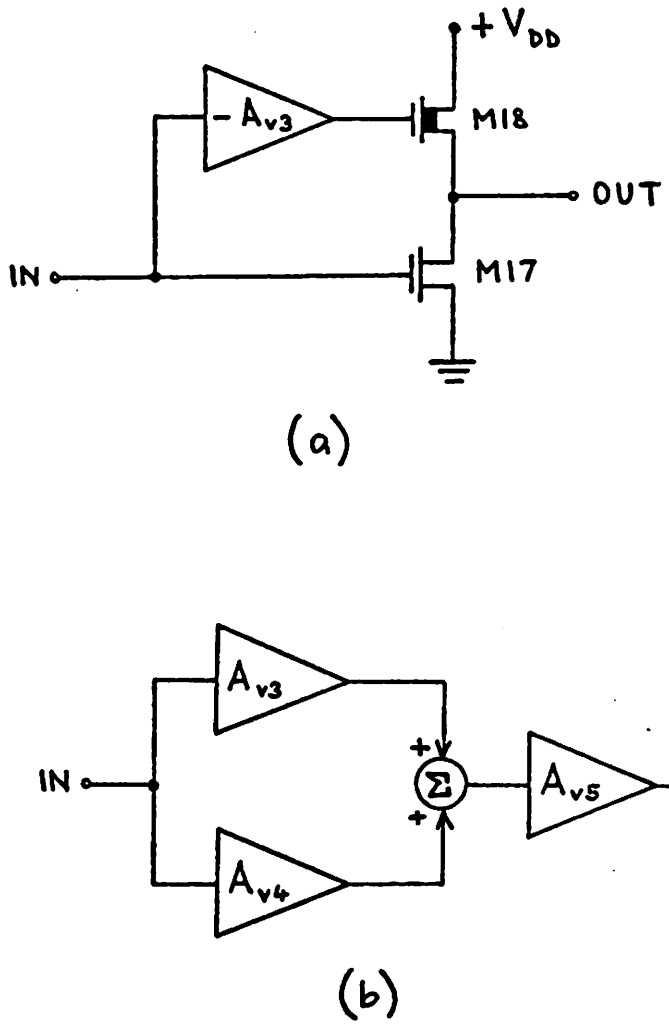
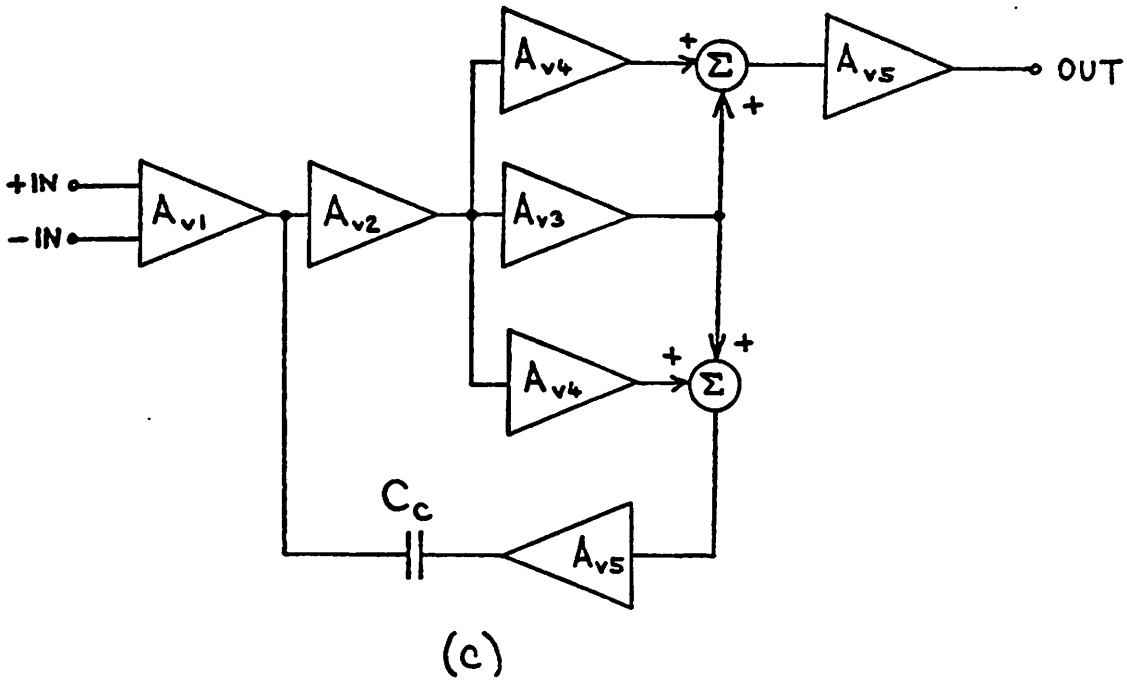


Figure 5.12: (a) Circuit diagram of the feedforward path
(b) Block diagram of a



(c)

(d)

Figure 5.12: (c) Block diagram of the operational amplifier
(d) Block diagram of the differential pair

The gain can be found as

$$A_{vtot} = A_{v1}A_{v5} = 42.6 \tag{5.94}$$

5.3.5. Common-mode Rejection Ratio

The CMRR will be mainly determined by the input stage. The common-mode voltage gain of the input stage can be derived as

$$A_{cm1} = r_{03}\frac{g_{m1}(r_{01}\|r_{04})-g_{m2}r_{02}}{r_{03}[1+g_{m1}(r_{01}\|r_{04})]+r_{02}[1+(g_{m1}+g_{m2}+\frac{1}{r_{02}})(r_{01}\|r_{04})]} \tag{5.95}$$

The CMRR is then given by

$$CMRR = 20\ \log\frac{A_{v1}}{C_{cm1}} \tag{5.96}$$

Naturally, $A_{cm1} = 0$ for $r_{01} = r_{02} = r_{04} = \infty$. Assuming the value of $\lambda = 0.11/\ell$ [49], we can estimate that $r_{04} = 1.063$ MΩ. Then $A_{cm1} = 0.2209$ for $r_{01} = r_{02} = \infty$ and hence CMRR = 46.31 dB. This is rather low but since CMRR is not important for our application it is not necessary to increase it.

5.3.6. Unity-gain Frequency

A 6 pF capacitor has been used for compensation of the operational amplifier. The small-signal impedance at the source of M3 is $r_{03} = 470.8$ kΩ if r_{02} is neglected. The capacitance at this node is given by the compensation capacitor multiplied by $A_{v2}(A_{v3}+A_{v4})A_{v5}$. Therefore the frequency of the dominant pole is (see Eq. (4.96) and (4.106a))

$$f_{3dB} = \frac{1}{2\pi r_{03}C_cA_{v2}(A_{v3}+A_{v4})A_{v5}} = 485\ \text{Hz} \tag{5.97}$$

Equation (5.97) would contain $(r_{02} \| r_{03})$ instead of r_{03} if $r_{02} \neq \infty$.

The unity-gain frequency GBW of the operational amplifier is approximately (Eq. (4.99))

$$GBW = f_{3dB} A_{vtot} = 2.57 \text{ MHz} \tag{5.98}$$

An attempt was made to simulate the operational amplifer using the circuit analysis program SPICE 2. This program uses the MOSFET model which is derived from the Frohman-Grove model [50]. The simulation predicted a total gain of 9750, further the dominant pole was at 250 Hz and the unity-gain frequency was at 4.7 MHz. The total power supply current was 1.1 mA. Measurements performed on fabricated amplifiers showed that values prediced by hand calculation were more accurate than the values predicted by SPICE 2 simulation. The difference is obviously due to different modeling approach.

Nevertheless, the computer simulation can help to predict frequency behavior of the amplifier because all voltage gains and quiescent currents are scaled up in the same way.

The capacitances do not scale with the exception of the Miller capacitance which scales with the gain (Eq. (5.97)). The node capacitances have to include metal interconnect capacitances and pin capacitances.

Figure 5.13a shows the frequency response of the operational amplifier without feedforward path, i.e., the gates of M15 and M17 are connected to a DC voltage source. The form of the response suggests that there is a pair of complex poles in the right half plane due to pole-splitting. The simulations confirmed that this configuration is not stable.

The frequency response of the feedforward path is shown in

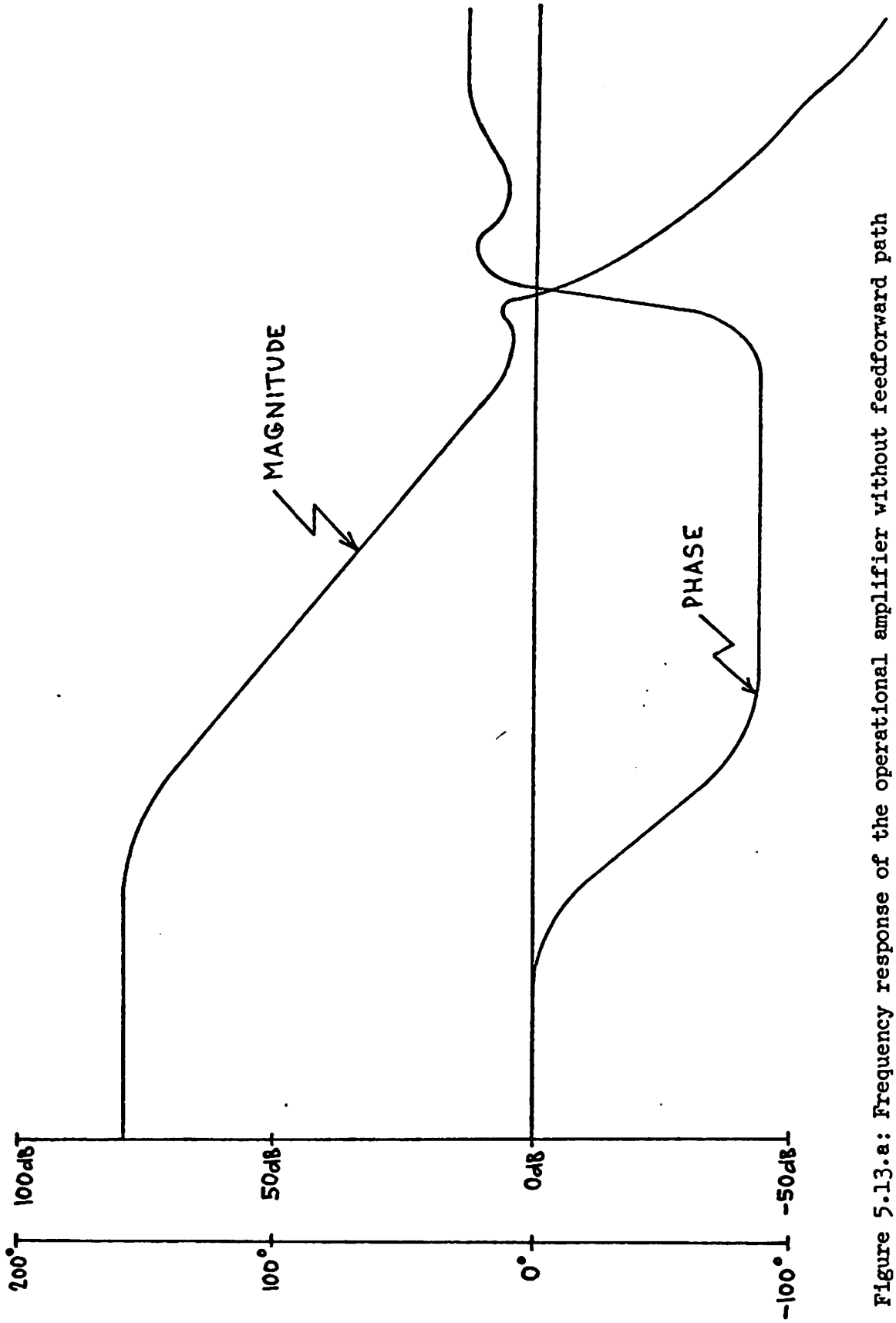


Figure 5.13.a: Frequency response of the operational amplifier without feedforward path

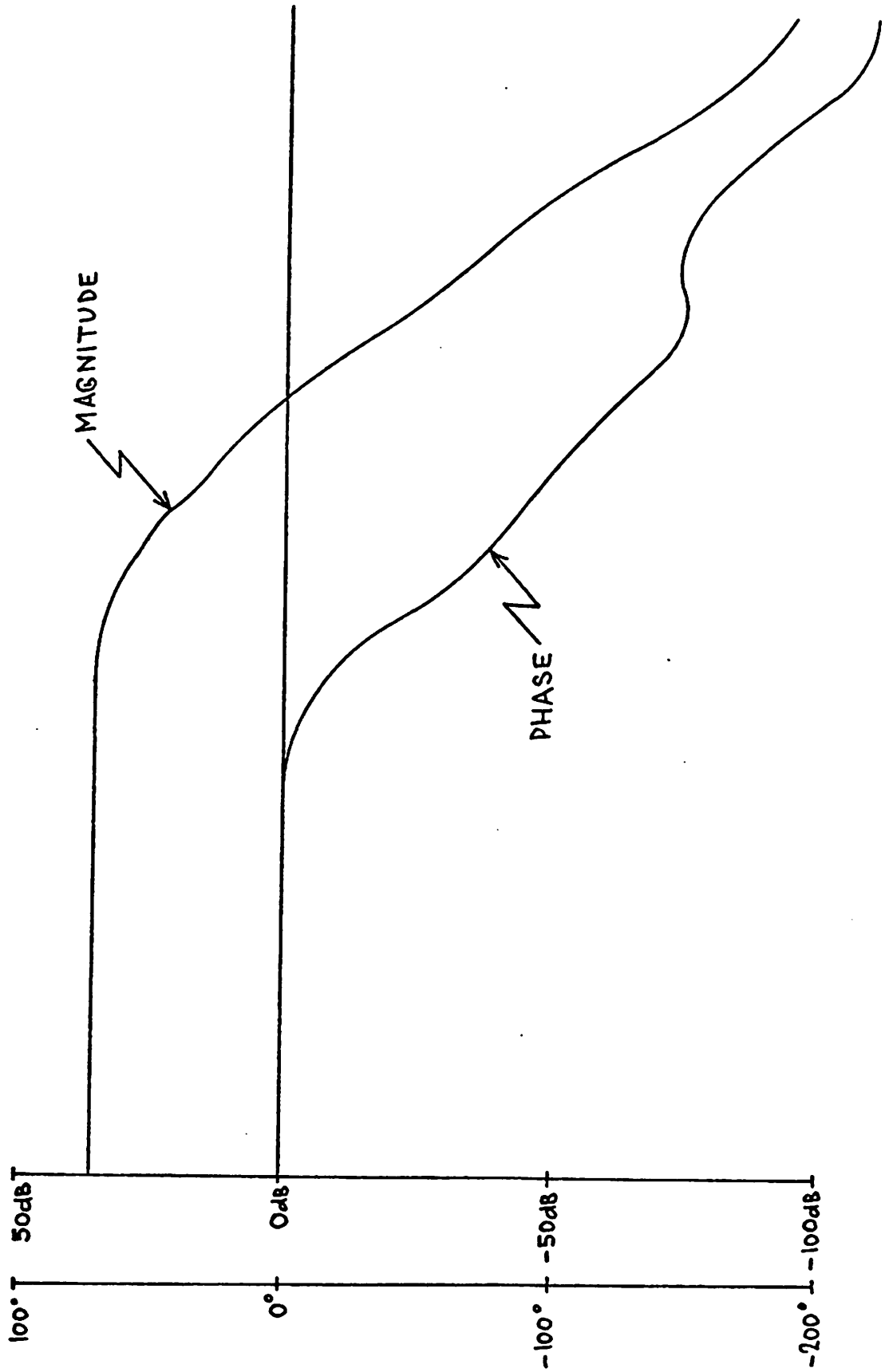


Figure 5.13.b: Frequency response of the feedforward path

Fig. 5.13b. The effect of the feedforward can be seen from Fig. 5.13c which shows the frequency response of the complete operational amplifier (see Section 4.5.2). The phase margin is $\phi_m = -2.5°$ and consequently the amplifier would not be stable when connected as a voltage follower (Eq. (5.13)).

The stability problem of a sampled data integrator discussed in Section 5.1.1 can be now solved for our particular case. From the circuit lay-out the approximate values are $\alpha C \simeq 4$ pF, $C \simeq 2$ pF and $C_{par} \simeq 2$ pF (rather large because the inverting input is connected to a package pin for testing purposes). Using Eq. (5.10) and (5.11) we find $\beta = 1/3$ and $\beta' = 1/2$. The amplifier will be stable because $\phi_m = 81°$ for $1/\beta' = 6$ dB.

According to the frequency response shown in Fig. 5.13c the first two poles needed for the small-signal settling time estimate are $p_1/2\pi = 250$ Hz and $p_2/2\pi = 3.5$ MHz. The conservative hand calculation yielded $p_1/2\pi = 485$ Hz and GBW = 2.57 MHz. Let us assume that the second pole lies at the hand calculated unity-gain frequency. When all other poles and all zeros are neglected, the settling time t_s can be estimated using Eq. (5.16), (5.17) and (5.18) as $t_s \simeq 0.74$ μsec.

The dominant pole of the differential pair can be predicted from the following expression:

$$f_{3dB} = \frac{1}{2\pi(r_{02} \| r_{03})C_3} \tag{5.59}$$

From above we get $r_{02} = \infty$ and $r_{03} = 470.8$ kΩ. From lay-out we obtain $C_3 = 3.6$ pF. The calculations then yield $f_{3dB} = 94$ kHz and GBW = 4 HMz.

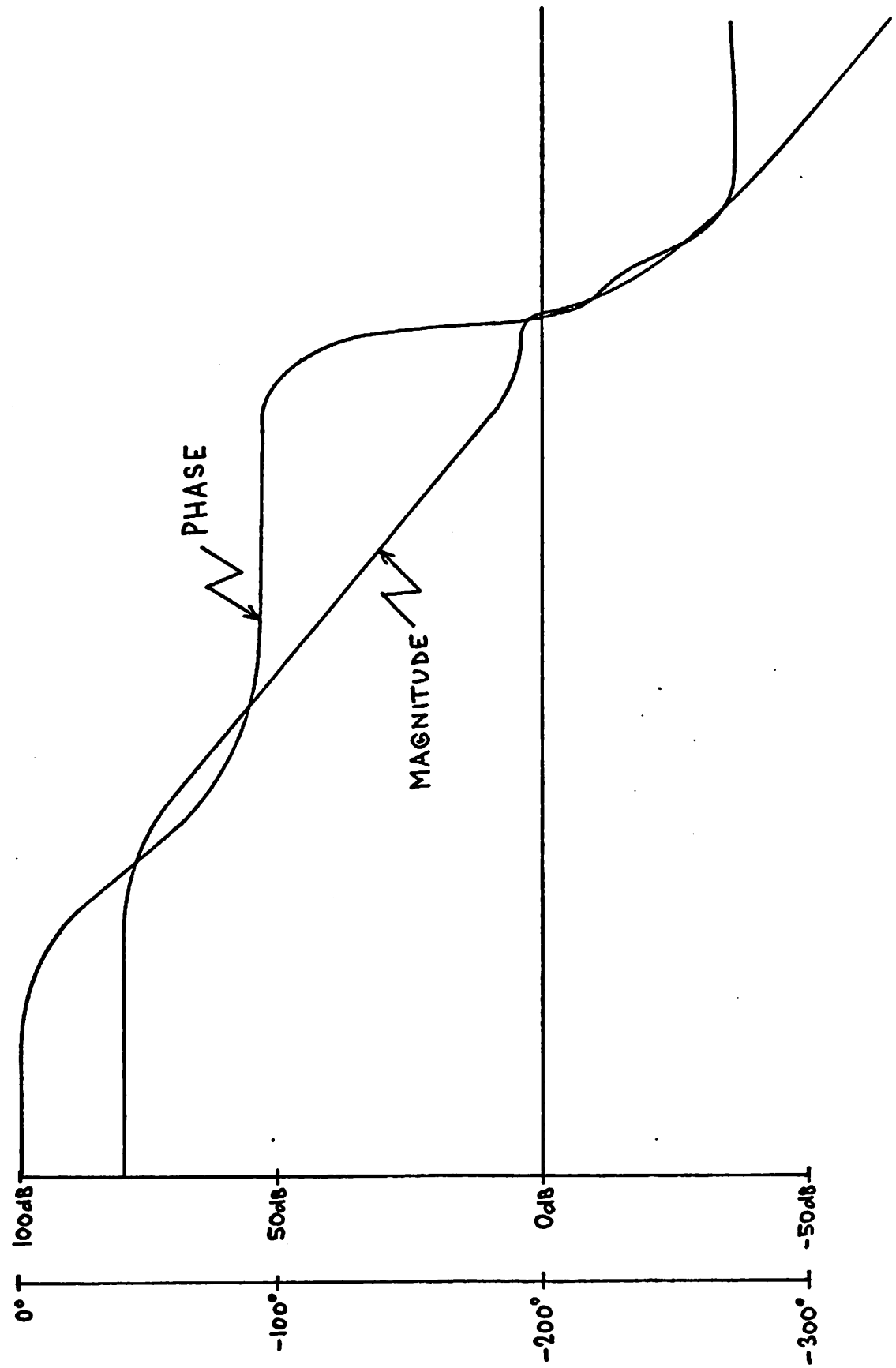


Figure 5.13.c: Frequency response of the operational amplifier with feedforward path

5.3.9. Conclusions

While the voltage gain of the differential pair is more than sufficient, according to hand calculation the voltage gain of the operational amplifier is about 10% lower than required. This would result in 1% Q variation (Eq. (5.73)) which is very small and therefore negligible.

As far as the slew rate requirement is concerned, it has been stated in Section 5.1.1 that the amplifier only needs to respond to the change of the output signal at the passband frequencies. The critical one will be obviously the center frequency f_0 for which the max. change is

$$\left.\frac{dv_{out}}{dt}\right|_{max} = \pi f_0 V_{out,pp} \tag{5.103}$$

for an output signal $v_{out}(t) = (V_{out,pp}/2) \sin \omega_0 t$. This will cause a change at the output of the amplifier of ΔV after a clock cycle T_c. Hence

$$\Delta V = \pi \frac{f_0}{f_c} V_{out,pp} \tag{5.104}$$

The slewing time can be then estimated from the formula $t_{slew} = \Delta V/SR$ as

$$t_{slew} = \frac{\pi}{SR} \frac{f_0}{f_c} V_{out,pp} = 0.4 \ \mu sec \tag{5.105}$$

for SR = 4.3 V/ μsec, $f_0/f_c = 0.0366$ and $V_{out,pp} = 15$ V.

Considering the small-signal settling time of 0.74 μsec and slewing time of 0.4 μsec we can conclude that the operational amplifier should be able to operate for clock rate in the order of several hundreds of kHz.

5.3.7. Slew Rate

When the differential input voltage exceeds the value of $2\sqrt{I_{D4}/(k'(\frac{W}{\ell})_2)}$, i.e. 0.81 V for our case, the amplifier slews at a limiting rate determined by the quiescent current of the input stage and the compensation capacitor. The max. slew rate depends on max. current the input stage can provide to charge or discharge the compensation capacitor. Under this condition the max. slewing rate across this capacitor is

$$\frac{dV_{c_c}}{dt} = \frac{I_{D3}}{C_c} \tag{5.100a}$$

for a negative-going output (see Fig. 5.11): since M2 is cut-off, the current I_{D3} diverted into the integrator consisting of the capacitor C_c and the amplifier $A_{v2}(A_{v3}+A_{v4})A_{v5}$ [37]. Similarly we can find

$$\frac{dV_{c_c}}{dt} = \frac{I_{D4}-I_{D3}}{C_c} \tag{5.100b}$$

for a positive-going output. The max. slew rate is then given by

$$SR = 4.3 \text{ V}/\mu\text{sec} \tag{5.101}$$

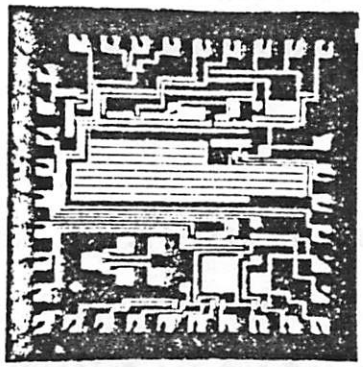
for $C_c = 6$ pF, $I_{D3} = 25.67$ μA and $I_{D4} = 51.33$ μA.

5.3.8. Output Impedance

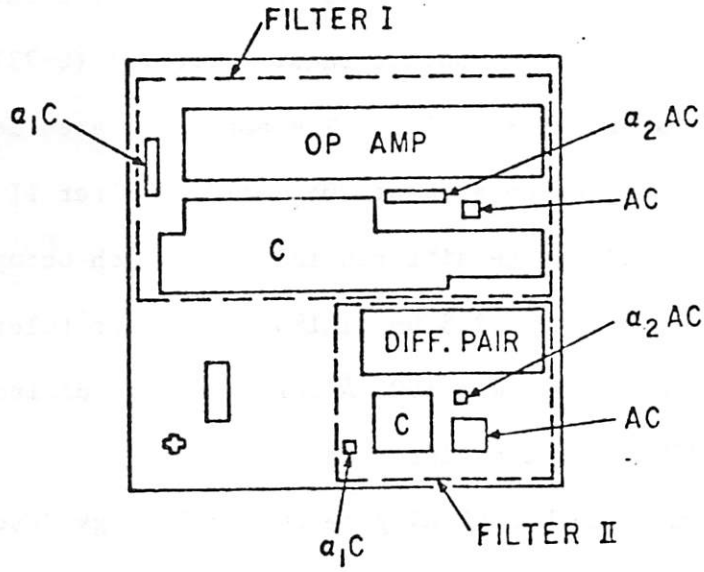
The output impedance of the amplifier is given by

$$Z_{out} = \frac{1}{g_{m18}} \left| r_{018} \right| r_{017} \tag{5.102}$$

For our case $Z_{out} \approx 2.9$ kΩ. The same value applies for the differential pair.



(a)



(b)

Figure 6.1: (a) Photograph of the integrated circuit
(b) Lay-out block diagram of a

CHAPTER 6

EXPERIMENTAL RESULTS

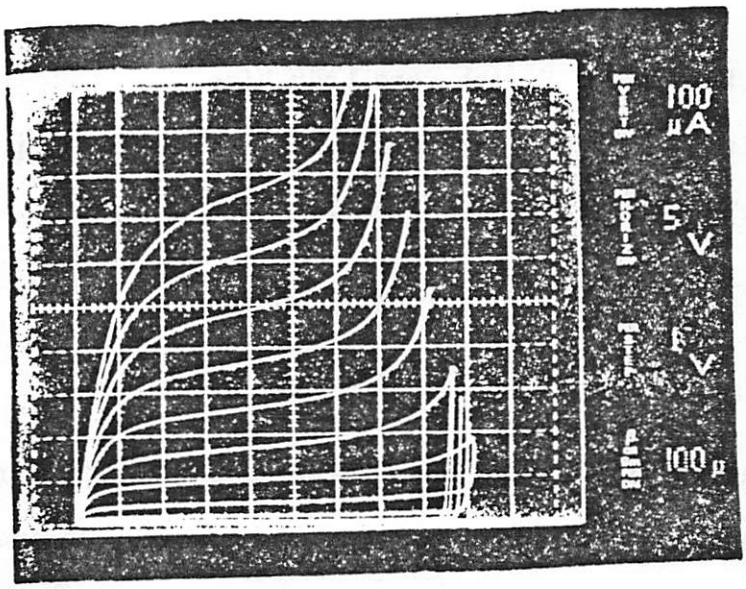
6.1. Introduction

Two version 3 low pass filters (Fig. 3.10a) have been fabricated. One was designed to be a high Q filter with Q = 73.14 at a center frequency of $f_0 = 0.0366\ f_c$, while the second had the relatively low Q of 0.99 at a center frequency of $0.0165\ f_c$.

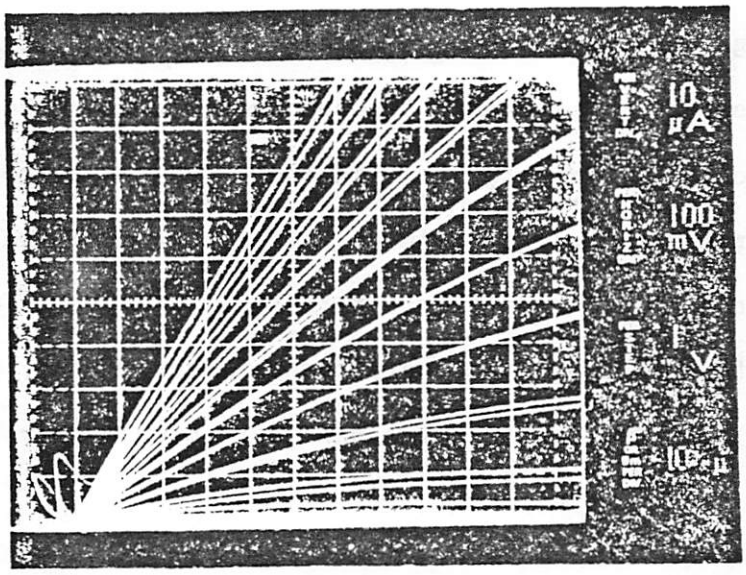
6.2. Description of the Integrated Circuit

The photograph of the completed IC is shown in Fig. 6.1a. The overall IC size is 76 x 76 mil including contact pads. Filter I (Q=73) uses the operational amplifier shown in Fig. 5.9. The amplifier area is 636 mil^2 and the total filter occupies an area of 2050 mil^2. Filter II (Q=1) has an area of 784 mil^2 including the differential pair which occupies 320 mil^2. A 10 μm minimum feature size and 2.5 μm minimum alignment tolerance were used. The thin oxide thickness was 1000 Å for capacitor dielectrics (grown over n^+) and 700 Å for transistor gates.

The process used an n-channel Aℓ-gate MOS technology described in the appendix. The starting material was lightly doped ($C_B=5x10^{14}cm^{-3}$) p-type silicon with ⟨100⟩ crystal orientation. Therefore p^+ isolation diffusion was necessary in order to increase the threshold voltage of the parasitic thick oxide transistors. Further the whole wafer was implanted with boron (dose $7.8x10^{11}/cm^2$, energy 50 keV) so that the threshold voltages of all enhancement devices would be near 0 V with zero body bias. The depletion devices were implanted with phosphorous with a dose of $2.1 \times 10^{12}/cm^2$ at an energy of 150 keV. The threshold voltage of the



(a)



(b)

Figure 6.2: (a) I_D vs. V_{DS} of the enhancement mode MOSFET
(b) I_D vs. V_{DS} of the enhancement mode MOSFET

depletion loads is near -3 V with zero body bias.

The capacitor areas were defined solely by the metal pattern. The area ratios of the capacitors are as follows:

Filter I: $\alpha_1 = 0.028$, $\alpha_2 = 1.99$, $A = 0.015$

Filter II: $\alpha_1 = 0.06$, $\alpha_2 = 0.182$, $A = 0.295$

Because of higher sensitivity of Q to coefficients for filter I (high Q) an effort has been made to make the ratio of capacitor perimeters the same as the ratio of the areas (see section 5.1.11). This minimizes the dependence of the area ratio on the etching of the metal pattern. The smallest capacitor used in filter I was 2 pfs. and was 1 pf. in filter II.

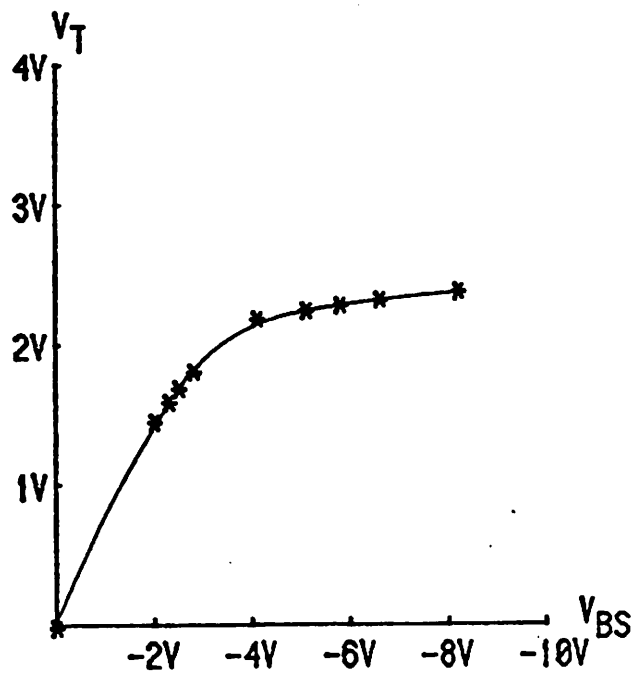
The package used was a 40 pin multilayer ceramic dual-in-line package. The measured capacitance between two adjacent unbonded pins was 0.2 pF and capacitance between a pin and the package ground was 1.5 pF.

As seen from the photograph in Fig. 6.1a, the IC contains 38 bonding pads. Most of these were used only for testing purposes. For the actual operation only four pads are necessary for a filter (input, output and two-phase clock) in addition to three pads for power supply, ground and substrate bias.

6.3. MOSFET Characteristics

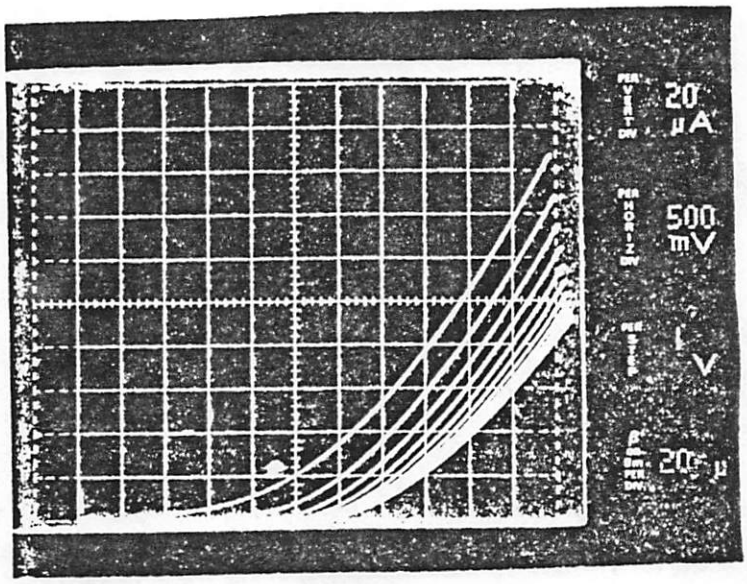
Two test devices were incorporated in the IC die. One was an enhancement mode device and the other one was a depletion mode device.

Figures 6.2a and 6.2b illustrate the drain current-voltage characteristics of the N-channel enhancement mode MOSFET, i.e. I_D vs. V_{DS}. The geometries were $w = 0.4$ mil and $\ell = 0.8$ mil. V_{GS} was varied 1V/step and last step was 10 V. The substrate bias used was $V_{BS} = 0$ V.



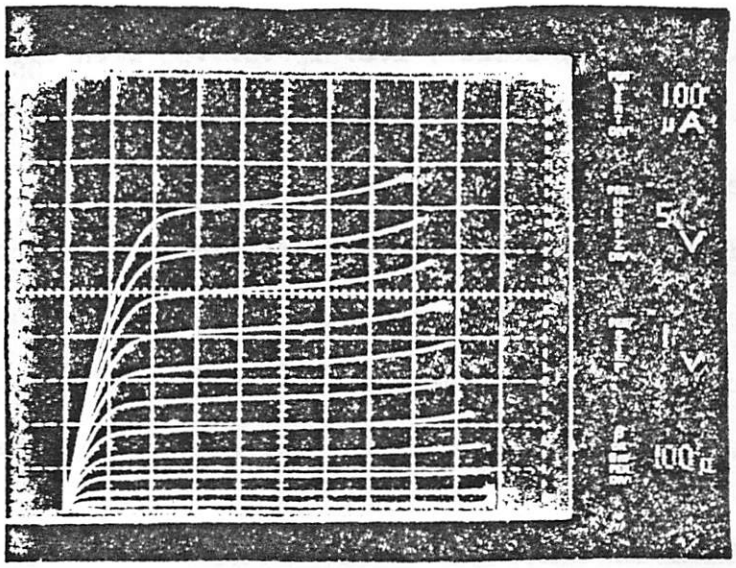
(d)

Figure 6.2.d: V_T vs. V_{BS} of the enhancement mode MOSFET

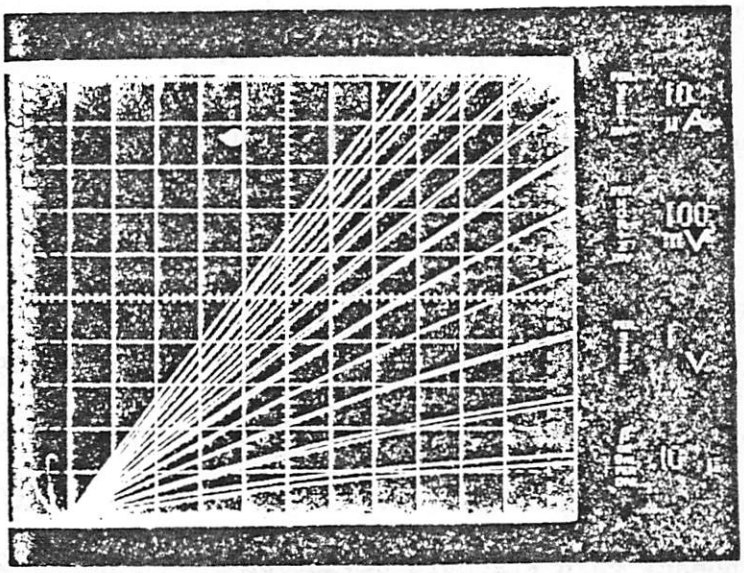


(c)

Figure 6.2.c: I_D vs. V_{BS} of the enhancement mode MOSFET



(a)



(b)

Figure 6.3: (a) I_D vs. V_{DS} of the depletion mode MOSFET
(b) I_D vs. V_{DS} of the depletion mode MOSFET

Fig. 6.2c shows the body effect, i.e. I_D vs. V_{BS} with $V_{GS} = V_{DS}$. The last step was $V_{BS} = -10$ V. The effect of substrate bias on the threshold voltage is shown in Fig. 6.2d.

The drain current-voltage characteristics of the N-channel depletion mode MOSFET can be seen in Fig. 6.3a and 6.3b. The dimensions were $w = 0.4$ mil and $\ell = 1.4$ mil; the substrate bias was $V_{BS} = 0$ V and last step was 10 V. Fig. 6.3c shows V_T vs. V_{BS} characteristics.

6.4. Amplifier Performance

Table III contains the measured performance of a sample of five amplifiers. The DC transfer characteristic of the operational amplifier can be seen in Fig. 6.4a. The power supply voltage was 15 V and substrate bias was -2.5 V.

When the substrate bias was varied, following parameter changes were noticed (with 15 V power supply):

Substrate bias	0V	-2.5V	-5V
Input offset voltage mean	120mV	49mV	23.4mV
Input offset voltage standard deviation	11mV	9mV	7mV
Low frequency gain mean	3750	6000	7850
Low frequency gain standard deviation	230	290	260

The equivalent input noise voltage of an amplifier can be expressed as (see sections 4.5.4 and 5.1.4)

$$\overline{v^2_{eq,tot}} = \overline{v^2_{eq,th}}\left(1+\frac{f_{Beq}}{f}\right) \qquad (6.1)$$

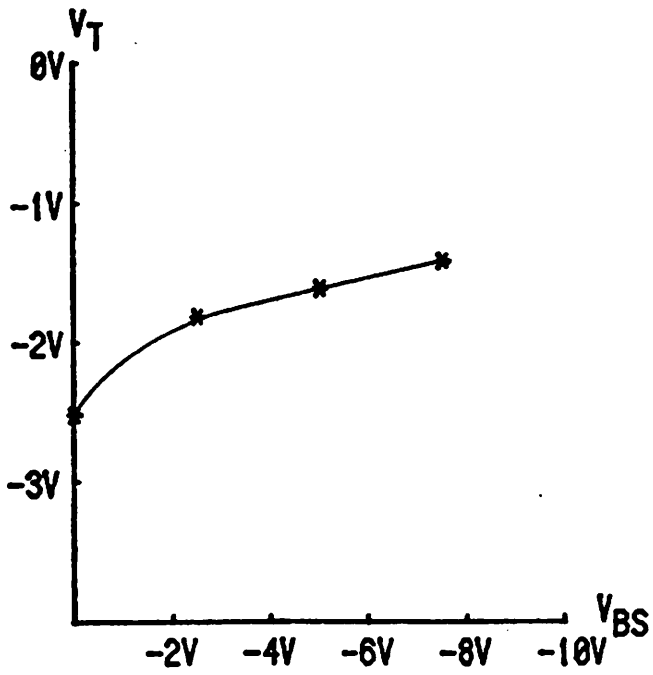
It has been found from measurements that the thermal noise was $\sqrt{\overline{v^2_{eq,th}}} = 100\ nV/\sqrt{Hz}$ and the flicker noise corner frequency was

TABLE III

PERFORMANCE PARAMETERS OF AMPLIFIERS

POWER SUPPLY +15V AND SUBSTRATE BIAS -2.5V

	OP. AMP.	DIFF. PAIR
Input offset voltage mean	49 mV	36.5 mV
Input offset voltage standard deviation	9 mV	20 mV
Low frequency gain mean	6000	40
Low frequency gain standard deviation	290	1
Common-mode rejection ratio	60 dB	56 dB
Unity-gain frequency	2 MHz	3.4 MHz
Slew rate	2 V/μs	2 V/μs
Power supply rejection ratio	48 dB	38 dB
Input noise voltage (up to 100 kHz)	45 μV	38 μV
Output voltage swing	+0.4 V, +14.3 V	+5.4 V, +14.0 V
Power consumption	13 mW	5 mW



(c)

Figure 6.3.c: V_T vs. V_{BS} of the depletion mode MOSFET

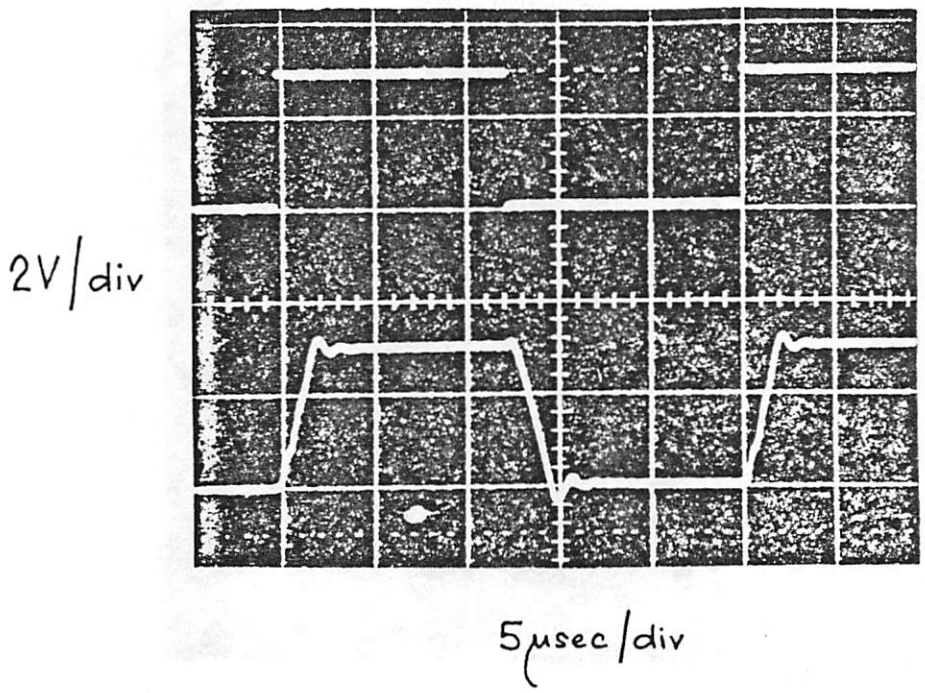


Figure 6.4.b: Step response of the operational amplifier connected as a voltage follower (load 55 pF). Top trace: input signal;bottom trace: output signal

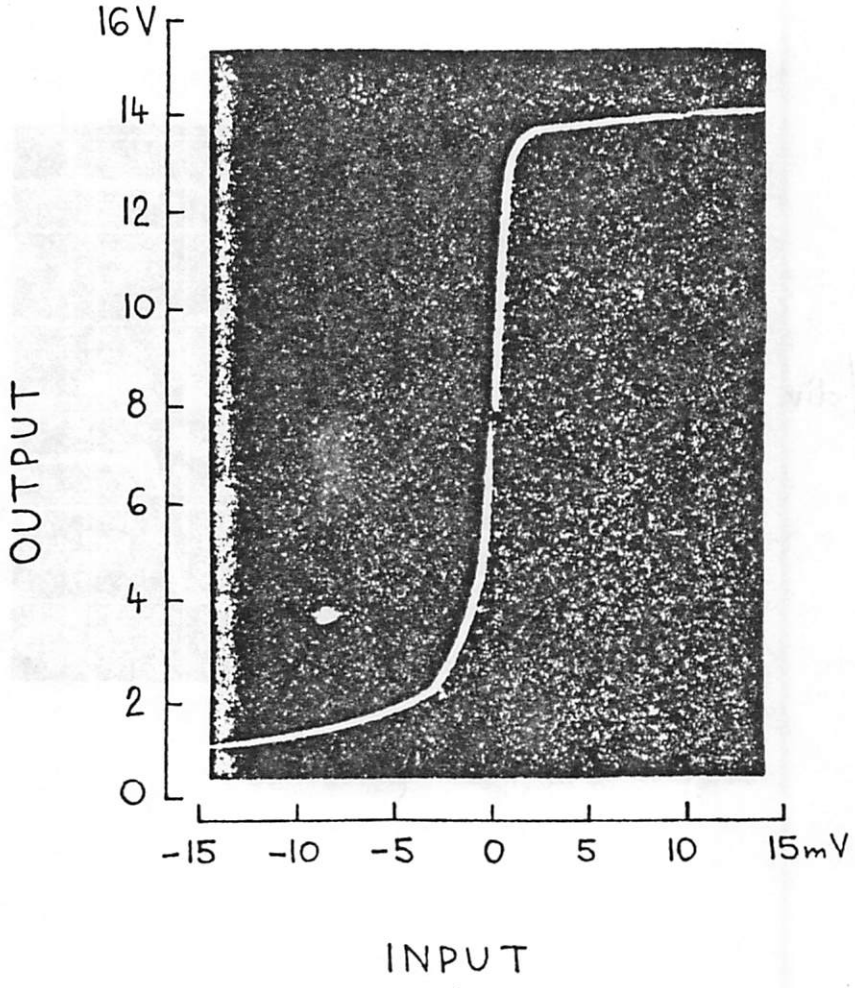


Figure 6.4.a: DC transfer curve of the operational amplifier

f_{Beq} = 5.5 kHz for the operational amplifier.

The operational amplifier had the tendency to oscillate when connected as a voltage follower without any load. This is due to the fact that the amplifier was compensated for its operation as a sampled data integrator only (sections 5.1.1 and 5.3.6). When the amplifier is to be used as a voltage follower, the compensation capacitor has to be larger. The oscillations stopped when either the substrate bias was lowered to 0 V or the amplifier was loaded by a capacitive load. Figure 6.4b shows the step response of the operational amplifier connected as a voltage follower and loaded by 55 pF.

The DC transfer characteristics of the differential pair is shown in Fig. 6.4c.

6.5. Amplifier Calculations Based on Measured MOSFET Characteristics

It is interesting to calculate the parameters of both amplifiers from the measured MOSFET characteristics.

First it is necessary to model our transistors. The best-fit of V_T vs. V_{BS} characteristics yielded two equations for the enhancement mode MOSFET (from Fig. 6.2d):

$$V_T = 1.215\sqrt{V}\sqrt{-0.556V-V_{BS}} \quad \text{for } -3V < V_{BS} < 0V \tag{6.2a}$$

$$V_T = 0.474\sqrt{V}\sqrt{17.47V-V_{BS}} \quad \text{for } -8V < V_{BS} < -4V \tag{6.2b}$$

Since the channel length modulation parameter λ from Eq. (4.5) is dependent on the electrical effective channel length ℓ (Eq. 5.83) we introduce a parameter $\lambda' = \lambda\ell$ so that

$$\lambda = \frac{\lambda'}{\ell} \tag{6.3}$$

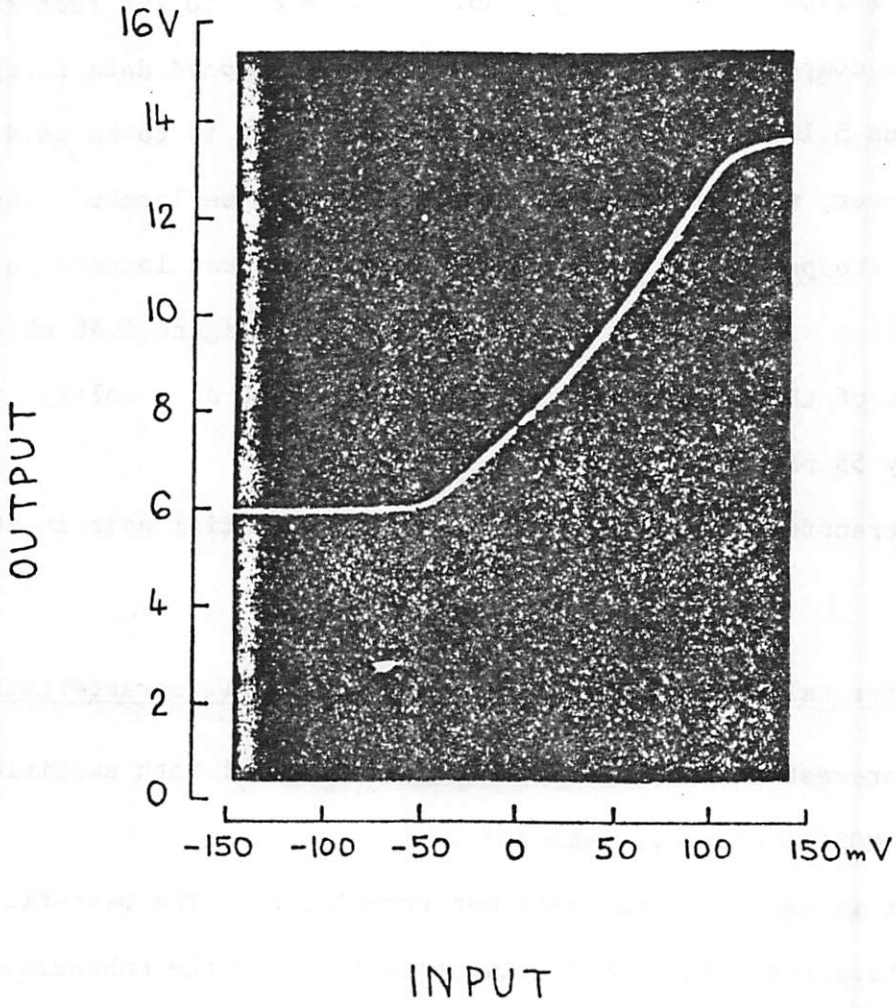


Figure 6.4.c: DC transfer curve of the differential pair

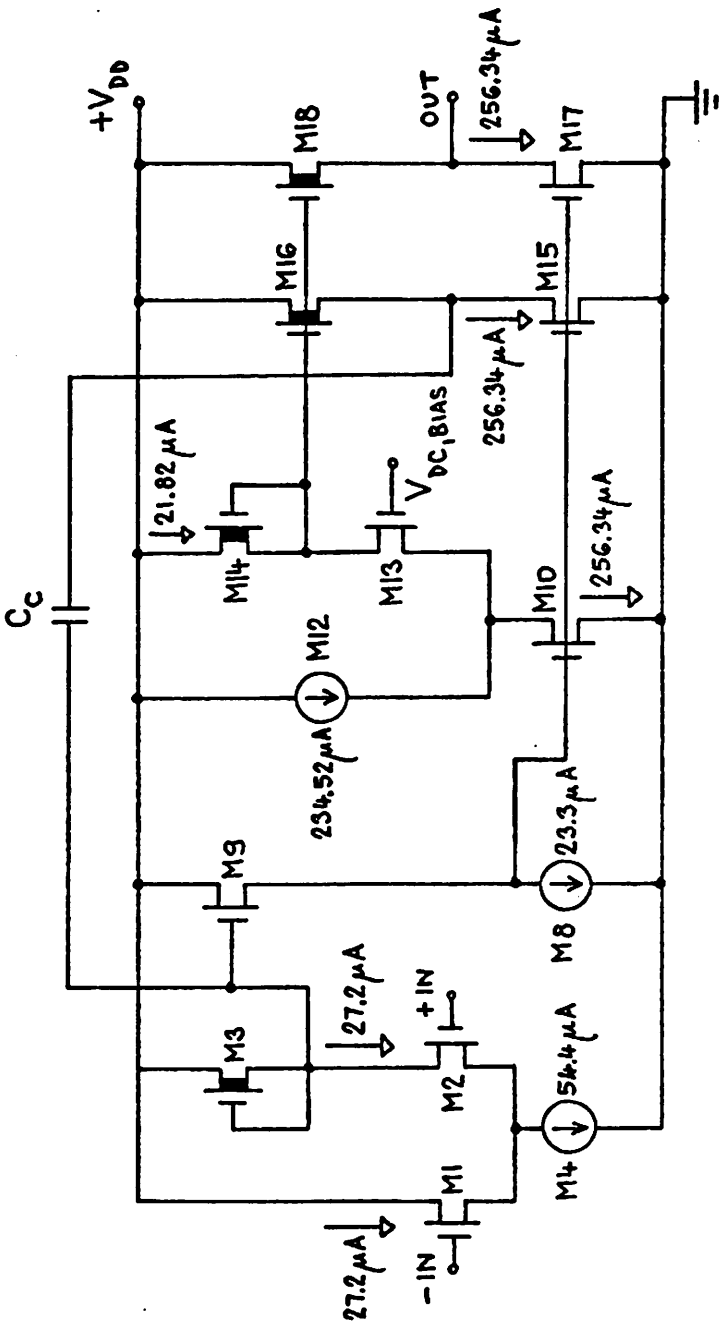


Figure 6.5: Bias currents in the NMOS operational amplifier

From measurements: $\lambda'_{ENH} = 7.06 \times 10^{-3}$ mil/V.

The threshold voltage equations for the depletion mode MOSFET can be found for best-fit from Fig. 6.3c as

$$V_T = -2.5V + 0.38 \sqrt{V} \sqrt{0.9V - V_{BS}} \tag{6.4}$$

The parameter λ'_{DEPL} was 4.545×10^{-3} mil/V.

The normalized conduction factor was in both cases $k' = 20\ \mu A/V^2$.

When calculating the quiescent current and voltages in the bias string M5, M6, M7 (Fig. 5.11a) there was considerable discrepancy between measured and calculated values. However, when Eq. (6.4) was changed to

$$V_T = -2.9V + 0.38 \sqrt{V} \sqrt{0.9V - V_{BS}} \tag{6.5}$$

the bias current calculation gave $I_D = 23.3\ \mu A$ and the quiescent voltages were $V_A = 2.8$ V and $V_B = 6.6$ V. The measured quiescent voltages were $V_A = 3$ V and $V_B = 6.7$ V.

The values of all quiescent currents in the operational amplifier are given in Fig. 6.5. The power supply current is then 0.87 mA and the power consumption 13 mW.

Calculations for the differential pair yield the power supply current of 0.334 mA and the power consumption of 5 mW.

The voltage gains of the individual stages can be calculated similarly to section 5.3.4. The values for the measured MOSFET characteristics and quiescent currents are $A_{v1} = 44.43$, $A_{v2} = 0.94$, $A_{v3} = 156.7$, $A_{v4} = 1.5$ and $A_{v5} = 0.93$. The total open-loop gain of the operational amplifier is then $A_{vtot} = 6143$. The gain of the differential pair is $A_{vtot} = 41.7$.

The common-mode rejection ratio can be derived as CMRR = 49.15 dB the output impedance as $Z_{out} = 2.93\ k\Omega$ and the slew rate as SR = 4.53 V/μsec.

TABLE IV

FILTER PERFORMANCE

		Filter I	Filter II
Clock rate f_c		102.4 kHz	16 kHz
Calculated:	center frequency f_0	3.75 kHz	264 Hz
	selectivity Q	73.14	0.99
Measured:	center frequency mean	3.715 kHz	287 Hz
	center frequency standard deviation	13 Hz	1 Hz
	selectivity mean	71.2	0.97
	selectivity standard deviation	2.2	0.004
	output wideband noise (rms)	0.85 mV	160 μV

The 3 dB frequency was determined from Eq. (5.97) being f_{3dB} = 424 Hz and the unity-gain frequency was GBW = 2.6 MHz for the operational amplifier. Similar calculations performed for the differential pair gave f_{3dB} = 97.7 kHz and GBW = 4.1 MHz.

There is obviously a need for good modeling of MOSFETs with shifted threshold voltage, especially as far as the effect of ion implantation on body effect is concerned. This would help to optimize the proper phase compensation and predict the transient behavior of the amplifier.

6.6. Filter Performance

In Table IV is a summary of the calculated and measured performance parameters obtained from five filters from three different wafers. The agreement is excellent between theory and measurements. The high Q filter has a sensitivity of 10 for the value of Q, thus the measured 3% variation in Q corresponds to a 0.3% accuracy of the capactiance ratios. Filter II has a sensitivity of 1 to most of the ratios which results in the 0.3% variation of the Q and center frequency of that filter.

In filter II there was an 8% discrepancy between the calculated and the measured mean value of the center frequency f_0. This error was due to an error in layout in which long metal leads connected the switches and the top plates of the smallest capacitors (which were approximately 1 pf). This increased the value of these switched capacitors by about 8%. This error could have been reduced during layout in three ways: reduce the length of the metal leads; increase the size of the capacitors; and take the effect of this parasitic into account since it will be a constant for a given layout of the metal leads. More care in layout was taken in filter I with result that even though the sensitivity was 10 times

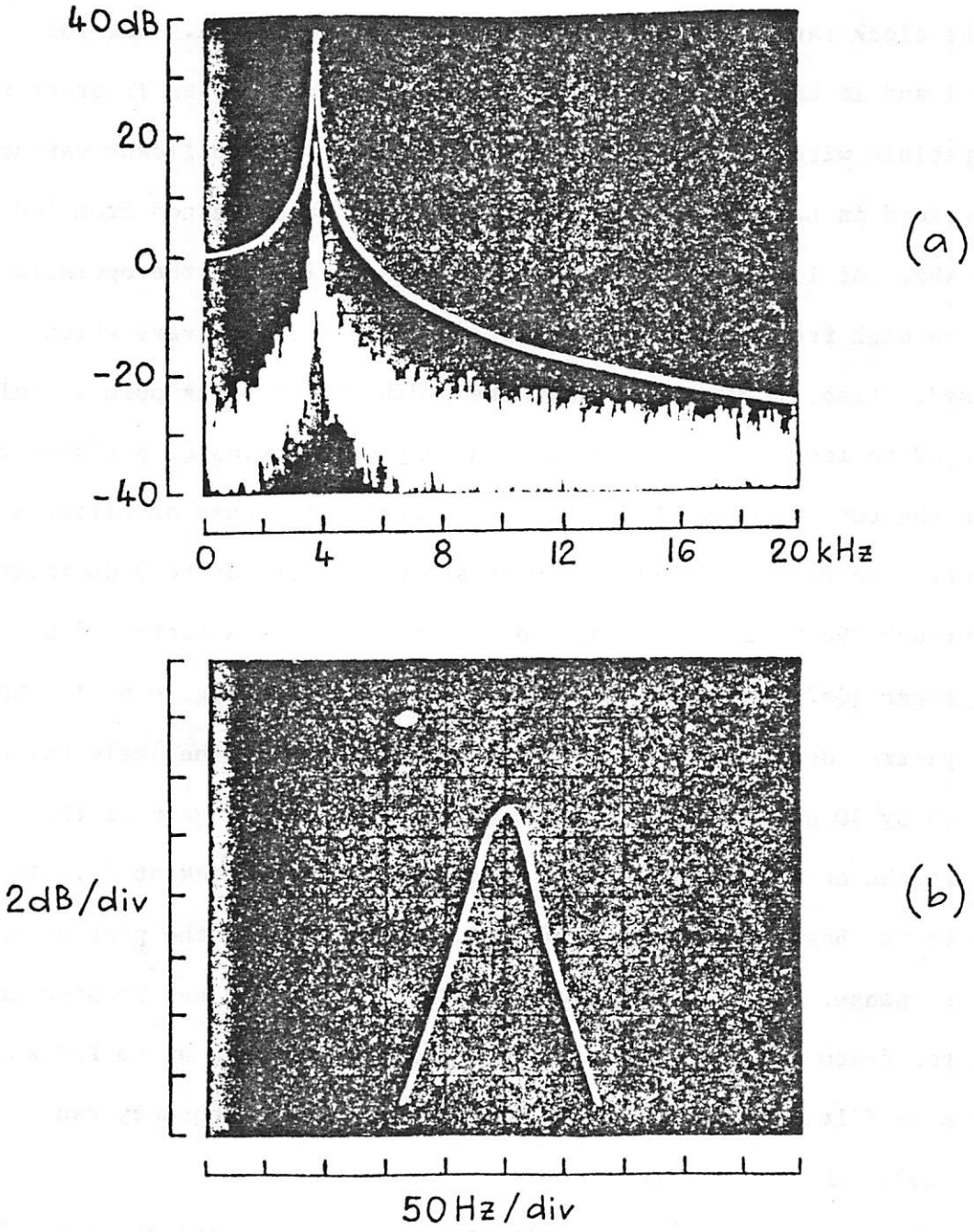


Figure 6.6: (a) Frequency response and noise spectral density (amplified by 30 dB) of filter I, operated at a clock rate of 102.4 kHz
(b) Detail of the peak of the response in a

higher for this filter the response was closer to the design goals.

The clock rates which were used to take data were 102.4 kHz for filter I and 16 kHz for filter II. These rates were chosen in order to be compatible with a systems application, however insignificant variations were noticed in the performance for clock rates which ranged from 100 Hz to 500 kHz. At low frequencies leakage currents limited the operation while the high frequency end was limited by the clock drivers which were used. Also, it was found that the width of the clock pulses could be reduced to less than 0.2 μsec without any degradation of performance.

In the top trace in Fig. 6.6a the frequency response of filter I is shown. The reference level of 0 dB at DC corresponds to 0 dB insertion loss through the filter. The peak of the response is a factor of Q times larger (Q=73.14 yields 37.3 dB). Also shown in Fig. 6.6a is the noise spectral density with a 30 Hz bandwidth in which the scale has been increased by 30 dB. As expected because of the 37.3 dB gain of the filter at the center frequency the noise also shows a peak at f_0. In Fig. 6.6b is shown an expanded scale of the region near the peak of the filter response. The very narrow 3 dB width of ≈ 50 Hz can be seen around the center frequency of 3715 Hz. The frequency response up to 200 kHz of the same filter is shown in Fig. 6.6c. The clock frequency can be seen at 102.4 kHz as expected.

In the upper curve in Fig. 6.7a is shown the response of filter II and in Fig. 6.7b is the response on an expanded scale at low frequencies. Also shown in Fig. 6.7a is the noise of the filter after an amplification of 30 dB (bandwidth 30 Hz). Since this filter has very little gain in the passband the noise is not amplified, however the 1/f noise of the input MOSFETs of the amplifier can be seen.

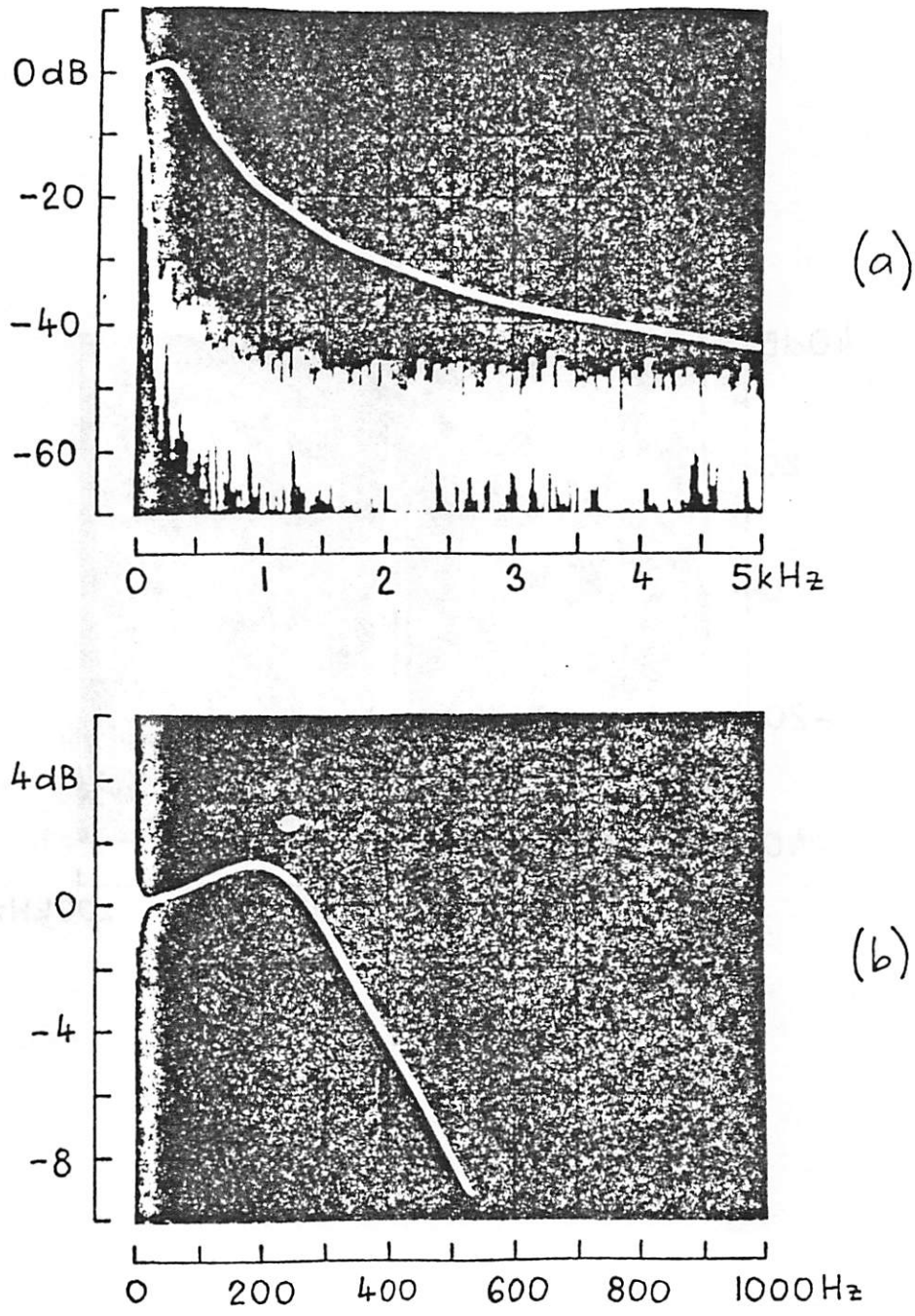
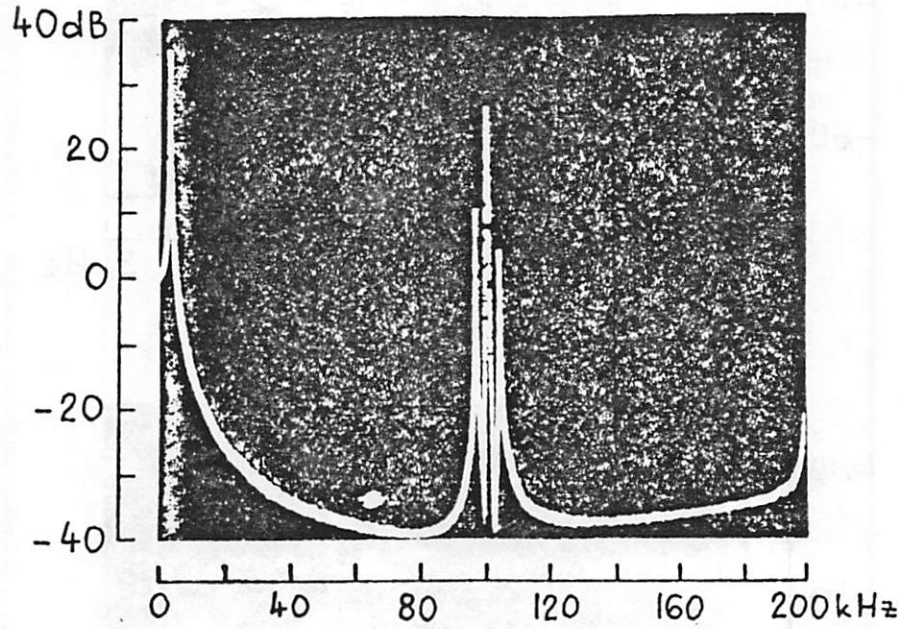


Figure 6.7: (a) Frequency response and noise spectral density (amplified by 30 dB) of filter II, operated at a clock rate of 16 kHz

(b) Detail of the response in a at low frequencies



(c)

Figure 6.6.c: Frequency response of filter I (f_c = 102.4 kHz) up to 200 kHz

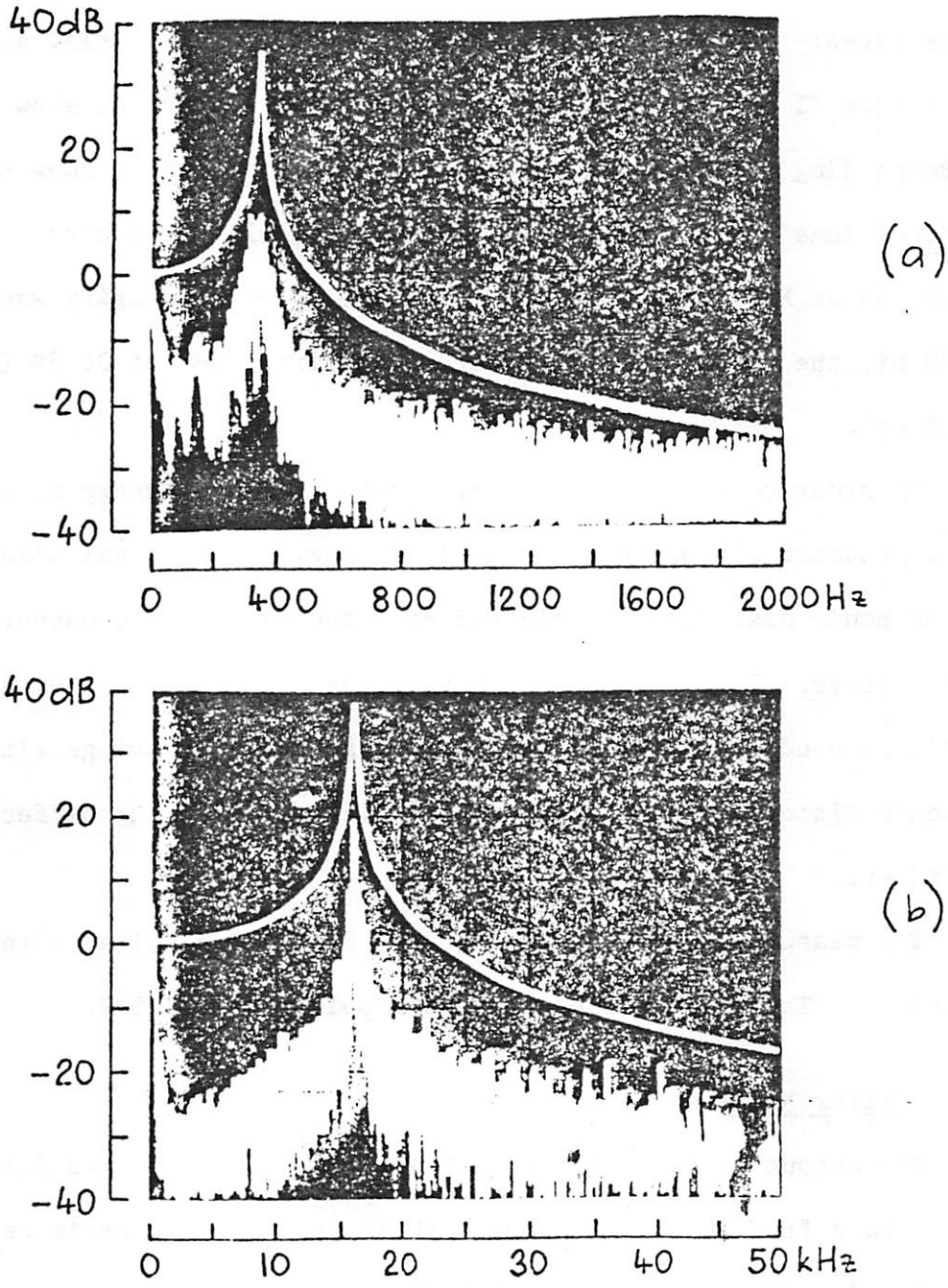


Figure 6.8: (a) Frequency response and noise spectral density (amplified by 20 dB) of filter I (f_C= 10 kHz)
(b) Frequency response and noise spectral density (amplified by 30 dB) of filter I (f_C= 500 kHz)

The next three photographs show the two filters operated at different clock rates: filter I in Fig. 6.8a (f_c=10 kHz) and in Fig. 6.8b (f_c=500 kHz) and filter II in Fig. 6.8c (f_c=160 kHz). The top traces show the corresponding frequency responses and the bottom traces show the noise spectral densities with a 30 Hz bandwidth in all three cases. With the exception of Fig. 6.8a in which the noise spectral density was amplified by 20 dB, the noise is shown after an amplification of 30 dB (Fig. 6.8b and 6.8c).

In order to define the dynamic range it is necessary to determine the dependence of the total harmonic distortion on signal size. In Fig. 6.9 the harmonic distortion is plotted as a function of the output signal for both filters. It is clearly seen that the high gain of the operational amplifier used in filter I results in larger output swings with decreased harmonic distortion in comparison to filter II with the differential pair amplifier.

The measured clock feedthrough was 800 mV for filter I and 200 mV for filter II. The amplitude of the clock pulses was 17.5 V.

6.7. Filter Noise

The output wideband noise (see Table IV) was measured integrated over a band from 20 Hz to f_c for each filter. Let us estimate the contribution of individual noise sources.

Figure 6.10 shows the version 3 filter including the equivalent input noise voltage source of the amplifier. The output voltage can be calculated as

$$V_{out} = \frac{k\alpha_1\alpha_2 V_{in} + \{[(1+\alpha_2)z-1][z-k]-\rho\alpha_2 z\}\sqrt{v^2_{eq,tot}}}{z^2-z(k+1)+k(1+\alpha_1\alpha_2)} \qquad (6.6)$$

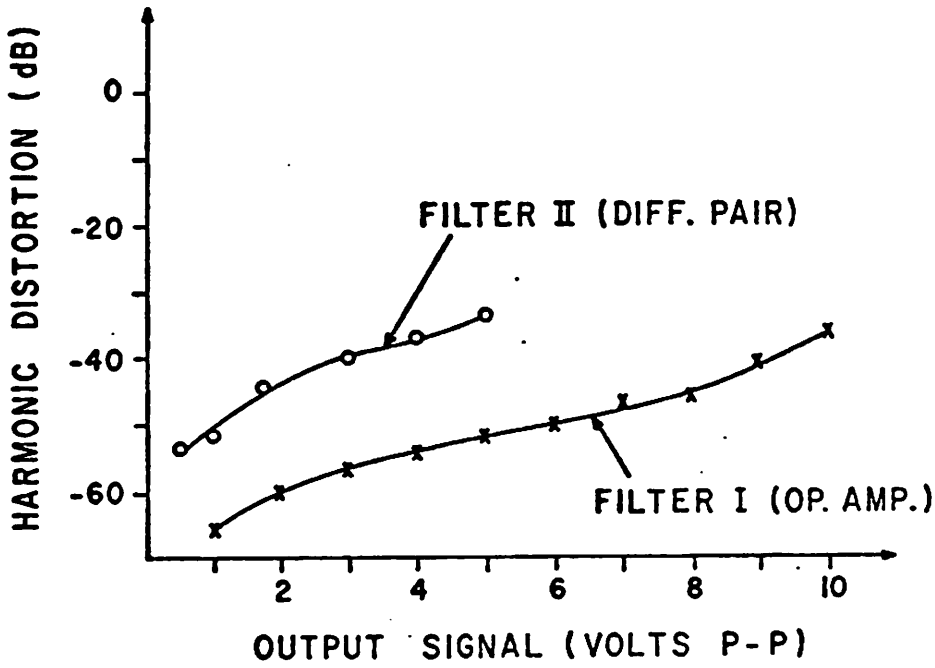
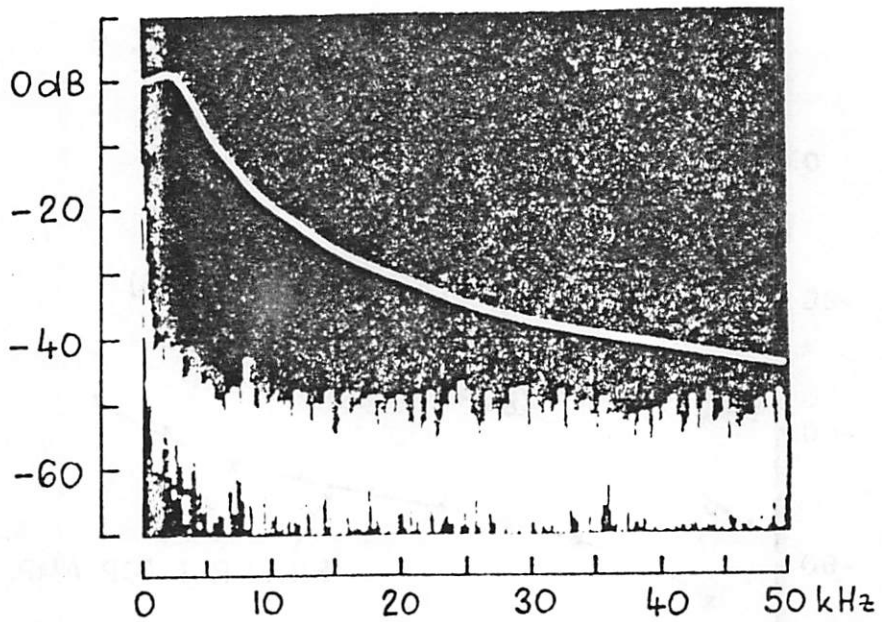


Figure 6.9: The harmonic distortion of both filters as a function of the output signal (signal frequency is 3.715 kHz for filter I and 100 Hz for filter II)



(c)

Figure 6.8.c: Frequency response and noise spectral density (amplified by 30 dB) of filter I1 (f_c= 160 kHz)

where

$$k = \frac{1}{(1+\alpha_1)(1+A\alpha_2)} \tag{6.7}$$

$$\rho = A\alpha_2(1+\alpha_1) \tag{6.8}$$

Considering only the equivalent input noise voltage source and a high clock rate, the output voltage is

$$V_{out} \approx (1+\alpha_2)\sqrt{\overline{v^2_{eq,tot}}} \tag{6.9}$$

for frequencies $f_0 < f < f_c$. The magnitude of the output voltage at the center frequency $\theta = 2\pi f_0/f_c$ is given by

$$V_{out}(z=e^{j\theta}) = \frac{Q}{\theta \sin\theta}\Big|(1+\alpha_2)(\cos 2\theta + j \sin 2\theta) + k - [1+(1+\alpha_2)k+\rho\alpha_2](\cos\theta + j\sin\theta)\Big|\sqrt{\overline{v^2_{eq,tot}}} \tag{6.10}$$

where $\overline{v^2_{eq,tot}}$ is the equivalent input noise of the amplifier at the frequency f_0.

The Eq. (6.6) represents a high-pass transfer function as far as the noise source $\overline{v^2_{eq,tot}}$ is concerned (Fig. 6.11). The noise at the output due to the amplifier is

$$\sqrt{\overline{v_1^2}} = \sqrt{\overline{v^2_{eq,th}}}\sqrt{\frac{f_{Beq}}{f_0}}\sqrt{\frac{f_0}{Q}}\left|V_{out}/\sqrt{\overline{v^2_{eq,tot}}}\right|_{f=f_0} \tag{6.11}$$

integrated over the 3 dB bandwidth $\Delta f = f_0/Q$ and multiplied by the gain at f_0 (see Eq. (6.10)). The equivalent input noise of the amplifier was given by Eq. (5.22).

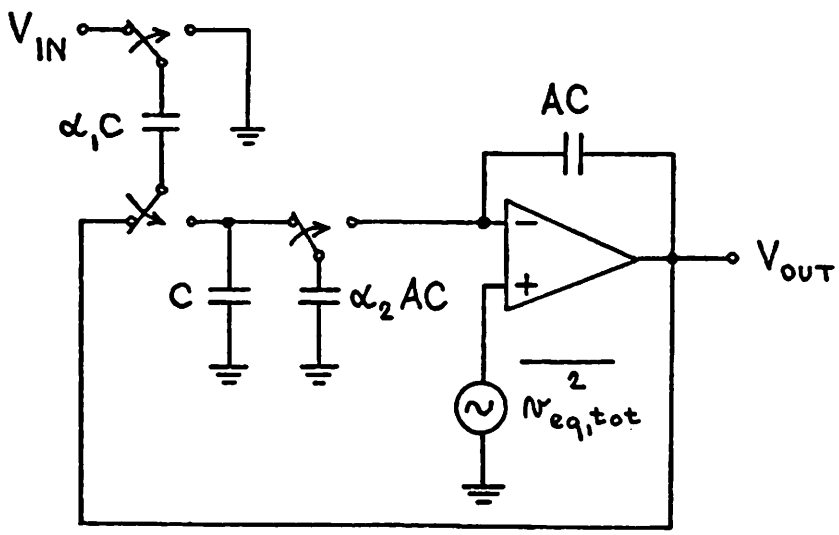


Figure 6.10: The version 3 filter including equivalent input noise voltage of the amplifier

Using values given in sections 6.4 and 6.6 the calculation based on Eq. (6.11) yielded $\sqrt{v_1^2}$ = 568 μV for filter I. When all the noise of the amplifier was multiplied by the transfer function and integrated up to the clock frequency f_c and the noise due to MOSFET switches $(kT/C)^{1/2}$ was added, the total output wideband noise was 578 μV. The photographs of the noise spectral density at the output of filter I shown in section 6.6 clearly show peaking of noise at f_0 which is consistent with our calculation. This noise is obviously dominant for filter I.

The measured output wideband noise was 850 μV for filter I. The discrepancy is due to calculation approximations, measurement inaccuracies, ground noise and noise pickup.

The noise calculations carried out in similar manner for filter II show that the MOSFET switches contribute mostly to the total output wideband noise for this filter. The calculated noise due to switches was 91.2 μV while the total output wideband noise up to f_c including the noise due to the amplifier was 96.2 μV. Again there was a discrepancy between the calculated and the measured noise, which was 160 μV for filter II. The photographs in section 6.6 show the noise spectral density at the output of filter II: however, it is necessary to realize that these pictures contain noise of the spectrum analyzer as well, particularly the 1/f component.

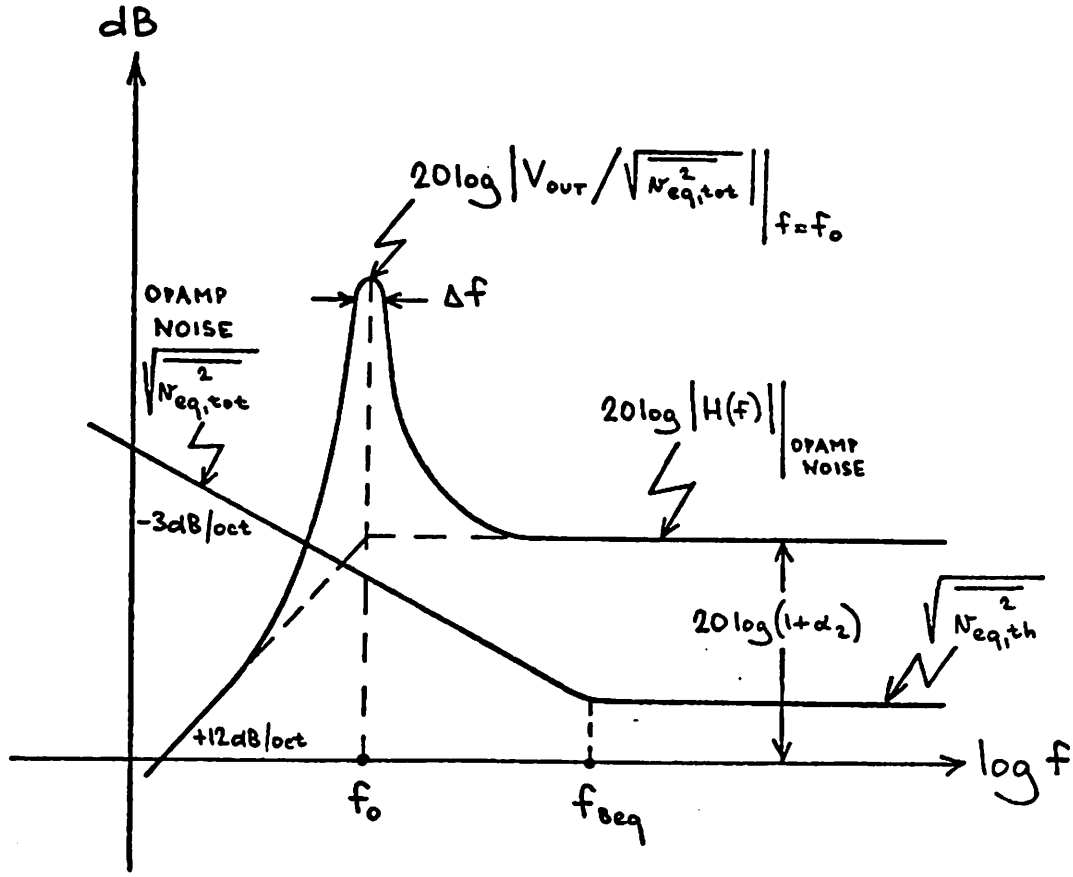


Figure 6.11: The transfer function of the version 3 filter for the amplifier noise as a function of frequency

APPENDIX

N-CHANNEL MOS ALUMINUM GATE PROCESS

Parts of this process, i.e. steps 1 to 20 and 31 to 36, have evolved in their present form through previous effort [51]. Two ion implants and a passivation (steps 21 to 30) have been added for this particular fabrication sequence.

Fabrication sequence

1. Initial wafer cleaning:
   a) DI:HF (9:1), room temperature, dip, 2 min
   b) TCE, 60°C, 10 min
   c) Acetone, room temperature, 2 min
   d) DI, rinse
   e) RCA1 cleaning:
      $NH_4OH:H_2O_2$:DI, (1:1:5), 75°C, 15 min
      DI, rinse
   f) RCA2 cleaning:
      HCL:H_2O_2:DI, (1:1:6), 75°C, 15 min
      DI, rinse
      N_2, blow dry
2. Initial oxidation: Initial oxidation furnace, growth of 0.92 μ wet oxide.
   a) Wet O_2, 0.5 ℓ/min, 1150°C, 90 min
   b) Dry N_2, 0.65 ℓ/min, 850°C, 10 min
3. Photoresist step (p+ isolation diffusion mask)
   a) Apply Kodak 747 (Micro neg) photoresist; 50 c.s.; 5000 rpm, 20 sec, single coat

CHAPTER 7

CONCLUSIONS

Three different versions of a new analog sampled data filtering approach based on state variable design techniques have been discussed. An important advantage of this approach is that monolithic high Q filters can be implemented using single channel MOS technology. Two lowpass second-order filters have been designed and fabricated and the experimental results confirm the theoretical considerations presented.

The switched integrators which were used to implement these filters have application in many other organizations. A particularly interesting one for implementing more complex frequency response functions is the use of leapfrog or active-ladder synthesis techniques [52]. The two pole filters described in this work are actually a limiting form of the leapfrog method which can be used to synthesize any number of poles and zeros with very low sensitivity.

c) N_2, 1.25 ℓ/min, 10 min (dry), 900°C

12. Etch phosphorous glass, HF:DI (1:3), dip, 1.5 min

13. RCA1 & RCA2 cleaning (see steps 1e, 1f)

14. Oxide growth over n+: n-type drive-in furnace

a) Wet O_2, 0.5 ℓ/min, 1100°C, 34 min

b) Dry N_2, 1.0 ℓ/min, 900°C, 10 min

15. Photoresist step (gate oxide mask)

Same as step 9, except (i), for which time is 6.5 min

16. RCA1 & RCA2 cleaning (see steps 1e, 1f)

17. Gate oxide growth: n-type drive-in furnace, wafer horizontal on boat.

a) Dry O_2, 1.5 ℓ/min, 1000°C, 110 min total time

b) N_2, 1.0 ℓ/min, 900°, 10 min

18. Implant: Boron, dose $7.8 \times 10^{11}/cm^2$, energy 50 keV

19. RCA1 cleaning (see step 1e)

20. Heat under infrared lamp, 10 min

21. Photoresist step (depletion load mask)

Same as steps 3a - 3h

22. Implant: Phosphorous, dose $2.1 \times 10^{12}/cm^2$, energy 150 keV

23. Photoresist strip

Same as step 3j

24. Oxide etch: etch only back side of the wafer using Q-tip, NH_4F:HF (5:1), room temperature

25. RCA1 & RCA2 cleaning (see steps 1e, 1f)

26. Passivation: n-type predeposition furnace

a) O_2, 0.1 ℓ/min
N_2, 1.25 ℓ/min
} 5 min (dry), 1000°C

b) Air dry, 15 min

c) Prebake, 90°C, 30 min

d) Expose mask, 3.5 sec

e) Spray develop, 30 sec

f) Spray rinse, 20 sec

g) Dry N_2

h) Postbake, 125°C, 30 min

i) Oxide etch, NH_4F:HF (5:1), room temperature, 9.5 min

j) Photoresist strip, RT-1, room temperature, 5 min

4. RCA1 & RCA2 cleaning (see steps 1e, 1f)

5. p+ predeposition: p-type predeposition furnace 950°C

   B_2H_6, 0.26 ℓ/min
   O_2, 0.013 ℓ/min
   N_2, 1.3 ℓ/min
   } Simultaneous flow, 15 min

6. Etch boron glass, HF:DI (1:3), dip, 1.5 min

7. RCA1 & RCA2 cleaning (see steps 1e, 1f)

8. Oxide growth over p+: p-type drive-in furnace, 1150°C

   a) Wet O_2, 0.5 ℓ/min, 16 min

   b) Dry N_2, 1.0 ℓ/min, 10 min

9. Photoresist step (n+ diffusion mask)

   Same as step 3, except (i), where etch for 10 min

10. RCA1 & RCA2 cleaning (see steps 1e, 1f)

11. n+ predeposition: n-type predeposition furnace, 1100°C, $POCℓ_3$, 0°C

    a) O_2, 0.1 ℓ/min
       N_2, 1.25 ℓ/min
       } 5 min (dry), 1100°C

    b) O_2, 0.1 ℓ/min
       N_2, 1.25 ℓ/min
       $POCℓ_3$, 0.096 ℓ/min
       } 20 min (dry), 1100°C

k) DI, rinse

ℓ) N_2, blow dry

33. Heat treatment: Sintering over, 450°C

N_2:H_2 (9:1), 1 ℓ/min, 5 min

b) O_2, 0.1 ℓ/min
   N_2, 1.25 ℓ/min
   POC_3, 0.096 ℓ/min
   } 2 min (dry), 1000°C

c) N_2, 1.25 ℓ/min, 10 min (dry), 900°C

27. Dip, H_2SO_4:H_2O_2 (4:1), 90°C (self-heating), 5 min

28. Photoresist step (contact mask)

Same as step 3, except (d), where mask is exposed 2.5 sec, then shifted one row, and again exposed 2.5 sec. This eliminates pinholes. Also, in (i) 1 min etch.

29. RCA1 & RCA2 cleaning (see steps 1e, 1f)

30. Dry under infrared lamp, 10 min

31. Evaporate aluminum, 0.3 μ to 0.4 μ thickness

32. Photoresist step (metallization mask)

a) Heat under infrared lamp, 10 min

b) Apply AZ1350J photoresist, 8000 rpm, 30 sec, single coat

c) Prebake, 90°C, 45 min

d) Expose mask, 12.5 sec

e) Develop with MF312 or AZ1350J developer, developer: DI, (1:1), 45 sec

f) DI, rinse

g) Postbake, 90°C, 30 min

h) Etch aluminum with aluminum etchant type A, 45°-50°C with ultrasonic agitation, 30 sec - 45 sec

i) DI, rinse

j) Strip photoresist with 1112 photoresist stripper, 50°-60°C, 2-3 min

[11] E. I. Jury, Theory and Application of the Z-Transform Method, John Wiley & Sons, Inc., New York, 1964.

[12] A. V. Oppenheim and R. W. Schafer, Digital Signal Processing, Prentice-Hall, Inc., 1975.

[13] R. W. Brodersen, "Introduction to Charge Transfer Device Discrete Time Processing," Wescon Professional Program, Los Angeles, September 1976.

[14] C. H. Séquin and M. F. Tompsett, Charge Transfer Devices, Academic Press, Inc., New York, 1975.

[15] D. L. Fried, "Analog Sampled Data Filter," IEEE J. Solid State Circuits, vol. SC-7, pp. 302-303, August 1972.

[16] J. L. McCreary and P. R. Gray, "All-MOS Charge- Redistribution A-D Conversion Techniques, Part I," IEEE J. Solid State Circuits, vol. SC-10, pp. 371-379, December 1975.

[17] W. J. Kerwin, et al., "State Variable Synthesis for Insensitive I. C. Transfer Functions," IEEE J. Solid State Circuits, vol. SC-2, pp. 87-92, September 1967.

[18] G. E. Tobey, J. G. Graeme and L. P. Huelsman, Operational Amplifiers - Design and Applications, McGraw-Hill Book Co., 1971.

[19] R. C. Agarwal and C. S. Burrus, "New Recursive Filter Structures Having Very Low Sensitivity and Roundoff Noise," IEEE J. Circuits and Systems, vol. CAS-22, pp. 921-927, December 1975.

[20] G. Daryanani, Principles of Active Network Synthesis and Design, John Wiley and Sons, 1976.

[21] P. W. Fry, "A MOST Integrated Differential Amplifier," IEEE J. Solid State Circuits, vol. SC-4, pp. 166-168, June 1969.

REFERENCES

[1] D. D. Buss, et al., "Transversal Filtering Using CTD's," IEEE J. Solid State Circuits, vol. SC-8, pp. 138-146, April 1973.

[2] R. W. Brodersen, C. R. Hewes and D. D. Buss, "A 500-Stage CCD Transversal Filter for Spectral Analysis," IEEE J. Solid State Circuits, vol. SC-11, pp. 75-84, February 1976.

[3] R. D. Baertsch, et al., "The Design and Operation of Practical Charge-Transfer Tranversal Filters," IEEE Trans. Electron Devices, vol. ED-23, pp. 133-141, February 1976.

[4] I. A. Young, P. R. Gray and D. A. Hodges, "Analog NMOS Sampled Data Recursive Filters," Proc. Int. Solid State Circuits Conf. (Philadelphia), pp. 156-157, February 1977.

[5] B. J. Hosticka, R. W. Brodersen and P. R. Gray, "MOS Sampled Data Recursive Filters Using State Variable Techniques," Proc. Int. Symp. on Circuits and Systems (Phoenix, Arizona), pp. 525-529, April 1977.

[6] B. J. Hosticka, R. W. Brodersen and P. R. Gray, "MOS Sampled Data Recursive Filters Using Switched Capacitor Integrators," IEEE J. Solid State Circuits, vol. SC-12, December 1977.

[7] Private communication: A. Fettweiss.

[8] A. B. Grebene, Analog Integrated Circuit Design, Van Nostrand Reinhold Co., 1972.

[9] S. D. Stearns, Digital Signal Analysis, Hayden Book Co., 1975.

[10] L. R. Rabiner, B. Gold, Theory and Application of Digital Signal Processing, Prentice-Hall, Inc., 1975.

[31] D. Frohman-Bentchkowski and A. S. Grove, "Conductance of MOS Transistors in Saturation," IEEE Trans. Electron Devices, vol. ED-16, pp. 108-113, January 1969.

[32] Y. A. El-Mansy and A. R. Boothroyd, "A Simple Two-Dimensional Model for IGFET Operation in the Saturation Region," Trans. Electron Devices, vol. ED-24, pp. 254-261, March 1977.

[33] H. Schichman and D. A. Hodges, "Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuits," IEEE J. Solid State Circuits, vol. SC-3, pp. 285-289, September 1968.

[34] W. M. Penney, et al., MOS Integrated Circuits, Van Nostrand Reinhold Co., 1972.

[35] J. N. Chalfan and J. C. Looney, "Linear Metal-Oxide-Semiconductor Integrated Circuits," Solid State Technology, pp. 31-39, May 1969.

[36] W. C. Black, R. H. McCharles and D. A. Hodges, "CMOS Process for High-Performance Analog LSI," Techn. Digest Int. Electron Devices Meeting (Washington, D. C.), pp. 331-334, December 1976.

[37] J. E. Solomon, "The Monolithic Operational Amplifier: A Tutorial Study," IEEE J. Solid State Circuits, vol. SC-9, pp. 313-337, December 1974.

[38] B. J. Hosticka, "N-MOS Operational Amplifier Study," Memorandum No. ERL-M578, University of California, Berkeley, 1976.

[39] D. A. Hodges, P. R. Gray and R. W. Brodersen, "Potential of MOS Technologies for Analog Integrated Circuits," to be published.

[40] W. R. Ong, "Noise Characterization of MOSFETs," M. S. Plan II Report, University of California, Berkeley, 1976.

[41] F. M. Klaassen, "Characterization of Low 1/f Noise in MOS Transistors," IEEE Trans. Electron Devices, vol. ED-18, pp. 887-891, October 1971.

[22] A. Boorward, E. Herrmann and S. T. Hsu, "Low-Noise Integrated Silicon-Gate FET Amplifier," IEEE J. Solid-State Circuits, vol. SC-10, pp. 542-544, December 1975.

[23] Y. P. Tsividis and P. R. Gray, "An Integrated NMOS Operational Amplifier with Internal Compensation," IEEE J. Solid State Circuits, vol. SC-11, pp. 748-753, December 1976.

[24] Y. P. Tsividis, P. R. Gray, D. A. Hodges and J. Chacko, "A Segmented μ-255 Law PCM Voice Encoder Utilizing NMOS Technology," IEEE J. Solid-State Circuits, vol. SC-11, pp. 740-747, December 1976.

[25] R. E. Suárez, P. R. Gray and D. A. Hodges, "All-MOS Charge Redistribution A-D Conversion Techniques, Part II," IEEE J. Solid State Circuits, vol. SC-10, pp. 379-385, December 1975.

[26] F. H. Musa and R. C. Huntington, "A CMOS Monolithic 3-1/2-Digit A/D converter," Proc. Int. Solid State Circuits Conf. (Philadelphia), pp. 144-145, February 1976.

[27] A. G. E. Dingwall and B. D. Rosenthal, "Low-Power Monolithic COS/MOS Dual-Slope 11-Bit A/D Converter," Proc. Int. Solid State Circuits Conf. (Philadelphia), pp. 146-147, February 1976.

[28] G. Smaragdoiu, K. Fukahori and P. R. Gray, "An All-MOS A/D Converter Using a Constant Slope Approach," IEEE J. Solid State Circuits, vol. SC-11, pp. 408-410, June 1976.

[29] J. F. Albarran and D. A. Hodges, "A Charge Transfer Multiplying D/A Converter," Proc. Int. Solid State Circuits Conf. (Philadelphia), pp. 202-203, February 1976.

[30] A. S. Grove, Physics and Technology of Semiconductor Devices, John Wiley and Sons, Inc., New York, 1967.

[54] M. V. Hoover, "An Introduction to the Characteristics and Applications of COS/MOS Transistors in Linear Service," IEEE Circuits and Systems, vol. 10, no. 1, pp. 2-11, February 1976.

[42] C. D. Motchenbacher and F. C. Fitchen, Low-Noise Electronic Design, John Wiley and Sons, 1973.

[43] R. D. Thornton, et al., Multistage Transistor Circuits, John Wiley and Sons, 1965.

[44] K. A. Pickar, "Ion Implantation in Silicon--Physics, Processing, and Microelectronic Devices," Applied Solid State Science, vol. 5, pp. 151-249, 1975.

[45] R. W. Brodersen and S. P. Emmons, "Noise in Buried Channel Charge-Coupled Devices," IEEE Trans. Electron Devices, vol. ED-23, pp. 215-223, February 1976.

[46] D. A. Hodges, private communication.

[47] V. L. Rideout, F. H. Gaensslen and A. LeBlanc, "Device Design Considerations for Ion Implanted n-Channel MOSFETs," IBM J. Res. Develop., pp. 50-59, January 1975.

[48] W. C. Black, private communication.

[49] C. Ott, "A Low Noise Output Stage for a CCD Transversal Filter," M. S. Plan II Report, University of California, Berkeley, 1976

[50] E. Cohen, "Program Reference for SPICE 2," Memorandum No. ERL-M592, University of California, Berkeley, 1976.

[51] J. L. McCreary, "Successive Approximation Analog-to-Digital Conversion Techniques in MOS Integrated Circuits," Ph.D. Thesis, University of California, Berkeley, 1975.

[52] F. E. J. Girling and E. F. Good, "The Leapfrog or Active-Ladder Synthesis," Wireless World, pp. 341-345, July 1970.

[53] Y. P. Tsividis, "Nonuniform Pulse Code Modulation Encoding Using Integrated Circuit Techniques," Ph.D. Thesis, University of California, Berkeley, 1976.