MOS SWITCHED CAPACITOR LADDER FILTERS

by

D.J. Allstot, Ro.W. Brodersen and P.R. Gray

Memorandum No. UCB/ERL M78/49

21 April 1978

MOS SWITCHED CAPACITOR LADDER FILTERS

by

D.J. Allstot, R.W. Brodersen, and P.R. Gray

Memorandum No. UCB/ERL M78/49

21 April 1978

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

MOS SWITCHED CAPACITOR LADDER FILTERS

David J. Allstot, Robert W. Brodersen and Paul R. Gray
Department of Electrical Engineering and Computer Sciences
and the Electronics Research Laboratory
University of California, Berkeley, California 94720

Abstract

A new technique for designing precision fully-integrated high-order filters using standard MOS technology is described. Switched capacitor integrators have been used to realize long time constants in small areas, and by interconnecting these integrators in a "leapfrog" configuration, monolithic high-order filters have been implemented with transfer functions that are very insensitive to component variations. Experimental results are presented for an NMOS fifth-order Chebyshev lowpass ladder filter with 0.1 dB passband ripple, a cutoff frequency of 3.4 kHz when clocked at 128 kHz, and a dynamic range of 83 dB. An efficient method for implementing transmission zeros is also presented, along with a complete design example, and additional experimental results for a third-order elliptic lowpass ladder filter which achieved 90 dB dynamic range, with a total power dissipation of 18 mW in a die area of 4400 mil^2.

Research sponsored by the Joint Services Electronics Program Contract F44620-76-C-0100. This paper was presented in part at the Int. Solid-State Circuits Conference (San Francisco), Feb. 1978.

I. Introduction

Precision high-order filters are widely used in various types of electronic equipment such as telecommunications and other voice-band systems. Monolithic implementation of these low frequency filters requires the realization of long time constants in small silicon areas, and the realization of transfer functions that are insensitive to parameter variations. In addition, it is desirable to obtain very precise responses without external trimming operations. Conventional active filters implemented with thin-film or hybrid technologies do not meet these requirements, and therefore are not suitable for many applications [1].

Recently, these objectives have been realized in a monolithic implementation using a compatible Bipolar/JFET technology [2]. Although excellent results have been obtained, this approach requires relatively large chip areas for low frequency applications, and the required bipolar process is not directly compatible with dense digital logic which is needed for many LSI system applications.

Another promising monolithic filtering approach uses charge transfer devices (CTD's) to implement sampled-data transversal filters [3]. In general, this approach has two main disadvantages: (1) The large insertion loss (which is typically 20 dB) limits the available dynamic range [4], and (2) the low sampling rates relative to the passband frequencies complicate the design of the continuous-time anti-alias

prefilter [5]. If higher clock frequencies are used relative to the passband frequencies in order to reduce the prefilter requirements, more CTD stages are required which further reduces the dynamic range and increases the silicon area requirements.

In the 1960's and early 1970's, filtering by using switches and capacitors was investigated theoretically [6]-[7]. At that time, a suitable integrated circuit technology did not exist which could efficiently realize these filters. Recent work using analog sampled-data techniques has demonstrated the viability of MOS technology for implementing second-order filters. One approach implements an MOS sampled-data equivalent of a direct-form second-order digital filter section [8]. This approach has a relatively high sensitivity of the transfer function to component variations with the additional disadvantage that the sensitivity increases as the ratio of the sampling rate to passband frequencies increases. Hence, there is a tradeoff between the sensitivity properties of the direct-form sampled-data filter, and the requirements for the continuous-time antialiasing prefilter. More recent approaches implement sampled-data versions of second-order or biquad active filters using switched capacitors to simulate resistors [9]-[11]. A major advantage of this approach is that the sensitivity of the response of these filters decreases with increasing clock frequency, in contrast to the direct-form implementation. Unfortunately, high-order

filters realized by cascading these second-order sections can be too sensitive to component variations to meet high-precision filtering requirements.

In this paper, "leapfrog" or "active ladder" analog sampled-data recursive filters are described which have been used to implement high-order filters with transfer functions that have very low sensitivity to component variations as compared to cascade realizations. When implemented in standard MOS technology, these filters achieve a very precise response with wide dynamic range while requiring small chip area, low power dissipation, and relatively low performance operational amplifiers [12]. The low sensitivity of these ladder filters is, to a first-order, independent of the sampling frequency. Thus, the anti-aliasing prefilter requirements are greatly reduced (compared to the CTD and direct-form approaches) by operating the filters at clock frequencies which are many times greater than the passband frequencies.

II. Switched Capacitor Integrators

Conventional filtering approaches used to implement audio and other low frequency filters would require RC differential integrators, as in Fig. 1(a), with long time constants [13]. If the time constants were realized monolithically as RC products, large amounts of chip area would be required. Another disadvantage of this approach is that in

order to insure reproducibility, the absolute values of both R and C must be tightly controlled, which is extremely difficult for typical temperature and processing variations.

These problems are overcome by using the switched capacitor circuit shown in Fig. 1(b) which, when the ratio of the sampling frequency to the maximum passband frequency is large, closely approximates the conventional differential integrator of Fig. 1(a) [9]-[10]. The differential switched capacitor integrator is operated with two-phase nonoverlapping clocks. During the sample phase, the switches are thrown to the left, and the difference between voltages V_1 and V_2 is sampled and stored on C_u. During the integration phase, the switches are thrown to the right, and the difference voltage is scaled and stored on C_I. By switching C_u at a high clock rate, f_c, relative to the passband frequencies, an equivalent resistance is obtained of value

$$R_{EQ} = \frac{1}{f_c C_u} \tag{1}$$

resulting in an integrator gain constant of

$$\omega_o = \frac{1}{R_{EQ} C} = f_c \left| \frac{C_u}{C_I} \right|. \tag{2}$$

The switched capacitor realizes a very large resistance in a very small chip area. For example, from Eqn. (1), it can be seen that by switching a 1 pF capacitor at 100 kHz, an equivalent resistance of 10 MΩ is realized in an area of only about 5 mil^2 for C_u plus a few additional mil^2 for the minimum geometry MOSFET switch transistors. If this

equivalent resistor is used in conjunction with $C_I = 10C_u$, a gain constant of 10^4 radians/sec is obtained. Since the gain constant in Eqn. (2) is determined by a ratio of monolithic capacitors, high matching accuracy and excellent temperature stability are obtained in monolithic MOS implementations [9]-[12].

III. Active Ladder ("Leapfrog") Filters

In this section, the sensitivity properties of doubly-terminated RLC ladder filters will be reviewed, and a method will be presented for transforming these passive networks into active ladder equivalents using switched capacitor integrators.

A. Sensitivity of Doubly-Terminated RLC Ladder Filters

The classical doubly-terminated RLC ladder network shown in Fig. 2(a) has a transfer function which has very low sensitivity in the passband to reactive element variations [15]. In fact, at those frequencies where a maximum power transfer condition exists, the sensitivity is actually zero for changes in these element values.

The low sensitivity is illustrated by considering a specific example. The fifth-order RLC lowpass ladder filter of Fig. 2(a) has been frequency scaled to realize a Chebyshev response with 0.1 dB nominal passband ripple and a nominal cutoff frequency of 3.4 kHz as shown in

Fig. 2(b) [16]. The transfer function of this particular filter is most sensitive to variations in C_3. Fig. 2(c) shows the simulated passband deviation from the nominal design for a ± 1 % variation in C_3. At those frequencies where the filter response of Fig. 2(b) has a gain of -6 dB, indicating maximum power transfer, the passband deviation and hence the sensitivity is zero. The sensitivity across the entire passband is very low since a ± 1 % variation in C_3 results in a maximum passband deviation of only ± 0.015 dB.

B. Synthesis of Active Ladder Filters

Figure 3(a) shows a typical section of an RLC ladder network containing a single inductor, L_2, and a single capacitor, C_3. The current through the inductor is

$$I_2 = \frac{1}{sL_2}V_2 = \frac{1}{sL_2}(V_1 - V_3) \tag{3}$$

which can be represented as a voltage

$$V_2' = RI_2 = \frac{R}{sL_2}(V_1 - V_3) \tag{4}$$

where R is a scaling resistance used to convert currents to voltages which can usually be set equal to 1 ohm. From Eqn. (4), it is seen that V_2' is the output of a differential integrator which can be implemented as the switched capacitor integrator labelled L_2 in Fig. 3(b). The capacitance ratio for this switched capacitor integrator depends directly on the value of L_2 and is given by

$$\frac{C_{L_2}}{C_u} = \frac{f_c L_2}{\omega_{co}} \tag{5}$$

where ω_{co} is the desired cutoff frequency of the filter, f_c is the sampling rate, and L_2 is determined from standard tables which are normalized for a cutoff frequency of 1 rad/sec [16].

Similarly, the voltage across the capacitor, C_3, is

$$V_3 = \frac{1}{sC_3} I_3 = \frac{1}{sC_3}(I_2 - I_4) \tag{6}$$

which can be converted to an equivalent all-voltage form of

$$V_3 = \frac{1}{sRC_3}(RI_2 - RI_4) = \frac{1}{sRC_3}(V_2' - V_4') \tag{7}$$

where R may again equal 1 ohm. V_3 is the output of an integrator, labelled C_3 in Fig. 3(b), with a capacitance ratio of

$$\frac{C_{C_3}}{C_u} = \frac{f_c C_3}{\omega_{co}}. \tag{8}$$

Notice that the capacitor ratio again depends directly on the value of the reactive element value, C_3. Because of this one-to-one correspondence between the integrator capacitor ratios (gain constants) and the reactive element values, the switched capacitor active ladder filter will retain nearly the same low sensitivity as the passive RLC prototype from which it was derived. This transformation procedure can be used to construct the complete active ladder equivalent for any RLC doubly-terminated passive ladder network. For example, the fifth-order all-pole RLC

lowpass filter of Fig. 2(a) has been transformed to its complete switched capacitor leapfrog equivalent shown in Fig. 4. An important point to note is that the clock phasing of adjacent integrators must be alternated to eliminate excess phase shift in order to preserve the desired low sensitivity [17]. In Section V, a complete design example including transmission zeros is given to illustrate the procedures described in this section.

IV. Practical Considerations for IC Implementations

As described in the previous section, passive doubly-terminated RLC networks can be converted to active ladder equivalents composed of MOS capacitors, switches, and operational amplifiers (op amps). Nonidealities associated with these components can affect the performance of switched capacitor ladder filters. In this section, the effects that these nonidealities have on the response of the filter will be presented.

A. Amplifier DC Offset Voltage

Fig. 4 shows that the gain around all two-integrator loops and all termination loops is negative, which defines a stable bias point even in the presence of op amp DC offset voltage. In terms of the overall filter, the individual op amp offsets contribute to a DC offset voltage at the output of the filter which is given by

$$V_{os} = \frac{\sum_{i=0}^{i=n} V_{os_i}}{2} \qquad (9)$$

where n is the total number of integrating stages, and V_{os_i} is the DC offset voltage of the i^{th} operational amplifier.

B. Amplifier Open-Loop DC Gain

A switched capacitor integrator is implemented using a differential amplifier, which in the case of Fig. 5(a), has an open-loop DC gain of A. Ideally, A is infinite, and the integrator has a pole at the origin of the s-plane as shown in Fig. 5(b). However, if A is finite, the effect is to produce a lossy integrator by moving the pole away from the imaginary axis as indicated by the arrow. Fig. 5(c) shows the simulated effect that op amp DC gain variations have on the frequency response of a fifth-order Chebyshev lowpass filter which has the nominal response of Fig. 2(b). In the lower trace, all five op amps have an open loop gain of 100. In this case, the filter has a DC gain error of 0.22 dB with a passband droop of 0.09 dB due to the poles being pushed away from the imaginary axis. In the upper trace of Fig. 5(c), all five op amps have an open loop gain of 1000, and the filter response shows a DC gain error of 0.02 dB and passband deviation of less than 0.02 dB. Hence, for this example, op amps with a gain of 1000 are sufficient.

C. Parasitic Capacitances

An MOS differential switched capacitor integrator is

shown in Fig. 6(a). The gate-to-diffusion overlap capacitance, labelled C_p, will feed a portion of the clock signal, ϕ_2, onto the output. The effect of this feedthrough is to produce a DC offset voltage at the output of the integrator [11]. Self-aligned MOS technologies with small overlap capacitances can be used to greatly reduce this effect.

It is more important to consider the parasitic capacitances associated with the inverting (upper as drawn) and non-inverting (lower as drawn) plates of the switched capacitor, C_u, labelled C_A and C_B respectively, in Fig. 6(b). First, consider the parasitic, C_B, which will be charged to V_2 when the switches are thrown to the left. When the switches are thrown to the right, C_B is discharged to ground, and thus has no effect on the charge stored on C_I. On the other hand, when the switches are to the left, the parasitic connected to the inverting plate, C_A, is charged to V_1, and when the switches are subsequently thrown to the right, C_A is discharged onto the integrating capacitor. Hence, C_A contributes an error charge whose effect must be minimized in the filter design.

Figure 6(c) shows the simulated effect that the inverting-plate parasitic capacitance has on the frequency response of the fifth-order Chebyshev lowpass filter. When $C_A = 0$, the ideal response is obtained. (All other parameters are assumed ideal.) The lower trace of Fig. 6(c) is for the case when $C_A = 0.01\ C_u$. In this case, there is a DC

gain error of 0.25 dB, and a slight peaking of 0.05 dB in the response. The amount of this peaking error which can be tolerated in a given application determines the minimum size of C_u relative to the inverting-plate parasitic. For typical monolithic MOS realizations, C_u ranges from about 0.5 pF to 2.5 pF.

D. Capacitor Ratio Errors

As mentioned in Section III, the doubly-terminated RLC ladder filter is very insensitive to component variations when there is maximum power transfer between input and output. The fifth-order switched capacitor lowpass ladder of Fig. 4 has been simulated for ± 1 % variations on all integrator capacitor ratios with a nominal design having a total passband ripple of 0.1 dB, with a cutoff frequency of 3.4 kHz when clocked at 128 kHz. As shown in Fig. 7, the worst case deviation in the passband was only ± 0.022 dB which agrees well with the sensitivity of the passive RLC prototype as described in Section III. In addition, previous work has shown that monolithic capacitor ratios can be easily matched to within a few tenths of a percent accuracy [14], and hence the typically observed passband variations due to capacitor ratio errors will be less than ± 0.022 dB for monolithic MOS realizations of this filter.

E. Noise Considerations

There are two primary sources of noise in switched

capacitor ladder filters. The first is due to the thermal noise of the MOS switch transistors, and the other primary source of noise is the op amps, which for this design typically have an RMS equivalent input noise of 50 μV. In many cases, this is the dominant source of noise.

The complete noise analysis of the switched capacitor ladder filters is quite complicated. In general, it can be stated that the output noise of the filter is composed of contributions from each amplifier and each switched capacitor. The amount of each contribution at the output is determined by transfer function from the noise source to the output. The filtering of internal noise sources is evident in the output noise spectrum of Fig. 8, which was taken from the third-order elliptic filter which will be described in Section VI.

F. Frequency Limitations

The maximum sampling frequency for MOS switched capacitor ladder filters is determined by the settling time characteristics of the MOS op amps. As the passband frequency is increased relative to the clock rate, large signal characteristics such as the slew rate become important and ultimately determine the maximum cutoff frequency relative to the clock rate. The switched capacitor filters described in this paper operated satisfactorily at a maximum clock rate of about 400 kHz.

The minimum sampling rate is determined by leakage currents in the reverse-biased pn junctions which cause a DC voltage drift which is typically on the order of 10 mV/sec, assuming a 1 pF capacitor, 100 μm^2 of junction area, and a thermal leakage current density of 10 nA/cm^2. This effect limits the minimum sampling frequency to a few hundred Hz.

V. Experimental Results for Five-Pole Lowpass Filter

In this section, results are presented for a fifth-order Chebyshev all-pole lowpass ladder filter. The filter has been integrated using an n-channel metal-gate depletion-load process with 10 micron minimum feature sizes.

A. NMOS Operational Amplifier

A differential amplifier is required to implement the switched capacitor integrators used in the active ladder filters. Fortunately, as mentioned in Section IV, relatively low performance op amps are required. For example, the op amp shown schematically in Fig. 9 which has been used to implement the filters is a simplified version of a recently reported design [10]. It features a DC open-loop gain of 1000 with a power dissipation of 6 mW. Table I summarizes the measured parameters for this operational amplifier.

B. Fifth-Order Lowpass Ladder Filter

The fifth-order all-pole lowpass filter shown

schematically in Fig. 4 has been integrated in NMOS technology. It was designed for the response of Fig. 2(b) with a sampling rate of 128 kHz. The measured frequency response of Fig. 10 shows very close agreement with the expected design values.

Table II summarizes the measured parameters for the fifth-order lowpass filter. The output noise in the frequency band from 300 Hz to 3 kHz is 180 μV_{RMS}, and the output voltage for 1 % total harmonic distortion (THD) is 2.6 $volts_{RMS}$. Using these numbers, the dynamic range for this filter is calculated to be 83.5 dB.

A die photo of the experimental chip is shown in Fig. 11. The op amp, shown in the lower left corner, was integrated in an area of about 400 mil^2. The upper section of the chip contains the fifth-order switched capacitor lowpass ladder filter. The five op amps are embedded in the center with the integrating capacitor arrays around the edges. The integrating capacitors range in value from about 10 pF to about 40 pF using a standard switched capacitor size of about 2.3 pF. The overall die size is about 100 mils by 100 mils, while the fifth-order filter itself is about 90 mils by 70 mils.

VI. Finite Transmission Zeros

A. Implementation Using Integrators/Summers

The addition of finite transmission zeros to the filter frequency response has great importance in many applications. The transmission zeros are easily obtained by adding shunt elements to the passive RLC prototype. For example, by adding the shunting capacitor C_2 across L_2 in Fig. 12(a), a complex transmission zero pair is obtained at the resonant frequency of the series arm given by

$$\omega_{zero} = [C_2 L_2]^{-1/2}. \tag{10}$$

Intuitively, it is clear that C_2 feeds a portion of V_1 forward to node B, and a portion of V_3 back to node A. Analytically, we can represent this by solving for V_1 and V_3:

$$V_1 = \frac{(I_0 - I_2)}{s(C_1+C_2)} + V_3 \left| \frac{C_2}{C_1+C_2} \right|, \tag{11}$$

and

$$V_3 = \frac{(I_2 - I_4)}{s(C_2+C_3)} + V_1 \left| \frac{C_2}{C_2+C_3} \right|. \tag{12}$$

Using these relationships, the RLC elliptic filter can be represented in the equivalent form of Fig. 12(b).

Eqns. (11) and (12) show that the realization of V_1 and V_3 requires a circuit which simultaneously performs the operations of integration and summation. This building block is shown in Fig. 13, where the summation is achieved

by adding the capacitor C_S to the standard switched capacitor differential integrator. Since the summation is inverting, the final switched capacitor circuit configuration must be slightly modified so that V_1 and V_3 are of the opposite sign [13],[17].

A switched capacitor equivalent of the third-order elliptic lowpass filter of Fig. 12(b) is shown in Fig. 14. Notice that only three op amps are required. The transmission zeros are realized by adding the feedback capacitor labelled C_{C_2} on the left, and the feedforward capacitor labelled C_{C_2} on the right. No additional op amps are required to implement transmission zeros, and since the summation terms are also determined by capacitor ratios, high precision is obtained in monolithic MOS implementations.

B. Design Example for a Third-Order Elliptic Filter

The first step in the design procedure is to determine the element values for Fig. 12(a) from standard tables which are normalized for a cutoff frequency of 1 rad/sec [16]. In this case, the desired parameters are 0.117 dB passband ripple, a minimum stopband rejection of 30.41 dB, and a normalized zero frequency of 2.6 rad/sec. The normalized element values are

$$R_1 = R_2 = 1\ \Omega \qquad 13(a)$$

$$C_1 = 1.0855\ F \qquad 13(b)$$

$$C_2 = 0.1466\ F \qquad 13(c)$$

$$C_3 = 1.0855\ F \qquad 13(d)$$

$$L_2 = 1.0090\ H. \qquad 13(e)$$

The next step is to calculate the capacitor ratios for a cutoff frequency of 3400 Hz (21363 rad/sec), and a zero frequency of 8.84 kHz when clocked at 128 kHz: (Referring to Eqns. (5) and (8) and Fig. 12(b).)

$$\frac{C_{C_1+C_2}}{C_u} = \frac{f_c(C_1+C_2)}{\omega_{co}} = 7.3824 \qquad 14(a)$$

$$\frac{C_{L_2}}{C_u} = \frac{f_c L_2}{\omega_{co}} = 6.0456 \qquad 14(b)$$

$$\frac{C_{C_2+C_3}}{C_u} = \frac{f_c(C_2+C_3)}{\omega_{co}} = 7.3824 \qquad 14(c)$$

and for the zero-forming capacitor ratios,

$$\frac{C_{C_2}}{C_{C_1+C_2}} = \frac{C_2}{C_1+C_2} = 0.119 \qquad 15(a)$$

and

$$\frac{C_{C_2}}{C_{C_2+C_3}} = \frac{C_2}{C_2+C_3} = 0.119. \qquad 15(b)$$

Finally, a minimum value for the switched capacitor, C_u, is chosen based on the considerations described in Section IV, and the integrating and zero-forming capacitor values are then calculated from Eqns. (14) and (15). Experimental results for an NMOS monolithic version of this filter are presented in the next section.

C. Elliptic Filter Experimental Results

The switched capacitor third-order elliptic filter of Fig. 14 has also been integrated using the same process and op amp described earlier, and is shown in the die photo of Fig. 15. The filter was designed to meet the specifications of the design example given above when clocked at 128 kHz. The measured response of Fig. 16 shows very close agreement with the expected design values. The zero insertion loss for this filter is achieved by doubling the size of the input switched capacitor, labelled $2C_u$ in the schematic of Fig. 14. Table III summarizes the measured filter performance for this filter. The increase in dynamic range to 90 dB is due to the presence of fewer noise sources as discussed earlier in Section IV.

In Fig. 15, the integrating capacitors are each about 20 pF, while the small (2 pF) capacitors directly to the left of the first and third integrating capacitors are used to implement the transmission zeros. The overall die size is about 40 mils by 110 mils.

VII. General Design Considerations

There are a variety of possible circuit configurations using MOS switches, capacitors, and op amps which can be used to implement active ladder filters. Some general design considerations for these circuits are summarized below:

[1] All nodes are connected to a voltage source or virtual ground except when being switched.

A node which is only connected to capacitors is particularly sensitive to parasitic capacitances connected to that node, and charge sharing between capacitors introduces extra poles which complicates the synthesis procedures. High impedance capacitive nodes are subject to charge buildup through leakage currents, ultraviolet radiation, and power-up transients, and therefore should be avoided in switched capacitor circuits.

[2] Minimize the number of operational amplifiers.

MOS operational amplifiers consume a major portion of the required die area, and almost all the power in switched capacitor filters. In the active ladder circuits, there is a need for arithmetic functions such as multiplications by fixed factors, sign inversions, and summing and differencing in addition to integration. In the circuits which have been described, these operations were performed by using MOS switches and capacitors in conjunction with operational amplifier integrators.

[3] Positive op amp inputs should be connected to a constant bias voltage.

If this rule is violated, the response of the circuit depends on the parasitic capacitances connected to the op amp inputs. These parasitics can induce errors, and

considerably complicate the design procedure.

When signals are applied to both op amp inputs, the common-mode performance of the amplifier becomes important since CMRR and common-mode range limitations can also induce errors in the filter response. By observing [3], there are no pure common-mode signals, and this problem is eliminated.

[4] The capacitor plate with the most substrate parasitic capacitance should be connected to the non-inverting input of the switched capacitor differential integrator.

As mentioned in Section IV, the inverting-plate parasitic capacitance determines the minimum switched capacitor size for a given tolerance in the frequency response, while bottom-plate parasitics have no effect on the response.

The first two rules listed above can be contradictory, and hence, the designer must decide on their relative importance. For example, in certain cases it has been shown that the number of op amps can be reduced to decrease the power and area requirements if rule 1 is violated [9]-[10]. However, the design was considerably more complicated and more sensitive to parasitics than for this paper, where the rules were observed in their order of importance as listed above.

VIII. Conclusions

A new approach for realizing precision monolithic

high-order filters in MOS technology has been described. This approach uses MOS switched capacitor integrators with gain constants determined by capacitor ratios to achieve excellent processing and temperature stability. By using these integrators in the active ladder configuration, precise frequency responses are obtained which are very insensitive to component variations. Results were presented for two different monolithic filters. The first circuit implemented a fifth-order Chebyshev all-pole lowpass response, and achieved a dynamic range of 83 dB with power dissipation of 30 mW. Sampling rates of 128 kHz were used to reduce the anti-aliasing prefilter requirements. The second circuit realized a third-order elliptic lowpass response, and achieved a dynamic range of 90 dB with a power dissipation of 18 mW.

This approach is applicable to bandpass filters [17], and by using weighted integrating capacitor arrays, programmable filters may be designed.

IX. Acknowledgements

The authors acknowledge helpful discussions with K.S. Tan, I.A. Young, G.M. Jacobs, and Prof. D.A. Hodges who are involved in other monolithic filtering approaches.

X. References

[1] R. A. Friedenson, R. W. Daniels, R. J. Dow and P. H. McDonald, "RC active filters for the D3 channel bank," Bell System Technical Journal, Vol. 54, No. 3, pp. 507-529, March 1975.

[2] K. S. Tan and P. R. Gray, "Fully integrated analog filters using Bipolar/JFET technology," IEEE J. Solid-State Circuits, this issue.

[3] D. D. Buss, D. R. Collins, W. H. Bailey, and C. R. Reeves, "Transveral filtering using charge transfer devices," IEEE J. Solid-State Circuits, Vol. SC-8, pp. 138-146, April 1973.

[4] R. D. Baertsch, W. E. Engeler, H. S. Goldberg, C. M. Puckette, and J. J. Tiemann, "The design of practical charge-transfer transversal filters," IEEE Trans. Electron Devices, vol. ED-23, pp. 133-142, Feb. 1976.

[5] C. H. Séquin, "Antialiasing inputs for charge-coupled devices," IEEE J. Solid-State Circuits, vol. SC-12, pp. 609-616, Dec. 1977.

[6] D. L. Fried, "Analog sampled-data filters," IEEE J. Solid-State Circuits, vol. SC-7, pp. 302-304, Aug. 1972.

[7] A. Fettweis, "Theory of resonant transfer circuits," Adv. Study Institute on Network and Switching Theory, Italy, Sept. 1966.

[8] I. A. Young, P. R. Gray and D. A. Hodges, "Analog NMOS sampled-data recursive filters," in Digest of Int. Solid-State Circuits Conf., Philadelphia, pp. 156-157, Feb. 1977.

[9] B. J. Hosticka, R. W. Brodersen and P. R. Gray, "MOS sampled data recursive filters using state variable techniques," in Proc. Int. Symp. on Circuits and Sys-

tems, Phoenix, Az, pp. 525-529, April 1977.

[10] B. J. Hosticka, R. W. Brodersen and P. R. Gray, "MOS sampled data recursive filters using switched capacitor integrators," IEEE J. Solid-State Circuits, vol. SC-12, pp. 600-608, Dec. 1977.

[11] J. T. Caves, M. A. Copeland, C. F. Rahim and S. D. Rosenbaum, "Sampled analog filtering using switched capacitors as resistor equivalents," IEEE J. Solid-State Circuits, Vol. SC-12, pp. 592-599, Dec. 1977.

[12] D. J. Allstot, R. W. Brodersen and P. R. Gray, "Fully integrated high order NMOS sampled data ladder filters," Digest of Int. Solid-State Circuits Conf., San Francisco, pp. 82-83, Feb. 1978.

[13] W. E. Heinlein and W. Harvey Holmes, Active Filters for Integrated Circuits, Prentice-Hall Intl., 1974.

[14] J. L. McCreary and P. R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques--Part I," IEEE J. Solid-State Circuits, vol. SC-10, pp. 371-379, Dec. 1975.

[15] H. J. Orchard, "Inductorless filters," Electronics Letters, vol. 2, pp. 224-225, June 1966.

[16] A. I. Zverev, Handbook of Filter Synthesis, John Wiley and Sons, Inc., New York, 1967.

[17] G. M. Jacobs, D. J. Allstot, R. W. Brodersen and P. R. Gray, "Design techniques for MOS switched capacitor ladder filters," IEEE Trans. on Circuit and Systems, Dec. 1978.

TABLE I. MEASURED NMOS OPERATIONAL AMPLIFIER PERFORMANCE PARAMETERS

Power Supplies	V_{DD} = 7.5v V_{SS} = -7.5v V_{BB} = -12.5v
DC Open Loop	1000
CMRR	54 dB
PSRR	46 dB
Unity Gain Bandwidth	1 MHz
Slew Rate	1.0 v/μsec
Power Dissipation	6 mW
Die Area	400 mil^2

TABLE II. MEASURED FILTER PARAMETERS FOR THE FIFTH-ORDER CHEBYSHEV LOWPASS LADDER FILTER

Clock Frequency	128 kHz
Ripple Bandwidth	3400 Hz
Total Passband Ripple	0.1 dB
RMS Output Voltage (1% THD)	2.7V
RMS Noise (300-3kHz)	180 μV
(300-50kHz)	335 μV
Dynamic Range	83.5 dB
Power Dissipation	30 mW
Filter Die Area	6600 mil^2

TABLE III. MEASURED FILTER PARAMETERS FOR THE THIRD-ORDER ELLIPTIC LOWPASS LADDER FILTER

Clock Frequency	128 kHz
Ripple Bandwidth	3400 Hz
Total Passband Ripple	0.15 dB
Minimum Stopband Rejection	30.4 dB
RMS Output Voltage (1% THD)	2.6 V
RMS Noise (300-3 kHz)	80 μV
Dynamic Range	90 dB
Power Dissipation	18 mW
Filter Die Area	4400 mil^2

FIGURE CAPTIONS

Fig. 1. (a) A conventional differential RC integrator, and (b) a switched capacitor differential integrator.

Fig. 2. (a) An RLC doubly-terminated fifth-order all-pole lowpass filter; (b) the nominal passband frequency response, and (c) deviations in the passband due to variations in C_3.

Fig. 3. (a) A section of an RLC ladder network, and (b) the active-ladder equivalent formed from switched capacitor differential integrators.

Fig. 4. A switched capacitor fifth-order all-pole lowpass ladder equivalent of the RLC filter of Fig. 2(a).

Fig. 5. (a) A switched capacitor integrator with op amp gain of A; (b) the integrator pole positions for infinite gain and gain of 100, and (c) the simulated effect of gain on the filter frequency response.

Fig. 6. (a) A switched capacitor differential integrator with MOSFET switch transitors and important parasitic capacitances, and (b) an equivalent symbolic representation; (c) the simulated effect of top-plate parasitic on the frequency response.

Fig. 7. Simulated deviations in the passband for the fifth-order filter for variations in the capacitor ratio of the third integrator.

Fig. 8. Output noise spectrum for a third-order elliptic lowpass switched capacitor ladder filter.

Fig. 9. NMOS depletion-load operational amplifier.

Fig. 10. (a) Measured response for the fifth-order Chebyshev switched capacitor ladder filter clocked at 128 kHz, and (b) the details of the passband.

Fig. 11. Die photo for the fifth-order all-pole lowpass switched capacitor filter. Bottom edge of chip contains test devices.

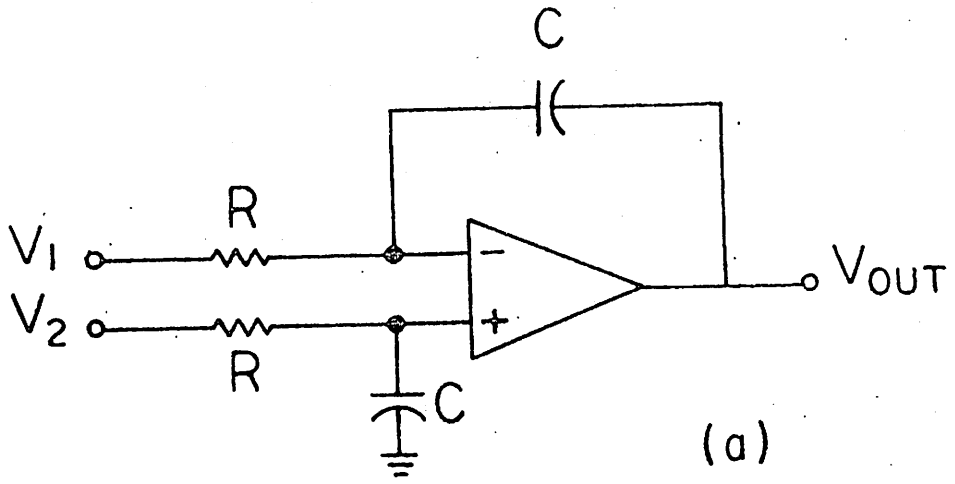
Fig. 12. (a) An RLC third-order elliptic lowpass filter, and (b) an equivalent form.

Fig. 13. A switched capacitor integrator/summer.

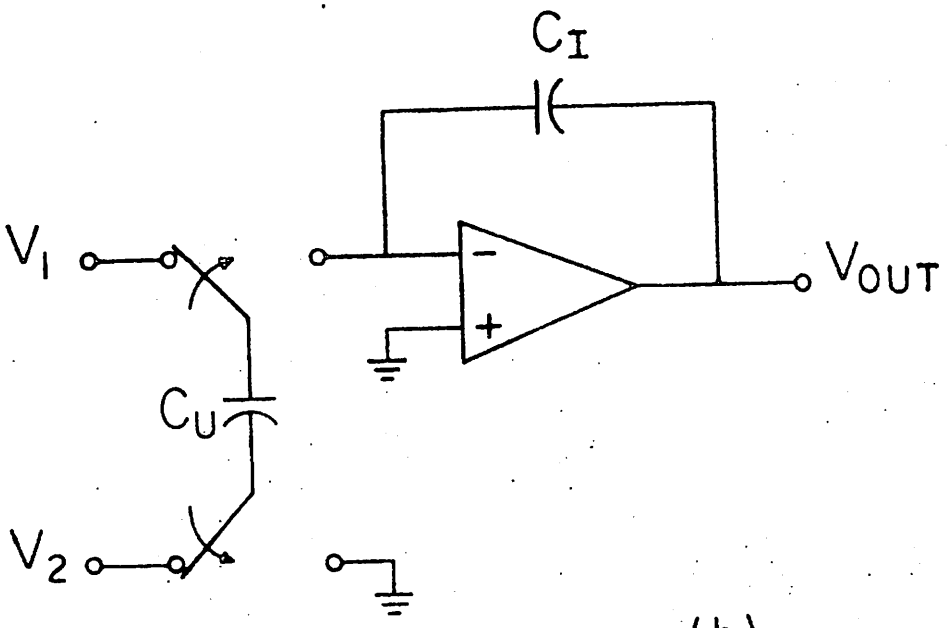
Fig. 14. A switched capacitor equivalent of the third-order elliptic lowpass filter.

Fig. 15. Die photo for the third-order elliptic lowpass switched capacitor ladder filter.

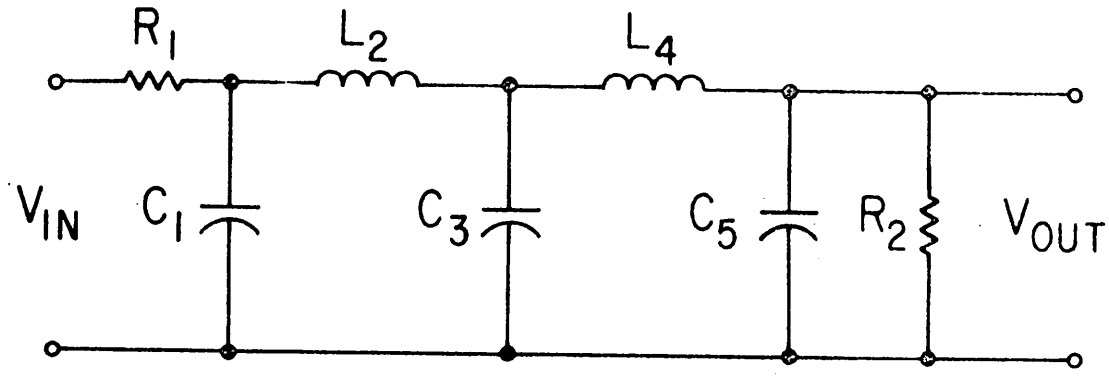
Fig. 16. (a) Measured response for the third-order elliptic switched capacitor ladder filter clocked at 128 kHz, and (b) the passband details.



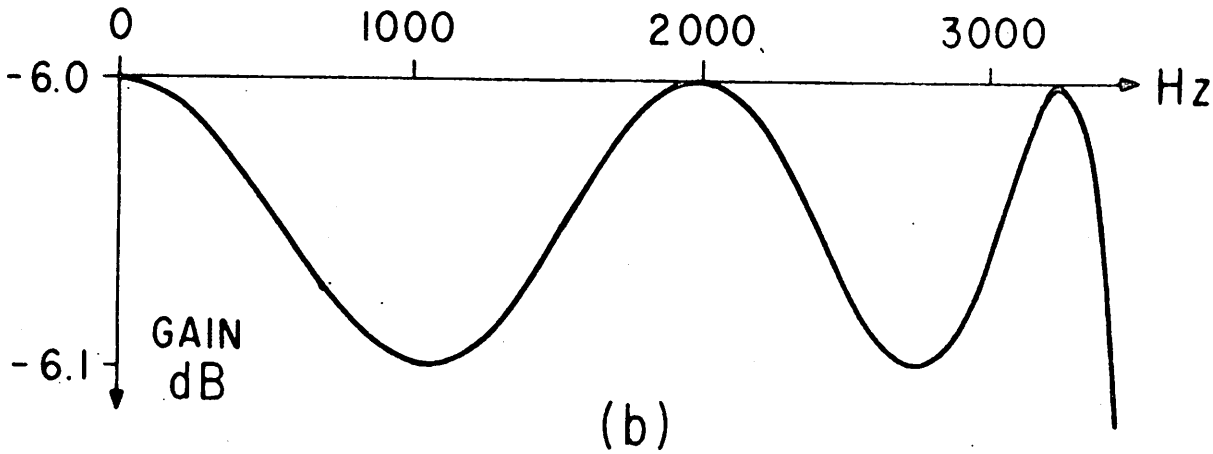
(a)



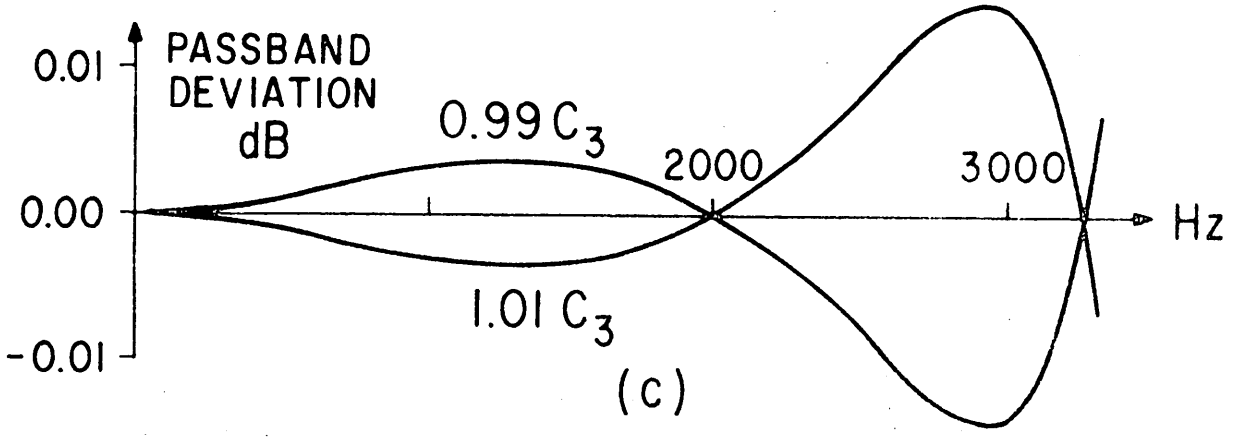
(b)


R1
L2
L4
VIN
C1
C3
C5
R2
VOUT

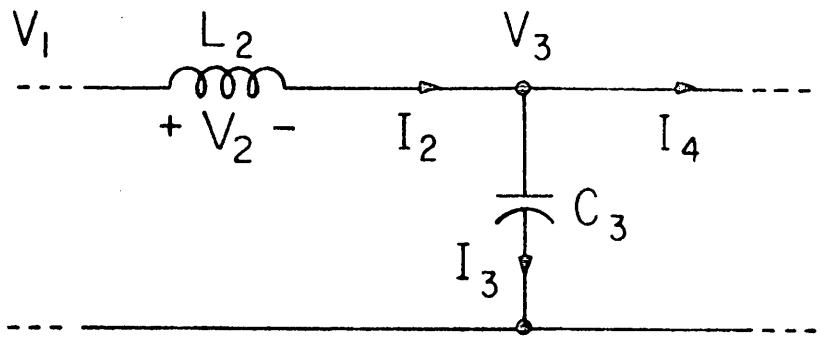
(a)


0
1000
2000
3000
-6.0
Hz
-6.1
GAIN
dB

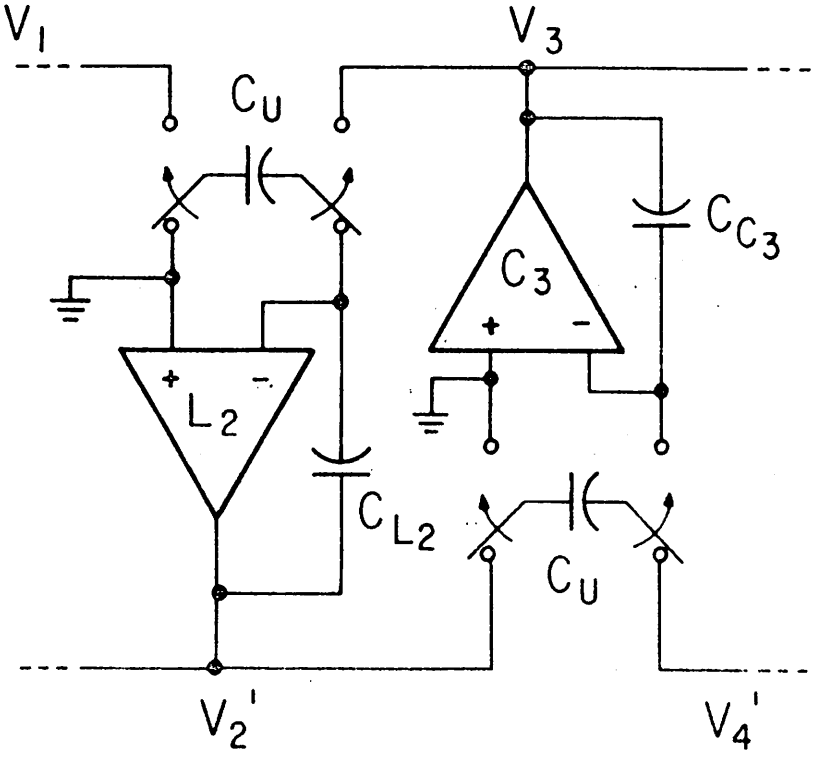
(b)


0.01
PASSBAND
DEVIATION
dB
0.99 C3
2000
3000
0.00
Hz
1.01 C3
-0.01

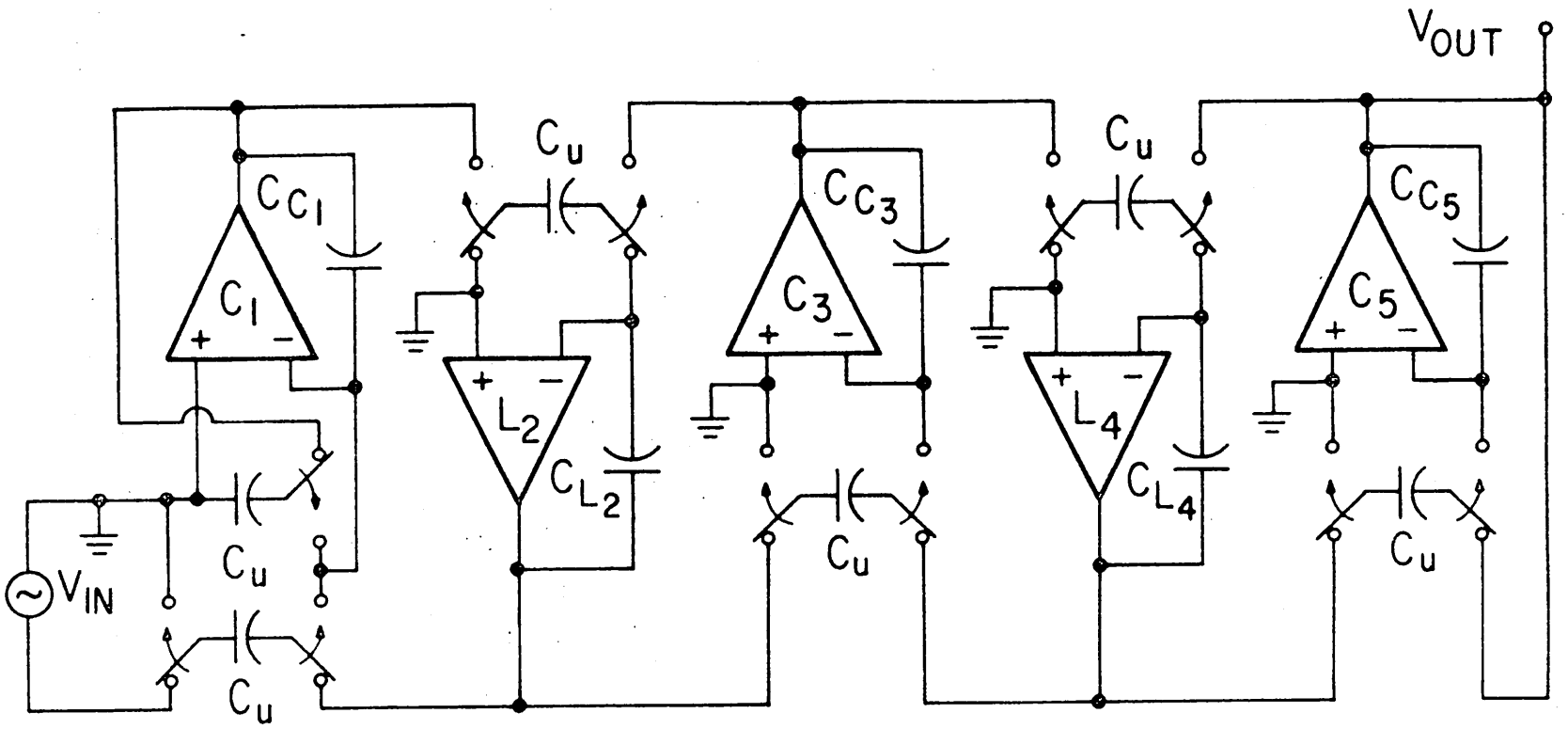
(c)

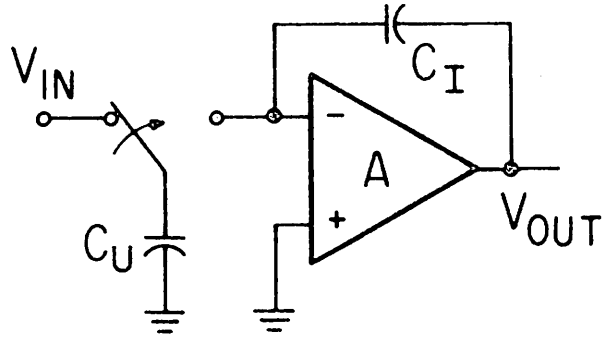


(a)

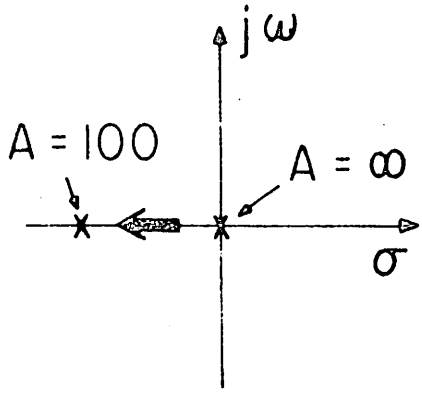


(b)

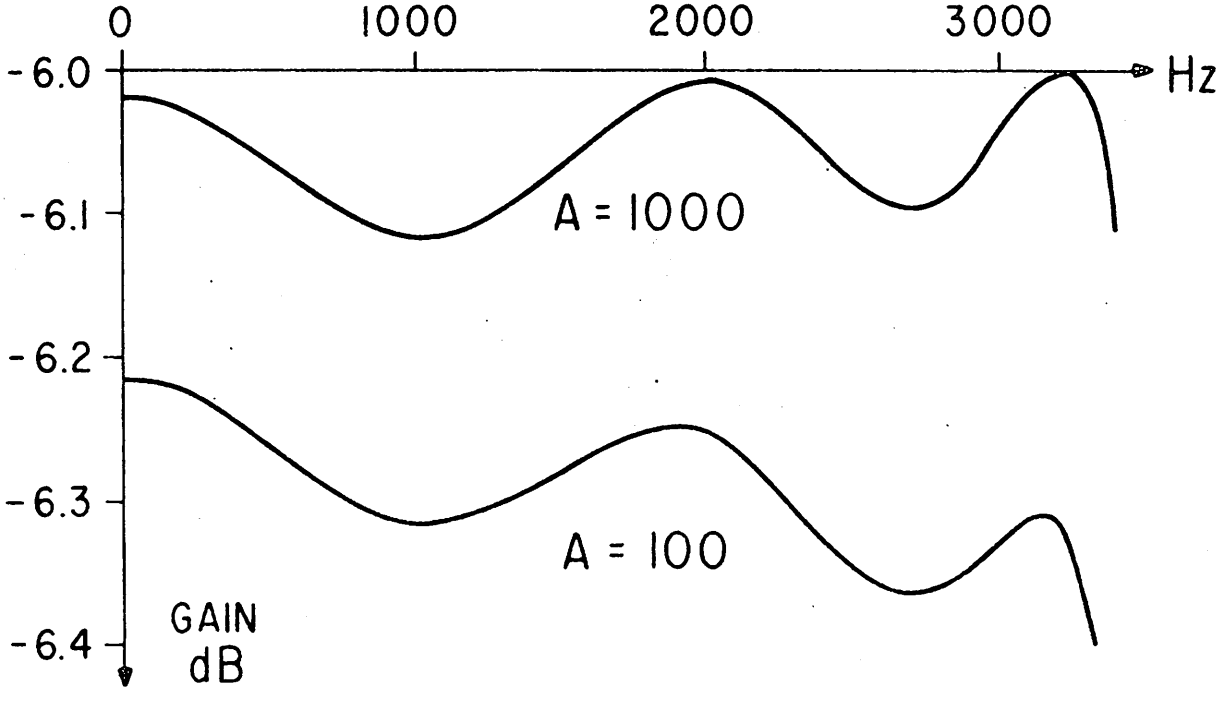

V_{OUT}
C_u
C_{C_1}
C_1
C_{C_3}
C_3
C_u
C_{C_5}
C_5
L_2
C_{L_2}
L_4
C_{L_4}
C_u
C_u
C_u
V_{IN}
C_u


V_{IN}
C_I
C_U
A
V_{OUT}

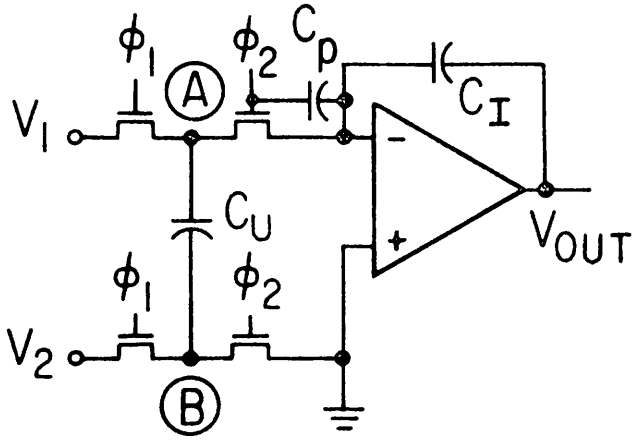
(a)


jω
A = 100
A = ∞
σ

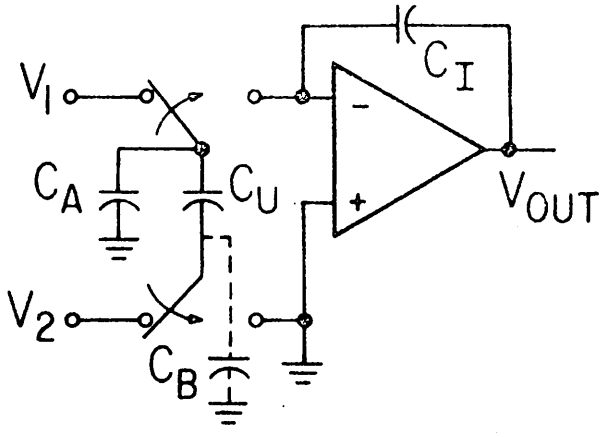
(b)


0
1000
2000
3000
Hz
-6.0
-6.1
-6.2
-6.3
-6.4
A = 1000
A = 100
GAIN
dB

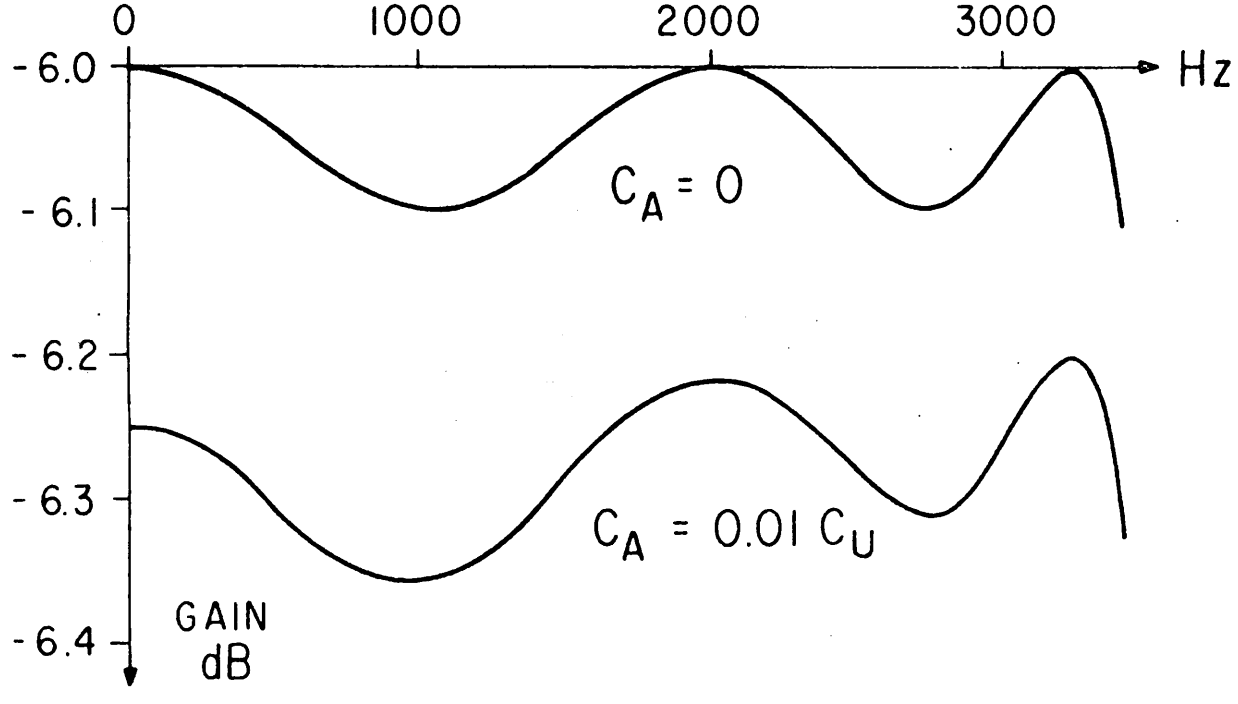
(c)


ϕ_1
ϕ_2
C_p
A
V_1
C_I
C_U
V_{OUT}
ϕ_1
ϕ_2
V_2
B

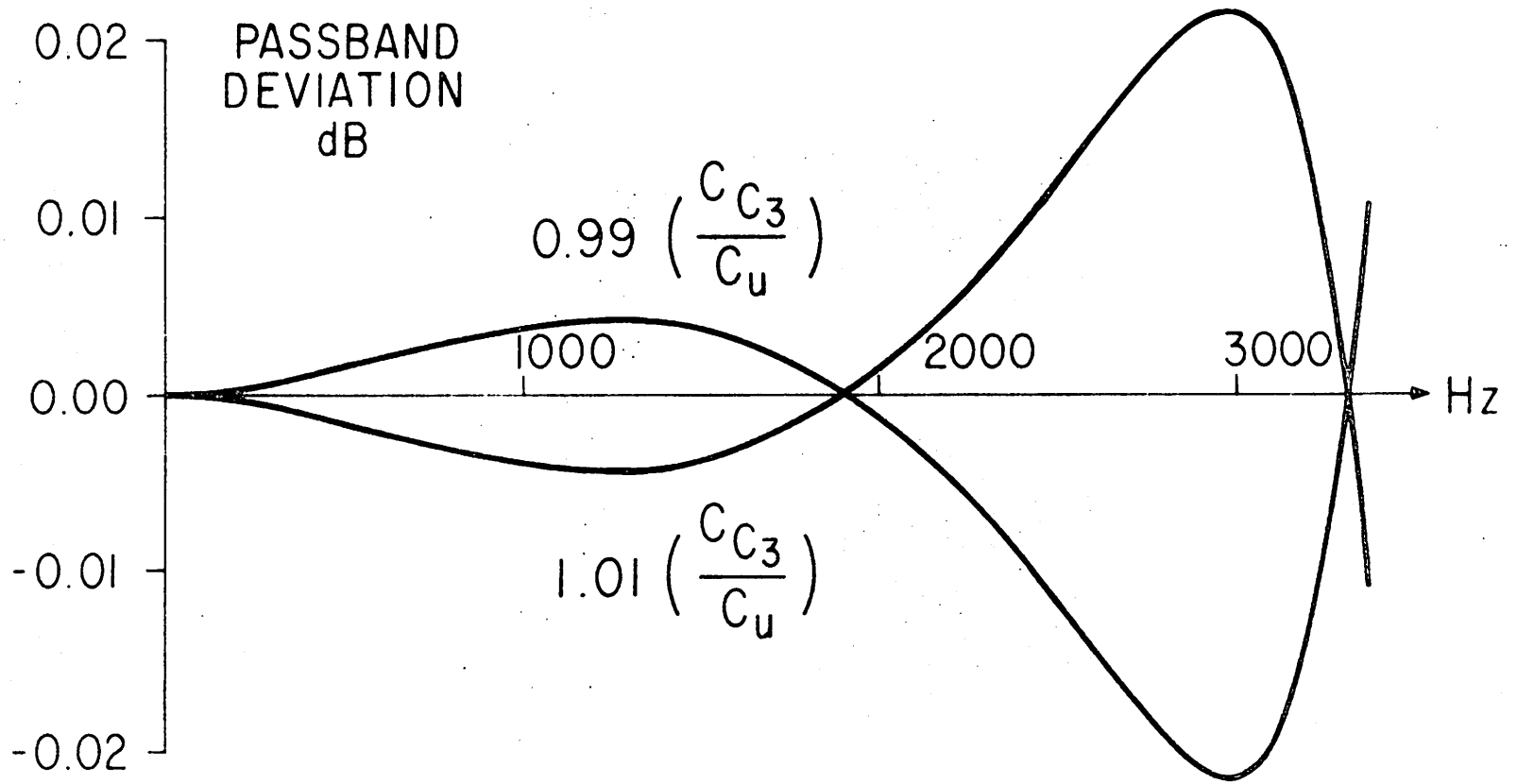
(a)

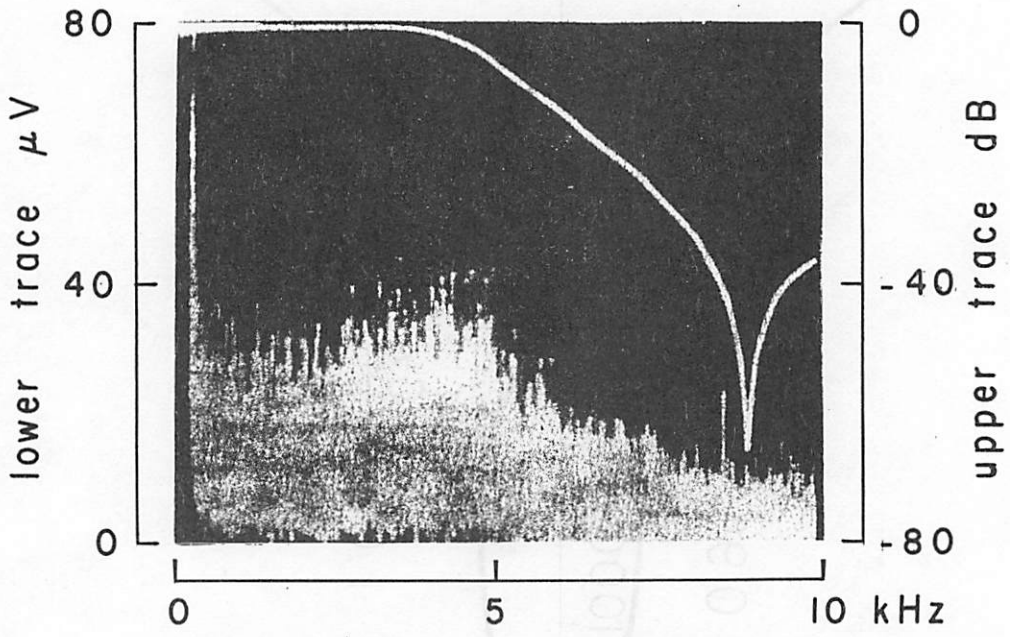

V_1
C_I
C_A
C_U
V_{OUT}
V_2
C_B

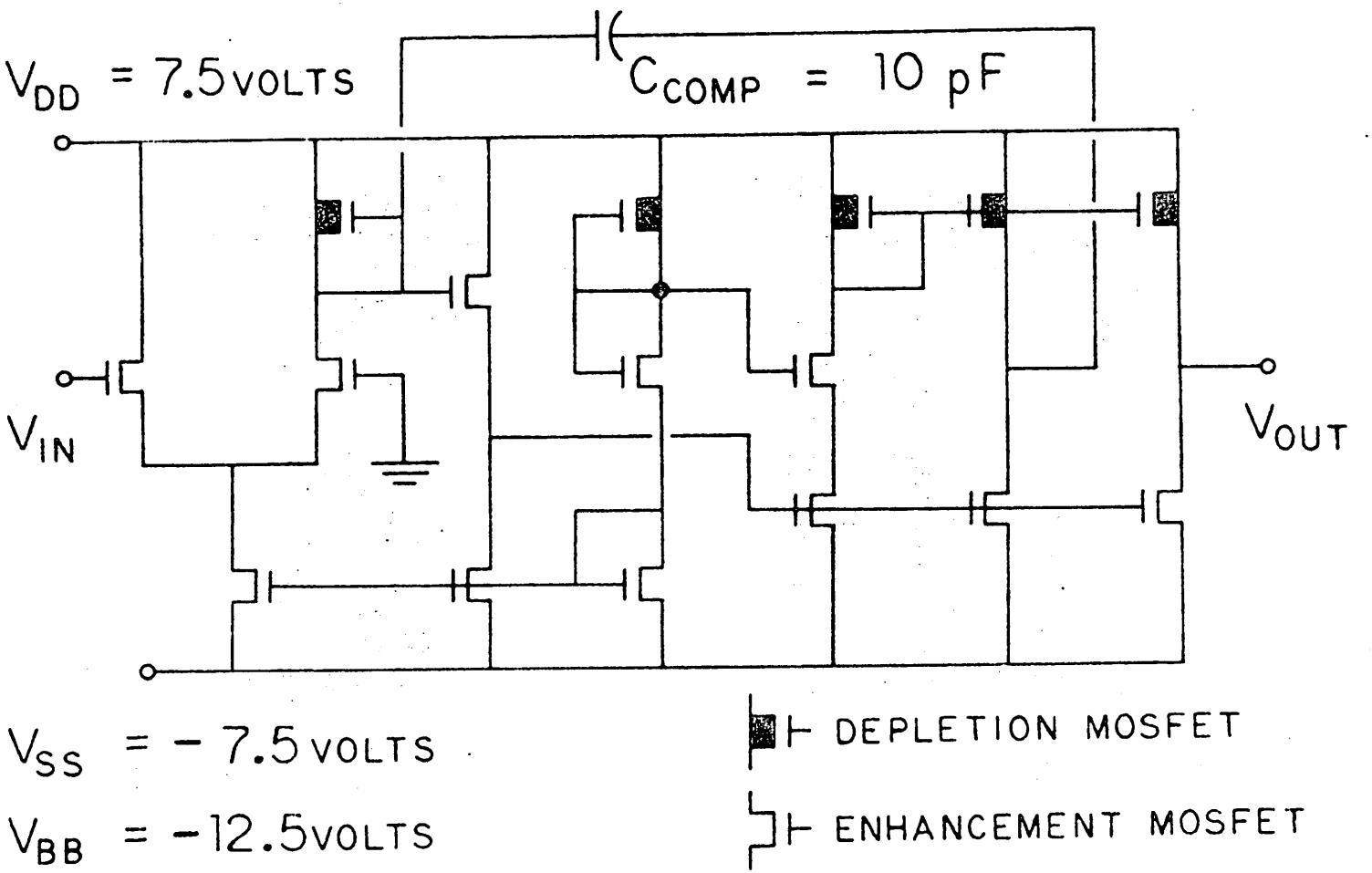
(b)

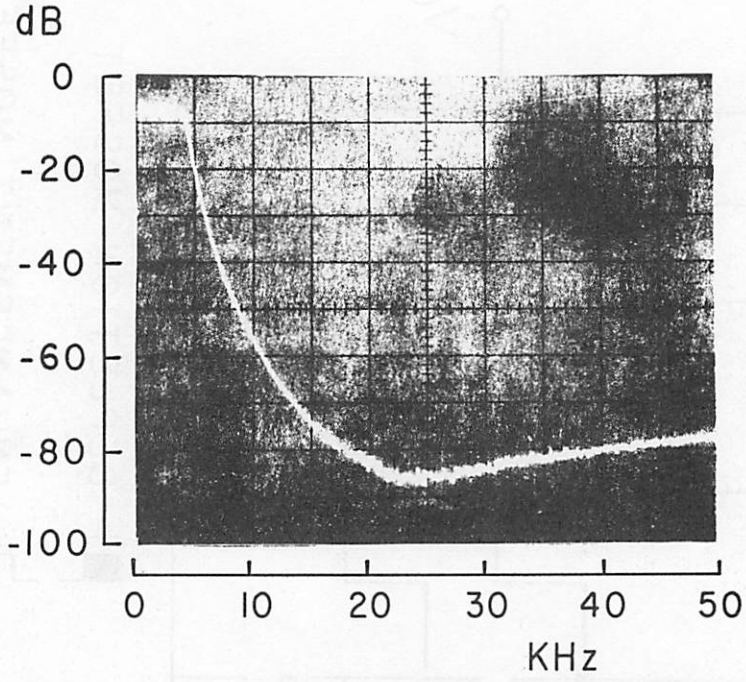

0
1000
2000
3000
Hz
-6.0
-6.1
-6.2
-6.3
-6.4
$C_A = 0$
$C_A = 0.01\ C_U$
GAIN
dB

(c)

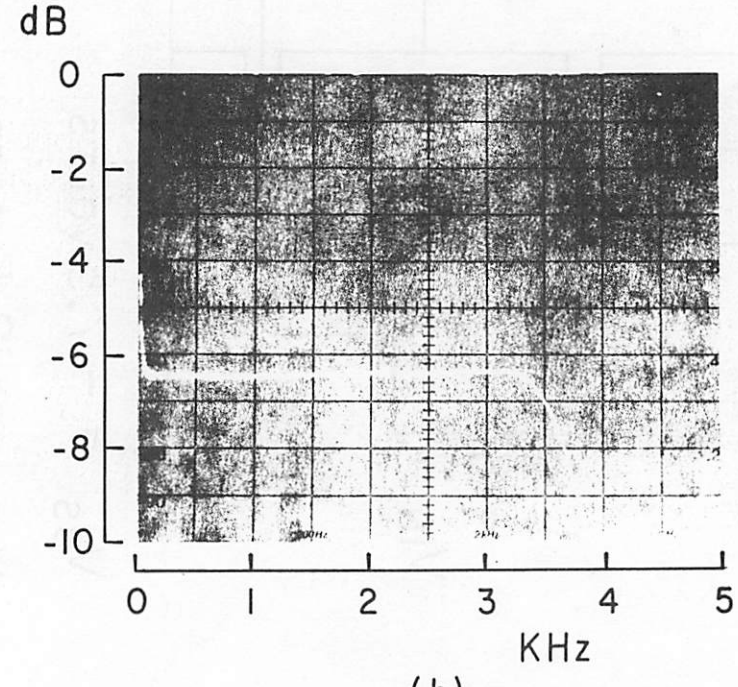

0.02
0.01
0.00
-0.01
-0.02
PASSBAND
DEVIATION
dB
0.99 (C_C3 / C_u)
1.01 (C_C3 / C_u)
1000
2000
3000
Hz


80
40
0
lower trace μV
0
-40
-80
upper trace dB
0
5
10 kHz


V_{DD} = 7.5 VOLTS
C_{COMP} = 10 pF
V_{IN}
V_{OUT}
V_{SS} = − 7.5 VOLTS
V_{BB} = −12.5 VOLTS
DEPLETION MOSFET
ENHANCEMENT MOSFET



(a)



(b)

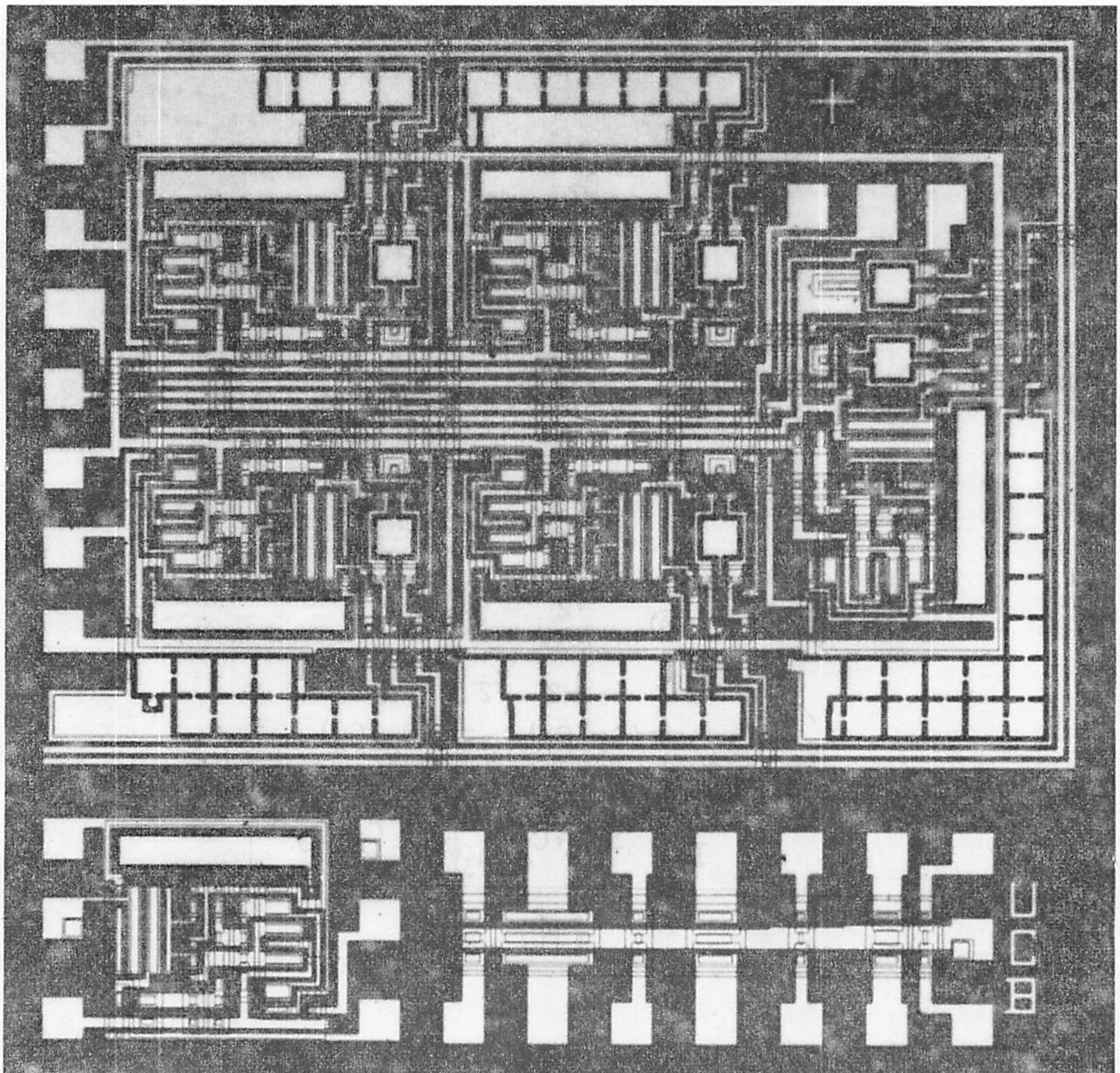
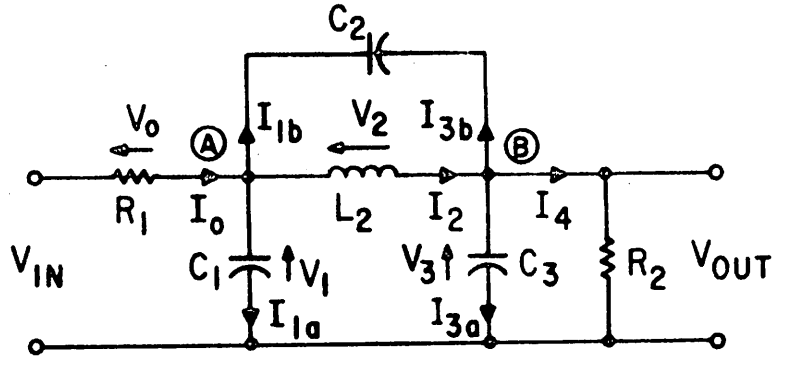
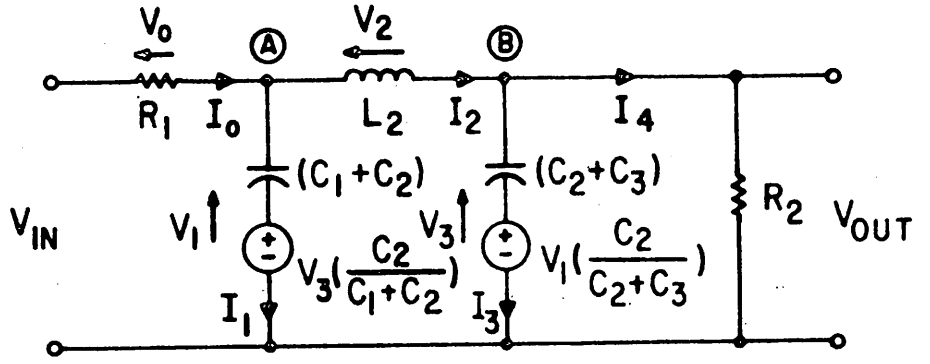


Fig. 11 Allstot, Brodersen, Gray

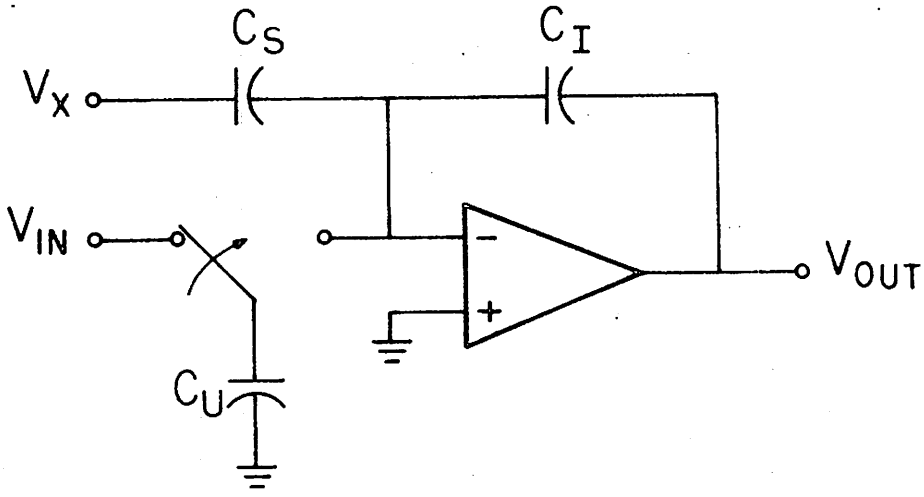

C2
V0
A
I1b
V2
I3b
B
R1
I0
L2
I2
I4
VIN
C1
V1
V3
C3
R2
VOUT
I1a
I3a

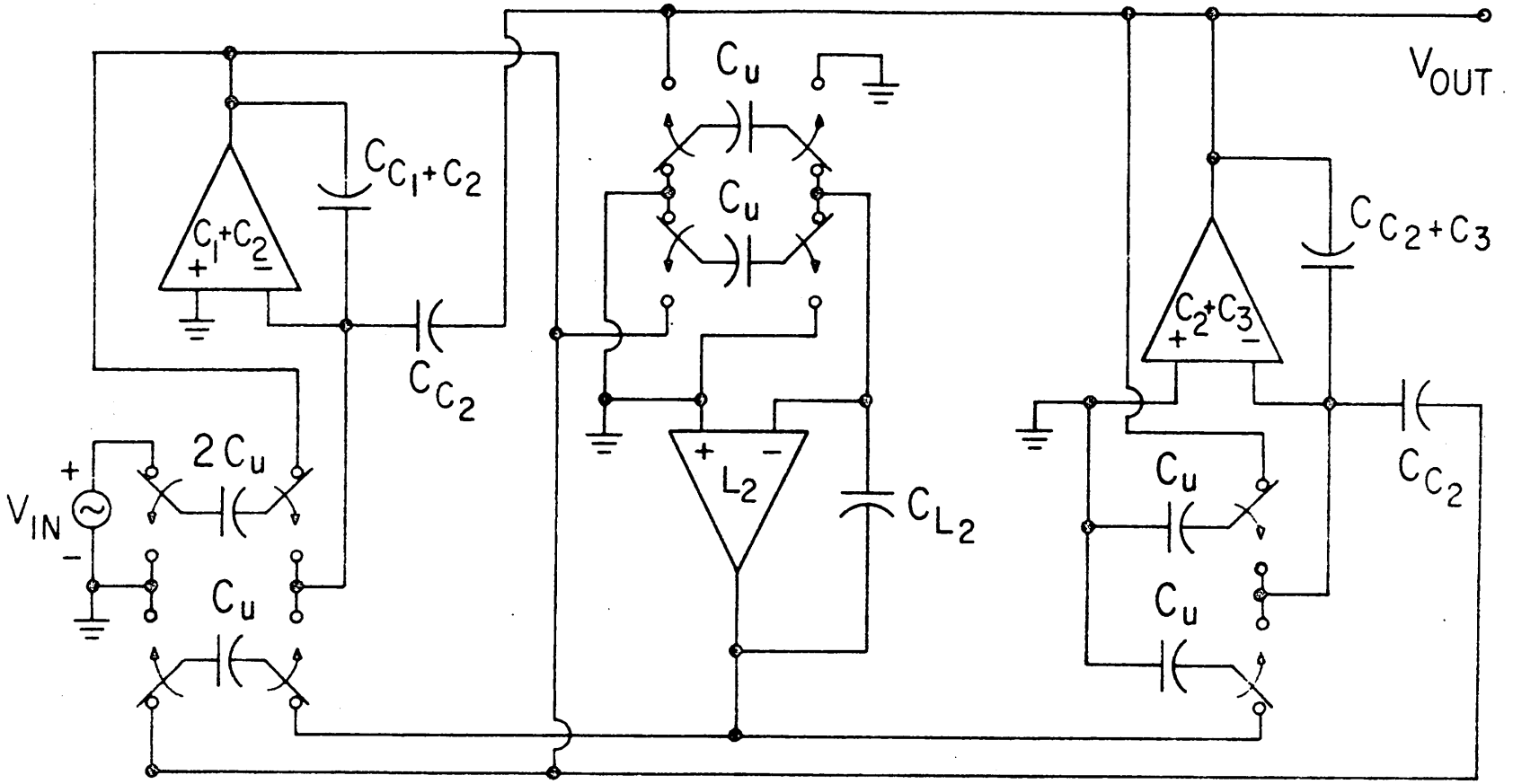
(a)


V0
A
V2
B
R1
I0
L2
I2
I4
(C1+C2)
(C2+C3)
R2
VOUT
VIN
V1
V3
V3(C2/(C1+C2))
V1(C2/(C2+C3))
I1
I3

(b)

Fig. 2 [illegible]


C_S
C_I
V_X
V_{IN}
V_{OUT}
C_U
−
+


V_{OUT}
C_u
C_u
$C_{C_1+C_2}$
C_1+C_2
C_{C_2}
$2C_u$
V_{IN}
C_u
L_2
C_{L_2}
$C_{C_2+C_3}$
C_2+C_3
C_{C_2}
C_u
C_u

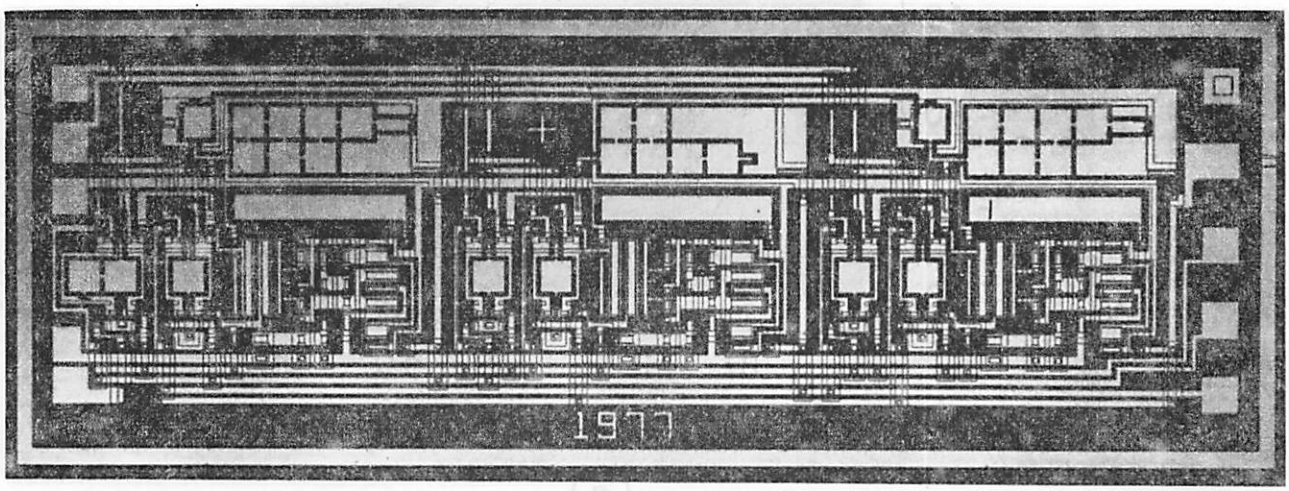
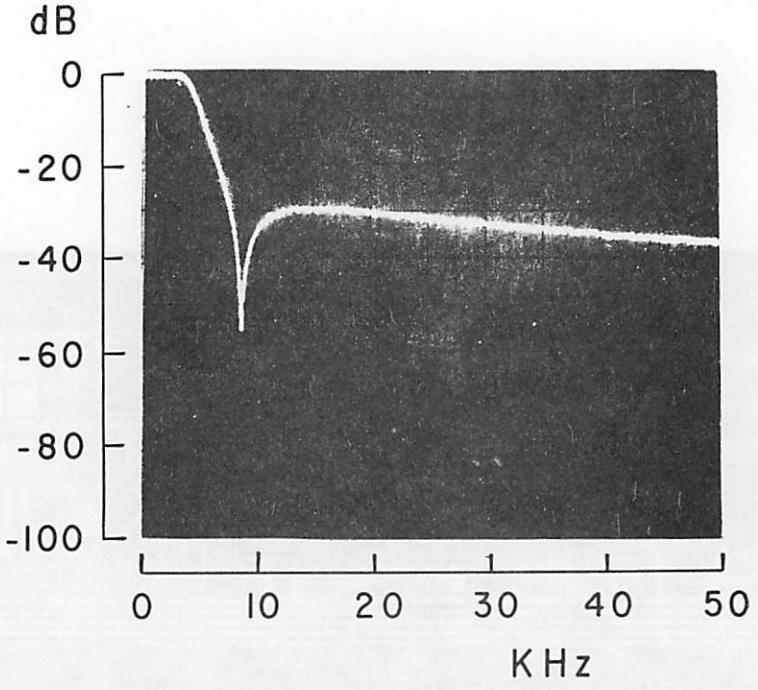
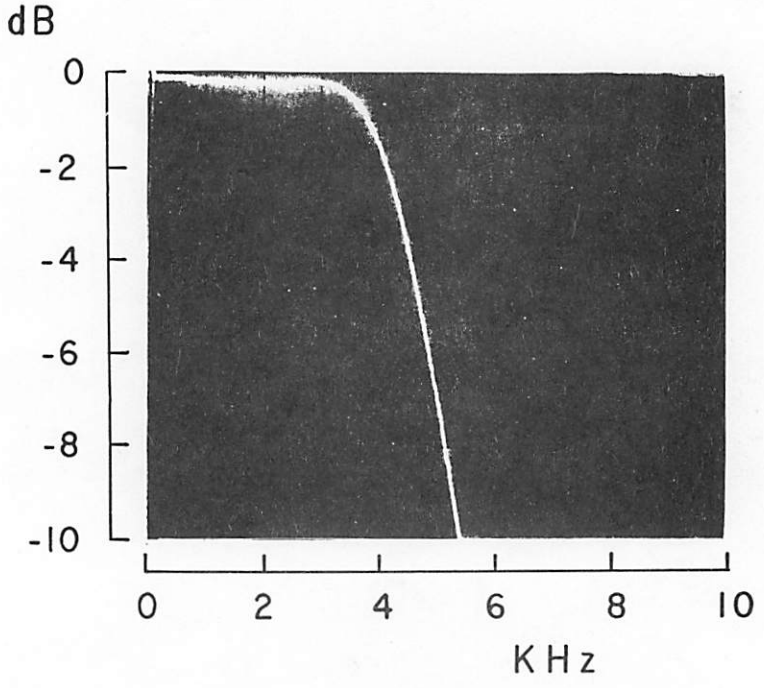


Fig. 15 Ayistat, Broderson, Gray



(a)



(b)