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MOS SWITCHED-CAPACITOR ANALOG SAMPLED-DATA RECURSIVE FILTERS

by

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MOS SWITCHED-CAPACITOR ANALOG SAMPLED-DATA RECURSIVE FILTERS

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ABSTRACT

The objective of this research has been to investigate whether analog sampled-data recursive filters can be fully integrated efficiently in MOS technology. A new technique for realizing precision audio frequency filters (lowpass, bandpass, or highpass) has been developed. A fully integrated prototype has been designed and fabricated using standard MOS technology. This high Q filter (Q=19) shows excellent control of its frequency response without need for component trimming. These filters occupy small silicon area, and are suitable for the multiplexing of two or more channels. Programmable filters and N-path filters can be realized with this technique.

In this approach ratioed MOS capacitors and MOS operational amplifiers are used to realize direct form biquadratic sections. These can be configured to implement any type of sampled-data filter response.

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Last, but not least, I wish to show my deepest appreciation to my parents by dedicating this dissertation to them.

## TABLE OF CONTENTS

	Page Nos.
CHAPTER 1 INTRODUCTION	1
CHAPTER 2 THE SWITCHED-CAPACITOR ANALOG SAMPLED-DATA RECURSIVE FILTER	5
Introduction	5
2.1 Sampled-data/Discrete-Time Filtering	11
2.2 The Switched-Capacitor Precision Analog Delay	11
2.2.1 Circuit Description	11
2.2.2 Practical Aspects to Integration of the Precision Analog Delay	16
2.3 Switched-Capacitor Implementation of an Analog Sampled-data Recursive Filter Second Order Section (Biquadratic)	27
2.3.1 A Four Amplifier Second Order Section	27
2.3.2 The Three Amplifier Second Order Section with Full Biquadratic Transfer Function	30
2.3.3 The Two Amplifier Second Order (bandpass) Section	38
CHAPTER 3 DESIGN CONSIDERATIONS FOR ANALOG SAMPLED-DATA RECURSIVE FILTERS USING THE SWITCHED-CAPACITOR SECOND ORDER SECTION (BIQUADRATIC)	44
Introduction	44
3.1 Sampled-data (discrete-time) Filter Design from the Analog Prototype Using Frequency Plane Mapping Transformations	45
3.2 Sensitivity and Accuracy Considerations	58
3.3 Parameter Design for Second Order Lowpass, Bandpass and Highpass Filters	65
3.3.1 General Theory	65
3.3.2 Design Parameters for the Monolithic Filters on the Experimental Test Chip	71
3.4 High Order Filter Design Examples	78
3.4.1 6th Order Elliptic Lowpass Filter	78
3.4.2 10th Order Chebyshev Bandpass Filter	92
CHAPTER 4 DESIGN OF THE COMPONENTS IN A FULLY INTEGRATED SWITCHED-CAPACITOR RECURSIVE FILTER	113
Introduction	113
4.1 Design of Precision Non-Binary Capacitor Ratios	113
4.2 An Internally Compensated High Gain NMOS Operational Amplifier	121
4.2.1 Process Description	126
4.2.2 The Input Stage	127
4.2.3 Source Follower Level Shift	129
4.2.4 Second Gain Stage	131
4.2.5 Output Stage	134
4.2.6 $V_T$ Insensitive Biasing	134
4.2.7 Simulated Performance	137
4.2.8 Additional Improvements to the Amplifier	137
4.3 Clock Feedthrough Cancellation	152
CHAPTER 5 PROTOTYPE FILTER TEST CHIP RESULTS	157
Introduction	157
5.1 NMOS Amplifiers	162
5.1.1 Version 1 Amplifier	162
5.1.2 Version 2 Amplifier	162
5.2 Ratioed Capacitor Accuracy	166
5.3 Clock Feedthrough Effects	172
5.4 Programmable Biquadratic Filter	174
5.4.1 Filter Responses	174
5.4.2 Filter Frequency Response Accuracy	179
5.4.3 Dynamic Range Performance	179
CHAPTER 6 CONCLUSIONS	183
APPENDIX I N-CHANNEL MOS ALUMINUM GATE PROCESS	185
APPENDIX II MOSFET DEVICE EQUATIONS AND SMALL SIGNAL PARAMETERS	190
3.5 Practical Considerations for Monolithic Switched-Capacitor Recursive Filters	99
3.5.1 Coefficient Error	99
3.5.2 Dynamic Range Considerations	101
3.5.3 Second Order Practical Considerations	111

CHAPTER 1

INTRODUCTION

Signal processing frequency selective circuits form a very large and expensive part of electronic communication and control systems. As large scale integration techniques become the driving force behind the introduction of the new and more sophisticated electronic systems, the need for a low cost and reliable method of implementing precision filters becomes increasingly important. Single-chip monolithic filters without external trimming are desirable to meet this need. If efficiently realized monolithically, they would also open the door for a new era of large scale integration, one that provides complete electronic systems on a single silicon chip.

Conventional active filters [40] [41] employ a combination of the monolithic bipolar technology to realize operational amplifiers, and thin film technology to realize capacitors and resistors. External laser trimming is used to achieve the desired frequency response. While being a significant advance over discrete component passive filters, these active filters do not fulfill the above requirements and are not appropriate for large scale integration of analog-digital subsystems and systems.

Digital filtering techniques are still unattractive for these applications because analog-to-digital (A/D) and digital-to-analog (D/A) conversions need to be performed with 12 to 14 bit accuracy, and/or high speed, in order to achieve a reasonable dynamic range. Currently it is difficult to realize a fully integrated digital filter incorporating A/D and D/A conversions with the necessary speed or accuracy all on the one monolithic chip.

APPENDIX III	MOSFET MODEL PARAMETERS FOR OPERATIONAL AMPLIFIER SIMULATION	194
APPENDIX IV	PROGRAM DINAP	197
APPENDIX V	SAMPLED-DATA RECURSIVE STRUCTURES WITH LOW COEFFICIENT SENSITIVITIES	199
APPENDIX VI	ANALOG NMOS SAMPLED-DATA RECURSIVE FILTER	204
APPENDIX VII	AN IMPROVED SWITCHED-CAPACITOR INTEGRATOR	207
APPENDIX VIII	SWITCHED-CAPACITOR FILTER SECTIONS IMPLEMENTING THE BILINEAR Z-TRANSFORMATION	210
REFERENCES		215

Analog sampled-data filters do not require these high accuracy A/D and D/A converters because they process the input analog signal directly and eliminate the problems of signal quantization. The use of charge-transfer-devices (CTDs) to implement transversal filters [3] [42] had been the most promising approach for monolithic filters up until the commencement of the work contained in this dissertation. However, since CTD transversal filters have only zeros of transmission (no poles) in their transfer function, they are relatively inefficient in their use of silicon area when implementing simple frequency responses with high Q or sharp transitions in magnitude. CTDs have a dark current which causes a decrease in dynamic range and a dc offset which at high temperatures and low frequencies (below 500 Hz) becomes a limitation on their performance. Also split-electrode CTD transversal filters have a substantial insertion loss due to the signal sensing technique which amounts to 20-30 dB in typical filters. This loss results in a degradation in signal-to-noise ratio of a fully integrated filter by that same factor, compared to a zero-insertion loss filter.

The objective of this research has been to investigate whether analog sampled-data recursive filters can be fully integrated efficiently in MOS technology. Analog sampled-data recursive filters have been described previously; but these employed many off-chip precision components [43] [44] [45].

The results of this work have shown that monolithic recursive filters can be implemented using analog sampled-data techniques which do not have the above disadvantages. Precise frequency responses are achievable without external trimming, and are controlled simply by ratioed MOS capacitors "switched" under the control of a single precise

system clock. The output signal voltage in these recursive filters can be sensed directly, instead of capacitively as with CTDs, resulting in a larger signal and thus significantly relaxing the requirements on the noise performance of the amplifiers. The inherently small leakage current at critical nodes in these filters means that this filtering technique can be used at low frequencies.

Chapter 2 of this dissertation describes the novel way of achieving the functions required to do analog sampled-data recursive filtering using only analog switches, capacitors and relatively low performance operational amplifiers. It will be seen that MOS technology is particularly well suited for implementing these filters for the following reasons: the high density of MOS components (e.g. MOS operational amplifiers can be 3-5 times smaller than their bipolar counterparts); the high precision and stability with which filter coefficients can be derived using ratios of capacitor values; and the essentially ideal characteristics of MOSFET switches. In this chapter the biquadratic section (2 poles and 2 zeros) is realized as a general purpose building block for second and higher order sampled-data filters.

Chapter 3 goes into the ways of designing lowpass, bandpass, and highpass filters using the switched-capacitor analog sampled-data biquadratic section. Consideration is also given to the practical aspects of the integrated circuit implementation.

The design of the basic components for a fully integrated prototype filter in single-channel aluminum gate MOS technology is presented in Chapter 4. This includes ratioed capacitors having maximum precision without trimming, and a high gain, low power, small area MOS operational amplifier.

Chapter 5 contains results from a fully integrated biquadratic sampled-data prototype filter. This circuit could be electrically programmed to provide a high  $Q(Q=19)$  lowpass, bandpass or highpass frequency response.

Chapter 6 presents the conclusions of this research work.

## CHAPTER 2

### THE SWITCHED-CAPACITOR ANALOG SAMPLED-DATA RECURSIVE FILTER

#### Introduction

The design and analysis of switched-capacitor analog sampled-data recursive filters makes use of the large body of discrete time signal processing theory that has been applied to digital filters [1,2], and more recently to charge transfer device filters [3]. This chapter shows how the functions necessary for analog discrete-time (sampled-data) signal processing (filtering) can be implemented in a monolithic form by means of ratioed switched MOS capacitors and operational amplifiers. These function blocks are then connected together to realize a second order transfer function that can have both poles and zeros (a general biquadratic transfer function). Three different ways of configuring the switched-capacitors and operational amplifiers to simulate the direct-form second-order recursive section are presented and discussed together with the practical aspects of this switched-capacitor recursive filter.

#### 2.1 Sampled-Data/Discrete-Time Filtering

The first step in discrete-time filtering is the sampling of a continuous-time input waveform at a rate greater than the Nyquist rate of twice the highest frequency in the signal. If the original signal is not appropriately bandlimited, lowpass filtering prior to sampling is needed to prevent aliasing.

Much of the literature on digital signal processing is actually applicable to discrete-time (sampled-data) signal processing without quantization of the signal amplitudes. Therefore it will be called upon freely in the description and analysis of the sampled-data

switched-capacitor filtering concepts presented in this dissertation.

The general form for the transfer function of a recursive filter of  $N$ th order in the usual  $z$ -transform notation is:

$$H(z^{-1}) = \frac{\sum_{i=0}^N \alpha_i z^{-i}}{1 + \sum_{i=1}^N \beta_i z^{-i}}, \quad 2.1$$

where  $z^{-1}$  is the unit delay operator.

The roots of the polynomial in the numerator provide the zeros of the transfer function and the roots of the denominator its poles. Unless the numerator polynomial is exactly divisible by the denominator polynomial, equation 2.1 has an impulse response of infinite duration and is classified as a Finite Impulse Response (FIR) filter.

Transversal filters, which are a subset of recursive filters, where all  $\beta_i = 0$ , are Finite Impulse Response Filters.

A great variety of structural realizations of equation 2.1 is possible. Three canonical forms are most often employed in digital filters. These forms are canonical in the sense that a minimum number of adders, multipliers, and delays is required to realize equation 2.1 in the general case. The first of these forms, shown in Figure 2.1, is called the direct form. This form is usually avoided if poles are tightly clustered, corresponding to a narrow bandpass filter or a sharp-cutoff lowpass or highpass filter, since then the poles of the direct-form realization are quite sensitive to error in the feedback coefficients  $\{\beta_i\}$   $\{\beta_i\}$  (i.e. small errors in the coefficients can cause large shifts of the poles).

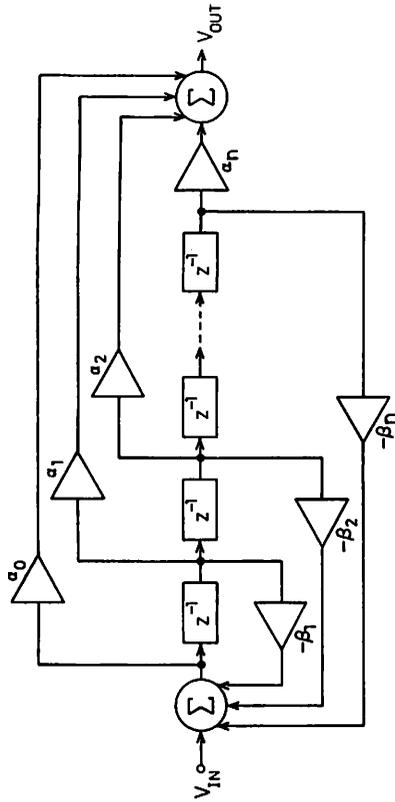


Figure 2.1: The direct form for a discrete-time filter.

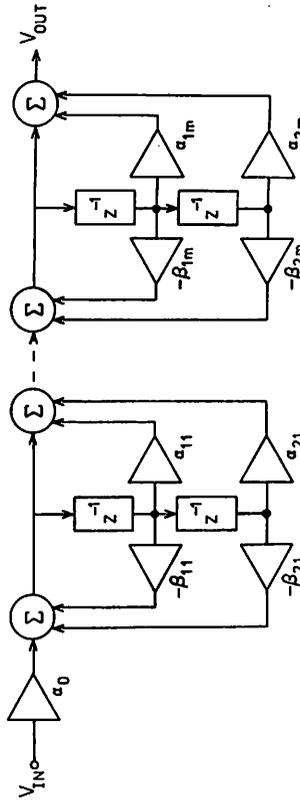


Figure 2.2: The cascade form for a discrete-time filter.

The second canonical form corresponds to a factoring of the numerator and denominator polynomials of equation 2.1 to produce an  $H(z^{-1})$  of the form;

$$H(z^{-1}) = \alpha_0 \prod_{i=1}^m \frac{\alpha_{2i} z^{-2} + \alpha_{1i} z^{-1} + \gamma_{1i}}{\beta_{2i} z^{-2} + \beta_{1i} z^{-1} + 1} \quad 2.2$$

Where  $m$  is the integer part of  $\frac{(n+1)}{2}$ . This is the cascade form for a digital filter depicted in Figure 2.2. Second-order factors (with real coefficients) have been chosen for equation 2.2 rather than a mixed set of first and second-order factors for real and complex roots. This is to simplify the implementation of the cascade form, especially when multiplexing is employed.

The third canonical form is the parallel form, shown in Figure 2.3, which results from a partial fraction expansion of equation 2.1 to produce;

$$H(z^{-1}) = \gamma_0 + \sum_{i=1}^m \frac{\gamma_{1i} z^{-1} + \gamma_{0i}}{\beta_{2i} z^{-2} + \beta_{1i} z^{-1} + 1} \quad 2.3$$

Where  $\gamma_0 = \frac{a_n}{b_n}$  and again all second order (denominator) factors have been chosen. Note that all three canonical forms are entirely equivalent with regard to the amount of storage required ( $n$  unit delays) and the number of arithmetic operations required ( $2n+1$  multiplications and  $2n$  additions per sampling period).

Another filter form which offers some advantages in the sensitivity performance of high order filters is the Multiple Feedback Structure (MFB) [5,6,7]. This is shown in Figure 2.4. The transfer functions  $T_i(z^{-1})$  are of the form;

$$T_i(z^{-1}) = \frac{\alpha_{0i} + \alpha_{1i} z^{-1} + \alpha_{2i} z^{-2}}{1 + \beta_{1i} z^{-1} + \beta_{2i} z^{-2}} \quad 2.4$$

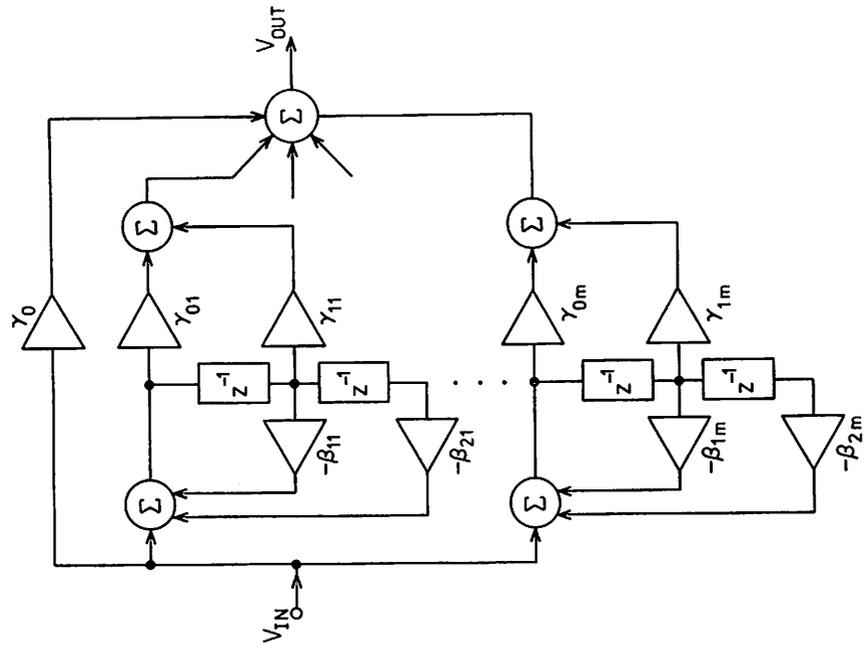


Figure 2.3: The parallel form for a discrete-time filter.

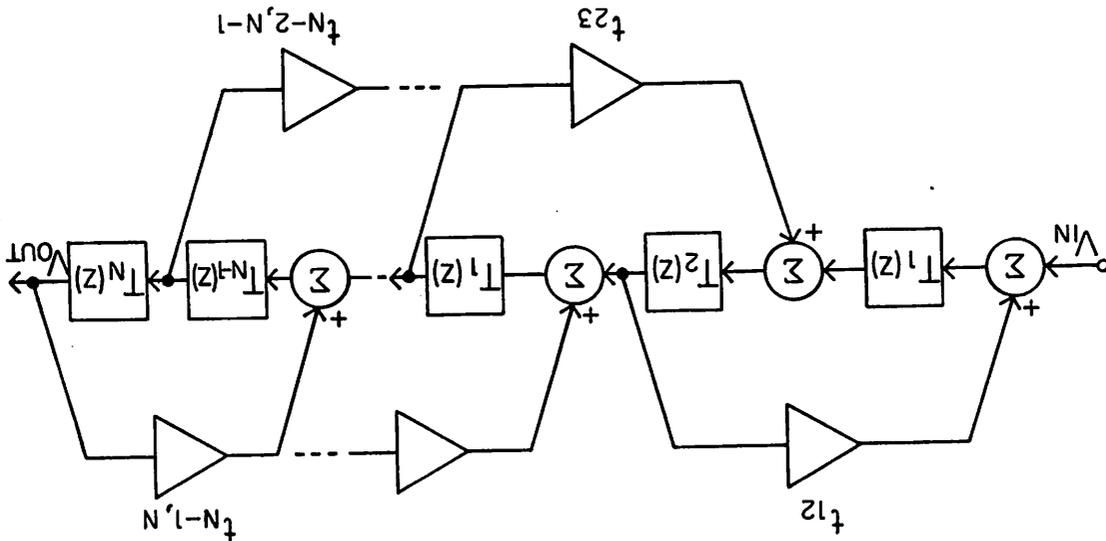


Figure 2.4: Multiple Feedback configuration.

and are realized by first or second order sections. For lowpass filters the basic block  $T_1(z^{-1})$  is first order, while for bandpass filters the basic block is a second order section.

The Follow-the-Leader Feedback (FLF) Configuration is another [8,9,10] structure that is useful for the design of low sensitivity, geometrically symmetrical, bandpass filters. This structure is shown in Figure 2.5. The transfer functions  $T_i(z^{-1})$  can be either the general biquadratic function of equation 2.4 [8,10] or the bandpass biquadratic function [9] of the form;

$$T_i(z^{-1}) = \frac{Y_{0i} + Y_{1i}z^{-1}}{1 + B_{1i}z^{-1} + B_{2i}z^{-2}} \quad 2.5$$

The former one removes the need for the output summing amplifier and all its associated weighted paths, i.e.  $a_i$ 's are not needed. The output is taken from  $T_n(z^{-1})$ .

It can be seen that the general biquadratic function (second order section) forms a basic building block in the realization of discrete-time filter transfer functions. The sections that follow in this chapter take one through the development of a monolithic means of implementing these second order building blocks (used in Figures 2.2, 2.3, 2.4, and 2.5). This enables any filter transfer function to be integrated on an MOS chip using switched-capacitors and MOS operational amplifiers.

2.2 The Switched-Capacitor Precision Analog Delay

2.2.1 Circuit Description

The circuit shown in Figure 2.6 can be implemented using two MOS

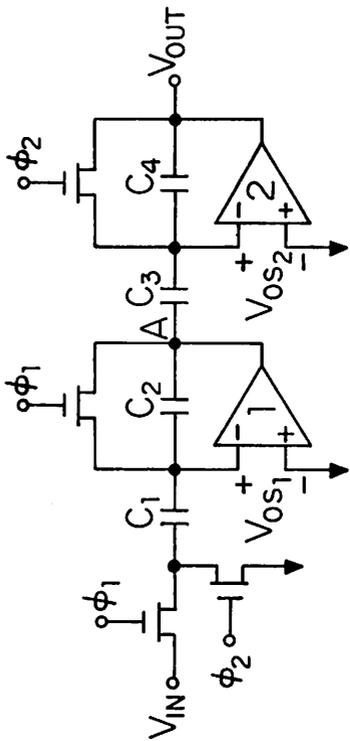
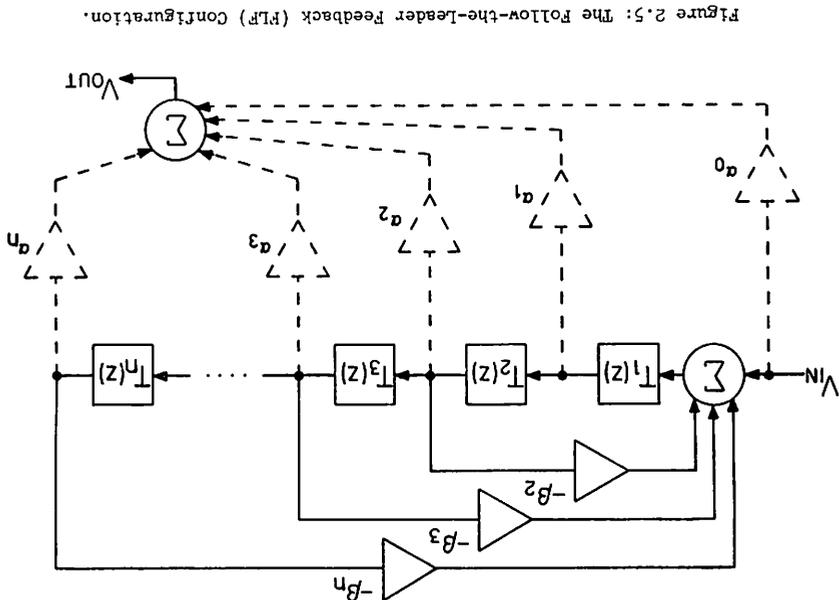


Figure 2.6.a: Precision analog discrete-time delay element with input multiplication.

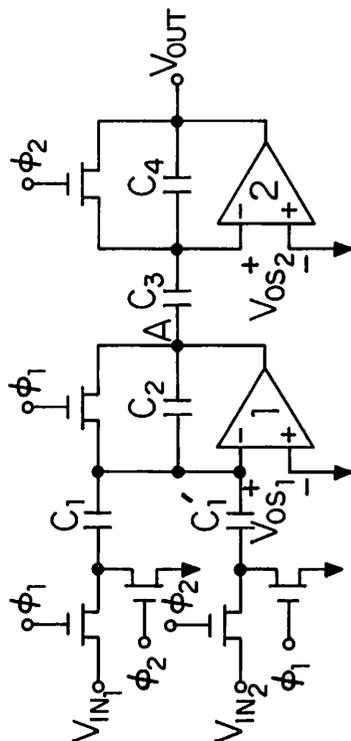


Figure 2.6.b: Precision analog discrete-time delay element with input multiplication and differencing ( $V_{IN} - V_{IN_2}$ ).

op. amps, four MOS switches and two pairs of ratioed MOS capacitors to realize a precision analog delay and multiply. Under the control of a two phase clock ( $\phi_1, \phi_2$ ), derived from a crystal controlled system clock, this circuit will transfer the input voltage, sampled at time "nT," to the output with one clock period of delay time "T." In the same interval this signal will have been multiplied by the ratio  $\frac{C_1}{C_2} \cdot \frac{C_3}{C_4}$ . The time constants formed by the capacitors and switches "ON" resistance are assumed always to be much smaller than the phase intervals. The sequences of events in the periodically clocked circuit is as follows:

During phase one when signal  $\phi_1$  is high\* and  $\phi_2$  is low, amplifier one is placed in unity gain and its inverting input is therefore held at virtual ground. While  $\phi_1$  is high, capacitor  $C_1$  has voltage  $V_{IN}(t)$  across it. The charge in  $C_1$  during phase one is  $Q_{C_1} = C_1 V_{IN}(t)$  and in  $C_2$ ,  $Q_{C_2} = 0$ , where  $t = nT$  at the end of  $\phi_1$ . In the second phase, when  $\phi_2$  is high and  $\phi_1$  is low, the input side of  $C_1$  is driven to ground and the charge in  $C_1$  redistributes into  $C_2$ . Thus during phase two, after all transients have settled out,  $Q_{C_1} = 0$ ,  $Q_{C_2} = C_1 V_{IN}(nT) = C_2 V_A$ .

At this time, the voltage present at the output of amplifier one is  $\frac{C_1}{C_2} V_{IN}(nT)$ . All the time during phase two, amplifier two is in unity gain and its inverting input is at virtual ground. Therefore capacitor  $C_3$  has voltage  $\frac{C_1}{C_2} V_{IN}(nT)$  across it and  $Q_{C_3} = C_3 \cdot \frac{C_1}{C_2} V_{IN}(nT)$ ,  $Q_{C_4} = 0$ .

\* The high voltage is equal to  $V_{DD}$  (positive supply for the op. amps.) low voltage is equal to  $V_{SS}$  (negative supply for the op. amps.)  
 -- enough positive gate voltage to maintain the analog switch in a low resistance state (ON) for all analog signals, and enough negative gate voltage to keep the analog switch in a high resistance state (OFF) for all analog signals.

When  $\phi_1$  goes high again, which is one clock period later than the beginning of the first  $\phi_1$  interval, the charge redistributes from  $C_3$  into  $C_4$  and  $Q_{C_3} = 0$ ,  $Q_{C_4} = C_3 \cdot \frac{C_1}{C_2} V_{IN}(nT) = C_4 V_{OUT}(nT+T)$ . This voltage at the output of the second amplifier is then  $\frac{C_1}{C_2} \cdot \frac{C_3}{C_4} V_{IN}(nT)$ . Since one clock period has occurred during this time, the signal at the output has been delayed one unit of time T and can be represented as:

$$V_{OUT}(nT+T) = \frac{C_1}{C_2} \cdot \frac{C_3}{C_4} V_{IN}(nT) \quad 2.6$$

In terms of the delay operator ( $z^{-1}$  notation) the transfer function is

$$\frac{V_{OUT}}{V_{IN}} = \frac{C_1}{C_2} \cdot \frac{C_3}{C_4} z^{-1} \quad 2.7$$

In this precision analog multiply and delay, the multiplication is controlled with the accuracy of the capacitor ratios  $\frac{C_1}{C_2} \cdot \frac{C_3}{C_4}$ , provided the amplifier gain is high enough, such that amplifier gain error is insignificant compared to capacitor ratio error. More precisely this can be seen from:

$$\frac{V_{OUT}}{V_{IN}} = \alpha_1 \alpha_2 z^{-1} \quad 2.8$$

where

$$\alpha_1 = \frac{\frac{C_1}{C_2}}{\frac{C_1+C_2}{A_1 C_2} + 1} ; \alpha_2 = \frac{\frac{C_3}{C_4}}{\frac{C_3+C_4}{A_2 C_3} + 1}$$

$A_1$  and  $A_2$  are the gains of each amplifier.

This circuit also has summing or differencing capability. Extra input signals can be summed simply by adding one more capacitor and two MOS switches to the inverting input of amplifier one and connecting them in the same manner as  $C_1$  in Figure 2.6a. If these switches are operated in the same sequence as the other input (in phase), the circuit performs summation. If these switches are operated with opposite phasing as shown in Figure 2.6(b), the circuit performs differencing

$$i.e. \quad V_{OUT} = [V_{IN1} z^{-1} - V_{IN2}] \frac{C_1}{C_2} \cdot \frac{C_3}{C_4} \quad 2.9$$

Thus the circuit of Figure 2.6 performs the function of delay (controlled by the system clock), multiplication (controlled by the capacitor ratios  $\frac{C_1}{C_2} \cdot \frac{C_3}{C_4}$ ) and summation or differencing, depending on the phasing of the clocks which control the input switches.

So far in this analysis of the precision delay element, it has been assumed that the op. amps. are ideal (no offset, infinite gain), the MOS delay switches are ideal and the signal nodes in the circuit do not have any parasitics to consider. The nonidealities in the MOS integration of the delay element and their effects will be considered next.

#### 2.2.2. Practical Aspects to Integration of the Precision Delay

The integration of the precision analog delay element with MOS technology makes this element very attractive. This is because the circuit is highly insensitive to many of the nonidealities that are present in the MOS implementation. The high input impedance (virtually ideal) of the MOS operational amplifier is a primary factor for the

usefulness of this technology for realizing the delay function. The following nonidealities will be considered: op. amp. offset, op. amp. finite gain, parasitic capacitances (overlap capacitance of the analog MOS switches, parasitic capacitances connected to signal nodes), junction leakage at the op. amp's inverting input, noise and distortion from the op. amp.

#### A. Operational Amplifier Input Offset.

Small input offsets for the op. amp. do not produce any harmful error in the performance of the precision delay and multiply element. This can be seen from the following analysis based on the circuit in Figure 2.6a and assuming that steady state conditions are reached.

At the end of interval  $\phi_1$ ,  $t = nT$ :

$$\text{Charge in } C_1 \text{ is } Q_{C_1} = C_1 [V_{IN}(nT) - V_{OS_1}]$$

$$\text{Charge in } C_2 \text{ is } Q_{C_2} = 0$$

During interval  $\phi_2$ :  $Q_{C_1} = -C_1 V_{OS_1}$

$$Q_{C_2} = C_1 [V_{IN}(nT)] = C_2 V_A$$

$$Q_{C_3} = C_3 [V_A - V_{OS_2}]$$

$$Q_{C_4} = 0$$

At the end of interval  $\phi_1$ ,  $t = nT + T$ :

$$Q_{C_1} = C_1 [V_{IN}(nT+T) - V_{OS_1}]$$

$$Q_{C_2} = 0$$

$$\begin{aligned}
 C_{C_4} &= C_3[V_A - V_{OS_2}] - C_3[V_{OS_1} - V_{OS_2}] = C_4 V_{OUT}(nT+T) \\
 &= C_3 \left[ \frac{C_1}{C_2} V_{IN}(nT) - V_{OS_1} \right] = C_4 V_{OUT}(nT+T) \\
 \therefore V_{OUT}(nT+T) &= \frac{C_1}{C_2} \cdot \frac{C_3}{C_4} V_{IN}(nT) - \frac{C_3}{C_4} V_{OS_1}
 \end{aligned}$$

then

$$V_{OUT}(t) = \frac{C_1}{C_2} z^{-1} V_{IN}(t) - V_{OS_1} \tag{2.10}$$

This result shows that the effect of amplifier input offset voltage is to shift the signal with a constant D.C. voltage equal to the offset voltage of the amplifier. Thus there is no detrimental effect for small (<100 mV) input offsets.

B. Finite Open Loop Gain of the Amplifier

Finite open loop gain of the amplifier causes a reduction in the multiplying constant of the precision analog delay. This error is described by equation 2.8.

However, provided the gain stays constant, this gain error can be corrected by modifying the capacitance ratio such that after the finite gain is included in the multiplying constant calculation, the resultant  $\alpha$  is the required value. The important consideration therefore is, how much does the multiplying constant  $\alpha$  change due to changes in the open loop gain of the amplifier. That is, what is the sensitivity of

$\alpha$  to amplifier gain A ( $S_{A_1}^{\alpha_1}$  or  $S_{A_2}^{\alpha_2}$ )?

$$\text{If } \alpha = \frac{\frac{C_1}{C_2}}{\frac{C_1+C_2}{AC_2} + 1}$$

then

$$\frac{d\alpha}{dA} = \frac{\alpha}{A} = \frac{\frac{C_1}{1 + \frac{C_1}{C_2}}}{1 + \frac{C_1}{C_2}}$$

$$= \frac{C_1}{A} \text{ for } A \gg \frac{C_1}{C_2} \tag{2.11}$$

Thus if the open loop gain of amplifier is 100 and it does not change by more than 10% due to processing variations, then assuming  $\frac{C_1}{C_2} = 2$  for example, the change in  $\alpha$  will be 0.3%. The conclusion is that high open loop gain of the amplifier is not the most important factor in producing highly reproducible multiplying constants for the precision delay. More important is how well the absolute value of the closed loop gain can be controlled.

C. Parasitic Capacitances (Figure 2.7)

Since there is "overlap capacitance" between gate and source and gate and drain in the MOS transistor switches, a portion of the clock signal will feedthrough, in the form of charge, onto the inverting input of each amplifier where it remains and produces a D.C. voltage at the output. The amount of feedthrough charge is determined by the

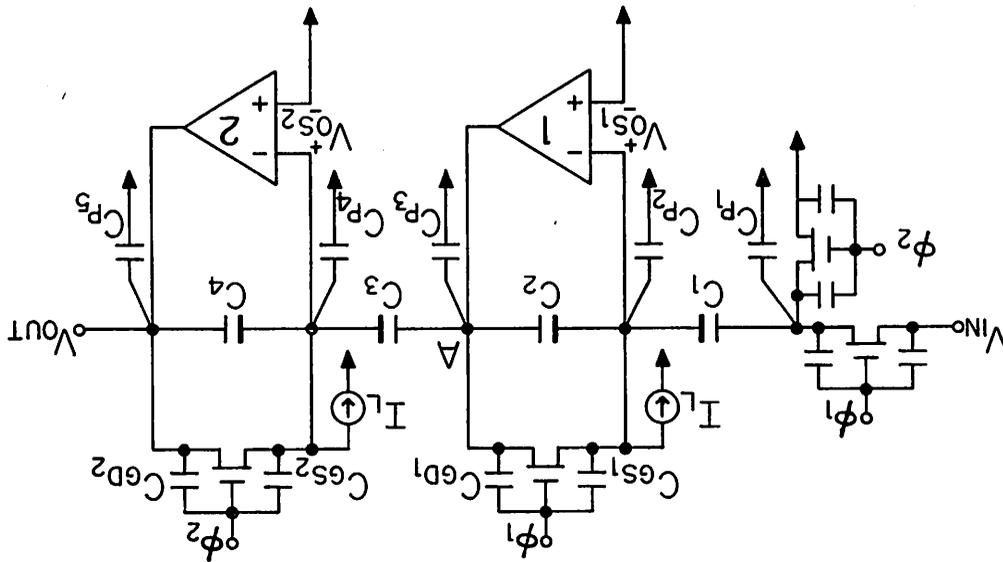
clock signal swing ( $V_{clock}$ ), the nonlinear capacitance  $C_{GS}$  between gate and source of the feedback switch (Figure 4.17), and the feedback capacitance ( $C_2$ ) between output and inverting input. Since the maximum positive excursion of the clock voltage is much larger than the transistor threshold voltage  $V_T$ , the average value of  $C_{GS}$  during device turn-off will be  $\frac{C_{OX}}{2}$ . All these factors are approximately constant with the operation of the circuit. The effect of clock feedthrough is to produce a constant D.C. offset in the signal at the output of the precision delay. For amplifier one in Figure 2.7:

$$V_{OUT,DC} = \frac{C_{GS}}{C_2} V_{clock} \quad 2.12$$

A very significant feature of the precision delay is that it is insensitive to any of the parasitic capacitances from signal nodes to ground (i.e. input, output,  $V_A$  or the inverting inputs to the amplifiers).

First note that each amplifier maintains its inverting input at virtual ground after steady state is reached during each of the two phase intervals. Thus from one phase interval to the next there is no change in the charge stored in the nonlinear capacitances  $C_{P2}$  and  $C_{P4}$ . This means that there is no loss of signal charge as it is clocked through the capacitors in the circuit. All other nodes in the circuit are driven by either the output impedance of the MOS amplifier (typically 1 k $\Omega$ ) or the "ON" resistance of an MOS switch (typically 2 k $\Omega$  for a minimum size device). The MOS capacitors might only be as large as 10 pF and therefore the time constants involved are typically 20 ns. The parasitic capacitances  $C_{P1}$ ,  $C_{P3}$ , and  $C_{P5}$  are charged and discharged by a voltage source in series with the MOS switch or the low output

Figure 2.7: Parasitic elements in the precision analog delay. ( $I_L$  is the leakage current to substrate from the reverse biased junction)



impedance of an amplifier, and this presents no problem.

D. Junction Leakage Current

Since the input, output and  $V_A$  nodes are always driven by either a voltage source in series with an MOS switch, or the low output impedance of an MOS amplifier, leakage current across pn junctions has no effect on the signal at these nodes. The other nodes to consider are the amplifier inverting inputs. The only source of leakage current at these nodes arises from the source junction area of the minimum size MOS switch connected to this node. However since the inverting input node is always held at virtual ground in the steady state, and the transient time is very small compared to the phase interval, the leakage current will remain constant. During the phase interval when the feedback switch is off there will be a constant leakage of positive charge from the inverting input side of  $C_2$  (or  $C_4$ ) -- this is the common plate of the MOS capacitors. The effect seen at the amplifier output is the signal voltage rising positively at a constant rate. Since the operation of the switched-capacitor circuit is only concerned with the voltage at the instant of time marked by the end of the half clock period, there will be a constant amount of charge loss from  $C_2$  due to constant leakage to the substrate, independent of the signal voltage. Therefore there is a constant D.C. voltage shift (offset) in the output signal through the precision delay:  $V_{DC} = \frac{I_L T}{C}$  where  $I_L$  is the leakage current, T is the clock period and C is the feedback capacitance value.

E. Noise.

The switched-capacitor precision analog delay has two sources of

noise. The first and usually more dominant source of noise at the delay output is the voltage noise of the MOS amplifiers. If a delay in the analog signal of one half a clock period ( $\frac{T}{2}$ ) is represented in z transform notation as  $z^{-1/2}$ , then the average noise at node A is (refer to Figure 2.8);

$$\bar{V}_A = \left\{ \left[ \frac{C_1}{C_2} \bar{v}_{n_1} z^{-1/2} \right]^2 + \left[ \left( 1 + \frac{C_1}{C_2} \right) \bar{v}_{n_1} \right]^2 \right\}^{1/2} \quad 2.13a$$

due to sampling during phase  $\bar{v}_{n_1}$  during phase  $\bar{v}_{n_1}$  during phase  $\bar{v}_{n_1}$  during phase  
one  
two

where  $\bar{v}_{n_1}$  and  $\bar{v}_{n_2}$  are the total effective rms noise sources referred to each amplifier's input. The total effective noise at the output follows from equation 2.12 (note that  $\bar{v}_{n_1} z^{-1/2} = \bar{v}_{n_1}$  since noise is uncorrelated).

$$\bar{V}_{OUT_n}^2 = \left( \frac{C_3}{C_4} \right) \left\{ \left( \frac{C_1}{C_2} \bar{v}_{n_1} \right)^2 + \left[ \left( 1 + \frac{C_1}{C_2} \right) \bar{v}_{n_1} \right]^2 + \bar{v}_{n_2}^2 \right\} + \left[ \left( 1 + \frac{C_3}{C_4} \right) \bar{v}_{n_2} \right]^2$$

if  $\frac{C_3}{C_4} = 1$

$$\bar{V}_{OUT_n}^2 = \left( \frac{C_1}{C_2} \bar{v}_{n_1} \right)^2 + \left[ \left( 1 + \frac{C_1}{C_2} \right) \bar{v}_{n_1} \right]^2 + \bar{v}_{n_2}^2 + 4\bar{v}_{n_2}^2 \quad 2.13b$$

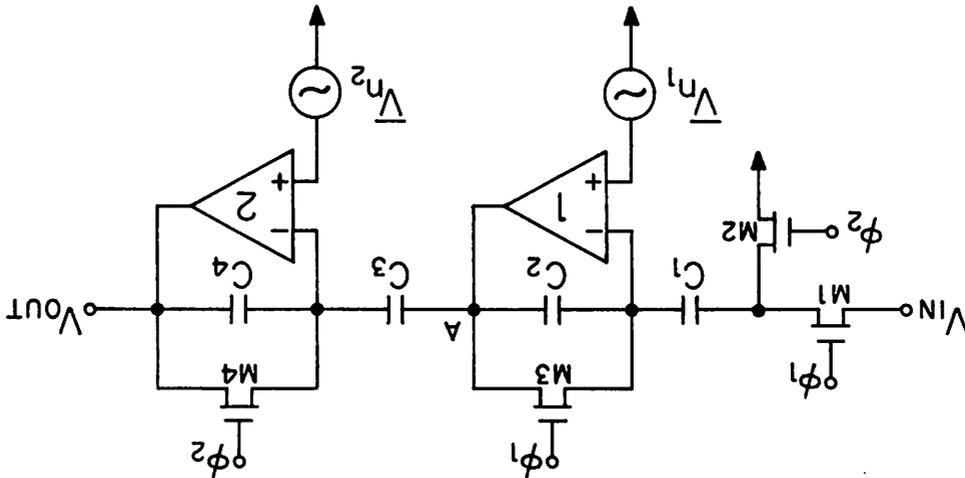
And if  $\frac{C_1}{C_2} = 2.0$  (for example a practical worst case).

$$\bar{V}_{OUT_n}^2 = 4\bar{v}_{n_1}^2 + 9\bar{v}_{n_1}^2 + \bar{v}_{n_2}^2 + 4\bar{v}_{n_2}^2$$

Since the amplifiers are identical  $\bar{v}_{n_1}^2 = \bar{v}_{n_2}^2$

$$\begin{aligned} \bar{V}_{OUT_n} &= 4.24\bar{V}_{n_1} \\ \text{or } \bar{V}_{IN_n} &= 2.12\bar{V}_{n_1} \quad \left(\frac{C_1}{C_2} = 2.0\right) \end{aligned}$$

Figure 2.8: Amplifier Noise Sources in the Precision Analog Delay.



The second source of noise arises from the switched-capacitors. The capacitance shunts the thermal noise from the MOS switches. In the delay circuit (Figure 2.8) the noise is the thermal noise from the MOSFET switch resistance of M3 and M4 (Figure 2.8). These MOSFETs are shunted by  $C_2$  and  $C_4$  respectively, which limit the total thermal noise contribution from each MOSFET to  $\sqrt{\frac{kT}{C_2}}$  and  $\sqrt{\frac{kT}{C_4}}$  respectively [25]. Capacitor  $C_1$  also introduces some capacitively shunted thermal noise with MOSFET's M1 and M2. However, since the unity gain bandwidth of the amplifier is at least an order of magnitude less than the cut-off frequency of the thermal noise ( $\omega_c = \frac{1}{R_M C_1}$  where  $R_M$  is the MOSFET "ON" resistance), these MOSFETs make a negligible contribution to the total effective noise at the output of the switched capacitor delay circuit. For a MOSFET "ON" resistance of 2 k $\Omega$  and  $C_1 = 5$  pf, the cut-off frequency would be 100 MHz. The MOSFET amplifier can have a unity gain frequency between 2 and 5 MHz, typically 3 MHz.

When the MOSFETs are "OFF" they are in a very high impedance state, thus the cut-off frequency reduces to a very low frequency in this case, and the noise voltage ( $\frac{kT}{C}$ ) becomes almost equivalent to a DC offset voltage.

If  $\frac{C_3}{C_4} = 1$  the total rms noise voltage at the output of the switched-capacitor delay in Figure 2.8 becomes;

$$\bar{V}_{OUT_n} = \left( \frac{kT}{C_2} + \frac{kT}{C_4} \right)^{1/2} \quad (\text{the sources are uncorrelated})$$

$$= 1.414 \sqrt{\frac{kT}{C_2}} \quad \text{if } C_2 = C_4 \quad 2.14a$$

$$\bar{V}_{IN_n} = \frac{\sqrt{2kT C_2}}{C_1} \quad 2.14b$$

Each of the two MOSFETs M3 and M4 leaves its bandlimited thermal noise in the shunt capacitance at the end of its "ON" phase interval.

For  $C_2 = C_4 = 5 \text{ pf}$

$$\bar{V}_{OUT_n} = 1.414 (29 \mu\text{V}) = 40.6 \mu\text{V rms}$$

$$\text{If } \frac{C_1}{C_2} = 2.0$$

$$\bar{V}_{IN_n} = 20.3 \mu\text{V rms}$$

#### F. Amplifier Transient Limitations

The maximum clock frequency for the MOS switched capacitor filter is determined by the settling time characteristics of the MOS amplifiers. Any error in the settling of the analog signal to its steady state level (after the feedback switch has opened the unity gain loop), cannot be distinguished from error in the multiplying constant  $\left(\frac{C_1}{C_2}\right)$  for example). The transient settling time of the amplifiers during each phase interval must be within the accuracy desired for the multiplying constant that this switched-capacitor circuit is realizing. For example if  $\pm 0.1\%$  accuracy on multiplying constants is required, then the amplifiers must settle to within  $\pm 0.1\%$  of the steady state

value (which is  $\frac{C_1}{C_2} V_{IN}$  for example) in each phase interval.

Typically the unity gain settling time (which is the worst case stability configuration) for the MOS amplifiers, described in Chapter 4, is 3.5 usec for a 4 V input step. This settling time includes both the slewing time (large signal, nonlinear) and the small signal settling time (linear) of the amplifier. The accuracy to which the amplifier settles at the end of each phase interval depends on the open loop gain at the frequency:  $\left[\frac{1}{\text{phase interval time}}\right]$ . Provided that the phase interval is longer than the slewing and settling time of the amplifier, the accuracy in the analog multiplication of low frequencies is determined by the amplifier open loop gain at those frequencies and accuracy for the higher frequency signals is determined by the amplifier gain at the higher frequencies. This is assuming that the amplifiers are always operating in a small signal (linear) transient mode at the end of each phase interval.

#### 2.3 Switched-Capacitor Implementation of an Analog Sampled-Data Recursive Filter Second-Order Section (Biquadratic Block)

##### 2.3.1 A Four Amplifier Second-Order Section

The previous section described the implementation of the three basic functions used in analog sampled-data (discrete time) recursive filters (see Figure 2.9). The functions performed by the precision analog delay element introduced there are shown in block diagram form in Figure 2.10(a). These functions are multiply, sum or difference input, and clock controlled delay. Figure 2.10(b) shows the full switched-capacitor circuit implementation of Figure 2.10(a).

The development of the analog sampled-data functions in switched capacitor form leads directly to a "first version" implementation of

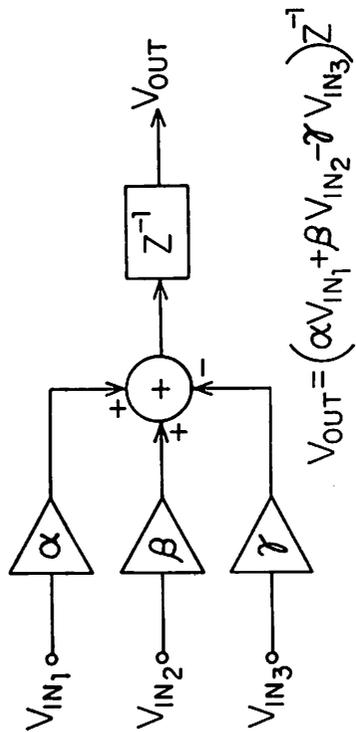


Figure 2.10.a: Block diagram of the precision analog delay with multiplication and summation.

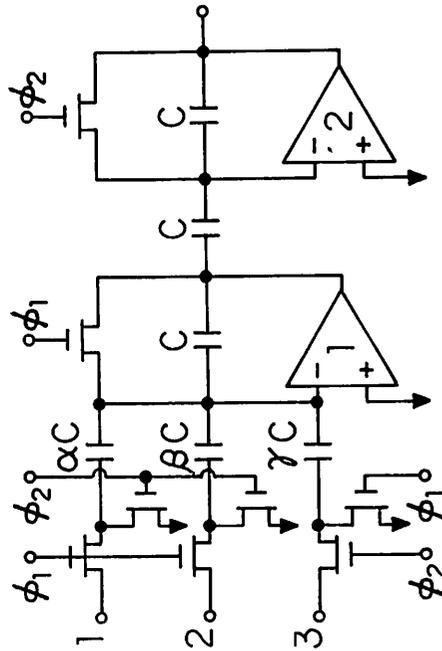


Figure 2.10.b: Complete switched-capacitor circuit implementation of figure 2.10.a.

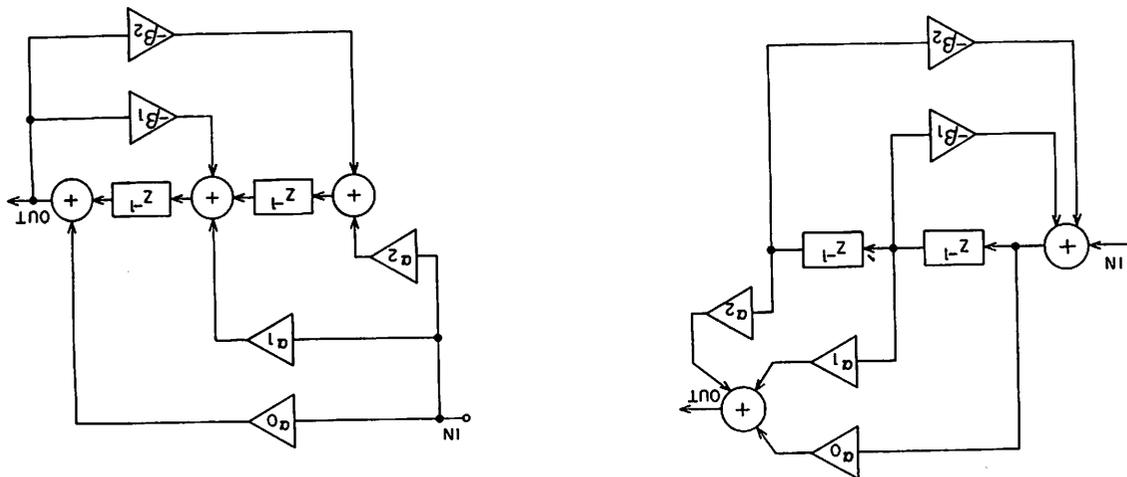


Figure 2.9: Two equivalent configurations for the direct form second order sampled-data recursive filter.

the second-order recursive section that has the topology of Figure 2.9(b). The full "first version" circuit is given in Figure 2.11. This circuit employs two amplifiers per full delay and therefore uses four amplifiers for the complete second order (biquad) section. Note that this biquad section (bandpass) has only one real zero and therefore does not implement the general biquadratic transfer function. An important point about the Figure 2.11 implementation is that all the voltage multiplications which occur in both the feedback and feedforward paths, are positive in sign. Such a restraint tends to make this implementation rather impractical since it has limited stable regions in the frequency plane where the poles can be placed (thus limiting the range of second order transfer functions that can be realized with this circuit). Another disadvantage of this circuit is that it requires four MOS amplifiers (and the necessary analog switches and ratioed capacitors) to implement a transfer function having two poles and one zero;

$$\text{i.e. } H(z^{-1}) = \frac{\alpha^2 a_1 z^{-1}}{1 + \beta_1 z^{-1} + \beta_2 z^{-2}} \quad 2.15$$

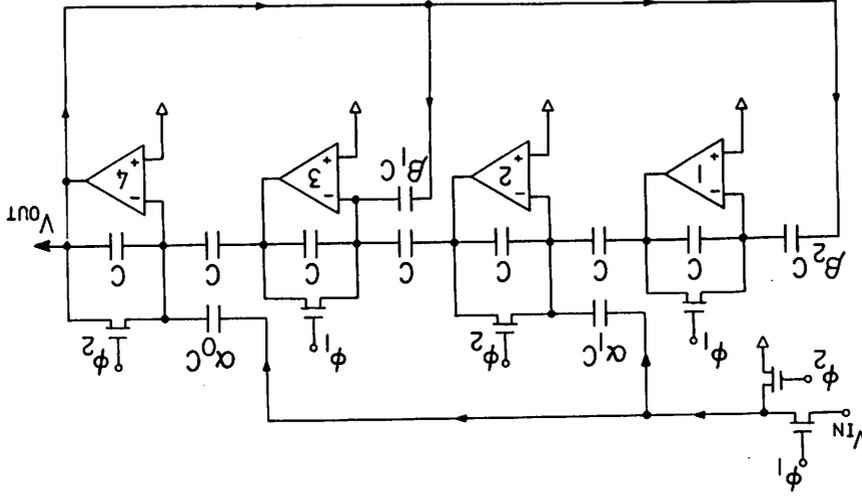
where  $\alpha_0, \alpha_1, \beta_1, \beta_2$  are restricted to positive values.

### 2.3.2 Three Amplifier Second-Order Section with Full Biquadratic Transfer Function

In order to explain the principle behind the operation of a three amplifier section, it is necessary to show how a negative multiply, with a half period of delay, can be realized.

If the circuit in Figure 2.12(a) is operated with M1 controlled by  $\phi_1$  and M2 by  $\phi_2$ , then the circuit functions the same way as the precision delay element in Figure 2.6, except that the delay is only

Figure 2.11: Four Amplifier Second Order Section (Biquad).



one half period ( $z^{-1/2}$ ).

$$i.e. \quad \frac{V_{OUT}}{V_{IN}} = \frac{C_1}{C_2} z^{-1/2} \quad 2.16$$

On the other hand if M1 is controlled by  $\phi_2$  and M2 by  $\phi_1$ , then the charge behaves according to the following sequence;

At the end of  $\phi_1$ :  $Q_{C_1} = 0$   
( $t=nT$ )

$Q_{C_2} = 0$

At the end of  $\phi_2$ :  $Q_{C_1} = C_1 V_{IN}(nT + \frac{T}{2})$

$Q_{C_2} = -Q_{C_1} = -C_1 V_{IN}(nT + \frac{T}{2}) = C_2 V_{OUT}(nT + \frac{T}{2})$

$$\therefore \frac{V_{OUT}}{V_{IN}} = -\frac{C_1}{C_2} \quad 2.17$$

While this circuit provides negative multiplication, there is no delay involved. One method of achieving the negative multiply with delay is shown in Figure 2.12(b). There are alternative structures that produce the same result. However it must be noted that from the point of view of maximum accuracy in the multiplication, it is preferable to leave the input capacitor  $C_1$  connected directly to the amplifier inverting input. This is because the alternative configuration, which has a switch connecting  $C_1$  to the inverting input and the voltage source, introduces a harmful parasitic junction capacitance shunting the signal path (see Section 3.3.3 for this circuit).

Consider the circuit operation of Figure 2.12(b): A four phase clock is necessary to control this circuit (this is the price paid for avoiding harmful parasitic capacitances). Assume  $t=nT$  at the end of  $\phi_1$ .

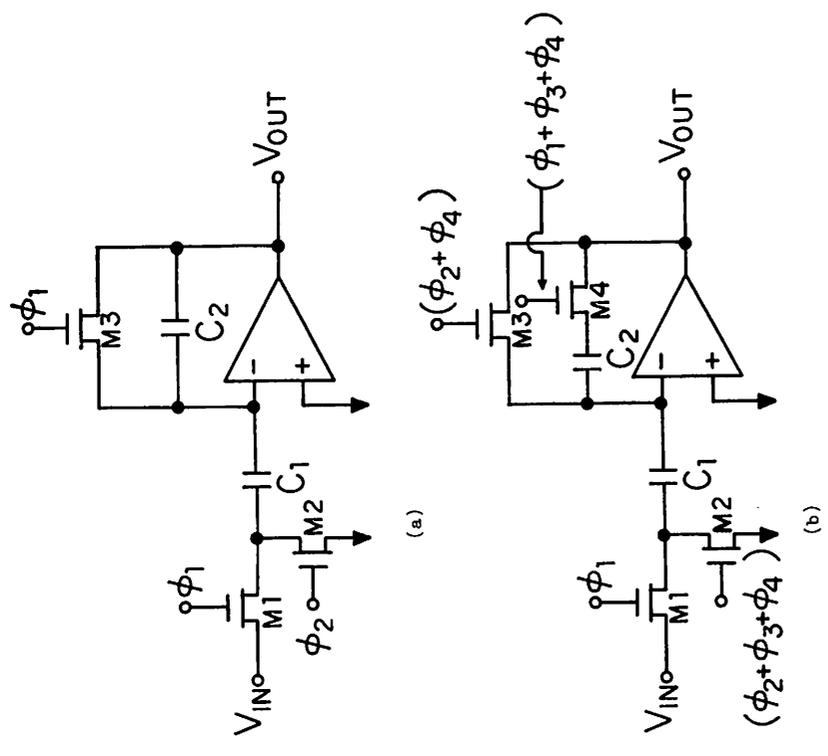


Figure 2.12: Analog Sampled-data Switched-capacitor circuits.  
 (a): Positive multiplication with delay, or with inverse clocking of the input switches; negative multiplication with no delay.  
 (b): Negative multiplication with delay.

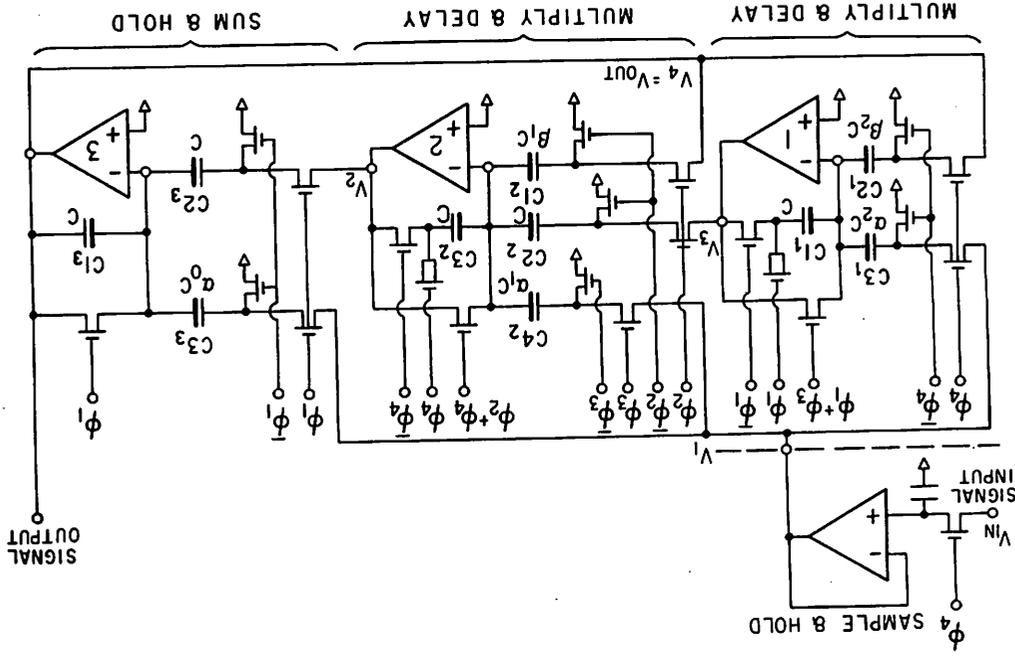


Figure 2.13: Three Amplifier Biquadratic Section.

At the end of  $\phi_4$ :  $Q_{C_1} = 0, Q_{C_2} = 0$

At the end of  $\phi_1$ :  $Q_{C_1} = C_1 V_{IN}(nT) = -Q_{C_2}$

At the end of  $\phi_2$ :  $Q_{C_1} = 0, Q_{C_2} = -C_1 V_{IN}(nT)$

At the end of  $\phi_3$ :  $Q_{C_1} = 0, Q_{C_2} = -C_1 V_{IN}(nT) = C_2 V_{OUT}(nT + \frac{T}{2})$

$$\therefore \frac{V_{OUT}}{V_{IN}} = -\frac{C_1}{C_2} z^{-1/2} \tag{2.18}$$

where  $z^{-1/2}$  represents the half period ( $\frac{T}{2}$ ) of delay that occurs from the end  $\phi_1$  to the end  $\phi_3$ .

Switched-capacitor implementation of a full biquadratic second-order section is shown in Figure 2.13, based on Figure 2.9(b) and the switched-capacitor circuits just described. It uses a four phase clock and three amplifiers, two of which are switched using the same scheme as Figure 2.12(b) to achieve negative multiplication capability (with the labelling shown;  $\beta_2$  path is negative,  $\beta_1$  path is positive,  $\alpha_0$  path is positive,  $\alpha_1$  path is negative,  $\alpha_2$  path is negative). The third amplifier's function is to realize the summing node at the output (see Figure 2.9b). Since  $\beta_1$  and  $\beta_2$  signal paths only see a fractional period of delay, amplifier three performs the necessary function of holding the output to provide the additional fractional delay to make two unit delays around the  $\beta_2$  loop and one unit delay around the  $\beta_1$  loop. Algebraically amplifier three provides a choice of three transfer functions (depending on the time of sampling at the output). Referring to Figure 2.13:

$$\frac{V_4}{V_1} = \left(\frac{V_4}{V_1}\right) = z^{-1/4} \text{ or } z^{-3/4}$$

Amplifier 3:

$$\left(\frac{V_4}{V_1}\right) = \left(\frac{V_4}{V_1}\right) = z^{-1/4} \text{ or } z^{-3/4}$$

where  $z^{-1/4}$  represents  $1/4$  of the delay period  $T$ .

Amplifier 2:

$$\beta_1 \text{ path: } \left(\frac{V_2}{V_4}\right) = +\beta_1 z^{-3/4} \text{ from end } \phi_2 \text{ to the end } \phi_1$$

$$\alpha_1 \text{ path: } \left(\frac{V_2}{V_1}\right) = -\alpha_1 z^{-1/2}$$

$$\beta_2 \text{ path: } \left(\frac{V_2}{V_3}\right) = z^{-3/4}$$

Amplifier 1:

$$\beta_2 \text{ path: } \left(\frac{V_3}{V_4}\right) = -\beta_2 z^{-1/2} \text{ from the end } \phi_4 \text{ to the end } \phi_2.$$

$$\alpha_2 \text{ path: } \left(\frac{V_3}{V_1}\right) = -\alpha_2 z^{-1/2}$$

Therefore analyzing the feedback loops

$$\text{Around the } \beta_2 \text{ loop: } \left(\frac{V_4}{V_2}\right) \cdot \left(\frac{V_3}{V_4}\right) \cdot \left(\frac{V_2}{V_3}\right) = (z^{-3/4}) \cdot (-\beta_2 z^{-1/2}) \cdot (z^{-3/4})$$

$$\text{Around the } \beta_1 \text{ loop: } \left(\frac{V_4}{V_2}\right) \cdot \left(\frac{V_2}{V_4}\right) = (z^{-1/4}) \cdot (-\beta_1 z^{-3/4}) = \beta_1 z^{-1}$$

$$= -\beta_2 z^{-2}$$

The input sample and hold amplifier provides the additional  $z^{-1/2}$  delay for the  $\alpha_1$  and  $\alpha_2$  paths (otherwise there would be distortion of the frequency response due to out of phase sampling at the input).

The complete switched-capacitor second order section has the following characteristics:

(i) It can realize up to two complex poles and two complex zeros anywhere in the  $z$  plane -- a true biquadratic function capability:

$$H(z^{-1}) = \frac{\alpha_0 \alpha_1 z^{-1} + \alpha_2 z^{-2}}{1 + \beta_1 z^{-1} + \beta_2 z^{-2}} \quad 2.19$$

(ii) The analog multiplications throughout all signal paths are not sensitive to any junction parasitic capacitance. Therefore the minimum size of the switched-capacitors is not determined by a parasitic capacitance. The capacitors can be made just as small as photolithography and etching will allow before degradation of capacitor ratio accuracy occurs due to the edge effects (refer to Section 4.1).

(iii) The capacitor ratios requiring the highest degree of accuracy for precision filters are the feedback coefficients  $\beta_1$  and  $\beta_2$ . Their maximum absolute value is close to 2.0 and 1.0 respectively. The closer the values of  $\beta_1$  and  $\beta_2$  are to this maximum, the more important the requirements on capacitor ratio accuracy. Smaller values for  $\beta_1$  and  $\beta_2$  do not require as much accuracy because either the  $Q$  of the filter is lower or the ratio of  $\frac{f_s}{f_0}$  is lower, or both (refer to Section 3.2 for further discussion on the sensitivity behavior of the filter). Thus due to the high accuracy only being required on ratios that are bounded by 2.0 and 1.0, high  $Q$  filters with precision tolerances on  $f_0$  and  $Q$  can be realized in a relatively small silicon area with this second order section. The deviations in  $f_0$  and  $Q$  depend on how well the capacitance ratios are controlled.

(iv) The use of a low sampling rate is desirable because of sensitivity considerations (see Section 3.2). However for anti-alias prefilter simplicity a high sampling rate would be preferred. Therefore the filter design will use the highest sampling rate possible while still maintaining the control required on the filter's response.

If the sampling rate is low then the filter can be multiplexed readily by adding one extra capacitor (with its own series switch) in parallel with the feedback capacitors for the multiplexed channel. The

number of multiplexed filter channels ( $N$ ) is determined by the unity gain settling time to 0.1% ( $\tau_a$ ) and the sampling rate ( $f_s$ ):

$$N = \frac{1}{4f_s \tau_a} \quad 2.20$$

(v) Mask programmable or electrically programmable filters are efficiently realized with this second order section due to the fact that the capacitor ratios are relatively small and minimum capacitance values can be quite small (0.5 → 1.0 pf). The double polysilicon gate NMOS technology with EPROM cell available [26] is an attractive process for implementing these switched-capacitor sampled data recursive filters. This technology provides capacitors with thermally grown oxide between poly I and II layers, with enhancement and depletion transistors available for the amplifier design.

### 2.3.3 The Two Amplifier Second Order (bandpass) Section

A second order bandpass filter can be implemented with switched-capacitors and just two amplifiers. The trade-offs involved will be discussed later in this section.

Ignoring the fact that it is undesirable to switch the input capacitors between a voltage source and the amplifier inverting inputs, because the parasitic junction capacitors will affect the charge multiplier performance, the circuit shown in Figure 2.14 could be used to realize a multiply and delay. This circuit does not have the feedback switch that was used to remove the charge from the feedback capacitor. The charge is subtracted off instead with the switched-capacitor  $C_2$ . This means that the circuit functions with a two phase clock as follows; assume  $t = nT$  at the end of  $\phi_1$ ,

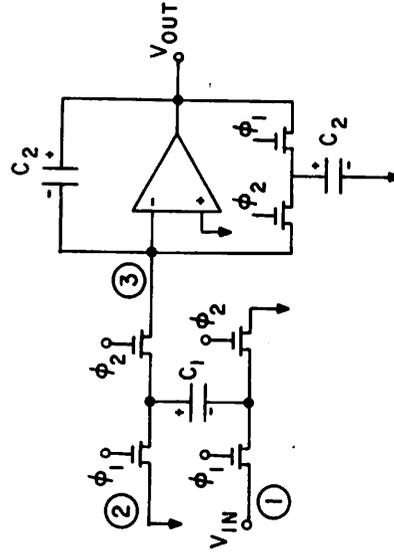


Figure 2.14: Multiplication element with a unit of delay ( $z^{-1}$ ).

At the end of  $\phi_1$ :  $Q_{C_1} = -C_1 V_{IN}(nT)$

$Q_{C_2} = C_2 V_{OUT}(nT)$

$Q_{C_2'} = C_2' V_{OUT}(nT)$

At the end of  $\phi_2$  ( $t = nT + \frac{T}{2}$ ):  $Q_{C_1} = 0$

$$Q_{C_2} = C_2 V_{OUT}(nT) + C_1 V_{IN}(nT) - C_2' V_{OUT}(nT) = C_2 V_{OUT}(nT + \frac{T}{2})$$

if  $C_2 = C_2'$  then  $Q_{C_2} = C_1 V_{IN}(nT) = C_2 V_{OUT}(nT + \frac{T}{2})$

At the end of  $\phi_1$  ( $t=nT+T$ ):  $Q_{C_1} = -C_1 V_{IN}(nT+T)$

$Q_{C_2} = C_1 V_{IN}(nT) = C_2 V_{OUT}(nT+T)$

Thus

$$\frac{V_{OUT}}{V_{IN}} = \frac{C_1}{C_2} z^{-1} \tag{2.21}$$

If node 1 in Figure 2.14 is connected to ground and  $V_{IN}$  is applied to node 2 then the transfer function is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{C_1}{C_2} z^{-1} \tag{2.22}$$

Two of these multiply and delay elements can be configured very easily to form a second order bandpass section. This is shown in Figure 2.15(a). Switched-capacitors  $C_2$  and  $C_2'$  can be combined into one switched-capacitor. Then the circuit simplifies to that shown in

Figure 2.15(b).

The two amplifier second order switched-capacitor bandpass filter is attractive from the point of view that it requires only two amplifiers and it operates under two phase clock control. However, the

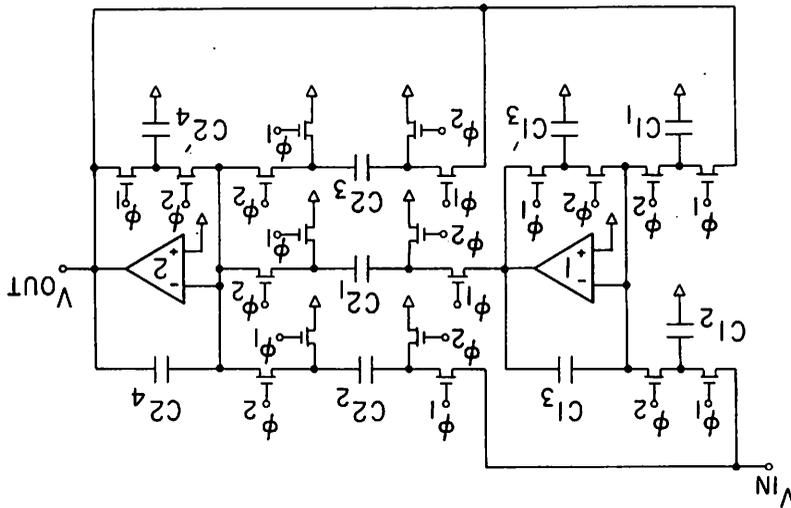


Figure 2.15.a: Two Amplifier Second Order Section (Biquad).

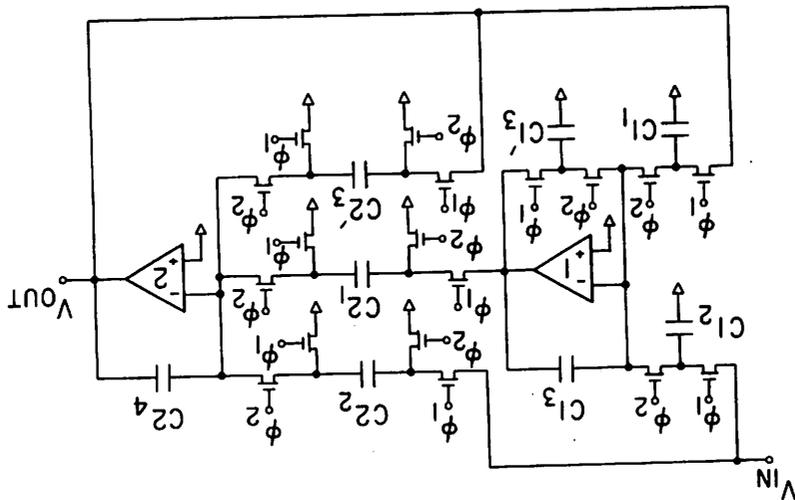
accuracy of the feedback and feedforward signal multiplications for the second order section will not be as good as the three amplifier realization, due to the presence of the parasitic junction capacitance on the capacitor plates that are being switched between a signal node (amplifier output or input voltage source) and an amplifier inverting input. The nonlinear junction capacitance will contribute to distortion and capacitance ratio error. It can only be minimized by making the capacitor much larger than the parasitic  $C_p$  -- how much larger depends on the accuracy desired.

A final limitation of the two amplifier second order section is that only bandpass (biquad) and lowpass transfer functions can be implemented. It is not the general second order biquadratic block capable of realizing lowpass, bandpass or highpass responses simply by changing the capacitor ratios and the phasing of the switches. These can be realized with the three amplifier section described previously. The two amplifier switched-capacitor biquad circuit realizes the transfer function:

$$H(z^{-1}) = \frac{\alpha_0 + \alpha_1 z^{-1}}{1 + \beta_1 z^{-1} + \beta_2 z^{-2}}$$

2.23

Figure 2.15.b: Two Amplifier Second Order Section with one less switched-capacitor than circuit (a).



## CHAPTER 3

DESIGN CONSIDERATIONS FOR ANALOG SAMPLED-DATA RECURSIVE FILTERS  
USING THE SWITCHED-CAPACITOR SECOND ORDER SECTIONIntroduction

The switched-capacitor second order section described in Section 2.3.2 can realize high or low Q filters having second order lowpass, bandpass, or highpass frequency characteristics. The transfer function of such filters involve the general biquadratic form:

$$H(z^{-1}) = \frac{\alpha_0 + \alpha_1 z^{-1} + \alpha_2 z^{-2}}{1 + \beta_1 z^{-1} + \beta_2 z^{-2}} \quad 3.1$$

The magnitude and sign of the coefficients  $\alpha_0$ ,  $\alpha_1$ ,  $\alpha_2$  and  $\beta_1$ ,  $\beta_2$  determine the positions (complex or real) of the poles and zeros respectively in the frequency plane. The switched-capacitor filter circuit described in Section 2.3.2 allows complete freedom in the choice of magnitude and sign for these coefficients.

If the zero(s) are placed at frequencies higher than the poles the filter response will be lowpass. If there is only one zero at zero frequency (occurs for  $\alpha_0 = 1.0$ ,  $\alpha_1 = -1.0$ ) then the filter is bandpass. If the zeros are at frequencies less than the two poles then the filter has a second order highpass response. The design of each of these filters is presented in Section 3.3. Experimental results for a fully monolithic realization of each of these filters are given in Chapter 5. Throughout the rest of this chapter consideration will be given to the various aspects of using an analog sampled recursive filter to implement second and higher order filters. These aspects will include

some analysis of the sensitivity and accuracy requirements for the capacitor ratios. The effects of nonidealities in the switched-capacitor circuit on the performance of the filter, are presented in the last section of this chapter.

## 3.1 Sampled-Data (Discrete-Time) Filter Design From the Analog Prototype Using Frequency Plane Mapping Transformations

The traditional approach to the design of discrete-time recursive filters (Infinite Impulse Response) involves the transformation of an analog continuous time filter into a discrete time filter meeting prescribed specifications [11]. This approach is reasonable in those cases where one can take advantage of analog designs that are given in terms of formulas or available design tables; e.g., frequency selective filters such as Butterworth, Chebyshev, or elliptic filters.

For those designs that are required to match arbitrary frequency response specifications, design procedures have been developed for use with a computer. They are based on approximating algorithms. In these cases a filter structure (architecture) is chosen prior to having the computer optimize the coefficients for the required transfer function.

To outline the method of transforming continuous time filter parameters into those for a discrete-time filter, the design of a two pole analog sampled-data bandpass filter will be considered. It is derived by transformation from a 2 pole analog continuous time bandpass filter.

In the continuous time/frequency  $s$  domain, the second order bandpass transfer functions is:

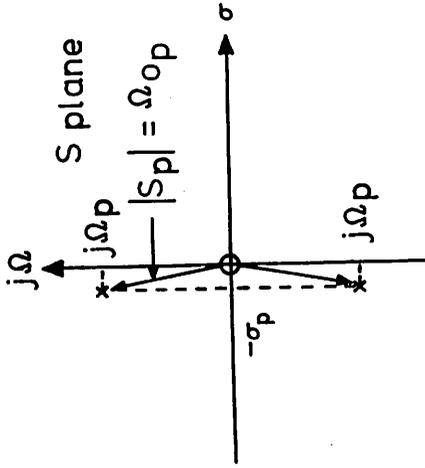


Figure 3.1: Singularity placement in the s-plane for a 2-pole bandpass filter.

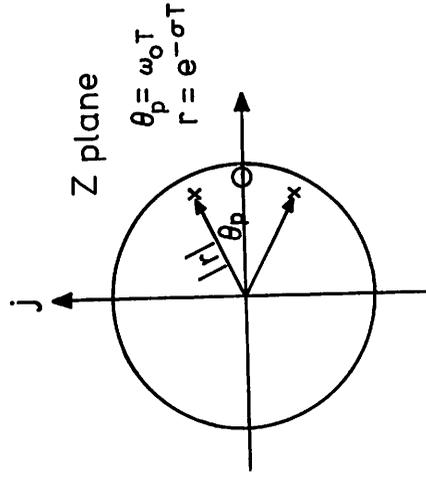


Figure 3.2: Singularity placement in the z-plane for the 2-pole bandpass filter transformed with the impulse invariant transform.

3.2

$$H(s) = \frac{2\sigma_p s}{s^2 + 2\sigma_p s + \Omega_p^2}$$

The poles and zero for this bandpass response are located in the s plane as shown in Figure 3.1.

The transfer function H(s) can be transformed to its discrete-time (z domain) equivalent with one of the four most widely used procedures for transforming to the discrete-time z domain [11]:

- (1) The method of mapping differentials (forward and backward differences): Forward Differences  $s = \frac{1}{T} \frac{1-z^{-1}}{z^{-1}}$

Backward Differences  $s = \frac{1-z^{-1}}{T}$

- (2) The impulse invariant transformation.

- (3) The bilinear z-transform:  $s = \frac{2}{T} \frac{(1-z^{-1})}{(1+z^{-1})}$

- (4) The matched z-transform technique.

Transformations (2) and (3) are the ones generally used in sampled-data filter design. The impulse invariant transformation has the property that the impulse response of the resulting discrete-time filter is a sampled version of the impulse response of the analog continuous time filter. The impulse invariant transform of Equation 3.1 is:

$$H(z^{-1}) = \frac{2\sigma_p [1-z^{-1} e^{-\sigma T} (\cos \Omega T + \frac{\sigma}{\Omega} \sin \Omega T)]}{1-2z^{-1} e^{-\sigma T} \cos \Omega T + z^{-2} e^{-2\sigma T}}$$

$$= \frac{\sigma_p + \sigma_1 z^{-1}}{1 + \beta_1 z^{-1} + \beta_2 z^{-2}}$$

3.3

Thus:  $\beta_1 = 2e^{-\sigma T} \cos \Omega T$

$$\beta_2 = -e^{-2\sigma T}$$

$$\alpha_0 = 2\sigma$$

$$\alpha_1 = -2\sigma e^{-\sigma T} \left[ \cos \Omega T + \frac{\sigma}{\Omega} \sin \Omega T \right]$$

Figure 3.2 shows the z-plane representation of the transformed singularities.

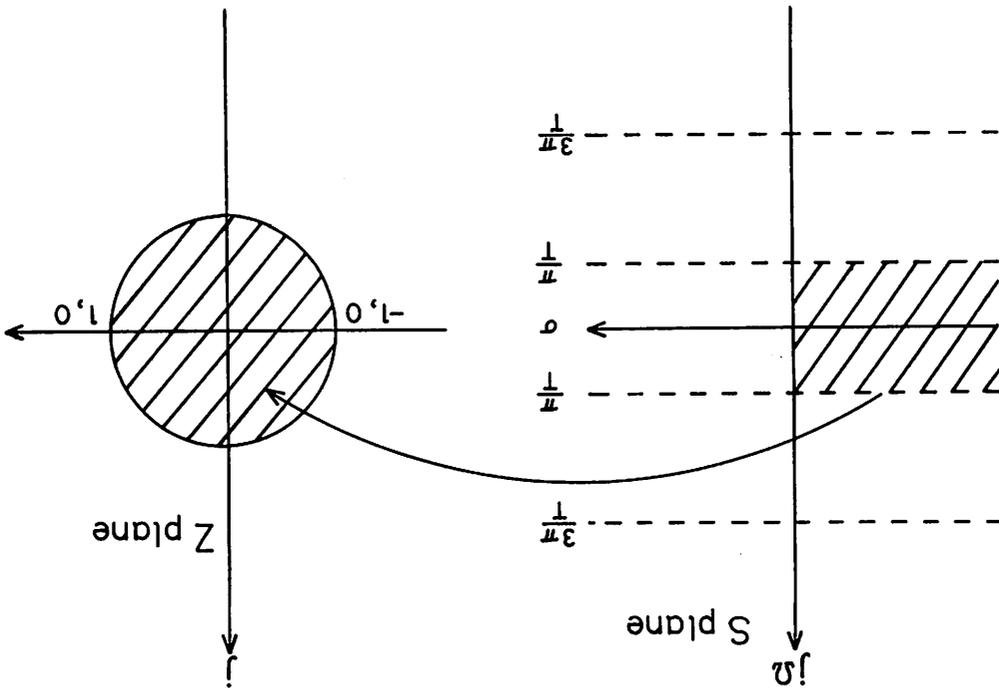
The frequency response of a discrete-time filter, designed with the impulse invariant transformation, is an aliased version of the frequency response of the continuous system from which it was derived. The discrete-time frequency response is:

$$H(e^{j\omega T}) = \frac{1}{T} \sum_{k=-\infty}^{\infty} H(j\Omega + jk\Omega_s) \quad 3.4$$

where  $\Omega_s = \frac{2\pi}{T}$  is the radian sampling frequency of the discrete-time filter. Figure 3.3 shows the mapping of the s plane to the z plane under the impulse invariant transformation. It can be seen that the discrete-time filter, when designed with the impulse invariant transformation, will be a good approximation to the continuous time filter only if the filter response itself bandlimits to the range  $-\frac{\pi}{T} < \Omega < \frac{\pi}{T}$ .

In contrast to the impulse invariant transform, the bilinear z-transformation does a conformal mapping from the s plane to the z plane. This preserves the desired algebraic form of the transfer function and avoids the problem of aliasing encountered with the use of impulse invariance because it maps the entire imaginary axis in the s plane onto the unit circle in the z plane. The bilinear z-transformation is the substitution;

Figure 3.3: Mapping of the s-plane to the z-plane with the impulse invariant transform.



$$s = \frac{2}{T} \left( \frac{1-z^{-1}}{1+z^{-1}} \right)$$

and therefore  $H(z) = H_a(s)$

$$s = \frac{2}{T} \left( \frac{1-z^{-1}}{1+z^{-1}} \right)$$

Under this transform the left half of the s plane is mapped inside the unit circle in the z plane and the right half of the s plane is mapped outside the unit circle in the z plane. Since the entire imaginary axis in the s plane maps onto the unit circle with one encirclement, there is a nonlinear relationship between analog frequency  $\Omega$  and discrete-time frequency  $\omega$  (frequency warping effect).<sup>\*</sup> This frequency warping is described by:

$$\Omega \rightarrow \frac{2}{T} \tan \left( \frac{\omega T}{2} \right) \quad 3.6$$

and Figure 3.4 shows an example of how this warping effect can be corrected for when transforming from the analog (continuous-time) prototype. The warping effect only modifies the frequency axis and does not distort the shape of the gain response. It can be an aiding factor in making transition regions much steeper (without increasing the number of poles). However the significance of this effect is dependent on how close the sampling frequency is to the transition region (the closer it is the larger the warping). The warping effect is negligible when the sampling frequency is more than about eight times greater than the transition region.

The discrete-time transfer function that results when the bilinear

<sup>\*</sup>This frequency variable notation will be adhered to from here on.

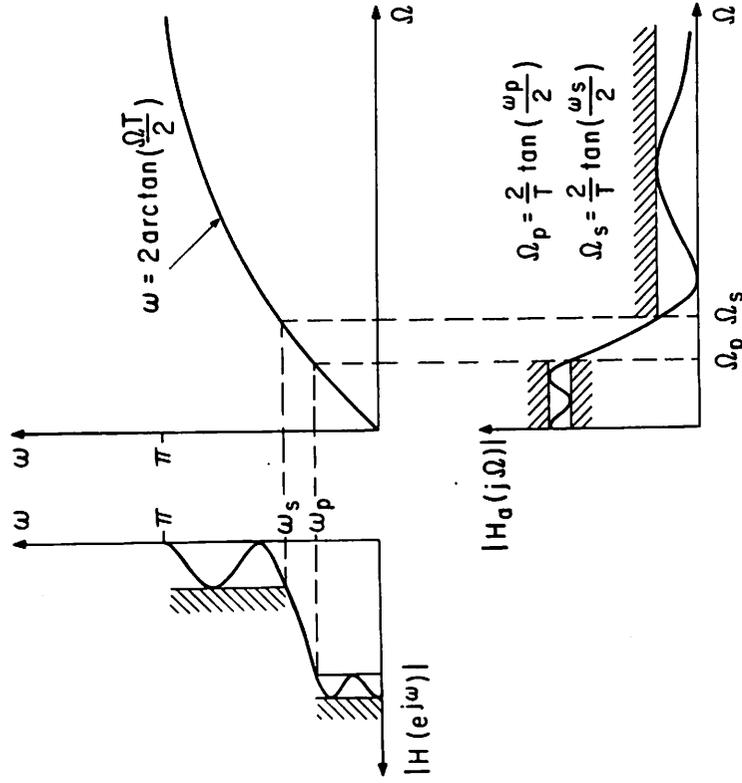


Figure 3.4: Frequency warping encountered in transformed analog lowpass filter to a sampled-data lowpass filter. To achieve the desired sampled-data cutoff frequency, the analog cutoff frequencies must be prewarped as indicated.

z-transformation is applied to continuous-time bandpass filter (Equation 3.2) is;

$$H(z^{-1}) = \frac{2\sigma \frac{2(1-z^{-1})}{1+z^{-1}}}{\left(\frac{2}{T}\right)^2 \left(\frac{1-z^{-1}}{1+z^{-1}}\right)^2 + 2\sigma \frac{2(1-z^{-1})}{1+z^{-1}} + \sigma^2 + \Omega^2}$$

$$= \frac{\sigma T(1-z^{-2})}{(1+\sigma T + \frac{T^2}{4}\omega_0^2) + (\frac{T^2}{4}\omega_0^2 - 2)z^{-1} + (1-\sigma T + \frac{T^2}{4}\omega_0^2)z^{-2}}$$

$$= \frac{\alpha_0 + \alpha_1 z^{-1} + \alpha_2 z^{-2}}{1 + \beta_1 z^{-1} + \beta_2 z^{-2}}$$

$$\alpha_0 = \frac{\sigma T}{1 + \sigma T + \frac{T^2}{4}\omega_0^2}$$

$$\alpha_1 = 0$$

$$\alpha_2 = -\frac{\sigma T}{1 + \sigma T + \frac{T^2}{4}\omega_0^2}$$

$$\beta_1 = \frac{\frac{T^2}{4}\omega_0^2 - 2}{1 + \sigma T + \frac{T^2}{4}\omega_0^2}$$

$$\beta_2 = \frac{1 - \sigma T + \frac{T^2}{4}\omega_0^2}{1 + \sigma T + \frac{T^2}{4}\omega_0^2}$$

Note that the discrete-time transfer function has two zeros, one at  $\omega = 0$  and one at  $\frac{\omega}{2}$ . The reason why this occurs is because  $H_a(s)$  has a zero at  $\Omega = 0$ , and at  $\Omega = \infty$ , the bilinear z-transform maps these to  $z = \pm 1.0$  ( $\omega = 0$ ,  $\omega = \frac{\omega_s}{2}$ ).

Both Equation 3.3 and 3.7 have the property that when the bandpass filter has high Q or  $\omega_s \gg \omega_0$  then  $\beta_1$  controls the center frequency and  $\beta_2$  the 3 dB bandwidth.

While the impulse invariant and bilinear z-transforms are the best methods to use in the design of an analog sampled-data filter with the switched-capacitor second order section shown in Figure 2.13, it is of interest to point out some effects that occur if forward or backward differences are employed.

Intuitively one can see that the derivative of an analog time function can be approximated by the difference between consecutive samples of the function. This approximation should get better as the sampling rate is increased (samples are closer together). This is the reason why designs using forward or backward differences have more accuracy the higher the sampling rate.

When using backward differences one makes the replacement

$$\frac{dy}{dt} \rightarrow \frac{y(n) - y(n-1)}{T} \quad 3.8a$$

In terms of the unit delay operator this corresponds to:

$$s = \frac{1 - z^{-1}}{T} \quad 3.8b$$

or

$$z = \frac{1}{1 - sT}$$

For  $s = j\Omega$

$$z = \frac{1}{1 - j\Omega T}$$

which can be written as:

$$z = \frac{1}{2} \left[ 1 + \frac{1 + j\Omega T}{1 - j\Omega T} \right]$$

$$z = \frac{1}{2} [1 + e^{j2 \tan^{-1}(\Omega T)}]$$

This describes a circle whose center is at  $z = \frac{1}{2}$  and radius is  $\frac{1}{2}$ . This mapping is shown in Figure 3.5. It can be seen that except for extremely small values of  $\Omega T$  (high sampling rate with respect to the frequency of interest), the image of the  $j\Omega$  axis in the  $s$  plane is off the unit circle in the  $z$  plane. Thus the sampled-data filter will accurately approximate the analog filter only when the sampling frequency ( $\frac{1}{T}$ ) is very high.

An integrator using the "series switched-capacitor" resistor introduced in the paper by Caves et al. [14] is equivalent to the backward differences transformation. When the sampling rate is not high in relation to the frequencies of interest phase lead is observed in the switched capacitor integrators. This phase shift gets worse at lower sampling rates because the mapping with the backward differences (replacement of  $\frac{1}{s}$  with  $\frac{T}{1-z^{-1}}$ ) places the poles further away from the unit circle in the  $z$  plane. Only when the sampling rate is high will the sampled-data filter based upon  $\frac{1}{s} \leftrightarrow \frac{T}{1-z^{-1}}$  accurately approximate the analog filter in gain response and sensitivity performance.

An alternative approximation to the derivative is a forward difference. When using forward differences one makes the replacement:

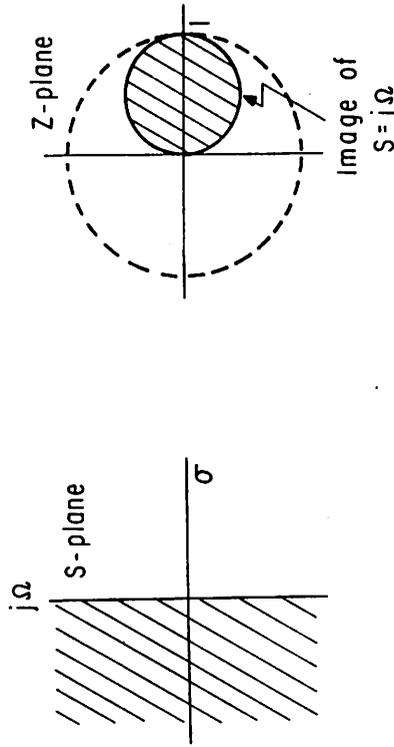


Figure 3.5: Mapping of the  $s$ -plane to the  $z$ -plane corresponding to the first backward difference approximation to the derivative function.

$$\frac{dy}{dt} \leftrightarrow \frac{Y(nT) - Y(n)}{T}$$

3.9a

which corresponds to

$$s = \frac{z-1}{T}$$

3.9b

or  $z = 1 + sT$

For  $s = j\Omega$ ,  $z = 1 + j\Omega T$ .

Here the mapping of the  $j\Omega$  axis in the  $s$  plane to the  $z$  plane amounts to a simple shift of the origin to  $z = 1$ , 0 (see Figure 3.6). However depending on how low the sampling rate is in relation to the frequencies of interest, the forward differences transformation will shift the poles towards the unit circle in the  $z$  plane and can even place them in the unstable region outside the unit circle. Sampled-data integrators based upon forward differences ( $\frac{1}{s} \leftrightarrow \frac{Tz^{-1}}{1-z^{-1}}$ ), will introduce a phase lag. To minimize the amount of phase lag  $\Omega T$  should be as small as possible. The "parallel switched-capacitor" resistor when used in an integrator as in Hosticka et al. [13] is equivalent to a forward differences transformation.

Allstot and Jacobs et al. [15, 16] in their work on switched-capacitor ladder filters identify the phase shift (lag) problem encountered when using the switched-capacitor integrator equivalent to backward differences. The solution described by Bruton [33] and used in the switched-capacitor ladder filters amounts to a cascade of one backward differences integrator with one forward differences integrator in each leap-frog path, such that the phase lag and lead from each will compensate one another and thus reduce the phase shift problem. This improvement

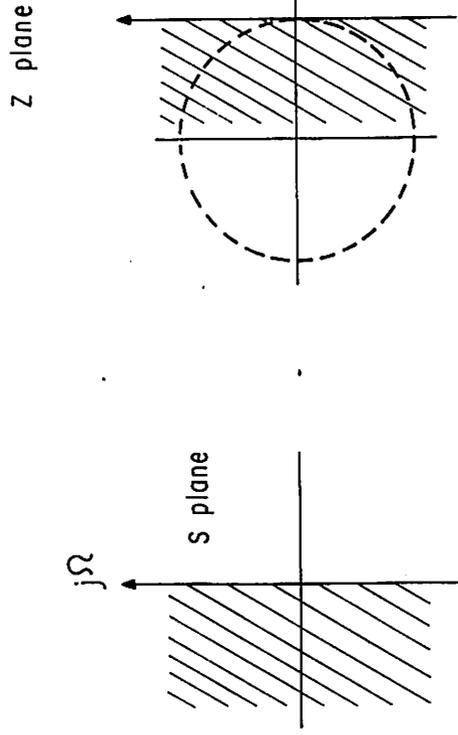


Figure 3.6: Forward differences mapping of the  $s$ -plane  $j\Omega$  axis to the  $z$ -plane.

will still only be accurate for a high sampling rate ( $\omega T$  small); however the accuracy at a given high sampling rate will be much better than if this technique was not employed.

### 3.2 Sensitivity and Accuracy Considerations

The important question to be asked when realizing a filter with the second order switched-capacitor sampled-data recursive form, is what are the accuracy requirements for the coefficients (capacitor ratios). Coefficient error causes the poles to move\* thus changing the 3 dB bandwidth ( $Q$ ) and the center frequency ( $\omega_0$ ). From Equation 3.3:

3.10a

$$\omega_0 = \frac{1}{T} \cos^{-1} \left( \frac{\beta_1}{2\sqrt{\beta_2}} \right)$$

3.10b

$$Q = \frac{\cos^{-1} \left( \frac{\beta_1}{2\sqrt{\beta_2}} \right)}{\ln \beta_2}$$

Accuracy requirements can be calculated from the sensitivity functions for the filter. Derived from Equations 3.10a and b, the second order bandpass filter has the following sensitivities to center frequency and  $Q$ :

(1) Sensitivity of center frequency to  $\beta_1$  and  $\beta_2$ :

3.11a

$$S_{\beta_1}^{\omega_0} = \frac{1}{(\omega_0 T)^2}$$

3.11b

$$S_{\beta_2}^{\omega_0} = \frac{1}{2} \frac{1}{(\omega_0 T)^2}$$

\*The coefficients determining the poles are more sensitive than the coefficients determining the zeros because feedback controls the pole locations.

(2) Sensitivity of  $Q$  to  $\beta_1$  and  $\beta_2$ :

3.11c

$$S_{\beta_1}^Q = \frac{1}{(\omega_0 T)^2}$$

3.11d

$$S_{\beta_2}^Q = \frac{1}{2} \frac{1}{(\omega_0 T)^2} + \frac{Q}{\omega_0 T}$$

For high  $Q$  filters  $\omega_0$  is only controlled by  $\beta_1$  and  $Q$  is controlled by  $\beta_2$ .

From Equations 3.11a,b,c,d it can be seen that the sensitivity of the filter response ( $\omega_0$ ,  $Q$ ) decreases as  $\omega_0 T$  increases. For coefficients that can only be realized with a finite limit on their achievable accuracy, it is desirable to choose the sampling frequency ( $f_s = \frac{1}{T}$ ) as close to  $\omega_0$  as practicable without putting stringent rejection requirements on the anti-alias prefilter.

While a low sampling rate switched-capacitor filter may require a more complex anti-alias filter than a high sampling rate one, provided the anti-alias filter can be integrated on chip (perhaps with the addition of a few non-precision external components) there is no major disadvantage to the approach, assuming the design meets the required specifications. The low sampling rate design has the advantage that it can be multiplexed, more so than a high sampling rate one where the settling time of the amplifier might be just a little less than the clocking time interval.

To understand the trade-offs involved in the design of a switched-capacitor filter with the second order section, consider the following design for application in touch tone filter networks [17]; a second

order bandpass filter having  $f_0 = 697 \text{ Hz} \pm 0.5\%$  and  $Q = 18 \pm 1$ . This filter is a precision filter; it has very tight tolerances on its Q and center frequency. Table I documents the feedback coefficients and their accuracy requirements for the second order section to meet this bandpass filter design specification. Designs based on 4 kHz and 8 kHz sampling frequency are given. The impulse invariant design Equations (3.3) have been used here. Sensitivity results are similar if the bilinear z-transform is used.

From Table I it can be seen that when the sampling frequency is increased (thereby easing the anti-alias filter requirements) the accuracy of the feedback coefficients (and thus the capacitor ratios) becomes more stringent.

The anti-alias prefilter for this design example needs to be as simple as possible. If off-chip components are necessary for the pre-filter, then it must be able to perform satisfactorily with standard non-precision (for low cost) components ( $\pm 1\%$  resistors,  $\pm 5\%$  capacitors, for example).

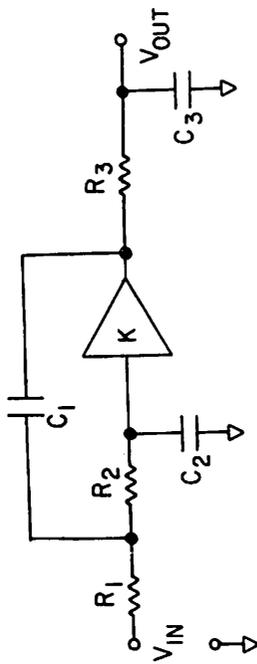
One possible design for the prefilter is the three pole active RC filter shown in Figure 3.7(a). This circuit is not very sensitive to component variations when the Q is low [22].

When the response is maximally flat and the 3 dB frequency is 2 kHz, this filter has the magnitude response shown in Figure 3.8. Perturbations in the pole locations, that are consistent with deviations for non-precision resistors and capacitors, produce negligible variation in the passband (less than 0.1 dB up to 1 kHz). There is more than 33 dB of rejection at 7 kHz and above, to prevent aliasing of the high

TABLE I SECOND ORDER BANDPASS FILTER DESIGN PARAMETERS.

REQUIRED COEFFICIENT ACCURACY %	COEFFICIENT		SENSITIVITY		SAMPLING FREQUENCY
	$\alpha_1$	$\alpha_2$	$\frac{\alpha_1}{Q}$	$\frac{\alpha_2}{Q}$	
$\pm 0.17$	$\pm 0.16$	$\pm 0.34$	$\pm 0.54$	$\pm 0.17$	8 KHz
$\pm 0.16$	$\pm 0.16$	$\pm 0.34$	$\pm 0.54$	$\pm 0.17$	4 KHz
$\pm 0.17$	$\pm 0.16$	$\pm 0.34$	$\pm 0.54$	$\pm 0.17$	8 KHz
$\pm 0.16$	$\pm 0.16$	$\pm 0.34$	$\pm 0.54$	$\pm 0.17$	4 KHz

$$\left. \begin{aligned} f_0 &= 697 \pm 0.5\% \\ Q &= 18 \pm 1 \end{aligned} \right\} \text{SECOND ORDER BANDPASS FILTER}$$



$$H(s) = \frac{H_0 \omega_0^2}{s^2 + 2\sigma s + \omega_0^2} \cdot \frac{1}{s + a}$$

$$H_0 = K$$

$$\omega_0 = \left( \frac{1}{R_1 R_2 C_1 C_2} \right)^{1/2}$$

$$\frac{1}{Q} = \left( \frac{R_2 C_2}{R_1 C_1} \right)^{1/2} + \left( \frac{R_1 C_1}{R_2 C_2} \right)^{1/2} - K \left( \frac{R_1 C_1}{R_2 C_2} \right)^{1/2}$$

$$a = \frac{1}{R_3 C_3}$$

Figure 3.7.a: Three Pole Lowpass Filter.

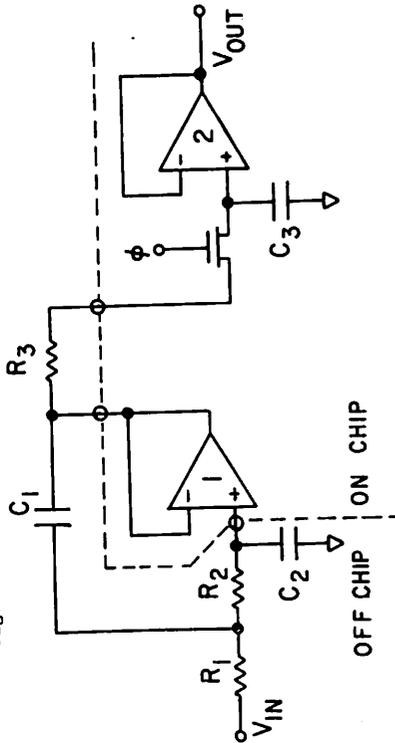
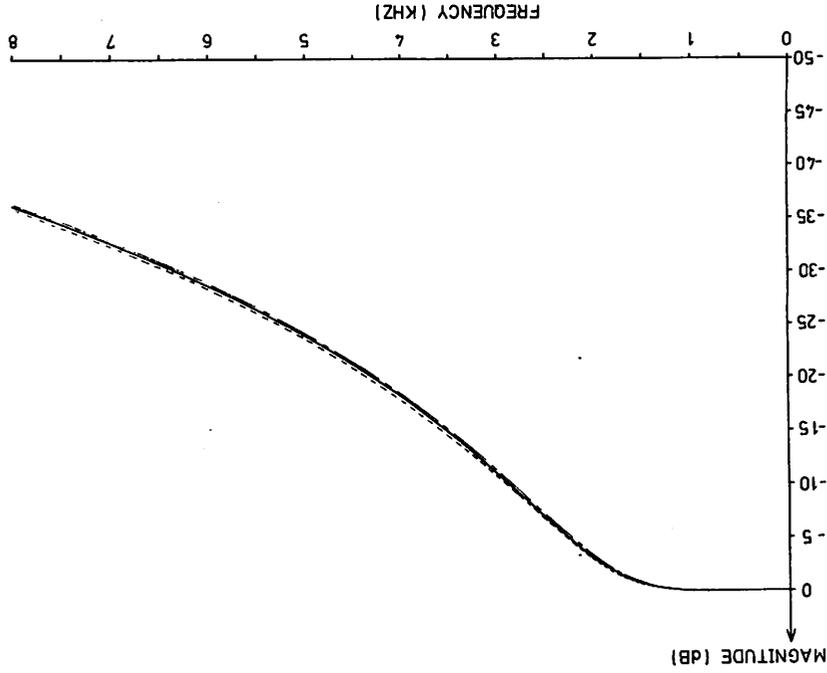


Figure 3.7.b: Three Pole Lowpass Filter with Sample and Hold Function included.

Figure 3.8: Nominal three pole maximally flat filter response together with the responses under deviations of  $\pm 1\%$  on resistors and  $\pm 5\%$  on capacitors in figure 3.7.a. 3dB frequency = 2 kHz



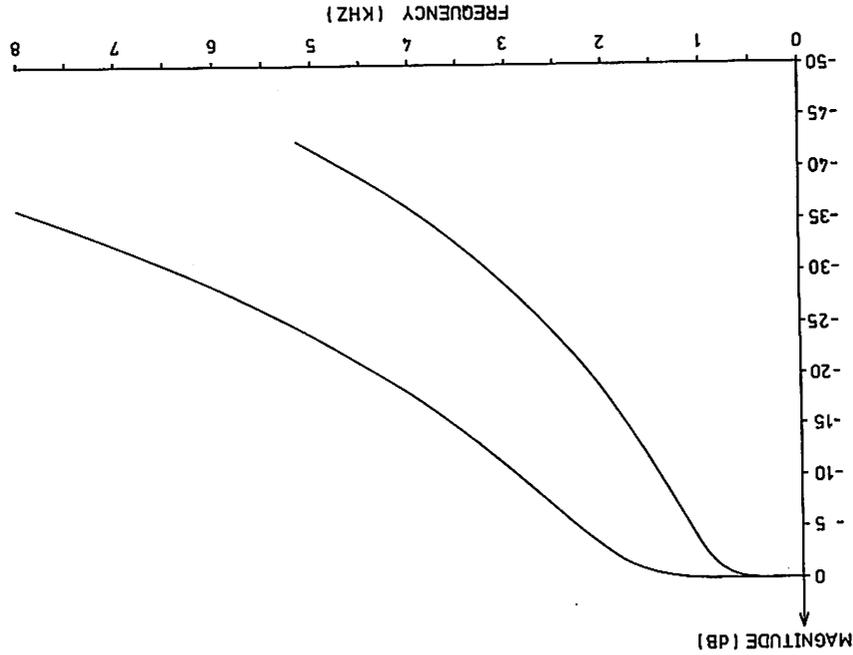
frequencies down into the passband of the discrete-time filter. Therefore it is suitable for the discrete-time bandpass design with a sampling frequency of 8 kHz. The sample and hold function can also be included with the anti-alias filter, as illustrated in Figure 3.7(b). The three resistors would be off-chip ( $\pm 1.0\%$  tolerance). The capacitors could be off-chip ( $\pm 5\%$ ), although it is also practical for the capacitors to be on-chip.

If 4 kHz sampling is used the prefilter then has to roll off its gain response to 30 dB of rejection at 3 kHz. Figure 3.9 shows the magnitude response for the same 3 pole active RC filter with a 3 dB frequency of 1 kHz. It appears to meet the rejection requirement for a 4 kHz sampling frequency, however the gain response has about 0.5 dB of loss at the center frequency of the discrete time bandpass filter (697 Hz). This is unacceptable since it has a distorting effect on the passband response of the bandpass filter with which it is in cascade.

An added advantage in designing the anti-alias filter sufficient for an 8 kHz sampling rate is that it allows the three other switched-capacitor bandpass filters in the "low group" (comprised of four bandpass filters with  $Q = 18$  and center frequencies 697 Hz, 770 Hz, 852 Hz, and 941 Hz) of the touch tone signaling frequencies, to share this one continuous time prefilter. The four bandpass filters in the "high group" could be implemented with the same architecture, but in this case the prefilter would need to use a 3 dB cut-off frequency of 4 kHz, to avoid any magnitude response droop, from the anti-alias low-pass, affecting the bandpass filter characteristics.

Thus it can be seen that system considerations are very important

Figure 3.9: Maximally flat lowpass magnitude responses: 3dB frequencies = 1 kHz and 2 kHz



in the design of switched-capacitor recursive filters with their anti-alias filter, to produce maximum overall chip simplicity.

The discrete-time bandpass filter that has been considered in this design example, requires  $\pm 0.16\%$  and  $\pm 0.17\%$  accuracy on each of the feedback coefficients  $\beta_1$  and  $\beta_2$ , respectively. This is based on the 8 kHz sampling frequency that was chosen for system simplicity of the monolithic circuit application. These accuracy requirements mean that the MOS capacitor ratios must hold to a little less than this tolerance. Previous work by McCreary et al. [18] prior to this research had shown that binary weighted arrays of ratioed MOS capacitors could be fabricated with accuracies of 0.1%. This lead to the expectation that perhaps non-binary ratios of MOS capacitors, like the ones needed in the proposed switched-capacitor filters, could achieve this kind of performance. This was in fact the case as the experimental results in Chapter 5 indicate. The special considerations given to the layout of the non-binary ratioed capacitors for maximum ratio accuracy are described in Section 4.2.

### 3.3 Parameter Design For Second Order Lowpass, Bandpass and Highpass Filters

#### 3.3.1 General

The design of a lowpass, bandpass and highpass filter is presented in this section. These filters were implemented on the NMOS chip described in Chapters 4 and 5.

In the continuous time domain the biquadratic transfer function

is:

$$H_a(s) = \left(\frac{n_2}{d_2}\right) \frac{s^2 + \left(\frac{n_1}{n_2}\right)st + (n_0/n_2)}{s^2 + \left(\frac{d_1}{d_2}\right)st + (d_0/d_2)} \quad 3.12$$

$$= K \frac{\frac{\Omega_0}{Q_z} s + \Omega_0^2}{s^2 + \left(\frac{Q_z}{Q_p}\right)st + \Omega_0^2}$$

Figure 3.1 shows the pair of complex poles  $s_p = -\sigma_p \pm j\Omega_p$  of  $H_a(s)$  and illustrates the definitions of the pole frequency  $\Omega_0$

$$\Omega_0 = \frac{d_0}{d_2} = \sigma_p^2 + \Omega_p^2 = |s_p| \quad 3.13$$

and pole Q

$$Q_p = \frac{d_2}{d_1} \Omega_0 = \frac{1}{d_1} \frac{\Omega_p}{2\sigma_p} = \frac{|s_p|}{2\sigma_p} \quad 3.14$$

The zero frequency  $\Omega_z = |s_z|$  and zero Q,  $Q_z = \frac{|s_z|}{2\sigma_z}$  are defined in a similar way to  $\Omega_0$  and  $Q_p$ . However  $Q_z$  does not play the same important role that the pole quality factor,  $Q_p$  does. For example  $Q_p + \infty$  or  $Q_p$  negative indicates instability while  $Q_z + \infty$  or  $Q_z$  negative are of no consequence. Thus  $Q_z$  is seldom used in characterizing the zeros. In many cases when zeros are being realized in a transfer function they lie at  $s = 0$ ,  $\infty$  or in complex conjugate pairs on the  $j\Omega$  axis (zero transmission at finite frequencies).

If the definitions in Equations 3.12, 3.13, 3.14 are combined,

the biquadratic transfer function can be written in the form:

$$H_a(s) = K \frac{s^2 + 2\sigma_z s + \omega_0^2}{s^2 + 2\sigma_p s + \omega_0^2} \quad 3.15$$

Filters with variations of this biquadratic transfer function are:

(i) Lowpass: 
$$H_a(s)_{LP} = \frac{K}{s^2 + 2\sigma_p s + \omega_0^2} \quad 3.16a$$

or 
$$H_a(s)_{LP} = \frac{K(s^2 + \omega_0^2)}{s^2 + 2\sigma_p s + \omega_0^2}$$

where  $|\omega_0| > |\omega_0|_p$ .

The gain response of a lowpass filter is shown in Figure 3.10(a).

(ii) Highpass: 
$$H_a(s)_{HP} = \frac{Ks^2}{s^2 + 2\sigma_p s + \omega_0^2} \quad 3.16b$$

or 
$$H_a(s)_{HP} = \frac{K(s^2 + \omega_0^2)}{s^2 + 2\sigma_p s + \omega_0^2}$$

where  $|\omega_0| < |\omega_0|_p$ .

The gain response of a highpass filter is shown in Figure 3.10(b).

(iii) Bandpass:

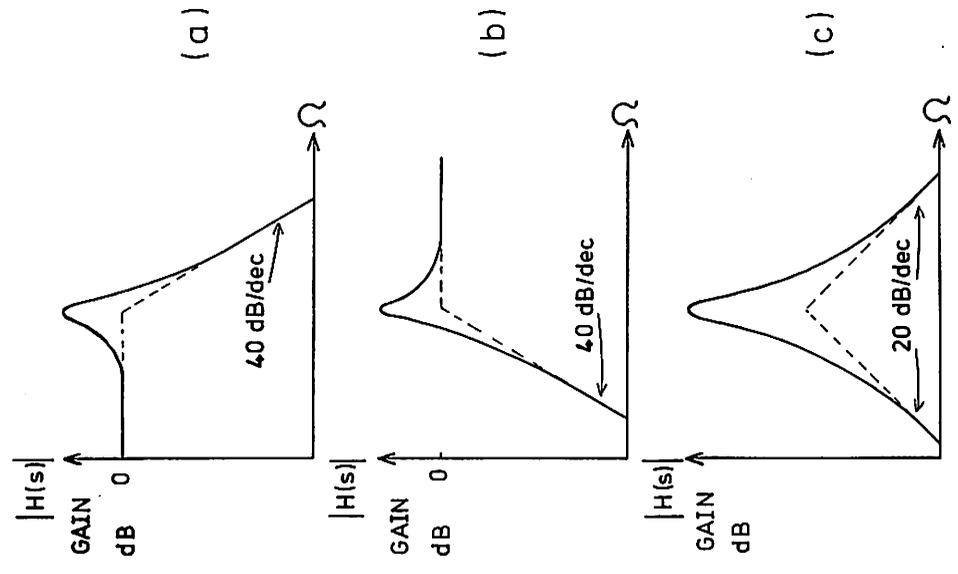


Figure 3.10: Biquadratic Gain Responses.

- (a): Lowpass.
- (b): Highpass.
- (c): Bandpass.

$$D_2 = 1 + \sigma_p T + \left(\frac{\Omega_0 T}{2}\right)^2$$

Thus comparing Equation 3.18 with Equation 3.17 the capacitor

ratios can be written;

$$\alpha_0 = \frac{D_1}{D_2} = \frac{\Omega_0 T}{1 + \sigma_z T + \left(\frac{\Omega_0 T}{2}\right)^2} \tag{3.19a}$$

$$\alpha_1 = \frac{\Omega_0 T}{-2\left[1 - \left(\frac{\Omega_0 T}{2}\right)^2\right]} \tag{3.19b}$$

$$\alpha_2 = \frac{\Omega_0 T}{1 - \sigma_z T + \left(\frac{\Omega_0 T}{2}\right)^2} \tag{3.19c}$$

$$\beta_1 = \frac{\Omega_0 T}{-2\left[1 - \left(\frac{\Omega_0 T}{2}\right)^2\right]} \tag{3.19d}$$

$$\beta_2 = \frac{\Omega_0 T}{1 - \sigma_p T + \left(\frac{\Omega_0 T}{2}\right)^2} \tag{3.19e}$$

Because the frequency axis is warped by the bilinear z-transform, the critical frequencies ( $\omega_0, \omega_0'$ ) in the continuous filter must be prewarped so that the sampled-data filter will yield the desired critical frequencies after this transformation. For example a critical

3.16c

$$H_a(s)_{BP} = \frac{Ks}{s^2 + 2\sigma_p s + \Omega_0^2}$$

The gain response of a bandpass filter is shown in Figure 3.10(c).

The realization of these filter functions is possible with just one of the switched-capacitor second order recursive sections described in Section 2.3.2. The design parameters are the capacitor ratios  $\alpha_0, \alpha_1, \alpha_2, \beta_1$  and  $\beta_2$  in the discrete-time biquadratic transfer function:

$$H(z^{-1}) = K \frac{\alpha_0 + \alpha_1 z^{-1} + \alpha_2 z^{-2}}{1 + \beta_1 z^{-1} + \beta_2 z^{-2}} \tag{3.17}$$

The coefficient values are found by transforming the biquadratic transfer function in the s domain to the z domain form with one of the transformations discussed in Section 3.1. If the filter function requires only the realization of a given amplitude response in the frequency domain, but does not demand any particular impulse response characteristic, then the bilinear z-transform is very good. Application of the bilinear z-transform to Equation 3.15 leads to:

$$H(z^{-1}) = K \frac{\frac{D_1}{D_2} - \frac{\Omega_0 T}{2\left[1 - \left(\frac{\Omega_0 T}{2}\right)^2\right]} z^{-1} + \frac{\Omega_0 T}{2\left[1 - \left(\frac{\Omega_0 T}{2}\right)^2\right]} z^{-2}}{1 - \frac{\Omega_0 T}{2\left[1 - \left(\frac{\Omega_0 T}{2}\right)^2\right]} z^{-1} + \frac{\Omega_0 T}{2\left[1 - \left(\frac{\Omega_0 T}{2}\right)^2\right]} z^{-2}} \tag{3.18}$$

where  $D_1 = 1 + \sigma_z T + \left(\frac{\Omega_0 T}{2}\right)^2$

frequency of 2.5 kHz and sampling frequency of 10 kHz require a continuous design with a critical frequency of about 3.2 kHz. The prewarping technique is described graphically in Figure 3.4. The critical frequencies will map according to the relationship;

$$\Omega_c = \frac{2}{T} \tan\left(\frac{\omega_c T}{2}\right) \quad 3.20$$

( $\Omega$  is the continuous critical frequency while  $\omega_c$  is the discrete domain critical frequency, the one desired in the final discrete-time design).

### 3.3.2 Design Parameters for the Monolithic Filters on the Experimental Test Chip (See Chapter 5)

(i) Lowpass Filter. This lowpass filter is second order with two complex poles and two complex zeros, the latter on the imaginary axis. The poles have a center frequency of 697 Hz  $\pm$  0.5%, and  $Q_u = 18 \pm 1$ . The 3 dB bandwidth frequencies of the final design are therefore,  $\omega_3$  dB =  $2\pi \cdot 677 \cdot 6389$  and  $2\pi \cdot 716 \cdot 3611$ . The continuous domain critical frequencies prewarped for the bilinear z-transform are:

$$\Omega_0 = 2\pi \cdot 714 \cdot 9438$$

$$\Omega_3 \text{ dB} = 2\pi \cdot 694 \cdot 1007 \text{ and } 2\pi \cdot 735 \cdot 8762$$

$$\Delta\Omega = 2\pi(41.7755) = 2\sigma_p$$

$$\text{and } \therefore Q_u = 17.1140$$

The sampling rate is 8 kHz. The resulting feedback coefficients  $\beta_1$  and  $\beta_2$ , based on the bilinear z-transform and defined in Equations 3.19(d) and (c) are

$$\beta_1 = -1.68216$$

$$\beta_2 = 0.97004$$

The complex zeros produce a finite transmission zero at 2 kHz (i.e.,  $f_z/4$ ). Therefore  $\sigma_z = 0$  and  $\omega_0 = 2\pi \cdot 2 \times 10^3$ . A scaling factor of  $K = \frac{1}{25.53}$  was chosen for design considerations given later with the highpass filter design. Based on Equations 3.19(a), (b) and (c):

$$\alpha_0 = 0.9212087 \cdot K = +0.03608$$

$$\alpha_1 = 0$$

$$\alpha_2 = 0.9212087 \cdot K = +0.03608$$

The location of these poles in both the continuous (s) and discrete (z) domain planes are shown in Figure 3.11(a).

A simulation of the frequency response of this sampled data recursive lowpass filter is shown in Figure 3.11(b). This result was obtained with the Digital Network Analysis Program called DINAP [34]. This computer program is described further in Appendix IV.

(ii) Highpass Filter. This highpass filter is second order with two complex poles and two complex zeros, the latter on the imaginary axis. As in the case of the lowpass filter the poles have a center frequency of 697 Hz  $\pm$  0.5%, and  $Q = 18 \pm 1$ . The feedback coefficients  $\beta_1$  and  $\beta_2$  are the same as before:

$$\beta_1 = -1.68216$$

$$\beta_2 = 0.97004$$

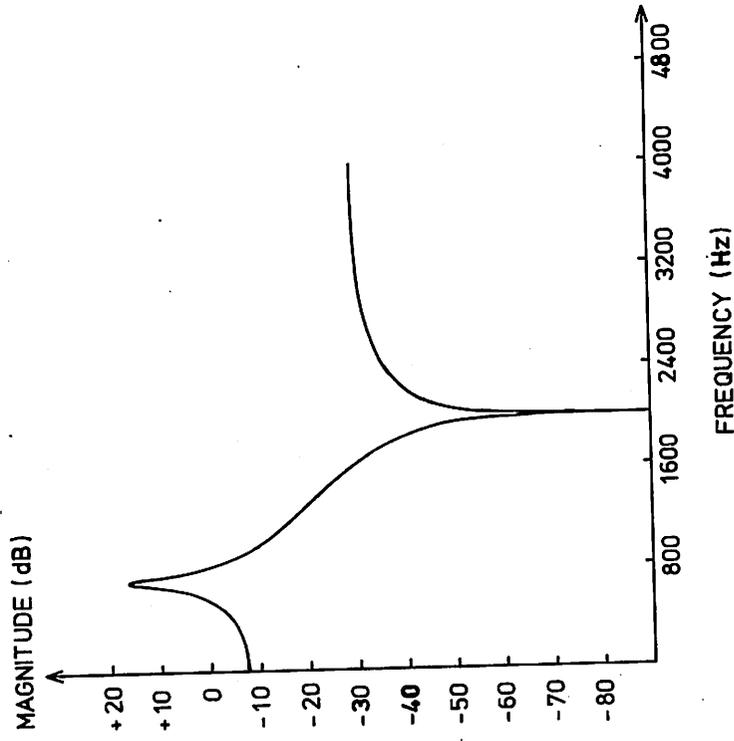


Figure 3.11.b: Simulated frequency response for the sampled-data recursive lowpass filter that was integrated (see figure 5.10 for the programmable filter's lowpass response).

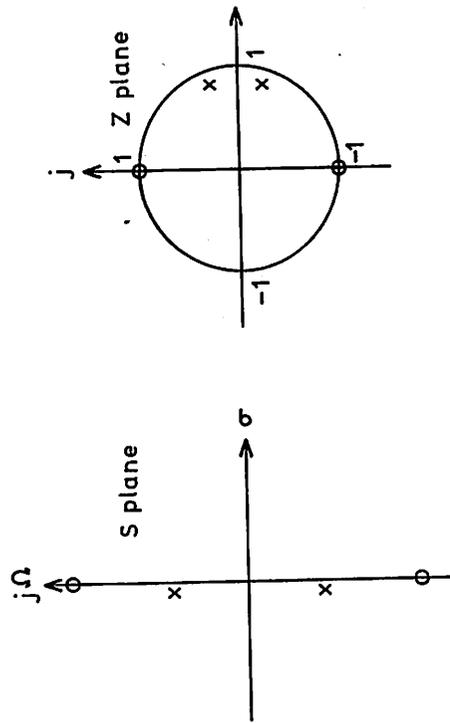


Figure 3.11.a: Pole and zero locations for the lowpass filter in the continuous and sampled-data frequency domains.

The complex zeros produce a finite transmission zero at 240 Hz. Therefore  $\alpha_2 = 0$  and  $\omega_z = 2\pi \cdot 240$ , and prewarped continuous design  $\omega_0 = 2\pi \cdot 240 \cdot 7131$ . Based on Equations 3.19(a), (b) and (c):

$$\alpha_0 = 0.9212087 \cdot K = 0.03608$$

$$\alpha_1 = -1.8097831 \cdot K = -0.07089$$

$$\alpha_2 = 0.9212087 \cdot K = 0.03608$$

where K the scaling factor has been chosen to be  $\frac{1}{25.53}$ , resulting in zero transfer function gain at  $f_0$ :

$$K = \frac{2\sigma_1\omega_0}{\omega_z^2 + \omega_0^2}$$

The location of these poles in the continuous and discrete domain planes are shown in Figure 3.12(a). A simulation of the frequency response of this sampled data recursive lowpass filter is shown in Figure 3.12(b). Once again DINAP was used to obtain this response.

(iii) Bandpass Filter. The bandpass filter, also second order, is derived from the continuous domain form given in Equation 3.16(c). As in the case of the lowpass and highpass the two complex poles have a center frequency of  $697 \text{ Hz} \pm 0.5\%$ , and  $Q = 18 \pm 1$ . Therefore the feedback coefficients  $\beta_1$  and  $\beta_2$  are the same as before:

$$\beta_1 = -1.68216$$

$$\beta_2 = 0.97004$$

The zeros which are at  $\omega = 0$  and  $\infty$  in the continuous domain are at

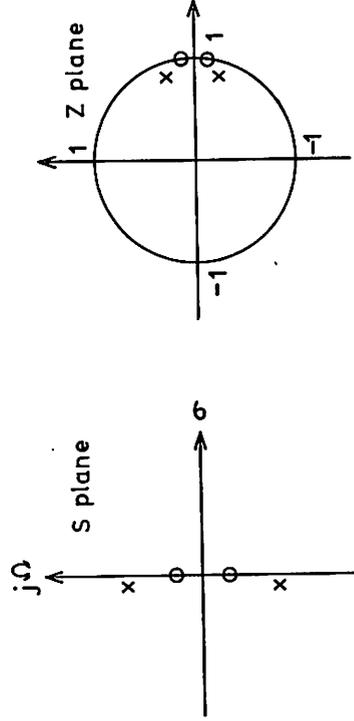


Figure 3.12.a: Pole and zero locations for the highpass filter in the continuous and sampled-data frequency domains.

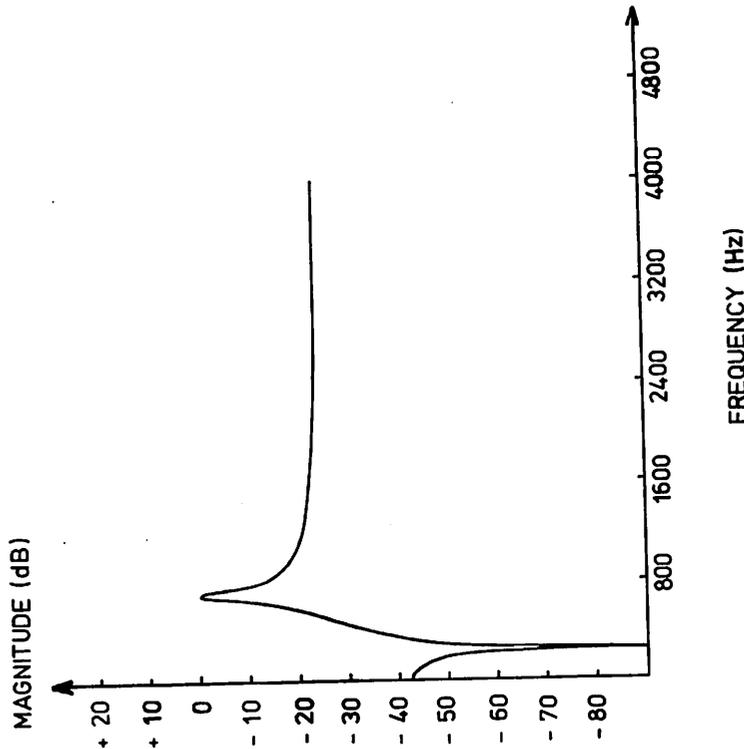


Figure 3.12.b: Simulated frequency response for the sampled-recursive highpass filter that was integrated (see figure 5.11 for the programmable filter's highpass response).

$\omega = 0$  and 4 kHz ( $f_g/2$ ) after the bilinear z-transform (that is zeros are at  $z = +1.0, -1.0$ ). The feedforward coefficients  $\alpha_0 = +1.0$ ,  $\alpha_1 = 0$ , and  $\alpha_2 = -1.0$  place the zeros at these frequencies.

For simplicity in the integrated test chip filter realization the following coefficients were used:

$$\alpha_0 = +0.9212087 \cdot K = +0.03608$$

$$\alpha_1 = 0$$

$$\alpha_2 = -0.9212087 \cdot K = -0.03608$$

As with the highpass and lowpass designs,  $K = \frac{1}{25.53}$ . Figure 3.13(a) shows the pole and zero placement in both the s plane and z plane. The DINAP frequency response simulation for this bandpass filter design is shown in Figure 3.13(b)

For each of the filter designs just given, an integrated realization was made on an experimental test chip. A description of the chip components is given in Chapter 4 and the measured results from these monolithic filters are given in Chapter 5.

### 3.4 High Order Filter Design Examples

#### 3.4.1 6th Order Elliptic Lowpass Filter

This filter is realized with a cascade of three biquadratic sections.

The first section realized in continuous time, performs the anti-alias function as well, and has a sample and hold output. The remaining two sections are implemented with switched-capacitor second order sections.

This 6th order elliptic filter has three pairs of complex conjugate poles and two pairs of complex zeros, the latter being on the imaginary

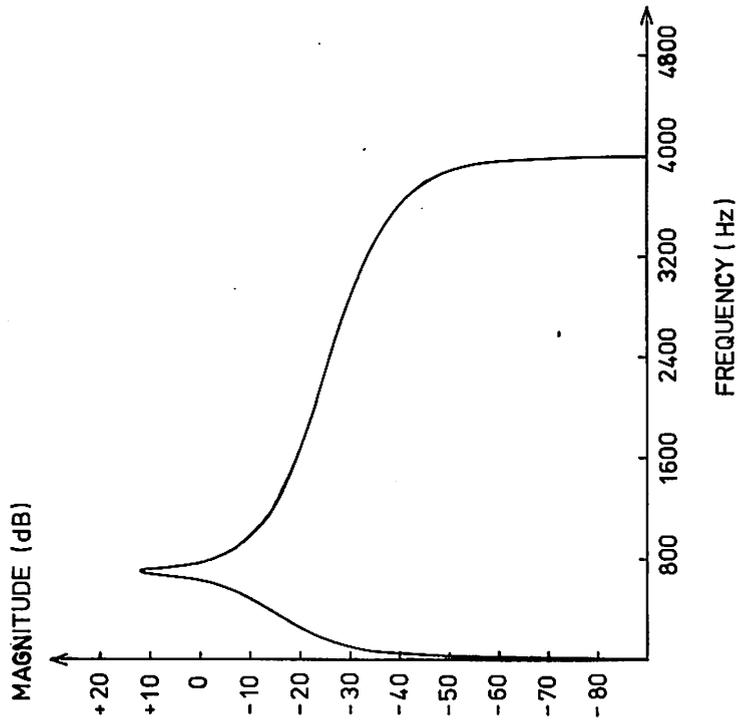


Figure 3.13.b: Simulated frequency response for the sampled-recursive bandpass filter that was integrated (see figure 5.12 for the programmable filter's bandpass response).

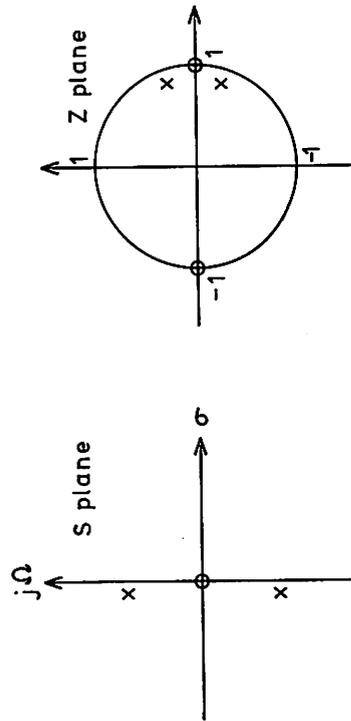


Figure 3.13.a: Pole and zero locations for the bandpass filter in the continuous and sampled-data frequency domains.

axis in the s plane. Figure 3.14 shows the location of these singularities in the s plane. In the s domain such a filter has the transfer function;

$$T(s) = H \frac{\omega_p^2}{(s^2 + s\omega_p/Q + \omega_p^2)^2} \prod_{i=1}^3 \frac{s^2 + \omega_{z_i}^2}{s^2 + s\omega_{p_i}/Q_i + \omega_{p_i}^2} \quad 3.21$$

where H is a multiplier constant and  $\omega_{p_i}$ ,  $\omega_{z_i}$ ,  $Q_i$  are the same notation as used previously in this Chapter.

Mikhael and Keys [19] optimized this transfer function to center the response appropriately within the amplitude specification boundaries of the Pulse Code Modulation communication system's transmit filter.

The result is a filter with ripple peaks not greater than 0.05 dB over the passband from 0 up to 3.2 KHz, 16 dB of attenuation at 4 KHz, and 39 dB or more attenuation of signals above 4.4 KHz. As the second order section sensitivity analysis in section 3.2 showed, a high Q section has more sensitivity of the amplitude response to the filter element variations than a low Q section. Mikhael and Keys' optimization procedure achieved the above specified response with the minimum possible value of section  $Q_p$ s.

To realize a 6th order elliptic filter having these specifications with a cascade of switched-capacitor recursive second order sections, one could optimize in the s plane to minimize  $Q_p$ s and then transform to the z plane. A much simpler approach would be to do the optimization in the sampled-data frequency plane directly. There are computer programs available [20], written in universities and industrial research laboratories, which do the design of sampled-data filters by optimization

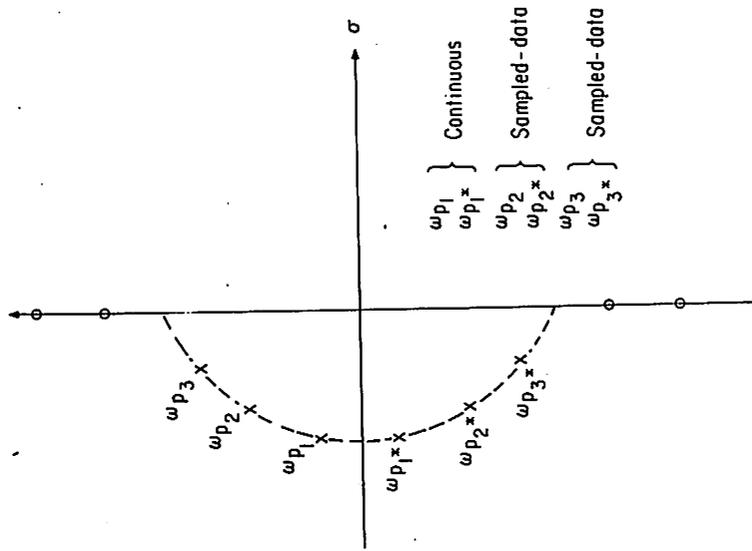


Figure 3.14: 6th Order Elliptic Lowpass Filter's singularity placements in the s-plane. The low Q pole pair could be implemented with either a sampled-data or a continuous time second order section.

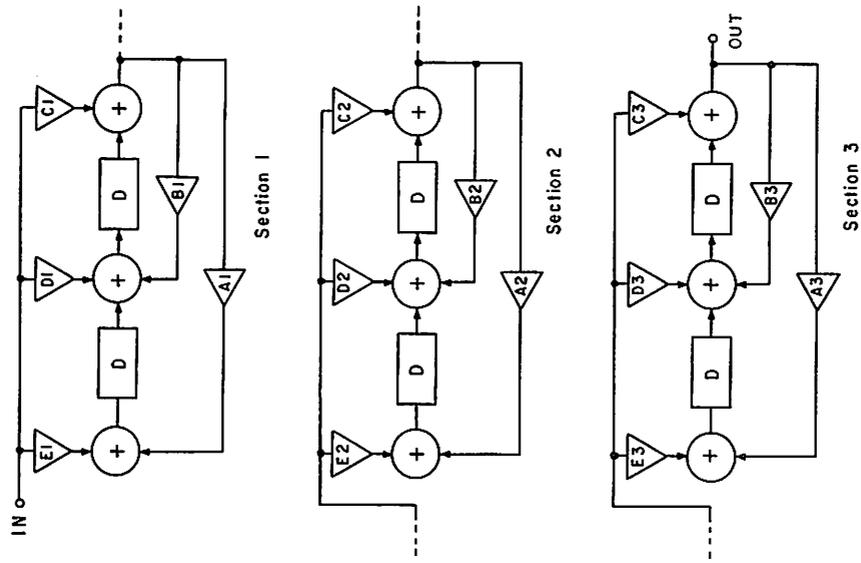


Figure 3.15: Analog Sampled-data 6<sup>th</sup> Order Elliptic Filter realized as a cascade of biquadratic sections.

in the z domain.

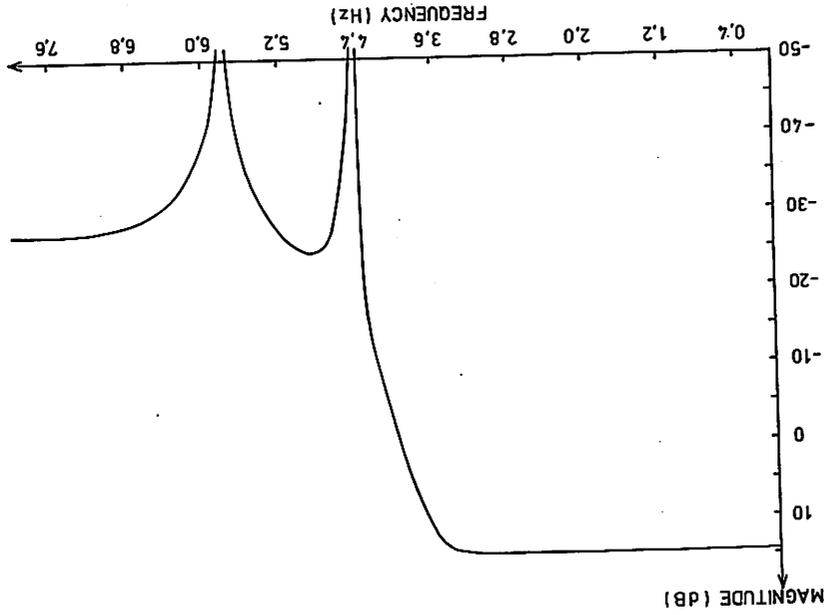
Figure 3.15 shows a cascade of three sampled-data recursive second order sections that implement the sampled-data equivalent of the 6th order elliptic filter transfer function described by Equation 3.21. The optimized filter function parameters for the PCM transmit filter given in Mikhael and Keys' paper were used to derive the sampled-data coefficients with the bilinear z-transform. The sampling frequency for the filter was chosen to be 32 kHz. Prewarping of the critical frequencies ensured that after transformation and frequency axis compression, the final response was equivalent to the desired passband characteristic.

The final design coefficients are given in Table II and the frequency response simulation is shown in Figure 3.16(a) and (b). The passband ripple is within 0.05 dB out to the 3.03 kHz cut-off frequency. The attenuation at 3.4 kHz is 0.6 dB while at 4 kHz it is 16 dB. There is 39 dB or more attenuation of signals above 4.4 kHz. The zeros are placed at 4.5 kHz and 5780 Hz.

The sensitivity of this 6th order elliptic lowpass filter was sufficiently low that a  $\pm 0.2\%$  deviation of the feedback coefficients (these are the most critical ones), resulted in a worst case ripple of 0.064 dB (an increase of 0.014 dB). Simulated responses are given in Figure 3.16(c).

The continuous time anti-alias prefilter with sample and hold can be integrated according to the same scheme presented in Section 3.2 and illustrated in Figure 3.7b. For the 32 kHz sampling rate the maximally flat anti-alias filter should have its 3 dB frequency at 8 kHz. This filter will then provide 33 dB of attenuation at 28 kHz. The off-chip

Figure 3.16.a: 6<sup>th</sup> Order Elliptic Lowpass Filter.  
 Ripple bandwidth = 3.03 kHz.  
 Maximum ripple = 0.05 dB.



i<sup>th</sup> SECTION

	1	2	3
$\omega_0$ (Hz)	2813.4	3532.2	3793.3
$Q_1$	0.582	1.46	5.00
$\omega_2$ (Hz)	$\infty$	4500.3	5781.6
$\alpha_{0i}$	0.04894	1.06005	1.00784
$\alpha_{1i}$	0.09787	-0.82592	-1.28148
$\alpha_{2i}$	0.04894	1.06005	1.00784
$\beta_{1i}$	-1.18483	-1.29588	-1.41995
$\beta_{2i}$	0.38056	0.65014	0.87721

Sampling Rate = 32 kHz

TABLE II. Coefficient values for Figure 3.15.

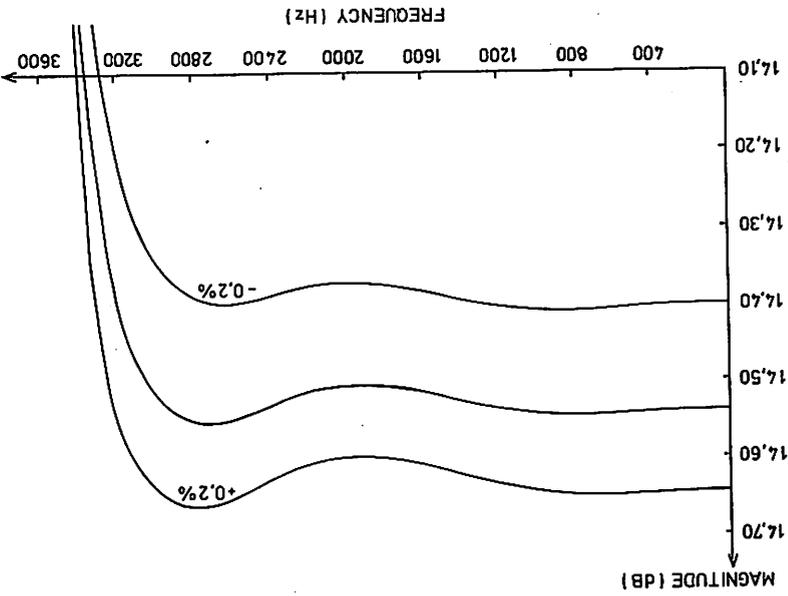


Figure 3.16.c: 6<sup>th</sup> Order Elliptic Lowpass Filter's Sensitivity Performance: Nominal coefficient response, together with responses for  $\pm 0.2\%$  deviation in the coefficients.

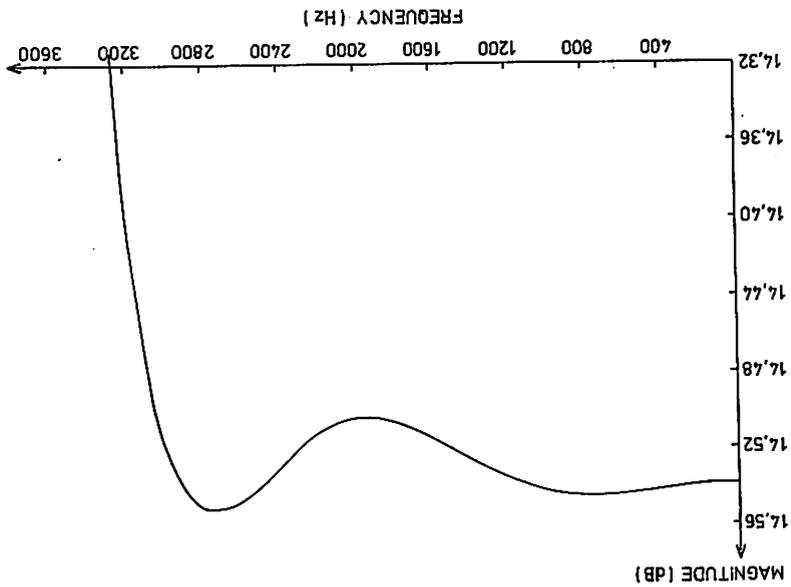


Figure 3.16.b: 6<sup>th</sup> Order Elliptic Lowpass Filter's Passband Response.

discrete components can be  $\pm 1\%$  resistors and  $\pm 5\%$  capacitors. It is possible to consider integrating the two capacitors on the monolithic chip and thus reduce the external component requirement.

While this scheme of implementing the 6th order elliptic lowpass filter employs three switched-capacitor biquadratic sections and the anti-alias filter, it can be reduced to two switched-capacitor biquadratic sections and one continuous time second order section. This is a result of the fact that the sensitivity of this lowpass filter to the  $Q$  and resonant frequency of the first second order section (with lowest  $Q$  and  $\omega_p$ ) is quite low. This sensitivity is sufficiently low that when the first section's  $Q_{p1}$  is varied by  $\pm 0.5\%$  and its  $\omega_{p1}$  by  $\pm 1.5\%$  while at the same time the other two sections have their feedback coefficients changed by  $\pm 0.2\%$ , the result was a 0.25 dB maximum gain variation across the passband for the worst case combination of the parameter deviations. The reason why the first sections  $Q_p$  was varied by  $\pm 0.5\%$  and its  $\omega_p$  by  $\pm 1.5\%$  while the other sections had their feedback coefficients varied by  $\pm 0.2\%$ , was to simulate how the gain response of the lowpass filter would perform if the first section is realized with the continuous time biquad circuit shown in Figure 3.17, the other two sections being realized in switched-capacitor form. Both sets of deviations are compatible with worst case achievable accuracy.

Figure 3.17 illustrates how the continuous time biquad is implemented together with the sample and hold for the switched-capacitor section that follows. The design equations for this biquad are given in Figure 3.7a. The sensitivity equations are given in reference [22]. Since  $K = 1$ , the  $Q$  is only sensitive to the square root of the capacitor

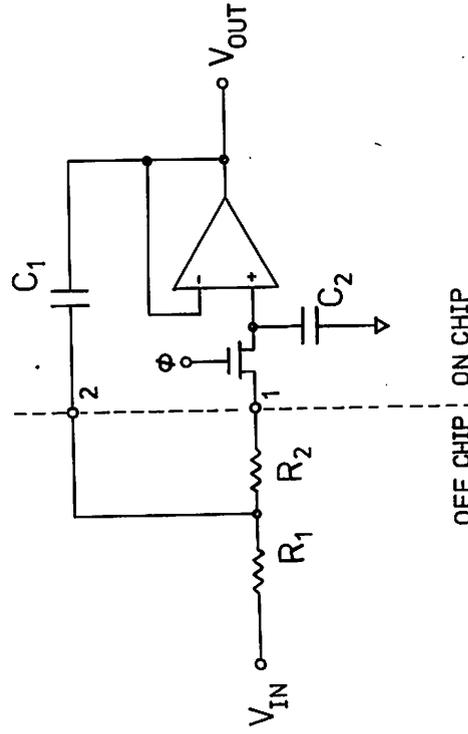


Figure 3.17: Continuous time second order section (biquad) with sample and hold output.

ratio,  $\sqrt{\frac{C_1}{C_2}}$ . The sensitivity of the resonant frequency  $\omega_p$  to each individual component (i.e.,  $R_1, R_2, C_1, C_2$ ) is + 0.5. It is proposed that if  $C_1$  and  $C_2$  are integrated on the filter chip along with the unity gain amplifier, and  $R_1$  and  $R_2$  are  $\pm 1\%$  resistors supplied from off-chip, the  $Q_p$  and  $\omega_p$  can be held within the deviations used for the previous simulations.

For example if  $R_1 = R_2 = 1 \text{ M}\Omega$ , then  $C_1 = 46.6 \text{ pF}$  and  $C_2 = 68.7 \text{ pF}$  to realize the first section  $Q_{p1} = 0.582$  and  $\omega_{p1} = 2\pi \cdot 2813$ . Since  $C_1$  and  $C_2$  are on chip their ratio will have similar accuracy to the switched-capacitor ratios. Nodes 1 and 2 in Figure 3.17 need to be taken out from the IC package. Therefore the parasitic capacitance to ground from the package pin must be included in the total value of  $C_2$ . A typical value for this parasitic capacitance to ground is 1.0 to 1.5 pF (a ceramic package). Thus the variation in the  $\frac{C_1}{C_2}$  ratio might be  $\pm 0.4\%$  for these values of  $C_1$  and  $C_2$ . This translates into a  $\pm 0.2\%$  uncertainty in the  $Q_p$  for this low Q, continuous time section, well inside the acceptable derivations as determined from simulation.

A deviation in the  $\omega_{p1}$  will arise from the  $\pm 1\%$  resistors. Since each has a sensitivity of + 0.5, the deviation in  $\omega_p$  is expected to be  $\pm 1.0\%$ .

The overall 6th order elliptic lowpass filter can be realized with a cascade of two switched-capacitor second order sections (Sections 2 and 3 in Figure 3.15), using three amplifiers per section, and one single amplifier continuous time biquad section (Figure 3.17). The continuous time biquad requires two off-chip resistors having  $\pm 1.0\%$  tolerance. It also performs the anti-aliasing with a sample and hold output for the switched-capacitor sections that follow.

### 3.4.2 10th Order Chebyshev Bandpass Filter

The configuration of this 10th order Chelyshev bandpass filter is based on the modified multiple feedback (MFB) bandpass structure described in the report by D. J. Mayer [23]. The complete structure which consists of five biquadratic sections is shown in Figure 3.18. Each biquadratic section can be implemented with the 3 amplifier switched-capacitor biquadratic block described in Section 3.2. There are two biquadratic sections to each multiple feedback loop. The timing of the switched-capacitor circuit is compatible with this configuration.

The coefficients for this filter are given in Table III. These coefficients were given in the Mayer report and come from the transformation of a proven low noise lowpass multiple feedback filter designed with numerical coefficient matching in the z-domain by Long [24]. This filter has 0.5 dB passband ripple and a cutoff frequency of  $\frac{f}{16}$  ( $f =$  sampling rate). For a sampling rate of 16 kHz, the final modified MFB bandpass filter has a 0.5 dB bandwidth of 2 kHz. The structure has low noise properties and scaling was used between sections to maximize the dynamic range.

Figures 3.19(a) and (b) show the DINAP simulations of the frequency response for this 10th order bandpass having the MFB configuration given in Figure 3.18 and coefficients in Table III. The sensitivity of this filter was tested by shifting the coefficients from their nominal values by  $\pm 0.2\%$ . The result was a worst case deviation in passband ripple of + 0.55 dB from the nominal peak for + 0.2% change in the coefficients, and - 0.32 dB from the nominal minima for - 0.2%.

\*Filter noise considerations will be discussed in the next section. Noise performance of this filter will be given there.

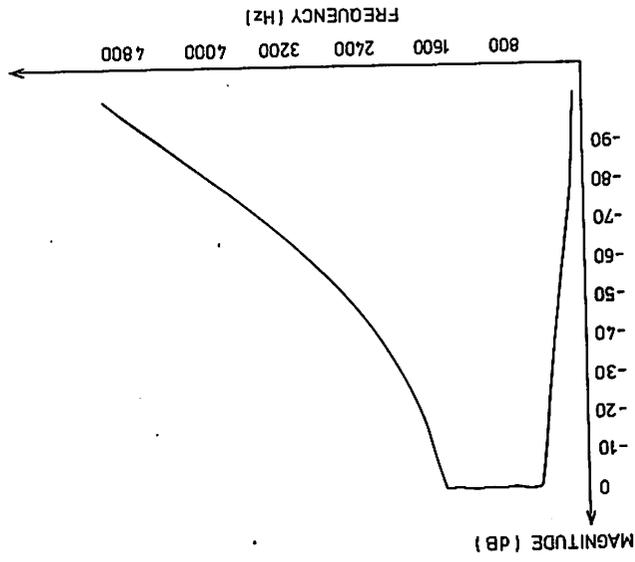


Figure 3.19.a: 10<sup>th</sup> Order Chebyshev Bandpass Response.

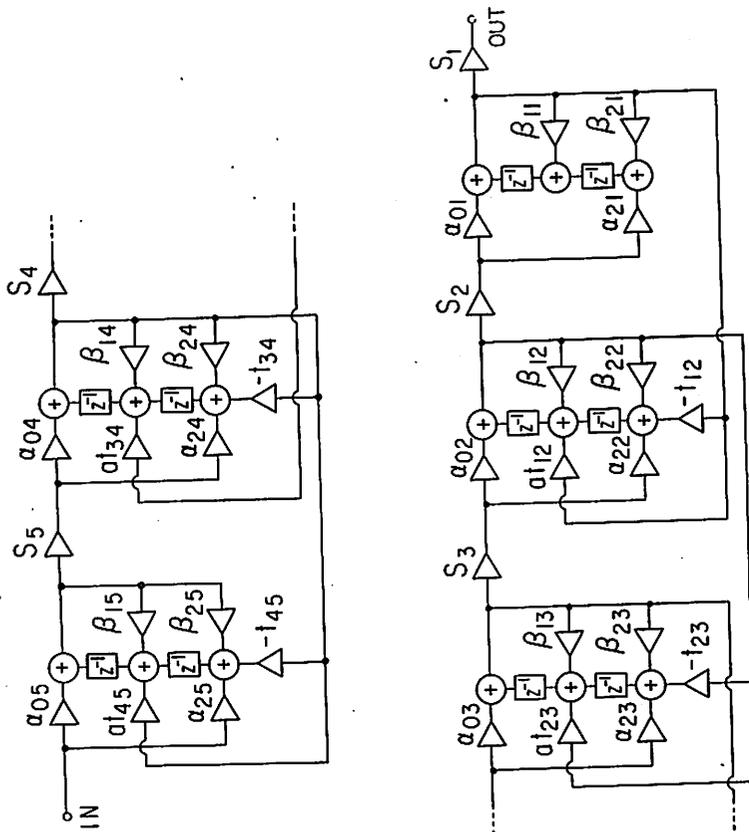


Figure 3.18: Multiple Feedback realization of a 10<sup>th</sup> Order Chebyshev Bandpass Filter.

Section i	1	2	3	4	5
$B_{1i}$	1.63890	1.88396	1.88396	1.88396	1.63890
$B_{2i}$	-0.73984	-1.0	-1.0	-1.0	-0.73984
$A_{0i}$	2.49280	2.08445	1.54183	2.52734	2.50939
$A_{2i}$	-2.49280	-2.08445	-1.54183	-2.52734	-2.50939
$S_i$	0.05492	0.05108	0.06761	0.05205	0.08406
$T_{i,i+1}$	-0.22639	-0.07853	-0.29497	-0.02612	-
$AT_{i,i+1}$	0.21325	0.07397	-0.27785	-0.24607	-

TABLE III. Multiple Feedback Coefficients for the Tenth Order Chebyshev Bandpass Filter (Figure 3.18)

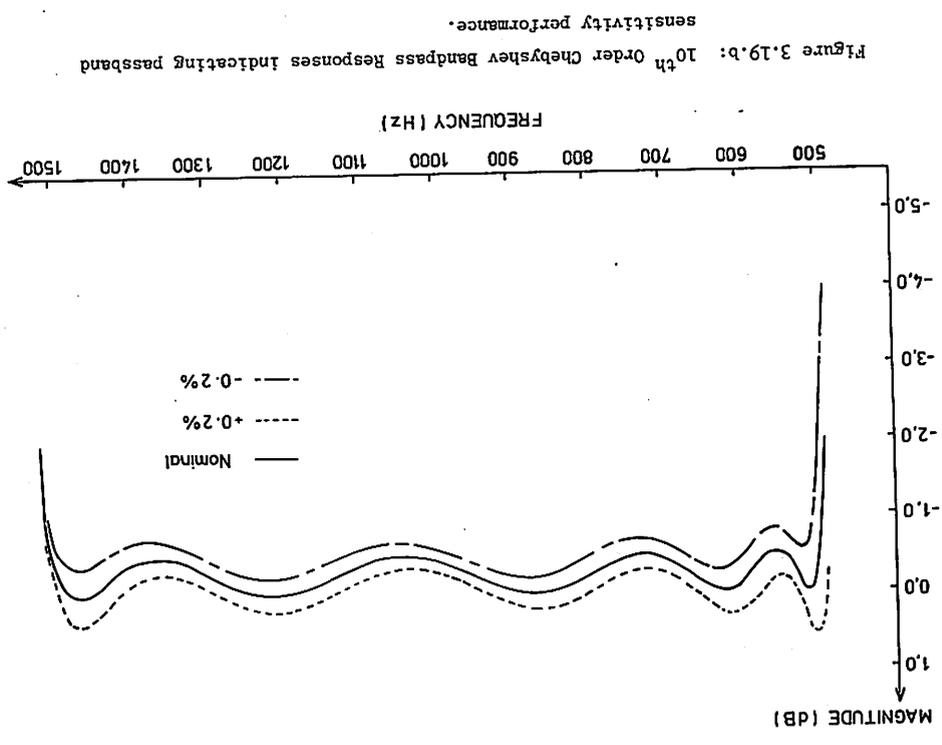
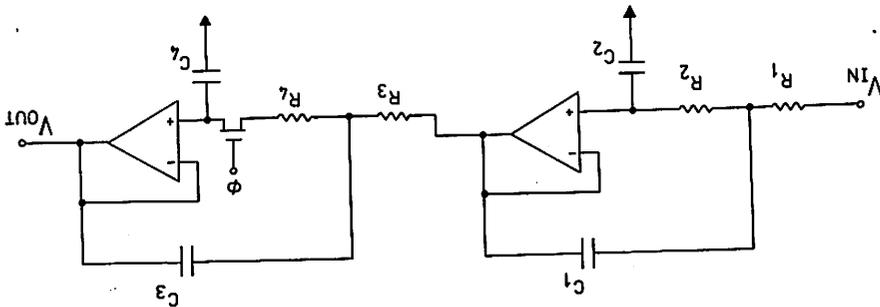


Figure 3.20: 4<sup>th</sup> Order Maximally Flat Anti-Alias Filter with Sample and Hold Output.

change in the coefficients. Figure 3.19(b) shows these responses plotted and the nominal response.

The continuous anti-alias prefilter and sample and hold function can be integrated in the same manner as for the previous switched-capacitor filter designs (scheme is shown in Figure 3.7(b)). Since the sampling rate is 16 kHz, the 3 dB cut-off frequency for this maximally flat prefilter should be 4 kHz. This three pole filter will provide 31 dB or more of attenuation of the second passband response centered about the sampling frequency. The anti-alias filter produces 0.7 dB of attenuation at the upper passband edge of 3 kHz. The sampled-data filter coefficients can be adjusted to give 0.7 dB of peaking at this frequency, and thus produce a uniform equiripple in the passband for the combined responses.

If the amount of attenuation at the frequency of the second passband is not large enough for practical application, the maximally flat lowpass can be increased to fourth order and still only require two amplifiers. This circuit is shown in Figure 3.20 and consists of two low Q second order sections with the second providing the sample and hold function as well. This anti-alias filter has 43 dB of attenuation at 13 kHz with a cut-off frequency of 4 kHz.

### 3.5 Practical Considerations for Monolithic Switched-Capacitor Recursive Filters

The performance of the monolithic switched-capacitor sampled-data recursive filters is controlled by the coefficient accuracy (frequency response) and the noise and distortion contributions from the MOSFET switches and amplifiers (dynamic range). These factors need careful

consideration when designing switched-capacitor filters. Analysis of their effects will now be given followed by the consequences of some other non-identities that have either small or negligible effects.

### 3.5.1 Coefficient Error

In Sections 3.3 and 3.4 the effects of coefficient errors on the frequency response of a number of sampled-data filters were presented. This was based upon either an analytical sensitivity calculation or simulation with the coefficients deviated from their nominal design value. Coefficient error is primarily dependent on the accuracy which the ratioed MOS capacitors can achieve. The absolute value of the ratio is not the important factor since this can be corrected for by adjusting the absolute area ratio on the mask. The most important result is how small the amount of spread occurring in the capacitor ratio is about its normal value. Section 4.1 will describe the method for "laying out" non-binary ratioed capacitors to achieve the minimum spread with standard MOS batch processing. Section 4.2 presents the spread in experimental measurements of the ratioed MOS capacitors fabricated on an experimental switched-capacitor filter test chip.

With ideal amplifiers the coefficient precision is determined by the sum\* of the capacitor ratio accuracies for each ratio that multiplies to form the overall coefficient value through its presence in the signal path.

Amplifier finite gain contributes a coefficient error equivalent to capacitor ratio error. Once again it is possible to correct the absolute value of the ratio to account for the finite gain error

\*If errors are random, this would be an RMS summation.

introduced when the amplifier gain is low. The effect of variations in the amplifier gain on the coefficient value was given in Section 2.2.2.B (sensitivity to amplifier gain).

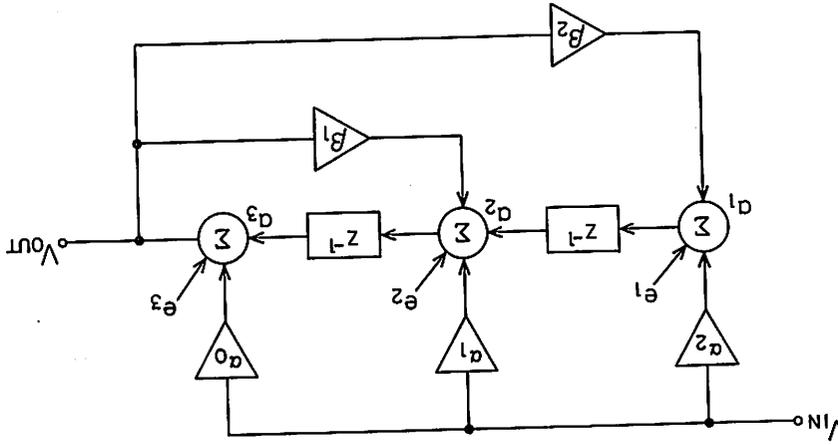
$$\text{i.e. } \frac{\alpha}{S_A} = \frac{1+\alpha}{A} \text{ for } A \gg \alpha$$

Where  $\alpha$  is the coefficient and  $A$  is the amplifier gain. Thus a 10% change in the gain results in 0.03% and 0.3% changes in  $\alpha$  about its nominal value of 2, when  $A$  is 1000 and 100 respectively.

Any error in the amplifier's transient settling time at the end of each phase interval will contribute to coefficient error. If this settling error remains at a constant proportion as signal amplitude varies, the coefficient error is like that from absolute capacitor ratio error or finite gain error. This is the case only when the amplifier has a small-signal settling time limitation. When slew rate and other nonlinear transient effects are present the settling error introduces a source of signal distortion. This distortion source can be minimized by making nonlinear transient time effects, like slew rate, negligible compared to the phase interval. Amplifier transient limitations were discussed for the delay element in Section 2.2.2.F. The same considerations are applicable to the switched-capacitor recursive filters.

The MOS capacitor itself is a very highly stable component. Experimental results have shown that this device has a voltage coefficient as low as 10 ppm/V while the temperature coefficient is 26 ppm/°C [18]. These parameters are already quite small, but since the filter response performance is dependent primarily on the ratio of two capacitors, the filter will be highly insensitive to changes in the temperature

Figure 3.21: Noise and distortion model for a second order section of the direct form.



of the circuit and also to large signals on the capacitors.

3.5.2 Dynamic Range Considerations

A. Noise

The noise sources present in the switched-capacitor "sum, multiply and delay circuit" block were introduced and analyzed in Section 2.2.2.E. The effect of these noise sources on the overall noise performance of the switched-capacitor sampled-data recursive filters will now be considered.

In Section 2.2.2.E the analysis resulted in expressions for the total input referred noise, into the switched-capacitor "sum, multiply and delay" block, due to the amplifiers noise and the capacitively shunted thermal noise from the MOSFET switches. These are described by Equations 2.13(a) and 2.14(a). For a one amplifier switched-capacitor circuit block (Figure 2.12) these equations simplify to:

$$\bar{v}_{OUT_n} = \left[ \left( \frac{C_1}{C_2} \right)^2 + \left( 1 + \frac{C_1}{C_2} \right)^2 \right]^{1/2} \bar{v}_{n_1} \quad 3.22a$$

where  $\bar{v}_{n_1}$  is the total input referred amplifier rms noise. If there is more than one switched input capacitor,  $C_1$  is replaced with  $\sum C_n$ , the sum of the "n" input capacitors,  $C_2$  will be  $C_F$  the feedback capacitor.

(2) Effective Output Noise Due to Switch Thermal Noise:

$$\bar{v}_{OUT_n} = \sqrt{\frac{kT}{C_2}} \quad 3.22b$$

For analysis these noise sources can be introduced at the output of each multiply and sum amplifier in the filter. Figure 3.21 shows the

three noise sources  $e_1$ ,  $e_2$  and  $e_3$  in the second order section. Each of these sources is composed of an amplifier noise component and a switch thermal noise component (Equation 3.22(a) and (b)). The transfer function from node  $a_i$  to the output of the filter is:

$$\begin{aligned} \frac{\bar{e}_{out_i}}{e_i} &= \frac{z^{3-i}}{1+\beta_1 z^{-1}+\beta_2 z^{-2}} = H_a(z^{-1}) \\ &= \frac{z^{3-n}}{1-2r \cos \theta z^{-1}+r^2 z^{-2}} \end{aligned} \quad 3.23$$

The ratio of the output noise variance to the input noise variance is determined by the complex integral in the  $z$  plane:

$$\frac{\bar{e}_{out_i}^2}{e_i^2} = \frac{1}{2\pi j} \oint_{\Gamma} H_a(z) H_a(z^{-1}) z^{-1} dz \quad 3.24$$

The total noise variance at the filter output, based on superposition since the noise sources are uncorrelated, is given by the sum of the squares of these output noise components. Evaluation of the complex integral Equation 3.24 with Equation 3.23, can be done using the integral tables in Jury [21]. The result is:

$$\frac{\bar{e}_{out_i}^2}{e_i^2} = \frac{1+r^2}{(1-r^2)(1+r^2-2r^2 \cos 2\theta)} \quad 3.25a$$

$$\bar{e}_{out_n}^2 = \sum_{i=1}^M e_{out_i}^2 \quad 3.25b$$

Thus knowing the input RMS noise of the amplifier and the size and ratio of the switched-capacitors, the total RMS noise,  $e_{out_n}^2$ , at the output of the second order section can be calculated. It can be seen from Equation 3.23 that the noise sources will be filtered to the output. If the second order section has a high  $Q$  ( $r$  small) the noise will be amplified in the passband region of the resonant frequency.

An example calculation of the RMS noise at the output of a monolithic switched-capacitor second order recursive section, as shown in Figure 2.13, will now be given. This calculation is based on Equations 3.22(a) and (b), using the following assumptions that are good examples of the practical situation.\* The MOS amplifiers have an RMS equivalent input noise of 50  $\mu$ V, the feedback capacitance for each of the three amplifiers is 4 pf, and the ratio of  $\Sigma C_n/C_F$  for amplifiers 1, 2 and 3 respectively is 1.0, 2.7, and 1.0. The amplifier related noise at the filter output is therefore going to be 112  $\mu$ V, 230  $\mu$ V, and 112  $\mu$ V for amplifiers 1, 2 and 3 respectively, from Equation 3.22(a). The MOSFET switch related noise at each amplifier output is 32  $\mu$ V rms. These two components are what make up  $e_1$ ,  $e_2$  and  $e_3$  in Figure 3.21.

It can be seen that the dominant source of noise arises from the amplifier noise. The transfer function of this noise to the "sum, multiply and delay" block output is highly dependent on the size of the capacitance ratio for the  $\beta_1$  coefficient. The worst case situations are when the second order section realizes a high  $Q$  filter with a large ratio of sampling frequency to resonant frequency ( $f_s/f_0$ ). If the

\*Chapters 4 and 5 describe an experimental fully integrated filter and its measured performance.

A DINAP simulation of the noise behavior exhibited by this second order section bandpass filter is given in Figure 3.22. This simulation was with a 14 bit floating point rounding on the coefficient multiplications, thus endeavoring to simulate the switched-capacitor filter as realistically as possible (i.e. amplifier noise and switch thermal noise).

Noise simulations were also made for the switched-capacitor realizations of the 6th order elliptic lowpass and the 10th order bandpass Chebyshev filters. Once again 14 bit rounding was used for these simulations of the digital filter equivalent circuits, a worst case situation. The results are given in Figures 3.23 and 3.24, lowpass and bandpass filters respectively.

B. Distortion

The distortion performance can be characterized in a similar manner to the noise analysis. There are two sources of distortion; one from the amplifier nonlinearities present in its transfer curve, and the other occurring when the ON-resistance of the MOSFET switches produces a finite time constant in the charging of the switched-capacitors that is comparable to the phase interval.

The amplifier distortion can be referred to the output of each amplifier in the filter. Thus distortion sources from the three amplifiers in the second order section will be introduced at  $e_1$ ,  $e_2$  and  $e_3$  ( $v_{d1}(f)$ ,  $v_{d2}(f)$  and  $v_{d3}(f)$ ) in the circuit diagram of Figure 3.21. The amplifier distortion will have a frequency spectrum consisting of harmonics of the fundamental large signal frequencies present in the filter.

The finite resistance of the MOSFET analog switch is another possible

Q is high but the ratio  $\frac{f_s}{f_0}$  is near to four, this noise component is reduced drastically because  $\beta_1$  now has a small value ( $\theta \approx 90^\circ$ ).

For a bandpass filter with  $Q = 18$ ,  $f_0 = 697$  Hz and  $f_s = 8$  kHz, the transfer function for the noise from Equation 3.25 is:

$$\frac{e_{out}^2}{e_1^2} = 0.970042$$

$$\frac{e_{out}^2}{e_2^2} = 62.545$$

$$2r \cos \theta = 1.68216$$

Therefore the total RMS noise at the filter output is;

$$\frac{e_{out}^2}{e_1^2} = 62.545[e_1^2 + e_2^2 + e_3^2]$$

- where  $e_1 = 116 \mu V$
- $e_2 = 232 \mu V$
- $e_3 = 116 \mu V$

$$\therefore e_{out} = 17.8 \text{ mV. rms.}$$

This noise is bandlimited by the filter to within its passband region. While this noise level is quite high it is worthwhile to note that assuming a  $\pm 5.0$  V maximum signal swing, the noise sources  $e_1$ ,  $e_2$  and  $e_3$  are equivalent to the quantization noise from 14 to 15 bit

accuracy\* on the floating point coefficient multiplies, assuming this high Q filter was implemented as a digital filter.

\*Quantization noise has a uniform power density spectrum of  $\frac{2^{2b}}{12}$ , where b is the number of bits. The MOS amplifiers have a 1/f noise component in addition to the uniform thermal noise spectrum. If the passband of the switched-capacitor filter is at a higher frequency than the 1/f corner frequency then the noise performance of the switched-capacitor filter can be approximated by simulating the filter with the noise analysis in DINAP and introducing a uniform quantization noise equivalent to the amplifier spot noise.

Figure 3.23: DINAP output noise power spectral density simulation for the 6<sup>th</sup> order lowpass chebyshev filter with 14 bit rounding computation.

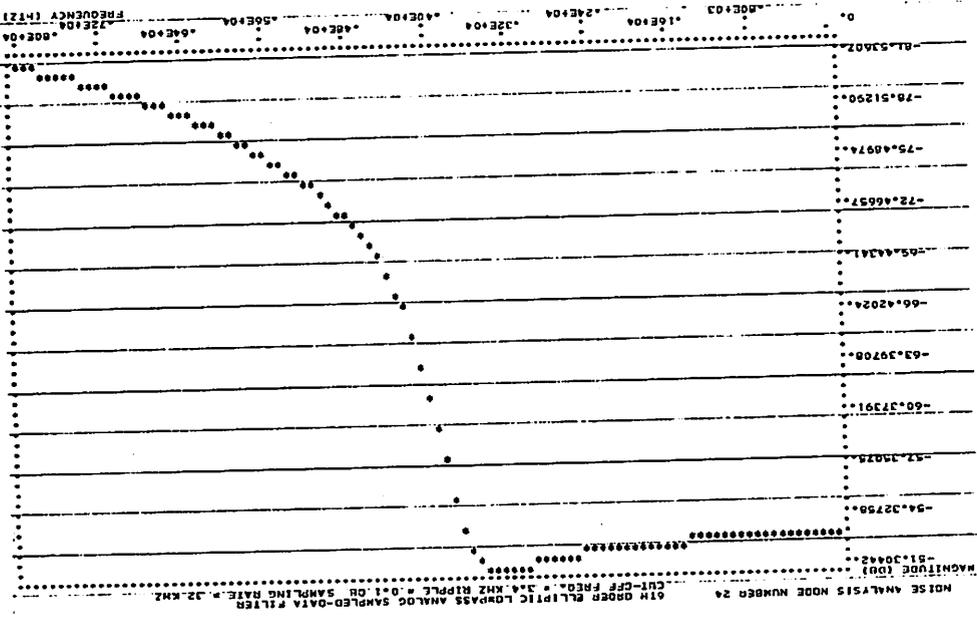
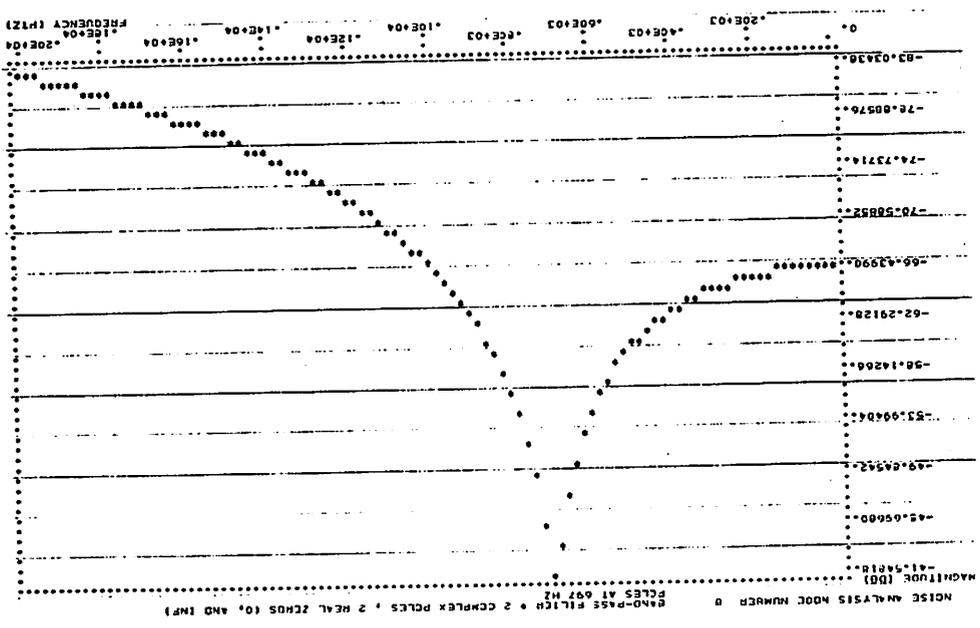


Figure 3.22: DINAP simulation of the second order bandpass filter output noise power spectral density, under 14 bit rounding computation. The filter has a Q of 18.



source of output signal distortion in the switched-capacitor filter.

Consider the circuit in Figure 2.12(a) with M1 driven by  $\phi_1$  and M2

by  $\phi_2$ ;  $t = nT$  at the start of  $\phi_1$ .

At the end of the  $\phi_1$  interval:

$$V_{C_1}(nT + \frac{T}{2}) = V_{IN}(nT) \left(1 - e^{-\frac{T}{2R_S C_1}}\right) \tag{3.27a}$$

where  $R_S$  is the "ON" resistance of the MOSFET and  $T$  is the clock period.

At the end of the  $\phi_2$  interval:

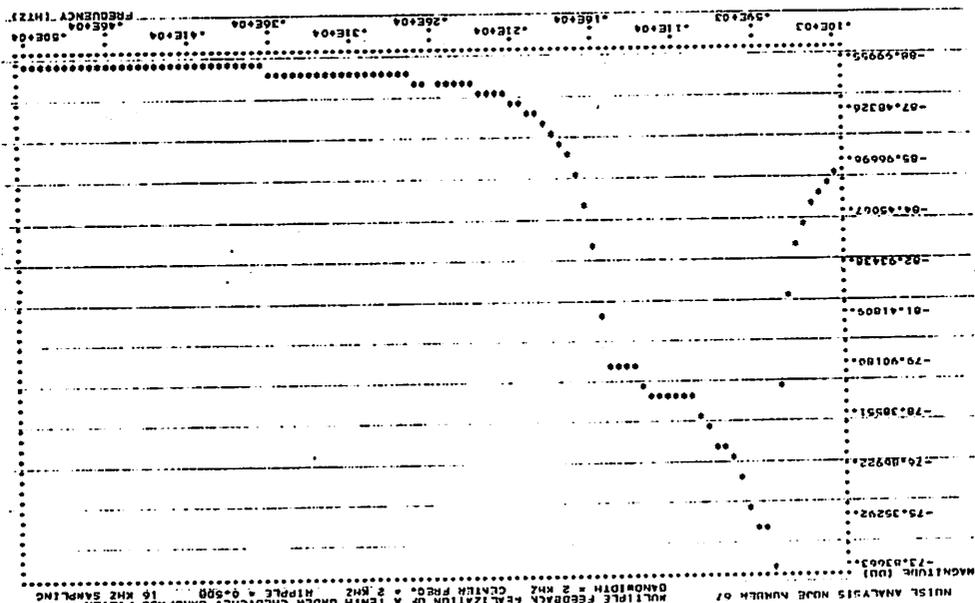
$$V_{OUT}(nT+T) = V_{IN}(nT) \left(\frac{C_1}{C_2}\right) \left(1 - e^{-\frac{T}{2R_S C_1}}\right) - V_{IN}(nT) \left(\frac{C_1}{C_2}\right) e^{-\frac{T}{2R_S C_1}} \left(1 - e^{-\frac{T}{2R_S C_1}}\right) \tag{3.27b}$$

If  $R_S$  is a constant the first term in this equation represents the multiplied signal with some error that is indistinguishable from capacitor ratio error. The second also is like some capacitor ratio error.

However  $R_S$ , the drain to source resistance of the MOSFET in the "on" state, is highly dependent on the gate to source voltage. For large signals the  $V_{GS}$  of the switch will change, thus changing  $R_S$  as the signal varies. This is then a source of distortion, as described by Equation 3.27(b) where  $R_S$  is now a function of the signal voltage. As long as  $R_S$  remains small enough throughout the signal swing, such that the  $R_S C_1$  time constant is negligible compared with the phase interval, then the distortion level will be small.

The distortion from the amplifiers and the switches sees a frequency response transfer function to the output of the filter described by Equation 3.23. The distortion is bandlimited by the frequency

Figure 3.24: DINAP output noise power spectral density simulation for the 10<sup>th</sup> order bandpass chebyshev filter with 14 bit rounding computation.



response of this transfer function. The distortion power spectrum from these source nodes ( $e_1$ ,  $e_2$ , and  $e_3$ ) can be summed at the filter output.

Finally with the noise and distortion performance characterized, the dynamic range can be calculated. This involves the ratio of RMS signal for a specific % of distortion divided by the RMS noise voltage; the ratio is given in decibels. 1% distortion occurs when the root mean square of the distortion harmonics at the filter output, is 40 dB below the fundamental signal voltage level.

### 3.5.3 Second Order Practical Considerations

Section 2.2.2 analyzed the effects of the MOS analog switch overlap capacitance (clock feedthrough) and junction leakage current on the performance of the switched-capacitor multiply and delay. The device one needs to consider is the unity gain feedback switch. The result is that these parasitics simply cause a D.C. offset voltage on the output signal of the multiply and delay, similar to that from amplifier input offset voltage.

In the case of the switched-capacitor recursive filter, this D.C. offset source sees the D.C. transfer function of Equation 3.23 to the output. The signal passing through the switched-capacitor filter will receive a D.C. offset component. This has no harmful effect on the frequency response, the only undesirable aspect is that if this offset voltage is large (much greater than 100 mV say), the maximum signal for a given level of distortion will be reduced, due to asymmetrical clipping of the signal. Thus the dynamic range is reduced.

In metal gate MOS technology the overlap capacitance can be quite large (15 pF/cm) and may cause an offset voltage in the order of half

a volt or larger (Equation 2.12).

The D.C. offset voltage will be different at each of the filters' internal nodes, and in some cases will be negative at one and positive at another. This situation reduces the dynamic range even more since the maximum signal swing will have to be much less than for an all positive D.C. voltage situation.

Since the feedthrough offset can be much larger than the amplifier offset and leakage offset when metal gate MOS is used, a cancellation scheme was employed on the metal gate MOS experimental filter chip to minimize the clock feedthrough voltage (charge). This scheme is described in Section 4.3. Experimental results are given in Section 5.3. If the filter is implemented with self-aligned silicon gate technology, the clock feedthrough is significantly reduced to a negligible level.

Parasitic junction capacitances from signal nodes to substrate or ground do not degrade the performance of the filter since these nodes are either voltage driven by the amplifier or are at virtual ground (inverting input). The reasons are the same as those presented in Section 2.2.2.C for the multiply and delay circuit (Figure 2.7). In silicon gate NMOS (with 30  $\Omega$ -cm substrate) these parasitic junction capacitances are in the order of 10 fF for typical signal node junctions. In metal gate NMOS this capacitance can be up to ten times larger. This presents no limitation on the three amplifier switched-capacitor recursive filter.

CHAPTER 4

DESIGN OF THE COMPONENTS IN A FULLY INTEGRATED SWITCHED-CAPACITOR RECURSIVE FILTER

Introduction

A fully integrated switched-capacitor second order recursive filter was fabricated in the ERL integrated circuits laboratory using a four mask single channel (enhancement) aluminum gate NMOS process (appendix A). This chip included all elements illustrated in the full circuit diagram of figure 2.13, including the sample and hold amplifier.

Section one of the chapter describes the precision ratioed capacitor layout, while section two goes into the design of the NMOS amplifier that uses single channel enhancement transistors. Since many amplifiers are integrated on the one chip in these filters, the amplifier design was focused on it having small area, low power, high gain, and fast transient performance. Its performance was to be insensitive to processing parameters. Section three describes the circuit employed for minimizing the clock feedthrough-induced DC offset present at each amplifier output.

4.1 Design of Precision Non-Binary Capacitor Ratios

The ratioed MOS capacitors are implemented in metal gate NMOS as illustrated in Figure 4.1(a), with thermally grown oxide between metal and heavily doped silicon. This diagram also shows the amplifier connected in a switched-capacitor circuit. Note that the inverting input has no path for leakage current other than the minimum size source diffusion of the feedback switch. The low impedance output of the amplifier drives the n+ diffusion side of the capacitor and thus

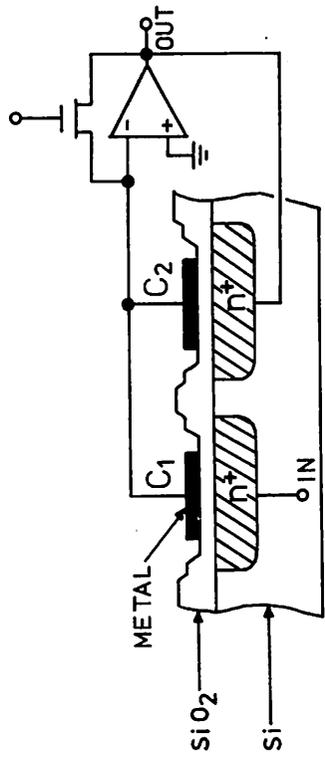


Figure 4.1.a: Ratioed capacitors implemented in metal gate NMOS technology.

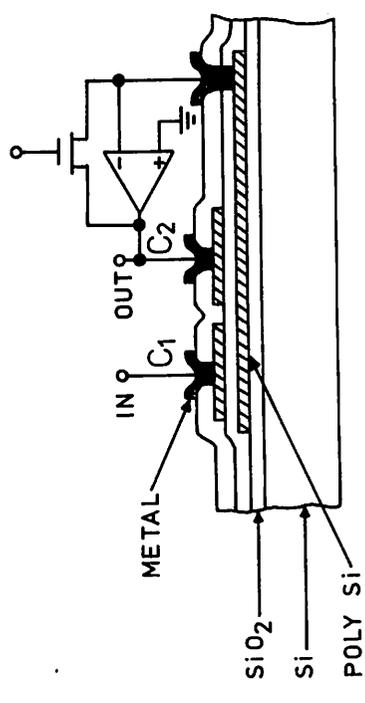


Figure 4.1.b: Ratioed capacitors implemented in double polysilicon gate NMOS technology.

the parasitic junction capacitance, from the diffusion plate of the capacitor to substrate, has no adverse effect on the switched-capacitor circuit operation.

With double polysilicon NMOS (enhancement and depletion transistors) the capacitors can be realized with thermally grown oxide between the two layers of heavily doped polysilicon [26]. This structure is shown in Figure 4.1(b). Once again the connection of the amplifier is indicated.

With each of these processes the ratio of two capacitors is equal to the ratio of the areas defining those capacitors. This is because the permittivity of the insulator,  $\epsilon_{OX}$ , and the insulator thickness  $t_{OX}$  are very uniform in these standard MOS processes having a thermally grown oxide dielectric. Deposited oxides and nitrides exhibit dielectric relaxation effects which can seriously limit capacitor ratio accuracy.

In either of the MOS processes described the capacitance ratio is solely controlled by the area ratio defined on one mask; the metal mask in metal gate NMOS, and the second polysilicon mask in the double polysilicon NMOS. Special precautions in the layout of this mask contribute significantly to the maintenance of accurate capacitance ratios, insensitive to processing variables like different etching conditions from wafer to wafer, from die to die, and from one capacitor edge within a die to another. The wafer to wafer "edge uncertainty" arises from variations in the amount of etching needed to etch through the metal or polysilicon thickness. Since the metal and polysilicon are deposited films their thickness is not accurately controlled, e.g.

perhaps only to  $\pm 30\%$  on a 1.0  $\mu\text{m}$  film thickness. The die to die and within one die capacitor edge variations arise from proximity changes in the chemical etchant's rate of reaction, where in one region the chemical etchant is exhausted more quickly than in another. If plasma etching is used, this second source of edge variation is greatly reduced. The mask working plate itself has a source of edge shift due to variation in emulsion thickness and development time.

The special precautions employed in the layout of the ratioed capacitors are the following [18].

(i) The two capacitors' area ratio  $\frac{A_1}{A_2}$  must equal the two capacitors' perimeter ratio  $\frac{P_1}{P_2}$  in order that they be insensitive to the edge shift arising from etchant undercutting and changes in the mask dimensions. In the case of non-binary ratios,  $A_1$  and  $A_2$  are not multiples of a basic cell as is the case for binary ratios.

(ii) The layout of the capacitors should be such that each edge in the pattern area has the same spacing to a surrounding pattern edge. In such a layout every capacitor will show a uniform etching front to the etchant.

(iii) To eliminate the effect of long range oxide gradients the capacitors should be laid out with a common centroid pattern. Experimentally, oxide gradients of 10-100 ppm/mil have been observed [18].

(iv) The capacitor layout should be insensitive to mask misalignment.

Figure 4.2 shows a geometric pattern that could be either the metal or the second poly mask. It satisfies the layout precautions (i) to (iv). If double polysilicon NMOS technology is used the

interconnection of the poly II plate of the capacitor is done with a metal layer. These capacitors are then alignment insensitive. If metal over n<sup>+</sup> diffusion (metal gate NMOS) is used for realizing the capacitors, then interconnecting metal "stubs" form the common node. Figure 4.3 illustrates the complete layout of two ratioed MOS capacitors, constructed with metal gate NMOS. They satisfy precautions (i) to (iv) as much as possible, within the restraints of interconnect requirements. The capacitance is defined by the metal edge across its width "D" and the thin oxide edge at the ends of its "L" dimension (metal overlaps thick oxide). The capacitances remain constant as long as the metal remains inside the width of the thin oxide regions and overlaps at the ends. The capacitance resulting from the interconnecting metal "stubs" is also constant. Neglecting the area of these metal interconnection "stubs" (which is very small), the capacitor ratio is defined by:

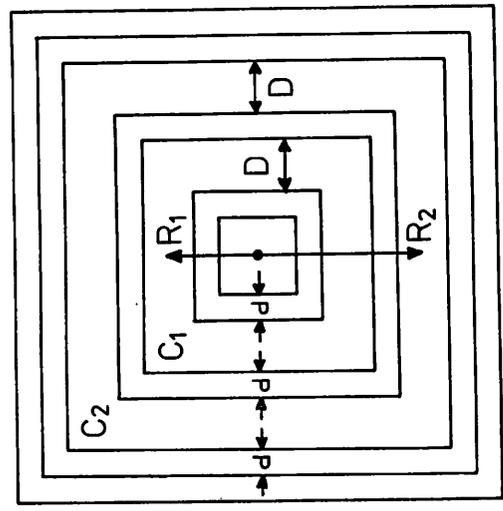
$$\frac{C_1}{C_2} = \frac{A_1}{A_2} = \frac{(L_1 - 2\delta')(D - 2\delta)}{(L_2 - 2\delta')(D - 2\delta)} = \frac{L_1 - 2\delta'}{L_2 - 2\delta'} \quad 4.1$$

where  $\delta$  = deviation in the metal edge from design value

$\delta'$  = deviation in the thin oxide edge from design value.

It has previously been observed [26] that the thin oxide edge is more precisely and smoothly defined than the metal edge. The scanning electron microscope photograph in Figure 4.4 shows the surface of a metal NMOS capacitor (part of that whose layout is given in Figure 4.4). The superior quality of the thin oxide edge compared to the metal edge can be seen.

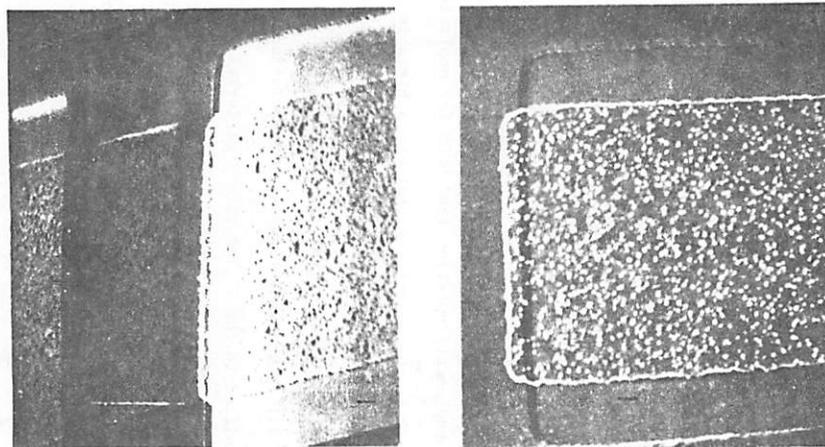
Provided  $\delta'$  is extremely small compared with the dimensions  $L_1$  and  $L_2$ , then  $\frac{C_1}{C_2}$  will have accuracy that is effectively independent of  $\delta'$ . A conservative estimate for  $\delta'$  is 0.4  $\mu\text{m}$  [26]. Therefore to achieve 0.1%



$$\frac{C_1}{C_2} = \frac{\text{AREA}_1}{\text{AREA}_2} = \frac{\text{PERIMETER}_1}{\text{PERIMETER}_2} = \frac{R_1}{R_2}$$

$d$  = MINIMUM FEATURE SIZE

Figure 4.2: Layout configuration for precision ratioed MOS capacitors (metal or the second poly pattern).



1 μm ]

Figure 4.4: Two Scanning Electron Microscope views of the metal and thin oxide edges in a ratioed MOS capacitor (metal gate NMOS technology).

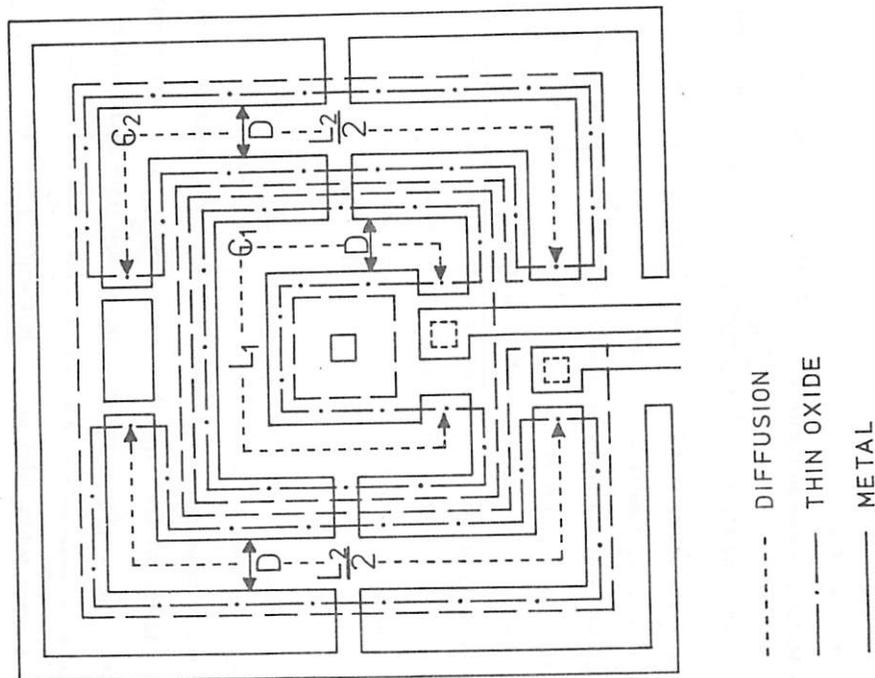


Figure 4.3: Metal Gate MOS mask layout of two non-binary ratioed capacitors that have a ratio close to the value  $\frac{C_1}{C_2} = 0.5$ .

However, since many such amplifiers may be present on one chip, the area and power must be kept to a minimum. The amplifier should be capable of fast settling when driving capacitive loads. It should also be insensitive to device parameters, especially threshold voltage. Amplifier noise, a major limitation on the filter's dynamic range, must be as low as is possible within the other design restraints. In order to minimize the effect that finite amplifier gain has on the filter response, without resorting to capacitor ratio adjustment, the amplifier design was directed towards obtaining an open loop gain of 2000. The design also concentrated on low power, small area and fast settling in the presence of capacitive loads.

Previous work had shown that a low gain operational amplifier could be realized with single channel NMOS technology [27]. At the time this filter work started, depletion load NMOS was not available as a technology in the ERL IC laboratory. Since then attention has been paid to the advantages of enhancement/depletion load NMOS for amplifier design [29], [30]. It is shown in these articles that the achievable gain per stage for a simple inverter is much higher with depletion transistor loads than enhancement transistor loads, given the same silicon area. However, a single channel (all enhancement transistors) operational amplifier was designed and realized in the IC laboratory at Berkeley with performance comparable to the depletion load amplifiers in almost all aspects, including silicon area. In addition to the sampled-data recursive filters, this amplifier is suitable for the sense circuitry application in charge coupled devices. MOS amplifiers having only enhancement transistors are needed for use with charge coupled devices because the depletion device is not present.

Figure 4.5(a) shows the full circuit diagram of the operational

matching of  $\frac{C_1}{C_2}$ ,  $\frac{L_1}{2}$  must be approximately 400  $\mu\text{m}$  (16 mil). This is also a conservative calculation because it assumes  $C_2$  does not change.  $C_2$  will also be affected by  $\delta'$  in the same manner as  $C_1$ , so the effect of  $\delta'$  on the ratio  $\frac{C_1}{C_2}$  will be somewhat reduced. If  $L_1$  and  $L_2$  are very long the jaggedness in the metal edge will average out its effect on the area of  $C_1$  and  $C_2$ .

The layout as shown in Figure 4.3 can realize the ratio  $\frac{C_1}{C_2} = 2.0$  independent of  $\delta$  and  $\delta'$ , since  $\frac{C_1}{C_2} = \frac{L_1}{(L_2 - 2\delta')} = 2.0$  when  $L_1 = 2L_2$ . This is because  $C_2$  has one split and  $C_1$  has two splits. If this layout has only one split in  $C_2$  then it is suitable for  $\frac{C_1}{C_2}$  ratios that are close to 2.0, while simply adding a second split to  $C_2$  and adjusting  $L_1$  and  $L_2$  to their design values, will allow  $\frac{C_1}{C_2}$  to realize accurate values that are close to 1.0. The alignment insensitive interconnection between the metal plates of the capacitors must be included in the total area calculation for each capacitor. The number of inside and outside corners in the metal pattern for each capacitor must match as closely as possible to the ratio being realized.

#### 4.2 An Internally Compensated High Gain NMOS Operational Amplifier

The requirements imposed on the amplifier for the MOS implementation of the switched capacitor biquadratic section described in Chapter two are a little different from those for a general purpose operational amplifier. For example the amplifier drives capacitive loads rather than resistive ones, and does not require large common mode input range and common mode rejection. In addition, extremely low input offset voltage and offset voltage drift are not of primary importance as the analysis in Chapter 3 has shown.

Figure 4.5.b: Block diagram description of the amplifier circuit in (a).

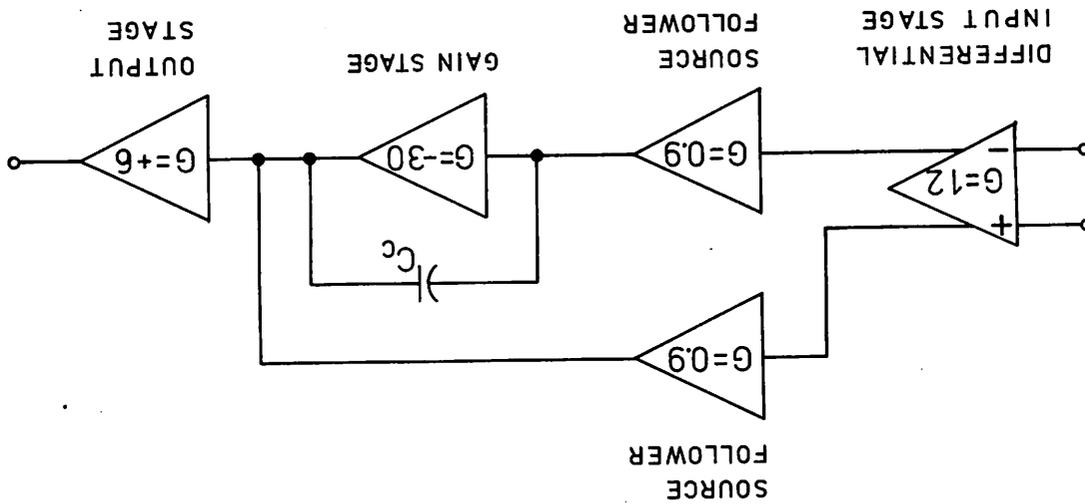
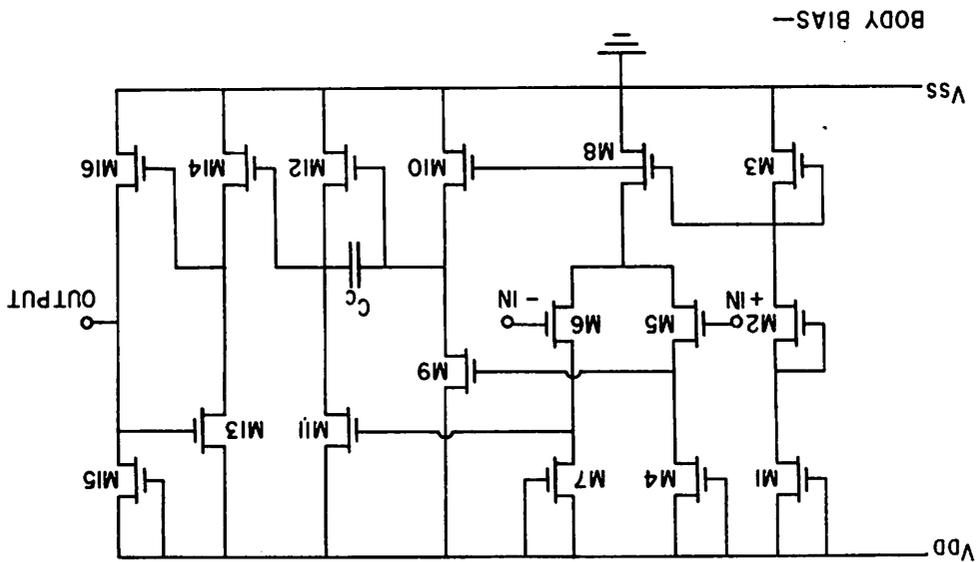


Figure 4.5.a: NMOS Operational Amplifier (with only enhancement transistors).  $C_c = 11$  pF.



amplifier with the device geometries given in Table IV. A block diagram of this amplifier circuit, shown in Figure 4.5(b), illustrates the signal paths. The input stage is a source-coupled pair differential amplifier with one single-ended output (as in a para-phase amplifier). This drives a second gain stage through a source follower level shift. The second gain stage consists of a driver and enhancement load, whose gate is biased by the voltage present on the second output of the differential input stage, rather than the  $V_{DD}$  supply. This connection provides a feedforward path with small phase shift at high frequencies. The second gain stage has a feedback capacitor to realize a dominant pole through Miller compensation. This simple two transistor gain stage drives a shunt-shunt feedback output stage. The bias point interdependence of the stages is such that since all devices in the circuit track one another, the biasing maintains all stages, except the output stage, in their high gain active region independent of  $V_T$  and mobility.

Appendix II describes the DC and small signal model for the MOS transistor. This is used to analyse the amplifier in this section.

#### 4.2.1 Process Description [see Appendix I also]

The amplifier was fabricated as part of a fully monolithic switched-capacitor recursive filter using n-channel Al-gate MOS technology. No  $p^+$  isolation diffusion was employed, however a low resistivity type substrate ( $1-2 \Omega \text{ cm} / 5 \times 10^{15} \text{ Boron atoms/cm}^3$ ) was used to raise the field threshold to more than + 20.0 volts with a small substrate bias applied. The enhancement device threshold was 0.2 V for zero substrate bias. To simulate higher threshold voltages, more typical of industrial

DEVICE	W( $\mu\text{m}$ )	L( $\mu\text{m}$ )
M1	12.7	76.2
M2	12.7	457.2
M3	254	12.7
M4	12.7	152.4
M5	254	12.7
M6	254	12.7
M7	12.7	152.4
M8	254	12.7
M9	12.7	429.3
M10	254	12.7
M11	12.7	429.3
M12	254	12.7
M13	12.7	50.8
M14	190.5	12.7
M15	16.3	17.8
M16	254	12.7

TABLE IV. Mask device dimensions for the Amplifier circuit in Figure 4.5(a).



where  $\gamma$  = body factor

$\phi_F$  = bulk silicon Fermi potential

$V_{BB}$  = substrate bias relative to ground

$V_{D5}$  = drain voltage of M5 relative to ground

With device sizes shown, the differential input stage has a gain of 10 to the single-ended output. Only one half of the available differential gain has been used since this enabled the advantageous use of feedforward for phase compensation of the overall amplifier.

The common-mode gain of the input stage is controlled by the output resistance of M8. The common-mode gain is given by:

$$A_{V_{cm}} = \frac{1}{2r_{o8} g_{m4}} \tag{4.3}$$

where  $r_{o8}$  is the small signal output resistance of M8 and  $g_{m4}$  is the small signal transconductance of M4. By increasing the channel length of M8 one can reduce the common mode gain. The common mode gain of the input stage is approximately 0.04 with the device sizes as shown in Figure 4.6.

#### 4.2.3 Source Follower Level Shift

The single-ended output from the input stage is applied to the gate of M9, a source follower which DC level shifts the signal down in voltage to drive the gate of the second gain stage's driver device, M12. M10, whose gate is controlled by the same DC voltage as M8, provides the quiescent current to bias the source follower. Figure 4.7 shows the circuit for this source follower and the second gain stage which it drives. The voltage gain of this source follower is

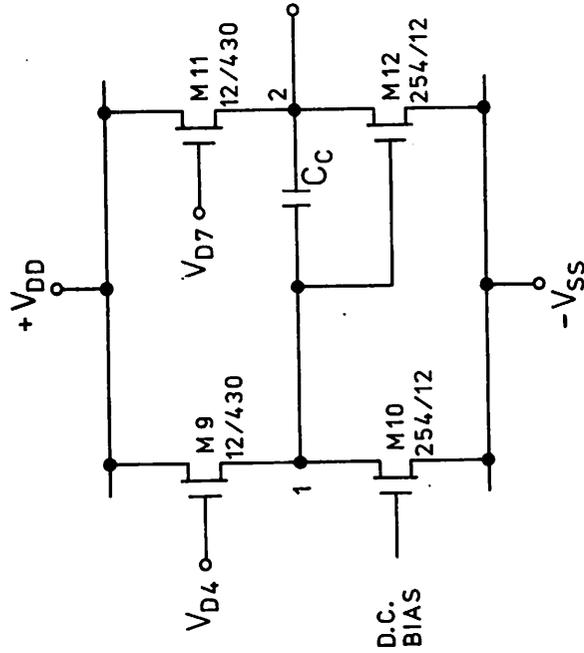


Figure 4.7: Source follower driving the second gain stage.  $C_c = 11$  pF.

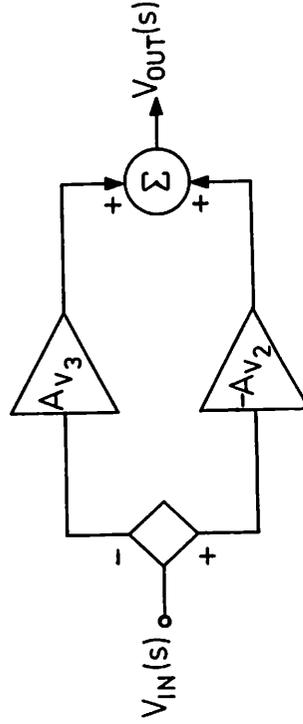


Figure 4.8: Small signal block diagram of the circuit in figure 4.7. Small signal components at  $V_{D4}$  and  $V_{D7}$  are out of phase with each other.

the differential input stage). The low frequency gain for this stage is given by;

$$A_{V2} = \frac{g_{m12}}{g_{m11}} \cdot \frac{1}{1 + \frac{Y}{2 \sqrt{V_{D12} + V_{BB} + 2\phi_F}}} \quad 4.6$$

The value of this gain is 25.

The output of this stage forms the summing node for the "feedforward" path that provides some phase compensation in this three stage amplifier. Figure 4.8 illustrates the principle of the feedforward compensation.  $A_{V2}$  is the high gain, low frequency amplifier stage with two poles and one zero, the latter arising from the source follower.  $A_{V3}$  is the low gain (a simple source follower in fact) high frequency stage with one pole and one zero that are close to each other. This feedforward stage provides a low phase shift path at high frequencies. This path maintains the frequency stability of the amplifier.

$$A_{V2}(s) = \frac{A_{V2}(0) (1 - \frac{s}{z_1}) (1 + \frac{s}{z_2})}{(1 + \frac{s}{p_1}) (1 + \frac{s}{p_2})} \quad 4.7$$

$$A_{V3}(s) = \frac{A_{V3}(0) (1 + \frac{s}{z_3})}{(1 + \frac{s}{p_3})} \quad 4.8$$

$A_{V2}(s)$  describes the signal path from  $V_{D4}$  to the output of the circuit in Figure 4.7, while  $A_{V3}(s)$  describes the signal path from  $V_{D7}$  to the output. The compensation capacitor  $C_C$ , in addition to

described by;

$$A_V(s) = \frac{g_{m9} + sC_1}{\alpha_9 + \frac{1}{r_{o9}} + \frac{1}{r_{o10}} + s(C_1 + C_2)} \quad 4.4a$$

$$\text{where } \alpha_9 = \frac{1}{1 + \frac{Y}{2 \sqrt{V_{D10} + V_{BB} + 2\phi_F}}}$$

$C_1$  is total capacitance between input and output (mostly  $C_{gs9}$ ).

$C_2$  is the total capacitance between the source follower output and ground.

At low frequencies and since  $r_{o9}$  for the devices is large compared

to  $\frac{1}{\alpha_9}$ , Equation 4.4a becomes:

$$A_{V0} = \alpha_9 \quad 4.4b$$

The value of this gain is 0.89. The output impedance is given by:

$$R_{OUT} = \frac{1}{g_{m9}} \parallel r_{o9} \parallel r_{o10} \quad 4.5$$

This impedance when multiplied with the sum of the input capacitance to M10, the total junction capacitance connected to this node and the Miller multiplied feedback capacitance  $C_C$ , forms the dominant pole in the amplifier.

4.2.4 Second Gain Stage

The second gain stage is a simple inverter in which the load device has its gate biased by the voltage at  $V_{D7}$  (the second output of

4.2.5 Output Stage

The output stage is shown in Figure 4.9. The use of shunt-shunt negative feedback allows this circuit to realize a moderate amount of gain while being broad-band in nature [28,29]. Also the output impedance,  $\frac{1}{g_{m15}}$ , of the M15/N16 inverter, is reduced by the loop-gain  $\frac{g_{m16}}{g_{m15}}$ . This allows a lower output impedance with less quiescent current in M15 and M16, than when feedback is not employed. The gain of this output stage, assuming negligible body effect, is given by:

$$A_{V4} = \frac{g_{m14}}{g_{m13}} \left[ \frac{g_{m16}}{g_{m15}} \frac{1}{1 + \frac{g_{m16}}{g_{m15}}} \right] = \sqrt{\frac{(M/L)_{14}}{(M/L)_{13}}} \times \left\{ 1 + \sqrt{\frac{(M/L)_{16}}{(M/L)_{15}}} \right\} \quad 4.10$$

The device geometries were chosen such that: (i) the input capacities to this stage did not load the output of the second gain stage, (ii) the amplifier had a fast transient response with 10 pF connected directly to the output (0V to  $\pm 4.0V$  step in under 3.5 usec), and (iii) maximum output voltage swing was achieved. A gain of 7.0 was realized in this stage. The overall amplifier gain, from simulation, was 1800.

4.2.6  $V_T$  Insensitive Biasing

The complete amplifier, shown in Figure 4.5(a), derives its DC

introducing a dominant pole, also introduces a right half plane zero corresponding to  $\omega_{z1} = \frac{g_{m12}}{C}$  [31]. This right half plane zero occurs at a low frequency because of the low transconductance from the MOS device. This is highly undesirable since it degrades the phase of the complete amplifier by  $90^\circ$  at high frequencies while at the same time stops the 20dB/decade roll off created by the dominant pole in the magnitude response.

The overall transfer function for the scheme in Figure 4.8 is:

$$\frac{V_{OUT}}{V_{IN}} = A_{V_{TOT}}(s) = A_{V_2}(s) + A_{V_3}(s) \quad 4.9a$$

With the substitution of Equations 4.7 and 4.8 and refactorization, this equation takes the form:

$$A_{V_{TOT}}(s) = (A_{V_2}(0) + A_{V_3}(0)) \frac{(1 + \frac{s}{z_1})(1 + \frac{s}{z_2})(1 + \frac{s}{z_3})}{(1 + \frac{s}{p_1})(1 + \frac{s}{p_2})(1 + \frac{s}{p_3})} \quad 4.9b$$

The feedforward path has introduced new zero locations, which can be used to compensate the whole amplifier.  $\omega_{p1}$  is the dominant pole produced by the Miller compensation capacitance  $C_C$ . The final location of the zeros is determined mainly by  $\omega_{p1}$  and the original zeros  $\omega_{z2}$  and  $\omega_{z3}$ , the latter being controlled by  $C_{gs9}$  and  $C_{gs11}$ . The design must ensure that any zeros below the unity gain cross-over frequency are placed as close as possible to their matching pole. This is necessary to avoid any "doublet" contributing a large slow settling component to the transient response [32].

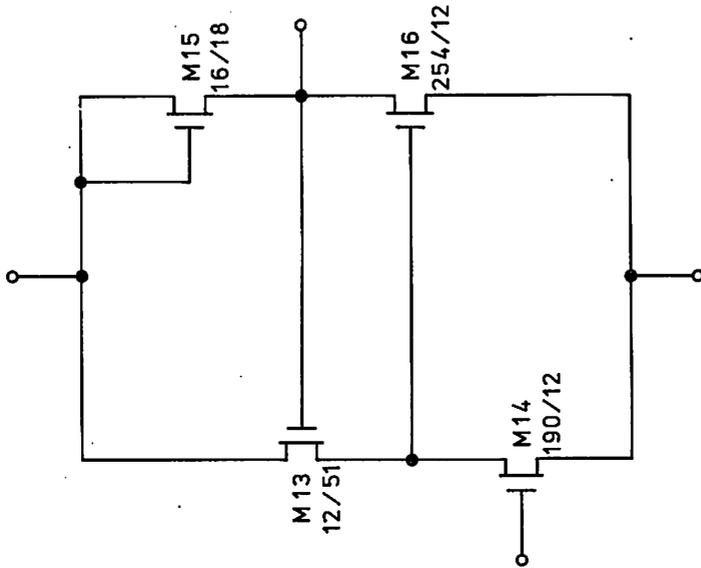


Figure 4.9: Output Stage.

biasing from the three transistor string M1, M2, and M3, each of which is always in saturation because their gate and drain are connected. The quiescent voltages in the circuit are designed to track and maintain all devices, up to M14, in the saturation region independent of the value of  $V_T$ . This is based on the fact that the  $V_T$  and mobility of the devices in the circuit will track, even though the absolute value might vary across the wafer.

The quiescent voltage tracking will now be explained.  $(\frac{W}{L})_n$  denotes the "n" transistor's geometric ratio after lateral diffusion has been taken into account. The input stage is symmetrical, such that for zero differential input,  $V_{GS4} = V_{GS7}$ , independent of  $V_T$ . Geometries  $(\frac{W}{L})_{10}$ ,  $(\frac{W}{L})_8$  and  $(\frac{W}{L})_3$  are all the same so that  $I_{10} = I_8 = I_3 = I_1$ . Therefore a current of  $\frac{I_1}{2}$  flows through M4 and M7. Since  $(\frac{W}{L})_4 = (\frac{W}{L})_7 = \frac{1}{2}(\frac{W}{L})_1$ , therefore  $V_{GS1} = V_{GS4} = V_{GS7}$ . This means that  $V_{GS2} + V_{GS3} = V_{GS9} + \dots$ .  $V_{DS10} = V_{GS11} + V_{DS12}$ . The choice of  $(\frac{W}{L})_2/(\frac{W}{L})_3 = (\frac{W}{L})_9/(\frac{W}{L})_{10}$  results in  $V_{GS2} = V_{GS9}$  and therefore  $V_{DG10} = 0$  with  $V_{DS10} = V_{GS10} = V_{GS3}$  independent of  $V_T$ . Now since  $V_{DS10} = V_{GS3}$ , and if  $(\frac{W}{L})_2/(\frac{W}{L})_3 = (\frac{W}{L})_{11}/(\frac{W}{L})_{12}$  then  $V_{GS2} = V_{GS11}$  and  $V_{DG12} = 0$ . Thus  $V_{DS12} = V_{GS12} = V_{DS10} = V_{GS3}$  independent of  $V_T$ . As long as  $V_T > 0$ , M10 and M12 will remain in the saturation region where their transconductance is high and  $I_{10} = I_{12}$ .

The geometries were chosen such that the quiescent current in M3, M8, M10 and M12 is 20  $\mu A$  when  $V_{DD} = +10 V$ ,  $V_{SS} = -10 V$  and  $V_{BB} = -15 V$ . This choice consumed minimum power while also providing good frequency response from the input stage and high slew rate when charging the compensation capacitor. The total power for the amplifier was 15 mW for

$$V_{DD} - V_{SS} = 20 \text{ V}, V_{BB} - V_{SS} = -5 \text{ V}.$$

#### 4.2.7 Simulated Performance

Computer simulation was done using the circuit analysis program SPICE2. The device model parameters were determined from experimental characteristics of devices that were fabricated with the process conditions described in Section 4.2.1. The derivation of these model parameters is described in Appendix III.

Table V gives the DC operating point voltages and currents predicted by simulation for zero differential input voltage and  $V_{DD} = 10 \text{ V}$ ,  $V_{SS} = -10 \text{ V}$ ,  $V_{BB} = -15 \text{ V}$ . The DC transfer characteristic of the amplifier is given in Figure 4.10, and the frequency response in Figures 4.11(a) and (b). The transient response of the amplifier was tested for unity gain with a 10 pF load connected directly to the output. The simulated responses for input voltage steps from 0 to  $\pm 4.0 \text{ V}$  are given in Figures 4.12(a) and (b). The worst case settling time to 0.1% was 3.5  $\mu\text{sec}$ .

Experimental results for this amplifier design are presented in Section 5.2. The total silicon area for the amplifier was  $0.29 \text{ mm}^2$  ( $450 \text{ mils}^2$ ) when realized with Al-gate NMOS technology with 12  $\mu\text{m}$  minimum dimension. When laid out for a double polysilicon NMOS process [26] using 6  $\mu\text{m}$  minimum dimension this area reduced to  $0.16 \text{ mm}^2$  ( $250 \text{ mils}^2$ ).

#### 4.2.8 Additional Improvements To The Amplifier

In a second version of this all-enhancement NMOS amplifier some additional features were added to improve the circuit performance.

An increase in the second stage gain without increasing the

DEVICE	$V_{GS}$ (v)	$V_{DS}$ (v)	$V_{BS}$ (v)	$I_D$ ( $\mu\text{A}$ )
M1	7.00	7.0	-18.00	18
M2	11.52	11.52	-6.48	18
M3	1.48	1.48	-5.00	18
M4	7.51	7.51	-17.45	10.5
M5	2.09	4.58	-12.91	10.5
M6	2.08	4.85	-12.91	9.5
M7	7.24	7.24	-17.76	9.5
M8	1.48	7.91	-5.00	20
M9	11.01	18.53	-6.47	18
M10	1.48	1.47	-5.00	18
M11	10.91	18.15	-5.00	14.5
M12	1.474	1.854	-5.00	14.5
M13	7.48	17.48	-7.52	124
M14	1.85	2.52	-5.00	124
M15	10.00	10.00	-15.00	850
M16	2.52	10	-5.00	850

TABLE V. D.C. Operating Point Conditions for the Transistors in the NMOS Amplifier Simulation (Version 1).  $V_{DD} = 10\text{V}$ ,  $V_{SS} = -10\text{V}$ ,  $V_{BB} = -15\text{V}$ .

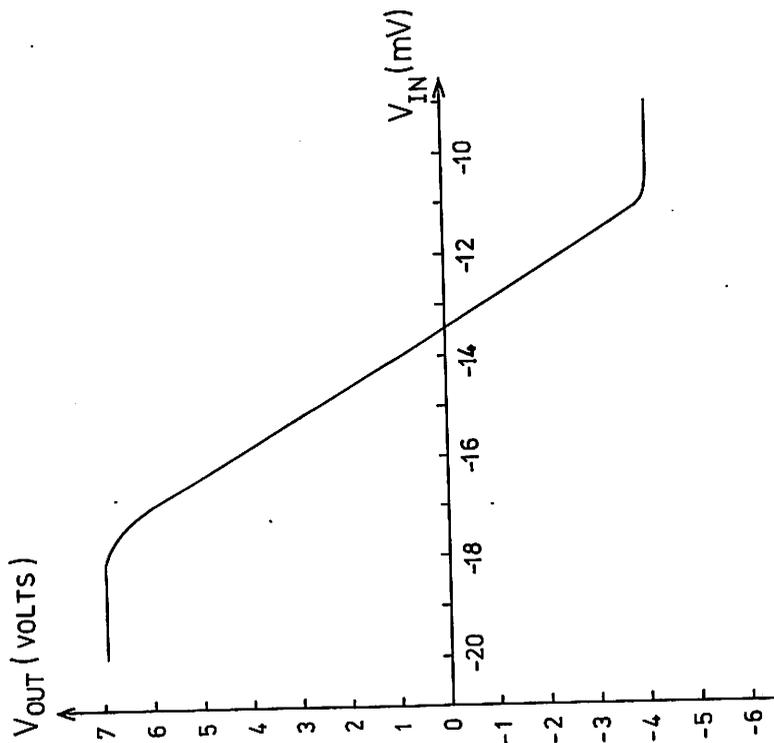
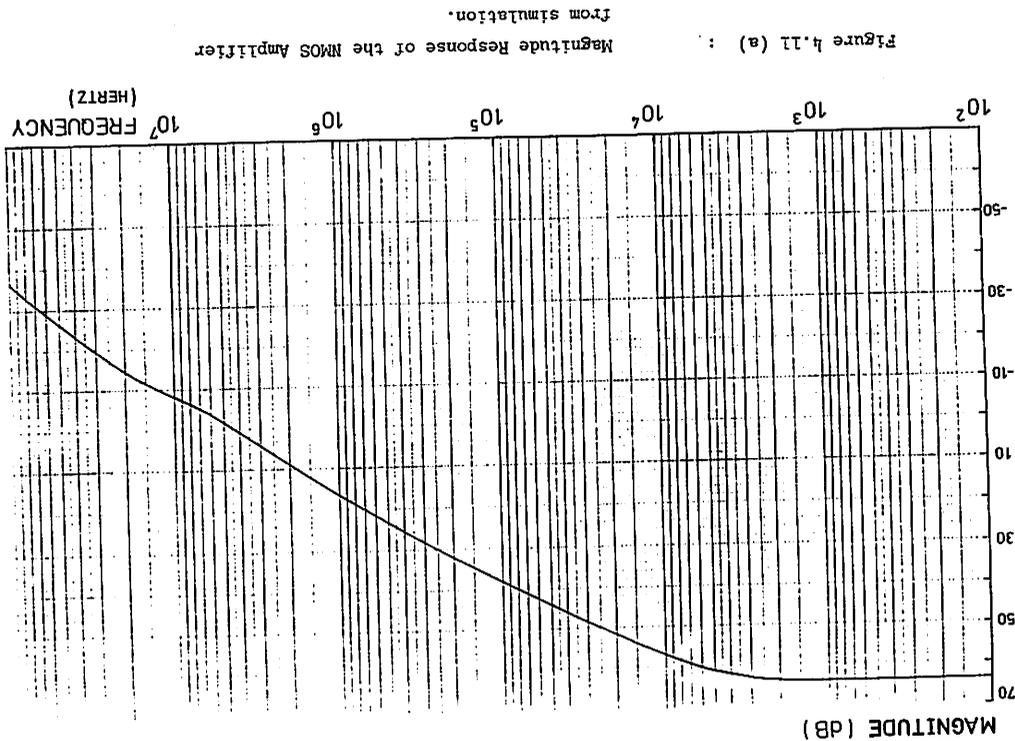


Figure 4.10: Simulated DC transfer characteristic of the NMOS amplifier. ( $V_{DD} = 20\text{ V}$ ,  $V_{BB} = -5\text{ V}$ ).

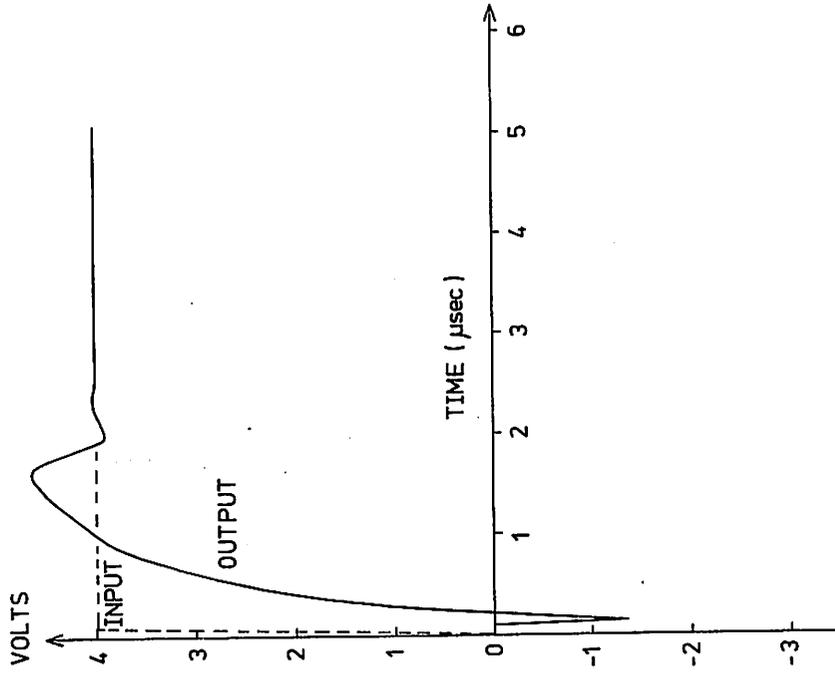


Figure 4.12.a: Simulated Transient Response for the Amplifier in Unity Gain with a 10 pF load (+4 V input step).

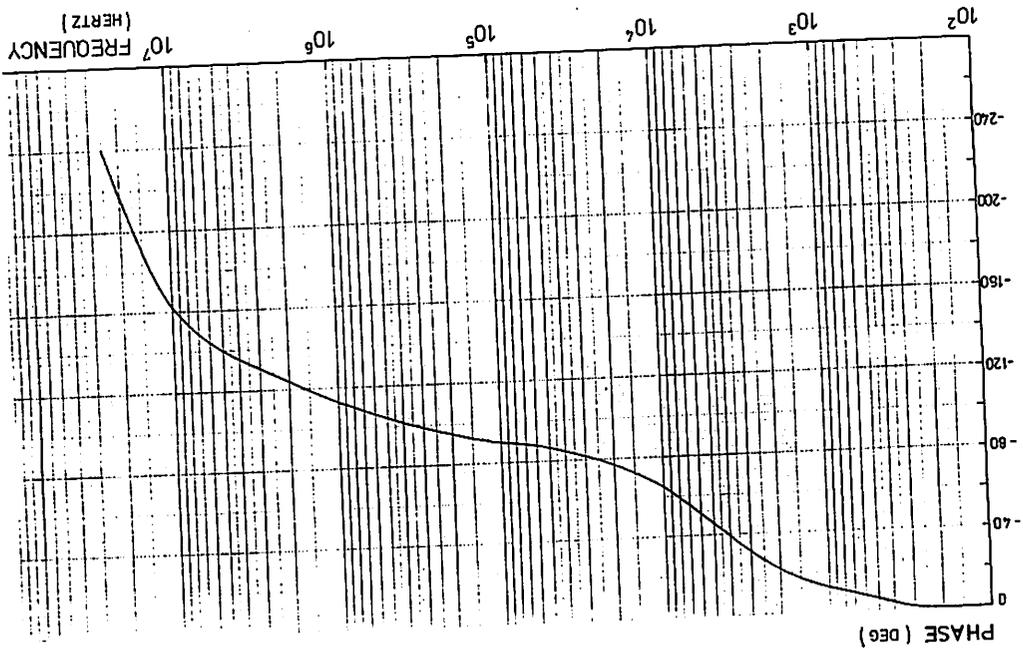


Figure 4.11 (b) : Phase Response of the NMOS Amplifier from simulation.

inverter area was obtained by using the split-load inverter [31]. The complete second version of the amplifier is shown in Figure 4.13a, with the device geometries given in Table VI.

Bypass capacitance has been introduced into the two source follower signal paths in order to lower the dominant zero frequency and move it closer to the second dominant pole. This enables the unity gain bandwidth to be increased from 1.5 MHz up to 3 MHz with two bypass capacitors of 3.8 pF and  $C_C = 14$  pF. The phase margin was increased from  $45^\circ$  to  $55^\circ$ . When  $C_C = 7$  pF the slew rate is higher, however the time over which damped oscillation occurs is longer. The overall settling time with either value of  $C_C$  was about 3.0  $\mu$ sec for 0 to  $\pm 4.0$  V steps. The slew rate was 5 V per  $\mu$ sec. Figure 4.14 shows the simulated frequency response for  $C_{B_1} = 3.8$  pF,  $C_{B_2} = 3.8$  pF and  $C_C = 14$  pF, while Figure 4.15 gives the 0 to  $\pm 4$  V step response of the amplifier in unity gain with 10 pF connected directly at the output.

Finally common mode feedback was added to the input stage as shown in Figure 4.13. M1' and M1 sense the common mode voltage at nodes  $V_{D4}$  and  $V_{D7}$  of the input stage, and control the current into the M3, M8 current mirror. Thus if the common mode output voltage for the input stage increases, then the current through M3 increases and is mirrored into the current source M8. This increased current in M8 causes the common mode output voltage to remain unchanged from the original value. Thus more control has been placed on the DC operating points of  $V_{D4}$  and  $V_{D7}$  in the input stage. From simulation the common mode rejection ratio for the overall amplifier was found to be 90 dB.

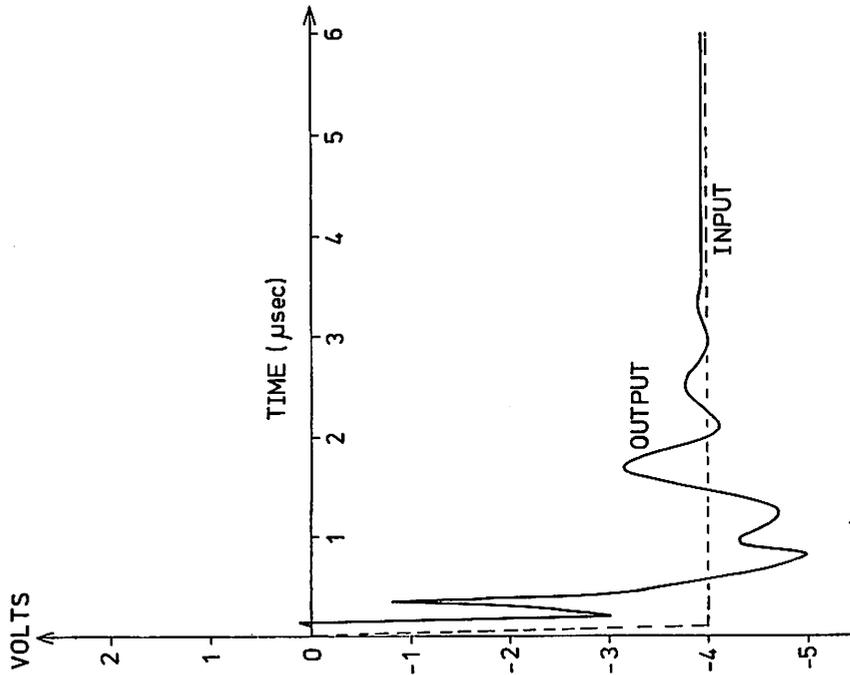


Figure 4.12.b: Simulated Transient Response for the Amplifier in Unity Gain with a 10 pF load. (-4 V input step).

DEVICE	W(μm)	L(μm)
M1	12.7	396.2
M1'	12.7	396.2
M2	12.7	203.2
M3	254	12.7
M4	12.7	152.4
M5	254	12.7
M6	254	12.7
M7	12.7	152.4
M8	254	12.7
M9	12.7	203.2
M9'	12.7	203.2
M10	254	12.7
M11	12.7	203.2
M11'	12.7	203.2
M12	254	12.7
M13	12.7	50.8
M14	190.5	12.7
M15	12.7	38.1
M16	254	12.7

TABLE VI. Mask device dimensions for the Amplifier circuit in Figure 4.13

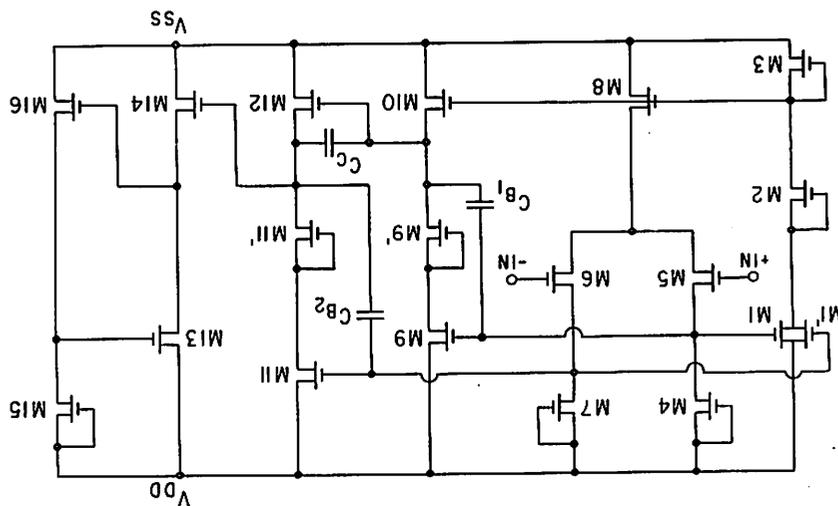


Figure 4.13.a: ENHANCEMENT NMOS OPERATIONAL AMPLIFIER  
 $C_{B1} = C_{B2} = 3.8 \text{ pF}$ ,  $C_C = 7 \text{ pF} + 14 \text{ pF}$ .

Figure 4.14 (a) : Magnitude Response of the CMOS Amplifier (Version 2) from simulation.

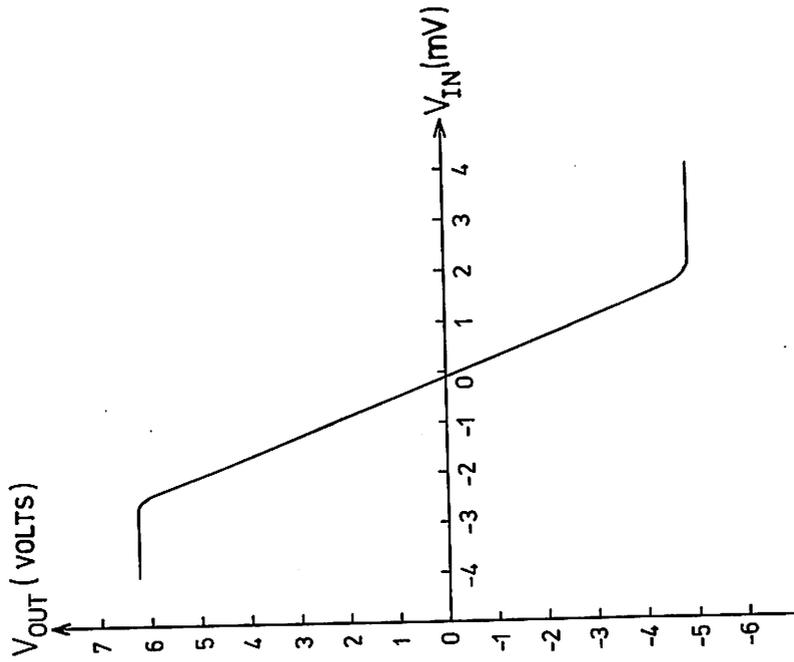
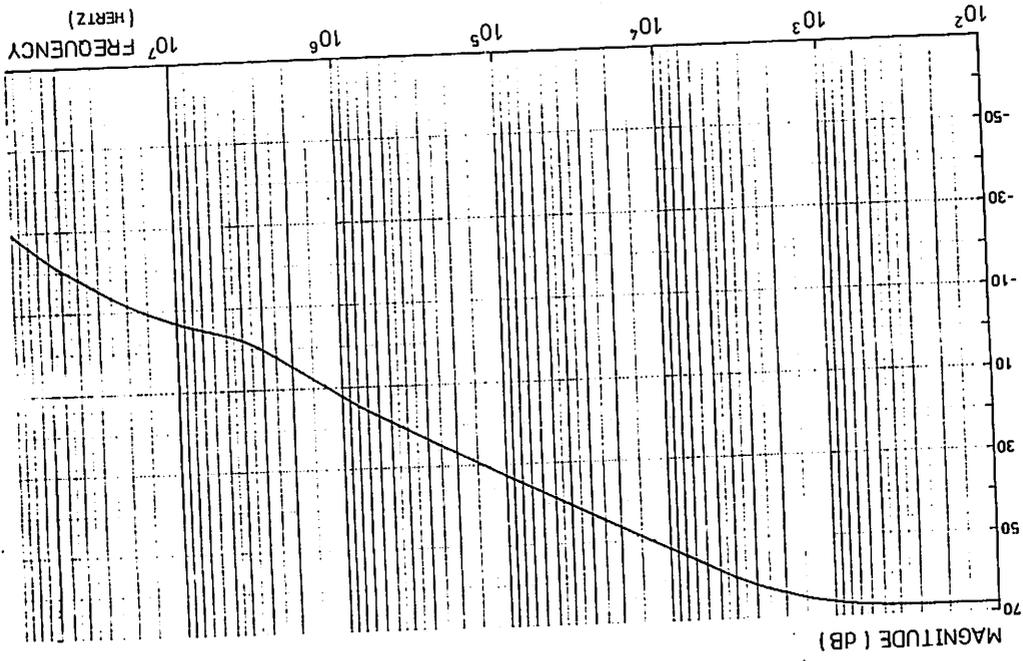


Figure 4.13.b: Simulated DC transfer characteristic of the CMOS amplifier, Version 2. ( $V_{DD} - V_{SS} = 20\text{ V}$ ,  $V_{BB} - V_{SS} = -5\text{ V}$ ).

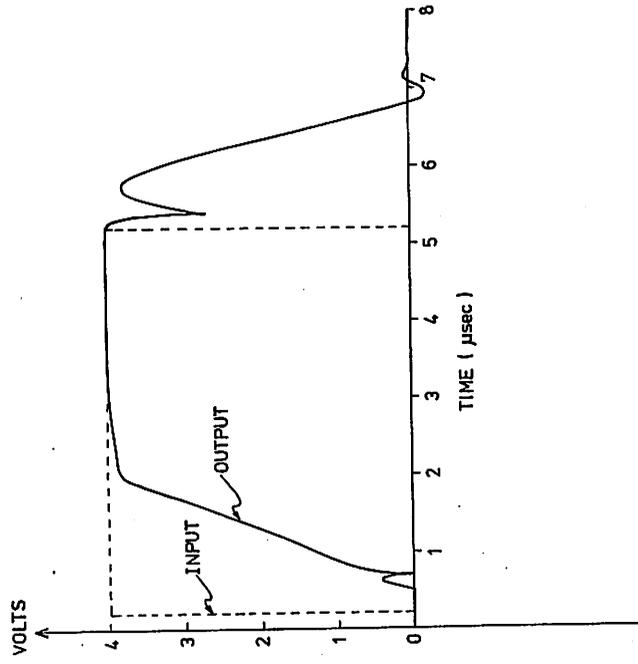


Figure 4.15.a: Simulated Transient Response for the Amplifier (Version 2) in Unity Gain with a 10 pF load. (+4 V input step).

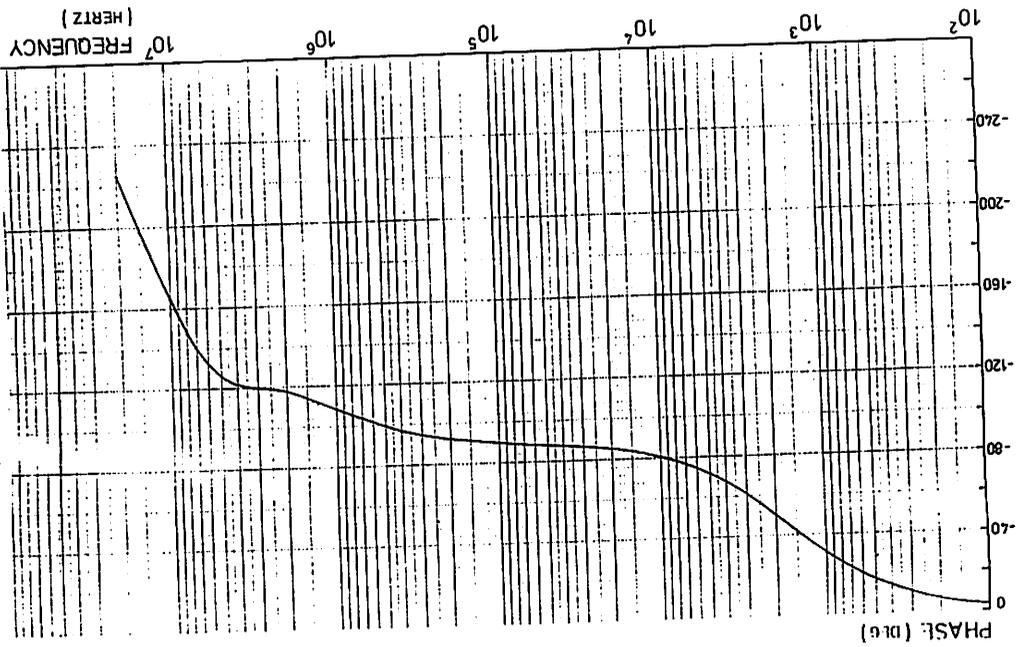


Figure 4.14 (b) : Phase Response of the MOS Amplifier (Version 2) from simulation.

4.3 Clock Feedthrough Cancellation

The effect of clock feedthrough on the switched-capacitor multiply and delay was considered in Section 2.2.2 C. The feedthrough produces a DC voltage at the amplifier output (see Figure 4.16) that is approximately given by Equation 2.12 and shown here:

$$V_{OUT,DC} = \frac{C_{GS}}{C_2} \times |V_{clock}| \tag{4.11}$$

This effect occurs when the feedback switch (M3) is turned off.  $C_{GS}$  is the nonlinear gate to source capacitance of the feedback switch, with the characteristic shown in Figure 4.17. Since the maximum positive excursion of the clock voltage is much larger than the  $V_T$  of the feedback switch,  $\frac{C_{OX}}{2}$  is a good approximation to the average  $C_{GS}$  capacitance during device turn off. The maximum positive excursion of the clock voltage is usually the same as the analog positive supply,  $+V_{DD}$ . Thus a good approximation to the DC voltage at the output caused by clock feedthrough is given by:

$$V_{OUT,DC} = \frac{C_{OX}}{2} \cdot \frac{V_{DD}}{C_2} \tag{4.12}$$

When the magnitude of this DC voltage is unacceptable, a "charge-cancelling" MOSFET can be added to the circuit, as shown in Figure 4.18. This device produces a first order cancellation of the feedthrough effect with a drastic reduction in this DC voltage, as shown by the experimental results in Section 5.3.

The charge-cancelling transistor is a dummy MOS device with its

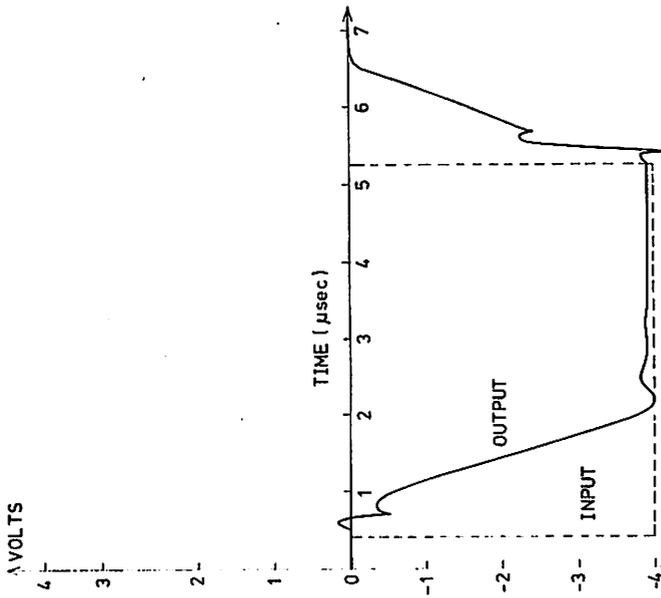


Figure 4.15.b: Simulated Transient Response for the Amplifier (Version 2) in Unity Gain with a 10 pF load. (-4 V input step).

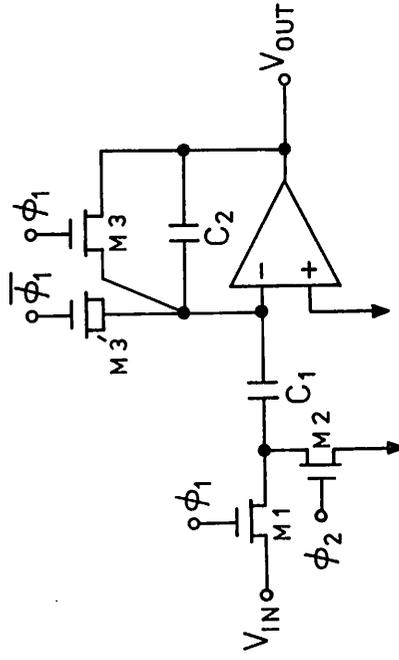


Figure 4.18: Switched-capacitor multiply and delay with charge-cancelling device.

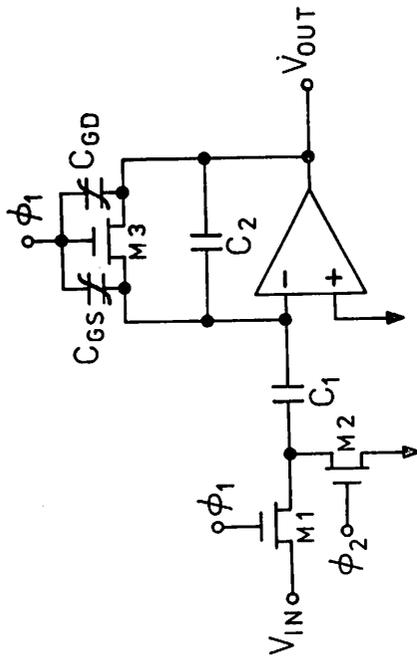


Figure 4.16: Sources of Clock Feedthrough.

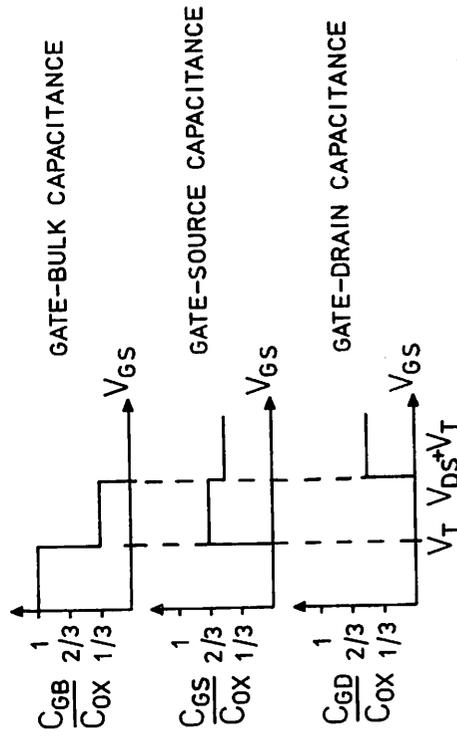


Figure 4.17: Piecewise Linear Model of the MOSFET Capacitances.

source and drain short-circuited to prevent DC current flow and with one half the channel area of the feedback transistor M3. The voltage applied at the gate of the charge-cancelling device is the complement of  $\phi_1$  the feedback transistor's gate voltage.

When metal gate NMOS technology is used careful attention must be given to the layout of the feedback transistor with the charge-cancelling device, in order that the circuit remain insensitive to misalignment. The geometry shown in Figure 4.19 tends to compensate for masking misalignments by keeping the source and drain overlap capacitances equal. M3' occupies the minimum device area ( $\frac{W}{L} = 1$ ), therefore M3 has a  $\frac{W}{L}$  ratio of 2.0.

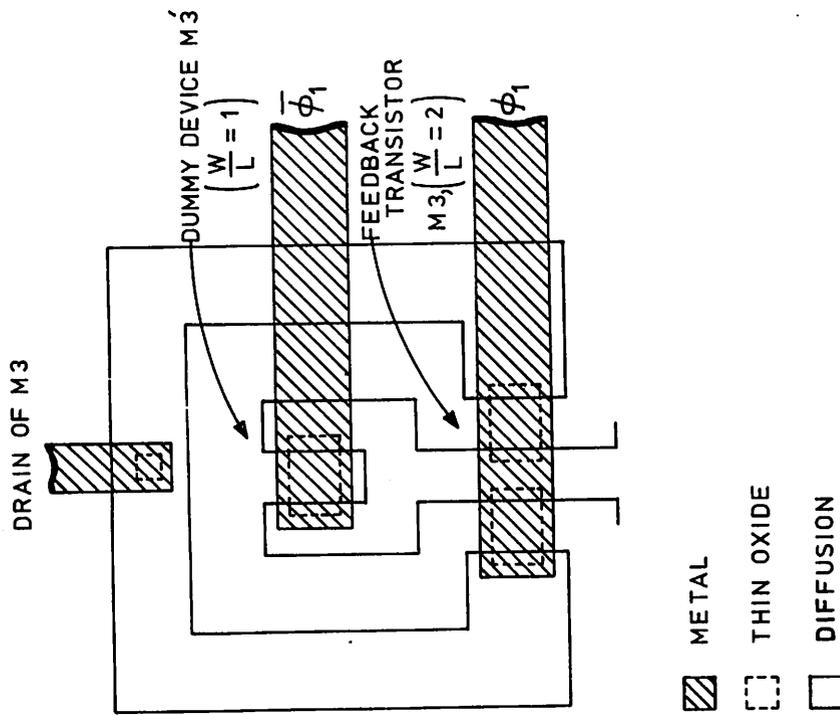


Figure 4.19: Layout geometry for the feedback switch with its charge-cancelling device.

CHAPTER 5  
PROTOTYPE FILTER TEST CHIP RESULTS

Introduction

The test chip contained a completely monolithic biquadratic filter (two poles and two zeros), which could be programmed, under the control of some MOS switches, to achieve a high Q ( $Q = 18$ ) lowpass, bandpass, or highpass filter response. The complete schematic of this filter is given in Figure 2.13. It implements the biquadratic transfer function described by Equation 2.19. The coefficients and the value for the feedback capacitors 'C' used around each amplifier are given in Table VII.

Figure 5.1 is a microphotograph of a first version test chip in Al-gate NMOS technology. Appendix I outlines the fabrication schedule used in making this circuit. Appendix III presents the MOS transistor characteristics achieved and the parameters used for modelling these devices. This test chip contained all the analog switches and ratioed capacitors required in the high Q second order section, and just one all-enhancement NMOS amplifier whose circuit was described in Figure 4.4. Section 5.1.1 presents the typical measured performance parameters achieved with this amplifier. Section 5.2 gives data from this test chip on the accuracy of the ratioed MOS capacitors.

Figure 5.2 is a microphotograph of the second test chip in Al-gate NMOS technology, which contained all four amplifiers in addition to the analog switches and ratioed capacitors for the biquadratic filter (Figure 2.13). The amplifier used in this implementation was described in Figure 4.13. Its measured parameters are given in Section 5.1.2,

COEFFICIENT	VALUE
$\alpha_0$	+ 0.03608
$\alpha_1$	0.0/- 0.07089
$\alpha_2$	+ 0.03608
$\beta_1$	- 1.68216
$\beta_2$	+ 0.97004
'C' for Amplifier 1 ( $CL_1$ )	4.73 pF
'C' for Amplifier 2 ( $CL_2$ )	8.14 pF
'C' for Amplifier 3 ( $CL_3$ )	7.95 pF

TABLE VII. Filter coefficients and their feedback capacitor value (refer to Figure 2.13).

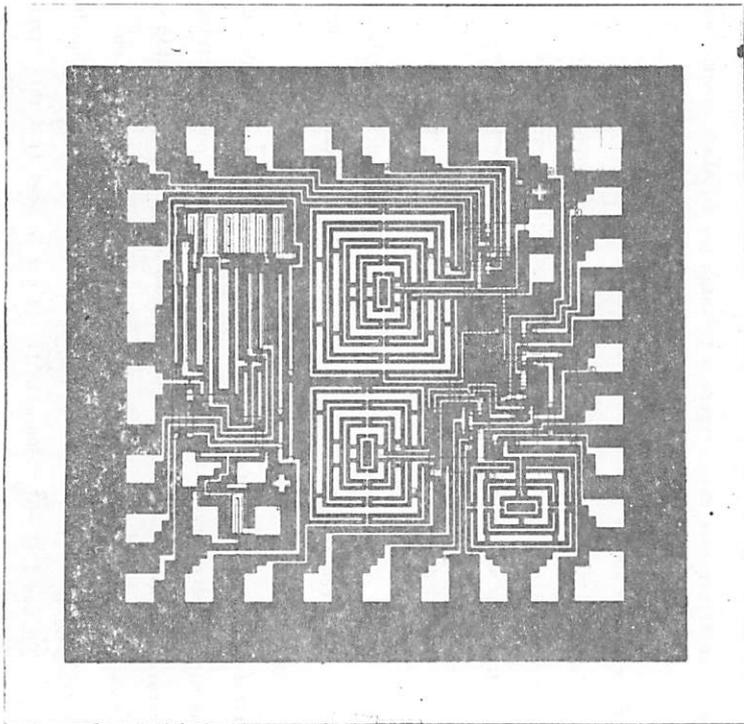


Figure 5.1: Microphotograph of the filter test chip fabricated in Al-gate NMOS technology. The amplifier is in the upper section of this picture, together with some test devices.

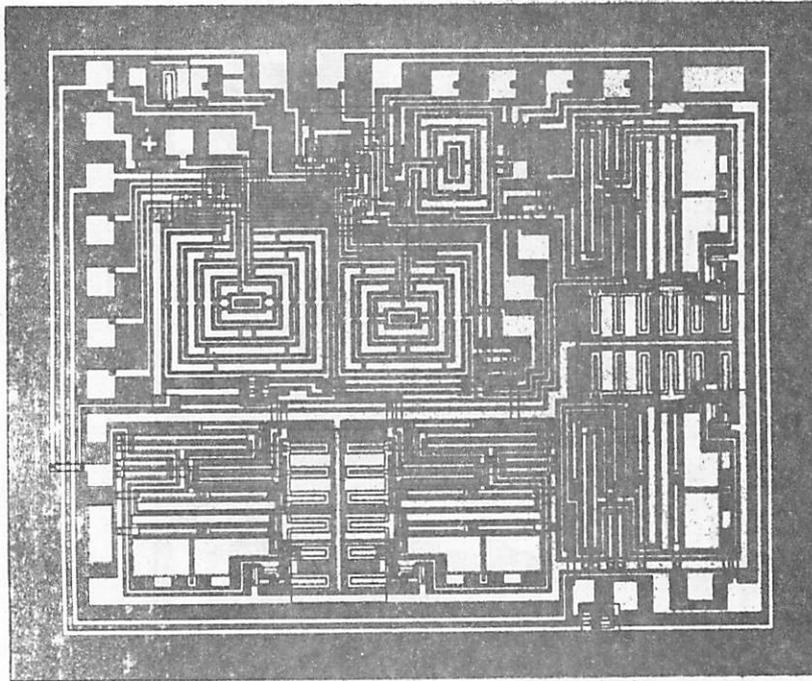


Figure 5.2: Microphotograph of the fully integrated programmable biquadratic filter, fabricated in Al-gate NMOS technology. The four amplifiers in this circuit (figure 2.13) are situated in the bottom and left-hand sections of this picture.

while the performance of the programmable biquadratic filter is presented in Section 5.4. The die area of this self-contained monolithic switched capacitor recursive filter was  $5.16 \text{ mm}^2$  (8000 mils<sup>2</sup>). Area of the amplifier was  $0.50 \text{ mm}^2$  (800 mils<sup>2</sup>). The layout rules required the minimum source to drain spacing on the mask to be  $12 \text{ }\mu\text{m}$ , with the other minimum feature sizes not less than  $10 \text{ }\mu\text{m}$ . The minimum alignment tolerance was the gate oxide to diffusion of  $2.5 \text{ }\mu\text{m}$ , which was used for the gate to source and gate to drain overlap.

Section 5.3 gives the result of the clock feedthrough effect in the first filter test chip (Figure 5.1) which had no clock feedthrough cancellation scheme, and in the second filter test chip (Figure 5.2) which did have such a scheme, as described in Section 4.3.

Figure 5.3 is a microphotograph showing the same biquadratic filter implemented with a double polysilicon gate NMOS technology. This chip in addition to all the analog switches, capacitors and amplifiers, contains the logic for generating the four phase non-overlapping clock which controls this switched-capacitor filter.

The test chips shown in Figure 5.1 and 5.2 were fabricated in the Integrated Circuits fabrication laboratory at the University of California, Berkeley. The double polysilicon gate NMOS implementation of the filter (Figure 5.3) was fabricated at American Microsystems Inc. (AMI). The minimum gate length with this technology was  $6 \text{ }\mu\text{m}$ , and the minimum feature size was  $5 \text{ }\mu\text{m}$ . The area of the NMOS amplifier on this chip was  $0.20 \text{ mm}^2$  (300 mils<sup>2</sup>). This amplifier circuit is similar to the one described in Figure 4.4. The total die area for the complete biquadratic filter was  $1.61 \text{ mm}^2$  (2500 mils<sup>2</sup>). It can be seen from this circuit

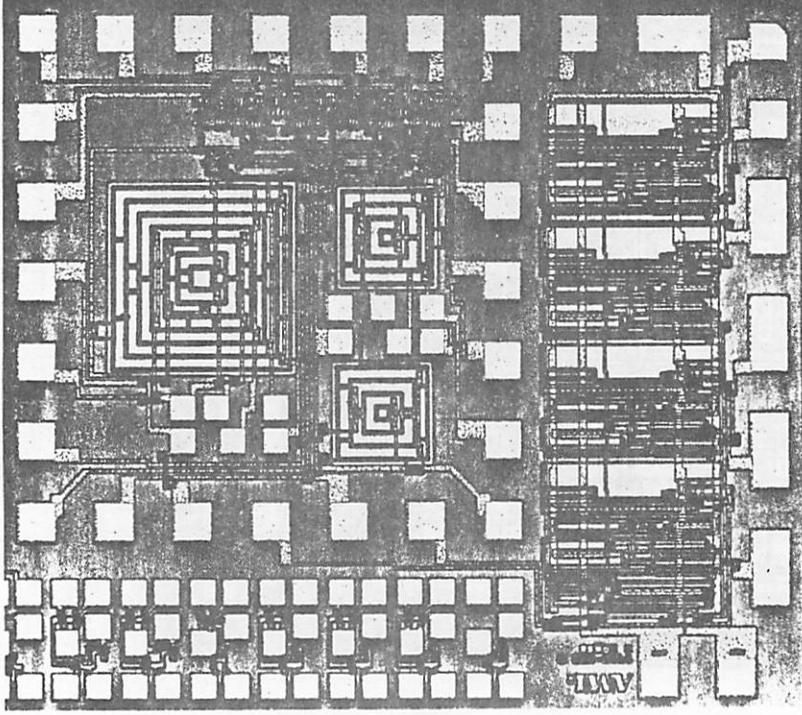


Figure 5.3: Microphotograph of the biquadratic filter implemented with double polysilicon gate NMOS technology.

that industry standard NMOS technology offers a very high level of analog circuit function density on a silicon integrated circuit.

### 5.1 NMOS Amplifiers

#### 5.1.1 Version 1 Amplifier

The all-enhancement NMOS amplifier shown in Figure 4.4 and described in Section 4.2 was fabricated with the Al-gate NMOS technology (see Appendix I and III) on the first test chip (Figure 5.1).

Table VIII contains the measured performance from a sample of ten amplifiers. The D.C. transfer characteristic for this operational amplifier can be seen in Figure 5.4. The power supply voltages were  $V_{DD} = +7.5$  V,  $V_{SS} = -7.5$  V,  $V_{BB} = -7.5$  V. Figure 5.5 shows the step response of the operational amplifier when connected as a unity gain buffer with a 10 pF load directly on the output. These measured results agree quite well with the simulation results in Section 4.2.

When the power supply voltage was varied, the low frequency gain and output voltage swing changed as follows:

Supply	Body Bias	Low Frequency Gain	Output Swing
+7.5 V	0 V	1800	8.0 V
+5.0 V	0 V	1000	4.2 V
+3.5 V	0 V	500	2.5 V
+7.5 V	-5.0 V	2000	6.2 V

#### 5.1.2 Version 2 Amplifier

A version 2 all-enhancement NMOS amplifier, as shown in Figure 4.13

TABLE VIII

### Performance Parameters of the NMOS Amplifier (Version 1)

Power Supplies:  $V_{DD} = +7.5$  V,  $V_{SS} = -7.5$  V  
 Substrate Bias = 0 V ( $V_{BB} = -7.5$  V).

Low Frequency Gain Mean	1800
Low Frequency Gain Standard Deviation	200
Input Offset Voltage Mean	-36 mV
Input Offset Voltage Standard Deviation	40 mV
Common Mode Input Range	+ 3.6 V to - 7.4 V
Common Mode Rejection Ratio	58 dB
Positive Power Supply Rejection	63 dB
Negative Power Supply Rejection	66 dB
Slew Rate	+ 2.0 V/ $\mu$ sec, - 3.0 V/ $\mu$ sec
Step Response Settling Time to 0.1%:	
for a - 2.5 V to + 2.5 V step:	4.0 $\mu$ sec
for a + 2.5 V to - 2.5 V step:	4.5 $\mu$ sec
for a 0 V to $\pm$ 1 V step:	3.5 $\mu$ sec
Output Voltage Swing	+ 3.2 V to - 4.2 V
Power Consumption	15 mW

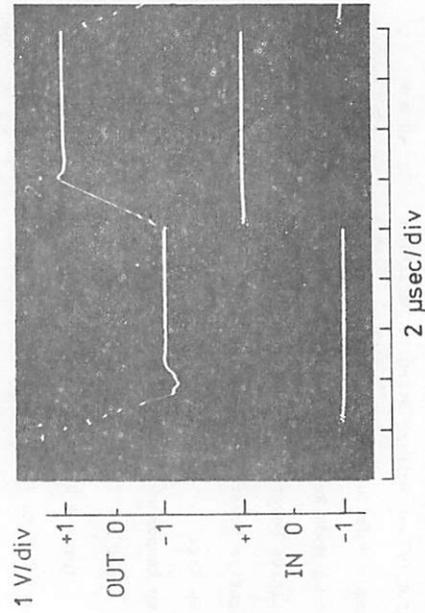
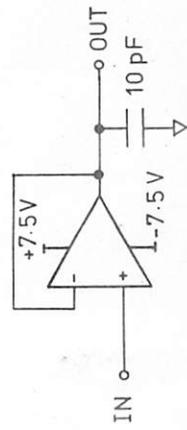


Figure 5.5: Step response of the NMOS Operational Amplifier (Version 1) in unity gain.

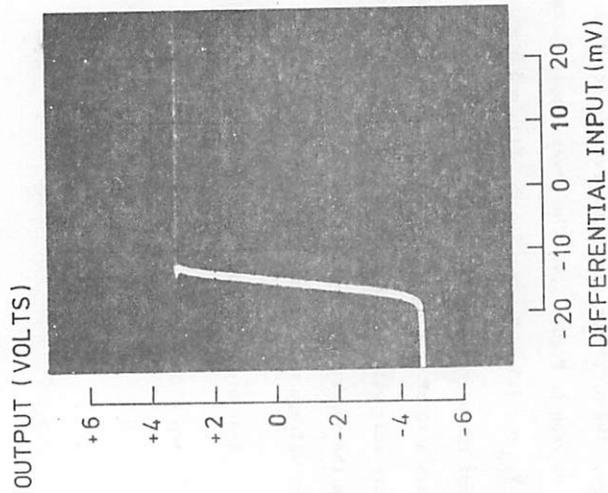


Figure 5.4: Measured DC Transfer Characteristic of the NMOS Operational Amplifier (Version 1).

and described in Section 4.2.8, was fabricated with the Al-gate NMOS technology on the second filter test chip (Figure 5.2). This amplifier had an improved phase margin and higher low frequency gain.

Table IX contains the measured performance from a sample of eight amplifiers on two different wafers. The D.C. transfer characteristic for this operational amplifier can be seen in Figure 5.6. The power supply voltages were  $V_{DD} = +10.0$  V,  $V_{SS} = -10.0$  V,  $V_{BB} = -12.5$  V. Figure 5.7 provides information about the common mode input range and the common mode rejection ratio. This photograph is a trace of the input offset voltage as a function of common mode input voltage. Figure 5.8 shows some step responses of the operational amplifier when connected as a unity gain buffer with a 10 pF load directly on the output. These measured results also agree quite well with the simulation results in Section 4.2.8.

The amplifier was designed to have zero offset based on simulation. The -20 mV offset mean that was measured arose from inaccuracies in the device model used for simulation. This offset can be reduced to zero by trimming device geometries on the mask.

### 5.2 Ratioed Capacitor Accuracy

A histogram of capacitor ratio measurements taken from the first test chip is given in Figure 5.9. These results indicate that the capacitor ratio can be held to within a tolerance of 0.1%, since more than 67% of the measurement sample fell within these limits. These measurements were made at a probe station using a Hewlett Packard Digital LCR meter. The capacitance values involved were  $C_1 = 13.95$  pF,  $C_2 = 8.34$  pF. It is possible that a large component of the observed

TABLE IX  
Performance Parameters of the NMOS Amplifier (Version 2)

Power Supplies: $V_{DD} = +10.0$ V, $V_{SS} = -10.0$ V	
Substrate bias = -2.5 ( $V_{BB} = -12.5$ V)	
Low Frequency Gain Mean	2200
Low Frequency Gain Standard Deviation	200
Input Offset Voltage Mean	-20 mV
Input Offset Voltage Standard Deviation	5 mV
Common Mode Input Range	+ 5.0 V to - 8.5 V
Common Mode Rejection Ratio (at zero common mode input voltage)	72 dB
Positive Power Supply Rejection	80 dB
Negative Power Supply Rejection	74 dB
Slew Rate	+ 5 V/usec, - 2 V/usec
Step Response Settling Time to 0.1%:	
for a 0 V to + 1 V step:	2.0 usec
for a 0 V to - 1 V step:	2.0 usec
for a - 2 V to + 2 V step:	3.5 usec
for a + 2 V to - 2 V step:	3.0 usec
Output Voltage Swing	+ 3.2 V to - 7.4 V
Total Input Referred Noise (0 to 50 kHz bandwidth)	60 to 80 $\mu$ V rms
Power Consumption	15 mW

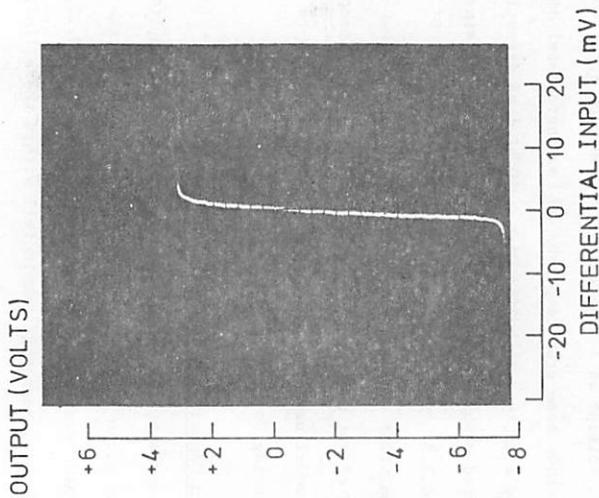


Figure 5.6: Measured DC Transfer Characteristic of the NMOS Operational Amplifier (Version 2).  
Input offset was -18mV but is set to zero in the above curve.  
 $V_{DD} = 20\text{ V}$ ,  $V_{BB} = V_{SS} = -2.5\text{ V}$ .

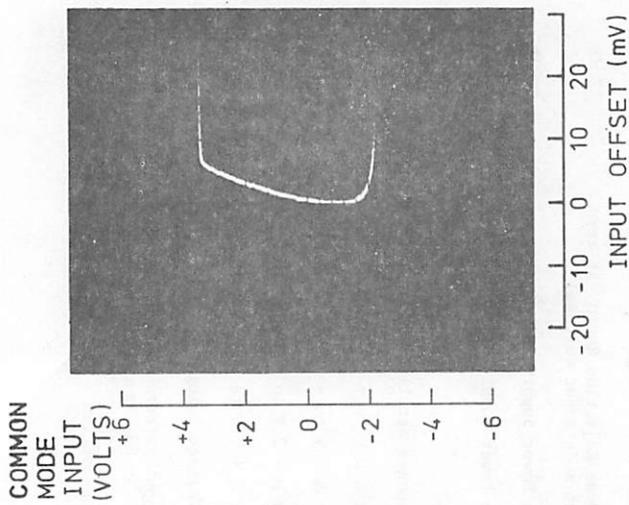


Figure 5.7: Common Mode Input Performance of the NMOS Amplifier (Version 2).

Figure 5.9: Measurement distribution of ratioed MOS capacitors (Al-gate NMOS technology).

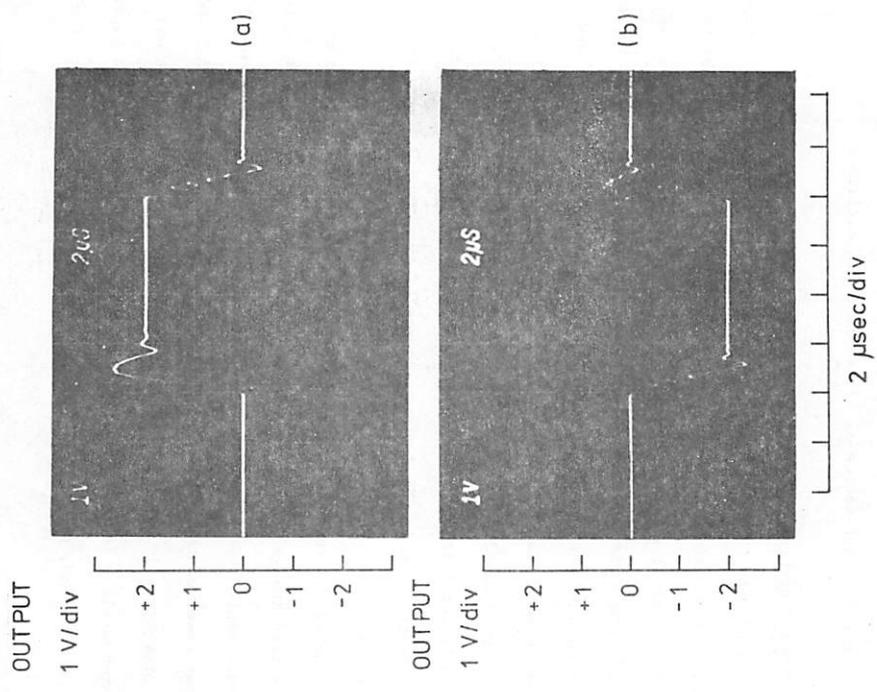
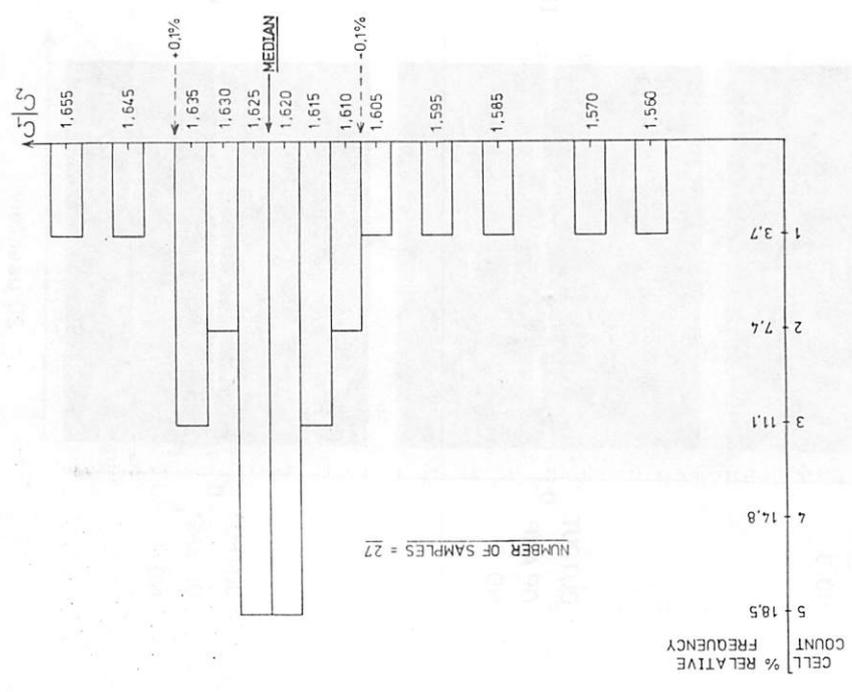


Figure 5.8: Measured Transient Responses of the NMOS Operational Amplifier (Version 2) in the unity gain connection with a 10 pF load.

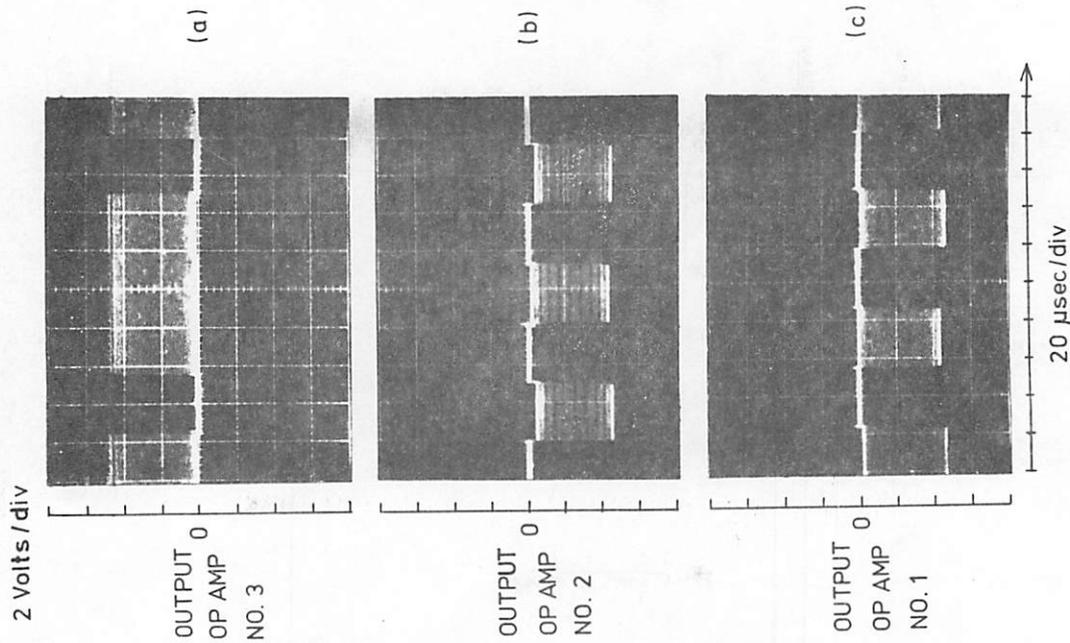


Figure 5.10 (a), (b), and (c): Analog sampled-data waveforms present at each amplifier output (filter circuit in figure 2.13). An asynchronous sinusoidal signal is present.

capacitor ratio variation was due to error in the reproducibility of capacitor measurements with this instrument and the probe station. Thus it seems that the best means of learning what accuracy the ratioed MOS capacitors can achieve, is to measure the frequency response of the monolithic filter and look for variations in the critical frequencies. These results can then be related back to a capacitor ratio error, since this is the dominant source of filter response variation.

### 5.3 Clock Feedthrough Effects

The effects of clock feedthrough were given in Section 4.3. Experimentally it was observed with the first switched-capacitor filter test chip that without clock feedthrough cancellation, a rather large D.C. offset voltage was present in the analog sampled-data signal at the output of each of the three amplifiers. From Figures 5.10(a), (b) and (c) it can be seen that D.C. offsets of + 2.4 V occurred at the output of amplifiers 3 and 2, and - 2.2 V at the output of amplifier 1. Since the amplifiers' input offset voltage is typically less than 50 mV, the clock feedthrough is the dominant source of the large D.C. offsets observed.

The second version switched-capacitor filter test chip had the clock feedthrough cancellation circuit described in Section 4.3 included at each amplifiers' inverting input (the feedthrough sensitive node). It was observed that the D.C. offset at the output of amplifier 3 and 2 was approximately + 150 mV, while at the output of amplifier 1 it was approximately - 140 mV. Since the amplifier on this chip had a typical offset of 20 mV, and there is a multiplication of this offset to the

filter output of about 7 times, it can be concluded that the feed-through cancellation scheme does function as expected in Section 4.3. The feedthrough effect on the output of each amplifier has been reduced to something in the order of 10 mV or less. Measurement of each of each amplifier's input offset voltage would be necessary in order that a more accurate conclusion of feedthrough cancellation performance could be made. This fully monolithic switched-capacitor filter only had one amplifier (the input sample and hold) accessible for such a measurement.

#### 5.4 Programmable Biquadratic Filter

##### 5.4.1 Filter Responses

Three types of frequency response (lowpass, bandpass, and high-pass) were realized with the fully monolithic switched-capacitor recursive filter test chip shown in Figure 5.2. This was done by simply changing the clock voltage signals to the switched capacitors  $\alpha_0C$ ,  $\alpha_1C$  and  $\alpha_2C$ . The design of the filter parameters was given in Section 3.3.2.

The lowpass response is shown in Figures 5.11(a) and (b), the bandpass response in Figures 5.12(a) and (b), and the highpass response in Figures 5.13(a) and (b). The sampling rate for each of these was 8 kHz. To achieve these responses the feedback coefficients were kept the same, while the input coefficients  $\alpha_0$ ,  $\alpha_1$ ,  $\alpha_2$  were altered by changing the clock signals controlling the input switches, according to the system shown in Table X.

\*Using Equation 2.10 and capacitor ratios given in Table VII for the switched-capacitor filter (Figure 2.12).

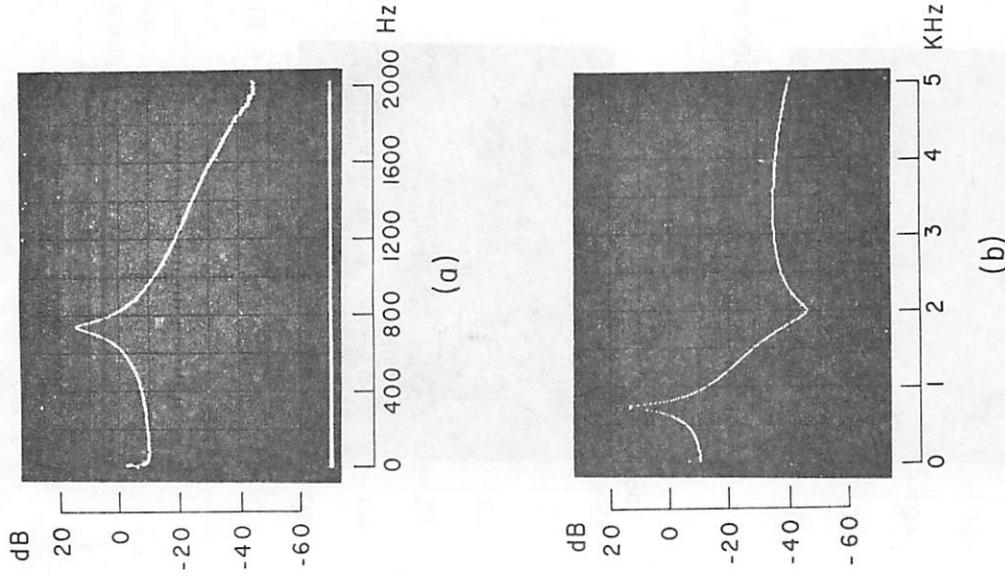
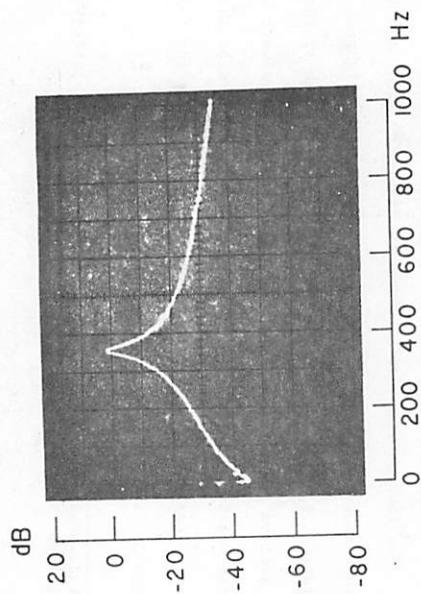
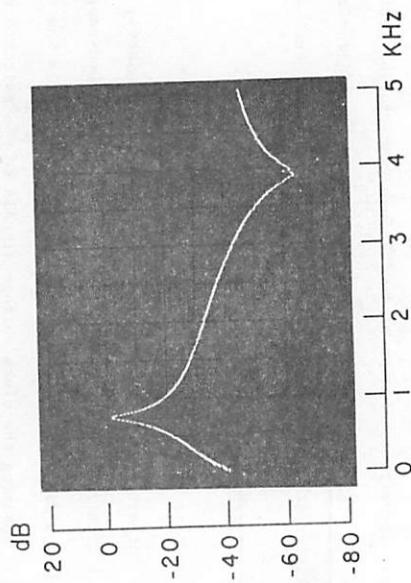


Figure 5.11 (a) and (b): Measured lowpass filter response (the simulation is in figure 3.11)

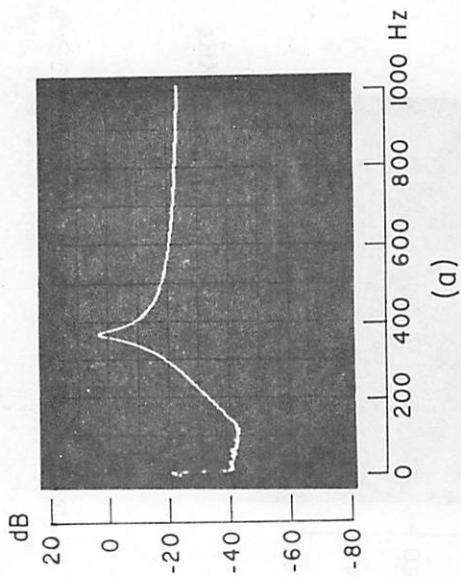


(a)

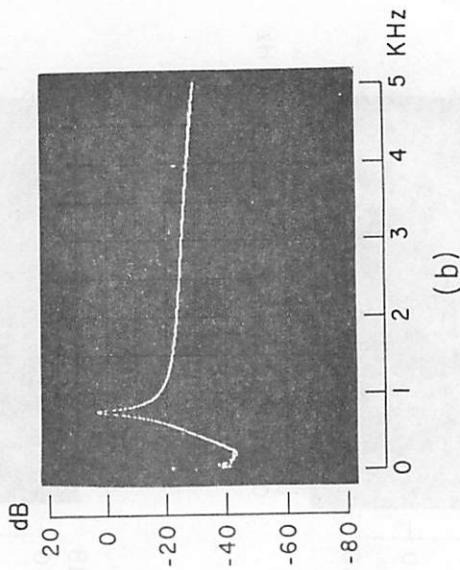


(b)

Figure 5.12 (a) and (b): Measured bandpass response (simulation is in figure 5.13).



(a)



(b)

Figure 5.13 (a) and (b): Measured high-pass response (simulation is in figure 3.12).

5.4.2 Filter Frequency Response Accuracy

A sample size of four fully monolithic bandpass filters were carefully measured to obtain data on the accuracy of the filter center frequency ( $f_0$ ) and bandwidth (Q). Center frequencies of 725 Hz, 728 Hz, 730 Hz and 734 Hz with an 8 kHz sampling rate were obtained, resulting in a mean of 729 Hz and a standard deviation of 0.52%. The 3 dB bandwidth varied over a range from 35 Hz to 42 Hz and the typical Q was 19 (with  $\pm 1.5$  variation).

These frequency response results reflect back to transfer function coefficient accuracies of about  $\pm 0.2\%$ . Since the pole placing coefficients ( $\beta_1$  and  $\beta_2$ ) are determined by the multiplication of two (for  $\beta_1$ ) and three (for  $\beta_2$ ) ratioed capacitors, each capacitor ratio must be in the 0.12% standard deviation range of accuracy. This is assuming random variations in the ratios forming each coefficient.

The error in the mean value of center frequency and Q can be corrected by trimming the capacitor ratio areas on the mask. With this test chip filter the Q achieved was close to the design value of 18, while the center frequency was about 4% away from the design value of 697. The wide deviation in the latter was accounted for in the absolute value of the capacitance ratio forming  $\beta_2$  with amplifier 1. This ratio had been laid out 1.3% lower than it needed to be.

This sampled-data filter chip was capable of operating with a pass-band centered as low as the 1 to 10 Hz region (due to the excellent low leakage property), and as high as 7 kHz (limited by amplifier settling time), simply by varying the clock frequency.

5.4.3 Dynamic Range Performance

A. Noise

The effect of noise sources in the switched capacitor filter on its

TABLE X

Clock Control of the Input Switches in the Programmable Filter (Figure 5.2)

Filter coefficients determining the transmission zeros for:

	Lowpass	Bandpass	Highpass
$\alpha_0$	0.036	0.036	0.036
$\alpha_1$	0	0	- 0.070
$\alpha_2$	0.036	- 0.036	0.036

Clocking Sequence for the Gates of the Transmission Device and

Grounding Device Respectively Controlling Capacitors:

$\alpha_0C$	$(\phi_1, \bar{\phi}_1)$	$(\phi_1, \bar{\phi}_1)$	$(\phi_1, \bar{\phi}_1)$
$\alpha_1C$	$(V_{SS}, V_{DD})$	$(V_{SS}, V_{DD})$	$(\phi_3, \bar{\phi}_3)$
$\alpha_2C$	$(\phi_3, \bar{\phi}_3)$	$(\phi_4, \bar{\phi}_4)$	$(\phi_3, \bar{\phi}_3)$

output noise was considered in Section 3.5.2.A. Experimentally the noise was measured over the frequency band from 0 Hertz out to half the sampling rate (4 kHz). Figure 5.14(a) shows the noise spectrum, on a linear scale, out to 4 kHz (half the sampling rate). It can be seen that the switched-capacitor filter bandlimits the noise about its center frequency. Also, because of the high Q nature of this filter, the noise has been amplified.

The RMS noise was measured with an RMS voltmeter and a filter before it to bandlimit the noise to those frequencies less than the one half of the sampling rate. The measured output RMS noise was found to be 15 to 20 mV over the sample of four monolithic filters. This was measured for the lowpass response shown in Figure 5.14(b) - the noise spectrum is superimposed on a linear scale. This result agrees with the calculation of the filter noise that was given in Section 3.5.2.A. Since the amplifiers are contributing between three and four times more noise than the switches, an improvement in this noise performance would be achieved by using a lower noise amplifier. For example an amplifier with 10  $\mu$ V of RMS input noise (0 to 50 kHz) would reduce the noise by about 10 dB. Also since the switched-capacitor filter is band-limiting the amplifier noise power density, which is dominantly 1/f noise around the center frequency, reduction in the 1/f noise corner frequency with the thermal noise, would greatly reduce the effect of amplifier noise on the filter.

#### B. Distortion

The switched-capacitor filter output signal contained 1% total harmonic distortion (THD) for an output signal of 4.0 volts peak-peak (1.42 volts rms) at the center frequency. It was observed that the distortion

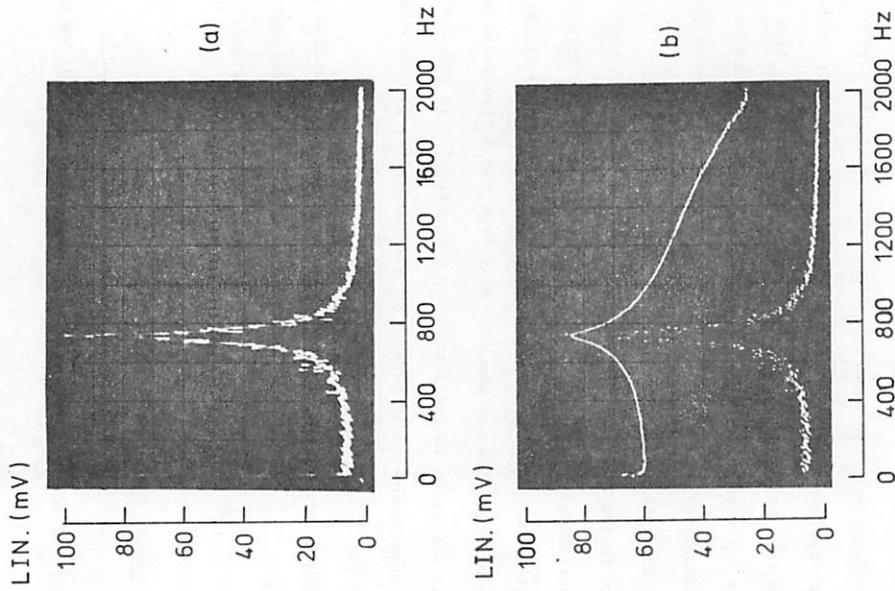


Figure 5.14: Measured noise spectrum at the output of the integrated biquadratic filter, with the input connected to ground.

(a) Lowpass filter's output noise.

(b) Lowpass filter response superimposed on its noise trace.

increased very rapidly around the 4.0 volts peak-peak level, confirming the hypothesis that this distortion was arising from the amplifiers' positive output swing limitation of +3.2 V which caused clipping. Clipping of the output sampled-data waveform at around + 3.2 V was observed with the oscilloscope. Thus the maximum signal level for 1% total harmonic distortion could be increased beyond 4.0 V p-p by increasing the output swing of the NMOS amplifier. CMOS or depletion load NMOS technology provides the capability of larger output voltage swing when used in the amplifier design. It is possible that a 6 to 10 dB improvement in the maximum output signal level for 1% total harmonic distortion could be achieved by using an amplifier designed with either one of these technologies.

#### C. Dynamic Range

The measured results on noise and distortion given in the two previous parts of this section mean that the overall dynamic range of this switched-capacitor filter is 40 dB (RMS output voltage for 1% THD/RMS output noise). Improvements that reduce the noise level by -10 dB and increase the maximum voltage for 1% THD by +10 dB appear to be possible, as discussed in parts A and B of this section. If these improvements were achieved the resulting dynamic range would be 60 dB.

### CHAPTER 6 CONCLUSIONS

A new technique enabling the integration of audio frequency filters in MOS technology has been developed. This approach uses switched ratioed MOS capacitors and MOS amplifiers to realize precision multiplication (with either sign), summation, and delay (sample/hold). With these elements an analog sampled-data recursive filter, having the general biquadratic transfer function, was integrated in single-channel MOS technology. This prototype filter demonstrated that high Q filters, with very precise control of the critical frequencies, can be realized in standard MOS technology without the use of external trimming. The ratio-matching of capacitors was found to achieve a 0.12% standard deviation. The ability to program the filter to produce different frequency responses was also demonstrated. This was done simply by switching in different capacitor ratios for the filter coefficients.

The biquadratic section realized is a basic building block for higher order filters. The area per section when integrated with double polysilicon gate technology is around 2000 mils<sup>2</sup>. Compared with other alternative low sensitivity structures [13] [15], this approach has the following advantages: (1) High Q resonances may be achieved in small silicon area because the capacitor ratios forming the coefficients have an upper limit of 2, and the minimum size capacitor can be small -- there is no parasitic capacitance to suppress.

(2) While the filter sensitivity to coefficient deviation is higher than with the other structures, the coefficients in this approach can exploit the full potential of the ratioed MOS capacitor accuracy without interference from parasitic junction capacitances which can vary.

(3) The lower sampling rates used with this approach (but sufficiently high to simplify the anti-alias filter design), enable a higher degree of filter multiplexing.

The switched-capacitor analog sampled-data filter technique described has the potential to realize monolithic filters with passbands at low frequencies (< 10 Hz), limited only by the leakage current from a minimum size MOSFET source diffusion, and at high frequencies (50-100 KHz), limited by the settling time of the MOS amplifiers.

The realization of an internally compensated operational amplifier, in single-channel MOS aluminum gate technology and using only enhancement devices, achieved higher gain (2200), lower power (15 mw) and smaller area than any previous design. The unity gain settling time to 0.1% was 3.5 usec for a 4 V input step and a 10 pF capacitive load.

#### APPENDIX I.

##### N-CHANNEL MOS ALUMINUM GATE PROCESS

A description of the process used to fabricate the switched-capacitor analog sampled-data recursive filter test chip described in Chapter 4 is contained in this appendix. This NMOS process evolved to its present form through previous efforts [38] [39]. Although the steps necessary for p<sup>+</sup> isolation diffusion are included for completeness, such diffusion has not been used in fabricating the test chip, since it was found unnecessary as explained in Chapter 5. The substrate used was p-type, 100 orientation, and 1-2 Ω-cm resistivity. The process sequence follows below, the abbreviation "DI" stands for deionized water.

##### Fabrication Sequence:

###### 1. Initial wafer cleaning:

- a) DI:HF (9:1), room temperature dip (2 min.)
- b) TCE, 60°C, 10 min.
- c) Acetone, room temperature, 2 min.
- d) DI, rinse
- e) Piranha clean for 15 min.  
 $H_2SO_4:H_2O_2$  (4:1) @ 90°C.
- f) DI, rinse

N<sub>2</sub> blow dry.

###### 2. Initial oxidation: Initial oxidation furnace, growth of 0.92 μm of wet oxide.

- a) Wet O<sub>2</sub>, 0.5 μ/min, 1150°C, 90 min.  
(2.18 on R2-15-B).
- b) Dry N<sub>2</sub>, 0.65 μ/min, 850°C, 10 min  
(2.5 on R2-15-B).

10. Piranha Clean (step 1e)
11. n<sup>+</sup> predeposition: n-type predeposition furnace, 1050°C; POC<sub>2</sub>, 0°C.
- O<sub>2</sub>, 0.1 l/min (2.5 on R2-15-A)  
N<sub>2</sub>, 1.25 l/min (5.0 on R2-15-B)  
Simultaneous flow for 5 min (dry), 1100°C.
  - O<sub>2</sub>, 0.1 l/min.  
N<sub>2</sub>, 1.25 l/min.  
N<sub>2</sub>/POC<sub>2</sub>, 0.096 l/min (6.0 on R2-15-AAA)  
Simultaneous flow for 20 min (dry), 1100°C.
  - N<sub>2</sub>, 1.25 l/min, 10 min (dry), 900°C.
12. Etch Phosphorous glass, NH<sub>4</sub>F:HF, 5:1, 10 sec dip.
13. Piranha Clean (step 1e).
14. Oxide growth over n<sup>+</sup>: n-type drive-in furnace.
- Wet O<sub>2</sub>, 0.5 l/min, 1100°C, 34 min.
  - Dry N<sub>2</sub>, 1.0 l/min, 900°C, 10 min.
15. Photoresist step (gate oxide mask)  
Same as step 3 with oxide etch time of 6.5 min.
16. Piranha Clean (step 1e)
17. Gate oxide growth: n-type drive-in furnace
- TCE purge the furnace for at least 60 min.
  - Set furnace to dry O<sub>2</sub>, 1.5 l/min (6.5 on R2-15-B) and temperature at 1000°C. Insert wafer and leave for 110 minutes.
  - N<sub>2</sub>, 1.0 l/min, 900°C, 10 min. (nitrogen anneal).
18. Etch oxide off the backside of the wafer.
19. Piranha Clean (step 1e)
20. Passivation: n-type predeposition furnace.
- O<sub>2</sub>, 0.1 l/min (2.5 on R2-15-A).  
N<sub>2</sub>, 1.25 l/min (5.0 on R2-15-B).  
Simultaneous flow @ 1000°C, 5 min. (dry).

3. Photoresist step: (p<sup>+</sup> isolation diffusion mask)
- Apply Kodak 747 (Micro Neg) photoresist; spin @ 5000 rpm, 30 sec, single coat.
  - Air dry, 15 min.
  - Prebake, 90°C, 30 min.
  - Expose mask, 4.5 sec.
  - Spray develop, 40 sec.
  - Spray rinse, 30 sec.
  - Alcohol Dip, 7 sec.  
1:1 isopropyl/methanol.
  - Light DI rinse
  - Light N<sub>2</sub> blow dry
  - Postbake, 125°C, 30 min.
  - Oxide etch, NH<sub>4</sub>F:HF (5:1), room temperature, 9.5 min. (0.1µm/min).
  - Photoresist strip, H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub> (4:1), 90°C, 5 min.
4. Piranha Clean (step 1e)
5. p<sup>+</sup> predeposition: p-type predeposition furnace 950°C.
- B<sub>2</sub>H<sub>6</sub>, 0.26 l/min (11.1 on R2-15-D)
  - O<sub>2</sub>, 0.013 l/min (1.7 on R2-15-D)
  - N<sub>2</sub>, 1.3 l/min (5.05 on R2-15-B)
- All gases flow simultaneously for 15 min.
6. Etch boron glass, HF:DI (1:3) dip, 1.0 min.
7. Piranha Clean (step 1e)
8. Oxide growth over p<sup>+</sup>: p-type drive-in furnace, 1150°C.
- Wet O<sub>2</sub>, 0.5 l/min, 16 min. (1.5 on R2-15-B)
  - Dry N<sub>2</sub>, 1.0 l/min, 10 min. (2.5 on R2-15-B)
9. Photoresist step (n<sup>+</sup> diffusion mask)  
Same as step 3 with oxide etch for 10 min.

- 1) Strip photoresist with RT-1 stripper, 5 min. Ensure the wafer is dry beforehand.
- m) DI rinse and N<sub>2</sub> blow dry.
27. Sintering treatment: 15 min @ 450°C in a "forming gas" atmosphere flowing (N<sub>2</sub>/H<sub>2</sub>).

- b) O<sub>2</sub>, 0.1  $\mu$ /min.  
N<sub>2</sub>, 1.25  $\mu$ /min.  
POCl<sub>3</sub>, 0.096  $\mu$ /min. (6.0 on R2-15-AAA).  
Simultaneous flow, 2 min (dry), 1000°C.
- c) N<sub>2</sub>, 1.25  $\mu$ /min, 10 min (dry), 900°C.
21. Piranha Clean (step 1e).
22. Photoresist step (contact mask)  
Same as step 3 with oxide etch time of 1.0 min.
23. Piranha Clean (step 1e)
24. Dry under infrared lamp, 30 min.
25. Evaporate aluminum, 0.8  $\mu$  to 1.0  $\mu$  thickness.
26. Positive Photoresist (metal mask)
- a) Make sure wafer is very dry (use infrared lamp if necessary).  
HMDS-coat in vapor for 5 min.
- b) Apply AZ1350J photoresist, 8000 rpm for 30 sec (single coat)
- c) Prebake, 80°C, 15 min.
- d) Expose mask, 4.0-8.0 sec (depending on lamp intensity).
- e) 100°C bake.
- f) Develop with AZ1350J Developer.  
Developer:DI (1:1), 60 sec.
- g) High temperature postbake, 140°C, 10 min.
- h) Etch aluminum with aluminum etchant type A, 50°C with ultrasonic agitation. Remove wafer when metal pattern just starts to appear.
- i) DI rinse and bake for 5 min @ 140°C.
- j) Finish etching of the aluminum pattern.
- k) DI rinse.

APPENDIX II

MOSFET DEVICE EQUATIONS AND SMALL-SIGNAL PARAMETERS

The following simple NMOS device equations from the Shichman and Hodges MOSFET model are satisfactory for first-order calculations. The basic MOSFET transistor symbol is given in Figure A.1(a).

(1) Nonsaturation region ( $V_{GS} - V_T > V_{DS}$ ):

$$I_D = k' \left(\frac{W}{L}\right) [2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \tag{A.1}$$

(2) Saturation region ( $V_{GS} - V_T \leq V_{DS}$ ):

$$I_D = k' \left(\frac{W}{L}\right) (V_{GS} - V_T)^2 \tag{A.2}$$

where  $W$  and  $L$  are the gate width and length, respectively,  $V_T$  is the threshold voltage, and the quantity  $k'$  is given by

$$k' = \frac{1}{2} \mu_0 C_{OX} \tag{A.3}$$

where  $\mu_0$  is the effective electron mobility of carriers and  $C_{OX}$  is the gate oxide capacitance per unit area.

The operation of the MOS transistor as a four-terminal device is considered by including the effect of substrate-source bias through the threshold voltage  $V_T$ . If  $V_{T0}$  represents the value of  $V_T$  for  $V_{BS} = 0$ , then:

$$V_T = V_{T0} + \gamma (\sqrt{V_{BS} + 2\phi_F} - \sqrt{2\phi_F}) \tag{A.4}$$

where  $\phi_F$  is the Fermi potential and  $\gamma$  is given by:

$$\gamma = \frac{\sqrt{2\epsilon_s q N_A}}{C_{OX}} = \text{body effect coefficient.} \tag{A.5}$$

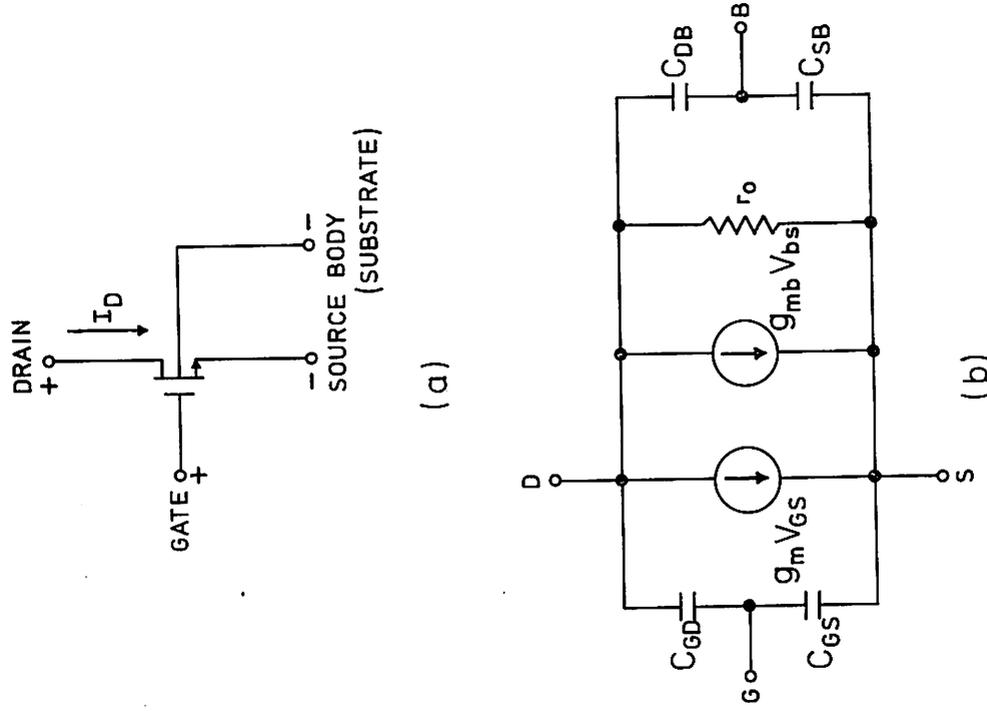


Figure A.1: (a): MOSFET circuit symbol. (b): Small signal equivalent circuit for the MOSFET.

The dependence of  $V_T$  on  $V_{BS}$  gives rise to a  $V_{BS}$ -to- $I_D$  transconductance  $g_{mb}$ .

The small signal equivalent circuit, including intrinsic MOS parasitic capacitances, is shown in Figure A.1(b).

Here  $\epsilon_S$  is the permittivity of silicon,  $q$  the electron charge, and  $N_A$  the substrate impurity concentration.

For some applications it is important to express the fact that  $I_D$  is dependent on  $V_{DS}$  in the saturation region, i.e. that the drain current characteristic has some finite slope even if this slope is rather small. The equation in the saturation region can then be modified to show this effect:

$$I_D = k' \left(\frac{W}{L}\right) [V_{GS} - V_T]^2 (1 + \lambda V_{DS}) \quad \text{A.6}$$

where  $\lambda$  is the channel length modulation parameter.

The small signal MOSFET parameters are defined in terms of partial derivatives of the terminal voltages and currents.

(1) Nonsaturation region:

$$\text{- transconductance; } g_m = \frac{\partial I_D}{\partial V_{GS}} = 2k' \left(\frac{W}{L}\right) V_{DS} \quad \text{A.7}$$

$$\text{- output conductance; } \frac{1}{r_o} = \frac{\partial I_D}{\partial V_{DS}} = 2k' \left(\frac{W}{L}\right) (V_{GS} - V_T - V_{DS}) \quad \text{A.8}$$

(2) Saturation region:

$$\text{- transconductance; } g_m = 2 \sqrt{k' \left(\frac{W}{L}\right) I_D (1 + \lambda V_{DS})} \quad \text{A.9}$$

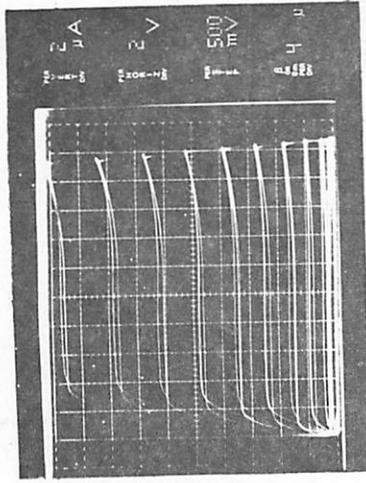
$$\text{- output conductance; } \frac{1}{r_o} = \frac{\lambda I_D}{1 + \lambda I_D} \quad \text{A.10}$$

Since usually  $\lambda V_{DS} \ll 1$  the last two expressions can be written:

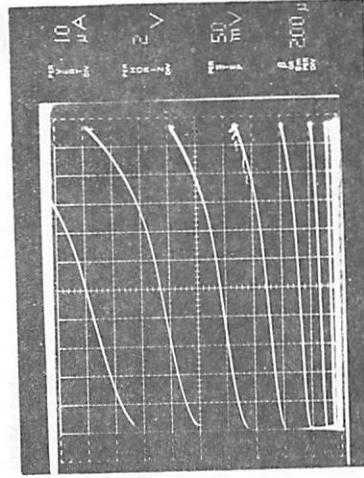
$$g_m = 2 \sqrt{k' \left(\frac{W}{L}\right) I_D} \quad \text{A.11}$$

and

$$\frac{1}{r_o} = \lambda I_D \quad \text{A.12}$$



(a)



(b)

Figure A.2: MOSFET  $I_D$  versus  $V_{DS}$  characteristics (enhancement devices).

(a) Long Device :  $W/L = 0.075$ .

(b) Wide Device :  $W/L = 33$  (after lateral diffusion).

### APPENDIX III

#### MOSFET MODEL PARAMETERS FOR THE OPERATIONAL AMPLIFIER SIMULATION

Figure A.2(a) and (b) show the drain current-voltage characteristics of two N-channel aluminum gate enhancement mode MOSFET test transistors measured on the prototype filter test chip. The long device has mask dimensions of  $W = 10$  mil and  $L = 0.5$  mil while the wide device has  $W = 0.6$  mil and  $L = 8$  mil.

A substrate MOS capacitor was also included on the chip for process evaluation. From capacitance-voltage measurements [46] with this capacitor, the p-type substrate doping at the surface was calculated to be  $5 \times 10^{15} \text{ cm}^{-3}$ , the oxide thickness:  $770 \text{ \AA}$ , the threshold voltage  $V_{GS}^{Q_{SS}}$  (zero body bias voltage):  $0.2 \text{ V}$ , and the surface state density  $(\frac{Q_{SS}}{q})$ :  $7 \times 10^{-2} \text{ cm}^{-2}$ .

From the device behavior in the linear region of the test transistors, the electron mobility ( $\mu_0$ ) was calculated to be  $850 \text{ cm}^2/\text{v. sec}$ . Also using the linear region of the two test devices (one wide and one long) the lateral diffusion was calculated to be  $4.2 \text{ \mu m}$  -- the ratio of the two devices' drain currents, at the same  $V_{GS}$  and  $V_{DS}$  condition, is dependent only on their geometry ratio.

SPICE2 was used for the simulation of the MOS operational amplifier circuit. The drain current characteristics of the test transistors were simulated on SPICE2 first. The MOS model for SPICE2 is described in [47]. The parameter values derived for the wide device and the long device were verified by comparing the simulated characteristics with those actually measured (Figure A.2(a) and (b)). In the saturation region drain current was matched to within 10% over the useful range of  $V_{GS}$  and  $V_{DS}$ . The MOS model parameters used in the SPICE2 simulations of the MOS operational amplifier were:

<u>Parameter</u>	<u>Description</u>	<u>Value</u>
NSUB	Substrate Doping	$5.0 \times 10^{15} \text{ cm}^{-3}$
UO	Surface Mobility	$850 \text{ cm}^2/\text{v.s.}$
T <sub>OX</sub>	Oxide Thickness	$0.0777 \times 10^{-4} \text{ cm}$
XJ	Metallurgical Junction Depth	$4.2 \times 10^{-4} \text{ cm}$
LD	Lateral Diffusion Coefficient	0.83
LAMBDA	Channel Length Modulation Parameter	0.02 wide device 0.0056 long device
UCRIT	Critical E Field for Mobility Degradation	200 K V/cm
UEXP	Critical Field Exponent	0.05
NSS	Effective Surface State Density	$7.12 \times 10^{10} \text{ cm}^{-2}$
GS	Gate-Source Overlap Capacitance per cm of Channel Width	33 pF/cm
CGD	Gate-drain Overlap Capacitance per cm of channel width	33 pF/cm
CBD	Zero bias Substrate-source Junction Capacitance per cm <sup>2</sup> of Junction Area	22 nF/cm
CBS	Zero bias Substrate-drain Junction Capacitance per cm <sup>2</sup> of Junction Area	22 nF/cm

## APPENDIX IV

## Program DINAP

DINAP stands for Digital Network Analysis Program [34]. It was developed at the School of Electrical Engineering in Purdue University to perform three kinds of analysis on digital filters built from the following three basic elements:

1. Digital adder
2. Delay unit (delays signal for one sampling period).
3. Multiplier (scales the input by a fixed constant).

The types of analysis are:

1. Frequency response (sinusoidal steady-state response to a single input, i.e. all elements are assumed linear).
2. Noise analysis (approximation to power spectral density of noise due to round-off error at the output of all multipliers and input quantization noise).

3. Transient analysis.

The synthesis of switched-capacitor analog sampled-data recursive filters can be verified through the frequency response analysis of DINAP. These filters only have the three basic elements: the adder (summation), the delay unit, and the multiplier. During frequency response analysis full precision is set for the multipliers and the information line. Therefore the analog sampled-data filters are simulated to within the accuracy of the computer arithmetic for these conditions.

The effect of noise on the signal paths within the analog sampled-data filter can be simulated by using the noise analysis in DINAP. By choosing the information line bit precision suitably, one can see the effect of broadband noise on the output. In the digital filter the

broadband noise arises from signal quantization and rounding on the information line. In a switched-capacitor filter the broadband noise arises from the MOS amplifier broadband noise (there is also a  $1/f$  noise component at frequencies less than 1-5 kHz).

## APPENDIX V

## SAMPLED-DATA RECURSIVE STRUCTURES WITH LOW COEFFICIENT SENSITIVITIES

The experimental results presented for the switched-capacitor biquadratic section in Chapter 5 were those of a direct form realization of a second-order sampled-data recursive filter (Figure A.3). The sensitivities of  $\omega_0$  and  $Q$  for this structure were given in equations 3.11(a)-(d), based on small  $\omega_0 T$ . It could be seen there that high  $Q$  sections which had small  $\omega_0 T$  (high ratio of sampling rate to center frequency) were most sensitive to variations in the ratioed capacitors determining the coefficients. On the other hand for  $\omega_0 T$  close to  $\frac{\pi}{4}$  (i.e.  $\frac{f_0}{f_s} = 1/4$ ) and high  $Q$ , these sensitivities are much smaller. This can be seen from the pole sensitivities which in general form are:

$$[\theta = \omega_0 T, \beta_1 = 2r \cos \theta, \beta_2 = -r^2].$$

$$s_{\beta_1}^r = 0 \quad \text{A.13(a)}$$

$$s_{\beta_2}^r = -\frac{1}{2r} \quad \text{A.13(b)}$$

$$s_{\beta_1}^\theta = -\frac{1}{2r \sin \theta} \quad \text{A.13(c)}$$

$$s_{\beta_2}^\theta = -\frac{1}{2r^2 \tan \theta} \quad \text{A.13(d)}$$

When the achievable accuracies of the ratioed capacitors are insufficient to obtain the required frequency response control, then alternative low sensitivity structures must be considered.

Gold and Radar [35] have proposed a coupled form realization whose structure is shown in Figure A.4. The transfer function for this is:

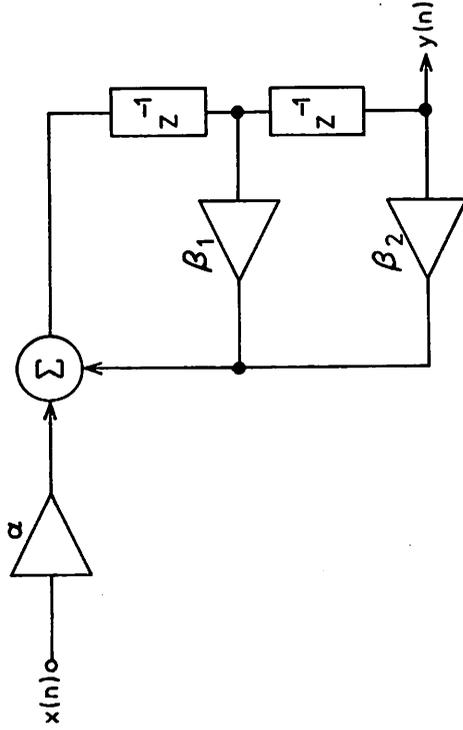


Figure A.3: Direct form second order section.

$$H(z) = \frac{k_0 k_1 z^{-2}}{1 - (m_1 + m_2)z^{-1} + (m_1 m_2 - k_1 t)z^{-2}} \quad \text{A.15}$$

while the direct form shown in Figure A.3 has the transfer function:

$$H(z) = \frac{\alpha z^{-2}}{1 - 2r \cos \theta z^{-1} + r^2 z^{-2}} \quad \text{A.16}$$

Thus these two filters realize the same pole pair of:

$$m_1 + m_2 = 2r \cos \theta$$

$$m_1 m_2 - k_1 t = r^2$$

Minimum sensitivity occurs for  $m_1 = m_2 = r \cos \theta$  and is roughly proportional to  $\frac{Q}{\omega_0^T}$  [36]. This coupled form structure also has significantly improved noise performance over the direct form when  $\omega_0^T$  (i.e.  $\theta$ ) is small [23].

Another low sensitivity second-order section was developed by Agarwal and Burrus [37] for sampled-data filters with poles near the unit circle and with poles near  $z = 1$  (i.e. high Q and small  $\omega_0^T$ ). This structure is shown in Figure A.5. It has the property that when the poles asymptote to  $z = 1$ , the sensitivities to the feedback coefficients approach 1.0, somewhat similar to the parameters of a state-variable filter second-order filter. In switched-capacitor form this structure (Figure A.5) has a very simple realization since the basic element:

$$\frac{z^{-1}}{1-z^{-1}}$$

is a sampled-data integrator or accumulator, and has the switched-capacitor form shown in Figure A.6(b).

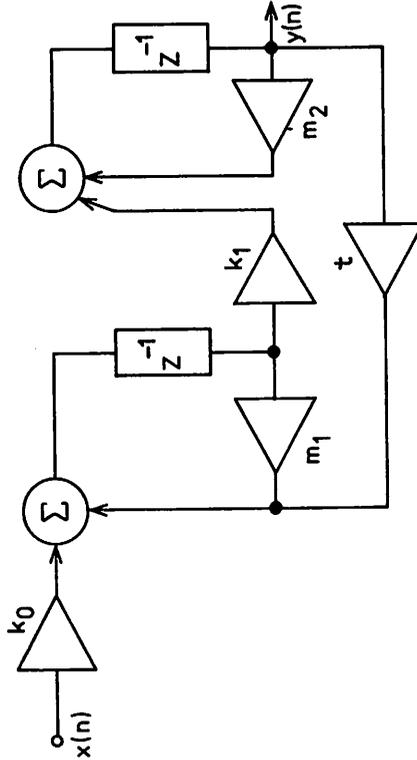


Figure A.4: The coupled form second order section.

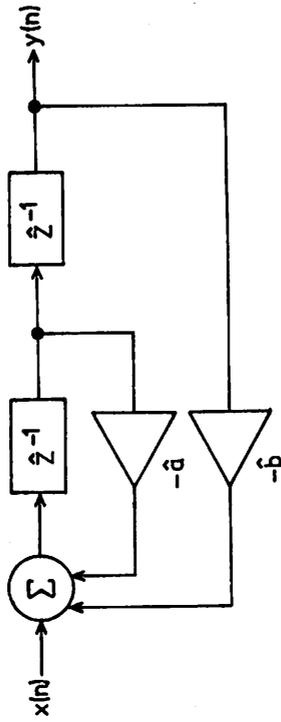
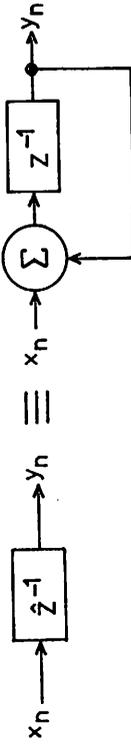
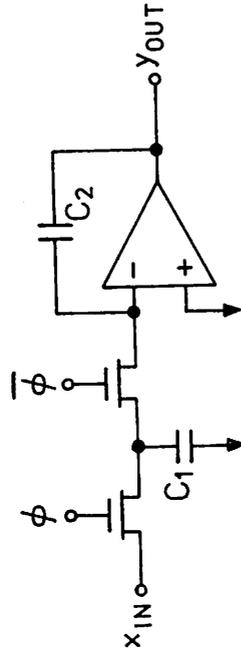


Figure A.5: Low sensitivity second order section by Agarwal and Burrus (see figure A.6.a for the  $z^{-1}$  block description).



(a)



(b)

Figure A.6: (a): Sampled-data integrator. (b): Switched-capacitor integrator.

This second-order filter is the same as the version 1 sampled-data state-variable filter in the paper by Hosticka et al. [13]. Both of these filters have low sensitivities when  $\omega_0 T$  (i.e.  $\frac{f_0}{f_s}$ ) is very small. When  $\omega_0 T$  is not very small the finite "phase shift" through the sampled-data integrator moves the poles and lowers their Q. Thus the design must use higher Q than the actual desired value; the price paid for this is higher sensitivity. The cause of this problem is that this sampled-data integrator is equivalent to integration by backward differences, which is only accurate for high sampling rates (refer to equation 3.8).

The Agarwal and Burrus low sensitivity second-order section, and the sampled-data state variable filter from Hosticka et al., have lower output signal to noise ratios than the coupled form and direct form structures. Unlike the latter, their signal to noise ratios do not increase with sampling rate, but remain proportional to  $Q^2$ .

To overcome the problem of phase shift in discrete-time integrators used with digital ladder filters, Bruton [33] proposed a lossless discrete-time integrator. This was easily implemented in switched-capacitor form for the ladder filters [16] and improved the sensitivity performance. However, the ideal sensitivity of the doubly terminated ladder is still not attained because the terminations require a one half delay element, which could not be implemented. High sampling rates are still necessary to maintain a close approximation to the zero sensitivity of this doubly terminated structure. The two papers in Appendices VII and VIII address this problem of realizing switched-capacitor filters that will have the ideal sensitivity of a continuous-time filter equivalent, no matter what sampling rate (high or low) is used in the design.

APPENDIX VI

The following paper was presented at the 1977 IEEE International Solid State Circuits Conference, (Philadelphia) held on the 16th, 17th and 18th February.

## SESSION XIII: MOS SAMPLED DATA SIGNAL PROCESSING

## THPM 13.5: Analog NMOS Sampled-Data Recursive Filter\*

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MONOLITHIC INTEGRATION of precision audio frequency filters has been a difficult objective to reach. Active RC filters using numerous off-chip precision RC elements have been in use for years<sup>1</sup>. Transversal filters using CCD or BBD approaches occupy very large silicon areas when fully integrated with all peripheral circuits<sup>2</sup>. Fully integrated digital filters require precision linear A/D coders and also require a large silicon area<sup>3</sup>. Analog sampled-data recursive filters have been described previously, but these employed many off-chip precision components<sup>4,5</sup>.

This paper will describe the design of a fully-integrated NMOS analog sampled-data recursive bandpass filter, and discuss experimental results for the critical elements and for partially integrated feasibility models in both metal-gate and silicon-gate NMOS technologies.

A block diagram for the canonic form of a second-order recursive filter is shown in Figure 1 (a). The transpose equivalent form of Figure 1 (b) is simpler to realize in this case. The latter has been implemented as an analog sampled-data system, as shown in Figure 2. Multiplier coefficients are realized using precision-ratioed integrated capacitors and integrated operational amplifiers. For instance, the feedback coefficient  $\alpha_2$  is determined by the ratio of input capacitance  $\alpha_2 C$  to integrating capacitance  $C$  at the left in Figure 2. This integrating multiplier also provides a time delay with period and precision determined by a system clock. Four equal, nonoverlapping clock phases control the operation of the complete second-order section. Multiple subscripts on phase

labels indicate switches which must remain closed during each of several phases.

In the narrowband approximation, center frequency  $f_0$  is determined primarily by a  $\alpha_1$  while bandwidth or  $Q$  is primarily a function  $\alpha_2$ . The sensitivity of  $f_0$  to  $\alpha_1$  is approximately  $(2\pi f_0/f_s)^{-2}$ , while the sensitivity of  $Q$  to  $\alpha_2$  is approximately  $Q/(2\pi f_0/f_s)$ . As an example, consider a filter requiring  $f_0 = 697 \text{ Hz} \pm 0.5\%$  and  $Q = 18 \pm 1$ : assume an 8 kHz sample rate. In this example  $\alpha_1$  and  $\alpha_2$  each must be controlled to within  $\pm 0.17\%$ .

The NMOS operational amplifier used is shown in Figure 3. It has higher gain and lower power consumption than a previously-reported design<sup>6</sup>. Open-loop gain of 2000 was required to minimize coefficient error due to amplifier gain variations. Internal compensation is achieved with a 7-pF capacitor; feedforward is exploited to enhance stability. A shunt-shunt feedback output stage provides a low output impedance.

Measured parameters for a NMOS metal-gate enhancement-only version of this amplifier include gain of 2000; settling time to 0.5% for a 2-V step and 20 pF load, 8  $\mu\text{s}$ ; and 16-mW power consumption from a 15-V supply.

For maximum precision, ratioed capacitors were designed with common-centroid geometry, nearly constant area/perimeter ratios, and constant metal or polysilicon etch width. These precautions minimize the effects of oxide thickness gradients, and of variations in resist exposure and etch undercut<sup>7</sup>. The geometries evident in Figures 4 and 5 permit realization of capacitor pairs, triples, or quads of arbitrary ratios; only a single mask level need be modified to change capacitor ratios. Preliminary data show ratio accuracy on the order of 0.1%.

Experimental measurements on a discrete-component breadboard confirmed all essential features of filter performance.

BIAS CIRCUIT

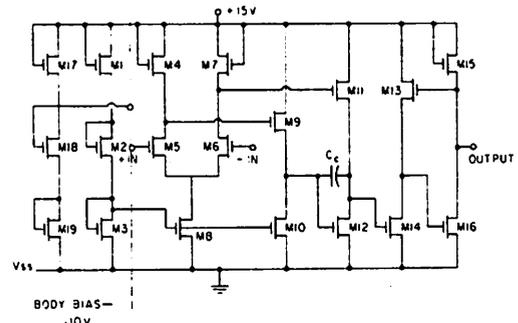


FIGURE 3 - Schematic of operational amplifier. A single bias circuit is shared by all amplifiers in the filter. Amplifier die area is about 500 mil<sup>2</sup> in metal-gate NMOS.

\*Research sponsored by the National Science Foundation Grant ENG73-04184-A01.

<sup>1</sup>Mitra, S.K., Editor. "Active Inductorless Filters". IEEE Press, 1971.

<sup>2</sup>Hewes, C.R., "A Self-Contained 800 Stage CCD Transversal Filter", Proc. Int'l. Conf. on the Application of Charge-Coupled Devices, p. 309-318; 1975.

<sup>3</sup>Edwards, G.P., et al., "A MOS LSI Double Second-Order Digital Filter Circuit", ISSCC Digest of Technical Papers, p. 20-21; Feb., 1975.

<sup>4</sup>Smith, D.A., et al., "Programmable Bandpass Filter and Tone Generator Using Bucket-Brigade Delay Lines", IEEE Trans. Comm. 22, 7, p. 921-925; July, 1974.

<sup>5</sup>Mattern, J. and Lampe, D.R., "A Reprogrammable Filter Bank Using CCD Discrete Analog Signal Processing", IEEE Jour. Solid-State Circuits SC-11, 1, p. 88-92; Feb., 1976.

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<sup>7</sup>McCreary, J. L. and Gray, P.R., "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques - Part 1", IEEE Jour. of Solid-State Circuits SC-10, 6, p. 371-379; Dec., 1975.



## APPENDIX VII

The following article was published in the "Electronics Letters,"  
27th April 1978, Vol. 14, No. 9.

## AN IMPROVED SWITCHED-CAPACITOR INTEGRATOR

*Indexing terms: Integrating circuits, Switched networks*

A novel switched-capacitor integrator is described which results in the mapping of the analogue frequency axis directly on the unit circle of the  $z$ -plane. The circuit requires one extra capacitor and additional switches. It makes the design much easier and doubles the effective sampling rate.

Recently, there has been great interest in the realisation of analogue filters using switched and fixed capacitors and active elements.<sup>1-3</sup> The basic building block of these filters is the integrator shown in Fig. 1. Assuming that the time constants

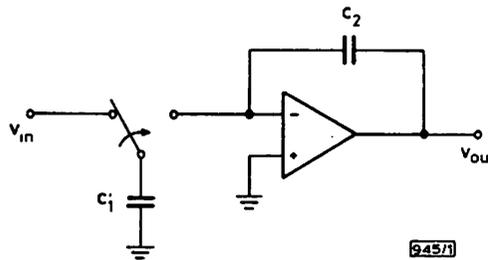


Fig. 1 Basic switched capacitor integrator

formed by  $C_1$  and the resistances of its charging and discharging circuits are much smaller than the switching period  $T$ , the output voltage of the circuit satisfies the difference equation<sup>1</sup>

$$C_2 v_{out}[nT] = C_2 v_{out}[(n-1)T] - C_1 v_{in}[(n-1)T] \quad (1)$$

corresponding to a transfer function

$$H(z) \triangleq \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2} \frac{z^{-1}}{1-z^{-1}} \quad (2)$$

For radian frequencies satisfying  $\omega \ll 1/T$ , on the unit circle in the  $z$  plane  $z = e^{j\omega T} \cong 1 + j\omega T$ , and  $H(z) \cong -(C_1/C_2)/j\omega T$ . Hence, the circuit response approximates that of an integrator for low analogue frequencies.

For higher frequencies, the approximation becomes poor. In fact, the mapping  $s \rightarrow z - 1$  which is implicit in the transfer function (eqn. 2) transforms the  $j\Omega$  axis of the analogue  $s$ -plane into a vertical line going through the  $z = 1$  point in the  $z$  plane, rather than into the unit circle.<sup>4</sup> Hence, analogue filter responses (other than very-low-frequency lowpass ones)

will become distorted when switched-capacitor integrators replace the analogue ones. Thus, an active filter circuit, such as the well-known leapfrog circuit,<sup>5</sup> will not automatically transform into an equivalent sampled-data filter simply by replacing all integrators.

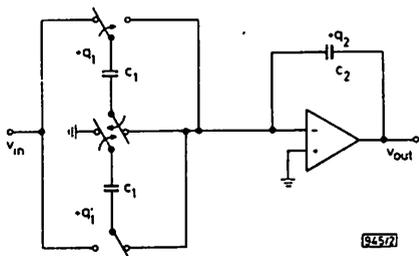


Fig. 2 Switched capacitor integrator which results in doubled sampling rate and the bilinear transformation

Next, some modifications of the circuit of Fig. 1 are described which overcome this difficulty. Consider the circuit shown in Fig. 2. If the switches are in the positions indicated during the period  $(n-1)T$  to  $nT$ , then  $q_1$  grows from  $q_1[(n-1)T] = 0$  to  $q_1(nT) = C_1 v_{in}(nT)$ , while  $q_1$  decreases from  $q_1[(n-1)T] = C_1 v_{in}[(n-1)T]$  to  $q_1(nT) = 0$ . Both changes decrease  $q_2$  by these same amounts. Hence,

$$\begin{aligned} q_2(nT) - q_2[(n-1)T] &= C_2 v_{out}(nT) - C_2 v_{out}[(n-1)T] \\ &= -C_1 v_{in}(nT) - C_1 v_{in}[(n-1)T] \end{aligned} \quad (3)$$

results. During the time  $nT < t < (n+1)T$ , the switches are in their other positions and the capacitors change roles. Clearly, eqn. 3 remains valid.

Using z-transformation, eqn. 3 gives the transfer function

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2} \frac{1+z^{-1}}{1-z^{-1}} \quad (4)$$

Since the circuit is to function as an integrator, the relation, implied by eqn. 4, between the analogue complex frequency variable  $s$  and the sampled-data variable  $z$  becomes the familiar bilinear transformation<sup>4</sup>

$$s = \frac{2}{T} \frac{1-z^{-1}}{1+z^{-1}} \quad (5)$$

Eqn. 5 maps the  $j\Omega$  axis of the  $s$  plane on the unit circle in the  $z$  plane; the radian frequencies are related by  $\Omega T/2 = \tan(\omega T/2)$ . Hence, for low-frequency lowpass filters ( $\omega \ll 1/T$ ), the linearity error is proportional to  $(\omega T)^3$ , rather than  $(\omega T)^2$  as for the approximation represented by eqn. 2. More importantly, since the  $\omega$  and  $\Omega$  axes are mapped onto each other, any analogue filter response will essentially preserve its character; e.g. an analogue bandpass filter will become a sampled-signal bandpass filter, of the same passband ripple and stopband loss, etc. The effects of aliasing and the nonlinearity of the  $\Omega$ - $\omega$  mapping must, of course, still be considered. However, there is no need to prewarp the poles and zeros of the

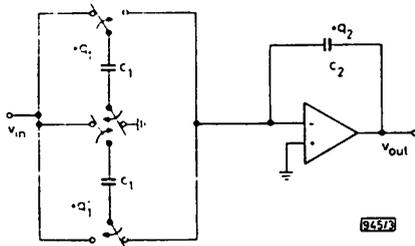


Fig. 3 Alternative realisation of the circuit of Fig. 2

288

analogue filter, or to optimise iteratively the sampled-signal circuit. Also, the sampling rate is effectively doubled.

The price paid for the improved performance and ease of design is, of course, the additional capacitor, and extra switches, each corresponding to two m.o.s.f.e.t.s in integrated realisation. It is conjectured that the sensitivity of a leapfrog-type filter designed using the modified structure is lower than that of one constructed from the integrators of Fig. 1, since the correspondence with the doubly-terminated LC filter is better preserved in the new structure.

Other circuits can be constructed which satisfy eqn. 3, and hence act as sampled-signal integrators. One such circuit is illustrated in Fig. 3. Here, the two capacitors take turns in charging and discharging  $C_1\{v_{in}(nT) + v_{in}[(n-1)T]\}$  into  $C_2$ .

Simpler circuits, using only one switched capacitor  $C_1$ , are also possible, if asymmetric clock pulses and/or unequal sampling intervals can be tolerated.

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## APPENDIX VIII

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## SWITCHED-CAPACITOR FILTER SECTIONS IMPLEMENTING THE BILINEAR TRANSFORMATION

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ABSTRACT

Some novel switched-capacitor filter sections are proposed that can implement analog sampled-data filters based upon the bilinear transformation from analog active filters. A two-input-single-output switched-capacitor circuit is presented which can function either as a lossless summing integrator, or as a lossless difference integrator with an extra output term. As an application, a low sensitivity filter section using this circuit is described. Also switched-capacitor circuits are presented for the realization of a difference integrator and a lossy sum integrator, which are the only components needed for the realization of the sampled-data version of a multifeedback active filter.

I. INTRODUCTION

In a recent letter [1], a single-input integrator containing switches, capacitors and an operational amplifier was described. Its transfer function could be obtained from that of an ideal analog integrator via the bilinear transformation  $s = (2/T)(z-1)/(z+1)$ ; hence, (using Bruton's definition<sup>2</sup>) it is a lossless integrator. This transformation has also been the basis of other recent work<sup>3,4,5</sup>.

In this paper a related circuit is first given which extends the basic function of the circuit given in reference [1], to summing and subtracting

integration. This is followed by a description of some new switched-capacitor integrator circuits that are useful in the low-sensitivity multi-feedback ("leapfrog") filter configuration<sup>6</sup>, namely a differential integrator for its internal stages, and lossy integrators for the first and last stages. All these circuits possess the important advantage that their transfer functions relate to those of their analog models via the bilinear transformation. Hence the frequency axes of the analog filter model and the derived sampled-data circuit are exactly mapped onto each other.

II. LOSSLESS SWITCHED-CAPACITOR INTEGRATOR CIRCUITS

Consider the circuit of Fig. 1. The basic equations relating the charges and voltages before and after the operation of the switches are

$$\begin{aligned} q_1(n-1) &= C_1[v_+(n-1) - v_2(n-1)] \\ q_1(n) &= C_1[v_1(n) - v_+(n)] \\ q_1'(n-1) &= C_1[v_+(n-1) - v_1(n-1)] \\ q_1'(n) &= C_1[v_2(n) - v_+(n)] \end{aligned} \quad (1)$$

and

$$\begin{aligned} q_2(n-1) &= C_2[v_o(n-1) - v_+(n-1)] \\ q_2(n) &= C_2[v_o(n) - v_+(n)]. \end{aligned} \quad (2)$$

From Fig. 1, clearly also

$$q_2(n) - q_2(n-1) = q_1(n-1) - q_1(n) + q_1'(n-1) - q_1'(n). \quad (3)$$

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Substituting from (1) and (2) into (3), and taking the z-transform, gives

$$V_o(z) = -\frac{C_1}{C_2} \frac{1+z^{-1}}{1-z^{-1}} [V_1(z)+V_2(z)] + [2 \frac{C_1}{C_2} \frac{1+z^{-1}}{1-z^{-1}} + 1]v_+(z). \quad (4)$$

For  $v_+ \equiv 0$ , (4) gives

$$V_o(z) = -\frac{C_1}{C_2} \frac{1+z^{-1}}{1+z^{-1}} [V_1(z)+V_2(z)], \quad (5)$$

corresponding to the transfer function of a lossless summing integrator. For  $v_+ \equiv v_2$ , (4) becomes

$$V_o(z) = \frac{C_1}{C_2} \frac{1+z^{-1}}{1-z^{-1}} [V_2(z)-V_1(z)] + V_2(z). \quad (6)$$

Hence, now the output voltage is the discrete equivalent of the integral of  $(V_2-V_1)$ , plus the input  $V_2$ . As an example application of the latter circuit, Fig. 2a illustrates how this circuit can be utilized as a building block in the low-sensitivity second-order filter section realizing

$$\frac{V_{out}}{V_{in}} = \frac{b_1 b_2}{s^2 + b_1 s + b_1 b_2} \quad (7)$$

The second stage of the section in Fig. 2b corresponds to the case when  $v_+ \equiv v_2 \equiv 0$ . Then the circuit of Fig. 1 reverts to the single-input integrator discussed in Ref. 1.

A delay free loop can arise when using this integrator based on the bilinear transformation. A sample and hold is then required at the filter's input to avoid the input signal feeding directly through to the output.

### III. SWITCHED-CAPACITOR FILTER SECTIONS FOR MULTIFEEDBACK ACTIVE FILTERS

Fig. 3a illustrates the realization of the differential integrator. At time  $(n-1)T$ , the stored charges are

$$\begin{aligned} q_1(n-1) &= C_1 [v_1(n-1) - v_+(n-1)] \\ q_1'(n-1) &= C_1 [v_2(n-1) - v_-(n-1)] \\ q_2(n-1) &= C_2 [v_-(n-1) - v_o(n-1)] \\ q_2'(n-1) &= C_2 v_+(n-1). \end{aligned} \quad (8)$$

At time  $nT$ , the charges become

$$\begin{aligned} q_1(n) &= C_1 [v_2(n) - v_-(n)] \\ q_1'(n) &= C_1 [v_1(n) - v_+(n)] \\ q_2(n) &= C_2 [v_-(n) - v_o(n)] \\ q_2'(n) &= C_2 v_+(n). \end{aligned} \quad (9)$$

For ideal operational amplifier performance,  $v_+ = v_-$ ; also, the input currents of the amplifier

are zero. Hence, due to the conservation of charge,

$$\begin{aligned} q_2(n) - q_2(n-1) &= q_1(n) - q_1(n-1) \\ q_2'(n) - q_2'(n-1) &= q_1'(n) - q_1'(n-1). \end{aligned} \quad (10)$$

Combining the above relations and using z-transformation, the result

$$V_o(z) = \frac{C_1}{C_2} \frac{1+z^{-1}}{1-z^{-1}} [V_1(z) - V_2(z)] \quad (11)$$

is obtained. Clearly, (11) is the discrete-time version of the input/output relation of a difference integrator. Leakage current from the inverting input node of the amplifier, can present a practical problem with this circuit.

Figure 3b illustrates an alternative realization for the difference integrator. It can be analyzed in the same manner as the circuit of Fig. 3a, and turns out to have the same transfer function. Its leakage characteristics, however, are expected to be better.

Figure 4 shows the circuit needed for the input and output stages of the multiloop-feedback filter. The analog circuit which it models has the transfer function

$$V_o(s) = k_1 \frac{V_1(s) + V_2(s)}{s + s_0} \quad (12)$$

where  $s_0 > 0$ . Using the bilinear transformation (12) is transformed into

$$V_o(z) = k_2 [V_1(z) + V_2(z)] \frac{1+z^{-1}}{1-(1-d)z^{-1}} \quad (13)$$

where  $d = (s_0 T)/(1+s_0 T/2) > 0$ . Next, it will be shown that this is the input/output relation of the circuit of Fig. 4.

At time  $(n-1)T$  (i.e., one clock interval  $T$  before the situation shown in Fig. 4), the stored charges are

$$\begin{aligned} q_1(n-1) &= C_1 [v_-(n-1) - v_2(n-1)] \\ q_1'(n-1) &= C_1 [v_-(n-1) - v_1(n-1)] \\ q_2(n-1) &= C_2 [v_-(n-1) - v_o(n-1)] \\ q_3(n-1) &= d \cdot C_2 v_o(n-1) \\ q_3'(n-1) &= 0. \end{aligned} \quad (14)$$

After the switches change their positions to that shown in Fig. 4, the charges become

$$\begin{aligned}
 q_1(n) &= C_1[v_1(n)-v_-(n)] \\
 q_1'(n) &= C_1[v_2(n)-v_-(n)] \\
 q_2(n) &= C_2[v_-(n)-v_o(n)] \\
 q_3(n) &= 0 \\
 q_3'(n-1) &= v_o(n).
 \end{aligned}
 \tag{15}$$

Conservation of charge requires that

$$\begin{aligned}
 q_2(n) - q_2(n-1) &= q_1(n) - q_1(n-1) + q_1'(n) - q_1'(n-1) \\
 &\quad - q_3(n) + q_3(n-1)
 \end{aligned}
 \tag{16}$$

Substituting from (14) and (15) into (16) and using z-transformation (13) is obtained, with  $k_2 = -C_1/C_2$ .

It is important to note that a "leapfrog" filter built using the building blocks of Figs. 3 and 4 will be insensitive to variations of the capacitances for two different reasons: first, because the circuit models a doubly-terminated reactance two-port, and secondly, because only the ratios of the capacitance affect the transfer function. Hence, such a filter will be a prime candidate for integrated realizations, as pointed out (for different switched-capacitor filters) by previous authors<sup>7,8</sup>.

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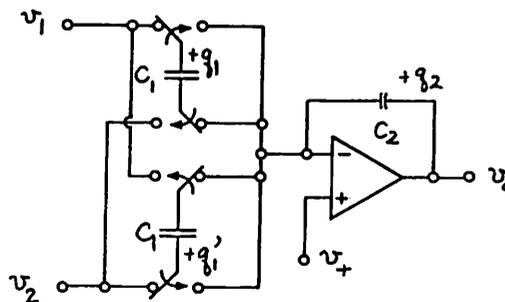


Fig. 1. Sum/difference integrator.

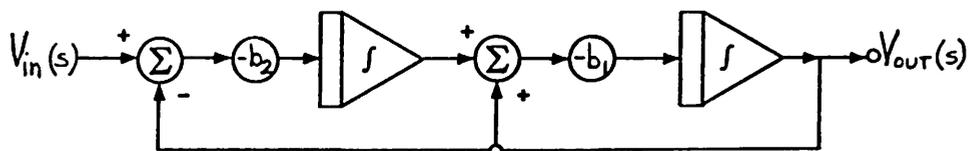


Fig. 2a. Block diagram of a second-order filter section.

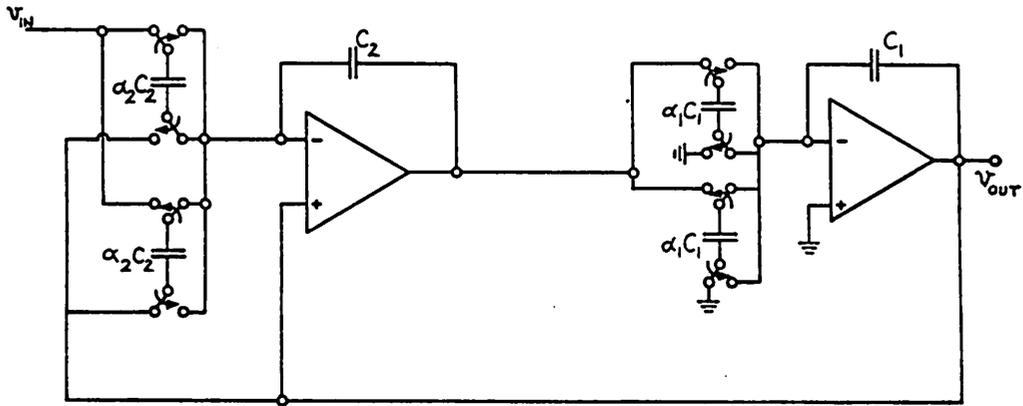


Fig. 2b. Circuit diagram;  $\alpha_1 = b_1 T/2$ ,  $\alpha_2 = b_2 T/2$ .

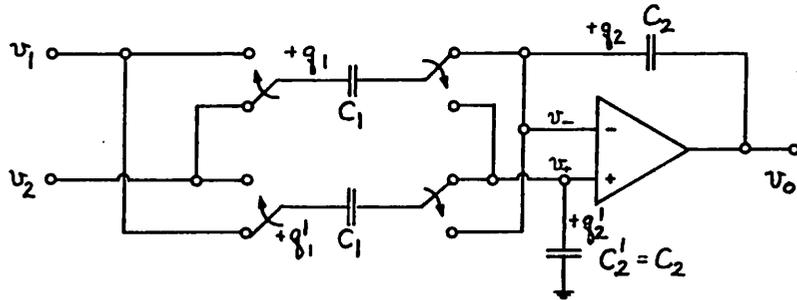


Fig. 3a. Difference integrator.

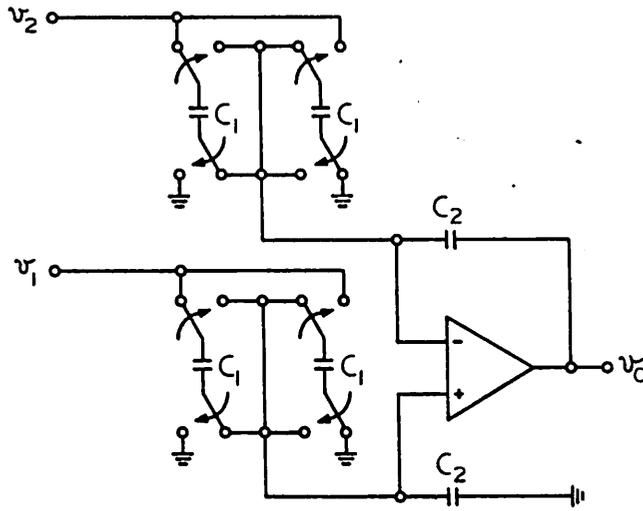


Fig. 3b. Difference integrator.

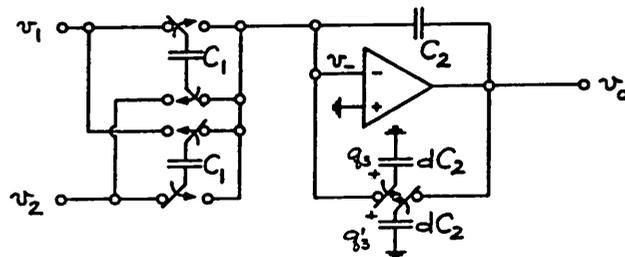


Fig. 4. Lossy sum integrator.

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