HIGH-ORDER CONTINUOUS-TIME MONOLITHIC ANALOG FILTERS

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HIGH-ORDER CONTINUOUS-TIME MONOLITHIC ANALOG FILTERS

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Paul R. Gray
Chairman of Committee

ABSTRACT

The objective of this research is to investigate techniques of realizing high-order, continuous-time, monolithic analog filters. A new approach for realizing monolithic filters is proposed, and a partially integrated prototype has been designed and fabricated using an analog integrated circuit technology.

This approach is based on the recognition that what is really needed is a long time constant monolithic integrator which can be effectively realized in a small silicon area. Precision monolithic integrators have been designed and fabricated using a bipolar compatible ion-implanted JFET process. Each of these monolithic integrators occupies an active area of 850 mil^2 and has a power dissipation of only 4 mW. Several of these integrators have been used in an active-ladder or 'leapfrog' configuration to realize a fifth-order 8 kHz Chebyshev lowpass filter with 0.1 dB passband ripple. A dynamic range of 85 dB has been obtained. Also, no external trimming operations and no anti-aliasing prefilter are required.

ACKNOWLEDGEMENTS

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CHAPTER 1

INTRODUCTION

Frequency selective circuits are widely used in communication and control systems. In many applications, these filters must cut off sharply and must have small passband ripple. These tight specifications can only be met with precision high-order filters. One typical example is the channel bank voice-frequency lowpass filters in telephone communication systems [1].

If monolithic integrated circuit technology is to be used to integrate functional systems, it is important to develop techniques to efficiently implement these filters. One approach for realizing precision high-order filters is to use the digital filtering technique. So far, there has been little success in this approach. The major reasons are as follows. Since the input signal is analog in nature, it has to be first converted into a finite digital word by using an analog-to-digital converter (ADC). Having processed the signal, the digital output has to be converted back to analog form with the use of a digital-to-analog-converter (DAC). With this digital filter system, in order to achieve a dynamic range of 70 dB, ADC and DAC of (approximately) 12 bit accuracy are required. Currently, it is still difficult to realize a fully

integrated digital filter system with ADC and DAC of such accuracy on the same chip, because the required silicon area will be prohibitively large [2].

Sampled-data analog filter systems are attractive because by processing the input analog signal directly (instead of quantizing the signal to a digital word first), the problem associated with realizing high accuracy ADC and DAC has been eliminated. One promising sampled-data approach uses charge transfer devices (CTD) to implement transversal filters [3],[4]. However, these CTD transversal filters generally suffer a large insertion loss (typically 20 dB). In order to obtain filter dynamic ranges in excess of 70 dB, a low noise output amplifier is required [5]. With currently existing integrated MOS operational amplifiers, it is difficult to achieve the required level of noise performance. Another promising technique is the switched capacitor sampled-data filters [6],[7]. It has been shown that this approach can achieve a dynamic range of about 80 dB. However, both the MOS switched capacitor filter technique and the CTD transversal filter approach suffer from the fact that they are sampled-data systems which require continuous-time prefilters to minimize the aliasing effects. In some applications, it is important to have a continuous-time analog filters which have no such drawback.

Conventionally, continuous-time analog filters (in

the audio frequency range) are realized by cascading several low order active-RC filter sections [8],[9]. This approach typically requires a combination of the monolithic technology to realize operational amplifiers, and thin film technology to realize capacitors and resistors. In addition, this technique often requires precision external trimming in order to achieve the desired frequency response. From the standpoint of increasing reliability, reducing physical size and manufacturing costs, it is desirable to develop techniques of integrating the entire precision high-order analog filter, and preferably without any external trimming operations.

Until now, there has been little success in realizing such a continuous-time, monolithic analog filter. One of the reasons is that it is difficult to precisely control the absolute values of monolithic components like capacitors, resistors and current sources. These components may vary with process and temperature. Another reason is that it is difficult to efficiently realize long RC time constants (which are required for low frequency operations) using conventional monolithic techniques.

The objectives of this research is to investigate methods of overcoming the above difficulties, and to study the techniques for realizing high-order, continuous-time, monolithic analog filters.

The results of this work have shown that a high-order, continuous-time, analog filter can be realized. It has a wide dynamic range (greater than 80 dB), and has low power dissipation [10],[11]. Also, it can be implemented in a small silicon area with no external trimming needed. This technique has been demonstrated with the realization of a fifth-order 8kHz Chebyshev lowpass filter with a passband ripple of 0.1 dB using a standard bipolar compatible ion-implanted JFET technology [12],[13]. Excellent agreement between the experimental and designed values has been obtained.

The next chapter describes the two basic high-order filter realization approaches, namely, the cascade and the direct (non-cascade) approaches.

Chapter 3 describes a class of filters which uses integrators as basic elements. The advantages and disadvantages of two high-order filter realization techniques using integrators as building blocks are discussed.

Chapter 4 describes the basic structure of a monolithic integrator which can be efficiently realized in a small silicon area. A technique of stabilizing the bandwidths of the integrators, and thus the bandwidth of the filter, is presented.

In Chapter 5, practical design considerations of monolithic integrators and monolithic high-order analog

filters are discussed in detail.

Chapter 6 describes the performance of a monolithic integrator which has been designed and fabricated in the I.C. Laboratory of the University of California, Berkeley. These integrators have been used to construct a complete fifth-order lowpass filter using the techniques described in Chapter 4. The performance of the filter is evaluated.

Chapter 7 gives the summary and conclusions of this research.

CHAPTER 2

HIGH ORDER FILTER REALIZATION TECHNIQUES

2.1. Introduction

There is a wide variety of high-order filter techniques available to filter designers. These techniques in general can be classified into two main categories, namely, the cascade approach which implements a given transfer function by cascading a number of first-order and second-order sections, and the direct approach which realizes the entire transfer function in one circuit.

In this chapter, we will give a general review of the high-order filter realization techniques. First, we will discuss the realization of low-order filters using active-RC filter techniques. These low-order sections are frequently used in the cascade realization of high-order filters. Next, we will discuss different techniques of implementing high-order filters using the direct approach. We will describe the well known doubly-terminated passive-ladder networks. These networks are very insensitive to component variation in the passband, and in fact has zero sensitivity when the power is matched between the source and the load. Because of this unique property, they have brought about many interesting inductorless active-RC filters such as the simulated inductance, the

frequency-dependent-negative-resistance (FDNR) and the analog-computer-type filters. Finally, we will discuss some of these inductorless active-RC filters. These filters are important because they can be realized using monolithic integrated circuit technology.

2.2. Cascade Approach

The cascade realization of high-order filters are implemented by cascading several first-order and second-order stages. Each of the second-order sections corresponds to the realization of a pair of complex poles, while each of the first-order sections corresponds to the realization of a real pole in the s-plane.

The first-order sections can be realized using simple lead or lag passive networks, and will not be discussed here. The second-order sections are typically designed to have very high input impedance and very low output impedance so as to allow cascade connection without any additional buffer amplifier. Active-RC filters are most suitable for this type of application, and thus are frequently used for realizing second-order filters. We will briefly discuss the second-order active-RC filters according to the number of amplifiers needed in the circuit realization.

2.2.1. Single amplifier Filters

Many circuit configurations have been suggested for realizing second-order section using active-RC techniques [14]-[18]. However, most of the known single amplifier filter realizations can be classified into two major categories [19], namely, negative feedback (NF) and positive feedback (PF) types, as shown schematically in Figure 2.1. In this figure, n_1, n_2 and n_3 are passive RC networks. In general, the type of RC feedback networks determines the transfer function and the sensitivity properties of the resulting active filter.

Figure 2.2 shows a few examples of the single amplifier filters. Circuit (a) is a lowpass while circuit (b) is a bandpass realization of the multiple feedback type [14]. The highpass realization, as shown in circuit (c) is of the pole-zero cancellation type [17] and circuit (d) is the familiar Sallen and Key NF bandpass realization [16]. Circuit (e) is a single amplifier realization of biquad circuit [18] using twin-T structure to implement the RC network n_1. These circuits, (a) to (e), can be classified under the NF configuration. Circuit (f) is a biquad circuit using PF configuration, in which the passive feedback network n_2 is a ladder network. A general comparison of the sensitivities of these circuits can be found in reference [19]. In general, the choice of which single amplifier filter to use is usually determined by the tradeoffs

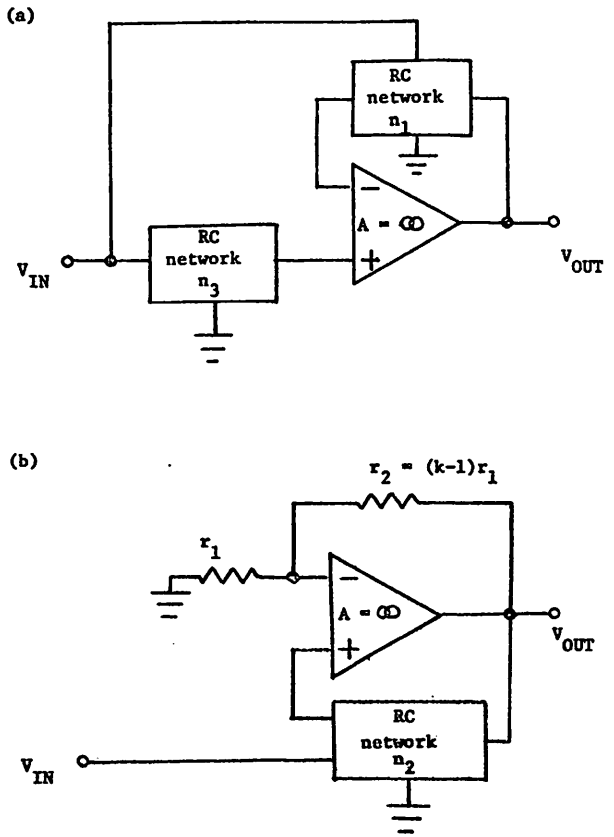

Figure 2.1 (a) A general single-amplifier negative feedback (NF) configuration.

(b) A general single-amplifier positive feedback (PF) configuration.

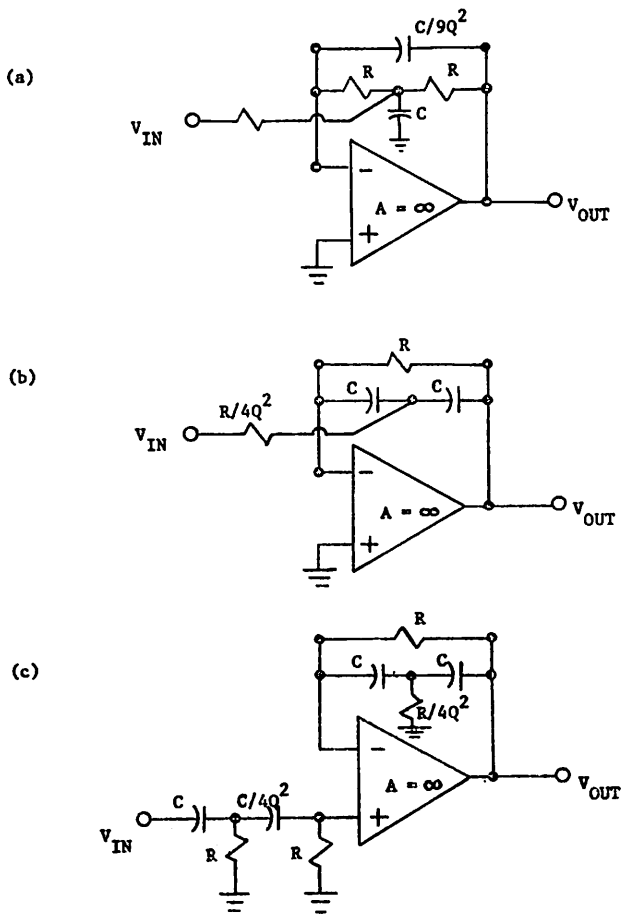

Figure 2.2 Examples of single-amplifier filters:
(a) lowpass filter, (b) bandpass filter,
(c) highpass filter.

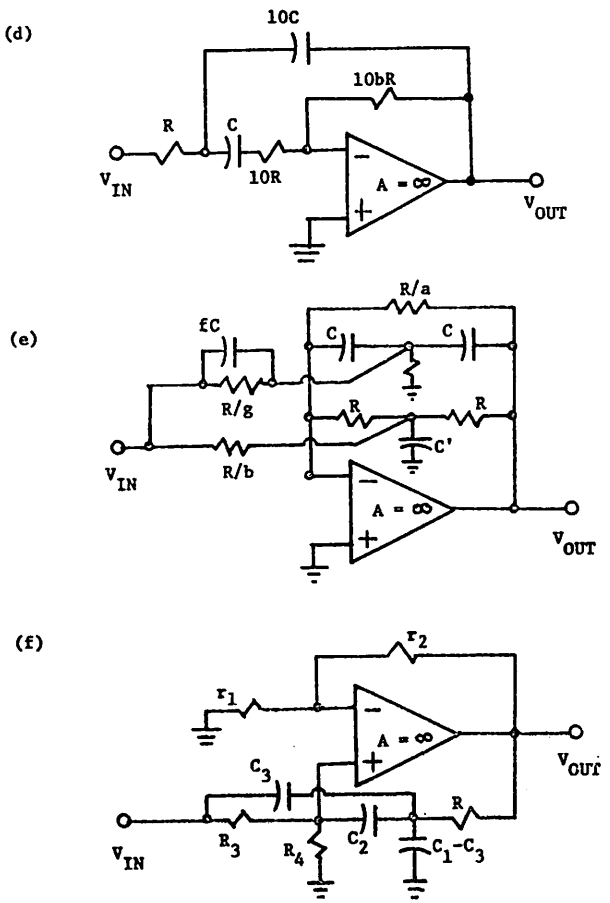

Figure 2.2 (cont'd) (d) Sallen and Key bandpass filter
(e) biquad circuit using NF configuration
(f) biquad circuit using PF configuration

among the sensitivities of ω and Q, the required number of passive elements and the spread in values of the passive elements.

2.2.2. Multiple Amplifier Filters

There are various ways of realizing second-order section using multiple operational amplifiers. A detailed comparison of 15 multiple amplifier filters can be found in reference [20]. In this section, we will discuss one of the most important and frequently used multiple amplifier filters, namely, the second-order state variable circuit.

This state variable filter can be used to realize a general biquadratic transfer function of the form

$$H(s) = \frac{F(s)}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \qquad (2.1)$$

where s is the complex frequency variable, ω_o and Q characterize the pair of complex poles, and F(s) is a polynomial of order ≤ 2 determining the type of filter function.

The circuit shown in Figure 2.3 can be used to realize a biquad transfer function [21]. It requires two integrators and one summer. By taking the outputs at different nodes, one can obtain a highpass, a lowpass and a

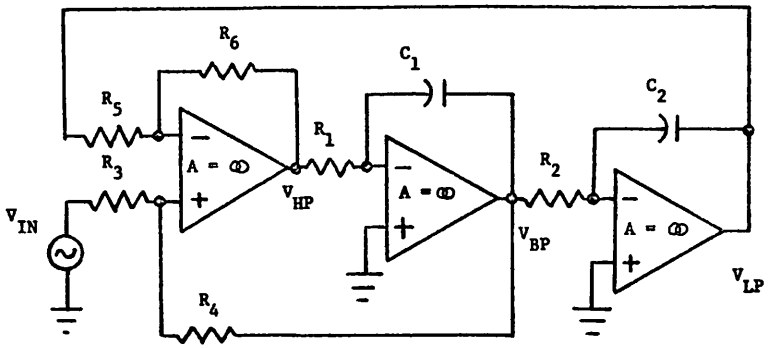

Figure 2.3 A second order state-variable circuit.

bandpass transfer functions. The transfer functions of this circuit are given by the following expressions:

$$\frac{V_{LP}}{V_{in}}(s) = \frac{\frac{1+R_6/R_5}{1+R_3/R_4}\,\frac{1}{R_1R_2C_1C_2}}{s^2+\frac{1+R_6/R_5}{1+R_4/R_3}\,\frac{1}{R_1C_1}\,s+\frac{R_6}{R_5R_1R_2C_1C_2}} \qquad (2.2)$$

$$\frac{V_{HP}}{V_{in}}(s) = \frac{\frac{1+R_6/R_5}{1+R_3/R_4}\,s^2}{s^2+\frac{1+R_6/R_5}{1+R_4/R_3}\,\frac{1}{R_1C_1}\,s+\frac{R_6}{R_5R_1R_2C_1C_2}} \qquad (2.3)$$

$$\frac{V_{BP}}{V_{in}}(s) = \frac{-\frac{1+R_6/R_5}{1+R_3/R_4}\,\frac{s}{R_1C_1}}{s^2+\frac{1+R_6/R_5}{1+R_4/R_3}\,\frac{1}{R_1C_1}\,s+\frac{R_6}{R_5R_1R_2C_1C_2}} \qquad (2.4)$$

Equations (2.2),(2.3),(2.4) correspond to the second-order lowpass, highpass, and bandpass filters respectively. If an additional summer is used, one can obtain an all-pass filter, a bandreject filter, as well as any other second-order filter.

The state variable realization is, in general, less sensitive to element variation than a single amplifier realization. For that reason, it is sometimes used for high Q bandpass applications. Also, this type of filters requires relatively low performance amplifiers. The

spreads of component values can be smaller and the post-adjustment (or tuning) can be done easily. However, the major disadvantage of this type of filters is that it requires three operational amplifiers.

2.3. Direct (non-cascade) Approach

The cascade approach to the realization of high-order transfer functions has the major appeal of simplicity. However, this approach has the disadvantage that typically it requires narrower component tolerances than some direct realizations such as the doubly-terminated passive ladder networks. The difference in the required tolerances can be quite significant in high-order cases, as will be discussed in Chapter 3.

In this section, we will describe the doubly-terminated passive-ladder networks, as well as some inductorless active-RC filters which use the direct approach to implement high-order transfer functions.

2.3.1. Doubly-Terminated RLC Ladder Networks

There are many classes of passive filters which uses the direct implementation approach, the most important of which is the doubly-terminated ladder networks. A ladder network is composed of elements connected alternately in series and in parallel as shown in Figure 2.4.

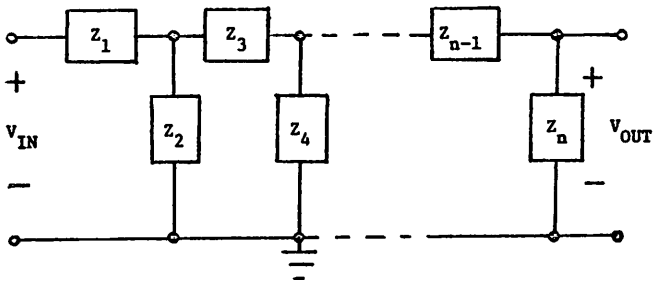

Figure 2.4 A ladder network.

The doubly-terminated passive RLC ladder networks may be used to realize transfer functions with left-half plane poles and imaginary axis zeros. The ladder networks which realize lowpass, highpass, bandpass and bandreject filters are shown in Figures 2.5 and 2.6. Transmission zeros may be implemented by the proper choice of LC impedances in the series and shunt arms of the ladder. For instance, the lowpass filter of Figure 2.5 can be modified to include two pairs of transmission zeros by simply adding two shunt capacitors C_2 and C_4, as shown in Figure 2.7. The design of the doubly-terminated RLC ladder filters has been described extensively in various publications [22].

One unique property of the doubly-terminated RLC ladder network is that it is very insensitive to component variations in the passband. Let us examine the sensitivity of the lowpass filter shown in Figure 2.5. In this network, the values of R_S and R_L are chosen such that maximum power is transferred from the source to the load when all reactive component values are exactly as designed. Under this condition, it is clear that any reactive element value changes, either up or down, can only cause the power transferred to the load to decrease (or V_o to decrease). Thus the quadratic curve of Figure 2.8 is obtained. In fact, as seen in Figure 2.8, in the neighborhood of the exact value of any reactive component, and at every frequency in the passband region where the max-

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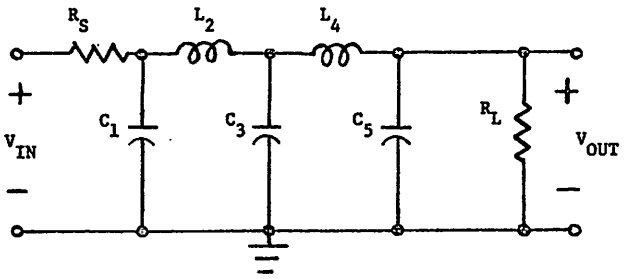

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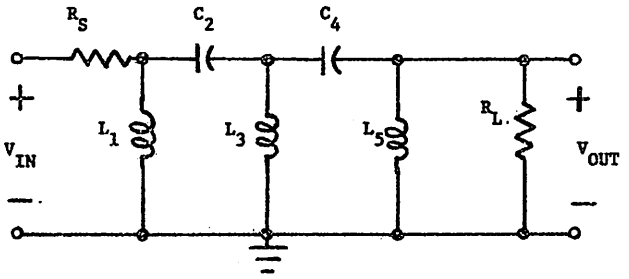
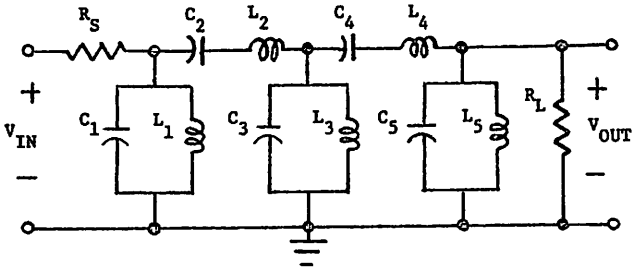


Figure 2.5 (a) A fifth-order lowpass filter

(b) A fifth-order highpass filter.

(a)



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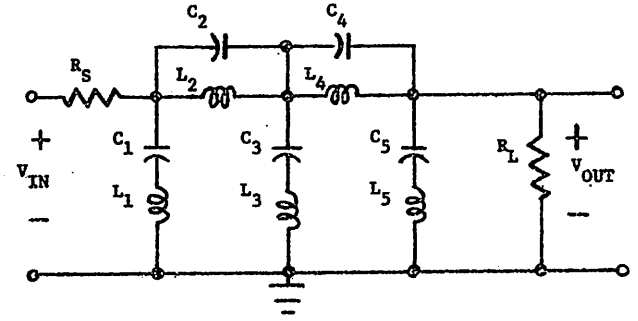

Figure 2.6 (a) A fifth-order bandpass filter

(b) A fifth-order bandreject filter

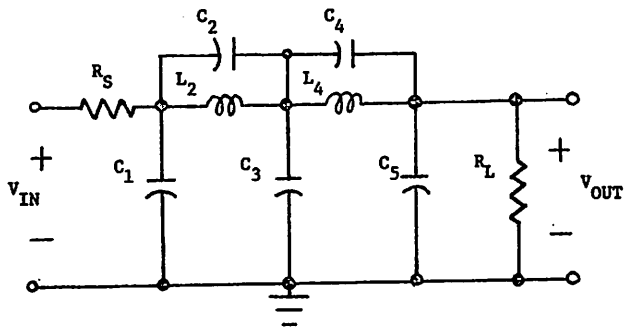

Figure 2.7 A fifth order lowpass filter with two pairs of transmission zeros.

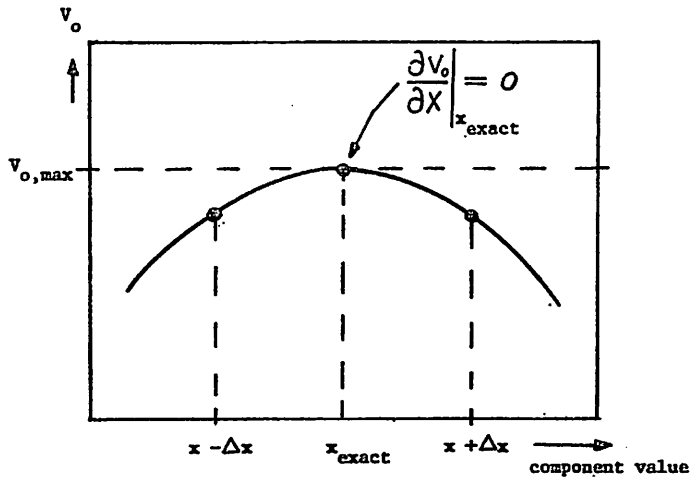

Figure 2.8 A sketch of the sensitivity of a doubly-terminated RLC ladder filter.

imum power transfer condition occurs, this doubly-terminated passive-ladder network has zero sensitivity (i.e. $\left.\frac{\partial V_o}{\partial x}\right|_{x_{exact}} = 0$). This unique property has made these doubly-terminated networks very popular, and has brought about many important inductorless active-RC filters which are derived from this ladder network.

2.3.2. Simulated Inductance Method

One drawback of the doubly-terminated RLC networks is that for low frequency operations, such as in audio applications, inductors of relatively large values are needed. These inductors are bulky and expensive to manufacture. Thus these networks cannot be effectively realized. One way of overcoming this problem is to replace each inductor in the passive doubly-terminated ladder networks by a simulated inductor or Gyrator circuit. In this way, the doubly-terminated ladder networks can be realized without using any inductor while retaining the low sensitivity property of the ladder filters.

One circuit which realizes a grounded inductor is shown in Figure 2.9 [23]. In this circuit, the impedance looking between terminals 1 and ground is given by

$$Z_{in} = sC_1R_1R_2 \qquad (2.5)$$

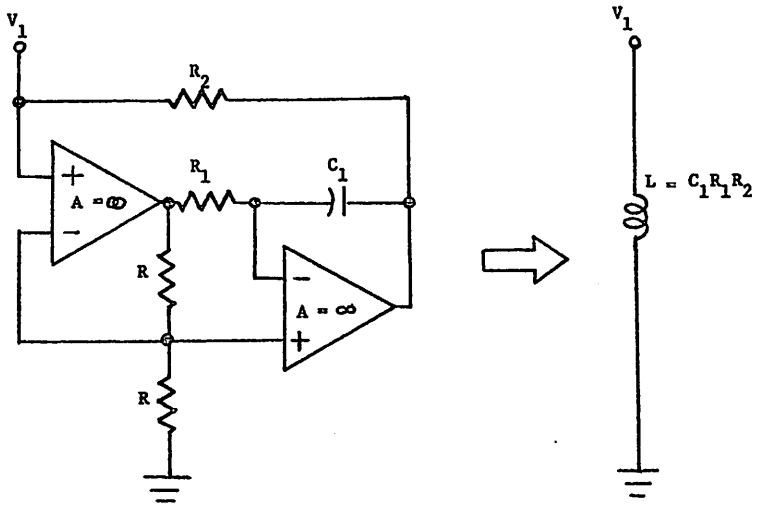

Figure 2.9 Simulated inductance with one terminal grounded.

and thus the simulated inductance, L, is equal to

$$L = C_1 R_1 R_2 \qquad (2.6)$$

This simulated inductance technique, using grounded inductor circuit of Figure 2.9, is very attractive for realizing highpass filters with no floating inductors. For example, in Figure 2.10, the fifth-order doubly-terminated highpass filter with two pairs of transmission zeros contains only two grounded inductors. These grounded inductors can be directly replaced by the circuit shown in Figure 2.9.

Presently, it is still not practical to simulate a floating inductance with good stability, simply because the circuit is quite complex. For this reason, filters which contain floating inductors, such as most of the lowpass and some bandpass filters, cannot be effectively realized using this technique.

However, this problem may be overcome by employing more sophisticated methods, one of which is to use the impedance transformation technique.

2.3.3. Frequency Dependent Negative Resistance (FDNR) Method

The use of impedance scaling is well known in classi-

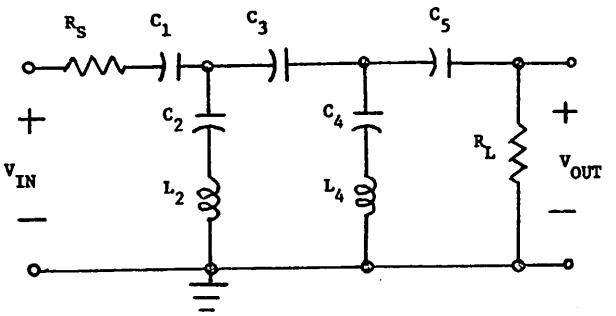

Figure 2.10 A doubly terminated fifth-order highpass ladder filter with two pairs of transmission zeros.

cal circuit theory. Although the scaling factor is usually a positive real constant, it can be taken to be complex or frequency dependent [24]. For example, all components of the passive RLC network can be scaled by a frequency dependent scaling factor, 1/s, as shown in Figure 2.11. In this Figure, it is seen that an inductor of L henries is replaced by a resistor of L ohms, a resistor of R ohms is replaced by a capacitor with 1/R farads, and a capacitor with C farads is replaced by a frequency-dependent-negative-resistance (FDNR, also known as supercapacitor) with an impedance of $1/s^2C$. Thus by having this 1/s impedance scaling, all the inductors have been eliminated. However, we have introduced additional FDNR elements.

One circuit which realizes a grounded FDNR is shown in Figure 2.12. In this circuit, the impedance looking between terminal 1 and ground is given by

$$z_{in} = \frac{1}{(s^2 R_1 C_1 C_2)} \tag{2.7}$$

and hence, the FDNR value, E, is equal to

$$E = R_1 C_1 C_2 \tag{2.8}$$

This FDNR method, using the grounded FDNR circuit of Figure 2.12, is best for realizing lowpass filters with no

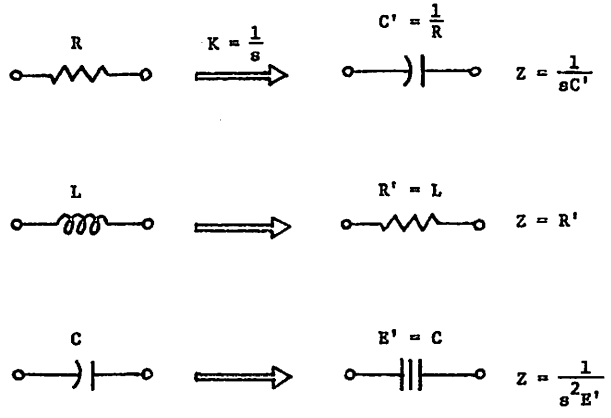

Figure 2.11 The effects of scaling the impedances of RLC components by $\frac{1}{s}$

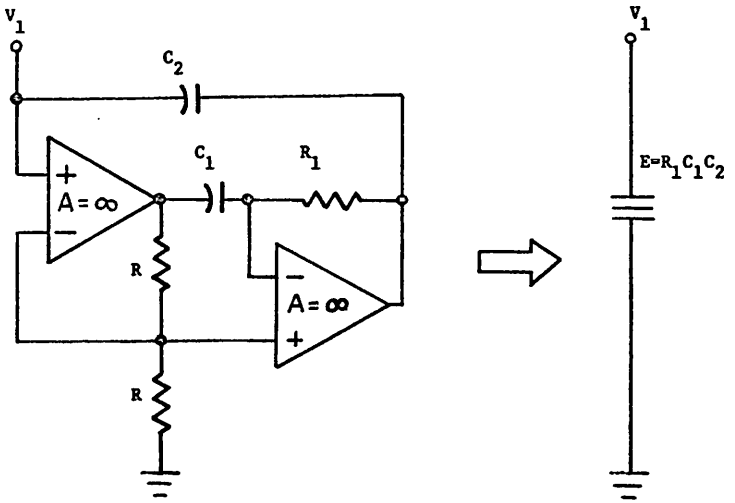

Figure 2.12 Realization of a grounded FDNR.

floating capacitors. As shown in Figure 2.13(a), the fifth-order doubly-terminated lowpass filter with two pairs of transmission zeros requires only two grounded capacitors. By applying the 1/s transformation to this lowpass filter, the resulting circuit is shown in Figure 2.13(b). This circuit consists of two capacitors, five resistors and two FDNR elements. These grounded FDNR elements can be directly replaced by the circuit of Figure 2.12.

Presently, it is still difficult to simulate floating FDNR element with good stability. Because of this, filters which contain floating capacitors such as most of the highpass and some bandpass filters cannot be effectively realized using this technique.

It is interesting to note that while the simulated inductance technique can be efficiently used to realize highpass filters, the FDNR technique can be efficiently used to realize lowpass filters. To realize bandpass or bandreject filters, a combination of these two techniques may be used [25].

2.3.4. Analog-computer-type Filters

Analog computer or state-space principles can be applied to realize filter systems. In this section, we will describe two basic ways of realizing the analog-

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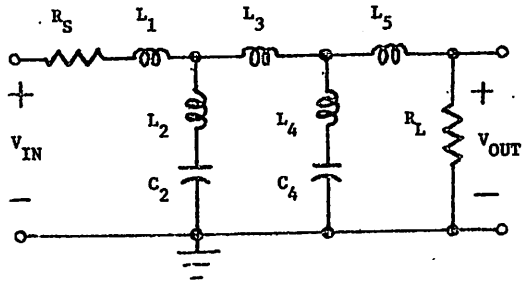

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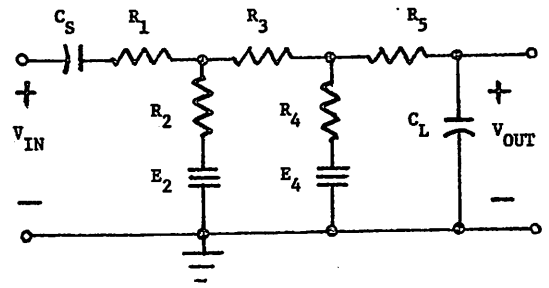


Figure 2.13 (a) A fifth-order minimum-C lowpass filter, and (b) a simulation of the filter by impedance scaling.

computer-type filters.

One way of realizing analog-computer-type filter is to derive it from a given transfer function. We will first consider a general case of deriving an n^{th} order filter from a given transfer function of the form

$$H(s) = \frac{V_2}{V_1} = \frac{a_m s^m + a_{m-1} s^{m-1} + \ldots + a_1 s + a_\emptyset}{s^n + b_{n-1} s^{n-1} + \ldots + b_1 s + b_\emptyset}, \quad a_m \neq \emptyset \quad (2.9)$$

where a_i and b_i are real constants. Equation (2.9) can be represented by a signal flow graph as shown in Figure 2.14. From this signal flow graph, the circuit which implements this transfer function can be realized using integrators and summers, as shown in Figure 2.15. It is interesting to note that the state variable circuit described in section 2.2.2 is actually a limiting case (where n=2) of this realization. In general, this type of realization is not absolutely stable for $n \geq 3$ [25], and hence they are relatively sensitive to parameter variations. Thus this technique may not be suitable for high-order filter realization.

One other way of realizing analog-computer-type filter is to derive it from an existing passive RLC network [25]. As an illustration, the passive ladder network shown in Figure 2.16(a) has been transformed into the analog-computer-type filter (also known as active-ladder

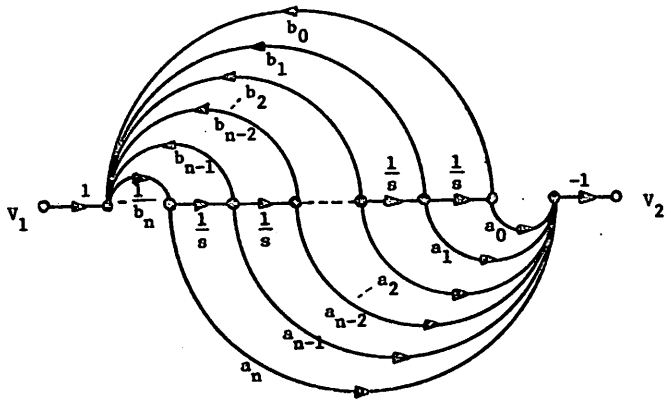


Figure 2.14 A signal flow graph to realize the transfer function.

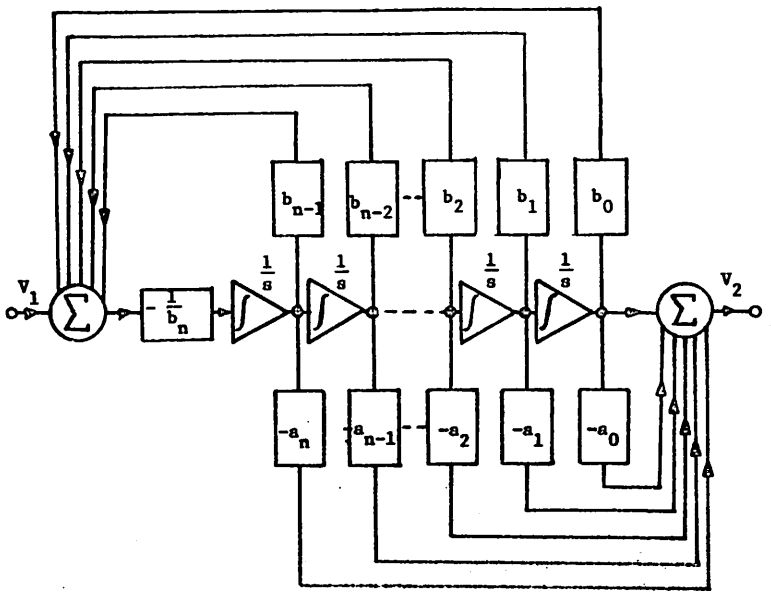
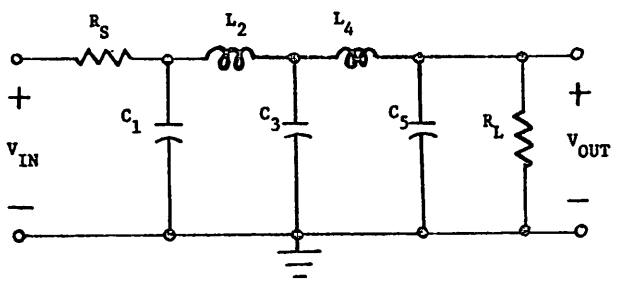


Figure 2.15 Implementation of the signal flow graph using integrators and summers.

(a)



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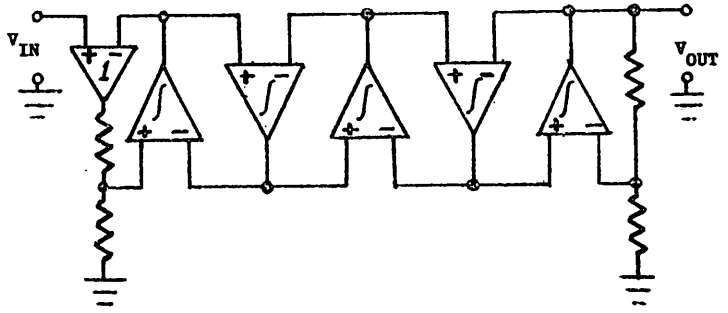


Figure 2.16 (a) A doubly terminated lowpass ladder filter

(b) An analog computer realization of (a)

or 'leapfrog' filters) as shown in Figure 2.16(b). The procedure for this transformation will be discussed in Chapter 3. An important characteristic of this type of transformation is that there is a one-to-one correspondence between the passive element values of the passive network and the gain-constants of the integrators of the active-ladder filter. Because of this one-to-one correspondence, this analog-computer-type filter retains the sensitivity property of the passive prototype. This technique is important because the analog-computer-type filters (realized using integrators and summers) can be readily integrated using integrated circuit technology.

CHAPTER 3

FILTERS UTILIZING INTEGRATORS AS BUILDING BLOCKS

3.1. Introduction

In this chapter, we will discuss a special class of filters which uses integrators as building blocks. This class of filters can be used to realize a variety of filter systems, such as lowpass, highpass, bandpass and bandreject filters. This class of filters is important because precision integrators can be readily realized using Integrated Circuit technology.

First, we will discuss how integrators can be used to realize various types of low-order filter stages. These low-order sections can be used to realize high-order filters using the cascade approach. In particular, we will analyse the sensitivity of a fifth-order lowpass filter which uses this technique. Next, we will derive the analog-computer-type filter from a doubly-terminated passive-ladder network (i.e. direct approach). The sensitivity behavior of this filter is then analysed. Finally, the advantages and disadvantages of these two high-order filter realization approaches are compared.

In this chapter, the design of lowpass filters will be emphasized. Realization of other transfer functions

can be easily implemented using the same principle.

3.2. High-Order Filters by Cascade Approach

The cascade realization of high-order filters can be implemented with several first-order and second-order stages. The first-order and second-order filters, which use integrators as basic elements, will be described.

3.2.1. First-Order Filters

The first-order passive lowpass filter is shown in Figure 3.1(a). By inspection, the transfer function of this circuit is given by

$$H(s) = \frac{V_o}{V_{in}} = \frac{1}{sRC + 1} \tag{3.1}$$

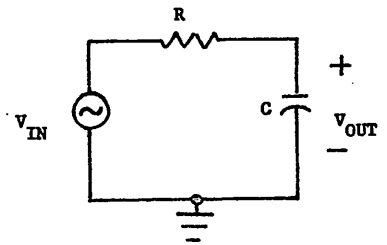
and the time constant of this circuit is RC.

This passive filter can be equivalently realized using an integrator shown in Figure 3.1(b). The transfer function of this circuit is given by

$$H(s) = \frac{V_o}{V_{in}} = \frac{1}{\frac{s}{\omega_o} + 1} \tag{3.2}$$

where ω_o is the gain-constant of the integrator. Comparing equations (3.1) with (3.2), it is noticed that the

(a)



(b)

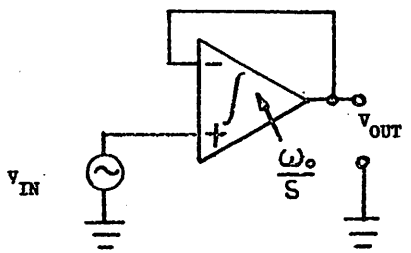


Figure 3.1 (a) A first-order lowpass filter.

(b) A first-order lowpass filter realized with an integrator.

first-order passive network can be realized with an integrator (where $w_o = 1/RC$). However, to realize a first-order highpass filter, additional summing amplifier is needed.

3.2.2. Second-Order Filters

One possible realization of a second-order filter is shown in Figure 3.2. This circuit requires only two resistors and two differential input integrators. Despite its simplicity, three different transfer functions are available. These transfer functions can be easily derived and are shown below:

$$\frac{V_{BR}}{V_{in}} = \frac{R_8}{R_7+R_8} \quad \frac{w_1w_2 + s^2}{s^2 + \frac{w_1R_7}{R_7+R_8}s + w_1w_2} \tag{3.3}$$

$$\frac{V_{BP}}{V_{in}} = \frac{-R_8}{R_7+R_8} \quad \frac{sw_1}{s^2 + \frac{w_1R_7}{R_7+R_8}s + w_1w_2} \tag{3.4}$$

$$\frac{V_{LP}}{V_{in}} = \frac{R_8}{R_7+R_8} \quad \frac{w_1w_2}{s^2 + \frac{w_1R_7}{R_7+R_8}s + w_1w_2} \tag{3.5}$$

Examining these expressions carefully, we notice that equations (3.3), (3.4), (3.5) correspond to the second-

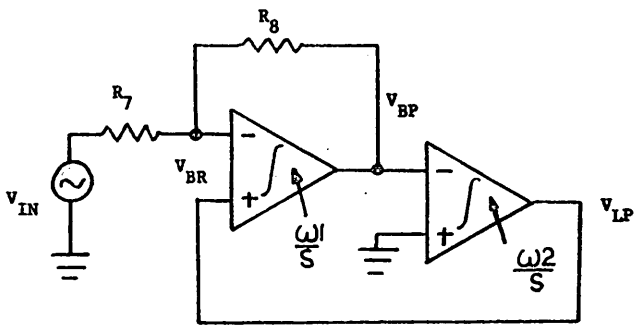


Figure 3.2 A second-order filter realized with two integrators.

order bandreject, bandpass and lowpass transfer functions, respectively. Highpass transfer function can be obtained by taking the difference between V_{BR} and V_{LP}. For these transfer functions, it is interesting to note that

$$\omega_o = \sqrt{\omega_1 \omega_2} \tag{3.6}$$

$$Q = \left(1+\frac{R_8}{R_7}\right)\sqrt{\frac{\omega_2}{\omega_1}} \tag{3.7}$$

where ω_o corresponds to the resonance frequency, and Q corresponds to the quality factor of the second-order filter.

Notice that if we assume $\omega_1 = \omega_2 = \omega$, then $\omega_o = \omega$ and $Q = (1 + R_8/R_7)$. Hence ω_o and Q are independent of each other, and thus can be independently tuned if necessary.

To determine the usefulness of this second-order filter, the sensitivity of the network parameters due to element value changes are derived as follows:

$$S^{\omega_o}_{\omega_1} = S^{\omega_o}_{\omega_2} = \frac{1}{2} \tag{3.8}$$

$$S^{Q}_{\omega_1} = -\frac{1}{2} \tag{3.9}$$

$$S^{Q}_{\omega_2} = \frac{1}{2} \tag{3.10}$$

$$S^{Q}_{\frac{R8}{R7}} = \frac{R_8}{R_7+R_8} \qquad (3.11)$$

Equations (3.8) to (3.11) indicate that this second-order filter has relatively low sensitivities, and thus may be used to realize high Q filters. This is not surprising as this filter is a second degree state-variable filter which is known to have low sensitivity.

3.2.3. Sensitivity of the Cascade Approach

The first-order and second-order filters described can be cascaded together to realize high-order filters. In this cascade approach, each of the second-order sections corresponds to the realization of a pair of complex poles, while each of the first-order sections corresponds to the realization of a real pole in the s-plane.

As an illustration, the procedure for implementing a fifth-order lowpass filter will be described. The normalized ($\omega = 1$) transfer function of a fifth-order Chebyshev lowpass filter with passband ripple of 0.1 dB is shown as follows:

$$H(s) = \frac{V_o}{V_{in}}(s) = \frac{H_o}{s^5+1.744s^4+2.7707s^3+2.397s^2+1.4356s+0.4095} \qquad (3.12)$$

where H_o is just a scaling factor. A plot of the magnitude response of this filter as a function of frequency is shown in Figure 3.3.

To implement this filter by the cascade approach, we need to factorize equation (3.12) into the products of first-order and second-order functions. The resulting equation is shown below:

$$H(s) = \frac{H_o}{(s^2+0.333s+1.195)(s^2+0.872s+0.636)(s+0.539)} \qquad (3.13)$$

Thus the fifth-order lowpass transfer function can be realized by cascading two second-order sections and one first-order stage. The transfer function of the first-order stage is given by

$$H_0(s) = \frac{K_0}{s+0.539} \qquad (3.14)$$

$$\text{i.e.} \quad \omega_0 = 0.539 \qquad (3.15)$$

$$Q_0 = 0.5 \qquad (3.16)$$

The transfer functions of the second-order sections are given by

$$H_1(s) = \frac{K_1}{s^2+0.872s+0.636} \qquad (3.17)$$

$$\text{i.e.} \quad \omega_1 = 0.7974 \qquad (3.18)$$

$$Q_1 = 0.9145 \qquad (3.19)$$

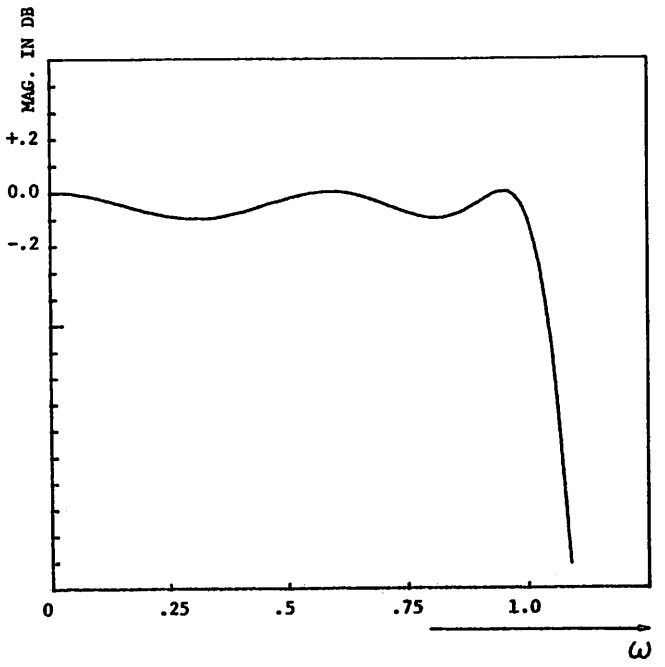


Figure 3.3 A fifth-order Chebyshev lowpass filter with 0.1 dB passband ripple.

and

$$H_2(s) = \frac{K_2}{s^2+0.333s+1.195} \tag{3.20}$$

i.e. $$\omega_2 = 1.093 \tag{3.21}$$

$$Q_2 = 3.282 \tag{3.22}$$

By cascading these sections together, the given transfer function, as described by equation (3.12), can be realized. The block diagram of this cascade realization is shown in Figure 3.4. A complete circuit diagram for realizing such a fifth-order lowpass filter using the first-order and second-order sections described earlier in this chapter, is shown in Figure 3.5.

To illustrate the usefulness of this cascade approach, the sensitivity of the circuit of Figure 3.5 is analysed in the following way. Each of the parameters of the filter is independently varied by $\pm 2\%$, and the deviation in magnitude response is then plotted across the frequency band of interest, as shown in Figure 3.6 and 3.7. From these simulated results, it is noticed that the high Q second-order section is most sensitive to parameter variations. The most sensitive parameter is ω_c. With a $\pm 2\%$ variation in ω_c, the passband of the response is changed by almost 0.5 dB.

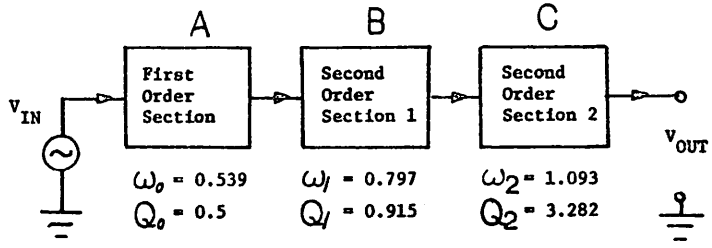


Figure 3.4 A block diagram of the cascade realization of the fifth-order lowpass filter.

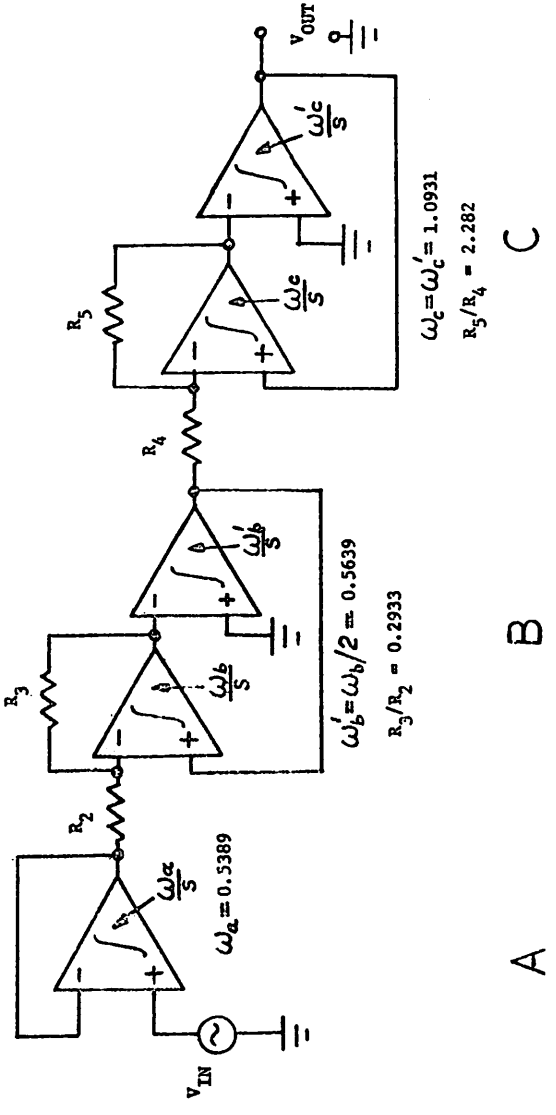


Figure 3.5 A circuit implementation of the fifth-order lowpass filter by cascade method.

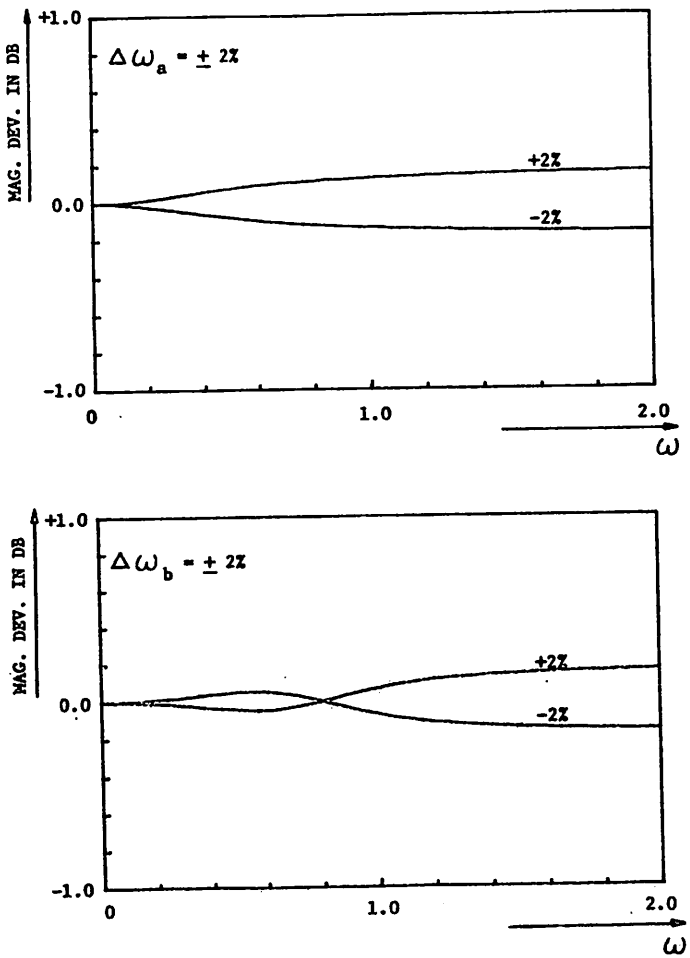


Figure 3.6 Simulated deviations for the fifth-order filter due to variations in the gain-constants of the integrators (cascade approach).

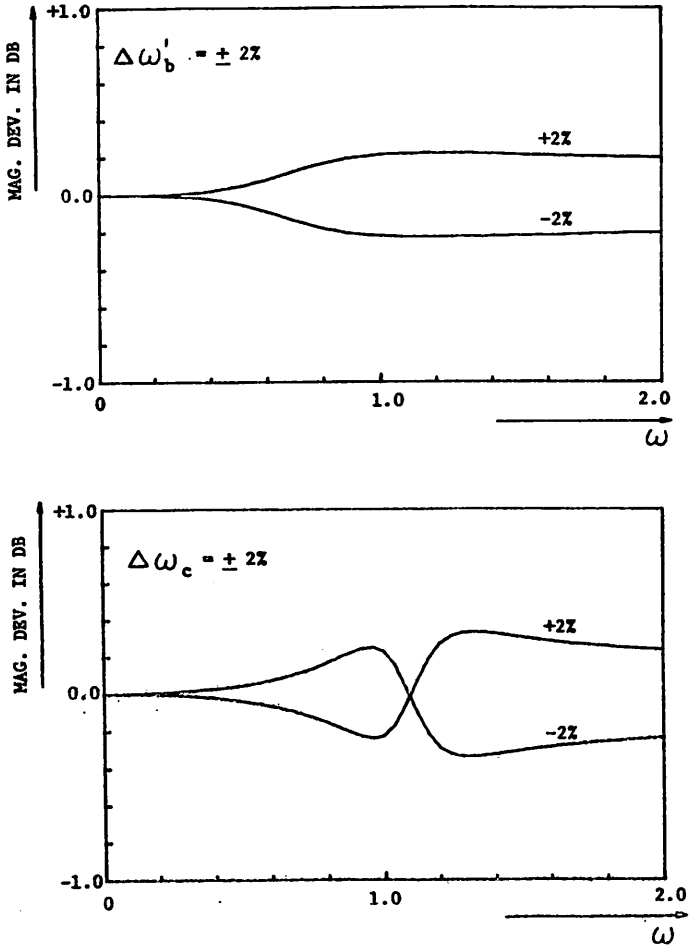


Figure 3.6 (cont'd) Simulated deviations for the fifth-order filter due to variations in the gain-constants of the integrators (cascade approach).

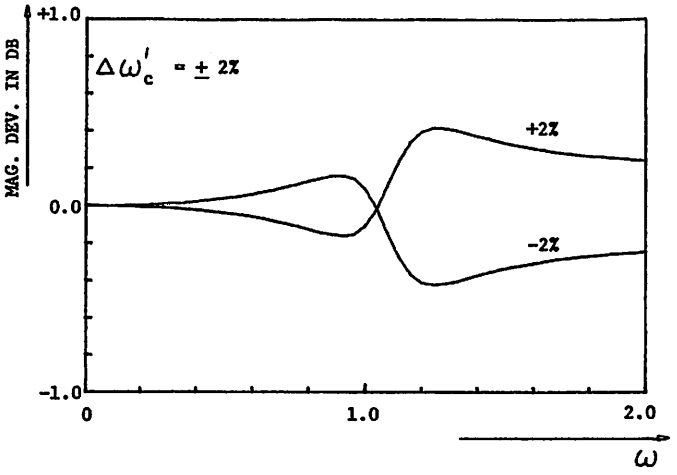
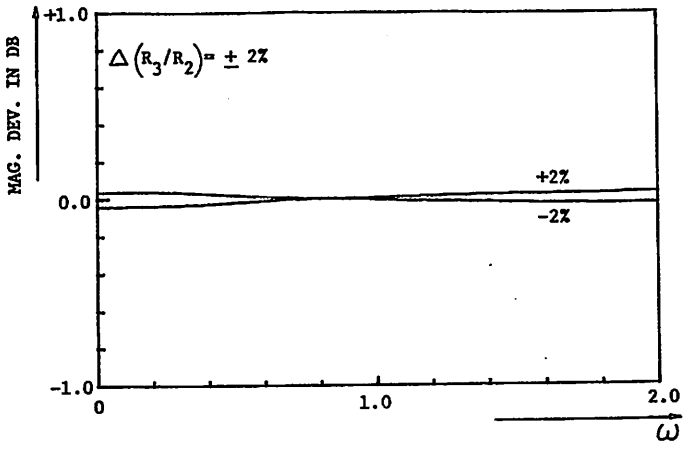


Figure 3.6 (cont'd) Simulated deviations for the fifth-order filter due to variations in the gain-constants of the integrators (cascade approach).



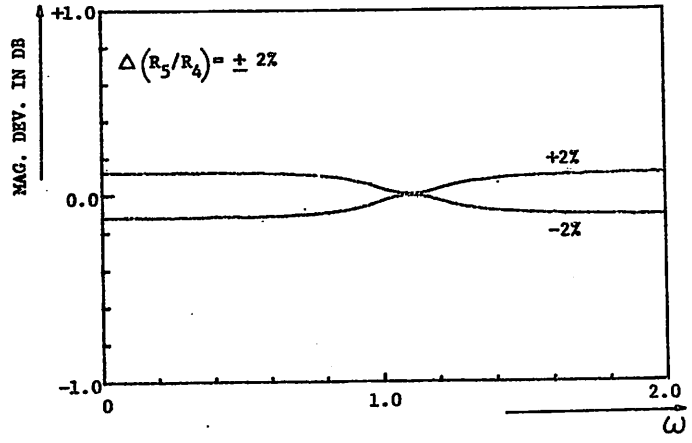


Figure 3.7 Simulated deviations for the fifth-order filter due to variations in the resistor ratios (cascade approach).

3.2.4. Inclusion of Transmission Zeros

The addition of transmission zeros to a filter response has great importance in many filter applications. Typically transmission zeros are included so as to achieve a faster transition between the passband and the stopband of the response without resorting to a filter of higher order.

Transmission zeros can be incorporated in the design of high-order filters using the cascade approach. In this section, the basic technique which can be used to implement transmission zeros will be described.

The fourth-order lowpass filter shown in figure 3.8 will be used to illustrate this approach. As seen in this circuit, the fourth-order filter is realized by cascading two second-order sections. The transfer function of this filter is given by the following expression:

$$H(s) = \frac{V_o}{V_{in}}(s)$$

$$= H_\emptyset \frac{\omega_1\omega_2\omega_3\omega_4}{\left(s^2+\frac{R_1\omega_1 s}{R_1+R_2}+\omega_1\omega_2\right)\left(s^2+\frac{R_3\omega_3 s}{R_3+R_4}+\omega_3\omega_4\right)} \qquad (3.23)$$

where $H_\emptyset = \left[\frac{R_2}{R_1+R_2}\right]\left[\frac{R_4}{R_3+R_4}\right]$.

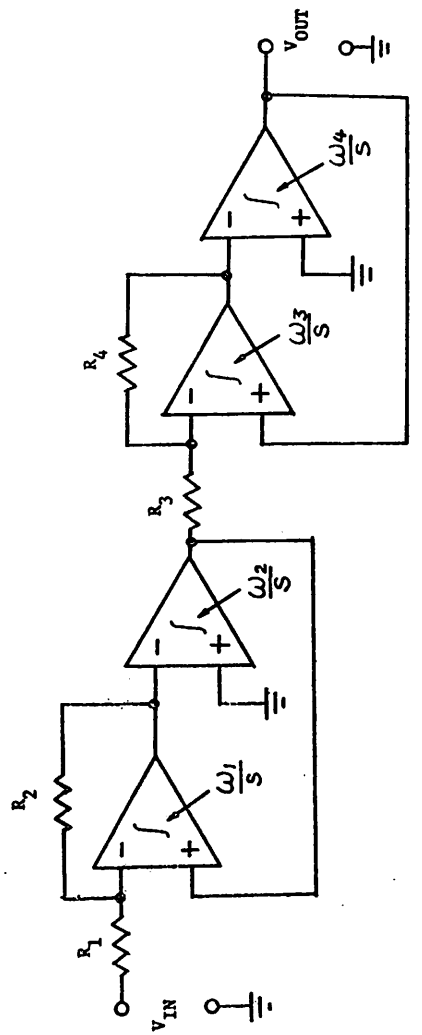


Figure 3.8 A fourth-order lowpass filter.

Transmission zeros can be realized by summing the lowpass and bandreject outputs in a certain proportion. For instance, this summing method can be implemented with an additional buffer amplifier and one resistor, as shown in Figure 3.9. The transfer function of this circuit is then given by

$$H(s) = \frac{V_o}{V_{in}}(s)$$

$$= H_\emptyset \frac{R_{3a}}{R_{3b}} \frac{\omega_1\omega_2\omega_3\omega_4 \left[(1+R_{3b}/R_{3a})\omega_1\omega_2+s^2 \right]}{\left(s^2+\frac{R_1\omega_1 s}{R_1+R_2}+\omega_1\omega_2\right)\left(s^2+\frac{R_3\omega_3 s}{R_3+R_4}+\omega_3\omega_4\right)} \qquad (3.24)$$

where $R_3 = \frac{R_{3a}R_{3b}}{R_{3a}+R_{3b}}$, $H_\emptyset = \left[\frac{R_2}{R_1+R_2}\right]\left[\frac{R_4}{R_3+R_4}\right]$, and the transmission zeros are located at

$$s_{1,2} = \pm j\sqrt{(1+R_{3a}/R_{3b})\omega_1\omega_2} \qquad (3.25)$$

Thus with simple modification, transmission zeros can be implemented in the cascade approach.

3.3. High-Order Filters by Direct Approach

It is well known that the passive doubly-terminated ladder network achieves the lowest sensitivity under the maximum power transfer condition. This passive-ladder network can be transformed into the analog-computer-type

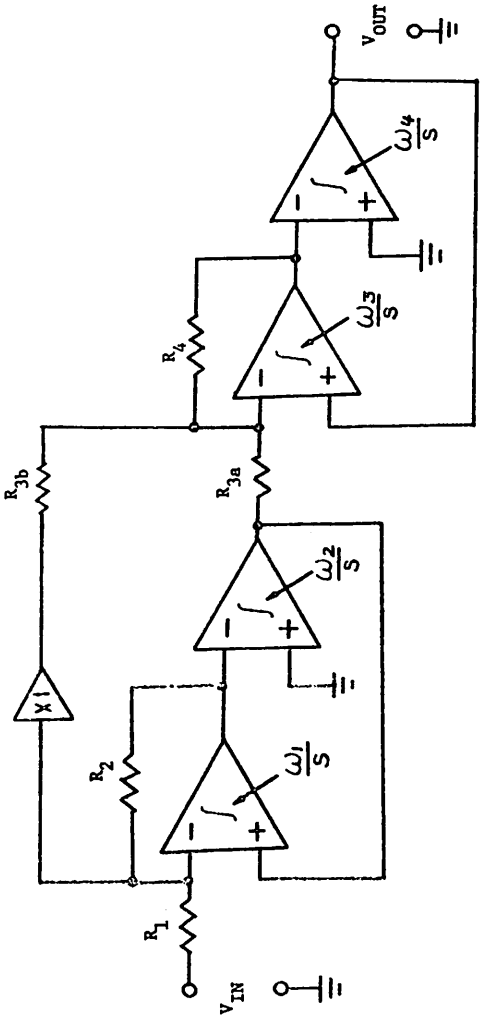


Figure 3.9 A fourth-order lowpass filter with a pair of transmission zeros.

filters. In this section, a detailed description of this transformation will be presented [25].

3.3.1. Passive-Ladder to Active-Ladder Transformation

A passive doubly-terminated fifth-order lowpass ladder network which is used as a prototype for the passive to active-ladder transformation is shown in Figure 3.10. In this figure, the voltage and current of each passive element are labelled. A complete set of Kirchoff's loop and node equations is shown below:

$$V_{\emptyset} = V_{in} - V_1 \tag{3.26a}$$

$$I_{\emptyset} = \frac{V_{\emptyset}}{R_S} \tag{3.26b}$$

$$I_1 = I_{\emptyset} - I_2 \tag{3.26c}$$

$$V_1 = \frac{I_1}{sC_1} \tag{3.26d}$$

$$V_2 = V_1 - V_3 \tag{3.26e}$$

$$I_2 = \frac{V_2}{sL_2} \tag{3.26f}$$

$$I_3 = I_2 - I_4 \tag{3.26g}$$

$$V_3 = \frac{I_3}{sC_3} \tag{3.26h}$$

$$V_4 = V_3 - V_5 \tag{3.26i}$$

$$I_4 = \frac{V_4}{sL_4} \tag{3.26j}$$

$$I_5 = I_4 - I_6 \tag{3.26k}$$

$$V_5 = \frac{I_5}{sC_5} \tag{3.26l}$$

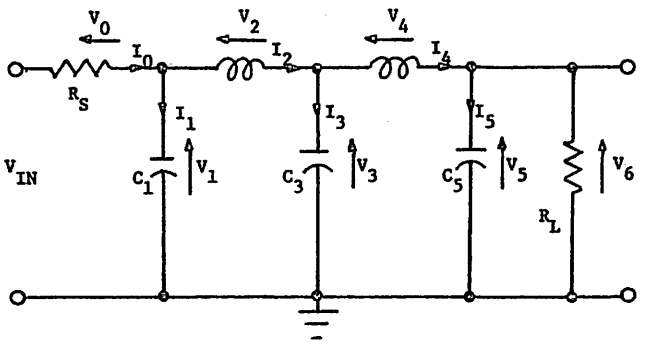


Figure 3.10 Doubly terminated RLC fifth-order all-pole ladder filter.

$$V_6 = I_6 R_L \tag{3.26m}$$

$$V_o = V_6 \tag{3.26n}$$

The signal flow graph is then constructed by drawing the nodes representing the branch voltages and currents in a regular array, as shown in Figure 3.11(a). In this figure, each voltage or current node is defined by the signal paths flowing into it. The branch gain of the signal path is labelled next to each arrow. Multiple inputs into a single node are considered as summation.

Since the final circuit will be implemented using integrator, it is necessary to transform the current nodes to voltage nodes. This is done by multiplying all current nodes by a scaling resistance, R, so that the current nodes, I_i, are now represented as the voltages, $V_i' = I_i R$ as shown in Figure 3.11(b). Also, to maintain the proper relationships between the voltage and current nodes, the branch gains are also scaled by R. Thus they become dimensionless voltage transfer functions.

From the signal flow graph representation of the passive-ladder network, the circuit of Figure 3.12 is obtained. It consists of two voltage dividers with

$$\frac{R}{R_S} = \frac{r_{S2}}{r_{S2} + r_{S1}} \tag{3.27}$$

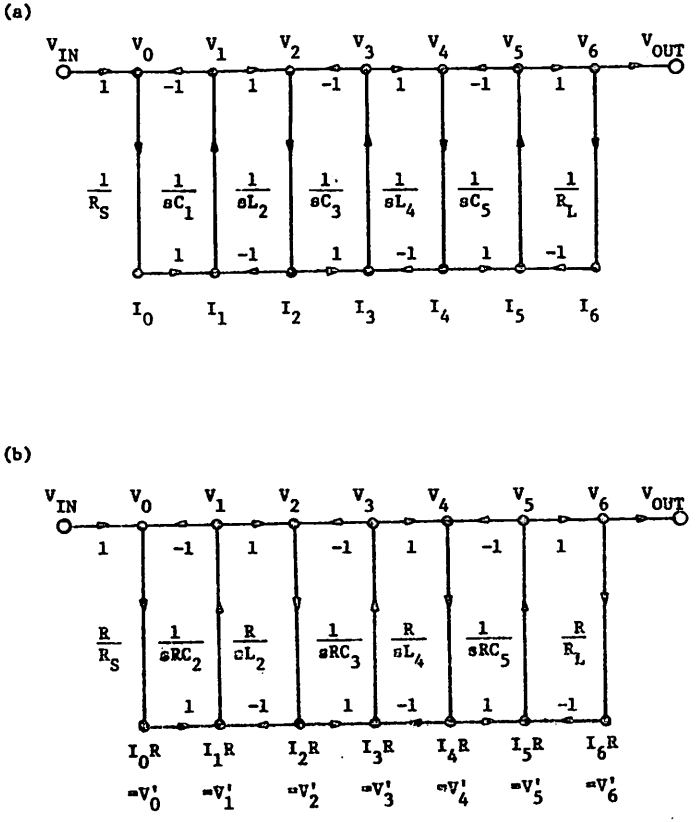
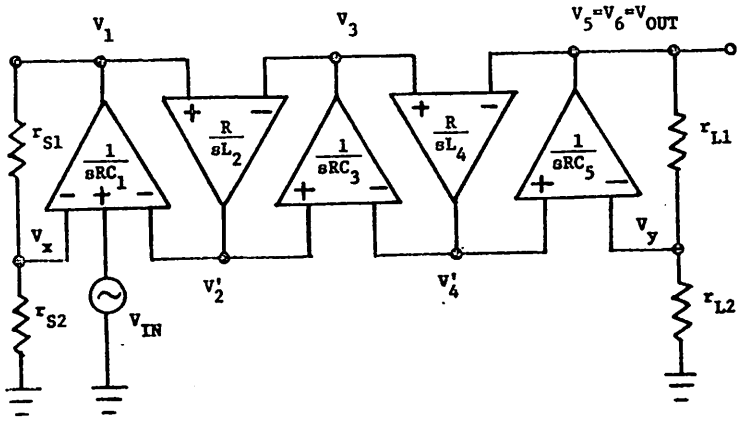


Figure 3.11 Flow diagram for the fifth-order all-pole lowpass ladder filter.



$$V_x = \frac{r_{S2}}{r_{S2} + r_{S1}}$$

$$V_y = \frac{r_{L2}}{r_{L2} + r_{L1}}$$

Figure 3.12 Active ladder circuit derived from the flow diagram of figure 3.11.

and

$$\frac{R}{R_L} = \frac{r_{L_2}}{r_{L_2} + r_{L1}} \qquad (3.28)$$

and five multiple input integrators with time constants

$$t_n = RC_n \qquad \text{for } n=1,3,5 \qquad (3.29)$$

and

$$t_m = \frac{L_m}{R} \qquad \text{for } m=2,4 \qquad (3.30)$$

This circuit can be further simplified by choosing proper values of R_S, R_L and R. Typically for a passive ladder filter, the value of R_S is chosen to be equal to R_L. Thus if we assume that $R_S = R_L = R$, then the circuit of Figure 3.12 can be simplified to the form shown in Figure 3.13. In this figure, the matching between the source and load is simulated by having unity feedback to the inputs of the first and last integrators.

As a result of this transformation, the transfer functions of the active-ladder and passive-ladder filters are identical. More importantly, there is a one-to-one correspondence between the reactive element values and the gain-constants of the integrators. Because of the one-to-one correspondence, this active-ladder network retains the sensitivity properties of the passive prototype.

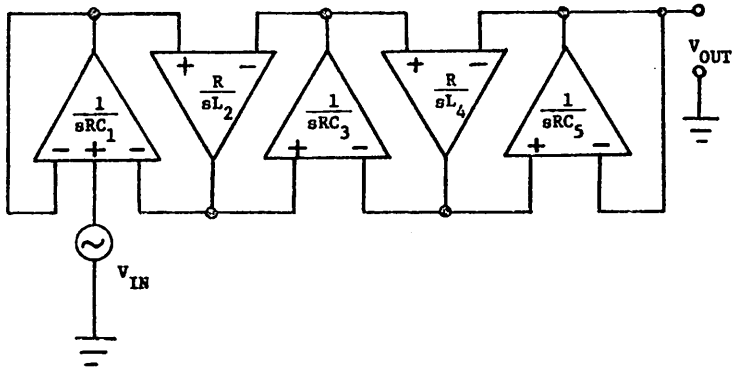


Figure 3.13 A simplified version of the active ladder circuit.

3.3.2. Sensitivity of the Direct Approach

To illustrate the sensitivity of the active-ladder network, the fifth-order lowpass filter of Figure 3.13 is designed to have a normalized cutoff frequency of $\omega = 1$ rad/sec, and a passband ripple of 0.1 dB. This filter is then simulated for $\pm$ 2% variations on all the gain-constants of the integrators, as shown in Figure 3.14. As seen from this figure, the most sensitive parameter is due to the gain-constant of the third integrator. In this case, the maximum deviation in the passband due to $\pm$ 2% change in the gain-constant of the third integrator is only 0.044 dB. This extremely low sensitivity of the active-ladder network is a key factor in the implementation of monolithic high-order filters.

3.3.3. Inclusion of Transmission Zeros in Active-Ladder Filters

For passive-ladder networks, transmission zeros are easily included by adding shunt elements to the network as shown in Figure 3.15(a). In this figure, by adding a shunting capacitor C_2 across L_2, a pair of transmission zeros is obtained (i.e. a pair of complex zeros on the $j\omega$ axis). The magnitude of the transmission zeros is given by the resonant frequency of the series arm, that is

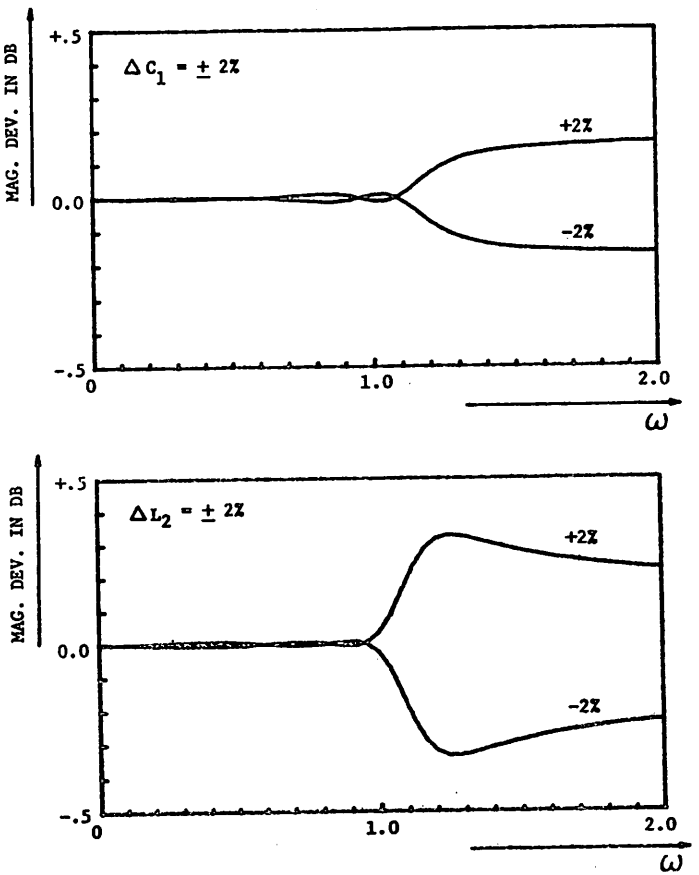


Figure 3.14 Simulated deviations for the fifth-order filter due to variations in the gain-constants of the integrators (direct approach).

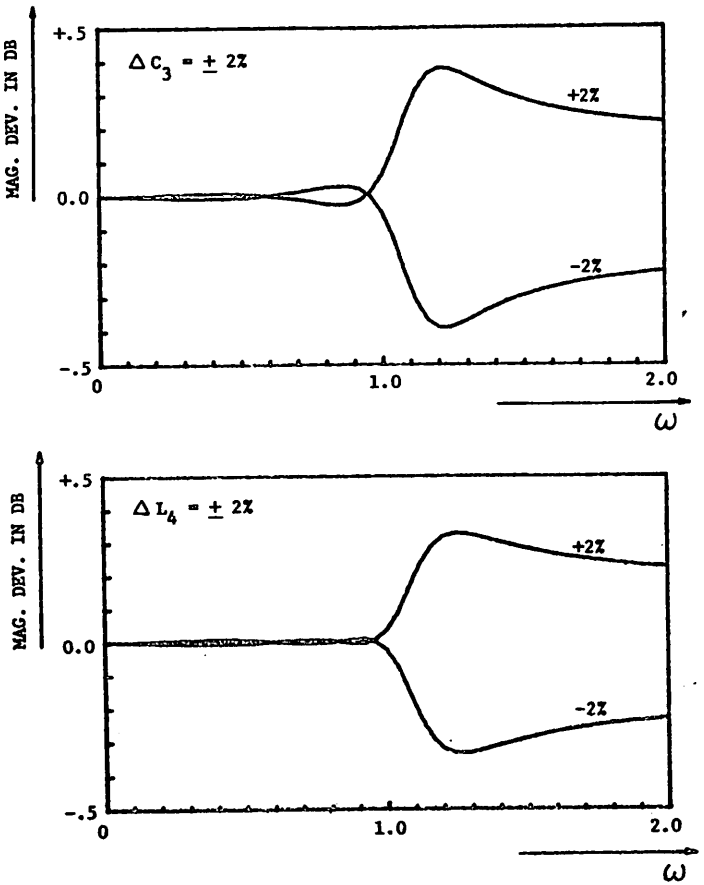


Figure 3.14(cont'd) Simulated deviations for the fifth-order filter due to variations in the gain-constants of the integrators (direct approach).

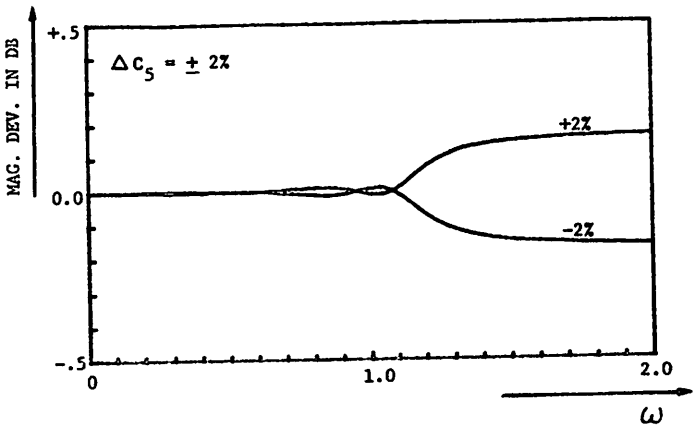
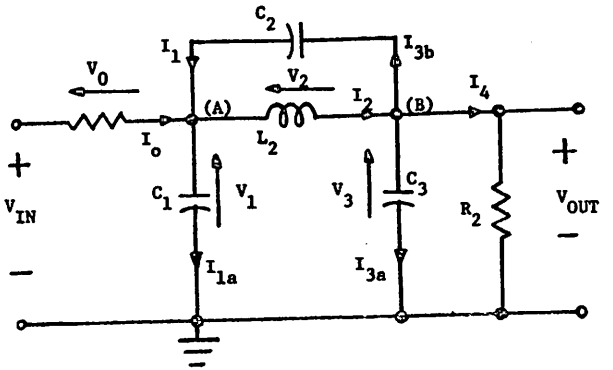


Figure 3.14(cont'd) Simulated deviations for the fifth-order filter due to variations in the gain-constants of the integrators (direct approach).

(a)



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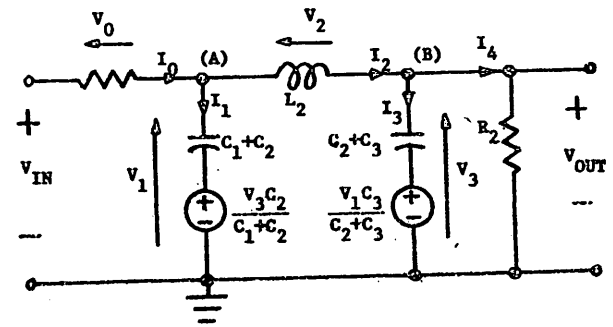


Figure 3.15 (a) An RLC third-order elliptic lowpass filter, and

(b) an equivalent form.

$$\omega_{zero} = (C_2 L_2)^{-1/2} \qquad (3.31)$$

One of the reasons that passive-ladder networks were very popular was because of the relatively simple way of incorporating transmission zeros. However to incorporate transmission zeros into the active-ladder circuit is not obvious. As will be described later on, transmission zeros can be incorporated into the active-ladder circuit with no additional integrator, only two additional capacitors are needed for each pair of transmission zeros.

Referring back to the circuit of Figure 3.15(a). Intuitively, it is clear that C_2 feeds a portion of V_1 forward to node B, and a portion of V_3 is also fed back to node A. Analytically, we will show that this circuit can be put in an equivalent form shown in Figure 3.15(b) [26].

By applying Kirchoff's current law at nodes A and B of Figure 3.15(a), the following equations are obtained.

Node A: $$I_\emptyset - I_2 - C_1 V_1 s - C_2 (V_1 - V_3) s = \emptyset \qquad (3.32)$$

$$V_1 = \frac{I_\emptyset - I_2}{s(C_1+C_2)} + V_3 \left(\frac{C_2}{C_1+C_2}\right) \qquad (3.33)$$

Node B: $$I_2 - I_4 - C_3 V_3 s - C_2 (V_3 - V_1) s = \emptyset \qquad (3.34)$$

$$V_3 = \frac{I_2 - I_4}{s(C_2+C_3)} + V_1 \left(\frac{C_2}{C_2+C_3}\right) \qquad (3.35)$$

Using these relationships, the equivalent form as shown in Figure 3.15(b) is thus obtained. From equations (3.33) and (3.35), we notice that the realization of V_1 and V_3 requires a circuit which simultaneously performs the operations of integration and summation.

Interestingly, this building block can be realized by adding one capacitor to the basic monolithic integrator circuit (cf. Chapter 4), as shown in Figure 3.16(a). In this figure, the addition of C_a introduces an ac current of $\Delta I = sC_a V_x$ into transistor Q_3. This current is then reflected as a change in the collector current of Q_4 because of the mirror circuit. This in turn draws a current of ΔI from the integrating capacitor C_c. The output voltage is thus changed by an amount equals to $\frac{C_a}{C_c} V_x$. The overall output voltage of this integrator/summer circuit is thus given by

$$V_o = \frac{G_m}{sC_c} V_{in} + \frac{C_a}{C_c} V_x \qquad (3.36)$$

where G_m is the transconductance of the input stage. For convenience, this integrator/summer circuit is represented in a schematic form as shown in Figure 3.16(b). This integrator/summer circuit can be used to implement transmission zeros.

As an illustration, the third-order elliptic lowpass

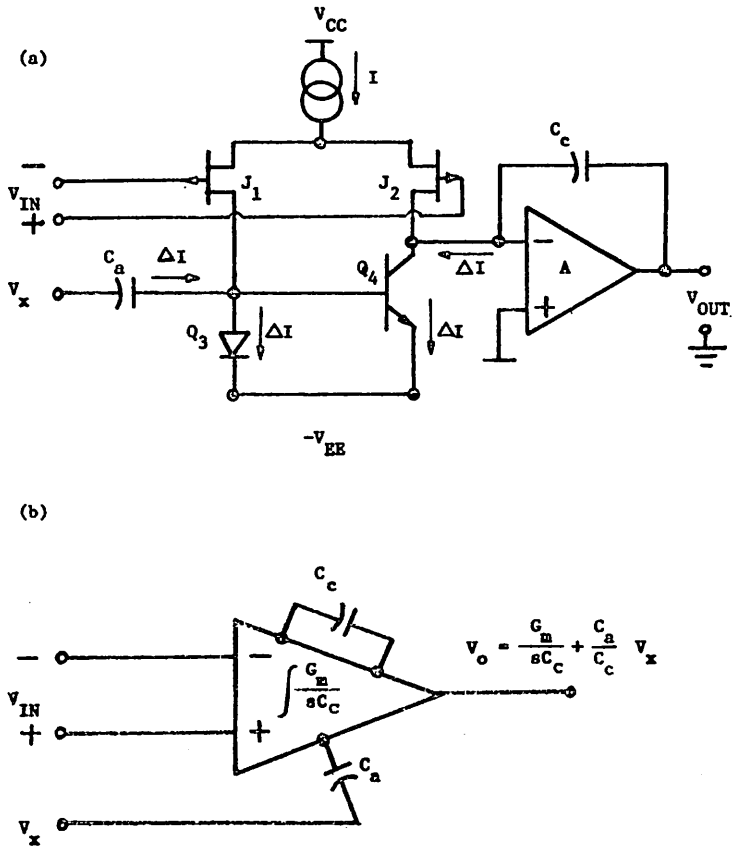


Figure 3.16 (a) The basic monolithic integrator/summer circuit, and

(b) a schematic representation of (a)

filter of Figure 3.17(a) has been transformed into the active-ladder structure using the integrator/summer circuit, as shown in Figure 3.17(b). Notice that transmission zeros are realized by simply adding the feedback and feedforward capacitors C_2. Thus with two additional capacitors, transmission zeros can be incorporated into the active-ladder filters.

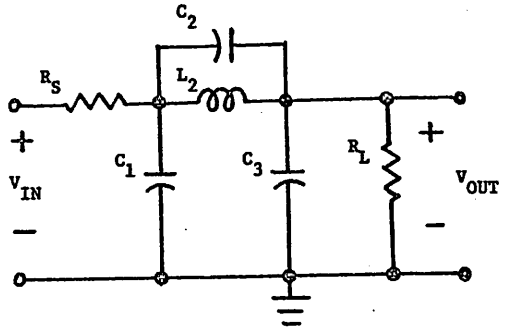
3.4. Comments

Two basic high-order filter techniques have been described, namely, the cascade and the direct approaches. These approaches are realized using integrators as basic building blocks. This class of filters is not limited to just lowpass filter realization. Highpass, bandpass and bandreject filters can be realized using integrators as basic elements [27].

From the sensitivity analysis of fifth-order lowpass filters (cf. section 3.2 and 3.3), it is seen that the direct approach, implemented using an active-ladder structure, is typically an order of magnitude less sensitive than the cascade approach. This extremely low sensitivity is very desirable. It enables the monolithic realization of high-order filters without any external trimming operations.

However, for certain applications, the cascade

(a)



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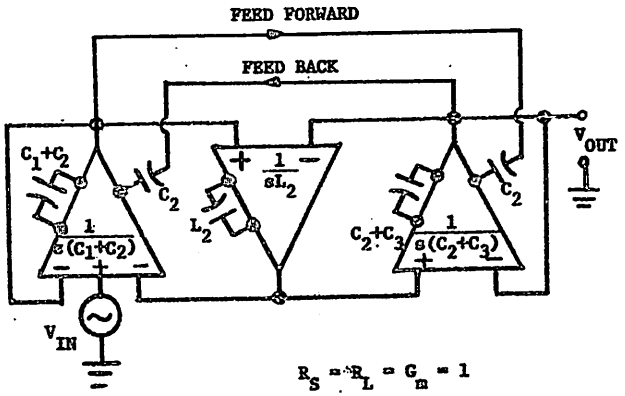


Figure 3.17 (a) An RLC third-order elliptic lowpass filter

(b) An active-ladder equivalent of the third-order elliptic lowpass filter.

approach may be preferred. For example, if a filter is specified in the time domain, then the cascade realization using second-order sections will give direct control over the natural frequencies (or eigenvalues), where each pair of the natural frequencies is determined by a second-order stage.

CHAPTER 4

PRINCIPLES OF MONOLITHIC ANALOG FILTER REALIZATION

4.1. Introduction

It has been shown that integrators can be used in a variety of circuit configurations to realize different filtering functions. In this chapter, we will outline the basic technique of realizing high-order, continuous-time, monolithic analog filters which uses integrators as basic building blocks.

First we will describe the requirements of precision monolithic integrators, followed by an outline of the basic structure of an integrator which can be effectively realized in a small silicon area. Finally, a technique of stabilizing the bandwidth of the filter will be presented.

This filter realization technique can be applied to both the cascade and the direct approaches described in Chapter 3.

4.2. Integrator Requirements

Precision integrator is a key element in monolithic filter realization. In this section, the requirements for realizing integrators with time constants in the audio

frequency range will be described.

A simple differential input integrator can be designed using two resistors, two capacitors and one operational amplifier, as shown in Figure 4.1. In this circuit, the output voltage, V_o, is given by

$$V_o = \frac{-1}{RC}\int V_{in}\, dt \qquad (4.1)$$

Hence by definition, the gain-constant of the integrator is equal to $\frac{1}{RC}$.

For low frequency operation, integrators of relatively small gain-constants (or long RC time constants) are required. For example, for a frequency of 5 kHz, with a monolithic capacitor of 30 pF, a resistor of 1 meg-ohm is needed. Precision monolithic resistors are usually realized by base diffusion which typically has a sheet resistivity of 200 ohm/□ . To implement the 1 meg-ohm resistance, a total of 5,000 squares will be needed. This large value of resistor cannot be efficiently realized using conventional monolithic approaches. Also, with conventional I.C. fabrication process, the variation in the absolute values of monolithic capacitors and resistors is large (typically 10 to 20 %), and the absolute values of resistors and capacitors vary with temperature (typical temperature coefficient for base resistor is +2000 ppm/^{o}C; for MOS capacitor is +26 ppm/^{o}C) [28]. Hence the

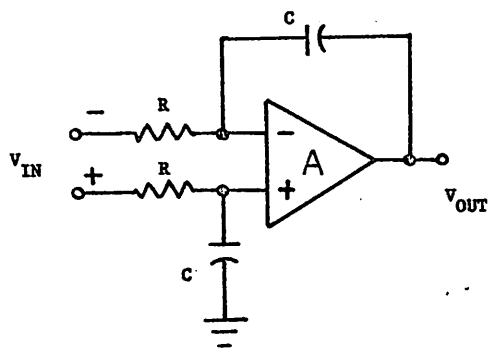


Figure 4.1 A simple RC differential input integrator.

absolute value of RC product is difficult to control.

In order to implement integrators monolithically and efficiently, a way to realize integrators with long time constants in a small silicon area is needed. Also, a technique for stabilizing the absolute magnitude of the RC product, or equivalently, the gain-constant of the monolithic integrator is required.

4.3. Monolithic Integrator

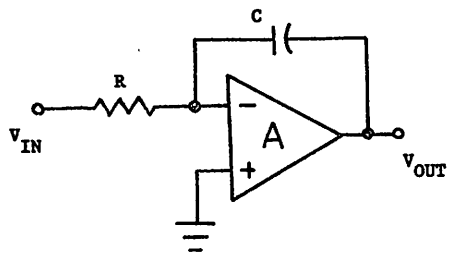
As described earlier, to realize an integrator with a small gain constants (or a long time constant), a large value of resistance must be realized. One way of realizing a large value resistor is to realize a small value of transconductance.

Let us look at an example. The circuit of Figure 4.2 (a) is an inverting integrator, in which the output voltage is given by

$$V_o = \frac{-1}{RC}\int V_{in}(t)\ dt \qquad (4.2)$$

The resistor R in this circuit can be replaced by a transconductance amplifier as shown in Figure 4.2 (b). In this figure, the output current is, by definition, given by

(a)



(b)

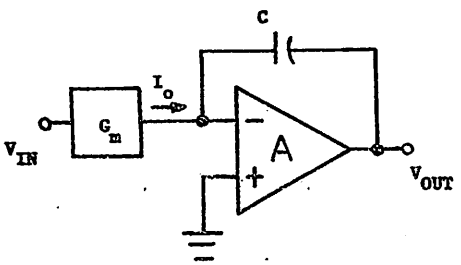


Figure 4.2 (a) An inverting integrator, and
(b) the same integrator with R being substituted by a transconductance amplifier.

$$I_o = G_m V_{in} \tag{4.3}$$

and thus the output voltage of the circuit is equal to

$$V_o = \frac{-G_m}{C}\int V_{in}\, dt \tag{4.4}$$

From equations (4.2) and (4.4), it is noticed that

$$G_m = \frac{1}{R} \tag{4.5}$$

Hence with this technique, to achieve a large value of resistance, a small value of transconductance, G_m, is needed.

A circuit which effectively realizes a small value of transconductance is shown in Figure 4.3. In this circuit, the input stage is a transconductance amplifier followed by an inverting gain stage and feedback integrating capacitor, C_c. The gain-constant of this integrator is precisely defined by the ratio of G_m to C_c, while the transconductance is expressed by the following expression:

$$G_m = \frac{\sqrt{2\, I_s\, I_{dss}}}{V_p} \tag{4.6}$$

where I_{dss} is defined as the saturation drain current, I_s is the biasing current source, and V_p is the pinch-off voltage of the junction field-effect transistor (JFET).

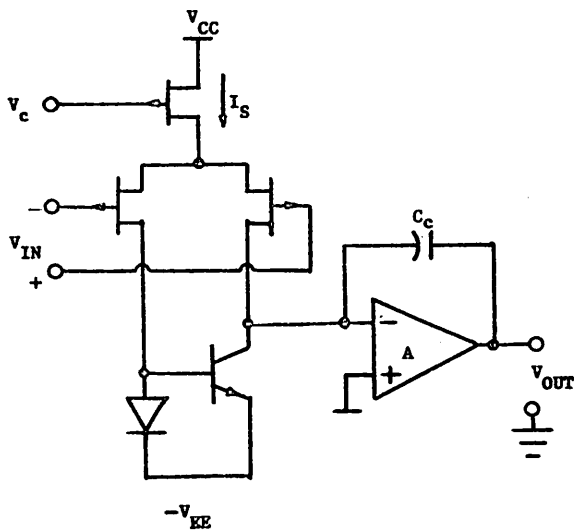


Figure 4.3 The basic monolithic differential input integrator.

In this circuit, to achieve an effective resistance of 1 meg-ohm, a transconductance of 1 micro-mho is required. This small value of the G_m can be easily achieved by designing JFET's with a small value of Z/L, as well as by operating the input stage with low current. The required chip area for realizing such a small value transconductance (and hence large value of resistance) is small.

By varying the voltage at the controlling node V_c ,as shown in Figure 4.3, the biasing current source,I_s, can be varied. By varying I_s, the G_m of the input stage is changed. Hence, by varying V_c, the G_m of the input stage, and thus the gain-constant of the integrator can be varied. This feature can be used to control the absolute magnitude of the gain-constant of the integrator, as described in the next section.

4.4. Control Technique

The absolute magnitude of the gain-constant of integrator is difficult to control due to process and temperature variations. This problem can be solved by utilizing the fact that while the absolute values of monolithic component parameters are not well controlled, the matching of one value to another on the same die is quite good. Based on this fact, the time constants of the

integrators can be locked to an externally supplied precision clock frequency using a phase-locked-loop system as shown in Figure 4.4 [29],[30]. The three main elements of this block diagram are the phase comparator, the voltage-controlled-oscillator (VCO) and the voltage-controlled-filter (VCF).

The oscillating frequency of the VCO is precisely defined by the gain constants of the two integrators (cf. section 5.5), and is given by

$$\omega_{osc} = \sqrt{\omega_1 \omega_2} \tag{4.7}$$

where ω_1, ω_2 are the gain-constants. As described earlier, the gain-constant of the integrator can be controlled through V_c. Hence by controlling V_c, we can control the frequency of oscillation. The voltage-controlled-filter is designed using the same type of integrators as those of the VCO. The bandwidth of the filter is designed to be exactly proportional to the frequency of oscillator. By varying V_c, both the frequency of the oscillator and the bandwidth of the filter are varied, and the bandwidth of the filter tracks the frequency of the oscillator. The phase comparator compares the external precision clock frequency, f_s, to the frequency of the VCO, and generates an error voltage which is then fed back to the controlling node. In the steady

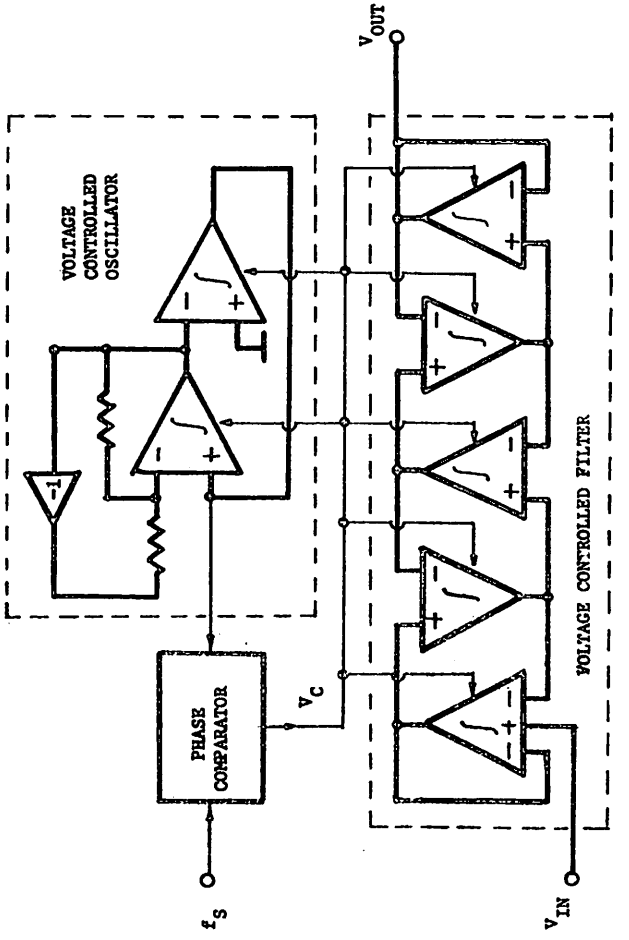


Figure 4.4 Block diagram of the filter system.

state, V_c forces the gain-constants of the integrators to have the desired values, such that the frequency of the oscillator is exactly equal to the external precision clock frequency. Since the bandwidth of the filter is exactly proportional to the frequency of the oscillator, hence the bandwidth of the filter is exactly proportional to the external precision clock frequency, and is independent of process and temperature variations.

The approach described above has several advantages. First, monolithic integrators with long time constants can be realized in small silicon area. Second, the ratio-matching of the gain-constants of integrators depends only on the ratio-matching of current sources and the ratio-matching of monolithic capacitors. These can be accurately realized [2],[13]. Finally, the absolute magnitudes of the gain-constants, and thus the bandwidth of the filter, can be precisely controlled by reference to an external precision clock frequency, and is insensitive to process and temperature variations.

CHAPTER 5

PRACTICAL CONSIDERATIONS FOR MONOLITHIC REALIZATION OF HIGH-ORDER ANALOG FILTERS

5.1. Introduction

A new approach for realizing high-order monolithic filters has been described. This technique can be applied to a special class of filters which uses integrators as basic building blocks.

In this chapter, we will consider the actual implementation of this filter technique in detail. First, practical considerations for the implementation of an active-ladder lowpass filter will be discussed. Then we will describe the actual design of a monolithic integrator. Also, we will discuss the nonidealities associated with the monolithic integrator and show how to minimize these errors. Finally the design of a voltage-controlled-oscillator and a phase detector will be presented.

5.2. Practical Considerations for a Fifth-Order Lowpass Filter

Integrators can be used in a variety of circuit configurations to realize different filtering functions.

Nonidealities associated with integrators can affect the performance of filters. In this section, we will describe the effects that these nonidealities, such as gain-constant error, DC gain error, phase error, noise and offset, have on the response of a filter. In particular, we will consider the design of a fifth-order Chebyshev lowpass filter which is realized using the active-ladder structure.

The cutoff frequency of this filter is designed to be 8 kHz, and the nominal passband ripple is 0.1 dB. The circuit diagram of the active-ladder filter is shown in Figure 5.1. In this circuit, the required unity-gain bandwidths of the integrators have values ranging from 4 kHz to 7 kHz as shown in Table 5.1

5.2.1. Effects of Gain-Constant Errors

Precision ratio-matching of the gain-constants (or unity-gain bandwidths) of integrators are required to achieve accurate filter responses. In order to observe the effects the gain-constant errors have on the frequency response of the filter, the fifth-order active-ladder filter of Figure 5.1 has been simulated for a $\pm 2\%$ variations on all the gain-constants of integrators. The simulated results are shown in Figure 5.2. In this figure, the solid line indicates the nominal magnitude response of

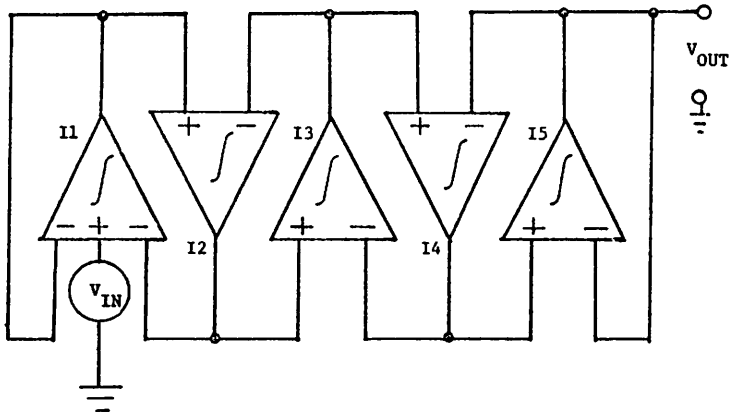


Figure 5.1 A fifth-order active-ladder all-pole filter.

TABLE 5.1

The required unity-gain bandwidths for realizing a fifth-order 8 kHz Chebyshev lowpass filter with 0.1 dB passband ripple

INTEGRATOR	UNITY-GAIN BW
I1	6.9759 kHz
I2	5.8343 kHz
I3	4.0506 kHz
I4	5.8343 kHz
I5	6.9759 kHz

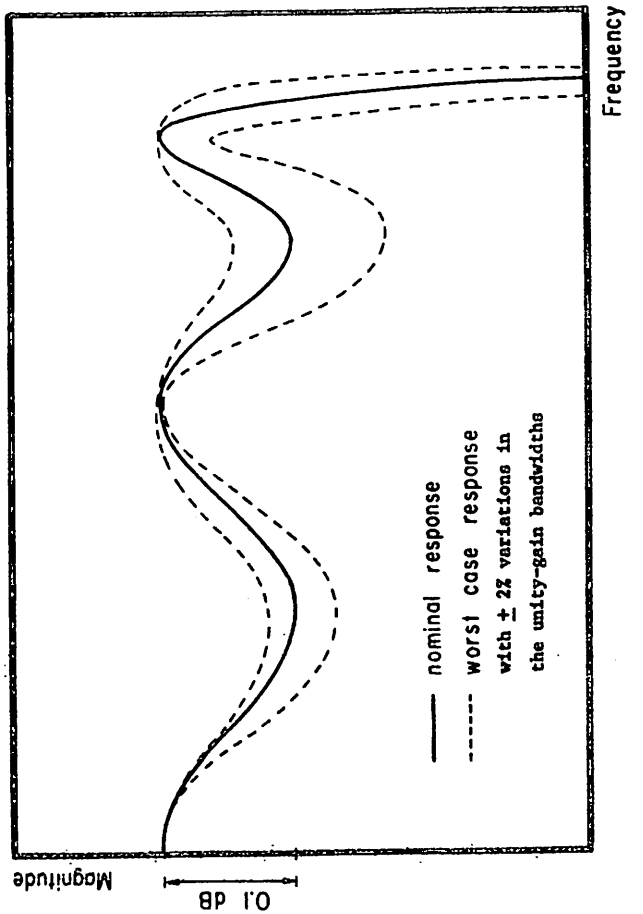


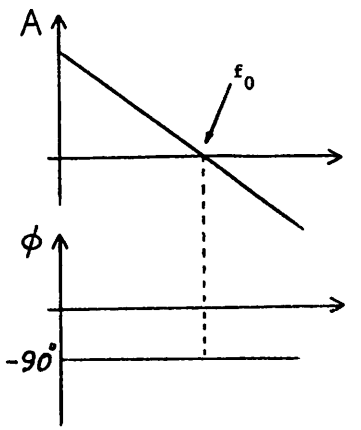
Figure 5.2 The simulated effects of gain-constant variation on the frequency response of the fifth-order active-ladder filter.

the fifth-order lowpass filter. The dotted lines indicate the bounds of the worst case deviations of any combinations of ±2% variations in the unity-gain bandwidths of the integrators. From these results, it is seen that the maximum deviations in the passband response due to ±2% gain-constant errors is less than 0.1 dB. Thus the active-ladder filter is very insensitive to gain-constant errors.

5.2.2. Effects of Integrator DC Gain Errors

Ideally, an integrator has the 1/f frequency response as shown in Figure 5.3(a). The phase is exactly 90 degrees and the gain at DC is infinite. Unfortunately, an actual monolithic integrator deviates from these ideal characteristics. For instance, a non-ideal integrator has a finite DC gain, as shown in Figure 5.3(b). This finite DC gain may affect the frequency response of the filter. Figure 5.4 shows the simulated effects that DC gain variations have on the frequency response of the fifth-order active-ladder filter described earlier. In this figure, the solid line is the nominal magnitude response of the filter, while the two dotted lines indicate the magnitude responses of the filter with integrator DC gains of 200 and 1000. When the gain is 200, the filter has a gain error of 0.11 dB at DC, with a passband droop of approximately 0.07 dB. When the integrator gain is 1000, the

(a)



(b)

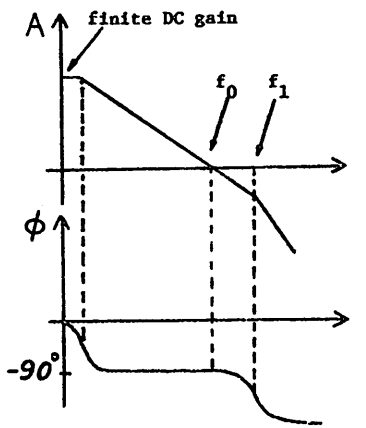


Figure 5.3 (a) An ideal integrator: the magnitude and phase responses

(b) A non-ideal integrator: the magnitude and phase responses.

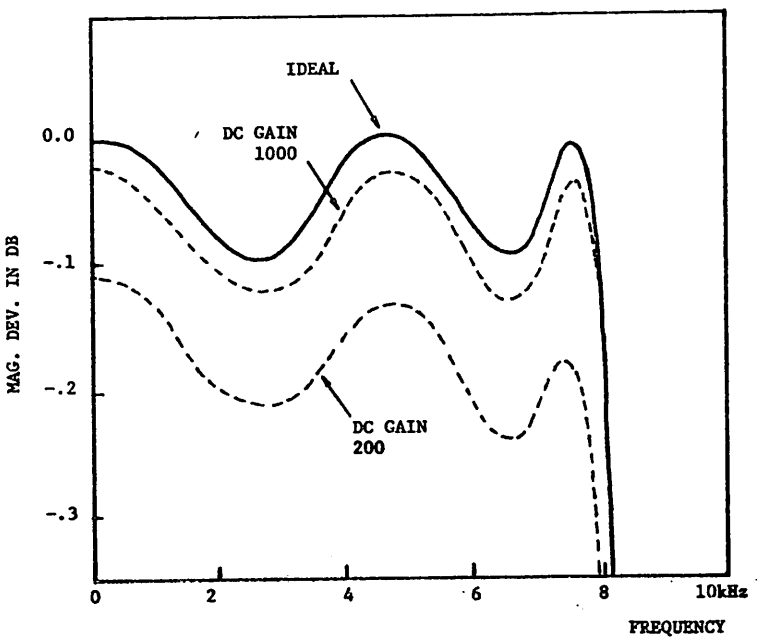


Figure 5.4 Simulated effects of DC gain on the frequency response of the active-ladder filter.

filter response shows a DC gain error of less than 0.025 dB, with a passband deviation of less than 0.015 dB. From these simulated results, it can be concluded that integrators with DC gain of greater than 1000 can be used to realize active-ladder filter with very accurate responses.

5.2.3. Effects of Excess Phase

Another non-ideal characteristic of the monolithic integrator is due to the presence of second pole, as shown in Figure 5.3(b). In this figure, f_0 corresponds to the unity-gain bandwidth, and f_1 corresponds to the second pole of the non-ideal integrator. Because of the presence of f_1, the phase at f_0 is not exactly 90 degrees. This excess phase will cause a slight peaking in the magnitude response of the fifth-order lowpass filter, as shown in Figure 5.5. In this simulated result, a 0.1 degree of phase error causes approximately a 0.1 dB peaking in the passband of the magnitude response. Typically, to achieve a phase error of less than 0.1 degree, the ratio of f_1 to f_0 has to be greater than 50. This ratio can be easily achieved using the monolithic integrator described in section 5.3.

5.2.4. Noise Considerations

The noise sources of the active-ladder filter are

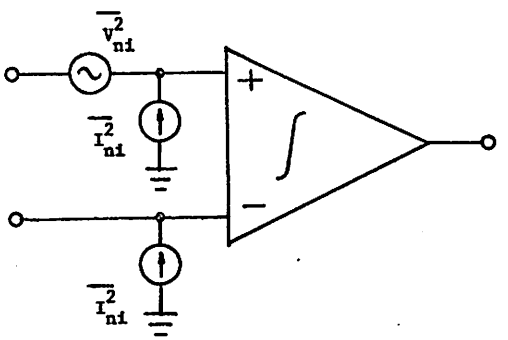


Figure 5.6 A complete integrator noise representation.

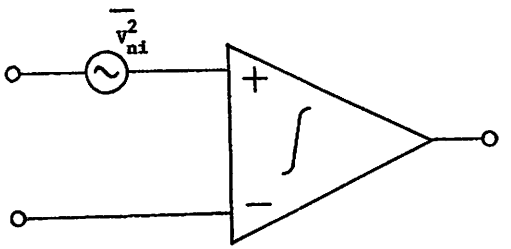


Figure 5.7 A simplified integrator noise representation.

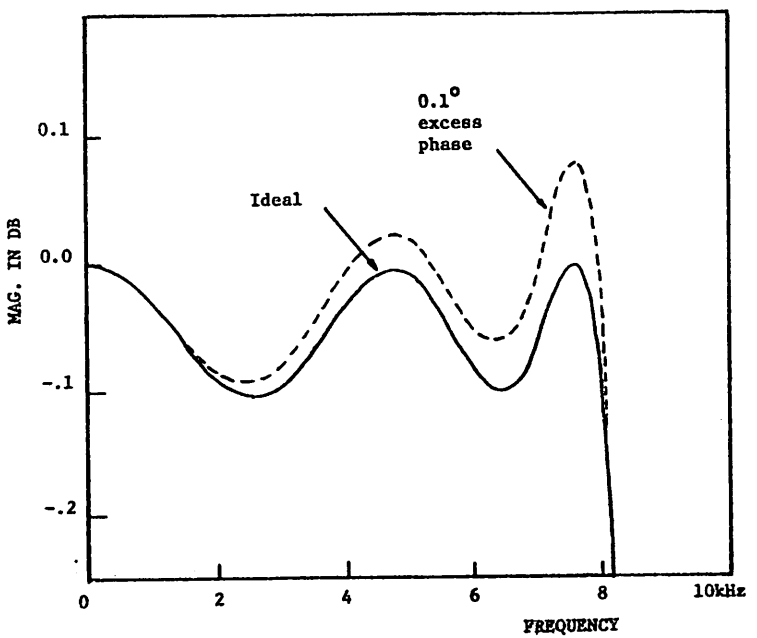


Figure 5.5 The simulated effects of excess phase on the frequency response of the active-ladder filter.

from the monolithic integrators. A complete noise representation of the integrator is shown in Figure 5.6. It consists of the equivalent input noise voltage and the two equivalent input noise current generators. Since JFET transistors will be used as input devices in the design of monolithic integrator, the equivalent input noise current, which is proportional to the input bias current of the integrator, can be neglected. Thus the noise representation of the monolithic integrator can be simplified to the form shown in Figure 5.7.

The equivalent input noise voltage of the fifth-order lowpass filter will be derived. A circuit diagram of the active-ladder filter with all its noise sources identified is shown in Figure 5.8. In this diagram, the noise voltage $\overline{V_{ni}^2}$, is the equivalent input noise voltage of the i^{th} integrator. Assuming that the noise sources are uncorrelated, then the output noise of the filter is given by

$$V_{n,out}^2 = \frac{F(s)}{G(s)G(s)} \tag{5.1}$$

where $$F(s) = V_{n1}^2+V_{n2}^2(sT_1+1)^2+V_{n3}^2(s^2T_1T_2+sT_2+1)^2+ V_{n4}^2(s^3T_1T_2T_3+s^2T_2T_3+sT_1+sT_3+1)^2+ V_{n5}^2\left[s^4T_1T_2T_3T_4+s^3T_2T_3T_4+s^2(T_3T_4+T_1T_4+T_1T_2)+ s(T_2+T_4)+1\right]^2$$

$$G(s) = s^5(T_1T_2T_3T_4T_5)+s^4(T_2T_3T_4T_5+T_1T_2T_3T_4)+$$

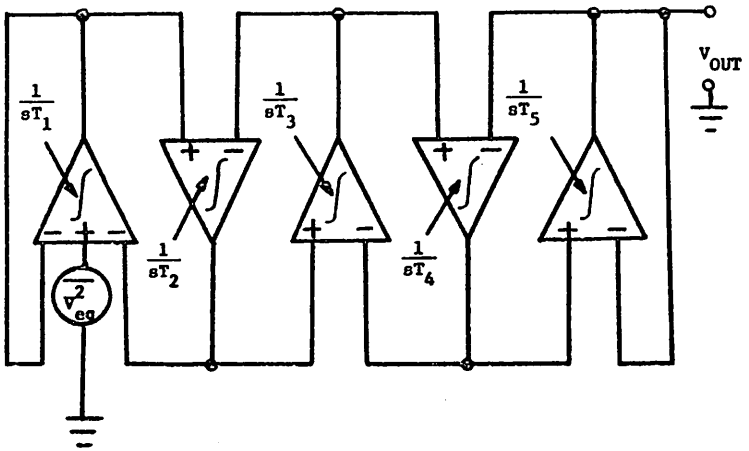


Figure 5.9 An active-ladder filter with an equivalent input noise voltage.

5.2.5. DC Offset Considerations

In this section, we will consider the effects the offset voltages of integrators have on the performance of the active-ladder filter.

The active-ladder filter circuit, with all its offset voltage sources identified, is shown in Figure 5.10. In this diagram, the offset voltage V_{osi}, is the offset voltage of the i^{th} integrator. The change in the output of the filter due to offset voltages of the integrator, is given by the following expressions:

$$V_{os,out} = \frac{K(s)}{G(s)} \tag{5.4}$$

where $K(s) = V_{os1}+V_{os2}(sT_1+1)+V_{os3}(s^2T_1T_2+sT_2+1)+$
$V_{os4}(s^3T_1T_2T_3+s^2T_2T_3+sT_1+sT_3+1)+$
$V_{os5}[s^4T_1T_2T_3T_4+s^3T_2T_3T_4+s^2(T_3T_4+T_1T_4+T_1T_2)+$
$sT_2+sT_4+1]$

and G(s) is defined in equation (5.1). Since offset voltages are DC voltages, therefore equation (5.4) can be further simplified to

$$V_{os,out} = \frac{(V_{os1}+V_{os2}+V_{os3}+V_{os4}+V_{os5})}{2} \tag{5.5a}$$

The equivalent input offset voltage of the filter can

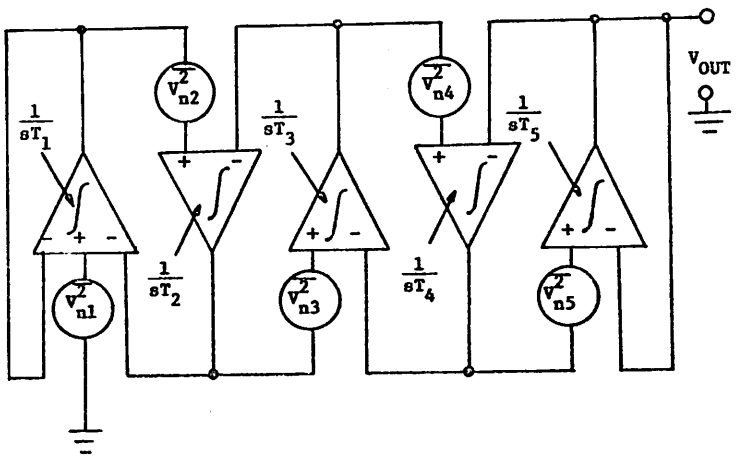


Figure 5.8 An active-ladder filter with noise sources.

$$s^3(T_2T_3T_4+T_1T_4T_5+T_3T_4T_5+T_1T_2T_3+T_1T_2T_5)+$$
$$s^2(T_1T_2+T_1T_4+T_3T_4+T_2T_3+T_2T_5+T_4T_5)+$$
$$s(T_1+T_2+T_3+T_4+T_5)+2$$

and T_1, T_2, T_3, T_4, T_5 are the time constants of the integrators.

To determine the equivalent input noise voltage of the filter, first we will determine the output noise of the active-ladder filter with a single equivalent input voltage generator, as shown in Figure 5.9. The output noise of this circuit can be easily derived and is given by

$$V_{n,out}^2 = \frac{V_{eq}^2}{G(s)G(s)} \tag{5.2}$$

where G(s) is defined in equation (5.1). By equating equations (5.1) to (5.2), the equivalent input noise voltage of the fifth-order active-ladder filter is obtained, and is shown below:

$$\overline{V_{eq}^2} = \sqrt{F(s)} \tag{5.3}$$

where F(s) is defined in equation (5.1). Thus the equivalent input noise voltage can be determined.

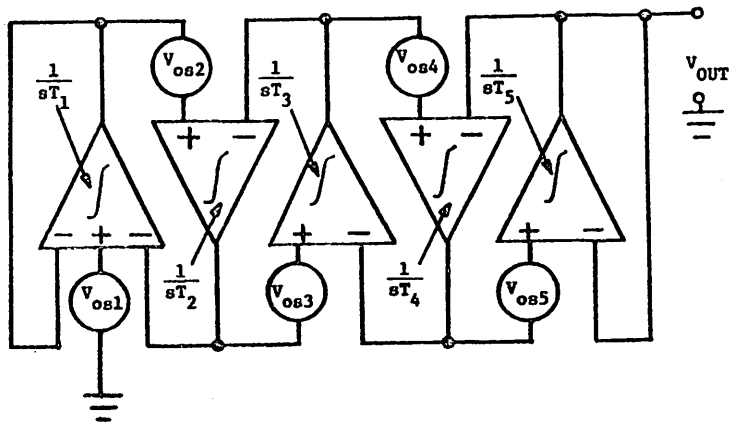


Figure 5.10 An active-ladder filter with offset voltage sources.

be calculated by dividing the output voltage of the filter by the gain of the filter. Typically, the gain of the lowpass filter at DC is 0.5. Thus the equivalent input offset voltage of the filter is

$$V_{os,in} = (V_{os1}+V_{os2}+V_{os3}+V_{os4}+V_{os5}) \qquad (5.5b)$$

The equivalent input offset voltage of the filter is thus equal to the sum of the offset voltages of integrators.

5.3. Monolithic Integrator

5.3.1 Objectives

The requirements for the monolithic integrators used in the realization of high-order filters were set as follows:

(a) The open loop gain of the integrator (at DC) should be greater than 1000. This is needed in order to have very precise frequency responses, as discussed in section 5.2.2.

(b) Since several integrators are needed to implement a high-order filter system, it is important to realize the integrator in a small silicon area. A monolithic integrator realizable in less than 1000 mil^2 was set as our goal.

(c) The power dissipation of an integrator should be less than 10 mW. This is to ensure that the power dissipation of a complete high-order filter system will not exceed the maximum limit of a low cost I.C. package (typically < 150 mW).

(d) In order to minimize the overall chip area, the maximum size of the integrating capacitor should be less than 30 pF.

(e) The ratio-matching of the unity-gain bandwidths (or gain-constants) of integrators should be better than 2%. This is needed to achieve accurate filter responses, as discussed in section 5.2.1.

5.3.2. Bipolar versus JFET

Typically, to realize a low frequency filter, integrators of relatively small gain-constants are needed. For instance, to realize an 8 kHz lowpass filter, the required gain-constants of the integrators are in the 8 kHz range. As described in Chapter 4, the gain-constant of a monolithic integrator is defined by the ratio of G_m to C_c. Thus if the maximum value of the integrating capacitor is 30 pF, then the value of G_m has to be reduced in order to achieve a small value of gain-constant.

In this section, we will investigate two different

approaches for realizing transconductance amplifiers with small G_m. One approach uses bipolar transistors, while the other uses JFET transistors as input devices. The JFET approach will be shown to have several advantages over the bipolar approach.

Let us first consider a simple bipolar input transconductance amplifier, as shown in Figure 5.11. In this circuit, transistors Q_1 and Q_2 are the emitter-coupled pair and transistors Q_3 and Q_4 are the active loads. The output current, I_o, of this circuit is given by the following expression:

$$I_o = \alpha_F I_{EE} \tanh\left(\frac{V_{in}}{2V_T}\right) \tag{5.6}$$

where α_F is the common base forward current gain of the bipolar transistor, V_T is the thermal voltage and I_{EE} is the biasing current source.

If the input signal is small, then equation (5.6) can be approximated by the following expression:

$$I_o \simeq \alpha_F \frac{I_{EE}}{2V_T} V_{in} \tag{5.7}$$

and thus

$$G_m = \alpha_F \frac{I_{EE}}{2V_T} \tag{5.8}$$

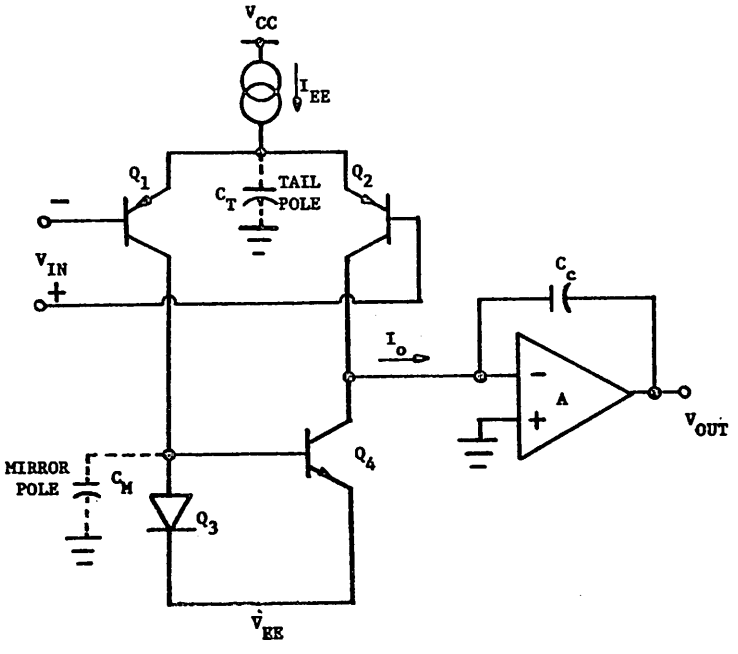


Figure 5.11 A simple bipolar-input transconductance amplifier.

As seen from equation (5.8), to realize a small value of G_m, the circuit has to be biased at a low current. For instance, to realize a G_m of a few micro-mho, a biasing current of a few tens of pico-amp is needed. This extremely low current is not practical. At this current level, the 'mirror' and 'tail' poles, as indicated in Figure 5.11, will severely bandlimit the amplifier [31]. Thus the circuit will not operate properly. Besides, this circuit is highly non-linear. A plot of output current, I_o, as a function of input voltage, V_{in}, using equation (5.6), is shown in Figure 5.12. As seen from this figure, this circuit has a linear range of only a few V_T (note: V_T = 26 mV at 300 ^oK). This circuit also suffers from slew rate limitation. The power bandwidth of this circuit, operated at such a low current, is only a few hundred hertz.

However, these difficulties can be greatly reduced by the use of a more complicated circuit, as shown in Figure 5.13. In this circuit, the relationship between the output current, I_o, and the input voltage, V_{in}, is given by the following transcendental equation:

$$V_{in} = V_T \ln\left[\frac{1 + I_o/I_{BB}}{1 - I_o/I_{BB}}\right] + \frac{I_{EE}I_o}{I_{BB}} R_E \qquad (5.9)$$

where I_{EE} and I_{BB} are the biasing current sources.

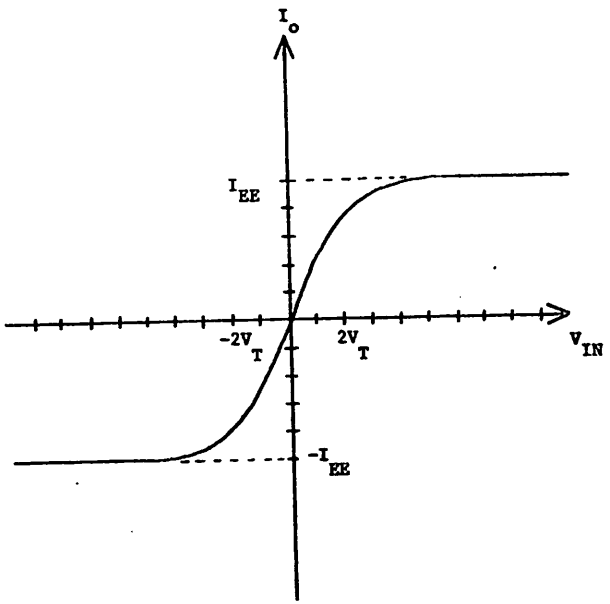


Figure 5.12 Output current as a function of differential input voltage.

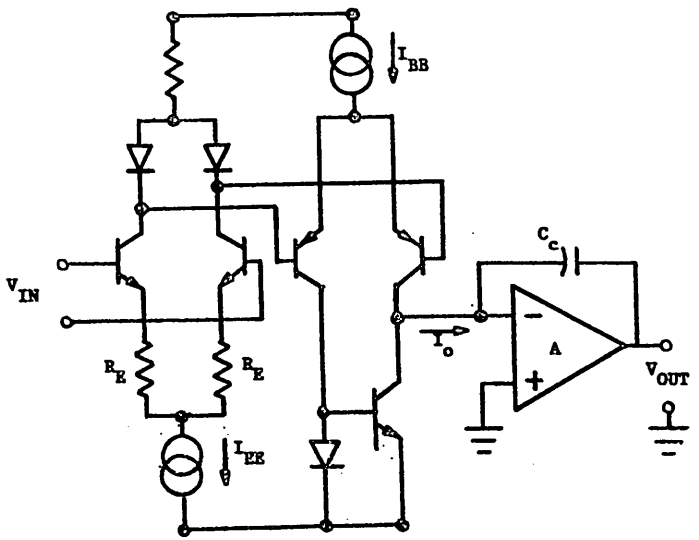


Figure 5.13 Transconductance amplifier with a predistortion circuit.

For small input signal, equation (5.9) can be approximated by the following expression:

$$I_o \simeq \frac{I_{BB}}{I_{EE}R_E} V_{in} \qquad (5.10)$$

that is

$$G_m = \frac{I_{BB}}{I_{EE}R_E} \qquad (5.11)$$

As seen from equation (5.11), to realize a small value of G_m, both the R_E and the current ratio $\frac{I_{EE}}{I_{BB}}$ have to be large. Assuming that R_E is a base diffused resistor of 10 kilo-ohm, then to achieve a G_m of 1 micro-mho, the current ratio $\frac{I_{EE}}{I_{BB}}$ is equal to 100. If we further assume I_{BB} = 4 uA (note: if I_{BB} is too small, the amplifier may be bandlimited and slew-limited), then I_{EE} of 400 uA is needed. The biasing current of this 400 uA alone will dissipate approximately 10 mW of power, using power supplies of $\pm$12 volts. If the biasing current is to be reduced, the value of resistor has to be increased, so as to achieve the desired value of G_m. Thus there is a trade-off between chip area (i.e. resistor size) and power dissipation (i.e. biasing current). Another disadvantage of this circuit is that it requires a relatively large number of devices. Thus the chip area required to implement this circuit may be large.

The main advantage of this circuit is that it has a wide range of V_{in} over which the circuit behaves in a near-linear way. A plot of I_o versus V_{in} using equation (5.9) is shown in Figure 5.14. Note that the maximum input voltage range has been increased from a few tens of millivolts (i.e. a few V_T) to a few volts (i.e. $I_{EE} \times R_E$ = 5 volts). Also, the circuit is no longer slew-limited. The power bandwidth is approximately 12 kHz (assume an output signal of 5 volt).

Next, we will investigate the JFET input transconductance amplifier. It is well known that the transconductance of a JFET is much lower than that of a bipolar transistor operated at the same bias current. This property is normally considered as a drawback, because the JFET circuit has to be biased at a much higher current level in order to achieve the same voltage gain as the bipolar counter-part. However, this low transconductance of JFET is most desirable for realizing monolithic integrator with small gain-constant. A transconductance stage using a P-channel JFET as input devices is shown in Figure 5.15. In this circuit, the output current, I_o, is given by [32]

$$I_o = \frac{I_s V_{in}}{V_p} \sqrt{\frac{2I_{dss}}{I_s} - \left(\frac{V_{in}}{V_p}\right)^2 \left(\frac{I_{dss}}{I_s}\right)^2} \qquad (5.12)$$

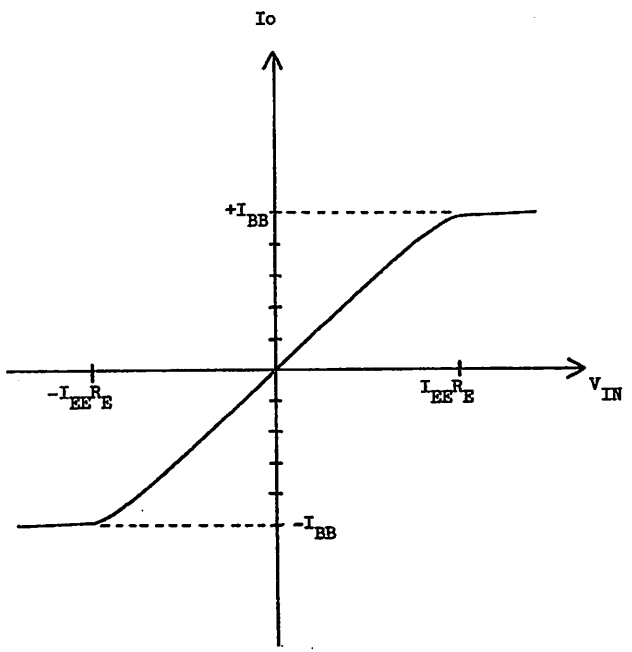


Figure 5.14 Output current as a function of differential input voltage.

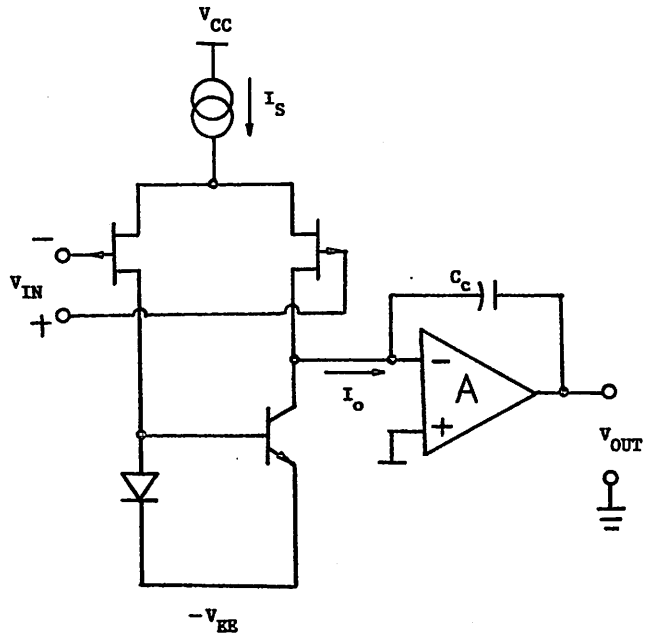


Figure 5.15 A transconductance amplifier using JFET as input devices.

Furthermore, the power dissipation of the G_m stage is less than 0.1 mW, using power supplies of $\pm$12 volts.

For the above reasons, the JFET input transconductance amplifier is preferred over the bipolar circuits, and will thus be used to realize monolithic integrator.

5.3.3. Transconductance Reduction Techniques

In this section, we will describe some circuit techniques which can be used to reduce the transconductance of a G_m stage.

The basic approach to G_m reduction is shown in Figure 5.17 [31]. In this circuit, a multiple drain structure of JFET, which can be easily realized in integrated circuit form, is used to split the drain current in such a way that part of the output current is diverted to the ground. As a result, the G_m of the circuit is reduced by a factor of $\frac{1}{1+n}$. However, care should be taken to ensure that the circuit is not bandlimited by the 'mirror' pole. This will occur if the biasing current through Q_3 is too small.

One variation of this basic technique is shown in Figure 5.18. In this circuit, one of the JFET drain current is fed into transistor Q_3 instead of the ground. In this way, the 'mirror' pole will be broadbanded. However, the emitter areas of Q_3 and Q_4 have to be ratioed

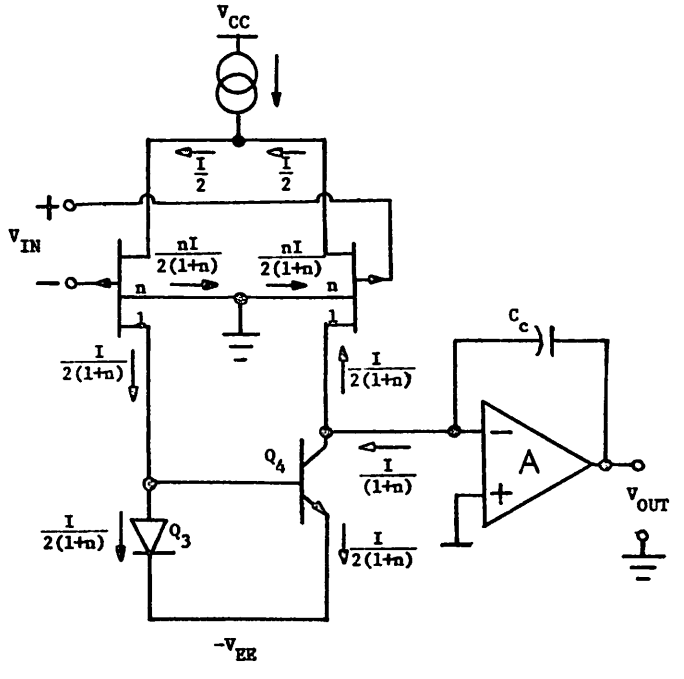


Figure 5.17 Basic G_m reduction technique using multiple drain JFETs.

where I_s is the biasing current source, I_{dss} is the saturation drain current, V_p is the pinch-off voltage of the JFET.

For small input signal, equation (5.12) can be approximated by the following expression:

$$I_o \simeq \frac{\sqrt{2I_{dss}I_s}}{V_p} V_{in} \qquad (5.13)$$

and thus

$$G_m = \frac{\sqrt{2I_{dss}I_s}}{V_p} \qquad (5.14)$$

Referring to equation (5.14), to realize a small value of G_m, we would like V_p to be large, and $I_s I_{dss}$ to be small. Assuming V_p = 4.0 volts and $I_{dss} = I_s$, then to realize a G_m of 1 micro-mho, a biasing current of 3 uA is needed. At this current level, good frequency response is expected. Also, this circuit is not slew-limited, as a power bandwidth of 9 kHz has been obtained. A plot of output current versus input voltage using equation (5.12) is shown in Figure 5.16. Notice that the maximum input voltage range of this circuit is in the order of V_p. Since V_p is typically a few volts, thus this circuit has a wide input voltage range. Another attractive feature of this circuit is that it is very simple, and thus the chip area required to implement this circuit is small.

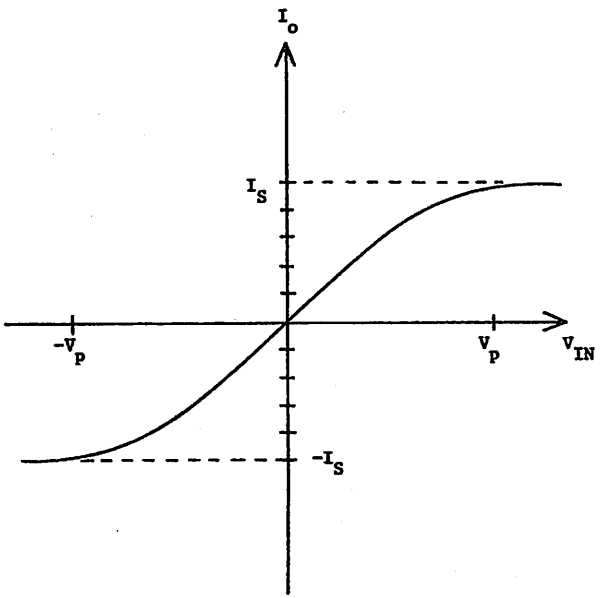


Figure 5.16 Output current as a function of differential input voltage.

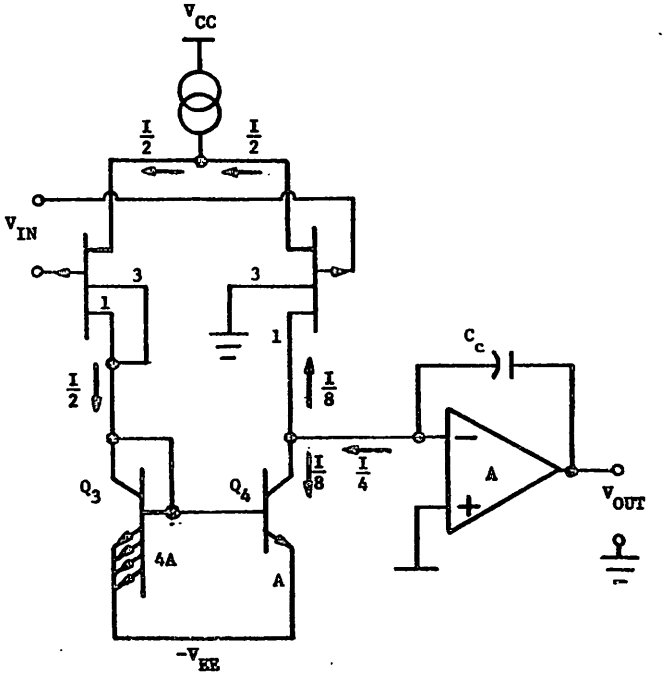


Figure 5.18 A variation of G_m reduction technique: this circuit maintains high current on diode side, thereby broadbanding the mirror pole.

accurately, otherwise offset will degrade.

Another variation is shown in Figure 5.19. In this circuit, the drains of the JFETs are cross-coupled in such a way that the AC signal is cancelled in the mirror circuit, while the DC remains completely balanced. In this way, the mirror pole is virtually eliminated. The drawback of this circuit is that the uncorrelated noise currents from the two JFET's add rather than subtract at the input to the mirror, thereby degrading the noise performance.

The circuit shown in Figure 5.20 is another variation. In this circuit, the drains of the JFET's are cross-coupled in such a way that the G_m of the amplifier is reduced by a factor of $\frac{(m+n+1)(n+1)}{1-mn}$. This circuit can be used to reduce G_m by a large factor, using only simple area ratios. For example, if n=1.5 and m=0.5, then the G_m is reduced by a factor of 30.

In general, the accuracy of the G_m of these circuits are strongly dependent on the area ratios of the transistors. Thus to achieve accurate matching of G_m, very precise area ratios will be needed.

5.3.4. Matching of Transconductances

In this section, we will consider the matching of the

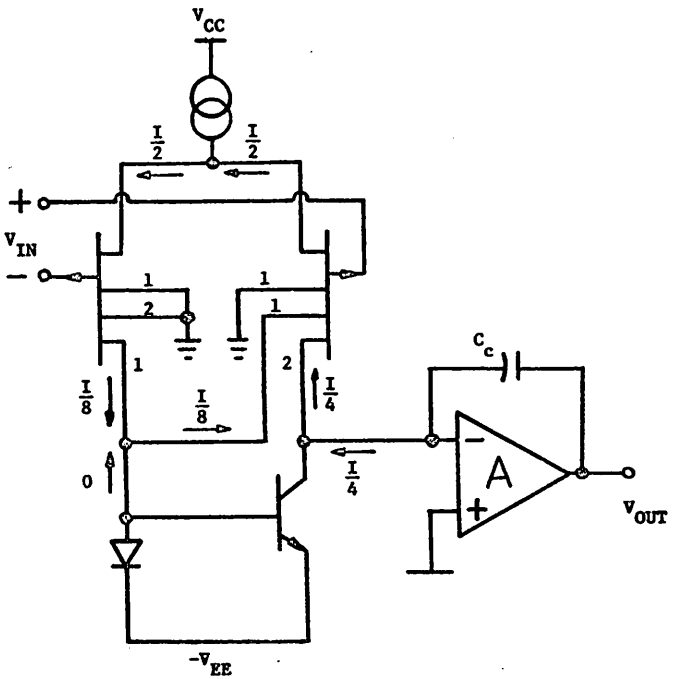


Figure 5.19 A variation of G_m reduction cross-coupled connection eliminates all AC current passing through the mirror yet maintains DC balance.

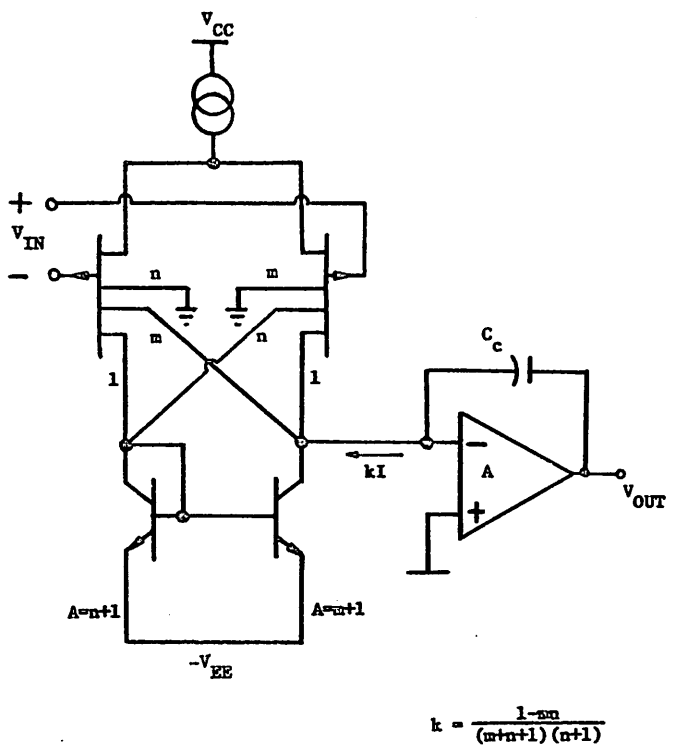


Figure 5.20 This circuit can be used to reduce G_m by a large factor using only simple area ratios.

transconductances. As described earlier, the G_m of the amplifier can be approximated by equation (5.14). As seen in this equation, to achieve an accurate G_m matching, we need to have accurate matching of I_{dss}, V_p and I_s.

It has been found experimentally that the ratio of $\frac{\sqrt{I_{dss}}}{V_p}$ is approximately a constant. This constant is proportional to the ratio of Z/L of JFET [33]. By assuming $\frac{\sqrt{I_{dss}}}{V_p} \simeq K \frac{Z}{L}$, equation (5.14) can be written as

$$G_m \simeq K \frac{Z}{L}\sqrt{I_s} \qquad (5.15)$$

Thus to achieve accurate matching of the G_m, we need to have accurate matching of Z/L and I_s. The ratio of Z/L is determined by the area of the JFET which can be accurately defined. However, the matching of I_s depends on the matching of current sources, and thus depends on the matching of JFET transistors. In order to obtain accurate matching of the JFET transistors, a bipolar compatible ion-implanted JFET process has been used. In this process, the matching of I_{dss} of the ion-implanted JFET transistors was found to be better than one percent [34]. This excellent matching of the ion-implanted JFET transistors is a key factor in the realization of accurate transconductances.

To further ensure accurate G_m matching, all the G_m

stages of the integrators are designed to be identical (note: different gain-constants of integrators can be achieved by scaling the ratios of the integrating capacitors). Also, the G_m reduction techniques described in section 5.3.3 will not be used in the design. This is because with these techniques, relatively large transistor areas will be needed in order to achieve accurate matching of G_m.

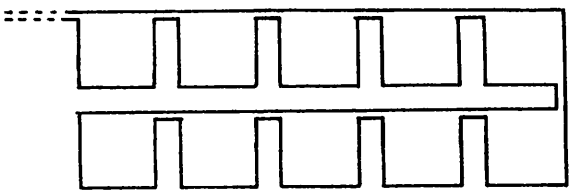
5.3.5. Matching of Integrating Capacitors

Previous work has shown that it is possible to achieve ratio-matching accuracy of a few tenths of one percent for monolithic MOS capacitors with integral ratios [2]. However, in realizing monolithic filters, typical ratio-matching of integrating capacitors are non-integral. To achieve accurate non-integral ratio-matching of capacitors, a special layout technique has been used.

This technique is best illustrated with an example. Let us consider the layout of two mnolithic capacitors of values 10.00 pF and 11.47 pF. If we assume that one unit of area represents 1 pF of capacitance, then the 10 pF capacitor can be realized in 10 units of area, as shown in Figure 5.21(a).

The realization of 11.47 pF capacitance can be divided into two parts: the realization of 11.00 pF and

(a)



(b)

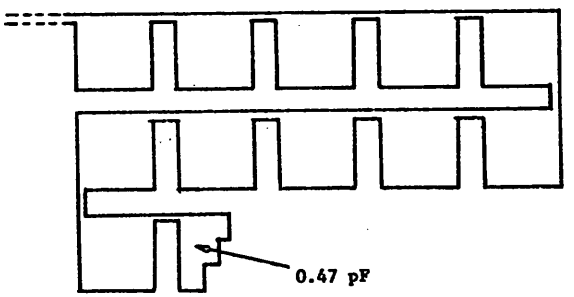


Figure 5.21 (a) The layout of a 10.00 pF MOS capacitor
(b) The layout of a 11.47 pF MOS capacitor

0.47 pF. The 11.00 pF capacitance can be realized with 11 units of area, as shown in Figure 5.21 (b). Accurate capacitance ratio-matching of 10 to 11 can thus be obtained. The remaining 0.47 pF of capacitance can be realized using 0.47 of a unit, also shown in Figure 5.21(b). By doing this, certain layout rules, which are required to achieve accurate ratio-matching of capacitors, are violated [35]. Thus the expected ratio-matching will not be as good as before. Let us examine what will happen if there is a 2 % error in the value of 0.47 pF. The resulting capacitance value will be 0.47x1.02 = 0.4794 pF. This will introduce an overall discrepancy of $\frac{(11.4794-11.47)}{11.47} \times 100\% = 0.08\%$. Thus by the use of this layout technique, non-integral ratio-matching of capacitances can be accurately achieved.

5.3.6. Multiple Input Integrator

Multiple input integrators are frequently used in implementing filters. For example, to realize an active-ladder lowpass filter, a three-input integrator is required.

In this section, the realization of a four-input monolithic integrator will be described. This four-input integrator can be realized by connecting two G_m stages to an inverting gain stage as shown in Figure 5.22. In this

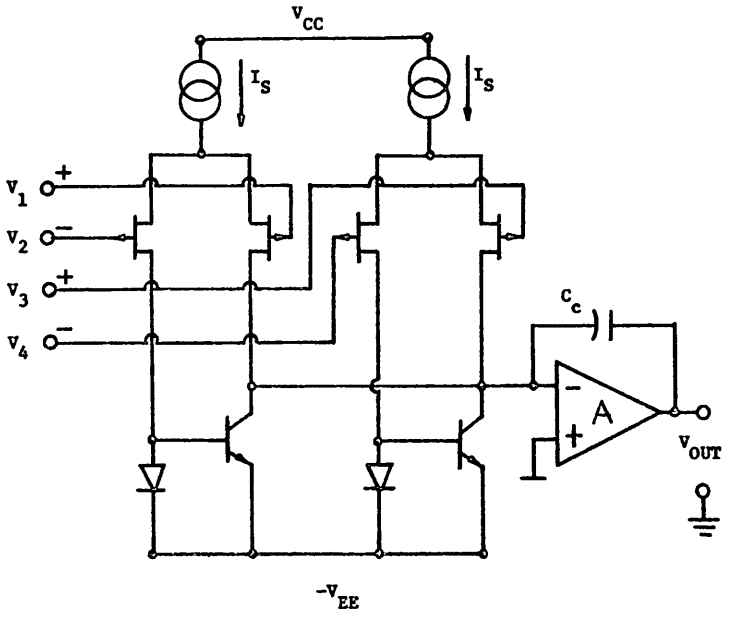


Figure 5.22 A four-input integrator.

circuit, if we assume that the G_m of the two input stages are identical, then the output of the integrator is given by

$$V_o = \frac{G_m}{C_c} \int \left[V_1(t)-V_2(t)+V_3(t)-V_4(t)\right] dt \qquad (5.16)$$

where $V_1(t), V_2(t), V_3(t), V_4(t)$ are input voltages, G_m is the transconductance of the input stage, and C_c is the integrating capacitor. To realize a three-input integrator, one input terminal should be grounded. In general, this technique can be applied to realize integrator with any number of inputs.

5.3.7. Increasing Input Voltage Range

As described earlier, the maximum input voltage range of the JFET transconductance amplifier is in the order of V_p. In practice, however, we would like to have the largest possible input voltage range, so that the circuit will have a wide range of linear operations. The input voltage range of the JFET G_m stage can be increased in two ways.

One obvious way of increasing the maximum input voltage range is to use JFET with high pinch-off voltage. The drawback of this approach is that as one tries to increase V_p, the input and output common mode ranges will be reduced. Thus, in the design of the G_m stage, a

pinch-off voltage of 4 volts is chosen as a compromise.

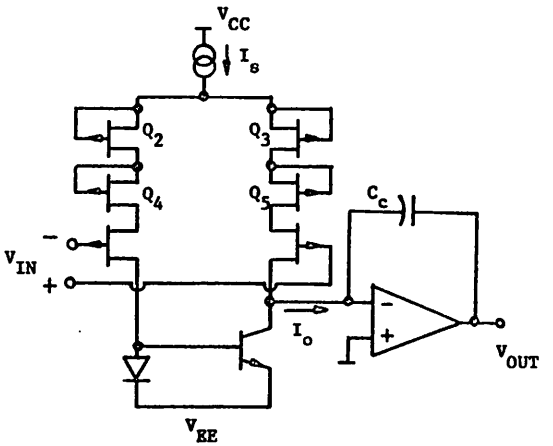
Another way of increasing the maximum input voltage range is to use the input stage as shown in Figure 5.23(a). In this circuit, four additional transistors, Q_2 through Q_5, are used as source degeneration JFET resistors. A plot of output current versus input voltage is shown in Figure 5.23 (b). Notice that by simply adding four transistors, the maximum input voltage range has been increased by a factor of three. Actually, we can add as many of the JFET resistors as necessary to improve the linearity of the transconductance amplifier. The disadvantage is that when the number of transistors increases, the chip area also increases. This may impose a practical limit on the maximum number of transistors used. Also, care should be taken to ensure that the frequency response of the circuit is not very much degraded by the gate to substrate capacitances of the source degeneration JFET resistors.

5.3.8. Distortion of the Integrator

One way of describing the non-linearity of an integrator is the specification of harmonic distortion.

As an illustration, the transfer characteristic of a transconductance amplifier is shown in Figure 5.24 together with the input voltage and output current

(a)



(b)

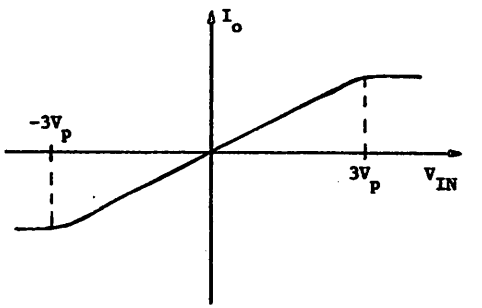


Figure 5.23 (a) The monolithic integrator with a new input stage to improve the linearity of the circuit
(b) A plot of I_o versus V_{IN}.

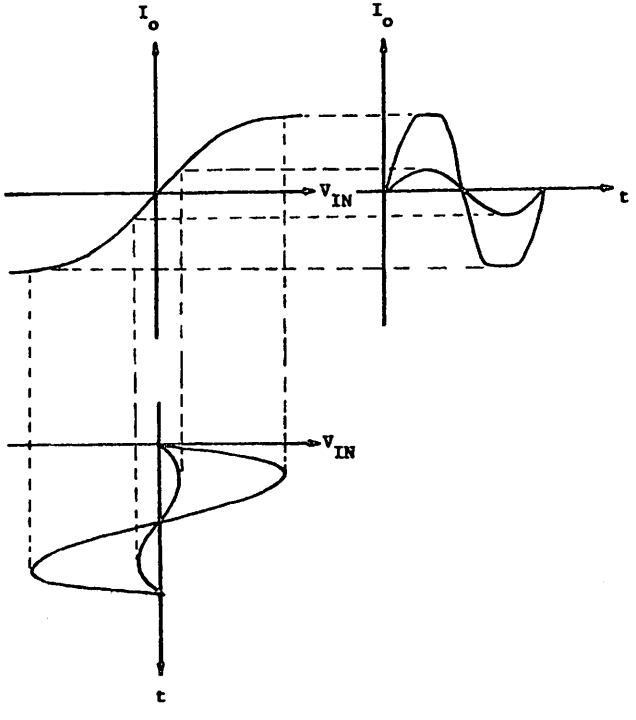


Figure 5.24 The transfer characteristic of the transconductance amplifier together with input voltage and output current waveforms.

waveforms. As shown in this diagram, when the input signal is small, the circuit behaves linearly. However, when the input voltage is comparable to the maximum input voltage range, $V_{in,max}$. the output waveform becomes distorted. From this illustration, it is clear that the harmonic content of the output current increases as input voltage increases.

In Figure 5.25, the total-harmonic-distortion (THD) of the output current is plotted as a function of the normalized input voltage. From this simulated result, it is noticed that to have a less than 1% THD at the output, the input voltage should be less than $\emptyset.4\ V_{in,max}$.

5.3.9. Control of Transconductance

One important feature of the monolithic integrator is that the G_m of the amplifier can be controlled by varying the biasing current. This feature can be used to stabilize the absolute magnitude of the gain-constants of the integrators, as described in Chapter 4.

In this section, the circuit of Figure 5.23(a) will be used to investigate the control range of G_m. A plot of G_m as a function of the biasing current is shown in Figure 5.26. As seen in this figure, by varying the current source from $\emptyset.8I_{dss}$ to $1.68I_{dss}$, the G_m of the amplifier can be varied over the range of $\pm 20\%$.

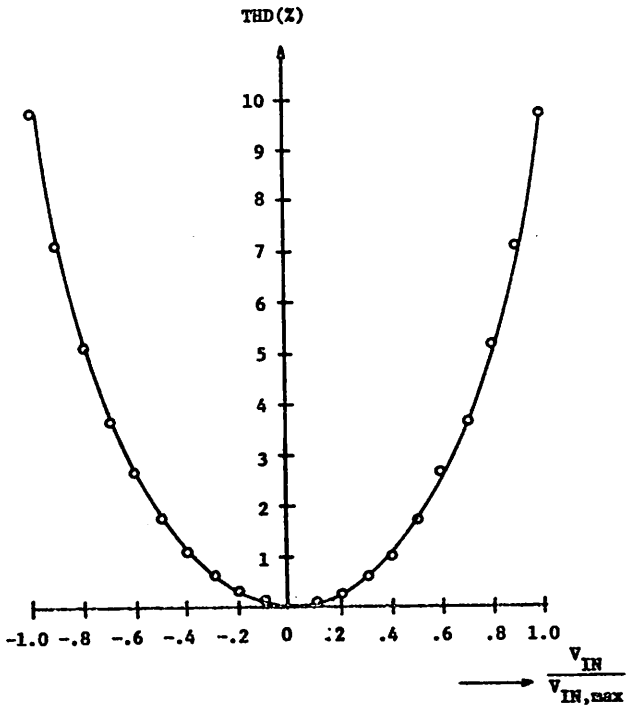


Figure 5.25 The total-harmonic-distortion of I_o as a function of input voltage. (simulated result)

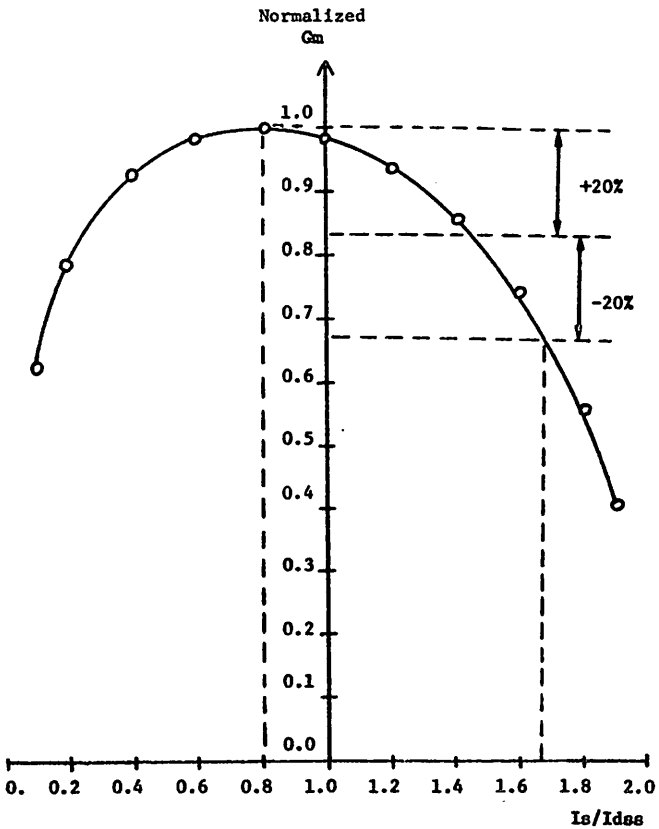


Figure 5.26 G_m as a function of biasing current. (simulated result)

However, one drawback of this circuit is that, when the G_m of the amplifier is varied, the maximum input voltage range also changes. For instance, when I_s is varied from $0.8I_{dss}$ to $1.68I_{dss}$, so as to achieve a $\pm 20\%$ variation in G_m, the maximum input voltage range is changed by a ratio of 2 to 1.

5.3.10. Final Design of the Monolithic Integrator

The final design of the monolithic integrator is shown in Figure 5.27. The input transconductance stage consists of transistors Q_1 through Q_{12}. Transistors Q_2 through Q_5 are used as source degeneration resistors. Transistors Q_8 through Q_{10} are used as active loads. Transistors Q_{11} and Q_{12} are used as emitter degeneration resistors to improve the noise and offset of the integrator. With no emitter degeneration, the noise and offset of the bipolar devices when referred to the input will be amplified by the ratio of the bipolar to JFET transconductances. By using JFET transistors as degeneration resistors, the noise and offset voltage of the integrator can be lowered with little increase in silicon area. Transistor Q_1 is the biasing current source. By varying this current, the transconductance of the input stage can be varied. This feature is used to control the bandwidth of the integrator, as outlined in chapter 4.

The next stage is the source follower which consists

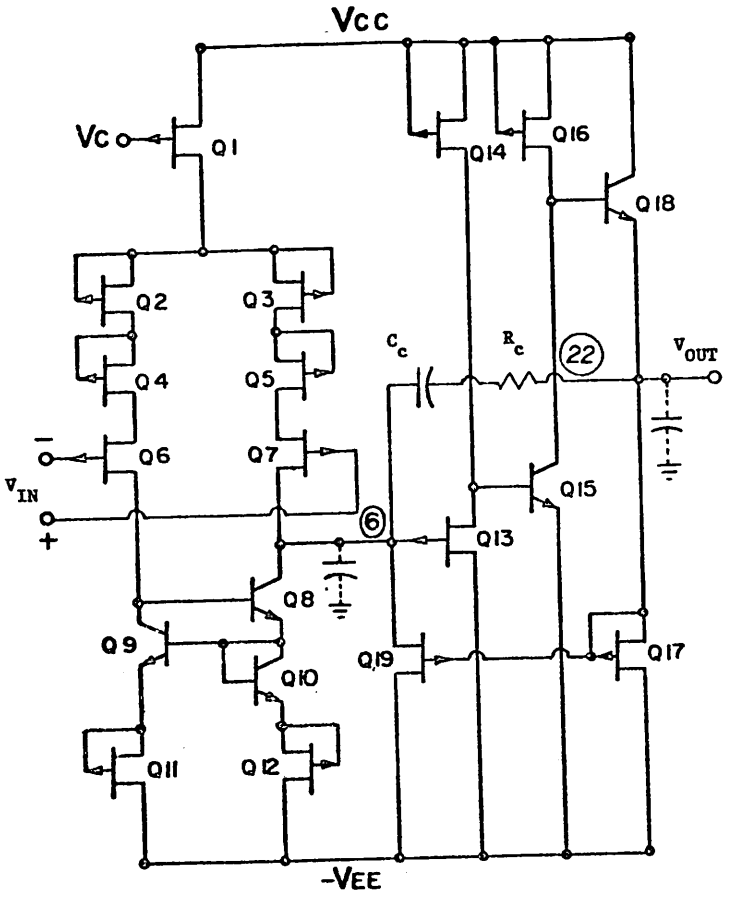


Figure 5.27 Final circuit diagram of the monolithic integrator.

of transistors Q_{13} and Q_{14}. This is used to minimize the loading to the transconductance stage. Transistor Q_{15} and Q_{16} constitute the common emitter inverting stage. Transistors Q_{18} and Q_{17} are used as emitter follower output stage to reduce the output impedance to about 10 kilo-ohms.

The output of the integrator is clamped by transistor Q_{19}, such that the output common mode range is always smaller than the input common mode range. This prevents the integrator from latching up.

A resistor, R_c (of a few kilo-ohms) is in series with the integrating capacitor, C_c, to provide a high frequency zero to improve the phase margin of the circuit.

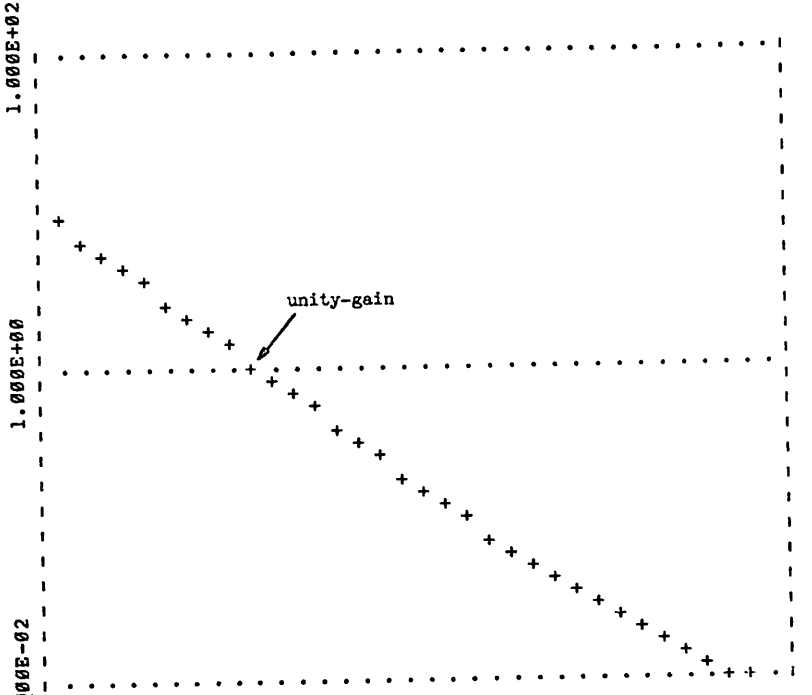
Computer simulation was used to evaluate the performance of the circuit. The circuit analysis program SPICE2 was used [36]. The parameters used for the device models were determined from experimental characteristics of devices that had previously been fabricated. A complete listing of the input data to the circuit analysis program SPICE2 is shown in Table 5.2. The simulated DC open loop gain of the integrator is greater 50,000. The simulated output magnitude and phase versus frequency of the integrator (with 30pF of integrating capacitor) are shown in Figures 5.28 and 5.29. From these figures, it is noticed that the phase error at the unity gain of the

TABLE 5.2

```
*** MONOLITHIC INTEGRATOR - BIFET PROCESS ***
*** TRANSCONDUCTANCE STAGE ***
JQ1 5 40 10 JM1 1.450
JQ6 7 31 3 JM2
JQ7 6 32 4 JM2
JQ4 3 45 15 JM1
JQ5 4 46 16 JM1
JQ2 15 55 5 JM1
JQ3 16 35 5 JM1
JQ11 13 41 11 JM1
JQ12 13 39 9 JM1
Q8 6 7 8 NPN1
Q9 7 8 11 NPN1
Q10 8 8 9 NPN1
*** INVERTING GAIN STAGE ***
JQ13 13 36 20 JM3
JQ14 20 50 10 JM1 3.50
JQ16 21 60 10 JM1 7.00
JQ17 13 52 22 JM1 7.00
Q15 21 20 13 NPN1
Q18 10 21 22 NPN1
*** INTEGRATING CAPACITOR ***
Q20 10 6 6 NPN2 1.76
CC 33 6 30PF
RC 22 33 3K
*** MODELING COLLECTOR-TO-SUBST. DIODES ***
DQ8 13 6 D1
DQ9 13 7 D1
DQ10 13 8 D1
DQ15 13 21 D1
*** MODELING GATE-TO-SUBST. DIODES ***
DQ1 13 40 D4
DQ6 13 31 D2
DQ7 13 32 D2
DQ4 13 45 D2
DQ5 13 46 D2
DQ2 13 55 D2
DQ3 13 35 D2
DQ11 13 41 D2
DQ12 13 39 D2
DQ13 13 36 D3
DQ14 13 50 D2
DQ16 13 60 D2
DQ17 13 52 D2
```

TABLE 5.2 (cont'd)

```
*** MODELING GATE RESISTANCES ***
RQ1 10 40 5K
RQ6 1 31 1K
RQ7 2 32 1K
RQ4 15 45 1K
RQ5 16 46 1K
RQ2 5 55 1K
RQ3 5 35 1K
RQ11 11 41 1K
RQ12 9 39 1K
RQ13 6 36 3.5K
RQ14 10 50 2K
RQ16 10 60 2K
RQ17 22 52 1K
*** POWER SUPPLIES ***
VCC 10 0 +12
VEE 13 0 -12
*** MODEL CARDS ***
.MODEL NPN1 NPN ( IS=1.26E-15 BF=150 BR=2.0 RB=500
+RC=2K TF=1.2N KF=5.0E-16
+CJE=0.64P CJC=0.80P PC=0.5 PE=0.7 VA=170 )
.MODEL NPN2 NPN ( IS=1.26E-15 BF=150 BR=2.0 RB=500
+RC=2K TF=1.2N KF=5.0E-16
+CJE=0.64P CJC=21.0P PC=0.5 PE=0.7 VA=170 )
.MODEL JM1 PJF ( VTO=-4.0   BETA=.500E-6 LAMBDA=2.0E-3
+ RD=200 RS=200 CGS=0.3P CGD=0.3P PB=0.6 IS=1.00E-15 )
.MODEL JM2 PJF ( VTO=-4.0   BETA=.500E-6 LAMBDA=2.0E-3
+ RD=400 RS=200 CGS=0.3P CGD=0.3P PB=0.6 IS=1.00E-15 )
.MODEL JM3 PJF ( VTO=-4.0  BETA=.0840E-3 LAMBDA=0.02
+ RD=200 RS=200 CGS=1.9P CGD=1.9P PB=0.6 IS=1.00E-15 )
.MODEL D1 D ( IS=1.26E-15 CJO=4.7PF PB=0.6 )
.MODEL D2 D ( IS=1.26E-15 CJO=5.3PF PB=0.6 )
.MODEL D3 D ( IS=1.26E-15 CJO=12.7P PB=0.6 )
.MODEL D4 D ( IS=1.26E-15 CJO=6.3PF PB=0.6 )
*** OUTPUT REQUEST ***
.OPTIONS NUMDGT=6
RIN 1 0 1N
VIN 2 0 -2.54M AC 1
.TF V(22) VIN
.AC DEC 10 100 1MEG
.PRINT AC VM(22) VP(22) VM(21) VP(21) VM(6) VM(20)
.PLOT AC VM(22) (1E-2,1E6)
.PLOT AC VP(22) (-180,180)
.END
```

FREQ (HZ)	VM(22)	1.000E-02
5.012E+02	8.425E+00	
6.310E+02	6.692E+00	
7.943E+02	5.316E+00	
1.000E+03	4.222E+00	
1.259E+03	3.354E+00	
1.585E+03	2.664E+00	
1.995E+03	2.116E+00	
2.512E+03	1.681E+00	
3.162E+03	1.335E+00	
3.981E+03	1.060E+00	
5.012E+03	8.417E-01	
6.310E+03	6.682E-01	
7.943E+03	5.303E-01	
1.000E+04	4.207E-01	
1.259E+04	3.335E-01	
1.585E+04	2.641E-01	
1.995E+04	2.089E-01	
2.512E+04	1.650E-01	
3.162E+04	1.302E-01	
3.981E+04	1.027E-01	
5.012E+04	8.130E-02	
6.310E+04	6.473E-02	
7.943E+04	5.200E-02	
1.000E+05	4.216E-02	
1.259E+05	3.446E-02	
1.585E+05	2.834E-02	
1.995E+05	2.344E-02	
2.512E+05	1.950E-02	
3.162E+05	1.631E-02	
3.981E+05	1.371E-02	
5.012E+05	1.158E-02	
6.310E+05	9.840E-03	
7.943E+05	8.464E-03	
1.000E+06	7.430E-03	

Figure 5.28 Magnitude response of the monolithic integrator (computer simulation).

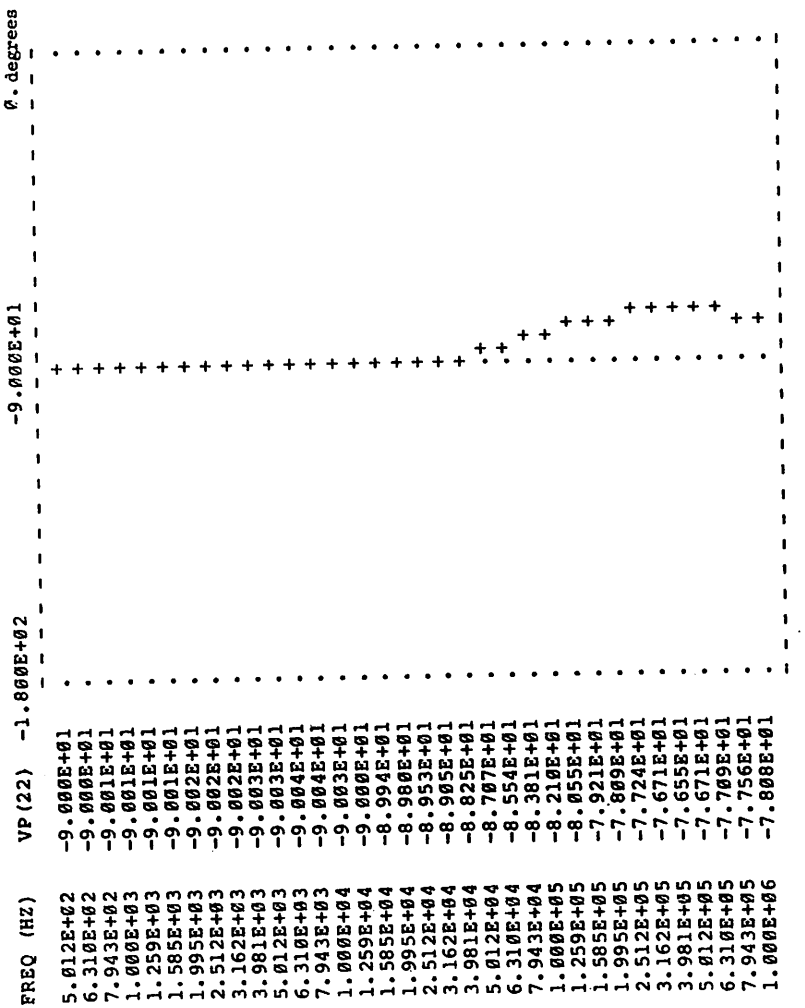


Figure 5.29 Phase response of the monolithic integrator (computer simulation).

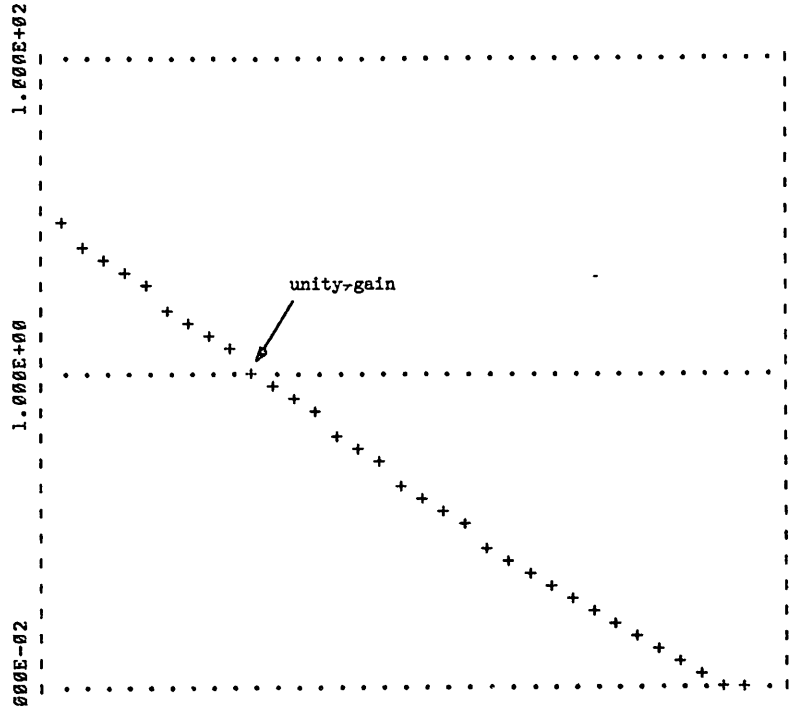
integrator is less than 0.03 degree. This 0.03 degree of phase error will introduce a passband deviation of less than 0.03 dB for a fifth order lowpass filter, as discussed in section 5.2.3.

To determine the sensitivity of the magnitude and phase responses of this integrator due to parasitics, two 20 pF capacitors were connected at nodes 22 and 6 to ground, as shown in Figure 5.27. The simulated output magnitude and phase versus frequency of the integrator are shown in Figures 5.30 and 5.31. It is seen from these figures that the unity-gain bandwidth is virtually unchanged. The phase at the unity gain of the integrator is shifted by only 0.01 degrees. In practice, the parasitic capacitances will be much less than what was used for the simulation. Thus this circuit is very insensitive to parasitic capacitances.

5.3.11. Noise Calculation

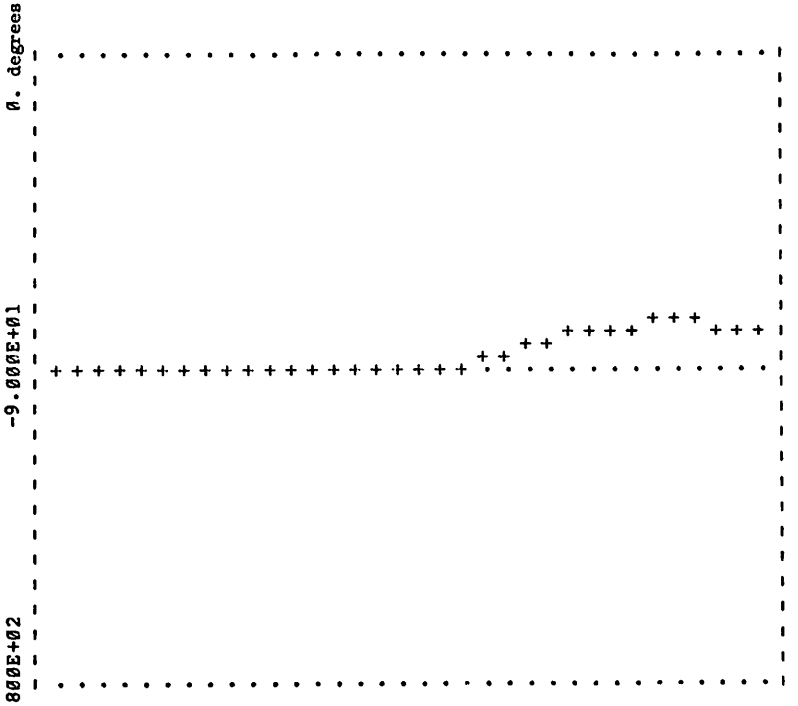
The circuit analysis program SPICE2 was used to evaluate the noise performance of the integrator.

The 1/f noise of the JFET transistor is omitted. This is because the ion-implanted JFET is a low noise device, and the corner frequency of this device is typically in the order of a few hundred hertz. At this frequency range, the 1/f noise of the bipolar transistor will



FREQ (HZ)	VM(22)
5.012E+02	8.424E+00
6.310E+02	6.691E+00
7.943E+02	5.315E+00
1.000E+03	4.222E+00
1.259E+03	3.353E+00
1.585E+03	2.664E+00
1.995E+03	2.116E+00
2.512E+03	1.680E+00
3.162E+03	1.335E+00
3.981E+03	1.060E+00
5.012E+03	8.416E-01
6.310E+03	6.681E-01
7.943E+03	5.303E-01
1.000E+04	4.206E-01
1.259E+04	3.335E-01
1.585E+04	2.641E-01
1.995E+04	2.089E-01
2.512E+04	1.650E-01
3.162E+04	1.302E-01
3.981E+04	1.027E-01
5.012E+04	8.129E-02
6.310E+04	6.472E-02
7.943E+04	5.199E-02
1.000E+05	4.216E-02
1.259E+05	3.446E-02
1.585E+05	2.835E-02
1.995E+05	2.345E-02
2.512E+05	1.952E-02
3.162E+05	1.633E-02
3.981E+05	1.374E-02
5.012E+05	1.162E-02
6.310E+05	9.901E-03
7.943E+05	8.548E-03
1.000E+06	7.548E-03

Figure 5.30 Magnitude response of the monolithic integrator with parasitic capacitances (computer simulation).



FREQ (HZ)	VP(22)
5.012E+02	-9.000E+01
6.310E+02	-9.001E+01
7.943E+02	-9.001E+01
1.000E+03	-9.001E+01
1.259E+03	-9.001E+01
1.585E+03	-9.001E+01
1.995E+03	-9.002E+01
2.512E+03	-9.002E+01
3.162E+03	-9.003E+01
3.981E+03	-9.003E+01
5.012E+03	-9.004E+01
6.310E+03	-9.004E+01
7.943E+03	-9.004E+01
1.000E+04	-9.004E+01
1.259E+04	-9.001E+01
1.585E+04	-8.995E+01
1.995E+04	-8.982E+01
2.512E+04	-8.955E+01
3.162E+04	-8.907E+01
3.981E+04	-8.828E+01
5.012E+04	-8.711E+01
6.310E+04	-8.559E+01
7.943E+04	-8.388E+01
1.000E+05	-8.218E+01
1.259E+05	-8.065E+01
1.585E+05	-7.933E+01
1.995E+05	-7.825E+01
2.512E+05	-7.744E+01
3.162E+05	-7.696E+01
3.981E+05	-7.685E+01
5.012E+05	-7.708E+01
6.310E+05	-7.753E+01
7.943E+05	-7.809E+01
1.000E+06	-7.866E+01

Figure 5.31 Phase response of the monolithic integrator with parasitic capacitances (computer simulation).

dominate, and thus the 1/f noise contribution of the JFET can be neglected. The noise parameters for NPN transistors used in the simulated are similar to those in 741 op-amp, as indicated in Table 5.2 [37].

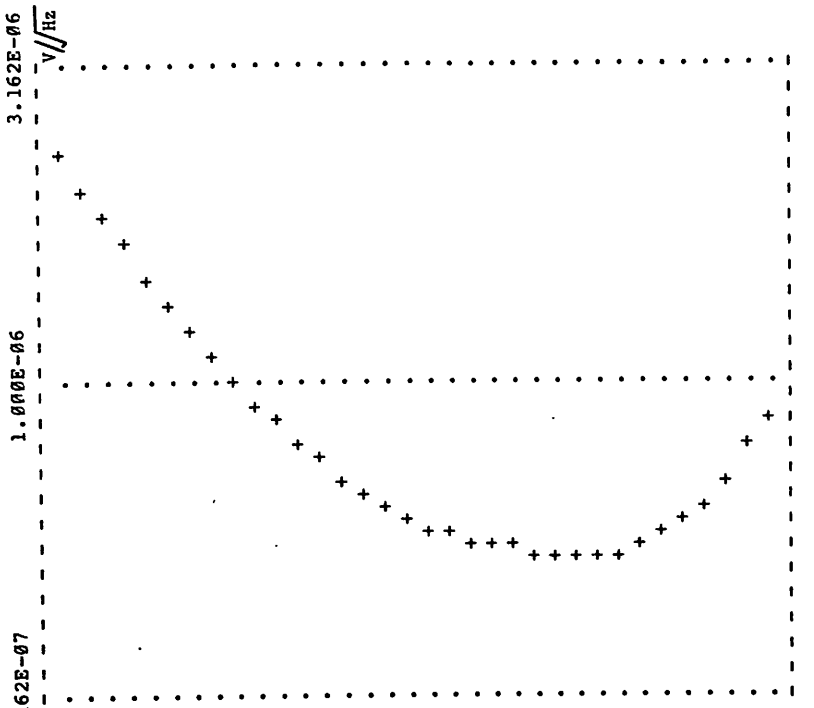
The equivalent input noise voltage as a function of frequency is shown in Figure 5.32. From this simulated result, the equivalent input noise voltage, over a frequency band of 10 kHz is found to be 60 uVrms.

5.3.12. Input Offset Voltage

The input offset voltage range expected in this monolithic integrator is moderately high. This is attributed to the low transconductance of the input stage. If we assume that there is a 0.5 % mismatch in the I_{dss} of JFET transistors (Q_2-Q_7, Q_{11}-Q_{12}), and a 5 % mismatch in I_{ES} of bipolar transistors (Q_8-Q_{10}), then the worst case input offset voltage is found to be 55 mV.

5.3.13. Slew Rate

The slew rate of this circuit can be calculated as follows: slew-rate= Is/Cc=12uA/30pF=0.4 V/usec. At this slew rate, the power bandwidth for an output of 10 Vp-p is 12.7 kHz. Hence this monolithic integrator circuit is not slew limited.



FREQ (HZ)	INOISE
5.012E+01	2.244E-06
6.310E+01	2.013E-06
7.943E+01	1.808E-06
1.000E+02	1.627E-06
1.259E+02	1.468E-06
1.585E+02	1.327E-06
1.995E+02	1.204E-06
2.512E+02	1.097E-06
3.162E+02	1.003E-06
3.981E+02	9.222E-07
5.012E+02	8.523E-07
6.310E+02	7.925E-07
7.943E+02	7.415E-07
1.000E+03	6.983E-07
1.259E+03	6.621E-07
1.585E+03	6.319E-07
1.995E+03	6.068E-07
2.512E+03	5.862E-07
3.162E+03	5.694E-07
3.981E+03	5.559E-07
5.012E+03	5.452E-07
6.310E+03	5.370E-07
7.943E+03	5.312E-07
1.000E+04	5.276E-07
1.259E+04	5.266E-07
1.585E+04	5.287E-07
1.995E+04	5.348E-07
2.512E+04	5.465E-07
3.162E+04	5.658E-07
3.981E+04	5.955E-07
5.012E+04	6.391E-07
6.310E+04	7.000E-07
7.943E+04	7.822E-07
1.000E+05	8.904E-07

Figure 5.32 Equivalent input noise voltage of the integrator as a function of frequency (computer simulation).

5.4. Voltage-Controlled-Oscillator (VCO)

The usefulness of the phase-locked-loop (PLL) concept described in Chapter 4 depends on the tracking between the voltage-controlled-oscillator (VCO) and the voltage-controlled-filter (VCF). The required tracking can be achieved by realizing the VCO on the same silicon chip using the same types of integrators as those in the filter section, and by designing the operating frequency of the VCO to be exactly proportional to the bandwidth of the filter. With these, any temperature and process variations will affect both the VCO and the VCF simultaneously. Thus the overall effects to the filter system will be cancelled.

In this section, we will describe the design of a VCO which uses integrators as basic elements. The operating frequency of the VCO is such that it is equal to the gain-constant of the integrator.

5.4.1. Development of an Oscillator from an Active-RC Filter

We can derive an oscillator from an active-RC filter simply by bringing the poles of the filter into the right-half plane. This is usually done with a simple modification, such as introducing a feedback network into the active filter. In this section, the development of an

oscillator from a second-order filter will be described.

For convenience, the second-order filter described in Chapter 3 is again shown in Figure 5.33. This active filter requires two integrators and two resistors. The resonant frequency of this filter is given by $\omega_o = \sqrt{\omega_1\omega_2}$, where ω_1,ω_2 are the gain-constants of the integrators. The transfer function of the bandpass output node, V_{BP}, is given by

$$a(s) = \frac{V_{BP}}{V_{in}}(s) = \frac{-s\omega_1}{s^2 + s\omega_1\left(\frac{R_7}{R_7+R_8}\right) + \omega_1\omega_2} \qquad (5.17)$$

where ω_1, ω_2 are the gain-constants of the integrators.

To realize an oscillator from this active-RC filter, we have to introduce a feedback loop between the output of the filter and V_{in}, as shown in Figure 5.34. Assuming the effects of feedback loading are small, then the overall gain of this circuit with feedback network is

$$A(s) = \frac{a(s)}{1 + a(s)f} \qquad (5.18)$$

Using equations (5.17) in (5.18), we obtain

$$A(s) = \frac{-s\omega_1}{s^2 + s\omega_1\left(\frac{R_7}{R_7+R_8} - f\right) + \omega_1\omega_2} \qquad (5.19)$$

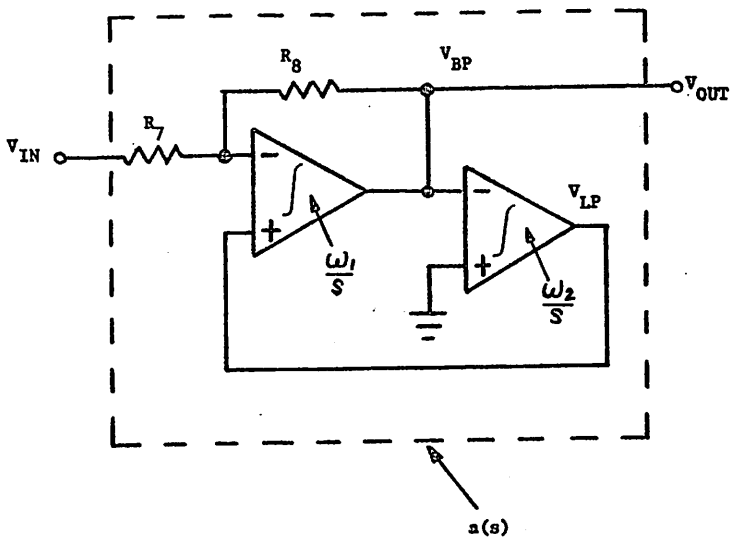


Figure 5.33 A second-order active-RC filter.

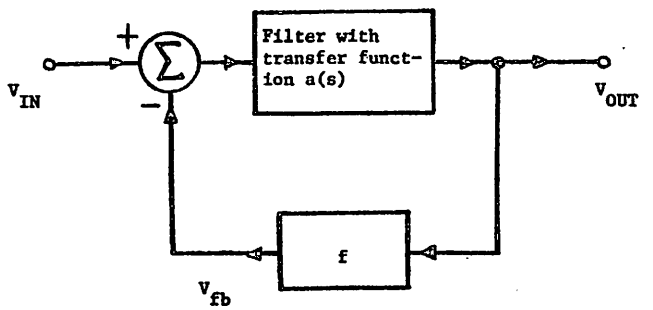


Figure 5.34 A feedback circuit configuration.

The poles of A(s) correspond to the roots of the equation

$$s^2 + s\omega_1\left(\frac{R_7}{R_7+R_8} - f\right) + \omega_1\omega_2 = 0 \qquad (5.20)$$

Thus the roots of equation (5.20) are given by

$$s_{1,2} = \alpha \pm j\beta \qquad (5.21)$$

where $\alpha = -\left(\frac{R_7}{R_7+R_8} - f\right)\frac{\omega_1}{2}$

$$\beta = (\omega_1\omega_2 - \alpha^2)$$

Using equation (5.21), the poles of A(s) for any given value of f can be determined. For example, when f=0, the poles are at

$$s_{1,2} = -\frac{\omega_1 R_7}{2(R_7+R_8)} \pm j\sqrt{\omega_1\omega_2 - \left(\frac{\omega_1 R_7}{2(R_7+R_8)}\right)^2} \qquad (5.22)$$

These poles correspond to the poles of the second-order filter without feedback. However, as f is made finite, the poles move towards the right-half plane. The locus of the roots is shown in Figure 5.35. Each point of this

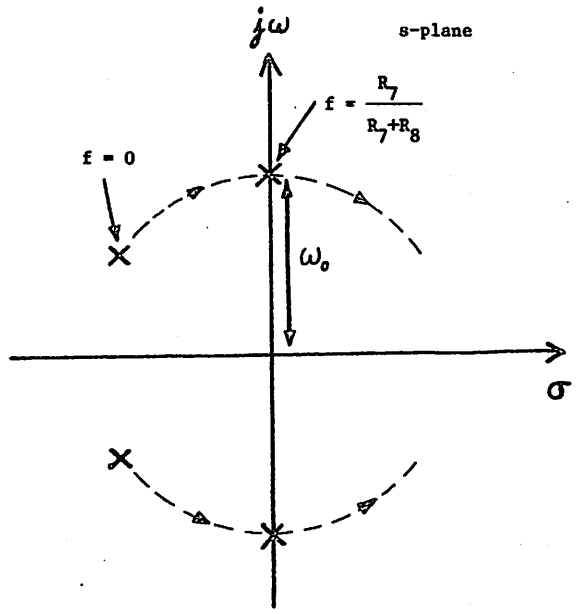


Figure 5.35 A root locus of the active-RC filter with feedback.

root locus can be identified with a value of f. When $f = \frac{R_7}{R_7+R_8}$, the poles will lie exactly on the jω axis, that is

$$s_{1,2} = \pm j\sqrt{\omega_1\omega_2} \qquad (5.23)$$

Hence when $f \geq \frac{R_7}{R_7+R_8}$, the circuit becomes unstable and oscillation will occur. The frequency of oscillation is determined by the distance of the complex poles from the origin of the s-plane, and is given by

$$\omega_o = \sqrt{\omega_1\omega_2} \qquad (5.24)$$

If we assume $\omega_1 = \omega_2 = \omega$, then $\omega_o = \omega$. Thus the frequency of oscillation is exactly equal to the gain-constant of the integrator.

In practice, if the feedback function f is designed to be equal to the minimum value of $\frac{R_7}{R_7+R_8}$, then any small variation in f may bring the complex poles back into the left-half plane. Thus the oscillation will stop. To ensure that oscillation will occur under the worst case conditions, the feedback function is designed to be larger than the required minimum value. Also, an amplitude-limiting mechanism is used to stabilize the steady-state oscillation amplitude. As the envelop of the output

waveform increases, the amplitude limiting mechanism will push the complex poles towards the left-half plane. However, when the oscillation signal is small, the amplitude-limiting mechanism will have no effect on the filter. As a result, a steady-state oscillation amplitude will occur when the poles are exactly on the imaginary axis. These basic techniques are frequently used in practice, and will be used in the final design of the VCO as well.

5.4.2. Final Design of the VCO

The final circuit of the VCO is shown in Figure 5.36. In this circuit, a unity-gain inverting amplifier is used to provide a feedback function of unity (i.e. f=1). The diodes D_1 and D_2 are used as an amplitude limiter to stabilize the steady-state oscillation amplitude. A Q of 6 is chosen as a compromise. This is because when the Q is too large, then the outputs of the integrators will be overloaded. If the Q is too small, the harmonic contents of the output waveforms will be undesirably high. In this circuit, there are two possible outputs, namely, at V_2 and V_3. Interestingly, the sinusoidal waveforms of these outputs are exactly 90^o out of phase due to the presence of an integrator between these two nodes.

As described earlier, the frequency of this oscilla-

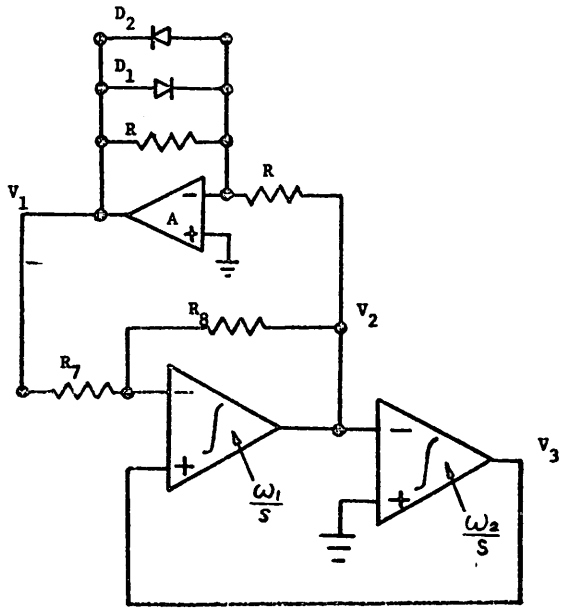


Figure 5.36 The final circuit of the VCO.

tor is equal to the gain-constant of the integrator (if we assume $w_1 = w_2 = w$). Since the gain-constant of the integrator is voltage controllable, thus the frequency of this oscillator is also voltage controllable. Hence this circuit is a voltage-controlled-oscillator.

5.4.3. Total-harmonic-distortion (THD) of the VCO

It is important to observe the harmonic distortion of the output sinusoidal waveforms. If the harmonic content is high, then the operating frequency of the oscillator will be shifted, and thus will be different from the fundamental frequency of the waveforms [38].

In order to estimate the distortion of the output waveforms of the oscillator, we will assume that the clipping of the amplitude limiter is hard and symmetrical. The waveform at V_1 thus approximates a square wave. The Fourier analysis of a square wave indicates that square wave consists of the odd harmonics as described by the following expression:

$$V_1 = \frac{4E}{\pi}\left[\sin(\omega t)+\frac{1}{3}\sin(3\omega t)+\frac{1}{5}\sin(5\omega t)+\ldots\right] \qquad (5.25)$$

At output node V_2, the fundamental frequency is multiplied by a factor of Q while the n^{th} harmonic is multiplied by a factor of $\frac{n}{n^2-1}$ approximately [38]. The relative amplitude of the third harmonic, with respect to the

fundamental, is thus changed from 1/3 (from equation 5.25) to

$$\frac{1}{3}x\frac{1}{Q}x\frac{n}{n^2-1} = \frac{1}{3}x\frac{1}{6}x\frac{3}{8} \text{ --> } 2.08\% \qquad (5.26)$$

and the fifth harmonic is changed from 1/5 to

$$\frac{1}{5}x\frac{1}{Q}x\frac{n}{n^2-1} = \frac{1}{5}x\frac{1}{6}x\frac{5}{24} \text{ --> } 0.69\%, \text{ etc} \qquad (5.27)$$

The total-harmonic-distortion (THD) is thus found to be less than 3 %. Hence, the square wave becomes a fairly good sine wave at V_2.

However, if the output waveform is taken from V_3, then the THD of the waveform will be even lower. Due to the presence of an integrator between V_2 and V_3, the harmonics of the waveform are further reduced by a factor of $\frac{1}{n}$. Thus the third harmonic at V_3 is reduced to

$$\frac{1}{n}x2.08\% = \frac{1}{3}x2.08\% \text{ --> } 0.69\% \qquad (5.28)$$

The fifth harmonic is reduced to

$$\frac{1}{n}x0.69\% = \frac{1}{5}x0.69\% \text{ --> } 0.14\%, \text{ etc.} \qquad (5.29)$$

and the THD at V_3 is found to be less than 1%.

Since the THD at V_3 is lower than that at V_2, it is more desirable to take the output from V_3. The less than 1% of THD will have negligible effects on the operating frequency of the oscillator.

5.5. Phase Comparator

One other component needed for realizing a complete filter system is the phase comparator (or phase detector). Monolithic phase detectors have been widely used in realizing monolithic PLL's such as the 560/561/562 series circuits.

In this section, the operations of this phase detector circuit will be briefly discussed [32]. The monolithic phase detector circuit is based on the Gilbert multiplier shown in Figure 5.37. This circuit may be used for three types of applications. When V_1 and V_2 are small, the circuit behaves as an analog multiplier. When V_2 is small and V_1 is large (i.e. large compared to $2V_T$), then the circuit acts as a modulator. However, when both the V_2 and V_1 are large, then the circuit behaves as a phase detector. For our application, we are interested in realizing phase detection, and thus requires the magnitudes of both V_1 and V_2 to be large.

Let us consider the input waveforms of V_1 and V_2 as shown in Figure 5.38(a) and 5.38(b). In this case, the

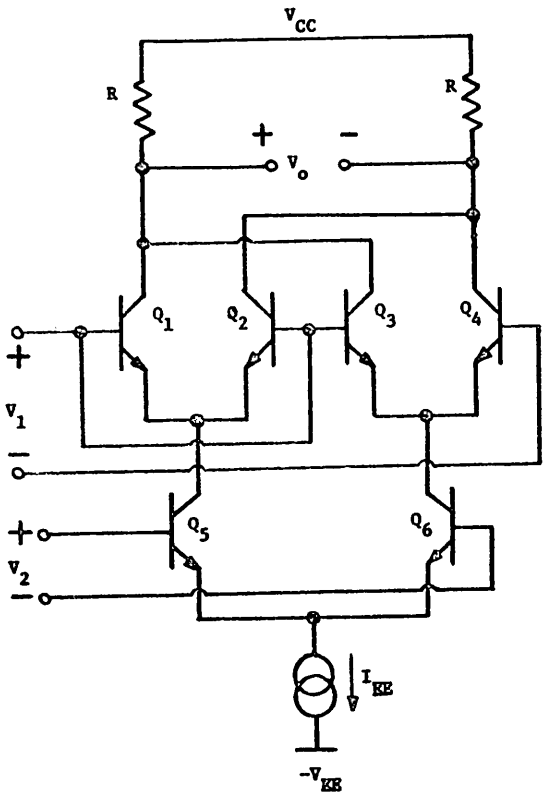


Figure 5.37 The phase detector circuit.

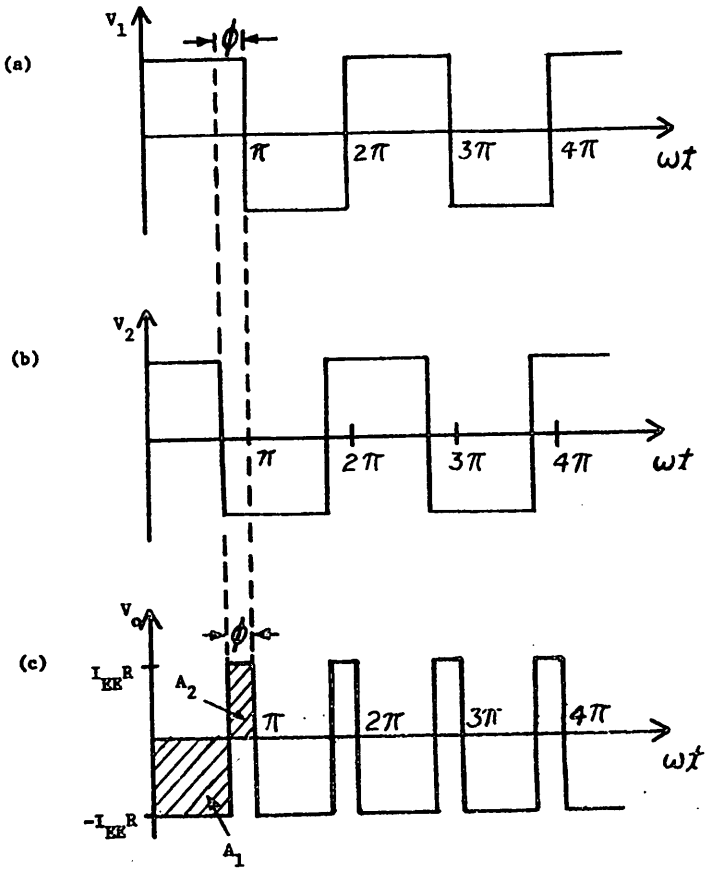


Figure 5.38 Typical input and output waveforms for a phase detector.

magnitudes of both inputs are large so that all the transistors in the circuit are behaving as switches. The resulting output waveform is shown in Figure 5.38(c). The output waveform consists of a DC component and a component at twice the incoming frequency. Assuming that the higher frequency component can be filtered out, then the DC component or V_{avg}, is given by

$$V_{avg} = \frac{1}{2\pi}\int_0^{2\pi} V_o(t)\,d(\omega_o t)$$

$$= -\frac{1}{\pi}(A1-A2) \qquad (5.30)$$

where A_1, A_2 are shown in Figure 5.38(c). Hence we can write

$$V_{avg} = -\frac{1}{\pi}\left[I_{EE}R(\pi-\phi)-I_{EE}R\phi\right]$$

$$= I_{EE}R\left(\frac{2\phi}{\pi}-1\right) \qquad (5.31)$$

The V_{avg} versus phase relationship described by equation (5.31) is plotted in Figure 5.39.

The above discussion assumed that the input waveforms were square wave. In practice, as long as the input signal amplitude is large, the actual waveshape is unimportant. The multiplier will simply switches from one state to the other at the zero crossing of the waveforms.

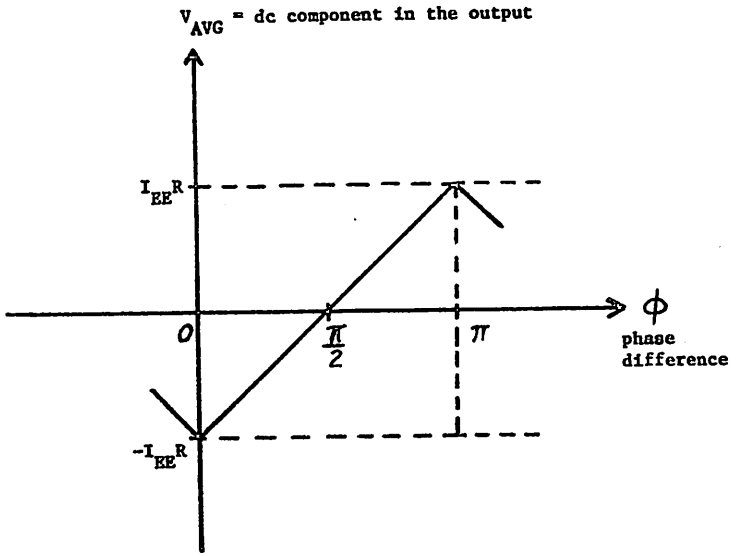


Figure 5.39 Output of the phase detector versus phase difference.

CHAPTER 6

EXPERIMENTAL RESULTS

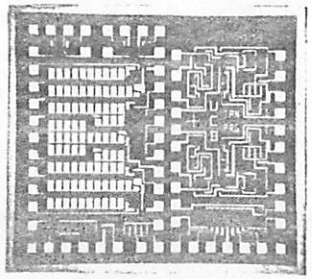
6.1. Introduction

Practical considerations for the design of an active-ladder filter has been described in Chapter 5. Computer simulation has shown that it is possible to implement this filter on a single I.C. chip. For experimental evidence of this, the integrator of Figure 5.27 has been fabricated as an integrated circuit at the University of California, Berkeley. A complete fifth-order active-ladder filter system was then constructed using these precision monolithic integrators as building blocks. The measurements performed on this experimental filter system and the results obtained will be described.

6.2. Experimental I.C. Description

A photograph of the experimental I.C. chip is shown in Figure 6.1. The overall chip size is 90 x 100 mils including the pads. A 10 um minimum feature size and a 5 um minimum alignment tolerance were used. In this chip, there are two identical integrators with each realized in a silicon area of 850 mil^2. Also, there are seven ratioed MOS capacitors of values ranging from 15 to 30 pF. These capacitors will be used to realize integrators with

(a)



(b)

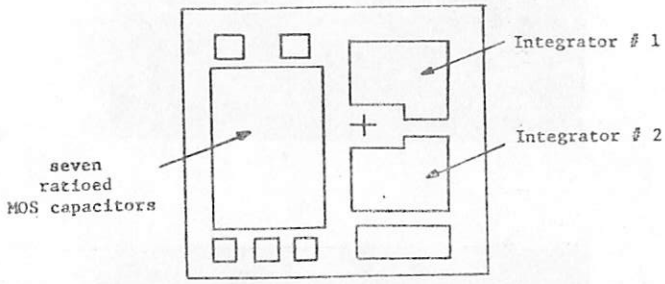


Figure 6.1 (a) A photograph of the experimental I.C.
(b) The layout block diagram of (a).

different gain-constants.

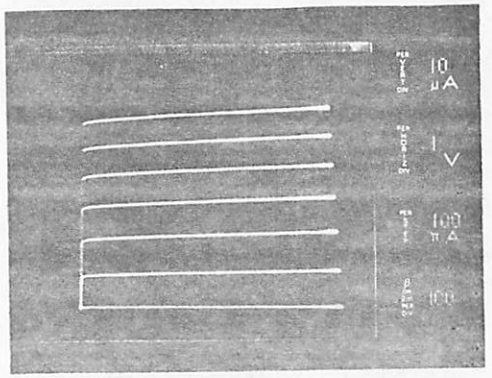
A bipolar compatible ion-implanted JFET process has been used. The process is similar to a standard bipolar process, with the addition of two ion-implantation steps. The first implant (boron) is used to create the channel, while the second implant (phosphorous) is used to realize the top gate of the JFET transistors. The JFET pinch-off voltage is designed to be 4 volts.

During the fabrication process, the n^+ buried layer step, which is typically used to reduce the collector and gate resistances, was intentionally omitted. This is possible because the monolithic integrator will be operated at low frequency where the effects of collector and gate resistances are negligible. Computer simulation of this circuit also indicated that it is not necessary to have the n^+ buried layer at the frequency range of interest. However, the n^+ buried layer should be used if the circuit is to be operated at higher frequency where the effects of phase error are significant.

6.3. Transistor Characteristics

Several NPN and JFET test devices were incorporated in the I.C. die. Figure 6.2(a) shows the measured collector current-voltage characteristics of a NPN transistor. As seen from this photo, the forward current gain of

(a)



(b)

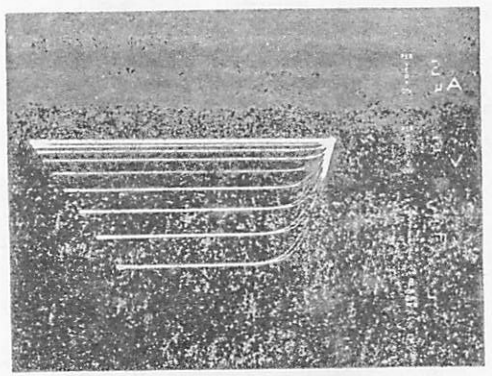


Figure 6.2 (a) NPN transistor characteristics

(b) P-channel JFET transistor characteristics

the transistor at I_c = 10 uA is approximately 120. The drain current-voltage characteristics of a P-channel JFET with Z/L=1/7 is shown in Figure 6.2(b). It is noticed that the pinch-off voltage is approximately 4 volts, and the saturation drain current, I_{dss}, is 9 uA. Both the breakdown voltages of the NPN and JFET transistors were greater than 50 volts.

Experimental data on the matching of I_{dss} were tabulated as shown in Figure 6.3. The standard deviation of the matching of I_{dss} based on a sample size of 99, is 0.2906%. This excellent matching was attributed to the accurate control of the ion-implantation steps.

6.4. Performance of Monolithic Integrators

The measured performance of the monolithic integrator agrees very well with the designed values. The DC transfer characteristic of the integrator using power supplies of ±12 volts is shown in Figure 6.4. The measured DC open loop gain is greater than 10,000. Also seen from the photo, the negative rail of the output is clamped to approximately -4.5 volts, which agrees closely with the predicted $-(V_{EE} - 2V_p)$ = -4.0 volts.

Both the measured power-supply-rejection ration (PSRR) and the common-mode-rejection ratio (CMRR) are 70 dB. The nominal unity-gain bandwidth using a 20 pF

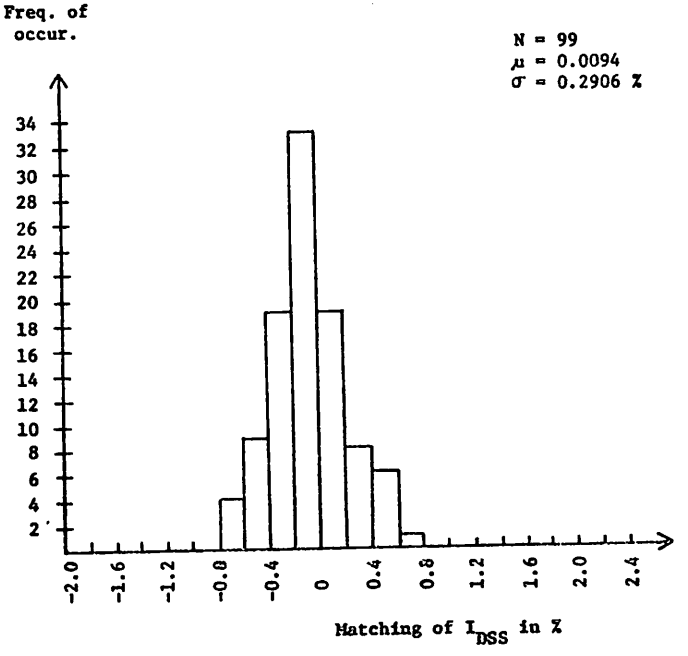


Figure 6.3 Distribution of the matching of I_{DSS}. N is the sample size, μ is the mean and σ is the standard deviation.

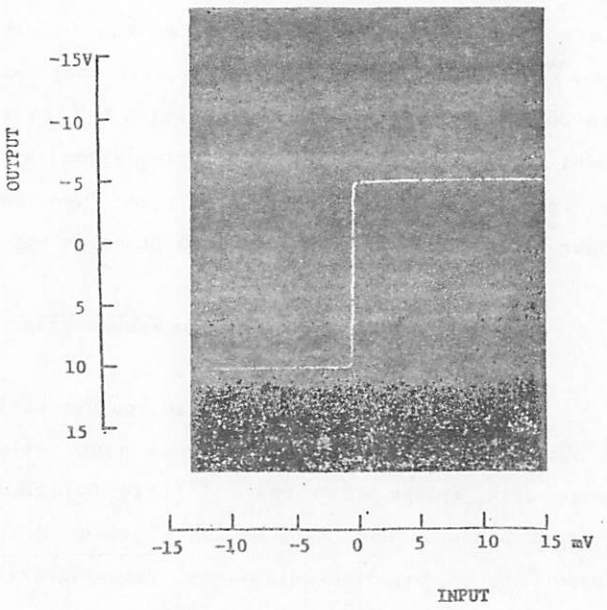


Figure 6.4 DC transfer curve of the integrator.

integrating capacitor is 7 kHz. The slew rate using a 20 pF integrating capacitor is 0.5 V/usec. The total power dissipation for each integrator is only 4 mW.

Realization of high-order filters requires precision ratio-matched integrators. The ratio-matching of integrators depends on the ratio-matching of G_m and C_c. Thus, the experimental data on the matching of G_m and C_c are tabulated as shown in Figures 6.5 and 6.6. Based on a sample size of 43, the standard deviation of the matching of MOS capacitors was 0.2424 % for this process, and the standard deviation of G_m based on 94 samples, was found to be 0.7468 %. Since these two parameters are uncorrelated, the standard deviation of the ratio-matching of monolithic integrators is $(0.7468^2+0.2424^2)^{1/2} = 0.7852$ %. This excellent matching of G_m will introduce a worst case deviation of less than 0.05 dB in the passband magnitude response of the fifth-order lowpass filter, as discussed in section 5.2.1.

The distribution of the input offset voltages is shown in Figure 6.7. Based on a sample size of 116, the mean was 20.18 mV, and the standard deviation was found to be 16.28 mV. Table 6.1 summarizes the performance of the monolithic integrator.

6.5. Performance of the Fifth-Order 8 kHz Lowpass Filter

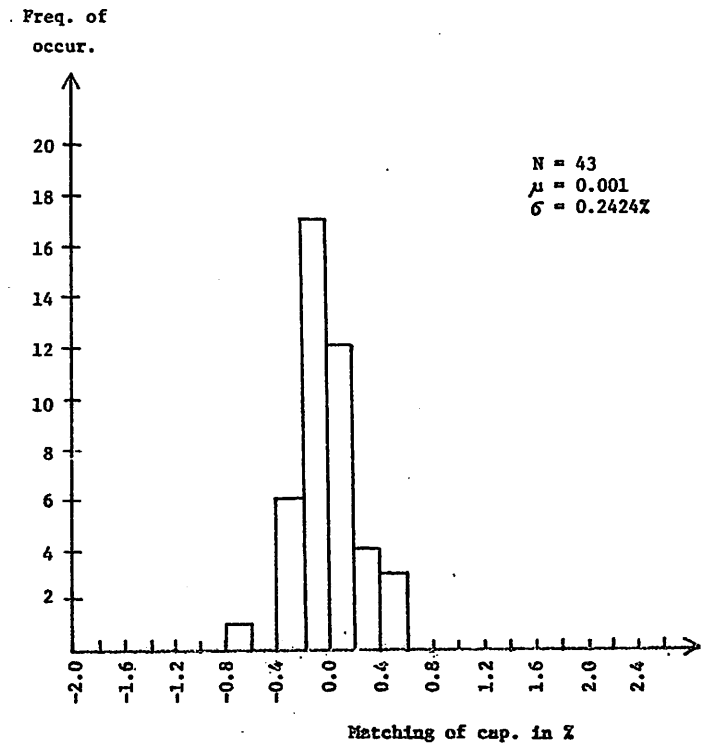


Figure 6.5 Distribution of the matching of capacitors.

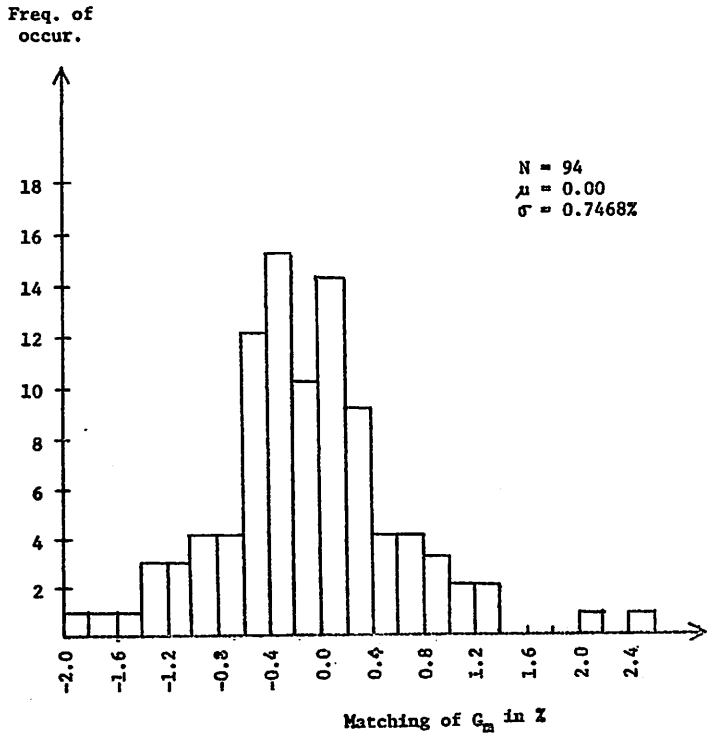


Figure 6.6 Distribution of the matching of G_m.

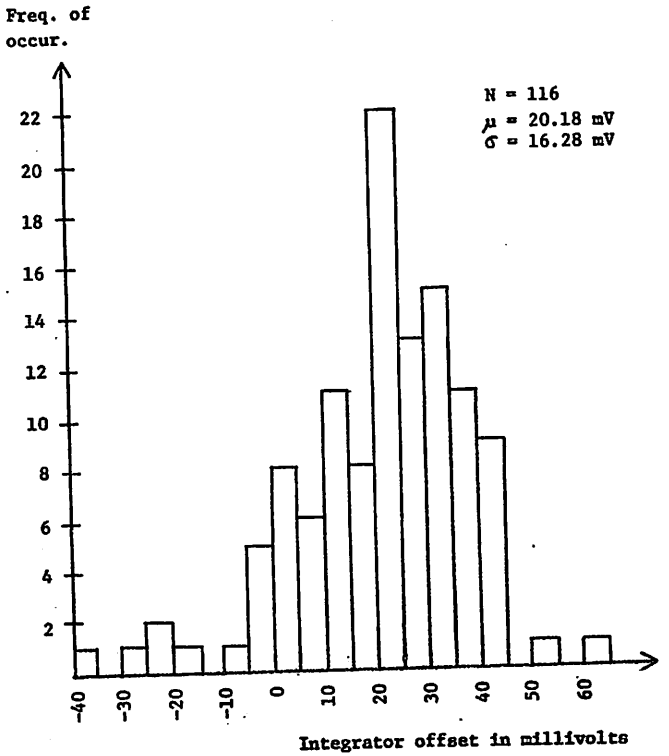


Figure 6.7 The distribution of the input offset voltages of monolithic integrators.

TABLE 6.1

INTEGRATOR PERFORMANCE DATA

Power supplies	±12V
DC open loop gain	> 10,000
CMRR, PSRR (DC)	70 dB
Nominal unity gain BW (with 20pF integrating cap.)	7 kHz
Slew rate (20pF integrating cap.)	0.5 V/usec
Input offset voltage (standard deviation)	16 mV
Power dissipation	4 mV
Chip area (excluding integrating cap.)	850 mil^2

The monolithic integrators described earlier have been used in a 'leapfrog' or active-ladder configuration to construct a fifth order 8 kHz Chebyshev lowpass filter with 0.1 dB passband ripple.

A total of seven integrators are required to realize the fifth-order all-pole filter, as shown in Figure 6.8. Two integrators are used in the VCO and five integrators are used in the filter section. The phase detector circuit of a commercial PLL I.C. (LM565) has been used in the experimental prototype. Also, a simple loop filter was designed using a lag network (with R=22 kilo-ohm and C=910 pF). However, this loop filter can be designed using an additional monolithic integrator if necessary. The estimated area to fully integrate this complete fifth-order filter system using the process described would be 10,000 sq. mils, and the total power dissipation would be approximately 50 mW.

The performance of the VCO agrees very closely with the design values. The output sinusoidal waveform was 8 Vp-p and the distortion was 1%.

The measured frequency response of the fifth-order lowpass filter is shown in Figure 6.9. The reference level of 0 dB corresponds to 0 dB insertion loss through the filter. Notice that this active-ladder filter has a 6 dB insertion loss. This is a characteristic of the

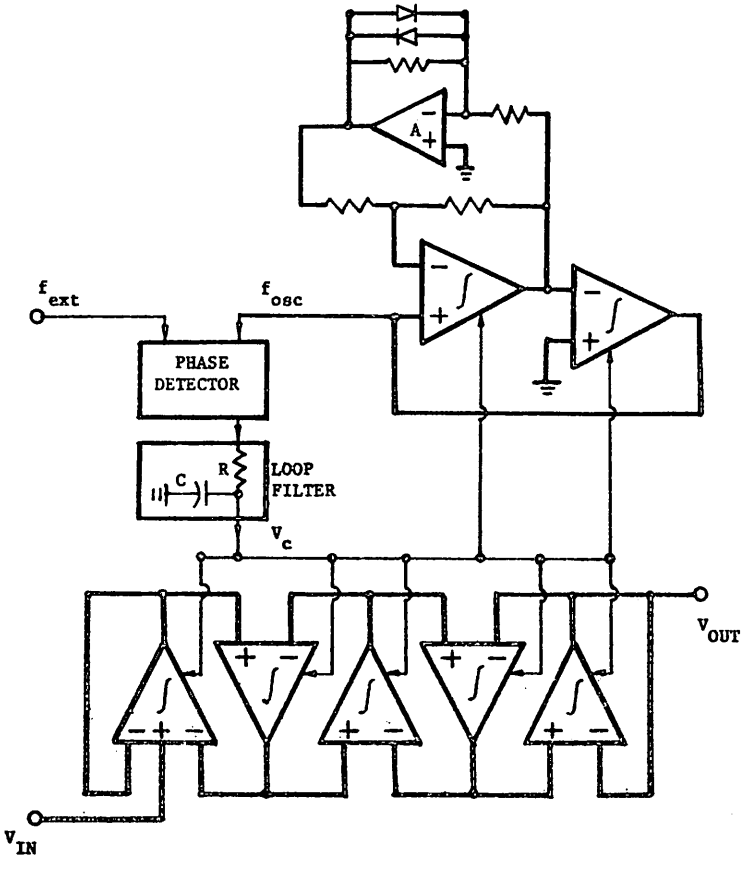


Figure 6.8 Block diagram of the fifth-order active-ladder all-pole filter.

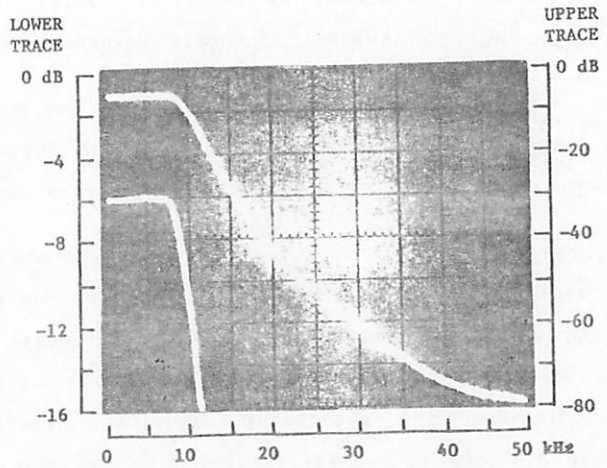


Figure 6.9 Measured frequency response of the fifth-order filter.

doubly-terminated ladder network from which the active-ladder filter was derived. The measured passband ripple is 0.1 dB to within 0.05 dB, and the cutoff frequency is 8 kHz. By varying the external clock frequency, the cutoff frequency of the filter can be varied over a range of 6 kHz to 10 kHz. The measured frequency response over a wider frequency range is shown in Figure 6.10. Notice that the stopband rolloff is approximately 100 dB/decade and the filter is performing well into the 200 kHz range without any aliasing problem. These measured data were obtained without any external trimming operations, and they agree very well with the expected design values.

A change of 50° in ambient temperature resulted in a passband deviation of 0.05 dB and a cutoff frequency variation of 1%. It should be noted that these results were obtained on a breadboarded filter system which consists of several packages of monolithic integrators. It is believed that for a fully integrated filter system, the sensitivity due to temperature variation will be very much reduced.

The filter is relatively insensitive to power supply variations. A 20 % variation in the power supply introduced less than 0.02 dB change in the passband of the magnitude response.

To determine the dynamic range of this fifth-order

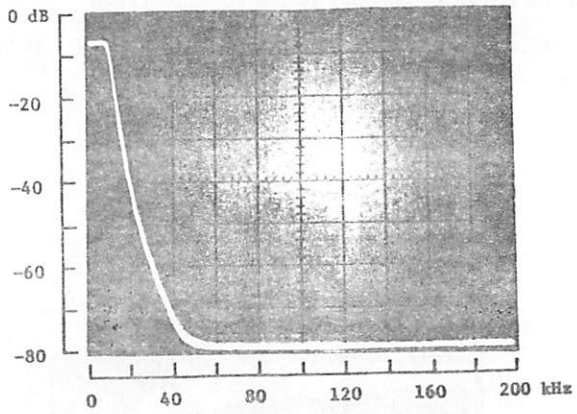


Figure 6.10 Measured frequency response of the filter over a wide frequency range.

filter, it is necessary to evaluate the noise and distortion performances of the filter. The noise spectral density (with 300 Hz bandwidth) is shown in Figure 6.11. Notice that the scale has been increased by 30 dB. Also shown in this figure is the frequency response of the filter. It is noticed that the noise spectral density peaks up near the band-edge of the lowpass filter. The measured output noise of the filter, in the frequency band of 100 Hz to 10 kHz is 200 uV_{rms}.

The measured total-harmonic-distortion (THD) of output at 1 kHz signal frequency is shown in Figure 6.12. As seen from this figure, when the output voltage is 7.5 Vp-p, the THD is only 0.3%. When the output is increased to 10 Vp-p, the measured THD is increased to 1%.

Based on the 1% THD output and the 200 uV_{rms} noise level, the dynamic range of the filter is found to be 85 dB. However, as the signal frequency is increased, the dynamic range of the filter decreases. The measured dynamic range of the 8 kHz filter as a function of signal frequency is shown in Figure 6.13. Notice that at the band-edge of the filter, the dynamic range is reduced to 76 dB. Table 6.2 summarizes the performance of this fifth-order lowpass filter.

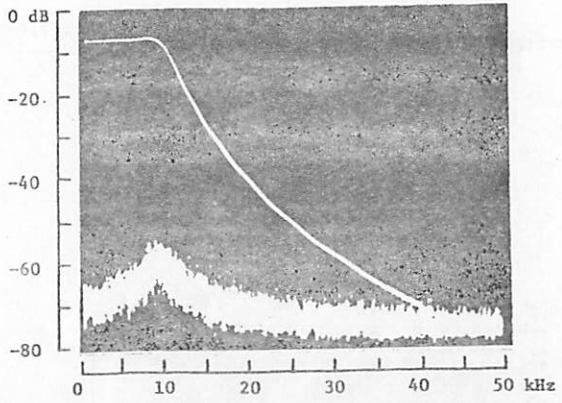


Figure 6.11 Frequency response and noise spectral density (amplified by 30 dB) of the lowpass filter.

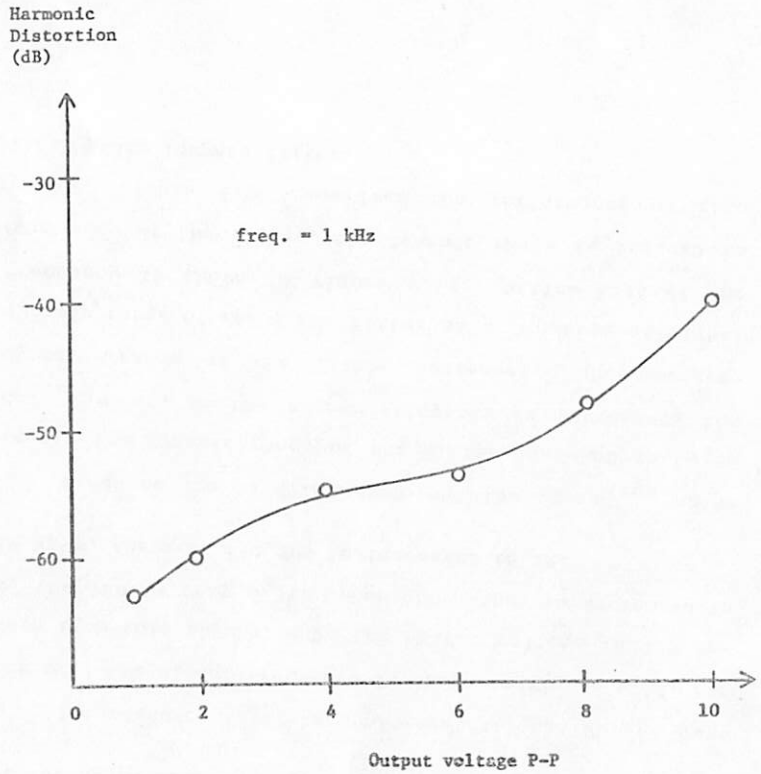


Figure 6.12 Measured harmonic distortion of the fifth-order lowpass filter at a signal frequency of 1 kHz.