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SYNTHESIS OF PIECEWISE-LINEAR NETWORKS

by

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# SYNTHESIS OF PIECEWISE-LINEAR NETWORKS<sup>†</sup>

L. O. Chua and S. Wong<sup>††</sup>

## ABSTRACT

Systematic methods for synthesizing nonlinear networks having a prescribed scalar or multi-dimensional piecewise-linear function are described. In the scalar case, precision active circuit building blocks using OP AMPs, transistors, diodes, and resistors are given for realizing piecewise-linear driving-point (DP) and transfer characteristic (TC) plots. In the multi-dimensional case, methods are given for realizing a multi-terminal nonlinear network having a multivalued piecewise-linear transfer function. Finally, these methods are generalized for synthesizing nonlinear n-ports having a prescribed multi-dimensional piecewise-linear driving-point function.

Although most of the basic building blocks are grounded active networks, converter networks are developed for transforming such grounded networks into floating networks having the same properties. By slight modifications of these converter networks, other useful conversion properties are also presented.

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## I. Introduction

One of the most basic problems in nonlinear network synthesis is the realization of driving-point and transfer characteristic plots, henceforth abbreviated DP and TC plots, respectively. Two basic approaches have been developed. One involves a piecewise-linear approximation [1], while the other involves a rational function approximation [2]. The first approach uses linear resistors, diodes, zener diodes and constant current diodes as basic building blocks, while the second method utilizes four-quadrant voltage multipliers. Both methods are quite sensitive to element parameter variations and both require careful adjustments. The piecewise-linear approach does not allow DP plots containing negative resistance segments unless transistors or other active elements are used. The rational function approach is quite elegant but it too suffers from several limitations. One of these being that it is generally much more expensive and sensitive if the DP plot involves rapid changes in slopes. Moreover, unlike the piecewise-linear approach, jump discontinuities cannot be allowed.

Several recent works [3-9] are aimed at improving and generalizing the above cited methods. Each of these works offers some interesting new approaches and ideas for synthesizing nonlinear networks. This paper represents a further contribution in this area. The methods to be presented in this paper may be considered as refinements and generalizations of the piecewise-linear approach. Using OP AMPs, transistors, diodes, and resistors as our building blocks, we are able to develop a family of precision piecewise-linear circuits which are inexpensive and easy to build. Moreover, all of these circuits are compatible with current integrated circuit technology and can therefore

be made in module form. We first develop basic circuit building blocks for realizing a prescribed piecewise-linear DP or TC plot which may contain segments with negative slopes, as well as jump discontinuities. These circuits are all in grounded form. Since many practical applications require floating circuits, we develop the concept of converter circuits so that any grounded circuit may be transformed into a floating circuit. This important technique was implemented by OP AMP circuits and the experimental results agree remarkably well with theoretical predictions. By a slight modification of these basic converter circuits many additional useful properties can also be implemented. For example, it is possible to transform a DP plot into a TC plot, and vice-versa, using the appropriate type of converters.

The preceding techniques and concepts are further generalized for synthesizing a multi-terminal nonlinear network having a prescribed multi-dimensional driving-point or transfer characteristic. In other words, a general technique for synthesizing piecewise-linear n-ports is also obtained.

## II. Synthesis of Piecewise-Linear Driving-Point Characteristics

Three basic elements are useful in the synthesis of voltage-controlled piecewise-linear DP plots: 1) The positive concave resistor characterized by

$$i = 0 \quad , \quad v \leq E$$

$$i = (v-E)/R, \quad v \geq E$$

where  $E$  is any constant voltage and  $R$  is positive; 2) the negative concave resistor which is similarly characterized except that  $R$  is negative; and 3) the step current source characterized by

$$i = 0, \quad v < E$$

$$i = I, \quad v > E$$

where  $E$  and  $I$  are constants. The  $v$ - $i$  characteristic of these elements are shown in Figs. 1(a), (c), and (e), along with basic circuit realizations shown in Figs. (b), (d) and (f), respectively. Notice that the OP AMP circuits shown in Fig. 1 are grounded one-ports. Any prescribed voltage-controlled piecewise-linear DP plot can be realized by connecting these basic elements in parallel. Current-controlled DP plot can also be realized by connecting a "dual" voltage-controlled element across port 2 of a gyrator [1].

Consider first the positive concave resistor shown in Fig. 1(b). Observe that diode  $D_1$  is off and hence  $i = 0$  for  $v \leq E$  where  $E = -E_S R_2 / R_1$  is the output voltage of the voltage source.<sup>1</sup> With the voltage  $E_S$  chosen to be the positive or the negative power supply of the OP AMP, the magnitude and the accuracy of  $E$  depend only on the ratio of the resistors  $R_1$  and  $R_2$ . For all  $v \geq E$ ,  $D_1$  is on and thus  $i = (v-E)/R$ . The slope of the  $v$ - $i$  characteristic is thus controlled by  $R$ . Observe that the diode  $D_1$  can be included in the integrated OP AMP  $A_2$  without additional cost. Consider next the negative concave resistor shown in Fig. 1(d). For  $v \leq E$ ,

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<sup>1</sup>The voltage source is simulated by the OP AMP circuit consisting of  $A_1$ ,  $R_1$ ,  $R_2$  and  $E_S$ . The voltage source circuit will henceforth be deleted and replaced by a box labelled "voltage source" in all subsequent circuits.

diode  $D_1$  is on and  $D_2$  is off. No current flows through  $R_4$  and hence  $v_1$  is identical to  $v$ . There is no voltage drop across  $R$  and  $i = 0$ . When  $v \geq E$ ,  $D_1$  is off and  $D_2$  is on, then  $v_1 = (v-E)R_4/R_3 + v$  and  $i = -(v-E)R_4/R_3R$ . The circuit thus behaves like a negative resistor of  $-RR_3/R_4$  Ohms. The ratio  $R_4/R_3$  should be about 0.1 so that the input dynamic range of the circuit will not be decreased substantially. The entire circuit except the resistors can be integrated into a single chip. It is interesting to observe that negative  $R$ ,  $L$ ,  $C$  elements can also be realized by slight modifications of this circuit.<sup>2</sup>

Consider next the step current source shown in Fig. 1(f). The open loop OP AMP  $A_2$  provides the step jump characteristic. With  $v < E$ ,  $A_2$  will be saturated positively and  $v_1 \approx 0.7V$ . There will be no input current  $i$  if the transistor is kept out of the reverse active region. This condition will be achieved if the input voltage  $v$  is greater than the negative saturation output voltage of  $A_3$ , which is about  $-13.5V$ . When  $v > E$ , the Zener diode keeps the output of  $A_2$  at  $-12V$ . If the transistor has a high  $\beta$ , the input current will be  $i = 2\beta/(\beta+1)R \approx 2/R$ . In this case, the input voltage should be higher than  $-10V$  in order to keep the transistor in the forward active region. The common base configuration of the transistor and the feedback provided by  $A_3$  keep the current  $i$  quite constant regardless of the input voltage  $v$ . The current step magnitude is determined by the Zener diode and the resistor  $R$  assuming that  $-10V$  can be accurately obtained. The exactness of the step magnitude can be improved if a step voltage source to be discussed in the next section is used instead of the

<sup>2</sup>In the negative concave resistor, if  $D_1$  is deleted,  $D_2$  is replaced by short circuit and  $E = 0$ , the resulting circuit behaves like a grounded negative resistor of  $-RR_3/R_4$  Ohms. Moreover, with  $R$  replaced by  $L$  or  $C$ , a negative inductor of  $-LR_3/R_4$  Henries, or a negative capacitor of  $-CR_4/R_3$  Farads is realized separately.

Zener diode. This basic element, excluding the resistor R, can be fabricated on a single chip. With slight modifications as discussed in the appendix, a negative step current source and a constant current source can also be realized. Notice that if the diodes in Figs. 1(b), (d) and (f) are reversed, the driving point characteristics of the resulting circuits for  $v < E$  and those for  $v > E$  will be inverted.

To verify the preceding theoretical predictions and the practicality of our synthesis approach, a circuit was assembled to realize the driving-point characteristic shown in Fig. 2(a). This highly nonlinear curve can be decomposed as a sum of the six basic curves shown in Figs. 3(a) through (f). Six corresponding basic elements are realized with their performance shown in Figs. 3(g) through (l). By connecting all these elements in parallel, the  $v$ - $i$  characteristic shown in Fig. 2(b) is obtained. The sharpness and the exactness of the resulting curves demonstrate that our basic circuit building blocks are indeed easily adjusted and implemented.

### III. Synthesis of Piecewise-Linear Voltage Transfer Characteristics

For the synthesis of piecewise-linear voltage transfer characteristics, only two basic elements are required: 1) a concave transfer function characterized by

$$v_0 = 0 \quad , \quad v \leq E$$

$$v_0 = m(v-E), \quad v \geq E$$

where  $m$  and  $E$  are positive or negative constants, 2) a step transfer function characterized by

$$v_0 = 0, \quad v < E$$

$$v_0 = kE, \quad v > E$$

where  $k$  is a constant.

A practical realization of the concave transfer function is shown in Fig. 4(b). When  $v \leq E$ , diode  $D_1$  is off and we have  $v_1 = E$ , and  $v_0 = 0$ . When  $v \geq E$ ,  $D_1$  is on and we have  $v_1 = v$  and  $v_0 = (v-E)R_6/R_4$ . The value of  $R_3$  is unimportant and hence can be included in the integrated circuit. The unity gain amplifier  $A_3$  prevents loading at the inverting input of  $A_2$ . If the connections of  $v_1$  and  $E$  to the summing circuit are interchanged, a negative  $m$  is obtained. In addition, the summing circuit is shared by every basic element. A step transfer function realization is shown in Fig. 4(d). When  $v < E$ ,  $A_2$  is saturated negatively and  $v_1 \approx -(0.7+E_Z)$ , where  $E_Z$  is the Zener breakdown voltage of the Zener diode. The exact value of  $E_Z$  is immaterial as long as it is larger than  $-E$ . This Zener diode is included to ensure that when  $v < E$ ,  $v_1$  is within the input dynamic range of  $A_3$  and  $A_4$ . Under these conditions, diodes  $D_2$  and  $D_3$  are both on, hence  $v_2 = v_3 = v_1$  and  $v_0 = 0$ . When  $v > E$ ,  $A_2$  is saturated positively and  $v_1 \approx 14V$ . Diodes  $D_2$  and  $D_3$  are both off, hence  $v_2 = 0$ ,  $v_3 = E$  and  $v_0 = kE$ . The connections of  $v_2$  and  $v_3$  to the summing circuit determine the sign of  $k$ . Notice that the circuits shown in Fig. 4 are grounded networks. Just as before, reversing the diodes in these circuits simply inverts the transfer characteristics for  $v < E$  and those for  $v > E$ . Except for the resistors in the summing circuit and the voltage

source, each circuit in Fig. 4 can be integrated into a single chip. In addition, this type of circuit presents essentially no loading to the input signal voltage  $v$ .

An absolute value circuit was built to demonstrate the practicality of this approach. The circuit shown in Fig. 5(a) is characterized by  $v_0 = |v-E|$  where  $E$  represents a shift of the origin. With  $E$  chosen arbitrarily to be 2 volts, the resulting voltage transfer characteristic is shown in Fig. 5(b). This absolute value circuit will be used later as a key element in the realization of multi-dimensional piecewise-linear functions.

#### IV. Synthesis of Characteristic Converters

##### A. Grounded-to-Floating DP Plot Converter

The method for synthesizing piecewise-linear DP plots discussed previously realizes only grounded one-ports; even though floating one-ports are usually required in practice. The circuit shown in Fig. 6(a) transfers the  $v$ - $i$  characteristic of the grounded piecewise-linear resistor  $R$  to that of the floating input port.<sup>3</sup> Assuming that  $v_1$  and  $v_2$  are the voltage levels with respect to ground at the two input nodes, then the output of OP AMP  $A_3$  with respect to ground is  $v_3 = v_1 - v_2 = v$ . This voltage level is applied to  $R$  and the current through  $R$ ,  $i_R = R(v)$ , is sensed by  $R_4$  such that  $v_4 = R_4 R(v) + v$ . Accordingly,  $v_5 = v_1 - R_4 R(v)$  and the input current at node 1 is  $i = R(v)$ . Similarly, the output current at node 2 is  $i = R(v)$ . The only restriction on this circuit is that  $v_1$  through  $v_6$  must be within the input or output dynamic range of the OP AMPs. To demonstrate the operation of this circuit, the grounded

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<sup>3</sup>In general, any grounded voltage-controlled nonlinear resistor can be used.

piecewise-linear resistor realized in Fig. 2 is chosen for  $R$ . When  $v_2$  is biased at 1 volt, the  $v$ - $i$  characteristic of input node 1 is shown in Fig. 6(b). Fig. 6(c) is a plot of the input current at node 2 versus the input voltage at node 1.

#### B. Grounded-to-Floating TC Plot Converter

The floating network shown in Fig. 7 has a voltage TC plot identical to that of the grounded piecewise-linear transfer function.<sup>4</sup>  $A$  is a differential-input differential-output unity-gain amplifier. Again, the voltages at all internal nodes with respect to ground must be restricted to the input or output dynamic range of the OP AMPs.

#### C. DP Plot-to-TC Plot Converter

The circuit shown in Fig. 8 exhibits a  $v_0$ -vs.- $v$  voltage TC plot in the same form as the DP plot of the nonlinear resistor  $R$ . The operation of this circuit is similar to that of the grounded-to-floating DP plot converter. The differential input signal  $v$  is converted to a grounded signal and is applied to  $R$ . The current-flowing through  $R$ ,  $i_R = R(v)$ , is sensed by  $R_1$  and hence  $v_0 = R_1 R(v)$ .

#### D. TC Plot-to-DP Plot Converter

The converter circuit shown in Fig. 9 converts a prescribed voltage TC plot to a similar DP plot at the input port. This circuit works just like the grounded-to-floating DP plot converter discussed earlier. If the voltage TC plot is expressed as  $f(v)$ , the DP plot measured across the input port will be given by  $i = f(v)/R_3$ .

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<sup>4</sup>This transformation property is of course valid regardless of whether the TC plot is piecewise-linear, or not.

## V. Synthesis of Multi-Dimensional Piecewise-Linear Transfer Functions

It was shown in [10-11] that any multi-dimensional piecewise-linear function can be globally represented as a sum of linear function, absolute value functions and step functions; namely

$$v_0 = a_0 + a_1^T v + \sum_{i=1}^n [g_i |\alpha_i^T v - \beta_i| + h_i \operatorname{sgn}(\alpha_i^T v - \beta_i)]$$

where  $v$  is the input voltage vector;  $a_0$ ,  $g_i$ ,  $h_i$ ,  $\beta_i$  are scalar constants and  $a_1$ ,  $\alpha_i$  are constant vectors. A general circuit configuration for simulating this expression is shown in Fig. 10.<sup>5</sup> As an example, the two-dimensional piecewise-linear function shown in Fig. 11(a) is described by six affine equations for the six regions defined by the three straight line boundaries. Theoretically, this function exhibits the families of transfer curves shown in Figs. 11(b) and (c). Using the preceding general formula, the coefficients associated with this function have been calculated in [11]; namely

$$v_0(v_1, v_2) = \frac{1}{2\sqrt{3}} |-\sqrt{3}v_1 + v_2| + \frac{1}{2\sqrt{3}} |\sqrt{3}v_1 + v_2| - \frac{2}{\sqrt{3}} |v_2|$$

The realization of this function is shown in Fig. 12(a). Figure 12(b) is a plot of  $v_0$  versus  $v_1$  with  $v_2$  held constant. The upper trace corresponds to  $v_2 = 0$  volt, while the lower trace is for  $v_2 = 1$  volt. Figure 12(c) is a plot of  $v_0$  versus  $v_2$  with  $v_1$  constant. The lower trace is for  $v_1 = 0$  volt whereas the upper trace is for  $v_1 = 1$  volt.

<sup>5</sup>The circuit shown in Fig. 10 is grounded. Floating network can be obtained with the inclusion of the differential-to-single-ended converter and the differential-input differential-output unity-gain amplifier.

## VI. Synthesis of Piecewise-Linear n-ports

With some modifications on the TC plot-to-DP plot converter, a piecewise-linear voltage-controlled n-port can be realized. The general method of realizing one of the input ports is shown in Fig. 13. The grounded transfer function is a multi-dimensional piecewise-linear voltage transfer function  $f(v_1, v_2, \dots, v_n)$  obtained from the prescribed driving point characteristic of input port 1,<sup>6</sup> namely

$$i_1 = f(v_1, v_2, \dots, v_n) / R_1$$

The systematic method discussed in the previous section can be used to realize  $f(v_1, v_2, \dots, v_n)$ . The same approach can, of course, be used to synthesize the remaining ports. In addition, gyrators can be connected in cascade with the input ports to realize current-controlled n-ports. In fact, by cascading the ports with appropriate types of mutators [1], even piecewise-linear n-port inductors and capacitors may be synthesized.

## VII. Conclusions

Methods of realizing any grounded or floating piecewise-linear DP plot or TC plot that includes negatively sloped segments and discontinuities are presented. A family of networks capable of transforming a prescribed DP plot into a similar TC plot, and vice versa, are discussed. Finally, the systematic methods for realizing piecewise-linear multi-dimensional

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<sup>6</sup>In general, if  $f(y)$  is an arbitrary multi-dimensional nonlinear function which is not piecewise-linear, a voltage-controlled nonlinear n-port can be similarly realized. Although there is presently no systematic way for realizing arbitrary multi-dimensional nonlinear functions which are not represented in piecewise-linear form, the approach proposed in [9] appears to be quite promising.

transfer functions, and n-ports, are presented. In addition to the accuracy and the flexibility of the basic circuit building blocks presented, these circuits are all compatible with existing integrated circuit technology. Consequently, these building blocks can all be integrated in module form. Finally, observe that since no special attention is paid to the frequency characteristic of these circuits, it can be improved with additional design efforts.

#### REFERENCES

- [1] L. O. Chua, Introduction to Nonlinear Network Theory, New York: McGraw-Hill, 1969.
- [2] N. R. Malik, G. L. Jackson and Y. S. Kim, "Theory and Applications of Resistor, Linear Controlled Resistor, Linear Controlled Conductor Networks," IEEE Trans. Circuits and Systems, vol. CAS-23, pp. 222-228, April 1976.
- [3] G. A. Nenov and H. Z. Shojlev, "Rotator and Reflector for Transfer Functions," Electronics Letters, New York: McGraw-Hill, 1969.
- [4] J. Glover, "Basic T Matrix Patterns for 2-port Linear Transformation Networks in the Real Domain," Electronics Letters, vol. 10, no. 23, November 14, 1974, pp. 495-497.
- [5] J. Glover, "Further Explanation of the Continuous Transformation Pattern on the AD-BC Plane," Electronics Letter, vol. 11, no. 4, February 20, 1975, pp. 75-76.
- [6] J. L. Heurtas, J. J. Acha and A. Gago, "New Rotator and Reflector Circuits," Proc. IEEE, vol. 65, no. 6, pp. 987-989, June 1977.
- [7] A. Chichocki, S. F. Filipowicz, and S. Osowski, "Analogue Simulation of the Nonlinear Transfer Characteristics: A Novel Approach," Electronic Circuits and Systems, January 1978, vol. 2, no. 1.
- [8] J. L. Huertas, J. I. Acha and A. Gago, "Design of General Voltage or Current Controlled Resistive Elements and their Applications to the Synthesis of Nonlinear Networks," IEEE Trans. on Circuits and Systems, submitted for publication.

- [9] J. L. Huertas, J. I. Acha and A. Gago, "Theory, Design and Applications of D-T Linear Transformation Circuits," IEEE Trans. on Circuits and Systems, submitted for publication.
- [10] L. O. Chua and S. M. Kang, "Section-Wise Piecewise-Linear Functions: Canonical Representation, Properties and Applications," Proc. IEEE, vol. 65, pp. 915-929, June 1977.
- [11] S. M. Kang and L. O. Chua, "A Global Representation of Multi-Dimensional Piecewise-Linear Functions with Linear Partitions," Proc. of the International Symposium on Circuits and Systems, New York, May 17-19, 1978.

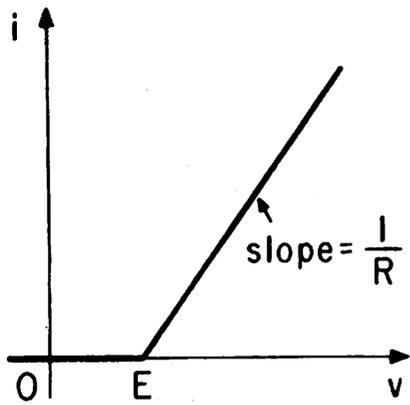
## Appendix

To obtain a negative step current source, one simply has to reverse the two terminals of the Zener diode in Fig. 1(f) and change the npn transistor into a pnp transistor as shown in Fig. A.1. Another modification of the circuit in Fig. 1(f) leads to the constant current source shown in Fig. A-2.

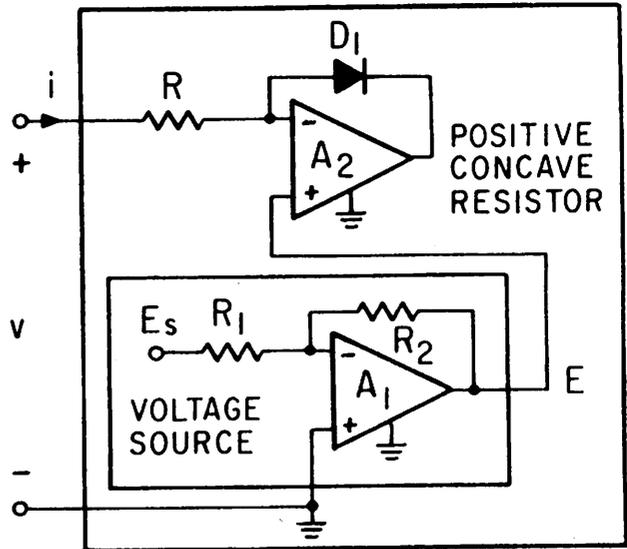
### List of Figure Captions

- Fig. 1. Basic elements for realizing piecewise-linear DP plots:  
(a)(b) Positive concave resistor. (c)(d) Negative concave resistor.  
(e)(f) Step current source.
- Fig. 2. (a) Piecewise-linear DP plot to be synthesized. (b) Experimental result (horizontal scale: 2 volts per division, vertical scale: 2 mA per division).
- Fig. 3. (a)(b)(c)(d)(e)(f) Decompositions of the piecewise-linear characteristic shown in Fig. 2(a). (g)(h)(i)(j)(k)(l) Experimental DP plots of the six basic elements (horizontal scale: 2 volts per division, vertical scale: 2 mA per division).
- Fig. 4. Basic elements for realizing piecewise-linear voltage TC plots.  
(a)(b) Concave transfer function element. (c)(d) Step transfer function element.
- Fig. 5. (a) An absolute value circuit. (b) TC plot of the circuit (horizontal scale: 2 volts per division, vertical scale: 2 volts per division).
- Fig. 6. (a) A grounded-to-floating DP plot converter. (b) DP plot at input node 1 with  $v_2$  biased at 1 volt. (c) Input current at node 2 versus input voltage at node 1, with  $v_2$  biased at 1 volt (horizontal scale: 2 volts per division, vertical scale: 2 mA per division).
- Fig. 7. A grounded-to-floating TC plot converter.
- Fig. 8. A DP plot-to-TC plot converter.
- Fig. 9. A TC plot-to-DP plot converter.

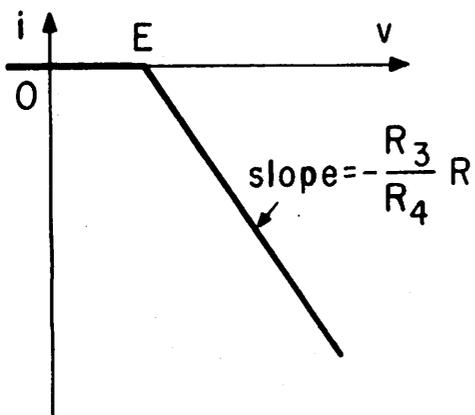
- Fig. 10. A systematic method for realizing multi-dimensional piecewise-linear transfer functions.
- Fig. 11. (a) A two-dimensional piecewise-linear transfer function to be synthesized. (b)(c) Theoretical characteristic of the function.
- Fig. 12. (a) Realization of the function in Fig. 11(a). (b) Output  $v_0$  versus input  $v_1$  with  $v_2$  held constant. (c) Output  $v_0$  versus input  $v_2$  with  $v_1$  held constant (horizontal scale: 1 volt per division, vertical scale: 1 volt per division).
- Fig. 13. General circuit configuration for synthesizing piecewise-linear voltage-controlled n-ports.
- Fig. A-1. A negative step current source.
- Fig. A-2. A constant current source.



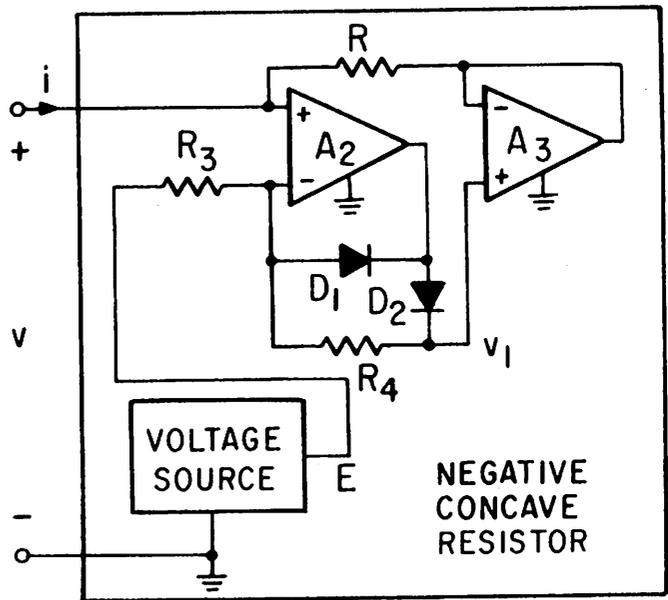
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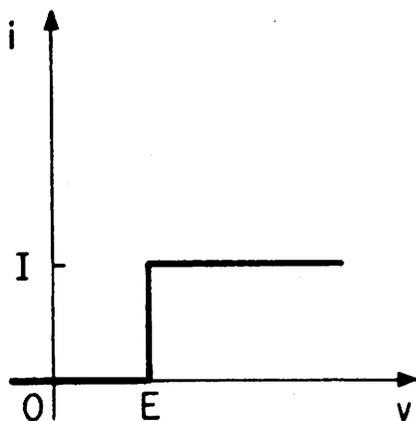
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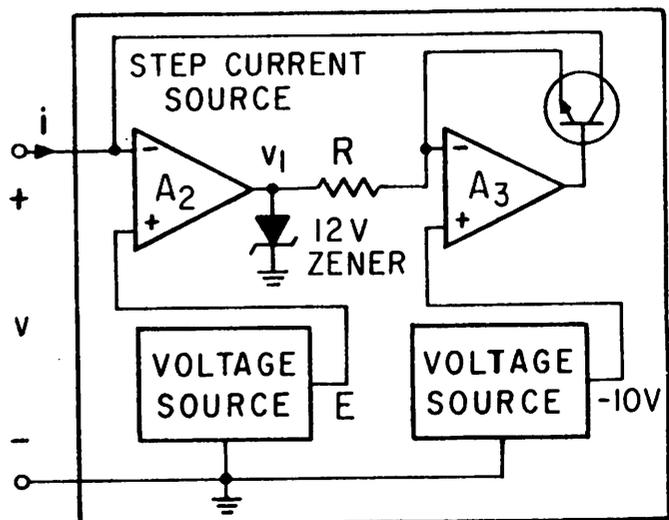
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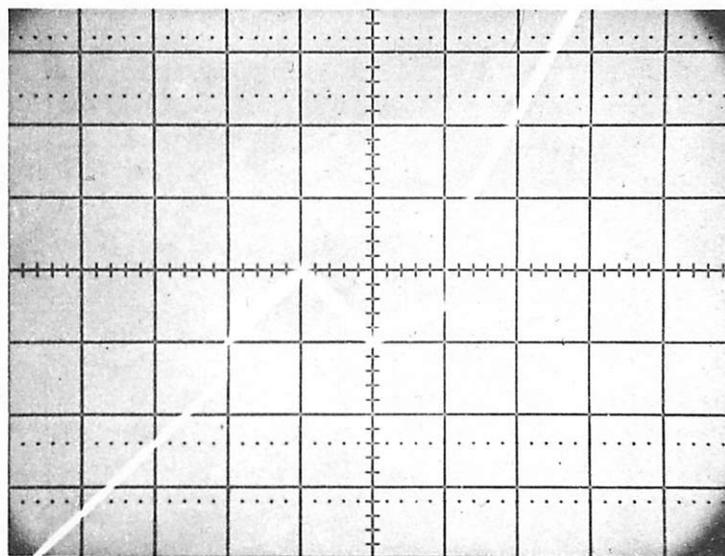
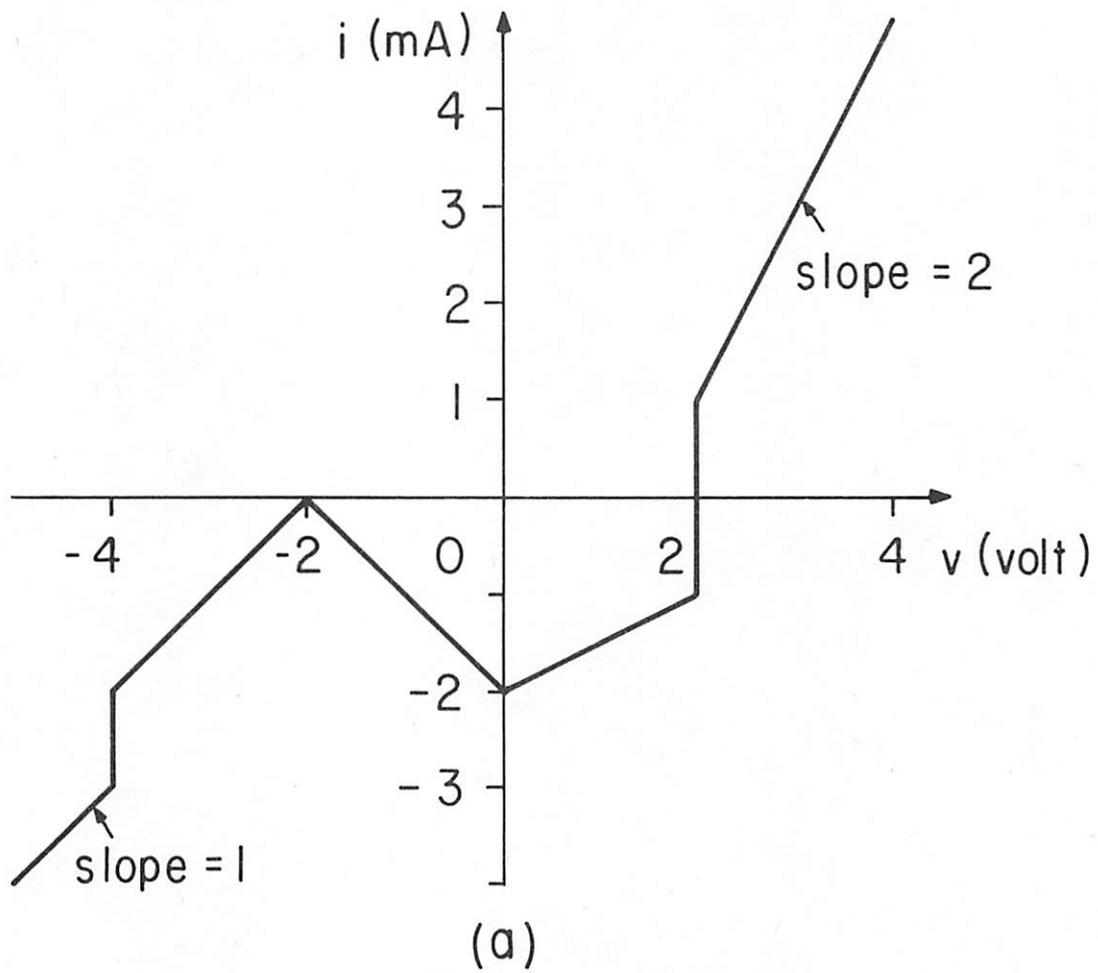


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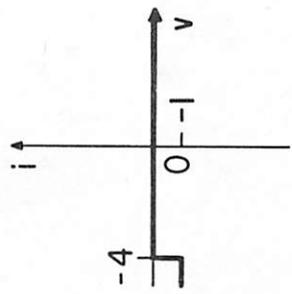
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Fig. 1

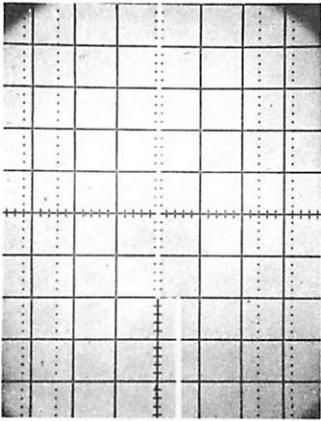


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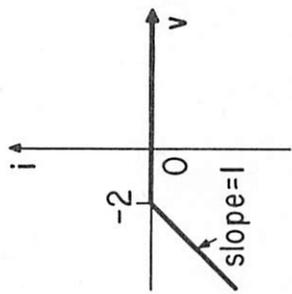
Fig. 2



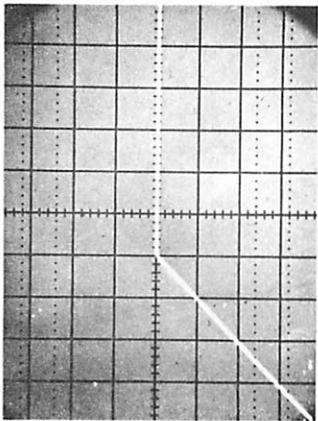
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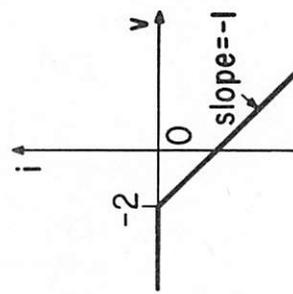
(g)



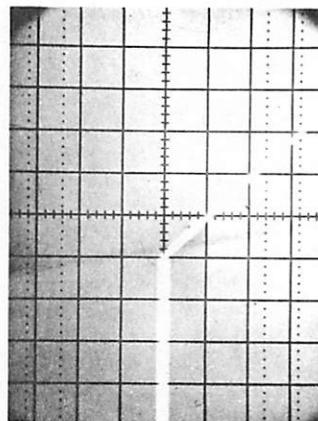
(b)



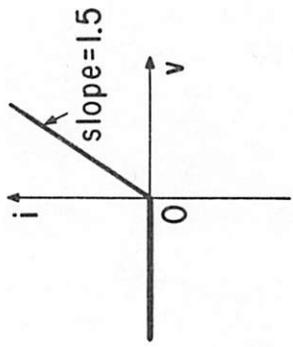
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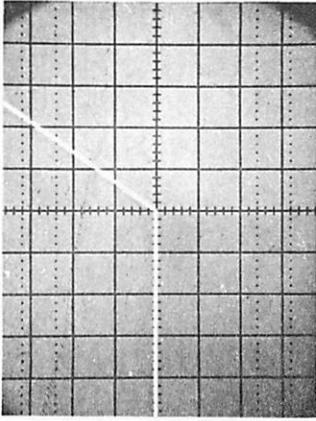
(c)



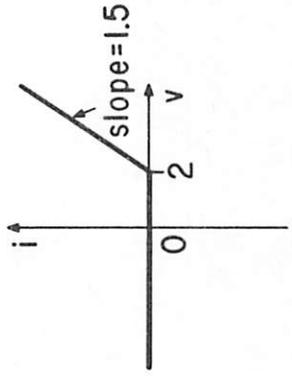
(i)



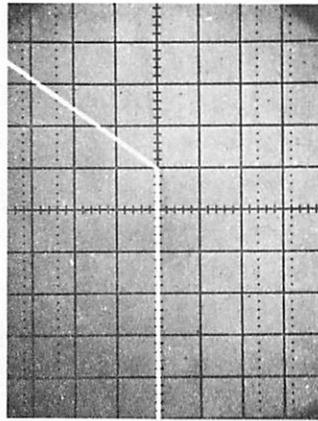
(d)



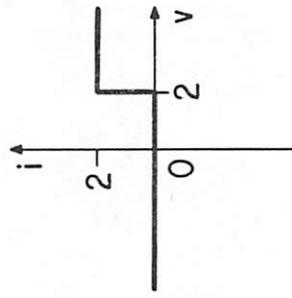
(j)



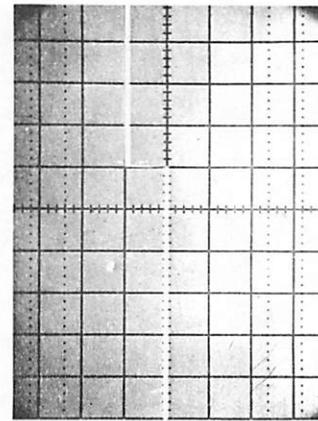
(e)



(k)

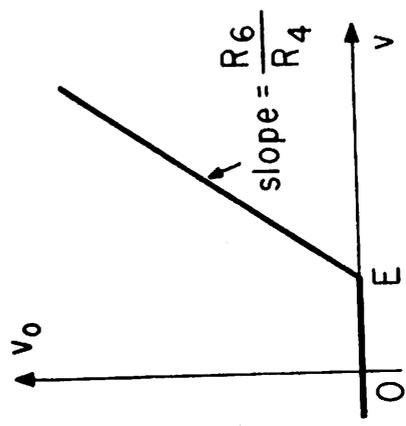
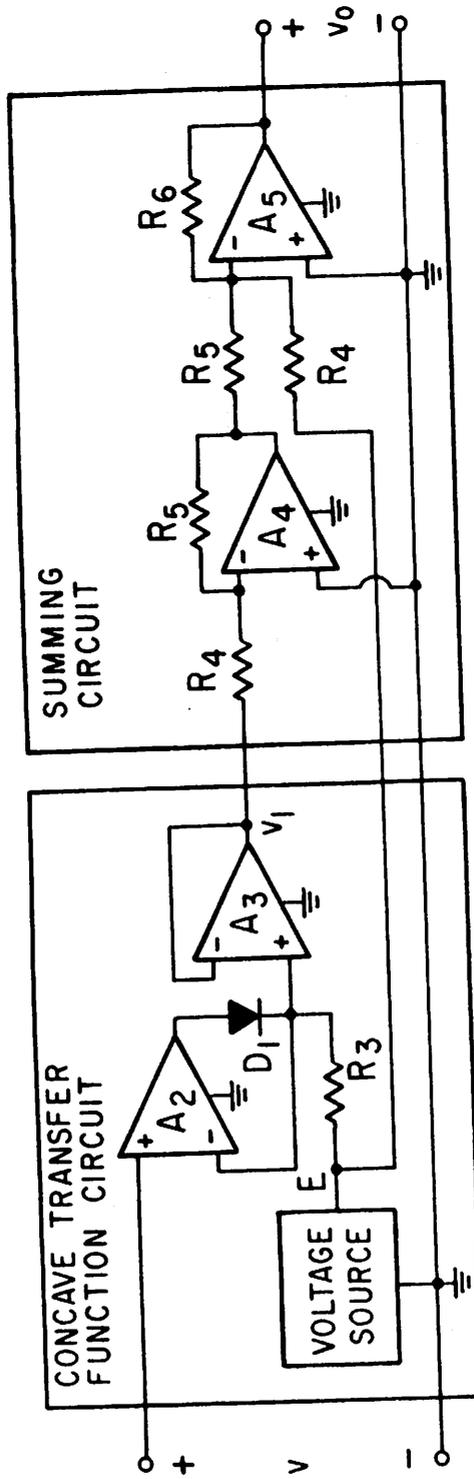


(f)

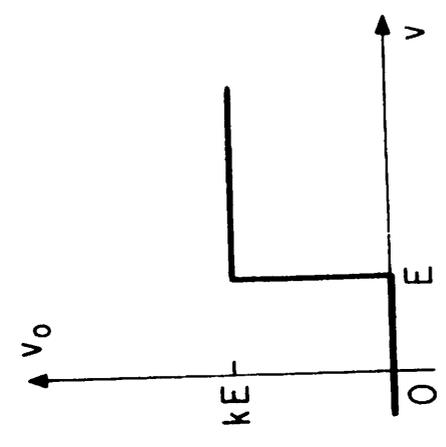
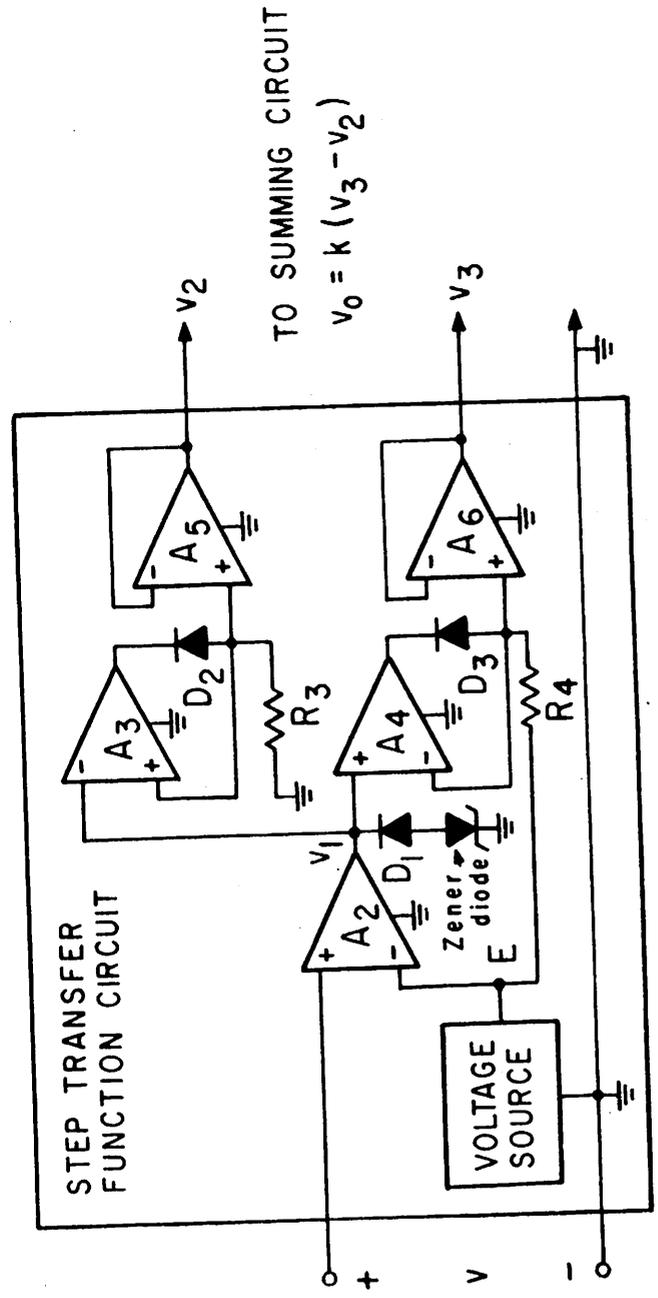


(l)

Fig. 3

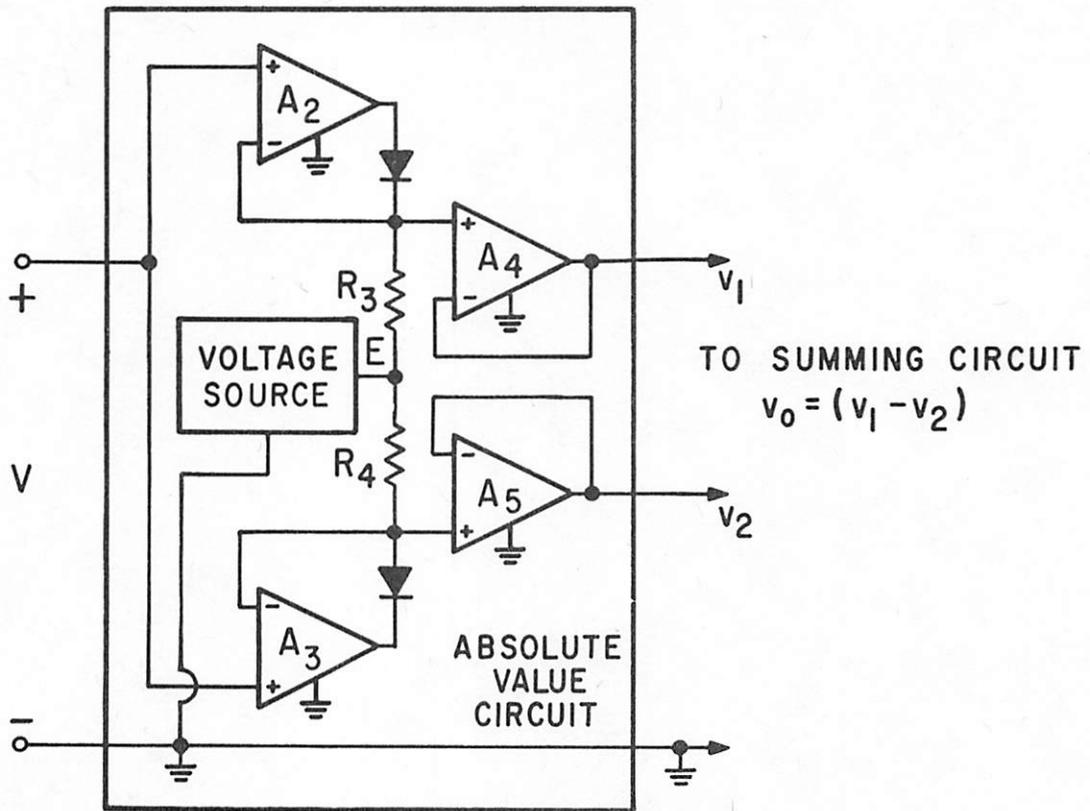


(b)

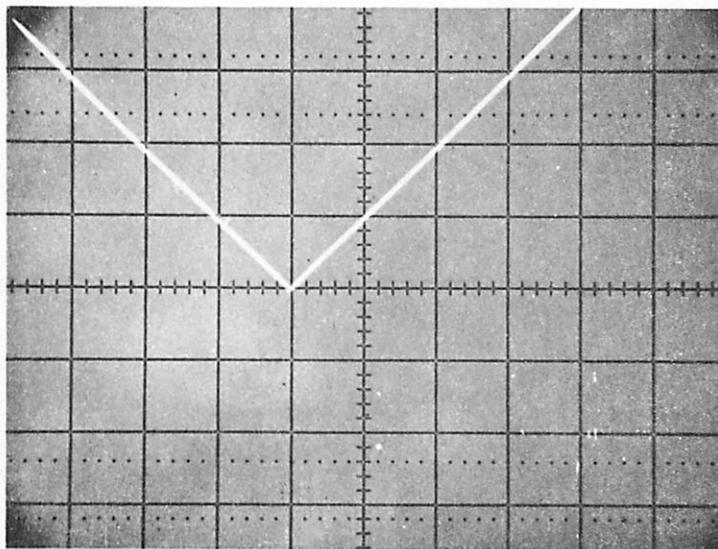


(d)

Fig. 4

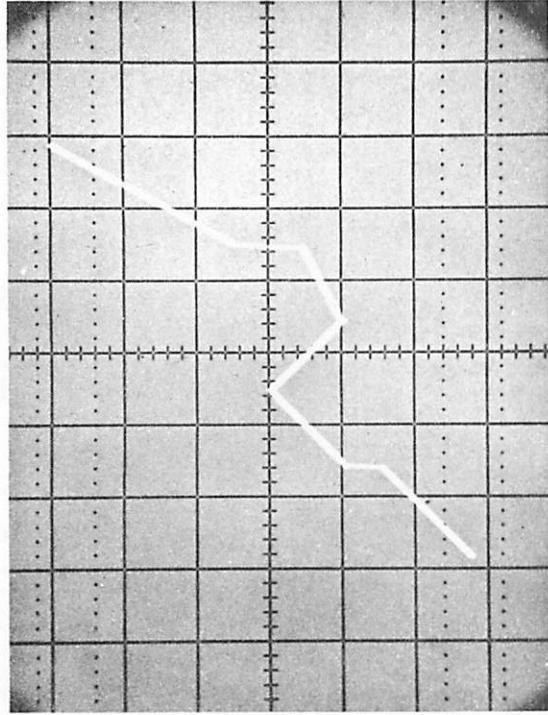


(a)

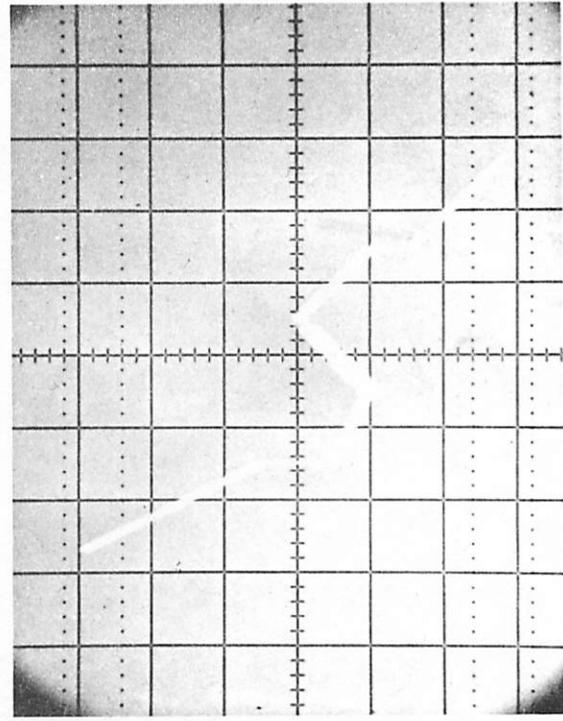


(b)

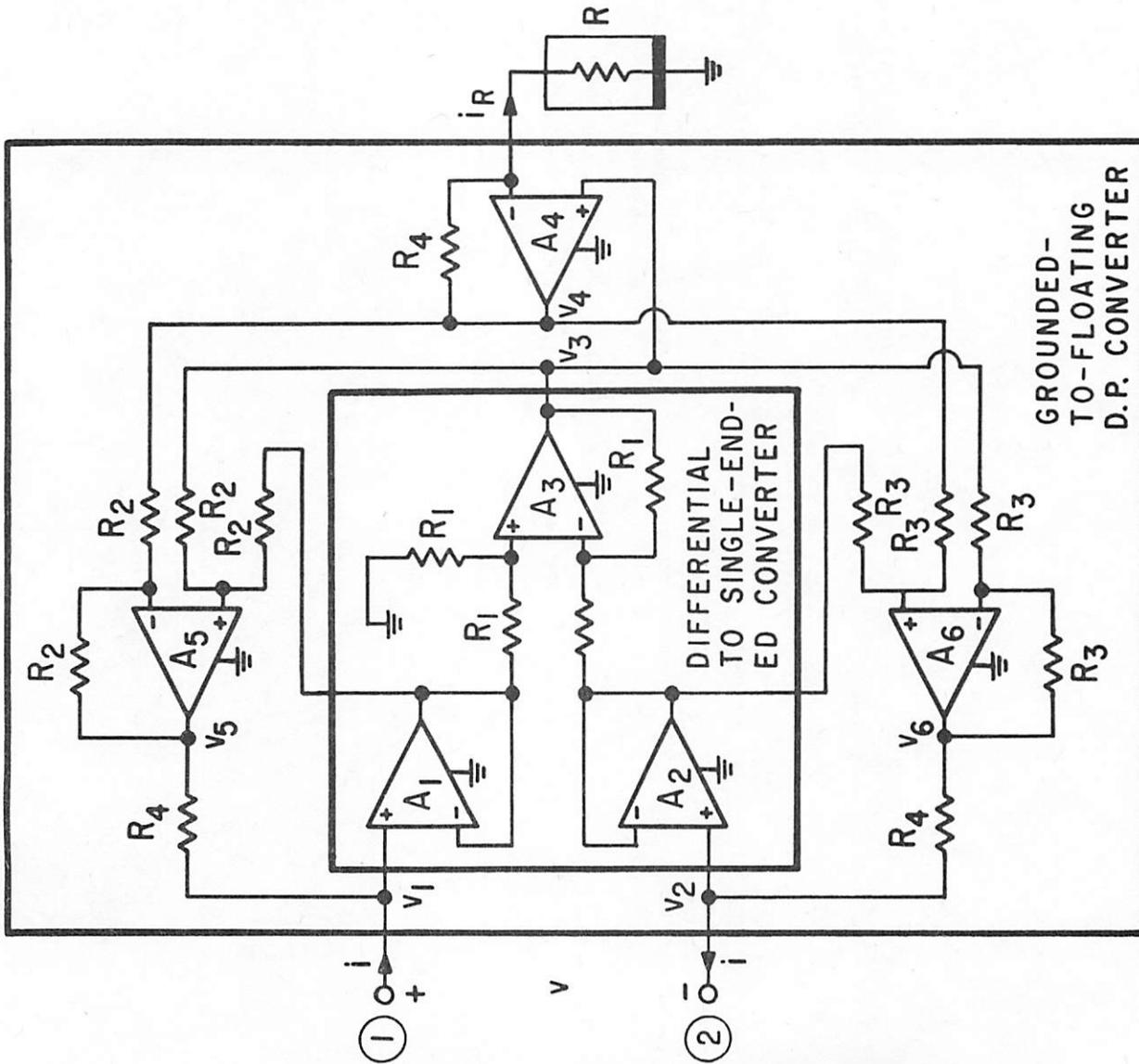
Fig. 5



(b)



(c)



(a)

Fig. 6

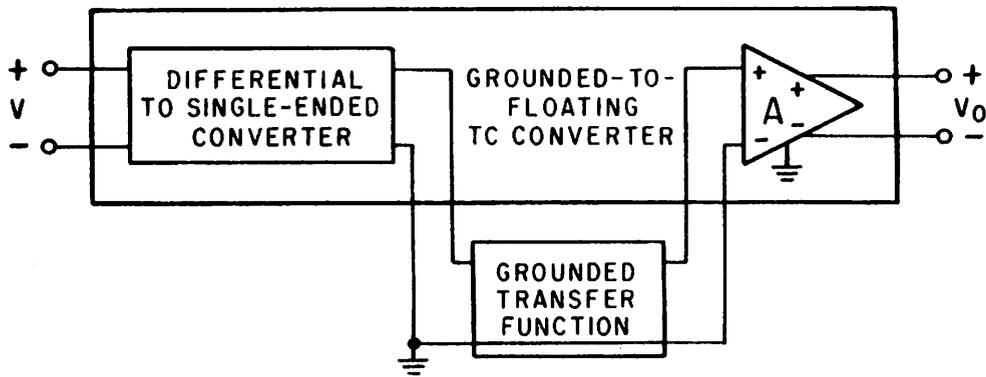


Fig. 7

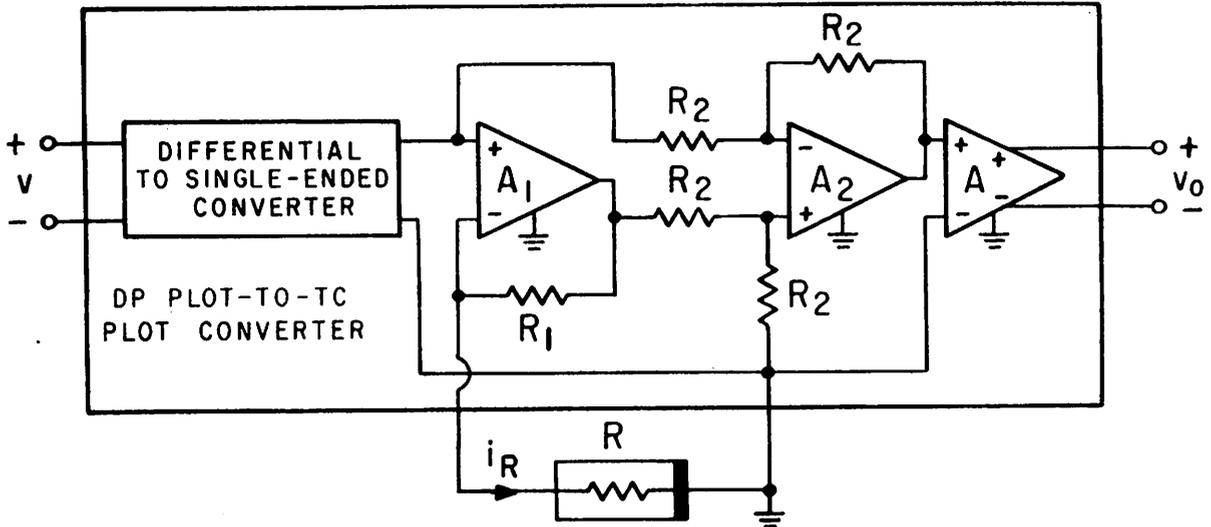


Fig. 8

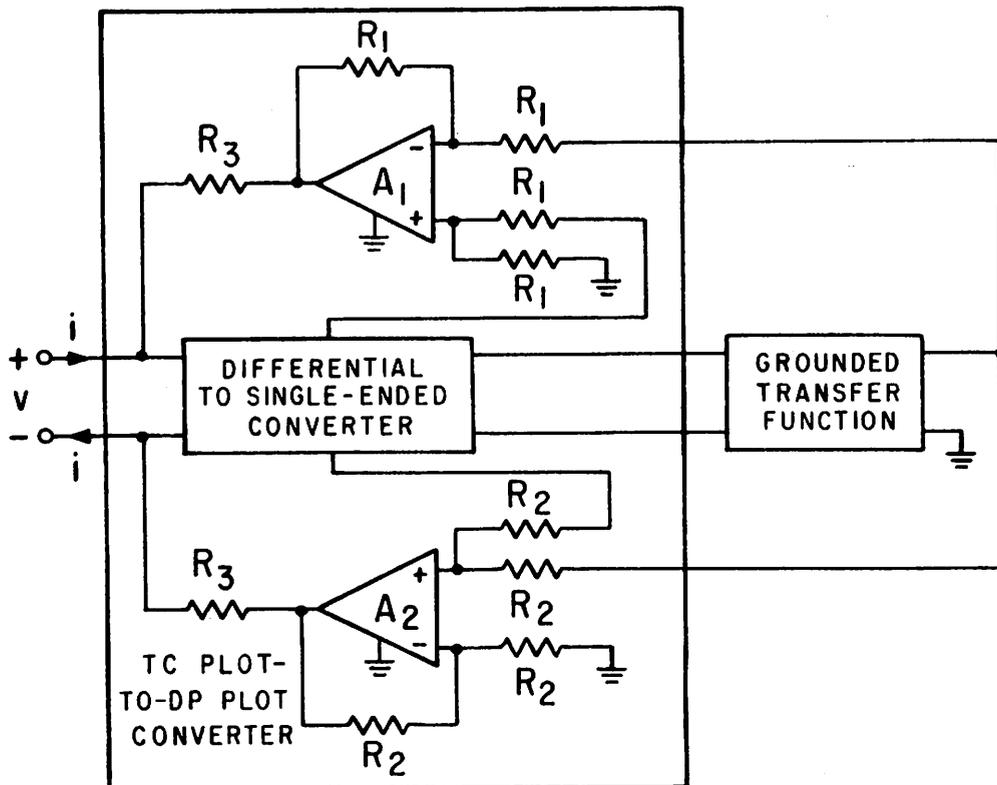


Fig. 9

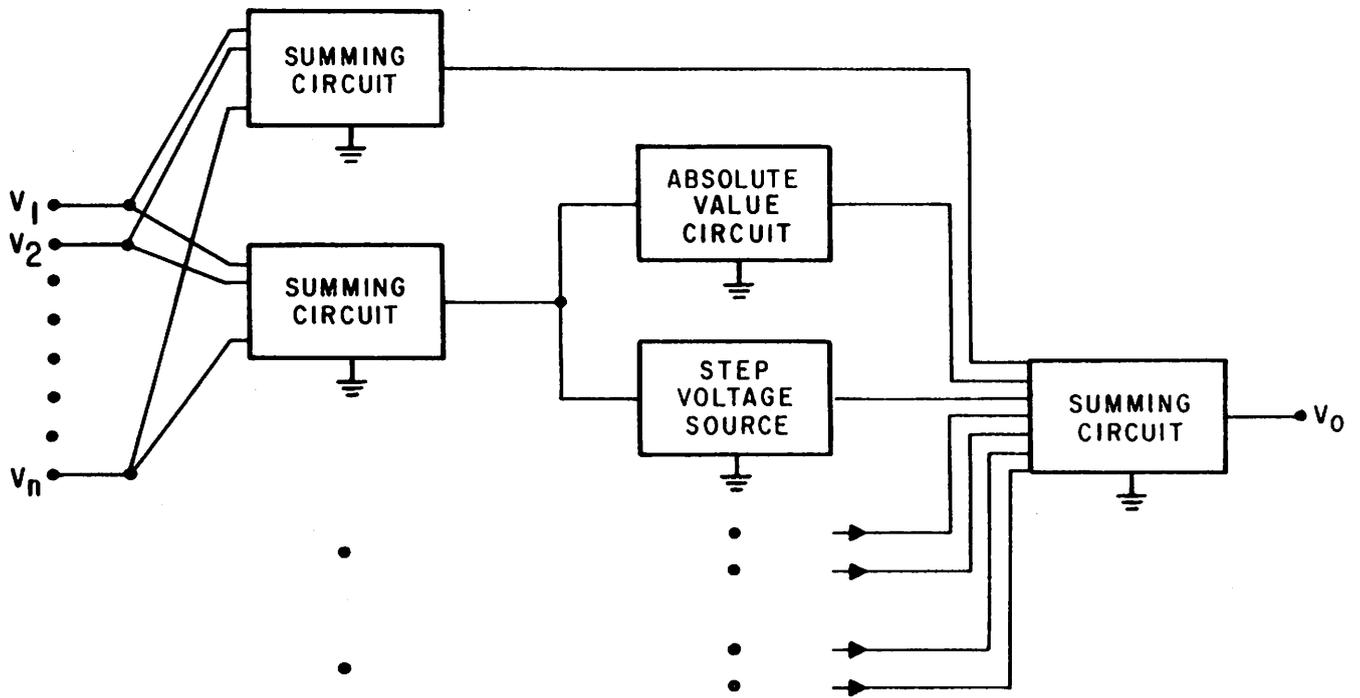


Fig. 10

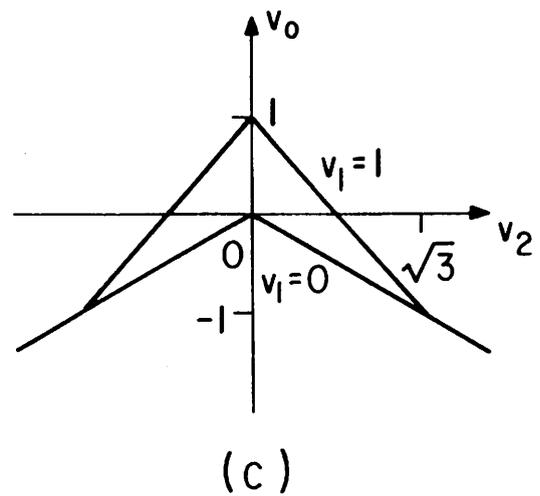
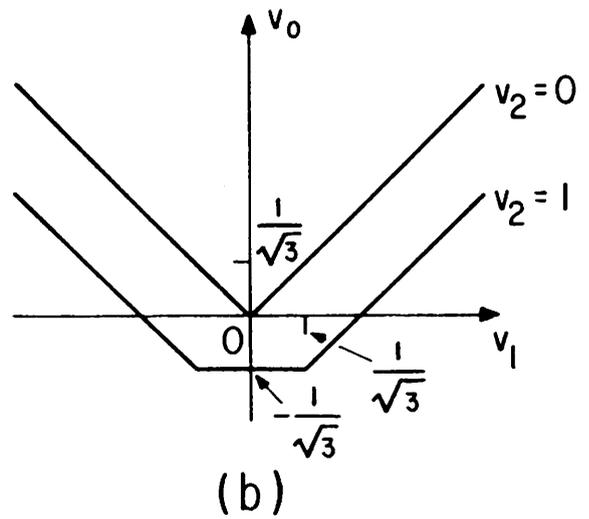
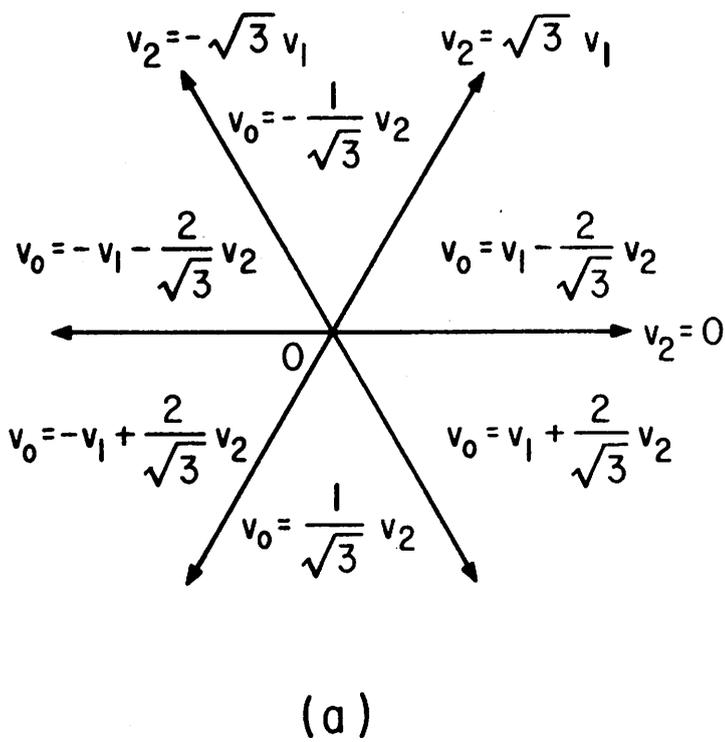
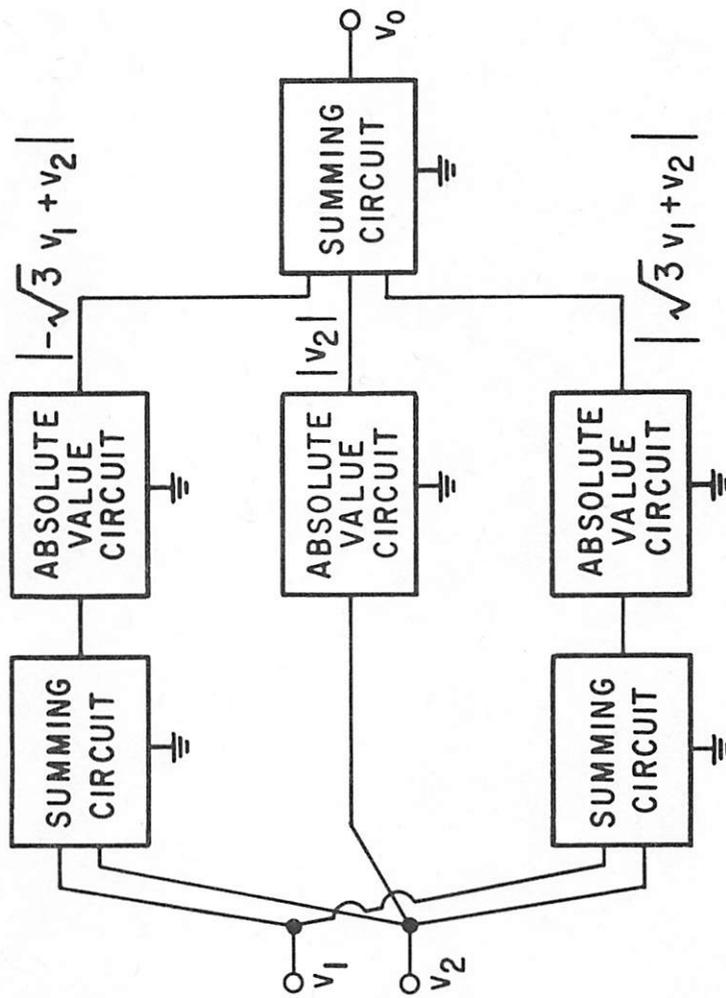
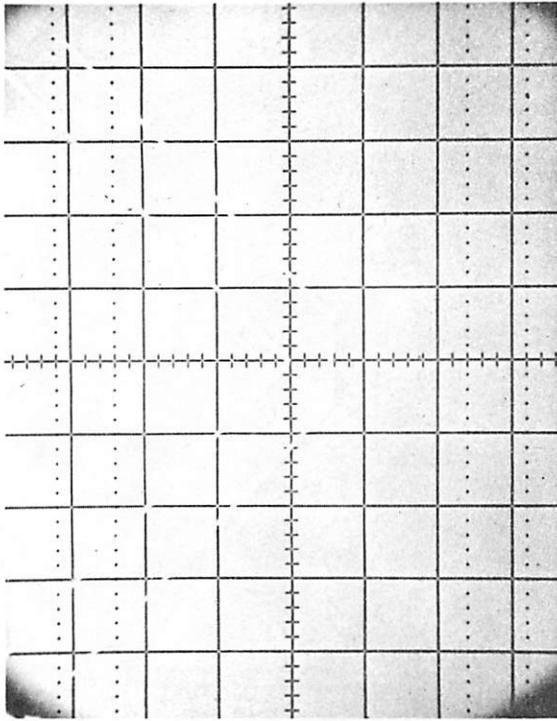


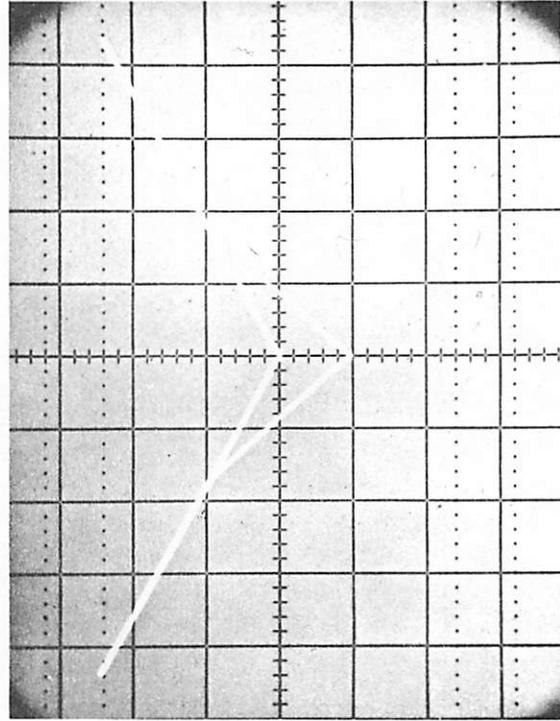
Fig. 11



(a)



(b)



(c)

Fig. 12

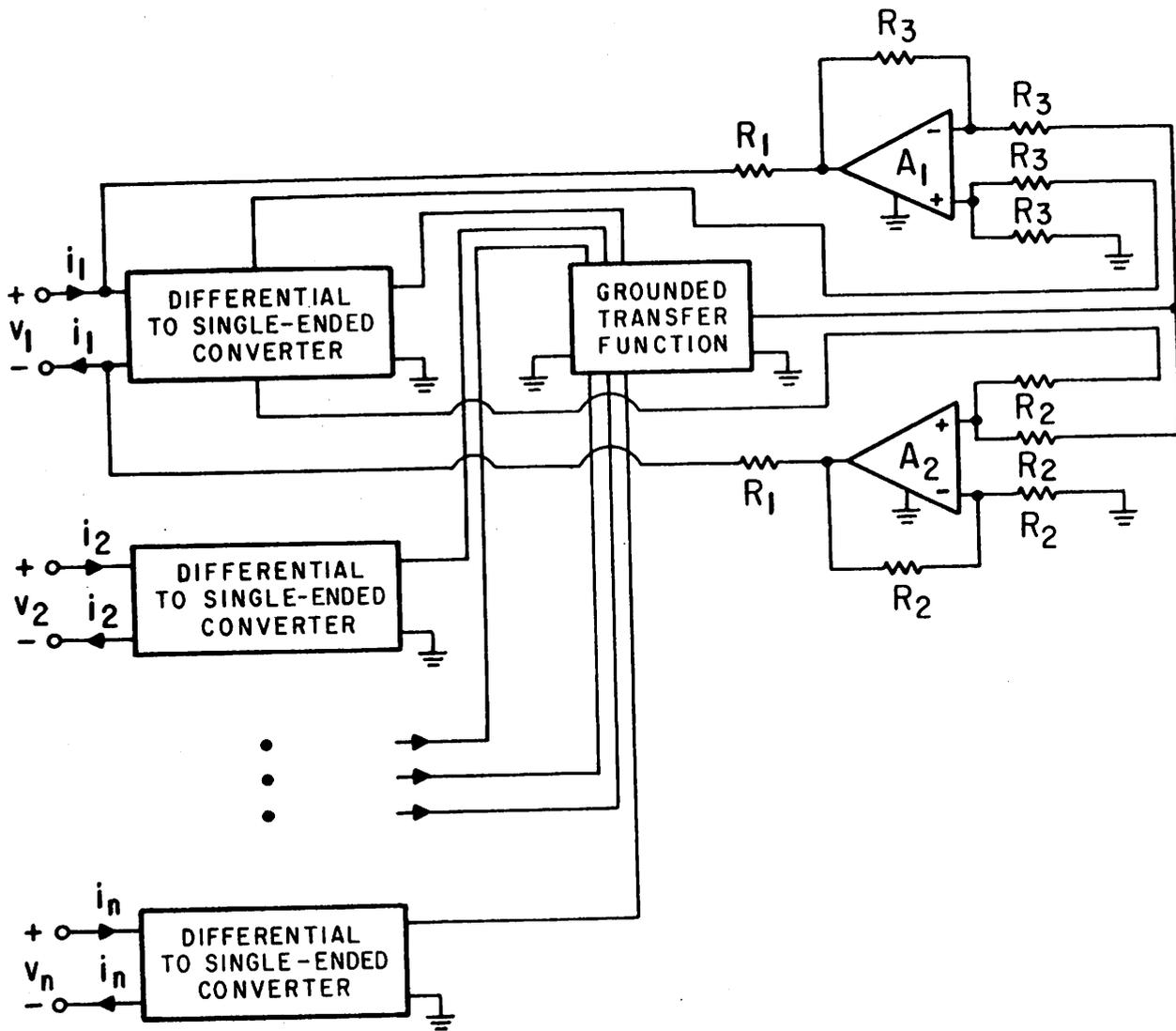
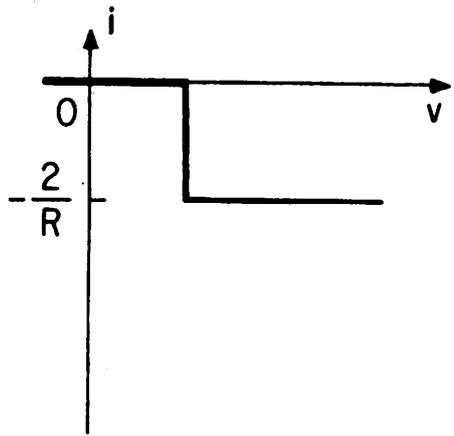
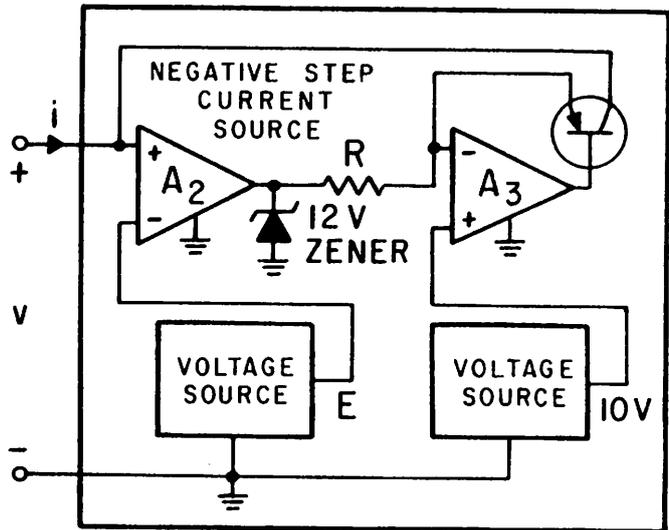


Fig. 13

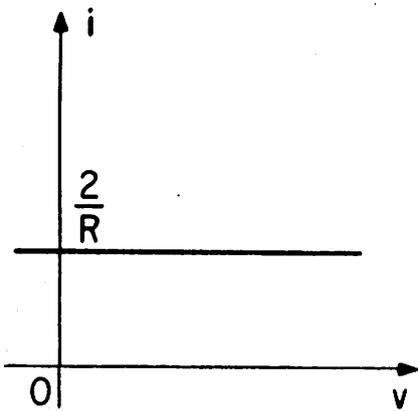


(a)

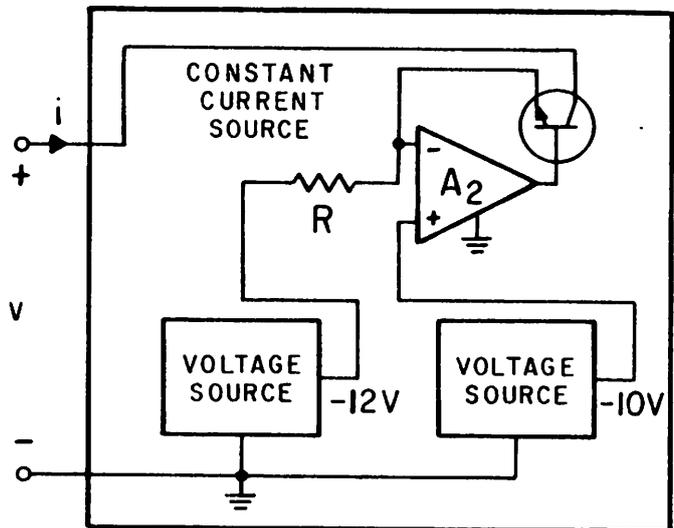


(b)

Fig. A-1



(a)



(b)

Fig. A-2