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SUTIDES IN MICROPOWER NMOS OPERATIONAL AMPLIFIER DESIGN

Memorandum No. UCB/ERL M78/85

11 December 1978

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

College of Engineering
Department of Electrical Engineering
and Computer Sciences

P.R. Gray

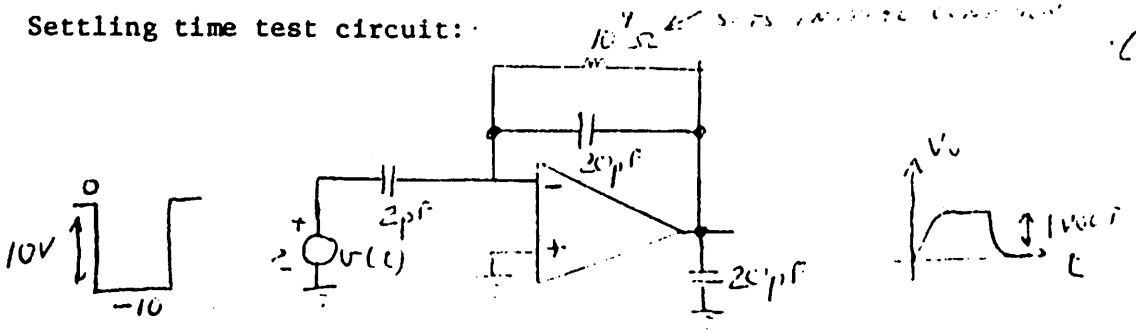
EECS 241
FALL 78

241 TERM PROJECT

The project is the design of a special-purpose micropower NMOS depletion mode operational amplifier for use in a switched-capacitor filter. The amplifier drives capacitive loads only. The following are the target specifications

- Supply Voltage ±5V
- Maximum power dissipation 1mW
- Output swing within .5 volts of supply
- Maximum capacitive load 20pF
- Input common mode range: ±1 volt
- Must settle to within 1mV of final value within ~~500ns~~ 2μs. in test ckt below (+,−)
- Input equivalent noise 200 nV per root hertz at 1 kHz (maximum)
- PSRR 60 dB min
- Gain greater than 1000 with a ±3 volt swing

Settling time test circuit:



Use the following device parameters:

Enhancement V_T (zero substrate bias)	.7V
Depletion V_T (zero substrate bias)	-3.0V
λ Enh, Depletion	$.02V^{-1}$
Substrate Doping	$5 \times 10^{+14}/cm^3$
UO	600 $cm^2/V\text{-sec}$
t_{ox}	1.0×10^{-5}m
x_j	2μ
LD	.77
Drain, source stripe width	14μ
Minimum channel length	7μ
K_F - FLICKER NOISE COEFF.	6×10^{-27}

Use the level two model in SPICE. You will be given a sub-account with $75.00 in it, and you may work in groups of two. Exceeding the limit of $75.00 per person will result in a lower final grade.

The final report is due the last day of class, and should include the following:

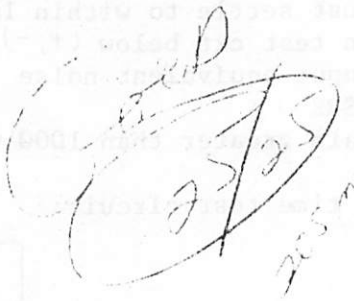
1. Description of circuit operation and a complete schematic showing all device sizes.
2. Computer output showing DC transfer characteristic.
3. Computer run showing settling time.
4. Noise analysis computer output.
5. PSRR simulation results.
6. A table showing all specs. achieved.

PRG/bjf
10/13/78

NMOS MICROPOWER OP AMP

Y.W. SING

J.W. JARVIS



UNIVERSITY OF CALIFORNIA

EECS 241 TERM PROJECT

FALL 1978

P.R. GRAY, ADVISOR

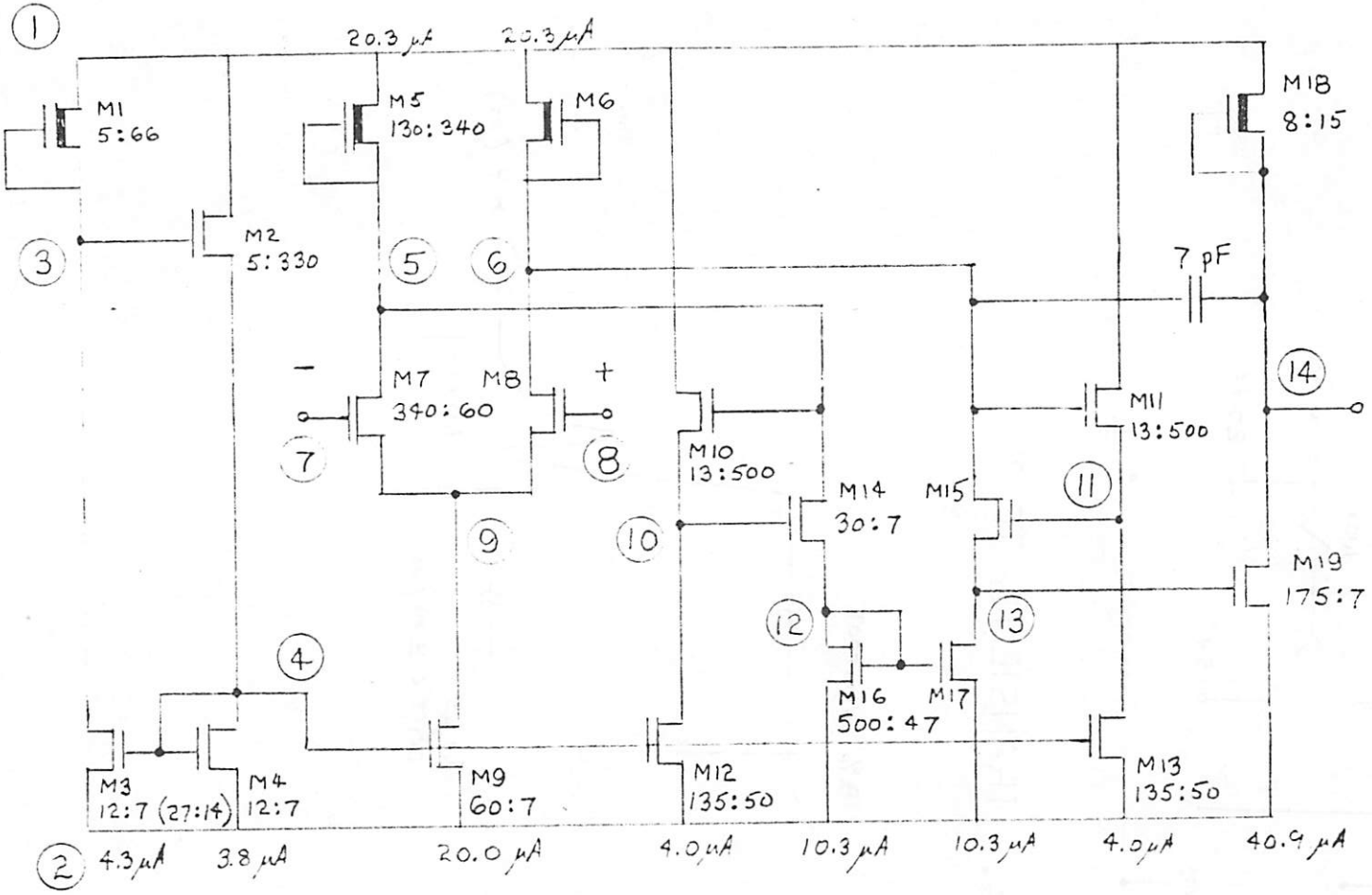


FIG 1. CIRCUIT SCHEMATIC

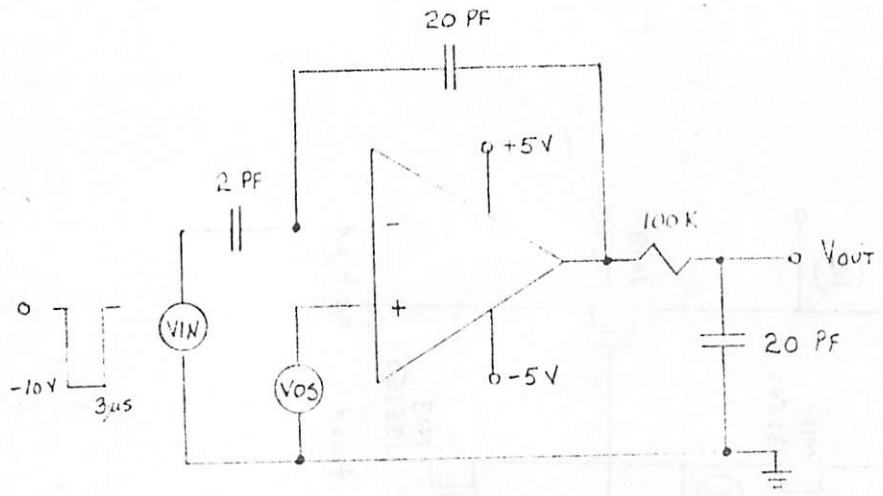


FIG 2. TRANSIENT TEST

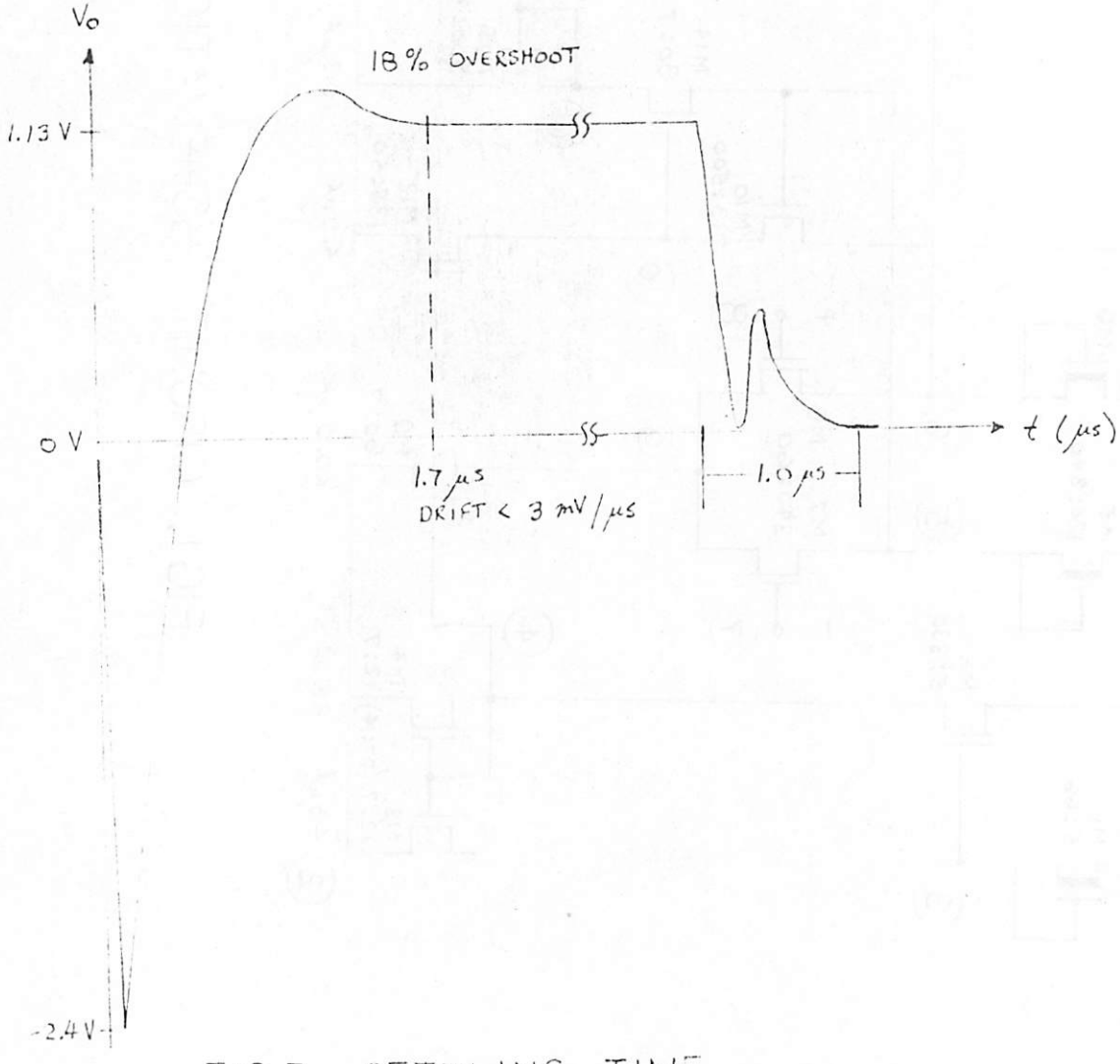


FIG 3. SETTLING TIME

ALL SPECS WERE ACHIEVED

TEST	TEST CONDITIONS	SPEC	SPEC ACHIEVED
MAXIMUM POWER	±5V	<1 MW	.976 mW
OUTPUT SWING	±5V	±4.5V	4.9/-4.8 V
OPEN LOOP GAIN	@ ±3V	>1000	1160 (19.3 × 60.1)
EQUIV. INPUT NOISE	1 KHz	< 200 $nV/\sqrt{Hz}$	186
PSRR	V_{DD} ±.5V V_{SS} ±.5V	>60 dB	88.4 dB 64.1 dB
CMRR	V_{IN} = 1 V V_{IN} = -1 V	>50 dB	76.3 dB 76.7 dB
SETTLING TIME - OUTPUT RISING OUTPUT FALLING	See Fig. 2,3	2 μs (.1% OF FINAL VALUE)	1.7 μs 1.0 μs (DRIFT <3 mV/μs)
V_{OS}	-	-	.1 mV
UNITY GAIN BW	-	-	1.0 MHz
PHASE MARGIN	-	-	74°

EE 241 TERM PROJECT

NMOS OP AMP

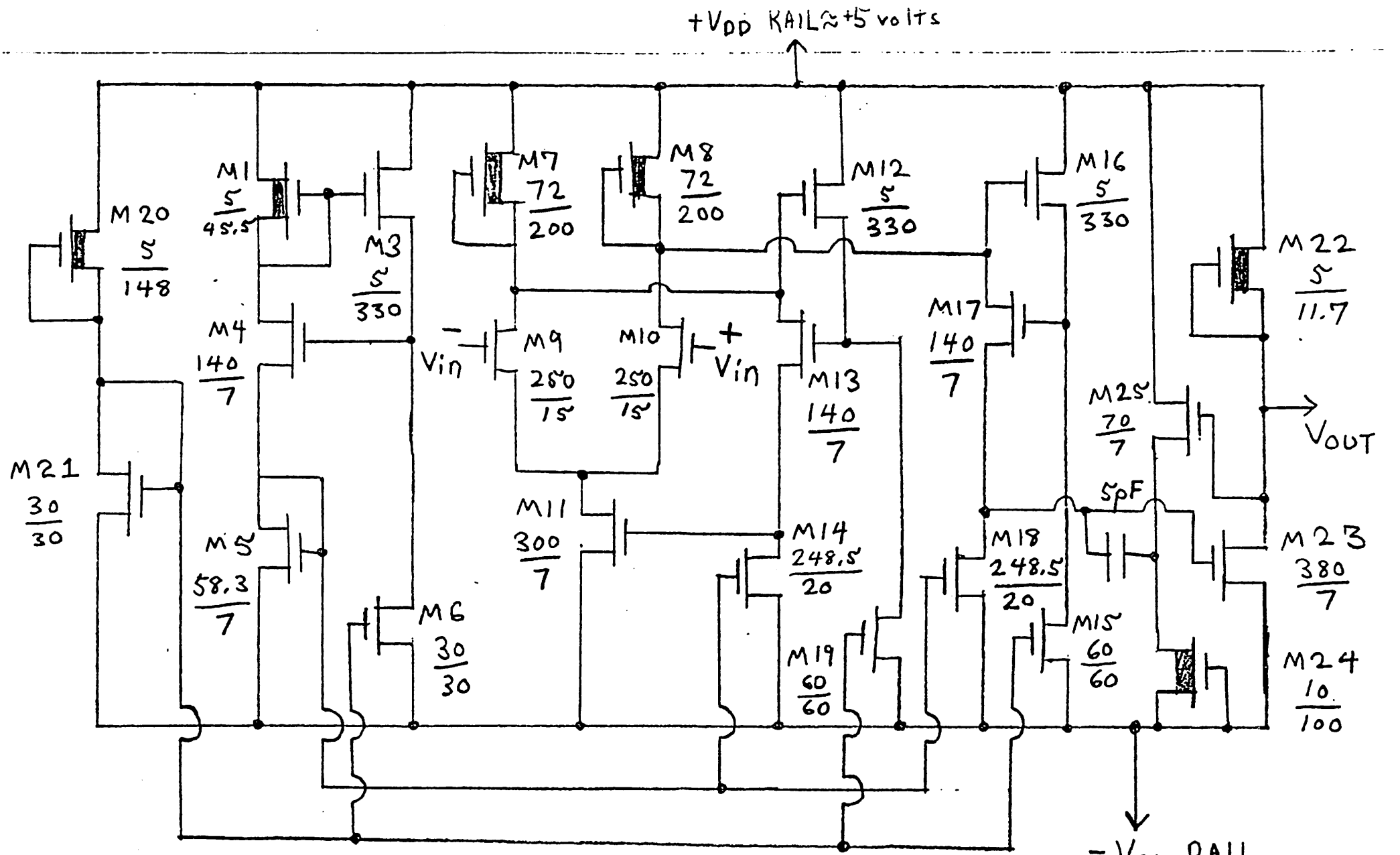
Good 25/25

by CHI NAN HSUE

(Partner: HAW MING HAUNG)

SPECIFICATIONS

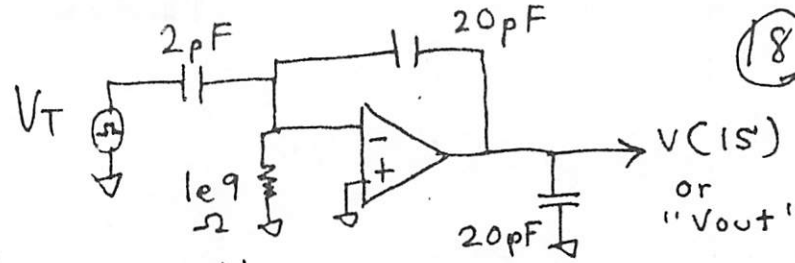
Power Dissipation	1.00 mw
Output Swing	within .1 volts either rail
Unity gain BW, phase margin	3 mhz, 65° (20pF load)
Gain margin	16 db (20 pF load)
Common Mode Rejection	@ ± 1 volt, −86 db.
Settling time to 1 mv with test cirkt. (see plot)	0 to 1 volt = 1.8 μs 1 volt to 0 volt = 1.4 μs
Input Equivalent Noise (see computer output)	193 nv. / √hz @ 1 khz.
PSRR	V_{DD} ± .5v. −100 db. V_{SS} ± .5v. −75 db.
Voltage gain at +3 volts out	1,300
Voltage gain at −3 volts out	3,200
Voltage gain at 0 volts out	4,000



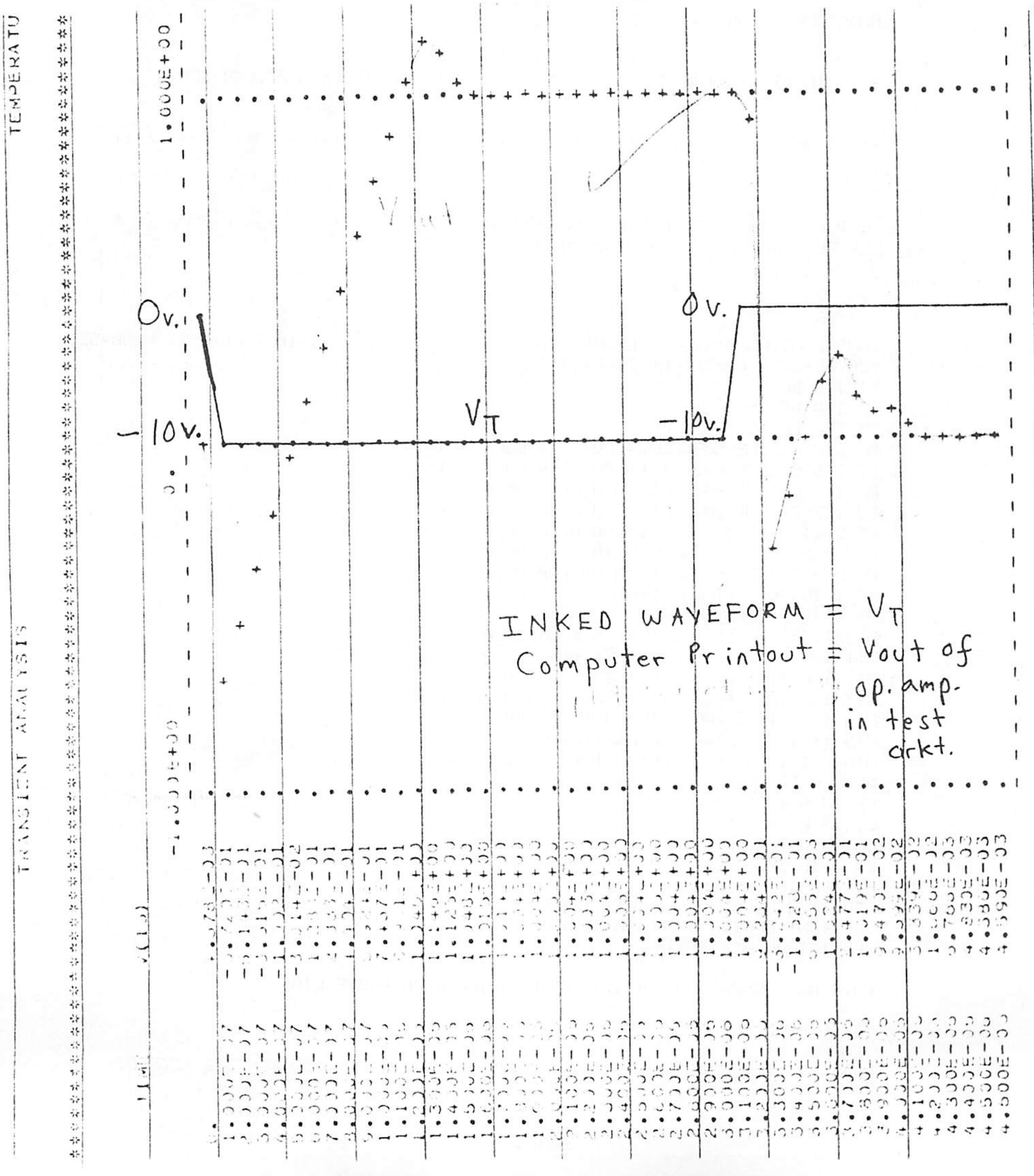
ALL MOSFETS HAVE SIZES NEXT TO THEM, WRITTEN AS: $\frac{W \text{ microns}}{L \text{ microns}}$

Transient Response

test circuit:



1. V_T is initially zero volts
2. Drops to −10 volts in .1 μs, or 100ns.
3. At 3 μs., it rises back up to 0 volts by 3.1 μs.



***** 30 NOV 78 ******** SPICE 2E.2 (26SEP78) ******** 19:40:15 *****

NMOS OPERATION AMPLIFIER

INPUT LISTING TEMPERATURE = 27.000 DEG C

****

.MODEL MA NMOS(VTO=0.7 UO=600 LAMBDA=0.02 NSUB=5E14 TOX=.1UP-7 XJ=1P-6 LD=0.77
+LEVEL=2 KF=6E-27 CGD=2.6E-10 CGS=2.6E-10)

.MODEL MD NMOS(VTO=-3 LAMBDA=0.02 UO=600 TOX=1E-7 XJ=1E-6 LD=0.77 NSUB=5E14
+LEVEL=2 KF=6E-27 CGD=2.6E-10 CGS=2.6E-10)
V1 1 0 DC 5
V2 2 0 DC -5
V3 3 0 DC -5
M1 6 4 8 3 ME W=300U L=20U AD=4200P AS=4200P
M2 7 5 8 3 ME W=300U L=20U AD=4200P AS=4200P
M3 1 6 6 3 MD W=45U L=267U AD=630P AS=630P
M4 1 7 7 3 MD W=45U L=267U AD=630P AS=630P
M5 8 11 2 3 ME W=36U L=10U AD=252P AS=252P
M6 10 9 2 3 ME L=40U W=21U AD=280P AS=280P
M7 9 9 2 3 ME L=11U W=5U AD=70P AS=70P
M8 1 10 10 3 MD L=119U W=5U AD=70P AS=70P
M9 1 10 9 3 ME W=5U L=143U AD=70P AS=70P
M10 11 9 2 3 ME W=13U L=7U AD=182P AS=182P
M11 12 9 2 3 ME W=13U L=7U AD=182P AS=182P
M12 1 6 11 3 ME W=100U L=73U AD=140P AS=140P
M13 1 7 12 3 ME W=100U L=73U AD=140P AS=140P
M14 1 13 13 3 MD W=5U L=10U AD=70P AS=70P
M15 13 12 2 3 MD W=43U L=7U AD=600P AS=600P
M16 7 1 14 3 MA W=5U L=45U AD=70P AS=70P
VS 5 0 DC 0
CF 11 6 1.5P
C1 13 0 2MP
C3 13 4 20P
C4 4 18 2P
R1 4 0 1G
VIN 18 0 PULSE 0 -1M 0.2U 0 0 4U
.OPTIONS ABSTOL=1E-8 VNTOL=1E-5
.PLOT TRAN V(13) VIN

WARNING: UNRECOGNIZABLE OUTPUT VARIABLE ON ABOVE LINE

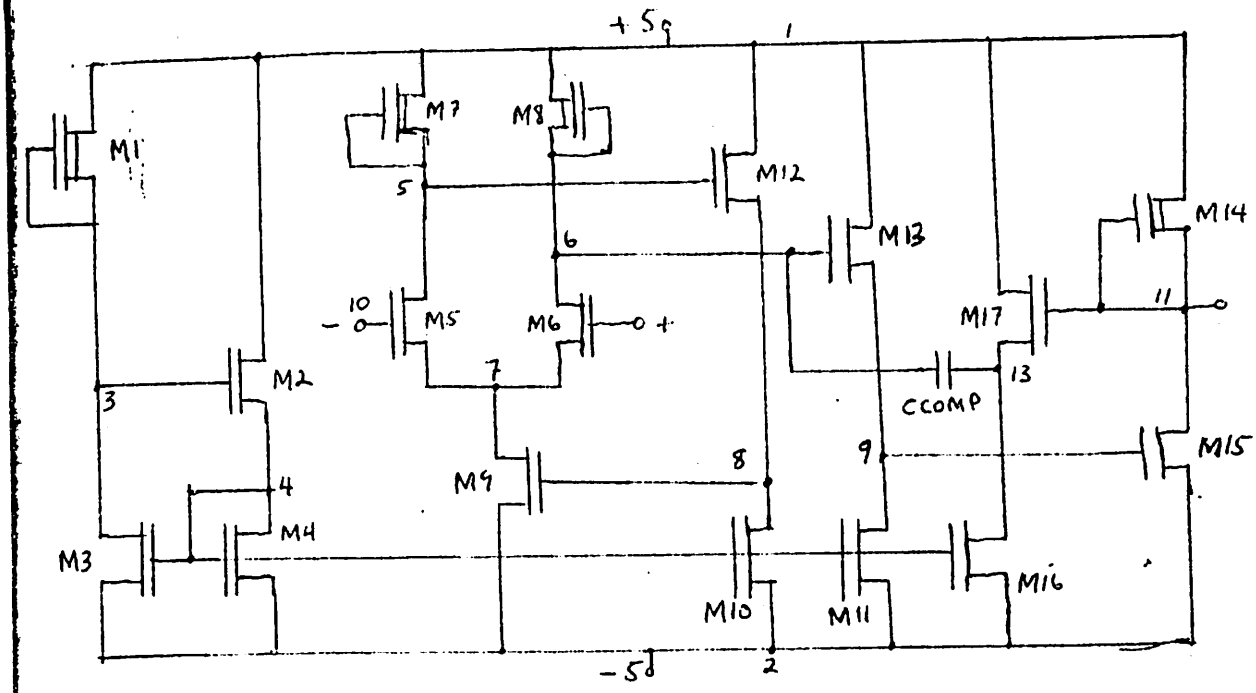
.TRAN 0.1U 8U
.END
********** 30 NOV 78 ********* SPICE 2E.2 (26SEP78) *********

Table 1

EECS 241 Term Project

for Prof. Gray

by Mike Honig
and Everett Herrera



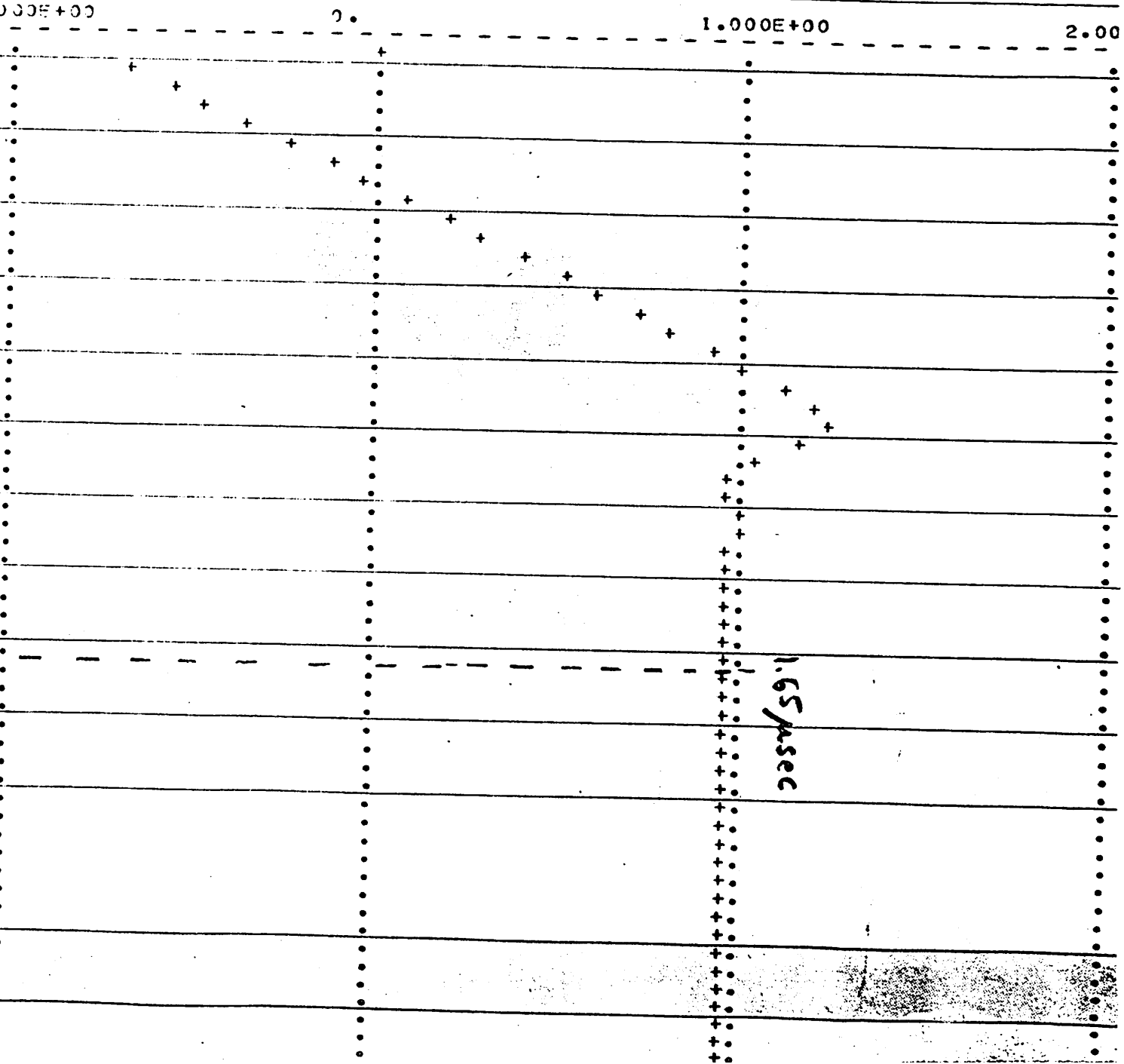
Device	Z (μm)	L (μm)	AD (μm^2)	AS (μm^2)
M1 (Depl.)	5	42	70	70
M2	5	137	70	70
M3	6	17	84	84
M4	6	17	84	84
M5	250	15	1000	1000
M6	250	15	1000	1000
M7 (Depl.)	50	395	700	700
M8 (Depl.)	50	395	700	700
M9	12	17	168	168
M10	6	17	84	84
M11	6	17	84	84
M12	5	137	70	70
M13	5	137	70	70
M14 (Depl.)	20	29	280	280
M15	19	9	266	266
M16	6	17	84	84
M17	5	55	70	70

CCOMP - .4 pf

Fig. 0 - Circuit Diagram and Device Sizes

Parameter	Value Realized	Value Specified
Power Dissipation	0.92 mW	1 mW
Output Swing	within .5 V of supply	same
Common Mode Range	at least ±1 V	same
CMRR	77 dB (+ direction) 94 dB (- direction)	50 dB
.1% Settling Time	1.65 usec	2 usec
Input Equivalent Noise	196.8 nV/ hz	200 nV/ hz
PSRR	95.5 dB (+ supply) 64.8 dB (- supply)	60 dB
Gain (±3 V swing)	1292	1000

TIME	V(11)
0.	7.243E-05
5.000E-08	-7.315E-01
1.000E-07	-5.774E-01
1.500E-07	-4.726E-01
2.000E-07	-3.930E-01
2.500E-07	-2.416E-01
3.000E-07	-1.342E-01
3.500E-07	-2.283E-02
4.000E-07	8.343E-02
4.500E-07	1.907E-01
5.000E-07	2.979E-01
5.500E-07	4.023E-01
6.000E-07	5.074E-01
6.500E-07	6.115E-01
7.000E-07	7.141E-01
7.500E-07	8.169E-01
8.000E-07	9.185E-01
8.500E-07	1.020E+00
9.000E-07	1.119E+00
9.500E-07	1.197E+00
1.000E-06	1.224E+00
1.050E-06	1.172E+00
1.100E-06	1.059E+00
1.150E-06	9.675E-01
1.200E-06	9.545E-01
1.250E-06	9.805E-01
1.300E-06	9.890E-01
1.350E-06	9.763E-01
1.400E-06	9.651E-01
1.450E-06	9.646E-01
1.500E-06	9.678E-01
1.550E-06	9.689E-01
1.600E-06	9.679E-01
1.650E-06	9.668E-01
1.700E-06	9.667E-01
1.750E-06	9.670E-01
1.800E-06	9.671E-01
1.850E-06	9.670E-01
1.900E-06	9.669E-01
1.950E-06	9.668E-01
2.000E-06	9.670E-01
2.050E-06	9.671E-01
2.100E-06	9.672E-01
2.150E-06	9.671E-01
2.200E-06	9.670E-01
2.250E-06	9.671E-01
2.300E-06	9.672E-01
2.350E-06	9.672E-01
2.400E-06	9.671E-01
2.450E-06	9.670E-01
2.500E-06	9.670E-01
2.550E-06	9.671E-01
2.600E-06	9.672E-01
2.650E-06	9.672E-01
2.700E-06	9.670E-01
2.750E-06	9.670E-01
2.800E-06	9.671E-01



Good for writeup 7/31

EECS 241 PROJECT

NMOS OPERATIONAL AMPLIFIER DESIGN

Prof. R. Gray

David J. Curtin

Robin L.P. Ying

December 1, 1978

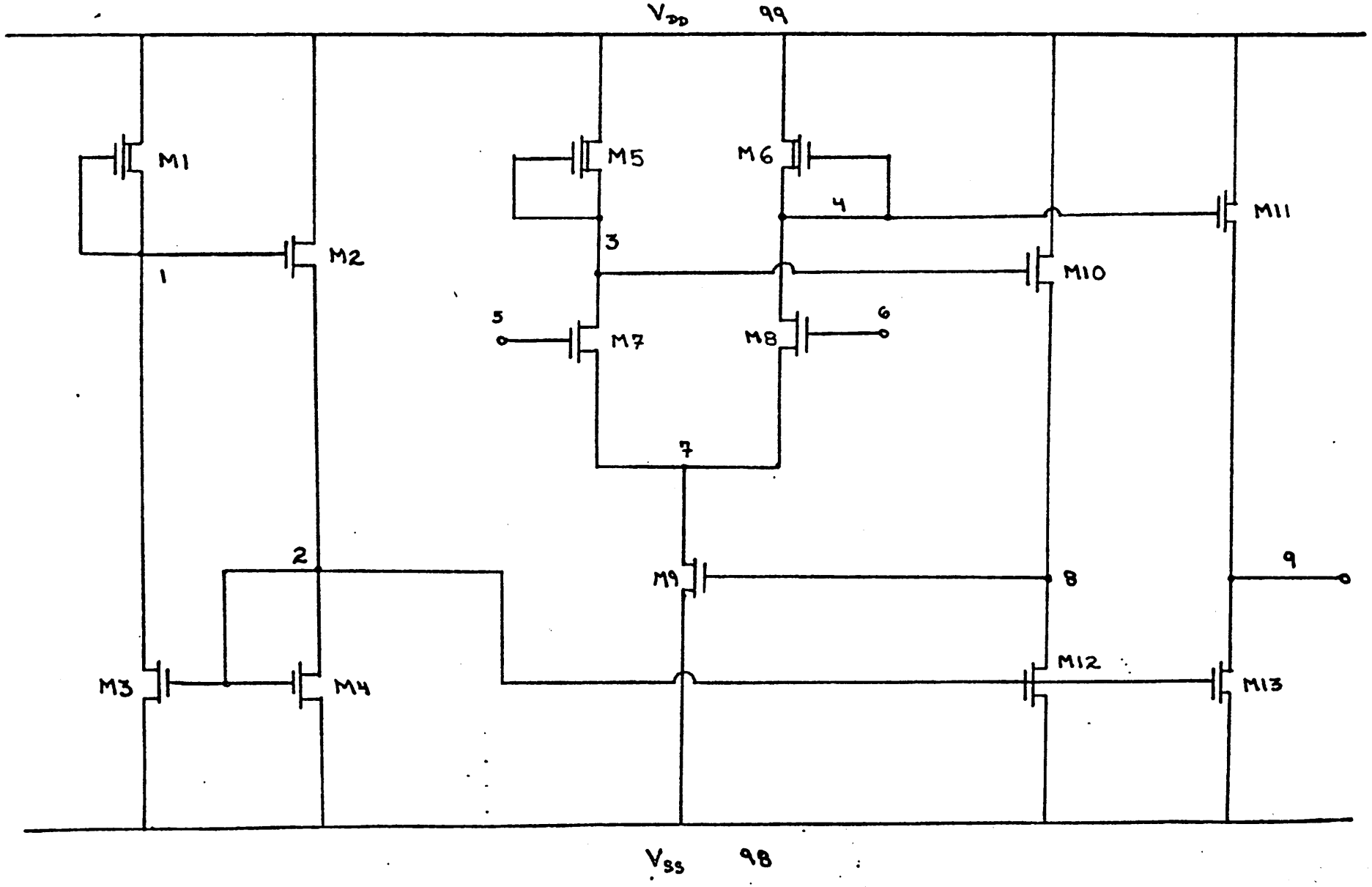


Figure 1 Input Stage

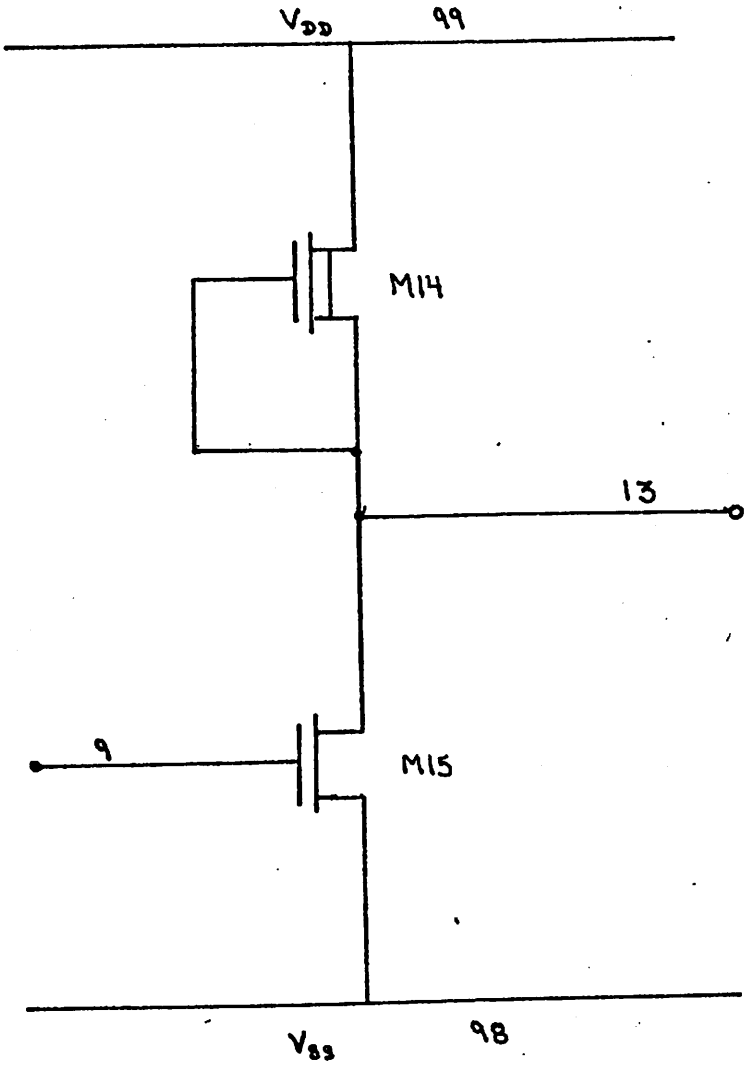


Figure 2

Output Stage

Table 1

Device Geometries

```
[illegible]MOS OPERATIONAL AMPLIFIER
*** DEVICES MODEL ***                                TOX=1.0E-7 NSUB=5.0E+14
.MODEL NMOS NMOS (LEVEL=2 VTO=+0.7 LAMBDA=0.02
+XJ=1U LD=0.77 UO=[illegible] KF=[illegible]E-27 AF=1.0)  TOX=1.0E-7 NSUB=5.0E+14
.MODEL PMOS PMOS (LEVEL=2 VTO=-3.0 LAMBDA=0.02
+XJ=1U LD=0.77 UO=600 KF=[illegible]E-27 AF=1.0)
*
*** INPUT STAGE ***
***** CURRENT IS: M1-M4 = [illegible]UA, M5-M8 = 10UA, M9 = 20UA, M10-M13 = 10UA ****
                                               L= 1350     AD= 70P      AS= 70P
M1    99   1   1   95  [illegible]  W= 50      L= 5840     AD= 70P      AS= 70P
M2    99   1   2   98  [illegible]  W= 50      L= 70       AD= 70P      AS= 70P
M3    1    2   95  95  [illegible]  W= 50      L= 600      AD= 700P     AS= 700P
M4    2    2   [illegible]  99  [illegible]  W= 500     L= 2490     AD= 700P     AS= 700P
M5    99   3   5   98  [illegible]  W= 500     L= 2490     AD= 700P     AS= 700P
M6    99   4   4   98  [illegible]  W= 500     L= 70       AD= 670P     AS= 412P
M7    3    5   7   99  [illegible]  W= 1800    L= 70       AD= 670P     AS= 412P
M8    4    5   7   98  [illegible]  W= 1800    L= 70       AD= 714P     AS= 714P
M9    7    3   [illegible]  99  [illegible]  W= 510     L= 1170     AD= 70P      AS= 70P
M10   99   3   [illegible]  98  [illegible]  W= 50      L= 1170     AD= 70P      AS= 70P
M11   99   4   9   98  [illegible]  W= 50      L= 70       AD= 364P     AS= 364P
M12   9    3   [illegible]  95  [illegible]  W= 200     L= 70       AD= 364P     AS= 364P
M13   6    2   [illegible]  98  [illegible]  W= 200
*
*** GAIN AND OUTPUT STAGE ***************************************************
***** CURRENT = 550UA ****************************  L= 8.5U   AD= 70P      AS= 70P
M14   99   13  13  98  [illegible]  W= 50      L= 70       AD= 1680P    AS= 1680P
M15   13   [illegible]  [illegible]  95  [illegible]  W= 1220
*
```

Table 3

	Circuit Specifications	Required Specifications
Power dissipated	0.984 mW	1mW
Gain for ±3V swing	4375 (72 dB)	1000 (60 dB)
Maximum swing	+ 5 V	+ 4.5V
	-4.952 V	- 4.5V
PSRR (w.r.t. V_{DD})	97.04 dB	60 dB
(w.r.t. V_{SS})	78.64 dB	60 dB
CMRR (+1V c.m.)	86.19 dB	50 dB
(-1V c.m.)	86.43 dB	50 dB
Input noise	196.5 nV/$\sqrt{Hz}$	200nV/$\sqrt{Hz}$
Settling time	2.8μs	2μs

MICROPOWER NMOS OP AMP

Peter Chu *
EE 241
P. R. Gray Instructor
12/1/78

* Note: This was a one man project.

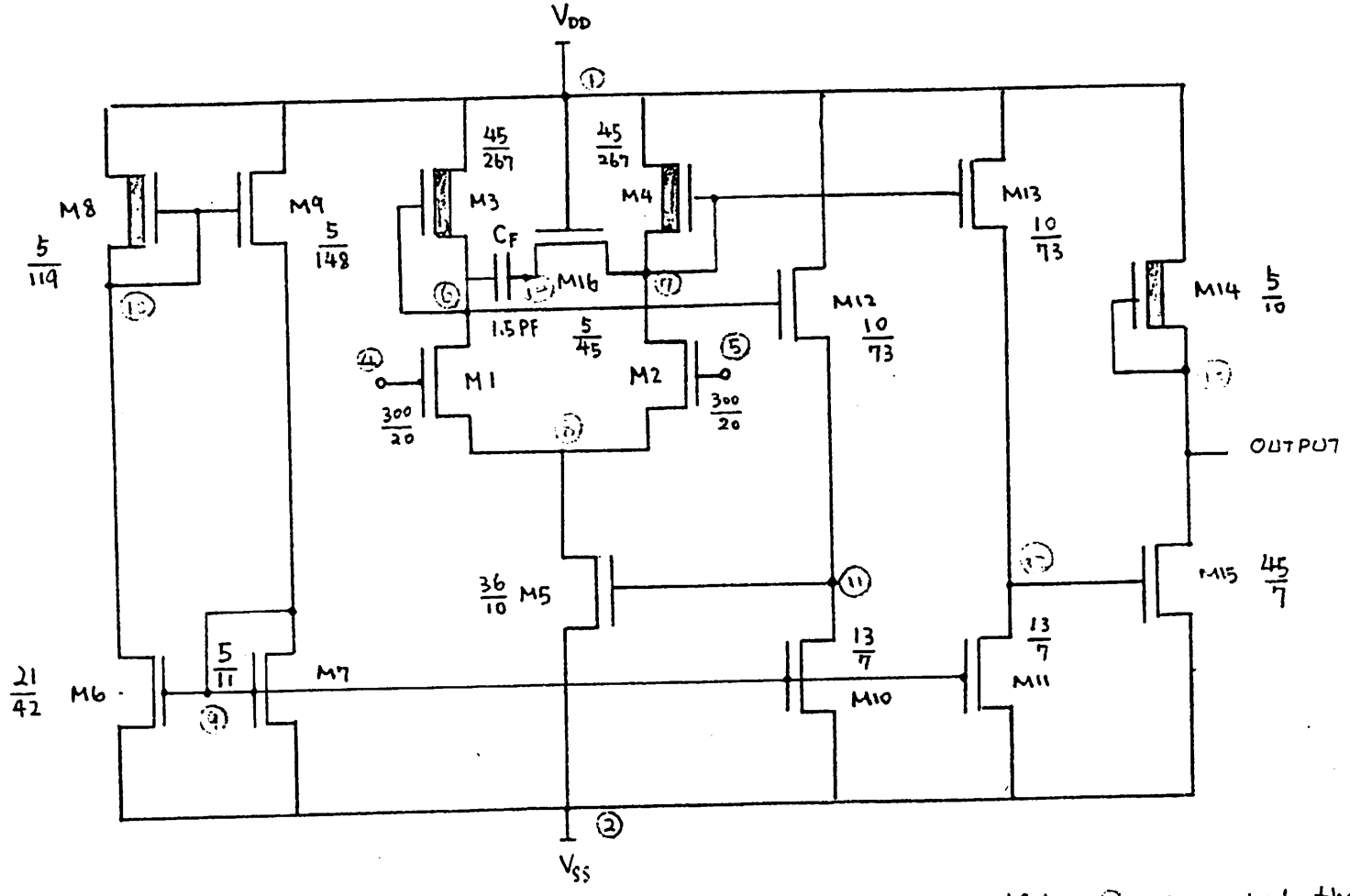
SUPPLY VOLTAGE	± 5V
MAX. POWER DISSIPATION	0.948 mW
OUTPUT SWING	-4.72V to +4.97V
MAX CAP. LOAD	20pF
CMRR UNDER COMMON MODE RANGE ±1 V	79 dB
SETTLING TIME	RISING 1.7μ
INPUT EQUIVALENT NOISE	185 nV/√Hz at 1KHz
PSRR	69.9 dB
GAIN WITH A ±3VOLT SWING	-2032

Table 5.

Feature of NMOS OP AMP.

Input Listing for Spice Transient Response

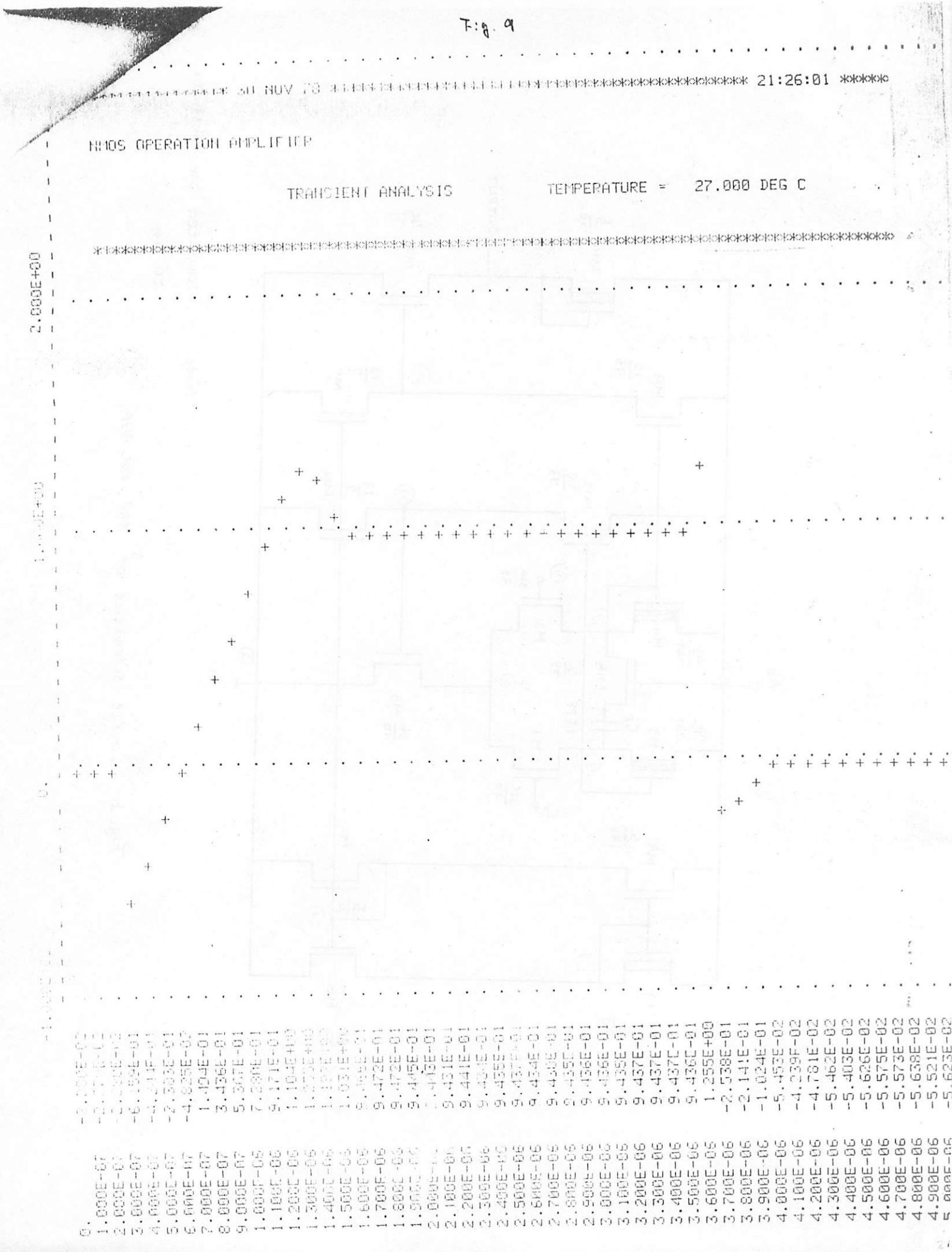
```
***** 30 NOV 73 ********  SPICE 2F.2 (26SEP72)  ******** 04:10:50 **

COMPLETE MOSFET OPERATIONAL AMPLIFIER

      INPUT LISTING                          TEMPERATURE =   27.000 DEG C

******************************************************************************

.OPTIONS ABSTOL=1E-3 VNTOL=1E-3
VT 16 0 PULSE(0 -10 0 100NS 100NS 30S 60S)
VDD 1 0 DC 5
VSS 0 2 DC 5
VOFF 21 0 DC .0
C1 12 19 5E-12
C2 16 13 2E-12
C3 15 13 2E-11
C4 15 0 2E-11
R1 13 0 1E9
M1 1 3 3 2 MOD1 L=45.5U W=5U AD=70P AS=70P
M3 1 3 4 2 MOD2 L=3300 W=5U AS=70P AD=70P
M4 3 4 5 2 MOD2 L=7U W=140U AD=2000P AS=2000P
M5 5 5 2 2 MOD2 L=7U W=58.3U AD=816P AS=816P
M6 4 14 2 2 MOD2 L=30U W=43U AD=400P AS=400P
M7 1 6 6 2 MOD1 L=200U W=72U AD=800P AS=800P
M8 1 10 10 2 MOD1 L=200U W=72U AD=300P AS=300P
M9 6 13 7 2 MOD2 L=15U W=250U AD=3000P AS=3000P
M10 10 21 7 2 MOD2 L=15U W=250U AD=3000P AS=3000P
M11 7 8 2 2 MOD2 L=7U W=300U AD=4000P AS=4000P
M12 1 6 9 2 MOD2 L=330U W=6U AD=70P AS=70P
M13 6 9 8 2 MOD2 L=7U W=140U AD=2000P AS=2000P
M14 8 5 2 2 MOD2 L=20U W=248.5U AD=3500P AS=3500P
M15 11 14 2 2 MOD2 L=60U W=10U AD=800P AS=800P
M16 1 10 11 2 MOD2 L=330U W=5U AD=70P AD=70P
M17 10 11 12 2 MOD2 L=7U W=140U AD=2000P AS=2000P
M18 12 5 2 2 MOD2 L=20U W=248.5U AD=3500P AS=3500P
M19 9 14 2 2 MOD2 L=50U W=60U AD=800P AS=800P
M20 1 14 14 2 MOD1 L=148U W=5U
M21 14 14 2 2 MOD2 L=40U W=5U AD=400P AS=400P
M22 1 15 15 2 MOD1 L=11.77U W=5U
M23 15 12 2 2 MOD2 L=7U W=83U AD=1000P AS=1000P
M24 15 2 2 2 MOD1 L=100U W=10U
M25 1 15 15 2 MOD2 L=7U W=70U AD=500P AS=500P
.MODEL MOD1 NMOS( LEVEL=2 VTO=-3.0
+ KF=6E-27
+LAMBDA= .02 TOX= 1.0E-7 NSUB= 5E14 XJ= 1E-6 LD= .77 UO=600 )
.MODEL MOD2 NMOS( LEVEL=2 VTO=0.7
+ KF=6E-27
+LAMBDA= .02 TOX= 1.0E-7 NSUB= 5E14 XJ= 1E-6 LD= .77 UO=600 )
.TRAN 100NS 60S
.PLOT TRAN V(15)
.END
```



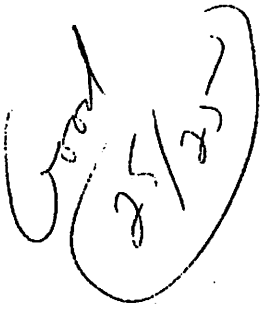
Node ③ connected the substrate to V_{SS}.

Fig. 1 Circuit schematics of the OP AMP

Fig. 9


30 NOV 78 21:26:01
NMOS OPERATIONAL AMPLIFIER
TRANSIENT ANALYSIS
TEMPERATURE = 27.000 DEG C
2.000E+00
1.000E+00
0.
0. 1.000E-07 2.000E-07 3.000E-07 4.000E-07 5.000E-07 6.000E-07 7.000E-07 8.000E-07 9.000E-07 1.000E-06 1.100E-06 1.200E-06 1.300E-06 1.400E-06 1.500E-06 1.600E-06 1.700E-06 1.800E-06 1.900E-06 2.000E-06 2.100E-06 2.200E-06 2.300E-06 2.400E-06 2.500E-06 2.600E-06 2.700E-06 2.800E-06 2.900E-06 3.000E-06 3.100E-06 3.200E-06 3.300E-06 3.400E-06 3.500E-06 3.600E-06 3.700E-06 3.800E-06 3.900E-06 4.000E-06 4.100E-06 4.200E-06 4.300E-06 4.400E-06 4.500E-06 4.600E-06 4.700E-06 4.800E-06 4.900E-06

A Low Power MOS Operational Amplifier



Jim Kleckner
EE 241
Fall 1978
Prof. P. R. Gray

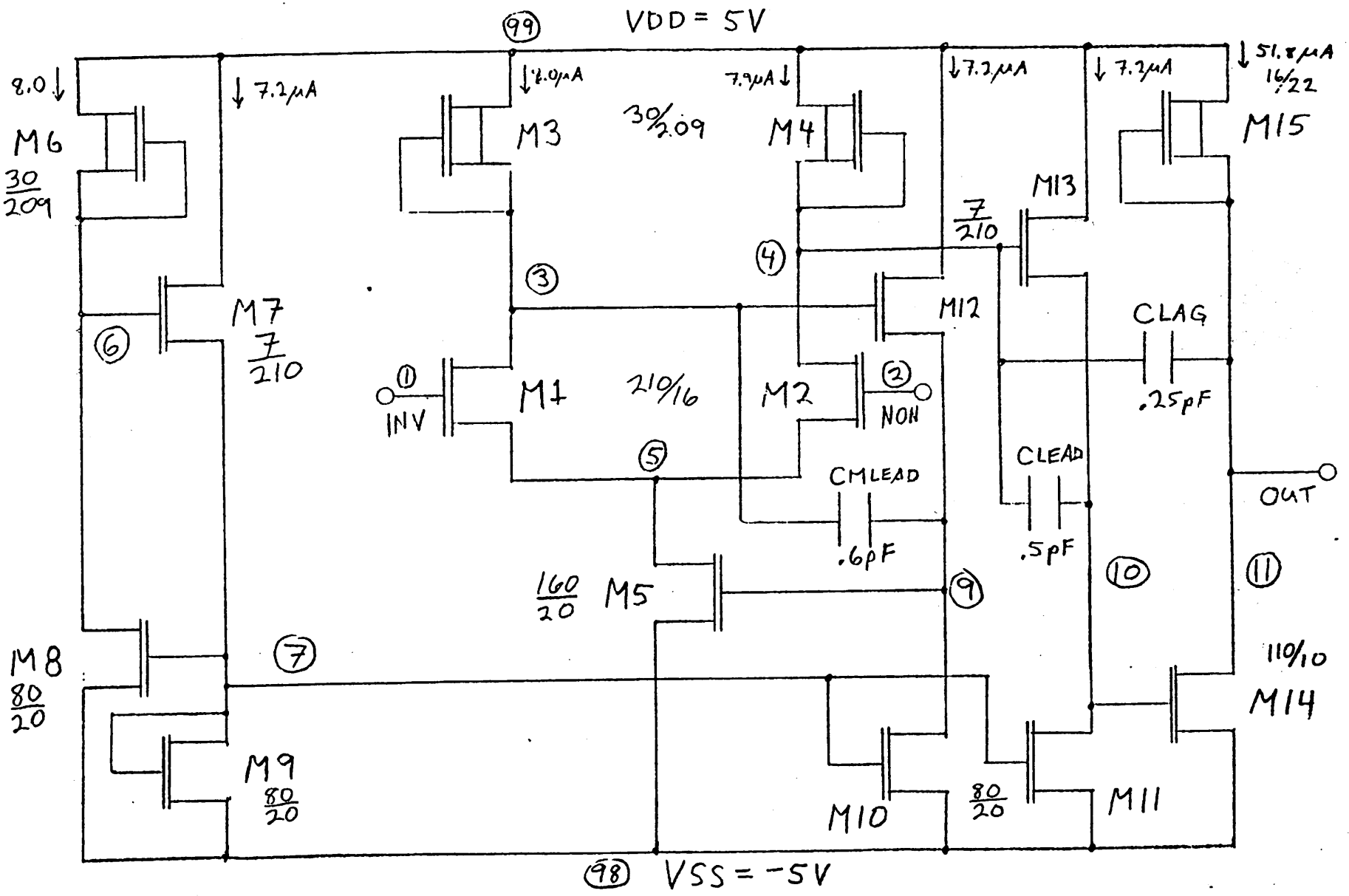


Figure 1. Circuit

Table 1. Specification Summary

Specification	Target	Achieved	Conditions
Power Dissipation	1 mW	.97 mW	V_{DD}= 5V; V_{SS}=-5 V; V_{out}=0 V
Common Mode Rejection	50 dB	84 dB	$\pm$1 Volt CM range
Power Supply Rejection	60 dB	75 dB	Change V_{OD} and V_{SS} by .5 V independently.
Settling Time	2 μs	1.65 μs	to 0.1% rising output
		1.10 μs	to 0.1% falling output
Input Equivalent Noise	200 $\frac{nV}{Hz}$	182 $\frac{nV}{Hz}$	at 1 KHz
Gain	1000	2350	at V_{out} $\pm$3 V
Output Swing	(-4.5,4.5)	(4.7,5.0)	Volts
Unity Gain Bandwidth	-	4.5 MHz	
Phase Margin	-	38	At unity gain.
	-	31	Lowest value before unity gain.
Slew Rate	-	2.3 V/μs	positive slew*
	-	5.5V/μs	negative slew*
Input Offset Voltage	-	-2.5 mV	

*Does not include capacitive feedthrough effects.

********** 30 NOV 78 ********** SPICE 2E.2 (26SEP78) ********** 13:3

NMOS MICROPOWER OP AMP - SING/JARVIS - BATTERY VERSION

TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG

****

TIME	V(14)
0.	-5.018E-03
5.000E-08	-2.432E+00
1.000E-07	-1.967E+00
1.500E-07	-1.507E+00
2.000E-07	-1.105E+00
2.500E-07	-7.913E-01
3.000E-07	-5.410E-01
3.500E-07	-3.293E-01
4.000E-07	-1.341E-01
4.500E-07	6.204E-02
5.000E-07	2.544E-01
5.500E-07	4.423E-01
6.000E-07	6.295E-01
6.500E-07	8.173E-01
7.000E-07	1.012E+00
7.500E-07	1.197E+00
8.000E-07	1.316E+00
8.500E-07	1.340E+00
9.000E-07	1.313E+00
9.500E-07	1.278E+00
1.000E-06	1.247E+00
1.050E-06	1.221E+00
1.100E-06	1.200E+00
1.150E-06	1.184E+00
1.200E-06	1.172E+00
1.250E-06	1.163E+00
1.300E-06	1.156E+00
1.350E-06	1.151E+00
1.400E-06	1.148E+00
1.450E-06	1.145E+00
1.500E-06	1.144E+00
1.550E-06	1.142E+00
1.600E-06	1.141E+00
1.650E-06	1.141E+00
1.700E-06	1.140E+00
1.750E-06	1.140E+00
1.800E-06	1.140E+00
1.850E-06	1.140E+00
1.900E-06	1.140E+00
1.950E-06	1.139E+00
2.000E-06	1.139E+00
2.050E-06	1.139E+00