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**ELECTRONICS RESEARCH LABORATORY**

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## DYNAMIC MODEL FOR THE ANALOG MULTIPLIER

A. Baranyi and L. O. Chua<sup>†</sup>

### ABSTRACT

Under reasonable assumptions, it is shown that the dynamic behavior of an analog multiplier driven by bandlimited signals  $v_X(t)$  and  $v_Y(t)$  can be modeled by

$$v_0 = K[v_X v_Y - T_A \dot{v}_X v_Y - T_B v_X \dot{v}_Y]$$

The three model parameters  $K$ ,  $T_A$ , and  $T_B$  can be determined by frequency-domain measurements.

This simple equation can in turn be modeled by a circuit containing 2 linear capacitors, 2 linear controlled sources, and an ideal multiplier described by  $v_0 = K v_X v_Y$ .

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## I. Introduction

The four-quadrant analog multiplier [1] shown in Fig. 1 is a standard nonlinear device which has numerous applications in the field of communication, computation and measurement [2], [3], [4], [5]. The transmission properties of communication subsystems such as modulators, demodulators or equalizers built with analog multipliers are closely related to the dynamic properties of the multiplier circuit. To evaluate the signal transmission through a complex nonlinear system built with analog multipliers, we need an accurate dynamic model for the multiplier circuit.

The analog multiplier operation was analyzed by Gilbert in detail with special emphasis on the "memoryless" nonlinear distortion parameters. In his paper the transient performance was only commented but no explicit relations for the dynamic properties are given. On the manufacturer's data sheets, the frequency dependence of the multiplier circuit is often characterized by phase shift and amplitude error parameters. They are related to measurements where one of the multiplier inputs is a sinusoidal AC voltage, and the other input is a DC voltage component. These parameters are not sufficient to calculate the multiplier output when time-varying signals are applied at both inputs.

In this paper we develop a circuit-theoretic model for the analog multiplier which is valid for bandlimited input signals. The model parameters can be determined by frequency-domain measurements. This measurement will also give information on the frequency range where our model is valid.

## II. The Dynamic Model

The dynamic model presented in this section for the analog multiplier circuit represents the bilinear terms of the multiplier output, thus the nonlinear distortion, feedthrough and slew rate effects are not considered in the model.

We assume that the inputs  $v_X(t)$  and  $v_Y(t)$  are bandlimited signals with a maximum angular frequency bandwidth  $\omega_B$ ; namely,

$$v_X(t) = \frac{1}{2\pi} \int_{-\omega_B}^{\omega_B} \hat{v}_X(\omega) e^{j\omega t} d\omega \quad (1)$$

$$v_Y(t) = \frac{1}{2\pi} \int_{-\omega_B}^{\omega_B} \hat{v}_Y(\omega) e^{j\omega t} d\omega \quad (2)$$

where the symbol " $\wedge$ " denotes Fourier transform variables.

In Section IV, we show that for sufficiently small  $\omega_B$ , the multiplier output  $v_0(t)$  can be represented by a dynamic model of the following form:

$$\boxed{v_0(t) = K[v_X(t)v_Y(t) - T_A \dot{v}_X(t)v_Y(t) - T_B v_X(t)\dot{v}_Y(t)]} \quad (3)$$

where the model parameters  $K$ ,  $T_A$ , and  $T_B$  can be determined by frequency-domain measurements as discussed in section III.

The dynamic model given in (3) is based on the assumption that the maximum signal frequency  $\omega_B$  is sufficiently small so that the higher-order derivatives of the output signal may be neglected.

For computer simulation of systems containing analog multipliers, an approximate circuit model of (3) is shown in Fig. 2. Here the derivative terms are realized by capacitors connected across the respective input terminals.

The output of this circuit can be obtained by inspection:

$$\begin{aligned}
v_0(t) &= K[v_X(t) - T_A \dot{v}_X(t)][v_Y(t) - T_B \dot{v}_Y(t)] \\
&= K[v_X(t)v_Y(t) - T_A \dot{v}_X(t)v_Y(t) - T_B v_X(t)\dot{v}_Y(t) + T_A T_B \dot{v}_X(t)\dot{v}_Y(t)] \\
&\approx K[v_X(t)v_Y(t) - T_A \dot{v}_X(t)v_Y(t) - T_B v_X(t)\dot{v}_Y(t)] \quad (4)
\end{aligned}$$

The last approximation is valid if  $T_A T_B \dot{v}_X(t)\dot{v}_Y(t)$  is negligible, which is a basic assumption of our dynamic model.

For completeness we give also an exact circuit model for (3) in Fig. 3. Here two ideal multipliers are necessary and the multiplier outputs are added by an op amp circuit. The circuit equations are as follows:

$$v_{01}(t) = K[v_X(t)v_Y(t) - 2T_B v_X(t)\dot{v}_Y(t)] \quad (5a)$$

$$v_{02}(t) = K[v_X(t)v_Y(t) - 2T_A \dot{v}_X(t)v_Y(t)] \quad (5b)$$

$$\begin{aligned}
v_0(t) &= \frac{1}{2} [v_{01}(t) + v_{02}(t)] \\
&= K[v_X(t)v_Y(t) - T_A \dot{v}_X(t)v_Y(t) - T_B \dot{v}_Y(t)v_X(t)] \quad (6)
\end{aligned}$$

### III. Measurement of the Model Parameters

The model parameters,  $K$ ,  $T_A$  and  $T_B$  can be measured by applying a DC voltage at one of the input ports and a swept-frequency sinusoidal signal at the other input port, and then measuring the phase shift and the amplitude response relative of the AC signals.

Let  $v_X$  be the DC voltage and  $v_Y$  the swept-frequency AC signal:

$$v_X(t) = V_{X0}, \quad v_Y(t) = V_{Y1} e^{j\omega t} \quad (7)$$

Substituting (7) into (3), we obtain

$$v_0(t) = K V_{X0} V_{Y1} e^{j\omega t} (1 - j\omega T_B) \quad (8)$$

The voltage gain  $A_Y$ , phase shift  $\phi_Y$ , and group delay  $\tau_Y$  can be expressed as follows:

$$A_Y(\omega) = KV_{X0} \sqrt{1 + \omega^2 T_B^2} \quad (9)$$

$$\phi_Y(\omega) = \arctan(\omega T_B) \quad (10)$$

$$\tau_Y(\omega) = \frac{T_B}{1 + \omega^2 T_B^2} \quad (11)$$

The parameters  $K$  and  $T_B$  can be calculated from the zero-frequency values of the voltage gain and the phase-slope (or the group delay) characteristics:

$$K = \frac{A_Y(0)}{V_{X0}} \quad (12)$$

$$T_B = \lim_{\omega \rightarrow 0} \frac{\phi_Y(\omega)}{\omega} = \tau_Y(0) \quad (13)$$

The time constant  $T_A$  can be measured in a similar way by applying a DC voltage at port  $Y$  and a swept-frequency AC signal at port  $X$ , and then measuring the zero-frequency phase slope or group delay between the  $X$  and the output ports respectively:

$$T_A = \lim_{\omega \rightarrow 0} \frac{\phi_X(\omega)}{\omega} = \tau_X(0) \quad (14)$$

From the measurement outlined above we can also determine the frequency range in which our dynamic model is valid by comparing the measured and the predicted characteristics computed from (9)-(11).

Using the results in section IV, the signs (positive or negative) of the model parameters  $T_A$  and  $T_B$  may be determined either from the "zero" in the differential-input amplifier transfer function, or from the "pole" corresponding to the parallel RC load impedance. In the former case the model will be valid over a relatively wider frequency range because the zero corresponds directly to a "time-domain" derivative, whereas the pole corresponds to a derivative calculated from a Taylor-series approximation.

As a rule of thumb, it can be stated that our model is valid over the frequency band where the phase characteristic is linear and the amplitude distortion is negligible.

It should be noted that the phase error defined in (10) is usually given in the manufacturer's data sheets for some specific loading conditions. Consequently, under these same loading conditions, the model parameters can be calculated directly from the device specifications. As an example we calculate the model parameters for the analog multiplier type MC 1495. On the data sheet the following parameters are given (for DC currents  $I_X = I_Y = 1\text{mA}$ , load resistance  $R_L = 11\text{K}\Omega$ , and differential-amplifier resistances  $R_X = R_Y = 15\text{K}\Omega$ ):

- (a)  $3^\circ$  relative phase shift between  $v_X$  and  $v_Y$  at 750 kHz.
- (b) 1% absolute error<sup>†</sup> due to input-output phase shift at 30 kHz.

From these parameters the following model constants can be calculated:

$$T_A = \frac{0.01}{2\pi \cdot 30 \cdot 10^3} = 53\text{ns}$$

$$T_B - T_A = \frac{3\pi}{180 \cdot 2\pi \cdot 750 \cdot 10^3} = 11\text{ns}$$

$$T_B = 53\text{ns} + 11\text{ns} = 64\text{ns}$$

The analog multiplier (MC 1495L) circuit shown in Fig. 1 was also simulated with the SPICE program [7] at the operating point  $I_X = I_Y = 1\text{mA}$ . The following typical integrated transistor model parameters are used: collector-base capacitance  $C_j = 0.6\text{pF}$  substrate capacitance  $C_s = 1.5\text{pF}$ , base resistance  $r_b = 100\Omega$ , forward transit time  $T = 0.6\text{ns}$ . For the stray capacitances, we pick  $C_X = C_Y = 1\text{pF}$

<sup>†</sup>The 1% "absolute error" in the data sheet means 1% "vector" error which corresponds to a 0.01 radian phase difference.

and  $C_L = 3\text{pF}$ . Different external load resistances were used in the computer simulation.

The model parameters  $K$ ,  $T_A$ , and  $T_B$  calculated from the simulated characteristics are given in Table 1 and Table 2, respectively. The simulated X-channel amplitude and phase responses for  $R_X = R_Y = 15\text{K}$  and  $R_L = 1\text{K}$  are shown in Figs. 4 and 5, respectively. They agree reasonably well with that predicted by (9) and (10) up to a frequency of 3 MHz.

Table 1. Model parameters obtained from computer simulation with  $R_X = R_Y = 15\text{K}$ .

$R_L$	$K$	$T_A$	$T_B$
11K	$9.4 \times 10^{-2}(\text{Volt})^{-1}$	53 ns	58 ns
5K	$4.3 \times 10^{-2}(\text{Volt})^{-1}$	11 ns	13 ns
1K	$8.6 \times 10^{-2}(\text{Volt})^{-1}$	-17 ns	-16 ns

Table 2. Model parameters obtained from computer simulation with  $R_L = 50\Omega$ .

$R_X = R_Y$	$K$	$T_A$	$T_B$
1.5K	$3.9 \times 10^{-2}(\text{Volt})^{-1}$	-0.3 ns	-0.3 ns
1K	$8.3 \times 10^{-2}(\text{Volt})^{-1}$	0.5 ns	0.6 ns
0.5K	0.3 $(\text{Volt})^{-1}$	1.8 ns	1.9 ns

The amplitude and phase characteristics corresponding to the load resistance  $R_L = 50\Omega$  have also been measured in an experimental setup.

A considerable feedthrough error due to stray couplings in the setup was observed in the measured characteristics. To eliminate the feedthrough error, an averaging procedure using both positive and negative dc input voltages is described in Appendix A.1. The measured phase slope characteristics are shown in Figs. 6, 7 and 8, respectively. The calculated model parameters are given in Table 3.

Table 3. Model parameters obtained from measurement with  $R_L = 50\Omega$ .

$R_X = R_Y$	K	$T_A$	$T_B$
1.5K	$3.8 \times 10^{-2}(\text{Volt})^{-1}$	-1.5ns	-1.1ns
1 K	$8.1 \times 10^{-2}(\text{Volt})^{-1}$	-0.4ns	0 ns
0.5K	$0.28 (\text{Volt})^{-1}$	1.2ns	1.7ns

Note that the measured and simulated characteristics are in reasonable qualitative agreement. The discrepancy may be attributed to the relatively high stray capacitances of the experimental setup.

The amplitude and phase characteristics within a frequency range of 30 MHz are shown in Figs. 9, 10, and 11. Observe that they are in reasonable agreement with (9)-(11) up to a frequency of 10 MHz, 15 MHz and 20 MHz respectively.

Finally, we remark that because of the various simplifying assumptions made in the model derivation in Section IV, the preceding model parameter determination procedure is only a approximate one. More accurate answers can be obtained by standard computer optimization techniques which minimizes the error between the characteristics predicted by our model and that measured experimentally in an actual circuit -- thereby including all stray parasitics. In this case, the parameters determined by (12)-(14) can be used as the initial parameters in the iteration procedure.

#### IV. Derivation of the Model

The circuit configuration given in Fig. 1 shows that the multiplier circuit is made up of two separate functional blocks. The block denoted by  $N_1$  is an input-voltage output-current converter realized by a differential-amplifier Darlington stages.

The output current of the differential amplifier drives the multiplier core, denoted by  $N_2$ , which is made up of six transistors ( $Q_5$  and  $Q_6$  operate as diodes). The multiplier output current is transformed into an output voltage by the load resistor  $R_L$ . In the following we calculate the transfer relation of each block separately and combine the results to develop an overall model for the multiplier circuit.

First we introduce the transistor model which will be used in the computations.

##### IV.1. Transistor Model

Our derivation of the "multiplier core" equations is based on the "charge control" transistor model [6]. Under normal operating conditions, we can assume that the transistors are operating in the forward active region with unity current gain, and the charge stored in the base-emitter junction is controlled by the forward current only.

We will neglect all capacitances normally present in a general nonlinear transistor model. The emitter-base capacitance is negligible in the analog multiplier because the transistors are forward biased. The collector-base and substrate capacitances are not negligible. However, it can be shown that the effects contributed by these capacitances can be included into the "stray" capacitances across the load resistances to be discussed in Section IV.4.

The transistor model corresponding to the above assumptions is shown in Fig. 6 where the notation  $f(v)$  is used for the exponential term and  $T$  denotes the inverse of the transistor cutoff frequency.

#### IV.2. Input differential-amplifier model

Consider the block labeled  $N_1$  in Fig. 1. Note that the emitter current of the Darlington stage is provided by a current-mirror arrangement and the transistors in the Darlington stage have sufficiently high  $\beta$  values such that the transistor parameters can be neglected in the computation of the transfer relation. The simplified equivalent circuit of the X-channel input amplifier is shown in Fig. 7. Here  $I_X$  is the constant current of the current source,  $R_X$  is an externally connected resistor,  $C_X$  represents the stray capacitance associated with the current source  $I_X$  and the resistor  $R_X$ . In practical applications, the resistor  $R_X$  is sufficiently large so the linear relation between  $i_X$  and  $v_X$  can be approximated by the equation

$$I_X(s) = \frac{V_X(s)}{Z(s)} = \frac{V_X(s)}{R_X} (1+sT_X) \quad (15a)$$

where  $T_X$  is the time constant  $R_X C_X$ . The frequency-domain equation (15a) corresponds to the time-domain relation of the following form:

$$i_X(t) = \frac{1}{R_X} [v_X(t) + T_X \dot{v}_X(t)] \quad (15b)$$

A similar expression can be derived for the AC current component  $i_Y(t)$  feeding the Y-input of the multiplier section:

$$i_Y(t) = \frac{1}{R_Y} [v_Y(t) + T_Y \dot{v}_Y(t)] \quad (16)$$

where  $T_Y$  is the time constant  $R_Y C_Y$ .

### IV.3. Multiplier Core Model

The circuit configuration of the multiplier core is repeated in Fig. 8. In the computation of the output current  $i_z(t)$  we use the transistor model given in Fig. 6. We introduce the operator  $D$  for  $T \frac{d}{dt}$  and we note that for bandlimited signals as defined in (1) and (2), the operator  $D$  has the following norm [8]:

$$\|D\| = \omega_B T$$

Since we are interested in the frequency range which is much smaller than the transistor cutoff frequency, we can assume

$$\|D\| \ll 1 \tag{17}$$

The Kirchhoff equations of the multiplier section can be written by inspection as follows:

$$v_1 - v_2 = v_5 - v_6 \tag{18}$$

$$v_4 - v_3 = v_5 - v_6 \tag{19}$$

$$(\mathcal{I}+D)(f_1+f_2) = I_X + i_X \tag{20}$$

$$(\mathcal{I}+D)(f_3+f_4) = I_X - i_X \tag{21}$$

$$(\mathcal{I}+D)f_5 - D(f_2+f_3) = I_Y + i_Y \tag{22}$$

$$(\mathcal{I}+D)f_6 - D(f_1+f_4) = I_Y - i_Y \tag{23}$$

where  $\mathcal{I}$  denotes the "Identity" operator, and  $f_k$  denotes  $f(v_k)$ . Using the relationship

$$\frac{f_j}{f_k} = e^{\lambda(v_j - v_k)} \tag{24}$$

Equations (18) and (19) can be rewritten in the form

$$\frac{f_1}{f_2} = \frac{f_5}{f_6} \quad (25)$$

$$\frac{f_4}{f_3} = \frac{f_5}{f_6} \quad (26)$$

We want to calculate the output current  $i_z(t)$  given by the equation

$$2i_z(t) = (f_1+f_3) - (f_2+f_4) \quad (27)$$

Recognizing the fact that for  $\|D\| \ll 1$ ,  $(\mathcal{Q}+D)^{-1}$  can be approximated by  $(\mathcal{Q}-D)$ , we can solve for  $(f_1+f_2)$  and  $(f_3+f_4)$  from (20) and (21) as follows [8]:

$$(f_1+f_2) = I_X + (\mathcal{Q}-D)i_X \quad (28)$$

$$(f_3+f_4) = I_X - (\mathcal{Q}-D)i_X \quad (29)$$

Using (25), we can express  $f_1$  and  $f_2$  in terms of  $(f_1+f_2)$ :

$$f_1 = \frac{f_5}{f_5+f_6} (f_1+f_2) \quad (30)$$

$$f_2 = \frac{f_6}{f_5+f_6} (f_1+f_2) \quad (31)$$

Similarly, using (26), we can express  $f_3$  and  $f_4$  in terms of  $(f_3+f_4)$ :

$$f_3 = \frac{f_6}{f_5+f_6} (f_3+f_4) \quad (32)$$

$$f_4 = \frac{f_5}{f_5+f_6} (f_3+f_4) \quad (33)$$

Using (30)-(33) the output current can be expressed as follows

$$2i_z = \frac{f_5-f_6}{f_5+f_6} [(f_1+f_2) - (f_3+f_4)] \quad (34)$$

Adding (22) and (23) we obtain

$$(\mathcal{Q}+D)(f_5+f_6) - D(f_1+f_2+f_3+f_4) = 2I_Y \quad (35)$$

Now, the sum of (20) and (21) gives

$$(\mathcal{D}+D)(f_1+f_2+f_3+f_4) = 2I_X \quad (36)$$

Since this equation must hold for all times, it follows that

$$D(f_1+f_2+f_3+f_4) = 0 \quad (37)$$

and

$$f_1 + f_2 + f_3 + f_4 = 2I_X \quad (38)$$

Substituting (37) into (35) and using a similar reasoning, we obtain

$$D(f_5+f_6) = 0 \quad (39)$$

and

$$f_5 + f_6 = 2I_Y \quad (40)$$

Let us derive next a relationship for  $(f_5-f_6)$  which will be needed later. Subtracting (23) from (22), we obtain

$$(\mathcal{D}+D)(f_5-f_6) - D(f_1-f_2-f_3+f_4) = 2i_Y \quad (41)$$

Using (30)-(33), we obtain

$$f_1 - f_2 - f_3 + f_4 = \frac{f_5-f_6}{f_5+f_6} [f_1+f_2 + f_3 + f_4] \quad (42)$$

Substituting (38) and (40) into (42), we obtain

$$f_1 - f_2 - f_3 + f_4 = \frac{I_X}{I_Y} (f_5-f_6) \quad (43)$$

Substituting (43) into (41), we obtain

$$\left[ \mathcal{D} + \left(1 + \frac{I_X}{I_Y}\right)D \right] (f_5-f_6) = 2i_Y \quad (44)$$

Using again the operator inversion formula

$$f_5 - f_6 = \left[ \mathcal{D} - \left(1 + \frac{I_X}{I_Y}\right)D \right] (2i_Y) \quad (45)$$

and substituting (28), (29), (40) and (45) into (34), we obtain

$$2i_Z = \frac{1}{2I_Y} \left[ \mathcal{Q} - \left( 1 + \frac{I_X}{I_Y} \right) D \right] (2i_Y) [\mathcal{Q} - D] (2i_X) \quad (46)$$

Equation (46) gives  $i_Z$  in terms of the two operators  $\mathcal{Q}$  and  $D \triangleq T \frac{d}{dt}$ . If we replace  $\mathcal{Q}$  and  $D$  by their defined operations and neglect all higher-order and/or product terms involving  $\dot{i}_X$  and  $\dot{i}_Y$  (in view of (17)), we would obtain

$$i_Z(t) = \frac{1}{I_Y} [i_X(t)i_Y(t) - T_1 \dot{i}_X(t)i_Y(t) - T_2 i_X(t)\dot{i}_Y(t)] \quad (47)$$

where

$$T_1 \triangleq T \quad (48)$$

and

$$T_2 \triangleq \left( 1 + \frac{I_X}{I_Y} \right) T \quad (49)$$

#### IV.4. Output impedance model

The multiplier current is transformed into an output voltage by the load impedance  $R_L$  in parallel with some parasitic stray capacitance  $C_L$ . The capacitance  $C_L$  includes not only the external stray capacitances, but also the equivalent capacitance due to the collector-base and substrate capacitances which we have neglected from the transistor model.

In the frequency domain the transfer relation is expressed by the transfer function of the parallel RC impedance

$$V_O(s) = \frac{2R_L}{1+sR_L C_L} I_Z(s) \quad (50)$$

For sufficiently low-frequency inputs the transfer function can be expanded into a Taylor-series about the origin

$$V_O(s) = 2R_L [1 - sT_L + s^2 T_L^2 - \dots] I_Z(s) \quad (51)$$

where  $T_L = R_L C_L$ .

The first two terms in (51) correspond to the following approximate time-domain equation

$$v_0(t) = 2R_L [i_Z(t) - T_L \dot{i}_Z(t)] \quad (52)$$

The neglected terms in the frequency-domain Taylor series expansion (51) would of course result in an error in the time domain. This can be neglected if the input frequency is sufficiently small.

#### IV.5. Complete model of the analog multiplier

The complete model of the analog multiplier can now be obtained by substituting (15b) and (16) into (47) and then putting the resulting relation into (52). Again, retaining only first-order terms involving  $\dot{i}_X$  and  $\dot{i}_Y$ , we obtain

$$\begin{aligned} v_0(t) &= \frac{2R_L}{I_Y} \left[ i_X(t)i_Y(t) - T_1 \dot{i}_X(t)i_Y(t) - T_2 i_X(t)\dot{i}_Y(t) - T_L \dot{i}_X(t)i_Y(t) \right. \\ &\quad \left. - T_L i_X(t)\dot{i}_Y(t) \right] \\ &= \frac{2R_L}{I_Y R_X R_Y} [v_X(t)v_Y(t) + T_X \dot{v}_X(t)v_Y(t) + T_Y v_X(t)\dot{v}_Y(t) - T_1 \dot{v}_X(t)v_Y(t) \\ &\quad - T_2 v_X(t)\dot{v}_Y(t) - T_L \dot{v}_X(t)v_Y(t) - T_L v_X(t)\dot{v}_Y(t)] \end{aligned} \quad (53)$$

This can be simplified as follows:

$$v_0(t) = K[v_X(t)v_Y(t) - T_A \dot{v}_X(t)v_Y(t) - T_B v_X(t)\dot{v}_Y(t)] \quad (54)$$

where

$$K = \frac{2R_L}{I_Y R_X R_Y} \quad (55)$$

$$T_A \triangleq T_1 + T_L - T_X \quad (56)$$

$$T_B \triangleq T_2 + T_L - T_Y \quad (57)$$

In actual operation, the time constants  $T_A$  and  $T_B$  are determined by the external elements  $R_L$ ,  $R_X$ ,  $R_Y$  and the associated stray capacitances  $C_L$ ,  $C_X$  and  $C_Y$ , respectively. Because of the presence of stray capacitances, the time constants of the "multiplier core" give only a lower bound on the performance limit.

#### V. Concluding Remarks

We have presented a simple dynamic model for the analog multiplier which can be used for computer simulation of complex communication subsystems containing analog multipliers. The model parameters can be determined by frequency-domain measurements. We have measured these parameters and also calculated them from computer simulation of the complete analog multiplier circuit. The results agree reasonably well over the frequency range of interest.

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## APPENDIX

### A.1. Elimination of Feedthrough Error in Model Parameter Measurements

In addition to the bilinear product terms in an ideal multiplier, the output of a "physical" multiplier normally contains also a number of feedthrough terms such as  $F_A v_X(t)$ ,  $F_B v_Y(t)$ ,  $G_A \dot{v}_X(t)$ ,  $G_B \dot{v}_Y(t)$ , etc. These extraneous terms could cause significant errors in model parameter measurements. As shown below, these errors can be eliminated if the measurements are made with both positive and negative dc voltages, and then averaging the respective measured parameter values.

A more realistic multiplier model which includes feedthrough terms is given by:

$$v_0(t) = K[v_X(t) v_Y(t) - T_A \dot{v}_X(t) v_Y(t) - T_B \dot{v}_Y(t) v_X(t) + F_A v_X(t) + F_B v_Y(t) + G_A \dot{v}_X(t) + G_B \dot{v}_Y(t)] \quad (A1)$$

Using the input signals given in (7) with positive and negative dc voltages  $V_{X0}$  and  $-V_{X0}$ , we obtain the following output voltages:

$$v_0^+(t) = F_A V_{X0} + [K V_{X0} (1-j\omega T_B) + F_B + j\omega G_B] V_{Y1} e^{j\omega t} \quad (A2)$$

$$v_0^-(t) = -F_A V_{X0} - [K V_{X0} (1-j\omega T_B) - F_B - j\omega G_B] V_{Y1} e^{j\omega t} \quad (A3)$$

The respective voltage gains  $A_Y^+$ ,  $A_Y^-$ , phase shifts  $\phi_Y^+$ ,  $\phi_Y^-$ , and group delays  $\tau_Y^+$ ,  $\tau_Y^-$  can be expressed in the form:

$$A_Y^+(\omega) = (K V_{X0} \pm F_B)^2 + (K V_{X0} T_B \mp G_B)^2 \omega^2 \quad (A4)$$

$$\phi_Y^+(\omega) = \arctan \frac{(K V_{X0} T_B \mp G_B)\omega}{K V_{X0} \pm F_B} \quad (A5)$$

$$\tau_Y^+(\omega) = \frac{K V_{X0} T_B \mp G_B}{1 + \omega^2 \left( \frac{K V_{X0} T_B \mp G_B}{K V_{X0} \pm F_B} \right)} \quad (A6)$$

The model parameters  $K$  and  $T_B$  can be calculated from the average zero-frequency values of the voltage gain and phase slope (or the group delay) characteristics:

$$K = \frac{A_Y^+(0) + A_Y^-(0)}{2} \quad (A7)$$

$$T_B = \lim_{\omega \rightarrow 0} \frac{\phi_Y^+(\omega) + \phi_Y^-(\omega)}{2\omega} = \frac{\tau_Y^+(0) + \tau_Y^-(0)}{2} \quad (A8)$$

The feedthrough error in the measurement of the time constant  $T_A$  can be eliminated in a similar way by applying positive and negative dc voltages at port Y and measuring the average zero-frequency phase-slope (or group delay) between the X and the output ports, respectively:

$$T_A = \lim_{\omega \rightarrow 0} \frac{\phi_X^+(\omega) + \phi_X^-(\omega)}{2\omega} = \frac{\tau_X^+(0) + \tau_X^-(0)}{2} \quad (A9)$$

From the difference between the zero-frequency values of the respective voltage gain and group delay characteristics, the feedthrough parameters  $F_A$ ,  $F_B$ ,  $G_A$ , and  $G_B$  can also be calculated using the following relation:

$$F_A = \frac{A_X^+(0) - A_X^-(0)}{2} \quad (A10)$$

$$F_B = \frac{A_Y^+(0) - A_Y^-(0)}{2} \quad (A11)$$

$$G_A = \lim_{\omega \rightarrow 0} \frac{\phi_Y^+(0) - \phi_Y^-(0)}{2\omega} = \frac{\tau_Y^+(0) - \tau_Y^-(0)}{2} \quad (A12)$$

$$G_B = \lim_{\omega \rightarrow 0} \frac{\phi_X^+(0) - \phi_X^-(0)}{2\omega} = \frac{\tau_X^+(0) - \tau_X^-(0)}{2} \quad (A13)$$

## A.2. Effects of Parasitic Capacitances

In Section IV.4 we have neglected the transistor collector-base and substrate capacitances and claimed that their effects can be included into the stray capacitances across the load resistors. In the following we will justify this claim.

Consider Fig. A1 where  $C_s$  and  $C_j$  denote the "substrate" and the "collector-base" junction capacitances of the transistors in the multiplier core. The inputs are loaded by capacitances  $C_I$  which includes the substrate capacitances of the differential amplifier transistors, and the collector-base capacitances of the input transistors in the Darlington configuration -- which are at virtual ground in view of the voltage source input. Hence, we have

$$C_I = 2C_s + C_j \quad (A14)$$

Since the substrate capacitances  $C_s$  are already in parallel with the load resistors, it suffices to analyze only  $C_j$ .

Since the parasitic capacitances contribute only to the derivative terms in our model, we can evaluate their effects by perturbation method. Here, we assume that the voltages across the parasitic capacitances are determined by the memoryless terms in the original multiplier core equations as given in (20)-(27) and (50).

The effect of the parasitic capacitances  $C_I$  and  $C_j$  can be calculated in two steps. First, we assume that the ac emitter-base voltages are sufficiently small to be neglected so that the input capacitances  $C_I$  have no effect on the multiplier dynamics. Hence, the junction capacitances  $C_j$  can be calculated as follows:

$$C_j \frac{d}{dt} (v_{j10}) = C_j \frac{d}{dt} (v_{j30}) = -C_j R_L \frac{d}{dt} (f_1 + f_3) \quad (A15)$$

$$C_j \frac{d}{dt} (v_{j20}) = C_j \frac{d}{dt} (v_{j40}) = -C_j R_L \frac{d}{dt} (f_2 + f_4) \quad (A16)$$

Here the subscript "zero" indicates that the emitter-base voltages have been neglected.

Including the current terms given by (A15) and (A16) into the multiplier core equations, we obtain:

$$(\mathcal{Q} + D)f_5 - D(f_2 + f_3) + C_j R_L \frac{d}{dt} (f_1 + f_2 + f_3 + f_4) = I_Y + i_Y \quad (A17)$$

$$(\mathcal{Q} + D)f_6 - D(f_1 + f_4) + C_j R_L \frac{d}{dt} (f_1 + f_2 + f_3 + f_4) = I_Y - i_Y \quad (A18)$$

$$2i_z = (f_1 + f_3 - f_2 - f_4) - C_j R_L \frac{d}{dt} (f_1 + f_3 - f_2 - f_4) \quad (A19)$$

It follows from (37) that the junction current contributions in (A17) and (A18) are zero.

Thus only the output current will be affected as in (A.19). This equation, however, corresponds to the fact that  $C_j$  is connected across the load resistance  $R_L$  as stated in Section IV.4.

Consider next the effect of the non-zero emitter-base voltages. From Fig. A1, we observe that the  $v_{jk}$  junction capacitance voltages will deviate from  $v_{jko}$  due to the base-emitter voltages:

$$\Delta v_{j1} = \Delta v_{j4} = v_6 \quad (A20)$$

$$\Delta v_{j2} = \Delta v_{j3} = v_5 \quad (A21)$$

The multiplier core equation can be written by inspection:

$$(\mathcal{Q} + D)(f_1 + f_2) = I_X + i_X + C_I \frac{d}{dt} (-v_1 - v_6) \quad (A22)$$

$$(\mathcal{Q} + D)(f_3 + f_4) = I_X - i_X + C_I \frac{d}{dt} (-v_3 - v_5) \quad (A23)$$

$$(\mathcal{G} + D)f_5 - D(f_2 + f_3) = I_Y + i_Y + (C_I + C_j) \frac{d}{dt} (-v_5) \quad (\text{A24})$$

$$(\mathcal{G} + D)f_6 - D(f_1 + f_4) = I_Y - i_Y + (C_I + C_j) \frac{d}{dt} (-v_6) \quad (\text{A25})$$

The output current can be written in the form:

$$2i_z = (f_1 + f_3 - f_2 - f_4) - C_j \frac{d}{dt} (v_5 + v_6 + v_5 + v_6) \quad (\text{A26})$$

To calculate the additional current terms in (A.22)-(A.26), we use the static values of the base-emitter voltages because they will result in the correct first-order derivatives which are necessary in our model. The static voltage components  $v_k^*$  are calculated from the static multiplier core currents  $f_k^*$  as defined below (corresponding to (20)-(23) and (25)-(27) without differentiation operations:

$$f_1^* + f_2^* = I_X + i_X \quad (\text{A27})$$

$$f_3^* + f_4^* = I_X - i_X \quad (\text{A28})$$

$$\frac{f_1^*}{f_2^*} = \frac{f_4^*}{f_3^*} = \frac{f_5^*}{f_6^*} \quad (\text{A29})$$

$$f_5^* = I_Y + i_Y \quad (\text{A30})$$

$$f_6^* = I_Y - i_Y \quad (\text{A31})$$

The following solutions of the static current equations are obtained after some algebraic manipulations:

$$f_1^* = \frac{(I_X + i_X)(I_Y + i_Y)}{2I_Y} \quad (\text{A32})$$

$$f_2^* = \frac{(I_X + i_X)(I_Y - i_Y)}{2I_Y} \quad (\text{A33})$$

$$f_3^* = \frac{(I_X - i_X)(I_Y - i_Y)}{2I_Y} \quad (A34)$$

$$f_4^* = \frac{(I_X - i_X)(I_Y + i_Y)}{2I_Y} \quad (A35)$$

$$f_5^* = (I_Y + i_Y) \quad (A36)$$

$$f_6^* = (I_Y - i_Y) \quad (A37)$$

Using the exponential characteristics defined in Fig. 6, the base-emitter voltage derivatives can be calculated as follow:

$$\frac{d}{dt} (v_1^*) = \frac{1}{\lambda} \left[ \frac{\dot{i}_X}{I_X + i_X} + \frac{\dot{i}_Y}{I_Y + i_Y} \right] \quad (A38)$$

$$\frac{d}{dt} (v_2^*) = \frac{1}{\lambda} \left[ \frac{\dot{i}_X}{I_X + i_X} - \frac{\dot{i}_Y}{I_Y - i_Y} \right] \quad (A39)$$

$$\frac{d}{dt} (v_3^*) = \frac{1}{\lambda} \left[ \frac{-\dot{i}_X}{I_X - i_X} - \frac{\dot{i}_Y}{I_Y - i_Y} \right] \quad (A40)$$

$$\frac{d}{dt} (v_4^*) = \frac{1}{\lambda} \left[ \frac{-\dot{i}_X}{I_X - i_X} + \frac{\dot{i}_Y}{I_Y + i_Y} \right] \quad (A41)$$

$$\frac{dv_5^*}{dt} = \frac{1}{\lambda} \left[ \frac{\dot{i}_Y}{I_Y + i_Y} \right] \quad (A42)$$

$$\frac{dv_6^*}{dt} = \frac{1}{\lambda} \left[ \frac{-\dot{i}_Y}{I_Y - i_Y} \right] \quad (A43)$$

Substituting (A38) - (A43) into (A22) - (A25), we obtain:

$$(\mathcal{Q} + D)(f_1 + f_2) = I_X + i_X - \frac{C_I}{\lambda} \left[ \frac{\dot{i}_X}{I_X + i_X} \right] \quad (A44)$$

$$(\mathcal{Q} + D)(f_3 + f_4) = I_X - i_X + \frac{C_I}{\lambda} \left[ \frac{\dot{i}_X}{I_X + i_X} \right] \quad (A45)$$

$$(\mathcal{G} + D) f_5 - D(f_2 + f_3) = I_Y + i_y + \frac{C_I + C_j}{\lambda} \left( \frac{-\dot{i}_Y}{I_Y - i_Y} \right) \quad (\text{A46})$$

$$(\mathcal{G} + D) f_6 - D(f_1 + f_4) = I_Y - i_y + \frac{C_I + C_j}{\lambda} \frac{\dot{i}_Y}{I_Y + i_Y} \quad (\text{A47})$$

$$2 i_z = f_1 + f_2 + f_3 + f_4 + C_j \frac{d}{dt} [0] \quad (\text{A48})$$

Assuming that  $i_y < I_Y$  and  $i_x < I_X$ , the above equations can be interpreted as if the inputs  $i_x$  and  $i_y$  were replaced by  $i_x - \frac{C_I i_x}{\lambda I_X}$  and  $i_y - \frac{(C_I + C_j) i_y}{\lambda I_Y}$ , respectively. Hence, the multiplier output current can be calculated by substituting the modified input currents into the original output current equation (47):

$$i_z(t) = \frac{1}{I_Y} \left[ \left( i_x(t) - \frac{C_I i_x(t)}{\lambda I_X} \right) \left( i_y(t) - \frac{C_I + C_j}{\lambda} \frac{\dot{i}_Y}{I_Y} \right) - T_1 \dot{i}_x(t) i_y(t) - T_2 \dot{i}_x(t) \dot{i}_y(t) \right] \quad (\text{A49})$$

Carrying out the multiplication inside the bracket and neglecting the product term  $\dot{i}_x(t) \dot{i}_y(t)$  we obtain the original expression but with a modified time constants:

$$T_1' = T_1 + \frac{C_I}{\lambda I_X} \quad (\text{A50})$$

$$T_2' = T_2 + \frac{C_I + C_j}{\lambda I_Y} \quad (\text{A51})$$

This change in the time constants will cause a corresponding change in the overall expressions for  $T_A$  and  $T_B$ ; namely,

$$T_A' = T_A + \frac{C_I}{I_X} \Delta T_A + \Delta T_A \quad (\text{A52})$$

$$T'_B = T_B + \frac{C_I + C_j}{\lambda I_Y} \Delta T_B \triangleq T_B + \Delta T_B \quad (\text{A53})$$

For a typical multiplier circuit with  $C_S = 1.5$  pF,  $C_j = 0.5$  pF and  $I_X = I_Y = I$  mA, we obtain from (14):

$$\begin{aligned} C_I &= 3.5 \text{ pF} & , & & C_I + C_j &= 4 \text{ pF} \\ \Delta T_A &= 0.09 \text{ ns} & , & & \Delta T_B &= 0.1 \text{ ns}. \end{aligned}$$

## FIGURE CAPTIONS

- Fig. 1. A typical 4-quadrant analog multiplier circuit.
- Fig. 2. An approximate circuit model for the dynamic analog multiplier model described by (3).
- Fig. 3. An exact circuit model for the dynamic analog multiplier model described by (3).
- Fig. 4. Simulated X-channel amplitude characteristic.
- Fig. 5. Simulated X-channel phase characteristic.
- Fig. 6. Phase characteristics with  $R_L = 50 \Omega$ ,  $R_X = R_Y = 1.5 \text{ K}$ .

Horizontal : 1 MHz per division

Vertical scale :  $10^\circ$  per division.

$$(a) \quad V_{Y0} = 1.5 \text{ V}$$

$$\frac{\phi_X^+(\omega)}{\omega} = -0.6^\circ/\text{MHz}$$

$$(c) \quad V_{X0} = 1.5 \text{ V}$$

$$\frac{\phi_Y^+(\omega)}{\omega} = +0.3^\circ/\text{MHz}$$

$$(b) \quad V_{Y0} = -1.5 \text{ V}$$

$$\frac{\phi_X^-(\omega)}{\omega} = 1.7^\circ/\text{MHz}$$

$$(d) \quad V_{X0} = -1.5 \text{ V}$$

$$\frac{\phi_Y^-(\omega)}{\omega} = 0.6^\circ/\text{MHz}$$

- Fig. 7. Phase characteristics with  $R_L = 50 \Omega$ ,  $R_X = R_Y = 1 \text{ K}$ .

Horizontal scale : 1 MHz per division

Vertical scale :  $10^\circ$  per division

$$(a) \quad V_{X0} = 1 \text{ V}$$

$$\frac{\phi_X^+(\omega)}{\omega} = -0.8^\circ/\text{MHz}$$

$$(c) \quad V_{Y0} = 1 \text{ V}$$

$$\frac{\phi_Y^+(\omega)}{\omega} = -0.1^\circ/\text{MHz}$$

$$(b) \quad V_{X0} = -1 \text{ V}$$

$$\frac{\phi_X^-(\omega)}{\omega} = 0.9^\circ/\text{MHz}$$

$$(d) \quad V_{Y0} = -1 \text{ V}$$

$$\frac{\phi_Y^-(\omega)}{\omega} = 0.1^\circ/\text{MHz}$$

Fig. 8. Phase characteristics with  $R_L = 50 \Omega$ ,  $R_X + R_Y = 0.5 K$ .

Horizontal : 1 MHz per division

Vertical scale :  $10^\circ$  per division.

(a)  $V_{Y0} = 0.5 V$

$$\frac{\phi_X^+(\omega)}{\omega} = 1^\circ/\text{MHz}$$

(c)  $V_{X0} = 0.5 V$

$$\frac{\phi_Y^+(\omega)}{\omega} = -0.6^\circ/\text{MHz}$$

(b)  $V_{Y0} = -0.5 V$

$$\frac{\phi_X^-(\omega)}{\omega} = 0.1^\circ/\text{MHz}$$

(d)  $V_{X0} = -0.5 V$

$$\frac{\phi_Y^-(\omega)}{\omega} = -0.6^\circ/\text{MHz}$$

Fig. 9. Amplitude characteristic (upper curve) and phase characteristic (lower curve) with  $R_L = 50 \Omega$ ,  $R_X = R_Y = 1.5 K$ .

Horizontal : 3 MHz per division

Vertical scale : 1 dB per division,  $10^\circ$  per division

(a)  $V_{Y0} = 1.5 V$

(c)  $V_{X0} = 1.5 V$

(b)  $V_{Y0} = -1.5 V$

(d)  $V_{X0} = -1.5 V$

Fig. 10. Amplitude characteristic (upper curve) and phase characteristic (lower curve) with  $R_L = 50 \Omega$ ,  $R_X = R_Y = 1 K$ .

Horizontal : 3 MHz per division

Vertical scale : 1 dB per division,  $10^\circ$  per division

(a)  $V_{Y0} = 1.5 V$

(c)  $V_{X0} = 1.5 V$

(b)  $V_{Y0} = -1.5 V$

(d)  $V_{X0} = 1.5 V$

Fig. 11. Amplitude characteristic (upper curve) and phase characteristic (lower curve) with  $R_L = 50 \Omega$ ,  $R_X = R_Y = 0.5 K$ .

Horizontal scale : 3 MHz per division

Vertical scale : 1 dB per division,  $10^\circ$  per division

(a)  $V_{Y0} = 0.5 V$

(c)  $V_{X0} = 0.5 V$

(b)  $V_{Y0} = -0.5 V$

(d)  $V_{X0} = -0.5 V$

Fig. 12. Simplified transistor circuit model.

Fig. 13. Simplified equivalent circuit of the X-channel input amplifier.

Fig. 14. The block  $N_2$  containing the multiplier core.

Fig. A.1. Multiplier core with parasitic capacitances.

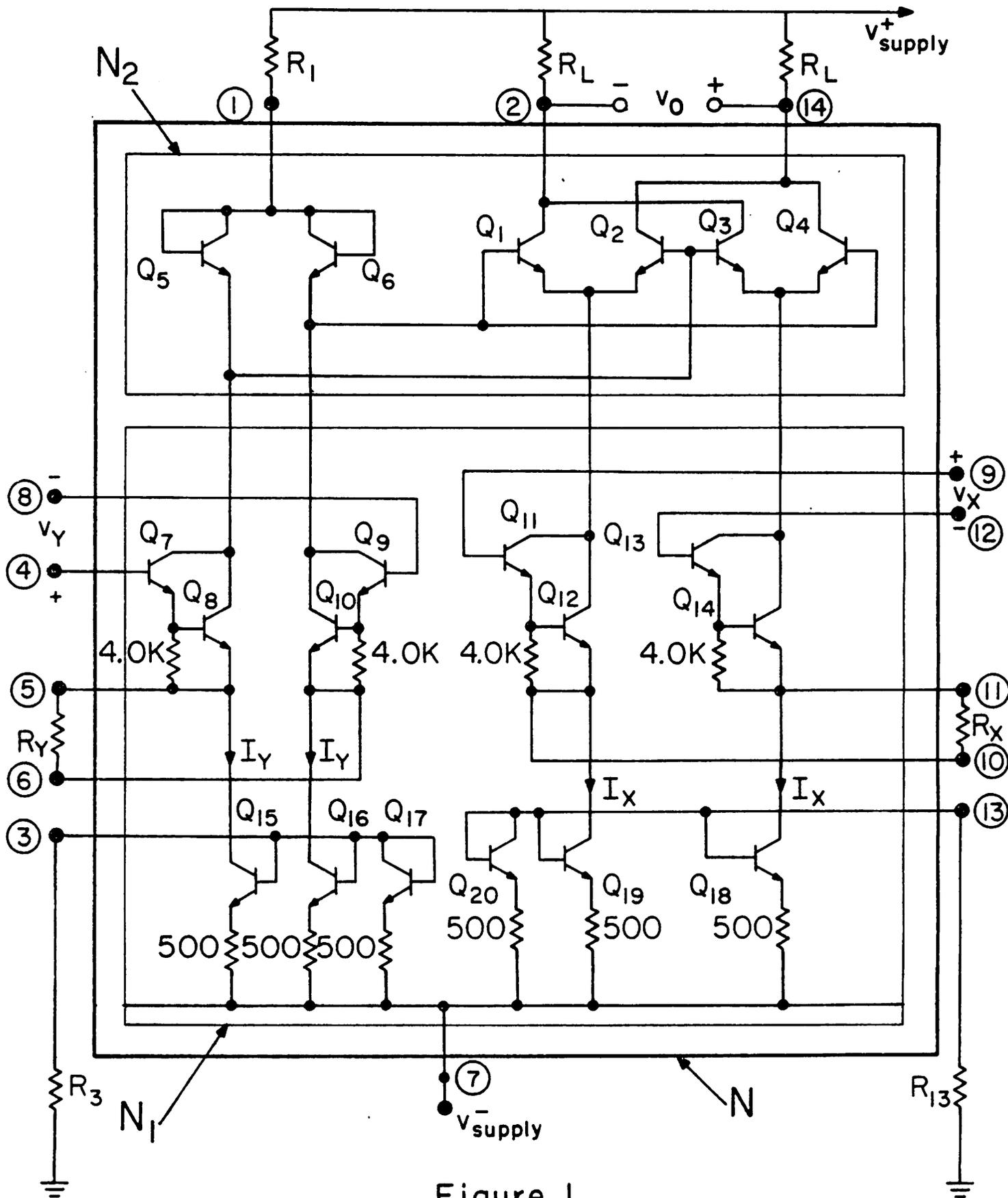


Figure 1

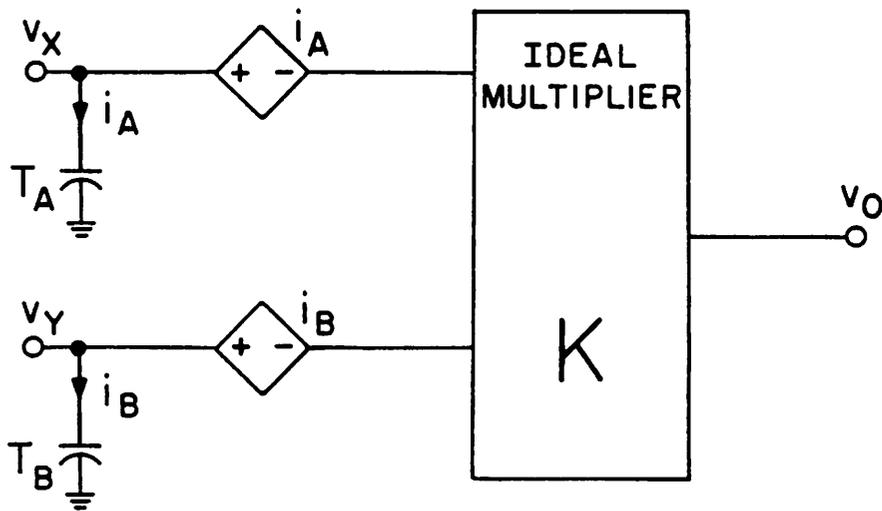


Figure 2

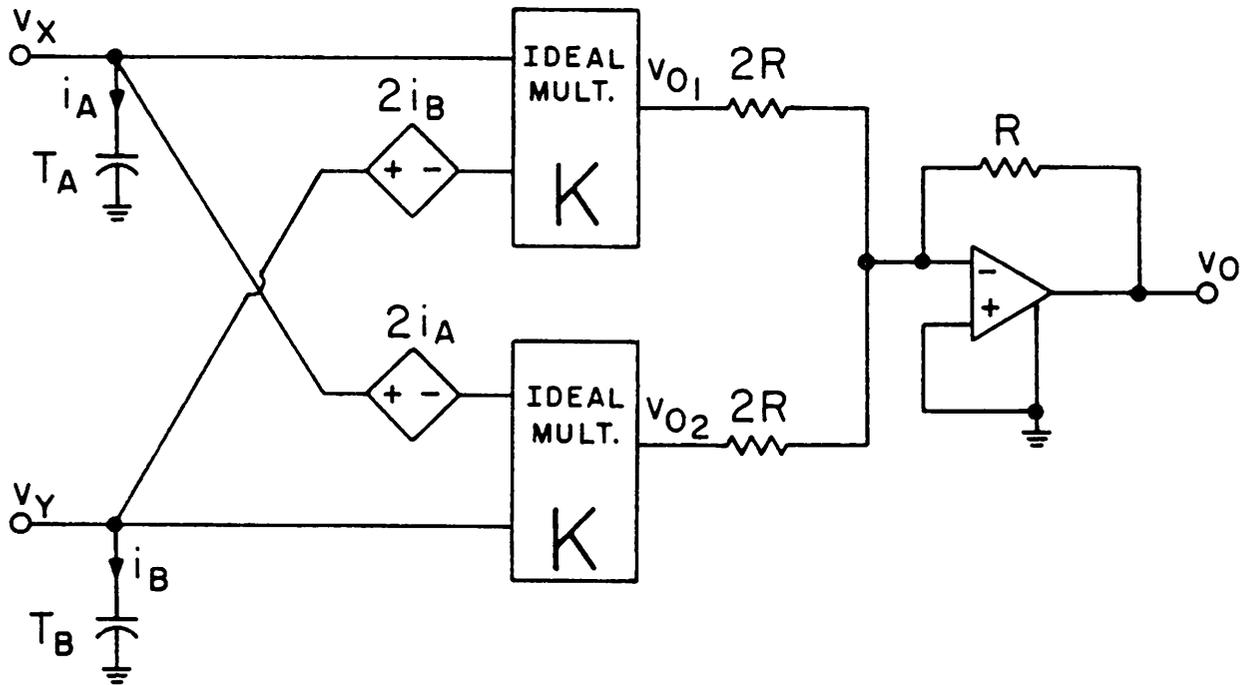


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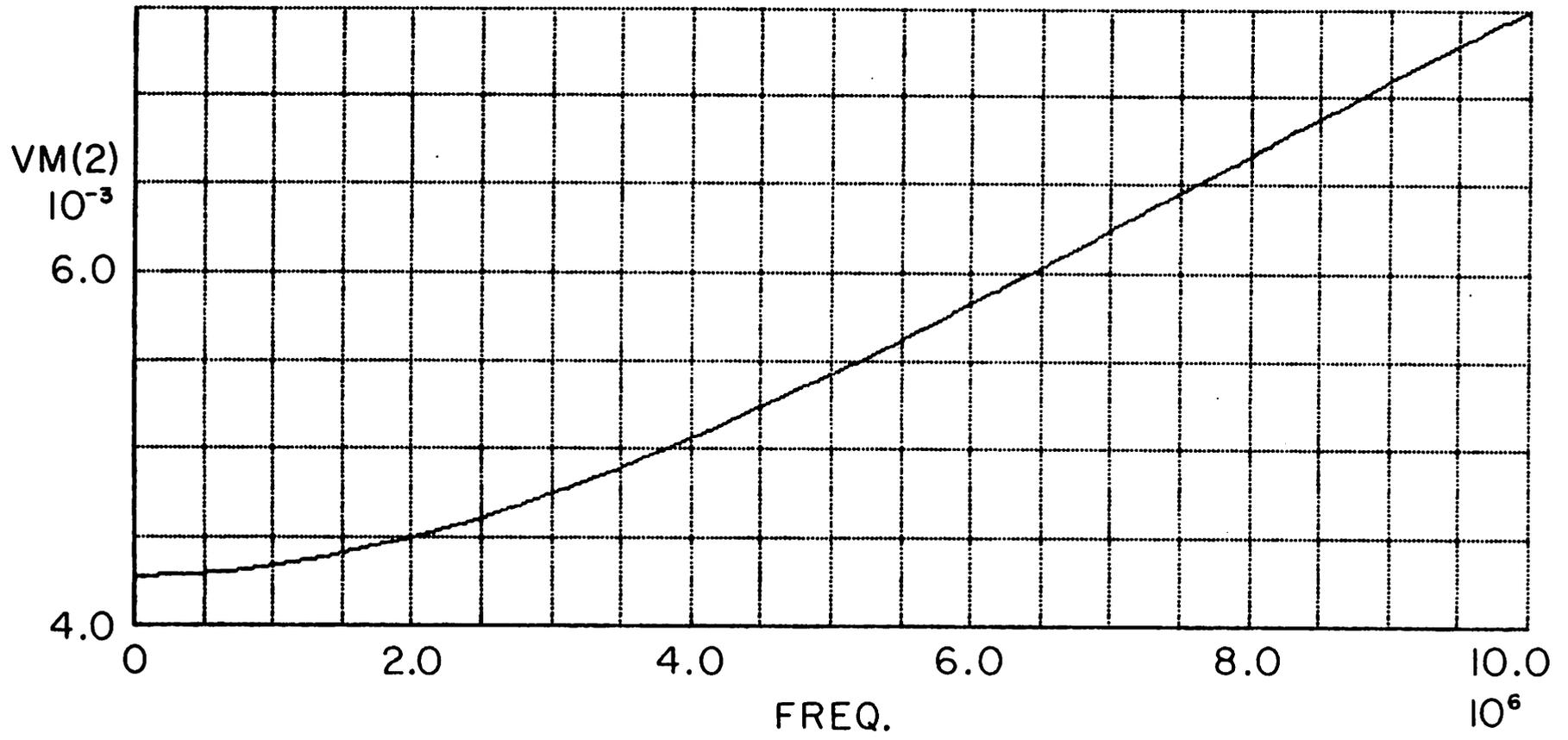


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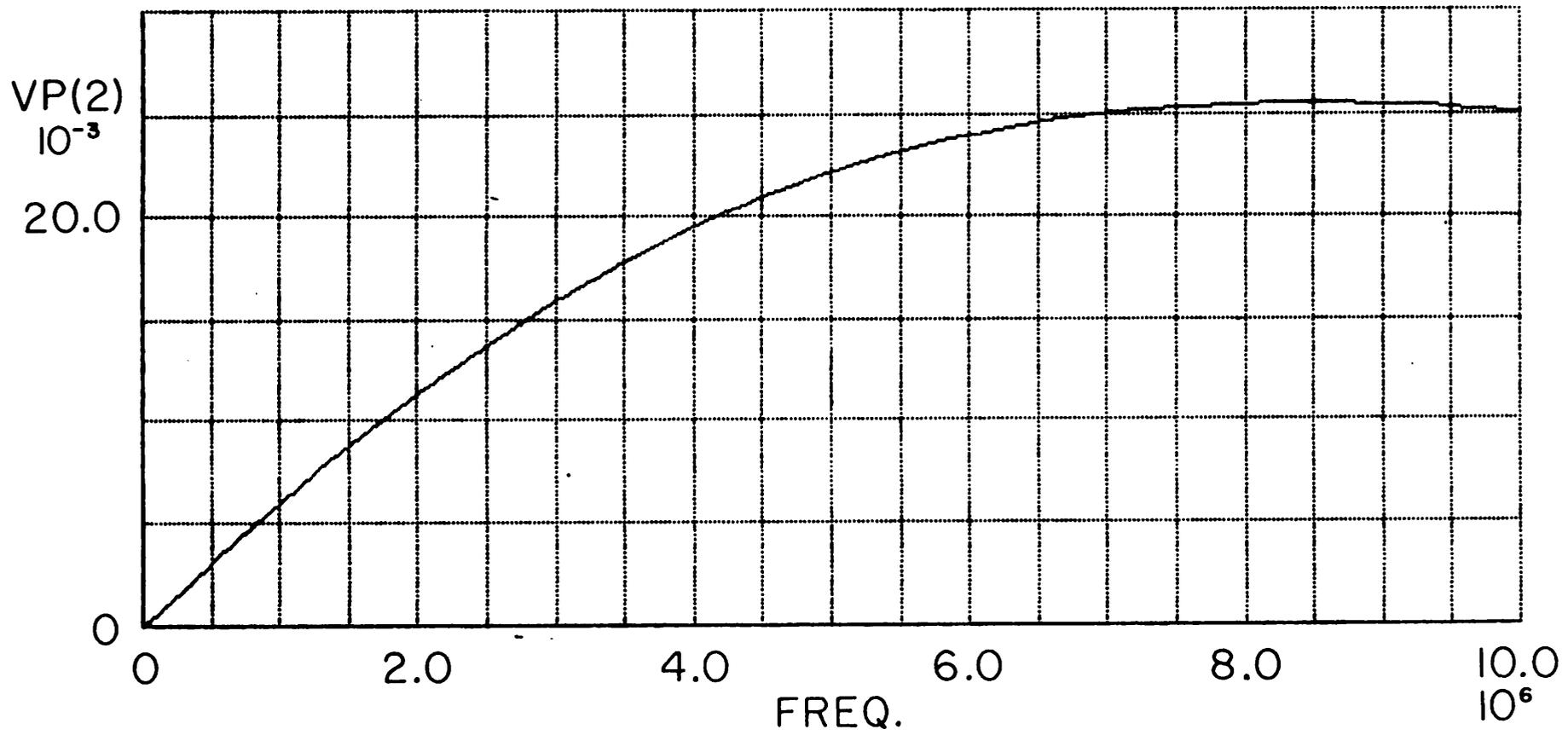
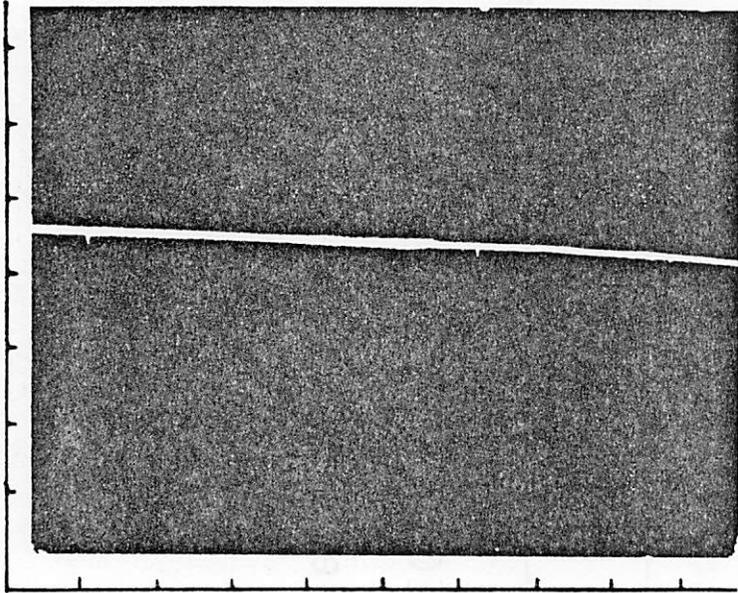
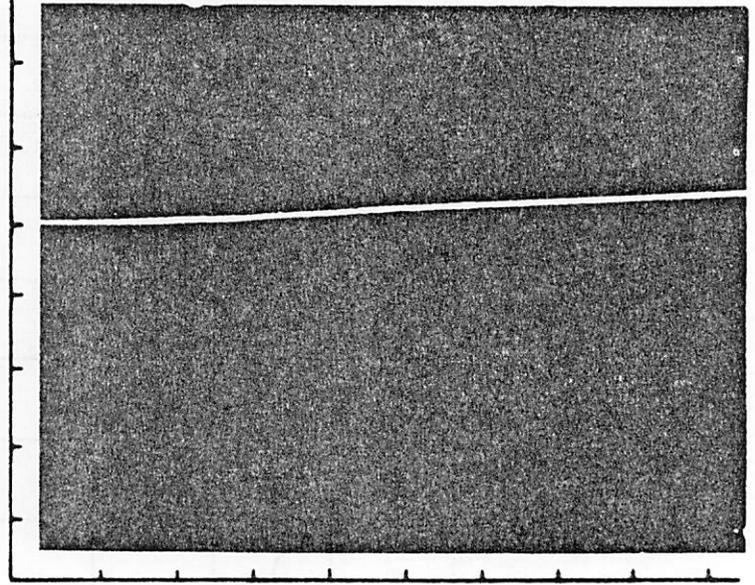


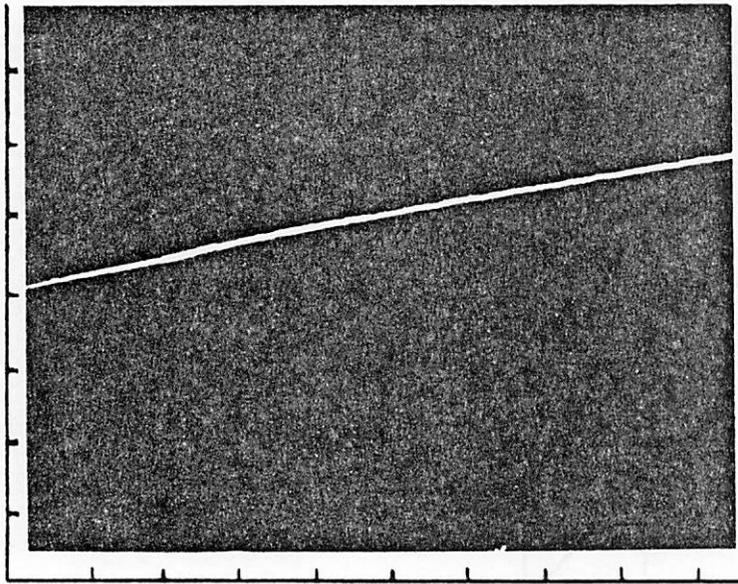
Figure 5



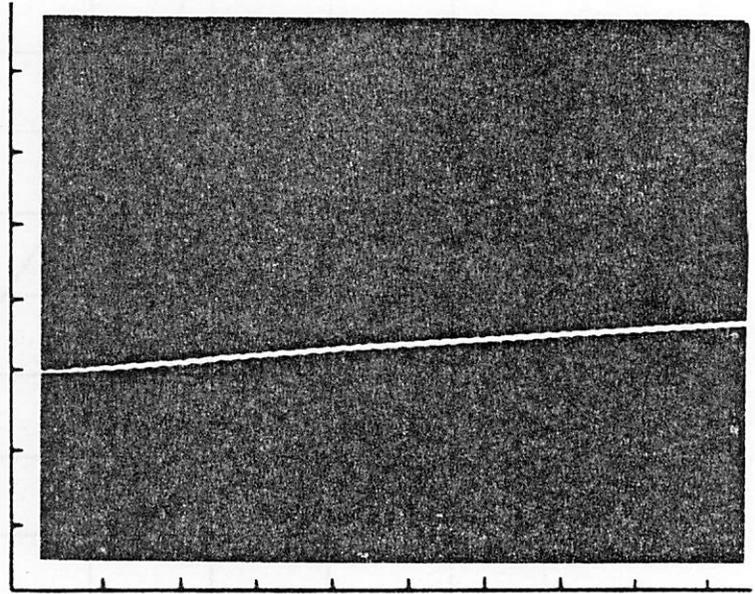
(a)



(c)

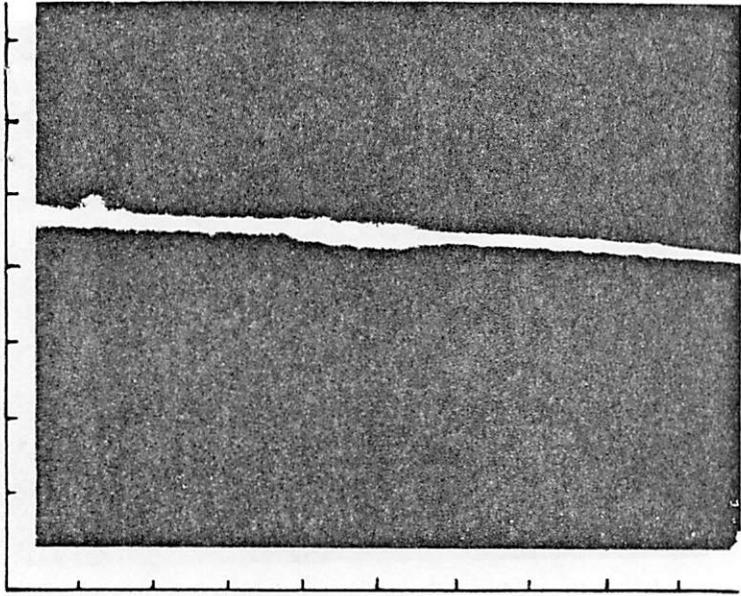


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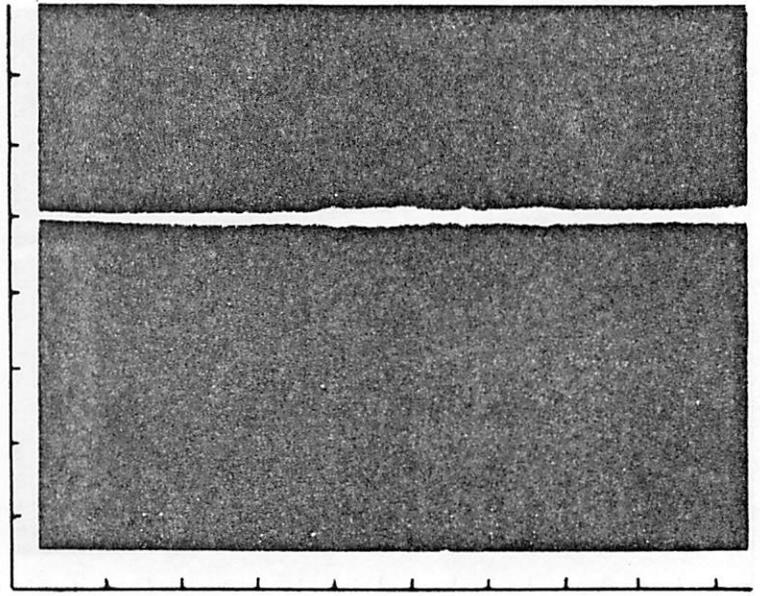


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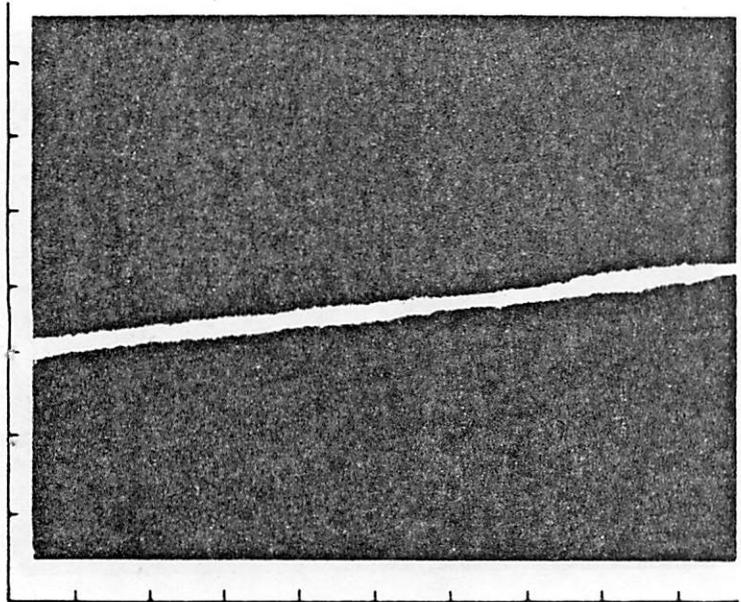
Figure 6



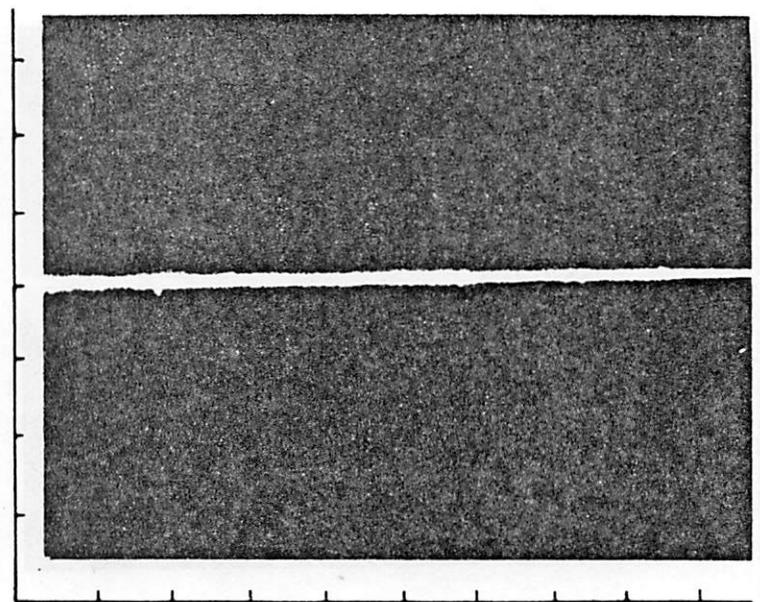
(a)



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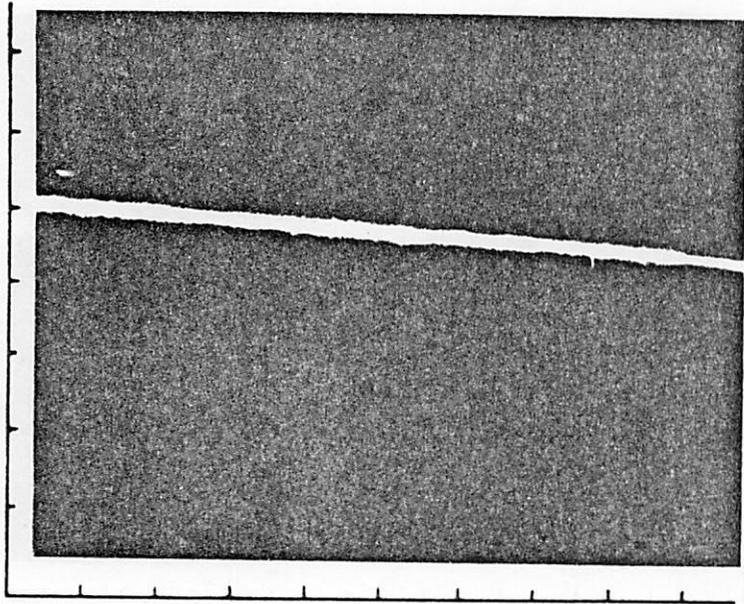


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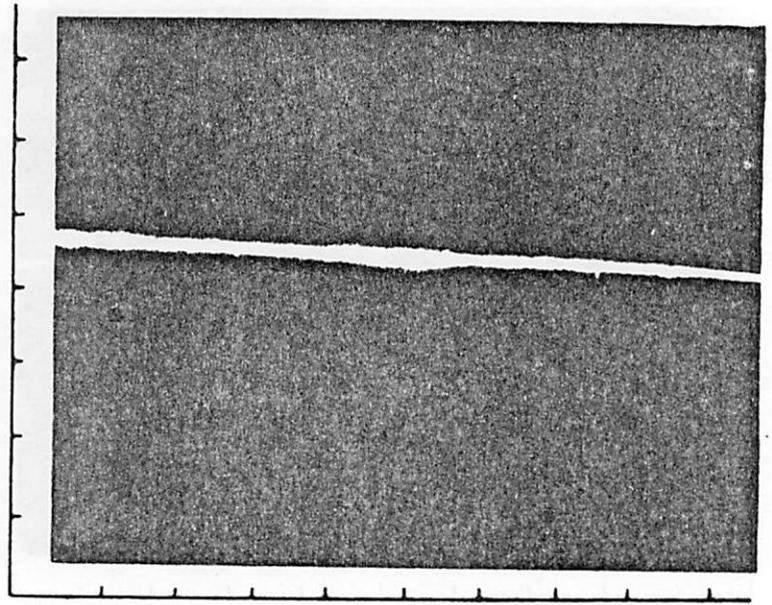


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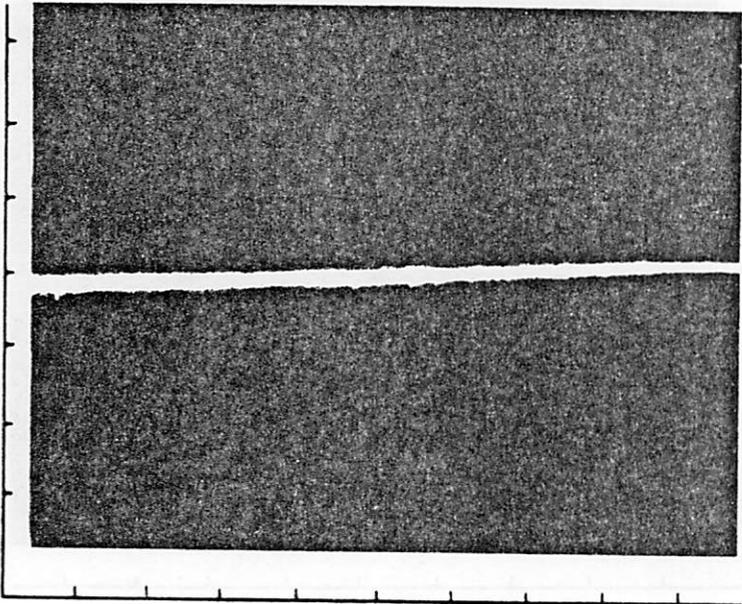
Figure 7



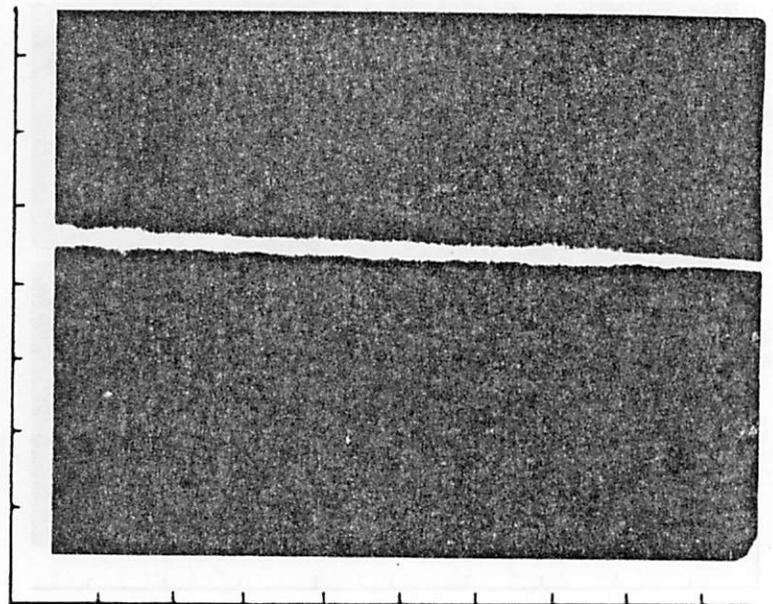
(a)



(c)

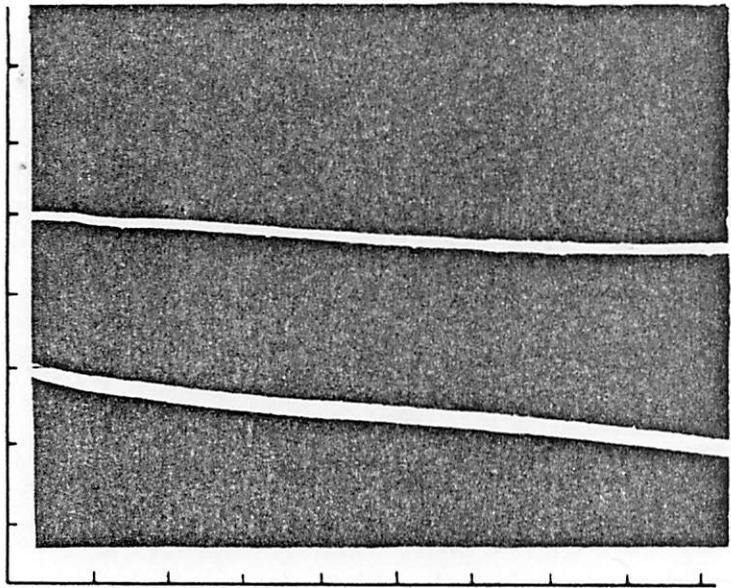


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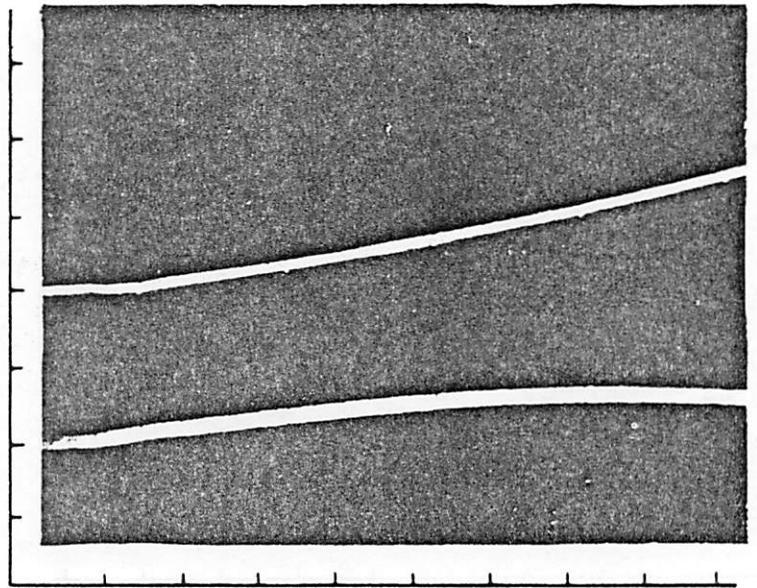


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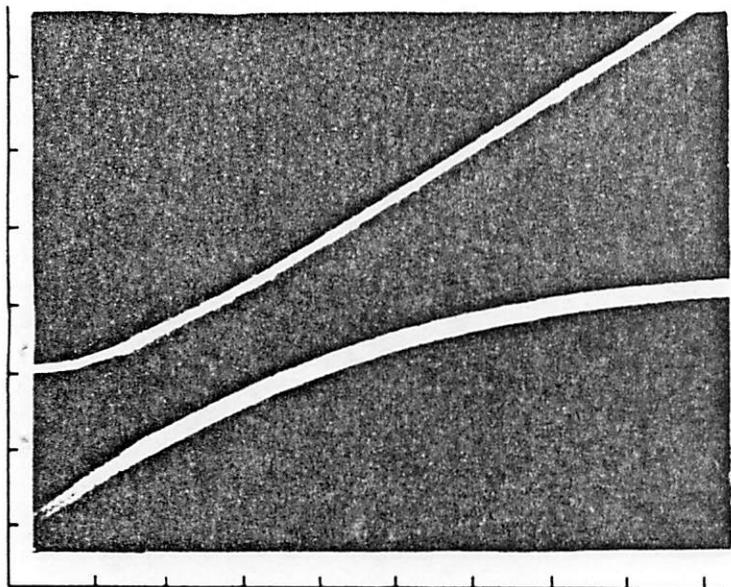
Figure 8



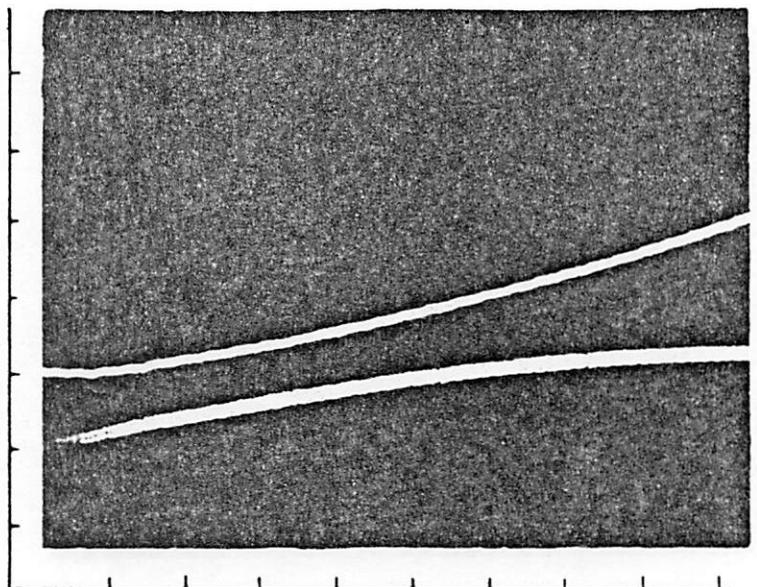
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(c)

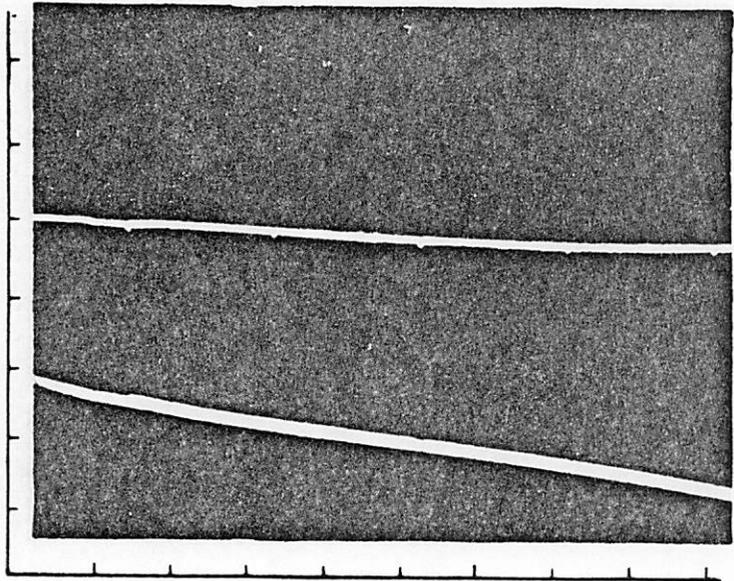


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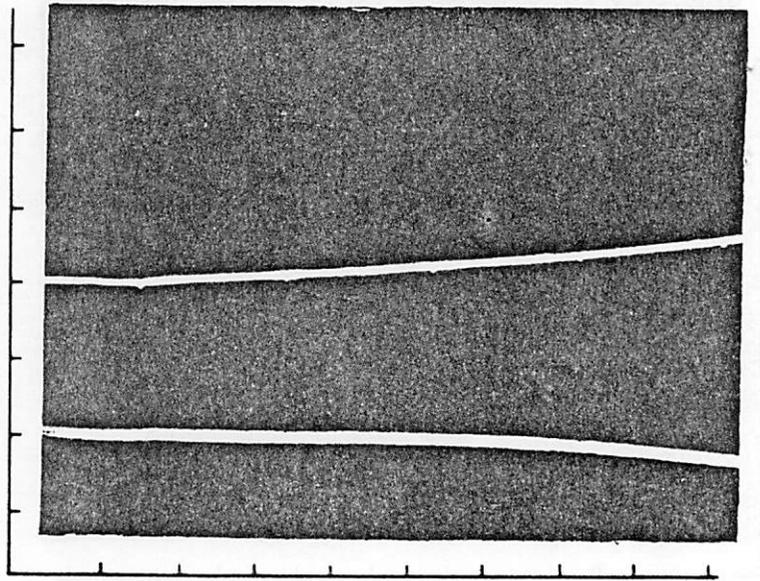


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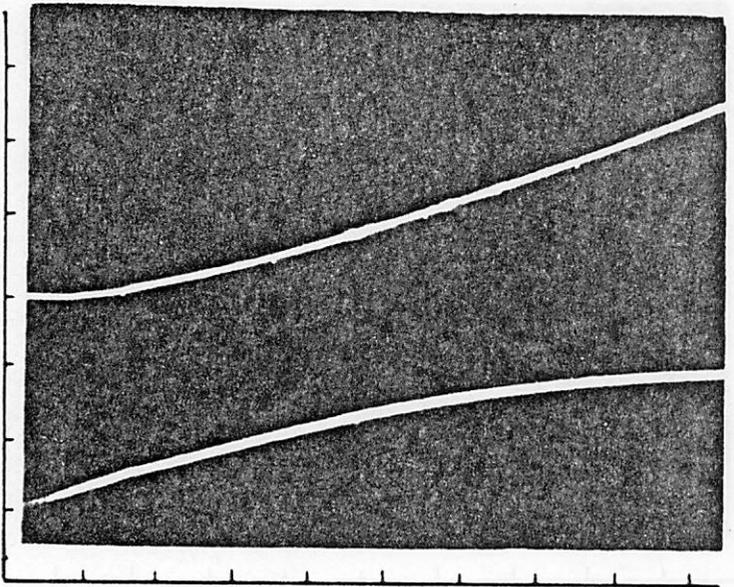
Figure 9



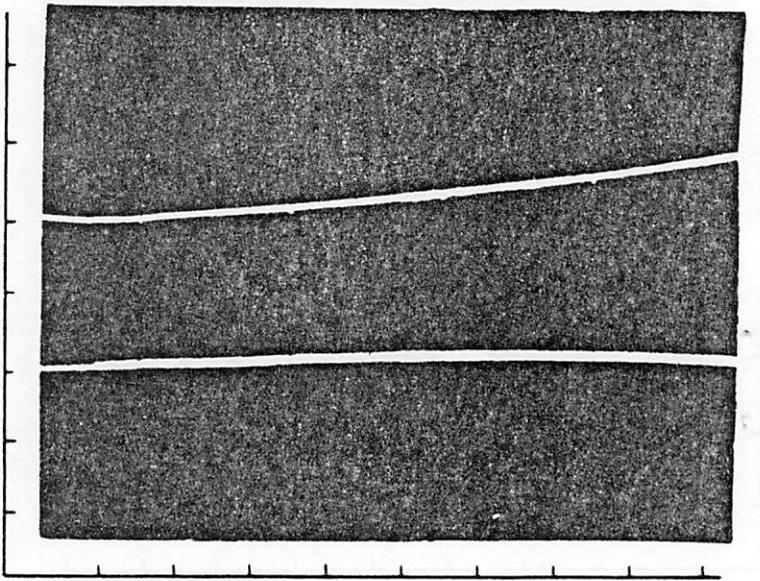
(a)



(c)

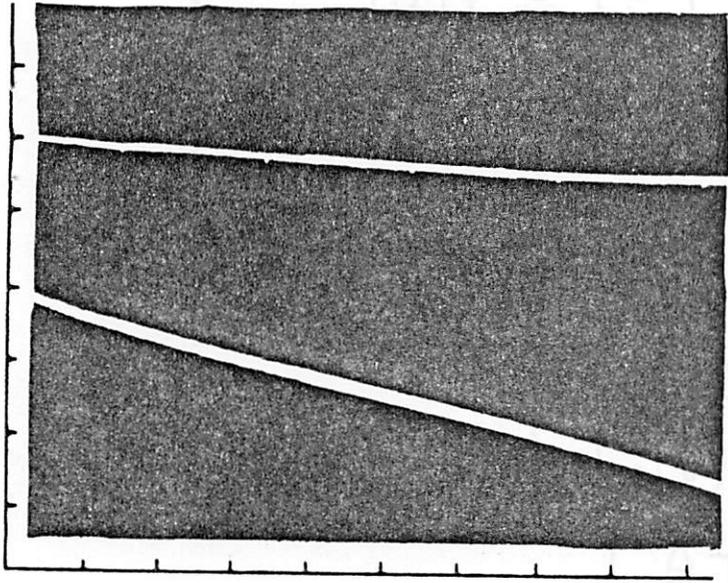


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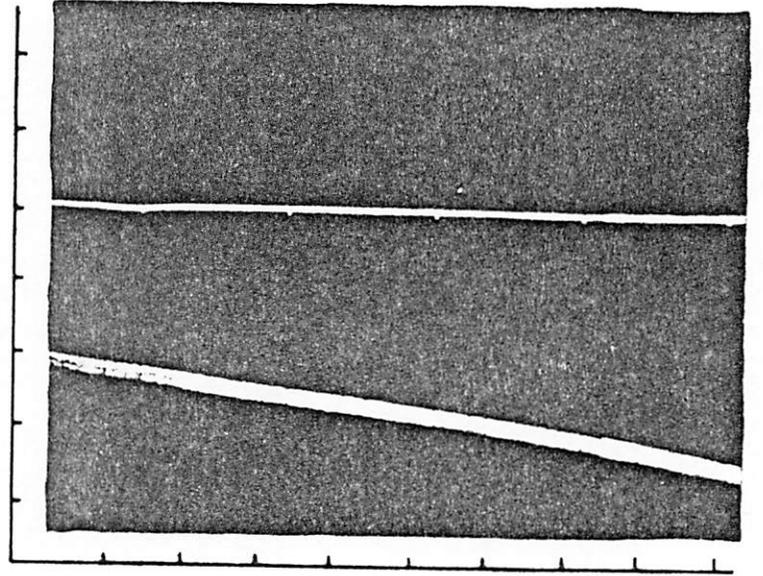


(d)

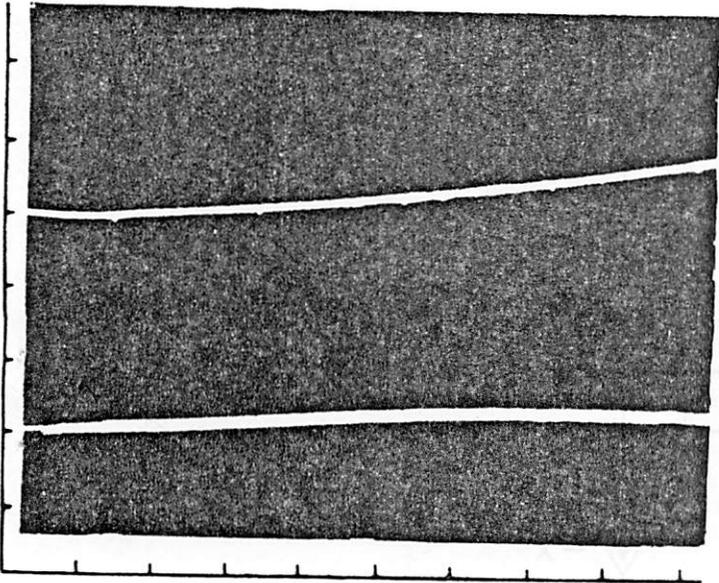
Figure 10



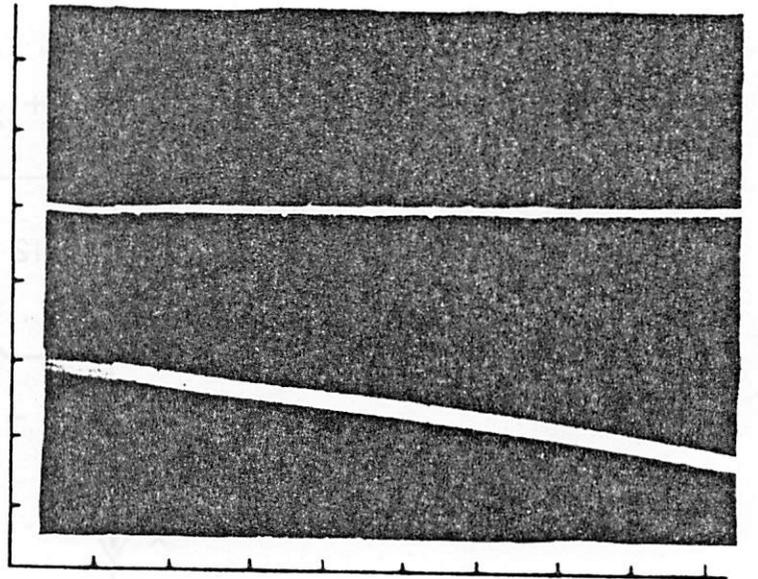
(a)



(c)

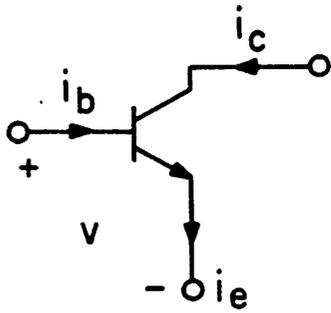


(b)



(d)

Figure 11



$$i_b = T \frac{d}{dt} f(v)$$

$$i_c = f(v)$$

$$i_e = \left(1 + T \frac{d}{dt}\right) f(v)$$

where

$$f(v) = I_s (e^{\lambda v} - 1) \approx I_s e^{\lambda v}$$

$$T \triangleq \frac{1}{\omega_T}$$

Figure 12

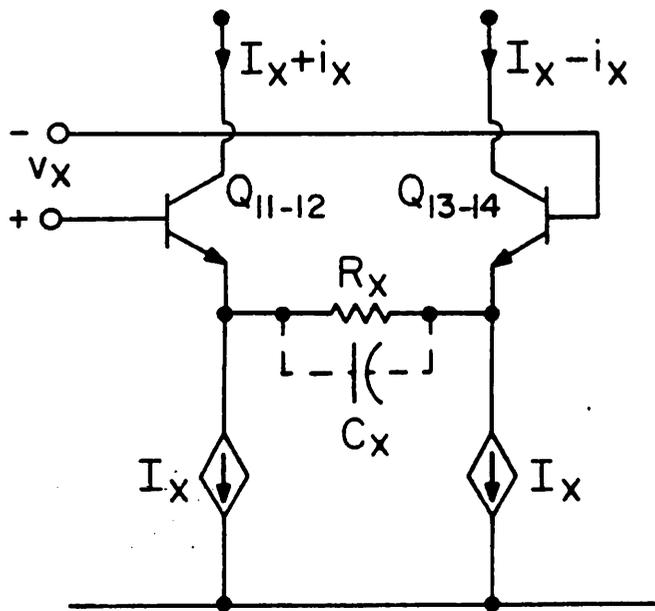


Figure 13

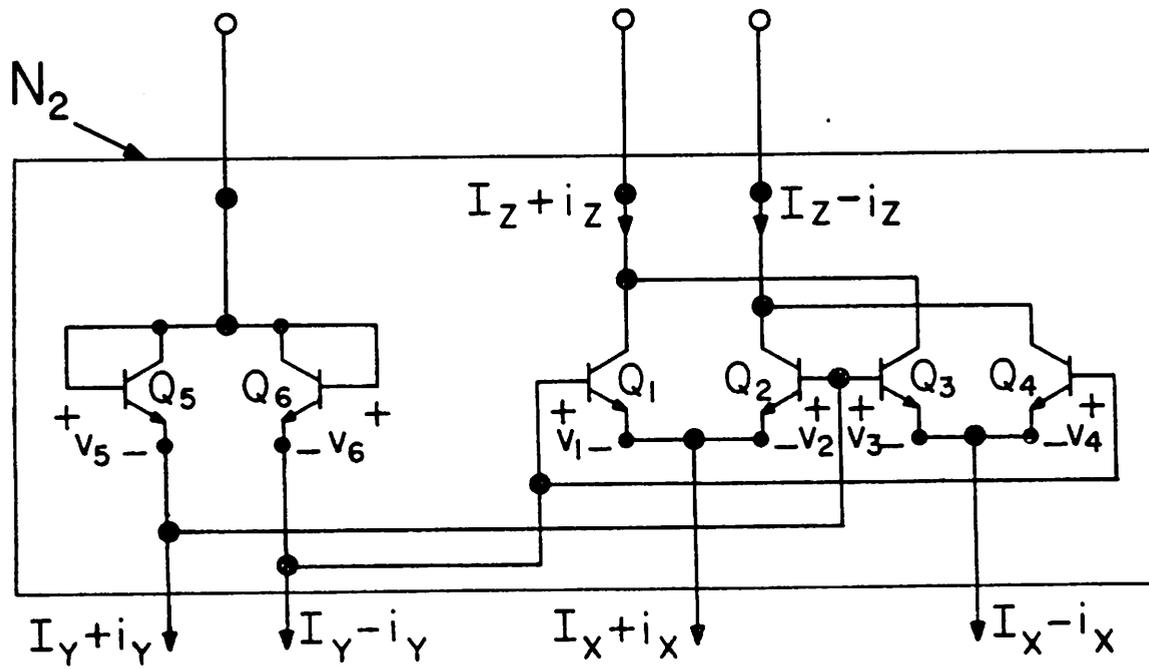


Figure 14

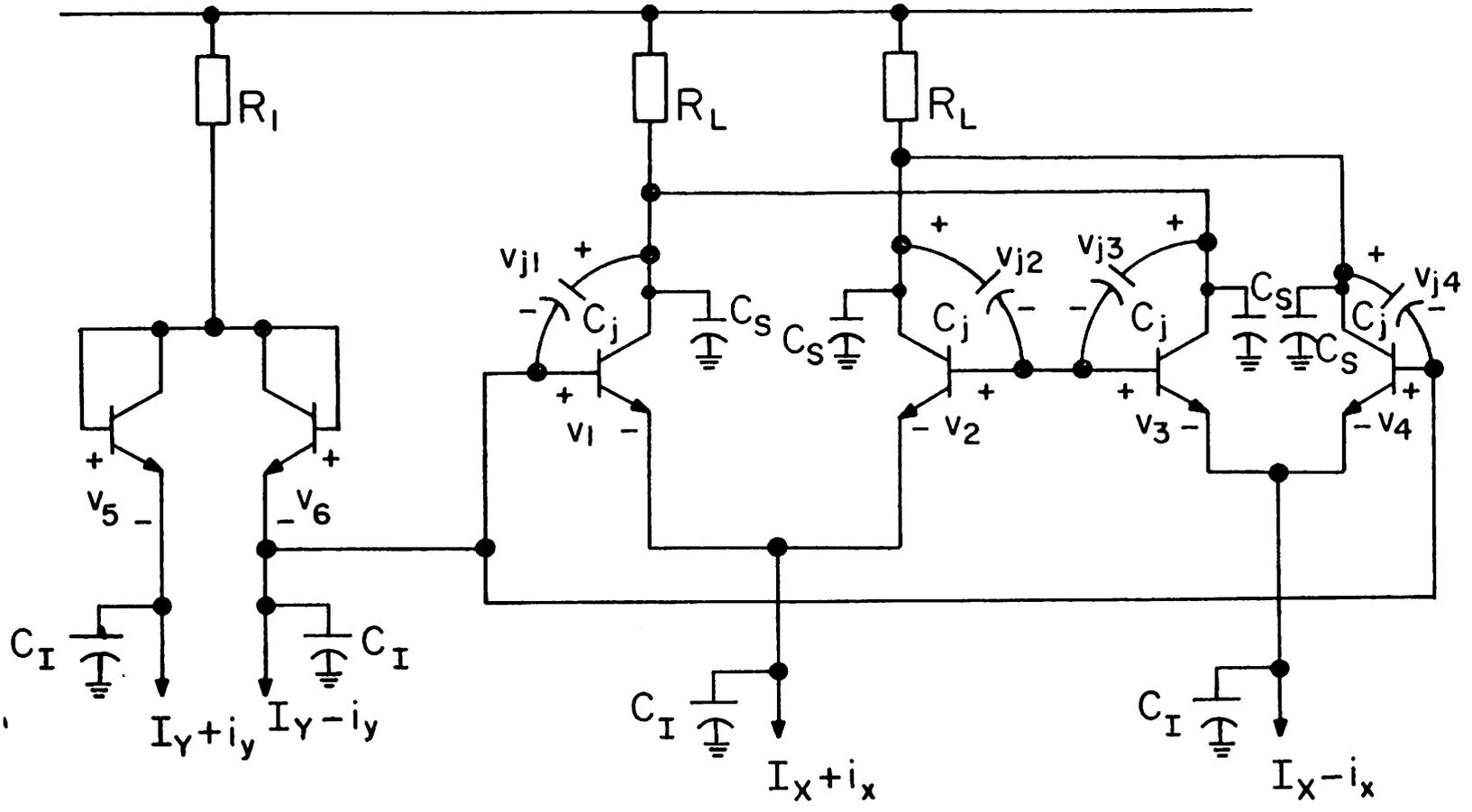


Figure A.1