A HIGH-FREQUENCY DIFFERENTIAL NARROW-BAND SWITCHED-CAPACITOR FILTERING TECHNIQUE

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Memorandum No. UCB/ERL M82/52

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

ABSTRACT

A HIGH-FREQUENCY DIFFERENTIAL NARROW-BAND SWITCHED-CAPACITOR FILTERING TECHNIQUE

by

Jesus Alejandro Guinea

PhD. Dept of Electrical Engineering and Computer Sciences

Signature.....
Chairman of Committee

A new resonator loss cancellation technique is described which allows the implementation of narrow-band , high-frequency switched-capacitor filters in NMOS depletion-load technology. The technique is based in the development of a SC integrator circuit with an inherent negative loss which when coupled together with a conventional lossy SC integrator results in a very low loss resonator circuit. The accuracy of the loss cancellation is guaranteed by the matching properties found in integrated circuits. The circuit uses local positive feedback to invert the polarity of the amplifier DC gain preeserving the high speed properties. The circuit implementation involves circuit which is conditionally unstable and is stabilized by feedback .

Single stage amplifiers are used in order to meet the fast settling required in high-frequency applications. The technique is employed in the design of a sixth order bandpass filter with center frequency of $100kHz$ and a effective Q factor of 20. The prototypee filter is $8mm^2$ in area and has a power dissipation of $30mW$. Experimental results from the IC prototype are presented.

ACKNOWLEDGEMENTS

I wish to express my gratitude to all the people who shared their time and a great deal of their knowledge during my stay at Berkeley. My thanks to Prof. Paul R. Gray for allowing me to work in his research group and to Prof. Donald O. Pederson and to my fellow students especially Dan Senderowicz and Oscar Agazzi. Special thanks to all the ERL people for their support during the integrated circuit fabrication. I want to acknowledge the Mexican Council of Science and Technology who supported this research, to the National Science Foundation , Grant ENG78-11397, Tektronix, Inc., and Xerox Corporation for partial grants employed for this research.

DEDICATION

To my wife Lorena in deep appreciation for her love, confidence and understanding. To my sons Sammy , Jose and Pablo who are a great help in my way through life. To my parents for their love and to many other friends who put their trust in me.

Contents

CHAPTER 1

INTRODUCTION

1.1. The Problem Description

Switched Capacitor (SC) filters have proven to be an effective way of implementing voiceband filtering functions in monolithic form. The extension of SC filters to frequencies of $100kHz$ and above could have an important impact in communications IF filters, e.g., AM, pilot carrier, as well as telecommunications circuits ,e.g., timing recovery . The application of SC filters to higher frequencies and narrow bandwidths requires the use of low sample rate to filter band-edge ratios. The active implementation requires operational amplifiers capable of fast settling, i.e., clock rates of $1MHz$ and above . High-frequency filters usually need accurate narrow bandwidths (high selectivity). The ladder filter implementation is based on lossless reactive elements which would need ideal amplifiers ; in such filters the transfer characteristics must be determined by the terminations and not by the highly variable amplifier gain and bandwidth. The amplifier requirements are a fast settling and a gain much larger than the filter effective selectivity Q.

The realization of high-gain, high-bandwidth amplifiers in MOS technology is a difficult task. High gain requires multiple gain stages, which complicates the problem of compensation of the circuit to achieve very large bandwidth. Single-stage differential amplifier configurations may be designed with CMOS that attain fast settling performance with high gain [55]. In NMOS technology single-stage amplifiers can give the required speed ; however, the very limited voltage gain per stage due to the lack of a complementary device makes the simultaneous realization of large DC gain and large bandwidth very difficult.

1.2. Loss Cancellation Technique

Positive feedback can be used to increase the effective value of the DC gain . PF compensation can be used in active filters but it requires special tuning procedures to guarantee that the right amount of positive feedback is applied [8]. In the monolithic implementation , the regulation of positive feedback to reliably achieve a stable high gain is a difficult design problem .

Ladder filters are realized by the interconnection of resonators (integrator pairs). In these filters a second alternative to reduce the effect of the finite gain is possible . It consists in canceling the finite gain effect (loss) in every resonator by applying all the necessary compensation to one of the integrators in every pair , i.e., *balanced loss compensation*. The operation of this technique lies in the fact that the transfer function is ultimately dependent on integrator loops in the filter. In this technique every loop in the filter consists of a lossy integrator and an overcompensated one. The overcompensation produces an effective *negative-loss integrator* . The negative loss circuit is realized by a local positive feedback which is defined by the transistors in the amplifier giving a negative loss value that very accurately matches the loss of the conventional amplifier (positive-loss). The technique replaces the high DC-gain requirement with that of gain matching . The latter is more easily achieved in a monolithic implementation where device matching properties define the accuracy of the positive feedback and and thus the accuracy of the finite gain effect cancellation. Furthermore, the NMOS negative-loss circuit is almost identical to the conventional amplifier assuring gain matching properties.

In Chap. 2, the analysis of the finite amplifier DC gain in the discrete time domain is presented. In this description the symmetry aspect of the balanced cancellation is clarified. In order to have an accurate cancellation, the transfer function pole for each of the SC integrators are located, along the z-domain real

axis, inside and outside the unit circle at an equal distance.

1.3. Synthesis of the Negative-loss Circuit

The essential concept presented in this dissertation is the use of the IC matching characteristics to provide the proper amount of positive feedback necessary to compensate the finite amplifier DC gain effect in SC filters. It is essential to find a realization for the negative-loss circuit which is symmetrical to a positive loss amplifier .

The negative loss can be obtained by several circuits . Three network open-loop transfer functions , $a_n(s)$, are presented. The alternatives are studied to get to the one that best satisfies the matching conditions . The non-Hurwitz open loop circuit proved to have advantages over the other implementations . The open loop transfer function has a single pole on the RHP and is brought to absolute stability by the close loop configuration. The circuit proposed belongs to a class of circuits which are conditionally unstable and can be utilized in linear circuits offering unique properties.

Experimental results demonstrate that effective resonator q factors of the order of 300 can be obtained from amplifier gains of 50±10%. The results very accurately predict the effectiveness of the cancellation in ladder SC filters. The analysis of circuit stability is included in Chap. 3.

1.4. NMOS Circuit Implemetation and Fabrication

Practical design of NMOS differential configurations for the negative loss which has the close resemblance to the single stage conventional circuit was performed and is presented in Chap 4. The circuits are highly symmetrical and give a DC gain matching of 2% for absolute values of the order of 50–80. The filter design consideration for high frequency narrow band filters are presented in Chap.5. The problem of component sensitivity is addressed by the use of

identical resonator leap-frog filter configurations which takes advantages of the matching properties of IC's to produce accurate center frequency resonators. This configuration requires component ratios of the order of the filter Q. The solution to this component spread problem is presented in Chap.5.

The prototype filter is a sixth order quasi-elliptic filter (transmission zeroes sightly in the LHP) with radian center frequency (ω_0) in the range of $100kHz$ and effective Q factor of 20±5%.

Single-poly depletion-load NMOS process used is a subset of a 12 masks CMOS process developed at UCB. It is a 4μ $700A^{\circ}$ gate oxide, process featuring shallow implanted junctions and implanted threshold correction. The process flow matrix is found in App.pro. All the fabrication including the mask making was done at the UCB solid state lab facility.

1.5. Experimental Results of the Prototype Filter

Table 1.1 shows the NMOS amplifier performance. Table 1.2 contains the measured data for the bandpass filter . These results indicate that the technique of implementing resonators with qualities close to 400 from amplifiers with typical DC gains of 50 is possible. A conventional approach would require an amplifier gain of 800.

1.6. Summary

A new circuit approach using parameter matching properties of IC's to control the loss cancellation of an active resonator is presented. It uses an internal positive feedback converter to produce an accurate and stable result. Implementation of narrow-band filters with Q limited by matching and not by the absolute DC gain value of the amplifiers results from this technique . A sixth order elliptic switched capacitor filter was fabricated in NMOS to demonstrate the technique. The technique has applications in many high frequency circuits

where the finite DC gain has undesired effects, e.g., Fast differential sample and hold circuits, Serial charge balance A / D, etc. The NMOS prototype circuit has filtering functions applications in the frequency range of 100kHz , e.g., mobile radio communication receivers, pilot carrier receivers and timing recovery circuits.

CHAPTER 2

REVIEW SC INTEGRATOR AND RESONATOR CIRCUITS

2.1. Introduction

In the early designs of SC filters, distortion of the transfer characteristics were encountered which were connected with amp non-idealities. This distortion resembles the phenomena of amplifier finite gain-bandwidth (GB) limitations found in active filters [41]. The effects of finite DC gain were not considered because of the high DC gain available in low frequeny op amps. The finite amplifier gain, however, has taken a dominant effect in the realization of high frequency SC filters. Examples of the gain effect were analyzed by Allstot for low pass SC filters [25]. The effect are a droop in the passband shape and distortion of the bandpass attenuation (ripple characteristics), as shown in Fig.2.1. The finite amplifier gain-bandwidth (GB) mainly affects the passband shape [13] as shown in Fig.2.2.

Sampled-data (S/D) filters showed less dependence on the finite bandwidth parameter than did the active filters , and in particular, in high frequency applications the design of fast amplifiers results in the finite gain taking a predominant role. The dependence on the amplifier GB is reduced by using fast single stage amplifiers whith settle to within the proper error band in the sampling period. The best settling response possible for a given amplifier determines the maximum sampling frequency which in turn determines the highest band edge frequenciesin the filter. After the amplifier has settled, the transient response presents an error which is a function of the finite amplifier DC gain (transient steady state error). The required filter accuracy determines the allowed *error band* of the amplifier transient response within the clock phase. The analysis of

the amplifier finite gain in the S/D integrator is introduced. The effect is similar to the loss in reactive passive elements and is referred as such in this work.

High order filters transfer characteristics are dependent on integrators and thus the analysis of the integrator losses can be generalized to arrive at the filter loss. The amplifier response within each clock phase in the sampled data domain is investigated to evaluate the loss effect in the integrator transient response. The loss cancellation alternatives are discussed, and the approach used in this research is presented. In high order filters it is important to consider not only the time response of the integrator implementation but the overall transient response of the filter longest signal path during a particular clock phase. In order to improve the value of the highest band-edge of the filter, the number of physical elements involved in the worst case path must be minimized.

2.2. Discrete Time Analysis

This section presents a review of the analysis of the S/D integrator and resonator circuits. The block diagram of a S/D system for each of the clock phases is shown in Fig.2.3. It has been demonstrated that the S/D implementation has effects on the overall filter which depend exponentially on the amplifier limitations [4]; this follows from the fact that the amplifier parameters affect the S/D circuit within each sampling clock phase.

For the S/D circuit, the data value at sampling time contains all the information , however, the response of the elements within the clock period previous to each sampling time determine that value and that is the reason for their fundamental importance.

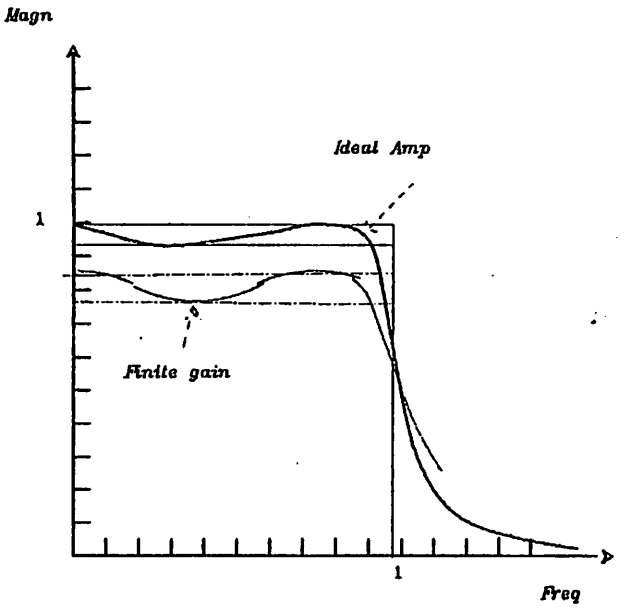


Fig.2.1 Finite op-amp gain effect in the filter transfer function

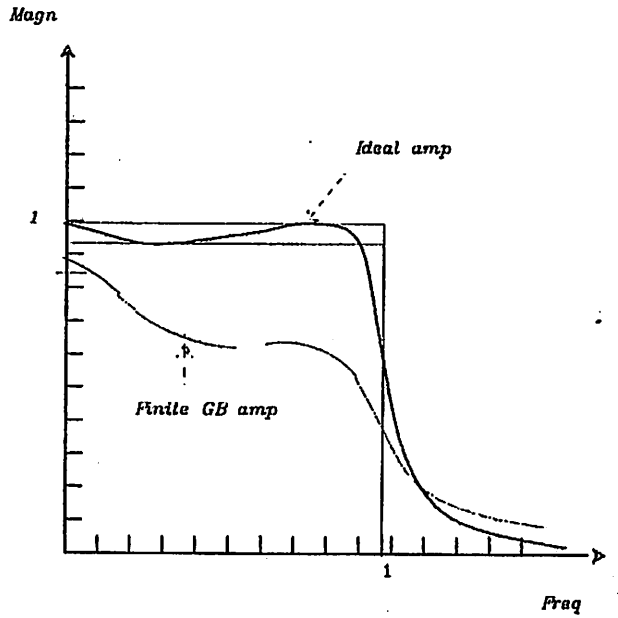


Fig.2.2 Finite op-amp GB effects on the filter transfer function

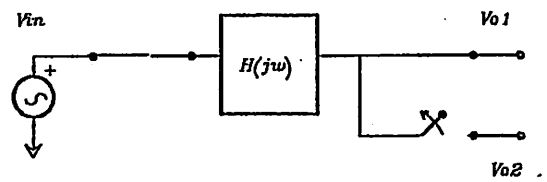


Diagram on Phase1

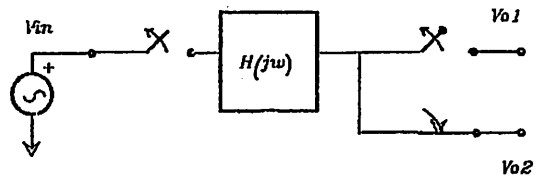


Diagram on Phase2

Fig.2.3 Sampled Data System Block Diagram

2.2.1. Sampled-data Integrator

The sampled data integrator circuit is shown in Fig.2.4. The amplifier in the S/D integrator is switched between two modes of operation : a charge hold mode and a charge transfer mode. In this nomenclature the clock phases are called the transfer and hold phase respectively. Fig.2.4a depicts the circuit configuration during the charge transfer phase $\Phi 1$, i.e., $nT_c < t < (n + \frac{1}{2})T_c$, where T_c is the sampling clock period. During the transfer phase , the amplifier moves charge from the sampling capacitor C_u to the integration capacitor C_f. If the amplifier is ideal ($\alpha \to \infty$) the transfer of charge is done instantaneously and the amplifier final output voltage is modified by a step value determined by the injected charge and the ratio of capacitors $\frac{C_u}{C_f}$. The accumulation of charge in C_f performs the *S/D integration function* (summation function):

$$V_o(n) = h(n) = \sum_{i=0}^{n} \frac{C_u}{C_f} V_i(n) \qquad (2.1a)$$

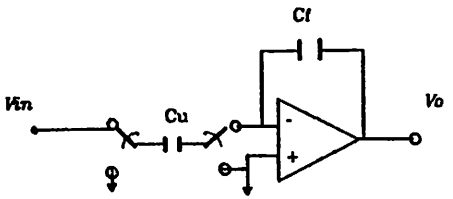
For a unit step discrete input $V_i(n) = u(n) = 1$ the response $h(n)$ has a general term given by:

$$V_o(n) = n \frac{C_u}{C_f} \qquad (2.1b)$$

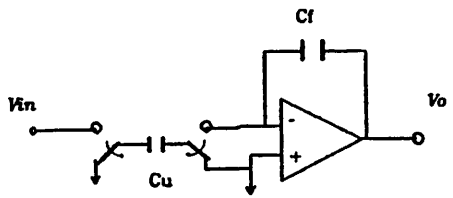
The response for a S/D unit step $u(nTc)$ is a S/D ramp function (staircase). Fig.2.5 shows the response for the ideal (lossless integrator) and the non-ideal (lossy) SC integrator. The latter is a damped version of the ideal ramp integrator output. The response for the lossy SC integrator converges to a constant value determined by a loss term p_i as we shall see later:

$$V_o(n)|_{n\to\infty} = \frac{C_u}{C_f} \frac{1}{1 - p_i} \qquad (2.1c) \qquad (2.1c)$$

The integrator response is related to the ability of the amplifier to settle within each clock phase as shown in Fig.2.5b. In the lossy integrator the



a) Phase 1 (Sampling Phase)



b) Phase 2 (Refresh Phase)

Fig.2.4 SC integrator on both clock phases

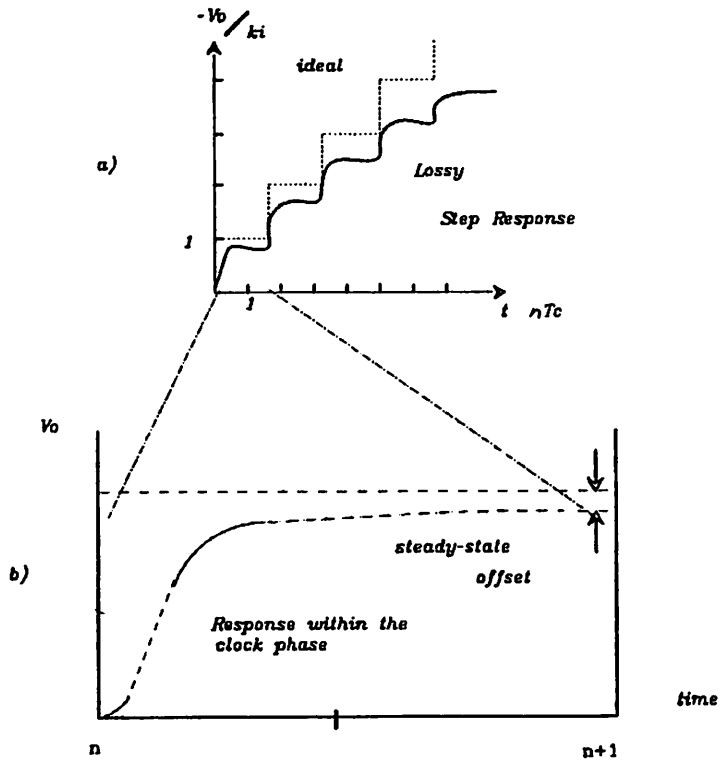


Fig.2.5 SC integrator step response and detailed transient within phase1

transient error at sampling time propagates in time. The amplifier output value reached within the clock phase comprises an error with respect to the ideal. The error depends on two phenomena:

1. *Amplifier finite gain-bandwidth product* which defines the settling time and contains a time-varying portion of the transient error which converges to zero, and
2. *Amplifier finite DC gain* which determines the final steady state error.

The settling error is neglected under the assumption that the clock period is long enough for the amplifier settling components to be much smaller than the error band and, in those conditions, the steady state error is dominant. The z-domain transfer function for the ideal integrator is given by:

$$H_i(z) = \frac{V_o(z)}{V_i(z)} = -K_i \frac{z^{-1}}{1 - z^{-1}} \tag{2.2}$$

The ideal integrator has a gain K_i and a transfer function pole equal to unity. The discrete time response was given in (2.1a).

Our concern in S/D filter design is the sinusoidal steady-state frequency response. The integrator frequency response is illustrated in Fig.2.6 The frequency response in SC filters has been widely studied [64, 69]. Even for the ideal amplifier implementation the S/D integrator has amplitude and phase errors with respect to the ideal integration function, $\frac{\omega_i}{j\omega}$, due to the exponential nature of the continuous to discrete time mapping. The ideal integrator function and the SC integrator errors are summarized below for the direct digital integrator (DDI) :

$$H_{ideal} = -\frac{\Omega_i}{j\Omega} \tag{2.3}$$

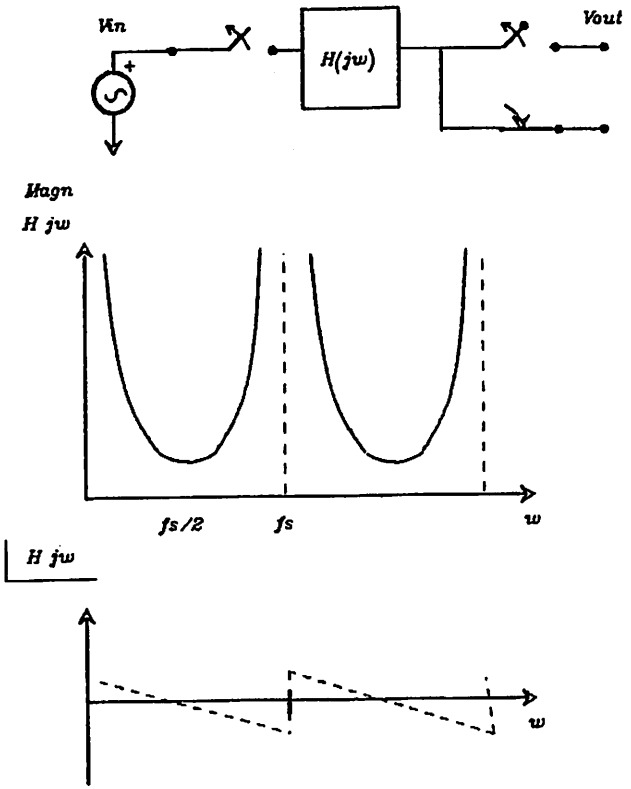


Fig.2.6 Frequency response of the SC integrator

The S/D filter frequency response is obtained by substitution of $z = e^{j\Omega T}$ in (2.1c) :

$$H_i(j\Omega) = \frac{V_o(j\Omega)}{V_i(j\Omega)} = -K_i e^{-j\Omega\frac{T_s}{2}} \frac{1}{\left[\frac{\sin\Omega\frac{T_s}{2}}{\Omega T_s/2}\right]} \qquad (2.4)$$

The phase and magnitude errors are :

$$\varepsilon_A(\Omega) = \frac{1}{\frac{\sin\Omega\frac{T_s}{2}}{\Omega T_s/2}} \qquad (2.5)$$

The phase-lead error is given by :

$$\varepsilon_\theta(\Omega) = e^{-j\Omega\frac{T_s}{2}} \qquad (2.6)$$

The phase error can be eliminated by using the so called lossless digital integrator (LDI) [17] or the bilinear integrator scheme [28]. The magnitude error has the effects of a non-linear frequency warping as shown in Fig.2.7 for both the LDI and the bi-linear integrators.

2.2.2. Lossy Integrator Circuit

The finite amplifier gain changes the integrator transfer characteristics by producing a shift of the integrator pole inside the unit circle in the z-plane, see Fig.2.8a. The z-domain analysis of this shifting (loss) results in :

$$H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{C_u}{C_f}\frac{z^{-1}}{1 - p_i^{-1}z^{-1}} \qquad (2.7a)$$

where the pole is given by :

$$p_i^{-1} = 1 - \frac{1}{a_o}\left(\frac{C_u}{C_f}\right) \qquad (2.7b)$$

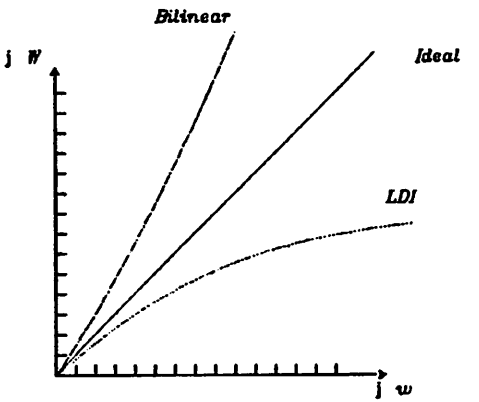
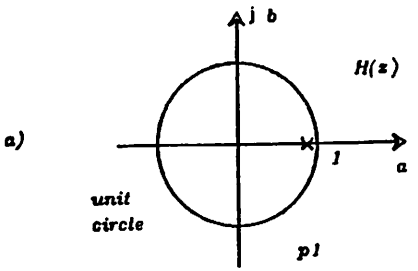


Fig.2.7 Freq. Warping for Bilinear and LDI Mappings



Pole Location for Lossy SC Integrator

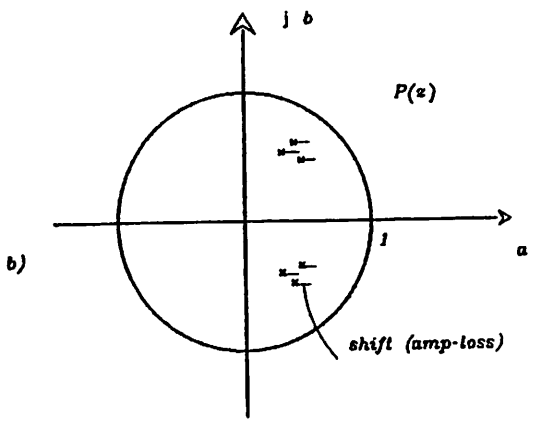


Fig.2.8 Pole shift due to the amp finite gain in high-order filters

and the unit step response is:

$$V_o(n)_{n\to\infty} = -\frac{C_u}{C_f}\sum_{j=1}^{n} p_i^{j-1} \tag{2.7c}$$

From the final value theorem, the response converges to:

$$V_o(n)|_{n\to\infty} = -\frac{C_u}{C_f}\frac{1}{1-p_i^{-1}} \tag{2.7d}$$

The pole location is away from unity by an error factor ε_p:

$$\varepsilon_p = 1 - p_i^{-1} \tag{2.7e}$$

The amplifier loss is then related to the pole error by ε_p which is proportional to the inverse of the amplifier DC gain.[1]

After calculating the effect at the integrator level, the performance of lossy integrators interconnected to form high order filters is studied. The effects of the loss in the integrator has the form of a change of variable, $z \to z + \varepsilon_p$, in the transfer function [60]. The effect of the integrator loss in the filter transfer func-

1.- Recently an elegant presentation of the errors in a SC integrator has been suggested [4] as follows:

$$H(\Omega) = H_i(\Omega)\frac{1}{\left[1-m(\Omega)\right]e^{-j\theta(\Omega)}} \tag{2.8a}$$

For small magnitude and phase errors it can be approximated as:

$$H(\Omega) = H_i(\Omega)\frac{1}{\left[1-m(\Omega)-j\theta(\Omega)\right]} \tag{2.8b}$$

The S/D magnitude $m(\Omega)$ and phase errors $\theta(\Omega)$ are referred to the ideal S/D integrator and not to the ideal sinusoidal steady-state integrator. For the finite gain amplifier the errors are given by:

$$m(\Omega) = -\frac{1}{a_o}\left(1+\frac{C_u}{2C_f}\right) \tag{2.9a}$$

$$\theta(\Omega) = \frac{C_u}{C_f}\frac{1}{2a_o\tan(\Omega\frac{T_c}{2})} \tag{2.9b}$$

The finite bandwidth amplifier in the SC integrator and in the filter response have been presented by Martin, et al.[4], and it has been demonstrated that the integrator error expressions can be directly applied in the standard formulae for active filters developed in the past, viz, tolerance and sensitivity analysis of filter characteristics.

tion $P_i(z)$ are represented by that same change of variable (Fig 2.8b) [85]:

$$P_i(z) = P(z + \varepsilon_p) \tag{2.10}$$

This equation has the same form as the loss effect in passive filters (two port lossless filters), see Fig.2.9. The analysis of the filter loss effects is therefore reduced to the analysis of the loss in the integrator circuit. Fig.2.10 shows a typical signal flow graph (SFG) of a higher order filter where the signal flow along the integrators in the filter is illustrated.

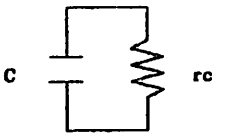
2.2.3. SC Integrator Loss in a Resonator Circuit

The integrator pair is connected in a negative feedback loop forming the resonator circuit, the circuit and block diagram are depicted in Fig.2.11a,b respectively. A unit pulse excitation to this lossless resonator results in a steady state oscillation response. Initial energy applied to the circuit is maintained through an oscillatory process in which energy is transfer between the individual integrators in each cycle of the resonator natural frequency, see Fig.2.11c. The resonator transfer function $P(z)$ is obtained from the integrator transfer functions using the Mason's rule, see Fig.2.11d. For the LDI integrator :

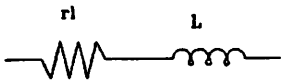
$$P(z) = \frac{-K_{1,2}\,\dfrac{z^{-1}}{1 - z^{-1}p_i}}{1 - K_{1,2}\dfrac{z^{-1}}{(1 - z^{-1}p_i)(1 - z^{-1}p_j)}} \tag{2.11}$$

where $K_{1,2}$ is give by the product of the individual integrator gains.

The closed loop pole locations are obtained through the root locus for the ideal case as shown in Fig.2.11d; the locus for the bilinear integrator case are also shown. The resonator final pole position is function of the S/D integrator circuit used: DDI, LDI, Bilinear. Fig.2.12



Loss Effect in a Capacitor



Loss in an Inductor

Fig.2.9

Parasitic Loss Effects in Passive Elements

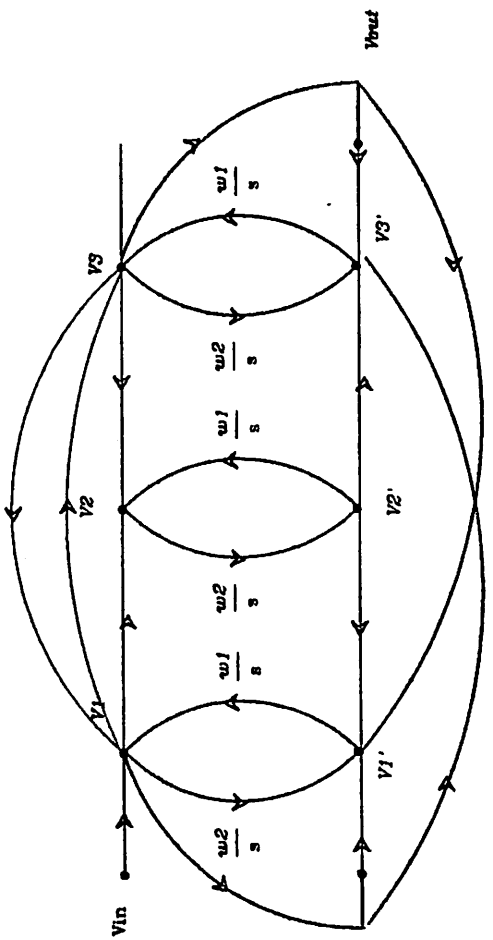


Fig.2.10 SFG for the Sixth Order Filter

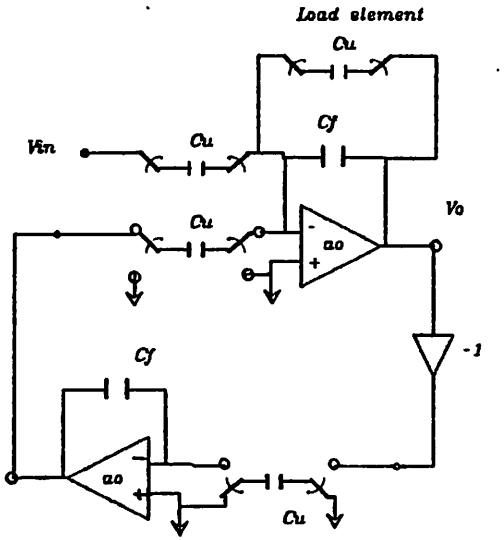


Fig.2.11a Terminated (loaded) SC Resonator

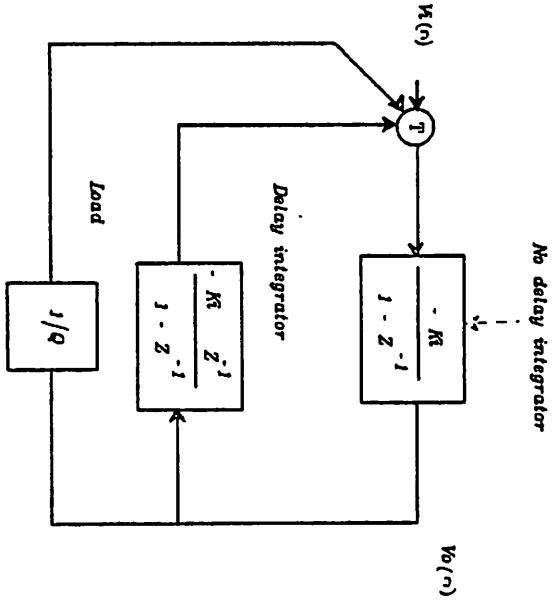


Fig.2.11b SC Resonator with Terminations

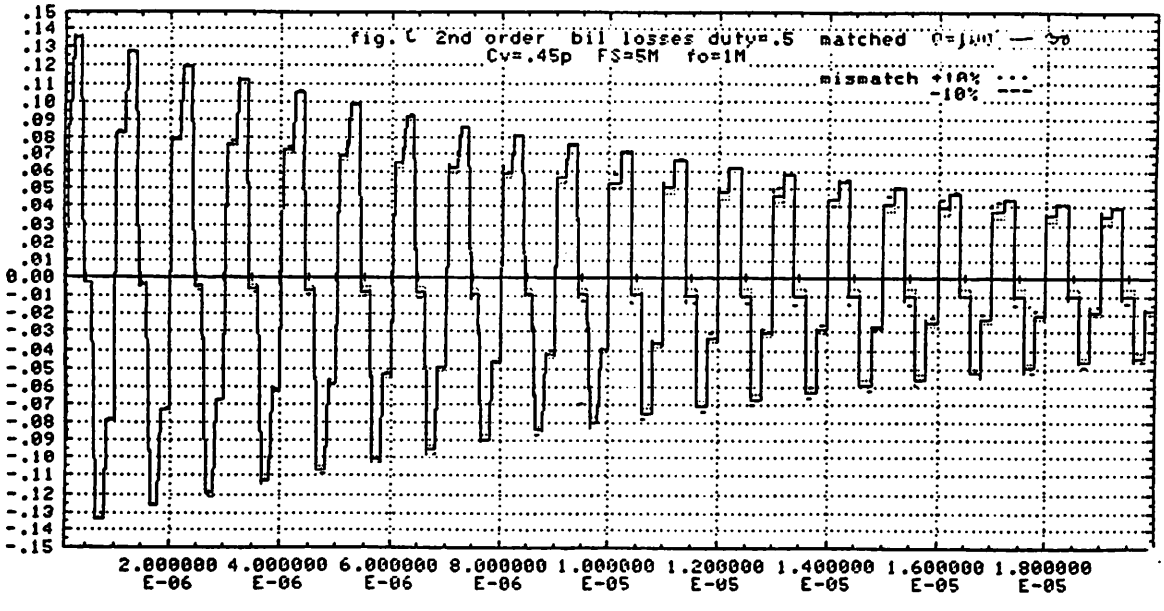


Fig.2.11c Impulse Response for the SC Resonator (Diana)

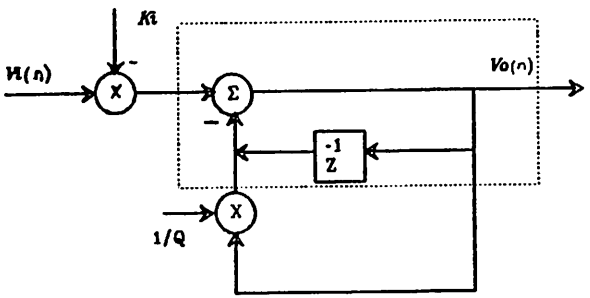
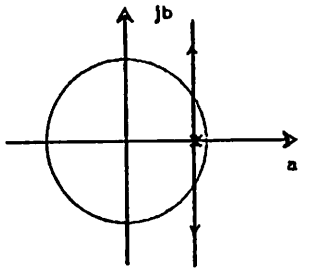
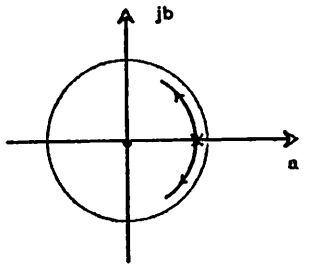


Fig.2.11d

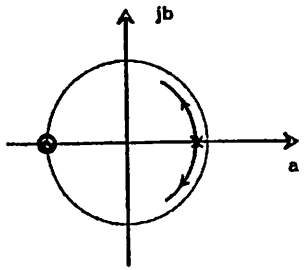
SC Integrator with Gain Ki and Load 1/Q



DDI Lossy Resonator Root Locus



LDI Lossy Resonator



Bilinear Integrators Resonator

Fig.2.12 Root Loci for Integrator Pairs

Ideal amplifiers realizing the LDI integrator have an equivalent transfer function with a half delay :

$$H_i(z) = \frac{V_o(z)}{V_i(z)} = -K_i \frac{z^{\frac{-1}{2}}}{1 - z^{-1}} \qquad (2.12a)$$

This is in reality implemented by using a *forward integrator* (no-delay) and a delayed SC integrator in each pair. For the bilinear SC integrator the transfer function is given by:

$$H_i(z) = \frac{V_o(z)}{V_i(z)} = -K_i \frac{1 + z^{-1}}{1 - z^{-1}} \qquad (2.12b)$$

The particular integrator results in different resonator closed loop locations. The DDI implementation has an extra delay in the loop which creates the phase error effect. The bilinear and LDI mappings have the fundamental property of transforming the continuous frequency axis $j\omega$ into the unit circle on the z-domain, resulting in a very accurate S/D transformation of continuous time filters. The LDI mapping uses a unit of delay injected to the integrator loop to create a zero at the origin and produce the ideal resonator loci, i.e., circular loci centered at the origin of the z- plane. The root locus for the bilinear mapping also follows the circular path due to the fact that the mapping introduces a pair of zeroes precisely at the mirror location of the integrator pole. The characteristics of the different mappings have been studied in the literature [3,84].

2.2.4. SC Resonator Frequency Domain Parameters

In the realization of 2-port lossless filters the resonator loss gives an indication of the loss effects (non-ideal amplifier) on the overall filter. The resonator response is characterized by a complex pole pair in the z-plane and a gain factor. The characteristic parameters are: the peak gain in the passband, $P(\omega_o)$, the center frequency Ω_o, and the $-3dB$ bandwidth. In the case of the active SC

implementation of a lossless resonator, the ratio of the center frequency to the $-3dB$ bandwidth is called quality factor q as opposed to selectivity factor Q used to refer to the selectivity of a terminated resonator or filter. The resonator quality parameter q is :

$$q \triangleq \frac{\Omega_o}{\Delta\Omega_{3dB}} \qquad (2.13)$$

The effects of the integrator loss in the frequeny response of the resonator are a finite resonator gain at the natural frequency $P(\omega_o)$ and a finite $-3dB$ bandwidth, see Fig.2.13a. Another finite amplifier gain effect consists of a shifting of the center frequency value. From the expression (2.12) the error obtained for low loss narrow band filters is of second order and can be neglected; this result is similar to the well known result from active filters. The resonator circuit canonical transfer function in the z-domain, $P(z)$, is:

$$P(z) = \frac{V_o(z)}{V_i(z)} = \frac{K_o(1 - \frac{z}{r_i})}{z^2 - 2R\cos\theta z + R^2} \qquad (2.14a)$$

where R , θ are the polar coordinates of the poles in the z-plane. The lossless resonator has its pole pair located along the unit circle $|z| = R = 1$, (infinite gain at the resonating frequency), see Fig.2.13b.

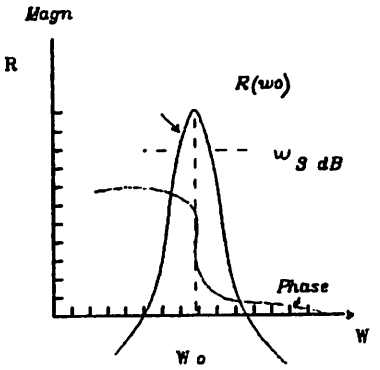
The resonator parameters are given by [6]:

$$f_o = \frac{f_s}{\pi}\sqrt{\theta^2 + \ln^2 R} \qquad (2.14b)$$

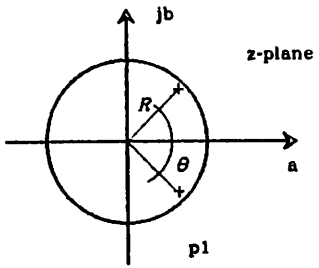
For the narrow-band case this equation can be approximated as:

$$f_o = \frac{f_s}{\pi}\theta \qquad (2.14c)$$

The q factor (resonator quality) is:



Lossy Resonator Freq. Response



Lossy Res. Root Locations

Fig.2.13ab Frequency Response and Root Loci for the SC Resonator

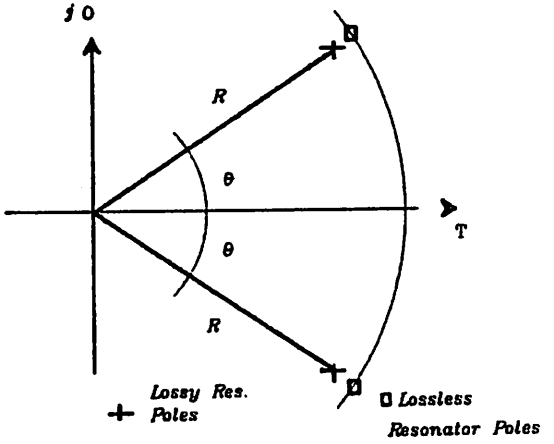


Fig.2.13c

SC Resonator pole locations (detail)

$$q = \frac{\Omega_o}{2fs} \frac{1}{\ln R} \qquad (2.14d)$$

The loss effect is defined by the inverse of the quality q, i.e., $loss = (\frac{1}{q})$. A lossless resonator is represented by an infinite q. For the narrow-band approximation, $\omega_o > \omega_{-3dB}$, the loss effect is given in terms of the pole location radius error $\varepsilon_r = (1 - R)$ [6], which is approximately related to the loss:

$$\frac{1}{q} \approx 2\frac{\varepsilon_r}{\Omega_o T_c} \qquad (2.15c)$$

The radius error ε_r is a function of the pole locations of the integrators in the pair and is given by $(1 - \sqrt{p_1 p_2})$. In terms of the integrator loss ε_{p_i}(2.7c) :

$$\epsilon_r \approx \frac{(\varepsilon_{p_1} + \varepsilon_{p_2})}{2} \qquad (2.15b)$$

In terms of the amplifier finite gain:

$$\frac{1}{q} \approx (\frac{1}{a_{o1}} + \frac{1}{a_{o2}}) \qquad (2.16)$$

The ideal resonator performance required for lossless accurate 2-port filters ($\frac{1}{q} = 0$) demands a means of compensation for the amplifier finite gain. The next section analyzes the effect of the amplifier finite gain on the final value of the transient response within the clock phase.

2.3. The Charge Transfer Process

The continuous-time characteristics of the amplifier are observed in how they affect the discrete time response of the SC integrator. The analysis performed here considers the amplifier response between samples where the

amplifier transfers charge , i.e., $\Phi 1$.[2]

The transient response $V_o(t)$ of the circuit of Fig.2.4 during $\Phi 1$ is equivalent to the step response of the network shown in Fig.2.15a with an input step of value $V_i(nT_c)$ and initial conditions in the integration capacitance, C_f, voltage. The response analysis can be further simplified if we look at the incremental output , i.e., $\Delta V_o = V_o(t) - V_o(nT_c)$, see Fig.2.15b.

The amplifier investigated is assumed to be a fast single stage amplifier and, for that case, the non-ideal operational amplifier characteristics are approximated by the following transfer function :

$$a(j\omega) = \frac{-a_o(\frac{j\omega}{\zeta_1} + 1)}{(\frac{j\omega}{\omega_1} + 1)(\frac{j\omega}{\omega_2} + 1)}; \ \omega_1 \ , \omega_2 \text{ and } \zeta_1 > 0 \qquad (2.18)$$

The frequency response for the fast single stage amplifier in Fig.2.16 shows the finite gain and bandwidth limitations.[3] The closed loop circuit in Fig.2.15 has a transfer function $H(s)$ dependent on the amplifier transfer function $a(s)$ and in the values of the capacitors C_u, C_f:

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{-\frac{C_u}{C_f}}{1 + \frac{1}{a(s)}\left[1 + \frac{C_u}{C_f}\right]}; \qquad \frac{C_u}{C_f} > 0 \qquad (2.19)$$

The unit-step response $h(t)$ is obtained from the inverse Laplace transform of (19). The settling time component of the response is determined by the value

---

2.-In a new double sampling technique developed by Choi and Brodersen [28] the amplifiers transfer charge in both clock phases effectively doubling the sampling frequency.

3.-The step response for the non-ideal closed loop circuit shows two different phenomena as discussed earlier ; namely, a finite rise time and an steady state error. The errors for typical multi-stage high gain amplifiers and for fast single stage designs are compared in terms of the highest band-edge speed and steady state error as shown in Fig.2.17. Fast settling single stage amplifiers designed to deal with higher frequencies inherently have low DC gain which results in a larger steady state error.

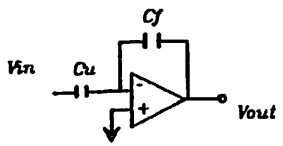


Fig2.15a Equivalent Closed Loop Amp within the Transfer Clock Phase

Step Response

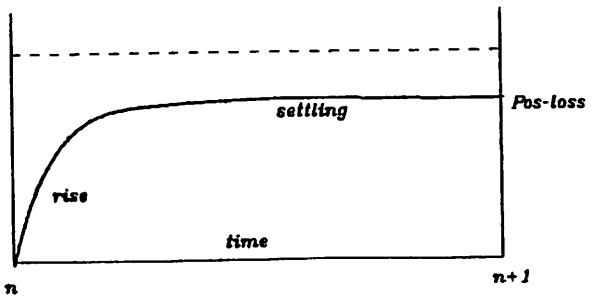
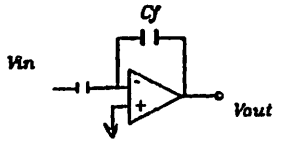


Fig2.15b Transient response within Phase1



Equivalent Circuit within phase1

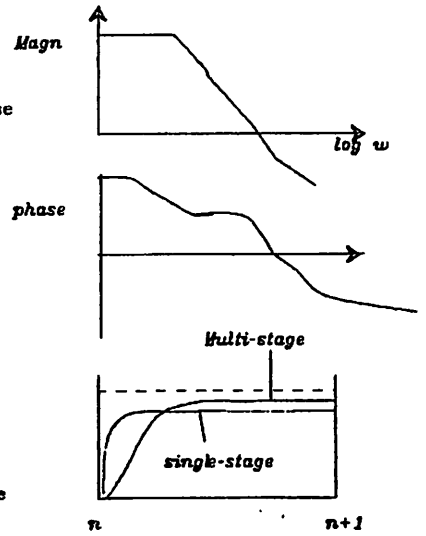


Fig.2.18
Freq. Response

Fig.2.17
Step Response

Fig.2.16 & 17
Amplifier Circuit within Phase1

and type of singularities in the amplifier. [4]

The required accuracy of the filter parameters determines the error band tolerated in the amplifier transient response. For example, a rule of thumb is that for a 10% accuracy on the filter seletivity $\frac{\Delta Q}{Q}$ the error band tolerated must be considerable smaller than 10%. Assuming that the amplifier settles within the clock period, the transient error is determined by the amplifier finite gain and is given by the *final value theorem*, $h(\infty)$:

$$h(t) \approx h(\infty) = H(0) = \frac{-\frac{C_u}{C_f}}{1 + \frac{1}{a_0}(1 + \frac{C_u}{C_f})} \qquad (2.20a)$$

where $H(0)$ is the closed loop transfer function evaluated at DC. The steady state error, ε_{ss}, is given by the difference of (20a) and the ideal amplifier require , $\frac{C_u}{C_f}$:

$$\varepsilon_{ss} = \frac{1}{a_0}\left[\frac{C_u}{C_f} + (\frac{C_u}{C_f})^2\right]\frac{1}{1 + \frac{1}{a_0}(1 + \frac{C_u}{C_f})} \qquad (2.20b)$$

The transient steady state error for the amplifier closed loop response and the z-domain integrator pole location error ε_{ss} (2b) are directly related, since they both are proportional to the inverse of the DC gain.

The resonator loss affects how accurately a filter can be implemented.[5]

4.-The value of the output pulse is obtained by scaling the unit step output by the step size $V_o(t) = h(t)V_i(nTc)$.

5.-For example, in the design of a second-order filter we require an ideal resonator which determines the center frequency and apply an external loading (resistive termination) to determine the transfer function shape, i.e., loaded LC pair selectivity Q_T. The finite amplifier gain effect must be kept well within the required filter selectivity tolerance. The attainable loaded filter selectivity Q in the presence of finite amplifier gain is given by [41] :

$$Q = \frac{1}{\frac{1}{Q_T} + \frac{1}{q}} \qquad (2.21)$$

2.4. Loss Cancellation Technique

2.4.1. Loss Cancellation Alternatives

From the two-port lossless filter theory the overall loss can be canceled by a compensation on every integrator in the filter. Another way to make the cancellation is to approach several integrators at a time. A cancellation of the loss in every two integrators is a natural way to deal with the loss, because such a configuration is almost always encountered in filter circuits.

2.4.2. Cancellation at the Integrator Level.

The most simple approach to compensate for the loss effect (2.16) is to increase the DC gain of each amplifier in the filter. Single-stage differential amplifier configurations may be designed with CMOS to attain fast settling performance with high gain [55] consistent with the amplifier requirements for a bandpass filter with effective Q of 40 ±5% and sampling rate of $5MHz$. In NMOS technology single-stage amplifiers can give the required speed , however the very limited voltage gain per stage due to the lack of a complementary device makes the simultaneous realization of large DC gain and large bandwidth very difficult. NMOS designers have invested a great deal of time improving linear circuit configurations to be able to compete with CMOS in terms of speed and power consumption. A full set of new linear designs has been proposed by Senderowicz that presents comparable characteristics [1]. The design of an NMOS circuit that could deal with the requirements of high frequency narrow-band filters would receive wide acceptance in the NMOS industry. A single stage NMOS amplifier optimizes the circuit speed and can give the required settling time (.5% error band) for $5MHz$ sampling rate. The DC gains of single stages operating with this settling time in NMOS is limited to values of 50–100 as discussed in Chap.4.

This equation indicates that in order to accurately define the filter Q by the termination Q_T, $\frac{1}{q}$ must be kept well below the required Q tolerance.

It is well known that the DC gain can be improved by using positive feedback. Fig.2.18a shows the schematic of a DC positive feedback amplifier using a differential input circuit. The DC gain after feedback is given by:

$$a_{of} = \frac{a_o}{1 - T} \tag{2.22}$$

where the loop gain $T = k_m a_o$ controls the amount of feedback and the gain increase [86]. By making the feedback loop gain close to unity, the amplifier DC gain can be made arbitrarily large as shown in Fig.2.18b. Besides the DC gain increase, the effects of positive feedback are observed in the circuit stability and, in particular, the DC gain sensitivity to the loop gain which also increases without bounds as shown in Fig.2.18c.

The effective DC gain (loss effect) for the positive feedback amplifier is a function of the feedback loop gain. From the allowed tolerance in the filter parameters, viz, $\eta_Q = \frac{\Delta Q}{Q}$, the minimum acceptable amplifier gain can be obtained :

$$a_{oe} \geq 2\frac{Q_T}{\eta_Q} \tag{2.23a}$$

where :

$$\eta_Q = \frac{\Delta Q}{Q} \tag{2.23b}$$

The minimum loop gain is:

$$T_{min} = 1 - \frac{a_o}{a_{oe}} = 1 - \frac{a_o \eta_Q}{2Q_T} \tag{2.23c}$$

PF compensation can be used in active filters but it requires special tuning procedures to guarantee that the right amount of positive feedback is applied

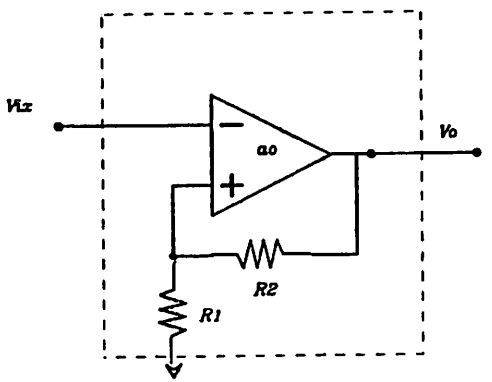
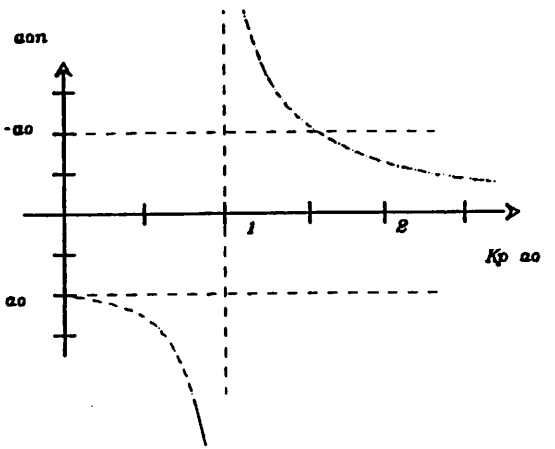
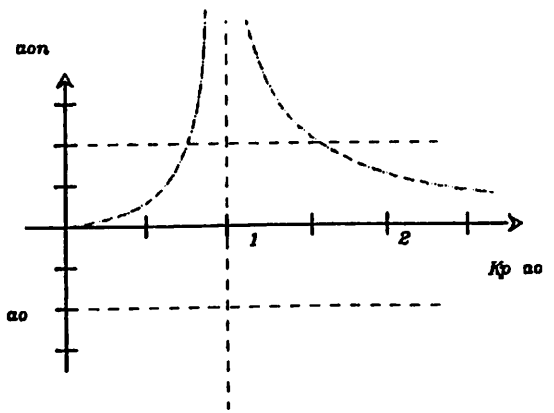


Fig.2.18a Positive Feedback Amplifier

$$\frac{Vo}{Vin} = ao$$



b) DC Gain after PF



c) Sensitivity to Loop Gain

Fig.2.18 Positive Feedback Effects

[8]. In a monolithic implementation the regulation of positive feedback to reliably achieve a stable high gain is complex and presents realizability problems [19]. A design difficulty was encountered in several monolithic PF configurations investigated.

The frequency domain analysis offers a simple tool to for the study of the circuit under positive feedback. In particular, the circuit transfer function root locations and the root displacement given by the feedback provide a great deal of insight on the operation of the circuits. With PF the gain is increased together with the transfer function first corner frequency. The first pole is important because it determines the DC gain which is the essential parameter in the analysis presented herein. The DC gain relates the unity gain frequency and the first pole $\frac{\omega_u}{\omega_{ic}} = a_o$. For the closed loop the dominant pole is shifted towards the origin as shown in Fig.2.19.

$$a_f(s) = \frac{-a_{of}}{\frac{s\tau\left(1 + (1 - k_p)a_o\right)}{(1 - k_p a_o)} + 1} \tag{2.24}$$

When the feedback loop gain is unity, the ideal infinite gain amplifier (continuous time integrator function) is obtained as shown in Fig.2.20:

$$a_{intf}(s) = \frac{-\omega_u}{s} \tag{2.25}$$

where ω_u is the unity gain frequency of the amplifier and also the integrator gain ω_u after positive feedback. Fig.2.21 shows the schematic of the circuit with PF. The closed loop dominant pole location ω_{ic} is:

$$\omega_{ic} = \omega_i\left(\frac{k_i}{1 + k_i} \cdot \frac{1}{a_o}\right) \tag{2.26}$$

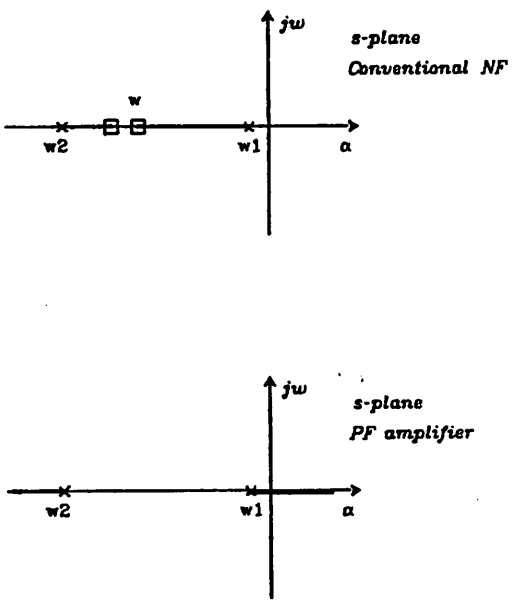


Fig.2.19 Root Loci for NF and PF amplifiers

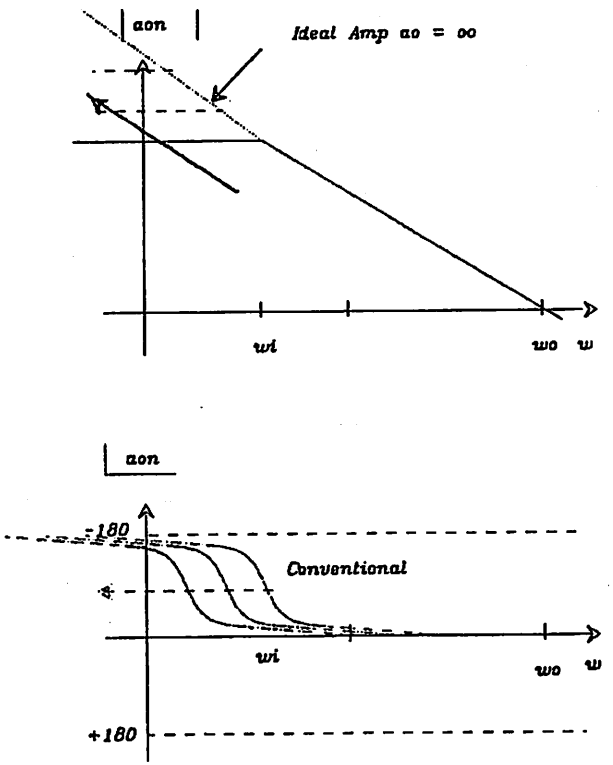


Fig2.20 Bode Plot Showing the Effects of PF

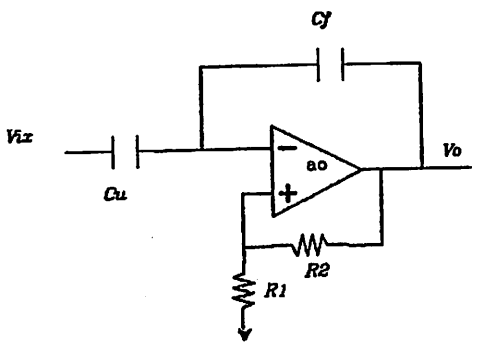


Fig.2.21 Closed Loop PF Amp during phase 1

where $k_i = \frac{C_u}{C_f}$ is the feedback ratio. The effective movement of the pole when closing the loop is given by the first term in the previous equation which is much larger than the open loop pole location. The closed loop pole location for the ideal and the gain limited case are separated by an amount directly related to the second term above, and this separation is a function of how good the gain boost is performed by PF.

The problem is how to guarantee that the positive feedback is accurate and stable. For the design of band-pass filters an alternative simpler solution is possible which guarantees accuracy and stability. This solution consists of a loss cancellation at the integrator pair.

2.4.3. The Negative-loss Integrator and Resonator Loss Cancellation

A balance cancellation consists in canceling the loss in a integrator pair by applying positive feedback to overcompensate one of the integrators of each pair. The overcompensation produces an integrator with an effective *negative-loss* , $\epsilon_{ss} < 0$, as opposed to the positive-loss of the conventional integrator. Notice that negative and positive terms are used to indicate the loss polarity and not the integrator gain polarity: both integrators are inverting integrators as far as the gain polarity is concerned.

From (2.7,16,20) the amplifier in the negative-loss integrator has a change of phase at DC in the open loop (the amplifier in the negative loss integrator is called in the following a negative loss amplifier). The NMOS circuits that present such characteristic are introduced in Chap.4 of this dissertation.

In the z-domain the transfer function for the negative-loss SC integrator has the same form as (2.7) but with the dominant pole larger than unity , see Fig2.22a , ($p_i > 1$).

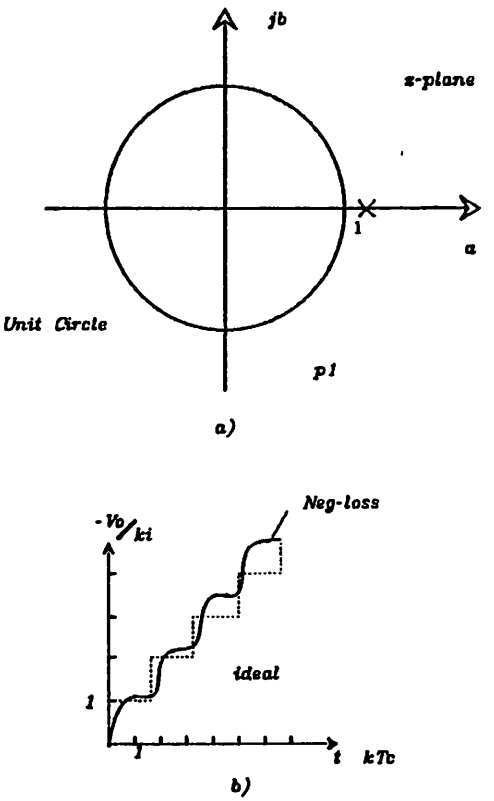


Fig2.22 Negative-loss Integrator a) Root Loci and b) step response

$$H(z) = \frac{V_o(z)}{V_i(z)} = -K_i \frac{z^{-1}}{1 - z^{-1}p_i^{-1}} \tag{2.27a}$$

$$p_{in}^{-1} \approx 1 + \frac{1}{a_o}\left(\frac{C_u}{C_f}\right) \tag{2.27b}$$

The output for this negative-loss SC integrator departs from the ideal ramp in the opposite direction than the positive-loss integrator did as shown in Fig.2.22. Looking at the amplifier transient within Φ1 ; the steady state value converges above the ideal Fig.2.23 by an amount proportional to the loss:

$$h_n(t) \approx h_n(\infty) = H_n(0) = \frac{-\frac{C_u}{C_f}}{1 - \frac{1}{a_o}\left(1 + \frac{C_u}{C_f}\right)} \tag{2.28}$$

A perfect resonator loss cancellation requires an exact matching of the loss value of the integrators. The balanced loss resonator , Fig2.24, transfer function is:

$$P(z) = \frac{-K_1 \frac{z^{-1}}{1 - z^{-1}p_1}}{1 - K_{1,2}\frac{z^{-1}}{(1 - z^{-1}p_1)(1 - z^{-1}p_2)}} \tag{2.29}$$

where p_1 and p_2 are the poles for the positive-loss and negative-loss amplifiers respectively.

Following the same analysis for the conventional case the quality factor for the SC resonator is :

$$\frac{1}{q} \approx \left(\frac{1}{a_o} - \frac{1}{a_{no}}\right) \tag{2.30a}$$

In terms of the DC gain matching (tolerance) i.e. η_a the loss is given by:

$$\frac{1}{q} \approx \eta_a \times \frac{1}{a_{no}} \tag{2.30b}$$

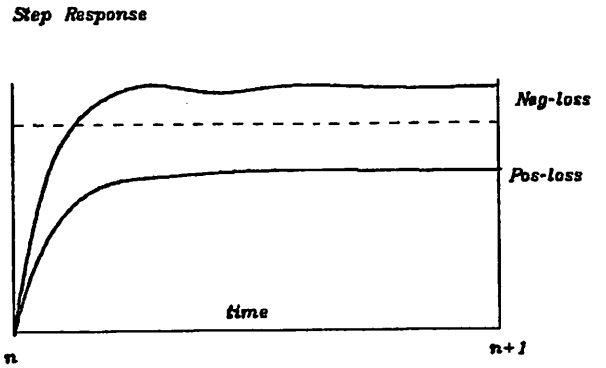


Fig2.23 Transient response withis Phase1

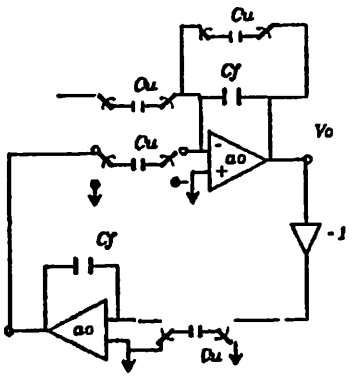


Fig2.24 . Balanced Loss Canceled Resonator

Assuming that the amplifier DC gains are matched the poles in the z-domain for negative and positive-loss circuits are located on the real axis inside and outside the unit circle symmetrically to $R_e(z) = 1$ The loss cancellation technique eliminates the high gain amplifier requirement of narrow-band filters and provides a reliable cancellation as accurate as the process matching permits.

The root locus analysis in the z-domain indicates that the closed loop poles merge together at the center of gravity (root locus breakaway point) which is identically unity for perfect matching as seen in Fig.2.25. The break-away point is the same as the one for the lossless resonator with a complex pair located along the unit circle . The root locus paths are circular for the LDI and bilinear mapping as mentioned before. Any amplifier mismatch in this technique, i.e., $\eta_a = \frac{a_o - a_{no}}{a_o}$, results in a displacement of the z-domain integrator poles in the real axis direction. For the balanced cancellation , the displacement is dependent on the matching and can be made much smaller than the conventional case which depends in the absolute value of the gain. The remaining loss after in the circuit is a small positive or negative number dependent on the direction of the mismatch. The sign of this loss is not relevant as long as the loss magnitude is negligible compared to the filter tolerance in which case it is masked by the value of the filter termination (2.21). If a conventional approach (using high gain amplifiers) would be chosen the equivalent amplifier gain , a_{oe}, would have been:

$$a_{oe} \approx 2\frac{a_o}{\eta_a} \qquad (2.30c)$$

For example: an amplifier DC gain a_o of 50 with 10% tolerance η_a will give for the conventional approach the equivalent of a gain a_{oe} of 1000. Modest gain matching produces considerable improvement. A second order terminated filter with a selectivity Q of 20 accurate within 10%, can be obtained from low gain amplifiers ($a_o = 50$) with gain tolerances of 30%. This requirement is easily met

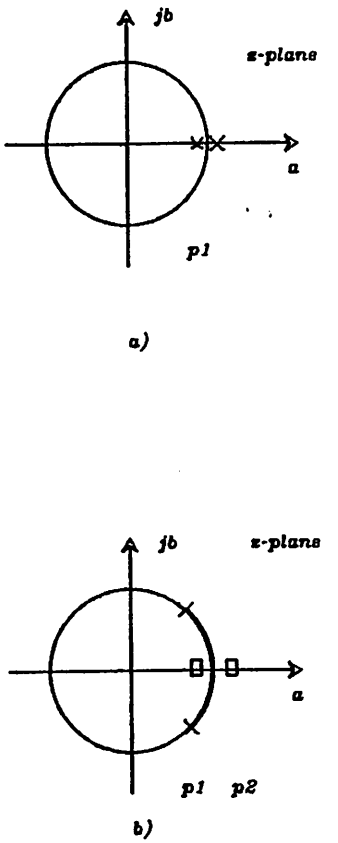


Fig.2.25 Root Locations for the Loss Balanced Resonator: Open Loop and Closed Loop

with state of the art NMOS amplifiers.

2.4.4. Other Requirements for the Negative-loss Amplifier

The discussion on the steady state frequency response has assumed that the amplifier has settled within the clock phase. The negative-loss must also comply with this settling conditions if it is of any use. In the optimum case we would have both amplifiers having the same settling response so that no one of them limits the ultimate filter speed. [6]

The transient steady state error at sampling time matches if the amplifiers DC gain match and the integrators use the same time constants $\frac{C_u}{C_f}$ in the resonator implementation which is indeed the case of the leap frog filter. The amplifier in the negative loss integrator has to have the same termination impedances and bias characteristics. In summary, the negative loss amplifier must use a similar single stage configuration. The prototype negative loss amplifier presented in Chap.4 very closely meets the requirements stated above.

2.5. Negative-loss Network Synthesis

From the amplifier requirements in the negative-loss integrator three network functions are proposed , $a_n(s)$:

1) Non-inverting amplifier.

$$a_n(s) = \frac{+\,a_{no}}{(\frac{s}{\omega_{1n}}+1)(\frac{s}{\omega_{2n}}+1)} \quad ; \ \omega_{1n}, a_{no} > 0 \tag{2.34}$$

6.-When capacitive feedback is applied, the poles, originally on the real axis, merge and split apart following the root locus in the same fashion as the typical resistive feedback. For the transient analysis, the effects at DC are determined by the final charge transfer. Depending in the amount of feedback we can have a transient response of an over-damped, critically damped or under-damped form. In order to optimize the settling, the design must have a well damped response. For single stage amplifiers , the wide band characteristics allow the application of large amounts of Feedback and still have a well damped response. In some cases, the control of the settling is done by zeroes which modify the root locus keeping the roots close to the real axis.

2) Non-minimum phase function. (non-inverting)

$$a_n(s) = \frac{-\,a_{no}(\frac{s}{c_{1n}}-1)}{(\frac{s}{\omega_{1n}}+1)(\frac{s}{\omega_{2n}}+1)} \quad ; \ \omega_{1n}, \omega_{2n} > 0 \ , \ c_{1n} > 0 \tag{2.35}$$

3) Non-Hurwitz single pole (non-inverting)

$$a_{n(s)} = \frac{-\,a_{no}}{(\frac{s}{\omega_{1n}}-1)(\frac{s}{\omega_{2n}}+1)} \quad ; \ \omega_{1n}, \omega_{2n} > 0 \tag{2.36}$$

All the expressions above give approximate functions in terms of the amplifier most dominant poles and zeroes. These approximations are valid as long as the root locus branches pertaining to the main circuit singularities are not fundamentally affected by other non-dominant roots. This implies that the effects from the non-dominant poles on the settling have died away and the remaining error is determined by the finite amplifier DC gain:

$$a_{total}(s) = a_n(s) \times M(s) \tag{2.37a}$$

$$a_{n(s)} = \frac{+\,a_{no}}{(\frac{s}{\omega_{1n}}+1)(\frac{s}{\omega_{2n}}+1)} M(s) \quad ; \ \omega_{1n}, \omega_{2n} > 0 \tag{2.37b}$$

$$M(s)|_{s=0} = 1 \tag{2.38}$$

The root locus for the conventional and the various negative-loss circuits are shown in Fig.2.28a. The root locus for the positive loss circuit depicts the required closed loop poles.

The first alternative for the negative-loss network obtains the modification of the dc gain directly by using a non-inverter amplifier, e.g., in a differential circuit implies the connection of the feedback with the opposite polarity. The root locus is the complement of the conventional negative feedback locus. The poles split apart and the first pole heads towards the RHP eventually resulting

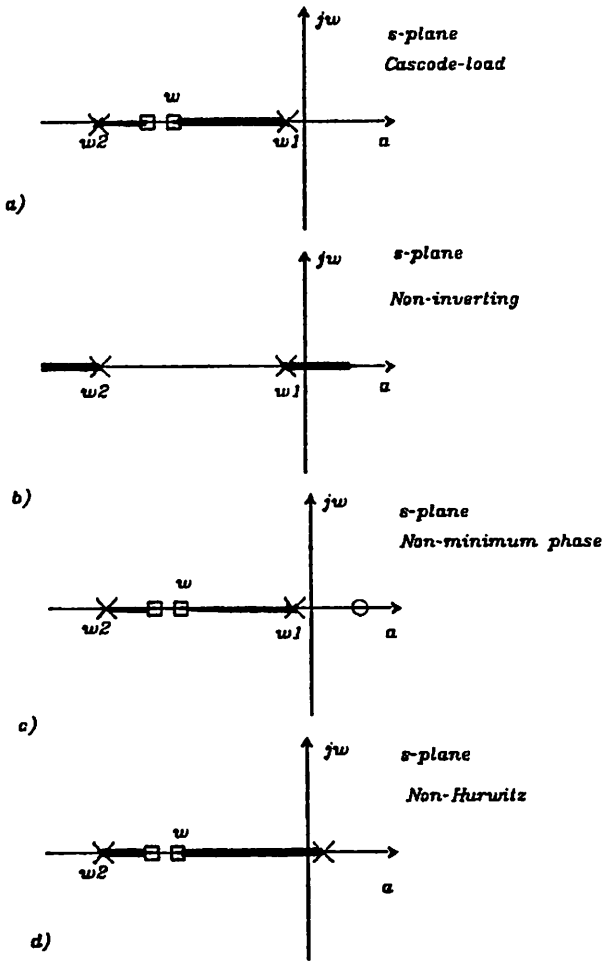


Fig2.26 Root Locus for the Neg-loss Alternatives

in a closed loop unstable pole as shown in Fig.2.26b.

In the second case the roots move in the right direction wide-banding the response and get to the final closed loop location in the (LHP), see Fig.2.26c. If the actual circuit implementation has the second root location similar to the positive loss case, the final settling performance would be comparable. The required phase change at low frequencies is produced by the non-minimum phase zero [57]. The accuracy of the compensation relies on the combined effects of the pole-zero pair and the DC gain.

From the root locus for the non-inverting alternative (first alternative above) an ideal network is proposed which implements *the dual root locus* (more exactly the dual of the dominant pole branch of the root locus as shown in Fig.2.26c). The network has a single pole in the RHP and all the other poles on the LHP. The feedback moves the RHP pole to the stable location on the LHP. The network that provides this behavior is called *conditionally unstable circuit* (non-Hurwitz). It uses the same feedback given by C_u and C_f to produce the negative loss.

For the real implementation of the circuit some considerations related to the high-order poles and zeroes of the amplifier must be made. The second dominant pole merges towards the first as shown in the root locus in a identical manner to the positive-loss integrator. The closed loop pole expression for the non-Hurwitz circuit is also given by (2.26) but in this case the loop gain is moving the open loop pole to the LHP as shown in Fig.2.26. The non-Hurwitz circuit frequency response is shown in Fig2.27.

The NMOS realization of the negative loss circuit uses internal positive feedback in a way such that the single RHP pole is obtained and it uses transistor transconductances to define the dominant pole location. In this form very accurate pole locations can be obtained with low sensitivity and the pole can be

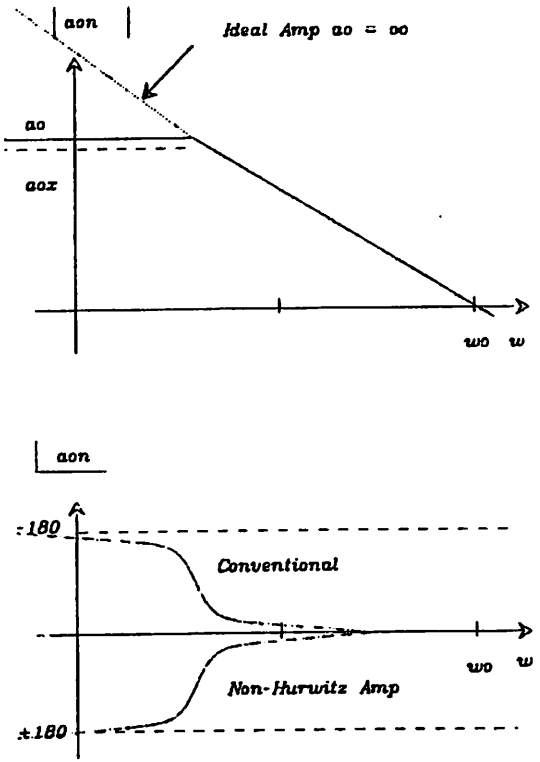


Fig.2.27

Freq. Response of the Non-Hurwitz Amp.

and the conventional amplifier

placed at the mirror location about $R_e(Z) = 1$ of the conventional circuit pole and have the required matching is a function of circuit symmetry. For a perfect match , the open loop amplifier first pole for the positive and negative loss cases are mirror image about the origin $s = o$ as shown in Fig.2.26:

$$\omega_1 = -\omega_{on} \tag{2.39}$$

The open loop DC gains for the conventional and non-Hurwitz amplifiers must match in absolute value for a perfect cancellation :

$$|a_o| = |a_{on}| \; ; \; \frac{1}{q} = 0 \tag{2.40}$$

The third realization alternative, conditionally unstable, was found to be superior in matching of static and transient characteristics. The pole assignment and the matching of the non-minimum phase circuit to the conventional circuit seemed to be more difficult to realize.

The frequency response of the new circuit $a_n(S)$ in open loop exhibits the match in the DC gain and the first pole location. The step response shows a steady state error of opposite polarity. The network can be realized in a monolithic form with a circuit almost identical to the positive loss circuit thus producing very accurate matching properties. Furthermore the circuit similarity guarantees drift-free performance due to the parameter tracking found in IC's; this was demonstrated by SPICE simulations in the presence of temperature and process perturbations.

2.5.1. Implementation Alternatives.

There are several ways in which positive feedback can be locally applied to a differential operational amplifier to produce the non-Hurwitz circuit. Local positive feedback is used to modify the sign of the network impedances (nega-

tive impedance converter) involved in the dominant pole (dc gain) and create the single RHP pole leaving the higher order poles on the LHP. The actual circuit implementation is discussed in Chap.4.

2.5.2. Circuit Stability

The negative loss open loop circuit $a_n(s)$ is unstable due to the presence of the RHP pole , see Fig.2.28. This unstability is conditional in the sense that after the closed loop connection to form $H(s)$ the circuit is stabilized. The closed loop circuit stability is seen in the stable impulse response.

The discussion here is for stability in the small signal case.[7] The large signal stability has to be studied to include the amplifier devices non-linearities. A more formal discussion in terms of the Nyquist stability criterion is presented in Chap.3.

2.6. Summary

We have presented several alternatives for the loss cancellation in active SC filters. The solution presented for the loss on a second order resonator is the use of one overcompensated integrator (negative loss) in the integrator pair. The types of functions which can realize the negative loss are studied an the best candidate is selected based on symmetry properties and. The concepts of controllability and observability for the new positive feedback circuit were discussed.

CHAPTER 3

FEEDBACK AND CONDITIONAL STABILITY

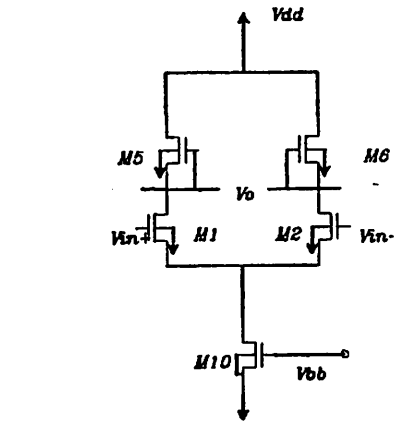
3.1. Introduction

This chapter is dedicated to the analysis of the conditional unstable circuit and the feedback configuration used to guarantee circuit stability. The class of circuits presented fall in between two main streams of circuit analysis: linear and digital circuit design. In the former, the design is very much concerned with accuracy and strict stability of the circuit functions. In the latter, the designers are interested in the speed of the switching functions (bi-stable and multivibrator circuits). The different approaches in these two fields are based on a division of the feedback concept into negative feedback (NF) and positive feedback (PF). This divided approach has missed the development of conditionally unstable circuits which can be stabilized and used advantageously in *linear circuits*.

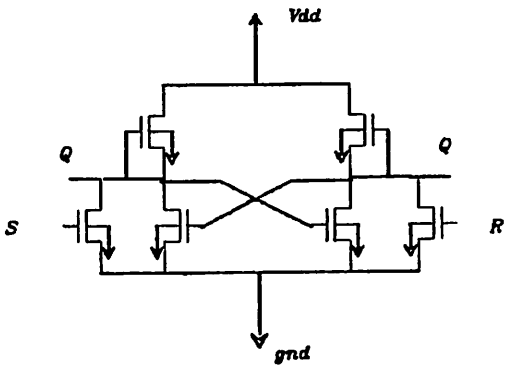
Although feedback is in itself one of the subjects which has received more emphasis in electrical engineering, the aspects treated in this work have not been given enough attention in circuit design literature. As a consequence they have not been used in actual design. Almost all the research has been centered on negative feedback in the context of linear or a non-linear circuits. Fig.3.1 shows a typical linear and non-linear (unstable) circuit.

3.2. An Illustrative Circuit

The simple circuit in Fig.3.2 is used to facilitate the presentation of the new conditionally unstable concept. The amplifier has a positive DC gain



Linear Differential Single Stage Amp



Bistable Circuit (Digital SR Flip Flop)

Fig3.1 Linear and Digital Circuits

Finite Gain Op amp
Infinite Bandwidth

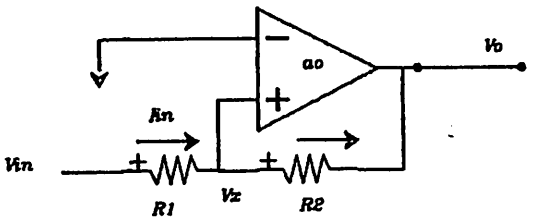


Fig3.2 Negative-loss Amplifier

$a_o > 0$. Feedback applied as shown is positive since the loop gain is positive. A loop gain larger than unity is assumed. (in here the resistive case is selected because it is more familiar , however the equations for the capacitive case are identical). The network equations give the stable closed loop characteristics:

$$I_{R_1} = \frac{V_{in} - V_s}{R_1} \tag{3.1a}$$

$$I_{R_2} = -\frac{V_o - V_s}{R_2} = I_{R_1} \tag{3.1b}$$

The amplifier with the resistive feedback provides a negative input resistance when the loop gain T is larger than unity, see Fig.3.3.

$$r_i = R_2 (1 - T) \tag{3.2a}$$

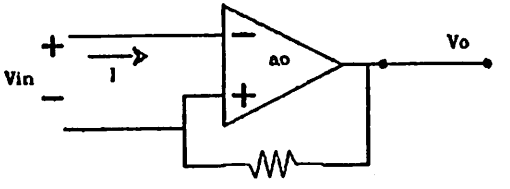
The amplifier input voltage is forced to go negative in response to the input step signal ; the output voltage is given by:

$$V_o = -a_o V_s \tag{3.2b}$$

The output is:

$$\frac{V_o}{V_i} = \frac{-\frac{R_2}{R_1}}{1 - \frac{1}{a_o}(1 + \frac{R_2}{R_1})} \tag{3.3}$$

The voltage across R_1 will be larger than the input by an amount inversely proportional to the gain (for the conventional NF case the voltage across the input resistance was smaller than the input by an amount proportional to the amplifier gain). For the infinite bandwidth amplifier , a stable condition is reached with the finite current flowing through the input and feedback resistors. The steady-state error in the step response is a function



$$rin = \frac{Vin}{I}$$

Fig.3.3 One Port Negative Resistance

of the DC gain as shown in Fig.3.4a. The capacitive feedback circuit is shown in Fig.3.4b. The transfer characteristic is the same as the resistive case (3.3b) with the substitutions $R_2 = C_f$ and $R_1 = C_a$. The resistive and capacitive circuits have dual systems of equations where the resistor is the dual of the capacitor and the current is the dual of charge. The duality is based on the fact that the capacitor network responds only to the time derivative of the signal. In the final steady state current flows in the resistive case with:

$$V_o = R_2 I_{in} \; ; \text{and} \; \frac{d(I_{in})}{dt} = 0 \tag{3.4}$$

whereas in the capacitive case the steady state is represented by charge:

$$V_o = C_f q_{in} \; ; \text{and} \; \frac{d(q_{in})}{dt} = 0 \tag{3.5}$$

In practice, if we build a prototype circuit to demonstrate this result using a standard op-amp, it will most probably be unstable due to the finite band-width of the amplifier circuit. This is because the feedback moves the amplifier poles towards unstable locations in the RHP. The amplifier open loop transfer function is assumed to be given by:

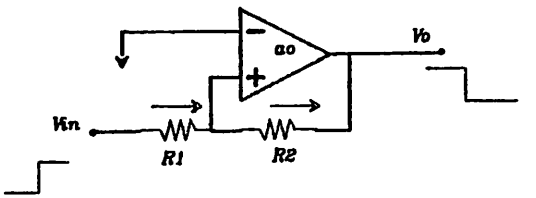
$$a(s) = \frac{+ a_o}{\frac{s}{\omega_i} + 1} \tag{3.6}$$

The closed loop function has the form:

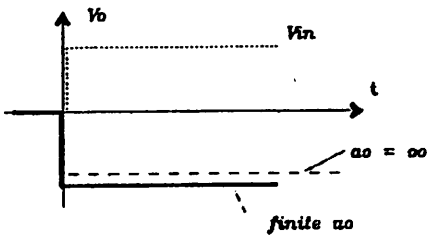
$$H(s) = \frac{-\frac{R_2}{R_1}}{\frac{s}{a_o \omega_i k_p} + \frac{1}{a_o k_p} \cdot 1} \tag{3.7}$$

where the dominant pole is given by:

All Resistive Feedback



Negative-loss Amplifier



Capacitive Feedback (charge)

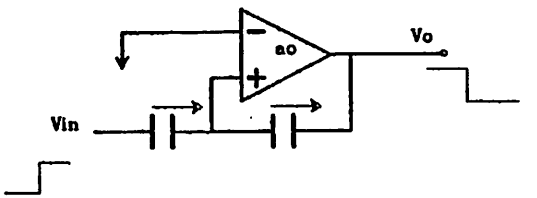


Fig.3.4 Closed Loop Amplifiers

$$s = \omega_1 (a_o\, k_p - 1) \tag{3.8}$$

where $a_o\, k_p$ is the loop gain and $k_p = \frac{1}{1 + \frac{R_2}{R_1}}$ or $\frac{1}{1 + \frac{C_1}{C_f}}$. The pole can then be moved to the RHP for a given amount of feedback. The system is conditionally stable to the value of the feedback loop gain. In particular the pole goes to the origin for a loop gain of unity $k_p = -(\frac{1}{a_o})$. For loop gain larger than 1, the phase at DC experiences a jump of 180° , see Fig.3.5a. The effects in the frequency domain are shown in Fig.3.5b. In particular the mirror of the open loop location is achieved for a loop gain of:

$$k_p = \frac{2}{a_o} \tag{3.9}$$

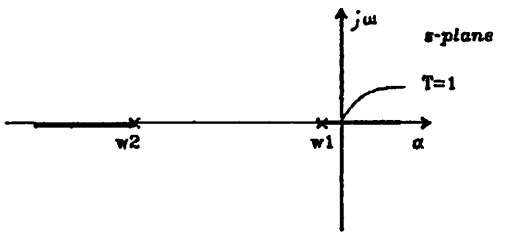
and the closed loop DC gain is :

$$aon = -(a_o - 2) \tag{3.10a}$$

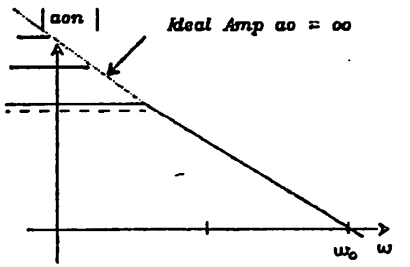
An unstable closed loop system results for a given value of the loop gain. However, instability does not result for all cases, as was seen in Chap.2. [1]

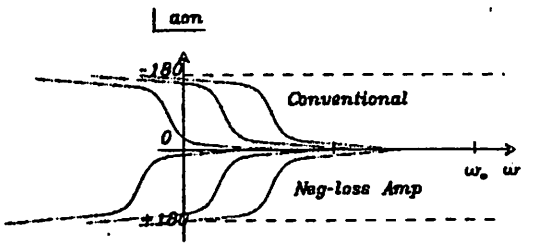
$$a(s) = \frac{-a_o}{\frac{s}{\omega_1} - 1} \tag{3.10b}$$

If the open loop system has a positive DC gain with a pole in the RHP the pole for the closed loop will be moved to the stable location. Root loci analysis for these networks is complicated by the fact that the circuits are not uni-lateral and an arrangement of the transfer function has to be performed in order to obtain the *true root loci*. A more formal discussion of the concept *conditional unstability* in terms of the Nyquist stability criterion is presented next.



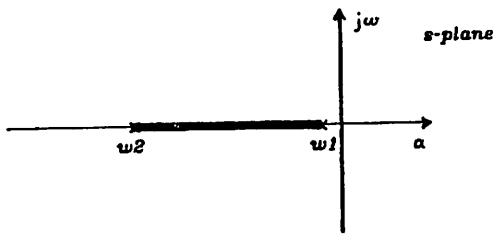
a) Root Locus for the PF Circuit



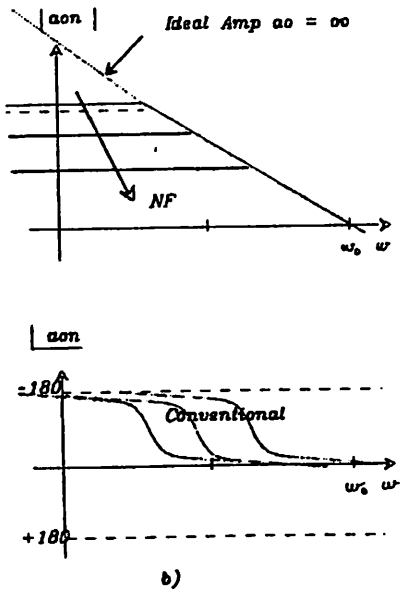


b)

Fig3.5ab PF Effects, Roots and Bode Plot



a) *Root Locus for the PF Circuit*



b)

Fig.3.6 NF Effects, Root locations and Bode Plot

3.3. Conditional Instability

The stability of a system is ultimately dependent on the systems parameters. The study of the conditions under which a given system can have an unstable behavior can be derived from the analysis in the frequency and time domains. The concept of conditional stability usually refers to a stable system (open loop) unto which feedback is applied. The stability analysis then determines the conditions under which the closed loop system is unstable (Routh Test, Nyquist Plot).

The concept above can be reversed, meaning that a feedback properly applied can modify an open loop unstable system to produce a stable closed loop system. In linear systems this argument is supported by the Nyquist stability criterion. In this work, a conditional unstable system is presented which is stabilized by feedback as presented in Chap.2. This is a typical compensation problem in Control systems. An example of a system with such characteristics is the classic problem of stabilization of a vertical pendulum [59].

1.- "Comments on stability"

If all the characteristic equation roots of a system are in the LHP the system is absolutely stable (bounded-input bounded-output stable). In the case of ideal passive elements we have stable systems in the sense of *Lyapunov*, i.e.L. (marginal stability) which includes pure oscillatory systems , i.e., ideal LC (lossless) resonator [62]. In real passive systems the components have dissipation which eventually make the system energy (Voltage and current) tend to zero (degeneration elements), i.e., strict stability (Asymptotically stable-in-the-sense-of-Lyapunov). The loss or dissipation is associated to a shift of the system poles inside the LHP.

Real oscillatory systems can be obtained by the use of active elements which supply the energy dissipated by the physical positive-losses, [61]. , e.g., LC active oscillator [75]. To produce an oscillator the active element has the effect of moving the poles to the $j\omega$ axis. If the poles are shifted further, they will eventually cross to the RHP to give an unstable circuit ; the circuit response is limited by non-linear effects in the circuit which add the necessary dissipation (limiting process) to keep the circuit poles along the imaginary axis.

The circuit activity as opposed to passivity can be stated formally in terms of the characteristic equations of the circuit elements (Energy dissipation or generation). In practice, it is sufficient to have the system transfer function representation to be non-Hurwitz to recognize an inherent activity involved [61]. Fig.3.7 shows two examples, one in which NF is used and the excess phase of the active elememts force the circuit to a unstable condition i.s.L. (NF conditional stability). The other circuit shows a stable system and how PF produces instability. These two examples present two causes of instability usually encountered in circuit design. In circuit design, the oscillation process is studied by the large signal transfer function which includes the non-

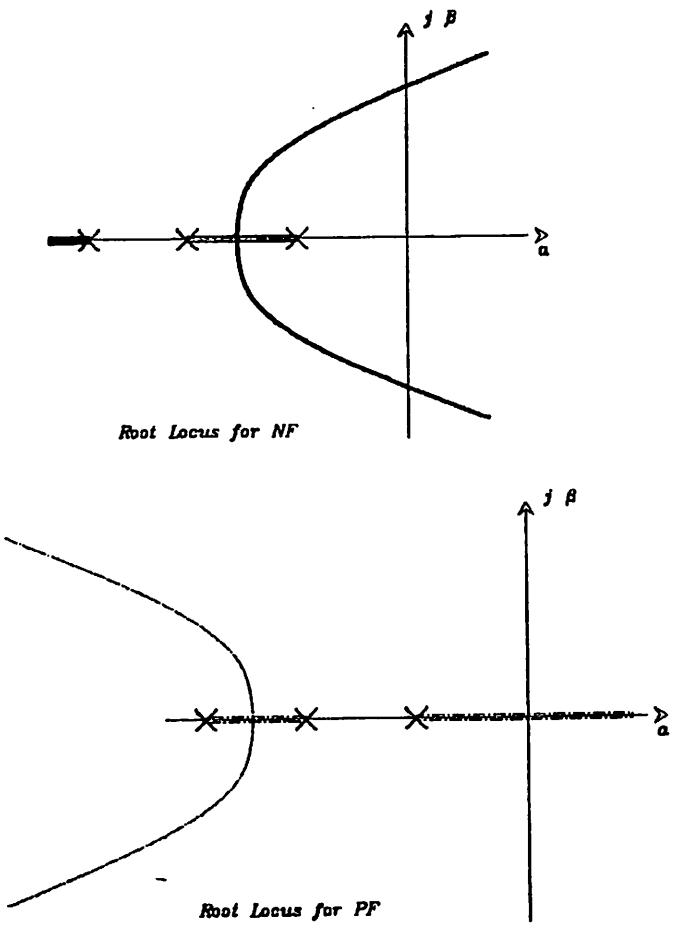


Fig.3.7 Complementary Root Locus for NF and PF

The non-Hurwitz circuit in Chap.2 is conditionally unstable and can be stabilized with capacitive feedback for small signals. Stability is only locally limited to the active operation of the devices in the network, e.g. , the negative resistance region on a cross coupled device.

The existence of a feedback configuration that stabilizes the unstable system in general is formally supported by the Nyquist stability criterion as follows: The open loop function has a number of poles in the RHP (P), for our case $P = 1$. For the Nyquist analysis we plot the loop transfer function and count the number of times (N) that the curve encircles the point, $R_s H(j\omega) = 1$ for PF case, and the number of closed loop poles which determines the stability is given by: $Z = P - N$ (Fig.3.8a). For the single RHP pole in open loop one encirclement will lead to stable closed loop behavior which is indeed the case for the feedback circuit proposed and studied in Chap.2. In the Nyquist polar plots, the frequency domain (gain and phase) requirements for the stabilizing feedback circuit are obtained. These considerations apply for the local stability around active device conditions.

If Nyquist analysis guarantees stability, it means that the closed loop system has all the poles back in the LHP as shown in Fig.3.6b. [2] The practical utilization of the concept of conditional unstability in a linear circuit is simplified by the use of simple systems (single stage amplifiers) whereas in high order systems the compensation for conditional instability can be very complex. This stability analysis does not guarantee the system absolute stability due to the fact that the amplifier has nonlinear devices. The non-linear effects in the system are determinant to the large signal stability . The analysis including the non-linearities is presented next.

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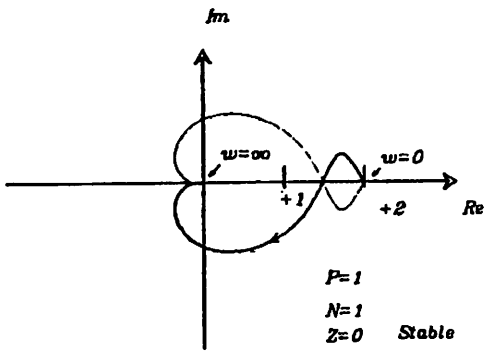
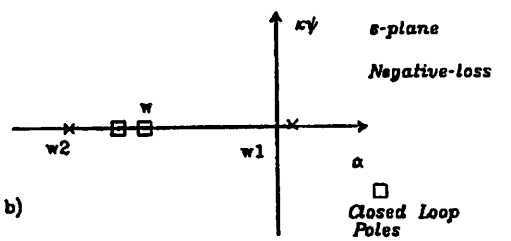
linear limiting considerations [75].



a) Nyquist Plot of the PF Circuit Loop Gain



b)

Fig.3.8 Negative loss Amplifier
Root Locus for Feedback Capacitance

3.3.1. Non-linear Analysis of Conditional Instability

The system with non-linearities is represented by a set of non-linear time-invariant differential equations. The complexity of the system even for this single stage amplifier is great and the theoretical analysis is not attempted here. Instead this dissertation present the experimental results which showed the stability (large signals) of the system as given in Chap.5. In the design stage however, the nonlinear system was fully simulated in the computer to have a preview of the circuit large signal behavior. The formal analysis of the system is very complex. Even gross approximations of the nonlinearities will result in complicated nonlinear equations similar to the Hill equation [74]. The availability of powerful circuit simulator programs like SPICE make the study of the circuit behavior much simpler.

Nevertheless it is essential to study the particular theoretical aspects of a nonlinear differential system to be able to establish and justify the tests to be performed in the simulation , e.g., transient large signal analysis, and the initial conditions and boundary values necessary for the simulation program. The analysis of the non-linear circuit in a simplified form is done next in order to form the required theoretical background.[3] The derivation of the system equations is performed in App.C. In this section the effect of the finite output resistance of the devices is neglected. The computer simulation of the circuit in closed loop is performed including all the transistor non-linearities. Fig.3.9a Shows the large signal circuit schematics of the

2.-The closed loop stability of the open loop negative-loss system is a classic problem of compensation in control systems [63]. In that example the goal is to stabilize an open loop unstable system (plant) and the compensation network design is presented. Another example of a conditional unstable system is the inverted pendulum [59]. This mechanic system analogy is very helpful in clarifying the operation and the stability of the closed loop circuit including large signal dynamics, non-linearities , etc.

3.-The simulation results must be carefully evaluated due to the fact that numerical approximation of the system equations can show stable response for unstable systems because the

differential amplifier in open loop.

The conditional unstable system dynamics (open loop) are described by the fourth order non-linear differential equation :

$$\begin{aligned}
\dot{V}_3C_3 &= V_3g_3 + f(V_3 - V_5) - f(V_1) + K \\
\dot{V}_5C_5 &= V_5g_5 + f(V_3 - V_5) + V_{dd}g_5 \\
\dot{V}_4C_4 &= V_4g_4 + f(V_4 - V_6) - f(V_2) + K \\
\dot{V}_6C_6 &= V_6g_6 + f(V_4 - V_6) + V_{dd}g_6
\end{aligned} \tag{3.12a}$$

where V_1 and V_2 are the input voltage drive and V_N are the node voltages, $gnCn$ are the total conductance and capacitance associated with each node and $f(v)$ are the multi-variable large signal device characteristics for the driver and cascode devices. The driver nonlinear characteristics in the saturation region are:

$$f(V1,V3) = \mu C_{ox}\frac{W}{2L}\left[V_1 - Vt\right]^2(1 + \lambda V_3) \tag{3.12b}$$

And for the triode region:

$$f(V1,V3) = \mu C_{ox}\frac{W}{L}\times\left[V_1 - Vt - \frac{V_3}{2}\right]\times\left[V_3\right] \tag{3.12c}$$

where Vt is the threshold voltage W and L are the device dimensions and V_1 is the gate to source voltage large signal voltage , and V_3 is the drain to source voltage. The equations for the other side of the circuit are obtained simply by exchanging $V1, V3$ for $V2, V4$. The circuit is biased in the active region by a bias current I.

The cascode load nonlinearity also has two operating regions as follows:

simulation solution has its particular numerical stability conditions.

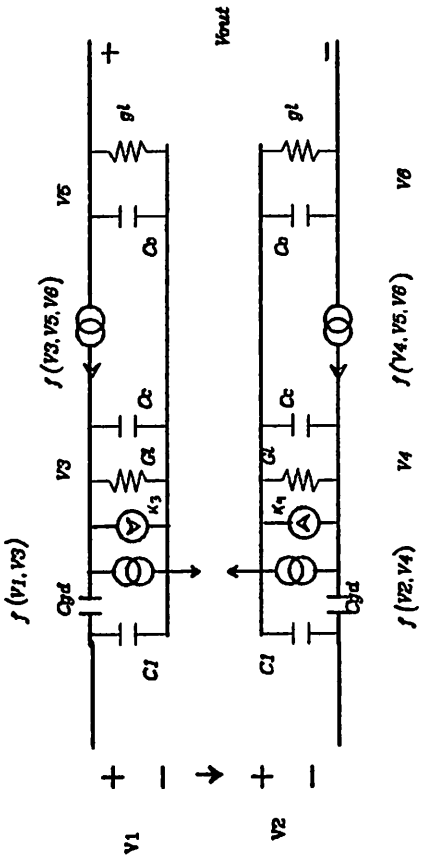


Fig.3.9a Large Signal Model for Negative-loss Amp

$$f(V3,V6,V5) = \mu C_{ox}\frac{W}{2L}\left(V_3 - V_6 - Vt\right)^2(1 + \lambda V_5 - V_3) \qquad (3.12d)$$

for the saturation region and:

$$f(V3,V6,V5) = \mu C_{ox}\frac{W}{L}\times\left(V_3 - V_6 - Vt - \frac{(V_5 - V_3)}{2}\right)\times\left(V_5 - V_3\right) \qquad (3.12e)$$

The equations of the other half circuit are obtained in the same way as before. The equations (3.12) are presented in block diagram form in Fig.3.9b. The circuit uses NMOS D loads which also give a nonlinear load characteristic , i.e., conductance function of the square root of the current. The solution for this nonlinear system depends strongly on the initial conditions and the kind of forcing functions employed (input drive variable). The set of boundary conditions for the nonlinear system is bounded due to the physical constrains of supply voltage and power. The systems output is the differential voltage $V_5 - V_6$. The complexity of this system makes a hand solution virtually impossible. The complexity of the nonlinearities do not present a well behaved system. The state of the art analysis of stability in the large by Popov and the Nyquist methods are difficult to apply for the system presented here and sufficient conditions for stability can not be guaranteed.

Some empirical relations can be obtained by analyzing partitions of the circuit, e.g., the cascode total nonlinearity can be obtained independent of the driver nonlinearity. From these procedures, some transfer functions approximations can be obtained which facilitate the understanding of the system behavior. Other simplifications can be obtained if the devices dependence on output voltage is eliminated leading to a lower order nonlinearity of the system equations.

The driver device is characterized by a monotonic nonlinearity (memoryless) given simply by the transistors output characteristics as

shown in Fig.3.10.

One more simplification is obtained by limiting the output range by clamping devices. The boundary conditions affect the nonlinear system in a way that the signal amplitude is limited to values where the transistor devices have enough gain to guarantee the recovery of the system to the active region. are affected in the direction of guarantee stability in the large. The nonlinearities in the load can be combined to give the nonlinear equivalent resistance characteristic which shows a hysteresis type nonlinearity as shown in Fig.3.11.

The open loop system dynamics are represented in block diagrams with the static nonlinearities separated from the frequency dependent characteristics Fig.3.12a. The system open loop static nonlinearity was obtained by SPICE simulation and it showed to have the form of a S shape function as shown in Fig.3.12b. Empirically the function can be fitted by a cubic (hysteresis) nonlinearity :

$$V_i = \alpha_1 V_o - \alpha_2 V_o^3 \qquad (3.13)$$

Such a system can operate in three different regions of the characteristics. For operation inside the negative slope region, the circuit gain is positive due to the negative resistance load. The gain is negative for the outside regions where the negative resistance has collapsed to a conventional (positive) resistance.[4] The conditionally unstable amplifier in open loop was simulated in SPICE to prove large signal response to initial conditions in the three operating regions. The system showed the typical bistable characteristic resulting from the hysteresis nonlinearity, i.e.,. similar to the Schmitt

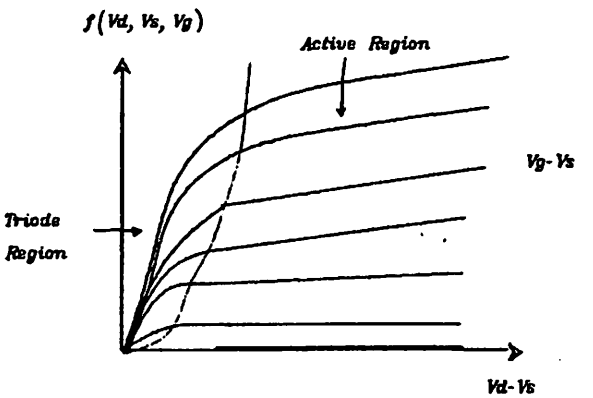


Fig.3.10 Transistor Nonlinearity

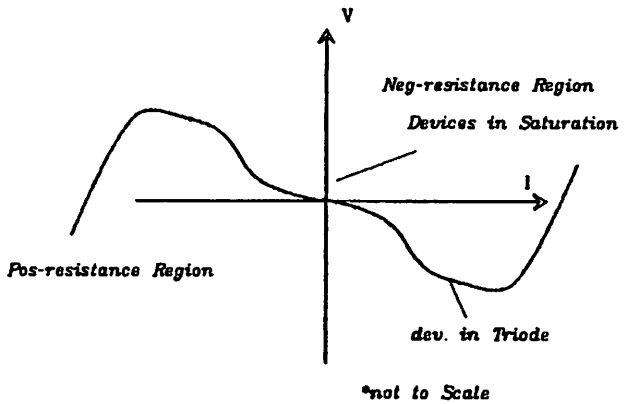
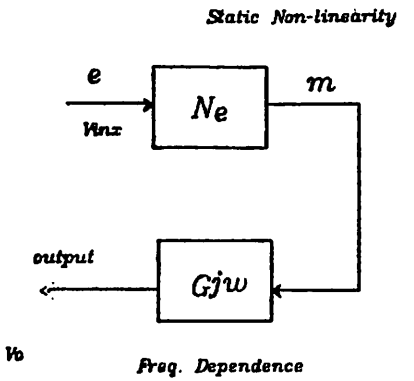
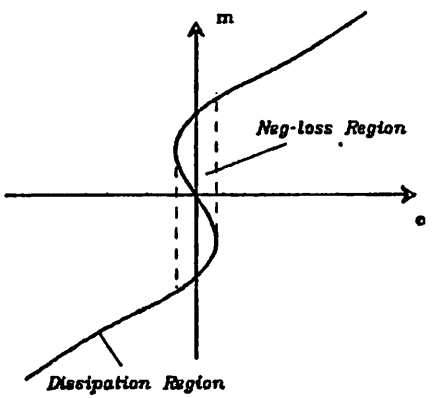


Fig.3.11 Nonlinear Negative Resistance



a) Nonlinear System
Open Loop Block Diagram



b) Hysteresis Static Nonlinearity

Fig.3.12

trigger circuit response. The results are plotted in the form of phase plane portraits in Fig.3.13.

The analysis of a system with this kind of nonlinearity is a classical problem in nonlinear oscillation circuits [74]. , viz, relaxation oscillators or bistable trigger circuits. A very interesting analysis of the system response as a function of the different input forcing functions has been presented by Hurtado [76]. Of particular interest is the result that the system under trigger traverses a region of indecisiveness where the output can stay for a not determined period of time. The analysis is based on simple models and the solution obtained by the perturbation method. The conditional unstable circuit is used with charge feedback (Capacitive input and feedback elements) in a sampled-data (S/D) system. The system of equations for the closed loop are presented next.

3.3.2. The Conditionally Unstable Circuit with Capacitive Feedback

Based on the open loop large signal dynamics described let us proceed to apply the feedback compensation which delivered the stable circuit for small signal (Chap.2). The circuit schematics show the feedback configuration , see Fig.3.14. The system block diagram is depicted in Fig.3.15. The system equations for the closed loop are also derived in App.C and represent a sixth order system (in these equations the finite output impedance of the transistors is neglected):

4.-The nonlinearity of the system produces three equilibrium points; one at the origin which is unstable , and two points symmetrically located about the origin which are asymptotically stable (so called meta-stable states because the system can be triggered back and forth between them by the input. Any initial condition inside around the origin will turn to drive towards one of the meta-stable points. The system response for this nonlinear case is strong function of the initial conditions and the type of input signals applied.

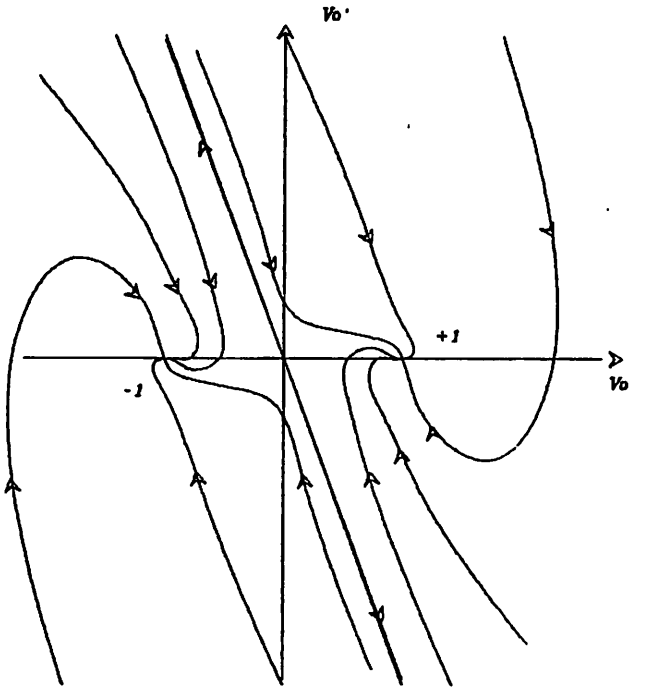


Fig.3.13

Phase Plane Portrait for a Bistable Circuit

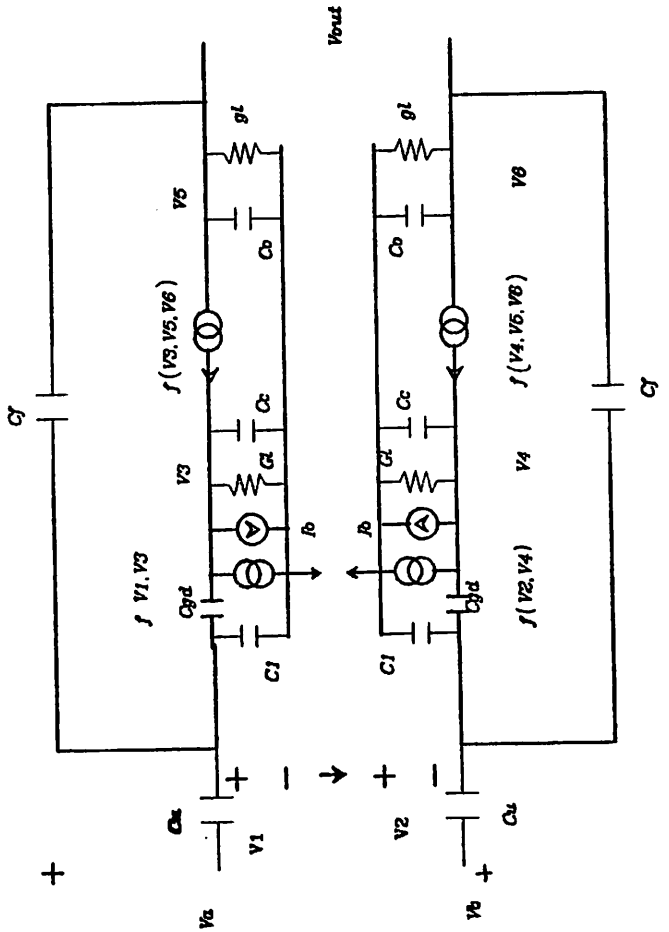


Fig.3.14 Large Signal Model for Negative-loss Amp with apacitive Feeback

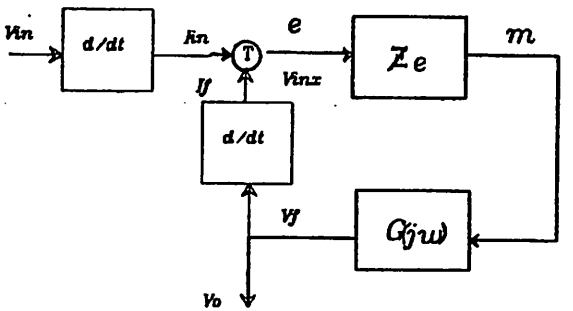


Fig3.15 Block Diagram of the Closed Loop Amplifier H(jw)

(3.14a)

$$\begin{aligned}
\dot{V}_a Cu1 + \dot{V}_1(C_f - Cu1 + C_s) - \dot{V}_5 C_f &= 0 \\
\dot{V}_b Cu2 &= 0 \\
\dot{V}_3 C_3 + \dot{V}_2(C_f - Cu2 + C_s) - \dot{V}_6 C_f &= -f(V_3 - V_6) - f(V_a) + V_3 g_3 + k_3 \\
\dot{V}_4 C4 &= -f(V_4 - V_5) - f(V_b) + V_6 g_5 + k_5 \\
\dot{V}_5 C_5 &= -f(V_4 - V_5) - V_5 g_5 + k_5 \\
\dot{V}_6 C6 &= -f(V_3 - V_6) - V_6 g_6 + k_6
\end{aligned}$$

where V_a and V_b are the differential input large signals given by:

$$V_a = V_1 + \frac{V_z}{2} \quad and \quad V_b = V_1 - \frac{V_z}{2} \tag{3.14b}$$

where V_z is a common mode signal.

The type of feedback utilized is shunt-shunt feedback with capacitive feedback and input coupling elements. These elements realize the time derivative function for the input voltage which is a step like signal. The input voltage signals are differentiated by the input capacitor to give the impulse like current signal to the amplifier (step charge). In the same form the output voltage variable is fedback as a current. Fig.3.16 shows the block diagram of the S/D nonlinear system.

As for the open loop system, computer simulation was used to evaluate stability. The main consideration at this point is that the closed loop system has proved to have a locally stable response in the active region. That implies that for any initial conditions around the active region, the system is asymptotically stable. Large signal stability must be studied to find out if any other stable point or limit cycle exists in the characteristics.

3.4. Computer Simulation

In order to solve the system and evaluate the stability, the full circuit was simulated in SPICE using as initial condition points outside the active

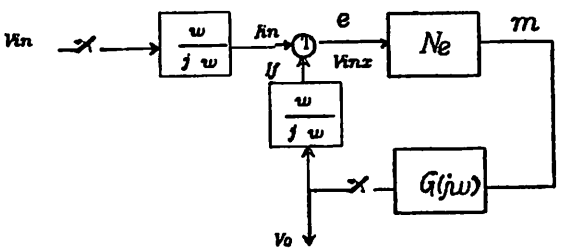


Fig.3.16

Closed Loop System with Sample Switches

region and applying the typical set of forcing functions available from the S/D system.[5]

The transient (large signal) analysis in SPICE shows that the feedback and forcing functions modify the system producing a single stable equilibrium point as shown in Fig.3.17. By proper manipulation of the input signals, this equilibrium point can bring the circuit to the active region where local stability exists.[6] This result means that even in the case of large signals perturbing the system outside the active region, the trajectory solutions return to the active region , viz, any other equilibrium points or limit cycles are unstable in the large so that the response eventually returns to the asymptotic stable region.

The phase plane analysis is used to illustrate the trajectories for the closed loop system. The circuit simulated also included the limiting at the output done by clamping devices which has the effect of holding the nonlinear load transistors in a region where the voltage gain is still considerably large which produces a faster and more reliable return to the active region, see Fig.3.18. The circuit stability within the linear region exists due to an effective degeneration created by the feedback. The simulation was done in the time domain and includes power supply transients. The closed loop cir-

5.-The system modeling and solution obtained by the computer can be misleading for the cases where there is marginal instability in the system. In fact the integration algorithm has to be very accurate to detect the stability of the system. The digital integration algorithm utilized must not include self damping which can make the circuit instability disappear form the numerical solution , e.g., gear Method level2. The simulation in SPICE was then done by trapezoidal and Gear third order integration.

6.- At this point , the mechanical analogy helps to understand the re-entry behavior. The vertical pendulum with a nonlinear limiting of the angular position θ is bistable in open loop. By a position forcing function at the pendulum base, the system can be brought to the operating region where the system is stable. Large perturbations can put the pendulum back to one of the outside states however the large signal stability means the return to the active region by the manipulating variable is possible. One extra consideration must be brought into the picture of this analogy and that is the S/D character of the circuit which can be represented in the analogy by a time varying brake which holds the instantaneous position of the pendulum for one clock phase and releases for the active clock phase.

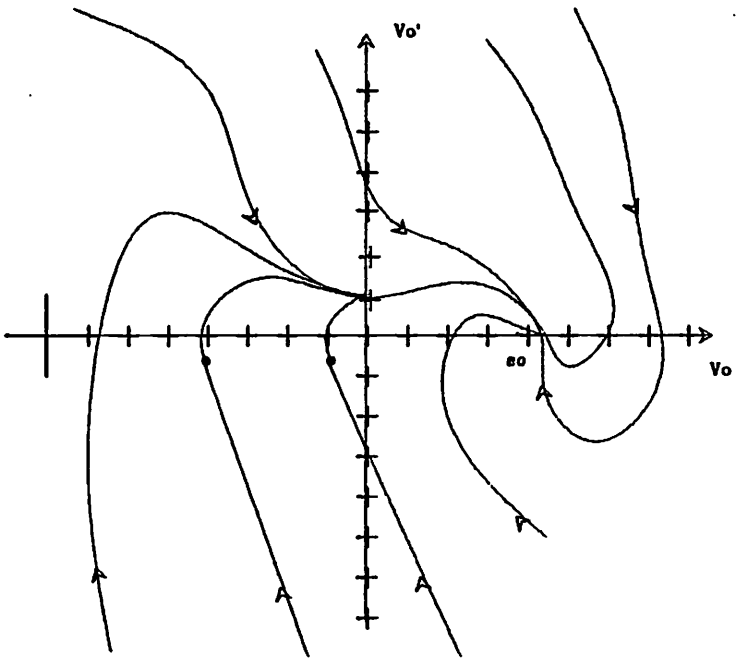


Fig3.17 Portraits for the Closed Loop

Response to Step Voltage Input

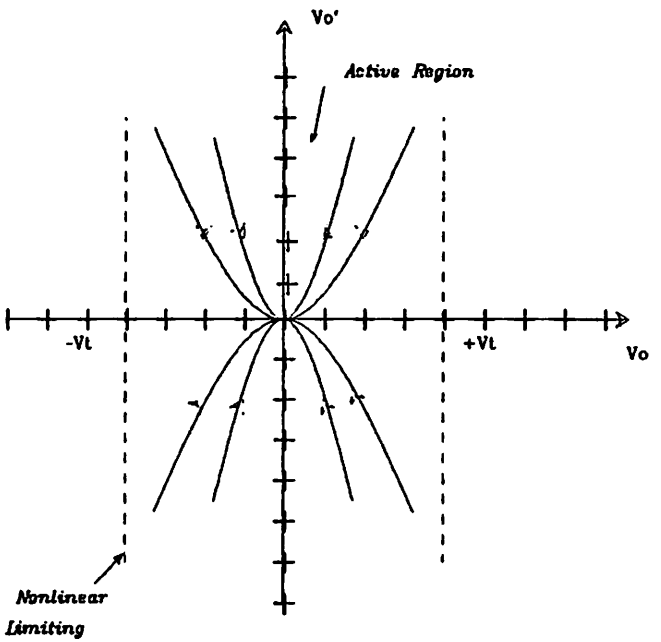


Fig3.18 Origin Locally Stable.

cuit showed to be asymptotically stable (about the origin) for a whole set of large signal initial conditions (DC unbalances) ; the outputs from transient SPICE simulation are shown in the Fig.3.19. The results are also presented in a state space plot in Fig.3.20a,b.

The plot shows two main results: First, the origin is stable in the presence of large signal perturbations and secondly , the system can be taken from the meta-stable state into the stable region. A *switching boundary* appears in the phase plane (or a switching surface in the state space) which separates the active clock phase and the hold clock phase. The system solution in the hold phase has slower time constants determined only by the leakage and parasitic capacitances and for any practical purposes the system is kept in equilibrium. A new switching in the phase plane to the transfer region comes with the clock phase and the system solution continues on a trajectory determined by the initial conditions held during the previous phase plus the current perturbation.

3.5. SC Resonator Large Signal Simulation

The stability of our negative loss circuit has been discussed. This circuit is used as a SC integrator in a high order sampled data filter. In particular it is connected in a negative feedback loop with a conventional lossy integrator circuit as illustrated in Fig.3.21. The resulting resonator small signal behavior showed a close to lossless realization as presented in Chap.2. For large signals the use of computer simulation is more essential.

The computer simulation of the resonator circuit in a S/D system is done using a S/D resonator as a representative system. The same large signal initial conditions and typical set of forcing functions used in the integrator simulation were experimented in the resonator simulation. The simula-

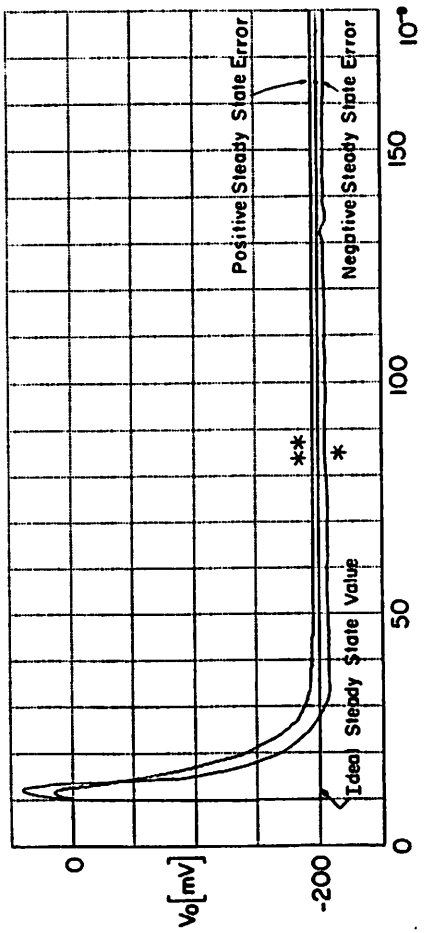


Fig.3.19 Closed Loop Step Response SPICE

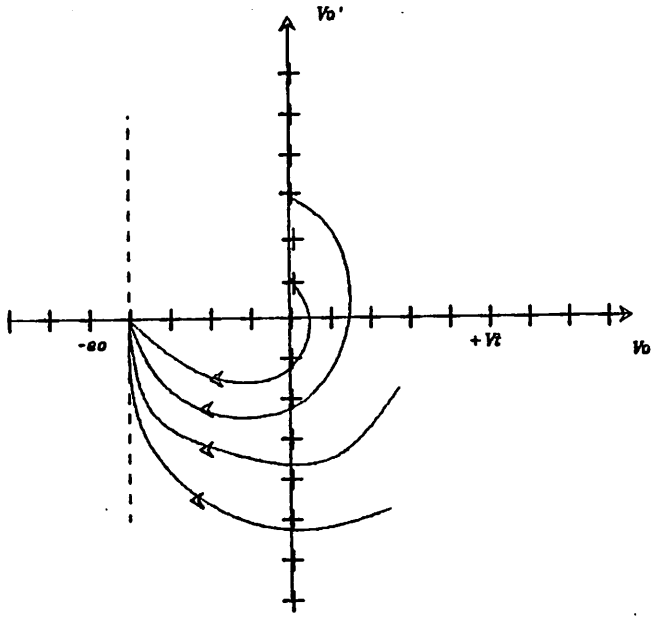
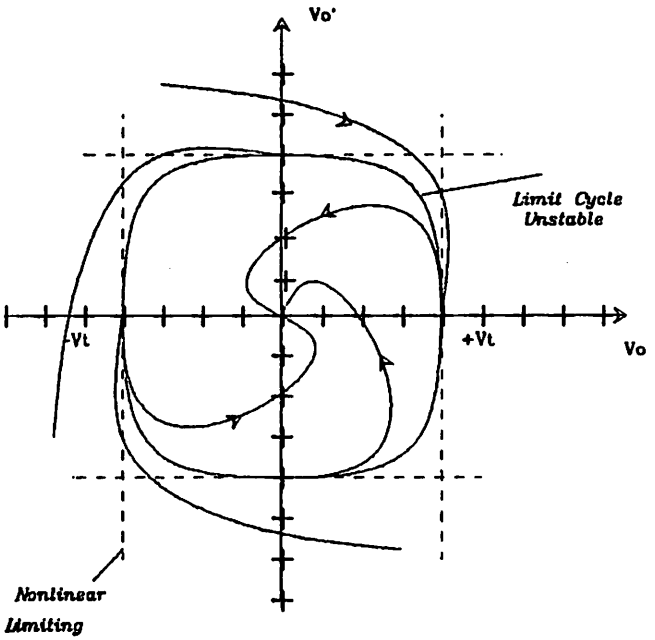


Fig.3.20a

Step Response within the Active Region



Origin Locally Stable.

Fig3.20b Phase Plane Portrait Constructed from Computer Simulation Results (SPICE)

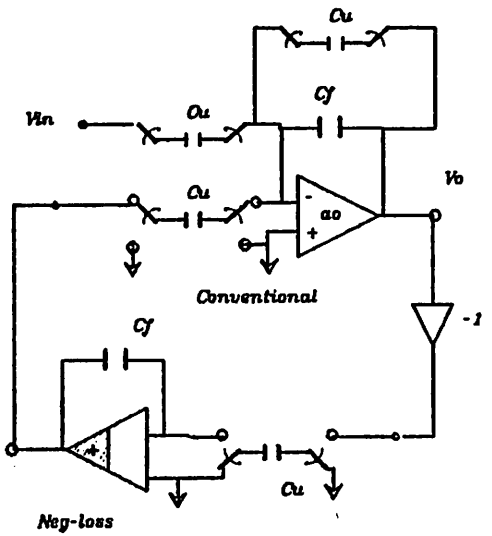


Fig3.21 Balanced Loss Canceled Resonator

tion was performed in the time domain including all the devices nonlinearities. The resonator has a close to lossless response shown by the stable oscillations response. The stability analysis is done by including a termination to the network. The results show a Q factor which closely agrees to the one obtained from the accurate termination elements, indicating the effectiveness of the lossless resonator realization. The results for the resonator are shown in Fig.3.22 where the asymptotical stability is observed.

The stability for the S/D resonator is illustrated in the phase plane by an spiral trajectory converging to the origin (Fig.3.23). In the resonator circuit the energy is easily represented in terms of the voltage signal at one integrator and its time derivative at the other integrator output. The output is compared with the lossless resonator unit-pulse response which has the circular trajectory (limit cycle). The lossy case draws an spiral towards the origin indicating energy dissipation .

The monolithic NMOS prototype filter fabricated demonstrated the stability and accuracy of the high order filter. The experimental results from the prototype sixth order filter are summarized in Chap.5.

3.6. The Negative-loss from a Circuit Design Point of View

A more intuitive explanation of how stability is built in the circuit follows. This approach is more familiar to circuit designers. The concepts utilized for this purpose are linear circuit relationships and negative resistance and conductance analysis.

The negative loss circuit is implemented in a single stage amplifier by using a negative load. The circuit has special properties because even though it is a simple non-inverting amplifier, it contains a phase lead of its dominant pole. The frequency response looks more like the typical common

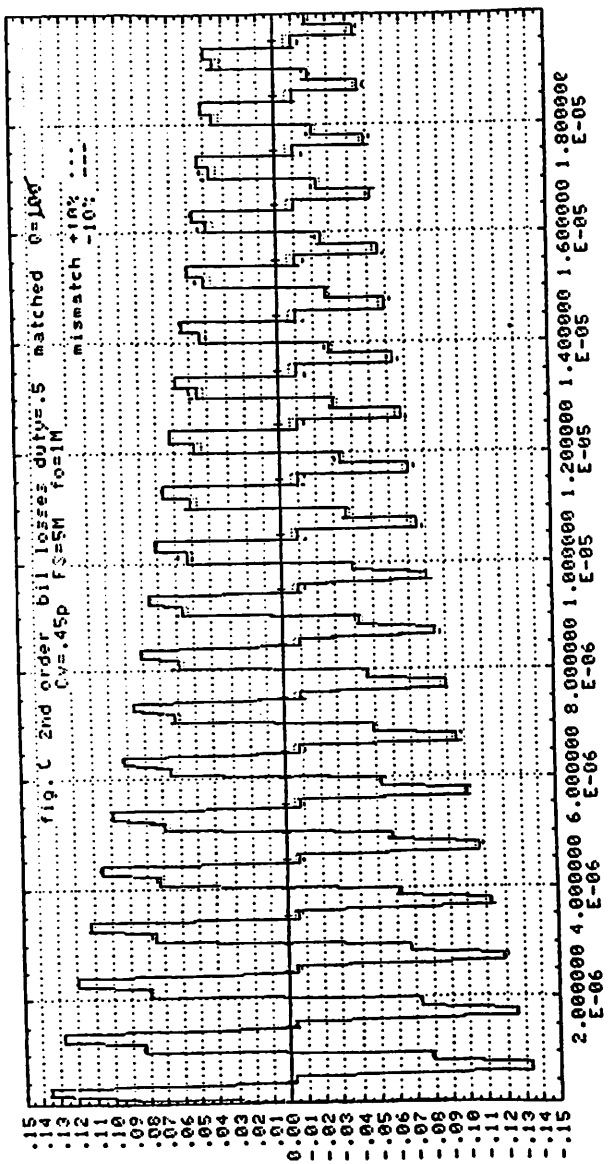


Fig.3.22 Resonator Impulse Response (SPICE)

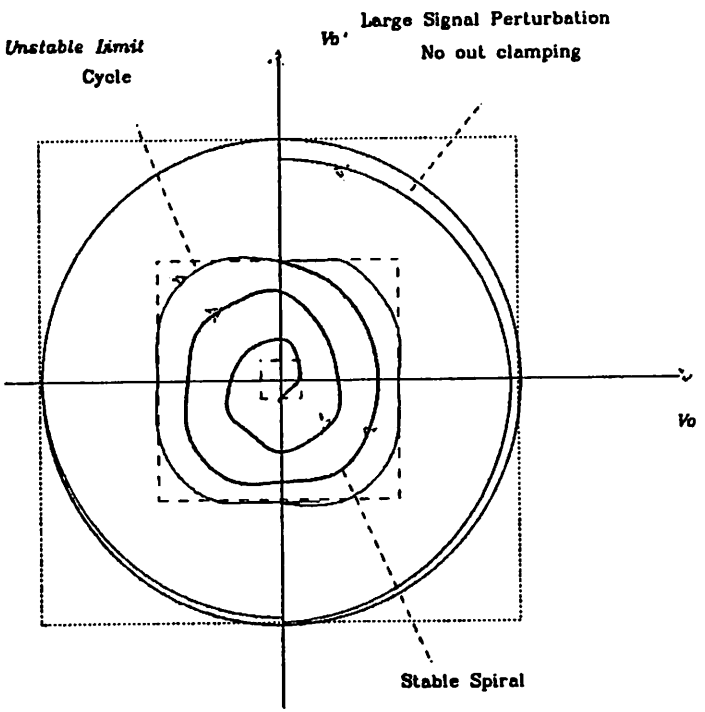


Fig.3.23

Phase Plane Portrait
of Resonator Circuit
Constructed from SPICE Results

source amplifier where instead of having a monotonic phase lag, a phase lead at low frequencies is produced and the high frequency transfer function look alike the conventional inverting circuit function. At DC the amplifier has experience a jump of 180 degrees in phase.

In the real circuit, a input transconductance stage is used to steer a current as a response to the input signal and due to the static negative load, it produces a negative voltage transition in terms of the conductance at DC at the drains of the differential pair Fig.3.24a,b. The voltage at the sources of the cross coupled circuit seen from these terminals has a current controlled static non-linearity.

The circuit eventually reaches the limits of the active region where one of the transistors goes into the low gain triode region and the effective value of negative resistance locally decreases, see Fig.3.25. If the signal is further increased the circuit reaches a region where the resistance collapses and abruptly changes to a typical positive resistance value. This is the same effect as the gain non-linearity presented in a different manner; in the present circuit this happens when one of the cross coupled transistors goes out of conduction (turns off).

The static characteristics themselves do not determine the stability of the circuit and only when the transient performance of the circuit is introduced can the stability be analyzed. For our closed loop circuit, we have an amplifier which for high frequencies reacts in the same form as the conventional amplifier. The transient analysis indicates that the leading (fast) transition of the positive input signal produces an error in voltage at the input which is rising $\frac{dV_e}{dt} > 0$, see Fig.3.26. The negative resistance does not respond to the leading edge and the output signal travels downwards

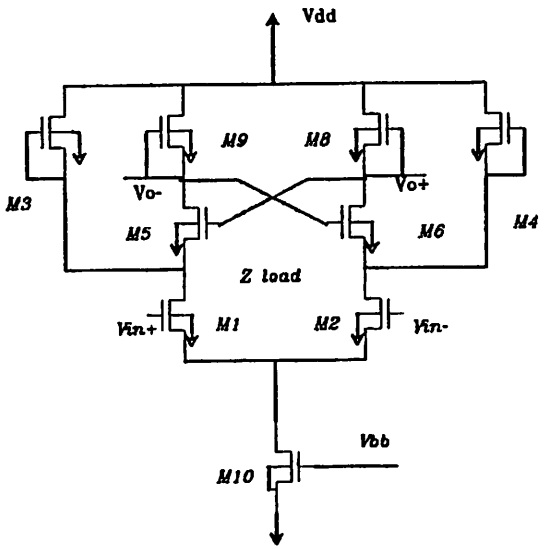


Fig3.24a Cascode Load and Cross Coupled Load NMOS Amplifiers

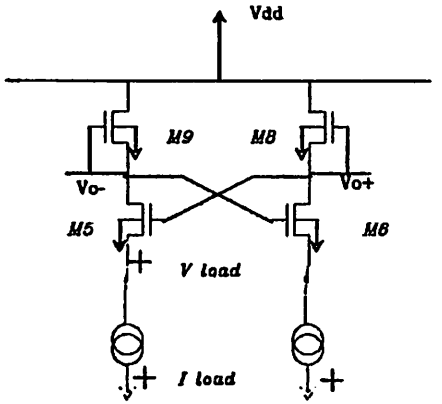


Fig.3.24b

Cascode Load and Cross Coupled Load NMOS Amplifiers

Fig.3.25 Hysteresis Static Nonlinearity

Fig.3.26 Detailed Step Response Shows
the Feedforward and Back-reaction Effects

$\frac{dV_o}{dt} < 0$. The negative output transition is coupled back through the feedback element opposite to the direction of the original input perturbance (back reaction). The feedback for fast signals is negative.

As the negative resistance responds, the feedback is produces the back reaction which can be observed in the response from computer simulation. The steady state DC gain has changed the polarity of the amplifier gain and the signal at the input has reached the steady state negative value. The process of the stable response is then a strong function of the frequency dependence of the amplifier and the negative load.

Outside the active region, depending on which type of non-linearity is present , the operation of the circuit can be returned to the negative resistor active region by either a voltage drive or a current drive in the proper circuit node, see Fig.3.27a for a set of typical $v-i$ transfer characteristics. The voltage feedback (shunt feedback) produces the effective voltage drive of the output or equivalently the current drive at the cross couple sources, providing the reliable large signal operation of the negative resistor. This is achieved by the current path provided by the shunt feedback which gives control through the cascode devices operating as voltage followers.

3.6.1. Negative-resistance as the Source of Negative-loss

The negative-loss circuit is obtained by the cross coupled circuit; some solid state devices can provide this characteristic , i.e., SCR, SCS, Tunnel diodes, UJT, Varactors, etc. [78] leading to faster loss cancellation circuits.

The negative-loss circuit realized by the cross coupled connection of inverter amplifiers has receive much attention (NIC and GIC circuits) [79], see Fig.3.27b. The circuit is approximated as a second order system due to

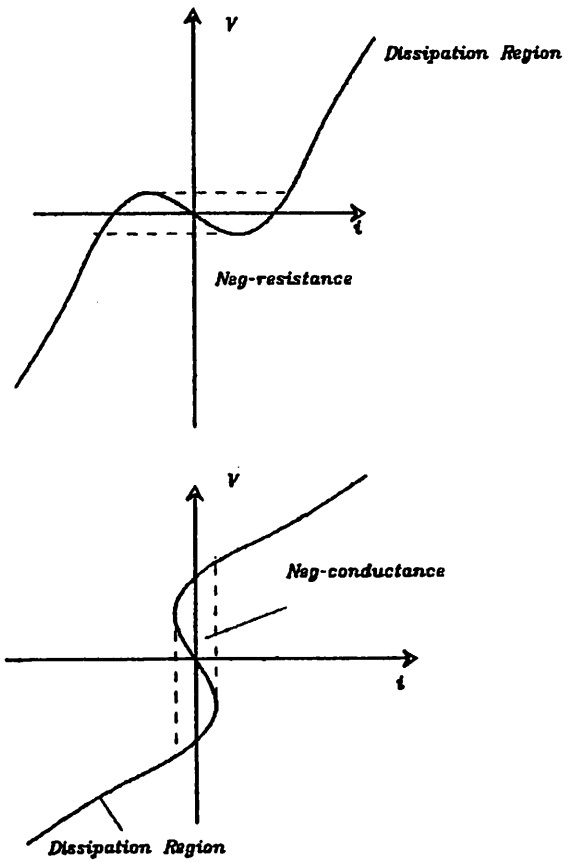
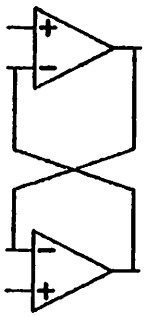


Fig3.27a Non-linear V-i Characteristics



a) Cross couple NIC Realization

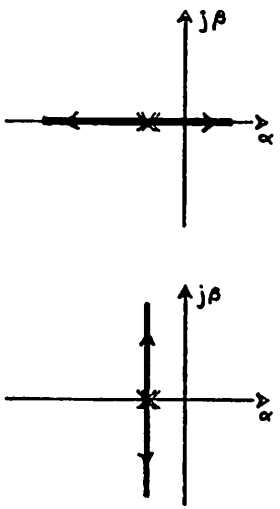


Fig3.27b Root Locus for Different Polarities of Feedback

the singularities of each device. Within the linear region , the transfer function has a pair of poles lying along the real axis at mirror locations about the origin, i.e., one RHP and one LHP pole. In terms of the open loop poles and the root locus, the different feedback configurations are depicted in Fig.3.27b. These circuits were of limited interest for linear circuit designers due to the restrictions with respect to circuit speed and stability [77]. This was so, because the implementation of PF was external to multi-stage active elements containing complex root distribution which very often lead to unstability problems.

3.7. Other Stability Considerations

3.7.1. DC versus AC Stability

The stability of this circuit is performed by capacitive feedback. At steady state the current is null and the circuit operating point is maintained in form of a charge (3.4.5). It is fundamental to review the operation of a capacitor in response to charge signals. This has been called the charge domain where signal is passed by transient of charge. The voltage signal time derivative is transferred by the capacitors. It is this charge signal which eventually looks like a DC steady state signal at the end of the transient. Capacitors do not block the (step) signal but pass it as charge. The final steady state response is a DC voltage.

3.7.2. Common-mode Stability

In practical active circuit design two different issues related to stability are encountered. One is the operation of the circuit when it is in the ideal common-mode operating point (the circuit has the required bias conditions)

and the second is the stability of the circuit for operation around the bias values . The response of the circuit is guaranteed as long as the circuit is in the particular active region. Both stability issues belong to the same unique more general large signal stability of the system which requires a large signal analysis.

DC perturbations, like offsets due to circuit mismatches, are the forcing functions for the system equations. The large signal equilibrium points for the system define the bias conditions. The solutions around the equilibrium points are dependent on the original system determined by the forcing function U. In the circuit of Fig.3.24, constant bias of the differential pair was presented. For this ideal system the bias stability is assumed. In the real circuit, the bias of the stage and thus the output nominal voltage is defined in open loop and hence it is not controlled.A large signal feedback circuit is used to regulate the bias points. The full circuit, with the common-mode bias circuit for the amplifier was included in the simulations.

True DC effects can come from circuit offsets. In the resonator circuit the offset signal travels along the circuit and affects the DC output signal.

3.8. Summary

This chapter has presented the conditionally unstable circuit functions which are stabilized by a feedback compensation circuit and applied to SC filters. The special properties of these circuits in time and frequency domains are presented and stability is discussed. The computer simulation is shown to be the vital tool in the analysis of the system. Even using simple models for the analysis, the analytical complexity of the final system is great. SPICE computer simulation was used to obtain the solutions for the system through a perturbation analysis.

CHAPTER 4

NMOS AMPLIFIER CIRCUIT DESCRIPTION

The amplifier circuits used in the negative loss and conventional integrator circuits are fully differential. This approach has several advantages: it increases the dynamic range and minimizes the common-mode errors such as power-supply coupling and clock feed-through. The circuit architecture and bias conditions are almost identical for both circuits. The fundamental difference in these circuits is the gain at DC and the fact that the dominant poles have opposite polarity. All the other circuit singularities are the same and thus the analysis done for one of the circuits applies accurately to the other by a simple change of sign to the calculations involved. In this chapter, the cascode circuit is analyzed in detail and then the results for the Negative-loss circuit are presented.

4.1. NMOS AMP DESIGN

4.1.1. The Single Stage Amplifier

The fast settling amplifier employs a single stage configuration as illustrated in Fig.4.1a in order to optimize the transient response. This is so due to the reduction of high-order poles resulting in a simple frequency compensation. The NMOS inverting amplifier DC gain a_o is limited by body effect (finite conductance g_{sb}) and channel length modulation (finite output conductance g_o) of the load transistors; for the input device transconductance g_{m1} we have:

$$a_o = -\frac{g_{m1}}{g_L} = -\frac{g_{m1}}{g_{sb} + go} \tag{4.1a}$$

$$a_o = -\frac{g_{m1}}{g_{m2}\,\eta + go} \tag{4.1b}$$

where g_m is the driver device transconductance and η is the body effect factor for the load device given by:

$$\frac{1}{\eta} = 2C_{ox}\sqrt{\frac{2\varphi + V_{bs}}{2q_e\varepsilon N_A}} \tag{4.2a}$$

$$\frac{1}{g_o} \propto \frac{1}{\lambda I} \tag{4.2b}$$

For the particular process used the body effect output resistance is comparable in value to the channel-length modulation resistance r_o. The gain vs. doping N_a is shown in Fig.4.1b which also shows the effect of channel length modulation. The output resistance starts to become dominant for low values of substrate doping.

4.1.2. Amplifier Circuit Speed

The single stage amplifier open loop (small signal) transfer function $a(s)$ was presented in Chap.2 ; it contains a pair of poles $\omega 1$ and $\omega 2$ and a feedforward zero ζ_1 :

$$a(s) = \frac{-a_o\left(\frac{s}{\zeta_1} - 1\right)}{\left(\frac{s}{\omega_1} + 1\right)\left(\frac{s}{\omega_2} + 1\right)} \tag{4.3}$$

The small signal model for the simple differential amplifier is shown in Fig.4.2a. The large signal transfer is not included here for brevity, and it can be found elsewhere [71]. The amplifier's settling characteristic is determined by the singularities in (4.1), see Fig.4.2b. The circuit's input time constant ω_2 is very small and even though there is Miller effect involved this time constant is not dominant:

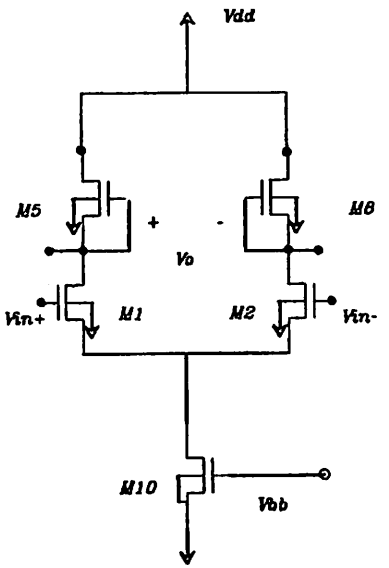


Fig4.1a Linear Differential Single Stage Amp

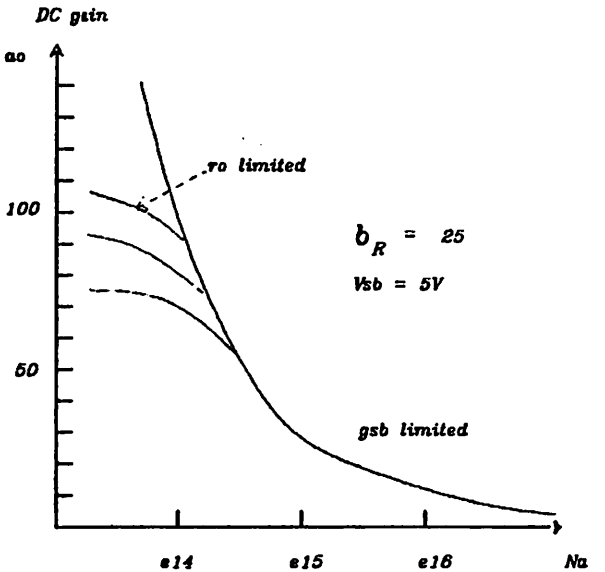
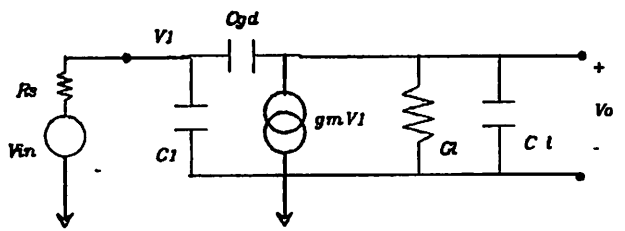
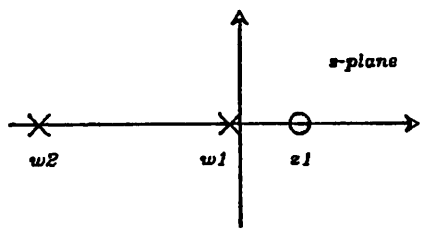


Fig4.1b Single Stage Amplifier DC Gain vs. Substrate Doping



a) Small Signal Model for the Single Stage Inverting Amp.



b) Root Loci for the Inverting Amp.

Fig.4.2

$$\omega_2 = \frac{1}{R_o C_{gs}} + \frac{1}{a_v C_{gd} R_o} \tag{4.4a}$$

The dominant time constant, determined by the load capacitance C_l and resistance R_l, is :

$$\omega_1 \approx \frac{1}{R_l C_l} \tag{4.4b}$$

The feedforward zero (non-minimum phase) determined by the gate to drain capacitance is :

$$\zeta_1 = \frac{g_{m1}}{C_{gd}} \tag{4.4c}$$

The unity gain frequency ω_u is determined by the transconductance of the input transistor M_1, $M2$ and the total capacitance at the output node 3/4:

$$\omega_u = \frac{g_{m1}}{C_l} \tag{4.5}$$

4.2. Cascode Load Differential Amplifier

The simple inverting amplifier gives little room to design for DC gain and speed specifications. The cascode load stage with an extra current bleeder shown in Fig.4.3 provides an improvement in terms of design flexibility. The current level can be independently assigned for the input stage and the cascode load, offering one more degree of freedom. M_1 and M_2 are the differential input transconductance pair with M_{d3} and M_{d4} as current bleeders to increase the current level of the input transistors while preserving the current in the cascode load and, as a consequence, the high speed of the stage. M_4 and M_6 are the cascoded load devices which provide the voltage gain stage with M_7 and M_8 as load devices. The driver device transconductance is proportional to the cascode and the bleeder current as given by :

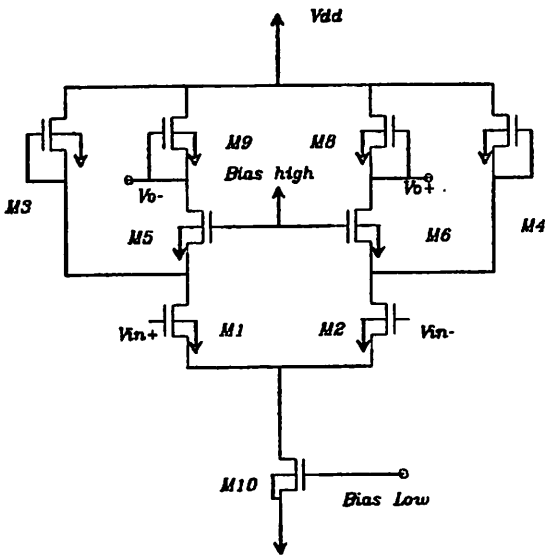


Fig.4.3

Cascode Load Single Stage Amplifier

$$g_m = \sqrt{2\beta(I_t + I_b)} \tag{4.6a}$$

where:

$$\beta = \mu C_{ox} \frac{W}{L} \tag{4.6b}$$

I_b is the bleeder device current and I_t is the cascode load bias current level. The output resistance r_o looking back towards the driver is also increased by the cascode load:

$$\frac{1}{go_t} = \frac{1}{\frac{\lambda_1\lambda_2 I_d (Vgs - Vt)}{2} + g_{mb}} \tag{4.7}$$

where go_t is the total output conductance.

The gain improvement in the NMOS cascode load comes mainly from the modification in the transconductance of the input devices. For the cascode load, in the body effect limited case, the gain is given by:

$$\frac{V_o}{V_i} = \frac{2}{\gamma}\sqrt{\frac{\beta_R(I_1 + I_b)}{\lambda_i}(Vsb + 2\varphi)} \tag{4.8}$$

β_R is the $\frac{W}{L}$-ratio of the driver to load devices.

4.2.1. Differential Cascode Load Small Signal Analysis

A small signal analysis is performed to calculate the DC gain. The circuit model is shown in Fig.4.4. The analysis utilizes the transistor names shown in the schematics. *Signal Flow Graph* (SFG) techniques were used because they offer a physical insight in the role of each transistor element in the amplifier. This is specially helpful in understanding the different ways the DC gain polarity can be reversed to obtain the negative loss amplifier. The cascode load small signal analysis has the SFG representation shown in Fig.4.5. Using Mason's rule

:

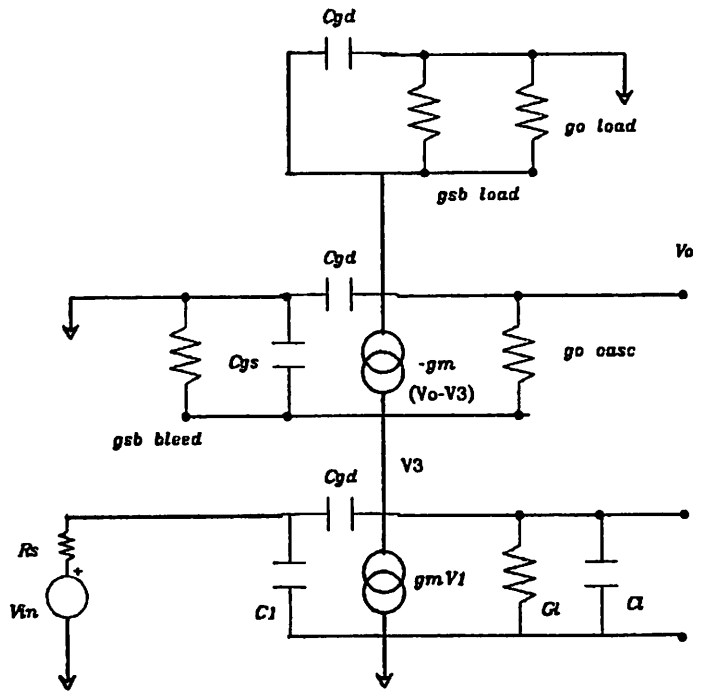


Fig.4.4 *Small Signal Model for the Cascode Amp*

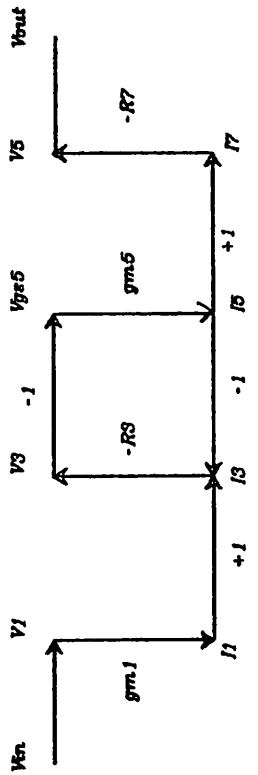


Fig.4.5 SFG for the Cascode Load Amplifier

(4.9)

$$a_{0i} = \frac{-g_{m1}R_7(g_{m5} + g_{b5} + G_5)R_3}{1 + (G_1 + g_{b6})R_2 + g_{m5}R_3 + G_6(R_3 + R_7) + b_{b7}R_7 - (-g_{b7} - G_5)G_1R_3R_7}$$

where g_{m_i} and G_i are respectively the transconductance and output conductance of the i device, g_{bi} is the body effect conductance and R_i is the node total output resistance which contains all the resistive effects of a particular node, e.g., body effect, channel length modulation effect, etc.

4.2.2. Cascode Load Circuit Speed Considerations

The characteristics of the amplifier as a function of the bleeder current are of interest; let us assume that the bleeder and bias current sources are increased simultaneously and thus the cascode current is maintained constant. With this, the output load is kept constant and all we are modifying is the driver transconductance. The DC gain and the unity gain bandwidth are proportional to the square root of the bleeder current (4.4). The first pole given by the output and the cascode pole are independent of the bleeder current.

From the SFG of the circuit used for the DC gain calculations the transfer function for the open loop can be obtained:

$$a(s) = \frac{V_o}{V_i} = -\frac{g_{m1}g_{m5}}{Y_3Y_6 + g_{m5}Y_5} \tag{4.10a}$$

where Y_i is the total admittance of node i:

$$Y_i = g_i + sC_i \tag{4.10b}$$

The input pole ω_3 is located at very high frequencies since Miller effect is negligible for this case (4.8). The dominant pole ω_1 is determined by the output node as in the simple inverter case (4.3b). The cascode devices with their C_{gs} capacitance provide a second pole ω_2 given by :

$$\omega_2 = \frac{g_{m2}}{C_{gs2}} \tag{4.11}$$

The frequency characteristics in open loop as a function of I_b are illustrated in Fig.4.6.

4.3. Prototype Amplifier Circuit Design

The amplifier speed requirements for the prototype narrowband filter are given in Table 4.1. The circuit is shown in Fig.4.7. The current level was dictated by the speed requirements and power dissipation. The total power per amplifier was $4mW$ ($200\mu A$ in each driver device). The driver size used is $\frac{W}{L} = \frac{120\mu}{8\mu}$ giving a transconductance of the order of $400\mu mho$. The current level for the cascode load circuit was $100\mu A$ for a transconductance of $100\mu mho$. The cascode devices have $\frac{W}{L} = \frac{80\mu}{8\mu}$ and current bleeders have an aspect ratio of : $\frac{W}{L} = \frac{20\mu}{20\mu}$. The depletion load device $\frac{W}{L} = \frac{20\mu}{20\mu}$ has, for this current level, transconductances of the order of $5\mu mho$ and body effect and channel length modulation resulting in an effective conductance of $4-10\mu mho$. The NMOS device circuit parameters of interest are shown in Table 4.2. For the simple differential pair the gain is 30–40 and for the cascoded output it is in the order of 80–90 at the nominal current levels; the closed loop steady state error is of the order of 1% which is larger than the effect of the finite settling for the frequencies of interest.

The sampling capacitance C_u value must be considerably larger than the circuit parasitics. In order to deal with sampling frequencies of the order of 1 to $6MHz$ the amplifier unity gain bandwidth must be larger than the clock frequency by at least a factor of five [4]. The cascode load amplifier has a bandwidth of $60MHz$ for the nominal current of $400\mu A$ (SPICE), see Fig.4.8. The step response initial delay is strongly influenced by the high order amplifier

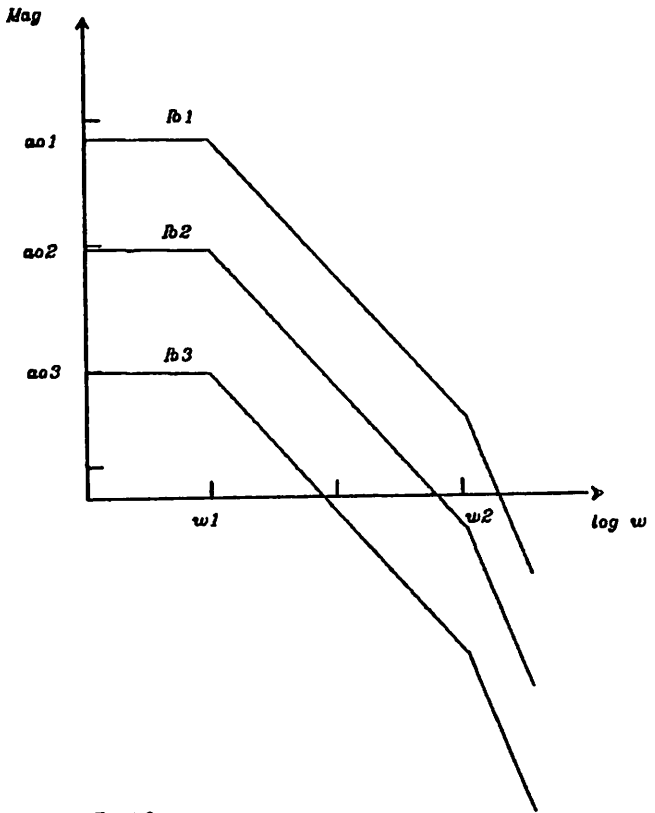


Fig.4.6.
Open Loop Freq. Response
with lb as a Parameter

TABLE 4.1

TYPICAL IF BANDPASS FILTER SPECS	
Center Frequency	256kHz
Center Frequency Acc.	+−1%
Maximum Passband Ripple	±1.5dB
Passband Gain	20dB
Passband Bandwidth	10KHz
Passband Bandwidth Acc.	±5%
Stopband Bandwidth	18KHz
Stopband Rejection	−36dB
Dynamic Range	60−80dB

OP-AMP REQUIRED PERFORMANCE	
DC gain	500
Bandwidth	> 50MHz
Settling Time 0.5%	< 100nsec

TABLE 4.2

	name	parameter	units	ENH	DEPL
1	LEVEL	model index	-	2	
2	VTO	zero-bias threshold voltage	V	0.7	2.7
3	KP	transconductance parameter	A/V**2	2.0E-5	3.1E-5
4	GAMMA	bulk threshold parameter	V**0.5	0.37	0.37
5	PHI	surface potential	V	0.65	0.65
6	LAMBDA	channel-length modulation (MOS1 and MOS2 only)	1/V	0.0	0.02
7	RD	drain ohmic resistance	Ohm	10.0	10.0
8	RS	source ohmic resistance	Ohm	5.0	5.0
9	CBD	zero-bias B-D junction capacitance	F	20FF	20FF
10	CBS	zero-bias B-S junction capacitance	F	20FF	20FF
11	IS	bulk junction saturation current	A	1.0E-15	1.0E-15
12	PB	bulk junction potential	V	0.87	0.87
13	CGSO	gate-source overlap capacitance per meter channel width	F/m	4.0E-11	4.0E-11
14	CGDO	gate-drain overlap capacitance per meter channel width	F/m	4.0E-11	4.0E-11
15	CGBO	gate-bulk overlap capacitance per meter channel length	F/m	2.0E-10	2.0E-10
16	RSH	drain and source diffusion sheet resistance	Ohm/sq.	40.0	40.0
17	CJ	zero-bias bulk junction bottom cap. per sq-meter of junction area	F/m**2	2.0E-4	2.0E-4
18	MJ	bulk junction bottom grading coef.	-	0.5	0.5
19	CJSW	zero-bias bulk junction sidewall cap. per meter of junction perimeter	F/m	1.0E-9	1.0E-9
20	MJSW	bulk junction sidewall grading coef.	-	0.33	
21	JS	bulk junction saturation current per sq-meter of junction area	A/m**2		1.0E-9
22	TOX	oxide thickness	meter	0.7E-7	0.7E-7
23	NSUB	substrate doping	1/cm**3	7.72E14	7.76E14
24	NSS	surface state density	1/cm**2	-2.50E11	8.50E11
25	NFS	fast surface state density	1/cm**2	1E11	1.0E11
26	XJ	metallurgical junction depth	meter	3.5E-07	3.5E-07
27	LD	lateral diffusion	meter	1.05E-7	1.05E-7
28	UO	surface mobility	cm**2/V-s	784.9	716.9
29	UCRIT	critical field for mobility degradation (MOS2 only)	V/cm	2.54E4	1.53E5
30	UEXP	critical field exponent in mobility degradation (MOS2 only)	-	0.008	0.0
31	UTRA	transverse field coef (mobility) (MOS2 only)	-	0.25	0.25
32	VMAX	maximum drift velocity of carriers	m/s	5.0E4	5.0E4
33	NEFF	total channel charge (fixed and mobile) coefficient (MOS2 only)	-	1.0	5.0
34	KF	flicker noise coefficient	-	1.0E-26	1.0E-26
35	AF	flicker noise exponent	-	1.2	1.2
36	FC	coefficient for forward-bias depletion capacitance formula	-	0.5	

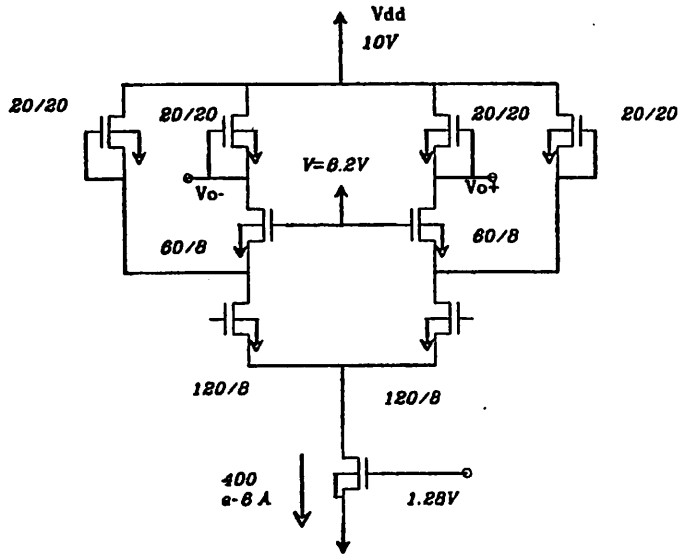


Fig.4.7.
Cascode Load Single Stage Amplifier with Device Aspect Ratios

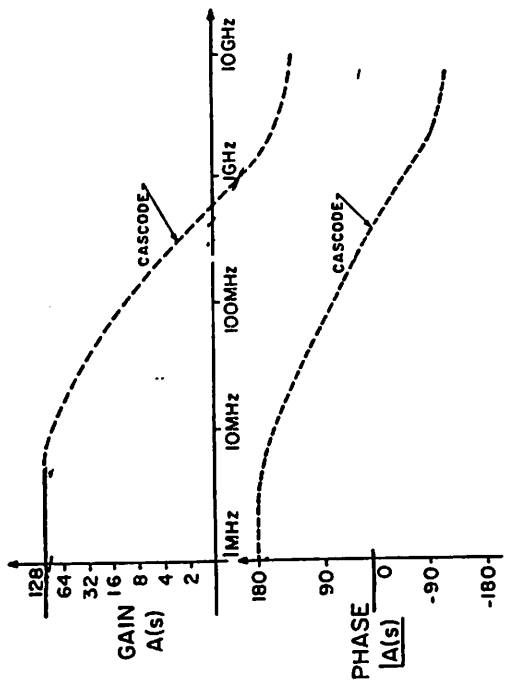


Fig.4.8 SPICE Frequency Response
Cascode Load Amplifier

poles and the rise time, 12–20 *ns*, is determined by the unity gain bandwidth. the settling time is determined by the transfer function singularities. The settling is ultimately dependent on the type of singularities in the circuit, i.e., oscillatory or low damping poles can produce long settling times. For the dominant pole situation, the analysis for " close " to settled conditions is dependent on the dominant time constant.

Besides the static and transient characteristics, other requirements related to common mode bias and rms amplifier noise and distortion have to be considered to obtain a reasonable compromise in amplifier gain-speed performance.

4.4. The Negative-loss NMOS Circuit

4.4.1. Implementation Alternatives

Two possible non-Hurwitz circuits are shown in Fig.4.9. The single stage differential pair employs local (internal) positive feedback. For this simple circuit PF can be applied in two forms: by using cross coupled pair at the amplifier load or by using source regeneration at the sources of the differential pair (as opposed to source degeneration used in negative feedback configurations to improve linearity and speed).

The negative resistance load is determined by the conductance of the crossed devices and the actual resistance at the output node :

$$r^{(-)} = -2\frac{R_L}{1+\frac{1}{g_{m_{cross}}R_L}} \qquad (4.12a)$$

The effective source conductance for the latter is determined by the transconductance of the crossed devices :

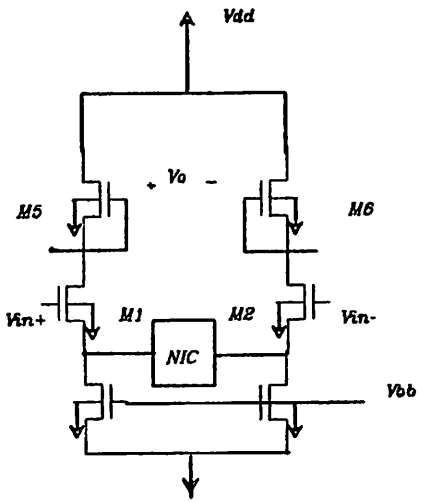


Fig4.9a Single Stage Amplifier with Local Positive Feedback

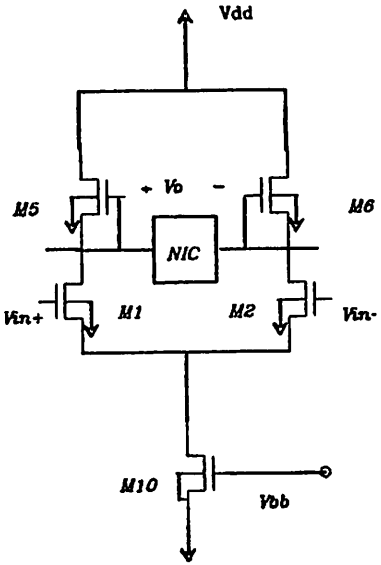


Fig4.9b Single Stage Amplifier with Local Positive Feedback

$$g^{(-)} = -2g_{m_{cross}} \qquad (4.12b)$$

These configurations have in common the cross coupled connection which implements the phase reversal at DC.

Small signal analysis and computer simulation were used for the selection of the final pair of circuits based on considerations of DC gain matching and circuit symmetry. The cross coupled load circuit shown in Fig.4.10a has the simplest configuration and provides the best partner circuit for the conventional cascode load amplifier on Fig.4.3.

The negative loss circuit step response in closed loop is shown together with the conventional circuit response in Fig.4.10b.

4.4.2. Small Signal Analysis of the Cross Coupled Load Circuit

Small signal analysis at DC is obtained from the SFG by the Masons's rule (Fig.4.11):

$$a_{0i} = \frac{-g_{m1}R_7(g_{m4} + g_{b5} + G_5)R_3}{1 + (G_1 + g_{b5})R_3 + g_{m5}(R_3 - R_7) + G_5(R_3 + R7) + g_{b7}R_7 - (g_{m5} - g_7 - G_5)G_1R_3R_7} \qquad (4.13)$$

The proposed cross coupled load amplifier is different from the simple cascode in bias points.The cascode needs some extra devices to bias the gates of $M_{4,6}$ as illustrated in Fig.4.3. By analysis of the circuit SFG a new circuit configuration to substitute for the cascode can be obtained which has exactly the same bias as the positive feedback circuit and requires no extra bias devices. The circuit is shown in Fig.4.12. The small signal gain is :

$$a_{0i} = \frac{-g_{m1}R_7(g_{m4} + g_{b5} + G_5)R_3}{1 + (G_1 + g_{b5})R_3 + g_{m5}R_3 + G_5(R_3 + R_7) + g_{b7}R_7 - (-g_{b7})G_1R_3R_7} \qquad (4.14)$$

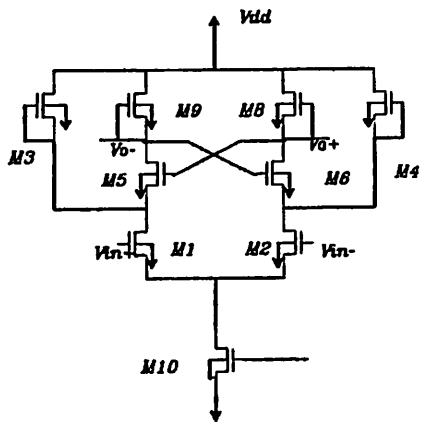


Fig4.10a
Cascode Load and Cross Coupled Load NMOS Amplifiers

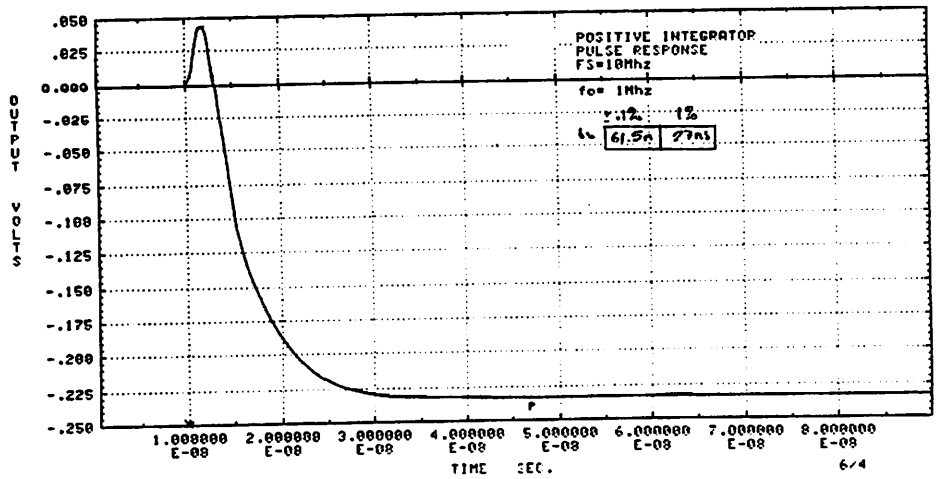


Fig4.10b Neg-loss Integrator Response within the Resonator Circuit

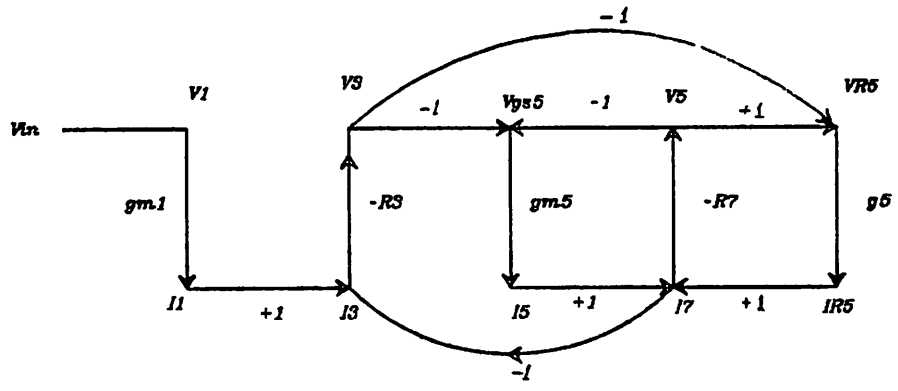


Fig.4.11 SFG for Cross Coupled Amp, Open Loop

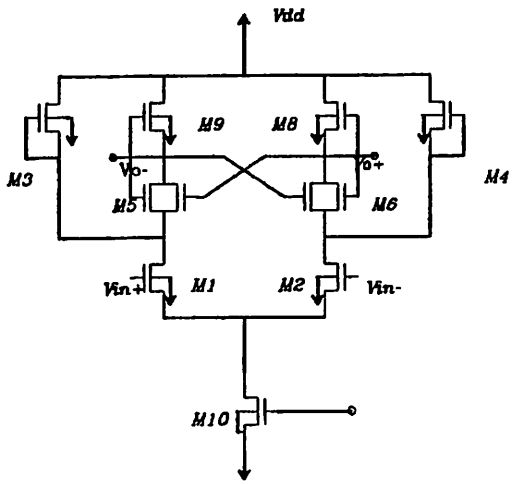


Fig4.12 Pos Loss Amp with Self Bias Cascode

4.4.3. Negative loss Circuit Speed Considerations

The SFG for the system is shown in Fig.4.13. It shows a brand new feedback branch which affects the transfer function in the denominator (4.12):

$$\frac{V_o}{V_i} = -\frac{g_{m1}g_{m3}}{Y_3Y_5 + g_{m3}(Y_5 - Y_3)} \tag{4.15}$$

The addition of this new loop changes the sign of the linear term in the characteristic equation leading to the dominant pole change of polarity. The particular analysis is straightforward as for the conventional amplifier case. The results give a dominant pole defined by the output as follows:

$$\frac{1}{\omega_1} \approx \frac{C_5g_3 + C_3g_5 + (C_5 - C_3)g_{m3}}{g_{m3}(g_5 - g_3)} \tag{4.16b}$$

$$\omega_2 \approx \frac{1}{\tau_5} + \frac{1}{\tau_3} + \left(\frac{1}{C_3} - \frac{1}{C_5}\right)g_{m3} \tag{4.16c}$$

where τ_i is the time constant of the node i.

SPICE simulation results are presented later in this chapter showing the close agreement of root locations for the positive and negative loss amplifiers.[1] For the positive feedback amplifiers the typical root locus as a function of C_f is shown in Fig.4.14a. The frequency domain transfer function for the negative loss amplifier is shown in Fig.4.14b.

4.5. Closed Loop Circuit Analysis

The analysis of the cascode inverting amplifier when connected with capacitive feedback follows. The small signal model is shown in Fig.4.15a. The SFG is shown in Fig.4.15b. The driving signal for the circuit in the SC integrator is equivalent to a voltage signal V_{in}.

SFG for the closed loop includes two new branches and result in the the following transfer function:

1.- Refer back to Chap.2 for the closed loop analysis of this circuit.

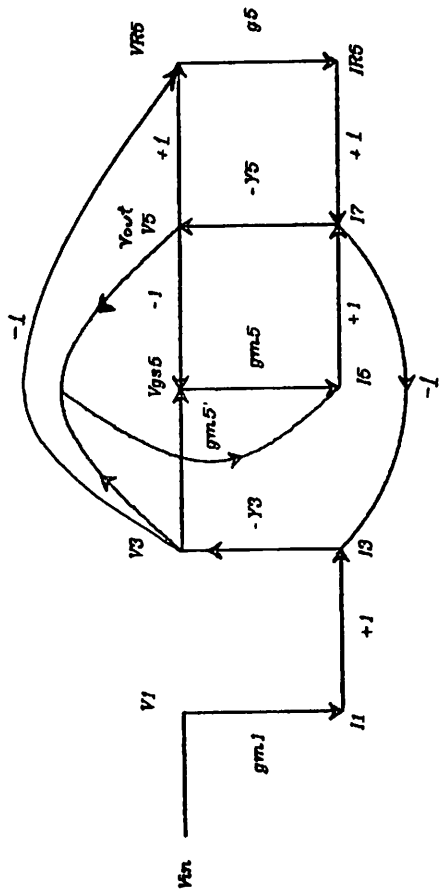


Fig4.13 SFG for pos-loss alternative circuit

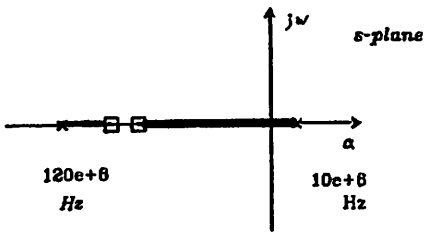


Fig4.14a Root Locl for the Inverting Amp.

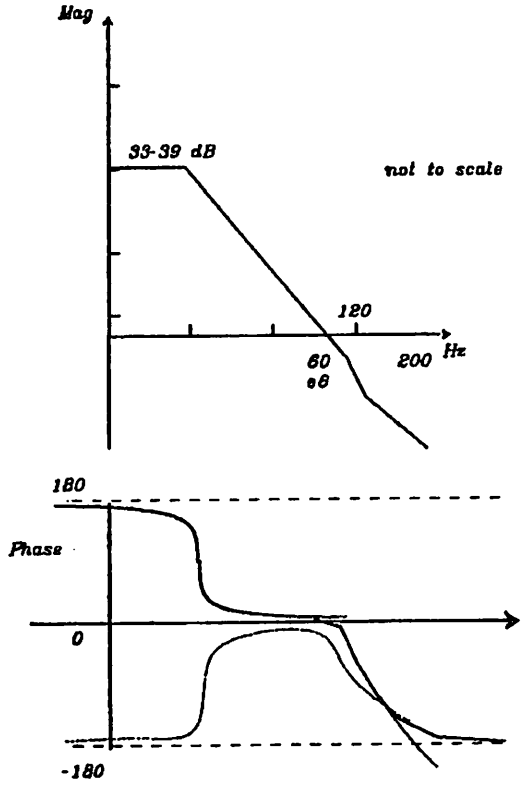


Fig4.14b
Freq. Response for Open Loop
Pos and Neg-loss Amps

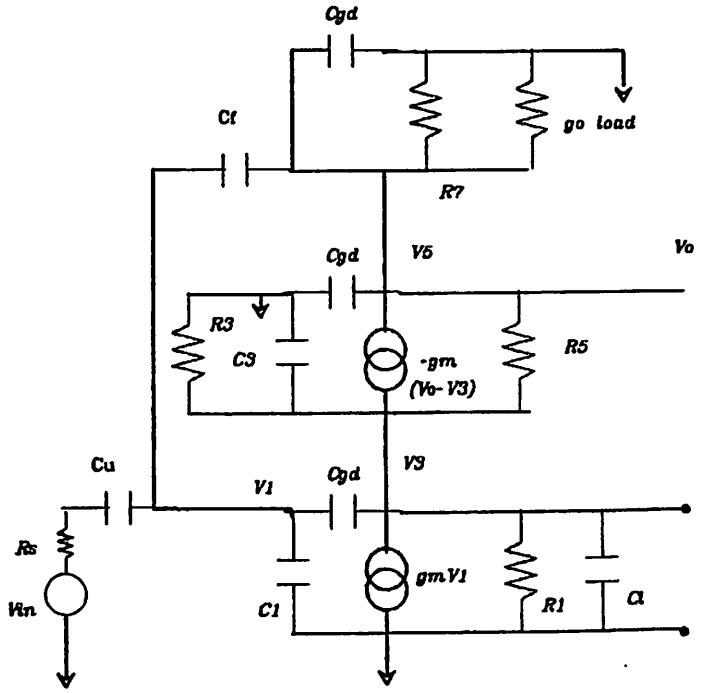


Fig4.15a Closed Loop Amplifier
Small Signal Model

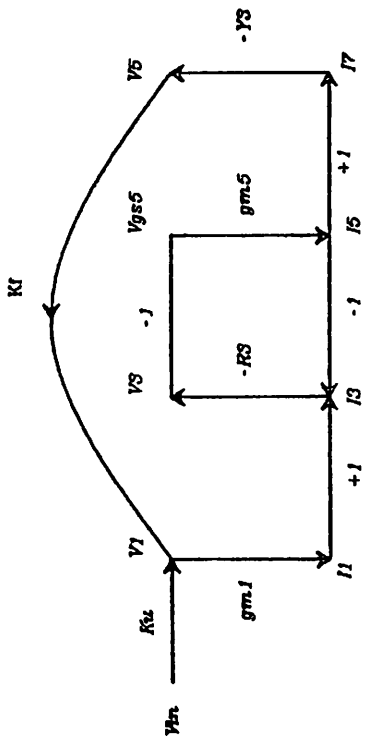


Fig.4.15b SFG For Closed Loop Amplifier

$$\frac{V_{o(s)}}{V_{i(s)}} = \frac{s^2 C_f C_3 + s C_f g_5 - g_{m1} g_{m5} \alpha}{s^2 C_3 C_5 + s(C_3 g_5 + C_5 g_5) + g_{m1} g_{m5} \beta + g_5 g_5} \tag{4.17a}$$

The block diagram for the open loop and closed loop circuit is shown in Fig.15c. The feedback moves the dominant pole towards higher frequencies in a similar way to the well known resistive feedback. Two differences are of importance: the initial conditions in the capacitors and the current that flows in the steady state for the resistor feedback case; in the capacitor feedback circuit a constant charge is kept in the capacitors at steady state. The signal flow along the circuit for both cases is characterized by similar equations as was presented in Chap.3. The closed loop transfer function $H(s)$ for the amplifier within one clock phase is given by :

$$H(s) = \frac{\dfrac{-H_o(\frac{s}{m_i}-1)(\frac{s}{m_j}+1)}{(\frac{s}{w_i}+1)(\frac{s}{w_j}+1)}}{1+\dfrac{T_o(\frac{s}{m_j}+1)(\frac{s}{m_i}-1)}{(\frac{s}{w_i}+1)(\frac{s}{w_j}+1)}} \tag{4.17b}$$

The root locus for this circuit as a function of the capacitance ratio $\frac{C_f}{C_u + C_s}$ is shown in Fig.4.15d where the widebanding effect on the amplifier is depicted by the dominant pole moving towards the LHP zero at high frequencies. The second pole travels to the left and its phase delay is reduced. H_o and T_o are the forward and loop DC gains respectively. The circuit analysis is straightforward and results in:

$$m_j = \frac{g_{m1} g_{mload}}{C_f g_{m2}} \tag{4.18a}$$

$$m_i = -\frac{g_{m2}}{C_{gs2}} \tag{4.18b}$$

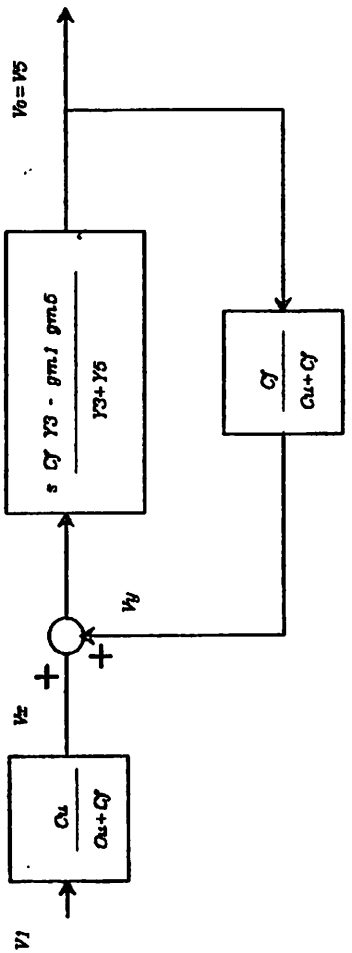


Fig4.15c Block Diagram for the Closed Loop Amplifier

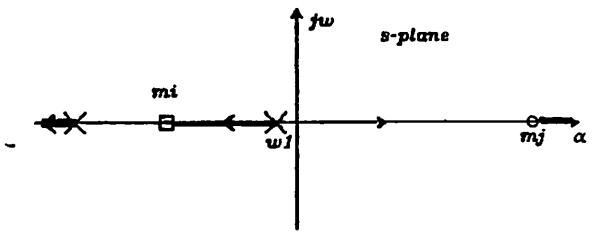


Fig4.15d Root Loci for the Inverting Amp. as Function of Feedback Capacitor

$$\omega_i = \frac{-a_0 g_{m2}}{C_{load}} - \frac{g_{m1}}{C_f} \qquad (4.18c)$$

$$\omega_j = -\frac{g_{m2}}{C_{gs2}} + \frac{g_i}{C_i} \qquad (4.18d)$$

The cascode configuration has very fast response due to the LHP zero that compensates for the second pole delay [55]. A conclusion drawn from the previous argument is that the analysis of the amplifier performance for close to steady state condition can be performed without lack of generality by looking at the first pole movement in the root locus.

These results were in close agreement with SPICE simulation. The cascode load amplifier is used in the prototype circuit; SPICE shows that this amplifier is fast enough to meet the speed requirements of the application in high-frequency SC filters, i.e., 0.5% settling in less than 50ns. The response is shown in Fig.4.18a. The frequency-domain analysis shows the pole-zero LHP pair produced by the cascoding as discussed above. Negative-loss SFG for the closed loop condition is shown in Fig.4.18b.

4.6. Other Aspects of Circuit Design

4.6.1. Circuit Noise

Noise is an important consideration for this case due to the wide bandwidth characteristics of the amplifier. For high frequency application the $\frac{1}{f}$ noise is not important. The thermal noise is the dominant contribution of amplifier noise within the filter passband. For the amplifier reported in this dissertation, the switch capacitor noise dominates.

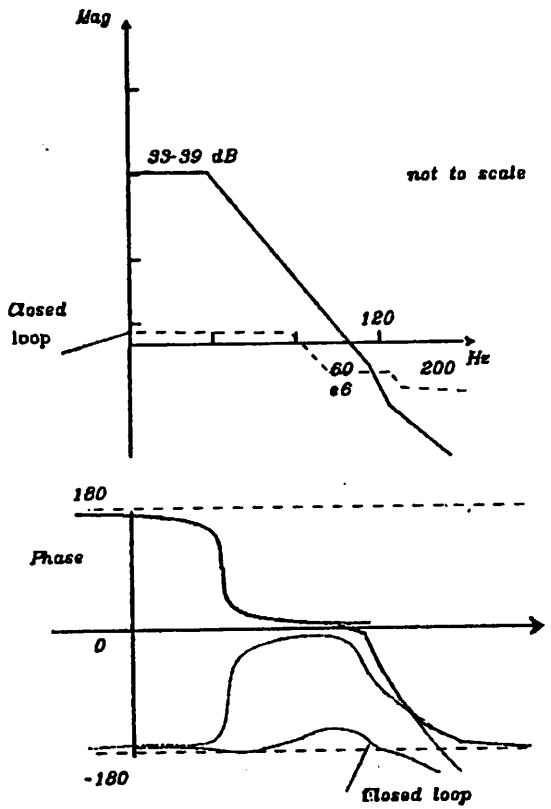


Fig4.18a
Freq. Response for Open Loop
Pos and Neg-loss Amps

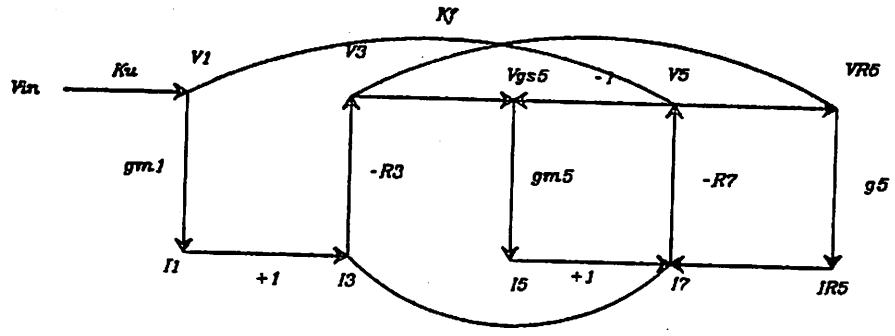


Fig.4.16b SFG for the closed loop Neg-loss Circuit

In fact, SPICE simulation shows a typical amplifier input referred noise of $60\frac{nV}{\sqrt{Hz}}$ whereas the switching noise can be larger than $\frac{300nv}{\sqrt{Hz}}$.

4.6.2. Switched Capacitor Noise

The thermal noise in the conducting channel of the switch transistor is sampled into the capacitor. This noise can be estimated as follows :

$$\frac{n_{rms}}{\Delta f} = 4kT_a R\,|S(f)|^2 \qquad (4.19)$$

where $S(f)$ is the frequency transfer function of the equivalent switch and capacitor RC_u network formed by the transistor channel resistance and the sampling capacitor[A]. The total noise is obtained by integrating over the frequency spectrum:

$$n_{rms} = \int_{-\infty}^{\infty} 4kT_a R\,|S(f)|^2 df \qquad (4.20)$$

From the simple low pass expression for $S(f)$:

$$S(f) = \left[\frac{1}{1 + (2\pi f RC)^2}\right] \qquad (4.21a)$$

from (20a) and (21):

$$\frac{n_{rms}}{\Delta f} = 4kT_a R \frac{1}{4R_{on}C_u} \qquad (4.21b)$$

When the sampling capacitor transfers charge to the integration capacitor the amplifier output noise is obtained in the same fashion but now the noise bandwith is approximately given by:

$$\Delta f \approx C_u \frac{fs}{C_f} \qquad (4.21c)$$

A. where k is the Boltzmann constant and T_a the ambient temperature.

one obtains :

$$n_{RMS} = \frac{kT_a}{C_u fs}\,\frac{C_u fs}{C_f} = \frac{kT_a}{C_f} \qquad (4.21d)$$

The first factor is the switch noise sampled in C_u and evaluated at the clock rate fs, the second is the integrator noise bandwith.

The SC noise presented to the integrator has the effect of a time varying offset. The noise calculations in the filter are performed by adding all the noise contributions in a given node and using the transfer function in the filter from that particular node to the output. This calculation is very time consuming. The use of computer programs to evaluate the noise performance in high order filters is vital. Almost all the state of the art circuit simulators include calculations of this type, e.g., SC simulators DIANA, SCORP, etc.

Another form of noise is *clock induced noise*. The switches couple the clock transitions to the signal paths. This effect, however, is common-mode in nature, and so the use of a fully differential technique is highly insensitive to its effects. The experimental measurement of this noise is given in Chap.5. The rejection is of the order of 60dB [23].

4.6.3. Power-supply Rejection

The differential amplifier provides rejection of the positive supply variations of the order of the common-mode rejection, 50dB. The coupling of supply noise is ultimately dependent on amplifier mismatch.

$$\frac{\delta V_o}{\delta V_{ss}} = \frac{\delta I}{\delta V_{ss}} \times \Delta R \qquad (4.22)$$

The high frequency power supply coupling is done through parasitic capacitors and is also determined by circuit mismatch. The negative supply presents a lower rejection factor because it is a function not of output resistances but of body effect in the driver devices. The circuit here was designed to operate on a single 10V supply which eliminates the problem of the negative supply dependence.

4.6.4. Amplifier Common Mode Bias

It is of fundamental importance to keep the bias point regulated to obtain maximum amplifier dynamic range. Fig.4.17a shows the common mode feedback bias circuit used. The common mode circuit must have a faster response than the filter response dictated by the dominant filter time constant. The design of a continuous time feedback approach will then require single stage amplification which again limits the gain and accuracy of the common mode loop. A novel dynamic common mode feedback technique recently introduced by Senderowicz [1] provides fast common mode feedback using SC circuit techniques as illus-

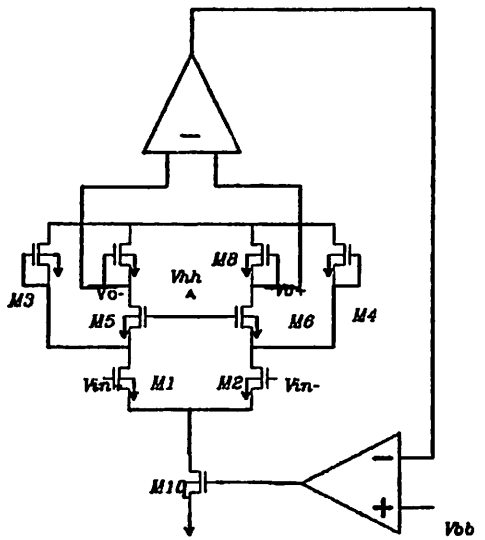


Fig.4.17a

Cascode Amp with Common Mode Feedback Bias

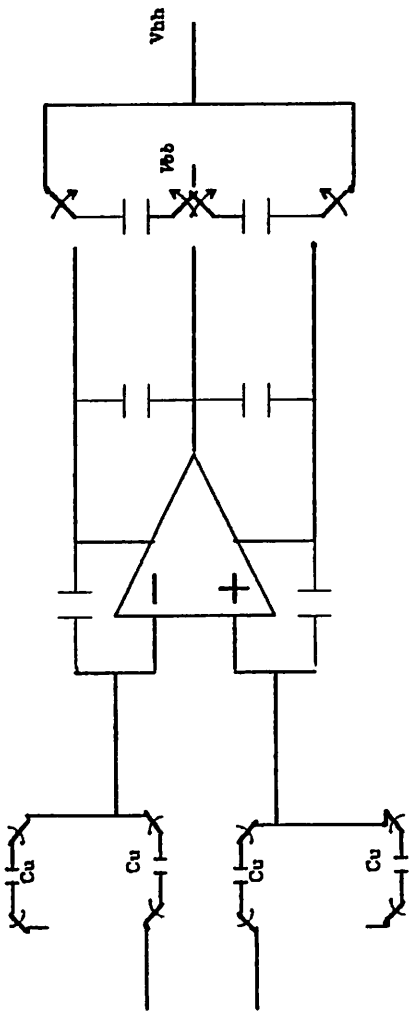


Fig4.17b Dynamic Common-mode Bias Schematic

trated in Fig.4.17b.[2]

The reference voltage uses a replica circuit as shown in Fig.4.18 to achieve very accurate matching and tracking properties in the amplifiers. The circuit schematic shows the replica devices for the amplifier bias current source and differential transistors M_1, cascode and load current sources. Two reference voltages are necessary: one is a high voltage V_{hh} for the bias of the output node, and the other is a low voltage Vbb to bias the differential pair current source.

4.6.5. Negative and Positive Loss Amplifier Static Characteristics

SPICE simulation for static small signal transfer was performed for the circuits described above, and the results are depicted in Fig.4.19. The static transfer characteristics, $\frac{V_o}{V_i}$, of the negative loss circuit provide a way to observe the circuit nonlinearity as presented in Chap.3 It depicts a linear positive gain region centered around the origin of the $\frac{V_o}{V_i}$-plane. A finite operating range is given by the output voltage swing that keeps the cross coupled devices in the active saturation region. At the borders of this region the non-linearity is produced by one device going to a triode mode of operation. The devices are within saturation for output voltage swing less or equal to $1\,V_T$.[3]

At the edge of the active negative resistance operating region the positive feedback gain collapses as discussed in the previous chapter. The DC static characteristics in open and closed loop for the negative and positive loss circuits

2. The operation uses two integrating capacitors C_i (capacitor bridge follower) which give AC common-mode feedback detection within every clock phase and common mode shift. The comparison with the common mode ideal reference level is done by SC switched resistor paths. The error (difference) produces a charge difference which is injected to the differential pair tail bias source. The correction for this loop is updated with the same rate as the filter sampling $\frac{T_o}{2}$ time. The common mode loop presents an integrator characteristic with a time constant given by $\frac{fsC_i}{C_u}$.

3. This swing limitation is not a problem for the particular application, i.e., narrow-band RF filters, since the signals handled are low level.

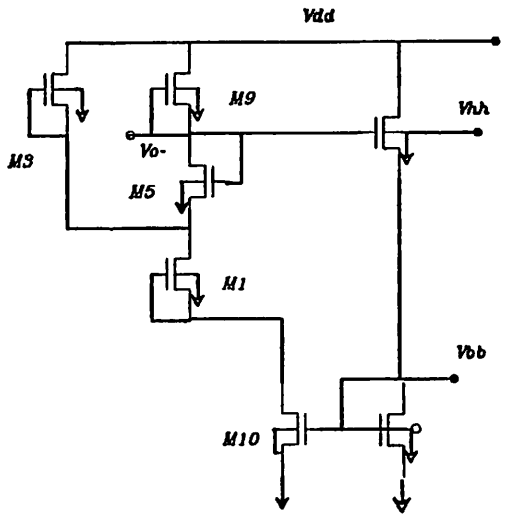


Fig.4.18 Replica Bias Circuit

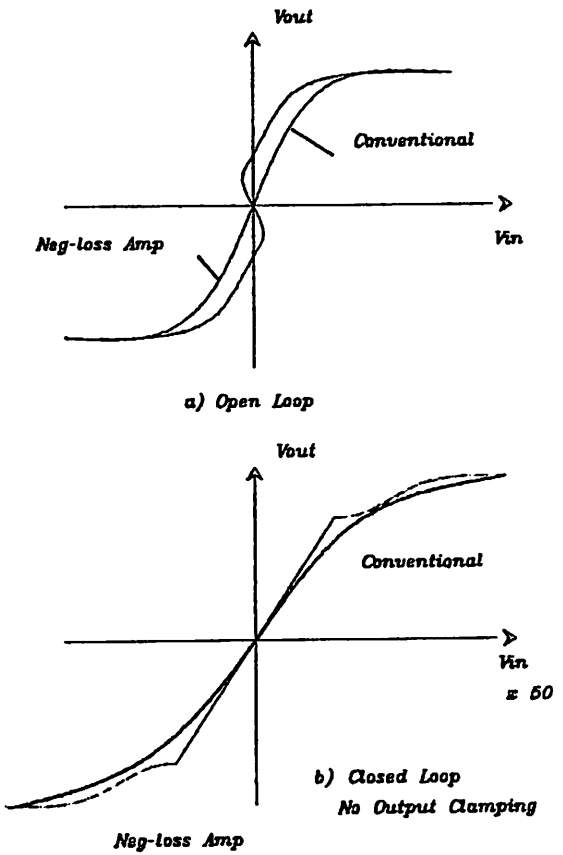


Fig.4.19 Static Transfer Characteristics (SPICE)

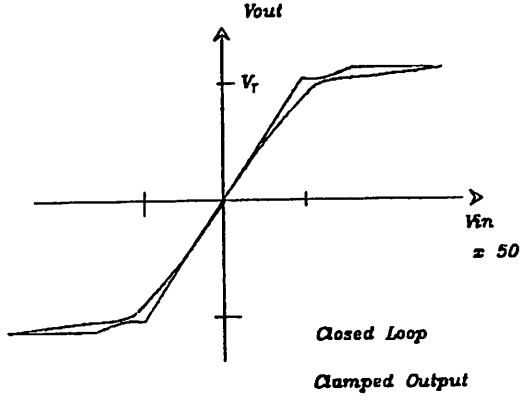


Fig.4.19c Static Transfer Characteristic
for Clamped Output Circuit

are shown in the figure. Within the active region the closed loop gain is negative and the nonlinearity has the form of a gain expansion (gain increasing with voltage). At the border of that region, the positive feedback collapses and the transfer presents a jump transition as seen in the figure and then continues towards saturation in the same form as the conventional amplifier.

4.7. Computer Simulation

Bias conditions and common mode feedback were simulated, followed by small signal frequency response and transient large signal analysis. The comparison in terms of matching of frequency responses for the three types of amplifiers are presented in Fig.4.20. An agreement of better that 2% was found for the DC gains under nominal conditions, and very similar frequency response were demonstrated.

The NMOS device parameters for SPICE2 were taken from experimental data and tailored to the NMOS level 2 model. Table 4.2 shows the summary of the relevant parameters. A problem in the simulation can arise from the lack of modeling of the charge conservation, and the simulation must be tailored by the parameter X_p which controls the charge distribution for drain and gate in the transistor saturation region.

Worst case device parameters were used in the simulation to analyze extreme conditions. Even though the temperature effects are not reliably modeled in SPICE2, temperature variations were used as a source of perturbation to measure the matching and tracking properties of the circuits. The results showed that the configurations do track one another in DC gain and frequency response. Therefore the loss cancellation is accurately maintained in presence of external perturbations.

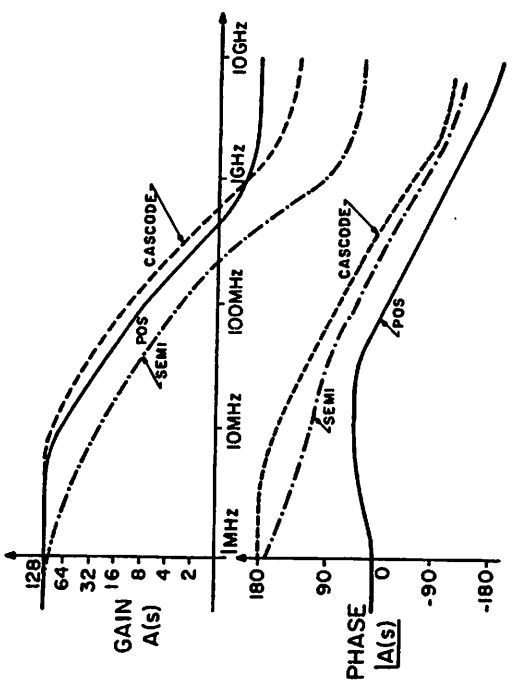


Fig.4.20 Frequency Response for the Cascode load
Neg-loss and Alternative Pos-loss

4.8. Summary

The actual NMOS implementation of the negative loss and positive loss circuits is presented together with the analysis of small signal static and transient circuit response and the results from computer simulation.

CHAPTER 5

PROTOTYPE SC FILTER REALIZATION AND EXPERIMENTAL RESULTS

5.1. Filter Design

A sixth order elliptic SC bandpass filter was selected to demonstrate the cancellation technique. The filter is intended for narrow-band applications. The prototype filter specifications are summarized in Fig.5.1 and are consistent with the definition in Zverev's filter design book [60]. The basic set includes the attenuation ripple in the passband A_p and the bandwidth at the cutoff frequency BW. Rejection bandwidth BWS at the attenuation A_s, and minimum stopband attenuation, $A_{min}(s)$. The specification parameters and a typical Cauer transfer function are shown in Fig.5.2.

The design used the *Leap-Frog (LF)* active simulation of an LC ladder, [25] The usual approach is to design a low pass equivalent filter and then use the lowpass-bandpass transformation, Table 5.1, to get the final filter characteristics. The equivalent elliptic lowpass is a third order elliptic filter illustrated in Fig.5.3a. The elements that produce the transmission zero are transformed by Thevenin equivalents to controlled voltage sources as shown in Fig.5.3b. Each L and C is simulated by an integrator as in Fig.5.3c. The SFG node variables are all converted to voltage to map the active realization as depicted in Fig.5.3d. Low pass to band pass transformation is performed which replaces every integrator by an integrator pair (resonator) as shown in Fig.5.3e [65]. The math involved in the transformation is simple and can be found in any classic filter design book.

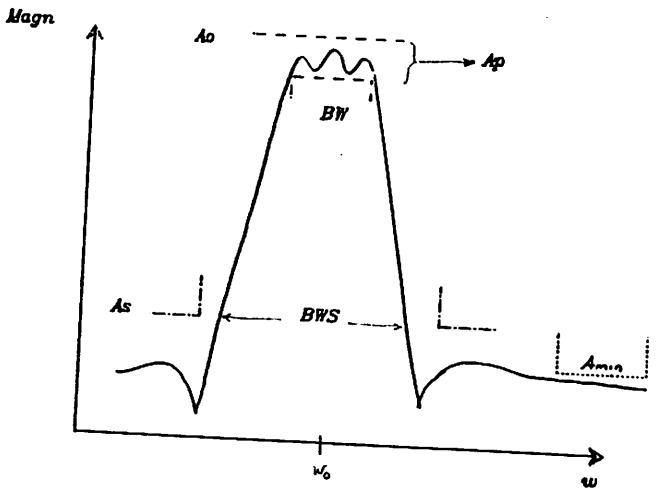


Fig.5.1 Bandpass Filter Terminology

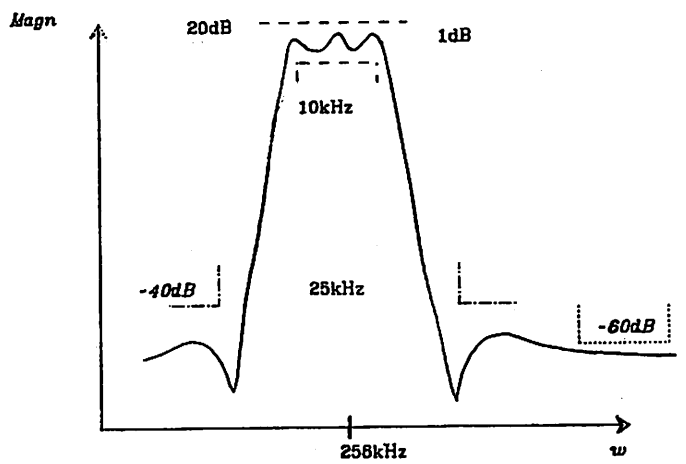
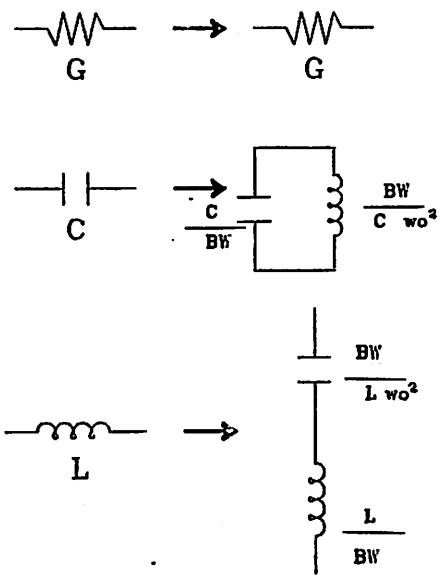
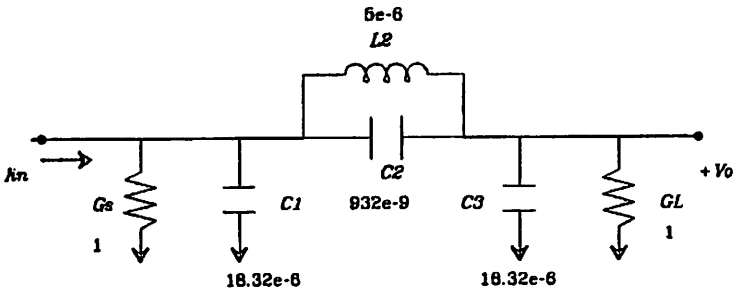


Fig.5.2 Typical Narrow-band IF filter Specs

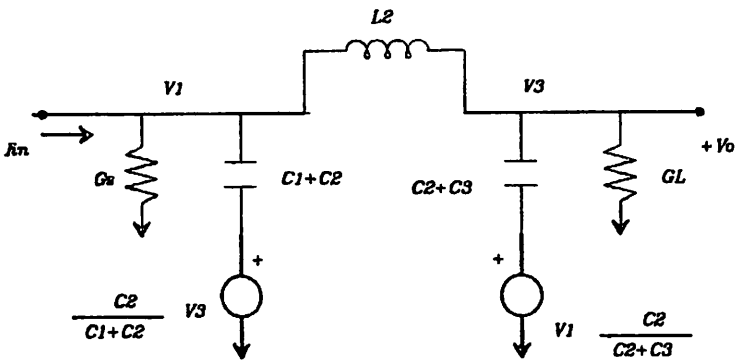
TABLE 5.1



Lowpass to Bandpass Transformation



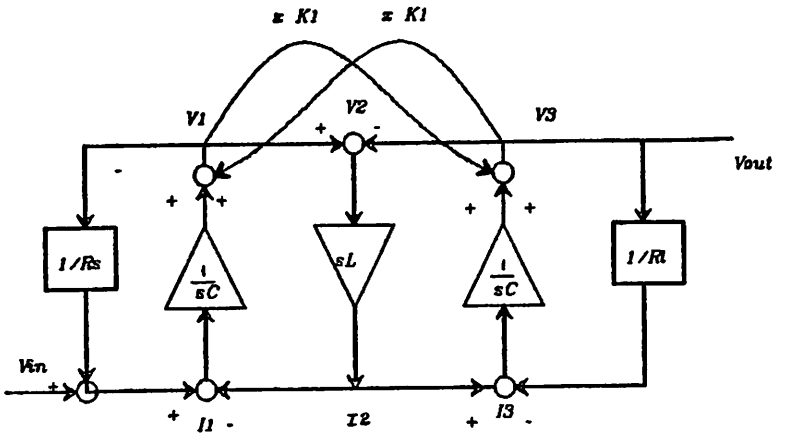
Third Order Lowpass Equivalent



Equivalent Elliptic Filter with

C-loop replaced by dependent sources

Fig.5.3



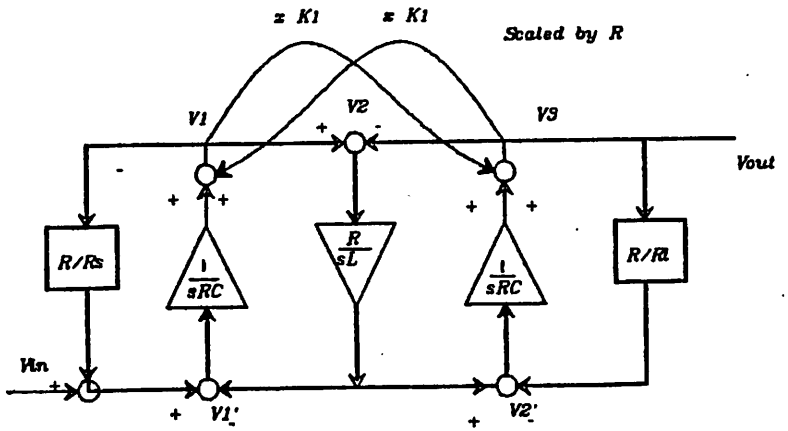


Fig5.3cd Block Diagram for the Leap-frog Implementation

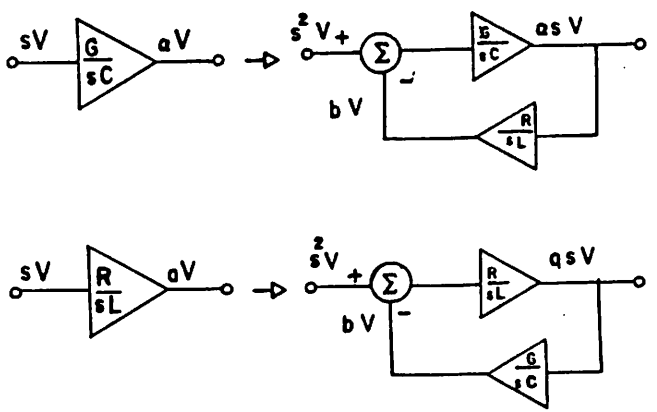


Fig.5.3e Active Low-pass Element to Band-pass Element

Low–Pass to Band–Pass Transformation on Active Filters

Besides the narrow band filter requirements in the amplifier DC gain, a very important aspect is the filter sensitivity. The bandpass filter has the same sensitivity to component variations as the low pass equivalent, however the filter sensitivity to the resonator center frequency increases proportionally to the Q factor of the resonators in the filter. We then must tightly control the variation of the components which determine the center frequency. This is done by using a filter configuration based on identical resonators where the center frequency is given by capacitor ratios as shown in Fig.5.4. The excellent matching properties found in IC capacitors permit very accurate definition of capacitor ratios and thus of the center frequency. A complete study of the sensitivity properties of the identical resonator active LF is given by Laker and Ghausi [47].

The use of scaling on the filter to reduce the configuration to identical resonators increases the dynamic range because it assures identical frequency peaking of the filter nodes. As a result of the scaling large attenuation factors are encountered in the couplings between resonators. The coupling factors are of the order of magnitude of the filter's resonator selectivity kQ and thus large capacitance value spread results. Capacitor voltage dividers offer a good circuit design solution to this problem [21] (Fig.5.5). Other techniques have been developed [82] which make use of resistors as attenuators to decrease the capacitor spread. The wide spread signal level may cause dynamic range problems. The switching noise must be kept out of the low level signal path. This can be done by using continuous time couplings (capacitive coupling). Capacitive couplings can be easily performed in the fully differential circuit scheme. The use of continuous couplings has the drawback that it increases the longest path due to direct coupling and in the case of elliptic filters can produce continuous time paths which can affect the final transfer function and even lead to instability [30, 40].[1]

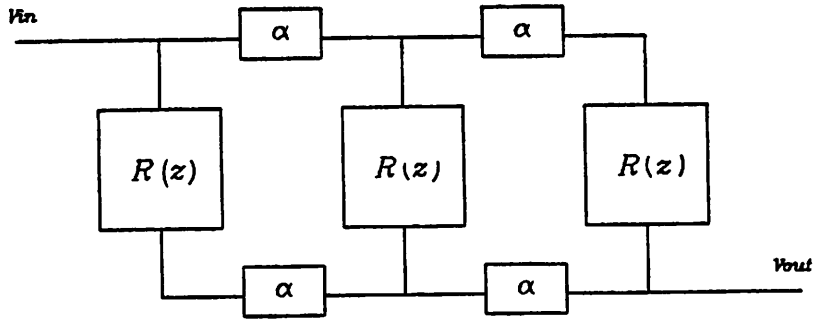


Fig5.4 Identical Resonator Filter Block Diagram

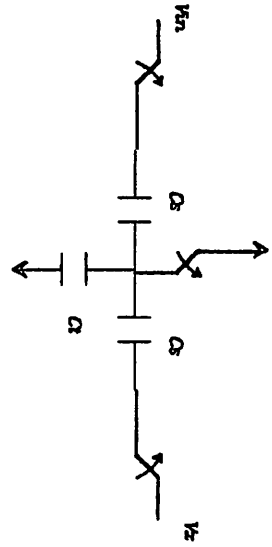


Fig.5.5 C Divider to reduce Component Spread

6.1.1. Filter Terminations

The terminations in a lossless 2 port ladder filter define the pole locations inside the LHP. The pole in turn determines the frequency transfer characteristics of the filter. The terminations in active filters are usually realized by precision resistors. The SC termination also gives a very precise loading of the lossless filter. In the LDI mapping, the termination can either have one delay or no delay. This results in errors in the filter transfer function. However this error in only important when the filter sampling frequency and center frequency are closer to each other. In high frequency LDI filters these termination errors are corrected to a certain extent by using complex conjugate terminations for the ladder filter [3]. A second way to obtain the pole shift is by using continuous time (AC) terminations. In this case the loss is produced by adding LHP zeroes in the filter, thus bending the root locus to the LHP. The AC losses are much simpler to implement because they do not require switches and save chip area

6.1.2. Parasitic Capacitance

Capacitor parasitic effects are a major consideration in the development of high frequency filters because they affect the transfer function in the form of a loss and determine amplifier settling time. The parasitic capacitance determines the smallest circuit capacitor size that can be used. Special circuit and layout design techniques are used to minimize the parasitic effects, e.g., top plate of the capacitor assigned to the parasitic sensitive node. The signal loss due to parasitics can be alleviated by parasitic free sampled data integrator schemes [72]. This provides a mean to reduce the total circuit capacitance substantially. The basic configurations for parasitic free inverting and non-

1.-In the resonator circuit the offset signal travels along the circuit and affects the DC output level. In active integrator design it is customary to add a large resistor in the feedback to guarantee that the integrators initial condition is zero. i.e., conditions of optimum dynamic range . Omitting this element leads to an initial condition in the capacitor which limits the fiter dynamic range. In filter design, the circuit termination (load elements) provides the reset to zero initial conditions.

inverting LDI integrators have been developed. Recently a bilinear circuit approach has been presented for parasitic free sampling which is easily implemented by the differential amplifier. [1]. In the balanced loss cancellation technique the error produced by parasitic capacitance at the amplifier input is large (proportional to the gain). the effect is also canceled by the balanced finite gain compensation technique. All the frequency prewarping, e.g., prewarp for bilinear or LDI mapping, is included in the filter synthesis at the low stages of the design [62].

6.1.3. Sampling Frequency Considerations

A key issue for high frequency SC realization, is keeping the sampling frequency very close to the Nyquist frequency, thus relaxing the amplifier speed required. In doing so, inaccuracies in the obtained SC filter compared to the original continuous time equivalent result. Examples of this kind of error are the out of phase terminations in LDI filters. This error can be decreased by using complex conjugate terminations or by using bilinear mapping techniques [3,39]. The differential bilinear switching scheme is shown in Fig.5.6.

The β factor, defined as the ratio of clock frequency, to filter frequency is reduced as mentioned before in order to extend the operation of SC filters to higher frequencies. More important than this ratio is the ratio between the amplifier gain-bandwidth product and the sampling clock period which completely determines error at sampling time. The NMOS single stage circuit presented has a GB of $60MHz$. Fig.5.7 shows the complete schematic for the sixth order quasi elliptic filter.

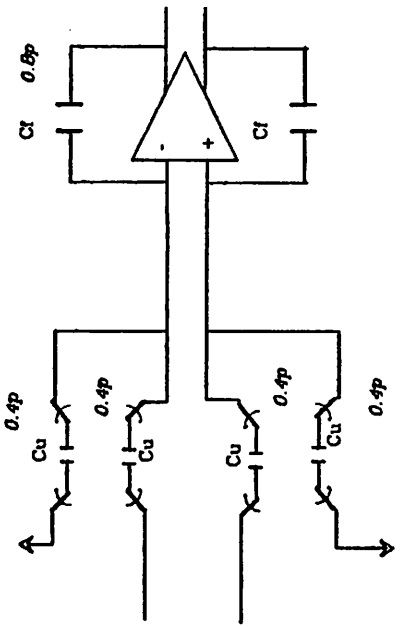


Fig.5.6 Parasitic Free Bilinear SC Integrator

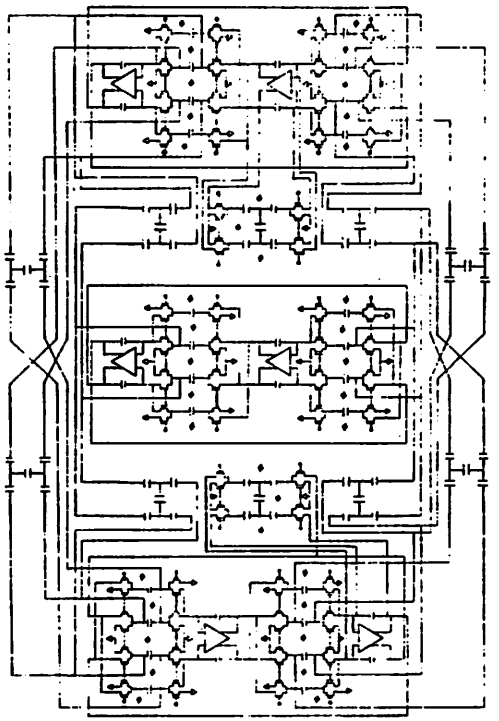


Fig.5.7 Sixth Order SC Filter Schematic

6.2. Prototype Filter Synthesis

The filter synthesis can be performed by filter tables or CAD techniques. The prototype presented here made use of both approaches. The active filter design is implemented by using SFG techniques as illustrated in Fig.5.8. The graph shows the filter consisting of loops of integrators which define the filter characteristic equation (Mason's rule). Two types of loops are encountered: very tightly coupled (resonators) and loosely coupled loops (inter-resonator couplings). The Loops with a single integrator (delay) and a negative feedback element form the terminations. The transmission zeroes appear as attenuation loops with no delay. The signal comes in and out of the nodes as shown in the graph. The implementation of these branches requires some circuit modification because they are adding signal to the amplifier output. The addition can be done by using the continuous coupling (adder-integrator) or an external adder amplifier. The latter solution requires one more active circuit. By re-routing the SFG as shown in Fig.5.9 a new graph which removes the transmission zero paths from amplifier outputs can be obtanied. A new set of branches is added to all the nodes where the original branch was affecting. Further analysis of the new SFG shows that some of the paths have negligible value. The effect of the removal of these paths is checked by a computer simulation of the new SFG which results in a shift of the transmission zeroes towards the left half plane. The new SFG of Fig.6.10 results. The modification primarily affects the phase characteristics of the transfer function and has negligible effect on the passband BW and BWS parameters. For the particular specifications of the proposed filter, the removal of the low level paths still meets the requirements.

6.3. Resonator Circuit Breadboard

A differential SC resonator breadboard was built to demonstrate the feasibility of the loss cancellation scheme in a filter configuration, see Fig.5.11. Stan-

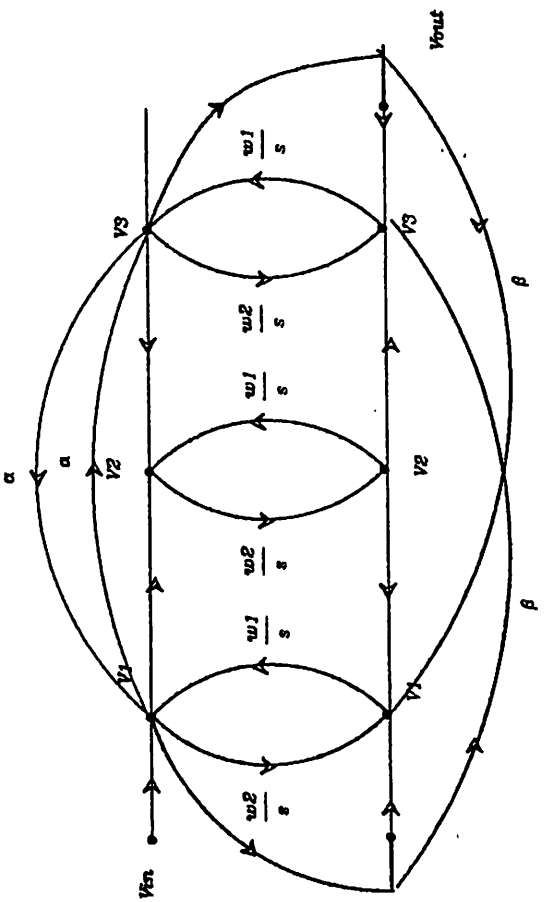


Fig5.8 Signal Flow Graph for the Sixth Order Filter

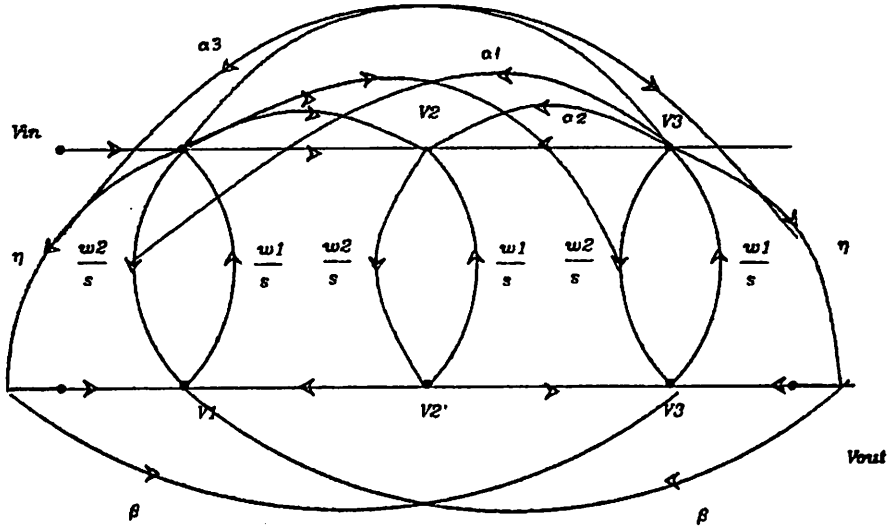


Fig.5.9 Sixth Order Elliptic Filter SFG

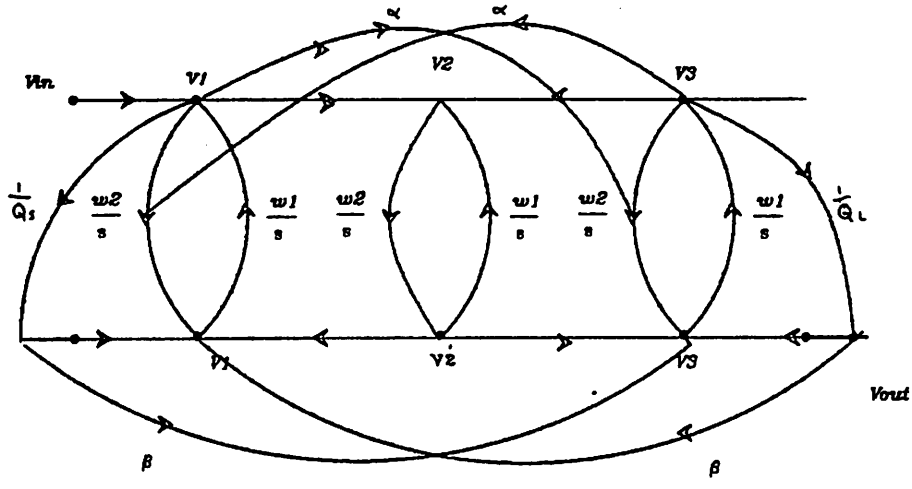


Fig.5.10 Sixth Order Semi-elliptic Filter

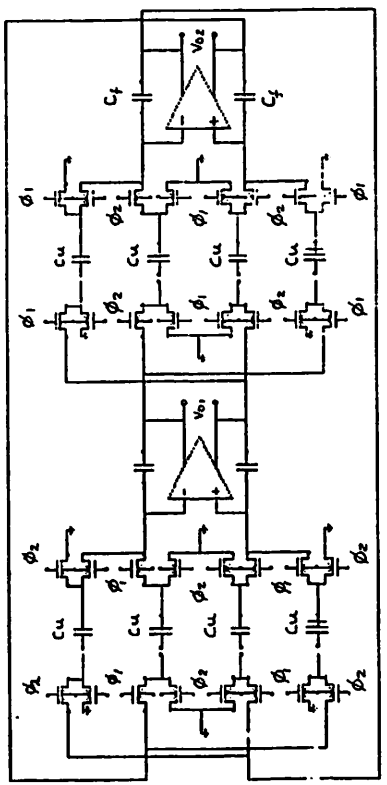


Fig.5.11 Fully Differential Resonator Breadboarded

dard NMOS parts where used to build the single stage amplifiers and CMOS switches realize the SC elements. The breadboard proved the circuit stability for large signal and stability against power supply transients. The breadboard was operated at scaled frequency and the results correspond closely with the expected loss cancellation. The stability in the large was experimentally demonstrated by this model. Data from the breadboard is included in Table 5.2.

5.4. A Few Comments on Circuit Simulation

The most important points regarding simulation were introduced in the previous chapter. In this section only a few remarks about simulation are included. The device level simulation was performed with SPICE2. The basic goal was to include the effects of the parasitic capacitance and interconnect resistance. The ballpark parameters used in the simulation were obtained from the actual layout by a layout extraction program (mextra) recently developed at Cal [54]. Worst case analysis was then performed to obtain the practical frequency limitation. The result from the simulation indicated that clock rates of the order of 5 MHz can be used. Experimental results showed a lower limit as discussed in sect. 5.4.

5.5. Layout Work

The circuit layout was done with computer graphics [80]; this permits a very structured layout design. The filter contained six levels of nesting. At the bottom level reside the typical size transistors (a wide and a narrow enhancement transistor and two types of depletion transistors), the switch transistors , the unit capacitance and the different contact units. At a second level the groups of transistors in stacked form realize the input transconductance,cascode load , bleeder and current source configurations.

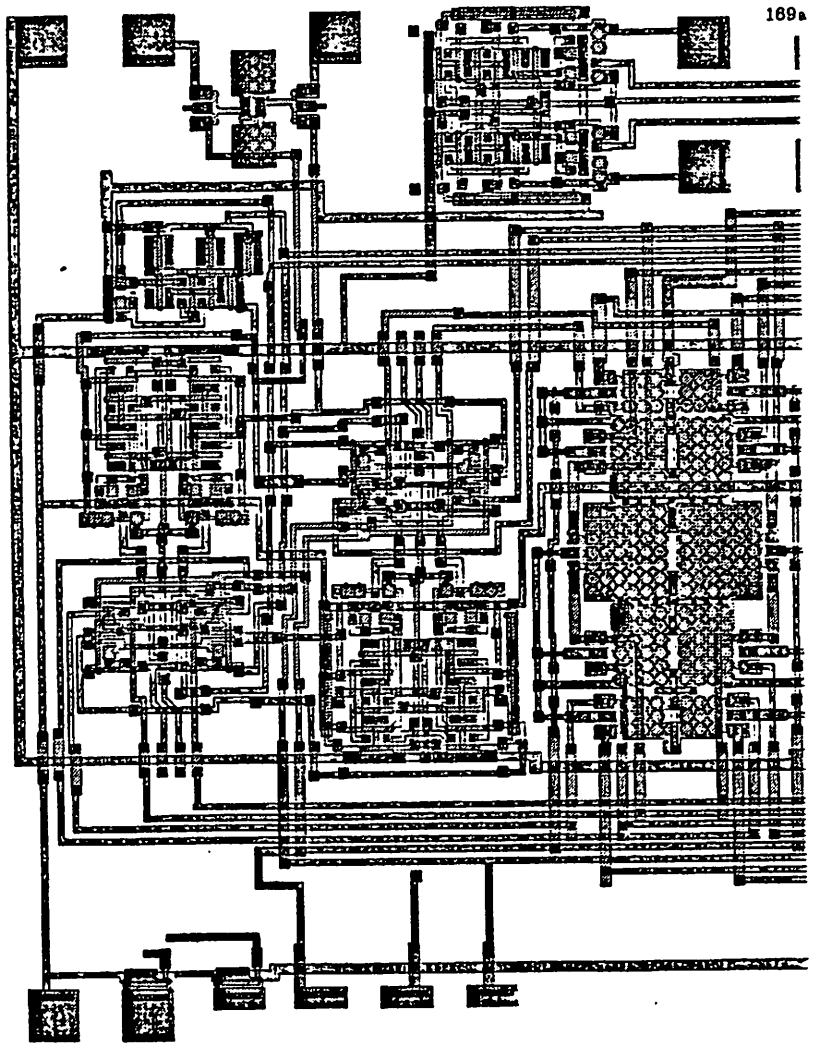


Fig.5.12a IC Resonator Layout

The capacitors are put together to form total capacitances. The third level joins the transistor configurations to form the op-amps and joins switches and capacitors in the SC array of the SC integrator. The resonator on the fourth level consists of the capacitor arrays and the amplifiers (Fig.5.12a). All the intercoupling and loss termination capacitors are merged in a capacitor bank. The interconnections between the elements of the previous level and power and I/O lines are performed at the fifth level.

The primary goal in the layout design was to optimize the symmetry and proximity of the circuit main elements in order to improve the parameter matching. The amplifiers configurations for the positive loss and negative loss are identical except for a short bridge which implements the cross couple load as depicted in Fig.5.12b. Stacked devices layout is used to improve device matching. Capacitor arrays are laid-out in symmetrical fashion in an alignment independent configuration. The full blown layout plot is shown in Fig.5.12c indicating the hierarchy levels in the design.

5.6. Fabrication

The single poly depletion load process (UCB) used is a derivation of a 12 masks CMOS process developed at UCB. It is a $8\mu m$ $700A^{o}$ gate oxide process featuring shallow implanted junctions and implanted threshold correction. The layout pattern was converted to a David Mann format and the actual seven masks were produced in a standard pattern generator. All the fabrication steps as shown in App.D including implants were done at the UCB solid state lab facility. The process has a GB of $800MHz$ and is suitable for the design of high speed op-amp, SC and digital circuitry. Process evaluation is also included in the appendix.

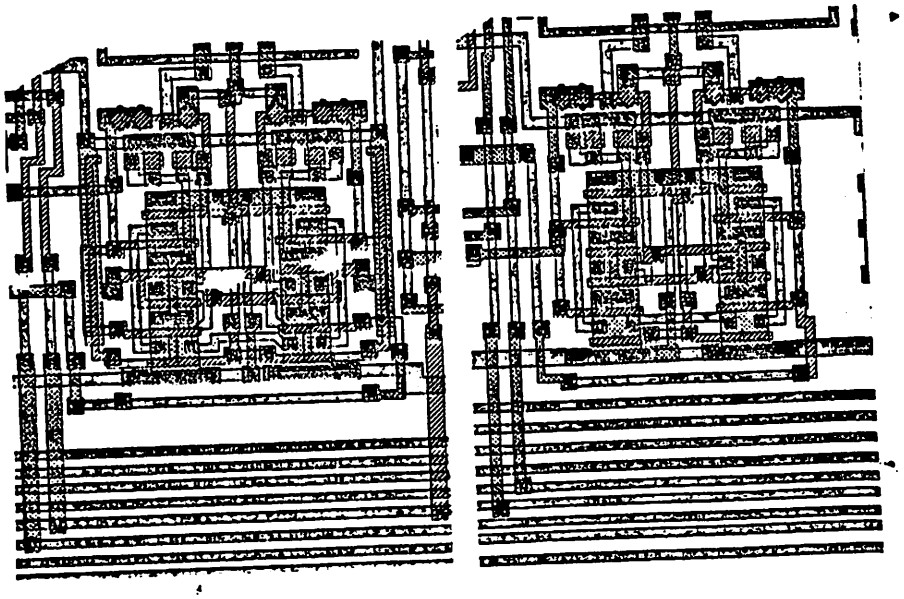


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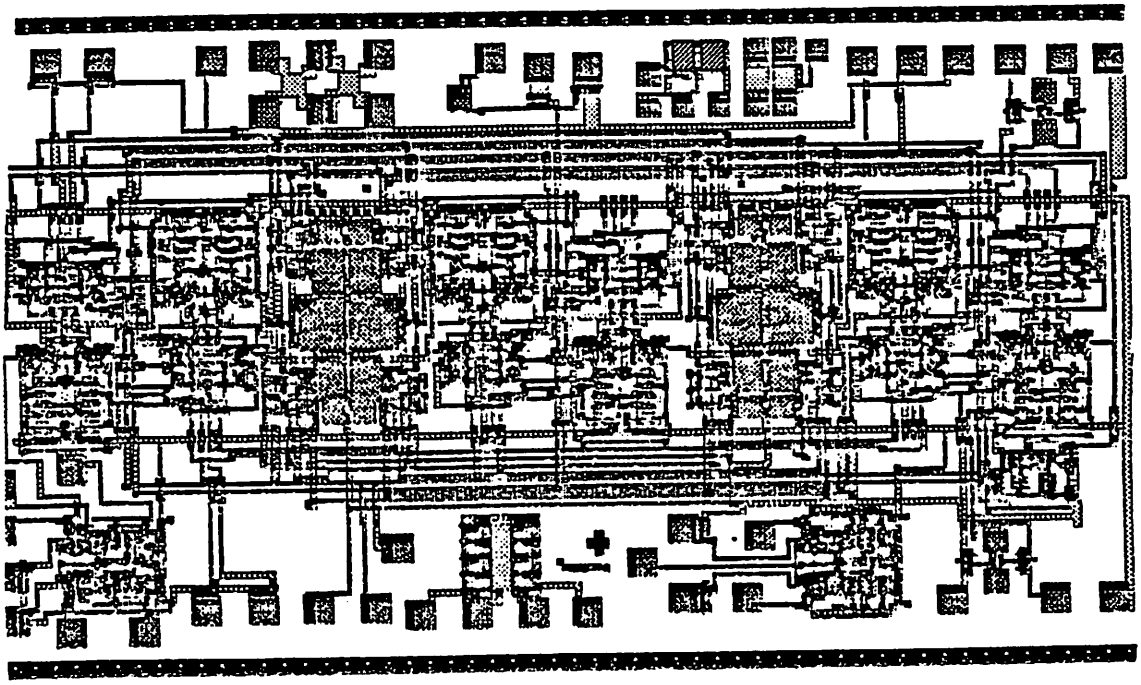
Fig.5.12b Amplifier Layout for Pos and Neg-loss



171a

Fig.5.12c Sixth Order Filter Layout

TABLE 5.2

BREADBOARD CIRCUIT	
$T = 25°C$ @ $VDD = 10V$	
Integration Cap Sample Cap Clock Rate	$220pF$ $56pF$ $40kHz$
Amplifier Voltage Gain Bias Current	30 $100\mu A$
Resonator Center Frequency Passband Gain Q factor 100 Output Swing	$8kHz$ $20dB$ $700mV$
Discrete Transistors Diff Pair Transistors Switches	$XSC2689A$ $CMOS4007$ $CMOS4047$

The photolithography was made with standard projection alignment techniques. The active die size is $4 \times 2mm$.

5.7. Experimental Results

5.7.1. Measurement set-up

All the measurements were done with University facilities. Device probing evaluated the device characteristics and the diffusion and poly resistivities. The amplifier measuring set-up for time domain response measurements is shown in Fig.5.13a. Table 5.3 shows the measured NMOS amplifier performance. Amplifier step response was measured with an capacitive feedback. The step response for the closed-loop configuration shows a 0.5% settling time of $160ns$ for 1 V output step for the amplifier with $C_u = 2.5pF$ and $C_f = 1pF$ loaded with a $10pF$ load is shown in Fig.5.13b. The input driving signal was a 1 Volt symmetric 1.3 MHz square wave.

5.7.2. Filter Measurements

The tests were performed under the set-up shown in Fig.5.14. The non-overlapping clock is off-chip crystal controlled and all the required phase control is done with CMOS digital parts. The filter is AC coupled to a programmable signal generator as shown (frequency synthesizer) and the output is evaluated in the standard spectrum analysis. The filter parameters are as defined earlier in this chapter.

5.7.2.1. Center Frequency.

The filter measured transfer function is shown in Fig.5.15 for a $500kHz$ sampling clock, $100kHz$ filter center frequency and $5kHz$ bandwidth at $-3dB$. Table 5.4 contains the measured passband and stopband data for the filter. For

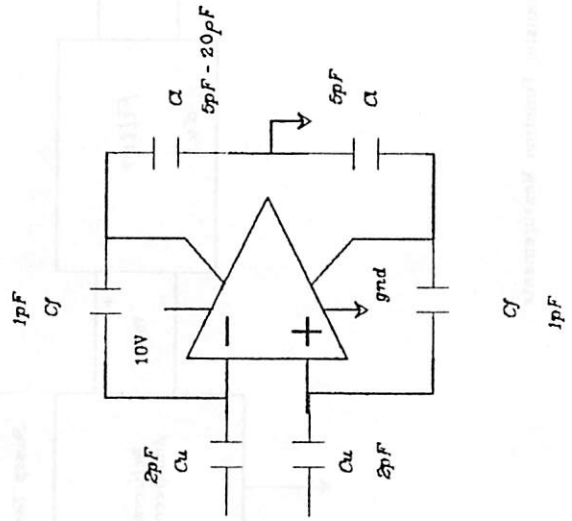


Fig.5.13a Amplifier Measurements Set-up

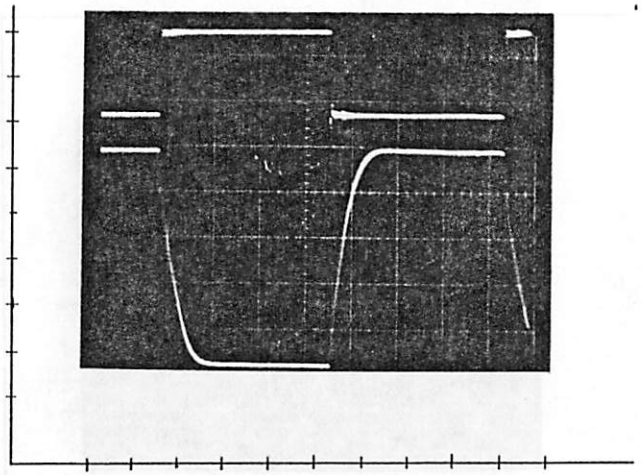


Fig.5.13b Experimental Step Response for the Positive Loss Amplifier

Step Response, Vdd=10v, Cload=20pF,
Closed Loop Gain = 2.5
Vert. 200mv/div Horiz. 100ns/div

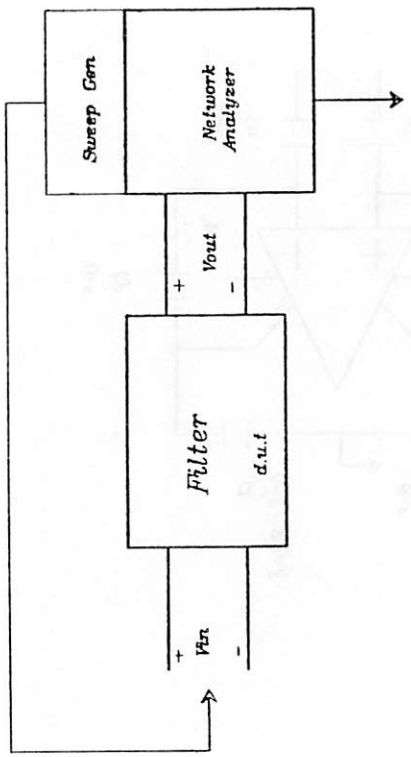


Fig5.14 Filter Transfer Function Measurements

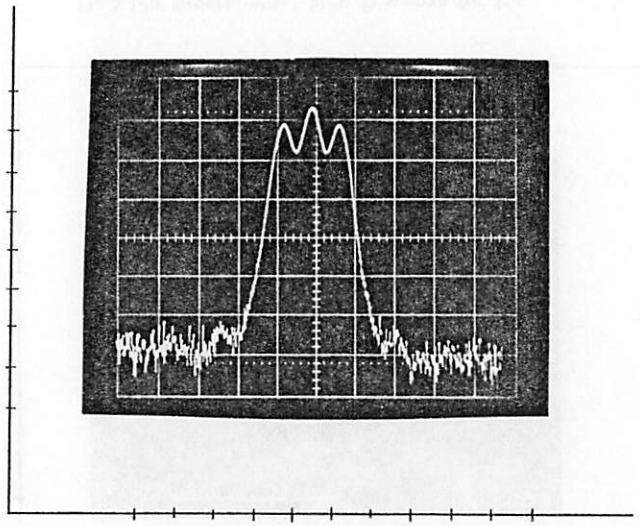


Fig.5.15 Experimental Filter Transfer Function

NMOS Filter Transfer Characteristics
Clock Rate = 1 MHz, fo = 200 KHz
Vert. 10dB/div Horiz. 5KHz/div

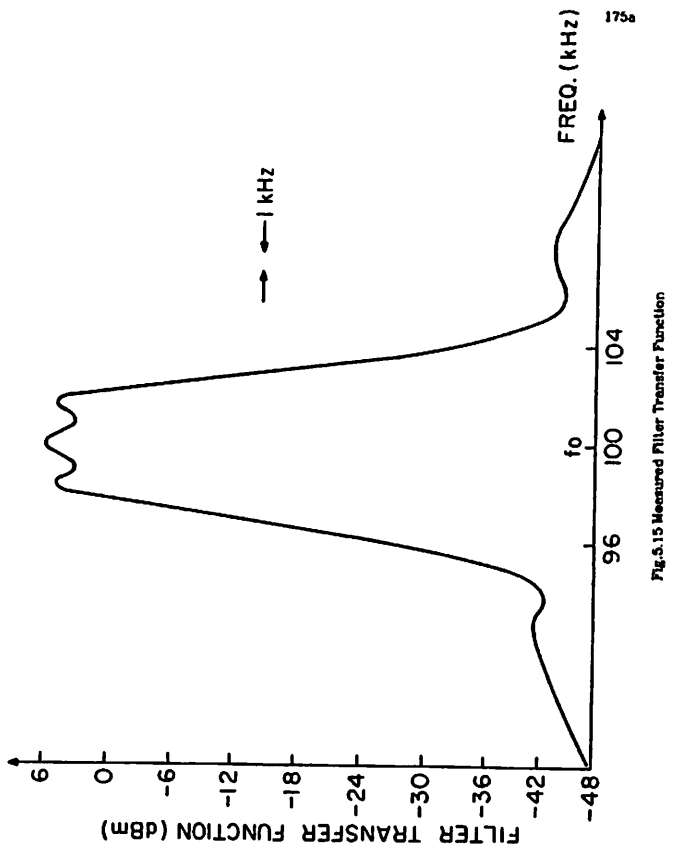


Fig.5.15 Measured Filter Transfer Function

TABLE 5.3

NMOS TEST AMPLIFIER PERFORMANCE $T = 25°C \oplus VDD = 10V$	
PARAMETER	Value
DC gain	50
Unity Gain Frequency	60*MHz*
Quiescent Current	600μA
Settling Time 0.5%	180*nsec*

TABLE 5.4

MEASURED BANDPASS FILTER CHARACTERISTICS $T = 25°C \oplus VDD = 10V$	
Center Frequency	200*KHz* / 100*kHz*
Passband Ripple Vout 6 dBm	=3.0*dB* / ±1.5*dB*
Passband Gain	20*dB*
Passband Bandwidth	10*kHz* / 5*kHz*
Stopband Bandwidth	18*kHz* / 9*kHz*
Stopband Rejection	−36*dB*
Output Swing @ 1%	780mV_{peak}
Third Harm. Disto.	
Out of Band signal @ 1%	310mV_{peak}
Intermod. Disto.	260 μV
RMS in-band noise	60*dB*
Dynamic Range	
Power Dissipation	30 *mW*
Maximum Clock Rate	2*MHz*

a sample rate of $500kHz$ the average measured filter center frequency was $103.12kHz$ with an accuracy from wafer to wafer of ±1.5%. This gives a β ratio of 3% deviation with respect to the designed value. Some of the distortion of the transfer function found are discussed in the context of passband attenuation and Q factor.

5.7.2.2. Selectivity Q

Filter selectivity is measured for different sampling rates. For $100kHz$ center frequency, the $-3dB$ bandwidth of $5kHz$ was obtained with a standard deviation of 5%. This indicates that the resonators in the filter achieved quality factors close to 400 from amplifiers with dc gains of 50. The desired Q factor obtained from this process starts to drop for a sampling rate of 2 MHz. This frequency limitation of the Q factor for different signal levels indicates the effects of parasitics in reducing the speed of the charge transfer. This phenomena can be reproduced in the computer simulation by adding parasitic load capacitance to the amplifiers, thus slowing down the charge transfer process. The effect can be eliminated by reducing circuit parasitics and optimizing layout routings. An effective center frequency to bandwidth ratio of 20 with 5% standard deviation was obtained.

5.7.2.3. Filters Passband Attenuation Ripple

For the filter operation at $100kHz$ center frequency, and an input signal level of $6dBm$ ($1mw$ at $50\Omega = 236mv_{rms}$), the measured passband ripple was $\pm 1.5dB$. The ripple is increased to $\pm 3dB$ for doubling the filter center frequency. The effects observed in the filter gain indicate that the variation comes from an error in the speed degradation of the op amps.

5.7.2.4. Out-of-band Rejection

The out-of-band rejection was met by the quasi elliptic filter. In fact the measured rejection agreed within 3 dB with respect to the designed value. The stopband shows $38dB$ of rejection for a bandwidth of $10kHz$ ±5%.

5.7.2.5. Filter Distortion

Distortion measurements were based in conventional IF receiver tests. Fig.5.16 shows the test set up where an In-band carrier-supressed AM signal is applied to the filter input until a 1% (-40dB) third harmonic distortion at the output is recorded. Output level recorded is $780mV_{peak}$. This level is defined as the nominal output level for the filter. Fig.5.17 depicts the third harmonic distortion values.

A figure of merit for narrow band filters is the intermodulation distortion. This parameter was measured by applying a CW in-band at the nominal level (defined earlier) to the filter and an out-of band signal, see Fig.5.16b. The undesired signal level is increased until the third in band intermodulation distortion reaches the -40 dB level. Distortion is measured at the nominal center frequency of $100kHz$. Fig.5.18 shows the plot for distortion as a function of output level. Fig.5.19 shows the photo of the spectrum analysis of the output for this distortion measurement.

5.7.2.6. Power Supply Dependence.

The static effects of power supply variations (±20%) were evaluated in the filter transfer function and the result proved that they are negligible. Minimum supply voltage for reliable operation was around $8V$.

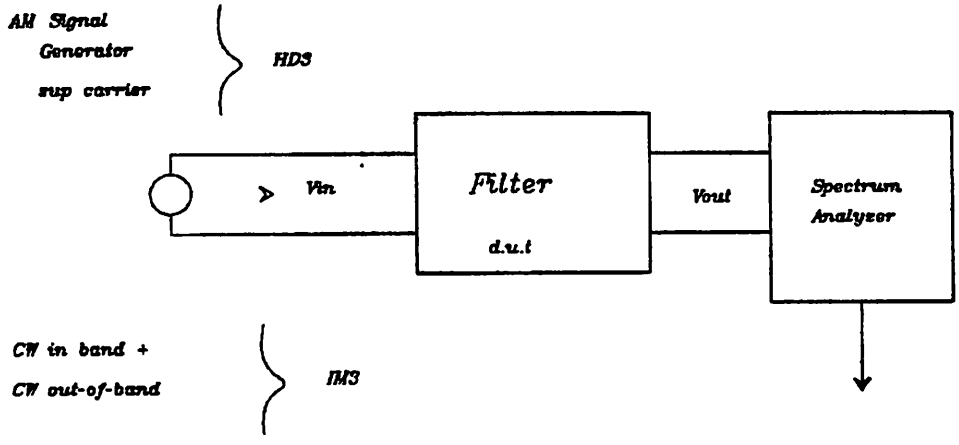


Fig.5.16 Filter Distortion Measurements

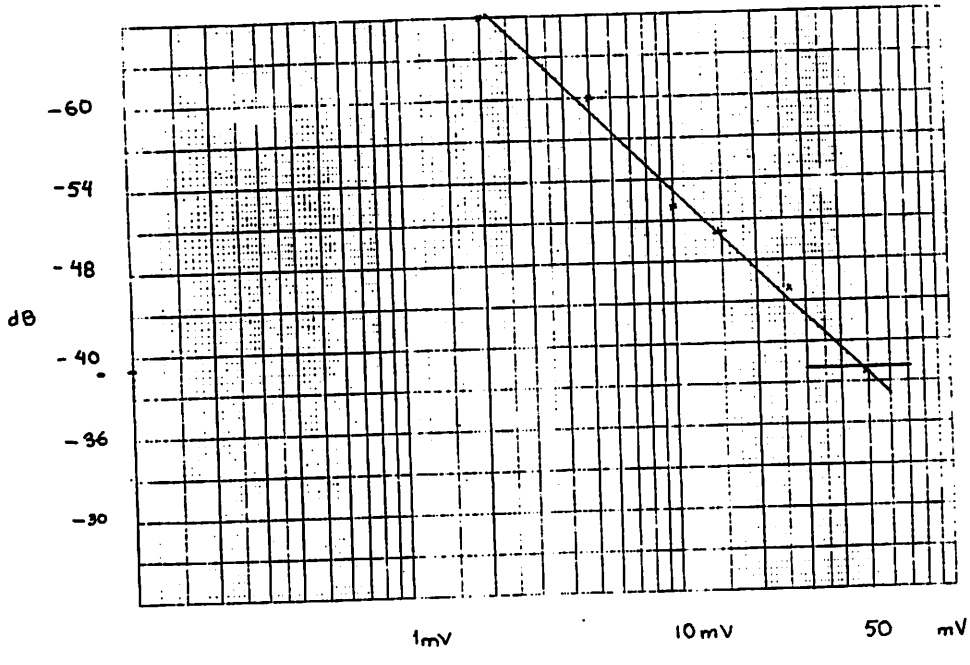


Fig.5.17 Third Harmonic Distortion vs. Signal Level

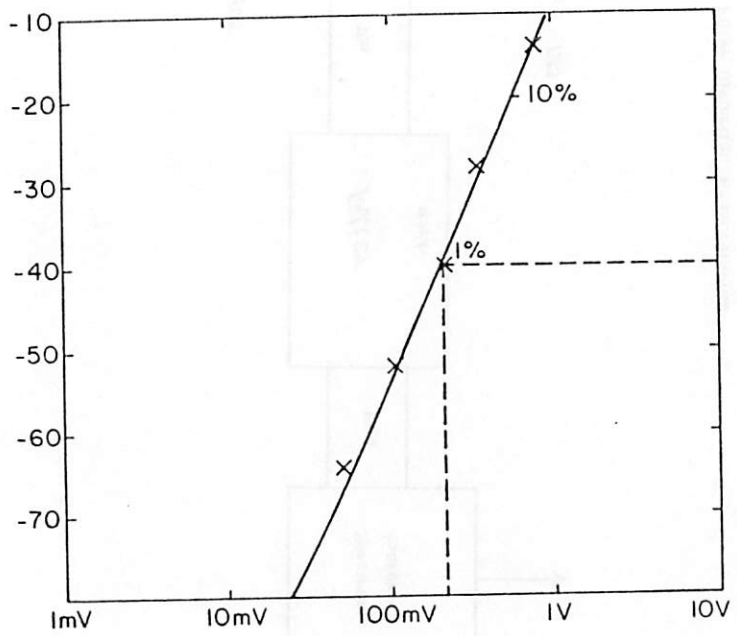


Fig.5.18 Distortion vs. Output Level

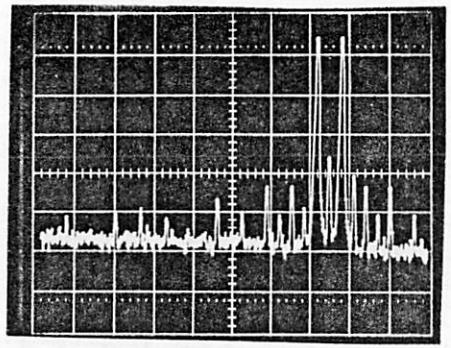


Fig.5.19 Spectrum Output showing Distortion Components

Horizontal 1 kHz / div

Vertical 6 dB/div

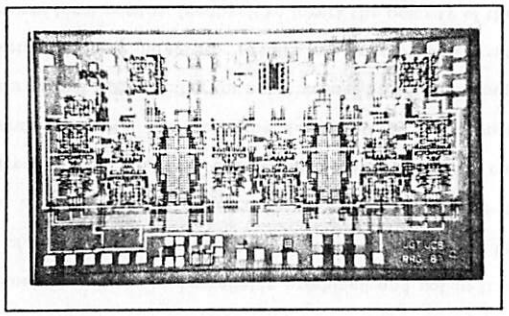


Fig.5.20 Die Photo for the Prototype Filter

NMOS Sixth Order High Frequency
Switched Capacitor Filter

5.7.2.7. Noise measurements.

The filters noise was measured with a low noise scope by the conventional transversal method [80]. The total filter in-band noise measured was $260\mu V$ which is then referred to the input by division by the filter passband gain. This noise determines the minimum detectable signal for the filters. With this and the maximum signal obtained from the distortion analysis a dynamic range of $60dB$ is computed.

The present circuit showed a low dynamic range which limits the range of applications. The transfer function distortion, in terms of passband ripple , limits the circuit operation to a maximum center frequency of $100kHz$. It is believed that new circuit configurations can be developed to increase the maximum output swing and reduce the noise leading to improvements of the order of 20 dB. A die photo of the NMOS chip, including test devices, is shown in Fig.5.20. The capacitor banks and resonator circuits are easily identified.

5.8. Summary

This chapter has presented the issues encountered in high-frequency narrow-band SC filter design. Although some theoretical concepts are added for completeness, CAD tools were used in the final design resulting in faster turnaround. The layout procedures were discussed and the technology fabrication process introduced.

CHAPTER 6

CONCLUSIONS AND FURTHER RESEARCH

A new circuit approach which uses parameter matching properties of IC's to provide an accurate loss cancellation to an active resonator circuit has been presented. Implementation of narrow-band filters with Q only limited by the amount of matching that can be reliable produced and not in the absolute dc gain value of the amplifiers is obtained. The loss cancellation technique has applications in many high frequency circuit where the amplifier finite DC gain has undesired effects, e.g., fast differential sample and hold circuits, serial charge balance A / D, etc. The technique is based in the development of a active SC integrator circuit with an inherent negative loss which when coupled together with a conventional lossy integrator results in a very low loss resonator circuit. The circuit uses local positive feedback to invert the polarity of the circuit gain at DC . The circuit implementation involves circuit which is conditionally unstable and is stabilized in large signal by the closed loop configuration used.

A sixth order elliptic switched capacitor filter was fabricated in NMOS to demonstrate the technique. Experimental results for the prototype filter were presented giving a $100KHz$ center frequency and Q factor of 20 accurate within 5%. The circuit fabricated presents applications for filtering functions in the range of $100kHz$ with moderate dynamic range $60dBi$, e.g., in mobile radio communication receivers, pilot carrier receivers and timing recovery circuits. The technique can also be used in lowpass and highpass ladder filter implementations where the finite gain limitation is a problem . Since the cancellation is done by overcompensation of one integrator in a pair, the method is more consistent with the even order filters thus it applies naturally well to symmetric filters such as lattice and matched filters.

Further work in the line of negative loss circuits can be directed towards the design of higher output swing (Dynamic Range) and low power dissipation circuits and in the development of techniques to improve the matching of amplifier DC gain to be able to resolve very high quality resonators. Further investigation of non-minimum phase circuits with negative loss characteristics is attractive. It is believed that much lower intermodulation distortion can be obtained from such implementation.

The technique does not only applies to NMOS but it can in practice be utilized in other technologies. Further investigation of the implementation of negative loss circuits in CMOS is a good extension of the present work.

An interesting result is that the negative loss circuit gives unique characteristics that can eventually be used in applications where the circuit stands alone , e.g., low distortion circuits .

APPENDIX A

SMALL SIGNAL FREQUENCY DOMAIN ANALYSIS

The analysis start with some assumptions regarding the directionality of the circuit characteristics. A unilateral circuit is defined as have a dominant forward transfer characteristics and a negligible backward transfer function. In that case the system can be analyzed by signal flow graphs (SFG) or block-diagram methods and a whole set of powerful design tools can be applied. Unilateral systems have an alternative representation in a matrix form where the matrix elements are related to the direction of the signal flow, [68]. The real amplifier circuits have feedforward transfer and they are characterized as bilateral systems. Techniques developed for unilateral systems can be applied after linear transformations modify the system equations in a unilateral form.

The simple inverter amplifier is presented first. Kirschoff current law applied to the nodes V_1 and V_o in the circuit gives the following:

$$\begin{array}{lll} (gs + sC_{in} + sC_{gd})V_1 & -sC_{gd}V_o & = gsV_i \\ (-sC_{gd} - g_m)V_1 & (g_l + sC_l + sC_{gd})V_o & = 0 \end{array} \qquad \text{(a1.1)}$$

The block diagram of the unilateral form of the system is shown in Fig.a1.1. Two forward gain block are given by:

$$\frac{V_o}{V_1} = \frac{sC_{gd} - g_m}{g_l + s(C_l + C_{gd})} \qquad \text{(a1.2)}$$

and:

$$\frac{V_x}{V_i} = \frac{g_s}{g_s + s(C_{in} + C_{gd})} \qquad \text{(a1.3)}$$

The feedback block is given by

$$\frac{V_y}{V_o} = \frac{sC_{gd}}{g_s + s(C_{in} + C_{gd})} \qquad \text{(a1.4)}$$

where V_x and V_y are dummy variables :

$$V_1 = V_x + V_y \qquad \text{(a1.5)}$$

The root locus can be obtained easily from the loop gain from equations (2) and (4). Arranging the characteristic equation the root locus in terms of Cgd is obtained as shown in Fig.a1.2 showing the pole splitting result.

The configuration of interest for SC circuits replaces the input conductance gs by a susceptance sC_u. The equations are obtained in the same form as above:

$$\frac{V_o}{V_1} = \frac{sC_{gd} - g_m}{g_l + s(C_l + C_{gd})} \qquad \text{(a1.6)}$$

$$\frac{V_x}{V_i} = \frac{sC_{gd}}{sC_s + s(C_{in} + C_{gd})} \qquad \text{(a1.7)}$$

The feedback block is given by:

$$\frac{V_y}{V_o} = \frac{sC_{gd}}{sC_s + s(C_{in} + C_{gd})} \qquad \text{(a1.8)}$$

The simple change in the equations has a essential effect in the root locus; the real axis root locus branches are reversed and a loop function zero appears on the RHP. The root locus is depicted in Fig.a1.3.

The cascode load amplifier showed in Fig.4.3 In order to reduce the complexity of the analysis some simplifications have been done, i.e., feedforward due to the drain to gate capacitance of the driver devices is neglected. The system of equations are transformed to a unilateral system. Kirschoff current law applied to the nodes in the circuit gives the following:

$$\begin{array}{lll} (sC_u + sC_f)V_1 & -sC_{gd}V_3 & = sC_uV_i \\ (-sC_{gd} + g_m)V_1 & (+g_3 + sC_3 + sC_{gd} + g_{m3})V_3 & = 0 \\ -C_fV_1 & +(sC_f + g_5 + sC_5)V_5 & = 0 \end{array} \qquad \text{(a1.9)}$$

The feedforward transfer functions are:

$$\frac{V_o}{V_i} = \frac{sC_f Y3 - g_{m1}g_{m5}}{(\alpha Y3 + Y5)} \qquad \text{(a1.10a)}$$

where :

$$Y3 = g_3 + sC_3 \; ; \quad Y5 = g_5 + s(C_5 + C_f) \qquad \text{(a1.10b)}$$

and:

$$\frac{V_x}{V_i} = \alpha = \frac{sC_u}{s(C_u + C_f)} \qquad \text{(a1.11)}$$

$$\frac{V_y}{V_o} = \beta = \frac{sC_f}{s(C_u + C_f)} \qquad \text{(a1.12)}$$

The system is transformed to the unilateral system in Fig.a1.4. The closed loop equation is obtained from Mason's rule:

$$\frac{V_{o(s)}}{V_{i(s)}} = \frac{s^2C_fC_3 + sC_fg_3 - g_{m1}g_{m5}\alpha}{s^2C_3C_5 + s(C_3g_5 + C_5g_3) + g_{m1}g_{m5}\beta + g_3g_5} \qquad \text{(a1.13a)}$$

The system has two zeroes and two poles which are approximately located as follows :

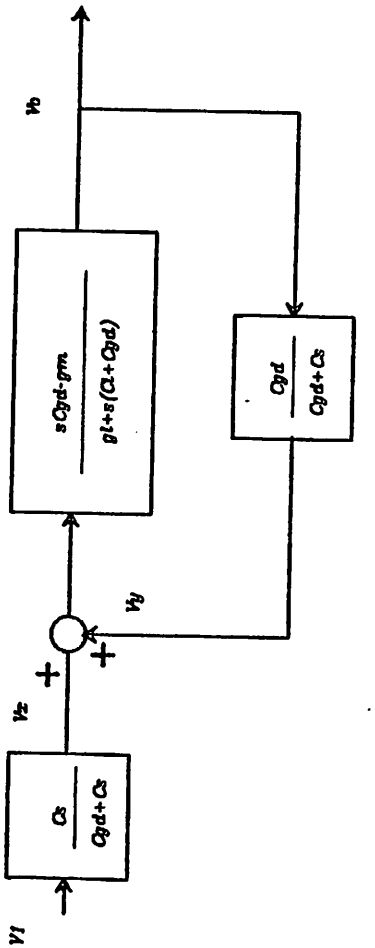
$$\zeta_1 = + \frac{g_3}{C_3} \qquad \text{(a1.13b)}$$

$$\zeta_2 = \frac{-g_{m1}g_{m5}}{g_3C_f} \qquad \text{(a1.13c)}$$

$$\omega_1 = \frac{-g_{m5}\alpha_o}{C_5} \qquad \text{(a1.13d)}$$

$$\omega_2 = -\left(\frac{g_3}{C_3} + \frac{g_5}{C_5}\right) \qquad \text{(a1.13e)}$$

The root locus as a function of C_f is depicted in Fig.a1.5



Figa1.1 Single Stage Block Diagram

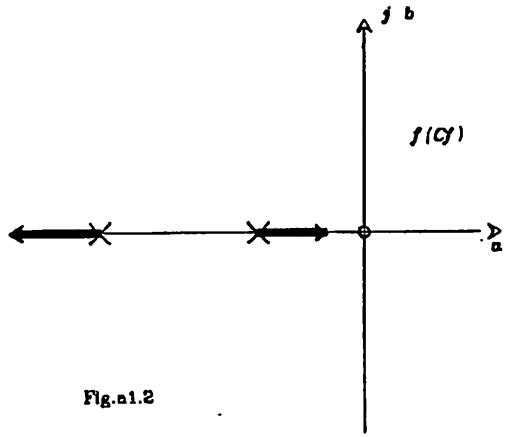


Fig.a1.2

Root Locus for Integrator

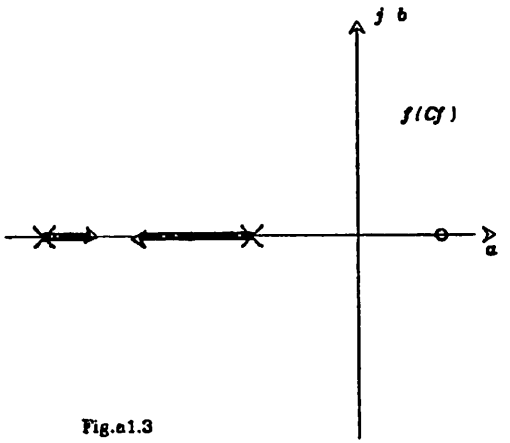


Fig.a1.3

Simple Amp with Charge Feedback

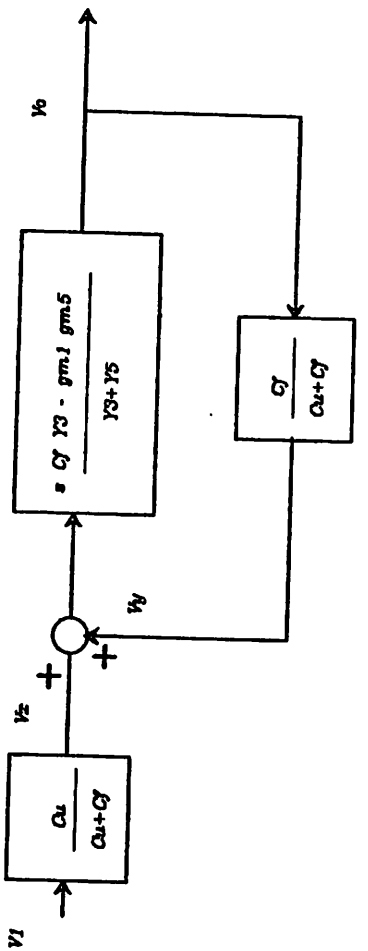


Fig.a1.4 Cacode Load Closed Loop Block Diagram

APPENDIX B

AMPLIFIERS FINITE SPEED EFFECT IN SC FILTERS

This dissertation has presented a method to compensate the finite amplifier gain effect in SC filters. The final goal however is to extend the application of SC filters to higher frequencies. In Chap.4 the settling characteristics of the amplifiers were discussed and in particular it was concluded that a single pole model for the amplifier can by employed for the single stage amplifiers presented. This appendix derives the effects of the amplifier finite bandwidth limitations assuming the amplifier speed is determined by a single pole roll-off with a unity gain frequency ω_u.

$$a(s) = \frac{V_o(s)}{V_i(s)} = -\frac{\omega_u}{s + \frac{\omega_u}{a_o}} \tag{b.1}$$

In the single roll-off situation, the rise time is determined by the unity gain frequency and the amplifier settling is also strongly dominated by this value for the single stage amplifier, i.e., during the settling process, the effect of the high frequency poles has died out and the low frequency time constants determine the response. For this analysis we assume that the closed loop pole is mainly determined by the feedback and the effect of a_o is neglected:

$$a(s) = \frac{V_o(s)}{V_i}(s) \approx -\frac{\omega_u}{s} \tag{b.2a}$$

This simple relation represents the following time domain expression:

$$\frac{dV_o(t)}{dt} = -\omega_u V_i(t) \tag{b.2b}$$

In the sampled data implementation, the amplifier speed i.e. pulse response settling, will define what is the allowable clock rate and the maximum filter frequency.

The inverting SC integrator (Fig.b1) is analyzed in both clock phases , viz, charge transfer phase $\Phi 1$ $(n - \frac{1}{2}, n)$ and reset phase $\Phi 2$ $(n - 1), (n - \frac{1}{2})$. During $\Phi 1$ the charge transfer process is obtained by charge conservation as:

$$C_f V_o(t) - C_f V_o(n - \tfrac{1}{2}) = (C_u + C_f)\left[V_i(t) - V_i(n - \tfrac{1}{2})\right] \tag{b.3}$$

where $V_o(t)$ is the output voltage within the clock phase and $V_o(n - 1/2)$ is the initial conditions for the charge at that node. The same reasoning applies for the voltage at the amplifier input V_i At the clock transition there is an instantaneous charge sharing between the capacitors, (assume C_u is reset).

$$V_i(n - 1/2) + = \frac{C_f}{C_u + C_f} V_i(n - 1/2) - + V_{in}(n - 1/2)\frac{C_u}{C_f + C_u} \tag{b.4a}$$

In the sampling used in the prototype circuit the input signal is held constant:

$$V_{in}(n - 1/2) = V_{in}(n) \tag{b.4b}$$

Charge flow is expressed by time derivative of (a1.3) as:

$$\frac{dV_o(t)}{dt} = \frac{C_u + C_f}{C_f}\ \frac{dV_i(t)}{dt} \tag{b.5}$$

From (5) and (2b) the we solve for $V_i(t)$:

$$V_i(t) = Me^{\frac{-t}{K}} \tag{b.6}$$

where $K = \omega_u \frac{C_f}{C_u + C_f}$ and M is the initial conditions $V_i(n - 1/2)$. At the end of the clock phase we have:

$$V_1(n) = Me^{\frac{-T}{2R}} = V_1(n - 1/2)\, a_1 \qquad (b.7)$$

From this equation and (1.3), the output voltage is:

$$V_o(n) = V_o\left(n - \frac{1}{2}\right) + \frac{(C_u + C_f)}{C_f}\left[V_1(n - 1/2)\, a_1 - V_1\left(n - \frac{1}{2}\right)\right] \qquad (b.8)$$

The analysis on $\phi 2$ is performed to obtain the values of V_1 necessary in (8) in terms of the input voltage.

The value of the input and output during the $\phi 2$ is determined by the amplifier response as:

$$\frac{dV_o(t)}{dt} = -\omega_u V_1(t) \qquad (b.9)$$

with initial conditions the input voltage at the previous sampling $V_{in}(n - 1)$ The solution in the same form as before leads:

$$V_1(n-1/2)- = V_1(n-1)e^{-T\frac{\omega_u}{2}} \qquad (b.10a)$$

$$V_1(n-1/2)- = V_1(n-1)\, a_2 \qquad (b.10b)$$

Substituting this result back into the instantaneous transition (4a) we obtain:

$$V_1(n - 1/2)+ = \frac{C_f}{C_u + C_f} V_1(n - 1)\, a_2 + \frac{C_u}{C_f + C_u} V_{in}(n - 1/2) \qquad (b.10c)$$

and the output voltage has the same form as (8):

$$V_o(n-1/2) = V_o(n - 1) + \left[1 - a_2\right] V_1(n - 1) \qquad (b.11)$$

From (11) into (8):

$$V_o(n) = V_o\left(n - \frac{1}{2}\right) + V_1(n - 1)(a_1 - a_1 a_2) + (1 - a_1)\frac{C_u}{C_f} V_{in}(n - 1/2) \qquad (b.12)$$

and from (4a) into (12)

$$V_o(n) = V_o(n - 1) + V_1(n - 1)(1 - a_1 a_2) + (1 - a_1)\frac{C_u}{C_f} V_{in}(n - 1/2) \qquad (b.13)$$

For the amplifier input V_1 in (1.7):

$$V_1(n) = \frac{C_f}{C_u + C_f} V_1(n - 1) a_1 a_2 + \frac{C_u}{C_f + C_u} V_{in}(n - 1/2)\, a_1 \qquad (b.14)$$

Z transforms:

The Z transforms for (13) and (14) is easily obtained. To facilitate the presentation the following constants are defined:

$$\begin{aligned} p_1 &= \frac{C_u}{C_u + C_f} a_1 \\ p_2 &= (1 - a_1)\frac{C_u}{C_f} \\ p_3 &= (1 - a_1 a_2) \\ p_{12} &= \frac{C_f}{C_u + C_f} a_1 a_2 \end{aligned} \qquad (b.15)$$

$$V_o(1 - z^{-1}) = -p_2 V_{in} - p_3 V_1 z^{-1} \qquad (b.16)$$

$$V_1(1 - p_{12} z^{-1}) = -p_1 V_{in} \qquad (b.17)$$

(16) in (15):

$$V_o(1 - z^{-1}) = \frac{\left[-p_1 p_3 z^{-1} - p_2\right] V_{in}}{1 - p_1 p_2 z^{-1}} \qquad (b.18)$$

The results can be given in terms of the root locations on thee z domain. The integrator has a LHP zero inside the unit circle which gives a Q reduction effect similar to the finite gain effect Fig.b2. From this analysis, the frequency domain results can be obtained in the form of an integrator magnitude and error phase [4]. The magnitude error or loss is given by:

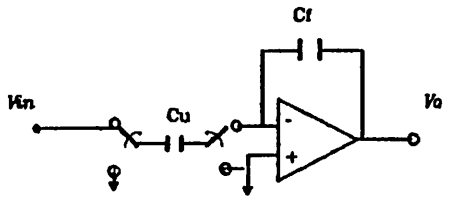
$$\frac{1}{q_{ei}} = -e^{-k}\left[-\frac{C_u}{C_f + C_u}\sin\omega T\right] \qquad (b.19)$$

where:

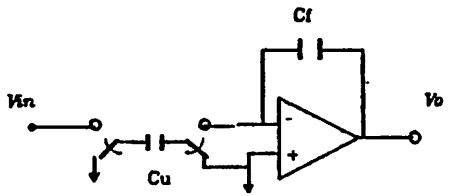
$$k = \pi \left(\frac{C_F}{C_F + C_u} \right) \beta \qquad \text{(b.20)}$$

Evaluated at the integrator corner frequency ω_o. The relation between the gain and speed limitation errors and the amp crossover frequency are exponentially related as indicated by (4). Whereas the typical continuous time filter has a linear relationship.

Equations (18, 19) give the SC integrator error effect due to the finite amplifier speed , from this, the fundamental relationship between the maximum sampling rate and a given amplifier speed is obtained. From these results we can establish the clock period range where the amp gain effect dominates the filter response and when the speed limitations begin to be important.

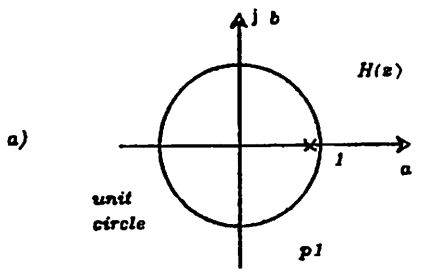


a) Phase 1 (Sampling Phase)

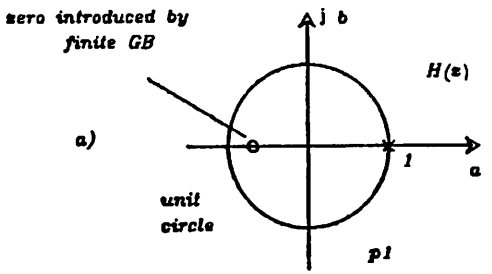


b) Phase 2 (Refresh Phase)

Fig.b1 SC Integrator on each clock phase



Finite Gain Effect



Finite GB effects

Fig.b2 Pole zero map for the SC integrator

APPENDIX C

DERIVATION OF THE NEGATIVE-LOSS SYSTEM NON-LINEAR EQUATION

The analysis uses the Kirchoff current law at the nodes of the fully differential amplifier. The nodes are numbered as in the schematics in Chap.3. The controlled nonlinear functions are voltage controlled current sources, e.g., $i_{oc} = f(V3, V6, V_b)$ indicates the current output for device 5 controlled in its input (V_{gs}) by voltages $V_b - V_3$ and the output current is modulated by the voltage V_b through the finite output impedance. The open loop equations below are for the nodes 3, 4, 5 and 6 where driving is done by voltage signal V_a and V_b:

$$\begin{aligned} V_3C_3 &= V_{33}g_3\, f(V3,V5,V_b) - f(V_a) + K \\ V_5C_5 &= V_{55}g_5\, f(V3,V5,V_b) \quad V_{dd}g_5 \\ V_4C_4 &= V_{44}g_4\, f(V4,V5,V_b) - f(V_b) + K \\ V_6C_6 &= V_{66}g_6\, f(V4,V5,V_b) \quad V_{dd}g_6 \end{aligned} \tag{c.1}$$

where V_a and V_b are the input voltage drive and V_N are the node voltages.

The system can be simplified by neglecting the finite output dependence of the NMOS transistors which is realistic for the present case. The resultant equations are written in Chap.3.

The closed loop system uses the schematic of Chap.3 and results in a sixth order system of nonlinear equations. The Kirchoff current law at the nodes 1, 2, 3, 4, 5 and 6 gives:

$$\begin{aligned} V_aC_{i1} + V_1(C_f - C_{i1} + C_a) - V_5C_f &= 0 \\ V_bC_{i2} &= 0 \\ V_3C_3 + V_2(C_f - C_{i2} + C_a) - V_6C_f &= -f(V_3 - V_6) - f(V_a) + V_{33}g_3 + k_3 \end{aligned} \tag{c.2}$$

$$\begin{aligned} \dot{V}_4 C_4 &= -f(V_4 - V_5) - f(V_4) + V_5 g_5 + k_5 \\ \dot{V}_5 C_5 &= -f(V_4 - V_5) - V_5 g_5 + k_5 \\ \dot{V}_6 C_6 &= -f(V_3 - V_6) - V_6 g_6 + k_6 \end{aligned}$$

where V_a and V_b are the system inputs and k_5 and k_6 are bias constants.

The system solution was obtained with computer simulation as indicated in Chap.3. The results proved to be similar to the classical nonlinear bistable system which is stabilized by feedback. The classical bistable system has the following form:

$$\begin{aligned} \dot{x}_1 &= x_2 \\ \dot{x}_2 &= -x_1(x_1^2 - 1) - \alpha x_2 \end{aligned} \qquad \text{(c.3)}$$

The equilibrium points are the solutions of the $\dot{x}_2 = 0$: $e_{-1} = -1$, $e_0 = 0$, $e_1 = 1$. The characteristics of the system are obtained by linearizing the system equation around the equilibrium points. The open loop circuit analysis indicates that the system has two stable equilibrium points at -1,1 and a unstable point at 0. The open loop presents the typical bi-stable system response. The characteristic equation for each linearized system determines the type of singularity around it.

The closed loop system shows a memory less nonlinearity modeled as follows: to give:

$$\dot{x}_1 = x_2 \qquad \text{(c.4)}$$

$$\dot{x}_2 = -x_1 - \alpha x_2 + v(t) \; ; \text{for} |x_1| < M$$

$$\dot{x}_2 = -K + v(t) \; ; \text{for} |x_1| \geq M$$

The phase plane portrait for the system is presented in Chap.3.

APPENDIX D

NMOS SILICON GATE PROCESS

A. Cleaning the Wafers

1.TCE 60° C 10 min.
2.Acetone room temp. 2 min.
3.Methyl alcohol forced jet while spinning
4.DI H_2O rinse, N_2 blow dry.
5.Piranha (H_2O : H_2SO_4—1:5) 5 min.
6.DI, blow dry
7.Dip in HF : H_2O—1 : 5 30 sec.
8.DI, blow dry

B.Thin Oxide Growth (TEMP = 1025° C)

1.Push O_2 (dry) 6.5cm 3 min.
2.Oxidation O_2 (dry) 6.5cm 52 min.
3.Anneal N_2 4.0cm 15 min.
4.Pull N_2 4.0cm 3 min.

C.Active Area Definition

1.Deposition Si_3N_4 1000 A
2.Photolithography mask 1
Standard Photolithography Positive Resist AZ 1350 Shipley
90° prebake 15 min.
110° C postbake 15 min.

3.Nitride Surface Oxide Removal HF : H_2O—1 : 10 10 sec, DI, N_2.
4.Plasma Etch Nitride
5.Field Implant Boron, 70 KeV, $2.5\times10^{13} cm^{-2}$
6.Strip Photoresist acetone / piranha ; DI, blow dry

D.Local Field Oxidation

1.Piranha
2.DI, blow dry
3.Field Oxidation Push O_2 (dry) 6.5 cm 3 min 950° C.
4.O_2 (dry) 6.5 cm 10 min 1000° C.
5.Stand by N_2 4.0 cm
6.Wet O_2 2.0 cm 700 min. 920° C.
7.Anneal N_2 4.0 cm 15 min. 920° C.
8.Pull N_2 4.0 cm 3 min. 920° C.

E.Capacitor Bottom Plate

1.Plasma etch Si_3N_4.

2.Remove thin Ox $HF : H_2O$—1 : 10 2 min hydrophobic
3.DI, blow dry
4.Capacitor mask 2
5.Bottom plate implant As 120 KeV $1.2\times10^{14}\ cm^{-2}$
6.Plasma etch photo-resist.
7.Piranha 5 min.
8.DI, blow dry

F. Depletion Implant

1.Depletion Load Mask 3
2.Depletion implant As 120 KeV $1.2\times10^{12}\ cm^{-2}$
Noise Compensated
3.Plasma etch photo-resist.
4.Piranha 5 min.
5.DI, blow dry

G.Gate Oxide Growth

1.Re-gate (1025° C)
a.Push O_2 (dry) 6.5 cm 3 min
b.Oxidize O_2 (dry) 6.5 cm 55 min.
c.Anneal N_2 4.0 cm 15 min.
d.Pull N_2 4.0 cm 3 min.

H.Threshold Adjustment

1.Enhancement Photolithography Mask 3
2.V_{TE} implant Boron. 50 KeV 4×10^{11}
noise compensation
3.Strip Photoresist in acetone 5 minutes.
4 .Piranha 5 min.
5.DI, N_2.

I.Self Alligned Gate Definition

1.Oxide dip in $HF : H_2O$—1 : 10 5~10 sec.
2.DI, blow or spin dry
3.Bake under IR lamp 10 min.
4.Poly Silicon deposition (5000 A).
5.Poly dope in N-predep furnace.
a.Push N_2 6.0 cm 3 min.
b.N_2—O_2 5.0 cm / 2.5 cm 5 min.
c.Dope N_2—O_2—$POCl_3$
5.0 cm/2.5 cm 6.0 cm. 30 min to 40 min .
d.N_2—O_2 6.0 cm / 2.5 cm 2 min.
e.N_2 5.0 cm 5 min.
f.Pull N_2 5.0 cm. 3 min.
6.Oxide dip in $HF : H_2O$—1 : 5 30 sec.
7.DI, N_2.
8.Dry IR .

9.Gate mask Definition
10.Plasma etch poly
11.Etch backside oxide completely with BHF.
12.DI,blow dry
13.Strip photoresist in acetone 5 min.
14.DI,blow dry
15.Piranha
16.DI,blow dry
17.IR dry

J.Source and Drain Definition

1.S/D implant As 200 KeV $3.5\times10^{15}\ cm^{-2}$
2.Backside implant BF_2 150 KeV $1\times10^{15}\ cm^{-2}$.
3.Piranha
4.DI,blow dry

K.Glass Deposition

1.Spin-on glass 3000 rmp, 30 sec.
2.Cure at 900° C for 10 min.
3.Repeat 1 and 2 to grow 7200 A at 1200 A per layer
4.Final cure at 900° C for 30 min.

L.Contact Plugs and Metallization

1.Contact mask 6
2.Etch contact oxide in BHF (2%) 7min
3.DI, blow dry
4.Deposit 1000 A of poly
5.Evaporate Aluminum (8000 A)
6.Metal mask 7
7.Etch Al ,
8.Plasma etch polysilicon plug layer .
9.DI, blow dry
10.Etch back side oxide with BHF.
11.DI, blow dry
12.Strip photoresist in acetone 5 min.
13.DI, N_2.
14.Evaporate Al on the back side ~1 μm.
15.Sinter Al in sintering furnace at 300° C in forming gas 14 cm 5 min.

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