A SWITCHED-CAPACITOR SYNCHRONOUS DETECTOR

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Memorandum No. UCB/ERL M83/36

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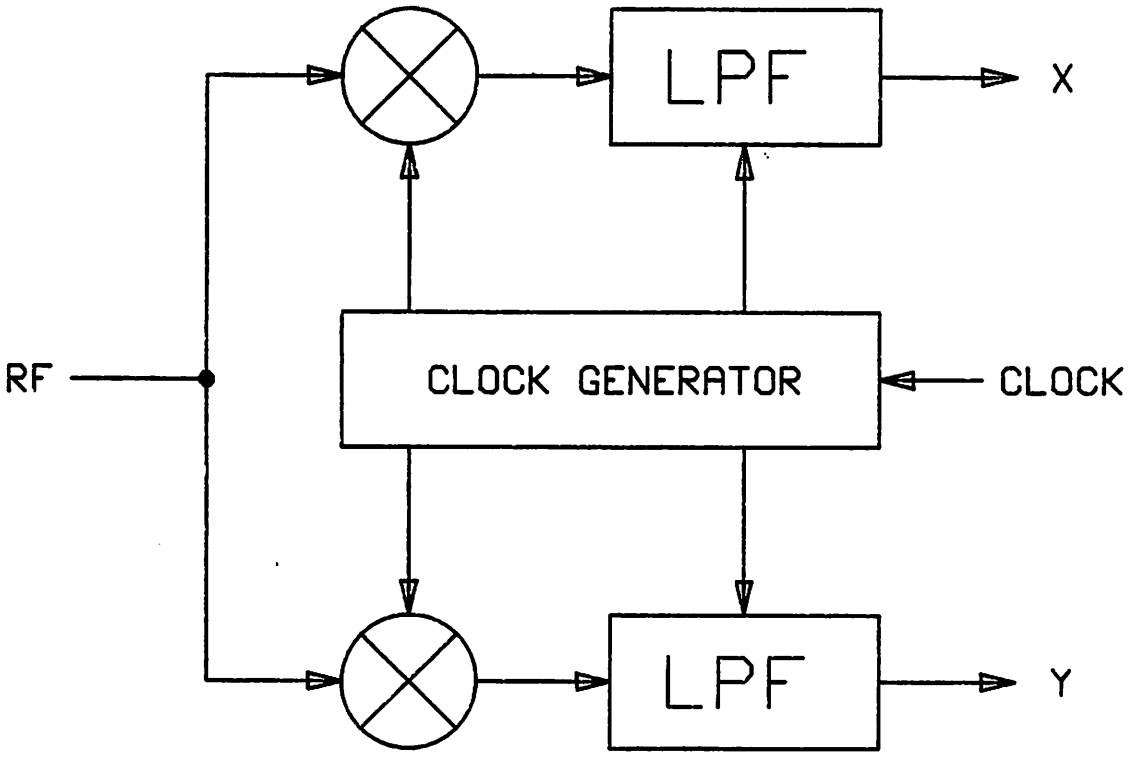

A SWITCHED-CAPACITOR SYNCHRONOUS DETECTOR

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Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of Master of Engineering.

ABSTRACT

This thesis reports on the design of a high performance switched-capacitor synchronous detector. In the process, it covers many error mechanisms and error reduction techniques that are useful in the design of high performance switched-capacitor circuits. In particular, distortion resulting from op amp, capacitor, and switch nonlinearities are covered in detail. The quadriphase clock scheme is introduced as a method for reducing gain and distortion errors created in the switch-capacitor system. Also presented in this thesis are noise reduction techniques and a CMOS low noise differential amplifier.

A switched-capacitor mixer is introduced that consists of several switched-capacitor resistors operating in parallel with interleaved clocks, which allows a sampling rate equal to the clock rate. In this example an 800kHz clock generates an eight point sinusoidal 100kHz LO signal. This mixer is used with a multiple clock rate filter, and these two form the heart of the detector. Included along with circuit descriptions are discussions of effects and modeling of distortion present in the mixer, and elimination of mixing products that alias into the output passband. This last feat is accomplished by using a new parasitic-insensitive bilinear integrator.

ACKNOWLEDGMENTS

I would like to acknowledge and thank the Network Measurements Division of Hewlett-Packard Company. Without their trust and support in the form of a fellowship and use of their excellent facilities and equipment, this project would have been much more painful. I would also like to acknowledge the contributions of Dr. Robert Meyer and Dr. Paul Gray, who helped guide this research; Geri Gmahling and Adrienne Graham, who typed the thesis; and Bruce Donecker and Nancy Bentley, whose thorough reading of the manuscript resulted in many clarifications and the addition of countless commas.

Lastly, I would like to dedicate this work to my parents. Through their love and guidance they have given me the strength and wisdom to progress this far in life. To them I owe all my success.

TABLE OF CONTENTS

Chapter 1
INTRODUCTION

This thesis reports on the design of a high performance switched-capacitor synchronous detector. In particular, distortion mechanisms and techniques to reduce distortion in both mixers and switched-capacitor circuits are covered in some depth. In addition several noise reduction techniques are discussed. No monolithic circuits were fabricated, so comments concerning monolithic error mechanisms must be considered somewhat speculative. A discrete version was built to obtain verification of as many of the concepts as possible. The overall topology and preformance of the circuit, and several results concerning distortion, were thus confirmed.

A specific application was in mind when this design was conceived. This detector was designed to be used in a network or impedance analyzer. Switched-capacitor technology was chosen to obtain a small, low cost, high performance solution that dissipated little power. Of the above, only high performance is not inherent in the technology. Since the output of the detector is processed digitally, it can be corrected for offset, gain, and quadrature errors. This leaves noise and distortion to be concerned with. Hsieh et al. have achieved good results in reducing noise to acceptable levels by combining several low-noise techniques. Though these techniques were used in this design, they will only be discussed lightly. See the excellent work already published in this area for more information [4][5][6].

This leaves distortion as the only remaining obstacle to achieving the required performance. The myriad of distortion mechanisms has not been well documented in the literature to date, and that is where most of the attention in this thesis will be focused. Both mechanisms discovered in the discrete

breadboard, and mechanisms thought to be important in monolithic switched-capacitor circuits will be covered.

1.1 Switched-Capacitor Concept

Switched-capacitor circuits emulate resistors using clocked switches and capacitors. They act as high quality replacements for monolithic resistors, which tend to be large as well as having poor linearity, stability, and accuracy. In contrast, capacitors have the highest linearity, stability, and accuracy of any component that is realizable in monolithic form. MOS capacitors even compare favorably to the best discrete components. Ratio accuracy can be as good as 0.1% to 0.01%. Switched-capacitor circuits can be synthesized where the transfer function is solely dependent on capacitor ratios and clock frequency. Consequently switched-capacitor circuits tend to be stable and well-behaved.

A resistor can be emulated by a clocked switch and capacitor by using the topology shown in figure 1.1. Initially the switch is in the left position so that the capacitor C is charged to voltage V_1. The switch is then thrown to the right and the capacitor is discharged to the voltage V_2. The amount of charge that flows into source V_2 is thus $q = C(V_1 - V_2)$. If the switch is thrown back and forth at a clock rate f_c, then the average current flow from V_1 into V_2 will be $C(V_1 - V_2)f_c$. The switched-capacitor circuit mimics a linear resistor in that the average current is proportional to the voltage across it. The size of this resistor is

$$R = \frac{1}{Cf_c} \tag{1.1}$$

In order for the switched or discrete-time nature of this circuit to be masked, the frequencies of interest passing through the resistor must be far less than the clock frequency.

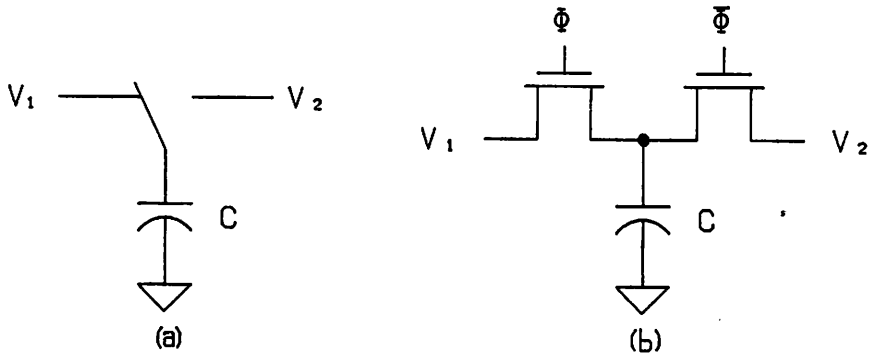

Figure 1.1: (a) An ideal switched-capacitor resistor. (b) A MOS implementation of (a).

Switched-capacitor filters are usually synthesized using integrators connected with feed-forward and feedback in state variable or leap-frog approaches. A simple integrator is shown in figure 1.2. The transfer function for a conventional RC integrator is $A_V = -1/RC_F s$. The transfer function of the switched-capacitor integrator is then

$$A_V = -\frac{C_I f_c}{C_F s} \tag{1.2}$$

Notice that it is solely a function of the ratio of C_I to C_F and the clock frequency f_c. This integrator topology suffers from two problems. First, it is sensitive to parasitic capacitance on the top plate of the capacitor. Second, it does not have differential inputs, a requirement in most filter designs. These problems are rectified in figure 1.3.

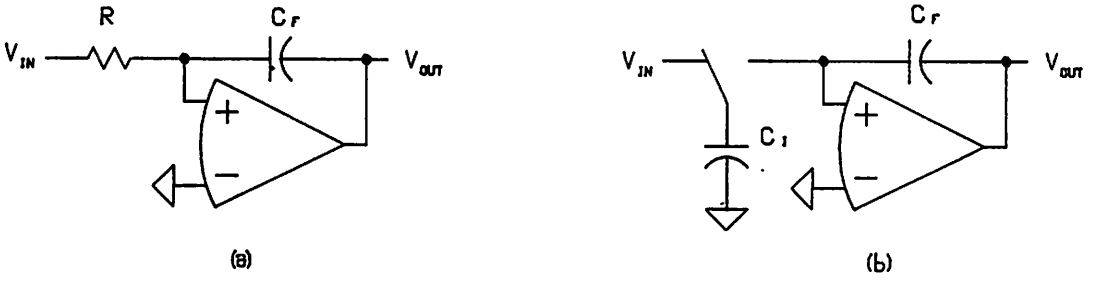

Figure 1.2: (a) Conventional RC integrator. (b) Switched-capacitor integrator.

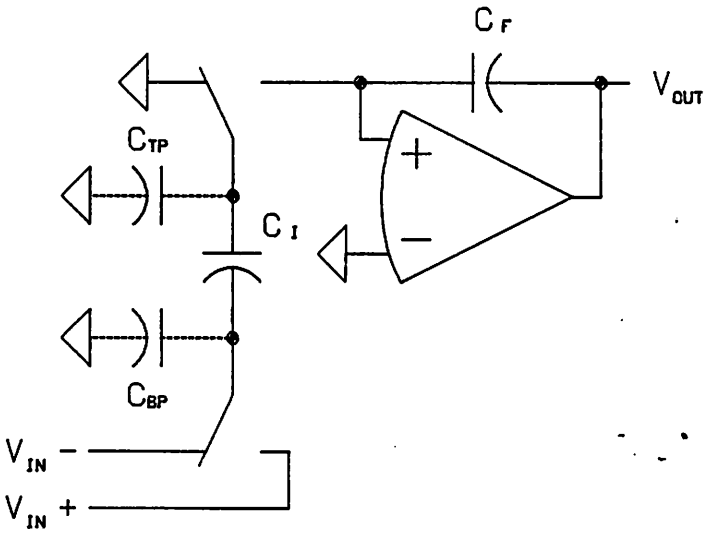

Figure 1.3: Parasitic-insensitive differential switched-capacitor integrator.

Any parasitic capacitance attached to the top plate of C_I (straight plate) has no effect because the top plate voltage is always zero. Any bottom plate (curved plate) parasitic has no effect because it is always driven by a voltage source and any charge from this capacitor will always flow to the voltage sources rather than C_I. The transfer function for this circuit is

$$V_{OUT} = \frac{C_I f_c}{C_{FS}}(V_{IN+} - V_{IN-}) \tag{1.3}$$

This was a brief introduction to the workings of switched-capacitor circuits. For a more complete coverage of this topic, see the tutorial article by Broderson et al. [1] or the book of reprinted articles by the same authors [2].

Chapter 2
SYNCHRONOUS DETECTION

The function of a synchronous detector in a network or impedance analyzer is to measure the amplitude and phase of a sine wave. Measurement of phase is with respect to a reference signal of the same frequency. For this application the frequencies of both the input and reference signals are fixed at 100kHz. For historical reasons the input signal will be called the RF (radio frequency) signal and the reference signal will be called the LO (local oscillator) signal. This is superheterodyne receiver jargon that is common terminology for mixers.

2.1 A Mathematically Ideal Detector

It is difficult to accurately measure magnitude and phase directly from the RF and LO signals (i.e., using a phase and a magnitude detector). It is also undesirable for two reasons. The first is that phase detectors have an inherent discontinuity between 180° and -180°. This usually causes problems in any mathematic processing that follows the detectors. For example, if phase is used to calculate group delay through a network, it will cause large errors at the phase discontinuity. The second reason is that once the magnitude of the signal is taken, it is no longer possible to drive down the noise floor with post-detection averaging. This can be seen if it is supposed that a zero input signal is measured that is contaminated with 100μV of noise. If the magnitude of this signal is calculated, and the average is taken, the result will be a stable 100μV. The result can never be the desired zero volts if there is any noise present. If instead, the cartesian equivalent of the polar magnitude and phase is measured, the time average of both x and y signals will go to zero. Now if x and y are converted to magnitude digitally, the magnitude will go to zero as desired. The actual

magnitude will not be identically zero unless x and y are averaged for an infinite number of samples. Averaging reduces the noise floor by a factor of $\sqrt{n}$ where n is the number of samples used in the average. Averaging over 100 samples will decrease the noise floor by 20 dB.

A synchronous detector does not generate magnitude and phase directly, but rather the cartesian equivalent. If phasor terminology is used, then the detector is said to produce the real and imaginary portions of the phasor. The relationship between the desired polar output and the actual cartesian output is

$$x = \mathrm{Re}\{A\, e^{j\vartheta}\} = A\cos\vartheta = \text{real portion}\dagger \tag{2.1a}$$

$$y = \mathrm{Im}\{A\, e^{j\vartheta}\} = A\sin\vartheta = \text{imaginary portion} \tag{2.1b}$$

$$A = \sqrt{x^2+y^2} = \text{magnitude} \tag{2.2a}$$

$$\vartheta = \tan^{-1}\frac{y}{x} + \mathrm{sgn}(y)[1-\mathrm{sgn}(x)]\pi = \text{phase} \tag{2.2b}$$

$$\text{where} \quad \mathrm{sgn}(z) = \begin{cases} 1 & \text{if } z \geq 0 \\ -1 & \text{if } z < 0 \end{cases}$$

The detector outputs x and y and equation 2.2a and 2.2b are used in the post processor to calculate magnitude and phase.

A block diagram of a synchronous detector is shown in figure 2.1. It is based on the following trigonometric identities:

$$\cos\alpha\cos\beta = \tfrac{1}{2}[\cos(\alpha+\beta)+\cos(\alpha-\beta)] \tag{2.3a}$$

$$\cos\alpha\sin\beta = \tfrac{1}{2}[\sin(\alpha+\beta)-\sin(\alpha-\beta)] \tag{2.3b}$$

† Phase is represented by ϑ, which is pronounced theta.

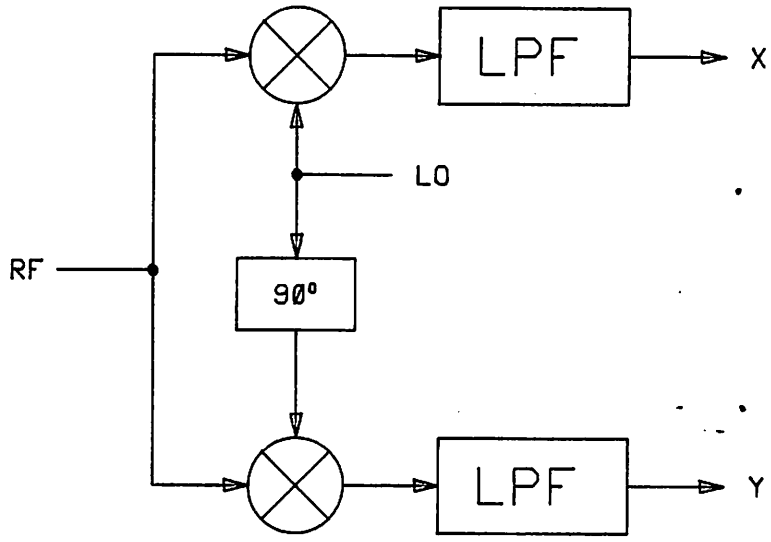

Figure 2.1: Synchronous detector block diagram.

These equations show that multiplying two sine waves together generates two more sine waves, one each at the sum and difference frequencies of the input sine waves. Another important result of these equations is that phase is conserved between input and output. This can be seen more clearly by setting $\alpha=\omega t+\vartheta$ and $\beta=\omega t$, where $\omega=2\pi 100\text{kHz}$. The following signals then appear at the output of the mixers.

$$A\cos(\omega t+\vartheta)\cos\omega t = \tfrac{1}{2}A[\cos(2\omega t+\vartheta)+\cos\vartheta] \tag{2.4a}$$

$$A\cos(\omega t+\vartheta)\sin\omega t = \tfrac{1}{2}A[\sin(2\omega t+\vartheta)-\sin\vartheta] \tag{2.4b}$$

Notice that both signals have components at D.C. and 200kHz. Also notice that the D.C. components are close to the desired cartesian outputs. The output low pass filters are used to remove the undesirable 200kHz components from the output (hence $f_{-3dB} \ll 200\text{kHz}$). Thus the overall transfer equations for an ideal synchronous detector are

$$X = \text{LPF}\{A\cos(\omega t+\vartheta)\cos\omega t\} = \tfrac{1}{2}A\cos\vartheta = \tfrac{1}{2}x \tag{2.5a}$$

$$Y = \mathrm{LPF}\{A\cos(\omega t+\vartheta)\sin\omega t\} = -\tfrac{1}{2}A\sin\vartheta = -\tfrac{1}{2}y \qquad (2.5b)$$

In both network analyzers and impedance analyzers, synchronous detectors are used in pairs and the ratio of complex outputs is what is really desired. Examples include impedance (v/i), gain (v_o/v_i), and reflection coefficient (b_1/a_1). This ratioing cancels the effect of the magnitude and phase of the LO. Only the frequency and spectral purity of the LO are of interest.

2.2 Effects of Distortion

Though synchronous detectors inherently require nonlinearity in their mixers for operation, this nonlinearity must be carefully controlled to prevent distortion. Ideally, a mixer multiplies two pure sine waves together to produce two other pure sine waves at the sum and difference frequencies. If the input sine waves are distorted, or if some other nonlinearity other than an ideal multiplication is used, then distortion at the output may result. Distortion effects can be modeled by locating parasitic nonlinearities in the block diagram of the detector before the multiplier. Modeling distortion mechanisms and predicting their effects on the output will be discussed in this section.

If the nonlinear transfer function for a generalized mixer is assumed to be memoryless and continuous then it can be expanded into a power series.

$$\begin{aligned} f(u,v) = {} & \gamma_{00}+\gamma_{10}u+\gamma_{20}u^2+\gamma_{30}u^3+\gamma_{40}u^4+\ldots \\ & \gamma_{01}v+\gamma_{02}v^2+\gamma_{03}v^3+\gamma_{04}v^4+\ldots \\ & \gamma_{11}uv+\gamma_{21}u^2v+\gamma_{31}u^3v+\ldots \\ & \gamma_{12}uv^2+\gamma_{13}uv^3+\ldots \end{aligned} \qquad (2.6)$$

If $f(u,v)$ is approximated by $g(u)h(v)$ (see figure 2.2) and this is expanded into a power series, the resulting structure of the expression is identical but the coefficients may differ.

changed by $g(u)$ or $h(v)$, but the signal will still be harmonic in nature. Therefore, if only purely periodic inputs are considered (i.e., consisting of only a fundamental signal and its harmonics) then the distortion on the input signals can be modeled by changing $g(u)$ and $h(v)$ slightly and using pure sine wave inputs.†

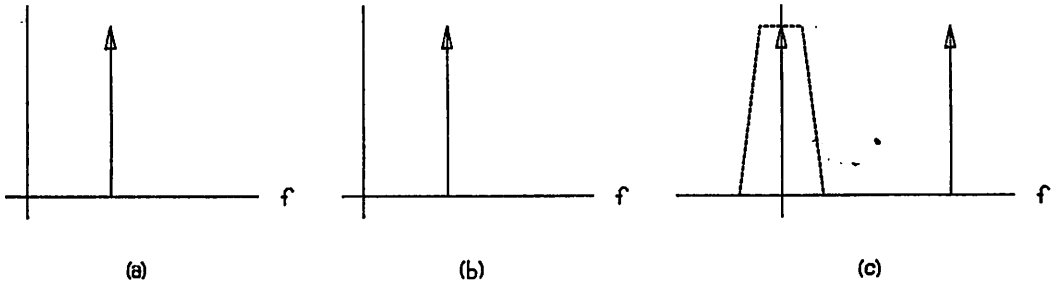

Figure 2.3: Mixing with no distortion. (a) RF input spectrum. (b) LO input spectrum. (c) Mixer output spectrum with passband of output filter superimposed.

Input and output signals for an ideal mixer are shown in the frequency domain in figure 2.3. The passband of the output filter is also shown for a synchronous detector. This is to show the signals that would actually be present on the output of the detector. For a mixer to be ideal, both $g(u)$ and $h(v)$ must be linear.

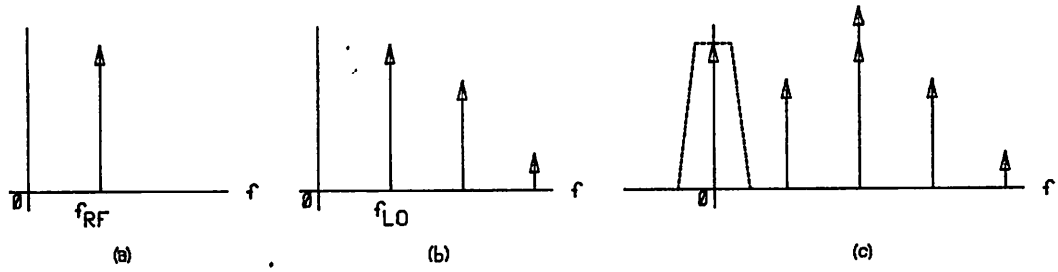

Figure 2.4: Mixing with distorted LO. (a) RF input spectrum. (b) LO input spectrum. (c) Mixer output spectrum.

† Since the power series is used to describe $g(u)$ and $h(v)$, the input signals and all of their derivatives must be continuous. This restriction is removed in the next section.

If either $g(u)$ or $h(v)$ is nonlinear, then spurious output sinusoids will be generated by the mixer. In a synchronous detector these spurious signals will be of no concern because they will be above the LO frequency, and therefore, outside the output filter's passband. This is shown in figure 2.4. Unfortunately if the nonlinearity is in $g(u)$ (the RF path) compression can be generated, which represents an error. Compression is generated by odd order nonlinearities [17].

If there is distortion in the LO channel (i.e. a nonlinear $h(v)$) and the input signal is contaminated with noise, then the resulting noise on the output may be higher than if the LO signal were a pure sine wave. This is because noise near the LO harmonics will be mixed down into the pass band of the output filter. This process is illustrated in figure 2.5. To minimize this problem either the distortion can be reduced in the LO channel or the input noise can be band limited by a low-pass filter on the input.

When both $g(u)$ and $h(v)$ are nonlinear, distortion products generated by the mixer will often fall on top of, or close, to the desired output signal. For example if both $g(u)$ and $h(v)$ generate second and third order distortion products, and both the LO and RF are 100kHz sine waves, then the output of the mixer will be given by equation 2.12.

$$S_{RF} = \cos(\omega t + \vartheta)$$

$$S_{LO} = \cos\omega t$$

$$g(S_{RF}) = a_0 + a_1\cos(\omega t + \vartheta) + a_2\cos2(\omega t + \vartheta) + a_3\cos3(\omega t + \vartheta) \tag{2.10}$$

$$h(S_{LO}) = b_0 + b_1\cos\omega t + b_2\cos2\omega t + b_3\cos3\omega t \tag{2.11}$$

$$\begin{aligned} g(S_{RF})h(S_{LO}) = {} & a_0b_0 + a_0b_1\cos\omega t + a_0b_2\cos2\omega t + a_0b_3\cos3\omega t \\ & + a_1b_0\cos(\omega t + \vartheta) + a_2b_0\cos2(\omega t + \vartheta) + a_3b_0\cos3(\omega t + \vartheta) \\ & + \tfrac{1}{2}\{a_1b_1[\cos\vartheta + \cos(2\omega + \vartheta)] \end{aligned}$$

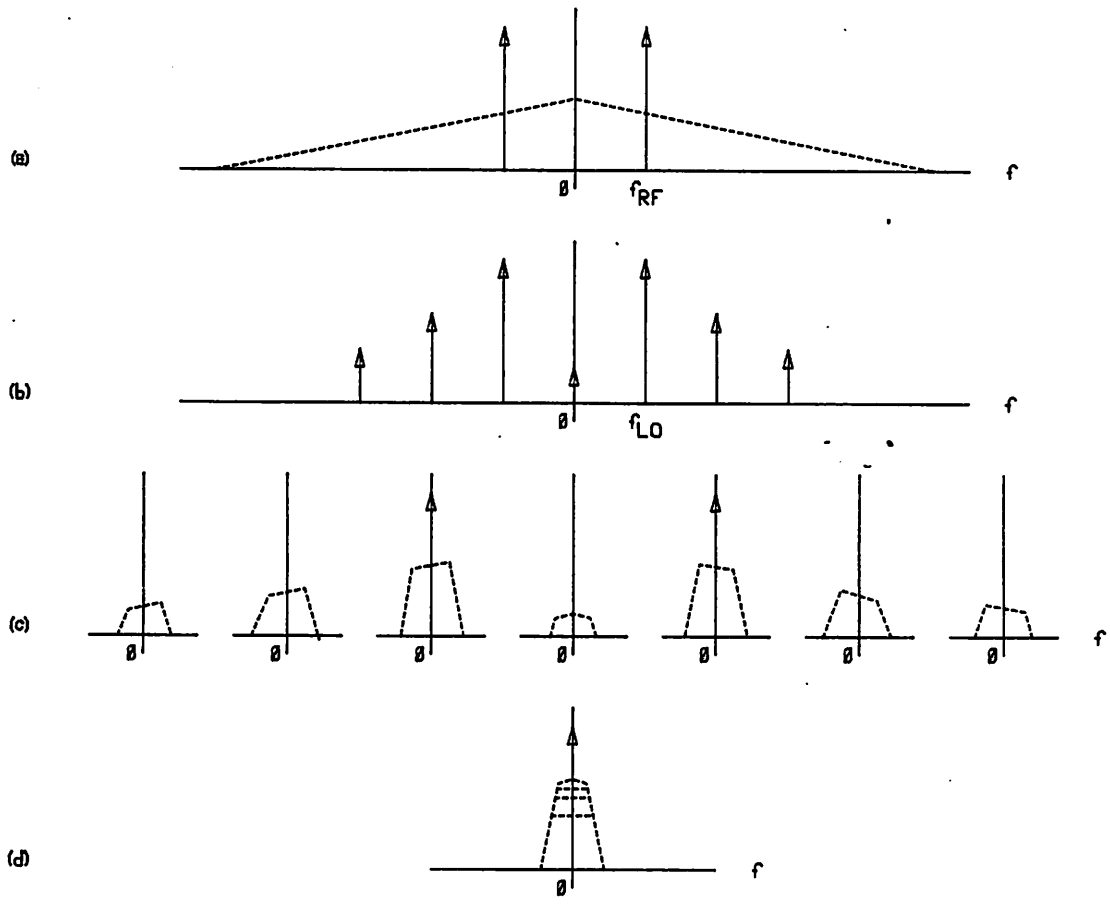

Figure 2.5: Wide-band noise on RF input mixing into output passband because of a non-sinusoidal LO. (a) RF input spectrum, triangle represents noise. (b) LO input spectrum. (c) Noise contribution in output passband from each LO spectral component. (d) Output signal, composite of (c).

$$
\begin{aligned}
&+ a_1 b_2[\cos(\omega t + \vartheta) + \cos(3\omega t + \vartheta)] \\
&+ a_1 b_3[\cos(2\omega t + \vartheta) + \cos(4\omega t + \vartheta)] \\
&+ a_2 b_1[\cos(\omega t + 2\vartheta) + \cos(3\omega t + 2\vartheta)] \\
&+ a_2 b_2[\cos 2\vartheta + \cos(4\omega t + 2\vartheta)] \\
&+ a_2 b_3[\cos(\omega t + 2\vartheta) + \cos(5\omega t + 2\vartheta)] \\
&+ a_3 b_1[\cos(2\omega t + 3\vartheta) + \cos(4\omega t + 3\vartheta)] \\
&+ a_3 b_2[\cos(\omega t + 3\vartheta) + \cos(5\omega t + 3\vartheta)] \\
&+ a_3 b_3[\cos 3\vartheta + \cos(6\omega t + 3\vartheta)]\}
\end{aligned} \tag{2.12}
$$

If this result is passed through a low pass filter then the output is

$$
\begin{aligned}
X &= \mathrm{LPF}\{g(S_{RF})h(S_{LO})\} \\
&= a_0 b_0 + \tfrac{1}{2}[a_1 b_1 \cos\vartheta + a_2 b_2 \cos 2\vartheta + a_3 b_3 \cos 3\vartheta]
\end{aligned} \tag{2.13}
$$

Only the cosϑ term is desired, all other terms are errors. The above expressions show that like order distortion products of $g(u)$ and $h(v)$ will mix down to DC in a synchronous detector and create errors. This can be minimized by making either or both of $g(u)$ and $h(v)$ as linear as possible and minimizing the distortion on the RF and LO signals. The distortion of the input signals can be reduced by placing band-pass filters before the inputs. If this distortion is created by previous stages, these filters will help by eliminating harmonics but will have no effect on compression.

To measure distortion in a synchronous detector conveniently, the RF and LO frequencies are slightly offset from each other. This is equivalent to making ϑ a function of time. Equation 2.14 shows that by replacing ϑ in equation 2.13 with $\vartheta\Delta\omega t$ the error terms become separated in frequency.

$$X = a_0b_0 + \tfrac{1}{2}[a_1b_1\cos(\Delta\omega t) + a_2b_2\cos(2\Delta\omega t) + a_3b_3\cos(3\Delta\omega t)] \qquad (2.14)$$

They are now easily isolated and can be measured with a spectrum analyzer. The Y output is similar to X and is given in 2.15.

$$Y = a_0b_0 - \tfrac{1}{2}[a_1b_1\sin(\Delta\omega t) + a_2b_2\sin(2\Delta\omega t) + a_3b_3\sin(3\Delta\omega t)] \qquad (2.15)$$

Notice that the distortion on the output of X and Y is harmonic in nature.

In review, smooth distortion in mixers can be modeled by predistorting the input signals and applying these to a perfect multiplier. If harmonic distortion is present on both the RF and LO channels then harmonic distortion will be present on the output. This distortion can be measured by slightly offsetting the RF and LO frequencies and viewing the output with a spectrum analyzer. If distortion is only present in the RF channel, then no harmonic distortion will be present on the output. Unfortunately the output will be subject to compression if the distortion is odd order. If there is no distortion present in either the RF

input signal or the RF channel, then distortion present on the LO channel will not cause distortion at the output. Since the signal level of the LO is fixed, compression on the output resulting from odd order distortions in the LO channel is not signal dependent and therefore represents only a gain error, which can be removed by post processing.

2.3 Discrete-Time Detection

A switched-capacitor detector does both its mixing and filtering in discrete-time. Discrete-time filters have been well described in the literature, so they will only be covered lightly here [3][8][9]. Discrete-time mixers on the other hand are more obscure, yet are important to the following topics. Hence, they will described in detail.

Switched-capacitor circuits sample the input signal at their sample rate, which is typically one half the clock rate. This can be modeled by multiplying the LO by an impulse train. The impulses occur every time the switches on the input open. This is because the charge transferred to the integrating capacitor (see figure 2.6a) is solely dependent on V_{IN} at the instant the switch is disconnected from the input. This is equivalent to first multiplying the input by an impulse train (i.e. sampling) and applying it to a conventional RC integrator (figure 2.6b).

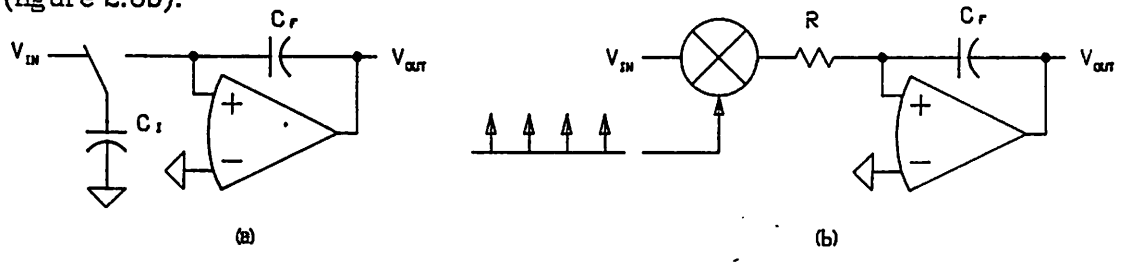

Figure 2.6: (a) Switched-capacitor integrator. (b) RC equivalent of (a) that models signal sampling.

In the mixer being described the LO is a 100kHz sine wave and the clock frequency is 800kHz. The equivalent discrete-time LO is shown both in the time-domain and in the frequency-domain in figure 2.7†.

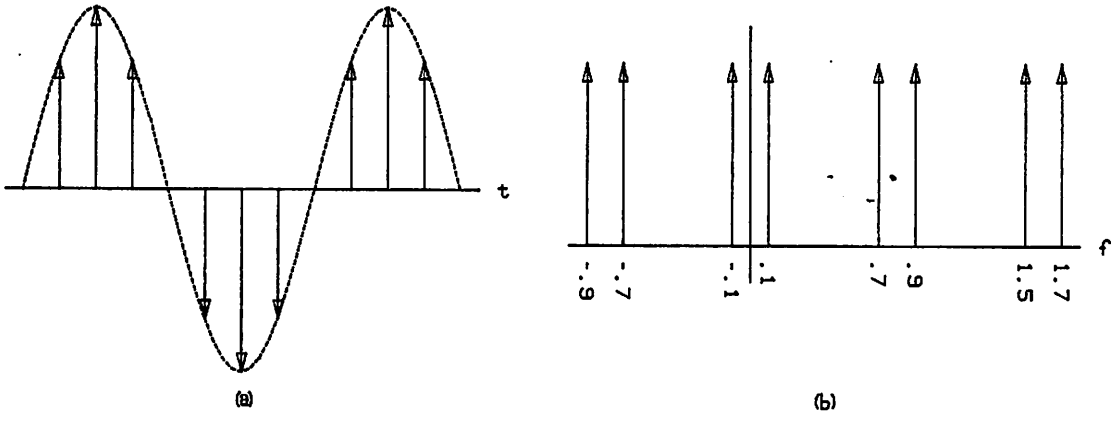

Figure 2.7: (a) LO signal in time-domain. (b) LO signal in frequency-domain (f in MHz).

Notice that there are LO components at

$$f = (800\text{kHz})n \pm 100\text{kHz}, \quad n = 0, \pm 1, \pm 2, \cdots$$

i.e.

$$f = \pm 100\text{kHz}, \pm 700\text{kHz}, \pm 900\text{kHz}, \pm 1.5\text{MHz}, \pm 1.7\text{MHz}, \cdots$$

If this signal is mixed (multiplied) with an input sine wave and the output filtered with a continuous-time low pass filter, the results are to the first degree the same as with the continuous-time mixer. This is because the sum and difference frequencies generated by the mixer (see equations 2.3a and 2.3b) all fall outside the passband of the output low pass filter, except for the DC output component generated by the 100kHz LO component mixing with the 100kHz input. This is identical to the continuous-time mixer. If a discrete-time filter is used on the

† Though this approach is similar to the one taken in the previous section, it should be noted that the power series approach is not valid in this case. This is because a nonlinearity that generates in impulse from a sine wave is discontinuous and does not have a power series expansion. When using a discontinuous LO it is best to abandon the power series and use the Fourier series of the LO to predict the mixer output spectrum.

output, many of the upper harmonics will alias down into the passband. This simply results in the output being quantized in time as impulses. In switched-capacitor circuits, the memory from the continuous-time integrators converts the impulses into steps, as figure 2.8 shows.

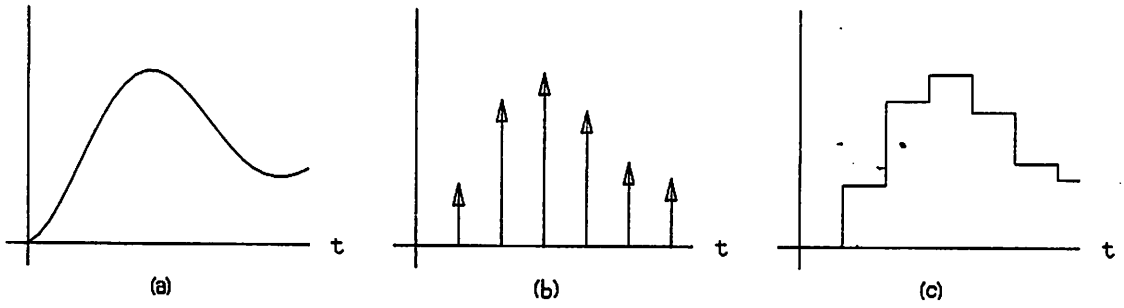

Figure 2.8: Step response of a discrete-time detector with; (a) continuous-time filter, (b) mathematically pure discrete-time filter, (c) switched-capacitor filter.

When the LO is no longer a sine wave the 90° phase-shifter of figure 2.1 becomes ill-defined. A phase-shifter can either shift the phase of the fundamental and all harmonics by 90°, which destroys the time-domain integrity of the signal, or it can leave the time-domain integrity intact and shift the signal in time by an amount equal to one quarter of the period of the fundamental. For the purposes of synchronous detection, the latter is the only sensible definition.

Chapter 3
CIRCUIT DESCRIPTIONS

Circuit description of the monolithic version of the synchronous detector is given in this section. The circuit is broken into four distinct subcircuits. They are: the mixer, the filter, the differential amplifier, and the clock generator. Each one is covered separately with an emphasis on describing the effect of local design decisions on the global operation of the detector. Later in the section the synchronous detector will be treated as a single block in a larger system. Requirements for interfacing to this block will be described. Lastly, the differences between the monolithic and discrete versions will be described.

3.1 The Interleaved Mixer

As described earlier, the function of the mixer is to multiply the RF signal by the LO. This is done by using the circuit shown in figure 3.1. The RF signal and its complement are applied to the switches. The LO signal is generated in the circuit by the pattern in time of switch openings and closures and the carefully chosen sizes for the capacitors. The output is the current i_{OUT} that flows from ground. This ground represents the virtual ground that is present at the input of the filter.

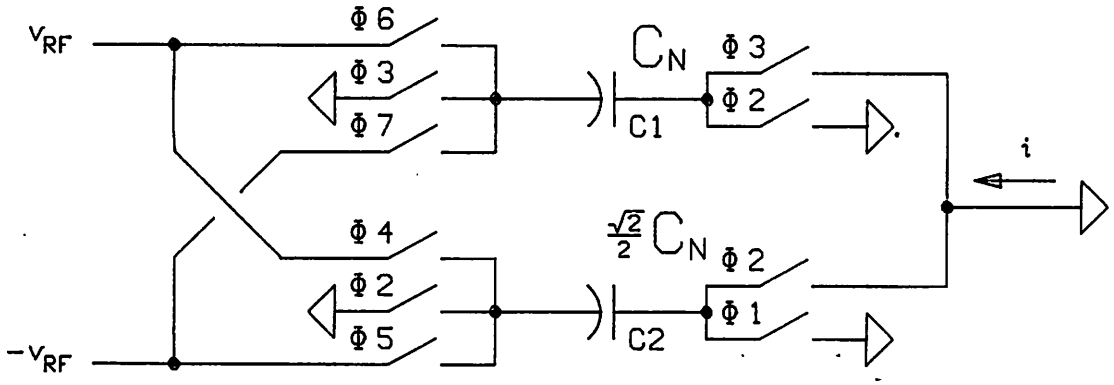

Figure 3.1: Eight point switched-capacitor mixer.

In the following algorithm, the step-by-step operation of the mixer is described with the aid of figures 3.1 and 3.2. Assume t_0=0 initially.

Start:

pre t_1 Switches Φ_1 and Φ_4 close.
$V_{C2} = V_{RF}(t)$

t_1 Switches Φ_1 and Φ_4 open.
$V_{C2} = V_{RF}(1.25\mu S)$

pre t_2 Switches Φ_2 close, C2 discharges through output.
$q_{OUT} = \frac{1}{2}\sqrt{2} C_N V_{RF}(1.25\mu S)$
• $i_{OUT} = \frac{1}{2}\sqrt{2} C_N V_{RF}(1.25\mu S) / 1.25\mu S$
Switches Φ_2 and Φ_6 close.
$V_{C1} = V_{RF}(t)$

t_2 Switches Φ_2 and Φ_6 open.
$V_{C1} = V_{RF}(2.5\mu S)$

pre t_3 Switches Φ_3 close, C1 discharges through output.
$q_{OUT} = C_N V_{RF}(2.5\mu S)$
• $i_{OUT} = C_N V_{RF}(2.5\mu S) / 1.25\mu S$
Switches Φ_1 and Φ_4 close.
$V_{C2} = V_{RF}(t)$

t_3 Switches Φ_1 and Φ_4 open.
$V_{C2} = V_{RF}(3.75\mu S)$

pre t_4 Switches Φ_2 close, C2 discharges through output.
$q_{OUT} = \frac{1}{2}\sqrt{2} C_N V_{RF}(3.75\mu S)$

- $i_{OUT} = \frac{1}{2}\sqrt{2}C_N V_{RF}(3.75\mu S)/\ 1.25\mu S$
  Switches Φ_2 and Φ_6 close.
  $V_{C1} = V_{RF}(t)$

t_4 Switches Φ_2 and Φ_6 open.
$V_{C1} = V_{RF}(5\mu S)$

pre t_5 Switches Φ_2 and Φ_3 remain open.
Neither C1 nor C2 discharge through output.
$q_{OUT} = 0$

- $i_{OUT} = 0$
  Switches Φ_1 and Φ_5 close.
  $V_{C2} = -V_{RF}(t)$

t_5 Switches Φ_1 and Φ_5 open.
$V_{C2} = -V_{RF}(6.25\mu S)$

pre t_6 Switches Φ_2 close, C2 discharges through output.
$q_{OUT} = -\frac{1}{2}\sqrt{2}C_N V_{RF}(6.25\mu S)$

- $i_{OUT} = -\frac{1}{2}\sqrt{2}C_N V_{RF}(6.25\mu S)/\ 1.25\mu S$
  Switches Φ_2 and Φ_7 close.
  $V_{C1} = -V_{RF}(t)$

t_6 Switches Φ_2 and Φ_7 open.
$V_{C1} = -V_{RF}(7.5\mu S)$

pre t_7 Switches Φ_3 close, C1 discharges through output.
$q_{OUT} = -C_N V_{RF}(7.5\mu S)$

- $i_{OUT} = -C_N V_{RF}(7.5\mu S)/\ 1.25\mu S$
  Switches Φ_1 and Φ_5 close.
  $V_{C2} = -V_{RF}(t)$

t_7 Switches Φ_1 and Φ_5 open.
$V_{C2} = -V_{RF}(8.25\mu S)$

pre t_0 Switches Φ_2 close, C2 discharges through output.
$q_{OUT} = -\frac{1}{2}\sqrt{2}C_N V_{RF}(8.75\mu S)$

- $i_{OUT} = -\frac{1}{2}\sqrt{2}C_N V_{RF}(8.75\mu S)/\ 1.25\mu S$
  Switches Φ_2 and Φ_7 close.
  $V_{C1} = -V_{RF}(t)$

t_0 Switches Φ_2 and Φ_7 open.
$V_{C1} = -V_{RF}(10\mu S)$

pre t_1 Switches Φ_2 and Φ_3 remain open.
Neither C1 nor C2 discharge through output.
$q_{OUT} = 0$

- $i_{OUT} = 0$

Go to start.

The statements marked with bullets (•) are the ones in which current flows from the output. During these times an impulse of current flows. When

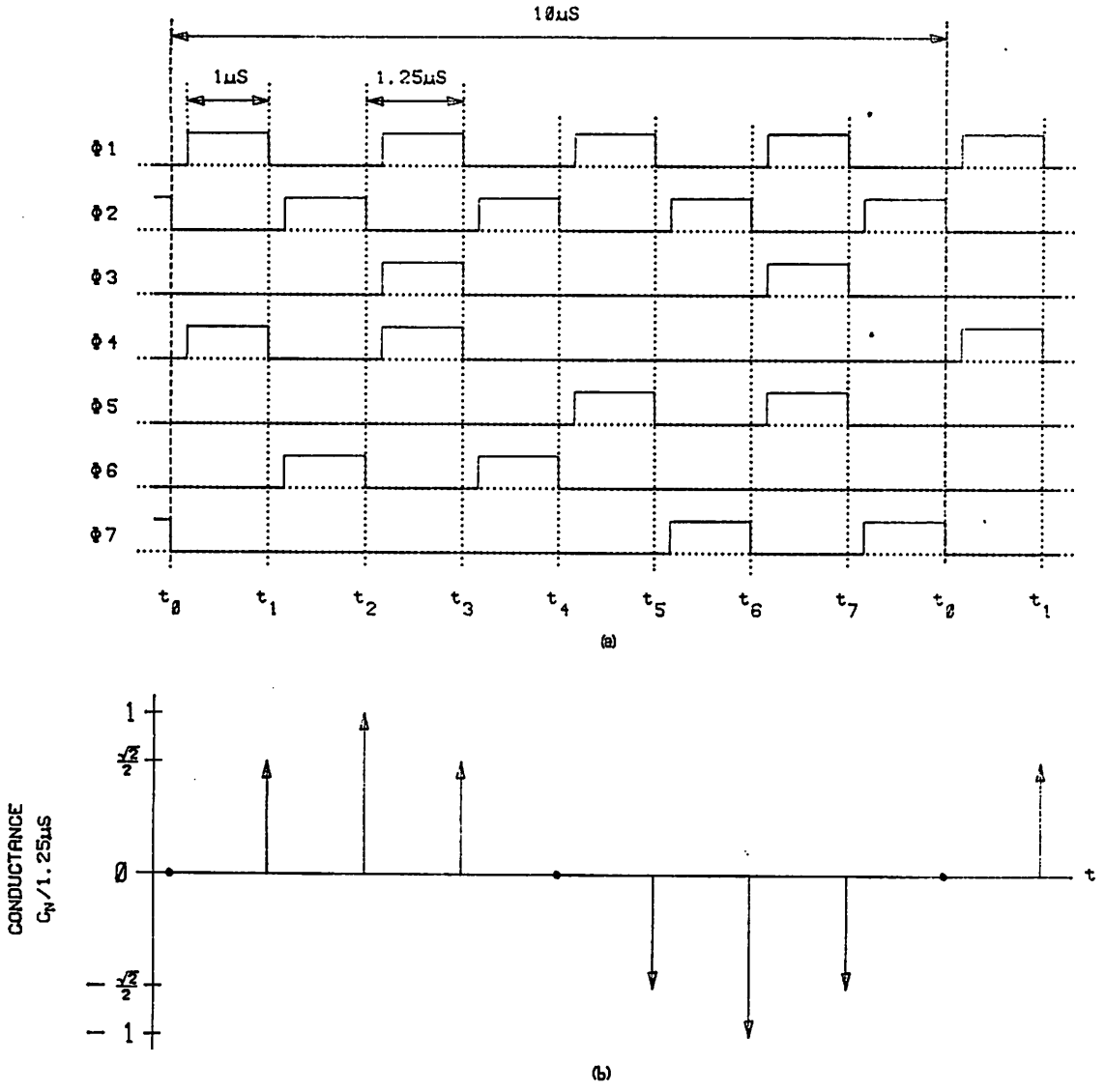

Figure 3.2: (a) Clock signals used with mixer (high level signifies switch is closed). (b) Effective LO signal.

averaged over one clock period of 1.25μS, it equals the current given in the statement.

The interleaved mixer has several desirable characteristics. First, like the switched-capacitor integrator presented in section 1, it is parasitic insensitive. Second, the mixer does not require a leading sample and hold circuit; the mixer

has that function built in. Why this feature is important will be made clear when distortion is discussed. Third, the input is sampled regularly, every 1.25μS. In the past switched-capacitor mixers have been designed where the sample period varies over an LO cycle, which introduces phase modulation that could result in odd behavior. Lastly, the charging and discharging of the capacitors is interleaved in time. This means that input sampling rate is equal to the clock rate. Usually the clock rate is twice the input sample rate. Interleaving allows a lower clock rate, which simplifies the design and reduces power dissipation.

Drawbacks of this design include the requirement for differential input. Since this is rarely provided, a single-ended to differential converter must be present, either on chip or off. Another drawback is that the clocking scheme is complex and will require a large number of clock lines, especially if CMOS transfer switches are used.

Due to the nature of the effective LO signal, the mixer rejects all signals on the input below 700kHz except those desired at 100kHz. Thus the input filter, which is required to reduce the detector susceptibility to high frequency noise and RF harmonics, must pass 100kHz and block everything above 700kHz. This is a mild specification for a filter and the reason why the eight point mixer was chosen. By adding more points to the LO cycle the lowest undesirable input signal frequency that the mixer is susceptible to increases. Unfortunately the clock rate also increases with the number of points in the cycle. The choice of eight points was a trade off between these two parameters.

Inaccuracies in the ratio of C1 to C2 will result in undesirable odd order harmonics in the effective LO. This will result in the mixer being susceptible to signals on the input in the region of the LO's odd order harmonics, such as RF harmonics and noise. This is not a serious problem if the values of the capacitors are close to their design values. A feature of this design is that the mixer in

its rather ideal form (linear elements) of figure 3.1 cannot generate even order harmonics on the LO.

3.2 Switched-Capacitor Filter

While similar in topology to most switched-capacitor filters currently in the literature, this application requires a filter that is unique in several ways. First, the constraints for the filter are specified in the time domain as opposed to the frequency domain. This limits the methods available to synthesize the filter to continuous-time approximations. Second, the filter must minimize the effects of input signals generated by the mixer that would normally create aliasing. This is important so that detector performance is not degraded. In the following subsections, these topics will be covered in detail.

3.2a Filter Response

The output filter exists for two reasons. The first is to remove mixing products from the output. The second is to reduce the noise bandwidth of the detector. To reduce the noise floor, noise bandwidth is made as small as possible while still allowing the filter to settle in a specified time. For this application the settling time was chosen to be 500μS to 0.1%. For a fast settling filter characteristic (one with a relatively constant group delay) the signal bandwidth will be near 4kHz.

Mixing products can be neatly eliminated by setting the clock frequency of the filter to be equal to, or a submultiple of, the lowest frequency mixing product. When this is done, the signal is averaged over one or more exact periods by the filter's integrators and thus, is eliminated. This technique requires a low clock frequency, which aggravates the aliasing problem, but it eliminates the need to tailor the filter response to eliminate the mixing products. This allows

the response to be optimized for transient response and noise bandwidth.

The error band on the setting time specification is small (.1%) and, as a consequence, requires a filter with little overshoot or ringing. Fortunately, this tends to minimize the noise bandwidth. Chen [14] showed that given a filter with a fixed rise time, noise bandwidth will be minimum when the step response is strictly free from overshoot. When this is true settling time is closely related to rise time, and the result should be applicable when settling time is specified. This means that either a first-order response or a Gaussian response is the most desirable. A five pole 4kHz maximally flat envelope delay (MFED) filter was chosen as a compromise between minimum settling time and minimum noise bandwidth. While not ideal, an MFED filter is a close approximation for both goals.

3.2b Filter Synthesis

Once the filter type has been chosen, it is easy to find an LC realization. The one in figure 3.3 was taken from Zverev [13] and the values were modified so that the cut off frequency was 4kHz. A leap-frog approach is taken to convert this circuit to an active RC equivalent. With this approach the inductor currents and capacitor voltages are taken to be state variables. They are calculated using differential integrators. For the circuit of figure 3.3

$$v_1(t) = \frac{1}{C1}\int_0^t (i_{in} - \frac{v_1}{R_S} - i_1)dt + v_1(0) \tag{3.1a}$$

$$i_2(t) = \frac{1}{L2}\int_0^t (v_1 - v_3)dt + i_2(0) \tag{3.1b}$$

$$v_3(t) = \frac{1}{C3}\int_0^t (i_2 - i_4)dt + v_3(0) \tag{3.1c}$$

$$i_4(t) = \frac{1}{L4}\int_0^t (v_3 - v_5)dt + i_4(0) \tag{3.1d}$$

$$v_5(t) = \frac{1}{C5}\int_0^t (i_4 - \frac{v_5}{R_L})dt + v_5(0) \tag{3.1e}$$

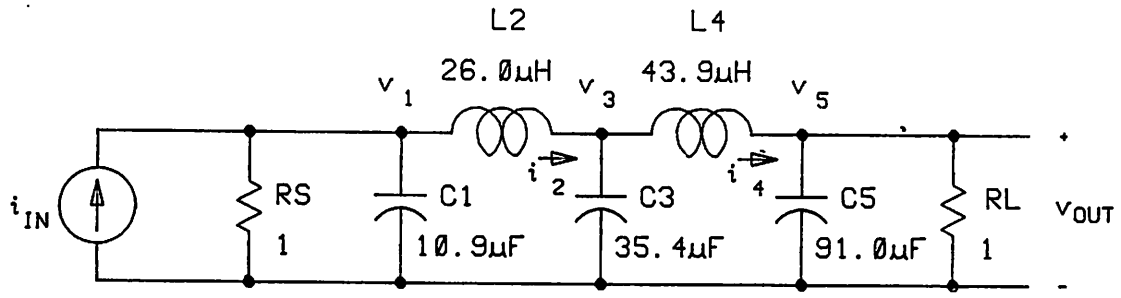

Figure 3.3: LC equivalent to detector output filter.

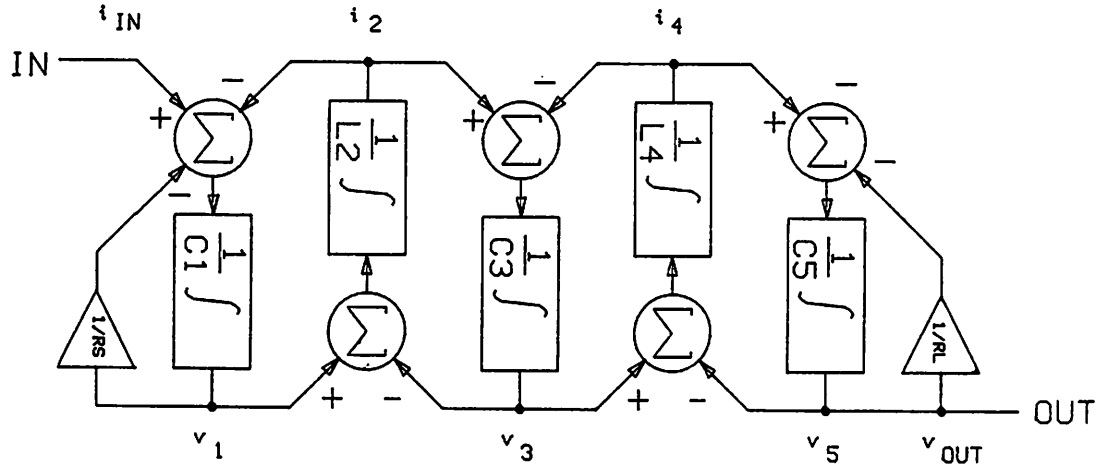

Figure 3.4: Leap-frog realization of figure 3.3

The block diagram for this approach is shown in figure 3.4. In this realization the state, input, and output variables are represented as voltages. Using the differential integrator shown in figure 1.3 a switched-capacitor version can be built. This is shown in figure 3.5. A sample frequency of 400kHz was used for

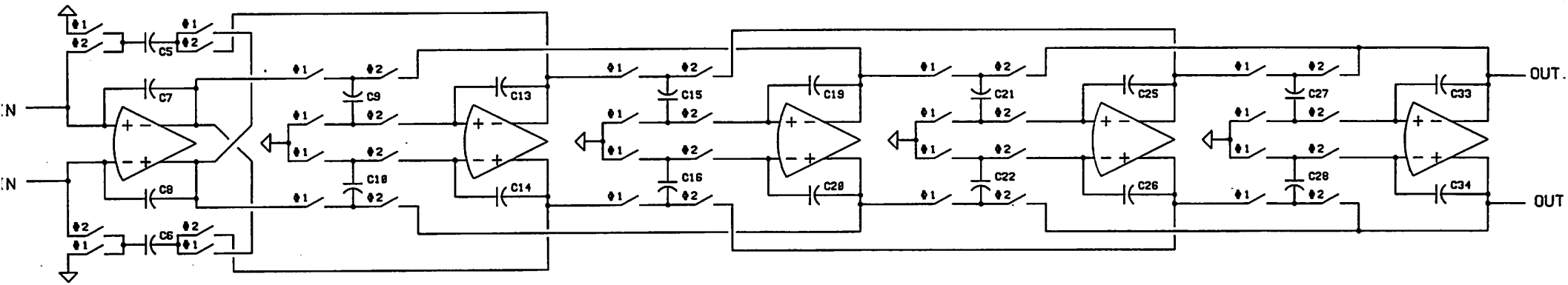

Figure 3.5: Switched-capacitor realization of figure 3.4 with 400kHz clock.

this example, which is the maximum available. This may be confusing at first because the mixer achieves an 800kHz sample rate. But this was because of an interleaving scheme that doubled the number of input capacitors and uses them to sample the input on alternating phases of the clock, thus effectively doubling the sample rate.

C5 = C6 = 2pf	C19 = C20 = 28.3pf
C7 = C8 = 8.7pf	C21 = C22 = 2pf
C9 = C10 = 2pf	C25 = C26 = 35pf
C13 = C14 = 20.8pf	C27 = C28 = 2pf
C15 = C16 = 2pf	C33 = C34 = 72.8pf

Figure 3.6: Capacitor values for figure 3.5.

To minimize the effect of parasitics it is desirable to make the size of the smallest capacitor as large as possible. Since the total amount of capacitance available on chip is fixed, it is necessary to minimize the ratio of the largest capacitor value to the smallest. The unity gain frequency of the integrators is fixed by the design and is equal to $f_u = f_c C_I/(2\pi C_F)$. One method that is available to reduce the ratio is to lower the clock rate on the latter stages. This reduces the latter stages normally high feedback capacitance with respect to the other capacitors in the circuit. If high frequency signals are present on the input of the filter, it then becomes important for the earlier stages to eliminate these signals before they reach the stages with the reduced clock rate, which would not be able to handle these signals properly.

Figure 3.7 shows a modified version of figure 3.5 that has its clock stepped from 400kHz for the first and second stages to 200kHz for stage three and finally to 100kHz for stages four, and five. Notice that the maximum to minimum capacitor value ratio has gone from 36 in the fixed clock frequency version to 18 in the multiple clock frequency version. Also notice that all switched-capacitor resistors in a feedback loop have the same clock frequency. This is important

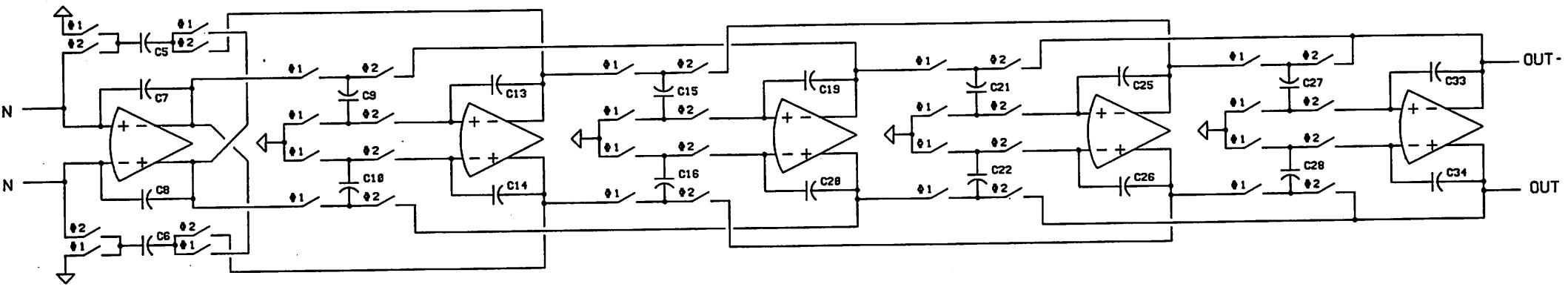

Figure 3.5: Switched-capacitor realization of figure 3.4 with 400kHz clock.

for stability and to assure the accuracy of the transfer function realization.

An advantage of the multiple clock version is that the integrating capacitors all tend to be near the same size. This means that when total on-chip capacitance is fixed, the integrating capacitors for the early stages of the multiple clock version tend to be significantly larger than the fixed clock frequency version's (the size of the integrating capacitor for the latter stages tend to be the same for both methods). Since the dominant noise source in switched-capacitor filters (kT/C) is inversely proportional to the size of the integrating capacitor, the multiple clock version has lower noise.

C5 = C6 = 8pf	C17 = C18 = 8pf
C7 = C8 = 34.8pf	C19 = C20 = 28.3pf
C9 = C10 = 4pf	C21 = C22 = 8pf
C11 = C12 = 8pf	C25 = C26 =35.1pf
C13 = C14 = 41.6pf	C27 = C28 = 8pf
C15 = C16 = 4pf	C33 = C34 = 72.8pf

Figure 3.8: Capacitor values for figure 3.7.

3.2c Parasitic Passbands

Standard design practice for switched-capacitor filters states that no signals should exist at the input of the filter with frequencies greater than half the sampling rate. Failure to comply to this constraint results in these signals being mixed down, possibly into the output passband of the filter. This error mechanism is called aliasing. Unfortunately, aliasing is unavoidable in this application and the filter must minimize its effects to minimize deterioration of detector performance.

With a pure 100kHz signal applied to the mixer, 200kHz and DC signals are generated that are input to the filter. If the filter shown in figure 3.7 is used, the 200kHz signal will be attenuated by the first two stages and then sampled at 200kHz by the switches at the input to the third stage. This results in the

remaining 200kHz signal being mixed down to DC. This is only slightly troublesome because this signal is phase coherent with the desired DC signal generated by the mixer and therefore creates only a quadrature error. More troublesome is that there is effectively a parasitic passband centered at 200kHz. Any signal that is within that passband is attenuated by stages one and two and then down converted by 200kHz to appear at the output of the filter within the passband. A parasitic passband also appears at 400kHz as well as every other multiple of 200kHz. The 100kHz clock rate for the switches at the input to stage four also creates parasitic passbands, which occur every 100kHz. Input signals must pass through three stages before being sampled at 100kHz and therefore the attenuation of these passbands is greater than those created by the 200kHz clock.

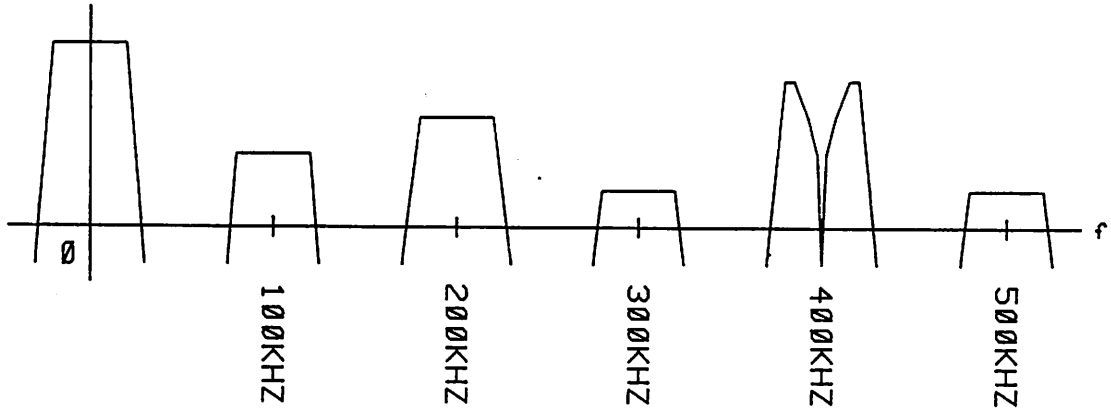

Figure 3.9: Desired and parasitic passbands of the filter in figure 3.7.

The parasitic passbands for the filter of figure 3.7 are shown in figure 3.9. Note that the 400kHz passband is large and has a null at exactly 400kHz. The size is from the signal only passing through one stage of the filter before it is sampled by the 400kHz clock at the input to stage two. The null results from the 400kHz input signal being integrated over exactly one period (i.e. it integrates to zero) before being sampled. The other parasitic passbands do not have nulls because once the input signal is sampled by stage one at 400kHz, the signal is decimated rather than averaged. This contrasts with the first stage where two

800kHz samples from the mixer are averaged for each sample at 400kHz.

Parasitic passbands create two serious problems. First is that harmonics of the mixer's input signal result in signals input to the filter that fall in these passbands. This significantly degrades the input harmonic rejection of the detector. One solution to this problem is to return to the use of a filter with a single clock rate of 400kHz. This was deemed undesirable earlier because of the large capacitor ratio. Another interesting solution is to use a filter with a 100kHz clock through out. This would still suffer from parasitic passbands every 100kHz but each would have nulls at multiples of 100kHz. Unfortunately this also suffers from a large capacitor ratio as well as significantly larger parasitic passbands that results from only one stage of filtering before sampling. This aggravates the second problem, which is decreased noise performance, because the noise in each of the parasitic passbands gets down-converted into the output passband of the filter.

The best solution to these problems is to use bilinear integrators in the filter. The benefit of bilinear integrators are that they average the present (v_n) as well as the previous (v_{n-1}) input voltage to calculate the integral. This means that an input signal that is at exactly one half the sample frequency will be averaged to zero. This results in a null in the transfer function of the bilinear integrator at half the sample rate. Thus as the clock frequency is reduced with each stage, the signal is first averaged, then decimated, rather than simply decimated. This places nulls in all the parasitic passbands of figure 3.9. Unfortunately all bilinear integrators reported to date suffer from parasitics.

3.2d Parasitic-Insensitive Bilinear Integrator

An approximation must be made to make the conversion of the filter from continuous-time to discrete-time. A continuous-time integrator is impossible to simulate exactly in discrete-time and therefore one of the three following approximations are made.

Forward Difference

$$V_{OUT}(n) = V_{IN}(n-1) + V_{OUT}(n-1) \tag{3.2a}$$

Backward Difference

$$V_{OUT}(n) = V_{IN}(n) + V_{OUT}(n-1) \tag{3.2b}$$

Trapezoidal or Bilinear

$$V_{OUT}(n) = \tfrac{1}{2}[V_{IN}(n) + V_{IN}(n-1)] + V_{OUT}(n-1) \tag{3.2c}$$

As the input frequency approaches the Nyquist frequency (i.e. one half the sample frequency) an integrator using the forward difference approximation will exhibit excess phase shift. This will tend to destabilize filters synthesized with these integrators. Integrators using the backward difference approximation exhibit reduced phase shift near the Nyquist frequency. This tends to over stabilize or reduce the Q of a filter built with these integrators. The equations show that the bilinear approximation is simply a combination of the first two approximations. So the imperfect phase shift of the first two approximations is combined and results in a nearly ideal phase shift versus frequency for the bilinear. This is shown in figure 3.10.

Circuits that realize the three approximations are shown in figure 3.11. Note that the bilinear integrator is simply a combination of the first two. The bilinear integrator needs an inverter to counter the inversion that occurs in the backward difference circuit. This inverter is inherent in differential mode circuits.

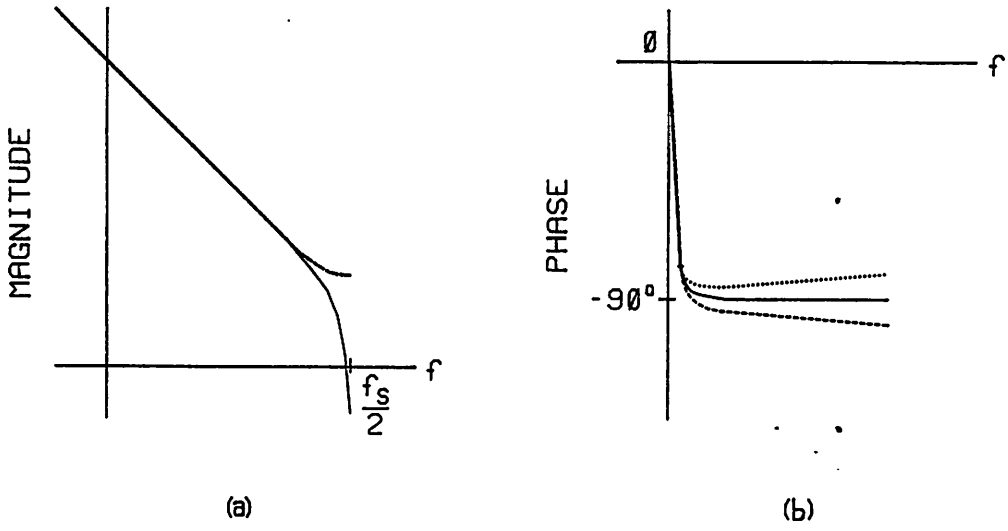

Figure 3.10: Frequency response of a bilinear integrator (solid) as opposed to integrators using forward (dashed) and backward (dotted) difference approximations.

Bilinear integrators offer two basic advantages. First their accurate phase characteristics allow the direct implementation of continuous-time circuits in discrete-time without predistorting the pole locations. There exists another way around this problem, which is to alternate forward and backward difference integrators such that each feedback loop contains one of each type. This works well but is not applicable to all filter topologies. This technique was used in figures 3.5 and 3.7. The second advantage is that the bilinear integrator has an inherent null in its amplitude response at the Nyquist frequency. The forward-backward loop method does not have this characteristic [3][10][11].

Figure 3.12 shows one half of the synchronous detector. This consists of the mixer and the bilinear version of the filter. The clock signals necessary to drive this circuit are shown in figure 3.13. A high level on these signals signifies that all switches using that clock are closed. The mixer has been modified slightly to compensate for a flaw in the filter. Every other cycle C5 parallels C7. This means that the size of the integrating capacitor, and therefore the gain, of the first stage is modulated at a 200kHz rate. This is compensated for by assuring

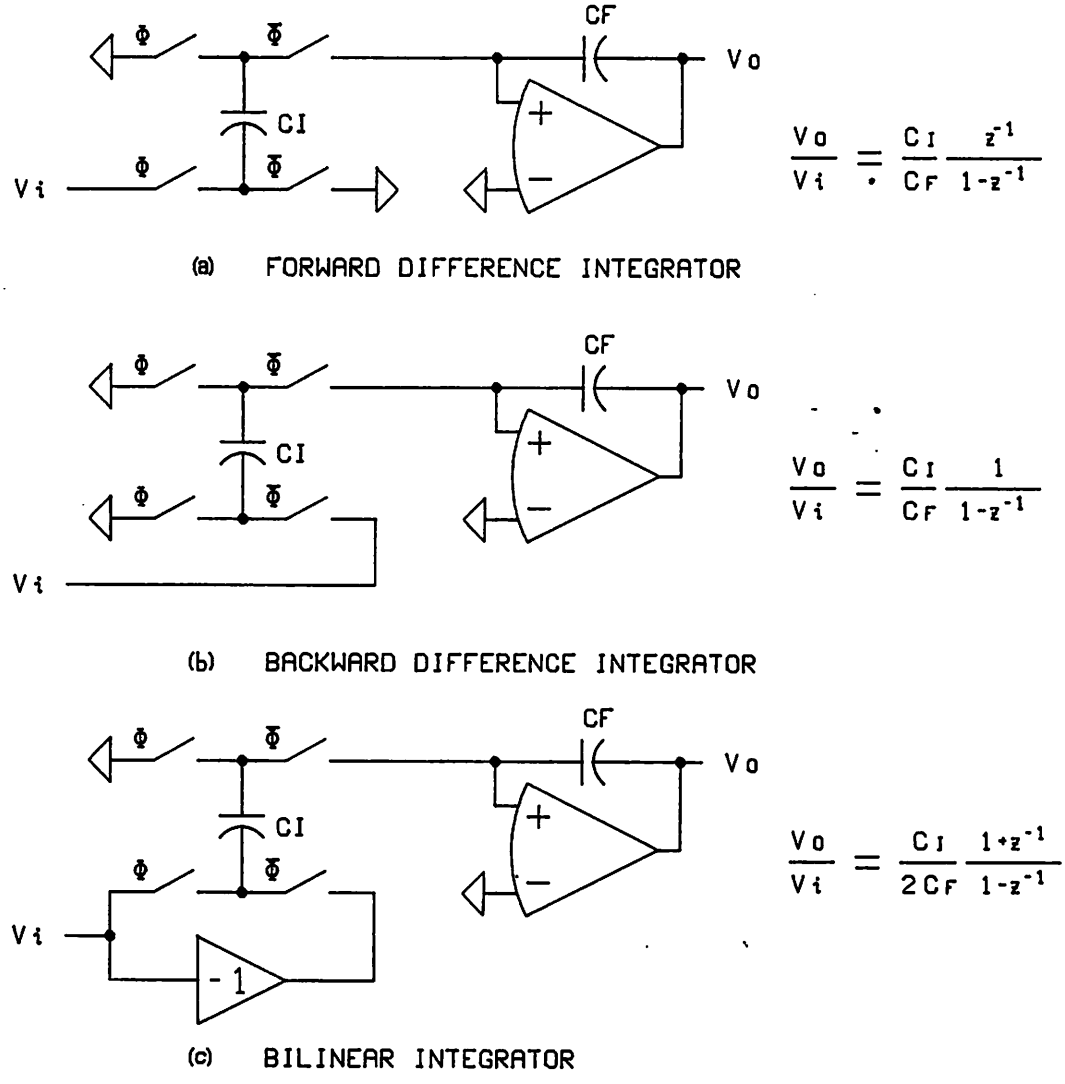

Figure 3.11: Parasitic insensitive realizations of three basic types of discrete-time integrators.

that when C5 parallels C7, C1 is the input capacitor that is discharged into the integrator and that the value of C1 has been increased by a factor of (C5 + C7)/ C7. This was done in figure 3.14, which is a list of capacitor sizes for figure 3.12.

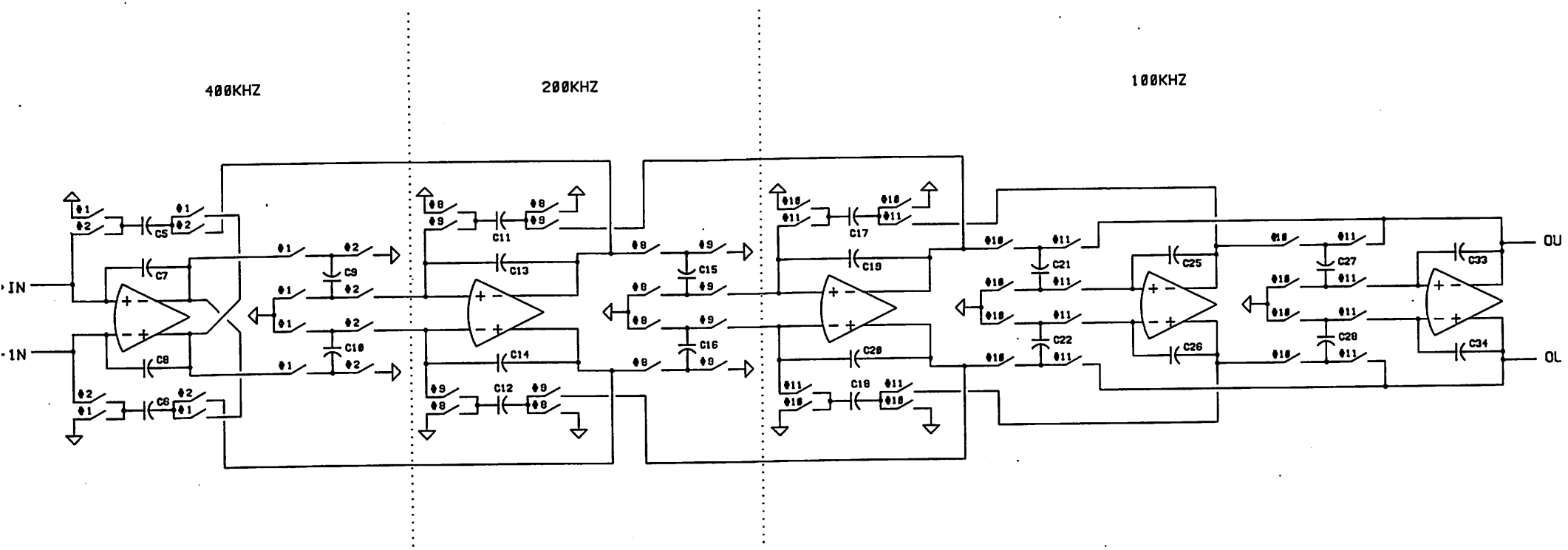

Figure 3.7: Filter of figure 3.5 with multiple clock frequencies.

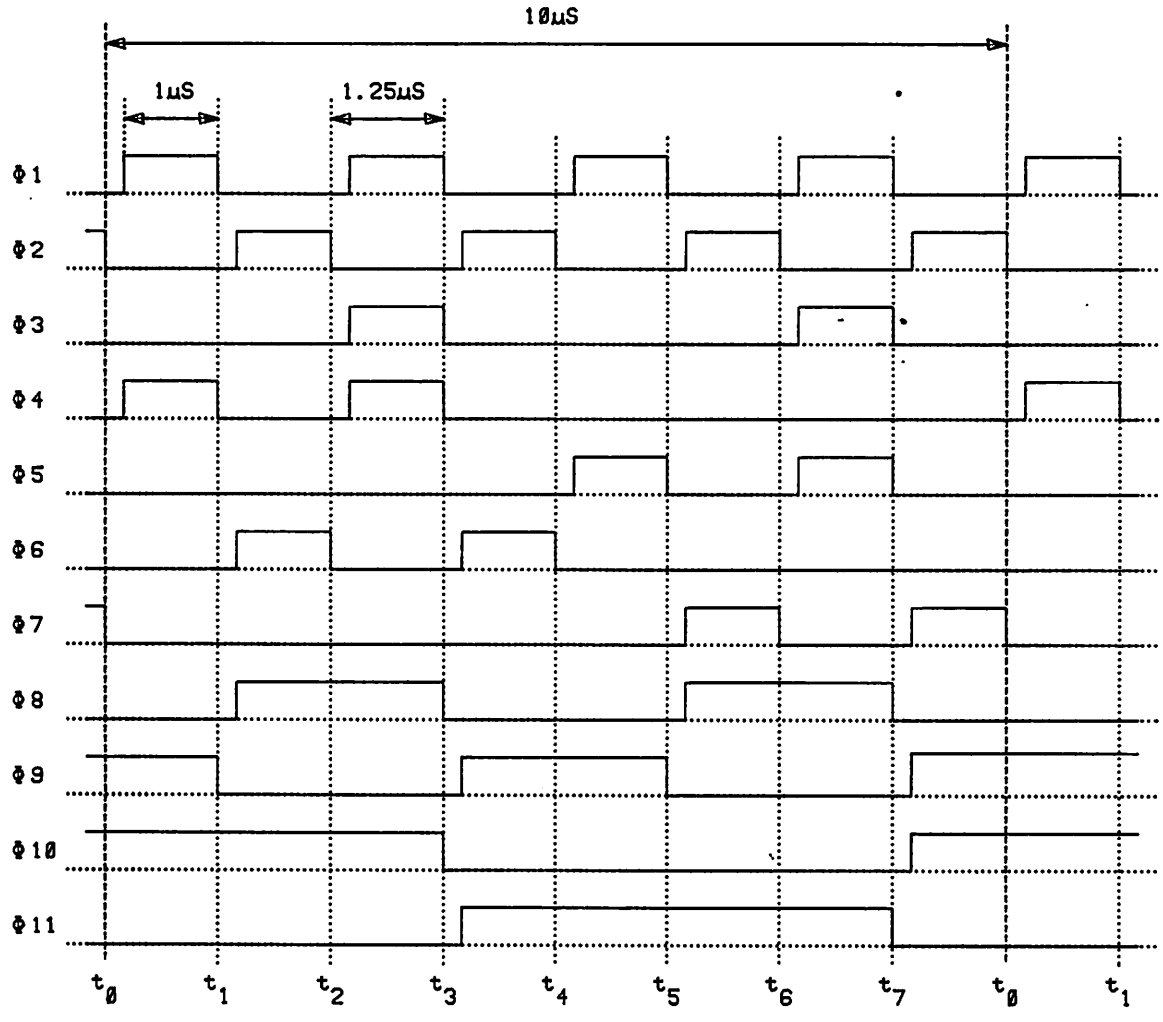

Figure 3.13: Clock signals for figure 3.12.

3.3 CMOS Differential Amplifier

To accommodate the bilinear circuits the operational amplifier must be differential output as well as differential input. This forces the topology of the amplifier to be somewhat unique. It also gives some benefits such as greater power supply noise rejection and reduced distortion. These are important in an instrumentation application because a large dynamic range is required. Also

C1 = C2 = 9.8pf	C15 = C16 = 4pf
C3 = C4 = 5.7pf	C17 = C18 = 8pf
C5 = C6 = 8pf	C19 = C20 = 28.3pf
C7 = C8 = 34.8pf	C21 = C22 = 8pf
C9 = C10 = 4pf	C23 = C24 = 35.1pf
C11 = C12 = 8pf	C25 = C26 = 8pf
C13 = C14 = 41.6pf	C27 = C28 = 72.8pf

Figure 3.14: Capacitor values for figure 3.12.

needed from the amplifier, because of the dynamic range requirement, is low noise. Both white noise and $1/f$ noise must be minimal. Attempts to reduce these types of noise in the amplifier are described in the next subsection. In the following subsections the amplifier circuitry is described briefly. After that the achieved specifications are presented.

3.3a Noise Reduction Techniques

As previously stated there are two types of noise created by the amplifier that must be minimized. They are $1/f$ noise and white noise. The white noise consists mainly of shot noise but there is a small thermal noise component. The effect of $1/f$ noise is reduced by chopper stabilization. Chopper stabilization effectively mixes $1/f$ noise up to some high frequency that is out of the passband of the filter, in this case 50kHz. This is done by reversing the two inputs to the differential amplifier at a 50kHz rate while also reversing the two outputs simultaneously. This is performed by the circuit in figure 3.15. In essence, this mixes the input signal up to 50kHz and then applies it to the amplifier. The amplifier adds $1/f$ noise that is centered around DC. This signal is then again mixed with a 50kHz signal. This brings the original signal back down to DC while moving the center frequency of the $1/f$ noise up to 50kHz and out of the passband of the filter. This process is discussed in depth by Hsieh [5].

It is important to use an amplifier that initially has little $1/f$ noise so that when chopper stabilized the skirts of the $1/f$ noise, now centered at 50kHz, do

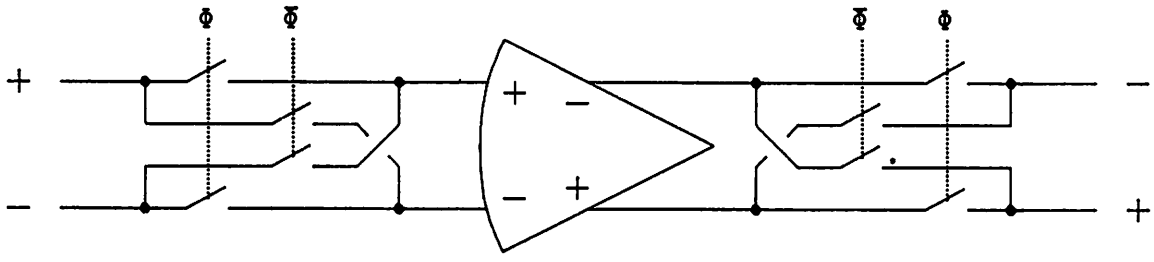

Figure 3.15: Chopper stabilization of differential amplifier.

not reach into the filter passband. This is done by designing the amplifier so that transistors that contribute noise to the output are made large. The output noise of a MOSFET in saturation is [16]

$$I_n^2 \approx 4kT\frac{2}{3}g_m\Delta f + \frac{k_f \quad I_D^{1.0}}{C_{OX}WL \quad f}\Delta f \qquad \text{where} \qquad k_f = 10^{-26}\frac{A^2}{V}\text{sec} \quad g_m = \sqrt{\frac{2W\mu C_{OX}I_D}{L}} \tag{3.3}$$

In this equation W represents channel width and L is channel length. The first term in the equation represents shot noise; the second represents $1/f$ noise. To find the input referred noise, both sides are divided by g_m^2.

$$V_n^2 \approx \frac{2}{3}\frac{4kT}{g_m}\Delta f + \frac{k_f I_D^{1.0}}{g_m^2 C_{OX}WLf}\Delta f \tag{3.4}$$

Thus equation 3.4 shows that input referred $1/f$ noise is inversely proportional to channel width. Also shown is that input referred $1/f$ noise is to the first order independent of drain current. This means that all devices acting as amplifiers should be as wide as possible. Equation 3.3 though shows that for devices acting as current sources to have low $1/f$ noise they should simply have a large area.

The chopping frequency of 50kHz was chosen because it is one half the clock frequency of the output stages of the filter. This places the inherent null

in the transfer function of a bilinear integrator right on top of the new center frequency of the $1/f$ noise. Chopping also mixes the offset voltage of the differential amplifier up to 50kHz where it is removed by the bilinear integrators.

Shot noise is created by DC current flow through the MOS transistors. To reduce shot noise in devices acting as amplifiers, equation 3.4 shows that they should be made wide, short, and run at a high quiescent current. This does not conflict with the desire for a wide device to reduce $1/f$ noise. To reduce shot noise in devices acting as current sources, equation 3.3 suggests that the device should be made long and narrow. This partially conflicts with the low $1/f$ noise requirements of large device area. The optimum solution is to make the device as long as possible. Thermal noise is generated by resistance present in the circuit, particularly in series with the gates of the input devices. So it is important to minimize the use and resistance of polysilicon at the input of the amplifier.

There are two different methods available for creating a totally differential amplifier. First is to simply combine two conventional op amps. Second is to modify a conventional op amp by removing the differential to single-ended converter and add another output stage. If this is done a serious problem is encountered. The common mode voltage is not defined and the quiescent operating point is free to drift and may drift outside the linear range of the amplifier. To correct this problem a common-mode feedback amplifier is added. These two differential amplifier schemes are shown in figure 3.16.

The differential amplifier/common-mode feedback scheme is inherently lower noise than the two op amp scheme because it has fewer devices that can contribute to the differential-mode output noise. In the differential amplifier/common-mode feedback scheme only devices in the differential amplifier can contribute to differential-mode output noise. Other parts of the

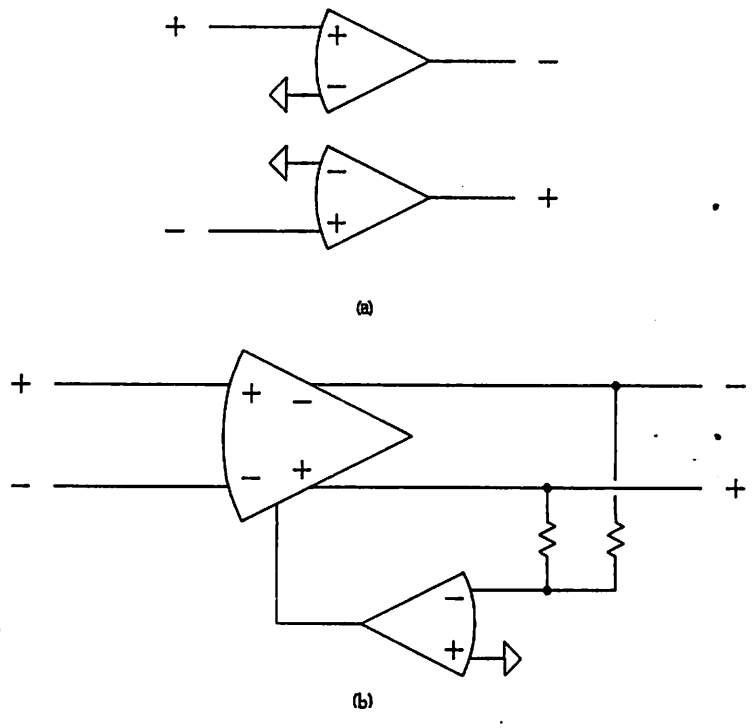

Figure 3.16: Differential input and output amplifiers. (a) Two op amp scheme. (b) Differential amplifier/common-mode feedback scheme.

circuit such as the bias or common-mode amplifier circuitry can contribute only common-mode noise, which is ignored by the circuit. In the two op amp scheme every device in both amplifiers is a potential contributor to differential mode noise. Even if the noise of the input stages dominates, there are two input stages to contribute differential mode noise in the two op amp scheme and only one in the differential amplifier/common-mode feedback scheme. So the two op amp scheme was not used.

3.3b Amplifier Circuit Description

The amplifier is shown in figure 3.17 and consists of four sections; the differential amplifier, the common-mode amplifier, the bias circuits, and the chopper stabilization switches. The chopper stabilization switches consist simply of four CMOS switches at the input and four at the output. The four input switches are minimum geometry to minimize charge injection onto storage

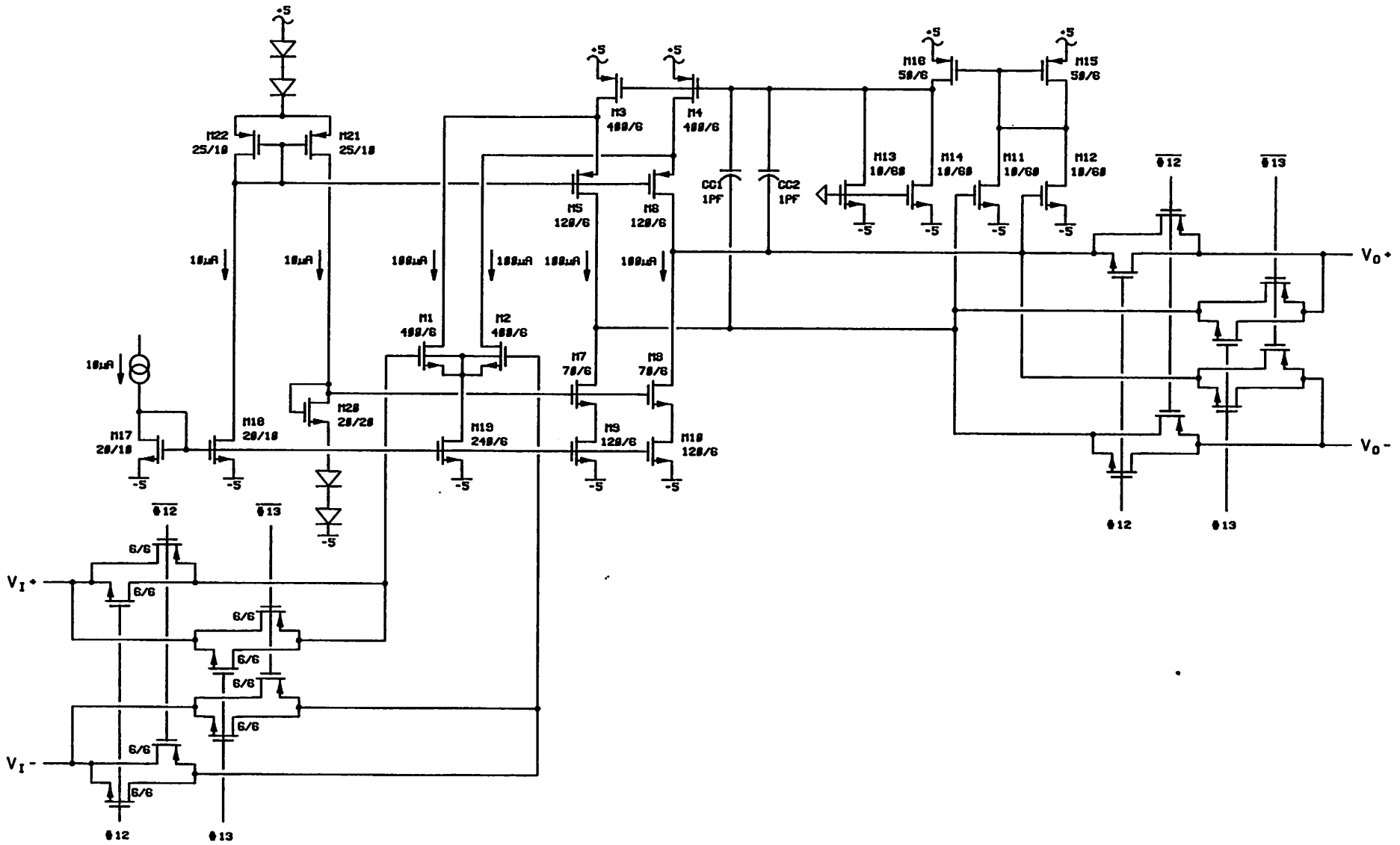

Figure 3.17: CMOS differential amplifier.

capacitors from switch parasitics. Output switches are minimum length but wide enough to guarantee an on resistance low enough so that they do not interfere with amplifier settling.

The differential amplifier is a single stage folded cascode. This results in an amplifier with moderate gain and high speed. Only moderate gain is required because the amplifier is being used in a low Q filter. Finite gain results in filter poles moving slightly from their desired locations, which is not significant in a low Q filter [3]. Cascoding of the amplifier provides higher bandwidth and gain. Making the amplifier with only one stage simplified considerably the process of making the amplifier stable with its required bandwidth. This is because there are no isolated poles of any consequence. The isolated pole created by cascoding is at a very high frequency and therefore it can be ignored. By connecting the feedback capacitors to the amplifier; the dominant amplifier pole is moved to the desired location and the non-dominant pole is moved to a higher frequency. This moves the lowest non-dominant pole well beyond the unity gain frequency of the amplifier (pole splitting [16]). This results in an amplifier with a closed-loop response with no overshoot or ringing.

To prevent isolated poles in the amplifier, the output stage was eliminated. This is possible, because only capacitors are driven with the amplifier, and consequently there is no DC load resistance to reduce the gain. Eliminating the output stage gives another significant advantage besides stability, lower noise. Typically the bandwidth of an output stage is much higher than the closed-loop bandwidth of the amplifier. Its noise bandwidth is also much higher. When the output of the amplifier is sampled by the switched-capacitor resistors, this high frequency noise is down converted by sampling, so that it could fall in the passband of the filter. This does not happen when the output stage is removed because the noise bandwidth of the amplifier then equals the closed-loop

bandwidth. This process is illustrated in figure 3.18.

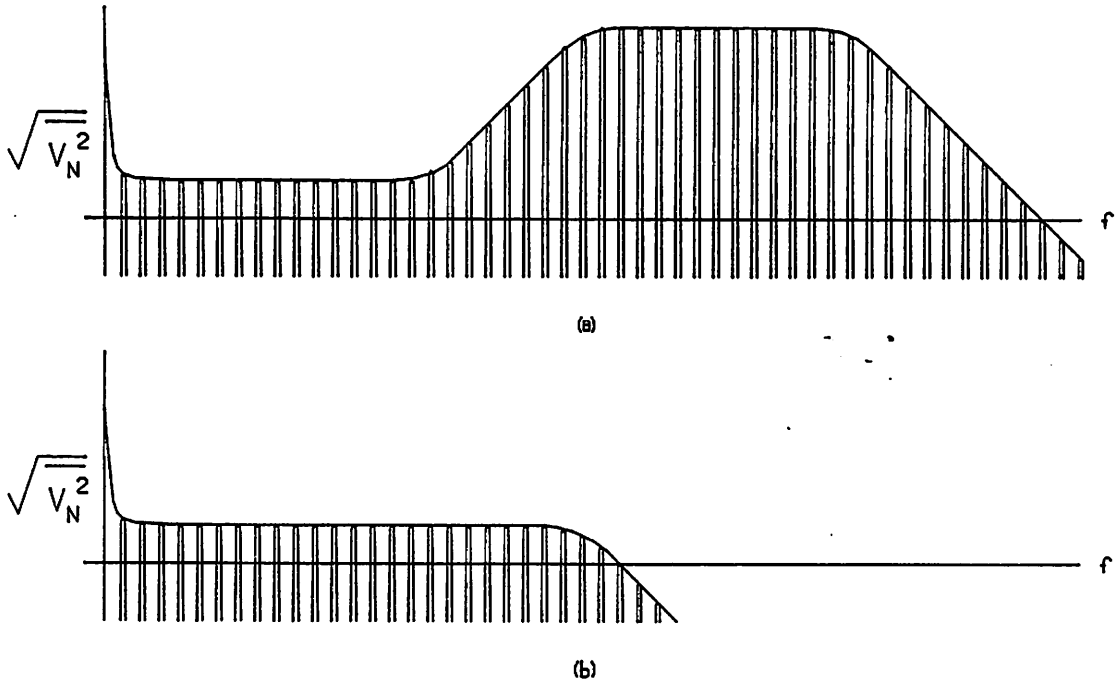

Figure 3.18: Noise at output of differential amplifier and parasitic passbands from sampling. (a) Amplifier with output stage. (b) Amplifier without output stage.

The common mode amplifier is a difficult function to implement well because of the large input voltage range over which it must work. This implementation uses two low g_m common source amplifiers, M11 and M12, to convert the two output voltage into currents. The amplifiers are very low gain to provide operation as linear as possible over the ±3V output operating range. The output of these two common source amplifiers are added together and that current is sourced by the input of a current mirror consisting of M15 and M16. The output current of the mirror is subtracted from two common source amplifiers whose inputs are connected to ground, M13 and M14. This difference current is integrated by the input capacitance of the transistors that set the bias current for the differential amplifier, M3 and M4. The circuit reaches quiescence when the difference current equals zero, which ideally happens when the average

input voltage for the first two common-source amplifiers equals the average input voltage for the second two. This occurs when the output common-mode voltage is equal to zero. If the input common-source amplifiers suffer from distortion, the common-mode voltage will vary as a function of the differential-mode voltage. In this design the common mode voltage changed from zero volts, with no differential-mode output signal, to negative one half volts with a four volts differential-mode output signal. This causes no real problems if the increased output voltage is known in advance and the amplifier is designed accordingly.

The common mode amplifier should settle at least coarsely before the output voltage is sampled. This is to minimize the chance of distortion created by the varying bias currents. Thus the common-mode amplifier should be fast. Unfortunately this requires large quiescent currents, which means linearity must be traded off against speed.

The bias circuitry provides three output voltages. One sets the operating current of the differential amplifier. The other two are used to bias the cascode transistors. A 10μA current, which is provided from off-chip, is used as a reference for the bias circuit. Simple current mirrors are used to bias the differential amplifier. To bias the differential amplifier properly the voltage on the sources of the cascode transistors should be from 1 to 1½ volts from the supply to allow enough drain to source voltage for the current source transistors to operate in the saturated region. This means the gate voltage for the cascode transistors should be referenced to the respective supplies. They should consist of the sum of a constant portion of 1½ volts and a portion that varies with temperature and device parameters to compensate for the effect of these on the on gate to source voltage of the cascode transistors. The constant voltage is roughly generated by two series junction diodes. The parameter and

temperature dependent portion is generated by a diode connected MOS transistor. This technique keeps the amplifier biased properly over a wide range of temperatures and device parameters.

3.3c Achieved Amplifier Specifications

Although the amplifier was never fabricated, it was extensively simulated using Hewlett-Packard's HPSPICE. This program is based on the University of California's circuit simulator SPICE, but it uses slightly different MOS models. The circuit was found to be stable and able to operate within required specifications over a temperature range of -55°C to 125°C and over foreseen device parameter variations. The test circuit is shown in figure 3.19. Achieved specifications are given in figure 3.20. Predicted transient waveforms are shown in figures 3.21 and 3.22.

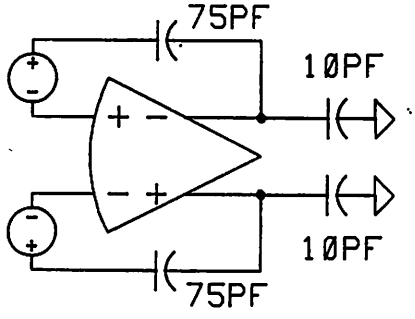

Figure 3.19: Differential amplifier test circuit.

3.4 Clock Generator

A state machine approach was used to generate the 17 clock phases needed to operate the synchronous detector. This circuit is shown in figure 3.23 with its output waveforms shown in figure 3.24. Clock signals for both mixers of the detector are generated. The proper way to connect these signals is shown in figure 3.25.

DM settling time to 0.1%†	250nS
DM unity gain bandwidth	10MHz
DM slew rate	20V/μS
DM input referred noise	8nV/$\sqrt{Hz}$
DM input referred noise‡	5.5nV/$\sqrt{Hz}$
CM settling time to 2%†	700nS
CM unity gain bandwidth	2MHz
power dissipation	5mW
circuit area	1000mils^2
technology used	6μ CMOS with P well

† For 4V differential step on output.
‡ Effective input referred noise for one half differential amplifier.

Figure 3.20: Typical differential amplifier specifications at 25°C.

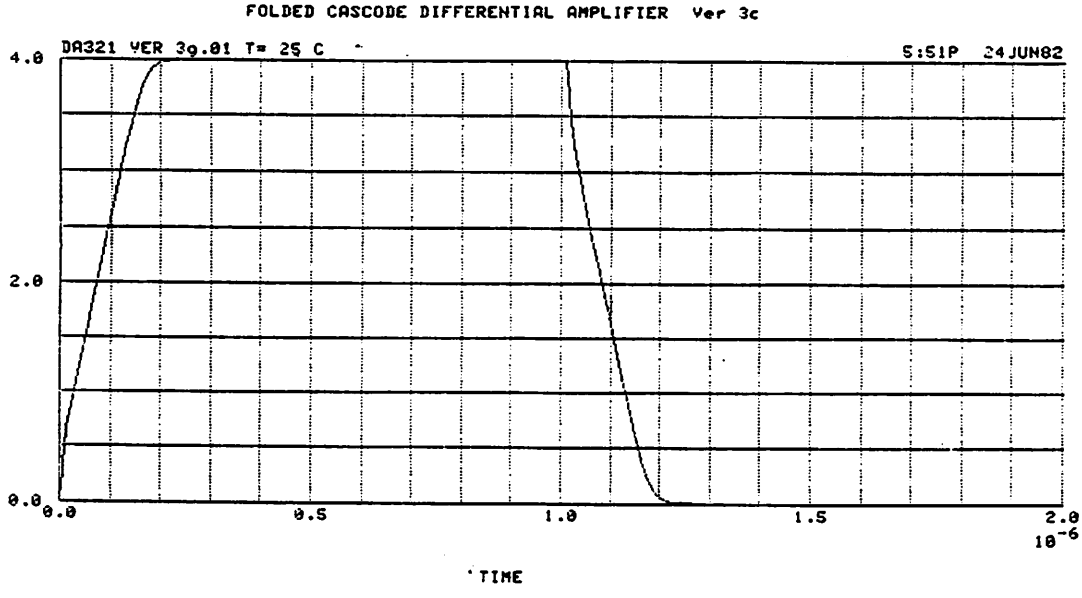

Figure 3.21: Differential output voltage pulse response.

An important requirement placed on the clock generator is that the clock signals should be skewed in time so that two switches that are connected to the same node are never on simultaneously. To achieve this goal a unique flip-flop was designed and the input clock signal was constrained to be the one shown in figure 3.24. The flip-flop is similar to a D flip-flop except when the data signal and the clock signal are both low. Under this condition, the output Q is reset to

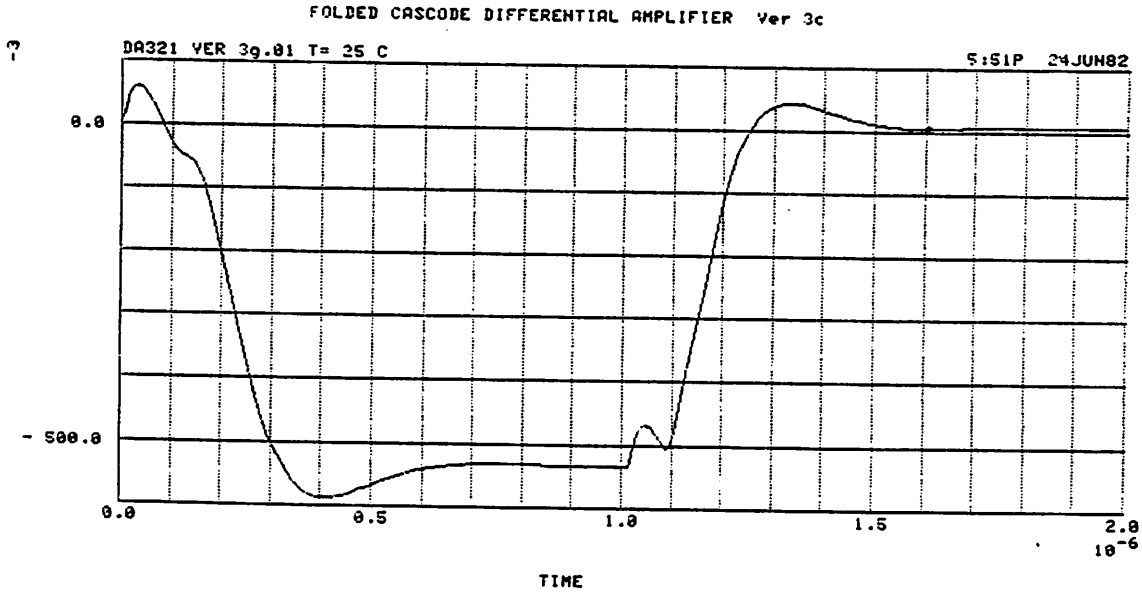

Figure 3.22: Common-mode output voltage pulse response.

logical zero. This forces those switches that are turning off to turn off 250nS (length of time input clock is low) sooner than they would if D flip-flops were used. This is also 250nS sooner than the switches that are turning on do turn on. The circuit for this flip-flop is shown in figure 3.26.

3.5 Monolithic Switched-Capacitor Synchronous Detector

To get proper performance from the synchronous detector it is important to interface to the circuit properly. This is especially true with the particular implementation used. The differential nature of the circuit requires that an off-chip single-ended to differential converter be provided for the input. Also a differential to single-ended converter for the output is needed. It may be possible to realize both of these circuits on-chip.

The clock generator provides a sample and hold trigger signal so that an external sample and hold can be synchronized to the detector clock. This

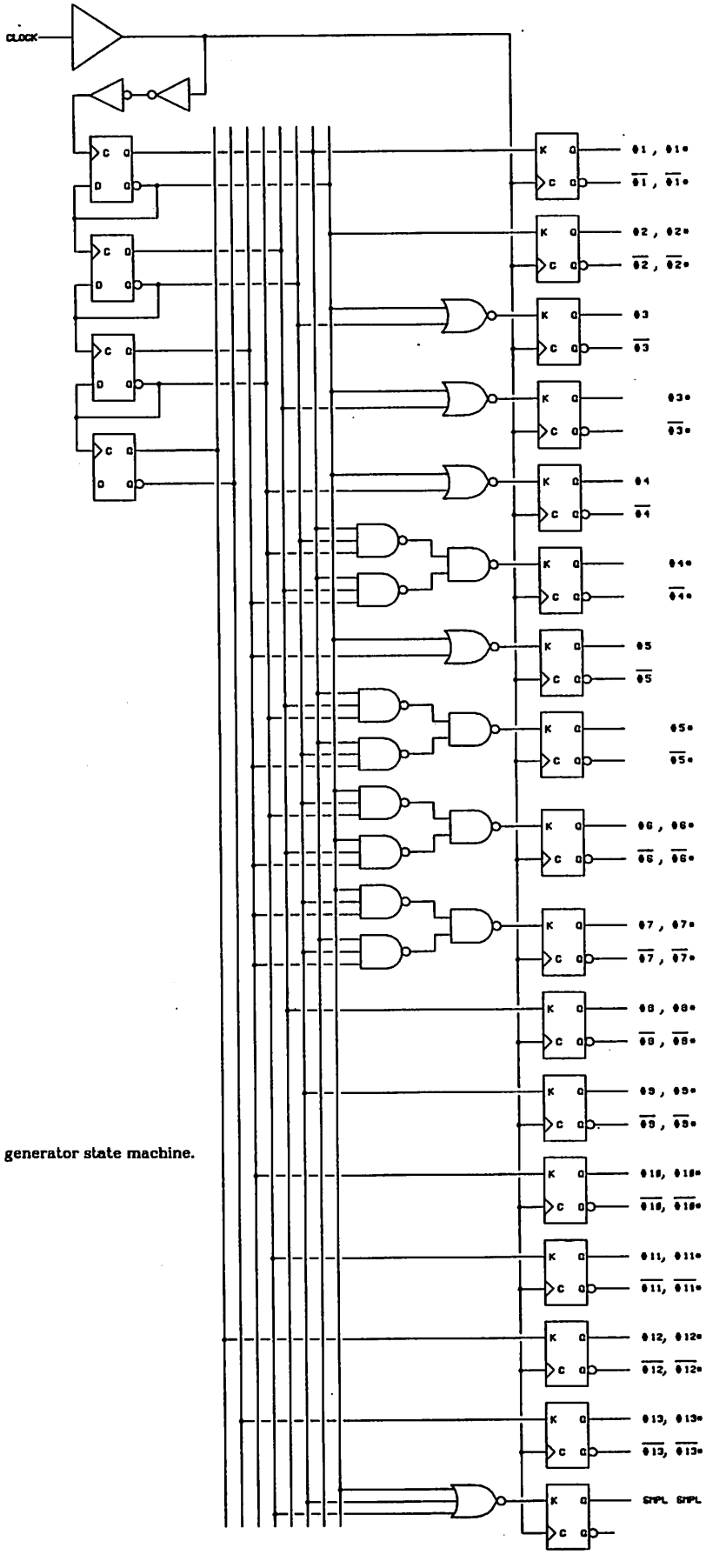

Figure 3.23: Clock generator state machine.

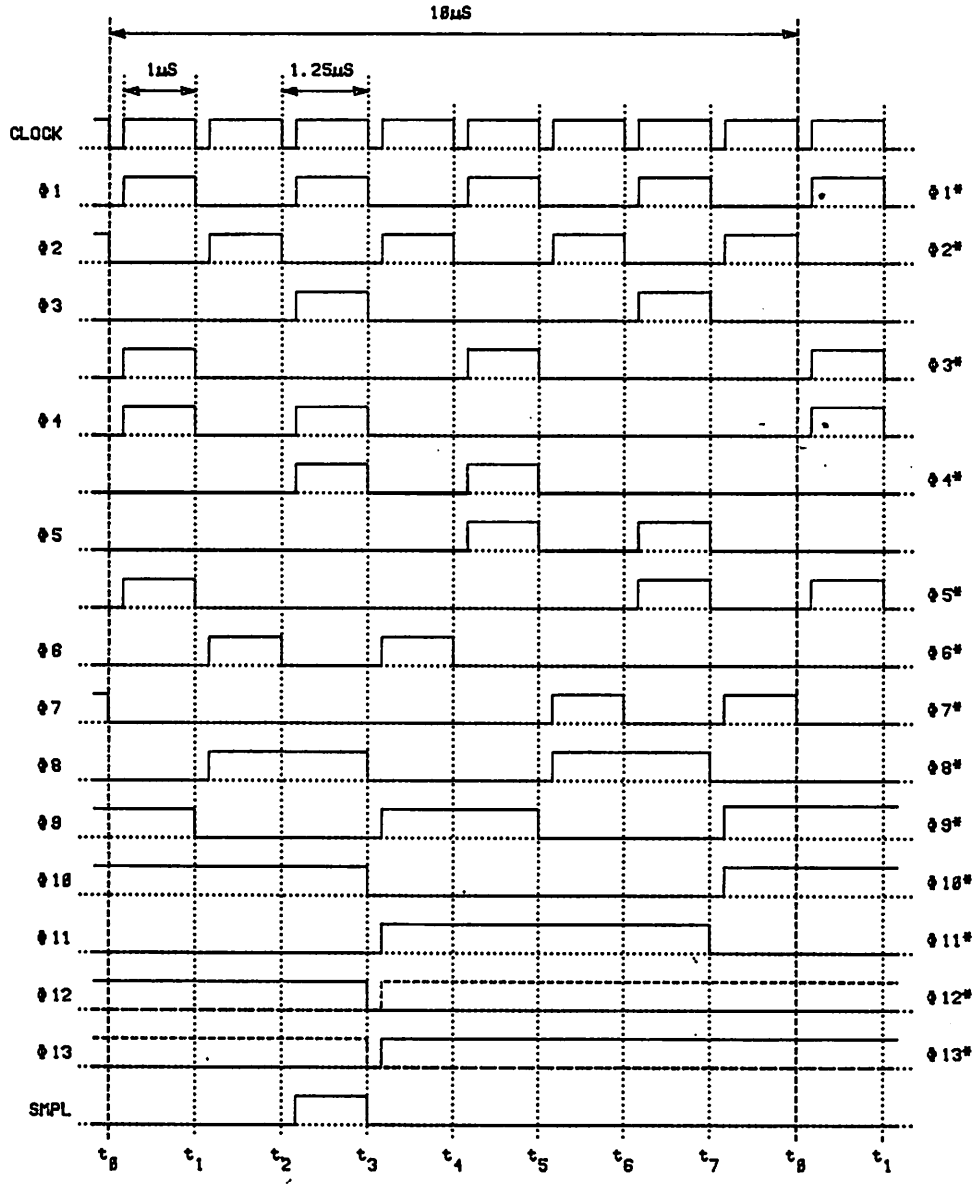

Figure 3.24: Clock generator output signals.

eliminates the possibility of taking data while the detector output is in transition. This signal is high for sample and low for hold. Since there is no buffer stage at the output of the detector, any circuit connecting to the output must be high impedance. There must be no resistive loading, because this will reduce the gain of the last stage and capacitive loading should be 10pf or less. Any more than this and the settling time of the last stage would be degraded, resulting in increased distortion as well as impaired frequency response.

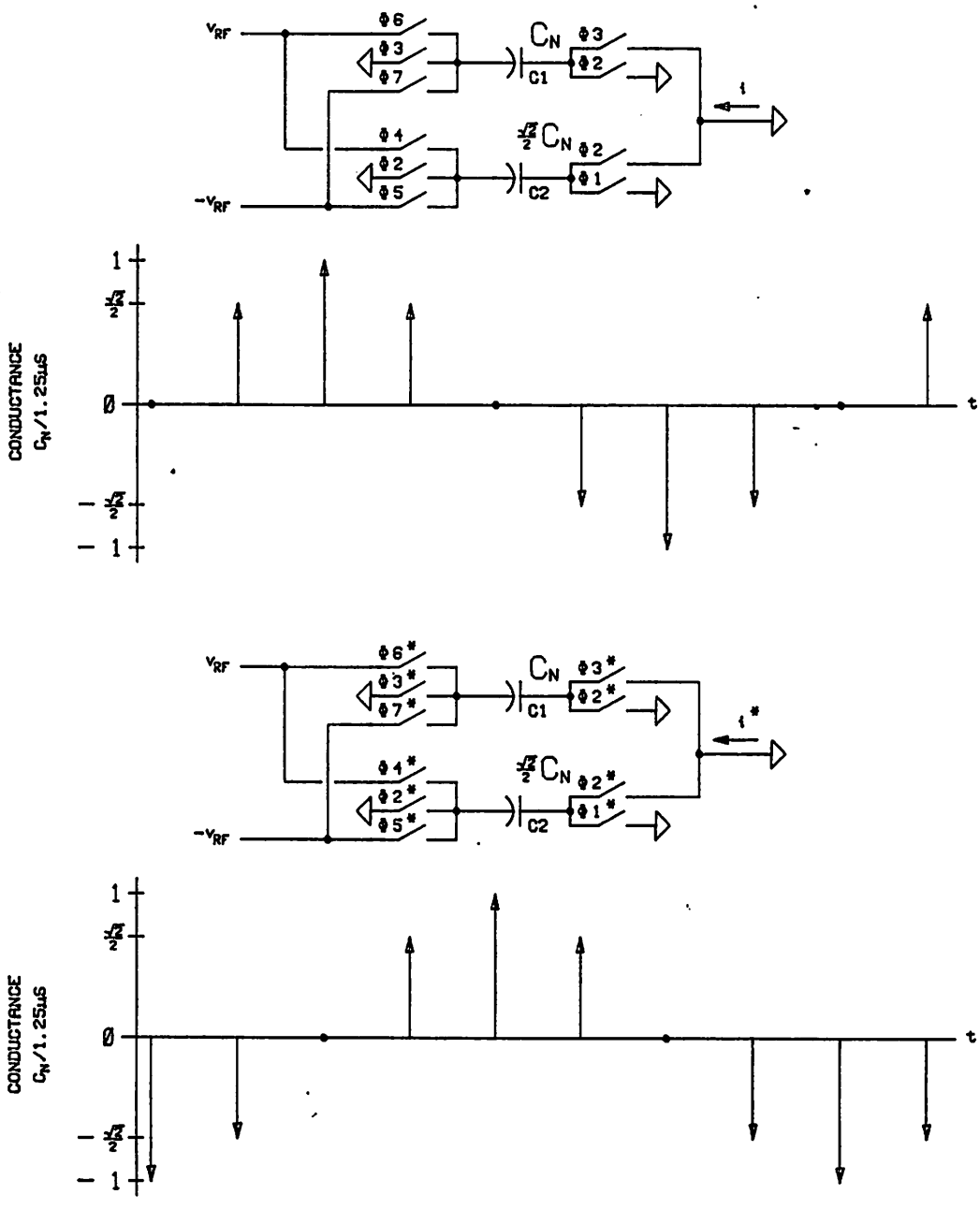

Figure 3.25: Correct phasing of the two quadrature mixers.

Since the detector is sensitive to signals near and above 700kHz, it would be helpful to place a low pass filter in front of the detector. This will tend to reduce the noise output and errors generated by the high order harmonics of the input signal. Since the input of the detector is not buffered, the impedance seen by the input of the detector should be low, less than 1kΩ. This is to prevent the

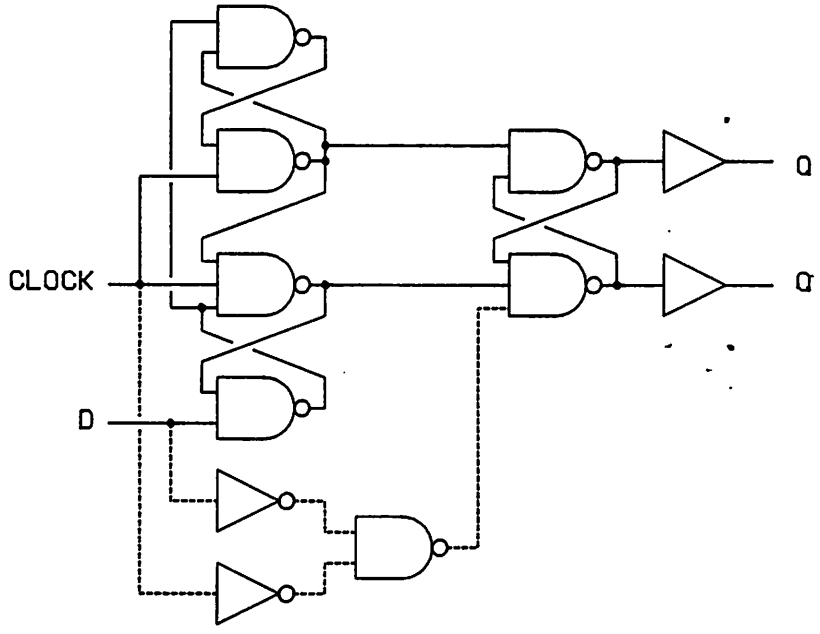

Figure 3.26: Gate level schematic of modified D flip-flop. Dotted line shows difference between modified and conventional D type flip-flops.

generation of distortion and the reduction of the conversion efficiency of the detector. These occur if the input capacitor time constants are increased by the input impedance to a point where the input circuit is not able to settle properly.

Given that the detector is properly used, the specifications shown in figure 3.27 should be achievable. These specifications are rough estimates made from computer simulations made on the individual sections of the circuit. The block diagram of the switched-capacitor detector is shown in figure 3.28.

Conversion efficiency† at	
0kHz	<-80 dB
100kHz	0 dB
200kHz	<-80 dB
300kHz	-60 dB
400kHz	<-80 dB
500kHz	-60 dB
600kHz	<-80 dB
700kHz	0 dB
800kHz	<-80 dB
900kHz	0 dB
1MHz	<-80 dB
bandwidth	4kHz
output noise (0 to 100kHz)	<30μV
maximum output	±4V differential
dynamic range	100 dB
distortion‡	<-70 dB

† Assumes .1% capacitor mismatch.
‡ At maximum output, assumes use of distortion reduction techniques discussed in the next chapter.

Figure 3.27: Estimated CMOS switched-capacitor synchronous detector performance.

3.6 Discrete Switched-Capacitor Synchronous Detector

The discrete version was built to prove the feasibility of a switched-capacitor mixer and to test to see if the topology was correct. Because of the extreme difference between parts available in discrete form and monolithic form, a prediction of monolithic version noise and distortion could not be made based on the discrete version's performance. Because of this the discrete version was greatly simplified. Only one mixer, one filter, and the clock generator was built. Since large dynamic range is not required, the mixer and filter were made single-ended. The schematic of the discrete version is shown in figure 3.29.

The discrete version was operated at LO frequencies of 1kHz, 10kHz, and 100kHz. Capacitor values equal to those used in the monolithic version were used as well as values scaled up by a factor of 100. All combinations of clock rate and capacitor values worked as expected except for the combination of fast

clock and large capacitors. Since the discrete version was built before the bilinear integrator was developed, the circuit was built using the alternating forward and backward difference integrator technique.

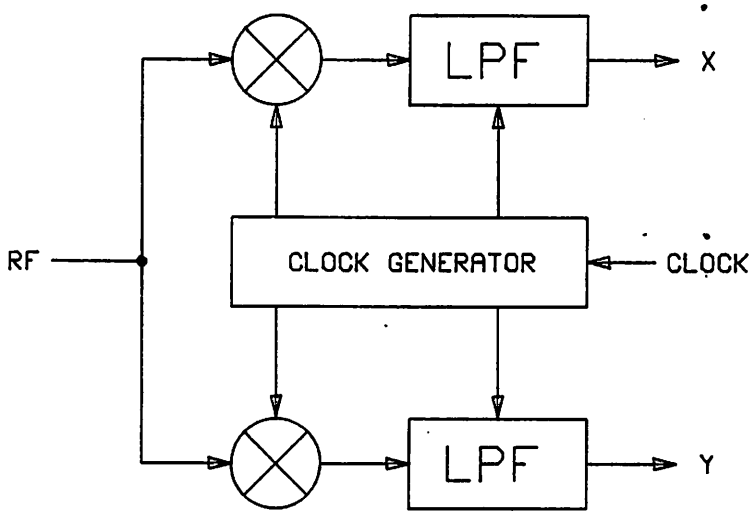

Figure 3.28: Block diagram of switched-capacitor synchronous detector.

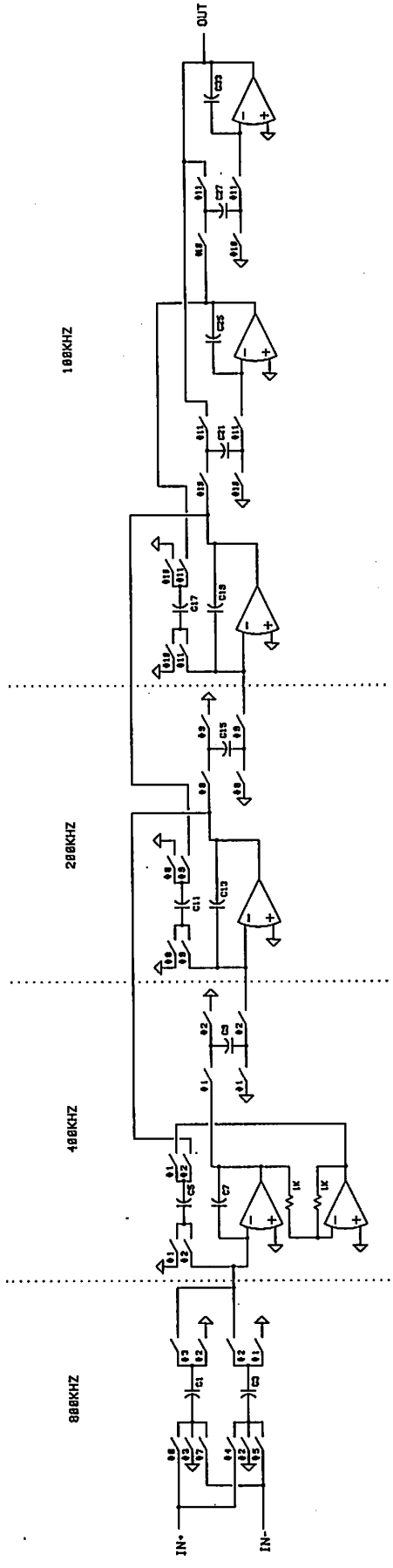

Figure 3.28: Schematic of discrete mixer and filter.

Chapter 4
SWITCHED-CAPACITOR ERROR MECHANISMS

Discussed in this chapter are the sources of error in the detector that are caused by the switched-capacitor nature of the circuit and cannot be easily corrected in post processing. They include noise and distortion. Distortion mechanisms for both monolithic and discrete versions will be presented.

4.1 Noise

There are two inherent noise sources in a switched-capacitor circuit. One is the op amp, which was covered in the previous chapter. The other is the on resistance of the switches. Hsieh [5] showed that this causes a switched-capacitor integrator to exhibit an equivalent noise that is identical to that produced by an RC integrator with equal component values. This noise is called kT/C noise because it is thermal noise with a magnitude that is inversely proportional to the size of the feedback capacitor. This forces die area to be large for low noise designs. Since die area is expensive, it is usually the limiting factor in reducing noise. So thermal kT/C noise in a good design dominates over op amp shot noise.

If the die area reserved for capacitance is fixed and if kT/C noise is dominant over op amp shot noise then going to a differential design will have no affect on the signal to white noise ratio. Though effective signal level is twice as large in a differential approach, the feedback capacitors for each path must be half as large, and this doubles the noise floor. Going to a differential approach does help reduce $1/f$ noise (by 3 dB) and increases rejection of errors such as those from power supply noise and switch parasitics.

When designing mixers, it is important to minimize noise associated with the LO. Both additive noise and phase noise on the LO contribute a noise component to the output of the mixer that is proportional to the input signal level†. This means that when this noise component is dominant, increasing the input signal level will not improve the signal to noise ratio on the output. Because of the limited dynamic range of most spectrum analyzers, this is a hard phenomenon to measure, since the noise floor must be measured while a large output signal is present. The situation is aggravated because the phase noise that is from $1/f$ noise is very close in frequency to the output signal. To minimize this problem the LO should be generated by a low noise crystal oscillator.

4.2 Monolithic Switched-Capacitor Distortion Mechanisms

There are three basic sources of distortion in a monolithic switched-capacitor circuit. They are capacitor nonlinearity, op amp input stage nonlinearity, and MOS switch parasitics. With good design these sources can be minimized. The discussion and arguments that follow are somewhat speculative since they have not been tried in monolithic form. Neither discrete realizations nor computer simulation can accurately predict the distortion created in monolithic circuits.

4.2a Distortion from Capacitors

Distortion from capacitor nonlinearity can be explored using the circuit shown in figure 4.1. This circuit is a single pole filter. If a slowly varying input is applied to this circuit and the integrator is ideal, then the output signal will be

† Additive noise is generally not a problem with mixers that use a switching LO. This is because the mixer is usually insensitive to small changes in the LO signal.

identically equal to the input, independent of C_I and C_F. This means that capacitor nonlinearity does not contribute to distortion. This parallels a similar property in nonresonant LC filters. That is, if the frequency of a signal passing through an LC filter is well within the passband, then capacitor and inductor nonlinearities will not distort the signal. The reason for this behavior in the switched-capacitor case is that the integrator forces the difference between the input voltage and the output voltage to zero. This is a consequence of the virtual short-circuit principle of infinite gain amplifiers.

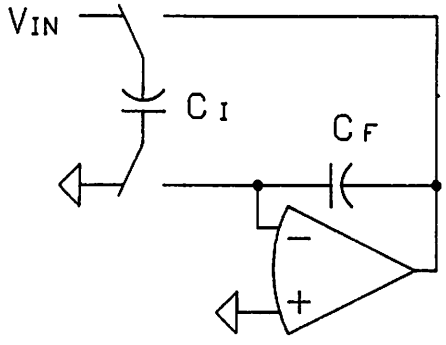

Figure 4.1: One pole switched-capacitor filter.

The immunity to capacitor nonlinearity distortion that the circuit in figure 4.1 enjoys can be extended to multi-stage filters if on each stage the same capacitor samples the input signal as well as the feedback signal. In other words, the filter must be made up of sections like the one shown in figure 4.2a as opposed to the one in 4.2b. Any difference that exists between C_{Ia} and C_{Ib} in figure 4.2b will create a difference between the input voltage and the feedback voltage. This voltage difference may have a significant nonlinear component because the cancellation in the voltage coefficient of C_{Ia} and C_{Ib} is lost. If C_{Ia} and C_{Ib} are laid out closely and similarly, then their nominal capacitance values should be very close. Then if both capacitors are wired such that both top plates tie to the input of the op amp (through a switch), the voltage dependence of the

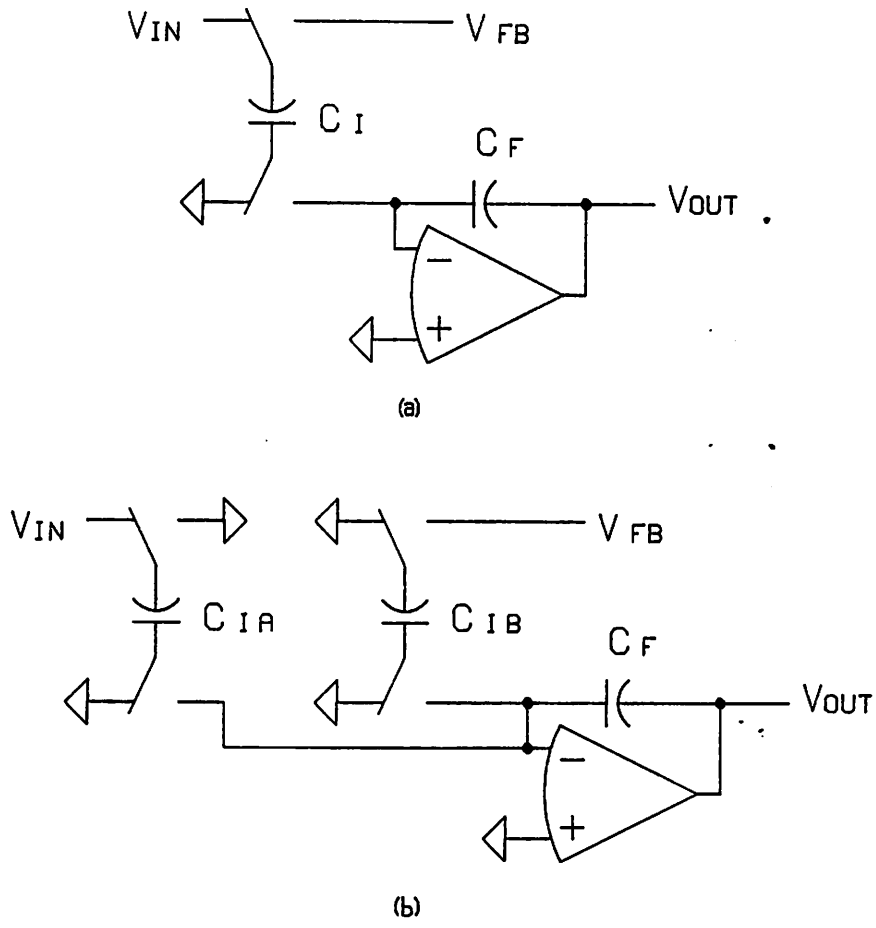

Figure 4.2: Switched-capacitor integrators with; (a) One input capacitor, (b) Separate input and feedback capacitors.

capacitors will cancel and any distortion created will be small.

It was not possible to make the input and feedback capacitors one and the same on all stages of the detector filter because the clock rate is not the same in each stage. This also leads to different values for the input C_{Ia} and feedback C_{Ib} capacitors. Fortunately the feedback capacitor is exactly twice as large as the input capacitor. This means that two capacitors that are identical to the input capacitor can be paralleled to create the feedback capacitor. If these two half-capacitors are then laid out in a common centroid geometry with the input capacitor, the error from capacitor mismatch will be small. Since the voltage on both the input and feedback capacitors is close to identical, the distortion resulting from the voltage coefficient of the capacitors will cancel. This is a

good argument for not using scaling. When scaling the filter, stages are designed so that the peak or maximum voltage possible on each stage is made equal to the maximum voltage that the circuit is capable of handling. This increases dynamic range by allowing each stage to operate with maximum signal level, not just the one with the largest peak signal level. Unfortunately, this means that the quiescent voltages on each stage are not equal, input capacitors must be split as in figure 4.2b, and input capacitor ratios are not integers. As a result the capacitor nonlinearity does not cancel.

Unlike the rest of the capacitors in the detector, the voltage dependence of mixer capacitors does affect the detector's performance. The voltage dependence of these capacitors, and ideally of all capacitors, should be minimized. McCreary [7] showed that this is done by doping the capacitor plates as heavily as possible. His data shows that if the poly plate of a metal-oxide-polysilicon capacitor is doped at 4×10^{18} atoms/cm^3 , a common value, then the voltage coefficient will be near 0.1%, which will create a second harmonic about 60 dB below a 4Vpp signal in this circuit. This poor number emphasizes the need for heavily doped plates, preferably heavier than 10^{20} atoms/cm^3. Since these capacitors are located in the mixer it is difficult to predict the effect of their voltage dependence. It is solely dependent on input voltage, so it can be modeled as a nonlinearity in the input path before the mixer. Harmonics generated by this distortion will to a large extent be rejected by the mixer. Compression will be the dominant effect, but to predict its magnitude, information on the higher order terms in the capacitor voltage-dependence series expansion is needed. This information is not readily available.

4.2b Distortion from Operational Amplifiers

There are two types of distortion present in switched-capacitor filters associated with operational amplifiers. The first type is common memoryless distortion caused by the nonlinearity of the input stage. The second is slew rate limiting.

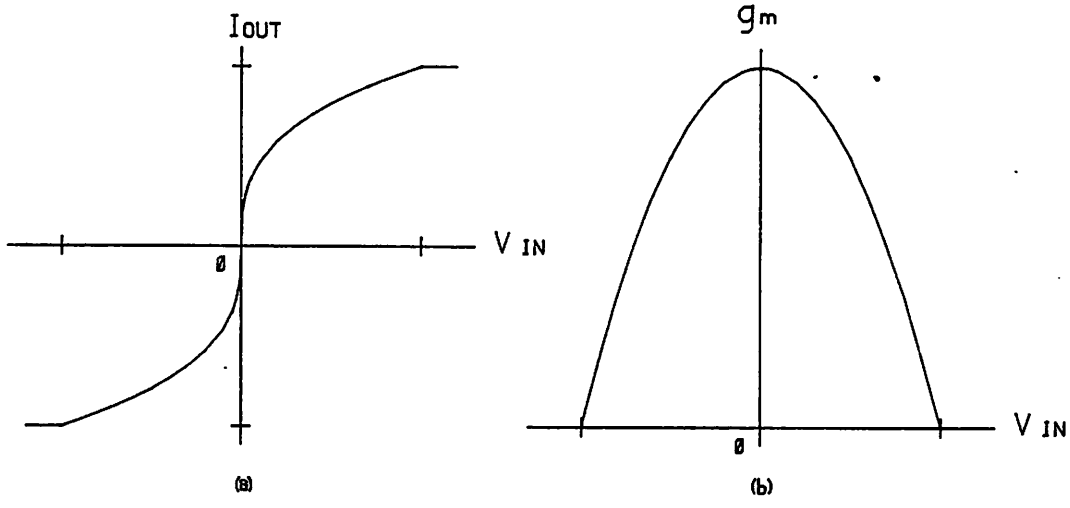

Figure 4.3: Normalized DC transfer curve for source-coupled pair. (a) Output current versus input voltage. (b) Transconductance versus input voltage.

Since the op amp used in the detector is single stage, the input stage is quickly isolated as the source of the memoryless distortion. Figure 4.3 shows the DC transfer curves for the input stage, a source-coupled pair.† Notice that the g_m of the stage falls as the input deviates from zero, which directly results in distortion. The key to reducing this distortion is to keep the input voltage as small as possible. Since this is a feedback amplifier acting in a discrete-time system, that can be done if two conditions are met. First, the DC gain of the amplifier must be large. Second, each stage must completely settle (i.e. the

† For simplicity, only distortion from g_m nonlinearity is discussed. But this is only half the picture. Voltage gain of a single stage amplifier is $A_V = g_m r_o$. The nonlinear output resistance r_o may contribute a significant amount of distortion.

settling time after slew-rate limiting should be at least 10 time constants long) before its output is sampled. This creates the requirement of having the input sampled and held, a function performed by the mixer.

If slew-rate limiting is neglected then the transient response closely resembles the classic one-pole response. The time constant is equal to the reciprocal of the angular closed-loop bandwidth of the amplifier. Thus the differential input voltage of an op amp embedded in a feedback amplifier experiencing a step transient will have the following form

$$V_{IN_{opamp}} = (V_{IN} - \frac{V_{OUT}}{A_{V_{DC}}}) e^{-\omega_{-3dB} t} + \frac{V_{OUT}}{A_{V_{DC}}} \tag{4.1}$$

This is illustrated in figure 4.4. To minimize distortion this input voltage should be minimized at the time the output is sampled. If adequate settling time is allocated, then the last term in equation 4.1 will dominate. This means that distortion will be inversely related to the DC open loop gain of the op amp. Fortunately this gain does not have to be large to reduce distortion to an insignificant level. The minimum gain predicted for the single stage op amp used in this design was near 2000. The maximum output voltage is 2Vp. This results in a maximum settled voltage on the input of the op amp of 1mV. This translates to a g_m modulation of 2ppm and generates third harmonic distortion 135 dB below the fundamental.

If the op amps are given enough time to settle properly, then slew-rate limiting is not a problem for a discrete-time system. If the output is connected to a continuous-time circuit, such as a reconstruction filter, or a discrete-time circuit running asynchronously to the switched-capacitor circuit, such as an analog to digital converter, then problems can result. Slew-rate limiting effectively adds to the output a train of error pulses where both the amplitude and the width of the pulses are proportional to the derivative of the output voltage‡.

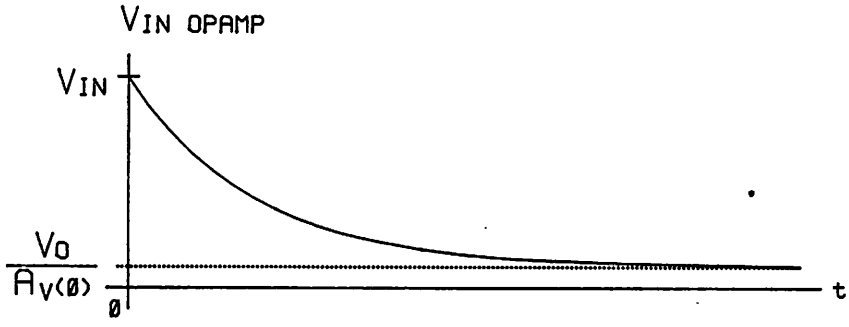

Figure 4.4: Voltage across input terminals of op amp embedded in feedback loop subjected to a step input (slew-rate limiting is neglected).

This is shown in figure 4.5.

If the output of a switched-capacitor circuit is being sampled by another discrete-time circuit such as an analog to digital converter, then the best way to eliminate the effect of slew-rate limiting is simply to synchronize the two circuits. This was provided for in the synchronous detector by providing a sample and hold strobe output. This output strobes the sample and hold after the detector has adequate time to settle.

There are two alternatives to deal with slew-rate limiting when driving a continuous-time circuit. One is to attach a high slew-rate or non-slew-rate limited sample and hold to the output of the switched-capacitor circuit as done above. The other is to increase the slew-rate of the op amps. Since increasing the slew-rate of an op amp usually results in decreasing noise performance, it is best in high performance applications to use a sample and hold. It should be possible to place this sample and hold on chip and eliminate the need for an output buffer.

‡ I would like to give credit to Kwang Lee for this particular view of slew rate limiting.

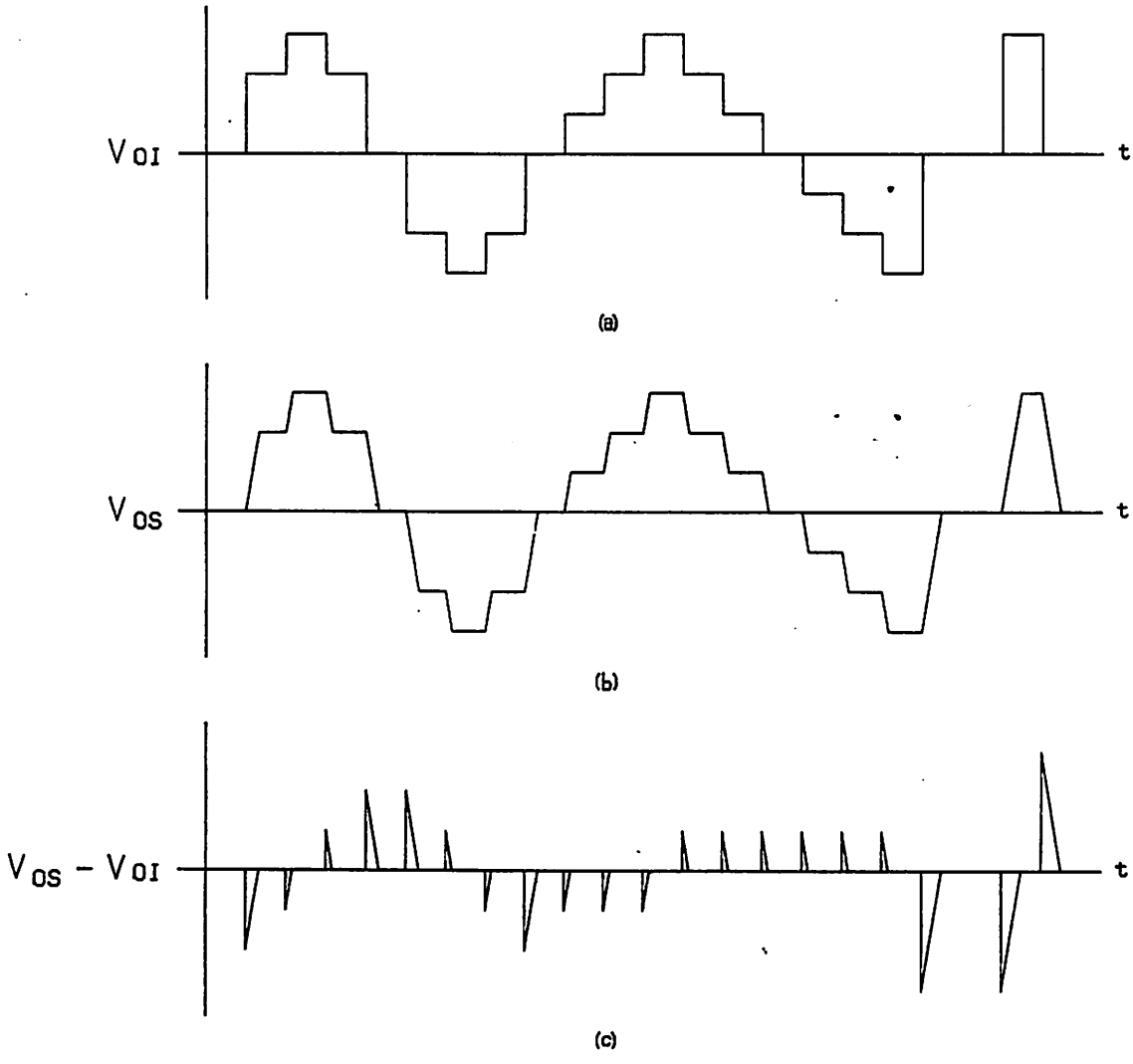

Figure 4.5: Effect of slew-rate limiting on output of switched-capacitor circuit. (a) Ideal arbitrary output voltage. (b) Slew-rate limited version of (a). (c) Error contributed by slew-rate limiting.

4.2c Distortion from the Switch and Capacitor System

The switch and capacitor system inherent to any switched-capacitor circuit creates several types of errors that are not well understood. The analysis of this system is very difficult for realistic conditions and computer circuit simulators do not have models adequate for the task of predicting even the existence of these error mechanisms. Indeed, most simulators are cavalier with the law of conservation of charge, allowing charge to be created and destroyed with little

concern. Since the switch and capacitor system error mechanisms generate errors via small amounts of excess charge, circuit simulators can not be counted on to give reliable predictions for this error mechanism.

There are two basic sources of error in the switch and capacitor system. One is from overlap capacitance and the other is from charge stored in the channel. Error from overlap capacitance can be analyzed by treating the switch and capacitor system as sample and hold.† With the circuit shown in figure 4.6 when the gate voltage goes negative to turn off the device, a small amount of charge is injected onto the hold capacitor from the drain overlap capacitance.

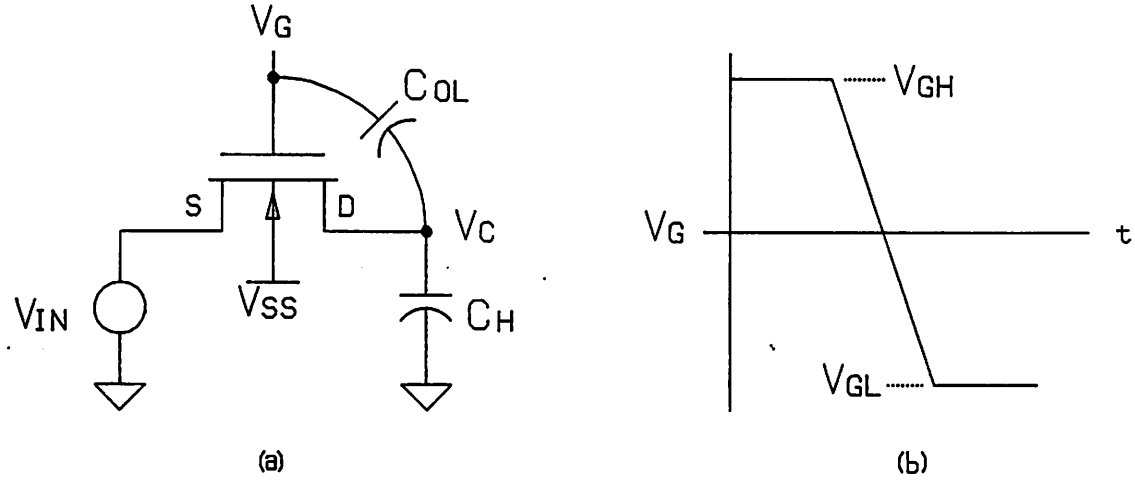

Figure 4.6: (a) Switch and capacitor shown with drain overlap capacitance extracted from MOSFET. (b) Applied gate voltage.

If the gate voltage decreases slowly, then any charge injected onto the hold capacitor while the channel still exists will flow to the input source and does not create an error. Once the channel disappears, the charge that is injected on the hold capacitor is trapped there, creating an offset voltage error. The amount of offset is

† I would like to give credit to Paul Gray for many of the ideas presented on this topic.

$$\Delta V = -\frac{C_{OL}}{C_H}(V_{IN}+V_T-V_{GL}) \qquad \text{where} \quad V_T = V_{TO}+\gamma(\sqrt{\varphi-V_{BS}}-\sqrt{\varphi}) \tag{4.2}$$

where $V_{IN}+V_T$ is the gate voltage at the point where the device turns off. Note that since ΔV changes with V_{IN}, the offset voltage is not simply an offset, but has a gain component as well. Also since V_T is a nonlinear function of V_{IN} (body effect [18]), the offset has distortion components as well. This can be seen if equation 4.2 is expanded.

$$\Delta V = -\frac{C_{OL}}{C_H}[V_{IN}+V_{TO}+\gamma(\sqrt{\varphi+V_{IN}-V_{SS}}-\sqrt{\varphi})-V_{GL}] \tag{4.3}$$

$$\Delta V = -\frac{C_{OL}}{C_H}\{V_{IN}+V_{TO}+\gamma\sqrt{\varphi-V_{SS}}[1+\frac{1}{2}\frac{V_{IN}}{\varphi-V_{SS}}\frac{1}{8}\left[\frac{V_{in}}{\varphi-V_{SS}}\right]^2 + \frac{1}{16}\left[\frac{V_{IN}}{\varphi-V_{SS}}\right]^3-\cdots]-\gamma\sqrt{\varphi}-V_{GL}\} \tag{4.4}$$

$$V_C = V_{IN}-\frac{C_{OL}}{C_H}[V_{TO}+\gamma(\sqrt{\varphi-V_{SS}}-\sqrt{\varphi})-V_{GL}+\left[\frac{\gamma}{2\sqrt{\varphi-V_{SS}}}\right]V_{IN} - \frac{\gamma}{8\sqrt{(\varphi-V_{SS})^3}}V_{IN}^2+\frac{\gamma}{16\sqrt{(\varphi-V_{SS})^5}}V_{IN}^3-\cdots] \tag{4.5}$$

Equation 4.4 was generated by applying Newton's binomial expansion to equation 4.3 and equation 4.5 assumes $\Delta V = V_C - V_{IN}$ where V_C is the final voltage held on the storage capacitor and V_{IN} is the input voltage at the instant the channel disappears. This shows that the hold voltage has offset, gain, and distortion terms. If typical values are substituted into equation 4.5, then offset and gain errors would have values between 1% and 0.1%. Second harmonic distortion would be near -90 dB while third would be below -100 dB. But this is a crude analysis. The assumption that the gate voltage changed slowly is not valid.

If the gate voltage is allowed to change rapidly, the charge injected onto C_H while a channel still exists is not totally allowed to flow into the source because of the non-zero and increasing resistance of the channel. This creates an

additional error that is dependent on the input voltage because channel on resistance varies greatly with input voltage. This means the numbers presented for the slowly changing gate voltage could get worse, but not by more than about 6dB. This is simply because C_{OL} is usually small, especially with modern self-aligned processes.

The other basic source of error in the switched-capacitor system also occurs when the gate voltage is allowed to change rapidly. When the gate voltage drops rapidly, the charge in the channel is not allowed a slow and orderly migration to the input source. Instead the charge has to evacuate quickly through one of three paths, out the source to the input voltage source, into the substrate by recombination, or out the drain into the hold capacitor. The amount of the charge in the channel is given by [18]

$$q_C = \frac{\varepsilon_{OX}}{t_{OX}}(V_{GH} - V_{IN} - V_T)WL \tag{4.6}$$

It is typically a much greater than the injected charge from overlap capacitance. It is also a nonlinear function of V_{IN} because of body effect. Therefore the error generated by q_C also has offset, gain, and distortion terms.

The fate of the channel charge is harder to predict than the charge from overlap capacitance. It does seem though, that once charge injection from overlap capacitance slightly decreased the voltage on the hold capacitor, there would be a weak electric field created across the channel that would act to draw the negative electrons from the channel to the input voltage source. This assumes C_H is small. This would tend to reduce the error, but it is unclear whether this effect is at all significant. One thing that is clear though, is that the rate of change of the input voltage does affect the fate of the channel charge. If, when the device has just turned off, the input voltage has a positive derivative, the channel electrons will be attracted and flow to the source. If the derivative

is negative the channel electrons will be repelled and flow to the drain and the hold capacitor. This results in an error that has strange properties, which can be explored by applying bandlimited white Gaussian noise to the input with zero mean and variable variance or amplitude. When the amplitude of the noise is small, the input signal has no affect on the channel charge and no distortion errors are created. If the amplitude of the noise is increased a threshold is passed where the input begins to have an affect on the fate of the channel charge. As the amplitude is further increased it will have more and more affect on the fate of the channel charge until finally the fate of the charge is completely determined. By this it is meant that, at some times all channel charge is flowing out the source, and at other times it all flows out the drain.

At this threshold the peak to peak error has reached its maximum for the amount of charge present and it may be dominating over the input voltage. If the input signal is further increased, the variance of the output signal will increase only slightly. This increase results from the larger amount of channel charge available because of the larger swing of the input voltage. If the input signal is further increased, a point will be reached where the input signal again dominates over the error. This is diagramed in figure 4.7. This curve is somewhat speculative, since little data on the error versus input signal level was taken.

During the transient when V_{GS} is less than V_T, but a channel still remains, the device can be considered to be in saturation because $V_{GS}-V_T < V_{DS} \approx 0$. This means that the device could have a large amount of gain. It is possible for a small voltage on the input to control a sizable portion of the channel charge, which could create an output error voltage that is significantly larger than the input voltage. This was observed while using a commercial DMOS FET and a 500 pf capacitor.

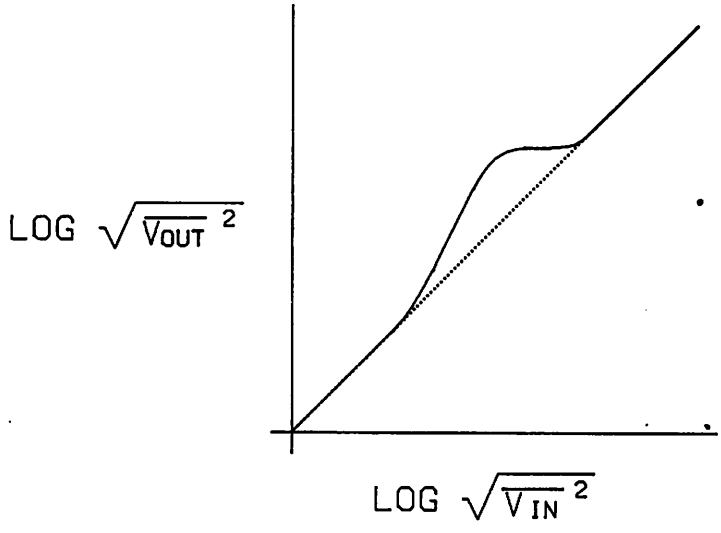

Figure 4.7: Variance of the output voltage versus the variance of a white noise input to a clocked switch-capacitor system.

Gain and distortion errors from both overlap capacitance and channel charge that result solely from input voltage variations, but not from input voltage derivatives, can be eliminated by using the circuit and clocking scheme shown in figure 4.8. In this scheme switch M2 opens before switch M1 and switch M4 opens before switch M3. This means that if parasitics are neglected, the error charge generated by M1 and M3 is rejected from the hold capacitor because there is no current path from the top plate when these switches open. The error charge on the remaining switches, M2 and M4, is independent of the input voltage because these switches are always at ground potential. This means they contribute no gain or distortion errors. The derivative of the input voltage will be present on these switches as they open though, so this circuit is not immune from that error. Fortunately this is only a problem for the input stage.

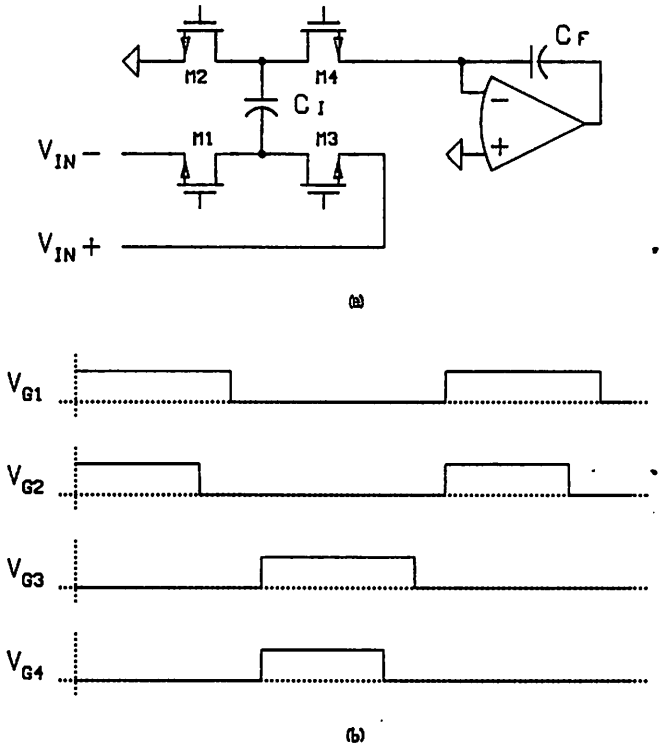

Figure 4.8: Quadriphase clocking scheme to eliminate gain and distortion errors that result from the switch-capacitor system.

To reduce all errors associated with the switch-capacitor system it is important to follow these basic guidelines:

- Always use minimum length devices for switching.
- To the extent that settling time constraints allow, use as large a storage capacitor as possible and make switch device width as small as possible.
- Use differential topology.
- Do not use excessive gate voltage swing.
- Minimize body effect.

Discrete Switched-Capacitor Distortion Mechanisms

The discrete prototype was built using LF356 Bi-FET op amps, LF13331 Bi-FET switches, and NPO ceramic multilayer capacitors. The fact that JFET switches were used rather than MOS switches leads to significant differences in distortion mechanisms between the discrete and the monolithic versions.

Three basic versions of the circuit were tried. First a low speed version was built using capacitor values 100 times larger than those chosen for the monolithic version (from 1nf to 10nf) and an LO frequency 100 times slower (1 kHz). This circuit resulted in distortion below the noise floor (-80dB) of the spectrum analyzer used. If the LO frequency was increased, distortion became measurable at 10kHz and increased slowly until 50kHz, at which point the distortion increased drastically. This is shown in figures 4.9 and 4.10.

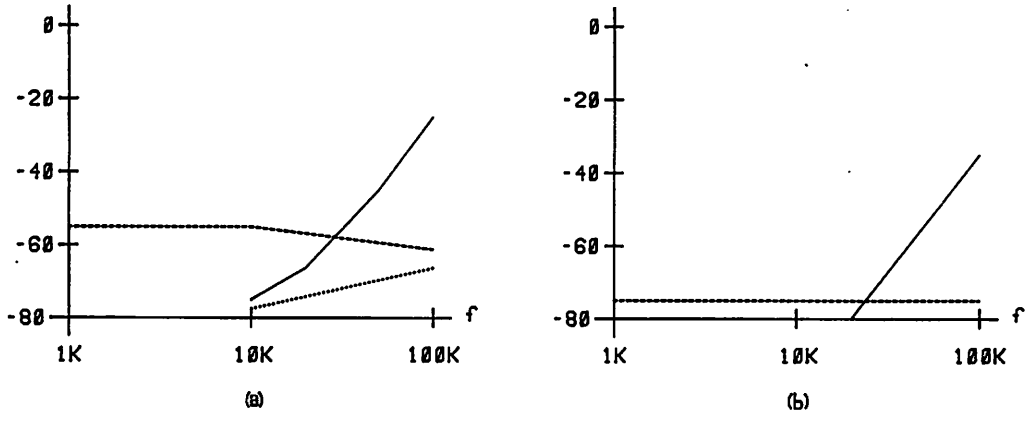

Figure 4.9: Distortion (dB) versus LO frequency with input voltage equal to 10Vpp for; large capacitor circuit (solid), small capacitor circuit (dashed), and quadriphase clock circuit (dotted). (a) Second harmonic distortion. (b) Third harmonic distortion.

The second version was identical topologically to the first but the capacitors were reduced to being equal in value to the ones used in the monolithic version. Its distortion performance was poorer at low frequencies but worked well with a 100kHz LO.

The third circuit used the quadriphase clock scheme shown in figure 4.8. The small capacitor values were used. This significantly reduced distortion at low frequencies, giving performance better than the large capacitor version. The performance advantage over the small capacitor scheme was only marginal with a 100kHz LO.

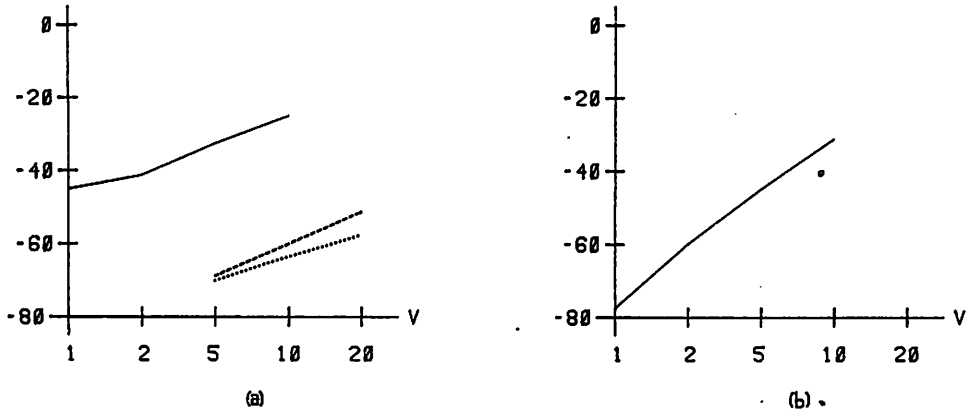

Figure 4.10: Distortion (dB) versus input voltage (Vpp) with LO frequency equal to 100 kHz for; large capacitor circuit (solid), small capacitor circuit (dashed), and quadriphase clock circuit (dotted). (a) Second harmonic distortion. (b) Third harmonic distortion.†

Distortion in the large capacitor version is primarily caused by insufficient settling time because of the large switch-capacitor time constants. At 100kHz only about 2 time constants are allocated for RC settling, which causes significant errors from nonlinear switch resistance, op amp nonlinearities, and time constant mismatch. Another significant error source is charge loss in the switch. Because of the particular switch used, it is possible to forward bias the gate-drain junction of the PFET switch if the drain becomes more positive than the source. This is likely to occur during transients in any of the circuits used, but is particularly acute in the case where large capacitor values are used at high clock rates.

In the small capacitor version the dominant distortion mechanism is charge injection from the switches' nonlinear gate capacitance. This is neatly eliminated when the quadriphase clock scheme is used. At high clock rates a different distortion mechanism becomes important that is not eliminated by the quadriphase clock. This distortion probably results from the op amps not fully

† Third harmonic distortion was unmeasurable on the small capacitor and quadriphase clock circuits even with 20Vpp input voltage.

settling.

The discrete circuit was built to test over-all circuit integrity and distortion performance. The circuit performed as expected, which is shown by the circuit's response to a gated sine wave applied to its input. See figure 4.11. Noise performance of the prototype was not measured. It was felt that the large difference between the discrete and monolithic version's op amps and switches would make comparisons between the two meaningless.

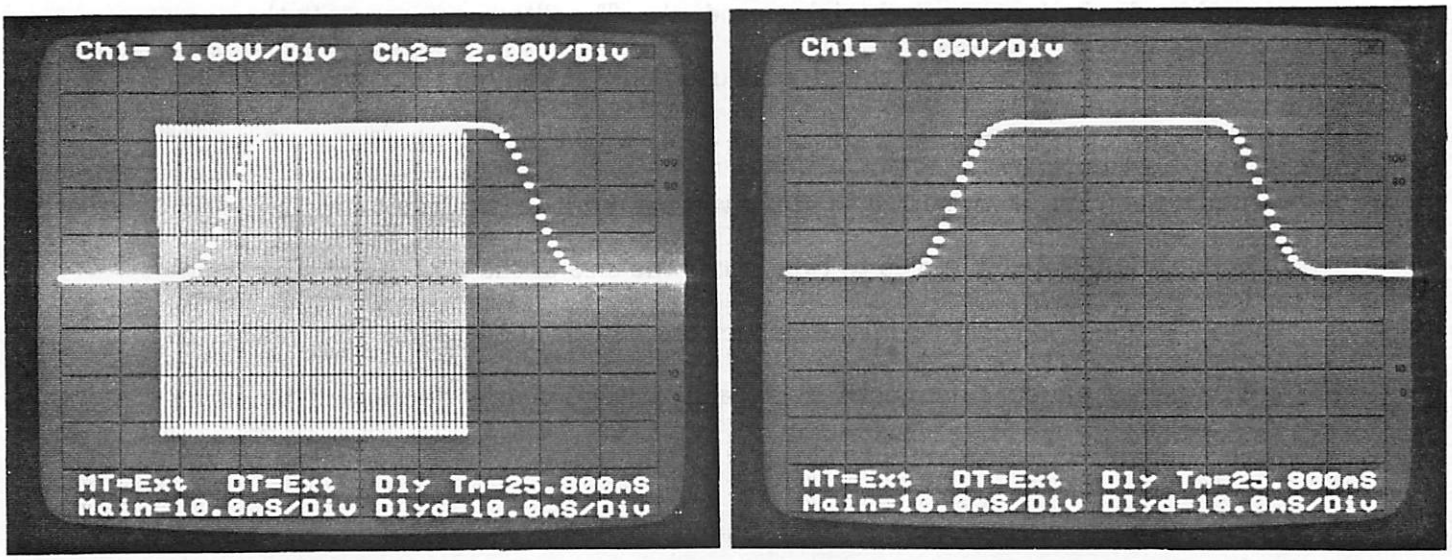

Figure 4.11: Pulse response of discrete detector with 1kHz LO. (a) Input signal and output response. (b) Output response alone.

Chapter 5
CONCLUSION

As is often the case, now that the design is complete, it was found that there are changes that could be made that would improve performance. The bilinear integrator was developed late, and its capabilities were not fully utilized because of inertia. Using the bilinear integrator it is possible to reduce the number of filter poles significantly. This is true since integrator response nulls can be placed to eliminate unwanted mixing products. The filter requirements then can be greatly relaxed, because the filter is used only to reduce the noise bandwidth of the output. It seems that a two pole filter would be optimum since it would combine good transient response at a given bandwidth and circuit simplicity. By reducing the number of poles to two, either the size of the circuit can be considerably reduced or the size of the capacitors can be increased. This results in better performance since both noise and distortion are decreased by using larger capacitors.

It is unclear what level of performance is achievable. Though this thesis covered the dominant error mechanisms in switched-capacitor circuits, the emphasis was on the mechanisms themselves rather than their absolute contributions to output error. This is because circuits were not fabricated and therefore no measurements could be made. Unbelievably, there has been little usable information about distortion published in the literature, so nothing can be inferred about the magnitude of the problem from this source. Fortunately there is literature available on noise performance and it appears from Hsieh et al. [4] that a noise floor of $700nV/\sqrt{Hz}$ is achievable in a five pole low pass filter.

In conclusion this thesis suggests that low distortion and frequency conversion are two tricks that can be added to the list of capabilities of switched-

capacitor techniques. These two results are achieved by using two circuits introduced in this thesis. Lower distortion is possible by using careful design practices and the quadriphase scheme for eliminating switch errors, and frequency conversion is produced by using the interleaved mixer. Another circuit that was introduced in this thesis was the parasitic-insensitive bilinear integrator. With these three circuits and the myriad of other standard switched-capacitor circuits it is possible to design and build high performance circuits. In particular, the desired high performance synchronous detector is possible.

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