HIGH PRECISION ANALOG CIRCUITS USING MOS VLSI TECHNOLOGY

by

Robert Chen-Tai Yen

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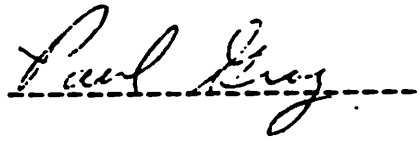

Paul R. Gray
Chairman of Committee

ABSTRACT

This dissertation describes new circuit techniques for improving signal resolution in MOS circuits. Various error sources such as 1/f noise and switch channel charge injection commonly encountered in MOS circuit designs were discussed. Simple models were presented for qualitative understanding of the physical mechanisms of these error sources.

The proposed circuit techniques have been demonstrated through the implementation of an NMOS switched capacitor instrumentation amplifier. This amplifier achieves 1 mV typical input offset voltage, greater than 95 dB PSRR, 120 dB CMRR, 0.15% gain accuracy, 0.01% gain linearity, and an rms input referred noise voltage of 30 uV per sample. It is concluded that the realization of an on-chip high precision analog data acquisition system using MOS VLSI technology is entirely feasible.

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Finally, I owe a special note of appreciation to my wife-classmate-research partner. Vivian Shen. for her continuous support and patience throughout the course of my Ph.D work.

DEDICATION

I would like to dedicate this dissertation to my parents. Rong-Chiao Yen and Lai-Chiu Tang. and to my wife Vivian Shen. Their confidence and patience with me made this work possible.

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CHAPTER 1 - INTRODUCTION

The rapid increase in MOS IC complexity which has occurred over the past few years has created the need to implement complete analog-digital systems on the same IC using MOS technology. Therefore, the implementation of analog functions in MOS technology has become more important [1].

Recently, several NMOS microprocessors with the A/D converter on chip have been described in the literatures [2]. Often such systems are required to interface directly with low-level transducers which produce small difference signal with large common mode signal superimposed. Traditionally, the analog functions implemented in MOS technology suffer from poor performance due to poor S/N ratio, slow speed, and large parasitic coupling among different signal paths. This is mainly due to the facts that MOS devices inherently display a large 1/f noise, and has a relatively small transconductance. This problem is further aggravated by the low voltage gain per stage in a NMOS circuit due to the body effect of the MOS transistor. A factor which often introduces significant amount of error in MOS switched capacitor circuits is the switch channel charge injection. Because of the unpredictable nature of

the switch channel charge injection under different circuit conditions. this has been the dominant error in the past.

The objectives of this dissertation are to study the elements which limit the signal resolution in MOS circuits; to devise circuit techniques which allow the realization of on-chip analog data acquisition systems for VLSI signal processing microcomputers which approach the fundamental limits of signal resolution imposed by the thermal noise of MOS transistors. The feasibility of the proposed circuit techniques are demonstrated through the development of an experimental instrumentation amplifier.

In the following Chapter 2. noise sources of a MOS operational amplifier are discussed. Noise power transfer function for each noise source to the output of the operational amplifier is also derived. Chapter 3 deals with switch channel charge injection. A distributed MOS model is presented for the computer simulation and understanding of switch charge injection mechanism. Several circuit techniques are also introduced to cure this problem. Chapter 4 describes circuit techniques for the implementation of a MOS switched capacitor instrumentation amplifier and sample/hold function. Balanced circuit configuration coupled with symmetric layout is used to achieve first-order cancellation of switch channel charge

injection and improvements of common mode and power supply rejection ratio. Double correlated sampling technique is employed to reduce circuit dc offset, low frequency noise, and to improve PSRR for dc or low frequency power supply variations. A special charge redistribution scheme is also described to allow the circuit CMRR to be independent of operational amplifier's CMRR, thus resulting in a very high overall common mode rejection ratio The circuit design for the experimental circuits are also described in Chapter 4. In Chapter 5, the experimental results of the circuits are presented to demonstrate the concept developed in this research. Finally, Chapter 6 contains the conclusion of this dissertation and future development in analog MOS circuits.

CHAPTER 2 - OPERATIONAL AMPLIFIER NOISE

Operational amplifiers and comparators are basic building blocks in many electronic circuits. Because of the incompatibility of inductors, and large precision resistors and capacitors in VLSI technology, the use of operational amplifiers in active circuits to simulate these passive components' function becomes essential in VLSI circuits. Also, because of the ever increasing computational power of VLSI digital processors. many analog signal processing systems are gradually being replaced by digital signal processing systems. The transition from an analog signal to a digital signal imposes strict requirements on the signal to noise ratio (S/N) and speed of an analog to digital converter of which, operational amplifier and comparator are the fundamental building blocks.

In general. a comparator can be considered as an operational amplifier operated in open loop condition. Thus. the S/N considerations for a comparator are very similar to those for an operational amplifier except the latter is bandlimited by a larger frequency compensation capacitor. Therefore, in this section only the noise behavior in an operational amplifier is treated.

SECTION 2.1 - Dominant Noise Sources in MOS Op-Amp

2.1.1 1/f Noise of MOS Transistors

One of the largest error source which limits the signal resolution in an analog MOS circuit is the low frequency noise associated with MOS devices. This noise source is generally termed as flicker noise. or 1/f noise due to its 1/f frequency dependence on its spectral density.

Flicker noise in an MOS transistor arises from random trapping [3] of the channel charge into the energy states at the interface between the silicon substrate and the silicon dioxide dielectric. This noise is most significant when associated with a direct current. It is because trapping and releasing of the channel charge modulates the current.

For an MOS transistor biased in the saturation region, the equivalent input referred 1/f noise voltage power spectrum density [4] is :

$$Veq^2 = k/(Cox*ZL*f)$$

k is a constant proportional to the number of the surface

states. It depends strongly on the fabrication process involved, and usually has a fairly large variation. Z is device channel width. L is device channel length. Cox is the gate capacitance per unit area. f is the frequency. It is obvious from the above equation that the equivalent input referred 1/f noise decreases with device area. This area dependence has also been observed by many other authors [5.6.7].

Fig.2.1 and Fig.2.2 show the measured equivalent input referred noise spectral density of both NMOS and PMOS devices for various geometries for a typical process [6]. For a device with W/L=100u/5u and biased in the saturation region with biasing current at 10 uA. the NMOS device exhibits a noise voltage spectral density of about 300 nanovolts per root hertz at 1 kHz. A corresponding PMOS device has only 70 nanovolts per root hertz at the same frequency. Thus. in a typical NMOS operational amplifier with NMOS differential input stage W/L=100u/5u. biasing current =10uA. the equivalent input referred noise voltage would be in the range of 320 uV. A corresponding CMOS amplifier with a PMOS differential input stage will have an equivalent input referred noise voltage of only 65 uV. Although no theoretical analysis has been reported to explain this phenomenon, an intuitive explanation still can be made.

The surface trapping states usually are located closer to the conduction band rather than the valence band. The hole has an effective mass which is a lot greater than that of an electron. Therefore, the hole would need more kinetic energy than the electron to jump into the surface state which lies between the conduction band and valence band. Because of the Boltzman's approximation, which indicates an exponential relationship between the kinetic energy a particle has and its jumping probability [8], much fewer holes will jump and get trapped in the Si-O2 interface states in a PMOS device than that of electron in an NMOS device.

If we observe the noise voltage spectral density of Fig.2.1 and Fig.2.2 more closely, we would find out that the corner frequency of this 1/f noise is somewhere between 10 kHz and 100 kHz, and 80% of its noise power is concentrated in the frequency range below 1 kHz. This particular feature indicates that the 1/f noise is highly correlated. Thus it is possible to reduce this 1/f noise by using a double correlated sampling circuit technique [Appendix A].

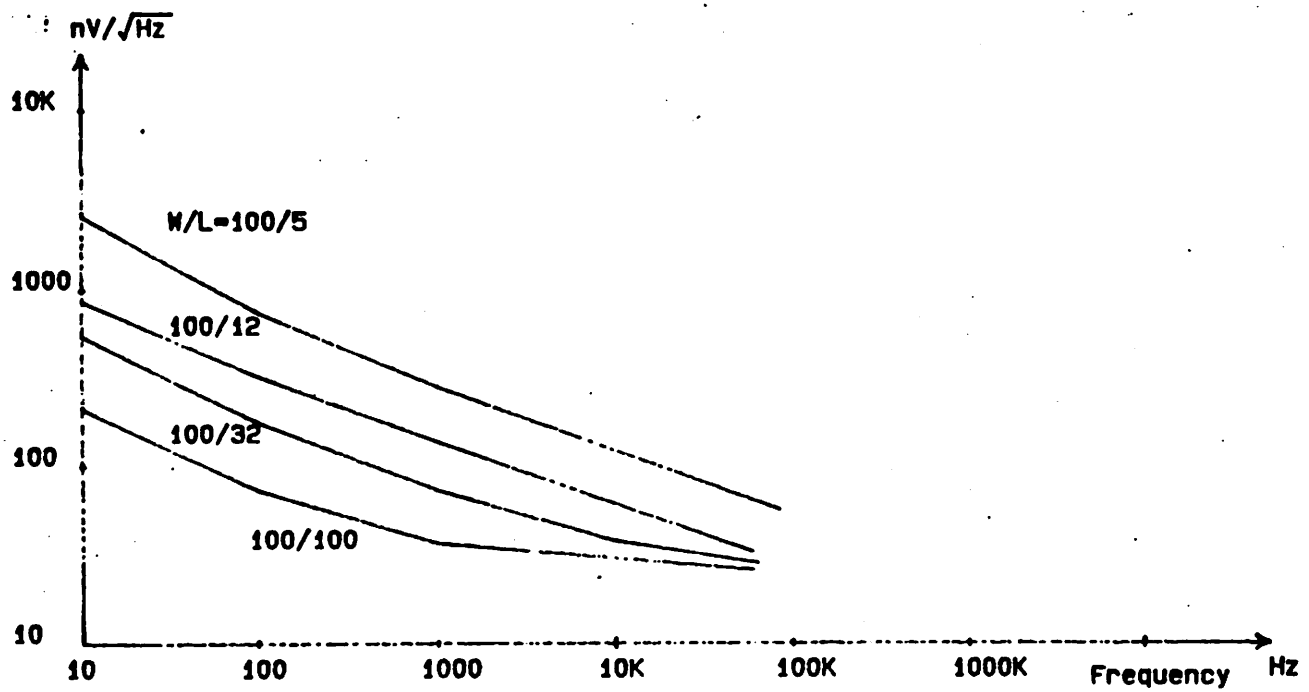


Fig.2.1 Equivalent Gate Input Noise of NMOS Devices

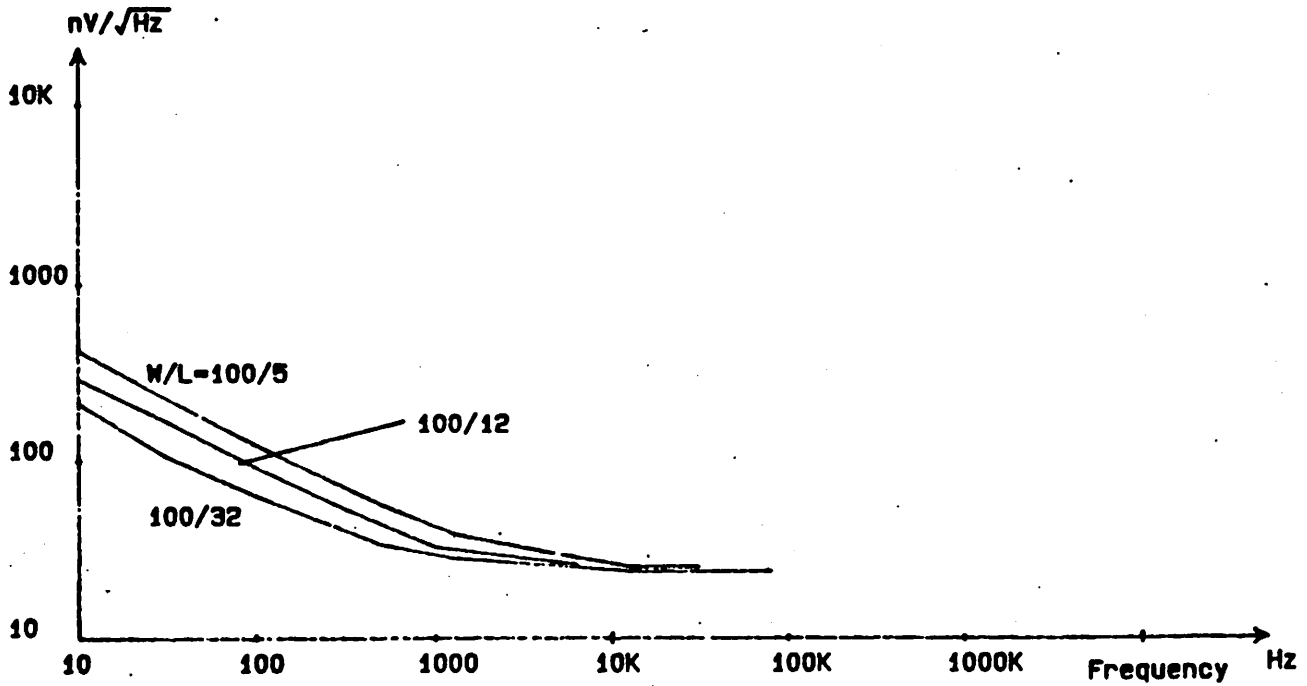


Fig.2.2 Equivalent Gate Input Noise of PMOS Devices

2.1.2 Thermal Noise of MOS Transistors

Any physical resistor exhibits a thermal noise which is the result of the random thermal motion of the carriers. The thermal noise voltage power spectrum density is represented by the equation:

$$\overline{V_{eq}^2} / f = 4KTR$$

K is the Boltzman's constant. T is the absolute temperature in Kelvin. R is the resistor value. Note that the noise power spectral density is constant with respect to frequency. It is flat up to the frequency range higher than most frequency range we are normally interested in [9]. Therefore. this thermal noise is also called white noise or just wide-band noise.

A MOS transistor is a device which forms an electrical channel to conduct current. This electrical channel is a physical path which has physical resistance. Thus, the MOS transistor also exhibits thermal noise as a normal resistor does. The channel resistance of an MOS transistor is a strong function of its bias condition. For the MOS transistor biased in the saturation region. its equivalent thermal resistance is [10] :

$$Req = (2/3)*Gm$$

$$Gm = (uCox*2I*W/L)^{1/2}$$

Gm is the transconductance of the MOS device. I is the biasing current. Thus, the noise power density for an MOS device in saturation region is given by the equation:

$$Veq^2 = 4KT(2/3Gm)$$

For the MOS transistor biased in the linear region, the equivalent thermal noise power spectral density is :

$$Veq^2 = 4KT/Gm$$

$$Gm = uCox*(Vgs - Vt)*W/L$$

As an example, the typical noise spectrum of an NMOS device with W/L=100u/5u operated in saturation region at a drain current of 50 uA would be about 30 nV per root hertz.

SECTION 2.2 - Noise Power Transfer Function of an Op-Amp

Most MOS operational amplifier configurations [4,11] employ two high gain stages followed by a near unity gain buffer with low output impedance, as shown in Fig.2.3. The equivalent input referred noise source of each stage is labelled as Vn1, Vn2, and Vn3 as shown in Fig.2.4. The simplified small signal equivalent circuit for this typical op-amp architecture with these noise sources is shown in Fig.2.5.

gm1 and ro1 are the transconductance and output resistance of the input stage respectively. gm2 and ro2 are the transconductance and output resistance of the second stage respectively. av3 and ro3 are the voltage gain and output resistance of the output stage respectively. C1. C2, and C3 are the parasitic capacitance at the ouput nodes of the corresponding stages. Cc is the Miller compensation capacitor.

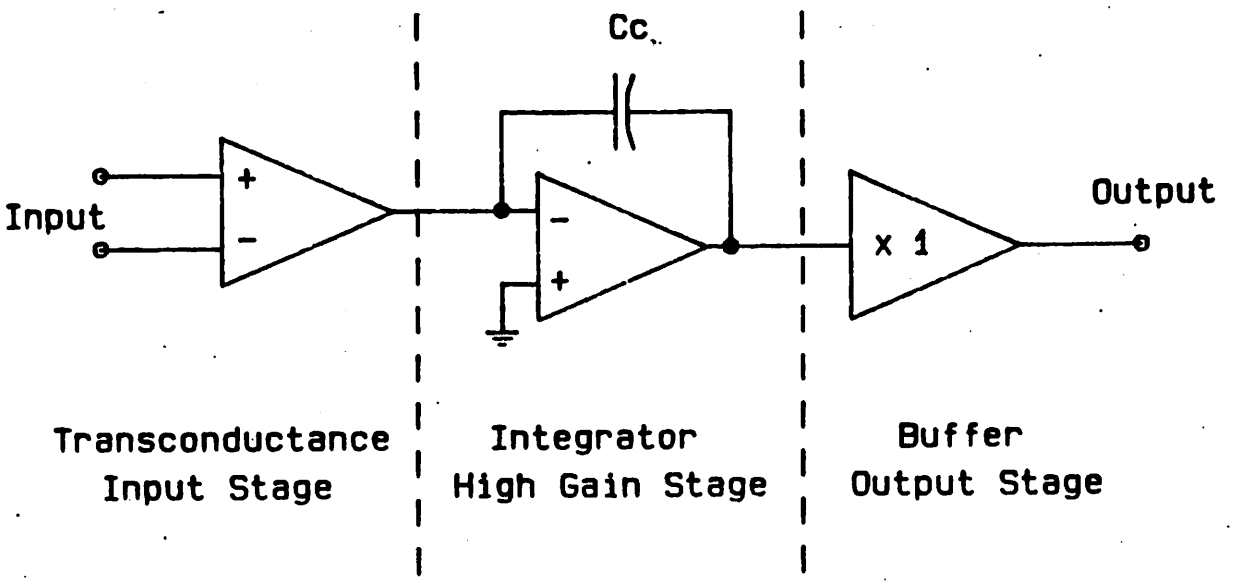


Fig.2.3 Typical Op-Amp Block Diagram

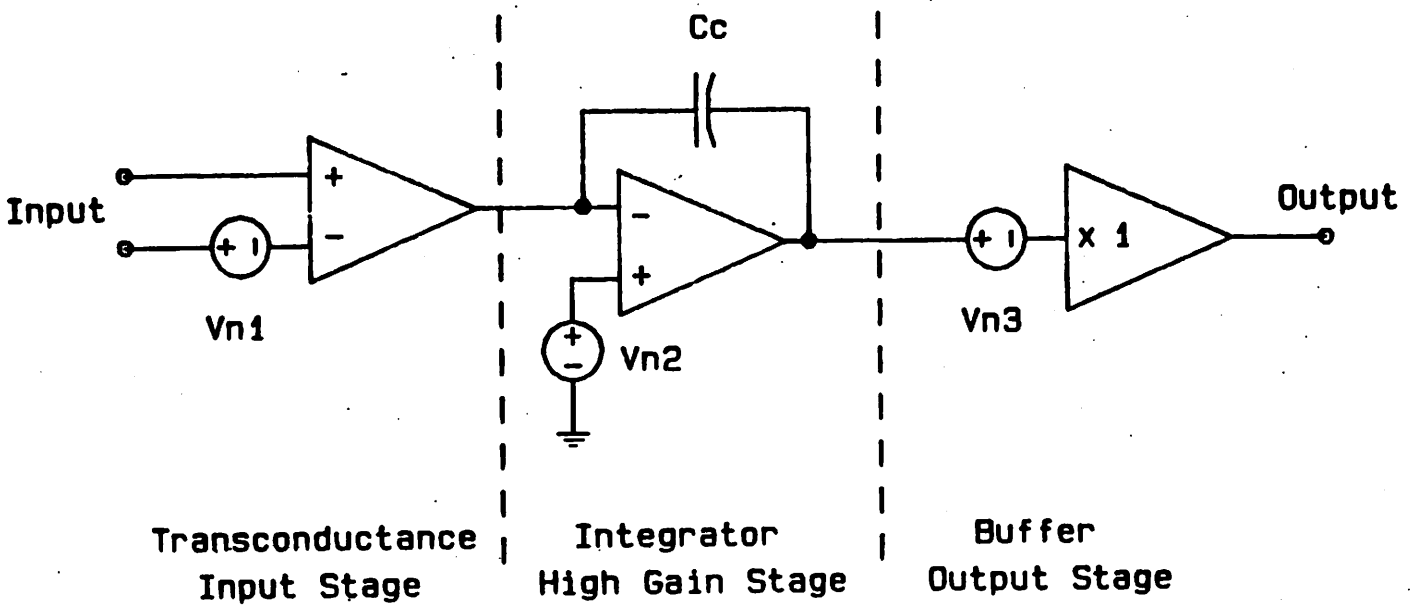


Fig.2.4 Equivalent Input Noise Source at Each Stage of an Op-Amp

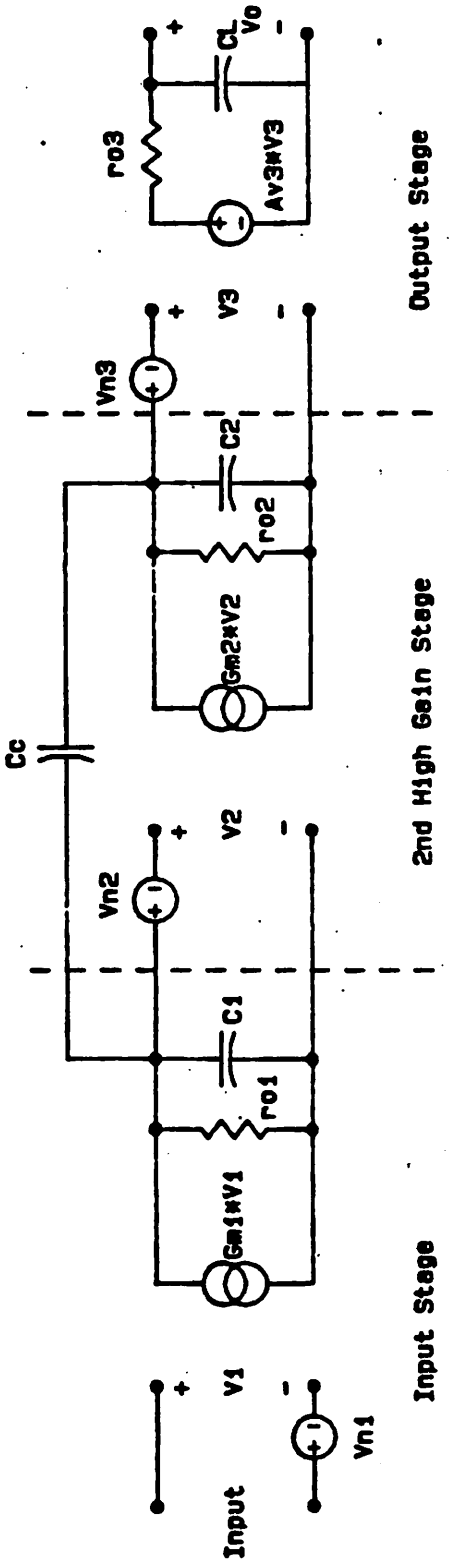


Fig.2.5 Small Signal Equivalent Circuit of an Op-Amp

Using nodal analysis [12] on Fig.2.5 to obtain the transfer functions from each noise source to the output of op-amp :

$$H1(S) = [Vo(s)/Vn1(s)]$$
$$= \{[Gm1*ro1*Gm2*ro2*(1-s*Cc/Gm2)]$$
$$* [Av3/(1+s*ro3*CL)] / D(s) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

where

$$D(s) = 1 + s*[ro2*C2+ro1*(Cc+C1)+Gm2*ro2*ro1*Cc]$$
$$+ s^2*ro2*ro1*[C1*C2+Cc*C2+Cc*C1]$$

$$H2(S) = [Vo(s)/Vn2(s)]$$
$$= \{ Gm2*ro2*(1+s*ro1*(C1+Cc))$$
$$* [Av3/(1+s*ro3*CL)] / D(s) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

$$H3(S) = [Vo(s)/Vn3(s)]$$
$$= \{ Av3/(1+s*ro3*CL) \} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3)$$

Av3 is the voltage gain of the output stage which is less than unity. In typical op-amp designs [10]. gm2 is usually much larger than gm1 to ensure a good frequency response. Input stage voltage gain gm1*ro1 is also designed to be much larger than one in order to obtain good power supply rejection and low input referred offset voltage. Thus,

$$gm2 >> gm1 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (4)$$

$$gm1*ro1 >> 1 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (5)$$

$$gm2*ro1 >> 1 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (6)$$

$$gm2 >> 1/ro1 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (7)$$

$$gm2/Cc >> 1/[ro1*(Cc+C1)] \quad \ldots\ldots\ldots \quad (8)$$

equation (8) is valid because the Miller capacitance Cc is usually larger than the parasitic capacitance C1 to obtain effective Miller compensation [13]. From equations (1). (2) and (3), the ratio of the output noise contributed by these three noise sources Vn1. Vn2 and Vn3 are :

$$H1(S)/H2(S) = [\, gm1*ro1*(1-s*Cc/gm2) \,] / [1+s*ro1*(Cc+C1)] \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (9)$$

$$H1(S)/H3(S) = [Vo(s)/Vn1(s)] = [Gm1*ro1*Gm2*ro2*(1-s*Cc/Gm2)]/ D(s) \quad \ldots \quad (10)$$

$$H2(S)/H3(S) = [Vo(s)/Vn2(s)] = Gm2*ro2*(1+s*ro1*(C1+Cc))/ D(s) \quad \ldots\ldots\ldots \quad (11)$$

For frequencies $w < 1/[\ ro1*(Cc+C1)\ ]$

$$H1(S)/H2(S) \sim [\ gm1*ro1\ ] \gg 1$$

$$H1(S)/H3(S) \sim [\ gm1*ro1\ ]/\ [\ w*ro1*Cc\ ] \gg 1$$

$$H2(S)/H3(S) \sim [\ gm2*ro2\ ]\ /[\ w*gm2*ro2*ro1*Cc\ ] > 1$$

For frequencies

$$1/[ro1*(Cc+C1)] < w < gm1*ro1/[ro1*(Cc+C1)]$$

where $gm1*ro1/[ro1*(Cc+C1)] = gm1/(Cc+C1) \ll gm2/Cc$

$$H1(S)/H2(S) \sim [\ gm1*ro1\ ]\ /[\ w*ro1*(Cc+C1)\ ] > 1$$

$$H1(S)/H3(S) \sim [\ gm1*ro1\ ]\ /[\ w*ro1*Cc\ ] > 1$$

$$H2(S)/H3(S) \sim [\ gm2*ro2\ ]\ /[\ w*gm2*ro2*ro1*Cc\ ] < 1$$

For frequencies $gm1/(\ Cc+C1\ ) < w < gm2/Cc$

$$H1(S)/H2(S) \sim [\ gm1*ro1\ ]\ /[\ w*ro1*(Cc+C1)\ ] < 1$$

$$H1(S)/H3(S) \sim [\ gm1*ro1\ ]\ /[\ w*ro1*Cc\ ] < 1$$

$$H2(S)/H3(S) \sim [\ ro1*(\ C1+Cc\ )\ ]\ /[\ ro1*Cc\ ] \sim 1$$

For frequencies $w > gm2/Cc$

$$H1(S)/H2(S) \sim [gm1*ro1*Cc] / [gm2*ro1*(Cc+C1)]$$
$$\sim gm1/gm2 \ll 1$$

$$H1(S)/H3(S) \sim [gm1*ro1*ro2*Cc*w]$$
$$/ [w*ro1*ro2*Cc*(gm2+w*(C1+C2))]$$
$$\sim gm1 / [gm2+w*(C1+C2)] \ll 1$$

$$H2(S)/H3(S) \sim [gm2*ro1*ro2*Cc*w]$$
$$/ [w*ro1*ro2*Cc*(gm2+w*(C1+C2))]$$
$$\sim gm2 / [gm2+w*(C1+C2)] < 1$$

Fig.2.6 illustrates the relative contribution of the output noise power due to the noise sources Vn1, Vn2, and Vn3 with repect to frequency. It is obvious from Fig.2.6 that for the frequencies less than the unity gain bandwidth of the op-amp, gm1/Cc, the total output noise is dominated by the noise source of the input stage Vn1. As the frequency increases toward the second stage feedforward zero frequency, both the second stage noise source Vn2, and output stage noise source Vn3 dominate the total output noise power. For frequencies larger than gm2/Cc, the second stage voltage gain falls below unity. Hence only the output stage noise source Vn3 is important.

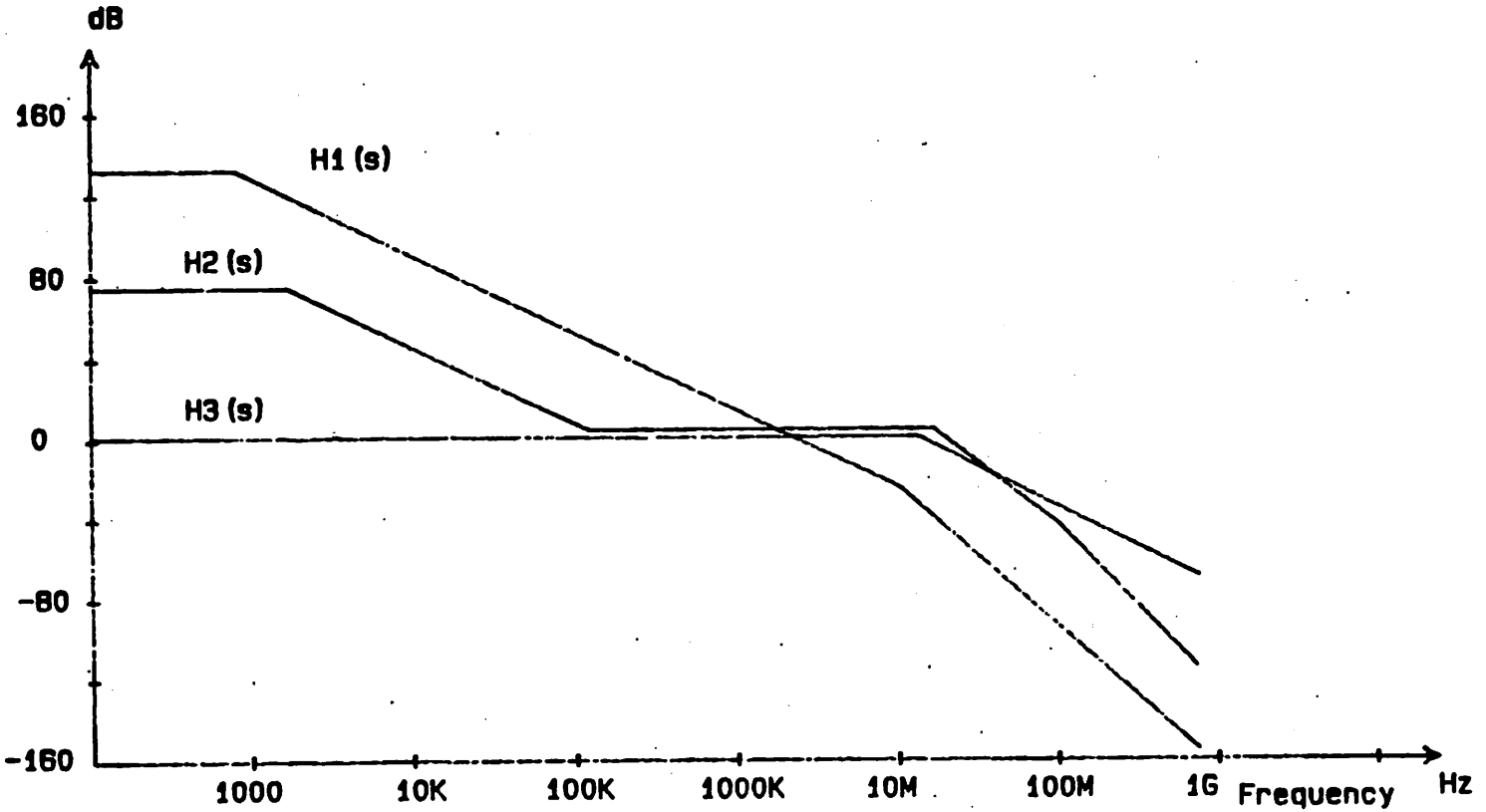


Fig.2.6 Output Noise Power Transfer Function of a Typical MOS Op-Amp

SECTION 2.3 - Simplified Operational Amplifier Noise Model

In a typical MOS operational amplifier, the corner frequency of the 1/f noise is anywhere from 1 kHz to 100 kHz depending on the factors mentioned in the previous section. In most cases, the corner frequency of this 1/f noise will be much lower than the unity gain frequency of an MOS operational amplifier, gm1/Cc which is on the order of 1 MHz or higher. Thus, from equation (12), for frequency range w < gm1/Cc, only the input stage noise source Vn1 is critical. The 1/f noise power of the op-amp contributed by the second gain stage and output stage would be much less than that of the input stage. Therefore, it is sufficient to consider just the input referred 1/f noise of the first stage.

The other important noise source in an MOS op-amp is the wide-band thermal noise due to the relatively low transconductance of an MOS device. Because this noise has a frequency range much larger than the unity gain bandwidth of an operational amplifier, it would be necessary to model this noise source into two parts. The first one is the equivalent input referred noise of the input stage, level shift, and gain stage of an op-amp. This noise is to be band-limited by op-amp's compensation capacitor. The second

one is the equivalent output referred noise of the output stage. This output stage thermal noise is to be band-limited by its own bandwidth or by its external loading capacitance.

The simplified noise model of an MOS op-amp is illustrated in Fig.2.7. Only two equivalent noise sources are required here to model the noise behavior of a typical MOS op-amp. E1, includes dc offset, 1/f noise, and the thermal noise of the input stage. E2, represents the thermal noise of the output stage. For power supply noise frequencies much lower than the unity gain frequency of the operational amplifier, it is also possible to model the effect of power supply variation into an equivalent input referred offset variation. Therefore, the dc offset, 1/f noise, broadband thermal noise, and power supply variation can all be modelled by the equivalent noise sources shown in Fiq.2.7.

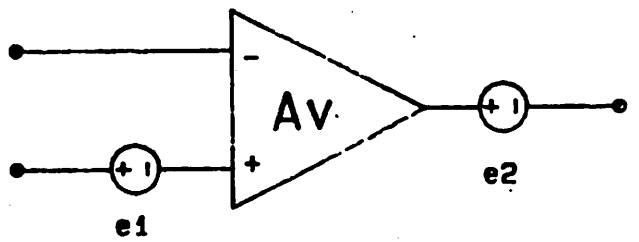


Fig.2.7 Simplified Noise Model of a MOS Op-Amp

CHAPTER 3 - MOS SWITCH INDUCED ERRORS

MOS switches are indispensable in MOS VLSI circuits such as switched capacitor filters. A/D, D/A converters. and many types of digital circuits. However, MOS switches often introduce significant amounts of error [1] due to clock feedthrough, channel charge injection, and channel resistance thermal noise. The error voltage introduced by the MOS switch is one of the fundamental sources that limit the accuracy of many MOS circuits.

Shown in Fig.3.1 is an MOS sample and hold circuit. The switch is connected to a sampling capacitor which is to be charged to the input signal level.

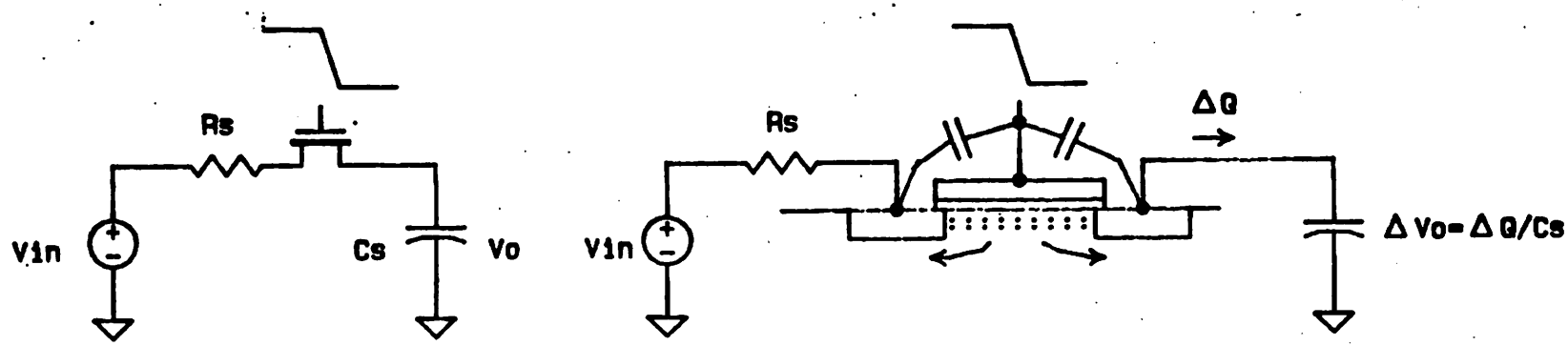


Fig.3.1 Channel Charge Injection and Clock Feedthrough of MOS Switch

When the switch is turned off, the amount of channel charge injected into the sampling capacitor will cause an error voltage on the sampling capacitor as a result of the sudden release of the charge under the gate of the switch. The clock feedthrough from the gate-drain and gate-source overlap capacitance also contribute to the error. The amount of clock feedthrough voltage is usually determined by the ratio of the gate to source/drain overlap capacitance and the sampling capacitance. However, the amount of channel charge that flows into the sampling capacitor as opposed to the amount that flows back to the input terminal is a complex function of the gate voltage fall time. input impedance level, and the size of the sampling capacitor [14]. For a typical switch size of 10X10 micron and a sampling capacitor of 5 pF, a 5 volt gate overdrive will introduce an error of 20 mV if half of the channel charge flows into the sampling capacitor.

In this chapter, a simple distributed MOS model is proposed to interpret the turn-off process of MOS switches under different conditions. Using this simple model, the dependence of channel charge injection error on the clock fall time. fabrication, and loading conditions can be found. The qualitative results obtained from computer simulation using this model agree very well with the experimental results.

SECTION 3.1 - Simplified Distributed MOS Model

A complete treatment of MOS device modelling can be found in many literatures [15,16]. In this section, we only intend to propose a simple distributed MOS model for the interpretation and simulation of the channel charge injection phenomenon of an MOS transistor qualitatively. The simple parameters used in this model can be modified easily.

3.1.1 MOS Transistor Model

The conventional MOS model [17] used in most circuit simulation programs [18] is shown in Fig.3.2. The first and second order effects of short channel MOS transistor are modelled using the following pertinent equations [19].

Threshold voltage variation due to substrate bias and short channel effect.

Saturation due to the scattering limited drift velocity of carriers and voltage-dependent output conductance.

Surface field dependent mobility.

Weak inversion conduction.

Charge controlled model of regenerative effects.

Temperature effects.

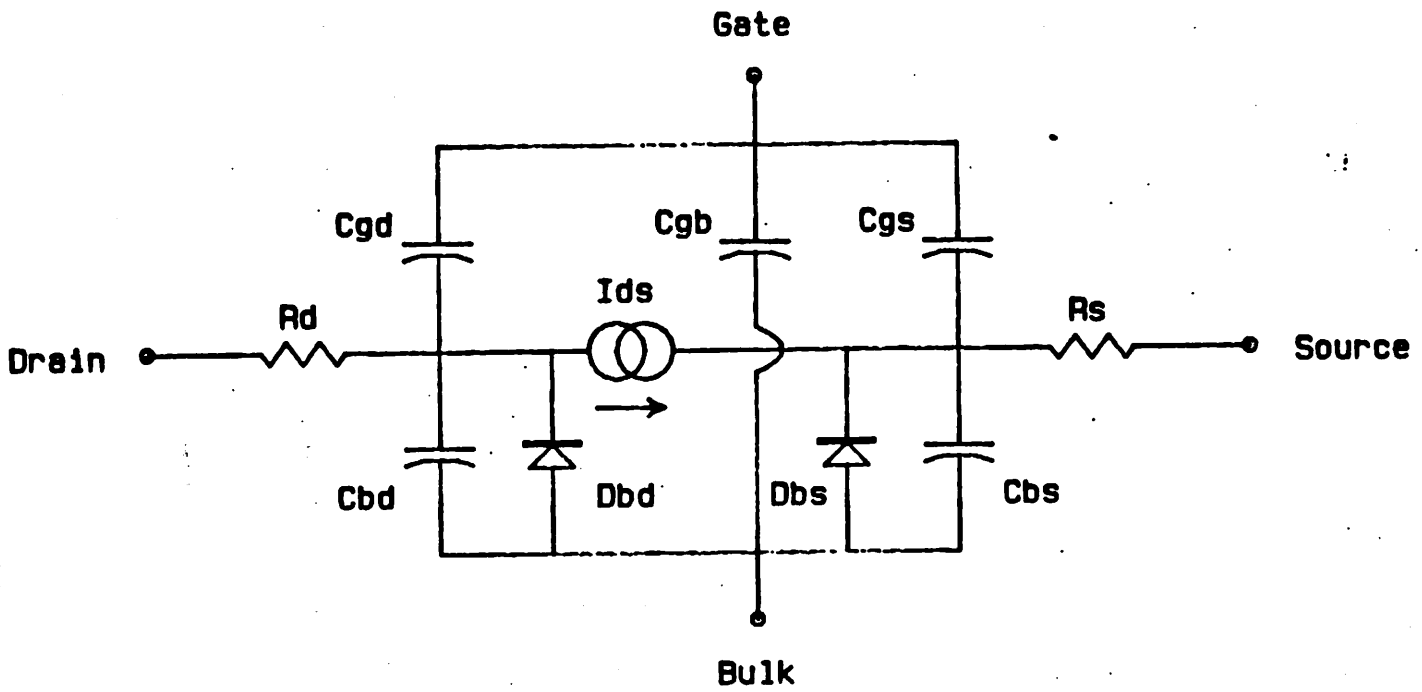


Fig.3.2 Typical MOS Model Topology Used in Computer Simulation Programs

Although the MOS model used in SPICE [18] is sufficient in simulating most MOS digital and analog circuits, the simulation of a precision switched capacitor MOS circuit still presents problems due to non-conservation of charges, and the exclusion of the charge pumping effect.

This problem is partially solved by the incorporation of charge-oriented model proposed by Ward and Dutton into SPICE [20]. The charge oriented MOS model is based on the actual distribution of charge in the MOS structure; the current at any node is related to the time derivative of the charge contained. In other words, the whole set of MOS equations used in this charge oriented model is based on the calculation of charge instead of just voltage and current. However, this model does not include the charge pumping effect nor consider the distributed channel case. This model regards the MOS channel as a voltage controlled current source with its current level be the time derivative of the charge contained at the corresponding nodes. Therefore, this model is neither adequate for the simulation of precision switched capacitor MOS circuits, nor for the estimate of their transient behavior qualitatively. A more sophisticated model would give more accurate results, but is not suited for use in circuit simulators because of the increased complexity [21].

3.1.2 Distributed MOS Transistor Model

The proposed distributed MOS model shown in Fig.3.3 is comprised of a number of small MOS transistors M1. ... , M7 connected in series. The gates and bulks of these small MOS transistors are connected to each other respectively. These small MOS devices are modelled by first order voltage-current equations as the one used in SPICE level 1 MOS model [22], which does not include the channel charge effect nor charge pumping effect.

The reverse biased diodes D3, D4 model the source/drain to substrate p-n junctions. Diodes D1. D2 connecting source and drain simulate the punch through effect of the small MOS devices. The punch through voltage of the small MOS transistors is determined by the turn-on voltage of diodes D1 and D2. It is also this punch through effect which drives the MOS transistor into saturation mode when the electrical channel becomes depleted at the drain side. Therefore, the punch through voltage of these small MOS transistors in the distributed MOS model determines the accuracy of this model.

The gate to channel capacitance are modelled by the capacitors Cg1 through Cg6 which are shunted from gate to

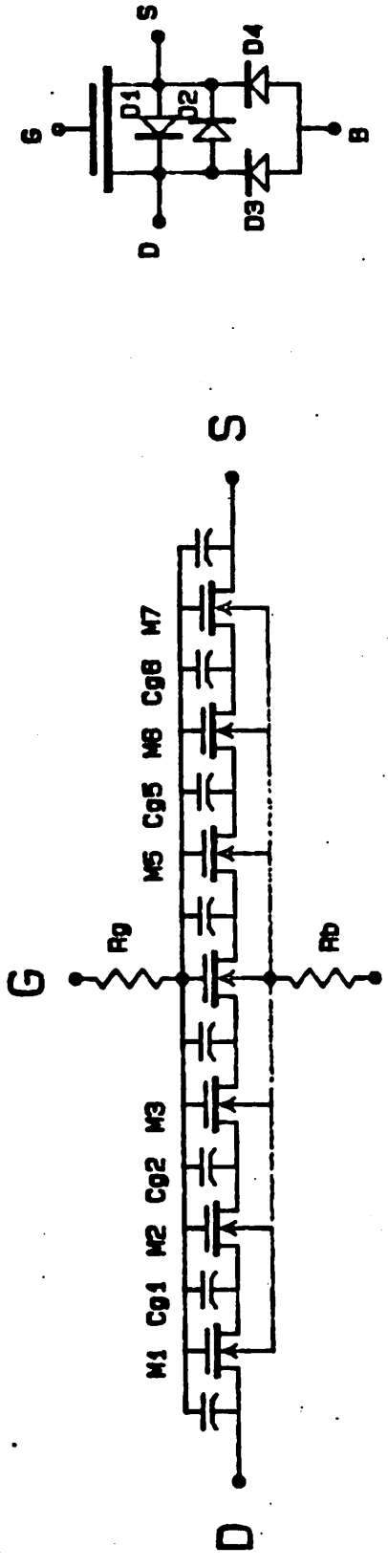


Fig.3.3 Distributed MOS Model

channel. Rg is the gate resistance, which can be neglected because the Rq*Cg time constant is on the order of a pico second, which is much smaller than the clock rise or fall time in any MOS circuit. Rb is the substrate resistance.

The distributed model for the MOS transistor in saturation mode is shown in Fig.3.4. The channel is pinched off at the drain side of the MOS transistor. Diodes D1 and D2 connecting the source and drain of the small device M1 simulate the punch through effect for device M1 when its channel ceased to exist. Because of the punch through effect in device M1 of the distributed MOS model, the charge can be swept across the channel pinched-off region, hence. maintaining the electric conduction between the source and drain of the transistor in the saturation mode.

The actual turn-on voltage of these diodes D1, D2 ..., depends on the substrate doping density. the distributed MOS device channel length, and the gate voltage applied. A detailed formulation of the punch through voltage can be found in many literatures [23].

Since we only intend to evaluate the channel charge injection mechanism qualitatively, only approximate values of the above mentioned parameters are used to simulate channel charge injection with different loading and switch

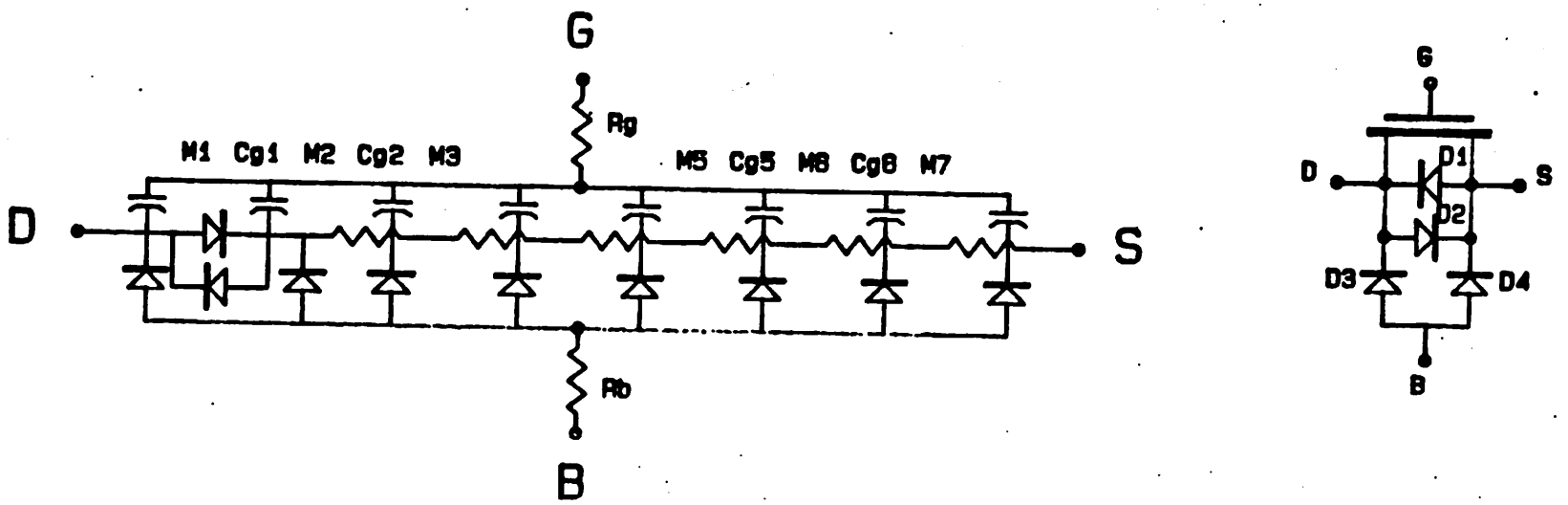


Fig.3.4 Distributed MOS Model for Device in Saturation Mode

transient conditions. Therefore, the turn-on voltage of these punch-through diodes can be arbitrarily set to 0.1 volt, and the channel length of the small MOS device is set to 0.1 um to minimize its gate capacitance effect on the distributed circuit model.

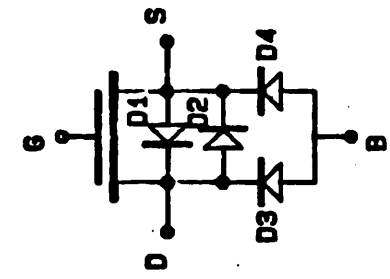
The distributed channel resistance is characterized by the turn-on resistance of these small MOS devices M1 through M7. The charge stored in the shunting capacitors Cg1 through Cg6 is the MOS transistor channel charge.

SECTION 3.2 - Turn Off Process of MOS Switches

When the switch is turned on in the triode region, it can be modelled by the distributed circuit shown in Fig.3.5. Capacitors C1, C2, ..., Cn represent the distributed gate to channel capacitors. Diodes D1, D2, ..., Dn are the distributed channel to bulk reverse biased p-n junctions. Resistors R1, R2, ..., Rn are distributed channel resistors, whose resistance values are functions of the voltage across the corresponding capacitors C1, ..., Cn. Rb is the substrate resistance, and rg is the gate resistance.

The channel charge in this mode is just the total amount of charge stored in the MOS capacitors, in the reverse biased channel to bulk p-n junction capacitances, and in the source/drain p-n junction capacitances.

At the steady state of turning on the MOS switch, there is no current flowing in the devices. The voltge across all the MOS capacitors are the same. Thus, all the channel resistors R1, R2, ..., Rn have the same resistance value. The channel to substrate diodes and the source/drain to substrate diodes are reverse biased at this state. Therefore, only reverse biased saturation currents flow



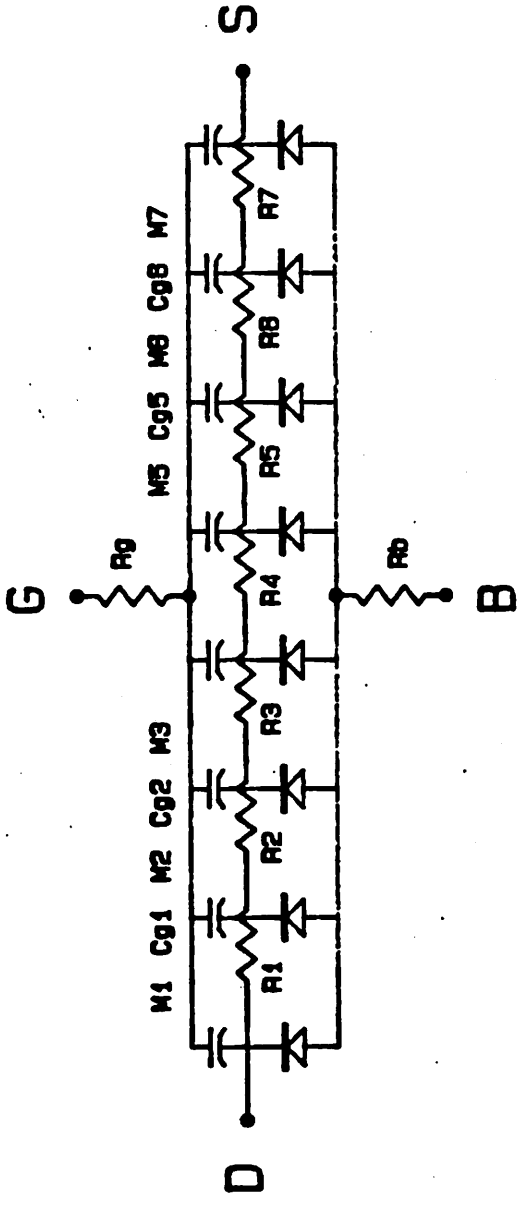


Fig.3.5 Distributed MOS Model for Device in Triode Mode

through these diodes. Because these diodes have gated-diode structure [24] in the turn-on mode. their surface states are filled by the inversion layer of the channel of MOS switch. Thus, only substrate saturation current dominates the overall leakage current, which is very small.

The reverse biased saturation current can be regarded as a very large resistor shunting the channel or drain/source to the substrate. Its magnitude is on the order of pico amp [3], which is very small compared to the steady state drain current in an MOS transistor in most circuits. Thus, substrate diode leakage effect usually can be neglected. However, under some conditions in linear MOS circuits where the voltage difference between drain and source is large. the reverse biased saturation current will be increased drastically due to the impact ionization effect [25] which takes place at the drain of MOS transistor. Therefore, the equivalent shunting resistance will be decreased greatly, and the effective output resistance of the MOS transistor will be reduced.

3.2.1 Turn-Off Mode

When the MOS switch is turned off, all the channel charge stored in the MOS capacitors and in the p-n junctions have to be discharged either through the drain/source. or through the substrate diodes. During the process of turning off the N-channel MOS switch. the gate voltage exercises a change of negative step. Depending on the transition time of the negative going step. the MOS switch will have a different response.

As the gate voltage starts to fall, the channel capacitance C1. ..., C7 start to discharge through the MOS devices M1. ..., M7 as shown in Fiq.3.6. If the impedance level at the source side of the MOS switch is much larger than that at the drain side. the gate capacitance C1 which are physically close to the drain side would get discharged much faster than the capacitors C7 which are physically close to the source side of the MOS switch.

The negative going step of the gate voltage is capacitively coupled onto the internal node 2 through node 7 of this distributed model when the clock voltage falls. The sudden voltage drop at node 2 caused by the transition of gate voltage will impose a potential difference across the

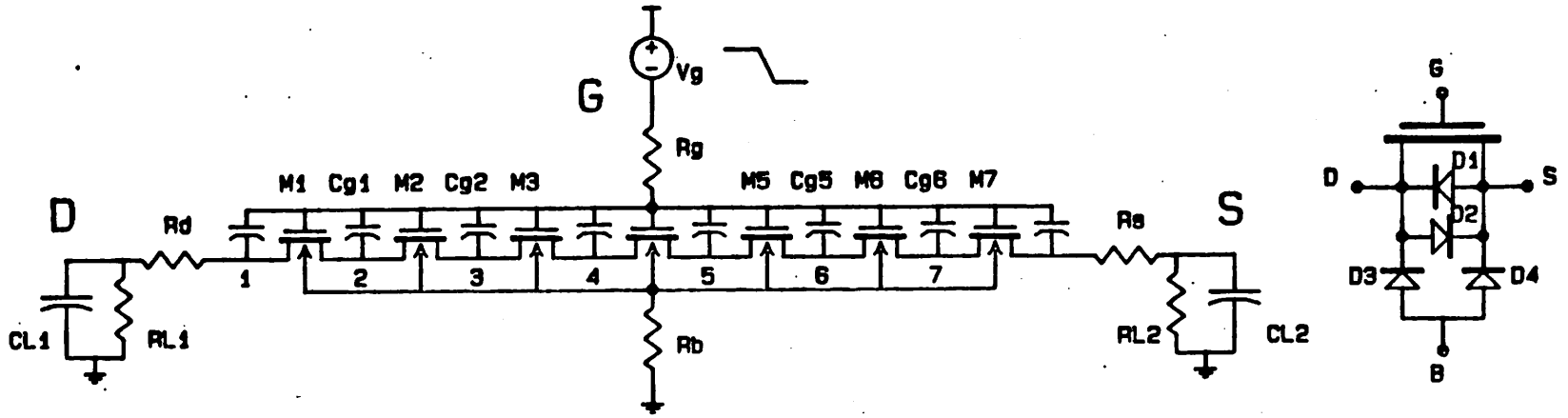


Fig.3.6 Distributed Model for MOS Switch with External Loading

small distributed transistor M1 if the external node 1 is at low impedance level. M1 will be in punch-through mode while the other small MOS transistors are still held on by the charge storage across the shunting capacitors. In other words, the MOS switch enters saturation mode, and the conduction channel at node 2 is pinched off. This mechanism propagates from node 2 through node 7 until the rest of the shunting capacitors C2,..., C7 are discharged. Subsequently, the MOS switch is turned off completely.

When the switch is turned off completely, the shunting capacitance no longer will have any effect on the circuit because the bottom plates of these shunting capacitors are disconnected from all the external nodes. In the simplified model of Fig.3.7, Cg is the gate capacitance assuming the channel still exists, Cd is the reverse biased channel to substrate diode junction capacitance. C1 is the external loading capacitance connecting to either source or drain, Ron is the channel resistance. and Rb is substrate spread resistance. The junction capacitance Cd is typically smaller than the gate to channel capacitance Cg. Local gate resistance Rg is much smaller than the channel-on resistance unless the poly interconnect resistance is included. Therefore, the time constant of Rg*Cg is much smaller than the time constant of Ron*Cg. Thus, the effect of the local gate resistance Rg can be neglected.

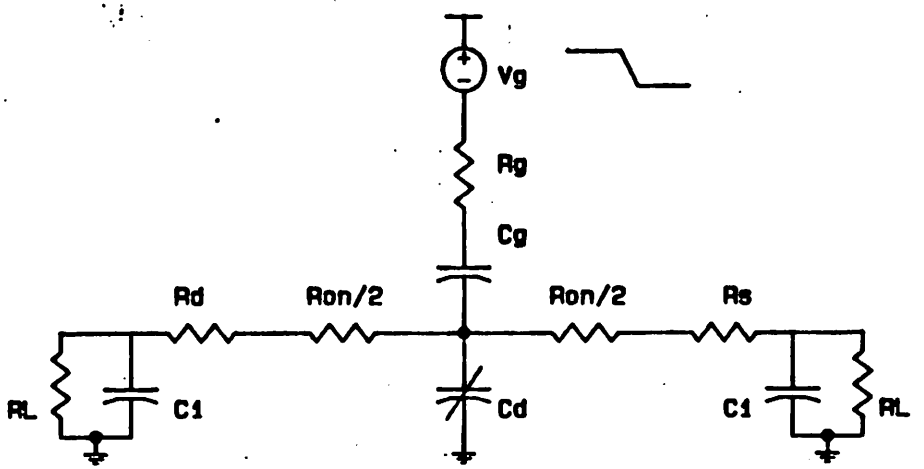


Fig.3.7 Simplified Lump Circuit Model for MOS Switch

3.2.2 Charges in the Depletion Regions

3.2.2.1 Substrate Depletion Region Charges

The sudden change of gate electric field would be directed onto either the inversion channel under the gate or the substrate depletion region when the clock voltage falls. If the clock fall time is larger than the Ron*Cl time constant imposed by the channel resistance and source/drain loading capacitance. the channel will behave like an electric shield for this change of electric field. Thus. no disturbance would occur on the substrate depletion region until the channel is depleted first. If the clock fall time is much smaller than the Ron*Cl time constant. or the channel has been depleted, then, the sudden change of the gate electric field would be directed onto the substrate depletion region. Because there is no mobile carrier in the substrate depletion region. the electric field will penetrate into the substrate. and cause a majority carrier current flow to discharge the charge in the substrate depletion region.

The time it takes to neutralize the change of electric field in the substrate is the substrate dielectric relaxation time which is on the order of few pico seconds

typically [26.27]. Therefore, for a clock fall time larger than 50 pico seconds, for example, the substrate will have sufficient amount of time to remove the space charge in the depletion region through substrate contact.

A large substrate contact resistor will not have any effect on the dielectric relaxation process because of the closed loop of the gate and substrate. Thus, substrate contact resistor can be treated as a gate resistor, which will limit the gate clock fall time.

Therefore, the charges stored in the source/drain and channel to substrate p-n junction capacitors are dumped back into the substrate when the MOS transistor is turned off. Thus, this portion of the channel charge does not contribute to any error voltage in the switched capacitor circuits.

3.2.2.2 Source/Drain and Channel Depletion Region Charges

This portion of the channel charge would have to flow into either drain or source electrode when the MOS switch is turned off. Thus, the redistribution of these charges will introduce an error voltage on the sampling capacitor.

3.2.3 Charge Pumping Effect

If the gate voltage has a very short fall time as compared to the time constant which consists of gate capacitance and one half of the channel-on resistance Ron*Cg, then, the Ron branch in Fig.3.5 would be considered as an open circuit during the clock transition time. As the result of the very short clock fall time, the gate capacitance. Cg, and the junction capacitance. Cd. form a voltage divider for the negative voltage step. Typically, Cd << Cg, most of the negative voltage step would be across Cd, and consequently, forcing the junction diode to forward biased.

For a typical MOS switch of 10 um by 10 um size. 1000 angstron gate oxide, and a 5 volt gate overdrive, one half of Ron*Cg is on the order of 0.2 nano second. In some digital circuits, the MOS switches are connected as transmission gates which have high body effect. thus, the effective gate overdrive would be reduced. As a consequence of the reduced gate overdrive. the channel-on resistance would be increased drastically, thus making this time constant Ron*Cg approaches 1~2 nanosecond. which is comparable to some high speed MOS gate delay [28]. Also the loading capacitance of these MOS transmission devices might

be the gate capacitance of another inverter which is roughly the same size as that of the switching device. Therefore, at least one half of the negative voltage step would be imposed across the source/drain to substrate junction diode at the side connecting to the inverter load. The diode may be forced to forward biased. Therefore, in high speed digital MOS circuits, the charge pumping effect will generate a huge amount of substrate currents which will cause a lot of noise in the circuits if this problem is not well handled.

In the precision analog MOS circuits, the operation speed is often limited by the settling time of the operational amplifier or the comparator, this time is much larger than few nanoseconds. The digital clock used to drive these analog MOS circuits are not optimized for their digital speed. Thus, the clock rise or fall time of the analog MOS circuits usually is much larger than a few nanoseconds especially when the interconnect resistance is considered. Also, the loading capacitance of the MOS switch is usually the input gate capacitance of an operational amplifier or a comparator, which is usually much larger than that of the switch device. Therefore, as a consequence of the much longer clock transition time and the larger loading capacitance, analog MOS circuits seldom experience any charge pumping effect.

3.2.4 Current Path Through Source and Drain Region

Refer to Fig.3.5 again, if there is no charge pumping effect during the turning-off process of the MOS switch. then, the channel charge has to be discharged through either drain or source or both.

3.2.4.1 Very Long Clock Fall Time

As the gate voltage falls, the amount of channel charge decreases. the channel resistance increases. and the channel charges flow into either drain or source or both. Because the clock fall time is very long, steady state is always maintained in the channel. Therefore, the distributed channel resistance R1. R2, ..., R4 will maintain the same value. Both the drain and source voltage will be at identical potential. Equal displacement current will flow from the channel to the source and the drain region until the channel get pinched off.

3.2.4.2 Short Clock Fall Time

Under matched loading conditions at the drain and source nodes, equal displacement current from the channel capacitor would flow into drain and source because of symmetry. Thus, exactly half of the channel charge will be dumped into the sampling capacitor. Refer to Fig.3.8, the conduction channel at the drain and source nodes would get pinched off first because the channel capacitance on these two nodes see a discharging path with resistance less than that of the channel capacitance in the mid-gate region. In the region where the channel exists, the charge is transported by the drift mechanism. In the region where the channel is pinched off, the charge is swept across the pinched off region by the strong longitudinal electric field in the space charge region.

When the loading impedance at the drain node and source node of the MOS switch are different, the channel at one side of the switch will get pinched off earlier than the channel at the other side of the switch. Therefore, unequal amount of channel charge will flow into the source side and drain side of the switch. Thus, an unpredictable amount of channel charge dumped into the sampling capacitor will cause an error voltage on the sampled signal.

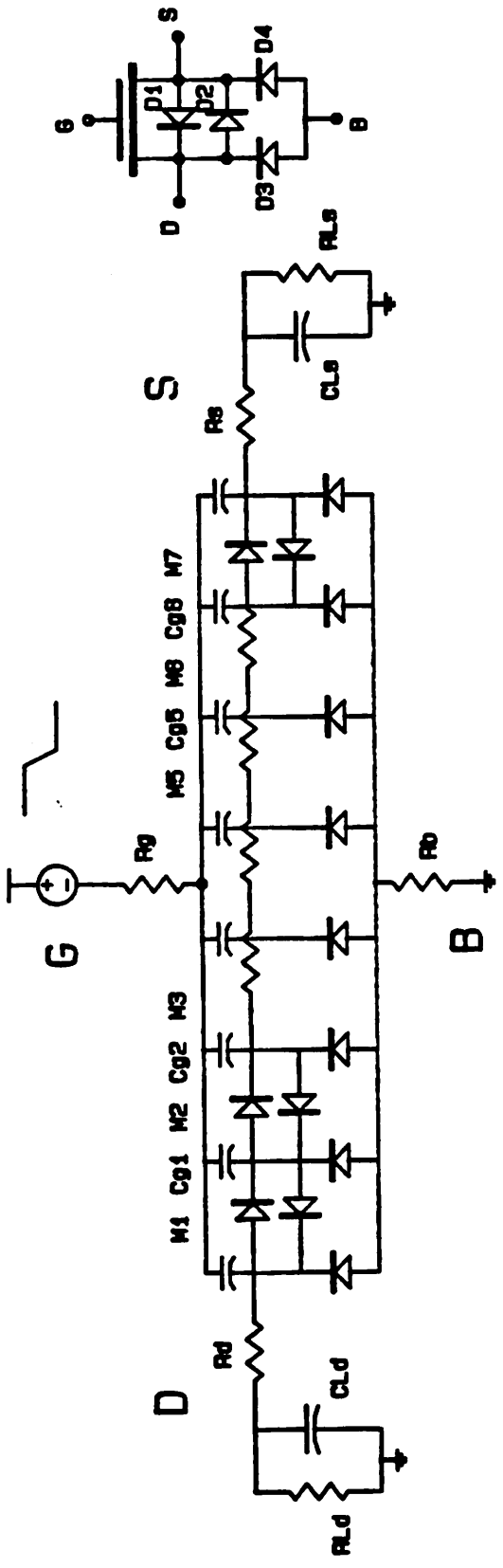


Fig.3.8 Distributed Model for Turning Off MOS Switch with Short Clock Fall Time

SECTION 3.3 - Experimental Verification of the Distributed MOS Model

An experiment was made to verify the validity of the distributed MOS model using discrete components, and the measured results were compared against the data obtained from computer simulation using distributed MOS model.

Shown in Fig.3.9 is the basic test circuit for this experiment. The fraction of the total amount of switch channel charge dumped into the sampling capacitor was observed with different source impedance and different clock fall time. The circuit configuration for computer simulations is shown in Fig.3.10, and the breadboard circuit is shown in Fig.3.11.

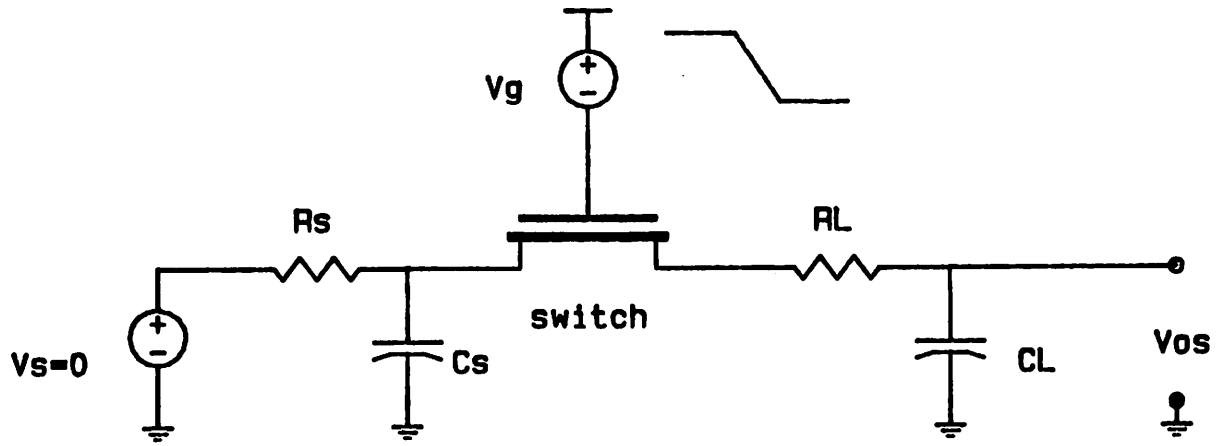


Fig.3.9 Switch Channel Charge Injection Test Circuit Schematic

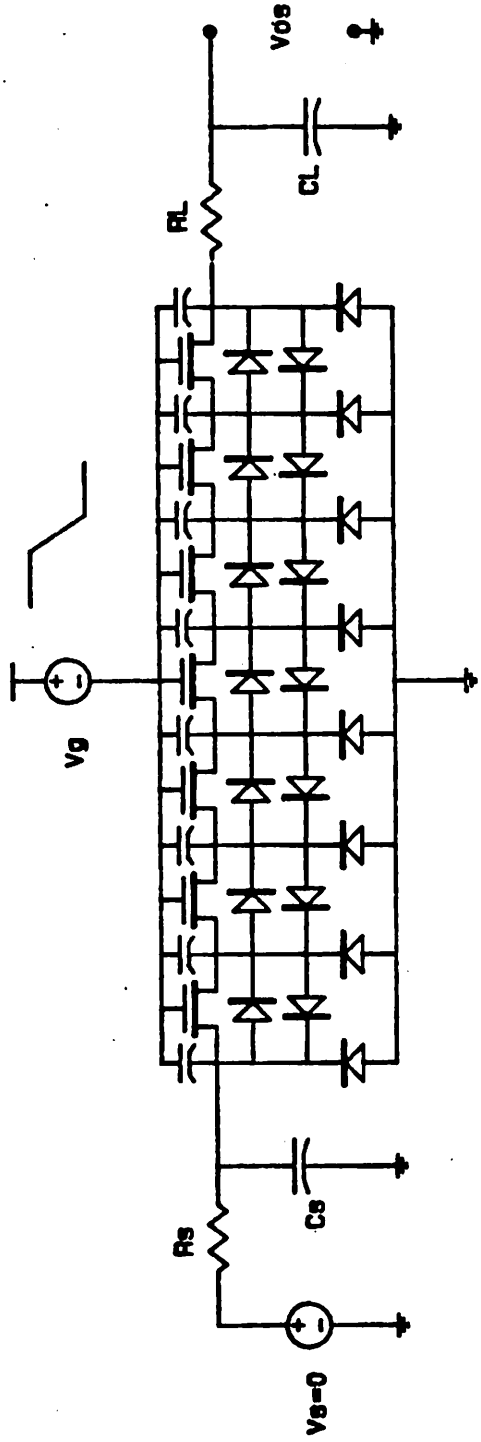


Fig.3.10 Circuit Schematic for Computer Simulation of Switch Channel Charge Injection

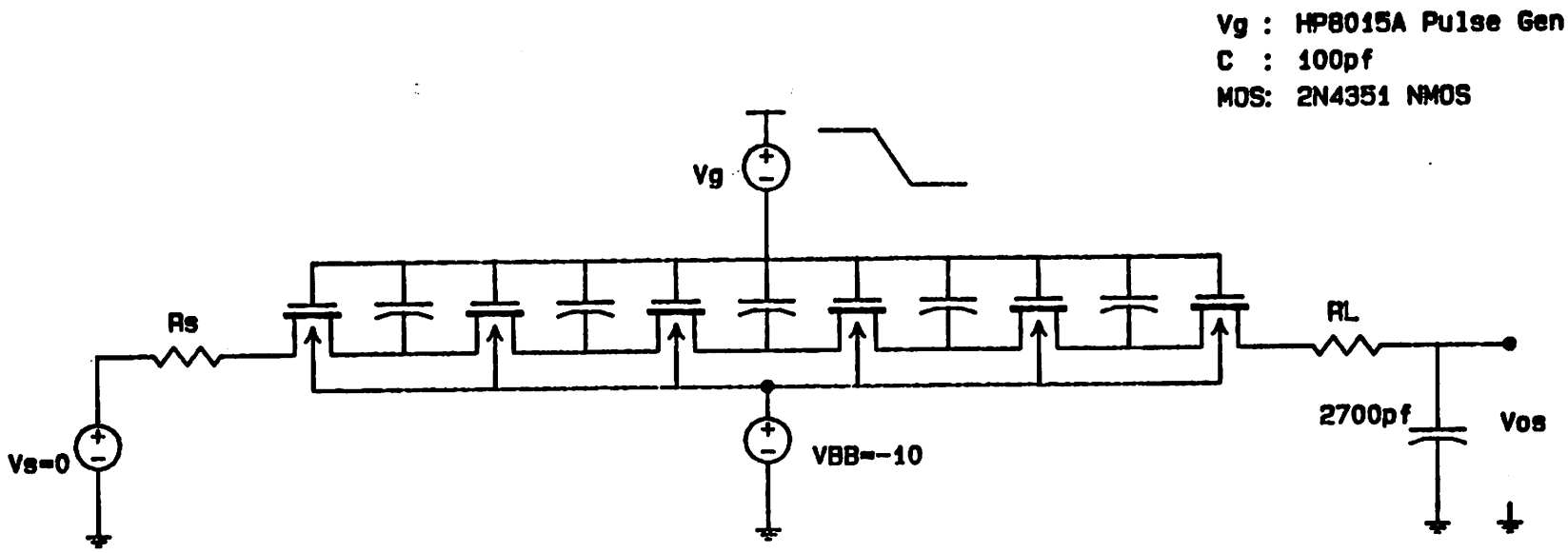


Fig.3.11 Breadboard Circuit Schematic for Switch Channel Charge Injection

The percentage of the total amount of switch channel charge dumped into the sampling capacitor CL is plotted against source resistance variation in Fig.3.12. Fig.3.13 shows the offset charge on the sampling capacitor versus clock fall time. Fig.3.14 is the offset charge plotted against the ratio of RC time constant of the source resistance and source capacitance to the clock fall time.

Good agreement was observed between the experimental results and computer simulations. It is apparent from these experiments that the offset charge is a strong function of the clock fall time, source resistance, load resistance, switch on-resistance, and switch gate capacitance. It is always expected to have less switch channel charge dumped into the sampling capacitor as the source impedance decreases and clock fall time increases.

The hypothesis on the turn-off process of the MOS switch in the previous section is supported by these experimental data, and the distributed MOS model is valid in the scope that it provides a quick tool to analyze the switch channel charge injection error qualitatively.

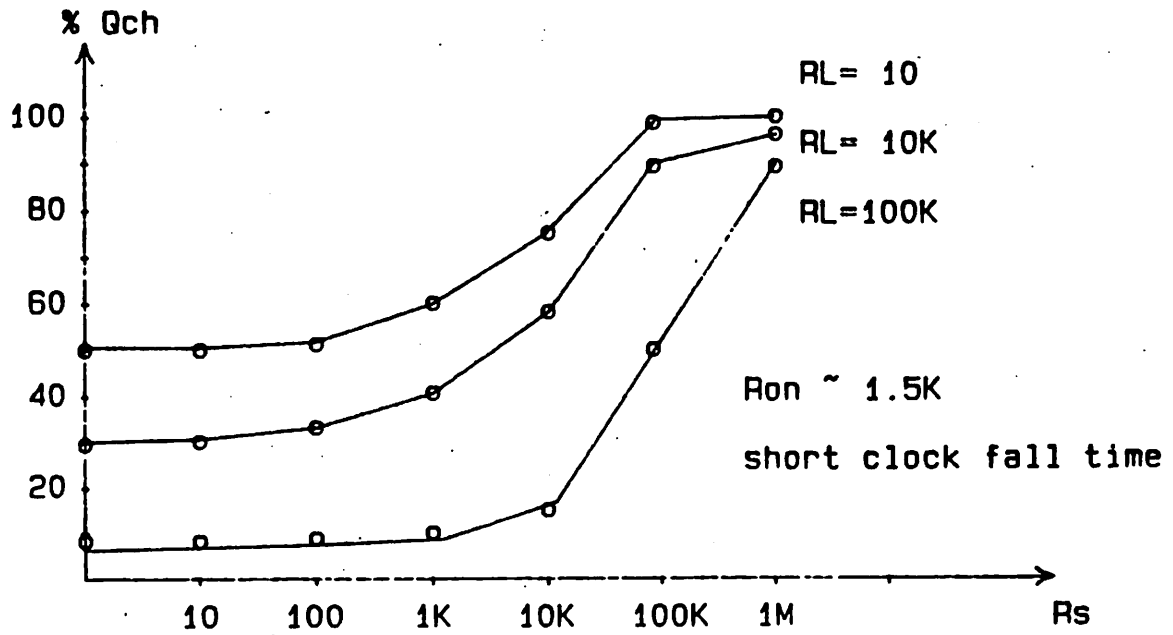


Fig.3.12 Channel Charge Injection as a Function of Source Resistance

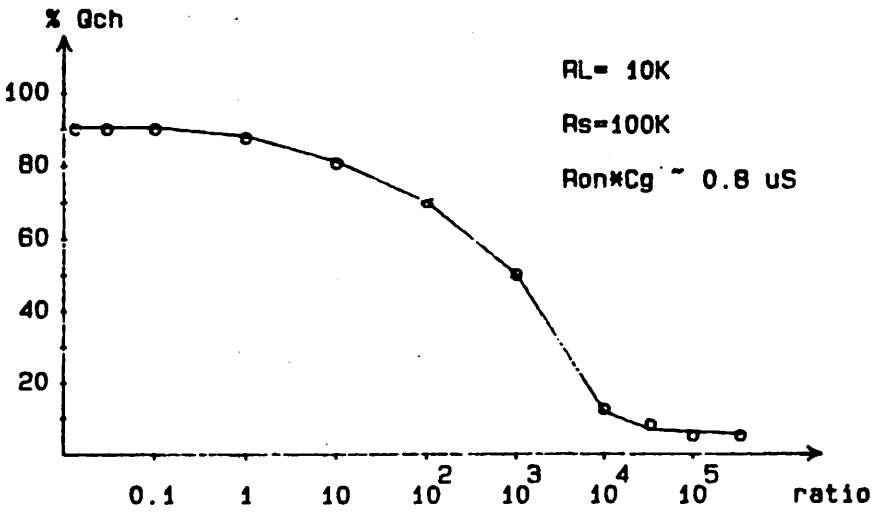


Fig.3.13 Channel Charge Injection as a Function of the Ratio: Clock Fall Time/ Switch Ron*Cg

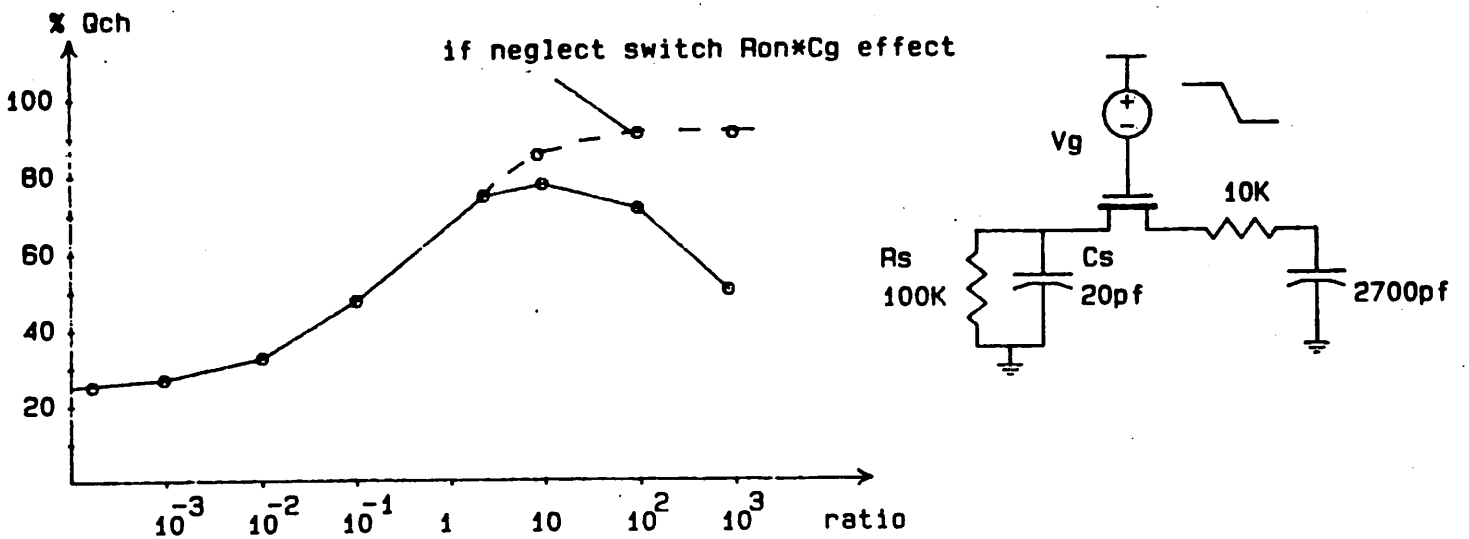


Fig.3.14 Channel Charge Injection as a Function of the Ratio : Clock Fall Time/ Rs*Cs

SECTION 3.4 - Circuit Techniques to Reduce Switch Charge Injection Induced Error

3.4.1 . Dummy Switch Charge Cancellation Technique

One approach to reduce the clock feedthrough voltage and channel charge injection error is to use a large capacitors [29,30]. However, the added complexity and the decreased circuit operating speed due to the large capacitor would limit the usefulness of the circuit. Another conventional method to reduce this type of error is to use a dummy switch [31,32] as shown in Fig.3.15. The dummy switch is made to be one half the size of that of the input switch, with its source and drain connected together. A clock with opposite phase of that of the input switch is applied to the dummy switch. Therefore, the clock feedthrough and channel charge injection caused by turning off the input switch is compensated by that of the dummy switch.

The input node of the input switch sees an impedance which varies a lot with different driving sources. while the dummy switch has a constant capacitive loading due to the sampling capacitor. Therefore, the amount of channel charge

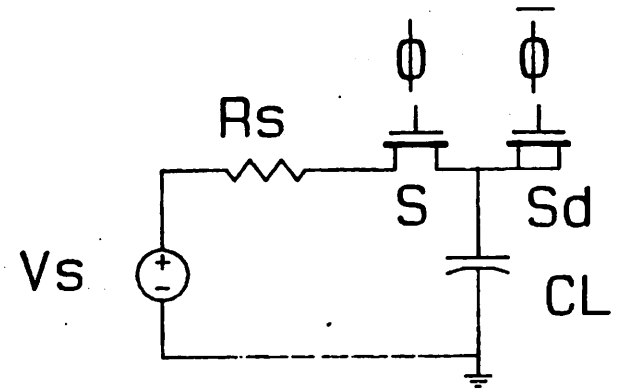


Fig.3.15 Switch Channel Charge Cancellation Using Dummy Switch Approach

injected from the dummy switch into the sampling capacitor is a constant offset with respect to various source and loading impedance levels while the amount of channel charge injected from input switch into the sampling capacitor depends heavily on the source and loading impedance levels. Thus, the amount of offset charge introduced by the dummy switch can only compensate the channel charge injected from the input switch to the first order. The best charge compensation occurred when the source impedance equals the load impedance and exactly half of the switch channel charge is injected into the sampling capacitor.

3.4.2 Dummy Capacitor Charge Cancellation Technique

The strong source impedance dependency of this dummy switch cancellation technique can be reduced significantly by adding a dummy capacitor [33] as shown in Fig.3.16.

In this approach, both a dummy switch and a dummy capacitor are used to assure that exactly one half of the channel charge will flow into the sampling capacitor. Thus, the dummy switch with half the size of the input switch can guarantee the exact cancellation of both the channel charge

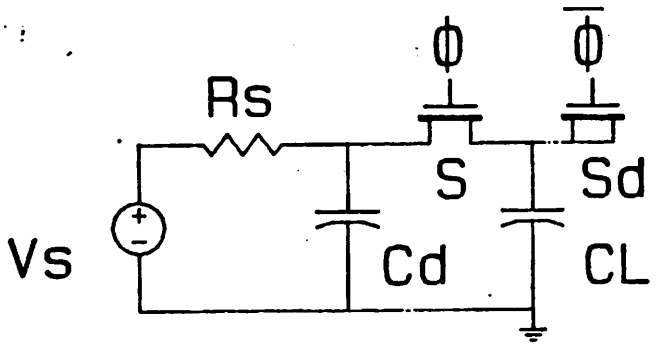


Fig.3.16 Switch Channel Charge Cancellation Using Dummy Capacitor Approach

injection and the clock feedthrough problems. This technique works well when the source impedance. clock frequency and fall time are all well controlled. However, when the signal is driven from an external source whose impedance level is low, this dummy capacitor will have very little effect on the channel charge cancellation. Take an extreme case for example, if the input signal is from an ideal voltage source with zero source impedance. then the dummy capacitor is essentially shorted.

The switch channel charge injection error on the sampling capacitor can be maintained at less than 1% of the total switch charge with wide range variation of the source impedance and clock fall time. The error starts to increase above 1% level only when the clock fall time gets to be larger than the RC time constant of the source resistor and dummy capacitor.

3.4.3 Differential Sampling Technique

The differential sampling configuration shown in Fig.3.17 uses two carefully matched switches and capacitors to sample the differential signal. The channel charge injection will introduce the same error voltage on these two

sampling capacitors, thus giving no differential error on the sampled voltages. Although the differential input voltage introduces a difference of channel charge in the two matched switches. this error term is proportional to the input differential voltage, and can be considered as a fixed gain error due to the sliqht variation of the capacitors' values.

One drawback in the configuration shown in Fiq.3.17 is that the channel charge cancellation relies on the matching of the two differential input impedances. For circuits integrated inside a chip, the driving sources' impedance level can be well matched. However, if the sampling switches and capacitors are to be interfaced with external siqnal sources whose impedance level will vary. then a slight modification of the balanced configuration shown in Fig.3.18 will guarantee the cancellation of channel charge error under all conditions. The dummy capacitors shown in Fig.3.18 serve the purpose of lowering and matching the source impedance level. Therefore, the size of these dummy capacitors do not have to match that of the sampling capacitors very accurately.

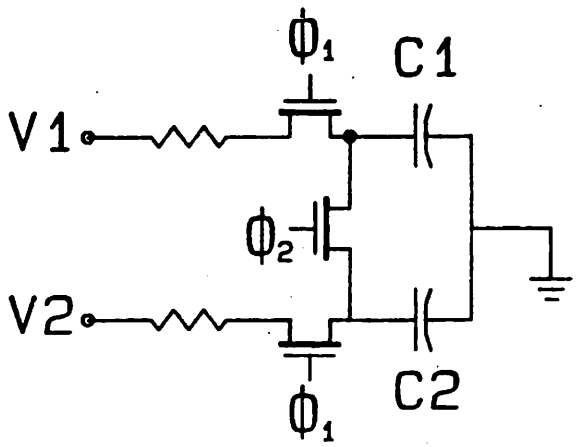


Fig.3.17 Balanced Differential Sample & Hold

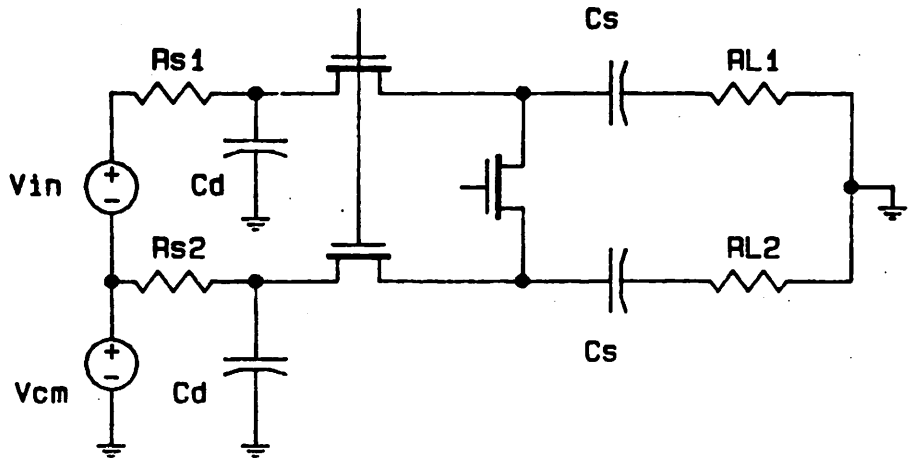


Fig.3.18 Differential Switch Channel Charge Cancellation with Dummy Capacitors

SECTION 3.5 - KT/C Noise

Another error source due to the sampling switch and capacitor is the KT/C noise [34]. This noise is generated from the broad-band thermal noise associated with the turn-on resistance of the switch. Since the switch on-resistor and the sampling capacitor form a low pass network which bandlimits the broadband thermal noise, the total Gaussian noise energy sampled onto the capacitor will be just KT/C. Fig.3.19 shows a sampling switch connected with a sampling capacitor. The noise power spectral density due to the channel resistance of this switch is [10] :

$$Vn^2/f = 4KTR$$

where R is the switch turn-on resistance which includes all the parasitic series resistance in the sampling path. K is the Boltzmann's constant, T is the absolute temperature in degree Kelvin, and f is the frequency bandwidth in hertz.

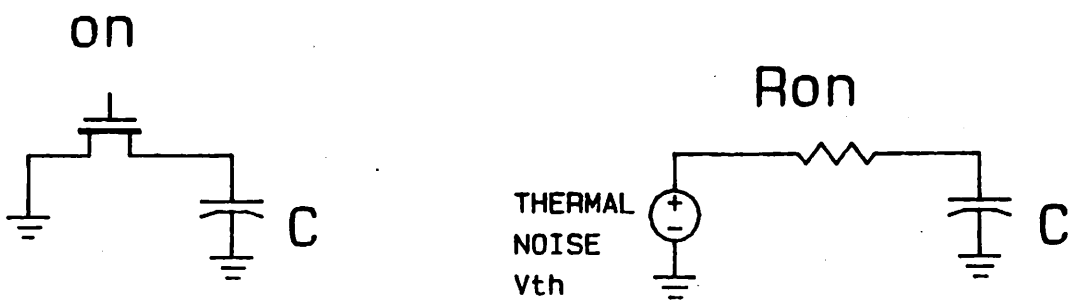
The noise voltage spectral density on the sampling capacitor is:

$$Vcn^2/f = 4KTR*|H(f)|^2$$

Where H(f) = 1/[1+(2*3.1416*f*RC)] is the low pass transfer function of the network formed by the switch and capacitor. Integrating Vcn**2 over all frequencies yields the squared noise voltage on the sampling capacitor:

$$V_c^2 = \int_0^\infty 4KTR|H(f)|^2 df$$
$$= KT/C$$

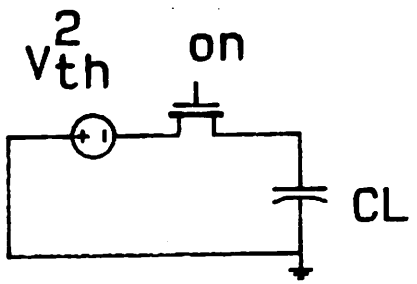
Shown in Table 3.1 is the KT/C noise power with respect to different sampling capacitor sizes. This KT/C noise represents a fundamental limit to the resolution of the system. For a sampling capacitor value of 10 pF, the standard deviation of this Gaussian noise is 25 uV at room temperature. For a system sampling at 200 kHz, this corresponds to an in-band noise density of 50 nV per root Hz, or an equivalent noise resistance of 1.5 mega ohm. Increasing the sampling rate decreases the in-band noise density, but the total amount of noise energy below the Nyquist frequency [35] remains constant. In the amplifier described in this thesis, KT/C noise is the dominant noise source. Other amplifier noise powers can be reduced by the use of double correlated sampling technique [Appendix A].



$$V_{TH}^2 = 4KT * Ron * df$$

$$Vo_{TH}^2 = \int_0^{\infty} V_{TH}^2 = KT/C$$

Fig.3.19 Switched Capacitor KT/C Noise



C	$\sqrt{KT/C}$	$V_{eq}/\sqrt{Hz}$ (fs=200 kHz)
1 pf	80 uV	170 nV
10 pf	25 uV	55 nV
100pf	8 uV	17 nV

Table 3.1 KT/C Noise of a Sample & Hold Circuit

CHAPTER 4 - SWITCHED CAPACITOR INSTRUMENTATION AMPLIFIER

This chapter describes the implementation of a switched-capacitor instrumentation amplifier which employs double correlated sampling to reduce the circuit dc offset and low frequency noise. This precisioned instrumentation amplifier also uses a balanced circuit configuration to achieve first order cancellation of switch channel charge injection. A charge redistribution scheme is also demonstrated which allows the circuit CMRR to be independent of the op-amp CMRR, thus resulting in a very high overall common mode rejection ratio in excess of 120 dB.

SECTION 4.1 - Circuit Description

A typical data acquisition system [36] generally consists of an input amplifier, sample and hold stage, and an A to D converter as shown in Fig.4.1.

The amplifier serves to increase the signal level prior to an A/D conversion. Input offset voltage is a key aspect of amplifier performance since it can limit dc system accuracy. In some systems, it is possible to measure and subtract the dc offset, however the equivalent input noise voltage represents a fundamental limit on the resolution of the system. Also, gain accuracy and gain linearity are critical parameters for instrumentation applications [37]. In some cases, a low-amplitude input signal is superimposed onto large common mode components due to electrostatic or electromagnetic induction. This further emphasizes the requirement for high common mode rejection. The data acquisition circuit may reside on the same chip as the digital LSI processor; therefore, the ability to reject power supply noise is also very important.

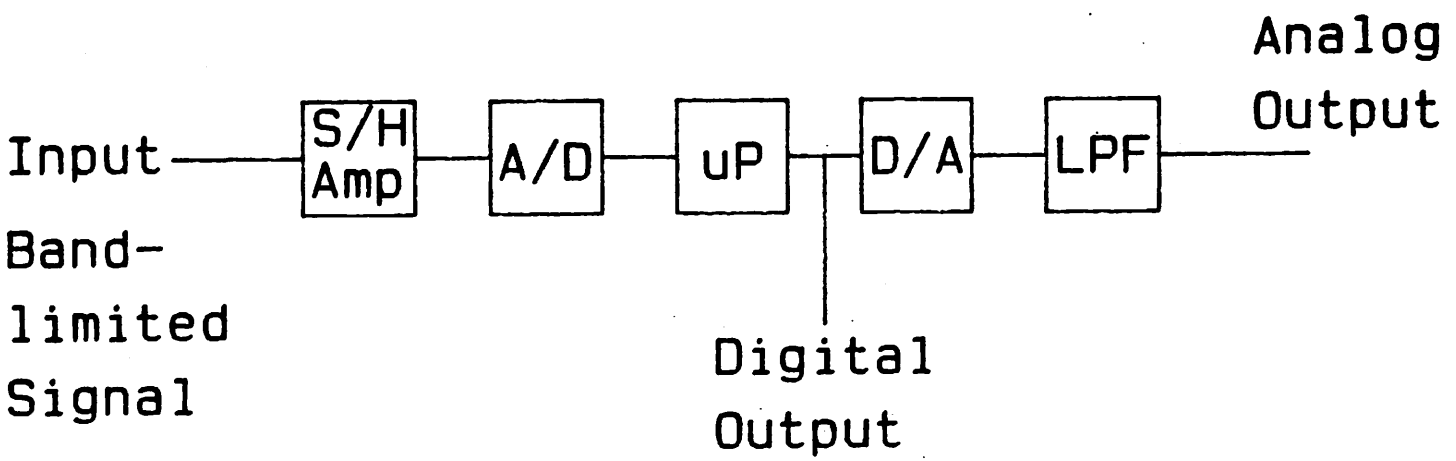
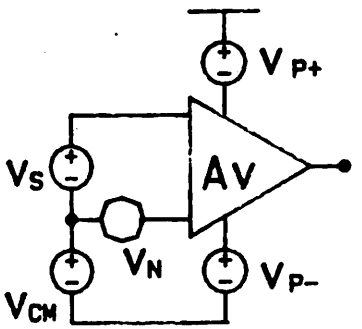


Fig.4.1a A TYPICAL VLSI SIGNAL PROCESSING SYSTEM



Vo=Av*Vs+A1*Vcm+A2*Vp+Av*Vn

Definitions:

Av=aVo/aVs PSRR=Av/A2

CMRR=Av/A1 Noise=Vn

Fig.4.1b Key Parameters for Instrumentation Amplifier

The MOS implementation of the double correlated sampling technique is shown in Fig.4.2. This circuit consists of a pair of sampling capacitors, C1, C2; gain setting capacitors. C3. C4; offset cancellation capacitors. C5, C6; and two differential amplifiers A1 and A2, where amplifier A1 is a broadband, low gain. differential preamplifier, and A2 is a high gain. differential operational amplifier.

The input signal is sampled on to the sampling capacitors C1, C2, and subsequently transferred to the gain setting capacitors C3. C4 through a sequence of switching operations. The output voltage will be a replica of the input differential signal with a voltage gain defined by the capacitor ratio C1 over C3 when capacitor C1 matches C2, and C3 matches C4. This circuit is fully differential so that all the switch charge injections and power supply variations are cancelled to the first order.

A more complete circuit schematic diagram which includes all the parasitic capacitances is shown in Fig.4.3. Circuit operation takes place in two phases as illustrated in Fig.4.4a.

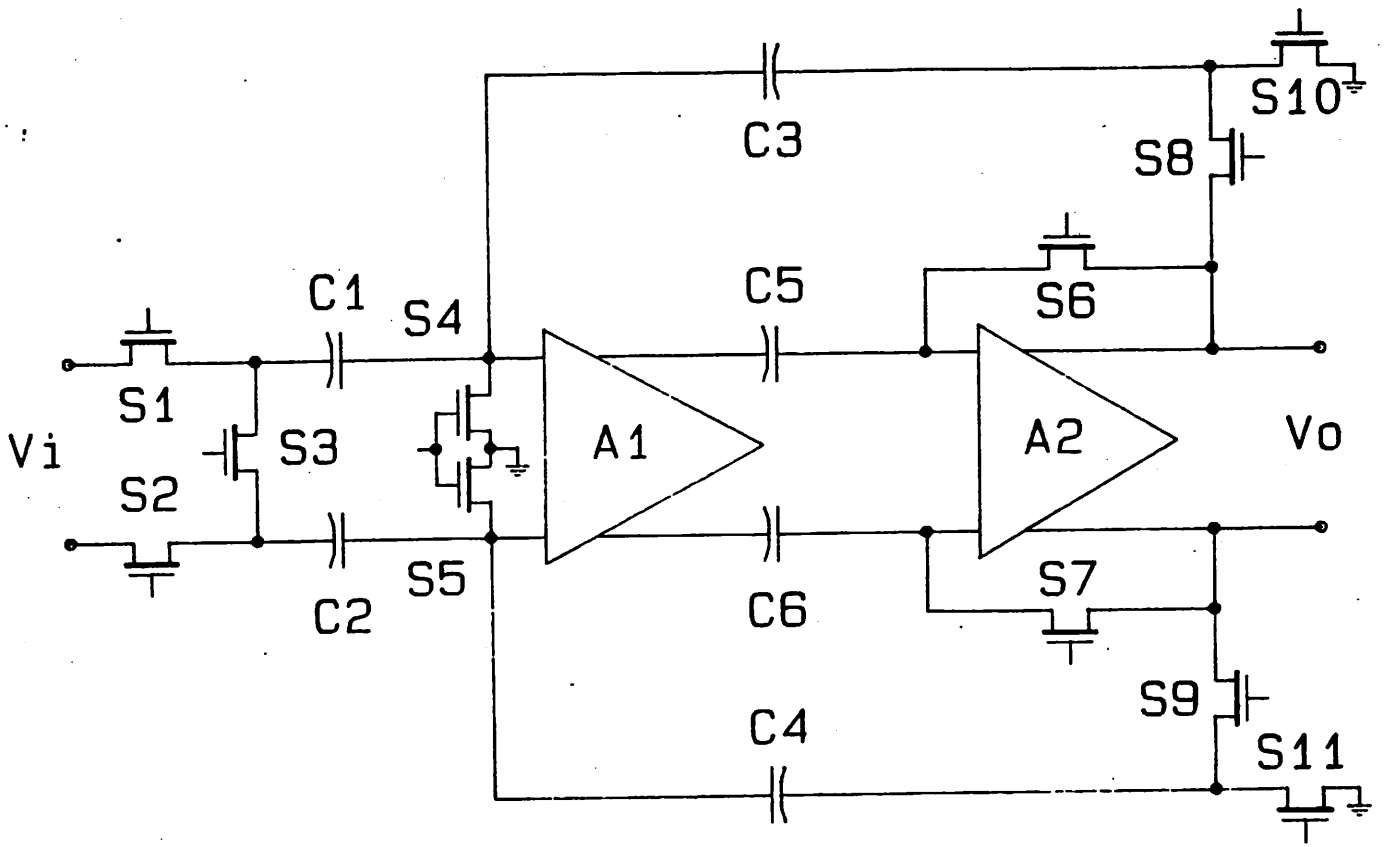


Fig.4.2 Differential DCS Instrumentation Amplifier

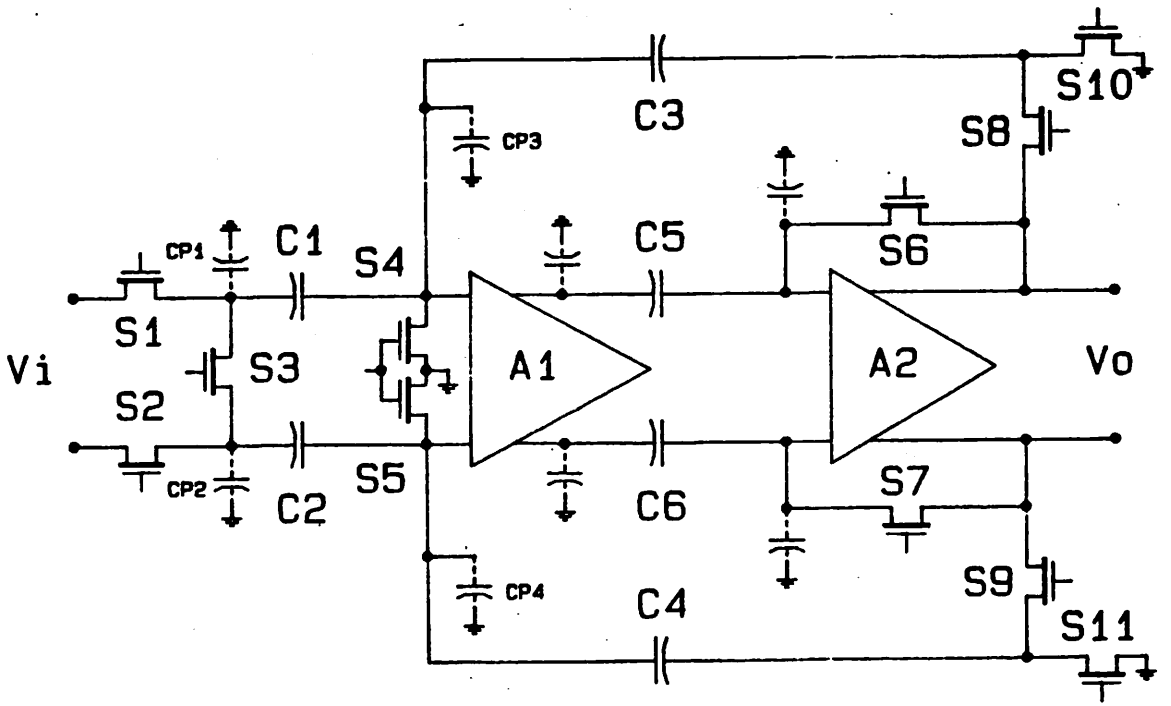


Fig.4.3 Instrumentation Amplifier with Parasitic Capacitances

In the sample mode, the switches are closed as shown in Fig.4.4a. In this mode the differential and common mode input voltages appear across both the sampling capacitors C1. C2, and the parasitic capacitors Cp1. Cp2 at the sampling nodes. The difference between the offset voltage of A1, and A2 is impressed across C5 and C6. The instantaneous value of the 1/f noise of both amplifiers is also stored. The parasitic capacitors Cp5 and Cp6 at the input nodes of the second op-amp A2 are also charged to the offset voltage of A2. The voltage across the feedback capacitors C3, C4 and the parasitic capacitors Cp3, Cp4 are reset to zero during this mode.

The input signal is sampled and a transition to the hold mode is made when clock one goes negative, turning off the input sampling switches and feedback switches. Subsequently, the switches are closed as shown in Fig.4.4b, and the voltage difference between the two inputs is forced to zero. This causes a charge redistribution in capacitors C1. C2. C3. and C4, which results in an output voltage which is mainly proportional to the input difference voltage.

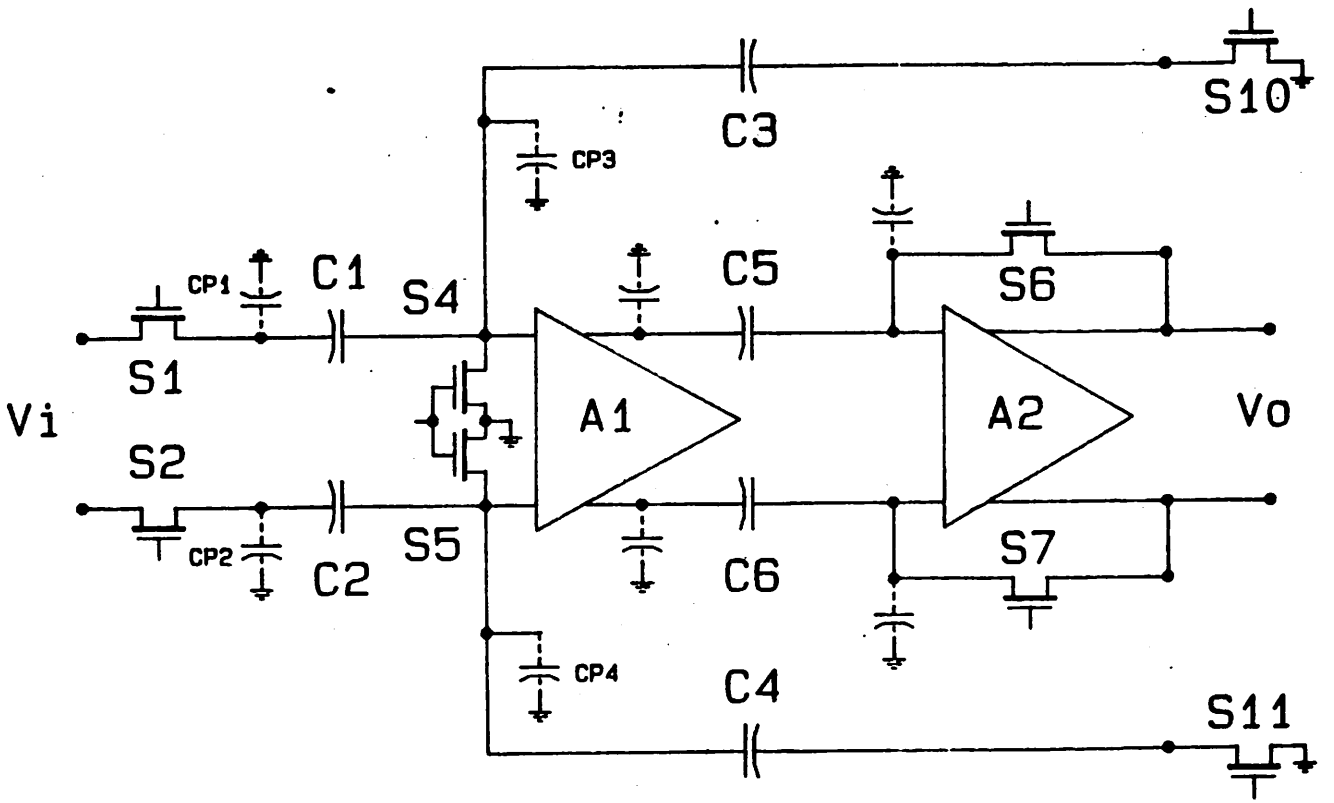


Fig.4.4a Sampling Mode of the DCS Switching Operation

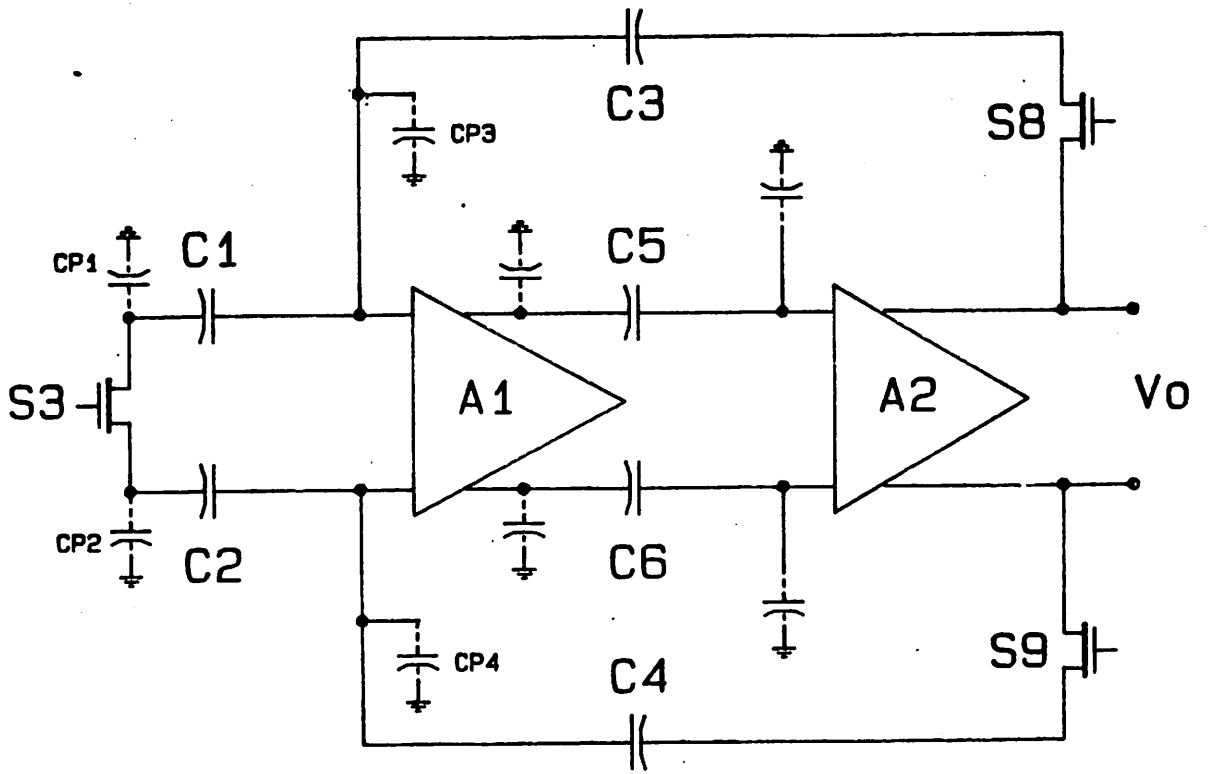


Fig.4.4b Hold Mode of the DCS Switching Operation

SECTION 4.2 - First Order Analysis of Switched Capacitor Instrumentation Amplifier

During the sampling mode, when clock 1 is high, the capacitors C1, C2, CP1, and CP2 are charged to:

$$Qc1 = (Vcm+Vdm)*C1$$

$$Qc2 = Vcm*C2$$

$$Qcp1 = (Vcm+Vdm)*Cp1$$

$$Qcp2 = Vcm*Cp2$$

and the capacitors C3, C4, CP3, and CP4 are all initialized to have zero voltage across them:

$$Qc3 = 0$$

$$Qc4 = 0$$

$$Qcp3 = 0$$

$$Qcp4 = 0$$

During the hold mode, the switches are closed as shown in Fig.4.4b, and the charges are redistributed among all the capacitors. Neglecting the second order effect due to voltage dependent parasitic capacitance. finite op-amp dc gain, and mismatch in channel charge injection. We obtain:

$$Vcp1 = Vcp2$$

$$Vc1 = Vc2$$

$$Vcp3 = Vcp4$$

Because the charges are preserved at nodes 1. 2. and 3. the node charges are:

at node 1.

$$Q1 = Qc1+Qc2+Qcp1+Qcp2$$

$$= Vcm*(C1+C2+CP1+CP2) + Vdm*(C1+CP1)$$

at node 2,

$$Q2 = -Oc1$$

$$= -(Vcm+Vdm)*C1$$

at node 3,

$$Q3 = -Oc2$$

$$= -Vcm*C2$$

In the hold mode after switch S3 is closed during the hold mode, the total capacitance at node 1 becomes CP1+CP2+CPS due to the contribution of the channel capacitance CPS from switch S3.

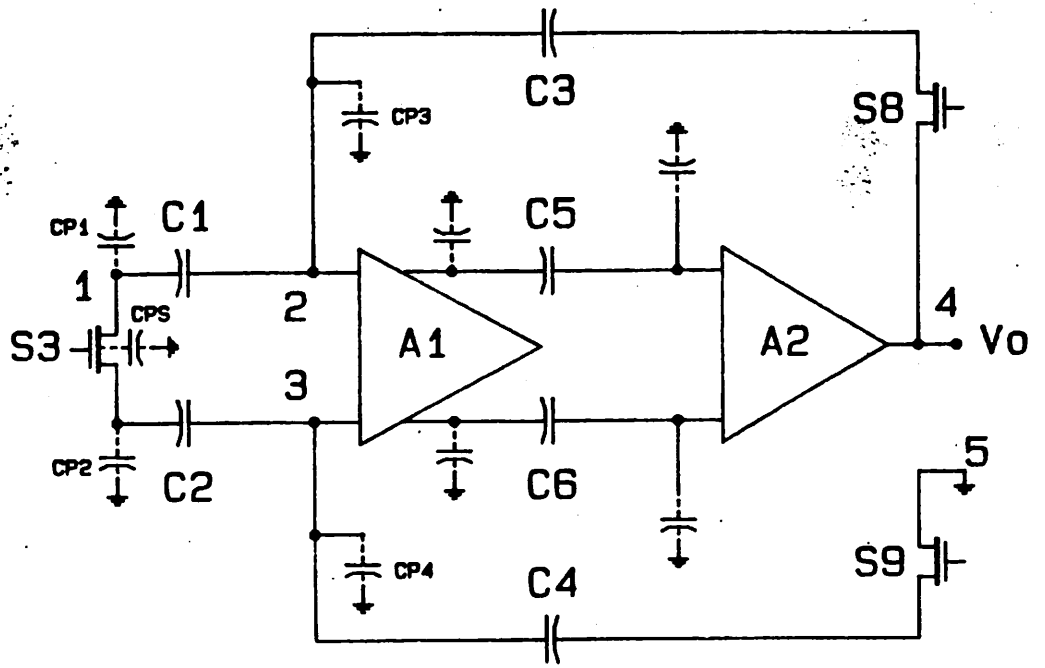


Fig.4.5 Circuit Schematic for Charge Redistribution Analysis

Refer to Fig.4.5, the voltage at each node is governed by the set of equations:

$$V1*(CP1+CP2+CPS)+(V1-V2)*(C1+C2) = Q1 \quad \ldots\ldots (1)$$

$$V2*CP3+(V2-V1)*C1+(V2-Vo)*C3 = Q2 \quad \ldots\ldots (2)$$

$$V2*CP4+(V2-V1)*C2+(V2-V5)*C4 = Q3 \quad \ldots\ldots (3)$$

To solve three equations with 4 unknowns, variable V5 is arbitrarily set to zero. The equations become:

$$V1*(CP1+CP2+CPS+C1+C2) - V2*(C1+C2) = Q1 \quad \ldots\ldots (4)$$

$$-V1*C1 + V2*(CP3+C1+C3) - Vo*C3 = Q2 \quad \ldots\ldots (5)$$

$$-V1*C2 + V2*(CP4+C2+C4) = Q3 \quad \ldots\ldots (6)$$

From equation (6) we get

$$V1 = V2*(CP4+C2+C4)/C2 - Q3/C2 \quad \ldots\ldots\ldots (7)$$

Substitute V1 into equation (4), and solve for V2. We obtain:

$$\{V2*(CP4+C2+C4)-O3\}*\{CP1+CP2+CPS+C1+C2\}/C2 - V2*(C1+C2) = Q1$$

$$V2 = \{Q1+Q3*(CP1+CP2+CPS+C1+C2)/C2\}/A \quad \ldots\ldots\ldots\ldots (8)$$

where $A=(CP4+C2+C4)*(CP1+CP2+CPS+C1+C2)/C2 - (C1+C2)$

Substitute equation (8) into (7) to solve for V1, and we obtain:

$$V1 = \{(CP4+C2+C4)/C2\}*\{Q1+O3*(CP1+CP2+CPS+C1+C2)/C2\}/A$$

$$- Q3/C2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (9)$$

Substitute equations (8) and (9) into equation (5) to obtain Vo:

$$Vo = \{-V1*C1+V2*(CP3+C1+C3)-O2\}/C3$$

$$= \{Q3*C1/C2-(CP4+C2+C4)*(C1/C2)$$

$$* [Q1+O3*(CP1+CP2+CPS+C1+C2)/C2]/A\}/C3 + \{(CPS+C1+C3)$$

$$* [Q1+Q3*(CP1+CP2+CPS+C1+C2)/C2]/A\}/C3-Q2/C3 \ldots (10)$$

The instrumentation amplifier is designed with a fully balanced configuration. All capacitor pairs and their associated parasitic capacitances are designed to achieve optimum matching. Therefore, the capacitance mismatch of the capacitor pairs can be characterized to the first order as follows:

$$C2 = C1+aC1$$

$$C4 = C3+aC3$$

$$CP2 = CP1+aCP1$$

$$CP4 = CP3+aCP3$$

where aC is the mismatched capacitance. which is usually much less than 1% of the total capacitance value if the capacitor used is carefully laid out with a capacitance value larger than 1 pf [38].

With this simplification in the capacitor values used in the switched-capacitor instrumentation amplifier, equations (6) ~ (9) can be rewritten as:

```
Q1 = Vcm*(2*C1+2*CP1+aC1+aCP1)+Vdm*(C1+CP1)

Q2 = -(Vcm+Vdm)*C1

Q3 = -Vcm*C2


A = (CP3+C1+C3+aCP3+aC1+aC3)

    * (2*CP1+2*C1+CPS+aCP1+aC1)/(C1+aC1) - 2*C1 - aC1


V2 = {Q1+Q3*(2*CP1+CPS+2*C1+aCP1+aC1)/(C1+aC1)}/A

V1 = V2*(CP3+C1+C3+aCP3+aC1+aC3)/(C1+aC1) - O3/(C1+aC1)

Vo = {-V1*C1+V2*(CP3+C1+C3)-Q2}/C3
```

SECTION 4.3 - Analysis of Second Order Effect of Switched Capacitor Instrumentation Amplifier

In this section, the effects on the circuit performance caused by the voltage dependent parasitic capacitance. MOS transistor body effect, finite op-amp voltage gain, and the nonlinear op-amp voltage gain characteristic are treated.

4.3.1 Voltage Dependent Parasitic Effect

The voltage coefficient of MOS capacitor is typically less than 5 ppm/volt. thus, any gain error contributed by this effect is very small that it can be ignored [39]. Therefore, gain nonlinearity effect caused by the voltage dependent p-n junction capacitance would be more important.

In this circuit. the capacitors are always charged or discharged to steady states. The charged stored in the junction capacitor shown in Fig.4.6 is related to its voltage by the following equations [24] :

$$Qcpv = A*q*Na*W$$

$$\text{where } W = [2E(phi+V)/qNa]^{1/2}$$

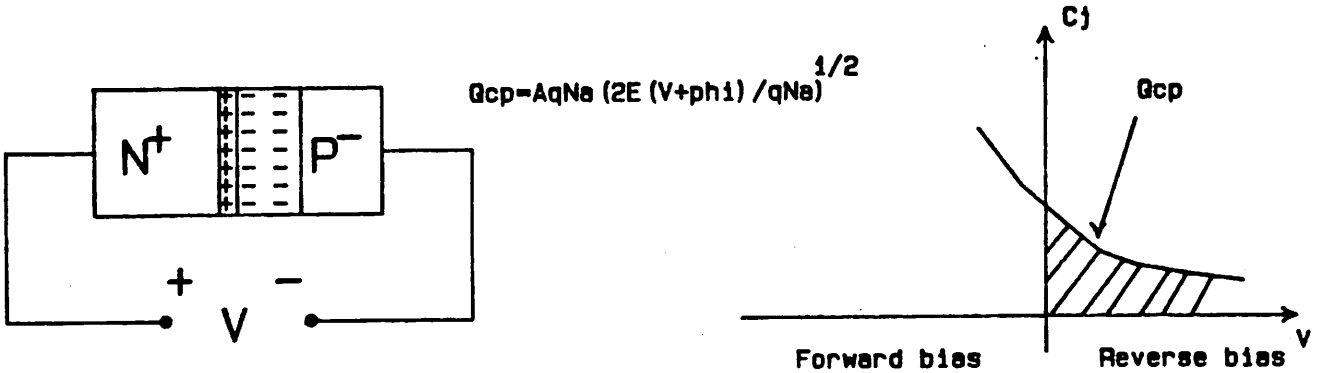


Fig.4.6 Voltage Dependent Junction Capacitance

W is the depletion width assumes one sided abrupt junction with the source/drain doping density Nd much larger than the substrate doping concentration Na. A is the cross-sectional area of the junction, q is the electron charge. E is the permitivity of the silicon substrate, and phi is the built-in potential of the p-n junction. Qcpv can be rewritten as :

$$Qcpv = CPv0*[phi+V]^{1/2}$$

CPv0 is the normalized depletion capacitance when phi+V equals one volt. The body effect of MOS transistors is essentially the depletion charge modulation effect in the channel-substrate depletion region. Thus, the body effect will have the same characteristic as that of the source/drain p-n junction assuming the threshold implanted region is fully depleted by proper substrate biasing. Therefore, the body effect on the switch channel charge of the input switches M1. M2. and the switch M3 can be included in the voltage dependent junction capacitance effect of the two parasitic capacitors CP1. and CP2 at the two input nodes.

By combining the finite op-amp voltage gain Av together with the voltage dependent capacitance. the circuit equations formulated in the last section will be modified as follows:

During the sample mode.

$$Qc1 = (Vcm+Vdm)*C1$$

$$Qc2 = (Vcm+Vdm)*C2$$

$$Qcp10 = (Vcm+Vdm)*CP10$$

$$Qcp1v = CP1v0*[(phi+Vbb+Vcm+Vdm)]^{1/2}$$

$$Qcp20 = Vcm*C2$$

$$Qcp2v = CP2v0*[(phi+Vbb+Vcm)]^{1/2}$$

$$Qc3 = Qc4 = 0$$

$$Qcp30 = Qcp40 = 0$$

$$Qcp3v = Qcp4v = 0$$

where CP10, CP20, CP30, CP40 are the voltage independent parasitic capacitances at the corresponding nodes 1, 2, 3,

and 4. CP1v0; CP2v0, CP3v0, and CP4v0 are the voltage dependent parasitic capacitances at these nodes, respectively. Vbb is the substrate bias voltage, and phi is the junction built-in voltage.

During the hold mode

$$Q1 = (V1-V2)*C1 + (V1-V3)*C2 + V1*(CP10+CP20) + (CP1v0+CP2v0)*(phi+Vbb+V1)^{1/2} + CPS*[V1+GAMMA*(phi+Vbb+V1)]^{1/2}$$

$$Q2 = V2*CP30 + CP3v0*(phi+Vbb+V2)^{1/2} + (V2-V1)*C1 + (V2-Vo)*C3$$

$$Q3 = V3*CP40 + CP4v0*(phi+Vbb+V3)^{1/2} + (V3-V1)*C2 + V3*C4$$

$$Vo = (V3-V2)*Av \quad \text{and}$$

$$Q1 = Qc1+Qcp10+Qcp1v+Qc2+Qcp20+Qcp2v$$

$$Q2 = -Qc1$$

$$Q3 = -Qc2$$

The above equations can be reorganized into three nonlinear equations with three unknowns, V1, V2, and Vo as follows:

$$V1*[C1+C2+CP10+CP20+CPS] - V2*[C1+C2] - C2*Vo/Av$$

$$= Q1 - V1*C1 + V2*[C1+C3+CP30] - Vo*C3$$

$$- (CP1v0+CP2v0)*(phi+Vbb+V1)^{1/2} - CPS*[GAMMA*(phi+Vbb+V1)]^{1/2}$$

$$= Q2 - CP3v0*(phi+Vbb+V2)^{1/2}$$

$$- V1*C2 + V2*[C2+C4+CP40] + [CP40+C2+C4]*Vo/Av$$

$$= Q3 - CP4v0*(phi+Vbb+V2+Vo/Av)^{1/2}$$

4.3.2 Nonlinearity of Op-Amp Open Loop Gain

The nonlinear voltage transfer function of an operational amplifier shown in Fig.4.7 can be modelled to the first order as:

$$Vo = Vt*Tanh(Vi*Av0/Vt)$$

$$Av = Vo/Vi$$

Av0 is the small signal voltage gain of the op-amp. at Vo equal zero volt. Vt is the voltage at which the small signal voltage gain of the op-amp starts to decrease drastically. Vt is determined by the op-amp characteristics. In the circuit implementation to be described in next section, this Vt is mainly determined by the depletion load MOSFET being driven out of the saturation region.

To get a closed form equation for the output voltage Vo from the equations formulated previously is very complicated. Thus, a computer program [Appendix B] was written to evaluate the output voltage with respect to different parameter variations. The parameters used in the simulation are shown in Fig.4.8. The simulation results are shown in Fig.4.9 through Fig.4.15.

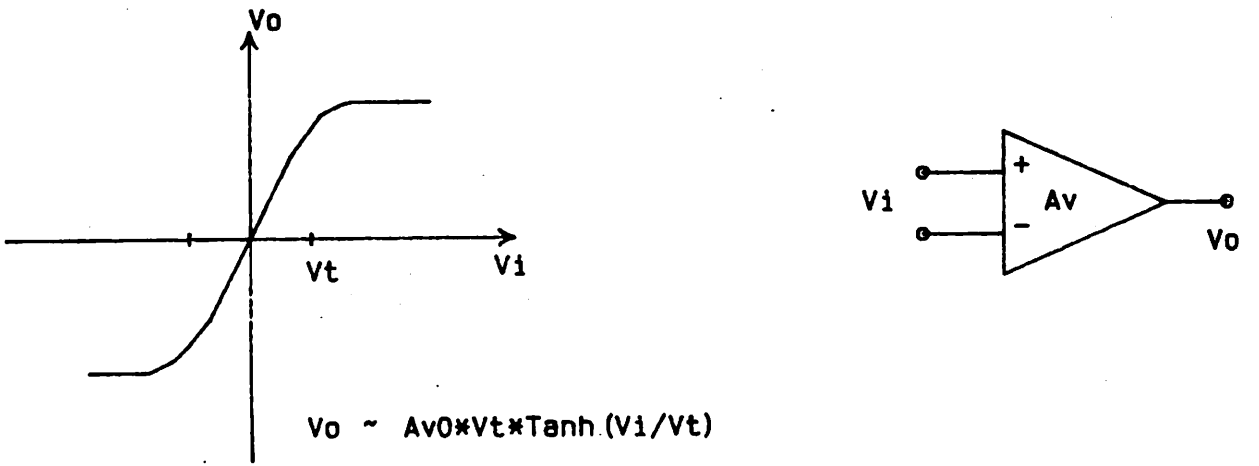


Fig.4.7 Voltage Transfer Curve of an Op-Amp

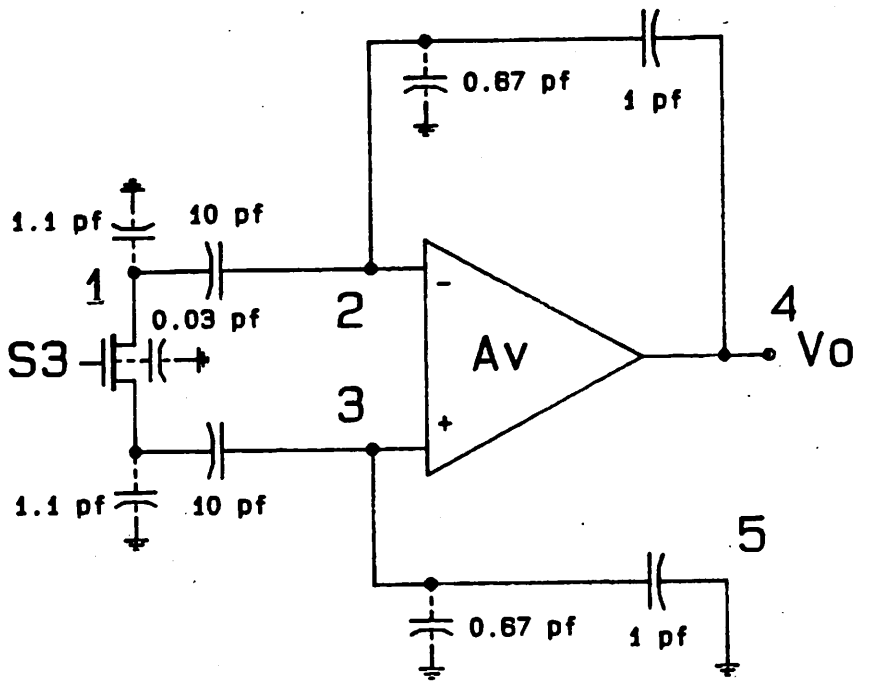


Fig.4.8 Circuit Schematic for Computer Simulation

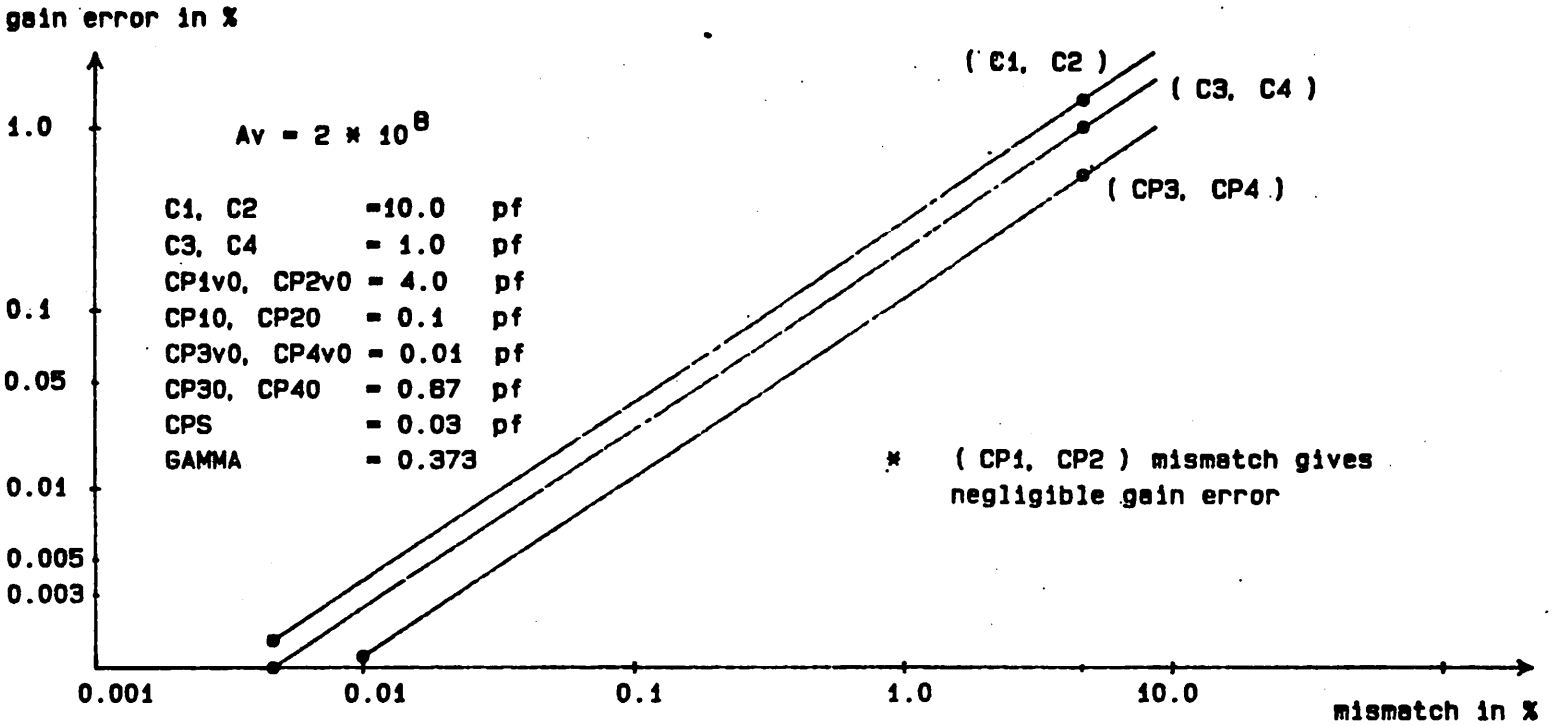


Fig.4.9 Gain Error w.r.p. Capacitance Mismatch with $Av=2*10^8$

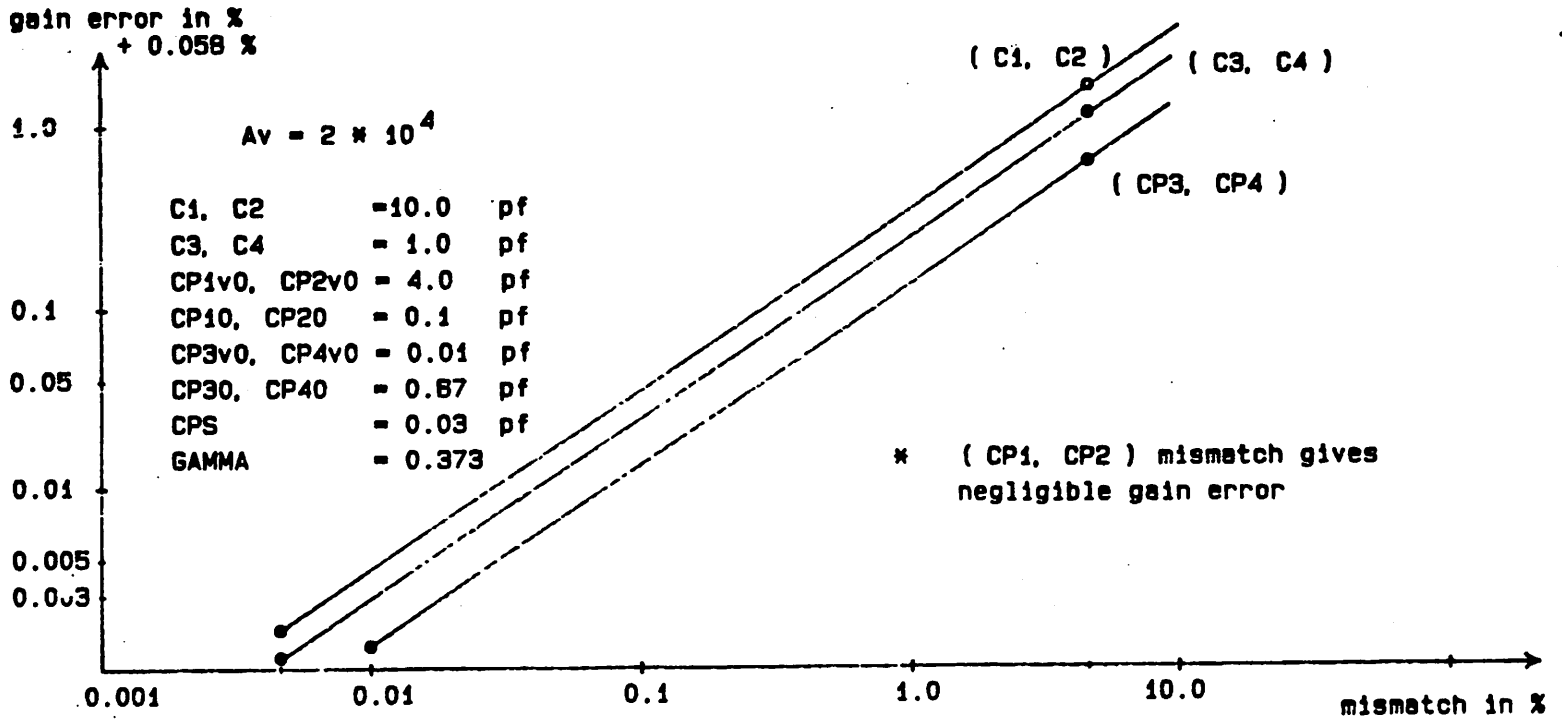


Fig.4.10 Gain Error w.r.p. Capacitance Mismatch with Av=20000

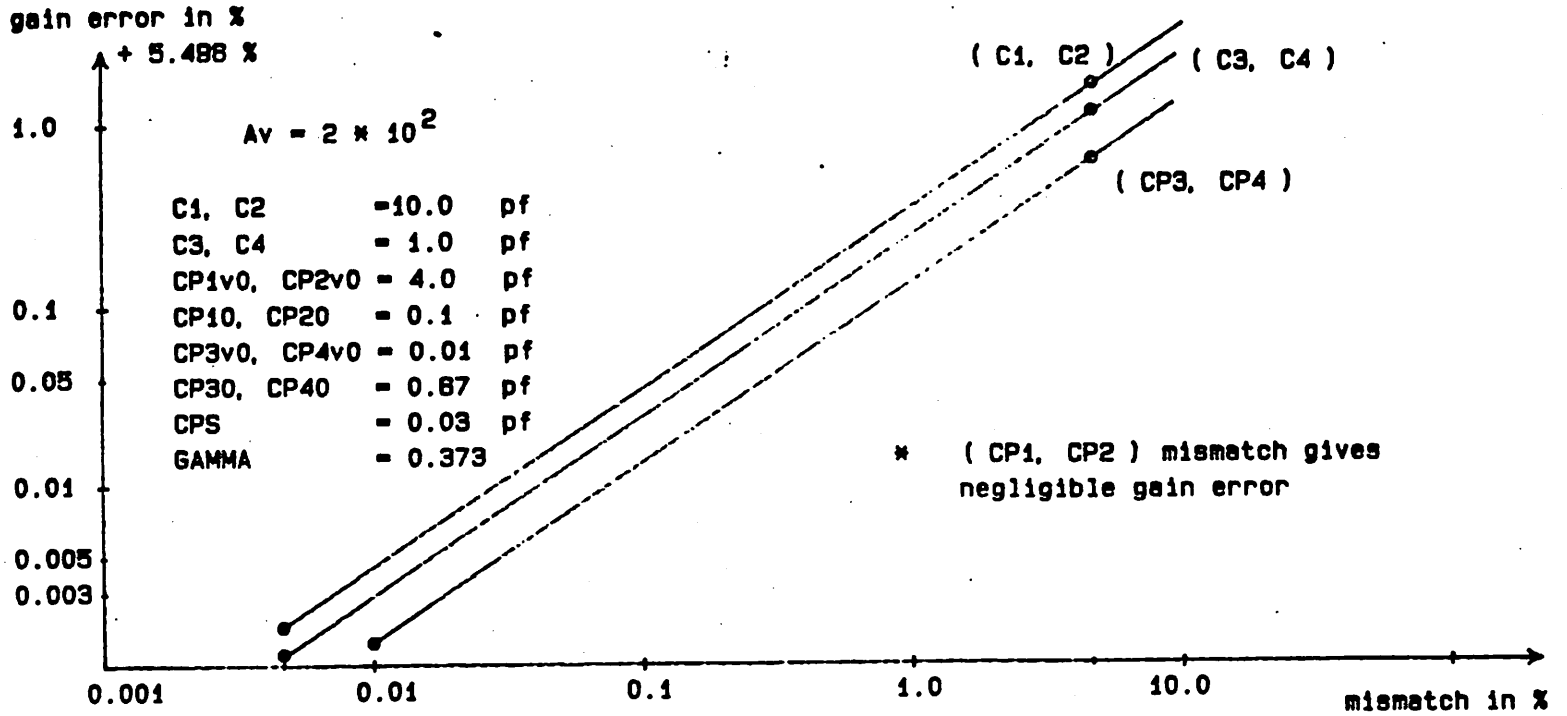


Fig.4.11 Gain Error w.r.p. Capacitance Mismatch with Av=200

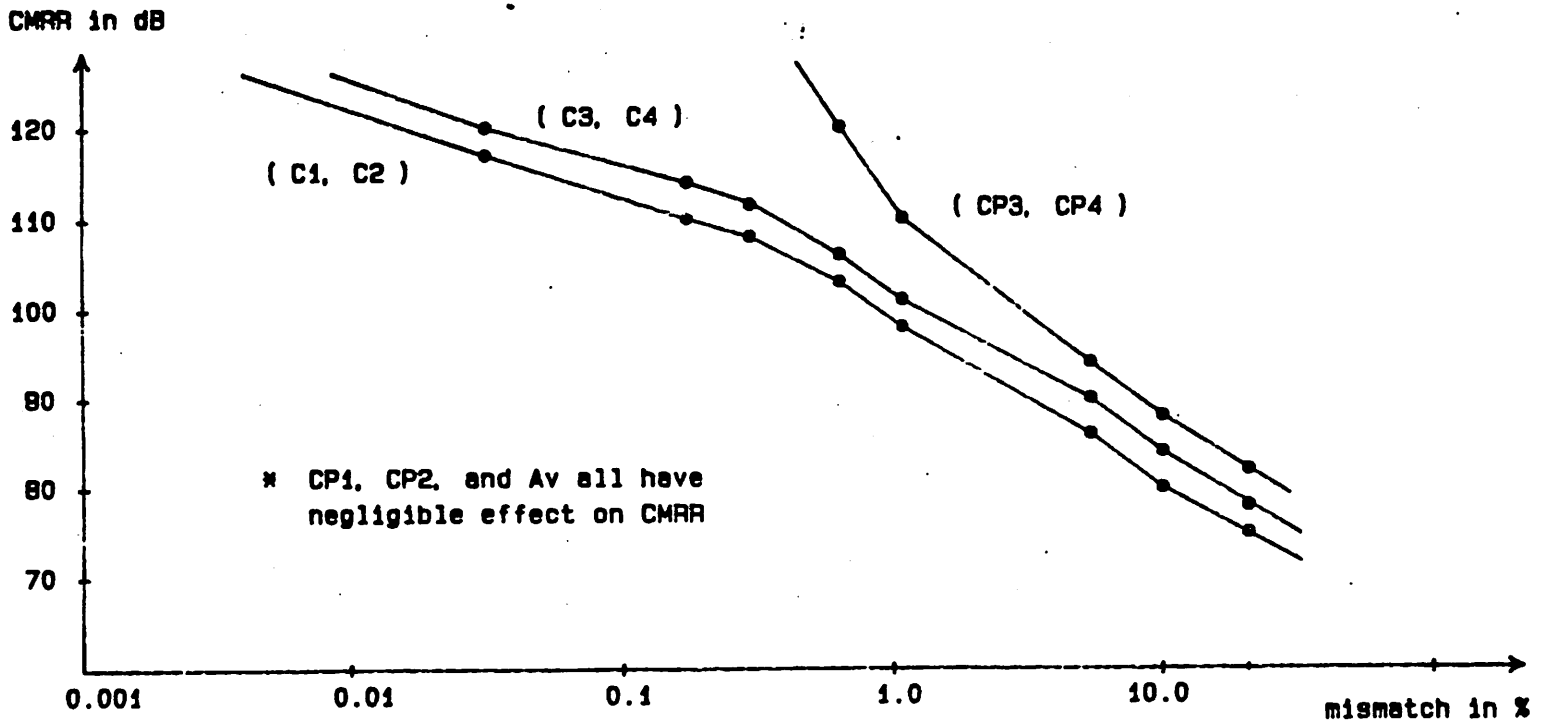


Fig.4.12 CMRR w.r.p. Capacitance Mismatch

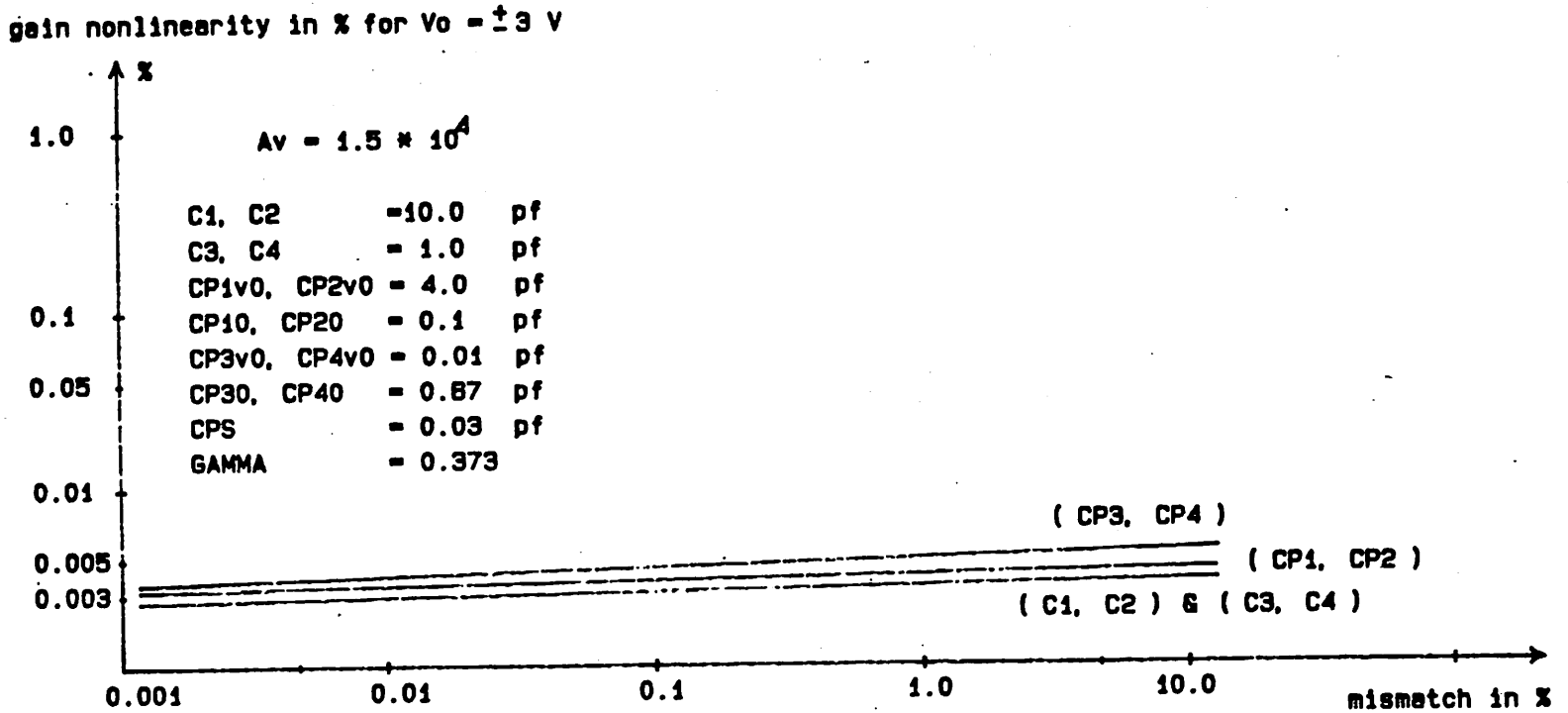


Fig.4.13 Gain Nonlinearity w.r.p. to Capacitance Mismatch

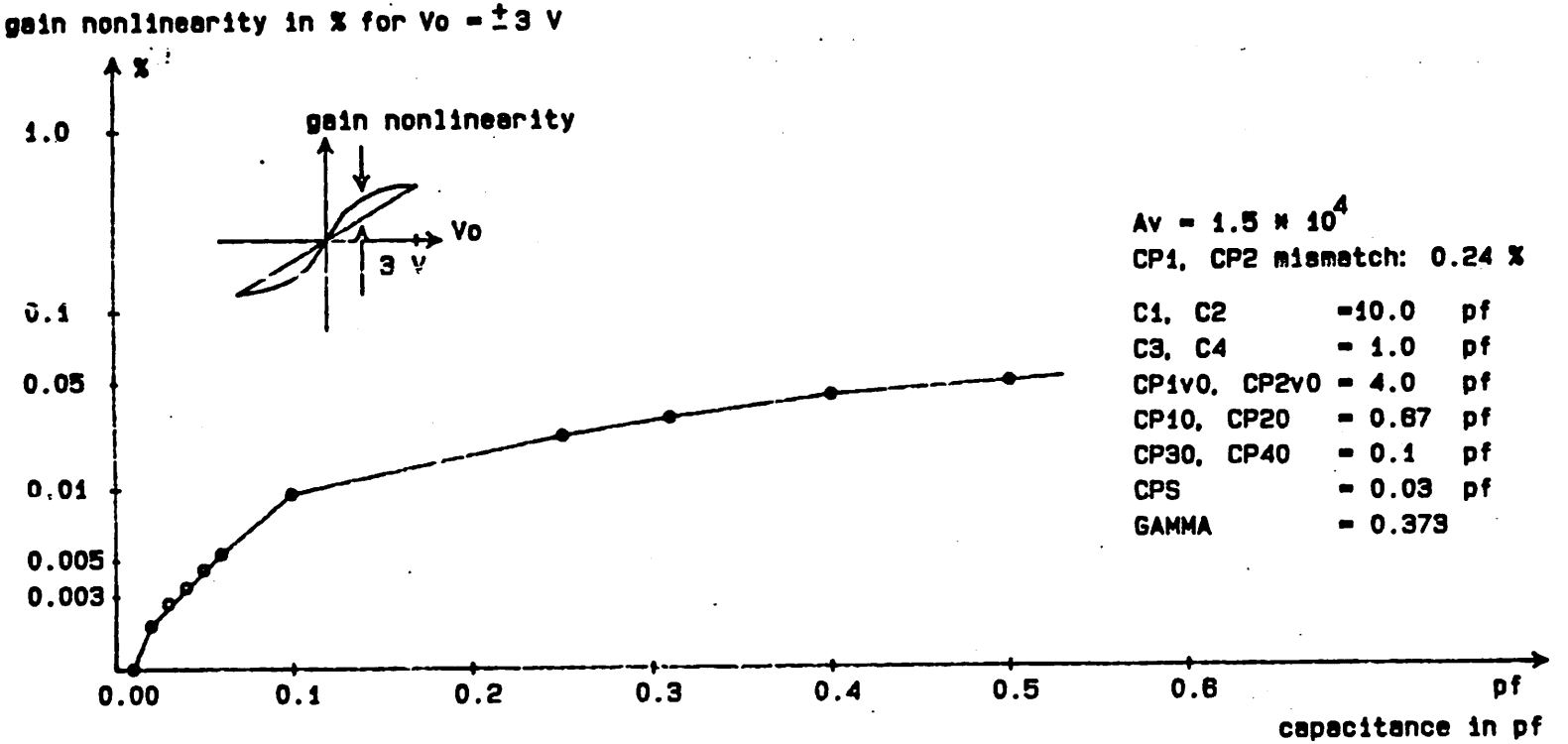


Fig.4.14 Gain Nonlinearity w.r.p. Voltage Dependent Parasitic Cp3 & Cp4

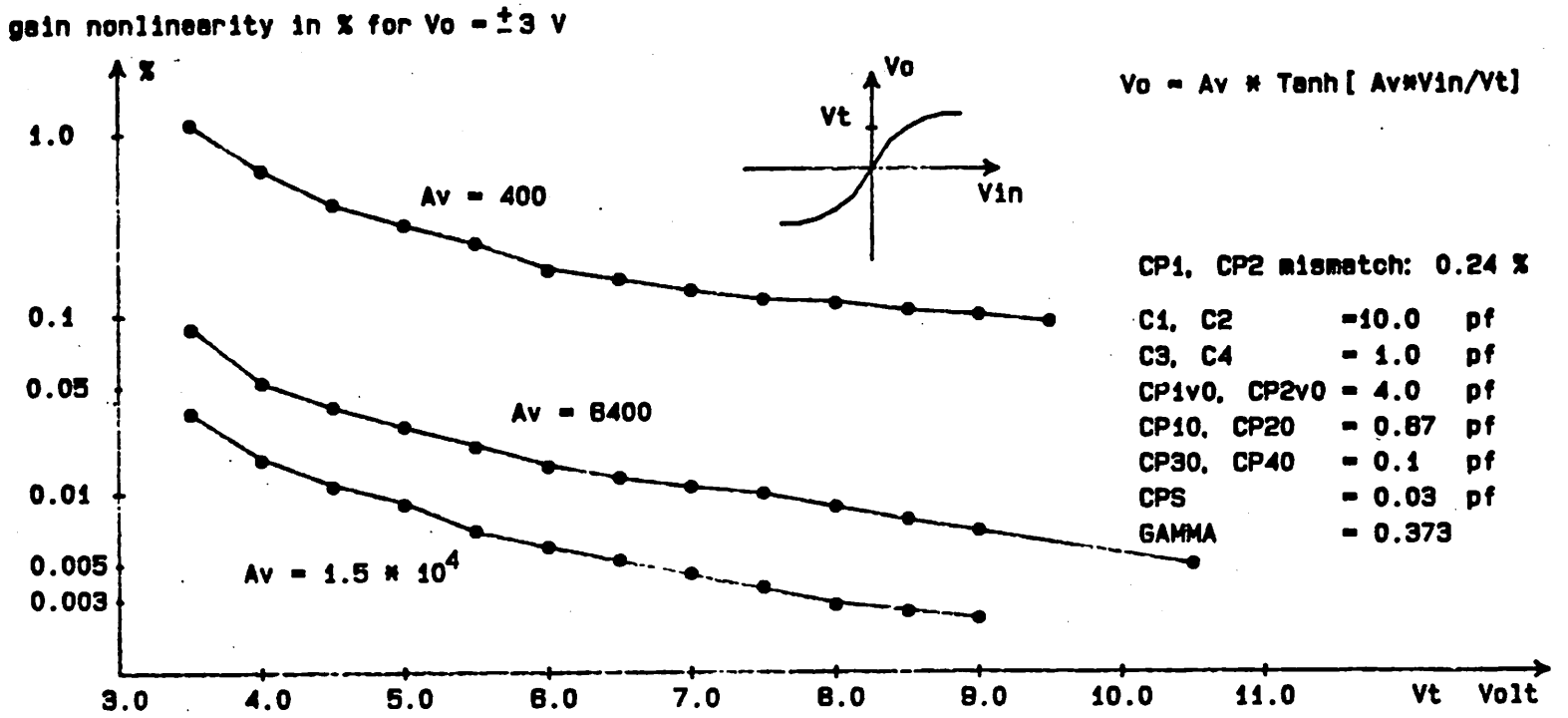


Fig.4.15 Gain Nonlinearity w.r.p. Op-Amp Open Loop Gain Nonlinearity

4.3.3 Input Switches Induced Error

The mismatch of the input switches will introduce a fixed gain error due to the dumping of additional signal charges into the sampling capacitors when the input switches are turned off. CMRR and offset are degraded even more seriously by the dumping of unequal charges into the sampling capacitors. This problem can be partially solved by the use of two additional switches M4 and M5 as shown in Fig.4.16.

The two switches M4 and M5 are connecting the top plates of the capacitors to ground. Because of the low impedance ground point. the switches M4 and M5 will be turned off slightly faster than the input switches M1 and M2. according to the model used in chapter 3. Therefore, the switches M4 and M5 serve as large resistors in series with the sampling capacitor charging path. As a consequence of this imbalance in impedance level at input switches' drain and source. a large portion of the input switches' channel charge will be injected back to the driving source when the input switches are turned off.

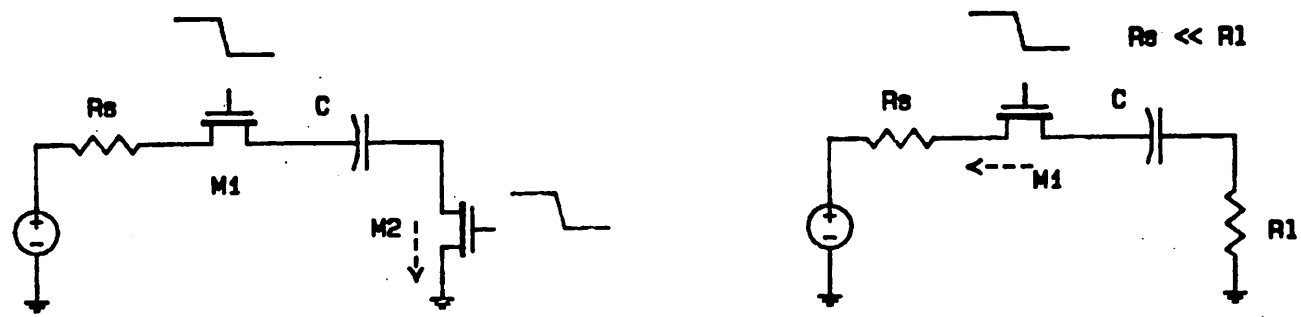
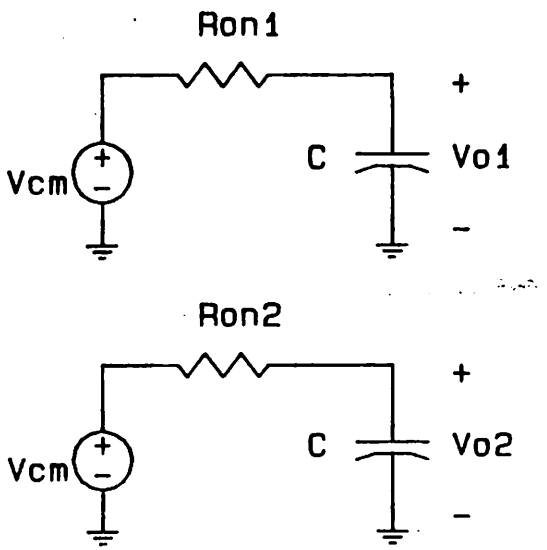
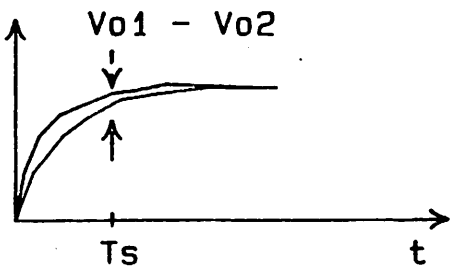


Fig.4.16 Input Switch Channel Charge Injection





$$CMRR\ dc = 20 * Log\left[e^{-Ts/t1} - e^{-Ts/t2} \right]^{-1}$$

Fig.4.17 CMRR Degradation due to Charging Time Mismatch

The channel charges injected by the two bottom switches M4 and M5 do not cause any significant error or any CMRR degradation because of the following reasons:

(1) The amount of charge injection into the sampling capacitors is very small because of the very low impedances of the metal ground line.

(2) The switch channel charges of M4 and M5 are independent of the input signal.

The mismatch of the input switches M1, M2 does not contribute to CMRR degradation. However, it does cause the two sampling capacitors to be charged to two different values during the sampling mode. Referring to Fig.4.17, the mismatches of the two input switches M1, M2 and that of the bottom switches M4, M5 are represented by different resistors R1 and R2 which stand for the switch turn-on resistors.

4.3.4 Summary of Circuit Description

From the data shown in the figures in 4.3.2 and 4.3.3, certain conclusions can be made regarding this circuit:

1. The gain error is determined primarily by the open loop gain of the op-amp.

2. The parasitic capacitance at the input nodes CP1, CP2 and CPS have negligible effect on the overall gain accuracy or CMRR of the circuit.

3. The parasitic capacitances at the amplifier summing nodes, CP3, and CP4, (both voltage independent part and voltage dependent part) have significant effects on circuit gain accuracy and gain nonlinearity. Although CP3 and CP4 are small capacitances, the matching of CP3 and CP4 is poor because of the large W/L input devices of the op-amp. Therefore, CP3/CP4 mismatch would be much larger than that of C1/C2 or C3/C4.

4. Gain nonlinearity is very sensitive to the size of the voltage dependent junction capacitance CP3v and CP4v at the summing nodes of the amplifier, even

if the matching between them is good. Half of the output voltage swing appears across these nodes. This alters the amount of charge flowing into the feedback and sampling capacitors by changing its node capacitance, hence altering the voltage gain when output voltage changes.

5. Common mode rejection ratio (CMRR) is very high. It is almost independent of any circuit parameter variations. Therefore, the CMRR is only limited by the mismatch of the two input switches. which not only introduces a fixed gain error and a common mode channel charge injection mismatch, but also yields a mismatch in the input capacitors' charging time. which will dominate the CMRR performance as the frequency goes up.

This S/C instrumentation amplifier has many advantages compared to other circuit techniques [37,40,41]. The amplifier does not experience any common mode shifts. Overall common mode rejection of the circuit is independent of the common mode rejection of the operational amplifier. As a consequence of the balanced nature of this circuit, switch charge injection and clock feedthrough are cancelled

to the first order. Equal and opposite voltage excursion on the capacitors eliminates capacitor nonlinearity to the first order.

Sampling bandwidth of this circuit is determined by the RC time constant of the input switch and capacitor. This time constant usually is much faster than the settling time of an operational amplifier. The gain is set by capacitor ratios, which has good initial accuracy [38], high temperature stability and is trimmable. Both the 1/f noise and the dc offsets are reduced by the use of double correlated sampling (DCS). The power supply rejection is also very high due to the use of DCS technique.

The overall performance of this circuit is limited by the mismatch of charge injection from the input switches. In this switched capacitor instrumentation amplifier circuit, cancellation of switch channel charge injection is achieved by circuit symmetry. The offset becomes limited primarily by the mismatches of the switch charge injection.

SECTION 4.4 - Experimental Implementation of Switched Capacitor Instrumentation Amplifier

Precision preamplifiers may be required to provide voltage gains ranging from 1 to 1000 [37]. The use of a single stage to obtain high voltage gain requires operational amplifiers with very large open loop gain. and very large capacitor ratios. In NMOS technology, the open loop voltage gain achievable in operational amplifier is often limited [4], and as a result. it is more desirable to use a relatively small fixed voltage gain for instrumentation amplifier. High voltage gain can be achieved by either cascading multiple low gain stages, or by using a single stage in a recirculating mode [42] as illustrated in Fig.4.18 and Fig.4.19 respectively.

In the circuit implementation described here. a fixed gain of ten per stage is used. Many A to D converters require a single-ended input voltage. Thus, a single-ended output referenced to ground must be produced. In this implementation, as shown in Fig.4.18, the first amplifying stage is fully differential. The last stage uses an operational amplifier to generate a single-ended output voltage.

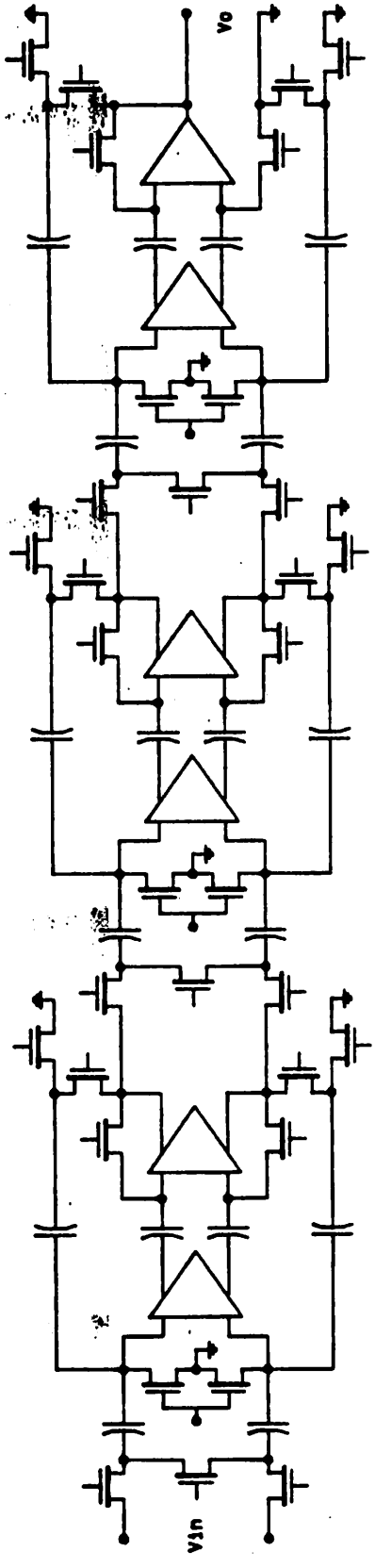


Fig.4.18 Cascaded S/H Instrumentation Amplifier

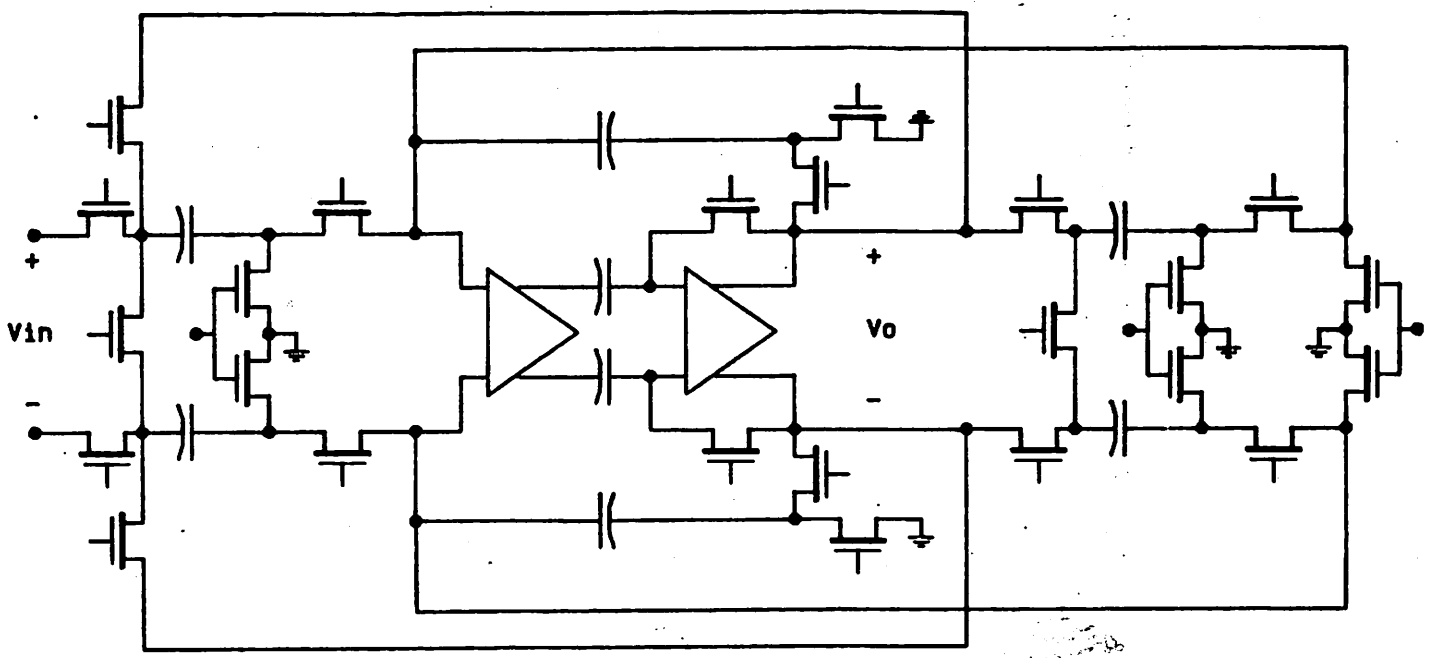


Fig.4.19 Cyclic S/H Instrumentation Amplifier

4.4.1 Operational Amplifier Design

The implementation of the DCS instrumentation amplifier shown in Fig.4.3 using NMOS technology poses some difficulties due to the fact that NMOS operational amplifiers generally have more parasitic poles and lower voltage gain per stage. These problems can be solved with a specially designed NMOS op-amp. In this section, the circuit constraints the DCS instrumentation amplifier imposed on the NMOS op-amp design, and the implementation of NMOS op-amps are described.

During the sampling mode, the switches are closed as shown in Fig.20a. The pole zero analysis circuit block diagram for amplifier A2 connected in unity gain feedback loop is shown in Fig.20b. It is clear that amplifier A2 in Fig.4.20.b is a differentiator, which has an additional pole due to the switches' turn-on resistance R1, R2, and the offset cancellation capacitors C5, C6. The series resistors M5, M6, implemented by MOS devices are inserted for proper pole-zero cancellation.

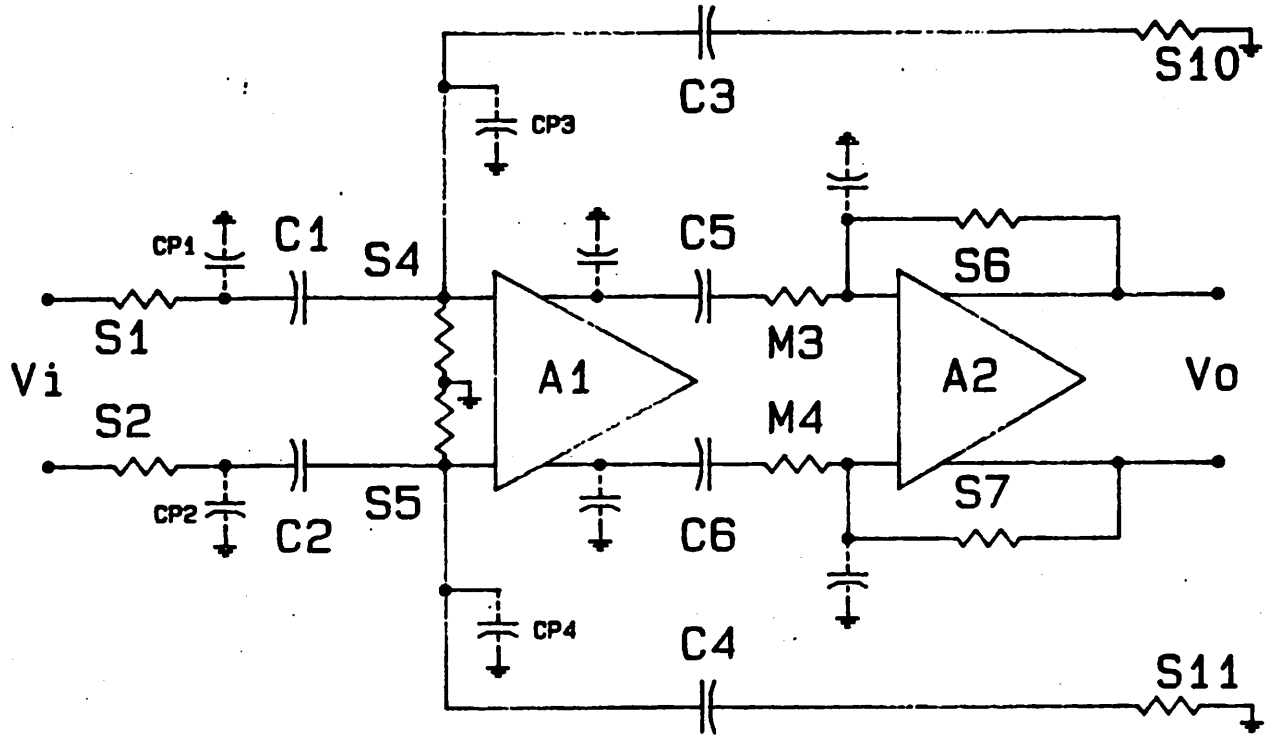


Fig.4.20a S/H Instrumentation Amplifier in the Sample Mode

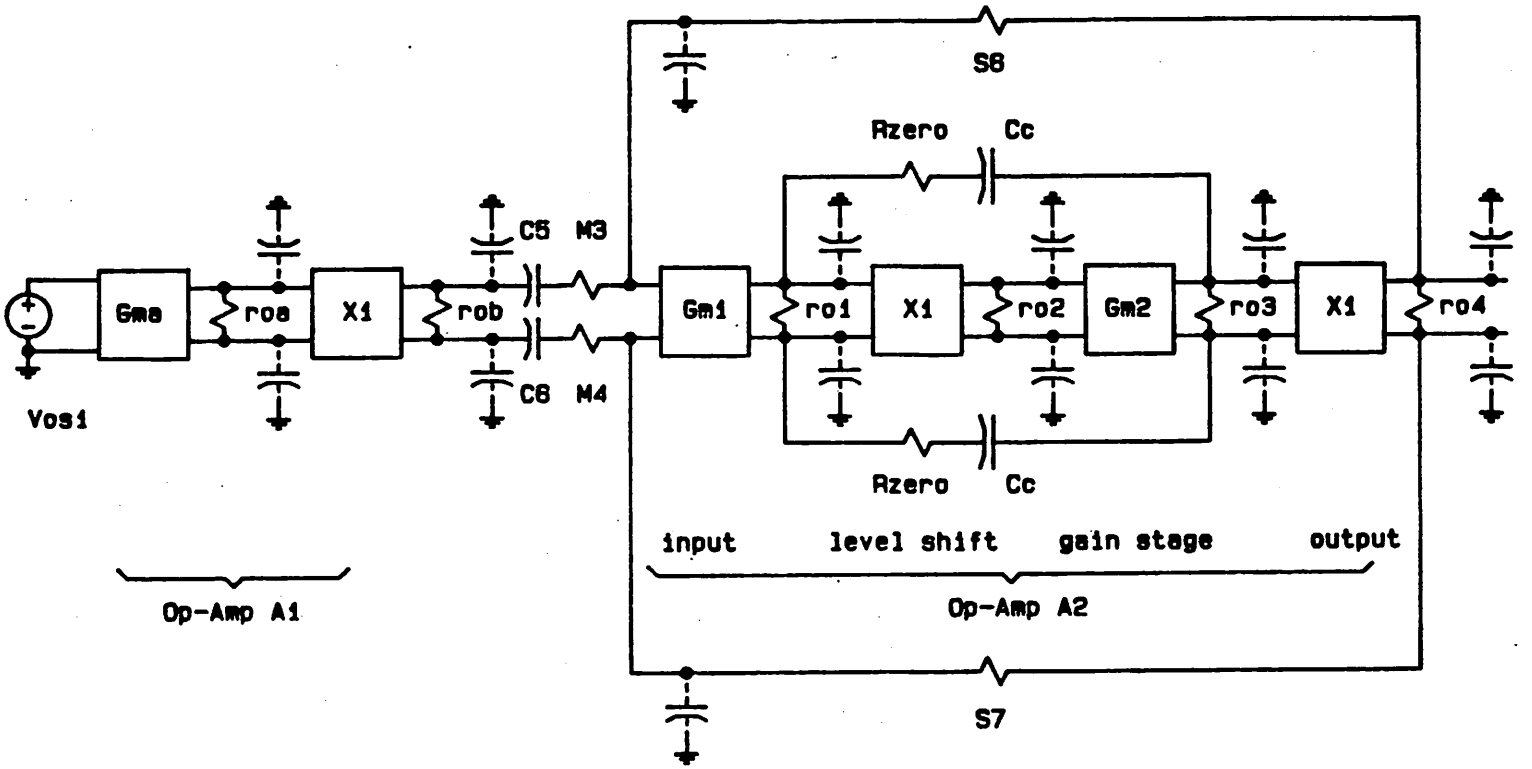


Fig.4.20b Small Signal Circuit of Op-Amps in the Sample Mode

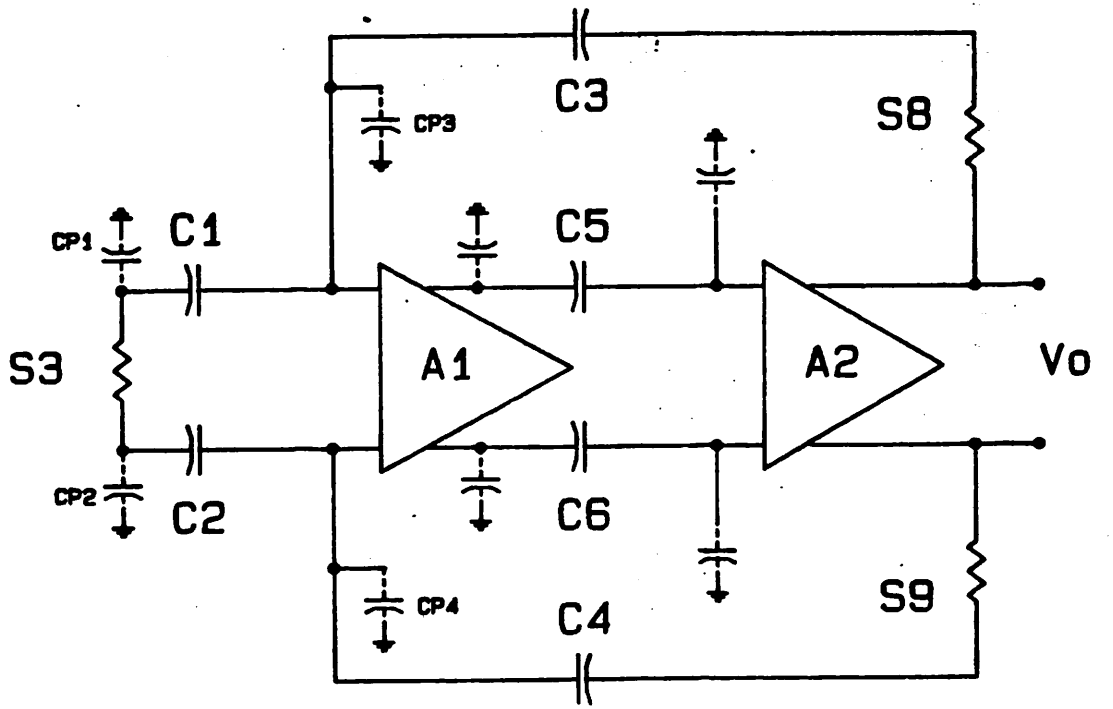


Fig.4.21a S/H Instrumentation Amplifier in the Hold Mode

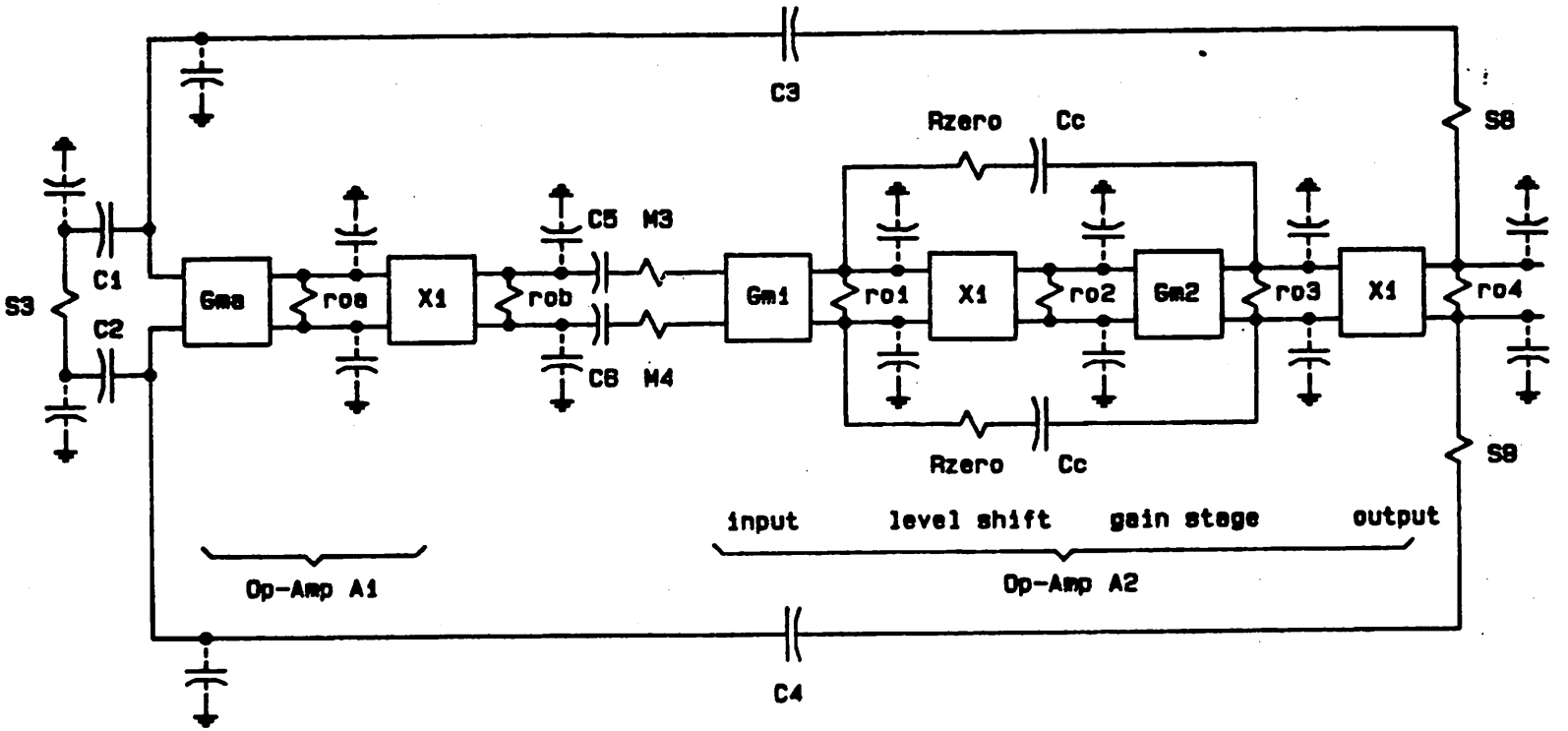


Fig.4.21b Small Signal Circuit of Op-Amps in the Hold Mode

In the hold mode, the switches are closed as shown in Fig.4.21.a. The pole zero analysis circuit block diagram for amplifier A1 and A2 connected in overall feedback loop is illustrated in Fig.4.21.b.

This global feedback loop consists of three gain stages, which normally have much worse parasitic pole positions than that of other configurations due to the higher output resistance associated with the gain stage. Therefore, the dominant pole of this circuit must be designed in such a way that the parasitic poles do not contribute too much phase shift at the unity gain frequency of the global feedback loop.

The instrumentation amplifier is designed for an operational speed of 200 kHz with 0.1% gain accuracy, the unity gain bandwidth of A2 is required to be larger than 500 kHz while it should also be as low as possible to reduce the effect of parasitic poles of the circuit.

For a 50% duty cycle of a 200 kHz sampling operation, the op-amp has to settle to within 0.1% of its final value within time T

$$T = 50\% * 1/200\ kHz$$

$$= 2.5\ uS$$

When the op-amp is connected in unity gain feedback configuration, its frequency response is shown in Fig.4.22.

$$H(S) = 1/\{1+S/(2*3.14159*Fu)\}$$

and the time domain unit step response is given by:

$$Vo(t) = 1 - \exp^{-t*(2*3.14159*Fu)}$$

where Fu is the unity gain frequency of the op-amp A2. It also assumes that the slew rate of this op-amp A2 is much faster than the settling time. For Vo(t) to reach 0.1% of its final value, it requires:

$$t*(2*3.14159*Fu) > 7$$

and $t = T = 2.5$ uS

thus $Fu > 7 / (2*3.14159*2.5uS)$

> 450 kHz

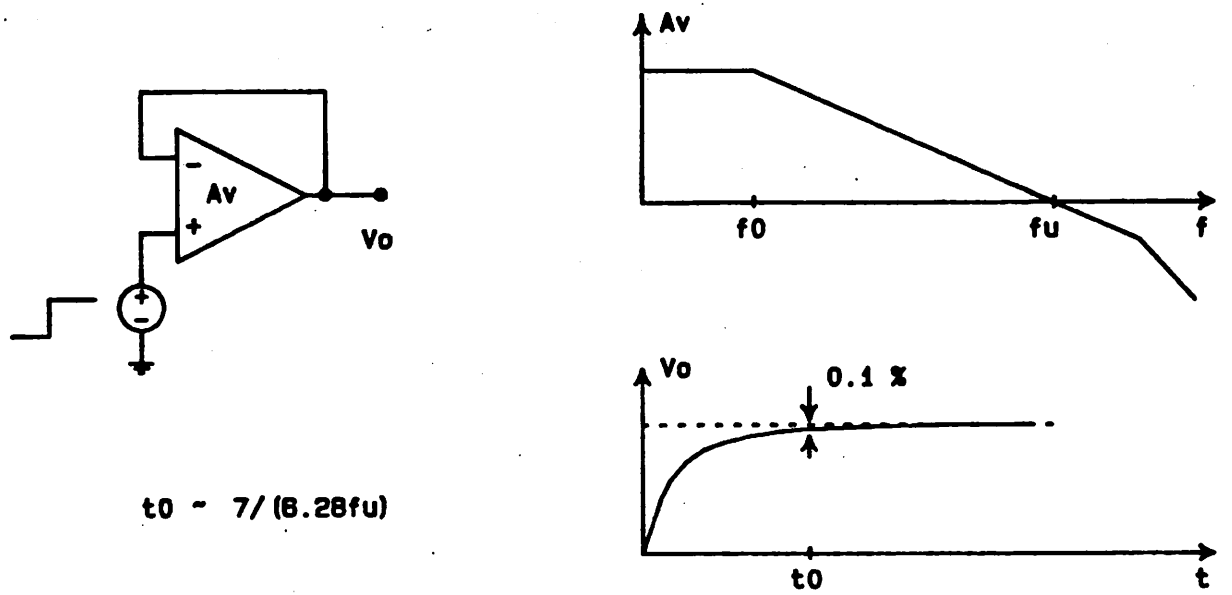


Fig.4.22 Frequency & Step Response of Op-Amp in Unity Gain Feedback

Special considerations have to be placed on the design of the operational amplifiers A1, A2 and the feedback switches. These design considerations are listed as follows:

4.4.1.1 Design considerations for amplifier A1

1. Its DC gain should be low enough so that its output does not get saturated by its own offset when the inputs are shorted as shown in Fig.20.a.

2. Its DC gain should be high enough so that the contribution of the channel charge injection error and noise voltage of the second amplifier A2 is minimized.

3. It must have a high enough bandwidth such that the closed loop feedback stability is assured in the hold mode as shown in Fig.11b.

4. It must have very low wide-band noise so that it will not limit the system's resolution.

4.4.1.2 Design considerations for amplifier A2

1. A2 must have a high DC voltage gain so the overall DC gain of amplifier A1 and A2 can provide enough feedback loop gain to achieve the desired gain accuracy.

2. It must be properly frequency compensated so as to assure stable operation for both the sample mode and the hold mode.

3. Common mode DC gain of the fully differential op-amp A2 must be less than one to assure the stability of the positive common mode feedback loop.

4.4.1.3 Some considerations regarding switches

1. Use minimum geometry to reduce channel charge injection.

2. Switch turn-on resistance should be minimized so as to move the parasitic poles to much higher

positions. The variation of turn-on resistance due to input signal changes and body effect are also important.

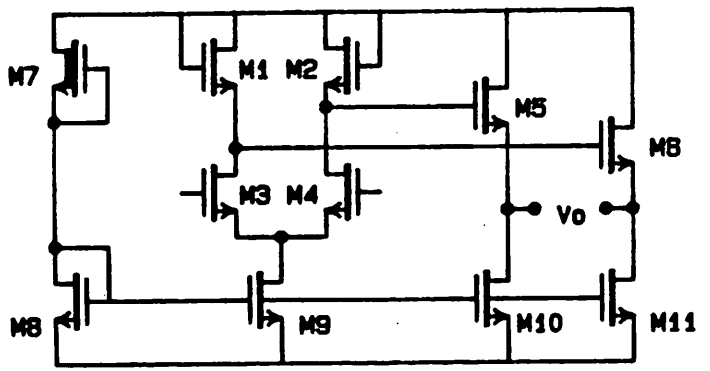
4.4.2 First Stage Amplifier A1

Shown in Fig.4.23 is the circuit schematic of amplifier A1 and a list of the device sizes used in this circuit. The bias circuit is made by transistors M1. M2, M7. M9, and M11. The DC biasing currents in this circuit track well with depletion mode threshold voltage variation. The current tracking is crucial to the frequency compensation of this circuit because the dominant pole and most of the parasitic poles/zeroes in amplifier A1 and A2 are closely related to the dc bias current. Therefore, poles and zeroes track well with each other, and the overall circuit feedback stability is always guaranteed.

High transconductance of the input devices are required to reduce the amount of thermal noise contributed by this amplifier, and low load resistances are required to maintain low voltage gain and higher bandwidth at the input stage.

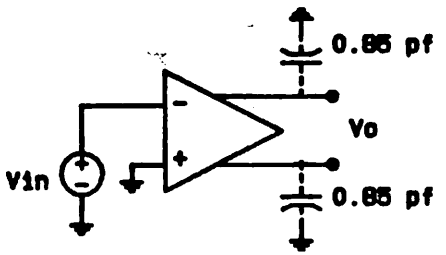
Thus, the enhancement mode transistors M3, M5 are used as loads to achieve a voltage gain of about 12. The wide bandwidth of this amplifier is also achieved by employing a source follower output stage to isolate the higher output loading capacitance from the high resistance node of the input stage.

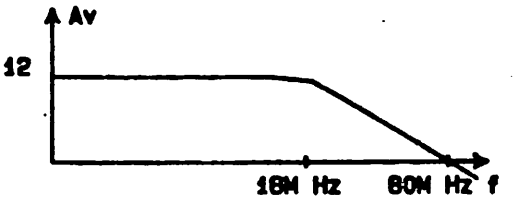
Fig.4.24 shows the simulated and measured open loop gain frequency response for a +- 7.5 volt power supply. The performance parameters of this amplifier is also listed. The measured offset voltage of this amplifier is less than 5 mV due to its fully differential configuration. Therefore, it is possible to increase the voltage gain of this amplifier without the output getting saturated by its own offset voltage.



DEVICE	W/L
M1	10/55
M2	10/55
M3	200/8
M4	200/8
M5	200/8
M6	200/8
M7	10/20
M8	120/25
M9	120/25
M10	120/25
M11	120/25

Fig.4.23 First Stage Op-Amp Circuit Schematic





Voltage Gain	12.0
Bandwidth	18M Hz
CMRR (dc)	~80 dB
PSRR (dc)	~80 dB
Input Offset	< 5 mV
Power Dissipation	2.2 mW

Fig.4.24 First Stage Op-Amp Performance Parameters

4.4.3 Second Stage Differential Operational Amplifier

The fully differential operational amplifier circuit schematic is shown in Fig.4.25. Its device sizes are listed in Table 4.1.

This amplifier uses two differential stages to achieve a voltage gain of about 1500. The replica bias circuitry [43] and common mode feedback of the input stage is composed of transistors M26, M27, and M1 through M7. They set the dc operating points for the input stage. Capacitor CM1 is used to frequency compensate the common mode feedback. Common mode frequency compensation is very important in high precision fully differential op-amp design. Due to the fact that common mode positive feedback occurs during the sampling mode, the overall common mode feedback loop gain must be much less than unity to achieve fast settling time in transient operation. Therefore, local feedback is required to reduce its overall common mode gain as well as to stabilize its dc operating conditions. As a result of the large common mode local feedback loop gain. capacitors CM1 and CM2 are required to ensure the proper common mode damping during transient operation.

The reference voltage is achieved [44] by stacking three enhancement mode transistors M23-M25. Though the bias current varies a lot with threshold voltage variation, the reference voltage is almost unaffected. Capacitors C1 and C2 are the Miller compensation capacitors. Transistors MC1 and MC2 are depletion mode devices connected as resistor for left half plane (LHP) zero compensation. The resistor value of these depletion mode devices tracks the dc bias currents of this circuit. Therefore, the relative position of this LHP zero and the parasitic poles of this circuit is roughly unaffected by process variations, hence, the circuit stability is assured.

The transconductance of the input stage is rather low in order to achieve low unity gain frequency without using a large compensation capacitor (Wu=Gm/C). The large input referred thermal and flicker noises associated with the use of low transconductance input stage are not crucial due to the use of double correlated sampling technique, and the use of a first stage amplifier A1. The output stage uses a simple source follower. Output voltage swing is limited to about one volt since this op-amp is to be used only at the front stage where the signal swing is small. Table 4.2 lists the op-amp performance parameters.

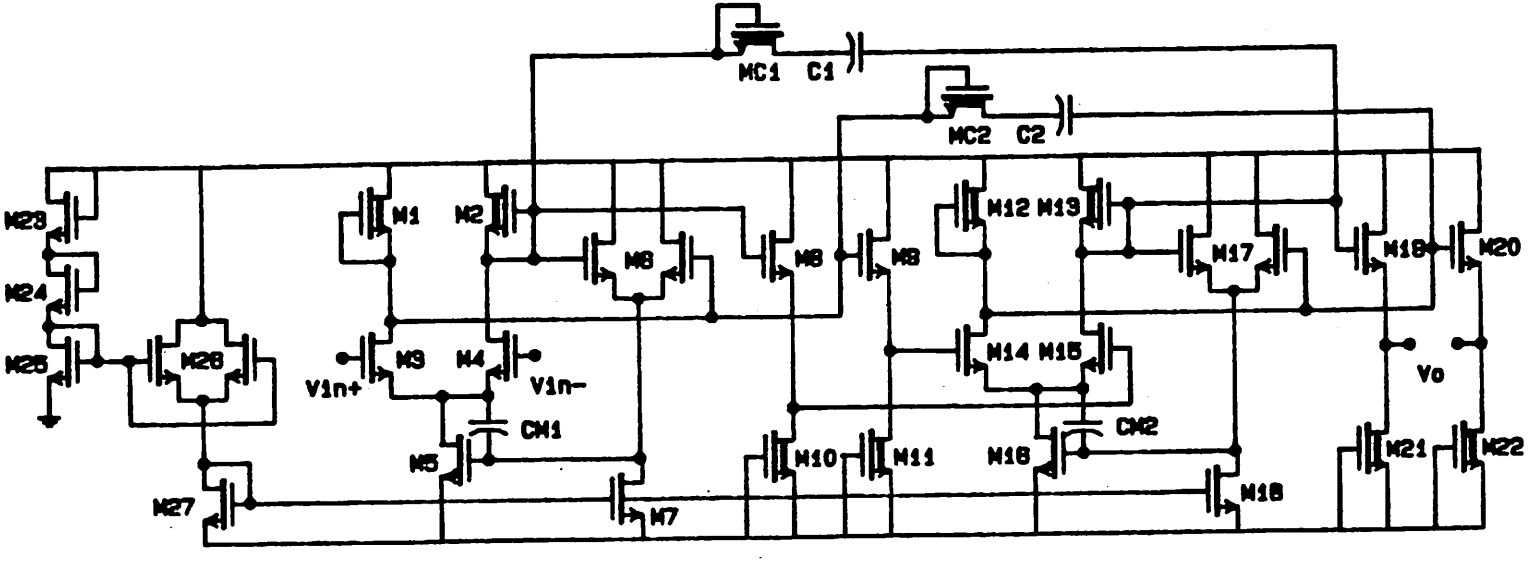


Fig.4.25 Fully Differential Op-Amp Circuit Schematic

DEVICE	SIZE	DEVICE	SIZE
M1	10/25	M18	140/7
M2	10/25	M19	200/10
M3	45/25	M20	200/10
M4	45/25	M21	40/20
M5	50/8	M22	40/20
M6	10/100	M23	50/10
M7	140/7	M24	50/10
M8	100/10	M25	50/10
M9	100/10	M26	10/100
M10	30/20	M27	140/7
M11	30/20	MC1	25/10
M12	17/25	MC2	25/10
M13	17/25	CM1	2.5 pf
M14	400/10	CM2	2.5 pf
M15	400/10	C1	6.0 pf
M16	85/8	C2	6.0 pf
M17	10/100		

Table 4.1 Differential Op-Amp Device Sizes

Open Loop Gain	1500
Input Offset	< 5 mV
Unity Gain Bandwidth	750K Hz
Phase Margin	95^{o}
Common Mode Rejection	90 dB
Power Supply Rejection	80 dB
Output Swing	$\pm$ 2.5 V
Slew Rate	3 V/uS
Power Dissipation	15 mW
Supply Voltage	$\pm$ 7.5 V

Table 4.2 Performance Parameters of Differential Op-Amp

4.4.4 Second Stage Single Ended Operational Amplifier A2

The single ended output operational amplifier shown in Fig.4.26 is a conventional NMOS op-amp design [43.45]. Transistors M1-M5, M20-M23, and M24-M29 are the input, gain, and output stages respectively. The input stage. bias circuitry, and common mode feedback circuit are similar to that of the fully differential op-amp which was described in the last section. The gain stage uses current injection technique to increase the transconductance of the gain stage. hence. improving its dc gain while pushes the right half plane (RHP) zero (Gm/C) to higher position. The push-pull output stage has a local feedback loop which comprises of transistors M26 and M28-M30 to achieve a low output resistance. This output stage has a capability to drive large capacitive load without losing a significant phase margin. Capacitors CZ and CZ1 are feedforward capacitors. CM is common mode compensation capacitor. CC is the Miller compensation capacitor. Depletion mode resistor. MC. is for RHP zero compensation. Only half of the input stage voltage gain is used. The sacrifice of a gain of two is traded for the elimination of a double-ended to single-ended conversion. hence eliminates an additional parasitic pole. Because of the DCS operation [Appendix A]

and the first stage amplifier A1, the dc offset and PSRR of this op-amp is not critical. This op-amp realizes a voltage gain of about 1500 with output voltage swing of about 6.5 volts. Table 4.4 lists the performance parameters of this op-amp.

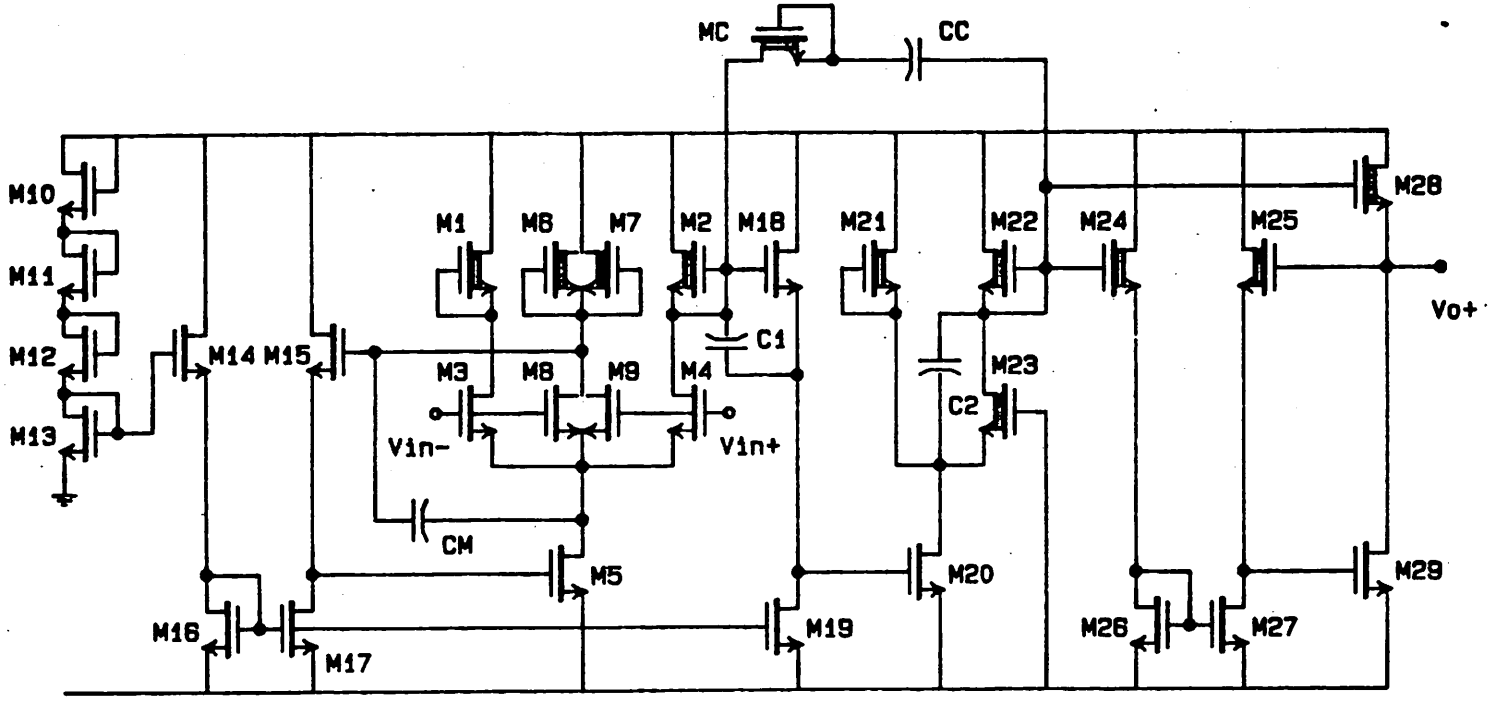


Fig.4.26 Single Ended Op-Amp Circuit Schematic

DEVICE	SIZE	DEVICE	SIZE
M1	10/25	M18	10/100
M2	10/25	M19	140/7
M3	45/25	M20	250/8
M4	45/25	M21	30/10
M5	50/8	M22	17/25
M6	10/25	M23	140/10
M7	10/25	M24	10/100
M8	45/25	M25	10/100
M9	45/25	M26	75/10
M10	50/10	M27	75/10
M11	50/10	M28	25/10
M12	50/10	M29	200/10
M13	50/10	MC	120/10
M14	10/100	C1	2.2 pf
M15	10/100	C2	1.2 pf
M16	140/7	CM	3.0 pf
M17	140/7	CC	6.0 pf

Table 4.3 Single Ended Op-Amp Device Sizes

Open Loop Gain	1500
Input Offset	30 mV
Unity Gain Bandwidth	750K Hz
Phase Margin	95^{0}
Common Mode Rejection	70 dB
Power Supply Rejection	60 dB
Output Swing	$\pm$ 4.5 V
Slew Rate	3 V/uS
Power Dissipation	30 mW
Supply Voltage	$\pm$ 7.5 V

Table 4.4 Performance Parameters of Single Ended Op-Amp

CHAPTER 5 - EXPERIMENTAL RESULTS OF SWITCHED CAPACITOR INSTRUMENTATION AMPLIFIER

5.1 Experimental IC Implementation

Experimental circuits for the fully differential stage and single ended output stage were designed and fabricated using a local oxidation poly-silicon gate NMOS process developed at the Berkeley IC Lab [Appendix C]. The minimum gate length used in these circuits was 7 um.

The replica capacitor structure [38] with a unit capacitance of 1 pF was used to satisfy the matching requirements for the gain accuracy and switch channel charge cancellation of the instrumentation amplifier circuits. Fig.5.1 shows the layout of the replica capacitor structure. This structure has the least sensitivity to misalignment error and process variation due to the symmetry of the polysilicon top plate which defines the capacitance. The bottom plate of the capacitor is implanted n+ region. The n+' region of these replicated capacitor units are connected together as an island in order to reduce the voltage dependent parasitic capacitance contributed by the perimeters of the n+ region.

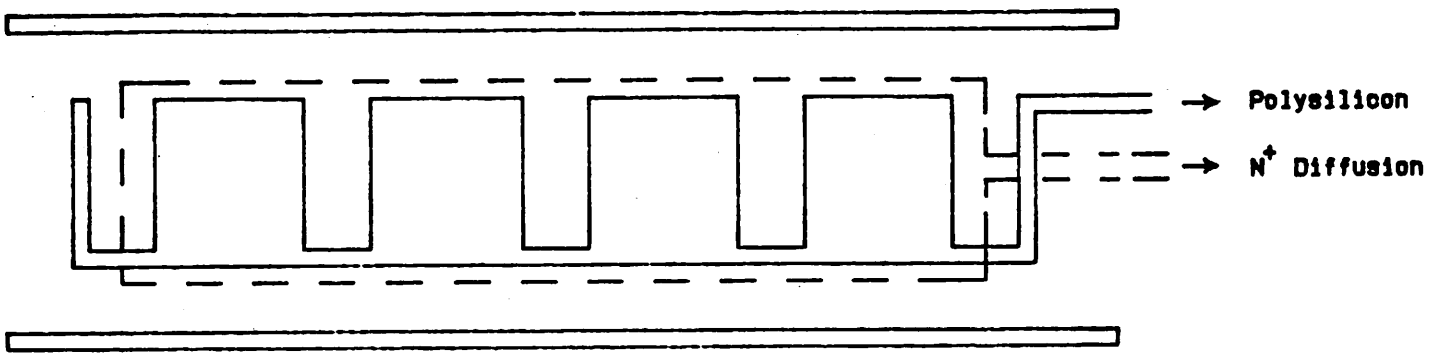


Fig.5.1 Replica Capacitor Layout Structure

The switches and opamps' input devices were laid out using mirror image technique for first order matching requirement. Common centroid or criss-crossed layout techniques are not necessary for these devices due to the additional layout complexity. In the circuits described here, input sampling capacitors are 10 pF each, feedback capacitors are 1 pF, and DCS capacitors are 3 pF. The input switches M1. M2 are 10u/10u, the offset-cancellation switches M6, M7 are 30u/10u.

The die photographes of the differential output and single ended output switched capacitor amplifiers are shown in Fig.5.2 and Fig.5.3 respectively. The top part of the die photo contains the matched capacitor arrays and the bottom part contains the differential amplifier. The symmetrical layout of the circuit is crucial to the matching of circuit components. The die area of these circuits are about 2500 square mils each.

The process yield of these circuits were quite high on the wafer level. However, for the ease of wafer probing on these experimental circuits. passivation glass was not applied onto the wafers. Therefore, a tremendous yield loss occured during scribing and packaging. Many packaged parts

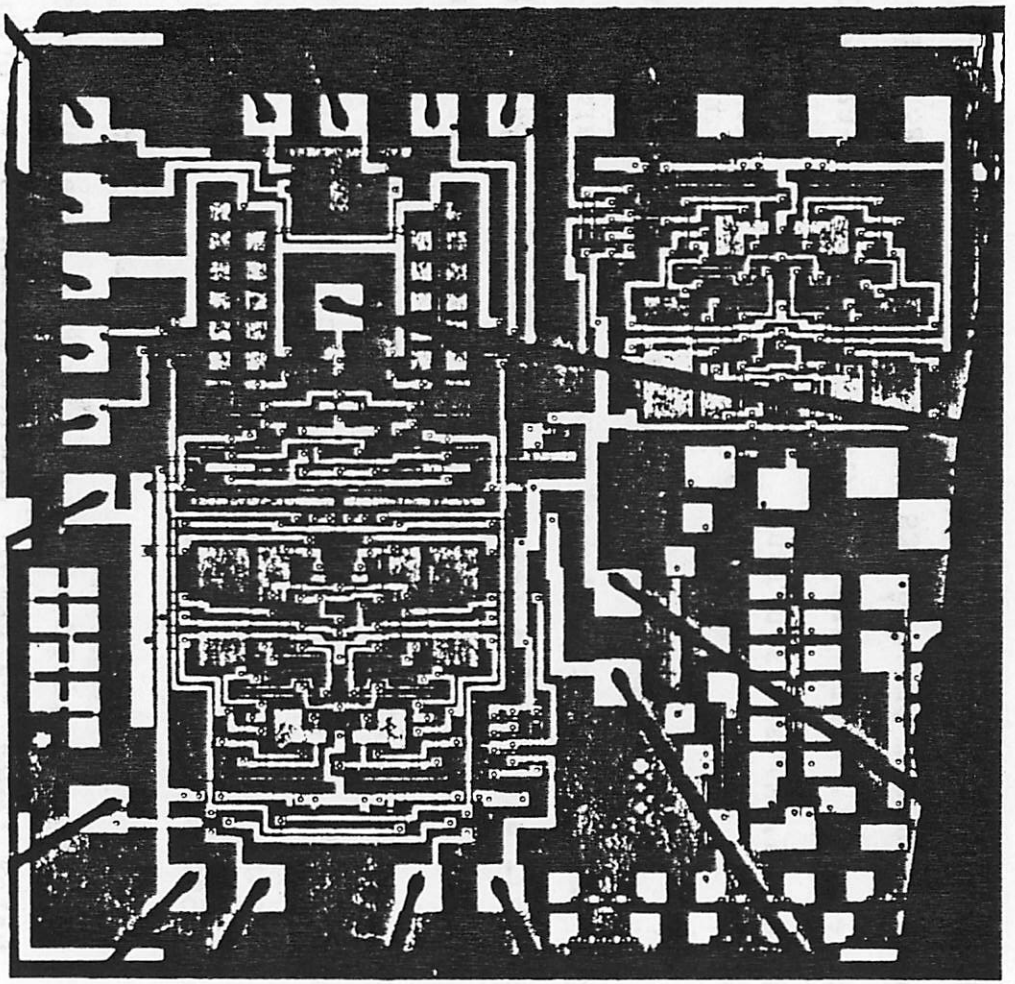


Fig.5.2 Chip Photomicrograph of the Differential DCS Switched Capacitor Instrumentation Amp

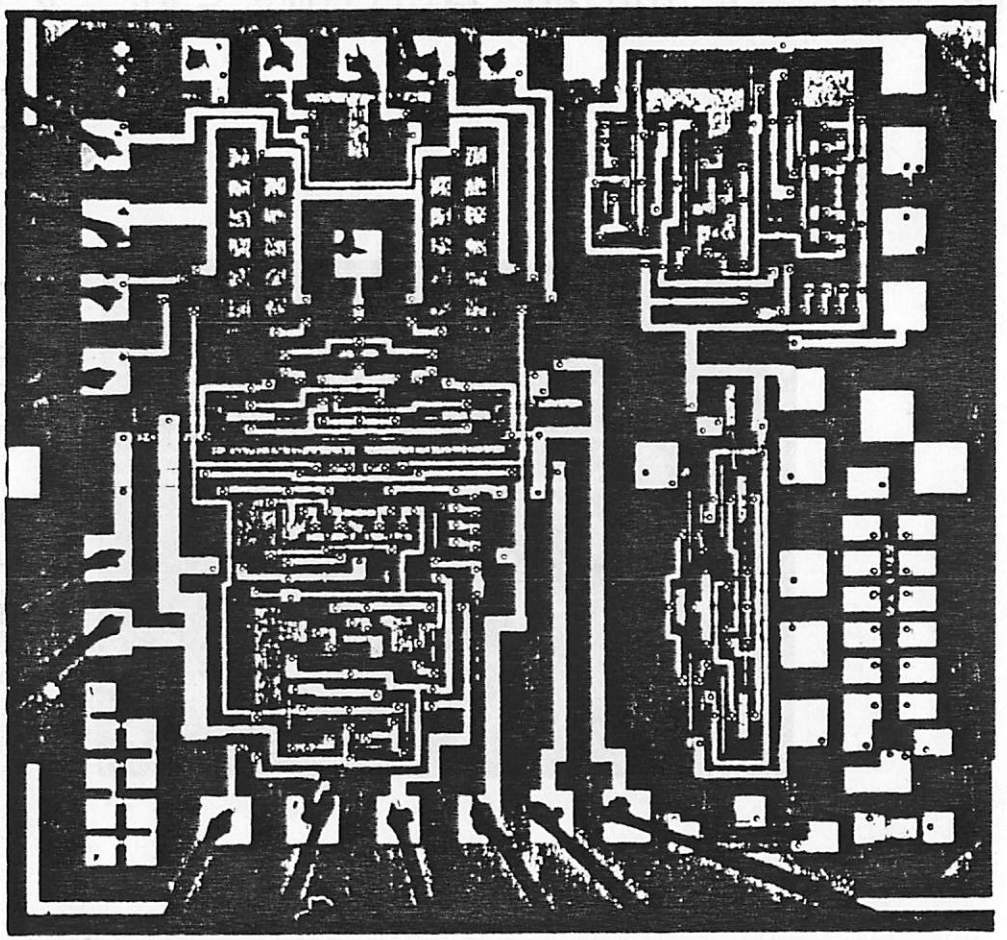


Fig.5.3 Photomicrograph of the Single Ended DCS Switched Capacitor Instrumentation Amp

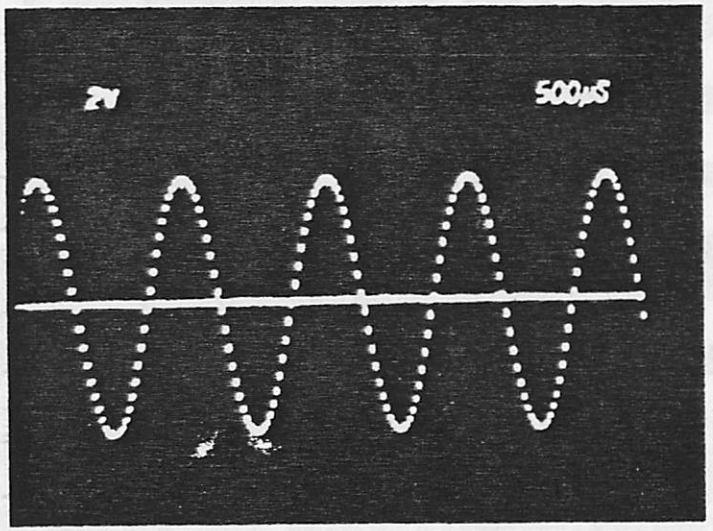


Fig.5.4 DCS Amplifier Output Waveform with Sinusoidal Input Signal

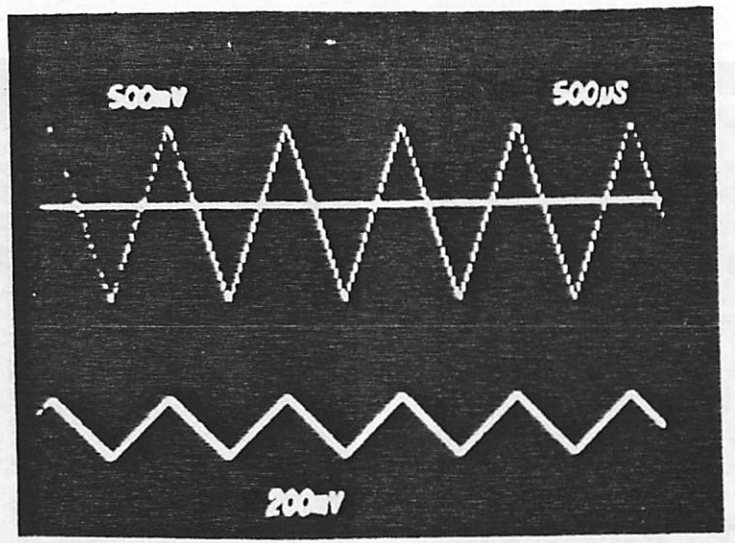


Fig.5.5 DCS Amplifier Output Waveform with Triangular Wave Input Signal

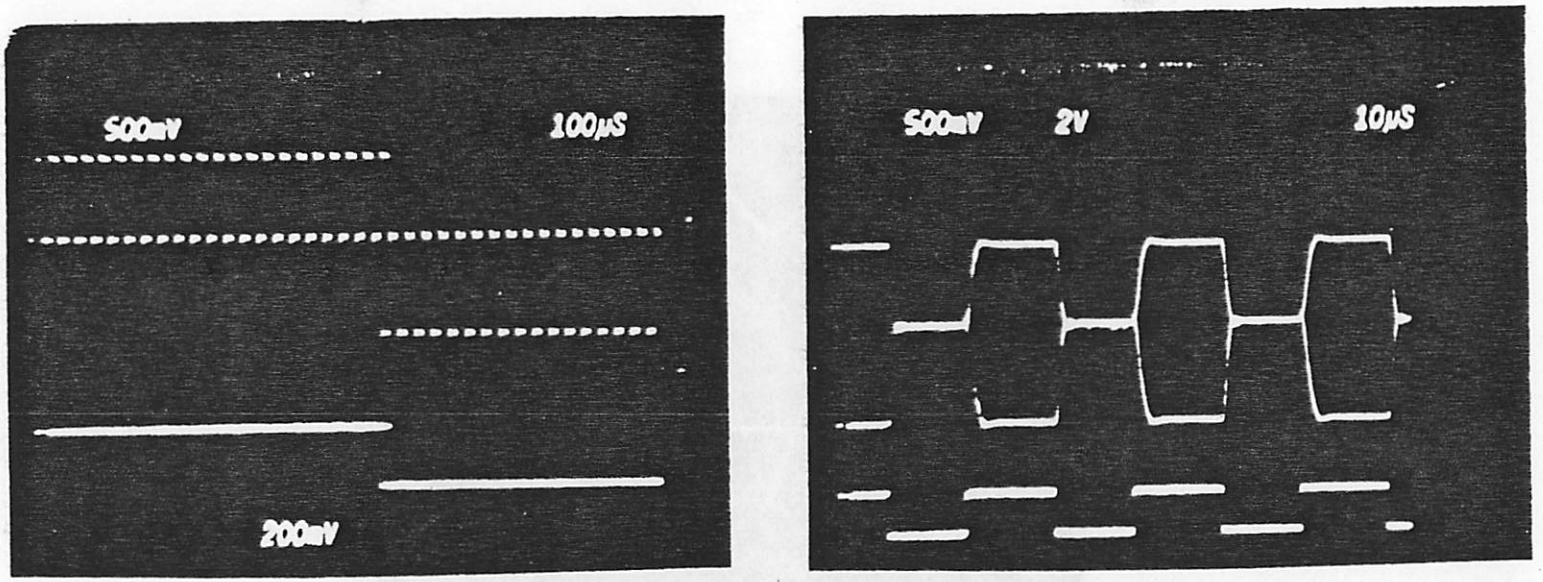


Fig.5.6 DCS Amplifier Output Waveform with Square Wave Input Signal

failed to pass the test mainly because the bonding wires popped off. As a consequence of this, only about ten good packaged parts were available for final detailed characterization.

The output waveforms of these circuits from a 1 kHz sinusoidal and triangular input signals are shown in Fig.5.4 and Fiq.5.5 respectively. The staircase-shaped waveform is the result of the sample and hold operation. Shown in Fiq.5.6 is the output waveform with a square wave input signal. The output is reset to its own offset value during the sample mode when clock 1 is high, and generates an amplified input sample during the hold mode when clock 2 goes high.

5.2 Input Offset Voltage

The edge variation between two matched components is around 0.1~0.2 um in a typical IC process [46]. Because relatively thick photo resist (AZ1350J ~ 1.3 um) was used during the IC fabrication in this project, an edge variation of about 0.15 um is expected. Gate oxide gradient across the whole 2-inch wafer was measured to be less than 1% of the oxide thickness. Thus, the oxide mismatch between two closly matched devices is negligible. Therefore, the mismatch between two matched switches for device size of 10u/10u can be calculated as follows:

The standard deviation of the width variation of two 10u long devices is

$$dW = 0.15u/\mathrm{sqrt}(10) \sim 0.05u$$

The standard deviation of the length variation of two 10u wide devices is

$$dL \sim 0.05u$$

Therefore, the standard deviation of the mismatch between two 10u/10u devices is estimated to be:

$$\text{mismatch} \sim 2.0*0.05u/10u \sim 1\%$$

In this experimental set up, the gate overdrive voltage was about 7 volts. Thus, the channel charge mismatch between the two input switches M1, M2 is estimated at about 0.003 pC, which should give an input offset voltage of about +- 0.3 mV.

The experimentally observed input offset voltage is shown in Fig.5.7 for five typical samples of the circuit as a function of source resistance. For small values of source resistance. the average value of the input offset voltage is 1 mV; this actually results from offset in the amplifier offset cnacellation switches M6. M7 and not from charge injection in the input switches.

In the single ended output circuit. one side of switch M6 is connected to the output of the operational amplifier which has some high output resistance during transient conditions. However, one side of switch M7 is always connected to ground. Therefore, switch M6 will always inject more channel charge into the DCS capacitor than M7 does. hence. causing a fixed offset voltage which is independent of the input signal source resistance. The spread of this offset is about 500 uV, which increases to about 1.0 mV at high values of source resistance because the percentage of the channel charge injected into the sampling capacitors increases. The +- 0.2 mV increase in the offset spread corresponds to the total amount of channel charge mismatch when all the channel charge flows back to the sampling capacitor. The observed offset voltage agrees well

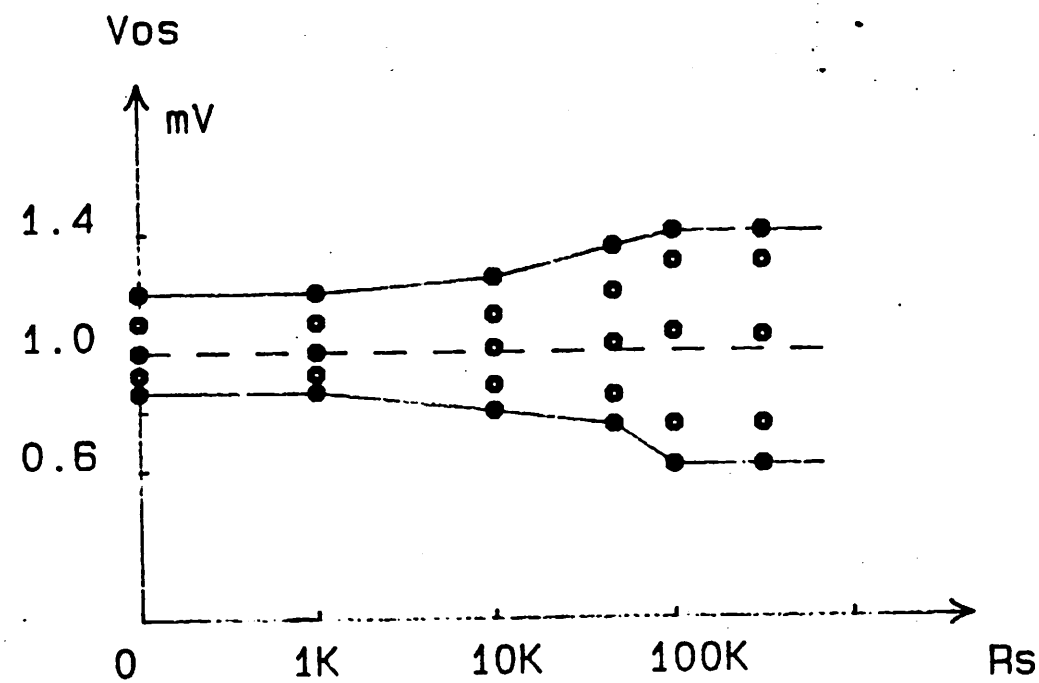


Fig.5.7 Experimentally Measured Input Referred Offset Voltage as a Function of Source Resistance

with the analysis. However, the observed increasing in the offset spread is a little less than the expected value due to the loading capacitance from the signal source, the bonding wires. ... etc. at the input nodes. The input capacitance loading has the effect of reducing the effective impedance level which results in less channel charge injection into the sampling capacitors.

5.3 Common Mode Rejection & Power Supply Rejection

The only switches which are exposed to common mode input signals are input switches M1 and M2. The typical mismatch of these switches is estimated to be about 1%; the common mode rejection ratio at DC is expected to be about 90 dB if all the switch channel charges are injected into the sampling capacitors.

Because the large loading capacitance of the input lead and signal source lowers the effective input impedance level. only a fraction of the switch channel charge will be injected into the sampling capacitors even if the source resistance is very large. From the +- 0.2 mV increase in offset spread shown in Fig.5.7, we can estimate that approximatly 60% of the input switches' channel charges are actually injected into the sampling capacitors. Thus, the common mode rejection ratio is about 95 dB at DC.

The measured common mode rejection ratio is shown in Fig.5.8 as a function of source resistance. The CMRR at low values of source resistance is about 120 dB. This is degraded to about 100 dB at higher values of source resistance as the amount of channel charge injected into the sampling capacitors increases.

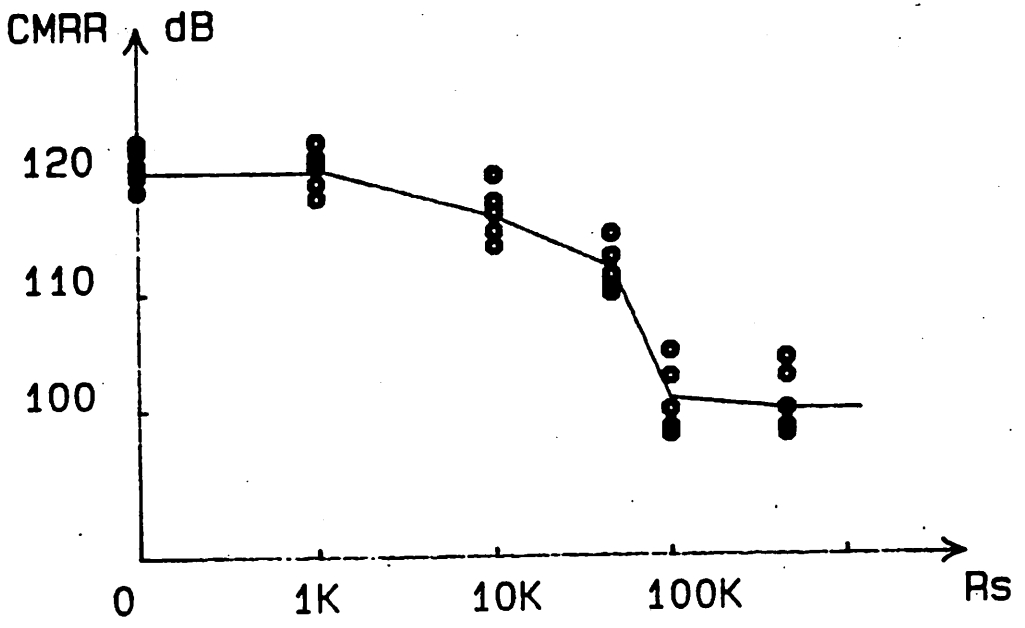


Fig.5.8 Experimentally Measured Common Mode Rejection Ratio as a Function of Source Resistance

The power supply rejection of these circuits should be considered in two categories. First, opamp power supply rejection and second, clock power supply rejection. The opamp power supply rejection ratio was measured to be very high because of the DCS operation which cancels any offset induced by power supply variations. The clock power supply rejection ratio is directly related to the input referred offset voltage caused by switch channel charge injection. Because of the unbalanced offset cancellation switches in the single ended circuit. the clock power supply rejection is only about 80 dB. For the fully balanced circuit, the clock power supply rejection is about 90 dB. The clock PSRR can be improved further if an on-chip regulator is used. The measured opamp PSRRs for both circuits are larger than 95 dB at low frequencies.

The very high values of CMRR and PSRR were measured using a HP spectrum analyzer. A large single frequency sinusoidal signal was applied to the common mode input and/or was in series with the power supply of the circuit. Thus. the circuit output will have a single frequency component with its amplitude inversely proportional to the CMRR or PSRR of the circuit.

5.4 Input Referred Noise Voltage & Offset Drift

Because the 1/f noise of the amplifier was reduced significantly by the use of double correlated sampling technique, the noise of the circuit is dominated by the KT/C noise of the input sampling capacitors. The thermal noise of the opamp is small due to the large gm used in the input devices. The KT/C noise of the input capacitors C1. C2 is about 30 uV, which agrees very well with the measured results.

The input offset voltage drift is also very low because the ambient temperature changes much slower than the clock frequency. thus an effective DCS can be achieved to cancel out the offset drift.

5.5 Closed Loop Voltage Gain Nonlinearity

Fig.5.9 illustrates the typical closed loop voltage gain nonlinearity observed for the instrumentation amplifier. The peak deviation from linear behavior is about 0.012% of full scale at +- 3 volts output swing. This nonlinearity results primarily from the nonlinear parasitic capacitance at the input of the operational amplifier. As it was verified through computer simulation in Section 4.3 that an operational amplifier with a higher open loop voltage gain will result in lower gain nonlinearity due to the fact that less charge was modulated by the nonlinear capacitances at opamp's summing nodes.

Table 1 shows the summary of the data measured at room temperature for power supply voltages of +- 7.5 volts. The closed loop voltage gain is 10 with an accuracy of 0.15%. which is caused primarily by the finite open loop voltage gain of the operational amplifiers.

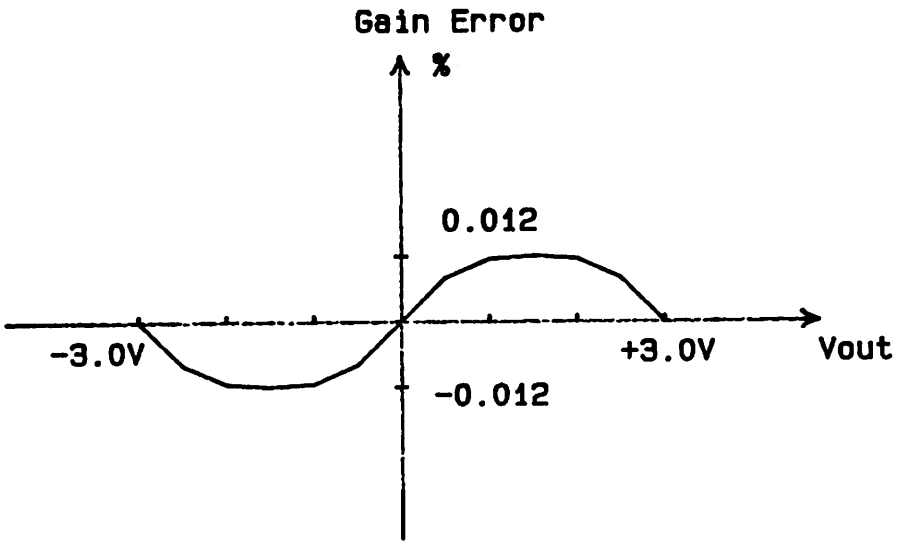


Fig.5.9 Experimentally Measured Closed Loop Voltage Gain Nonlinearity

Experimental Results, 25 °C., +7.5 & -7.5 volts		
Gain accuracy (G=10)		
average value		0.15 %
standard deviation		0.03 %
Input offset voltage		
average value		1.0 mV
standard deviation		0.5 mV
Gain linearity		0.01 %
Common mode rejection		
DC		120 dB
10K Hz		95 dB
Power supply rejection		
pre-amp stage	DC	> 95 dB
	1K Hz	> 95 dB
output stage	DC	95 dB
	1K Hz	95 dB
Input voltage range		+4.0, -8.0 volt
Output voltage range		
pre-amp stage		+0.5, -0.5 volt
output stage		+3.0, -3.0 volt
Acquisition time		~ 8 uS
Equivalent input noise (500K Hz BW)		~ 30 uV

Table 5.1 Summary of the Experimental Results

CHAPTER 6 - CONCLUSION

This thesis addressed the factors which limit the signal resolution in MOS circuits. Hypothetical models were proposed qualitatively for the understanding of the physical mechanisms of these factors. Through the understanding, we constructed a precision instrumentation amplifier sample-hold function using MOS technology. The measured data agrees well with the computer simulation. thus, consolidates our understanding in areas such as switch channel charge injection. thermal noise. flicker noise, component matching, design constraint, and technology limitation involved in MOS VLSI circuit design.

The performance levels achieved are generally somewhat inferior to recently reported bipolar instrumentation amplifiers [47]. The significance of the results achieved is that the compatibility with MOS technology allows a higher level of integration in the analog data acquisition interface with the digital interfacing and/or processing circuitry. without adding to the complexity of basic digital MOS technologies.

The experimental amplifier described in this thesis was implemented in NMOS technology, but it appears that a CMOS implementation could achieve significantly higher operating speed, better gain accuracy, lower gain nonlinearity, and lower power dissipation because of the higher available gain per stage and the resulting improvement in the CMOS operational amplifier's gain and bandwidth.

APPENDIX A - DOUBLE CORRELATED SAMPLING TECHNIQUE

Shown in Fig.A.1 is the block diagram of a linear system for implementing Double Correlated Sampling (DCS) technique [34]. s(t) represents the unwanted signal source (or noise), its signal power is to be reduced greatly by the use of DCS. p(t) is the sampling pulse train, h(t) is the impulse response of a zero hold circuit; p(t) and h(t) together form a zero order sample/hold function. The delay dt stands for any propagation or added delay in the signal path.

To examine the noise power reduction achieved by the DCS technique, the output power spectrum of y(t) is calculated [48] with input grounded. The sampling pulse train p(t) has a magnitude equals to unity and a sampling period of Ts. Thus, the output of the hold circuit is:

$$s_h(t) = s(nTs) \text{ convolves } h(t)$$

$$= \text{sum of } \{ s(nTs) * h(t-nTs) \} , \quad n \text{ is integer}$$

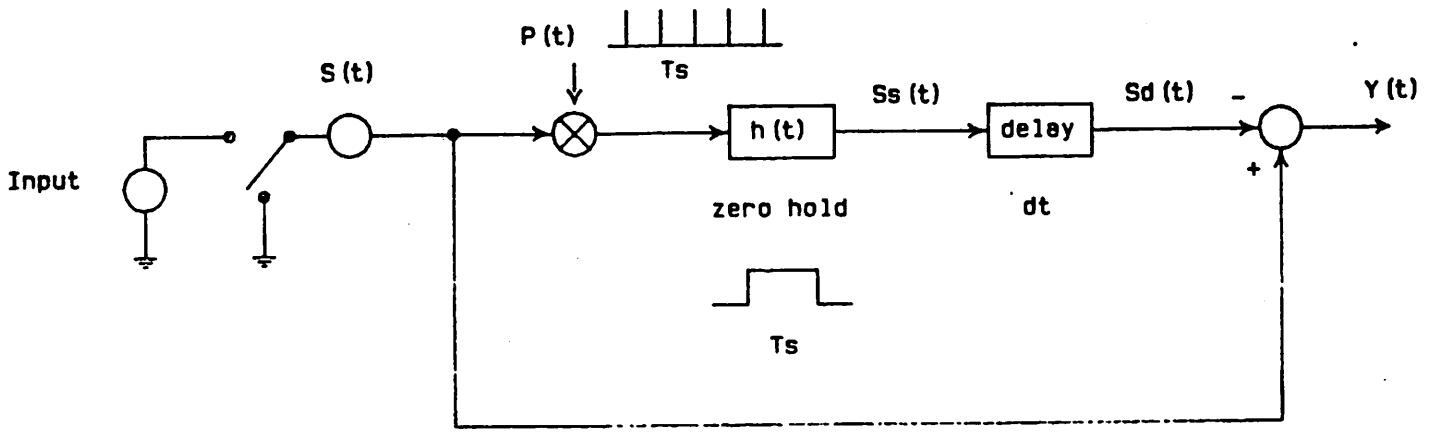


Fig.A.1 Double Correlated Sampling System Diagram

where

$$h(t) = 1 \qquad \text{for} \qquad Ts > t > 0$$

$$= 0 \qquad\qquad\quad \text{elsewhere}$$

The Fourier transform of the above equations are:

$$S_h(W) = \text{sum of } \{ H(W) * S(W-nWs)/ Ts \} , \quad n \text{ is integer}$$

where

$$H(W) = Ts \frac{Sin(WTs/2)}{WTs/2} e^{-jWTs/2}$$

and

$$Ws = 2*Phi/ Ts$$

After the added Ts/2 delay to the sample and hold circuit. the delayed output becomes:

$$s_d(t) = s_h(t-Ts/2)$$

and its Fourier transform is:

$$S_d(W) = S_h(W)\, e^{-jWTs/2}$$

The output of the DCS system y(t) is:

$$y(t) = s(t) - s_d(t)$$

thus,

$$Y(W) = S(W) - S_d(W)$$

$$= S(W) - \frac{1}{Ts}\, e^{-jWTs/2} * \text{sum of } \{ H(W) * S(W-nWs) \}$$

n: any integer

$$= S(W) * \left[1 - \frac{1}{Ts}\, H(W)\, e^{-jWTs/2} \right]$$

$$- \frac{1}{Ts}\, e^{-jWTs/2} * \text{sum of } \{ H(W) * S(W-nWs) \}$$

n: any integer but 0

If the output is bandlimited to the sampling frequency fs=1/Ts. the summation term in the above equation will drop out, thus,

$$Y(W) \sim S(W)*\left[\, 1 - \frac{1}{Ts} H(W)\, e^{-jWTs/2} \,\right]$$

$$Y(W) \sim S(W)*\left[\, 1 - \frac{1}{Ts} e^{-jWTs/2} * Ts * \frac{Sin(WTs/2)}{WTs/2} * e^{-jWTs/2} \,\right]$$

$$= S(W)*\left[\, 1 - Cos(WTs)*Sinc(WTs/2) + jSin(WTs)*Sinc(WTs/2) \,\right]$$

after some algebraic manipulations, the output power transfer function becomes:

$$|Y(W)|^2 / |S(W)|^2 = Y(W)*Y(W)^*$$

$$= \left[\, 1 + Sinc^2(WTs/2) - 2\, Cos(WTs) * Sinc(WTs/2) \,\right]$$

The power transfer function of the DCS system is plotted in Fig.A.2, it is obvious that the amount of noise reduction is most significant at low frequencies for wTs << 1. Fig.A.3 shows the output noise spectral density of the DCS system for the case that S(W) has an 1/f spectral characteristic.

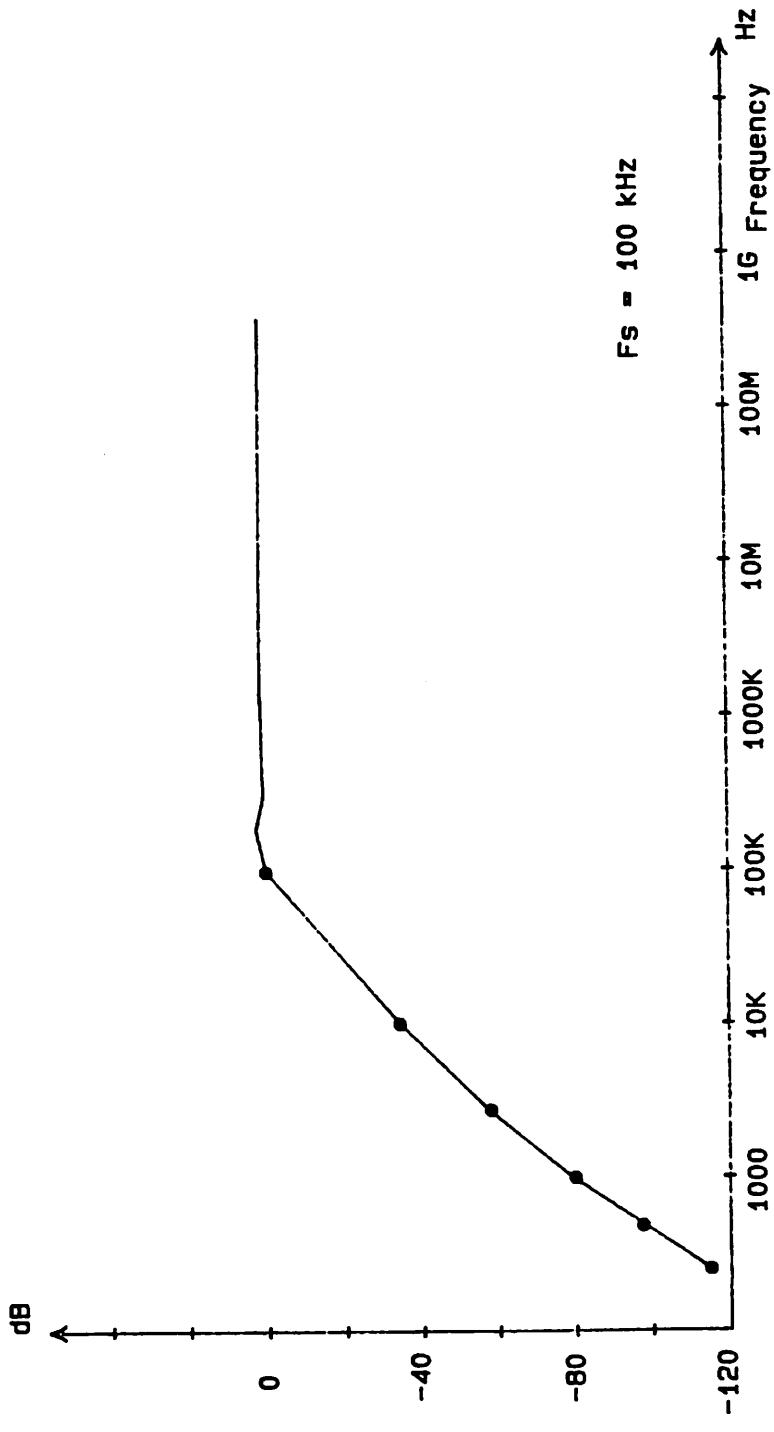


Fig.A.2 DCS System Power Transfer Function

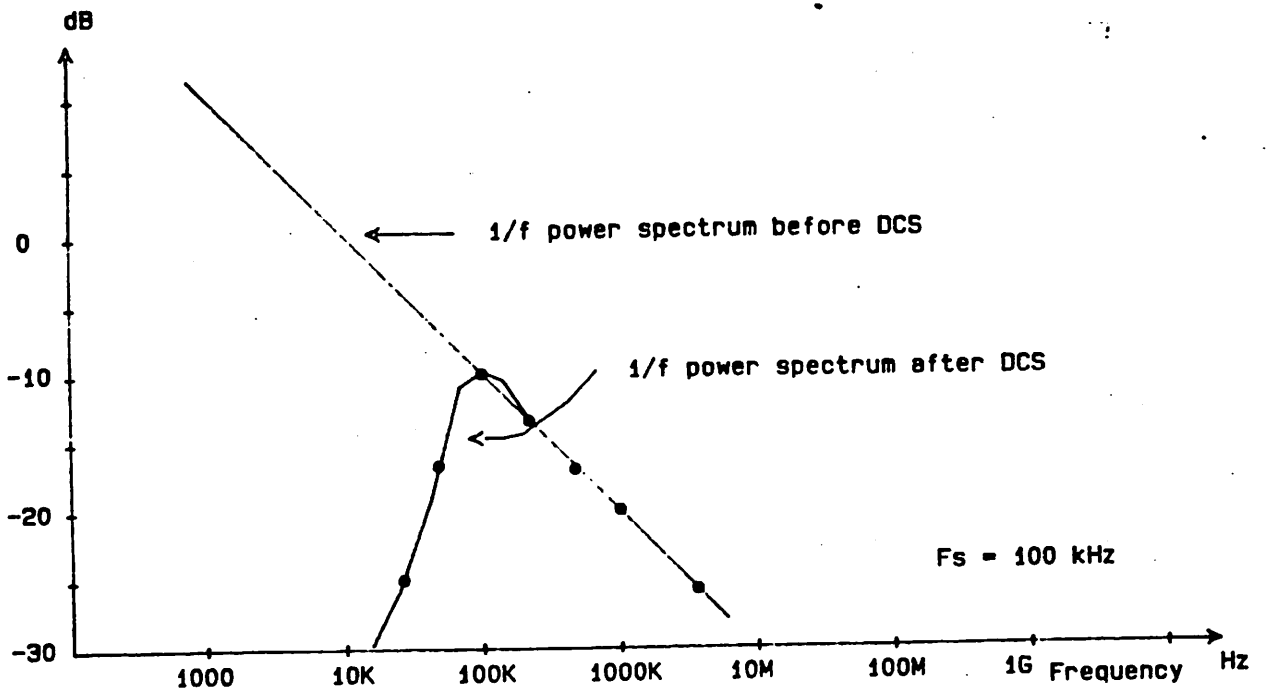


Fig.A.3 1/f Noise Reduction Using DCS Technique

APPENDIX B - FORTRAN PROGRAM FOR THE SIMULATION OF SWITCHED CAPACITOR INSTRUMENTATION AMPLIFIER

Fortran Program for S/C Instrumentation Amplifier

```
      WRITE(2,8)
8     FORMAT(' GAIN NON-LINEARITY, OPAMP GAIN NONLINEARITY')
      WRITE(2,11)
11    FORMAT(2X,'Vot.     GAIN NONLINEARITY IN %')
      Av0=200
      DO 651 J5=1.7
      WRITE(2,9) Av0
9     FORMAT(2X,'Av0='.1F15.2)
     C
19    FORMAT(1F3.0)
     C
      E1=0.047
      E2=-0.15
      E3=E1
      E4=0.24
     C
      C1=10.0
      C3=1.0
      CP1v0=4.0
      CP10=0.1
      CP3v0=0.0
      Vot=3.5
     C
      DO 650 N=1.40
     C
      CP30=0.67
      CPS=0.03
      Vbb=7.5
      Vphi=0.55
      Vk=Vbb+Vphi
      GAMMA=0.373
      Gain=C1/C3
     C
      C2=(1.0+E1/100.0)*C1
      C4=(1.0+E2/100.0)*C3
      CP2v0=(1.0+E3/100.0)*CP1v0
      CP20=(1.0+E3/100.0)*CP10
      CP4v0=(1.0+E4/100.0)*CP3v0
      CP40=(1.0+E4/100.0)*CP30
```

```
C
 Vcm=0.0
 Vdm=0.01
 GE=0.0
C
 DO 600 J1=1.2
C
 Vin=Vcm+Vdm
 Vol=Gain*Vin
C
 DO 555 K11=1.2
C
 Vo2=Vol/Vot
 vo2=abs(vo2)
 Vnn=(1.0+Vo2)/(1.0-Vo2)
 Vnn=SQRT(Vnn)
 Vil=(Vot/Av0)*ALOG(Vnn)
 Av=Vol/Vil
C
 Qc1=Vin*C1
 Qcp10=Vin*CP10
 Qcp1v=CP1v0*(SQRT(Vk+Vin)-SQRT(Vk))
 Qc2=Vcm*C2
 Qcp20=Vcm*CP20
 Ocp2v=CP2v0*(SQRT(Vk+Vcm)-SQRT(Vk))
C
 Q1=Oc1+Ocp10+Ocp1v+Oc2+Ocp20+Ocp2v
 Q2=-Qc1
 Q3=-Oc2
C
 T11=C1+C2+CP10+CP20+CPS
 T12=-(C1+C2)
 T13=-(C2/Av)
 T21=-C1
 T22=C1+C3+CP30
 T23=-C3
 T31=-C2
 T32=C2+C4+CP40
 T33=(C2+C4+CP40)/Av
C
 V11=Vcm+Vdm/2.0
 V22=Gain*Vdm/2.0
 V33=V22+Gain*Vdm/Av
C
```

```
      DO 500 I=1,5
     C
      Qk1=O1-(CP1v0+CP2v0+CPS*GAMMA)*(SQRT(Vk+V11)-SQRT(Vk))
      Qk2=Q2-CP3v0*(SQRT(Vk+V22)-SQRT(Vk))
      Qk3=O3-CP4v0*(SQRT(Vk+V33)-SQRT(Vk))
     C
      Z1=(T12*T21/T11)-T22
      Z2=(T13*T21/T11)-T23
      ZQ1=(Qk1*T21/T11)-Ok2
      Z3=(T32*T21/T31)-T22
      Z4=(T33*T21/T31)-T23
      ZQ2=(Qk3*T21/T31)-Qk2
      Y1=(Z2*Z3/Z1)-Z4
      Y2=(Z3*ZQ1/Z1)-ZQ2
      VO=Y2/Y1
      V2=(ZQ1-Z2*VO)/Z1
      V1=(Qk1-T12*V2-T13*VO)/T11
      V11=V1
      V22=V2
500   CONTINUE
     C
      Vol=VO
     C
555   CONTINUE
     C
      GA=VO/Vdm
      GE=(100.0*(GA-Gain)/Gain)-GE
     C
      Vdm=0.3
     C
600   CONTINUE
      WRITE(2,900) Vot,GE
      Vot=Vot+0.5
650   CONTINUE
      Av0=Av0*2.0
651   CONTINUE
     C
900   FORMAT(2X,2F15.6)
      STOP
      END
```

APPENDIX C - LOCOS POLYSILICON GATE NMOS IC PROCESS

This IC process [49] was developed with the following considerations:

* withstand 15 volt supply voltage
* very low leakage current for precision analog switched capacitor circuits applications
* shallow arsenic junction for low parasitic capacitance
* voltage independent linear capacitor structure
* local oxidation field oxide to increase circuit density
* CVD oxide (VAPOX) for reliable dielectric insulation between Al layer and poly layer
* metal over poly step coverage must be well controlled
* phosphorus plug rather than palladium silicide (PdSi) was used for much more reliable contact
* special test structures were designed to debug process
* process simulation program SUPREME [50] was used intermittently to verify the process profile

C.1 - MASK GENERATION

1. DIGITIZE IC LAYOUT

2. GENERATE PG TAPE

3. GYREX PATTERN GENERATOR

    scale factor 3.937
    generate 10X glass plate
    photo develop the glass plate
    visual inspection under microscope

4. SECOND REDUCTION WORKING MASK

    mounting the 10X plate on reticle frame
    step and repeat
    photo develop the working plate
    visual inspection

C.2 - IC FABRICATION PROCESS FLOW

1. STARTING MATERIAL

   boron doped p-type wafer
   25 ~ 50 ohm-cm resistivity
   <100> crystal orientation

2. INITIAL WAFER CLEANING

   visual inspection under strong light
   piranha (H_2SO_4 : H_2O_2 / 5:1) 10 min
   deionized water (DI) rinse, nitrogen N_2 blow dry

   HF:DI/1:10 dip 20 sec
   DI rinse and nitrogen blow dry

3. INITIAL OXIDATION ~ 1000 angstron

N_2	4.0cm	1000 deg C	push	3 min
O_2	6.5cm	1000 deg C	oxide	110 min
N_2	4.0cm	900 deg C	anneal	10 min
N_2	4.0cm	900 deg C	pull	3 min

4. NITRIDE DEPOSITION (LPCVD Si_3N_4 ~ 700 angstrons)

   wafer cleaned and very dry
   low pressure chemical vapor deposition furnace
   NH_4 :SiH_4 / 600 mT:100 mT 450 deg C, 40 min

5. MASK #1 ACTIVE AREA DEFINITION

HMDS vapor wafer surface treatment 5 min
nitrogen gas purge 10 min
AZ1350J positive photo resist PR, 8000 rpm 30 sec
prebake at 90 deg C 20min
projection alignment and exposure
AZ developer : DI / 1:1 60 sec
postbake at 110 deg C 30 min

6. NITRIDE ETCH

barrel type plasma reactor
descum, O_2 0.76 torr, 10 watt, 150 deg F, 5 min
nitride etch. SF_6 O_2 0.1 torr, 15 watt, 150 deg F.
~ 14 min. etch until pattern clears. ~ 20% overetch

7. FIELD IMPLANT

implant through initial oxide
use PR as implant mask
dose: Boron (BF), $1.40*10^{13}$ atoms/cm^2
implant energy: 110 keV, angle: 8 degree
strip off PR

8. LOCAL OXIDATION ~ 0.7 um

piranha clean
drive in furnace

O_2	6.5cm	1000 deg C	push	3 min
O_2	6.5cm	1000 deg C	drive in	20 min
O_2	3.0cm	900 deg C	wet oxide	280 min
N_2	4.0cm	900 deg C	anneal	15 min
N_2	4.0cm	900 deg C	pull	3 min

HF:DI/1:100 dip 90 sec

9. MASK #2 CAPACITOR BOTTOM PLATE DEFINITION

10. NITRIDE ETCH

barrel type plasma reactor
descum: O_2 0.76 torr, 10 watt, 150 deg F, 5 min
nitride etch: SF_6 O_2 0.1 torr, 15 watt, 150 deg F,
16 min. etch until pattern clears
HF dip off the remaining oxide

11. CAPACITOR BOTTOM PLATE IMPLANT

implant through ~ 50 angstron piranha oxide
PR as implant mask
dose: Arsenic (As), $1.0*10^{15}$ atoms/cm^2
implant energy: 120 keV, angle: 8 degree
strip off PR
plasma descum. O_2 0.76 torr, 80 watt, 20 min

12. IMPLANT ANNEAL AND CAPACITOR OXIDE GROWTH

O_2	6.5cm	900 deg C	push	3 min
O_2	6.5cm	900 deg C	oxide	15 min
N_2	4.0cm	900 deg C	anneal	20 min
O_2	6.5cm	1000 deg C	oxide	75 min
N_2	4.0cm	900 deg C	anneal	5 min
N_2	4.0cm	900 deg C	pull	3 min

13. NITRIDE REMOVAL

H_3PO_4 : H_2SO_4 / 95 : 5 at 165 deg C, ~ 40 min
etch until color stabilized

14. MASK #3 DEPLETION THRESHOLD IMPLANT DEFINITION

15. DEPLETION THRESHOLD VOLTAGE IMPLANT

implant through gate oxide
use PR as implant mask
dose: Phosphorus, $1.044*10^{12}$ atoms/cm^2
implant energy: 150 keV, angle: 8 degree
requires noise compensation for implant
strip off PR

16. ENHANCEMENT THRESHOLD VOLTAGE IMPLANT

implant through gate oxide
no implant mask required
dose: Boron (BF), $2.39*10^{11}$ atoms/cm^2
implant energy: 50 keV, angle: 8 degree
requires noise compensation for implant

17. POLYSILICON DEPOSITION ~ 0.45 um

plasma descum, O_2 0.76 torr, 60 watt, ~ 10 min

piranha clean, very dry
LPCVD furnace, 600 deg C, SiH_4 : 600 mT, 35 min

18. PHOSPHORUS PREDEPOSITION

O_2 :N_2 /2.5:5.0 cm	950 deg C	push	3 min
O_2 :N_2 :POCl/2.5:5.0:9.0 cm	950 deg C	pre-dep	15 min
O_2 :N_2 /2.5:5.0 cm	950 deg C	anneal	5 min
O_2 :N_2 /2.5:5.0 cm	950 deg C	pull	3 min

HF:DI/1:10 dip ~ 30 sec

19. MASK #4 POLYSILICON LAYER DEFINITION

20. POLYSILICON ETCH

barrel type plasma reactor
descum, O_2 0.76 torr, 10 watt, 150 deg F, 5 min
poly etch. SF_6 O_2 0.1 torr, 15 watt, 150 deg F,
4.5 min. etch until color change stabilized,
avoid overetch !!

21. SOURCE AND DRAIN N+ IMPLANT

HF dip off source/drain oxide
strip off PR
use poly and field oxide as implant mask
dose: Arsenic, $1.0*10^{16}$ atoms/cm^2
implant energy: 200 keV, angle: 8 degree
plasma descum, O_2 0.76 torr, 80 watt, ~ 20 min

22. IMPLANT ANNEALLING

N_2	4.0cm	900 deg C	push	3 min
N_2	4.0cm	900 deg C	anneal	40 min
N_2	4.0cm	900 deg C	pull	3 min

23. CVD OXIDE DEPOSITION ~ 1.0 um

SiH_4 :N_2 :P / 8.8cm:5.0cm:9.0cm, N_2 diluent: 5 cm
450 deg C, ~ 25 min

24. CVD OXIDE REFLOW AND SOURCE/DRAIN As DRIVE IN

O_2 :N_2 /2.5:5.0 cm	1000 deg C	push	3 min
O_2 :N_2 :POCl/2.5:5.0:9.0 cm	1000 deg C	pre-dep	20 min
N_2 : 5.0	1000 deg C	anneal	5 min
N_2 : 5.0	1000 deg C	pull	3 min

25. MASK #5 CONTACT DEFINITION

26. CONTACT ETCH

buffer HF (NH_4OH : HF / 5:1) ~ 6 min
use two step etch to avoid over etch
strip off PR

27. PHOSPHORUS PLUG AND GETTERING

wafer back side HF etch
piranha clean

O_2 :N_2 /2.5:5.0 cm	1000 deg C	push	3 min
O_2 :N_2 :POCl/2.5:5.0:9.0 cm	1000 deg C	pre-dep	20 min
N_2 : 5.0	1000 deg C	anneal	5 min
N_2 : 5.0	1000 deg C	pull	3 min

28. MASK #5 CONTACT HOLE DIP

HF:DI/1:10 dip ~ 45 sec
strip off PR

29. ALUMINUM DEPOSITION ~ 0.8 um

piranha clean
HF:DI/1:10 dip ~ 10 sec
DI rinse, nitrogen blow very dry
Al deposition using Veeco-Roger vacuum system

30. MASK #6 METALLIZATION PATTERN DEFINITION

31. ALUMINUM ETCH

Al type A etchant. 27 deg C, ~ 6 min
DI rinse thoroughly
inspection
strip off PR

32. SINTERING

forming gas H_2:N_2 /1:9 15cm. 350 deg C. 20 min

33. BACKSIDE PREPARATION

use Q-tip HF dip off backside oxide

34. WAFER PROBING

35. PACKAGING

wafer scribing using diamond scriber
acetone cleaning
chip mount on package
wire bonding

36. DONE !!

C.3 - DEVICE CHARACTERISTICS

enhancement device Vt	:	~ 0.6 V
depletion device (buried channel) Vtd	:	~ 3.7 V
field threshold voltage	:	~ 18 V
P-N junction breakdown voltage	:	~ 23 V
punch through voltage (for L ~ 6 um)	:	~ 20 V
source & drain N+ resistivity	:	~ 20 ohm/sq
N+ doped poly resistivity	:	~ 15 ohm/sq
capacitor bottom plate resistivity	:	~ 50 ohm/sq
contact resistivity (5u X 7u)	:	< 10 ohm
Al resistivity	:	~ .02 ohm/sq
minimum contact size resolved	:	3 um X 3 um
minimum device channel length resolved	:	3 um
functional circuit yield at wafer stage	:	> 85 %

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