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NEGATIVE RESISTANCE DEVICES: PART II

by

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Abstract

As a sequel to [1], this paper presents new analytical and topological guidelines for synthesizing negative-resistance devices. Among other things, these guidelines can be used to tune the devices by varying the magnitude and dynamic range of the negative (small-signal) resistance.

Necessary and sufficient conditions are given for a circuit containing only one bipolar transistor and linear reciprocal passive two-ports (e.g., ideal transformers) to exhibit a negative resistance. In the special case where the circuit contains only one ideal transformer, one transistor, and linear positive 2-terminal resistors, an equivalent topological criterion which can be checked by inspection is given.

Finally, three canonical negative-resistance one-ports containing two identical bipolar transistors, linear positive 2-terminal resistors, and batteries are synthesized to exhibit an odd-symmetric (hence active) voltage-controlled or current-controlled v-i curve.

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1. Introduction

This paper is a sequel to a recent publication [1] which gives a selected catalog of transistor negative-resistance devices made of two bipolar transistors and linear positive 2-terminal resistors. Since no internal power supply is required, all of these negative resistance devices are passive one-ports in the sense that their v-i curves are restricted to the first and third quadrants only. Hence the term negative resistance here is used to mean that a portion of the v-i curve has a negative slope; i.e., it has a negative small-signal resistance.

The algorithm used in [1] for synthesizing these circuits determines first a subclass of two-transistor circuits as potential candidates and uses a computer simulation program (SPICE) to identify those candidates which actually exhibit a negative resistance over some portion of their v-i curves. Although hundreds of new negative-resistance devices have been successfully synthesized using this algorithm, an excessive amount of computer time has been used to eliminate an even larger number of circuit candidates which turn out to be incapable of exhibiting a negative resistance.

One of the objectives of this paper is to develop analytical and topological guidelines (compared to the above cited trial and error elimination approach) for eliminating candidates which are unlikely to have a negative resistance. The term "guideline" is used pointedly here to suggest that an extremely small subclass of the eliminated candidates may in fact yield a negative resistance under some very stringent conditions--i.e., the resistance values and the transistor parameters must satisfy a set of inequalities whose feasible solution region in the parameter space is extremely small. While it is possible to derive some exact analytical elimination criteria, they inevitably involve solving a complicated nonlinear programming problem which would require more computer time than the above cited simulation approach. Consequently, from the practical synthesis point of view, we have found it much more useful to derive a number of guidelines in Section 2. Rather than tuning the resistance parameters by a trial and error approach, the guidelines in Section 2 will show which resistances must be increased and which must be decreased in order to enhance the chances of obtaining a negative resistance in each circuit candidate. These guidelines can also be used to alter the shape of the v-i characteristics for optimum performance.

The analysis developed in Section 2 allows us to shed much light on the three conjectures posed in [1]. A partial though not complete resolution of

these conjectures is given in Section 3.

In Section 4, we show that it is possible to obtain a negative resistance using only one bipolar transistor provided we are allowed to use a linear reciprocal passive 2-port resistor (e.g., an ideal transformer). Necessary and sufficient conditions for such a circuit to possess a unique d.c. solution is given. In the special case when the circuit contains only one transistor, one ideal transformer, and linear positive 2-terminal resistors, an explicit topological criterion is given which allows one to synthesize such negative resistance devices by inspection.

In the final Section 5, we investigate a rather specialized but important class of negative resistance devices; namely, those characterized by an odd-symmetric voltage-controlled or current-controlled v-i curve. Such devices are widely used as negative-resistance oscillators (e.g., the classic Van der Pol oscillator is a case in point [2]). Since an odd-symmetric non-monotonic v-i curve which exhibits a negative-resistance at the origin of the v-i plane must necessarily contain points in the second and fourth quadrants in addition to the first and third quadrants, such negative-resistance devices are active and hence must have at least one internal power supply. Using the guidelines developed in Sections 2 and 3, one odd-symmetric voltage-controlled and two odd-symmetric current-controlled negative resistance devices (using two bipolar transistors, linear positive 2-terminal resistors, and batteries) are systematically synthesized in Section 5. The first circuit turns out to be identical to that proposed by Rosenthal [3], possibly derived via an intuitive or ad hoc approach.†

Using a systematic though exhaustive analysis, it is possible to show that Rosenthal's circuit is the only possible odd-symmetric voltage-controlled negative-resistance device (using two bipolar transistors), modulo simple equivalent circuit transformations. In contrast, the two odd-symmetric current-controlled negative-resistance devices derived in Section 5 are new and distinct (not modulo an equivalent circuit transformation). Since all odd-symmetric negative-resistance devices containing two identical bipolar transistors can be transformed into one of the circuits in Section 5, these three circuits are essentially the only (modulo equivalent circuit transformations) possible two-transistor negative-resistance devices that exhibit an odd-symmetric negative-resistance v-i curve.

†Rosenthal gave no indication on how this circuit was conceived.

2. Parameter Tuning Guidelines for Two-Transistor Negative-Resistance Devices

Lemma A.4 (Appendix B) asserts that the presence of a feedback structure is a necessary condition for the existence of multiple d.c. solutions for transistor-resistor circuits, and hence it is also necessary for generating a driving-point v-i curve with a negative-resistance region. Since the feedback structure requires at least two transistors, the one-port N to be studied in this section, and in Section 3, is assumed to contain two transistors, and possibly some linear positive 2-terminal resistors, but no independent sources.

A. Circuit Properties of Two-Transistor One-Ports

Through computer simulation, numerous two-transistor negative-resistance devices have been generated and a selected subset has appeared in [1]. Here, we present some properties of such devices which will be used in the next subsection to derive some parameter tuning guidelines for shaping the associated v-i curves. Much of these properties depend on previous results due to Willson and his students which we summarized in Appendix B for ease of reference.

From Lemma A.6 in Appendix B, the driving-point v-i curves of two-transistor one-ports N can be classified into four types as depicted in Fig. 1; namely,

(1) Monotone-Increasing characteristic
(2) Multivalued characteristic
(3) Type-S characteristic
(4) Type-N characteristic

The following lemma follows directly from Lemma A.4 in Appendix B:

Lemma 1. In order for a two-transistor one-port N to exhibit a
(1) Multivalued
(2) Type-S
(3) Type-N
v-i curve respectively, it is necessary for N to possess a feedback structure when the driving port is
(1) short-circuited and open-circuited
(2) short-circuited
(3) open-circuited
respectively.

The small-signal conductance G of the one-port N is completely determined by Eq. (A.12) in Appendix B, where the matrices $\underset{\sim}{P}_0$, $\underset{\sim}{Q}_0$, $\underset{\sim}{P}_s$, $\underset{\sim}{Q}_s$ are determined by the circuit structure and resistor parameters, $\underset{\sim}{I}$ is determined by the transistor parameters, and $\underset{\sim}{D}$ is determined by the operating point where G is to be

evaluated. These matrices themselves are related to each other in a very complicated way.

Let $(\underset{\sim}{P}_s,\underset{\sim}{Q}_s)$ (resp.; $(\underset{\sim}{P}_0,\underset{\sim}{Q}_0)$) denote the source-free (i.e., set all independent sources to zero) linear four-port in Fig. A.3 which is characterized by the equation $\underset{\sim}{P}_s\underset{\sim}{v} = \underset{\sim}{Q}_s\underset{\sim}{i}$ (resp.; $\underset{\sim}{P}_0\underset{\sim}{v} = \underset{\sim}{Q}_0\underset{\sim}{i}$) when the driving port of N in Fig. A.4(a) is short-circuited (resp.; open-circuited). For simplicity, we will use the generic symbol $(\underset{\sim}{P},\underset{\sim}{Q})$ to denote either $(\underset{\sim}{P}_s,\underset{\sim}{Q}_s)$ or $(\underset{\sim}{P}_0,\underset{\sim}{Q}_0)$.

Since $(\underset{\sim}{P},\underset{\sim}{Q})$ is a <u>passive pair</u> [4], $\det(\underset{\sim}{Q}\underset{\sim}{D}+\underset{\sim}{P})$ will have the same sign for any diagonal matrix $\underset{\sim}{D}$ with <u>positive</u> elements, henceforth denoted by $\underset{\sim}{D} > 0$. Also if there exists no feedback structure after the driving port of N is short-circuited or open-circuited, then by Lemma A.2 $(\underset{\sim}{Q}\underset{\sim}{T},\underset{\sim}{P})$ is a <u>W_0-pair</u> [5] which, from Definition A.3 (Appendix B), implies $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) \neq 0$ for any $\underset{\sim}{D} > 0$. By continuity, $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P})$ has the same sign for any $\underset{\sim}{D} > 0$. Since $\underset{\sim}{T}$ is a diagonally-dominant matrix with a positive determinant, it follows that $\det(\underset{\sim}{Q}\underset{\sim}{D}+\underset{\sim}{P})\cdot\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) > 0$ for any $\underset{\sim}{D} > 0$. Hereafter we assume $\underset{\sim}{P}$ and $\underset{\sim}{Q}$ are chosen such that $\det(\underset{\sim}{Q}\underset{\sim}{D}+\underset{\sim}{P}) > 0$ for any $\underset{\sim}{D} > 0$ if $(\underset{\sim}{P},\underset{\sim}{Q})$ is a passive pair and $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) > 0$ for any $\underset{\sim}{D} > 0$ if $(\underset{\sim}{Q}\underset{\sim}{T},\underset{\sim}{P})$ is a W_0-pair.

Because $G(0)$ in Fig. A.4(c) is the small-signal conductance of a linear <u>passive</u> resistive one-port, it follows that $G(0) > 0$ (excluding the degenerate case $G(0) = 0$). Moreover, $\det(\underset{\sim}{Q}_0\underset{\sim}{D}+\underset{\sim}{P}_0) > 0$ and $\det(\underset{\sim}{Q}_s\underset{\sim}{D}+\underset{\sim}{P}_s) > 0$ for any $\underset{\sim}{D} > 0$ because $(\underset{\sim}{P}_s,\underset{\sim}{Q}_s)$ and $(\underset{\sim}{P}_0,\underset{\sim}{Q}_0)$ are passive pairs. Hence we can rewrite Eq. (A.12) in the form

$$G = K\cdot\det(\underset{\sim}{Q}_0\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0)/\det(\underset{\sim}{Q}_s\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s) \tag{1}$$

where

$$K = G(0)\cdot\det(\underset{\sim}{Q}_s\underset{\sim}{D}+\underset{\sim}{P}_s)/\det(\underset{\sim}{Q}_0\underset{\sim}{D}+\underset{\sim}{P}_0) \tag{2}$$

and $K > 0$.

<u>Theorem 1</u>. The driving-point v-i curve of the one-port N is
(1) Monotone-Increasing
(2) Multivalued
(3) Type-S
(4) Type-N
if and only if, the following respective criteria hold:
(1) $\det(\underset{\sim}{Q}_0\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0) \geq 0$ and $\det(\underset{\sim}{Q}_s\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s) \geq 0$ for any $\underset{\sim}{D} \in \mathcal{D}$.
(2) $\det(\underset{\sim}{Q}_0\underset{\sim}{T}\underset{\sim}{D}_0+\underset{\sim}{P}_0) < 0$, $\det(\underset{\sim}{Q}_s\underset{\sim}{T}\underset{\sim}{D}_s+\underset{\sim}{P}_s) < 0$ for some $\underset{\sim}{D}_0 \in \mathcal{D}_0$, $\underset{\sim}{D}_s \in \mathcal{D}_s$ and

$\mathcal{D}_0 \cap \mathcal{D}_s \neq \phi$, $\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}\underset{\sim}{D}_0'+\underset{\sim}{P}_0) \geq 0$, and $\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}\underset{\sim}{D}_s'+\underset{\sim}{P}_s) \geq 0$ for any $\underset{\sim}{D}_0' \in \mathcal{D} - \mathcal{D}_0$ and $\underset{\sim}{D}_s' \in \mathcal{D} - \mathcal{D}_s$.

(3) $\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0) \geq 0$ for any $\underset{\sim}{D} \in \mathcal{D}$, $\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}\underset{\sim}{D}_s+\underset{\sim}{P}_s) < 0$ for some $\underset{\sim}{D}_s \in \mathcal{D}_s$, and $\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}\underset{\sim}{D}_s'+\underset{\sim}{P}_s) \geq 0$ for any $\underset{\sim}{D}_s' \in \mathcal{D} - \mathcal{D}_s$.

(4) $\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s) \geq 0$ for any $\underset{\sim}{D} \in \mathcal{D}$, $\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}\underset{\sim}{D}_0+\underset{\sim}{P}_0) < 0$ for some $\underset{\sim}{D}_0 \in \mathcal{D}_0$, and $\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}\underset{\sim}{D}_0'+\underset{\sim}{P}_0) \geq 0$ for any $\underset{\sim}{D}_0' \in \mathcal{D} - \mathcal{D}_0$.

where $\mathcal{D} = \{\underset{\sim}{D} | \underset{\sim}{D}$ is a 4 x 4 positive diagonal matrix defined in Eqs. (A.13) and (A.14) associated with all possible operating points of $N\}$ and $\mathcal{D}_s$ (resp.; $\mathcal{D}_0$) is a proper connected subset of $\mathcal{D}$ such that the v-i curve in (3) (resp.; (4)) possesses a negative slope for any $\underset{\sim}{D}_s \in \mathcal{D}_s$ (resp.; $\underset{\sim}{D}_0 \in \mathcal{D}_0$).

Proof: The proof follows directly from Fig. 1 and Eqs. (1) and (2). □

Example 1

The two-transistor one-port in Fig. 2(a) can be shown to exhibit a type-S v-i characteristic and has a d.c. solution located in the negative resistance region; namely,

$$v_1 = 0.629\,V \quad v_2 = 0.53\,V \quad v_3 = 0.687\,V \quad v_4 = 0.53\,V$$

with i = 3.5 mA and v = 0.786 V.

When port X-Y is short-circuited (resp.; open-circuited), the associated four-port in Fig. 2(c) is described by $\underset{\sim}{P}_s\underset{\sim}{v} = \underset{\sim}{Q}_s\underset{\sim}{i}$ (resp.; $\underset{\sim}{P}_0\underset{\sim}{v} = \underset{\sim}{Q}_0\underset{\sim}{i}$) where

$$\underset{\sim}{P}_s = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & -1 & 1 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}, \quad \underset{\sim}{Q}_s = \begin{bmatrix} R_1 & 0 & -R_1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & R_2 & R_2 & R_2 \end{bmatrix},$$

$$\underset{\sim}{P}_0 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}, \quad \underset{\sim}{Q}_0 = \begin{bmatrix} R_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & R_2 & 0 & R_2 \end{bmatrix}.$$

Assuming $R_1 = 200\Omega$, $R_2 = 2k\Omega$, $D = \text{diag.}(d_1,d_2,d_3,d_4)$ where $d_k = f'(v_k)$, and $f(v_k) = I_s(e^{v_k/V_T}-1)$ (assume $I_s = 10^{-14}$A, $V_T = 26$ mV, $\alpha_f = 0.98$, $\alpha_r = 0.5$), we calculated $d_1 = 0.0126$, $d_2 = 5.48\times 10^{-4}$, $d_3 = 0.1173$, $d_4 = 5.48\times 10^{-4}$, $\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0) = 1.25 > 0$ and $\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s) = -491 < 0$ as predicted by (3) of Theorem 1. □

We now introduce a topological structure associated with the feedback structure which plays an important role in determining the shape of the v-i characteristics.

Definition 1. A 2-terminal element is said to be in series (resp.; in parallel) with the feedback structure iff the feedback structure is destroyed when this element is open-circuited (resp.; short-circuited).

By Theorem 1, it is required that $\det(\underset{\sim}{Q}_0\underset{\sim}{\sim}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0) \geq 0$ (resp.; $\det(\underset{\sim}{Q}_s\underset{\sim}{\sim}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s) \geq 0$) for any $\underset{\sim}{D} \in \mathcal{D}$ in order to generate a type-S (resp.; type -N) v-i curve. Since $\det(\underset{\sim}{Q}_0\underset{\sim}{\sim}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0) > 0$ (resp.; $\det(Q_s T D+P_s) > 0$) for any $\underset{\sim}{D} > 0$ if the feedback structure is destroyed when the driving port is open-circuited (resp.; short-circuited), it follows that if the driving port is in series (resp.; in parallel) with the feedback structure in a one-port N, then it is guaranteed that $\det(\underset{\sim}{Q}_0\underset{\sim}{\sim}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0) > 0$ (resp.; $\det(\underset{\sim}{Q}_s\underset{\sim}{\sim}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s) > 0$) for any $\underset{\sim}{D} > 0$. Observe that the converse is not true because even if the feedback structure is not destroyed, it is still possible that $\det(\underset{\sim}{Q}\underset{\sim}{\sim}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) \geq 0$ for any $\underset{\sim}{D} \in \mathcal{D}$ since $\mathcal{D}$ is only a proper subset of $\{\underset{\sim}{D} | \underset{\sim}{D}$ is a 4×4 positive diagonal matrix$\}$. Hence it is not necessary that the driving port be in series (resp.; in parallel) with the feedback structure in order to generate a type-S (resp.; type-N) v-i curve. However, from the practical design point of view, it is convenient to exclude the possibility that $\det(\underset{\sim}{Q}_0\underset{\sim}{\sim}\underset{\sim}{T}\underset{\sim}{D}_0+\underset{\sim}{P}_0) < 0$ (resp.; $\det(\underset{\sim}{Q}_s\underset{\sim}{\sim}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s) < 0$) for some $\underset{\sim}{D}_0 > 0$ (resp.; $\underset{\sim}{D}_s > 0$).

Therefore, to generate a type-S (resp.; type-N) v-i curve, we will restrict our attention in this paper to the class of one-ports which will lose its feedback structure when the driving port is open-circuited (resp.; short-circuited).

Observe that if the inherent source resistance is included in the driving source for a one-port which exhibits a type-S (resp.; type-N) v-i curve, then when the driving port is open-circuited (resp.; short-circuited), the feedback structure is retained after short-circuiting (resp.; open-circuiting) the source resistance as shown in Fig. 3. This observation may at first sight suggest that our restriction above is somewhat severe. However it has been shown in [1], and will be further justified below, that adding a resistor $R > 0$ in series or in parallel with the driving port may destroy the negative resistance by giving rise to either a monotone-increasing or a multivalued v-i curve. Hence we must always avoid connecting a resistor in series or in parallel with the driving port; otherwise we only diminish the possibility for

obtaining a negative-resistance region in the v-i curve. Hereafter we assume no resistor is connected in series or in parallel with the driving port. Another circuit which is excluded by the above restriction is given by the following example.

Example 2

The one-port in Fig. 4(a) has a type-S v-i characteristic as shown in Fig. 4(b). When the driving port is short-circuited, there exists a feedback structure obtained by short-circuiting R2 and open-circuiting R1 and R3 as shown in Fig. 4(c). But when the driving port is open-circuited, there exists another feedback structure obtained by short-circuiting R1 and R3 and open-circuiting R2 as shown in Fig. 4(d). □

Note, however, that the feedback structure in Fig. 4(d) is different from that in Fig. 4(c) which has been destroyed by open-circuiting the driving port. In order not to exclude this class of circuits from our above restricted class, let us relax this restriction as follows:

Assumption 1. In order to generate a type-S (resp.; type-N) v-i curve using a two-transistor one-port N every feedback structure obtained by short-circuiting (resp.; open-circuiting) the driving port should be destroyed when the driving port is open-circuited (resp.; short-circuited).

Even with this modification, some counterexamples to Assumption 1 exist as demonstrated by the following example:

Example 3

Figure 5(a) exhibits a type-N v-i curve as shown in Fig. 5(b). Observe that a feedback structure still exists when the driving port is short-circuited as shown in Fig. 5(c). □

Despite the existence of such counterexamples to Assumption 1, our extensive simulation results seem to support Assumption 1 in most cases. Also if we modify Fig. 5(a) by short-circuiting R4, then a type-N v-i curve still exists but the feedback structure in this case is destroyed when the driving port is short-circuited, as shown in Fig. 5(d). Hence Assumption 1 entails very little loss of generality.

It follows from Assumption 1 and Theorem 1 that the inequality $\det(\underset{\sim}{Q}_S \underset{\sim}{T} \underset{\sim}{D}_S + \underset{\sim}{P}_S) < 0$ (resp.; $\det(\underset{\sim}{Q}_0 \underset{\sim}{T} \underset{\sim}{D}_0 + \underset{\sim}{P}_0) < 0$) for some $\underset{\sim}{D}_S \in \mathcal{D}_S$ (resp.; $\underset{\sim}{D}_0 \in \mathcal{D}_0$) is sufficient to generate a type-S (resp.; type-N) v-i curve. Let us now discuss in detail the conditions on the circuit topology or element parameters

such that this inequality is satisfied.

Following the derivation in [3], we directly expand the determinant $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P})$ to obtain

$$\begin{aligned}\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) = {} & c^{1234}d_1d_2d_3d_4 + c^{123}d_1d_2d_3 + c^{124}d_1d_2d_4 \\ & + c^{234}d_2d_3d_4 + c^{134}d_1d_3d_4 + c^{12}d_1d_2 + c^{13}d_1d_3 \\ & + c^{14}d_1d_4 + c^{23}d_2d_3 + c^{24}d_2d_4 + c^{34}d_3d_4 \\ & + c^{1}d_1 + c^{2}d_2 + c^{3}d_3 + c^{4}d_4 + c^{0} \end{aligned} \tag{3}$$

where $\underset{\sim}{D} = \text{diag.}(d_1,d_2,d_3,d_4)$ and each c^σ denotes the determinant of a matrix $\underset{\sim}{M}$ in $C(\underset{\sim}{Q}\underset{\sim}{T},\underset{\sim}{P})$ [5], where M is formed by the columns of $\underset{\sim}{Q}\underset{\sim}{T}$ (corresponding to the indices in superscirpt σ) and $\underset{\sim}{P}$ (corresponding to the remaining columns). For example, $c^{13} = \det \underset{\sim}{M}$ where the 1st and 3rd columns of $\underset{\sim}{M}$ are taken from the 1st and 3rd columns of $\underset{\sim}{Q}\underset{\sim}{T}$, and the 2nd and 4th columns of $\underset{\sim}{M}$ are taken from the 2nd and 4th columns of $\underset{\sim}{P}$.

By Definition A.3 and Lemma A.2 in Appendix B, $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) > 0$ for any $\underset{\sim}{D} > 0$ if and only if N contains no feedback structure. Hence $c^\sigma \geq 0$ for any σ if there exists no feedback structure. On the other hand if there exists a feedback structure, then $(\underset{\sim}{Q}\underset{\sim}{T},\underset{\sim}{P})$ is not a W_0-pair and there exists some $\hat{\underset{\sim}{D}} > 0$ such that $\det(\underset{\sim}{Q}\underset{\sim}{T}\hat{\underset{\sim}{D}}+\underset{\sim}{P}) < 0$. Since $\hat{d}_i > 0$ for each i, there must exist at least one $c^\sigma < 0$ in the expansion of $\det(\underset{\sim}{Q}\underset{\sim}{T}\hat{\underset{\sim}{D}}+\underset{\sim}{P})$.

Consider the feedback structure shown in Fig. A.2. Throughout this paper, unless otherwise stated, the voltage v_i, i = 1, 2, 3, 4, denotes a transistor junction voltage, and $v_i > 0$ if and only if the corresponding junction is forward-biased. It was shown in [3] that one and only one coefficient of c^σ's is negative when the feedback structure is present, and this negative coefficient is related to the feedback structure as follows: $c^\sigma \triangleq c^{ij} < 0$ iff there exists an (i,j)-feedback structure [3], i.e., v_i, v_j are the bottom junction voltages in the feedback structure. In the case of Fig. A.2, $c^{13} < 0$.

Since c^{13} is only one of the sixteen coefficients in Eq. (3), the existence of a feedback structure is not sufficient to guarantee $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) < 0$ for any $\underset{\sim}{D} > 0$. Only those positive diagonal matrices $\underset{\sim}{D} > 0$ with d_1, d_3 much larger than d_2, d_4 could lead to $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) < 0$ because in this case $c^{13}d_1d_3$ will dominate all the other terms in Eq. (3).

If follows from this observation that in order to generate a negative-

resistance v-i curve using a two-transistor one-port N the presence of a feedback structure is only one necessary condition which involves circuit topology. In addition, we must require the circuit element parameters to satisfy two other necessary conditions:

(1) Topological Condition: $c^{13} < 0$ with $|c^{13}|$ as large as possible (assume a (1,3)-feedback structure).

(2) Bias Condition: Both transistors are biased in the forward active region (Defined in Definition A.1 in Appendix A) such that d_1 and d_3 are as large as possible; and d_2 and d_4 are as small as possible; or equivalently, $v_1 >> v_2$, $v_3 >> v_4$; and $v_1 > 0$, $v_3 > 0$.

Remark: Hereafter we say $v_1 >> v_2$ and $v_3 >> v_4$ iff $e^{v_1/v_T} >> e^{v_2/v_T}$ and $e^{v_3/v_T} >> e^{v_4/v_T}$.

Both topological and bias conditions are determined by the circuit structure and element parameters. Our design criterion for generating a negative resistance v-i curve is to find a circuit structure and a set of element parameters such that both conditions are satisfied. If both conditions tend to contradict each other, then we must choose a trade-off between them such that $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P})$ becomes negative for some $\underset{\sim}{D} > 0$.

Since each coefficient c^{σ} in Eq. (3) is nonnegative when no feedback structure is present, we may conjecture that c^{13} tends to become positive as the feedback structure tends to be destroyed. This is justified by the following theorem.

Theorem 2. Consider a two-transistor one-port with the feedback structure shown in Fig. 6(a). If a new resistor is added to Fig. 6(a) either (1) by soldering-iron entry in parallel with the feedback structure as shown in Fig. 6(b), or (2) by plier-type entry in series with the feedback structure as shown in Fig. 6(c), then

$$\det(\underset{\sim}{Q}'\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}') = K_1(\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P})+K_2) \tag{4}$$

$$(c^{\sigma})' = K_1(c^{\sigma}+K_2) \text{ for each } \sigma \tag{5}$$

where $K_1 > 0$, $K_2 > 0$ and $\underset{\sim}{P}\underset{\sim}{v} = \underset{\sim}{Q}\underset{\sim}{i}$ (resp.; $\underset{\sim}{P}'\underset{\sim}{v} = \underset{\sim}{Q}'\underset{\sim}{i}$) characterizes the linear four-port, across which the transistor pair are connected, before (resp.; after) the new resistor is added.

Proof: See Appendix C.1. □

Corollary 1. Let N be a two-transistor one-port with a feedback structure and let N' denote the same one-port except the resistance value of some of the resistors which are in series (resp.; in parallel) with the feedback structure is increased (resp.; decreased). Then

$$\det(\underset{\sim}{Q}'\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}') = K_1(\det(\underset{\sim\sim}{Q}\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P})+K_2) \tag{6}$$

$$(c^{\sigma})' = K_1(c^{\sigma}+K_2) \text{ for each } \sigma \tag{7}$$

where $K_1 > 0$ and $K_2 > 0$.

It follows from Corollary 1 that the one-port N tends to satisfy the topological condition if the feedback structure tends to be preserved as the element parameters are varied. In this case N is more likely to possess a negative-resistance region as long as the bias condition is also satisfied. This is demonstrated in the following examples.

Example 4.

Figure 7(a) is a two-transistor one-port with the feedback structure shown in Fig. 7(b), where R1 and R2 are in parallel and R3 is in series with the feedback structure. The v-i curves for various R1, R2 and R3 obtained through computer simulation are shown in Figs. 7(c),(d) and (e). Observe that the v-i curves tend to lose the negative-resistance region as R1 and R2 are decreased and R3 is increased because all of these variations tend to destroy the feedback structure. □

Example 5.

Figure 8(a) is the same as Fig. 7(a) except a new resistor R4 is added in series with the feedback structure as shown in Fig. 8(b). Note that R1 and R2 are in parallel whereas R3 and R4 are in series with thefeedback structure. The v-i curves for various R1, R2, R3 and R4 are shown in Figs. 8(c),(d),(e) and (f). By Corollary 1, the v-i curves tend to lose the negative-resistance region as R1 and R2 are decreased and R3 and R4 are increased. Figures 8(d), (e), and (f) indeed support this prediction. Note, however, that Fig. 8(c) does not follow our prediction; instead, the v-i curve tends to lose its negative-resistance region as R1 increases. This is because the bias condition tends to be violated in this case as R1 increases. □

In view of the above discussions and examples, we can now summarize our

parameter tuning criterion for generating negative-resistance v-i curves as follows:

> Parameter Tuning Criterion: Choose small (resp.; large) resistance values for those resistors which are in series (resp.; in parallel) with the feedback structure while ensuring that the bias condition is not violated.

As mentioned before, adding a resistor in series or in parallel with the driving port will only diminish the possibility of obtaining a type-S or type-N v-i curve. This observation was proved in [1] via a graphical method which we reproduce in Fig. 9 for ease of reference. We can also derive this observation by using the results derived in this subsection.

Consider first the case of Fig. 9(a) where the resistor is in seires with the driving port. By Eq. (1)

$$G' = K'\det(\underset{\sim}{Q}_0'\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0')/\det(\underset{\sim}{Q}_S'\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_S') \tag{8}$$

$$G = K\det(\underset{\sim}{Q}_0\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0)/\det(\underset{\sim}{Q}_S\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_S) \tag{9}$$

if N exhibits a type-S v-i characteristic, then by Assumption 1, the driving port as well as the resistor are in series with the feedback structure. Hence $\det(\underset{\sim}{Q}_0\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0) > 0$ and $\det(\underset{\sim}{Q}_0'\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0') > 0$ for any $\underset{\sim}{D} > 0$ because the feedback structure is destroyed when the driving port is open-circuited. Also by Theorem 2,

$$\det(\underset{\sim}{Q}_S'\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_S') = K_1(\det(\underset{\sim}{Q}_S\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_S)+K_2) \tag{10}$$

where $K_1 > 0$ and $K_2 > 0$ because adding a resistor in this case tends to destroy the feedback structure. Hence $\det(Q_S'TD+P_S')$ tends to become positive as the series resistance increases. It follows from Theorem 1 that the v-i curve of N' tends to be monotone-increasing, as predicted in Fig. 9(b).

If N exhibits a type-N v-i curve, then by Assumption 1, the driving port as well as the series resistor must be in parallel with the feedback structure. Hence $\det(\underset{\sim}{Q}_S\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_S) > 0$ for any $\underset{\sim}{D} > 0$ because the feedback structure will be destroyed when the driving port of N is short-circuited. With the resistor in series with the driving port of N', the feedback structure may still exist because of the series resistor. Hence it is possible that $\det(\underset{\sim}{Q}_S'\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_S') < 0$ for some $\underset{\sim}{D} > 0$. Also $\det(\underset{\sim}{Q}_0\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0) = \det(\underset{\sim}{Q}_0'\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0)$, since the series resistor "floats" when the driving port of N' is open-circuited. Hence it is possible that $\det(\underset{\sim}{Q}_0'\underset{\sim}{T}\underset{\sim}{D}_0+\underset{\sim}{P}_0') < 0$ for some $\underset{\sim}{D}_0 \in \mathcal{D}_0$ and $\det(\underset{\sim}{Q}_S'\underset{\sim}{T}\underset{\sim}{D}_S+\underset{\sim}{P}_S') < 0$ for some $\underset{\sim}{D}_S \in \mathcal{D}_S$.

By Theorem 1, the v-i curve of N' will become multivalued as predicted in Fig. 9(c).

The above observations can be explained in a similar way when the resistor is in parallel with the driving port, as shown in Figs. 9(d), (e) and (f).

B. Parameter Tuning Guidelines.

So far we have derived a criterion for generating negative-resistance devices. Another important problem on this subject is how to adjust the circuit parameters such that the range and slope of the negative-resistance region in the v-i curve can be "tailored" to fit practical applications. We first list some characterizing properties of v-i curves of negative-resistance devices from which some tuning guidelines will evolve.

The v-i curves in Fig. 10, which contain a negative-resistance region can be partitioned into four regions with three partitioned points called the starting, peak, and valley points, respectively. The v-i curve in each region is characterized by a different operating region for each transistor.

(i) Region I is a high-resistance region where both transistors are cut-off. The resistance in this region is determined by the total series resistance of the resistors which form a conducting path when both transistors are removed. If there is no conducting path when both transistors are removed, then the v-i relation in this region is determined by the transistor leakage current. As the driving voltage (resp.; current) increases in a type-N (resp.; type-S) device, one transistor begins to enter its forward active region where the starting point is located.

(ii) Region II is a low-resistance region where one transistor is in the forward active region while the other is still cut-off. As the driving voltage (resp.; current) increases, both transistors tend to become forward active and $\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}D+\underset{\sim}{P}_0)$ (resp.; $\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}D+\underset{\sim}{P}_s)$), which is still positive, decreases for a type-N (resp.; type-S) device until it reaches the peak point where $\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}D+\underset{\sim}{P}_0) = 0$ (resp.; $\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}D+\underset{\sim}{P}_s) = 0$).

(iii) Region III is the negative-resistance region where both transistors are forward active and $\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}D+\underset{\sim}{P}_0) < 0$ (resp.; $\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}D+\underset{\sim}{P}_s) < 0$) for a type-N (resp.; type-S) device. As the driving voltage (resp.; current) further increases, at least one transistor tends to become saturated and $\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}D+\underset{\sim}{P}_0)$ (resp.; $\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}D+\underset{\sim}{P}_s)$), which is negative in this region, will tend to increase for a type-N (resp.; type-S) device until it reaches the valley point where $\det(Q_0TD+P_0) = 0$ (resp.; $\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}D+\underset{\sim}{P}_s) = 0$). In this region, $\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}D+\underset{\sim}{P}_0)$

(resp.; $\det(\underset{\sim}{Q}_S\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_S)$) is a concave function of the driving voltage (resp.; current) with both end points equal to zero, and the small-signal conductance is determined by Eq. (1).

(iv) Region IV is a high (resp.; low)-resistance region for a type-N (resp.; type-S) device. In this region, at least one transistor is saturated and the small-signal conductance, which is positive due to violation of the bias condition, tends to a constant as the driving voltage (resp.; current) increases.

Let us now discuss the effects on the v-i curve due to changes in the resistance values. For simplicity, we only qualitatively list two general guidelines which hold when the bias condition, or the topological condition, remains satisfied as we tune the resistors.

Paremeter Tuning Guideline 1: (Effects on the negative-resistance magnitude)

Assume the bias condition is satisfied throughout the range of the following resistance adjustments. In order to increase the negative-conductance magnitude for a type-S (resp.; type-N) device, adjust the resistances in the direction such that the topological condition tends to be violated (resp.; preserved). More specifically, (a) Type-S device: Increase (resp.; Decrease) the resistance of each resistor which is in series (resp.; in papallel) with the feedback structure. (b) Type-N device: Decrease (resp.; Increase) the resistance of the resistor which is in series (resp.; in parallel) with the feedback structure.

In order to decrease the negative-conductance magnitude, reverse the above operations.

Proof: See Appendix C.2. □

Parameter Tuning Guideline 2: (Effects on the negative-resistance range)

Assume the topological condition is satisfied throughout the range of the following resistance adjustments. In order to increase the current (resp.; voltage) range of a type-S (resp.; type-N) negative-resistance region, adjust the resistances such that the bias condition tends to be satisfied for an increasing range of the driving current (resp.; voltage).

In order to decrease the current (resp.; voltage) range of the negative-resistance region, reverse the above operations.

Proof: See Appendix C.3. □

Remark: The parameter tuning guideline 2 is used mainly in simulation because

it is usually difficult to check by inspection.

Example 6.

In Fig. 11(a) R_1 and R_4 are in series while R_2, R_3, and R_5 are in parallel with the feedback structure. Increasing R_1 and R_4 and decreasing R_2, R_3, and R_5 will increase the negative-conductance magnitude as predicted by the parameter tuning guideline 1(a). This is confirmed in Figs. 11(b), (c), (d), (e), and (f). □

Example 7.

In Fig. 12(a) R_1 and R_3 are in series while R_2 and R_4 are in parallel with the feedback structure. It follows from the parameter tuning guideline 1(b) that decreasing R_1 and R_3 and increasing R_2 and R_4 will increase the negative-conductance magnitude, as is verified in Figs. 12(b), (c), (d), and (e). □

3. Three Conjectures: Partial Solutions

Among thousands of circuit candidates derived from the algorithms given in [1], hundreds of two-transistor one-ports which exhibit either a type-S or a type-N v-i curve have been identified by computer simulation. These simulation results seem to support the following three conjectures [1]:

Conjecture 1: For a one-port device containing two bipolar transistors to exhibit a negative small-signal resistance, it is necessary that in the associated feedback structure, the two emitters be connected to each other.

Conjecture 2: In order to obtain a two-transistor type-S negative-resistance device, the two transistors must be complementary, i.e., one is pnp, the other is npn.

Conjecture 3: In order to obtain a two-transistor type-N negative-resistance device, the two transistors must be of the same type, i.e., both npn or both pnp.

A counterexample to Conjecture 1 has recently been discovered by Willson and his student.† This circuit (Fig. 13(a)) has a feedback structure with one collector and one emitter connected together (Fig. 13(b)), and has been verified both by simulation and laboratory measurement to exhibit a type-S v-i curve as shown in Fig. 13(c). In spite of the existence of this counterexample, Conjecture 1 remains a valuable tool for generating negative-resistance devices. Indeed, we will show that the feedback structure stipulated by Conjecture 1

†Private communication.

(i.e., with both emitters connected together) has a "much better chance" of exhibiting a type-N or a type-S v-i curve than any other connections. To be specific, we will show that for each negative-resistance two-transistor circuit which violates Conjecture 1, we can derive a negative-resistance circuit satisfying Conjecture 1 by interchanging the emitter and collector terminals of one of the two transistors, provided the bias condition remains satisfied.

Consider the feedback structure shown earlier in Fig. A.2. Note that there are only three distinct interconnections between the emitter and collector terminal of each transistor, as shown in Fig. 14; namely, (1) two collectors are connected together; (2) one collector and one emitter are connected together; (3) two emitters are connected together.

It has been shown in [6] that $1-\alpha^{(1)}-\alpha^{(2)}<0$ is a necessary condition for the above transistor circuits to possess multiple d.c. solutions, where $\alpha^{(i)}$ denotes the gain of the controlled current source in the upper junction of transistor T_i. Hence, for the three circuits in Fig. 14, it is necessary that (1) $1-\alpha_r^{(1)}-\alpha_r^{(2)}<0$, (2) $1-\alpha_f^{(1)}-\alpha_r^{(2)}<0$, and (3) $1-\alpha_f^{(1)}-\alpha_f^{(2)}<0$ respectively, in order for the corresponding circuit to possess multiple d.c. solutions. Since the reverse current gain α_r is normally less than 0.5 for bipolar transistors, the configuration in Fig. 14(a) can never yield a negative small-signal resistance and hence only the last two configurations in Fig. 14 are possible candidates for negative-resistance devices.

Lemma 2. For the two-transistor one-ports N' and N'' in Fig. 15,† we have

(1) $\det(\underset{\sim}{Q}\underset{\sim}{T}'\underset{\sim}{D}+\underset{\sim}{P}) \geq \det(\underset{\sim}{Q}\underset{\sim}{T}''\underset{\sim}{D}+\underset{\sim}{P})$ for any $\underset{\sim}{D}>0$

$$\text{where } \underset{\sim}{T}' \triangleq \begin{bmatrix} 1 & -\alpha_r^{(1)} & 0 & 0 \\ -\alpha_f^{(1)} & 1 & 0 & 0 \\ 0 & 0 & 1 & -\alpha_f^{(2)} \\ 0 & 0 & -\alpha_r^{(2)} & 1 \end{bmatrix} \text{ and } \underset{\sim}{T}'' \triangleq \begin{bmatrix} 1 & -\alpha_r^{(1)} & 0 & 0 \\ -\alpha_f^{(1)} & 1 & 0 & 0 \\ 0 & 0 & 1 & -\alpha_r^{(2)} \\ 0 & 0 & -\alpha_f^{(2)} & 1 \end{bmatrix} \tag{11}$$

and

(2) $(c^\sigma)' \geq (c^\sigma)''$ for any index σ where $(c^\sigma)'$ (resp.; $(c^\sigma)''$) denotes the coefficient in the expansion of $\det(\underset{\sim}{Q}\underset{\sim}{T}'\underset{\sim}{D}+\underset{\sim}{P})$ (resp.; $\det(\underset{\sim}{Q}\underset{\sim}{T}''\underset{\sim}{D}+\underset{\sim}{P})$).

†Apart from the emitter and collector terminal labels, the two circuits N' and N'' are assumed to be identical.

Proof: Proof follows directly from the proof of Theorem 5 in [3], upon interchanging $\alpha_r^{(2)}$ and $\alpha_f^{(2)}$ in each term of the coefficients in the expansion of $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P})$. □

Lemma 2 shows that the topological condition is satisfied by N'' so long as it is satisfied by N'. It follows from Eq. (1) that

$$G' = K' \det(\underset{\sim}{Q}_0\underset{\sim}{T}'\underset{\sim}{D}+\underset{\sim}{P}_0)/\det(\underset{\sim}{Q}_s\underset{\sim}{T}'\underset{\sim}{D}+\underset{\sim}{P}_s) \tag{12}$$

and

$$G'' = K'' \det(\underset{\sim}{Q}_0\underset{\sim}{T}''\underset{\sim}{D}+\underset{\sim}{P}_0)/\det(\underset{\sim}{Q}_s\underset{\sim}{T}''\underset{\sim}{D}+\underset{\sim}{P}_s). \tag{13}$$

Without loss of generality, suppose Fig. 15(a) yields a type-S v-i curve, then by Assumption 1, the driving port is in series with the feedback structure. Since the feedback structure is destroyed when the driving port is open-circuited, it follows that $\det(\underset{\sim}{Q}_0\underset{\sim}{T}'\underset{\sim}{D}+\underset{\sim}{P}_0) > 0$ and $\det(\underset{\sim}{Q}_0\underset{\sim}{T}''\underset{\sim}{D}+\underset{\sim}{P}_0) > 0$.

By Lemma 2, $\det(\underset{\sim}{Q}_s\underset{\sim}{T}'\underset{\sim}{D}+\underset{\sim}{P}_s) \geq \det(\underset{\sim}{Q}_s\underset{\sim}{T}''\underset{\sim}{D}+\underset{\sim}{P}_s)$ implies that if N' possesses a negative small-signal resistance at some operating point Q, then $\det(\underset{\sim}{Q}_s\underset{\sim}{T}'\underset{\sim}{D}+\underset{\sim}{P}_s)$ is negative for some $\underset{\sim}{D} > 0$. Consequently, $\det(\underset{\sim}{Q}_s\underset{\sim}{T}''\underset{\sim}{D}+\underset{\sim}{P}_s)$ is also negative for the same $\underset{\sim}{D} > 0$ and hence N'' must also have a negative small-signal resistance at the same operating point Q. Of course it is unlikely that both circuits will have the same operating point. However if the bias condition is still satisfied by N'', then N'' will also exhibit a negative-resistance v-i curve. We will now show that the bias condition is usually satisfied by N'' so long as it is satisfied by N'.

Assume the external source values in Figs. 15(a) and (b) are identical. Then the equations corresponding to KCL, KVL and the element characteristics of N' and N'' are identical except that α_f and α_r associated with the transistor T_2 are interchanged. To simplify our analysis, let us first assume that corresponding branch currents of N'' and N' are identical. It follows from the Ebers-Moll equation in Eq. (A.4) and (A.5) that

$$i_3' = I_s(e^{v_4'/V_T}-1) - \frac{I_s}{\alpha_r}(e^{v_3'/V_T}-1) \tag{14}$$

$$i_4' = \frac{-I_s}{\alpha_f}(e^{v_4'/V_T}-1) + I_s(e^{v_3'/V_T}-1) \tag{15}$$

$$i_3'' = \frac{-I_s}{\alpha_f}(e^{v_3''/V_T}-1) + I_s(e^{v_4''/V_T}-1) \tag{16}$$

$$i_4'' = I_s(e^{v_3''/V_T}-1) - \frac{I_s}{\alpha_r}(e^{v_4''/V_T}-1). \tag{17}$$

Equating Eq. (14) with Eq. (16) and Eq. (15) with Eq. (17), we obtain

$$I_s(e^{v_4'/V_T}-1) - \frac{I_s}{\alpha_r}(e^{v_3'/V_T}-1)$$

$$= -\frac{I_s}{\alpha_f}(e^{v_3''/V_T}-T) + I_s(e^{v_4''/V_T}-1) \tag{18}$$

$$-\frac{I_s}{\alpha_f}(e^{v_4'/V_T}-1) + I_s(e^{v_3'/V_T}-1)$$

$$= I_s(e^{v_3''/V_T}-1) - \frac{I_s}{\alpha_r}(e^{v_4''/V_T}-1). \tag{19}$$

Since the operating point of N' is assumed to be located in the negative-resistance region, it follows that $v_3' >> v_4'$, and e^{v_3'/V_T} becomes the dominant term in the left hand side of Eqs. (18) and (19). We can therefore neglect the e^{v_4'/V_T} term and approximate Eqs. (18) and (19) as follows:

$$-\frac{I_s}{\alpha_r} e^{v_3'/V_T} = -\frac{I_s}{\alpha_f} e^{v_3''/V_T} + I_s e^{v_4''/V_T} \tag{20}$$

$$I_s e^{v_3'/V_T} = I_s e^{v_3''/V_T} - \frac{I_s}{\alpha_r} e^{v_4''/V_T}. \tag{21}$$

Multiplying Eq. (21) by α_r and adding the result to Eq. (20), we obtain

$$(\alpha_r - 1/\alpha_r) I_s e^{v_3'/V_T} = (\alpha_r - \frac{1}{\alpha_f}) I_s e^{v_3''/V_T}. \tag{22}$$

Solving for v_3'', we obtain

$$v_3'' = v_3' + V_T \ln(\frac{1/\alpha_r - \alpha_r}{1/\alpha_f - \alpha_r}). \tag{23}$$

Hence v_3'' must increase by a small amount, equal to $V_T \ln(\frac{1/\alpha_r - \alpha_r}{1/\alpha_f - \alpha_r})$ (approximately 28 mV for typical parameter values), in order to offset any discrepancy due to an interchange between α_r and α_f. By Eq. (21) it can be shown that even though v_4'' will increase by a significant amount, the inequality $e^{v_3''/V_T} >> e^{v_4''/V_T}$ is still satisfied. The above analysis represents only a rough approximation because the branch currents in N' and N'' are not the same. But simulation results tend to support its validity, at least qualitatively. The following example is a case in point.

Example 8.

The two circuits N' and N'' in Figs. 16(a) and (b) are identical except for an interchange between the emitter and the collector of transistor T_2. Both circuits are driven by an equal input current $i = 3.5$ mA, which can be shown to result in an operating point in the negative-resistance region for both circuits. Figure 16(c) gives a comparison between the voltage and current solutions in these two circuits. Note that v_3'' increases only by a small amount as predicted. Note also that although v_2'' and v_4'' increase by a rather substantial amount, they can be neglected when compared with v_1'' and v_3'' because $e^{v_1''/V_T} >> e^{v_2''/V_T}$ and $e^{v_3''/V_T} >> e^{v_4''/V_T}$. Hence the bias condition in N'' is still satisfied. □

It follows from the above observations that if the bias condition is still satisfied, which is true in most cases, then $\det(Q_{\sim S\sim} T''\underset{\sim}{D}'+P_{\sim S}) > \det(Q_{\sim S\sim} T''\underset{\sim}{D}''+P_{\sim S})$ where $\underset{\sim}{D}'$ (resp.; $\underset{\sim}{D}''$) corresponds to the operating point Q' (resp.; Q") in N' (resp.; N''). Also $\det(Q_{\sim S\sim} T'\underset{\sim}{D}'+P_{\sim S}) < 0$ because Q' is in the negative-resistance region. Note that Lemma 2 implies that $\det(Q_{\sim S\sim} T''\underset{\sim}{D}'+P_{\sim S}) \leq \det(Q_{\sim S\sim} T'\underset{\sim}{D}'+P_{\sim S})$ and hence

$$0 > \det(Q_{\sim S\sim} T'\underset{\sim}{D}'+P_{\sim S}) \geq \det(Q_{\sim S\sim} T''\underset{\sim}{D}'+P_{\sim S}) > \det(Q_{\sim S\sim} T''\underset{\sim}{D}''+P_{\sim S}).$$

Consequently, if N' exhibits a negative small-signal resistance at some operating point Q', then N'' will usually exhibit also a negative small-signal resistance at its new operating point Q". In the rare event when the bias condition is violated, we can adjust the element parameters and/or the external source of N'' to restore the bias condition and hance obtain a negative small-signal resistance at some other operating points.

The preceding analysis and observations justify the use of Conjecture 1 as a practical method for generating new two-transistor negative-resistance devices.

Let us now turn to Conjectures 2 and 3 which have so far neither been proved nor disproved. We will now prove them under the following condition (in addition to our standing Assumption 1).

Assumption 2. If both transistors are of the same (resp.; complementary) type, then the driving port is not in series (resp.; in parallel) with the feedback structure.

Remark: It is shown in Appendix C.4, by exhaustive analysis, that the topological condition and the bias condition are inconsistent (i.e., they contradict each other) in the class of circuits which violate Assumption 2.

We now prove Conjecture 2 under Assumptions 1 and 2. Let N be a type-S negative-resistance device containing two transistors of the same type. It follows from Assumption 1 that the driving port of N must be in series with a feedback structure. But this condition is excluded by Assumption 2. Hence N can not exhibit a type-S v-i characteristic. This proves Conjecture 2.

Similarly, we can prove that Conjecture 3 is true under Assumptions 1 and 2. □

4. One-Transistor Negative Resistance Devices

Circuits containing linear positive 2-terminal resistors, independent sources, and a single transistor can not have multiple d.c. solutions because no feedback structure can exist in such circuits. It is possible, however, to obtain multiple d.c. solutions if we allow the circuit to contain a 2-port resistor. In fact, we will show that this is so even for the simplest class of 2-port resistors; namely, linear, passive, and reciprocal. In particular, we will derive the necessary and sufficient condition for the uniqueness of d.c. solution in such circuits. In the special case where the 2-port is an ideal transformer, this necessary and sufficient condition will be shown to be equivalent to the existence of a certain topological structure which can be checked by inspection.

A. Single-Transistor Circuits Containing Linear Passive Reciprocal Two-Ports

Figure 17 shows the general configuration consisting of a transistor connected to a linear resistive 2-port $\hat{N}$ made of linear positive 2-terminal resistors, independent voltage and current sources, and linear passive reciprocal 2-ports.

Lemma 3. If $\hat{N}$ has a short-circuit conductance representation $\underset{\sim}{i} = \underset{\sim\sim}{G}\underset{\sim}{v} + \underset{\sim}{c}$, then N has a unique d.c. solution for all independent source values if and only if $\underset{\sim}{G}$ is diagonally dominant.

Proof: See Appendix C.5. □

Lemma 4. If $\hat{N}$ does not have a short-circuit conductance representation but has a hybrid representation $\underset{\sim}{i} = \underset{\sim\sim}{H}\underset{\sim}{v} + \underset{\sim}{c}$, then N has a unique d.c. solution for all independent source values if and only if (H_a, H_b) is a W_0-pair, where

$$\underset{\sim}{H}_a \triangleq \begin{bmatrix} 1+h_{12}\alpha_1 & -(h_{12}+\alpha_2) \\ 0 & 0 \end{bmatrix}, \quad \underset{\sim}{H}_b \triangleq \begin{bmatrix} h_{11} & 0 \\ -h_{12} & -1 \end{bmatrix}$$

and h_{ij} is the ij-th

component of the hybrid matrix $\underset{\sim}{H}$.

Proof: See Appendix C.6. □

Remark 1: In the case when both $\underset{\sim}{G}$ and $\underset{\sim}{H}$ do not exist, then (1) v_1 and v_2, (2) i_1 and v_2, and (3) v_1 and i_2 are linearly dependent simultaneously. In this case, N can be easily shown to have at most one d.c. solution.

Remark 2. In the special case when $\hat{N}$ contains no linear passive reciprocal 2-ports, we can verify that N has at most one d.c. solution without invoking the feedback structure as follows:

Case 1. When $\underset{\sim}{G}$ exists

Since $\underset{\sim}{G}$ characterizes a linear passive 2-port, $\underset{\sim}{G}$ must be a paramount matrix [9]. Since $\underset{\sim}{G}$ is a 2 x 2 matrix, this implies that $\underset{\sim}{G}$ is diagonally dominant. It follows from Lemma 3 that N has at most one d.c. solution.

Case 2. $\underset{\sim}{G}$ does not exist but $\underset{\sim}{H}$ exists

Without loss of generality, let us set all independent sources in $\hat{N}$ to zero. If both v_1 and v_2 are nonzero, then the non-existence of $\underset{\sim}{G}$ implies that they must be linearly dependent, i.e., there exist nonzero constants c_1 and c_2 such that $c_1v_1 + c_2v_2 = 0$. Since $\hat{N}$ contains only linear positive 2-terminal resistors, it follows from the no-gain property [10] that $|c_1/c_2| \leq 1$ and $|c_2/c_1| \leq 1$. These two inequalities imply that $|c_1/c_2| = 1$ and $|h_{12}| = 1$. Hence $(\underset{\sim}{H}_a, \underset{\sim}{H}_b)$ is a W_0-pair and by Lemma 4, N has at most one d.c. solution.

B. Single-Transistor Circuits Containing an Ideal Transformer

In this subsection we derive an equivalent criterion for unique d.c. solution in terms of the circuit topology. For simplicity we restrict N to contain linear positive 2-terminal resistors, independent sources, one transistor and only one ideal transformer, which is a special case of a linear passive reciprocal 2-port resistor.

Analogous to the "feedback structure" for two-transistor circuits, we now define a special topological structure for one-transistor circuits which can be used to determine the uniqueness of d.c. solution by inspection. In the following, both the transistor and the ideal transformer are considered as 2-ports.

Definition 2. (Degenerate and Nondegenerate Connection).

The above class of one-transistor circuit N is said to have a nondegenerate connection iff

(1) no transistor or transformer port is open-circuited and

(2) no transistor or transformer port is short-circuited and

(3) no transistor (or transformer) ports form a loop

after carrying out the following graph operations on N:[†]

(a) short-circuit all independent voltage sources and open-circuit all independent current sources.

(b) short-circuit some resistors (maybe none).

(c) open-circuit the remaining resistors.

N is said to have a degenerate connection iff it does not have a nondegenerate connection.

Two circuits with a nondegenerate connection are shown in Figs. 18(a) and (b), respectively. A circuit with a degenerate connection is shown in Fig. 19(a). Note that unlike the nondegenerate case where only one nondegenerate connection suffices, here it is necessary to show that no open and/or short circuit combination of R_1 and R_2 gives rise to a nondegenerate connection, as demonstrated in Figs. 19(b), (c), (d) and (e), where J_1 and J_2 denote the transistor port formed by the collector-to-base junction, and the emitter-to-base junction, respectively.

Theorem 3. The above class N of one-transistor circuits has a unique d.c. solution for any circuit parameters and any independent source value if and only if N has a degenerate connection.

Proof: See Appendix C.7. □

It follows from Theorem 3 that any one-transistor circuit with a nondegenerate connection has multiple d.c. solutions for some circuit parameters and independent source values. But just as in the two-transistor case where the existence of a "feedback structure" is only a necessary but not sufficient condition to guarantee the existence of a negative-resistance region for a circuit with a fixed source configuration, the existence of a nondegenerate connection in a one-transistor circuit with a fixed source configuration need not give rise to a small-signal negative resistance. We can apply the following two guidelines to enhance the chances of obtaining a negative resistance in such circuits:

Guideline 1: The resistance of each resistor to be short-circuited (resp.;

[†]Conditions (1), (2), and (3) need be satisfied for only one combination of (b) and (c).

open-circuited) to obtain a nondegenerate connection should be made as small (resp.; large) as possible.

Guideline 2: The resistances should be chosen such that the transistor is biased in the forward active region.

Unfortunately Guidelines 1 and 2 often contradict each other and the class N of one-transistor negative-resistance devices is rather small. Nevertheless, the following algorithm, which is based on the above guidelines, has successfully generated several one-transistor negative-resistance devices.

(1) Start with one of the three nondegenerate connections shown in Fig. 20 where the turns ratio is chosen such that $n > 0$ in Figs. 20(a) and (b) and $n > 1$ in Fig. 20(c). These choices for n are derived from the proof of Theorem 3.

(2) Create the driving port by a plier-type entry (resp.; soldering-iron entry) with any of the three nondegenerate connections in Fig. 20 in order to obtain a current-controlled (resp.; voltage-controlled) negative resistance characteristic. Observe that this step guarantees that the nondegenerate connection is destroyed when the driving port is open-circuited (resp.; short-circuited), thereby ensuring a unique solution for each input current (resp.; voltage), as required by a current-controlled (resp.; voltage-controlled) characteristic.

(3) Add resistors in accordance with Guidelines 1 and 2.

(4) Derive the small-signal resistance and determine whether it can be made negative for some input current (resp.; voltage). If not, modify the location of the resistors and repeat Step (3).

The following examples show two current-controlled negative-resistance devices generated by the above algorithm:

Example 9.

The circuit in Fig. 21(a) is obtained by connecting resistors R_1 (by soldering-iron entry), R_2 (by plier-type entry), and R_3 (by soldering-iron entry) to the circuit shown in Fig. 20(b). Its small-signal resistance across the driving port (obtained by a plier-type entry) is given by

$$\left.\frac{dv}{di}\right|_Q = \frac{R_1}{n} \frac{1}{(1+\beta+\frac{\gamma_\pi}{R_3})} [(1+\frac{\gamma_\pi}{R_3})\frac{1}{n} + \frac{n}{R_1}(1+\frac{\gamma_\pi}{R_3})R_2 + \frac{n\gamma_\pi}{R_1} - \beta] \qquad (24)$$

where $r_\pi = \frac{V_T}{I_C}$ and I_C is the collector current at the operating point Q where $\frac{dv}{di}$ is evaluated. The negative sign in front of β suggests that it may be possible to make $\frac{dv}{di}$ negative. Four families of current-controlled v-i characteristics have been simulated using SPICE with $\beta = 200$, $I_s = 10^{-14}$ A, and various choices of element parameters. They are shown in Figs. 21(b), (c), (d), and (e), respectively. □

Example 10.

The circuit in Fig. 22(a) is obtained by connecting resistors R1 (by plier-type entry), R_2 (by soldering-iron entry), and R_3 (by soldering-iron entry) to the circuit shown in Fig. 20(a). Its small-signal resistance across the driving port (obtained by a plier-type entry) is given by

$$\left.\frac{dv}{di}\right|_Q = \frac{1}{1+\beta+\frac{r_\pi}{R_3}}\left[r_\pi + R_1\left(1+\frac{r_\pi}{R_3}\right) - \frac{\beta R_2}{n} + \frac{1}{n^2}\left(1+\beta+\frac{r_\pi}{R_3}\right)R_2\right]. \tag{25}$$

Again, the presence of the negative sign in front of $\frac{\beta R_2}{n}$ suggests that it may be possible to make $\frac{dv}{di}$ negative. Four families of current controlled v-i characteristics have been simulated using SPICE with $\beta = 200$, $I_s = 10^{-14}$A, and various choices of element parameters. They are shown in Figs. 22(b), (c), (d), and (e), respectively. □

Remark: Both examples above gave a current-controlled negative-resistance device. it can be shown by an exhaustive analysis that it is impossible to generate a voltage-controlled negative resistance v-i curve using less than three resistors. In fact, we conjecture that it is impossible for any one-transistor circuit (containing one ideal transformer) to exhibit a voltage-controlled negative-resistance v-i curve.

5. Odd-Symmetric Negative-Resistance Devices

The voltage-controlled odd-symmetric negative-resistance one-port shown in Fig. 23(a) was first reported by Rosenthal [7]. Using the techniques developed in the preceding sections, we have synthesized the current-controlled odd-symmetric negative-resistance one-port shown in Fig. 24(a). Observe that internal power supplies are required in Figs. 23 and 24 because these two one-ports are active; i.e., their v-i curves have points in the second and the fourth quadrants. Our objective in this final section is to show how these two symmetric

circuits can be systematically synthesized.

Consider first the odd-symmetric voltage-controlled case. Without loss of generality, we can assume the associated one-port must have the basic circuit topology shown in Fig. 25 due to the following observations:

(1) A "feedback structure" is required to produce multiple d.c. solutions. (2) The transistors must be both npn or pnp in order for the circuit to exhibit rotational symmetry [8]. (3) The driving port must be in parallel with the feedback structure because each input voltage corresponds to a unique port current. Consequently the feedback structure must be destroyed upon short-circuiting the driving port. (4) At least one power supply is required. If possible, it would be desirable to use a single independent voltage source within the one-port. (5) Due to the horizontal symmetry requirement, the driving port can only be applied to both collector terminals by soldering-iron entry. (6) Due to the rotational symmetry requirement, the single internal voltage source can only be added across the collector-emitter terminals with the positive terminal of the voltage source connected to both collector terminals (due to bias condition).

Since the feedback structure in Fig. 25 is destroyed when the internal voltage source E is short-circuited, it is necessary to add at least two resistors R_1 and R_2, as shown in Fig. 26.

Note that the augmented circuit in Fig. 26 is identical to that shown in Fig. 23(a). Its v-i curve has been obtained by both computer simulation and laboratory measurements, and is shown in Fig. 23(b). This is the simplest two-transistor circuit which exhibits an odd-symmetric voltage-controlled negative-resistance v-i curve. In fact, it can be shown that any other two-transistor circuit having a similar odd-symmetric voltage-controlled v-i curve can be reduced to this basic circuit configuration.

Consider next the current-controlled one-port shown in Fig. 24(a). Its v-i curve has been obtained by both computer simulation and laboratory measurements, and is shown in Fig. 24(b). This circuit can be synthesized by the same approach used to derive the voltage-controlled one-port in Fig. 23(a). Note the differences between the two circuit topologies are due to the following observations:

(1) The driving port must be in series with the feedback structure in order to guarantee a unique d.c. solution for each input port current.

(2) Two internal independent voltage sources are used to avoid a direct connection between the two emitters. Otherwise the feedback structure will not be destroyed when the driving port is open-circuited.

(3) The driving port must be inserted by a plier-type entry between the two emitters in order to preserve the horizontal symmetry.

Remark: It is possible to trade one voltage source with two resistors as shown in Fig. 27(a). The resulting v-i curve shown in Fig. 27(b) is similar to that shown in Fig. 24(b).

Observe that the driving port in Fig. 27(a) is no longer in series with the feedback structure in view of the additional resistors R_3 and R_4. Hence the feedback structure in this case is not destroyed upon open-circuiting the driving port. However if the resistances of R_3 and R_4 are chosen to be very large, then the feedback structure will tend to be destroyed when the driving port is open-circuited. In this case, it is possible for the circuit to exhibit a current-controlled negative-resistance v-i curve.

Appendix:

A. Bipolar Transistor Model

The d.c. Ebers-Moll circuit model shown in Fig. A.1 is used to model the bipolar transistors throughout this paper. Each nonlinear resistor in this model is characterized by the usual pn junction equation

$$j_k = I_{0_k}(e^{v_k/V_T}-1). \tag{A.1}$$

To avoid redundancy, we will consider only the npn transistor model. The pnp case is similar except that the voltage polarity and the current direction are reversed. From Fig. A.1(a)

$$I_C = \alpha_f j_2 - j_1 = \alpha_f I_{ES}(e^{V_{BE}/V_T}-1) - I_{CS}(e^{V_{BC}/V_T}-1) \tag{A.2}$$

$$I_E = - j_2 + \alpha_r j_1 = - I_{ES}(e^{V_{BE}/V_T}-1) + \alpha_r I_{CS}(e^{V_{BC}/V_T}-1) \tag{A.3}$$

where I_{CS} and I_{ES} are the saturation current for the base-to-collector and base-to-emitter junction, respectively. The parameter V_T is called the thermal voltage and is approximately equal to 26 mV at 27°C.

Equations (A.2) and (A.3) can be recast into the following form often used for computer simulation.

$$I_C = I_S(e^{V_{BE}/V_T}-1) - \frac{I_S}{\alpha_r}(e^{V_{BC}/V_T}-1) \tag{A.4}$$

$$I_E = \frac{-I_S}{\alpha_f}(e^{V_{BE}/V_T}-1) + I_S(e^{V_{BC}/V_T}-1) \tag{A.5}$$

where $I_S = \alpha_f I_{ES} = \alpha_r I_{CS}$.

Due to the finite (0.5 V - 0.7 V) cut-in voltage, a physical bipolar transistor does not "turn on" or "turn off" when appropriate junctions are "forward" or "reversed" biased. From the practical point of view, it is more realistic to adopt the following definition of transistor operating regions:

Definition A.1. A bipolar transistor is said to be biased at the

(i) Forward Active Region

(ii) Saturation Region

(iii) Cut-Off Region
(iv) Reverse Active Region
iff the base-to-emitter junction voltage V_{BE} is
(i) greater
(ii) greater
(iii) less
(iv) less
than the cut-in voltage and the base-to-collector junction voltage V_{BC} is
(i) less
(ii) greater
(iii) less
(iv) greater
than the cut-in voltage.

B. Background Material

This section briefly reviews some results by Willson, Nielsen and Lee which are applied in this paper. Throughout this section, we restrict these results to the class of circuits N made of two transistors, linear positive 2-terminal resistors and independent voltage and current sources.

Definition A.2 [6] (Feedback Structure)

A circuit N is said to contain a feedback structure iff the structure of Fig. A.2 is present when some combination of short and open circuits replaces all resistors, and when each independent voltage (resp.; current) source is replaced by a short-circuit (resp.; open-circuit). The "transistor-like" symbol used in Fig. A.2 is meant to denote a transistor which can be either npn or pnp and can have either of the two possible orientations with respect to its collector and emitter terminals.

Lemma A.1 [5]. The d.c. equation of N can be characterized by

$$\underset{\sim\sim\sim}{Q}\underset{\sim\sim}{T}\underset{\sim}{f}(\underset{\sim}{v}) + \underset{\sim\sim}{P}\underset{\sim}{v} = \underset{\sim}{r} \tag{A.6}$$

where

$$\underset{\sim\sim}{P}\underset{\sim}{v} = \underset{\sim\sim}{Q}\underset{\sim}{i} + \underset{\sim}{r} \tag{A.7}$$

characterizes the linear resistive four-port with the two transistors extracted across the ports as shown in Fig. A.3. The equation

$$\underset{\sim}{i} = - \underset{\sim\sim}{T}\underset{\sim}{f}(\underset{\sim}{v}) \tag{A.8}$$

characterizes the Ebers-Moll model of the transistors, where

$$\underset{\sim}{T} \triangleq \begin{bmatrix} 1 & -\alpha_r & 0 & 0 \\ -\alpha_f & 1 & 0 & 0 \\ 0 & 0 & 1 & -\alpha_r \\ 0 & 0 & -\alpha_f & 1 \end{bmatrix}, \tag{A.9}$$

$$\underset{\sim}{f}(\underset{\sim}{v}) \triangleq [f_1(v_1)\ f_2(v_2)\ f_3(v_3)\ f_4(v_4)]^T. \tag{A.10}$$

and

$$f_k(v_k) = I_{0_k}(e^{v_k/V_T}-1). \tag{A.11}$$

The original definition of a W_0-pair for matrix pair $(\underset{\sim}{A},\underset{\sim}{B})$ is given in [5]. Here we adopt one of its equivalent property as our definition:

Definition A.3 [5]. (W_0-pair)

A matrix pair $(\underset{\sim}{A},\underset{\sim}{B})$ is said to be a W_0-pair iff $\det(\underset{\sim}{A}\underset{\sim}{D}+\underset{\sim}{B})$ is nonzero for any positive diagonal matrix $\underset{\sim}{D} > 0$.

Lemma A.2 [6]. Let N be described by Eq. (A.6), then $(\underset{\sim}{Q}\underset{\sim}{T},\underset{\sim}{P})$ is a W_0-pair if and only if N contains no feedback structure.

Lemma A.3 [5]. Equation (A.6) has a unique solution for any $\underset{\sim}{r}$ if and only if $(\underset{\sim}{Q}\underset{\sim}{T},\underset{\sim}{P})$ is a W_0-pair.

Remark: Willson's original theorem says "There exists a unique solution of the equation $\underset{\sim}{A}\underset{\sim}{f}(\underset{\sim}{x}) + \underset{\sim}{B}\underset{\sim}{x} = \underset{\sim}{c}$ for any n-dimensional vector $\underset{\sim}{c}$ in $\mathbb{R}^n$ and any $\underset{\sim}{f}$ in the class of F^n if, and only if, $(\underset{\sim}{A},\underset{\sim}{B})$ is a W_0-pair. Here, F^n denotes the collection of mappings from $\mathbb{R}^n$ onto $\mathbb{R}^n$, defined as $\underset{\sim}{f} \in F^n$ iff there exist for i = 1, 2, ..., n, strictly-increasing functions f_i, mapping $\mathbb{R}^1$ onto $\mathbb{R}^1$ such that for each $\underset{\sim}{x} = [x_1\ x_2\ \ldots\ x_n]^T$ in $\mathbb{R}^n$, $\underset{\sim}{f}(\underset{\sim}{x}) = [f_1(x_1)\ f_2(x_2)\ \ldots\ f_n(x_n)]^T$." In our case, the mapping f_i in Eq. (A.10) is only a strictly-increasing but not onto function. Hence the solution may not exist for the class of circuits N contained in this paper. However if the breakdown phenomenon in real transistors is included in the model, then the solution always exists.

Lemma A.4 [4]. N has a unique d.c. operating point for any independent source

Lemma A.5 [4]. Let G denote the driving-point small-signal conductance

evaluated at some operating point Q of the one-port N as shown in Fig. A.4(a). Then

$$\boxed{G = G(0)\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0)\det(\underset{\sim}{Q}_s\underset{\sim}{D}+\underset{\sim}{P}_s)/\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s)\det(\underset{\sim}{Q}_0\underset{\sim}{D}+\underset{\sim}{P}_0)} \tag{A.12}$$

where $\underset{\sim}{P}_0\underset{\sim}{v} = \underset{\sim}{Q}_0\underset{\sim}{i}$(resp.; $\underset{\sim}{P}_s\underset{\sim}{v} = \underset{\sim}{Q}_s\underset{\sim}{i}$) characterizes the linear 4-port to which the linearized transistor models are connected when the driving port x-y is open-circuited (resp.; short-circuited) as shown in Fig. A.4(b) and

$$\underset{\sim}{D} \triangleq \text{diag.}(d_1,d_2,d_3,d_4) \tag{A.13}$$

$$d_k \triangleq f_k'(v_k) \qquad k = 1, 2, 3, 4 \tag{A.14}$$

where the v_k's are the transistor junction voltages at the operating point Q with $v_k > 0$ when the corresponding junction is forward-biased, G(0) is the small-signal conductance across the driving port with each controlled source in the linearized transistor model being eliminated as shown in Fig. A.4(c).

Lemma A.6 [3]. A two-transistor circuit can possess at most three d.c. solutions for all possible circuit configurations.

C. Proofs of Lemmas and Theorems

1. Proof of Theorem 2

We first show that Eqs. (4) and (5) hold in the case when $(\underset{\sim}{P},\underset{\sim}{Q})$ (resp.; $(\underset{\sim}{P}',\underset{\sim}{Q}')$) represents $(\underset{\sim}{P}_0,\underset{\sim}{Q}_0)$ (resp.; $(\underset{\sim}{P}_0',\underset{\sim}{Q}_0')$).

Let G denote the small-signal conductance of the one-port in Fig. A.5(a) with its driving port in parallel with the feedback structure and let G' be the corresponding small-signal conductance in Fig. A.5(b) or (c). Then it follows from Eq. (1) that

$$G = K\det(\underset{\sim}{Q}\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P})/\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s) = M/N \tag{A.15}$$

$$G' = K'\det(\underset{\sim}{Q}'\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}')/\det(\underset{\sim}{Q}_s'\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s') = M'/N' \tag{A.16}$$

where

$$M \triangleq \det(\underset{\sim}{Q}\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) \text{ (resp.; } M' \triangleq \det(\underset{\sim}{Q}'\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}')) \tag{A.17}$$

$$N \triangleq \det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s)/K \text{ (resp.; } N' \triangleq \det(\underset{\sim}{Q}_s'\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s')/K'). \tag{A.18}$$

Since the feedback structure is destroyed when the driving port is short-circuited, it follows that

$$\det(\underset{\sim}{Q}_S\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_S) > 0 \text{ and } \det(\underset{\sim}{Q}'_S\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}'_S) > 0 \text{ for any } \underset{\sim}{D} > 0.$$

Hence $N > 0$ and $N' > 0$ in Eq. (A.18). Let G" denote the small-signal conductance of the one-port in Fig. A.5(d) (resp.; Fig. A.5(e)) with the newly added resistor short-circuited (resp.; open-circuited). It follows from Eq. (1) that

$$G'' = K'' \det(\underset{\sim}{Q}''_0\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}''_0)/\det(\underset{\sim}{Q}''_S\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}''_S)$$

$$= M''/N'' \tag{A.19}$$

where M" and N" are defined similarly as in Eqs. (A.17) and (A.18). Since the feedback structure is destroyed in Fig. A.5(d) (resp.; Fig. A.5(e)) when the new resistor is short-circuited (resp.; open-circuited), so $M'' > 0$ and $N'' > 0$ for any $\underset{\sim}{D} > 0$. Applying the bilinear transformation, we can rewrite

$$G' = M'/N' = (M+YM'')/(N+YN'') \text{ in Fig. A.5(b)} \tag{A.20}$$

and

$$G' = M'/N' = (M+RM'')/(N+RN'') \text{ in Fig. A.5(c).} \tag{A.21}$$

Therefore

$$M' = N'(M+YM'')/(N+YN'') \tag{A.22}$$

or

$$M' = N'(M+RM'')/(N+RN'') \tag{A.23}$$

Since $Y > 0$, $R > 0$, $M'' > 0$, $N'' > 0$, $N > 0$, and $N' > 0$, so $M' = K_1(M+K_2)$ where $K_1 = N'/(N+YN'') > 0$ and $K_2 = YM'' > 0$ or $K_1 = N'/(N+RN'') > 0$ and $K_2 = RM'' > 0$. Hence

$$\det(\underset{\sim}{Q}'\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}') = K_1(\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P})+K_2) \tag{A.24}$$

where $K_1 > 0$ and $K_2 > 0$. Since Eq. (A.24) is an identity for any $\underset{\sim}{D} > 0$, it follows from Eq. (3) that

$$(c^\sigma)' = K_1(c^\sigma+K_2). \tag{A.25}$$

The case when $(\underset{\sim}{P},\underset{\sim}{Q})$ represents $(\underset{\sim}{P}_S,\underset{\sim}{Q}_S)$ can be proved in the same way with G denoting the small-signal conductance of the one-port in Fig. A.5(f) where the driving port is in series with the feedback structure. □

2. Proof of Parameter Tuning Guideline 1

Equation (1) implies

$$G = K \det(\underset{\sim}{Q}_0\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0)/\det(\underset{\sim}{Q}_S\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_S). \tag{A.26}$$

In the type-N (resp.; type-S) negative-resistance region, $\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0) < 0$ (resp.; $\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s) < 0$). If the bias condition is still satisfied when the resistance of the resistor, which is in series (resp.; in parallel) with the feedback structure, increases (resp.; decreases) such that the topological condition is violated, then $|\det(\underset{\sim}{Q}_0\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_0)|$ (resp.; $|\det(\underset{\sim}{Q}_s\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}_s)|$) decreases. Hence $|G|$ decreases for type-N but increases for type-S negative-resistance devices. □

3. Proof of Parameter Tuning Guideline 2

If the topological condition is satisfied throughout the range of variation of resistances such that the bias condition is satisfied over a larger range of driving voltage (resp.; current) in type-N (resp.; type-S) negative-resistance devices, then the negative-resistance voltage (resp.; current) range will increase because the negative resistance occurs when both transistors are forward active (bias condition is satisfied). □

4. Very few two-transistor one-ports can exhibit a negative small-signal resistance if both transistors are of the same (resp.; complementary) type and the driving port is in series (resp.; in parallel) with the feedback structure.

Proof: It has been shown that the bias conditions, $d_1 >> d_2$ and $d_3 >> d_4$ are required in order to have $\det(\underset{\sim}{Q}\underset{\sim\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) < 0$. Hence the following conditions on the npn transistors are required in order to fulfill the above conditions where the voltage polarity and current direction on each junction voltage and current are shown in Fig. A.1.

Condition 1. $V_{BE_1} > V_{BC_1}$ and $V_{BE_2} > V_{BC_2}$; otherwise $d_1 < d_2$ and $d_3 < d_4$.

Condition 2. $V_{BE_1} > 0$ and $V_{BE_2} > 0$; otherwise the transistor will be cut-off since $V_{BE_1} > V_{BC_1}$ and $V_{BE_2} > V_{BC_2}$ are required.

Condition 3. $I_{E_1} < 0$ and $I_{E_2} < 0$; otherwise by Eq. (A.5), these inequalities will lead to $(V_{BC}-V_{BE}) > V_T\ell_n(1/\alpha_f) > 0$.

Condition 4. $I_{C_1} > 0$ and $I_{C_2} > 0$; otherwise by Eq. (A.4), these inequalities will lead to $(V_{BE}-V_{BC}) < V_T\ell_n(1/\alpha_r) = 18$ mV for $\alpha_r = 0.5$. Hence Condition 1 implies that 18 mV $> (V_{BE}-V_{BC}) > 0$. Such a bias condition is very tight and $d_1 >> d_2$ and $d_3 >> d_4$ can no longer be satisfied.

Condition 5. $I_{B_1} > 0$ and $I_{B_2} > 0$; otherwise the transistors will be cut-off.

Let us now analyze the following mutually exclusive cases:

Case I: Both transistors are of the same type.

There are three different ways for applying the driving source such that the driving port is in series with the feedback structure as shown in Fig. A.6. Here we use the voltage source excitation. The same result applies for current source excitation.

Case. I.1. The voltage source is located between the two emitters as shown in Fig. A.6(a).

Several resistors are required as shown in Fig. A.7 in order to fulfill the bias conditions:

(i) Resistor R_1 is required; otherwise Condition 1 is not satisfied.

(ii) Resistor R_2 is required; otherwise the KCL equation at node C_1 ($I_{C_1}+I_{B_2}=0$) is not satisfied since Conditions 4 and 5 imply $I_{C_1} > 0$ and $I_{B_2} > 0$.

(iii) Resistor R_3 is required; otherwise the KCL equation at node E_1 ($-I_{E_1}+I_{R_1}=0$) is not satisfied since $I_{E_1} < 0$ by Condition 3 and $I_{R_1} > 0$ by (i).

(iv) Resistor R_4 is required; otherwise the KVL equation ($V_{BE_1}+V_{R_3}=0$) is not satisfied since $V_{BE_1} > 0$ by Condition 2 and $V_{R_3} > 0$ by (iii).

(v) Resistor R_5 is required; otherwise the KCL equation at node B1 ($I_{B_1}+I_{R_4}=0$) is not satisfied since $I_{B_1} > 0$ by Condition 5 and $I_{R_4} > 0$ by (iv).

(vi) Resistor R_6 is required to increase the voltage at node C_1; otherwise transistor T_1 will be heavily saturated and Condition 1 will not be satisfied.

Simulation result shows that the bias conditions, $V_{BE_1} >> V_{BC_1}$ and $V_{BE_2} >> V_{BC_2}$, require R_1, R_4, and R_6 to be very large and R_2, R_3, and R_5 to be very small as shown in Table A.1. These values tend to destroy the feedback structure and by Corollary 1 in Section 2, the possibility for $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) < 0$ for some $\underset{\sim}{D} \in \mathcal{D}$ is extremely small if not zero (as yet we were unable to find even one example).

Case I.2. The voltage source is located between B_1 and C_2 with the positive terminal of the voltage source connected to B_1, as shown in Fig. A.6(b).

Several resistors are required as shown in Fig. A.8 in order to fulfill the bias conditions:

(i) Resistor R_1 is required; otherwise Condition 1 is not satisfied since $V_{BC_2} > V_{BE_2}$.

(ii) Resistor R_2 is required in order not to heavily saturate T_1.

(iii) Resistor R_3 is required; otherwise the KCL equation at node E_1 or E_2 ($I_{E_1}+I_{E_2}=0$) is not satisfied since $I_{E_1} < 0$ and $I_{E_2} < 0$ by Condition 3.

(iv) Resistor R_4 is required; otherwise the KCL equation at node C_2, ($I_{R_1}+I_{C_2}=0$) is not satisfied since $I_{C_2} > 0$ by Condition 4 and $I_{R_1} > 0$ by (i).

(v) Resistor R_5 is required; otherwise the KCL equation at node C_1 ($I_{C_1}+I_{B_2}+I_{R_4}=0$) is not satisfied since $I_{C_1} > 0$ by Condition 4, $I_{B_1} > 0$ by 5, and $I_{R_4} > 0$ by (iv).

(vi) Resistor R_6 is required in order not to heavily saturate T_2.

Simulation result shows that the bias conditions require R_1, R_2, and R_6 to be very large and R_3, R_4, and R_5 to be very small as shown in Table A.2. These values tend to destroy the feedback structure and by Corollary 1 in Section 2, the possibility for $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) < 0$ for some $\underset{\sim}{D} \in \mathcal{D}$ is very small if not zero.

Case I.3: The voltage source is located between B_1 and C_2 with the positive terminal of the voltage source connected to C_2, as shown in Fig. A.6(c).

Several resistors are required as shown in Fig. A.9 to fulfill the bias conditions:

(i) Resistor R_1 is required; otherwise T_1 is cut-off.

(ii) Resistor R_2 is required; otherwise the KCL equation at node B_1 ($I_{B_1}+I_{R_1}=0$) is not satisfied since $I_{B_1} > 0$ by Condition 5 and $I_{R_1} > 0$ by (i).

(iii) Resistor R_3 is required; otherwise the KCL equation at node C_1 ($I_{C_1}+I_{R_2}+I_{B_2}=0$) is not satisfied since $I_{C_1} > 0$ and $I_{B_2} > 0$ by Condition 4 and 5, and $I_{R_2} > 0$ by (ii).

(iv) Resistor R_4 is required; otherwise the KCL equation at node E_1 or E_2 ($I_{E_1}+I_{E_2}=0$) is not satisfied since $I_{E_1} < 0$ and $I_{E_2} < 0$ by Condition 3.

(v) Resistor R_5 is required; otherwise the voltage V_{BE_1} may not be sufficiently large because V_{CE_1} is limited to the junction voltage V_{BE_2}, and $V_{CE_1} = V_{R_2} + V_{BE_1}$ where $V_{R_2} > 0$ by (ii).

Simulation result shows that the bias conditions require R_1 and R_5 to be very large and R_2, R_3, and R_4 to be very small as shown in Table A.3. These values tend to destroy the feedback structure and by Corollary 1 in Section 2, the possibility for $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) < 0$ for some $\underset{\sim}{D} \in \mathcal{D}$ is extremely small if not zero.

Case II. One transistor is npn; the other is pnp.

Similarly to Case I, let us choose a voltage source excitation. Note that there are six different ways to apply the voltage source, such that it is in parallel with the feedback structure as shown in Fig. A.10. For simplicity, we only discuss two cases in Figs. A.10(a) and (c), the other cases follow similarly.

Case II.1. The voltage source is across the collector and emitter as shown in Fig. A.10(a).

Several resistors are required as shown in Fig. A.11 in order to fulfill the bias conditions:

(i) Resistor R_1 is required; otherwise the KVL equation ($V_{EC_2}+V_{BE_1}=0$) is not satisfied since by Condition 1 $V_{EC_2} > 0$ for the pnp transistor and $V_{BE_1} > 0$ by Condition 2.

(ii) Resistor R_2 is required; otherwise the KCL equation at node E_2, ($-I_{E_2}+I_{R_1}=0$) is not satisfied since $I_{E_2} < 0$ by Condition 3 for the pnp transistor and $I_{R_1} > 0$ by (i).

(iii) Resistor R_3 is required; otherwise the KVL equation ($V_{R2}+V_{EB_2}=0$) is not satisfied since $V_{R_2} > 0$ by (ii) and $V_{EB_2} > 0$ by Condition 2 for the pnp transistor.

(iv) Resistor R_4 is required; otherwise the KCL equation at node B_2 ($I_{R_3}+I_{B_2}=0$) is not satisfied since $I_{R_3} > 0$ by (iii) and Condition 5 implies $I_{B_2} > 0$ for the pnp transistor.

A simple analysis of Fig. A.11 shows that the inequality $R_3/R_4 > R_2/R_1$ must be satisfied; otherwise Condition 2, which implies that $V_{EB_2} > 0$ for the pnp transistor, is not satisfied. But this inequality will impose a constraint on the resistances which tends to destroy the feedback structure. Hence, by Corollary 1 in Section 2, the possibility for $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) < 0$ for some $\underset{\sim}{D} \in \mathcal{D}$ is very small if not zero.

Case II.2. The voltage source is across the collector pair as shown in Fig. A.10(c).

Several resistors are required as shown in Fig. A.12 in order to fulfill the bias conditions:

(i) Resistors R_1 and R_2 are required; otherwise the KVL equations

($V_{CE_1}+V_{EB_2}=0$ and $V_{EC_2}+V_{BE_1}=0$) are not satisfied since by Condition 1 $V_{CE_1} > 0$ and $V_{EC_2} > 0$, and by Condition 2 $V_{BE_1} > 0$ and $V_{EB_2} > 0$.

(ii) Resistors R_3 and R_4 are required; otherwise the KCL equations ($I_{B_1}+I_{R_2}=0$ and $I_{B_2}+I_{R_1}=0$) are not satisfied since $I_{B_1} > 0$ and $I_{B_2} > 0$ by Condition 5, and $I_{R_1} > 0$ and $I_{R_2} > 0$ by (i).

A simple analysis of Fig. A.12 shows that the inequality $R_1/R_4 > R_3/R_2$ must be satisfied; otherwise $V_{B_2} > V_{B_1}$ and $V_{B_1} - V_{B_2} = V_{BE_1} + V_{EB_2} < 0$, which violates Condition 2. But the resistances satisfying the above inequality would tend to destroy the feedback structure. Hence, by Corollary 1 in Section 2, the possibility for $\det(\underset{\sim}{Q}\underset{\sim}{T}\underset{\sim}{D}+\underset{\sim}{P}) < 0$ for some $\underset{\sim}{D} \in \mathcal{D}$ is very small if not zero. □

5. Proof of Lemma 3

From Fig. 17, the 2-port $\hat{N}$ is described by

$$\underset{\sim}{i} = \underset{\sim}{G}\underset{\sim}{v} + \underset{\sim}{c} \tag{A.27}$$

where $\underset{\sim}{i} \triangleq \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$ $\underset{\sim}{v} \triangleq \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$ $\underset{\sim}{c} \triangleq \begin{bmatrix} c_1 \\ c_2 \end{bmatrix}$ $\underset{\sim}{G} \triangleq \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix}$

and $g_{12} = g_{21}$ because $\hat{N}$ is reciprocal. Substituting the transistor equation

$$\underset{\sim}{i} = -\underset{\sim}{T}\underset{\sim}{F}(\underset{\sim}{v}) \tag{A.28}$$

where $\underset{\sim}{T} \triangleq \begin{bmatrix} 1 & -\alpha_2 \\ -\alpha_1 & 1 \end{bmatrix}$, $\underset{\sim}{f}(\underset{\sim}{v}) \triangleq \begin{bmatrix} f_1(v_1) \\ f_2(v_2) \end{bmatrix}$,

into Eq. (A.27), we obtain

$$\underset{\sim}{T}\underset{\sim}{f}(\underset{\sim}{v}) + \underset{\sim}{G}\underset{\sim}{v} + \underset{\sim}{c} = 0 \tag{A.29}$$

Since $f_i(\cdot)$ is strictly increasing, by Lemma A.3, $(\underset{\sim}{T},\underset{\sim}{G})$ is a W_0-pair if and only if Eq. (A.29) has a unique solution for any $\underset{\sim}{c}$. Since $\det \underset{\sim}{T} = 1 - \alpha_1\alpha_2 > 0$ and since $\det \underset{\sim}{G} = g_{11}g_{22} - g_{12}^2 \geq 0$ (because $\hat{N}$ is passive), it follows that $(\underset{\sim}{T},\underset{\sim}{G})$ is a W_0-pair if and only if

$$\det \begin{bmatrix} 1 & g_{12} \\ -\alpha_1 & g_{22} \end{bmatrix} = g_{22} + \alpha_1 g_{12} \geq 0 \qquad \text{and}$$

$$\det \begin{bmatrix} g_{11} & -\alpha_2 \\ g_{12} & 1 \end{bmatrix} = g_{11} + \alpha_2 g_{12} \geq 0.$$

Since α_1 and α_2 may assume any real value between 0 and 1, it follows that $g_{11} + \alpha_2 g_{12} \geq 0$ and $g_{22} + \alpha_1 g_{12} \geq 0$ if and only if $g_{11} \geq |g_{12}|$ and $g_{22} \geq |g_{12}|$, or equivalently, $\underset{\sim}{G}$ is diagonally dominant. □

6. Proof of Lemma 4

The two-port $\hat{N}$ is described by the hybrid representation

$$\underset{\sim}{y} = \underset{\sim\sim}{H}\underset{\sim}{x} + \underset{\sim}{c} \tag{A.30}$$

where $\underset{\sim}{y} \triangleq \begin{bmatrix} i_1 \\ v_2 \end{bmatrix}$ $\underset{\sim}{x} \triangleq \begin{bmatrix} v_1 \\ i_2 \end{bmatrix}$ $\underset{\sim}{c} \triangleq \begin{bmatrix} c_1 \\ c_2 \end{bmatrix}$ $\underset{\sim}{H} \triangleq \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix}$

Then $h_{22} = 0$ (otherwise $\hat{N}$ has a $\underset{\sim}{G}$ representation) and $h_{12} = -h_{21}$ ($\hat{N}$ is reciprocal). Substituting Eq. (A.28) into Eq. (A.30), we obtain

$$\begin{bmatrix} 1+h_{12}\alpha_1 & -(h_{12}+\alpha_2) \\ 0 & 0 \end{bmatrix} \begin{bmatrix} f_1(v_i) \\ f_2(v_2) \end{bmatrix} + \begin{bmatrix} h_{11} & 0 \\ -h_{12} & -1 \end{bmatrix} \begin{bmatrix} v_i \\ v_2 \end{bmatrix} + \begin{bmatrix} c_1 \\ c_2 \end{bmatrix} = 0 \tag{A.31}$$

By Lemma A.3, Eq. (A.31) has a unique solution for any $\underset{\sim}{c}$ if and only if

$$\left(\begin{bmatrix} 1+h_{12}\alpha_1 & -(h_{12}+\alpha_2) \\ 0 & 0 \end{bmatrix}, \begin{bmatrix} h_{11} & 0 \\ -h_{12} & -1 \end{bmatrix} \right) \text{ is a } W_0\text{-pair.}$$ □

7. Proof of Theorem 3

(Only if) This part is equivalent to showing that if N has a nondegenerate connection, then there exists a set of element parameters and independent source values such that N has multiple d.c. solutions.

By Definition 2, there exists a combination of short circuits and open circuits for the resistors in N such that the resulting circuit has exactly two possible structures after each independent source is eliminated as shown in Figs. 20(a) and (b).

(a) Common-Base Configuration

As shown in Fig. 20(a), $\hat{N}$ has no $\underset{\sim}{G}$ representation but has an $\underset{\sim}{H}$ representation

$$\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 0 & -n \\ n & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix} . \tag{A.32}$$

Since $\left(\begin{bmatrix} 1-n\alpha_1 & n-\alpha_2 \\ 0 & 0 \end{bmatrix}, \begin{bmatrix} 0 & 0 \\ n & -1 \end{bmatrix} \right)$ is not a W_0-pair if and only if $(n\alpha_1-1)(\alpha_2 n-n^2) < 0$. It follows from Lemma 4 that if we choose $n > \frac{1}{\alpha_1}$ or $0 < n < \alpha_2$, then the circuit in Fig. 20(a) has multiple d.c. solutions for some independent source values.

(b) Common-Emitter or Common-Collector Configuration

As shown in Fig. 20(b), $\hat{N}$ has no $\underset{\sim}{G}$ representation but has an $\underset{\sim}{H}$ representation

$$\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 0 & -n/n+1 \\ n/n+1 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix} \tag{A.33}$$

Since $\left(\begin{bmatrix} 1-\frac{n}{n+1}\alpha_1 & \frac{n}{n+1}-\alpha_2 \\ 0 & 0 \end{bmatrix}, \begin{bmatrix} 0 & 0 \\ \frac{n}{n+1} & -1 \end{bmatrix} \right)$ is not a W_0-pair if and only if $(\frac{n}{n+1}\alpha_1-1)[\alpha_2 \frac{n}{n+1}-(\frac{n}{n+1})^2] < 0$. It follows from Lemma 4 that if we choose $\frac{n}{n+1} > \frac{1}{\alpha_1}$ or $0 < \frac{n}{n+1} < \alpha_2$, then the circuit in Fig. 20(b) has multiple d.c. solutions for some independent source values. The inequality $\frac{n}{n+1} > \frac{1}{\alpha_1}$ implies that $n < -1$ and hence the structure in Fig. 20(c) must be used.

Figures 20(a), (b), and (c) are obtained by short-circuiting and/or open-circuiting the resistors. We can choose the turns ratio as required by the above inequalities and make the resistances of the short-circuited (resp.; open-circuited) resistors as small (resp.; large) as possible in order to obtain the nondegenerate connection in Fig. 20. By continuity, the limting circuits in Fig. 20 must also yield multiple d.c. solutions.

(if) If N has a degenerate connection, then any possible combination of

short circuits and/or open circuits for the resistors would result in (1) some open ports, or (2) some shorted ports, or (3) transistor (or transformer) ports forming a loop. Figure A.13 lists all possible structures of circuits having a degenerate connection (with independent source eliminated).

Note that N_{R_1} and N_{R_2} in Fig. A.13 are made of linear positive 2-terminal resistors. The three circuits in Figs. A.13(b), (c), and (d) behave in an identical way because no current flows in the wire connecting the two subcircuits. Hence, they can be reduced to the equivalent circuit shown in Fig. A.14(b) where R is the input resistance looking into N_{R_2} and n is the turns ratio. Figure A.13(a) can be reduced to the equivalent circuit shown in Fig. A.14(a), as proved in Appendix C.8, where $R_x \geq 0$.

Since one branch of each transformer in Fig. A.14 becomes floating and therefore has no effect on the d.c. solution, they can be eliminated without changing the solution. Since the remaining circuit consists of a single transistor and linear positive 2-terminal resistors, it must have a unique solution. □

The one-port to the left of AA' in Fig. A.13(a) can be reduced to the equivalent one-port to the left of AA' in Fig. A.14(a).

Proof: Assume the resistive two-port N_{R_2} in Fig. A.13(a) has a hybrid representation

$$\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ -h_{12} & h_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix} \tag{A.34}$$

Since

$$v_1 = v_x,\ v_2 = nV_x,\ \text{and}\ i_x - i_1 = ni_2, \tag{A.35}$$

combining Eqs. (A.34) and (A.35), we obtain

$$R_x = \frac{v_x}{i_x} = \frac{h_{22}}{h_{11}h_{22}+(h_{12}+n)^2} \geq 0. \qquad \square$$

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Figure Captions

Fig. 1. Four types of driving-point v-i characteristics exhibited by two-transistor one-ports: (a) Monotone-Increasing; (b) Multivalued; (c) Type-S; (d) Type-N.

Fig. 2. Circuit for Example 1.

Fig. 3. The inclusion of the source resistance R prevents the feedback structure from being destroyed.

Fig. 4. Circuit for Example 2.

Fig. 5. Circuit for Example 3.

Fig. 6. Adding a resistor (b) in parallel or (c) in series with the feedback structure.

Fig. 7. (a) A two-transistor one-port for Example 4; (b) Feedback structure for (a); (c) v-i curve for R_1 = 100, 200, and 400, R_2 = 10k, and R_3 = 300; (d) v-i curve for R_1 = 200, R_2 = 5k, 10k, and 20k, and R_3 = 300; (e) v-i curve for R_1 = 200, R_2 = 10k, and R_3 = 300, 1k, and 5k.

Fig. 8. (a) A two-transistor one-port for Example 5; (b) Feedback structure for (a); (c) v-i curve for R_1 = 100, 200, and 400 and R_2 = 10k, R_3 = 300, and R_4 = 2k; (d) v-i curve for R_1 = 200, R_2 = 5k, 10k, and 20k, R_3 = 300, and R_4 = 10k; (e) v-i curve for R_1 = 200, R_2 = 10k, R_3 = 300, 1k, and 5k, and R_4 = 5k; (f) v-i curve for R_1 = 200, R_2 = 10k, R_3 = 300, and R_4 = 5k, 10k, and 15k.

Fig. 9. (a) One-port N in series with a positive resistor to form a composite one-port N'. (b) The v-i curve of N' tends to be monotone-increasing for larger R if N exhibits type-S v-i curve. (c) The v-i curve of N' tends to be multivalued for larger R if N exhibits type-N v-i curve. (d) One-port N in parallel with a positive resistor to form a composite one-port N'. (e) The v-i curve of N' tends to be multivalued for smaller R if N exhibits type-S v-i curve. (f) The v-i curve of N' tends to be monotone-increasing for smaller R if N exhibits type-N v-i curve.

Fig. 10. (a) Operating regions in a type-S characteristic. (b) Operating regions in a type-N characteristic.

Fig. 11. (a) A two-transistor one-port for Example 6; (b) v-i curve for R_1 = 12k, 15k, and 30k, R_2 = 100k, R_3 = 2k, R_4 = 20k, and R_5 = 1k; (c) v-i curve for R_1 = 15k, R_2 = 40k, 100k, and 120k, R_3 = 2k, R_4 = 20k, and R_5 = 1k; (d) v-i curve for R_1 = 15k, R_2 = 100k, R_3 = 1k, 2k, and 2.5k, R_4 = 20k, and R_5 = 1k; (e) v-i curve for R_1 = 15k, R_2 = 100k, R_3 = 2k, R_4 = 15k,

20k, and 50k, and R_5 = 1k; (f) v-i curve for R_1 = 15k, R_2 = 100k, R_3 = 2k, R_4 = 20k, and R_5 = 300, 1k, and 1.5k.

Fig. 12. (a) A two-transistor one-port for Example 7; (b) v-i curve for R_1 = 200k, 500k, and 5M, R_2 = 200k, R_3 = 100, and R_4 = 10k; (c) v-i curve for R_1 = 200k, R_2 = 5k, 20k, and 100k, R_3 = 100, and R_4 = 10k; (d) v-i curve for R_1 = 200k, R_2 = 20k, R_3 = 100, 1k, and 5k, and R_4 = 10k; (e) v-i curve for R_1 = 200k, R_2 = 20k, R_3 = 100, and R_4 = 200, 3k, and 10k.

Fig. 13. Counterexample to Conjecture 1.

Fig. 14. Three possible connections for a feedback structure; (a) two collectors are connected together; (b) one collector and one emitter are connected together; (c) two emitters are connected together.

Fig. 15. Two one-ports which differ only in an interchange between the collector and the emitter terminal in transistor T_2.

Fig. 16. An example demonstrating little changes in the bias condition due to an interchange between the collector and the emitter of one transistor.

Fig. 17. General configuration of single-transistor circuits containing linear passive reciprocal two-ports.

Fig. 18. Circuits with a nondegenerate connection; in addition to eliminating the independent sources, (b) is obtained by short-circuiting R_1 and open-circuiting R_2 from (a); (d) is obtained by short-circuiting R_1 and open-circuiting R_2 from (c).

Fig. 19. (a) Circuit with a degenerate connection; (b) when the independent voltage source is short-circuited, L_1 is open circuited, and J_1 and J_2 form a loop upon open-circuiting R_1 and R_2; (c) L_1 is open-circuited and J_1 is short-circuited upon open-circuiting R_1 and short-circuiting R_2; (d) L_1 and L_2 form a loop, and J_1 and J_2 form a loop upon short-circuiting R_1 and open-circuiting R_2; (e) L_1 and L_2 form a loop and J_1 is short-circuited upon short-circuiting R_1 and R_2.

Fig. 20. Three fundamental structures for nondegenerate connection circuits; (a) common-base configuration; (b) common-emitter (or collector) configuration with $n > 0$; (c) common-emitter (or collector) configuration with opposite dot direction and $n > 1$.

Fig. 21. (a) A one-transistor one-port circuit for Example 9; (b) v-i curve for R_1 = 100, 1k, and 10k, R_2 = 50k, R_3 = 8k, and n = 10; (c) v-i curve for R_1 = 1k, R_2 = 10k, 50k, and 200k, R_3 = 8k, and n = 10; (d) v-i curve for R_1 = 1k, R_2 = 50k, R_3 = 1k, 8k, and 30k, and n = 10; (e) v-i curve for R_1 = 1k, R_2 = 50k, R_3 = 8k, and n = 5, 10, and 20.

Tables

Ohm						Volt			
R_1	R_2	R_3	R_4	R_5	R_6	V_{BE_1}	V_{BC_1}	V_{BE_2}	V_{BC_2}
1k	1k	100	10k	10k	50k	0.628	-0.499	0.672	-0.631
100	1k	100	10k	10k	50k	0	-0.18	0.676	-1.873
1k	10k	100	10k	10k	50k	0.582	0.156	0.665	-0.884
1k	1k	1k	10k	10k	50k	0	-1.392	0.667	0.544
1k	1k	100	1k	10k	50k	0	-2.025	0.676	-0.046
1k	1k	100	10k	100k	50k	0	-2.210	0.676	0.157
1k	1k	100	10k	10k	10k	0.666	0.264	0.688	0.029

Table A.1

Ohm						Volt			
R_1	R_2	R_3	R_4	R_5	R_6	V_{BE_1}	V_{BC_1}	V_{BE_2}	V_{BC_2}
10k	10k	100	100	100	10k	0.705	-0.43	0.677	-0.211
1k	10k	100	100	100	10k	0.705	-0.343	0.672	-0.028
10k	1k	100	100	100	10k	0.725	0.636	0.089	0.016
10k	10k	1k	100	100	10k	0.666	-0.072	0.637	-0.023
10k	10k	100	1k	100	10k	0.706	-0.593	0.66	0.572
10k	10k	100	100	1k	10k	0.683	0.605	0.077	0.004
10k	10k	100	100	100	1k	0.701	-0.091	0.696	0.4

Table A.2

Ohm					Volt			
R_1	R_2	R_3	R_4	R_5	V_{BE_1}	V_{BC_1}	V_{BE_2}	V_{BC_2}
1k	100	1k	100	10k	0.66	-0.086	0.639	-2.184
100	100	1k	100	10k	0.25	-0.25	0.499	-2.5
1k	10k	1k	100	10k	-0.412	-2.394	0.703	-1.645
1k	100	10k	100	10k	0.27	-0.027	0.297	-2.703
1k	100	1k	10k	10k	0.47	-0.143	0.594	-1.449
1k	100	1k	100	100	0.588	-0.133	0.706	-1.557

Table A.3

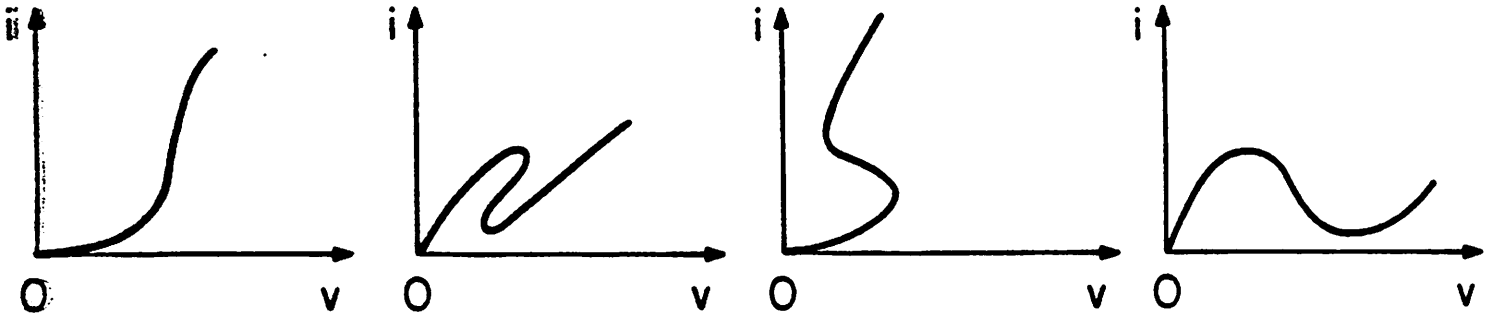


Fig. 1

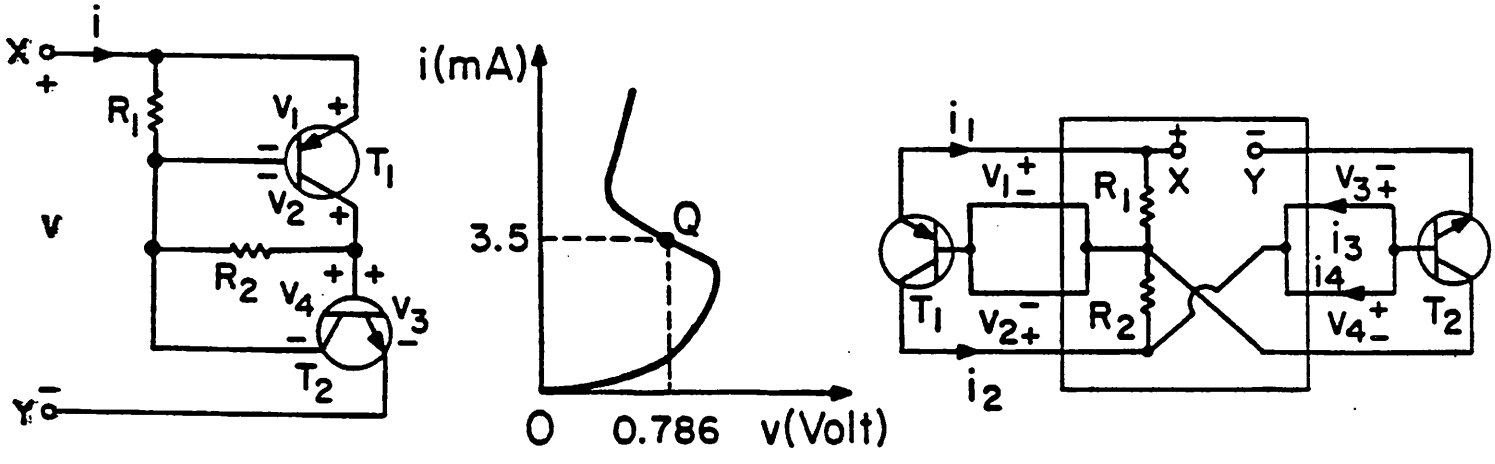


Fig. 2

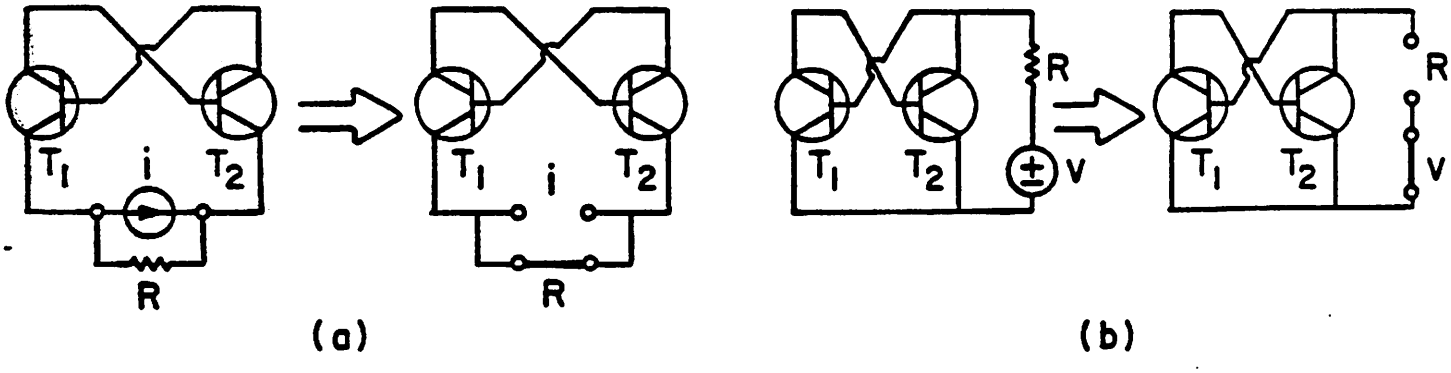


Fig. 3

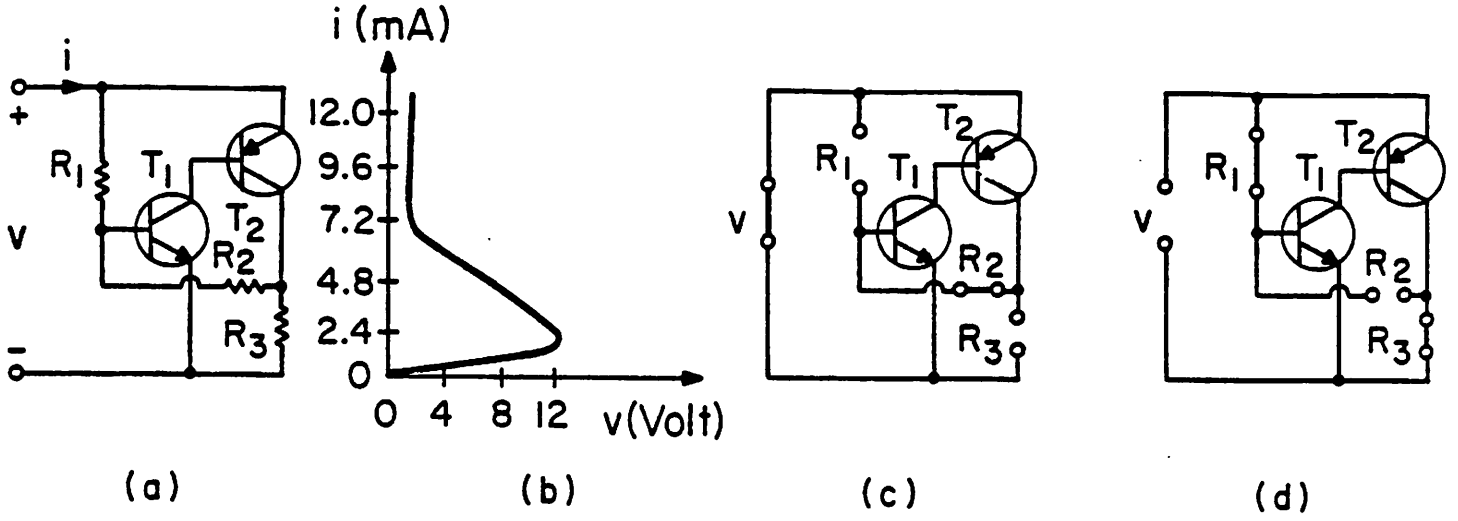


Fig. 4

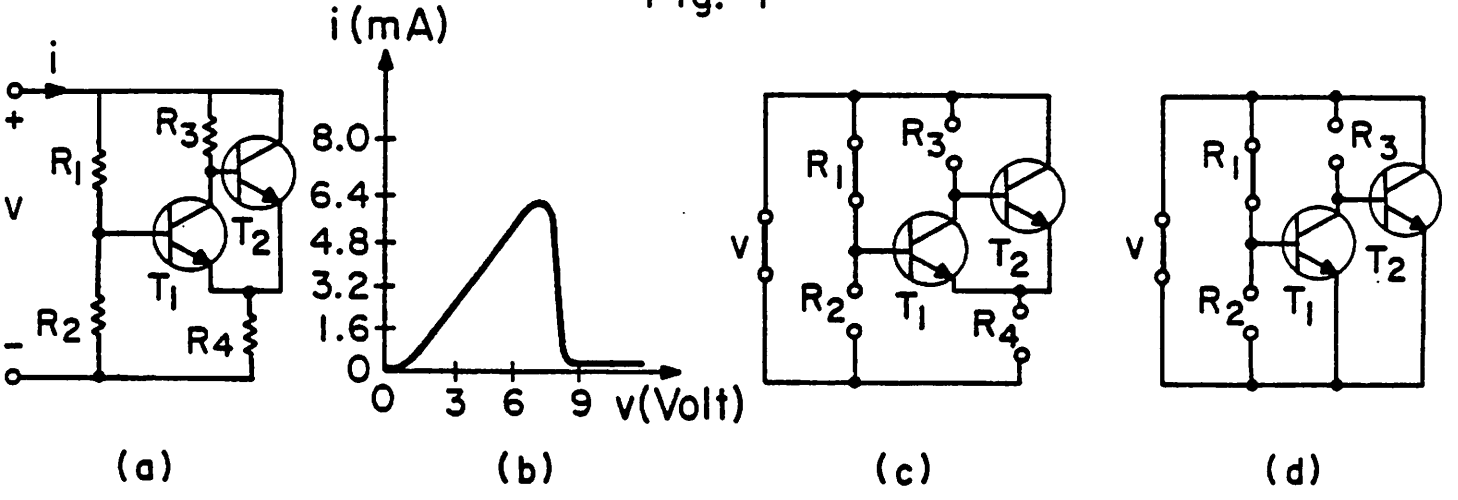


Fig. 5

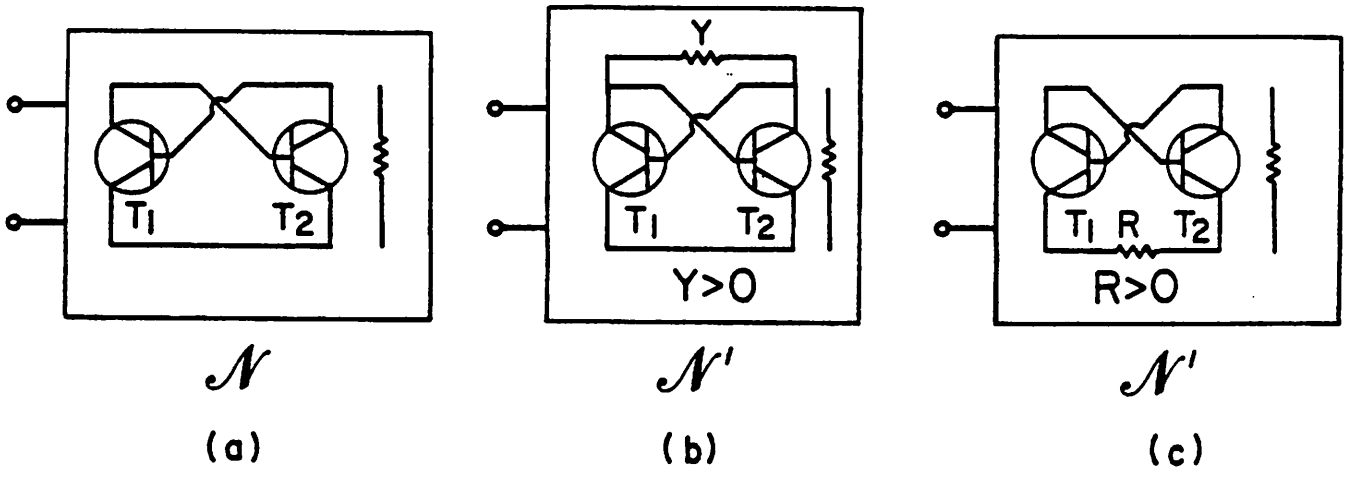


Fig. 6

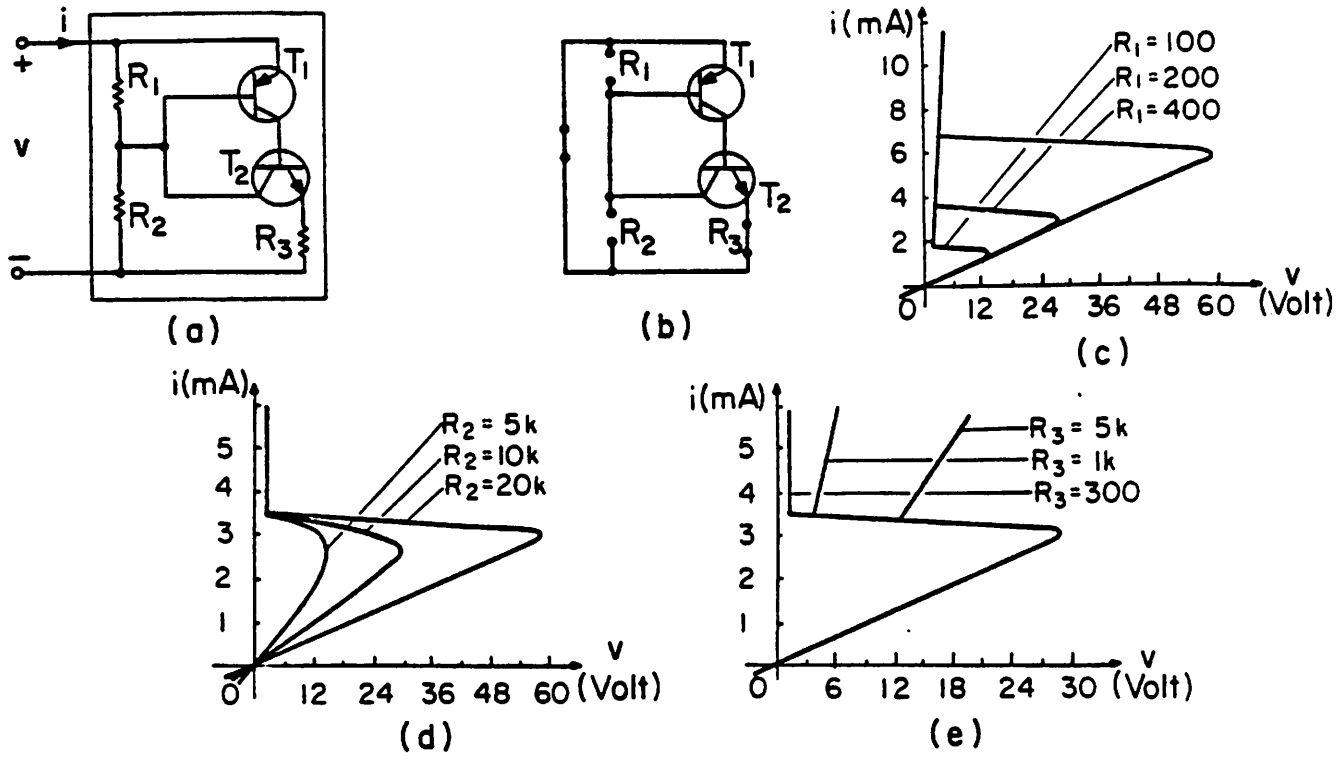

i
+
v
−
R1
T1
T2
R2
R3
(a)
(b)
i(mA)
R1 = 100
R1 = 200
R1 = 400
V (Volt)
(c)
R2 = 5k
R2 = 10k
R2 = 20k
(d)
R3 = 5k
R3 = 1k
R3 = 300
(e)

Fig. 7

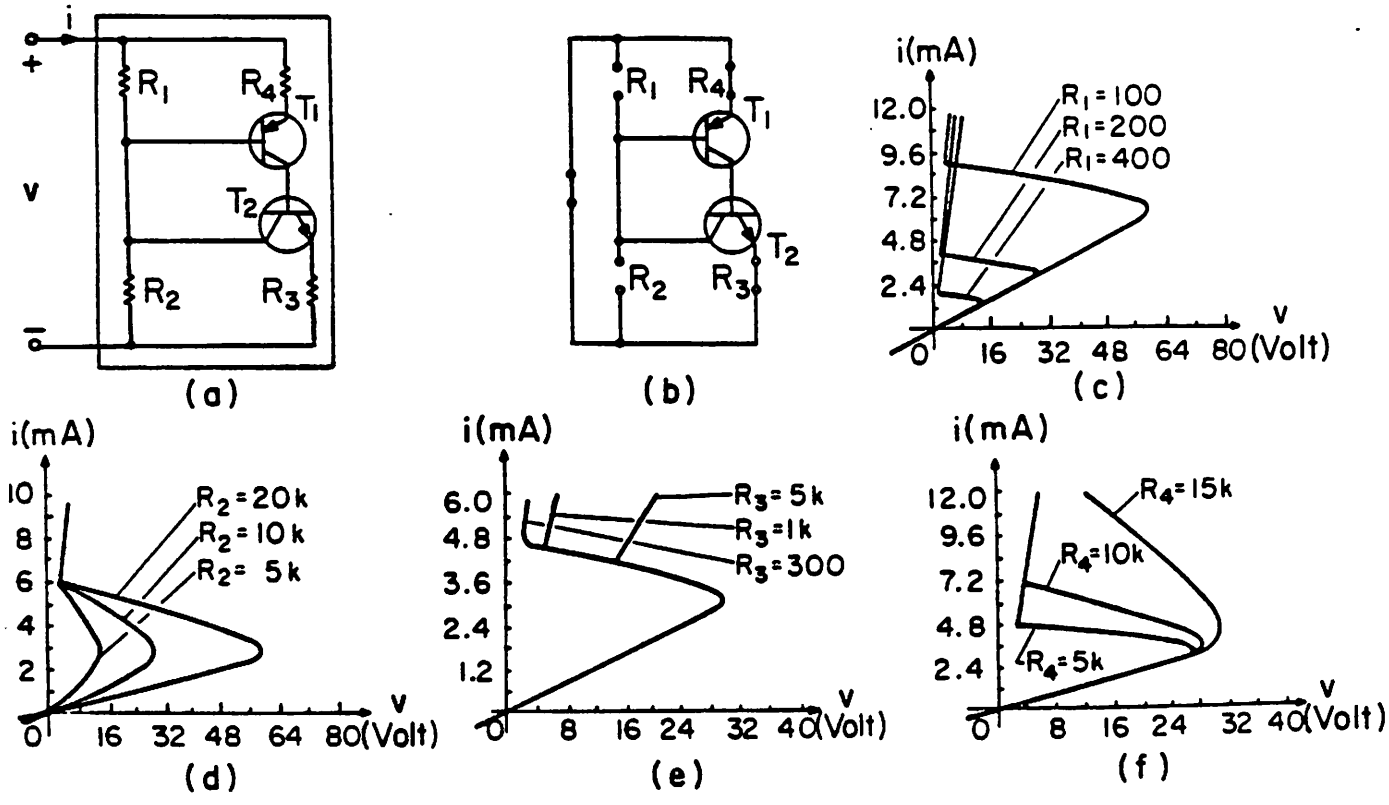
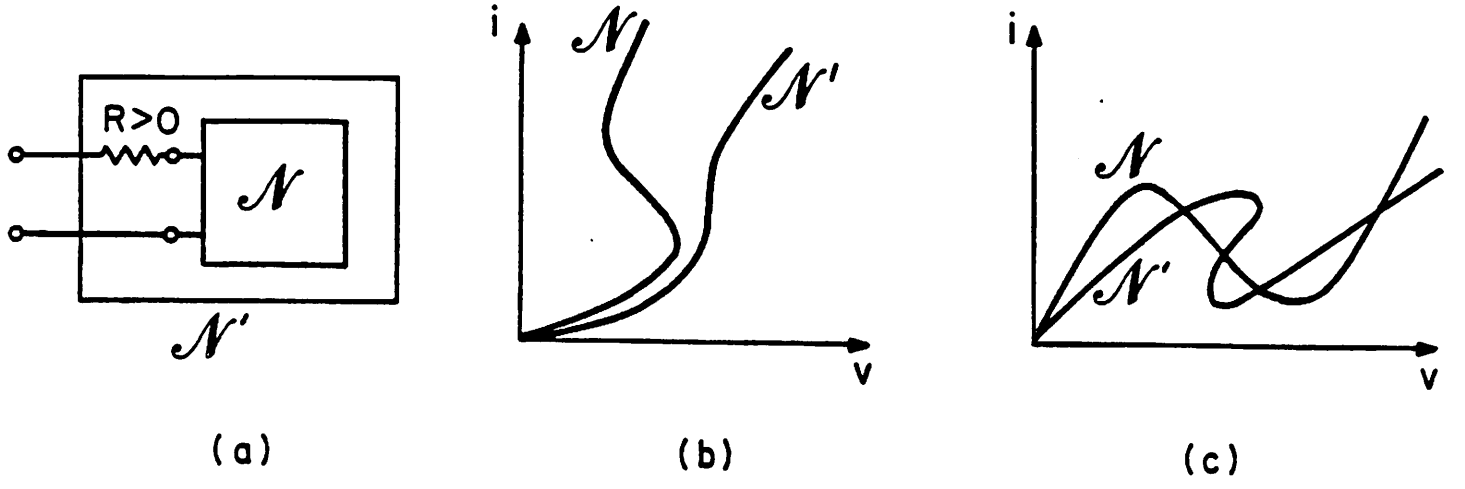

i
+
v
−
R1
R4
T1
T2
R2
R3
(a)
(b)
i(mA)
R1 = 100
R1 = 200
R1 = 400
V (Volt)
(c)
R2 = 20k
R2 = 10k
R2 = 5k
(d)
R3 = 5k
R3 = 1k
R3 = 300
(e)
R4 = 15k
R4 = 10k
R4 = 5k
(f)

Fig. 8


R>0
𝒩
𝒩'
i
v
(a)
(b)
(c)

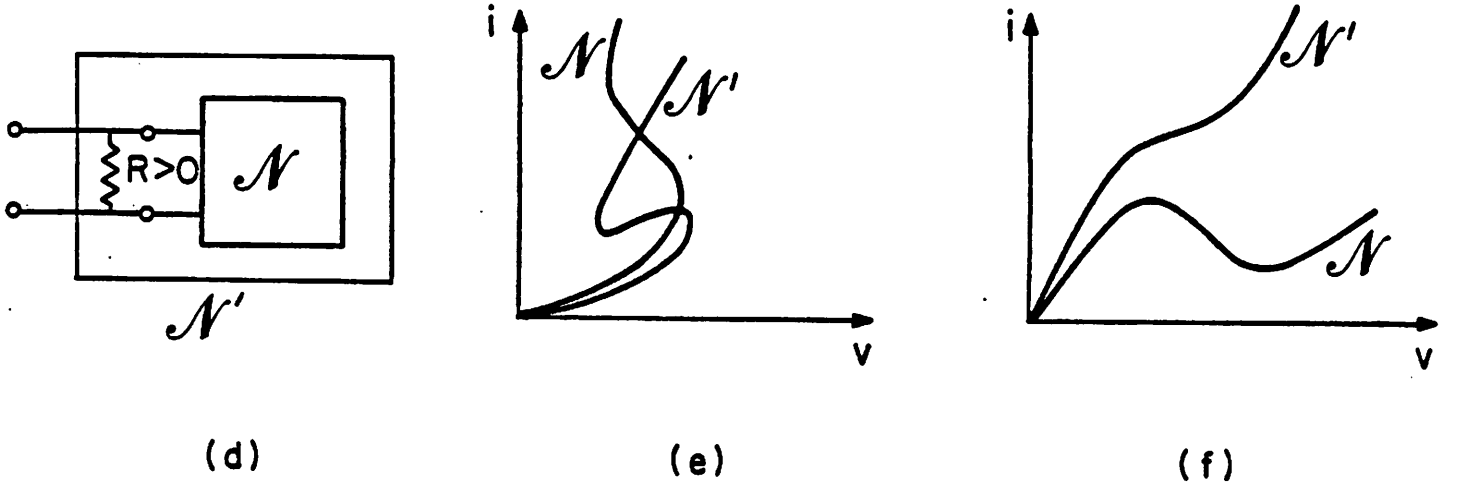

R>0
𝒩
𝒩'
i
v
(d)
(e)
(f)

Fig. 9

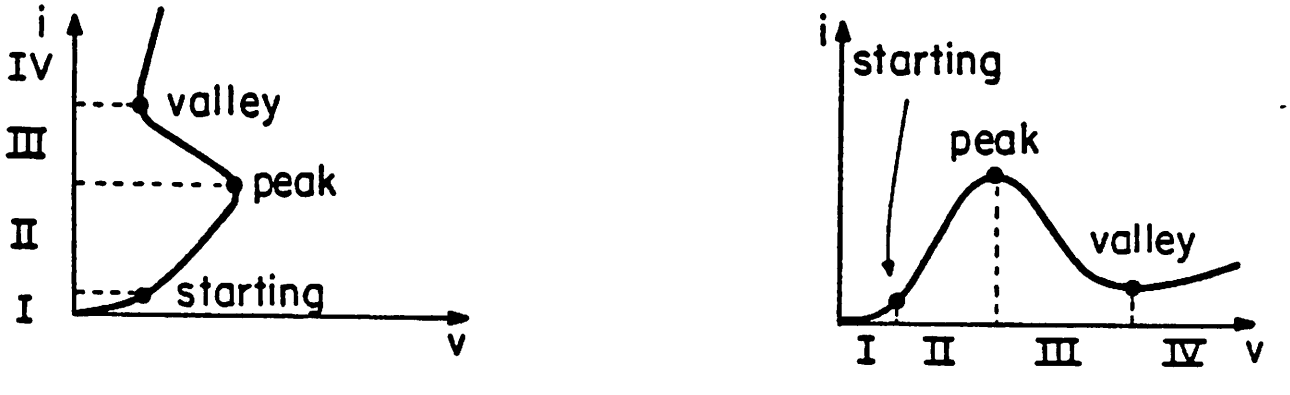

i
IV
III
II
I
valley
peak
starting
v
(a)
i
starting
peak
valley
I
II
III
IV
v
(b)

Fig. 10

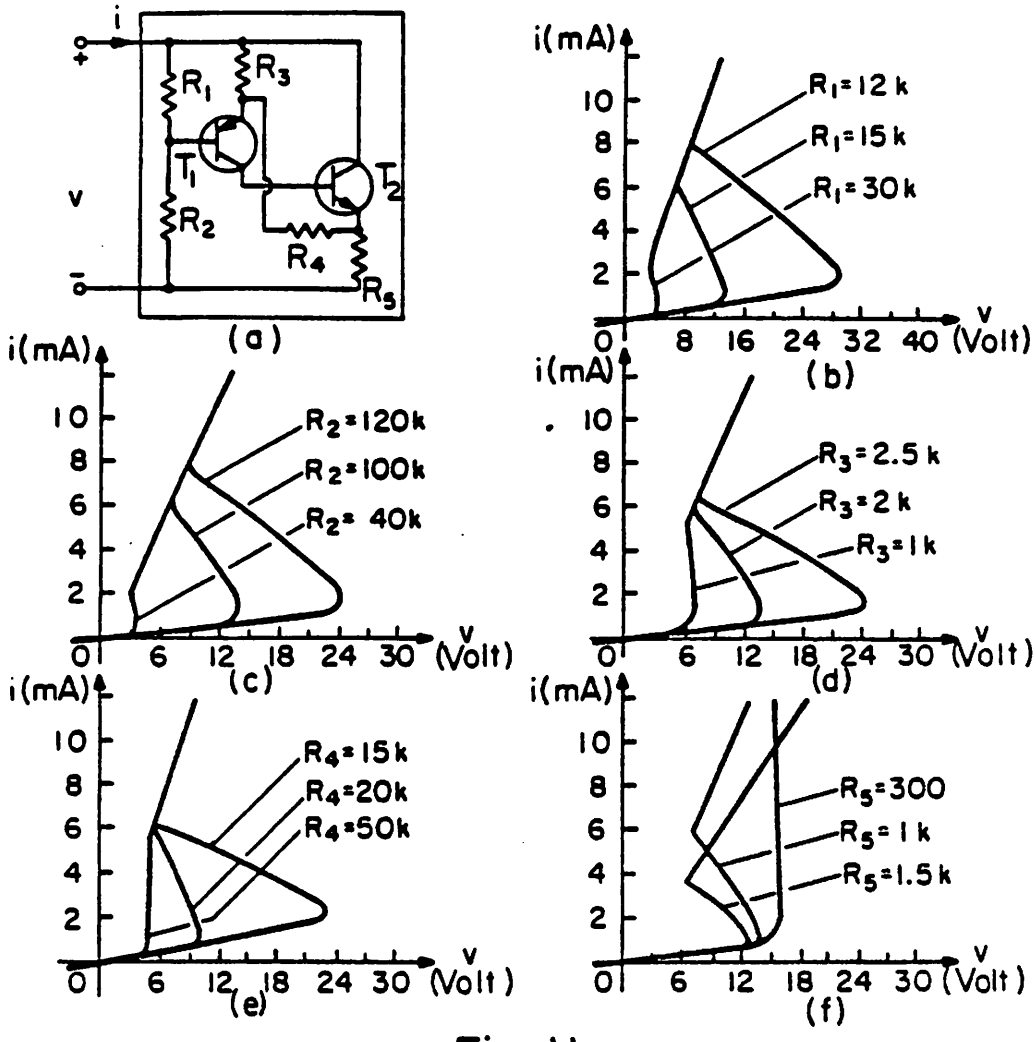

i
+
v
−
R1
R3
T1
T2
R2
R4
R5
(a)
i(mA)
R1=12 k
R1=15 k
R1=30 k
(b)
R2=120k
R2=100k
R2= 40k
(c)
R3=2.5 k
R3=2 k
R3=1 k
(d)
R4=15k
R4=20k
R4=50k
(e)
R5=300
R5= 1 k
R5=1.5 k
(f)
Volt

Fig. 11

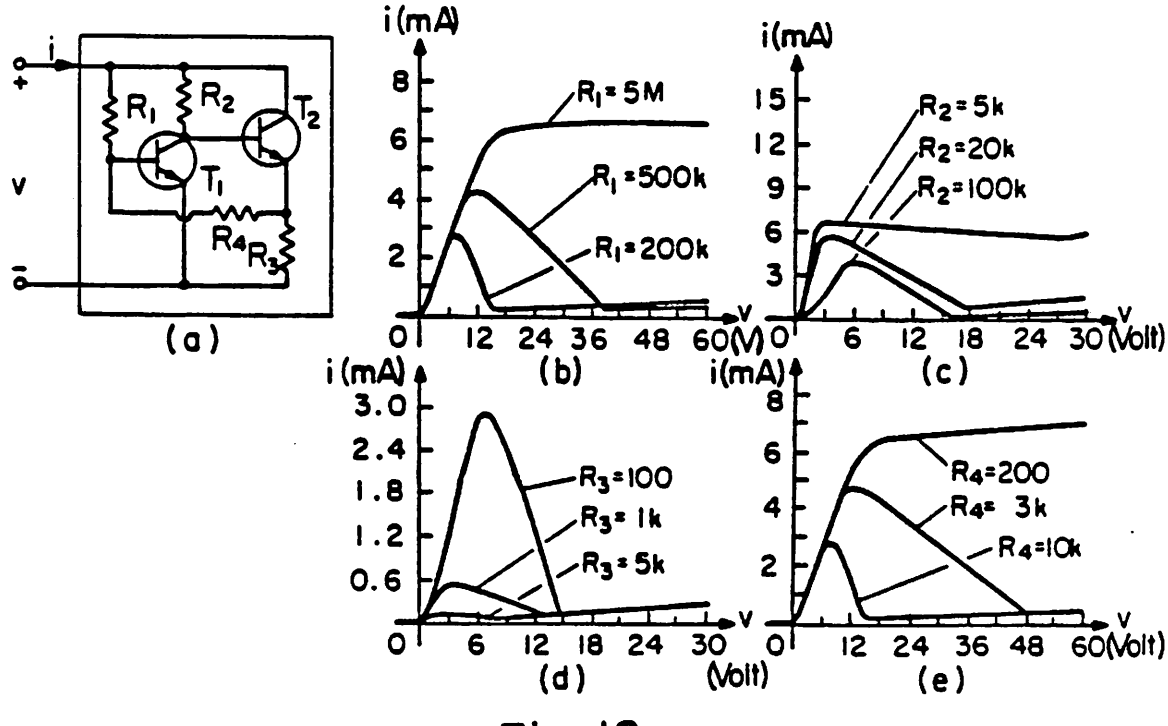

i
+
v
−
R1
R2
T2
T1
R4
R3
(a)
i(mA)
R1= 5M
R1=500k
R1=200k
(b)
R2= 5k
R2=20k
R2=100k
(c)
R3=100
R3= 1k
R3= 5k
(d)
R4=200
R4= 3k
R4=10k
(e)
Volt

Fig. 12

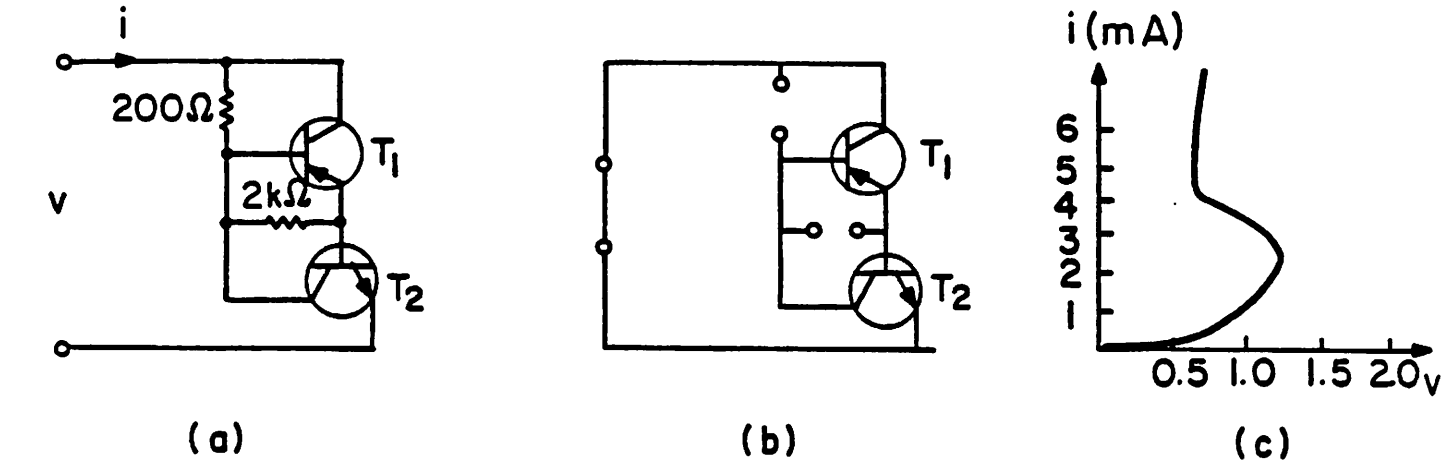


Fig. 13

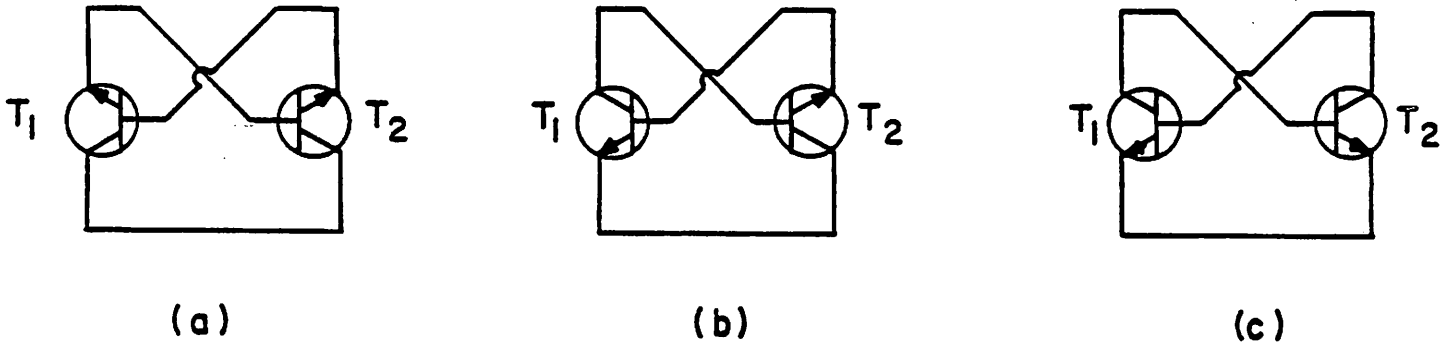


Fig. 14

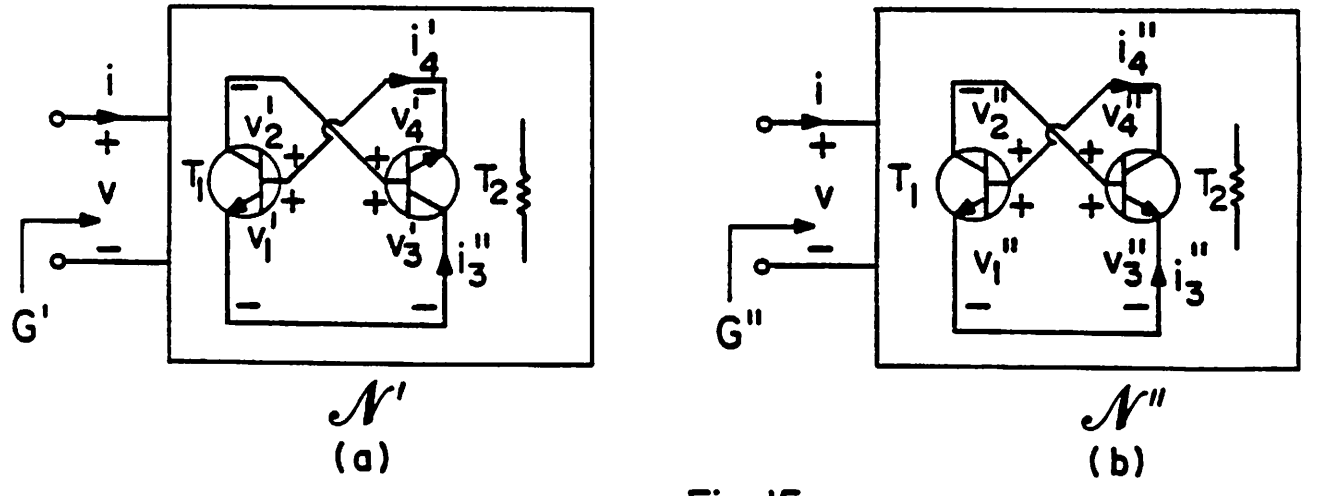
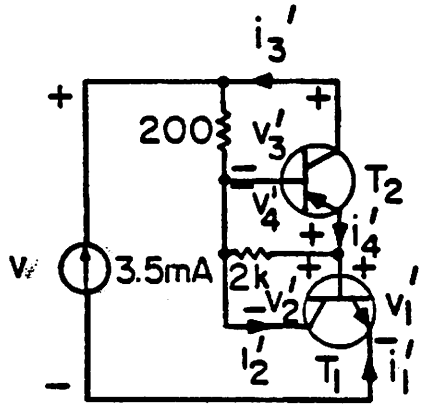
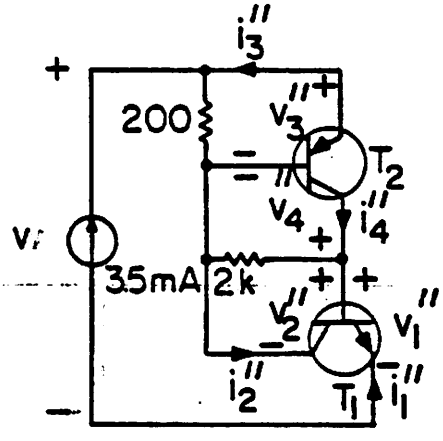


Fig. 15



(a)



(b)

	Q'(i=3.5mA,V=1.014V)	Q''(i=3.5mA,V=0.785V
v_1	0.687V	0.687V
v_2	0.288V	0.530V
v_3	0.615V	0.629V
v_4	0.288V	0.530V
i_1	-3.5mA	-3.5mA
i_2	3.43mA	3.42mA
i_3	-0.425mA	-0.357mA
i_4	0.213mA	0.342mA

(c)

Fig. 16

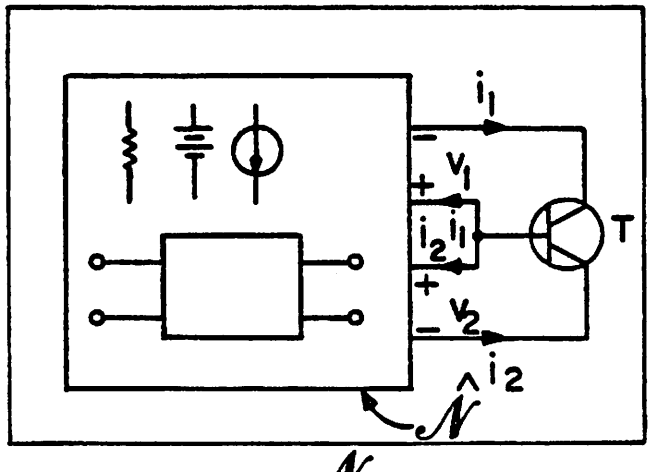


Fig. 17

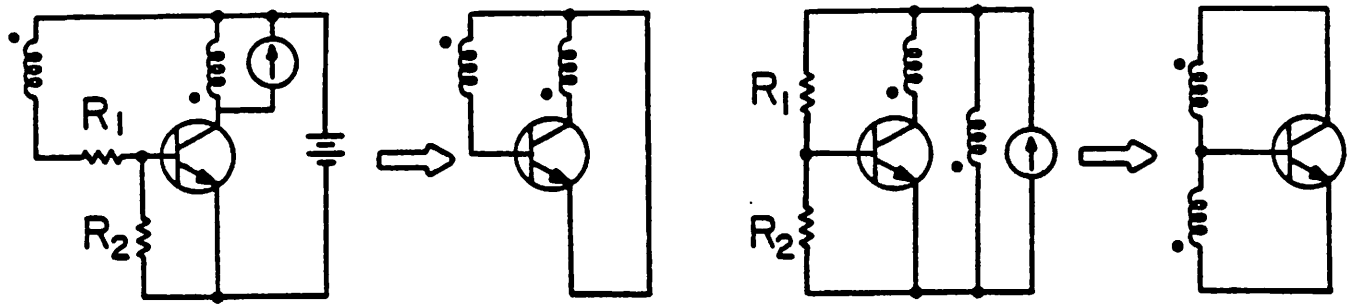


Fig. 18

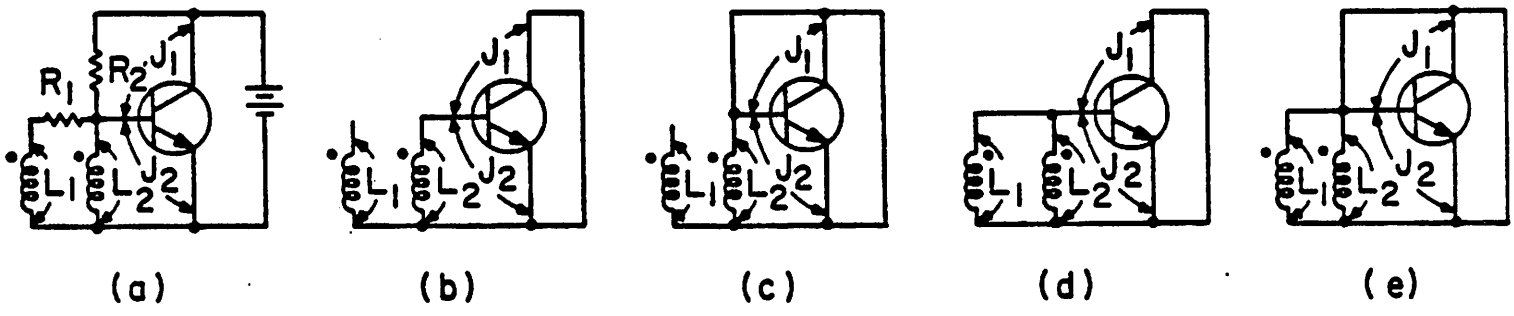


Fig. 19

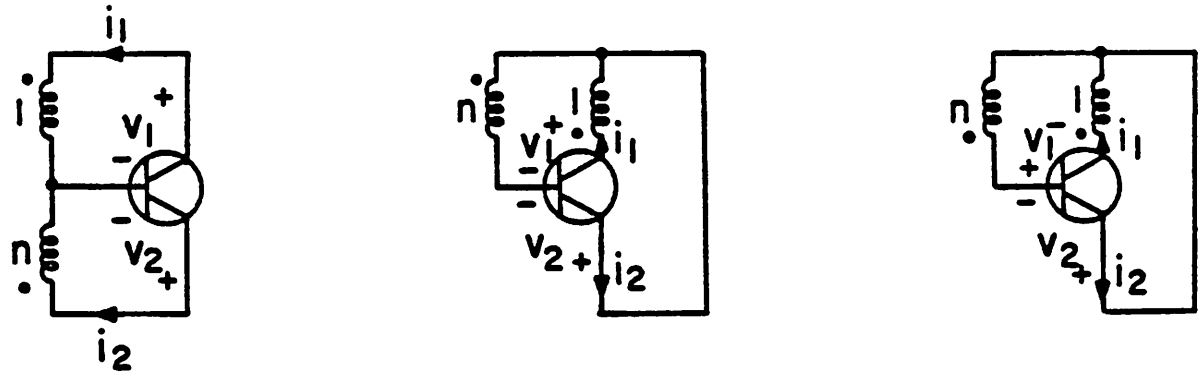


Fig. 20

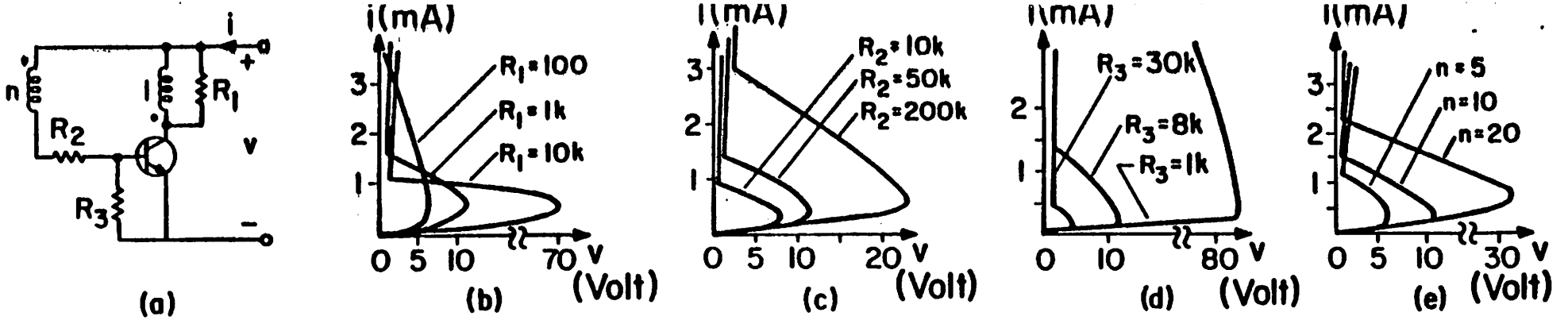


Fig. 21

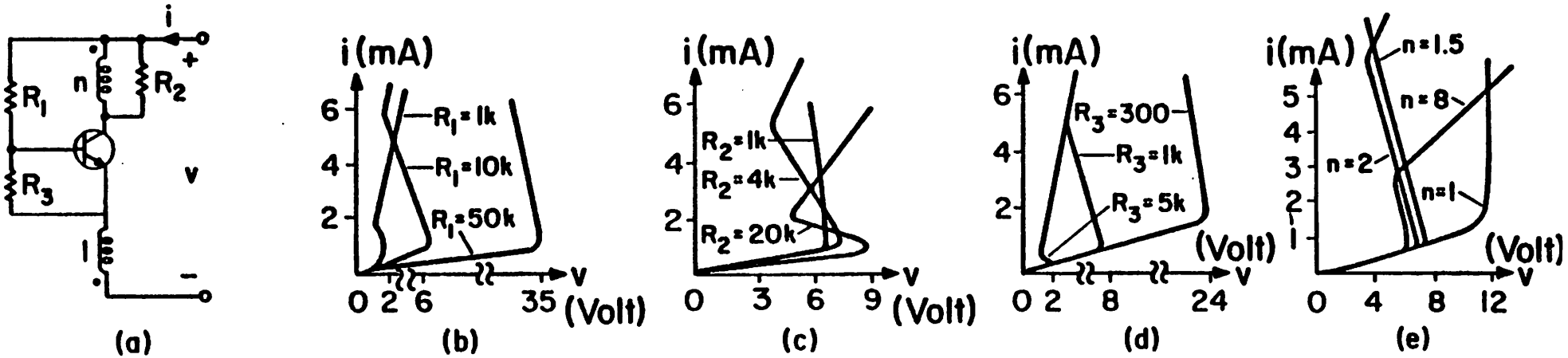


Fig. 22

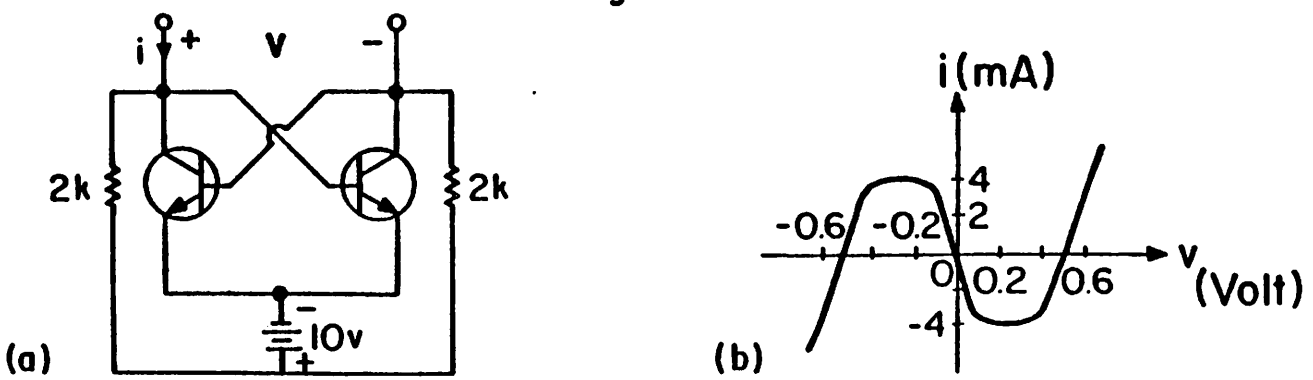
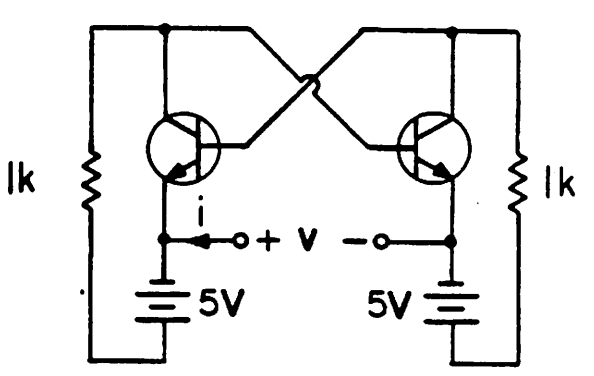
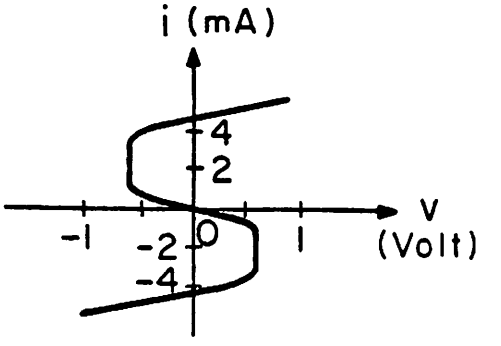


Fig. 23



(a)



(b)

Fig. 24

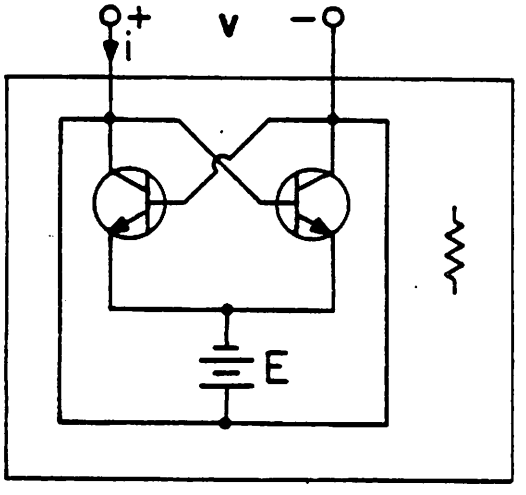


Fig. 25

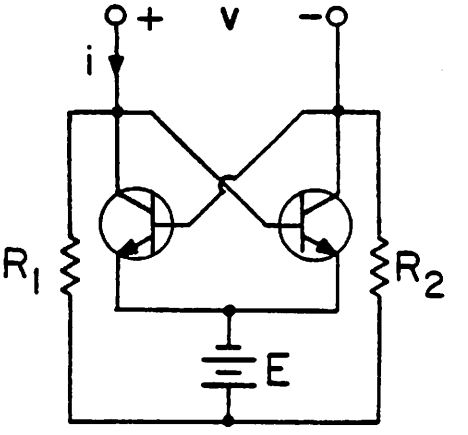
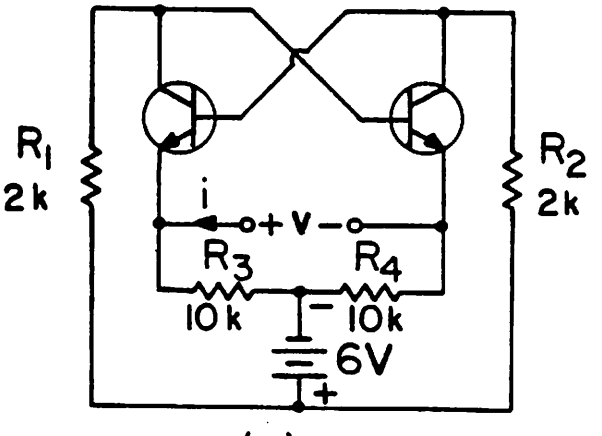
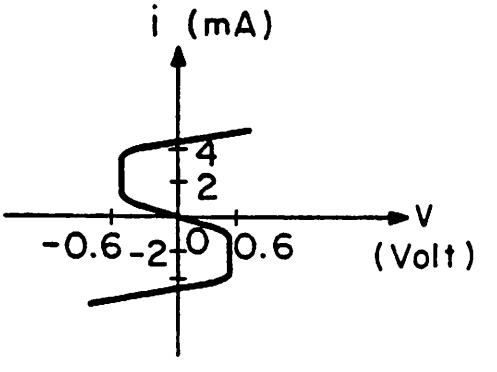


Fig. 26

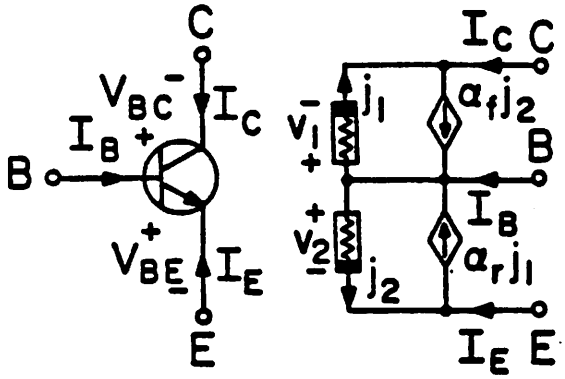


(a)

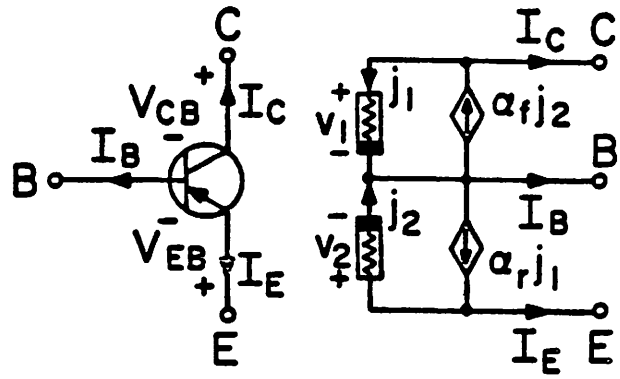


(b)

Fig. 27



(a)



(b)

Fig. A.1

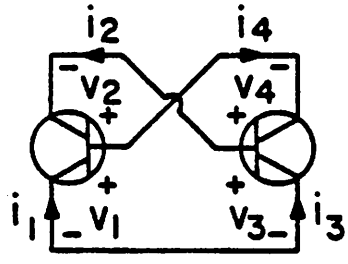


Fig. A.2

$\underset{\sim}{P}v = \underset{\sim}{Q}i + \underset{\sim}{r}$

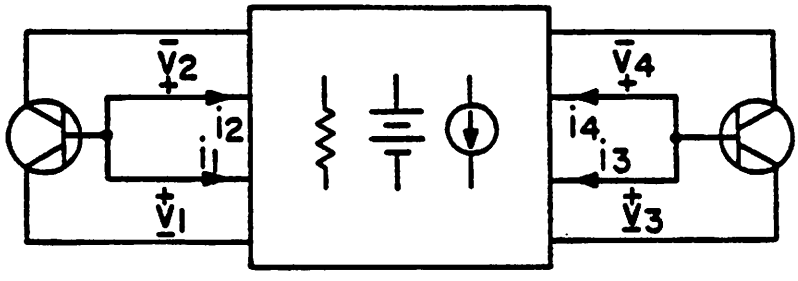
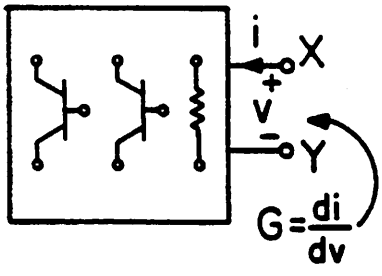
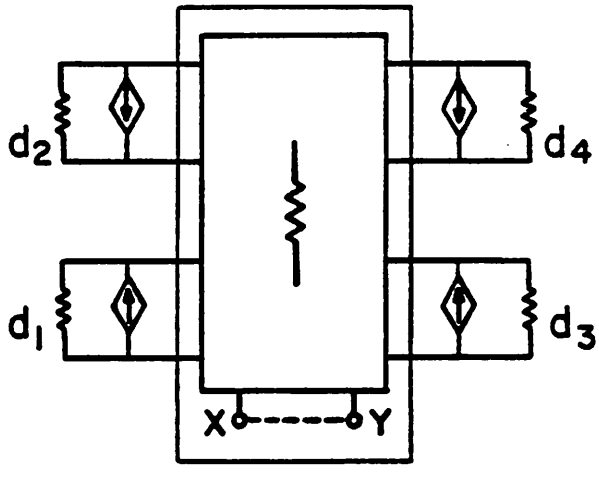


Fig. A.3



(a)

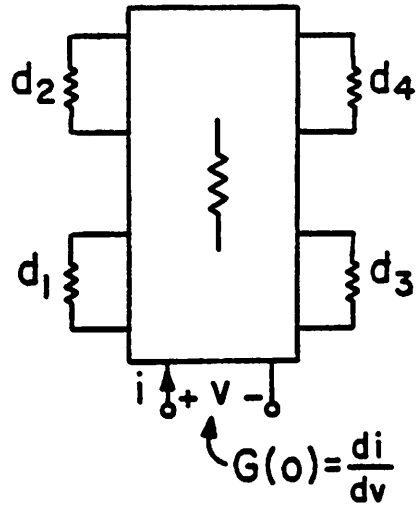


4-port equation is

$\underset{\sim}{P_o}v = \underset{\sim}{Q_o}i$ if X-Y is open

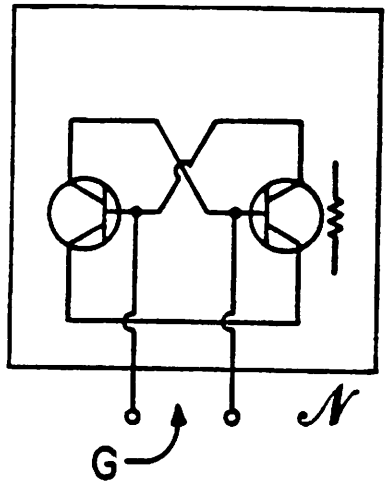
$\underset{\sim}{P_s}v = \underset{\sim}{Q_s}i$ if X-Y is shorted

(b)

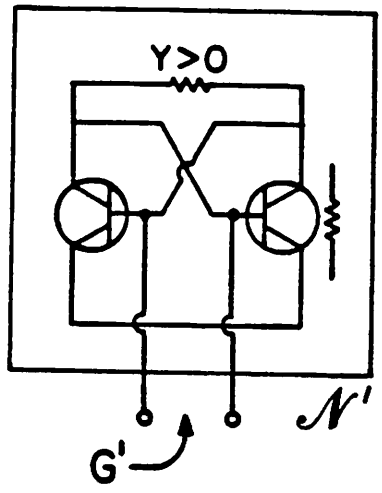


(c)

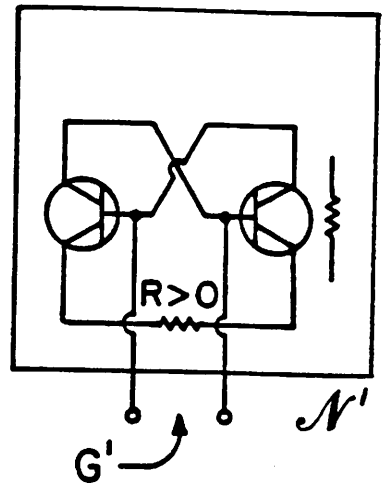
Fig. A.4



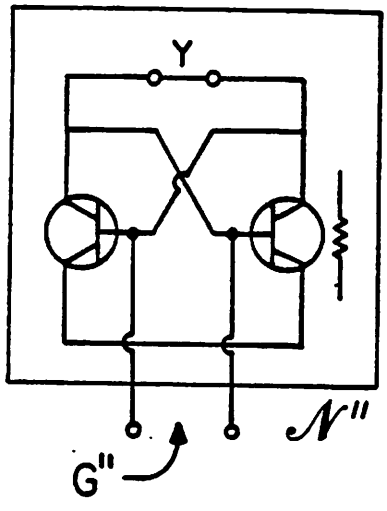
(a)



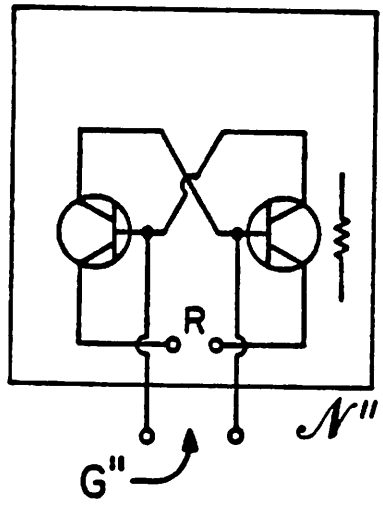
(b)



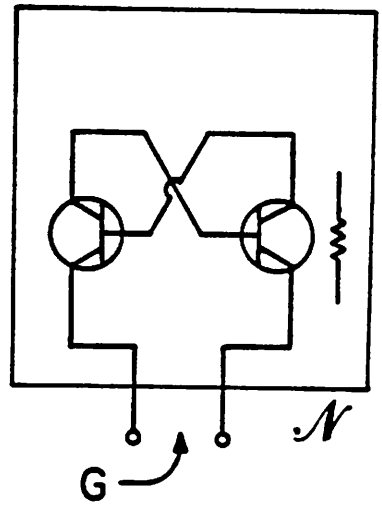
(c)



(d)

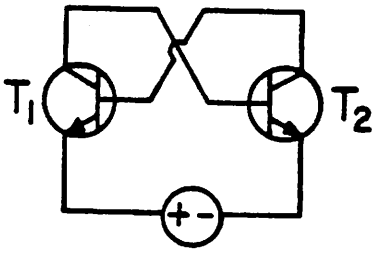


(e)

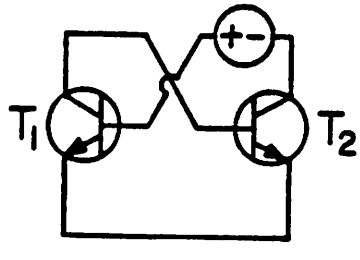


(f)

Fig. A.5



(a)



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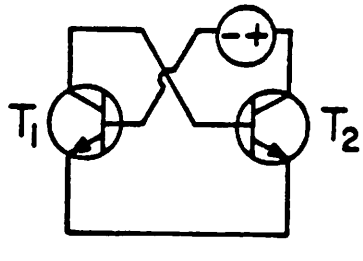


(c)

Fig. A.6

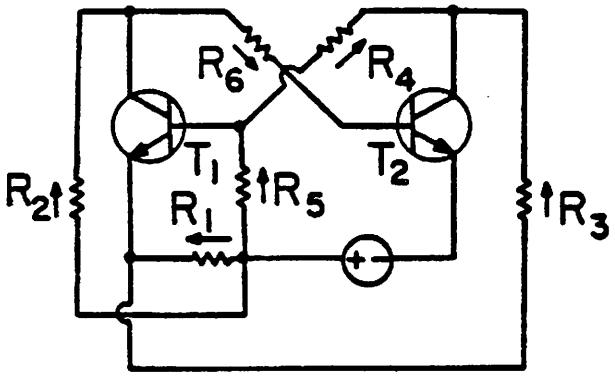


Fig. A.7

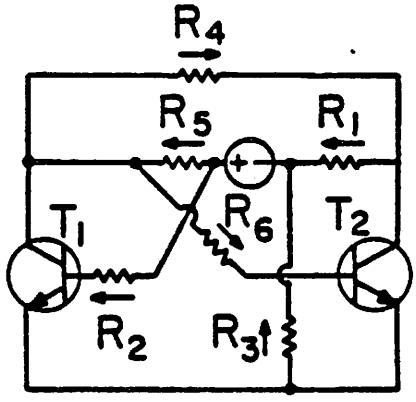


Fig. A.8

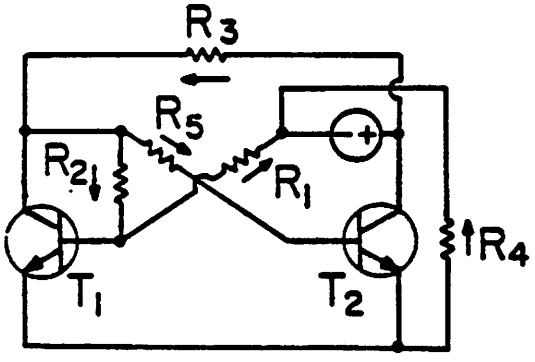
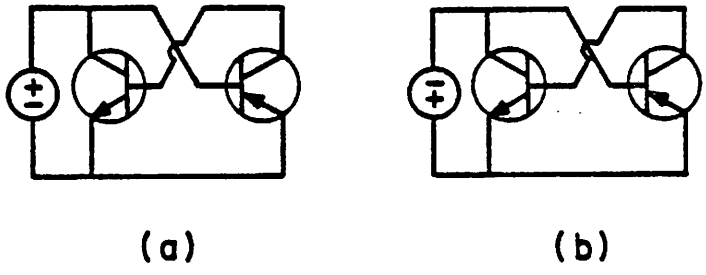


Fig. A.9



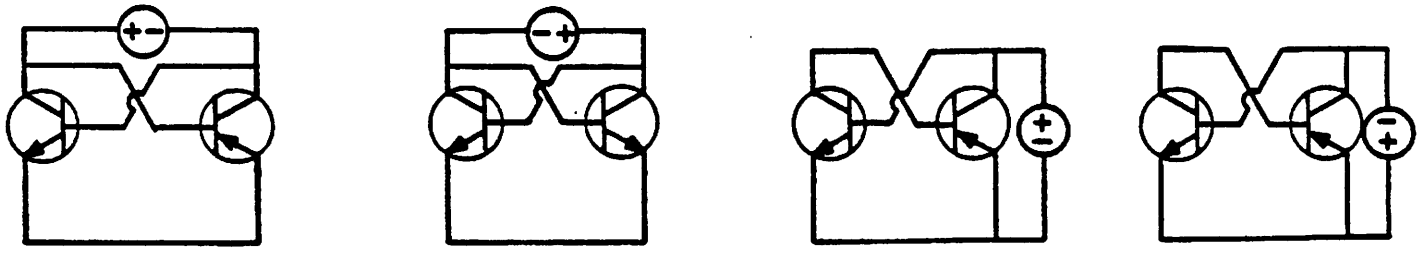


Fig. A.10

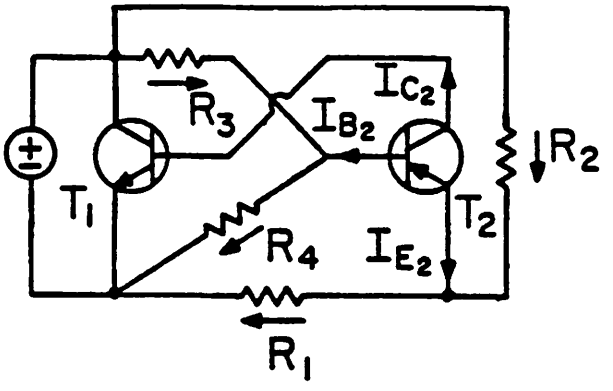


Fig. A.11

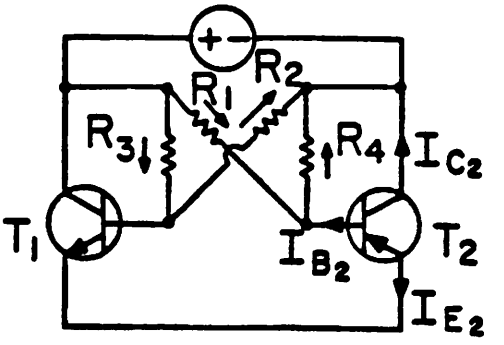
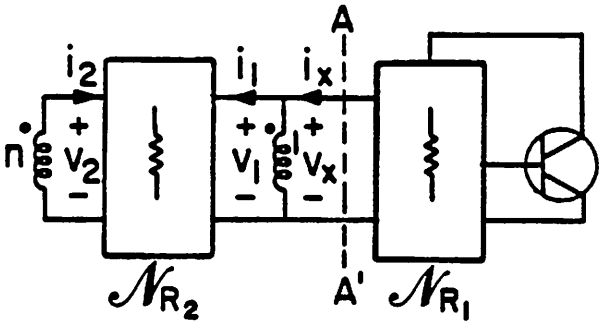
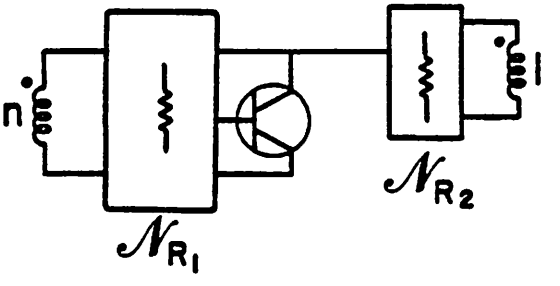


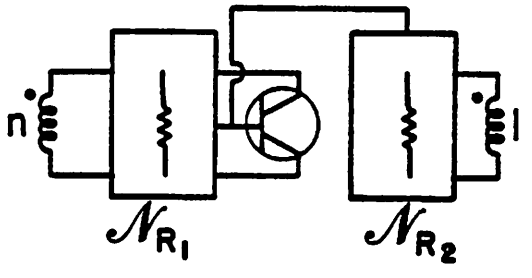
Fig. A.12



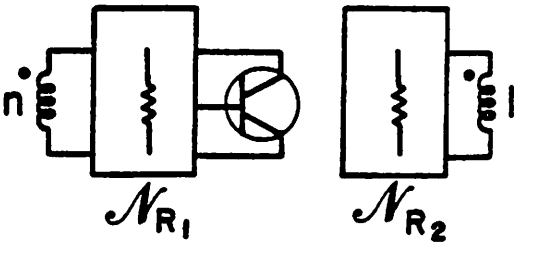
(a)



(b)

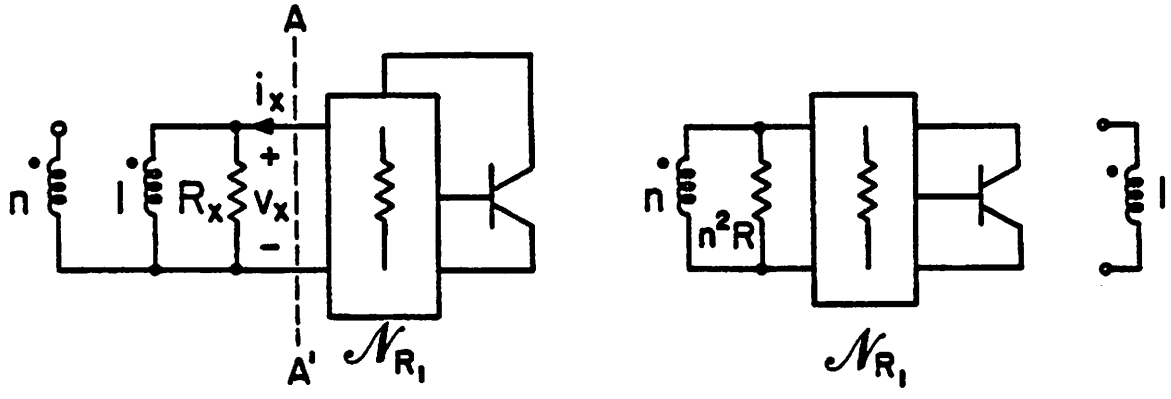


(c)



(d)

Fig. A.13



(a) (b)

Fig. A.14