BERKELEY CMOS PROCESS TEST PATTERNS

FROM EECS 290N and 2900

by

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ELECTRONICS RESEARCH LABORATORY

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BERKELEY CMOS PROCESS

TEST PATTERNS

Entire Catalog

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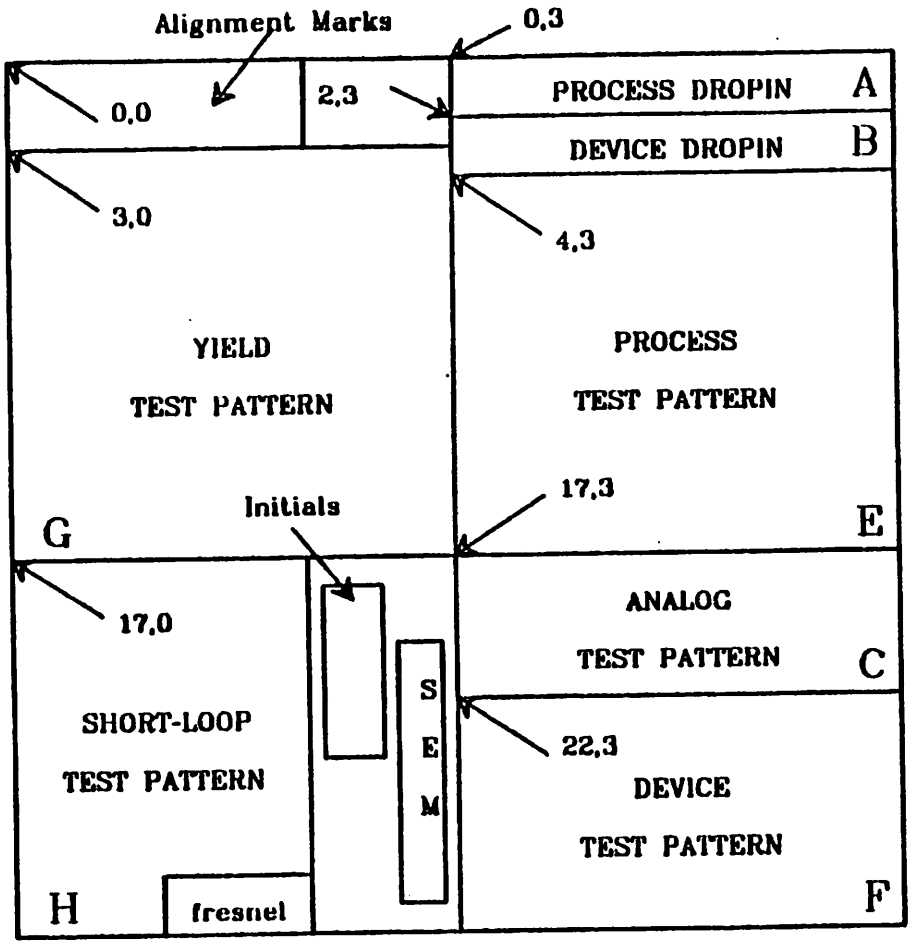
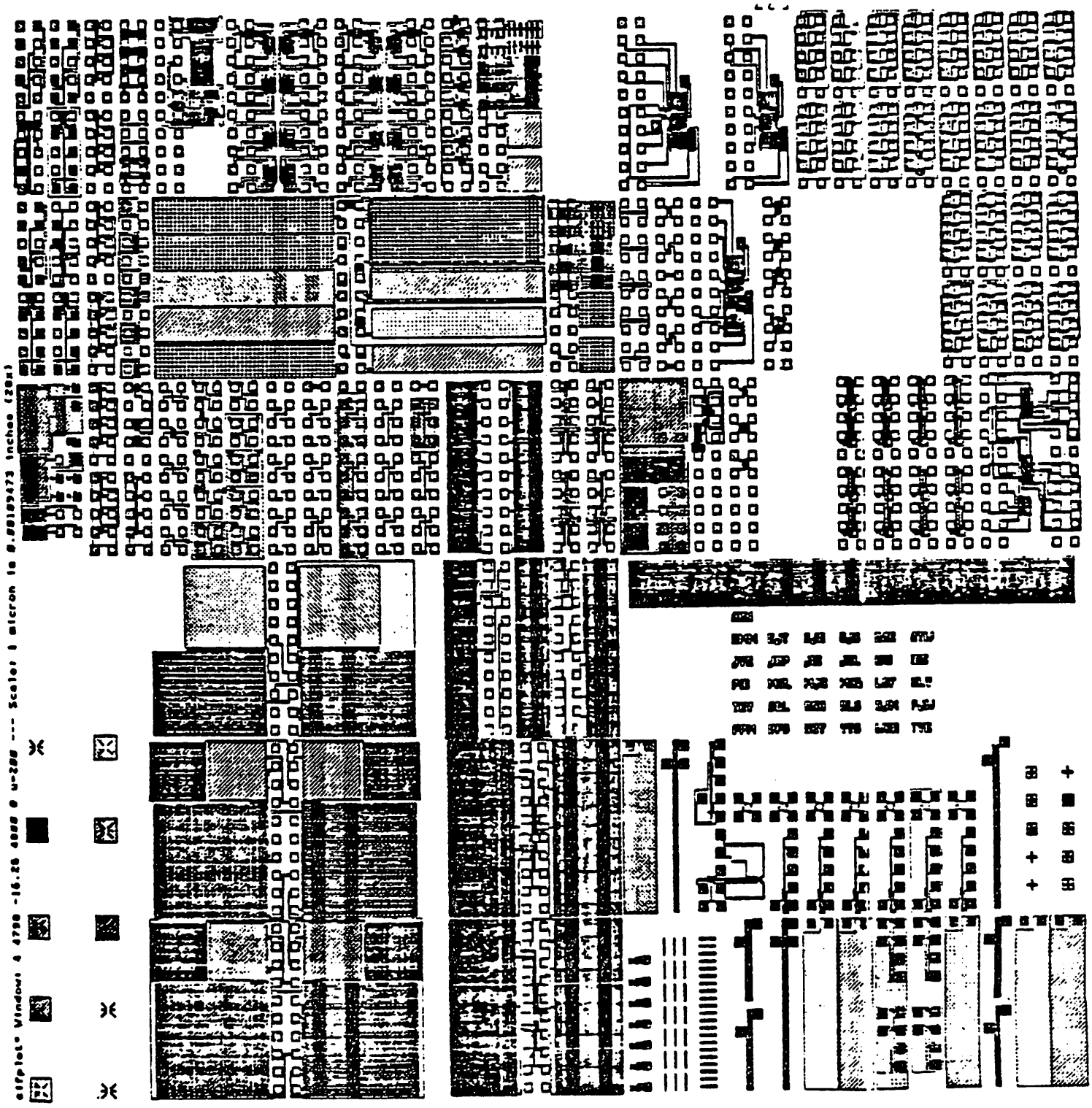
BERKELEY CMOS PROCESS TEST CHIP



testchip.cif

Entire EE290 Test Chip



290n-CMOS

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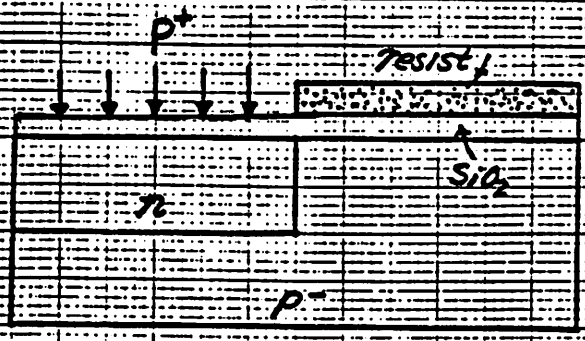

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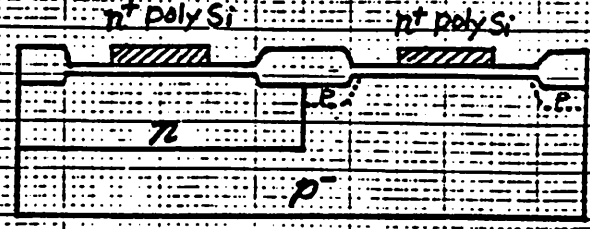

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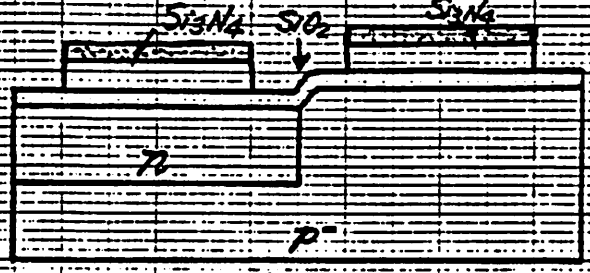

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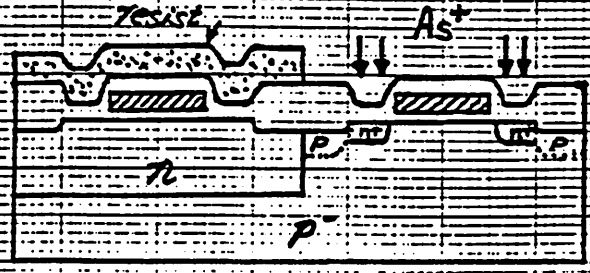

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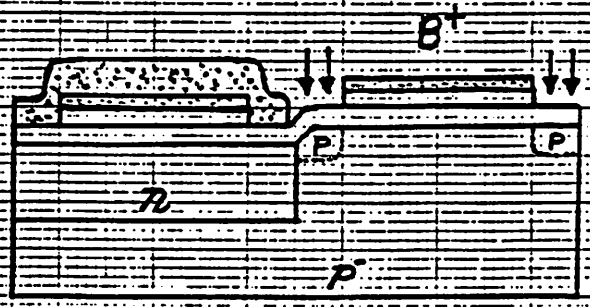

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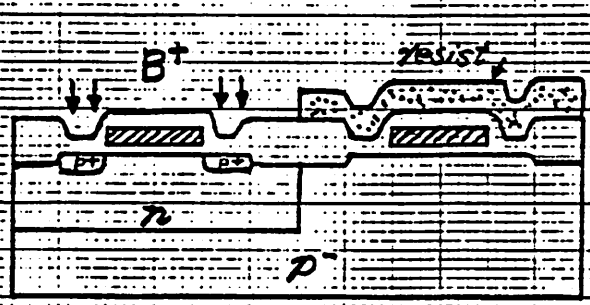

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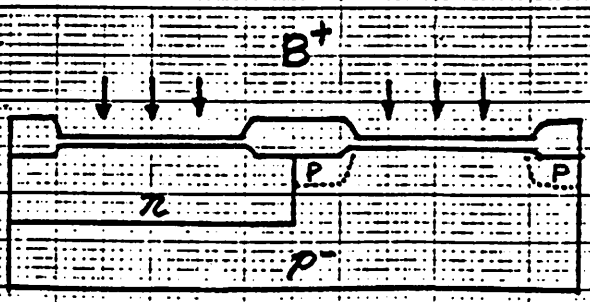

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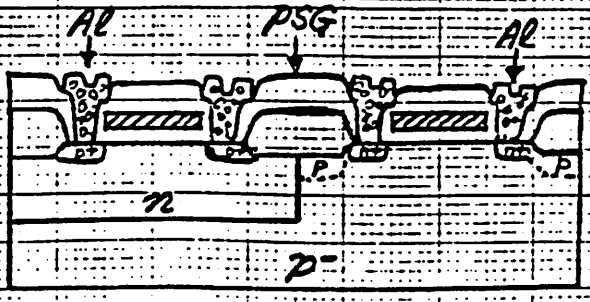

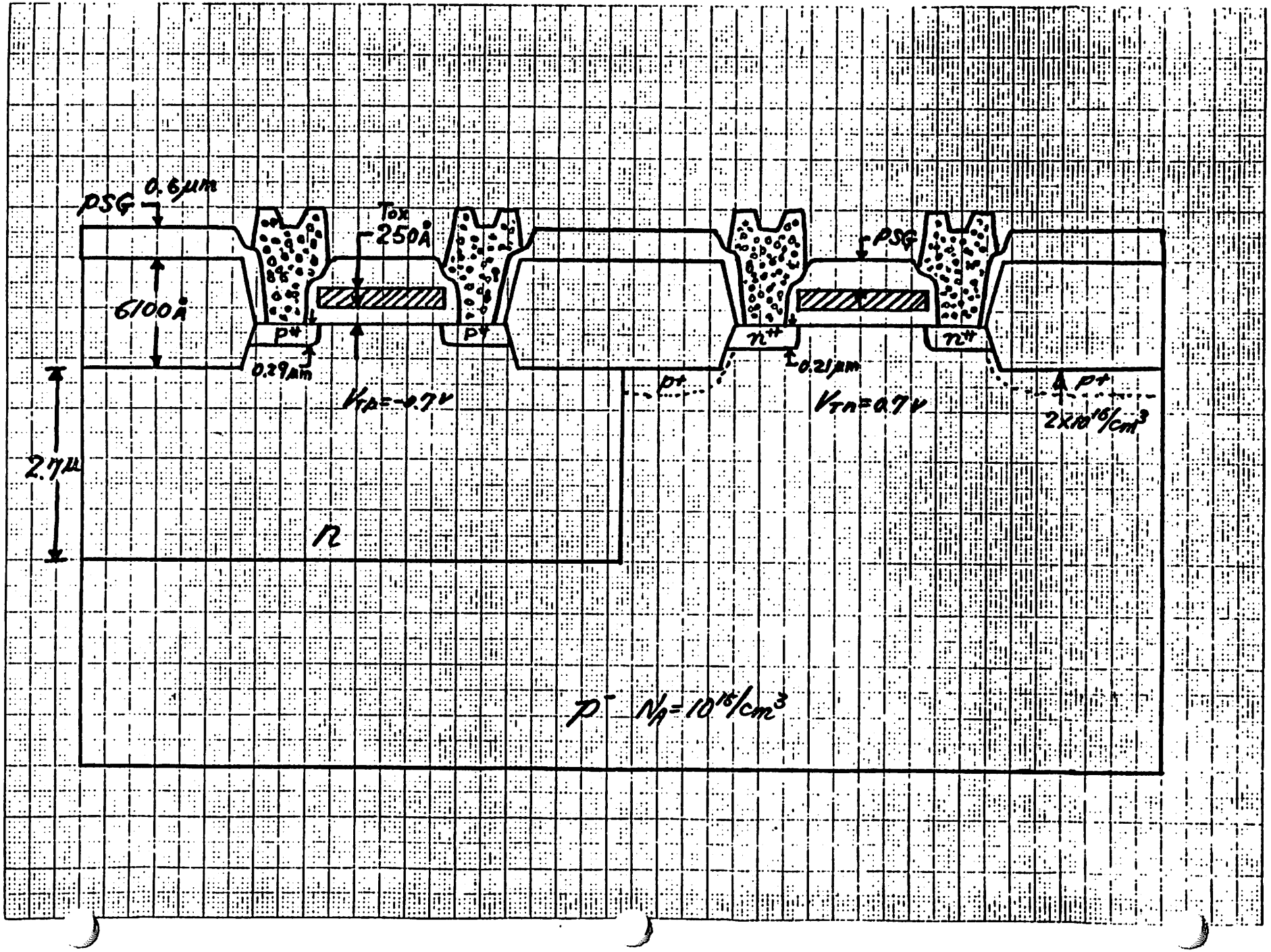
PSG
0.6μm
Tox
250Å
6100Å
P+
P+
0.29μm
V_{TP}=-0.7V
2.7μ
n
p+
n+
n+
0.21μm
PSG
V_{TN}=0.7V
p+
$2\times10^{16}/cm^3$
p⁻ $N_A=10^{15}/cm^3$

BERKELEY CMOS PROCESS
ANALOG TEST PATTERN

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Analog Test Pattern

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DISCUSSION

Analog Test Pattern

With the current rapid development of high performance MOS IC technology, the minimum feature size has advanced from 10um in production in the early 1970's to 2.5um in the early 1980's. The process of device shrinkage is still going on and we believe that minimum feature size for MOS will reach submicron domain in the late 1980's.

There are many research topics in integrated circuits at UC Berkeley. They include IC process development, device physics study, circuit designs, and development of computer-aided design packages. The advantages of having a good fabrication laboratory in our department are many folds. First, the process for each graduate student research could be different. The standard process line in the industry can not change so much for this kind of research. Second, all the process is under control by the student himself if he/she fabricates the circuit in our department. The third and the most important advantage is that the experience gained and the problems encountered give good feedbacks to the research in this department. This makes us stay at the front of IC technology.

In our efforts to develop a new Berkeley CMOS process, it is important to take into consideration how to accommodate the fabrication of analog circuits. Berkeley is in the leading position of analog circuit designs and we would like to be able to fabricate the analog circuits in our new laboratory.

The document for the analog test structure is presented in the following. Capacitors are important elements in analog applications, and have been included, as well as single resistors and the circuitry for the test of resistance matching. Also included are an operational amplifier, the important building block for advanced analog circuits, and the circuitries for the test of noise measurement and charge injection. These latter circuits employ the same opamp described above. Current mirror circuitry and various inverters have also been presented.

SUMMARY TABLE
Analog Test Pattern

Filename Sz-Blks	Structure	Purpose	Coordinates within 290n chip	Test Pat.	Func. Unit
cc0r0capsin 2	set of various Z/L	C-V dependence C-T dependence capacitance	c17r3	c0r0	c1r0
cc2r0capmat 1	array of capacitors	capacitor matching	c19r3	c2r0	c2r0
cc3r0invert 1	set of various inverters	DC transfer characteristics rise time fall time	c20r3	c3r0	c3r0
cc0r1resmat 2	set of various resistors	resistance matching	c17r4	c0r1	c0r1 c1r1
cc2r1noisem 2	transistors, resistors and opamp	noise measurement	c19r4	c2r1	c2r1
cc0r2qinjec 3	transistors and opamp	charge injection measurement	c17r5	c0r2	c0r2
cc4r1imirro 1	current mirror circuit	bias current matching, output impedance	c21r4	c4r1	c4r1
cc3r2opamp1 2	opamp	opamp offset, gain, slew rate	c20r5	c3r2	c3r2

FUNCTIONAL DESCRIPTION

Analog Test Pattern

Single Capacitors

Filename:

cc0r0capsin

Purpose:

This test chip is to characterize oxide thickness (tcox), over-etching (dL and dW), and edge modulation effects (mL and mW) of capacitors formed between polysilicon and n+ (CAP) layers.

Description:

The test chip consists of capacitors of various dimensions as tabulated below. The measured capacitance values allow one to derive tcox, dL, dW, mL and mW of the process.

Testing:

(1) Test Setup
Standard capacitance measurement (measure both stray capacitance and the total capacitance, subtract the former from the latter value).

(2) Test algorithms

(2.1) tcox (thickness of capacitor oxide)
This is expected to be different from the gate oxide thickness due to the faster growth rate over n+ layer.

$$tcox = 1.082E\text{-}7 / C1 \text{ in A}$$

(2.2) dL (along L direction)

$$dL = 28 \times (1 - 10C2/C1) \text{ in um}$$

(2.3) dW (along W direction)

$$dW = 28 \times (1 - 10C3/C1) \text{ in um}$$

(2.4) Check calculated data with C4 and C5, where

$$C4 = 32E\text{-}3 \times C1 \times (1 - 2dL/100)\ (1 - 2dW/100)$$

$$C5 = 8E\text{-}3 \times C1 \times (1 - 2dL/50)\ (1 - 2dW/50)$$

(2.5) mL (along L direction)

$$mL = 28 \times (1 - 10C6/C1) - dL \text{ in um}$$

(2.6) mW (along W direction)

$$mW = 28 \times (1 - 10C7/C1) - dW \text{ in um}$$

Pad Assignment:

PAD NUMBER	NAME	DIMENSIONS(WxL)
4,14	C1	560u x 560u
5,15	C2	560u x 56u
6,16	C6	560u x 4u x 14
7,17	C3	56u x 560u
8,18	C7	4u x 560u x 14
9,19	C4	100u x 100u
10,20	C5	50u x 50u

Note: (x,y) corresponds to
(top capacitor plate, bottom capacitor plate)

Matching Capacitors

Filename:

cc0r2capmat

Purpose:

This test chip is to determine the matching of small capacitors

Description:

Matching capacitors are used in switch capacitor filter and DAC circuits. The capacitance values used are however, too small to be determined accurately using the standard capacitance measurement technique as used in section 4. The method used here was claimed to be very accurate and insensitive to parasitic capacitance in the circuit (Ref:Hiroshi Iwai "On-Chip Capacitance Measurement Circuits in VLSI Structures", IEEE Trans on ED., vol ED-29, No.10, Oct 1983, pp.1622-1626).

The basic circuit configuration used is shown in Fig.5.1. C1, C2 form a capacitive divider. Input voltage, Vs, is 200mV peak sinusoidal waveform at 10KHz. Dc bias can be applied to the capacitors via TR1. VDC is the DC bias. Vp is a narrow pulsed waveform of 100Hz. Pulse width is 1us, 10V. This pulse will turn on TR1 periodically to maintain a dc bias at the common node of the two capacitors. There are three sources of errors namely, clock feed through in TR1, Voltage drop Vgs in TR2, and stray capacitance Cs at the capacitive node.

(1) Error due to clock feed through is minimized by using lock-in amplifier which is locked onto the input frequency of Vs. Hence the feed through signal at low frequency is removed.

(2) Vgs of TR2 can be eliminated by the following technique

   (a) Measure V01 with Vs across capacitance as in Fig.5.1;

   (b) Measure V02 with Vs and dc bias applied to VDC as in Fig.5.2. Then,

$$1 + C2/C1 + Cs/C1 = Vs/(V01 + Vs - V02)$$

   If C2>>Cs, then C2/C1 can be calculated.

(3) Cs can be eliminated from the above eqn. by repeating the measurement with C2'=2C2. Then

$$1 + 2C2/C1 + Cs/C1 = Vs/(V01' + Vs - V02')$$

Hence,

$$C2/C1 = Vs/(Vs+V01'-V02') - Vs/(Vs+V01-V02)$$

Testing:

(1) Test setup
The actual circuit used and the test setup is as shown in Fig.5.3. Note that:

(a) Vs = 200 mV peak 10KHz sine wave

(b) VDC = 0 to 5V

(c) Vp = 10V 100Hz pulse, pulse width = 1us

(2) Test Algorithms

(a) Measure Vo1, V02 according to function 1, 2 in table below.

(b) Measure V01', V02' according to function 3 and 4 in table below. Then calculate C2/C1 as discussed in text.

Pad Assignment:

PAD #	NAME	FUNCT#1	FUNC#2	FUNC#3	FUNC#4
1	Vout1	V01	V02		
2	Vac+	Vs+	GND	Vs+	GND
3	VBIAS	dc bias for current source			
4	Vout2	V01'	V02'		
11	VDD	VDD	supply		
12	Vac-	Vs-	GND	Vs-	GND
13	Vp	pulse input			
14	VIN	dc bias	dc bias	dc bias	dc bias
5	Vss	Vss supply			

Matching Resistors

Filename:

cc1r0resmat

Purpose:

This test chip is to characterize the matching of pairs of resistors and to determine the correction factors to the resistance value due to oversize contact area at both ends (dC) and corner effect (dR).

Descriptions:

Precision resistors used in analog circuits are poly and n+ diffusion (NNII) resistors. p+ diffusion and Nwell resistors are occasionally used for biased circuit. The pattern included in this test chip consists of all the above mentioned types of resistors. A Nwell pinch resistor is also included for completeness.

Testing:

(1) Test setup:
Direct resistance measurement.

(2) Test Algorithm:

(2.1) For matching pairs, calculate Ra/Rb

(2.2) For poly resistor:

$$dC(poly) = 3(10R11 - R1)/(R1 - R11) \text{ in squares}$$

$$dR(poly) = (60 + 2dC(poly))(R15 - R1)/10R1 \text{ in squares/corner}$$

(2.3) For n+ resistors:

$$dC(n+) = 1.5(10R13 - R3)/(R3 - R13)$$

$$dR(n+) = 0.2(30 + 2dC(n+))(r20 - R3)/R3$$

Pad Assignments:

PAD NUMBER	NAME	TYPE	DIMENSIONS	# of SQ.
Group A:c0r1				
(1,11)(2,12)	R1, R2	POLY	240uX4uX2	60
(3,13)(4,14)	R3, R4	n+	240uX8uX2	30
(5,15)(6,16)	R5, R6	p+	240uX8uX2	30
(7,17)(8,18)	R7, R8	Nwell	250uX10uX2	25
(10,20,19)	R9	Pinch	250uX10u	25
Group B:c1r1				
(1,11)(2,12)	R11,R12	POLY	24uX4uX2	6
(3,13)(4,14)	R13,R14	POLY	24uX4uX2	6
(5,15)	R15	POLY	240uX4u	60
(6,16)(7,17)	R16,R17	n+	24uX8uX2	3
(8,18)(9,19)	R18,R19	n+	24uX8uX2	3
(10,20)	R20	n+	240uX8u	

Operational Amplifier

Filename:

cc2r3opamp1

Purpose:

This circuit serves the purpose of evaluating a general purpose operational amplifier circuit, which is one of the most important building blocks in the analog applications. Some essential properties, such as DC gain, frequency response, unity gain bandwidth, and offset voltage can be directly characterized from this circuit. The result can then be compared with the SPICE simulation results.

Description:

An operational amplifier, which features a standard two-stage structure and a source follower output stage to drive the off-chip load, such as probes, is shown in Fig. 7-1. A bias circuit, outlined with the dotted line, is also shown in this schematic. A resistance, in the value of 11 K-ohms is required in the bias circuitry. However, at this moment, the sheet resistance is not fully characterized. As shown in the schematic, two pads are tapped out in the bias circuitry to provide controllability from the outside.

SPICE simulation has been performed on both the bias circuit and the operational amplifier. Results and the input decks are listed in APPENDIX. A summary of the performance as suggested by SPICE with a load of 20 pF is:

DC gain=30,000
Unity gain bandwith=3 MHz
Phase margin= 60 degrees

Testing:

(1) Test Algorithms

The following properties can be extracted from this circuit:

(a) DC open loop gain
(b) Frequency response
(c) Offset voltage

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	VDD	VDD supply
3	BIAS	opamp bias
10	VSS	VSS supply
12	OUT	opamp output
16	VIN+	opamp vin+
18	VIN-	opamp vin-
20	BIASTRIM	bias trim

Noise Measurement Circuitry

Filename:

cc1r2noisem

Purpose:

To characterize the noise generated by a pair of differential input devices.

Description:

The circuit schematic is shown in Fig. 8-1, where a pair of P-channel differential devices are connected to the inputs of the operational amplifier. The bias current source for this input pair is controlled with an external bias voltage for various bias current levels. The loads for this input pair are not on chip for flexibility, which will be described in the Testing section.

Testing:

1. Test Setup

The test setup of the noise measurement is shown in Fig. 8-2, where external resistance loads are connected to the devices under test for various gain levels. Two more resistors (10K and 100 ohms) form a voltage divider to provide a loop gain of 100.

2. Test Algorithms

The noise spectrum appears at the output node of the opamp, (node labeled **OUT**), is amplified by this closed loop configuration to be 100 times of that of the input differential pairs under test.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
7	INPUT1	input 1
8	INPUT2	input 2
11	OUT	output
12	BIAS	opamp bias
13	VDD	VDD supply
15	OPIN+	opamp positive input
17	OPIN-	opamp negative input
18	INBIAS	input stage bias
19	VSS	VSS supply
20	BIASTRIM	bias trim

Charge Injection Circuit

Filename:

cc2r0qinjec

Purpose:

The purpose of this circuitry is to characterize the charge injection effect as seen frequently in switched capacitor circuits.

Description:

The circuit schematic is shown in Fig. 9-1, where a sampling switch, comprised of a P-channel and an N-channel MOSFET, and a sampling capacitor in the value of 6 pico Farad, are connected to the positive input to the operational amplifier. An inverter is also implemented to provide the opposite polarity signal to the gate of the P-channel FET.

Testing:

1. Test Setup

The test setup is shown in the schematic in Fig. 9-2. The operational amplifier is connected as a unity gain buffer to conserve the charge. External operational amplifier and resistor dividers are also required to amplify the charge injection effect.

2. Test Algorithms

The charge injected from the sampling switch to the top plate of the sampling capacitor is converted into voltage according to V=Q/C. This voltage is buffered by the on-chip unity gain op. amp. and then amplified by the external fixed gain amplifier to be measured.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	VDD	VDD supply
3	BIAS	opamp bias
4	SAMPLE	sampling clock in
10	VSS	VSS supply
12	OUT	opamp output
16	VIN	input to be sampled
17	CAPBP	capacitor bottom plate
18	VIN+	opamp vin+
19	VIN-	opamp vin-
20	BIASTRIM	bias trim

Current Mirrors

Charge Injection w/o On-chip Opamp

Filename:

cc1r4imirro

Purpose:

The purpose of this block is to characterize the performance of the commonly used bias circuitry. Charge injection circuits are included, too.

Description:

The circuit schematics are depicted in Fig. 10-1. One NMOS current mirror and one PMOS current mirror circuits are included respectively. All the drawn device sizes are chosen as Z/L=40/6. Two charge injection circuits are included. One for the study of NMOS charge injection effect. The other one for the PMOS case. A 2pf capacitor is used in each charge injection circuit. A single transistor is used as a buffer instead of an on-chip opamp. For the circuit with on-chip opamp as a buffer, please consult section 9. The idea is that in case the on-chip opamp does not work well, we still can test the charge injection effect. Because the critical node is buffered so that direct coupling from the input signal probe to the output signal probe is not a problem.

Testing:

(1) Current Mirror Circuits:

(1.1)Test Setup

The test setup for the current mirror circuit is shown in Fig. 10-2. A current source is connected to the pin IREF. A voltage source with a current meter is connected the pin OUT.

(1.2)Test Algorithms

For each reference current value, vary the voltage of the voltage source and the current flowing through the current meter reflects the mirrored current. The plot of the mirrored current vs the voltage gives the performance of the current mirror circuit.

(2) Charge Injection Circuits:

Please consult section 9.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
1	OUT1	Output
2	IREF1	Reference current source
11	VSS1	VSS supply
3	OUT2	Output
4	IREF2	Reference current source
13	VDD2	VDD supply
5	SAMPLE3	Sampling clock in
6	VIN3	Input to be sampled
14	VGN3	Ground
15	OUTS3	Buffered xstr. source
16	OUTD3	Buffered xstr. drain
7	SAMPLE4	Sampling clock in
8	VIN4	Input to be sampled
9	VGN4	Ground
17	OUTS4	Buffered xstr. source
18	OUTD4	Buffered xstr. drain

Various Inverters

Filename:

co0r3invert

Purpose:

The purpose of this block is to characterize the DC transfer characteristic, rise time, and fall time of the CMOS inverters.

Description:

The circuit schematics are depicted in Fig. 11-1. Three CMOS inverters are included. The first one uses the feature size transistors which are suitable for digital applications. The second one uses the medium size transistors which are suitable for analog applications. The third one uses the transistors with the Z/L ratio equals to 3 for PMOS vs NMOS. The idea is to compensate the effect of mobility difference in PMOS and NMOS.

Testing:

(1) Test Setup
A power supply is connected across the pins VDD and VGN. A signal source is connected to the pin VIN and a oscilloscope is used to monitor the pin OUT.

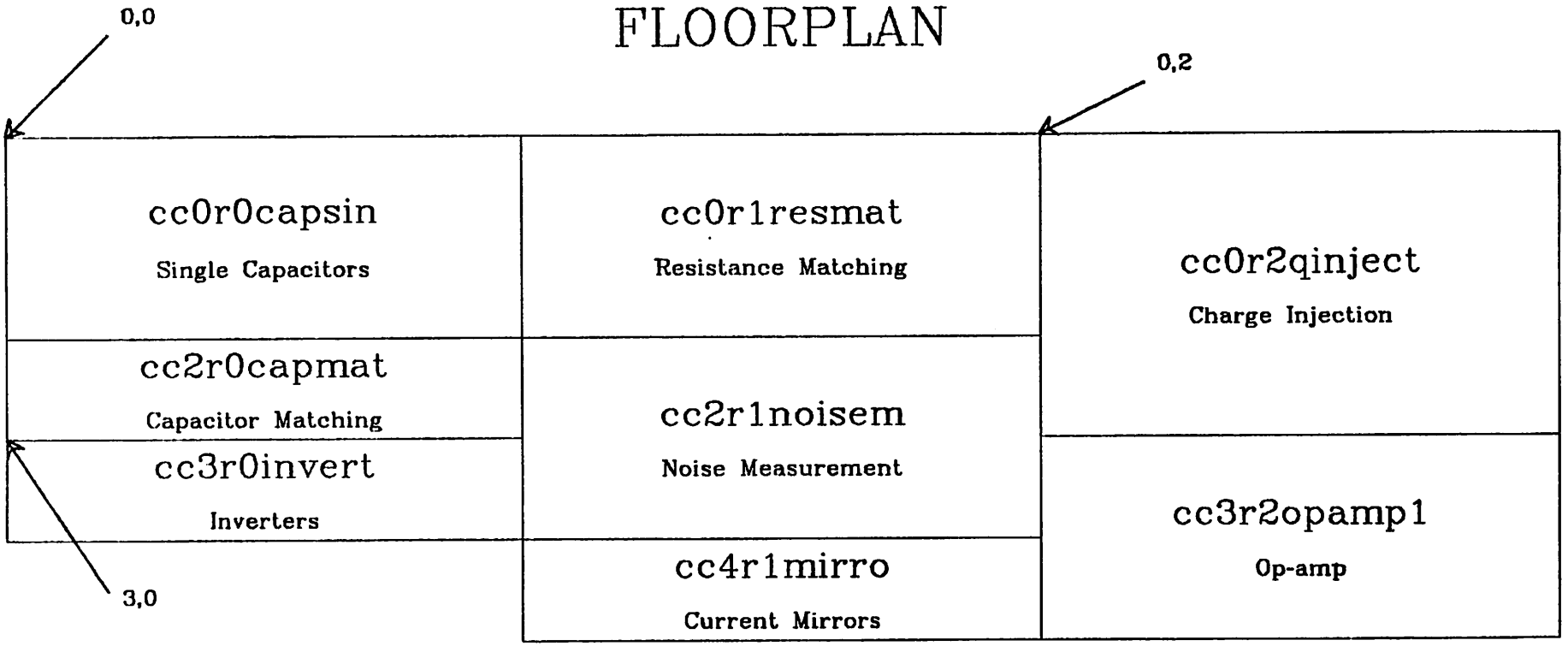
(2) Test Algorithms
Scan the input signal from 0 to Vdd (use 5 volts for 5-volt technology) and put the oscilloscope in the OUT vs VIN mode which displays the DC transfer curve directly.

Use the pulse train signal as input and the display on the oscilloscope shows the rising edge and falling edge performances of the inverter.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
1	VIN1	Inverter input
2	VDD1	VDD supply
11	VGN1	Ground
12	OUT1	Inverter output
3	VIN2	Inverter input
4	VDD2	VDD supply
13	VGN2	Ground
14	OUT2	Inverter output
5	VIN3	Inverter input
6	VDD3	VDD supply
15	VGN3	Ground
16	OUT3	Inverter output

ANALOG TEST PATTERN FLOORPLAN



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Analog Test Pattern

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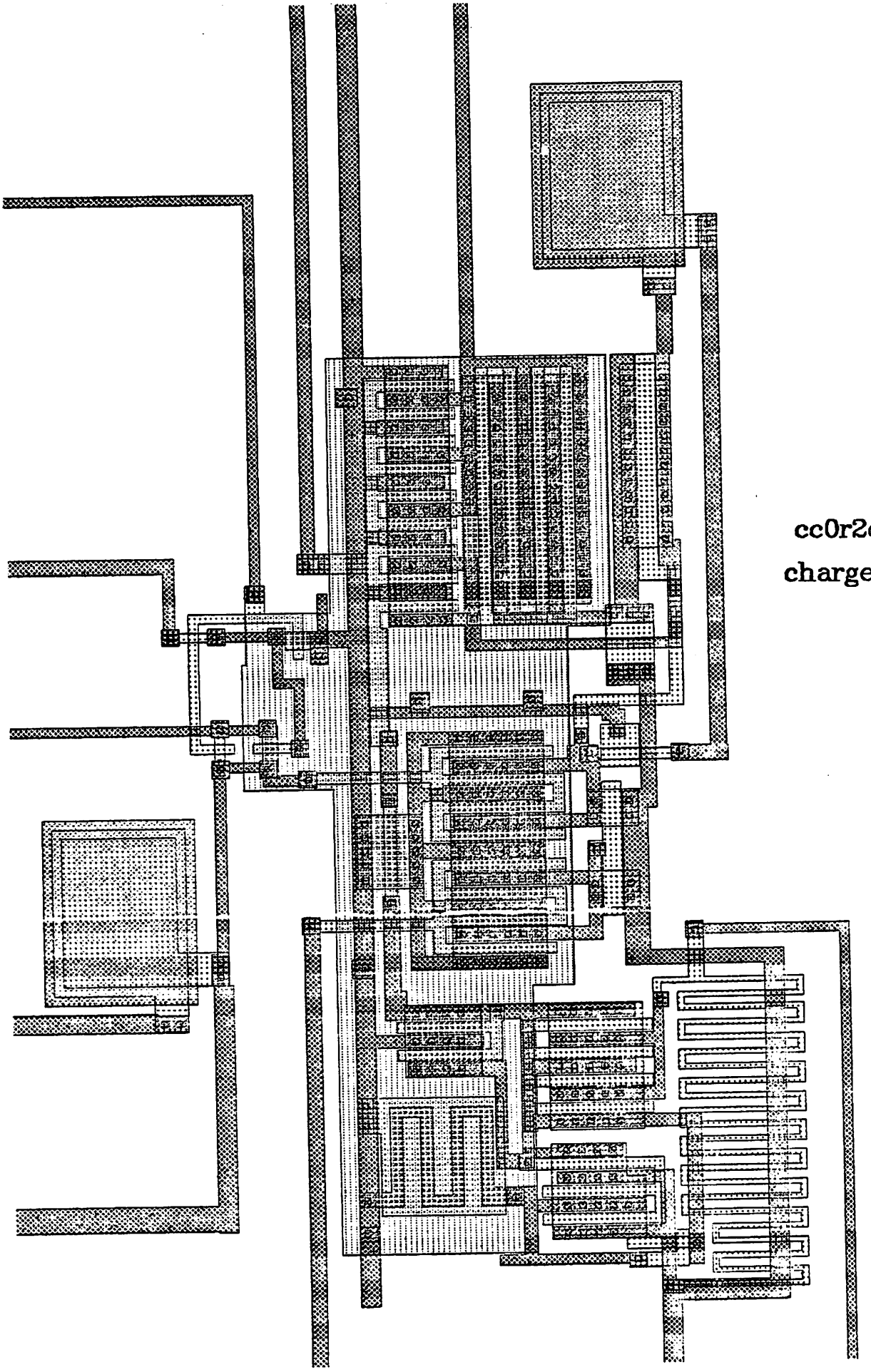
charge injection



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cc3r0invert.cif

inverters

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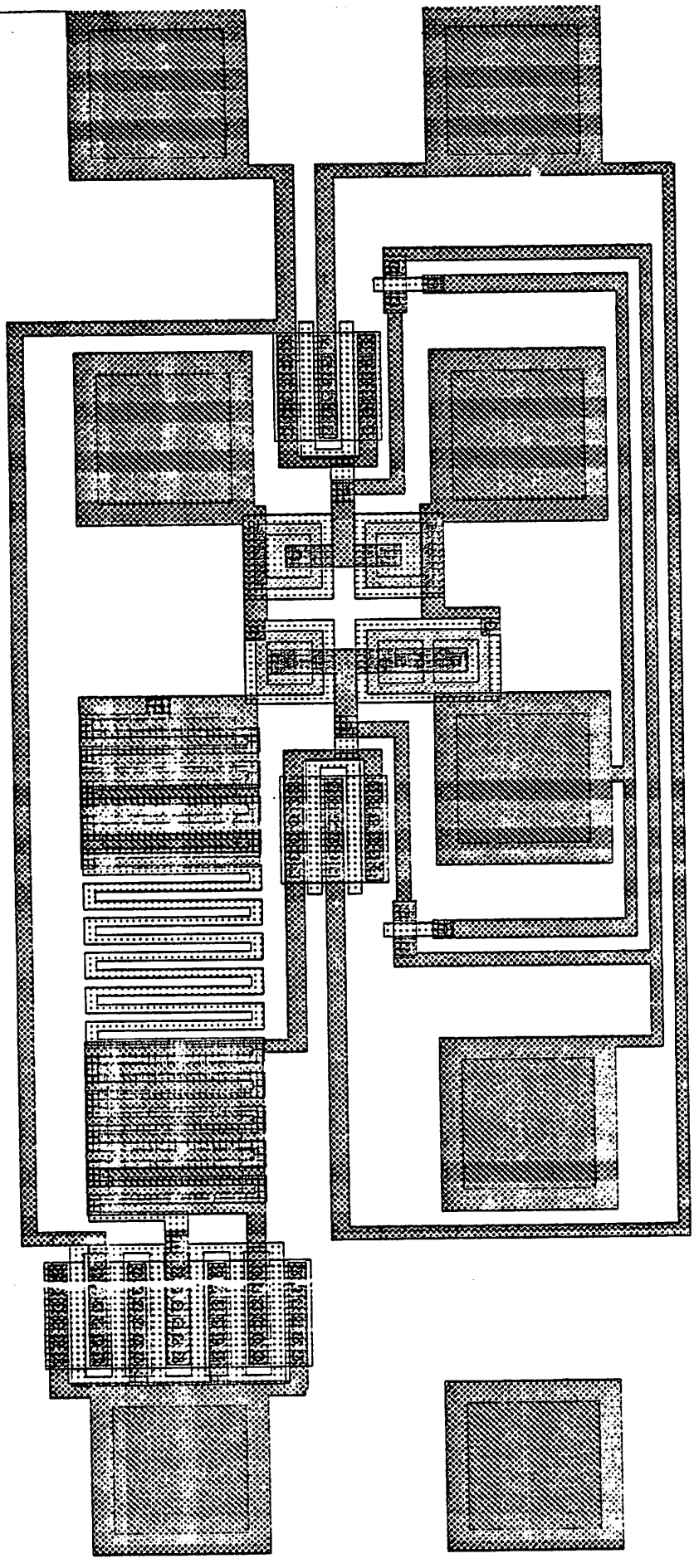
inverters

cc2r0capmat.cif

capacitor matching



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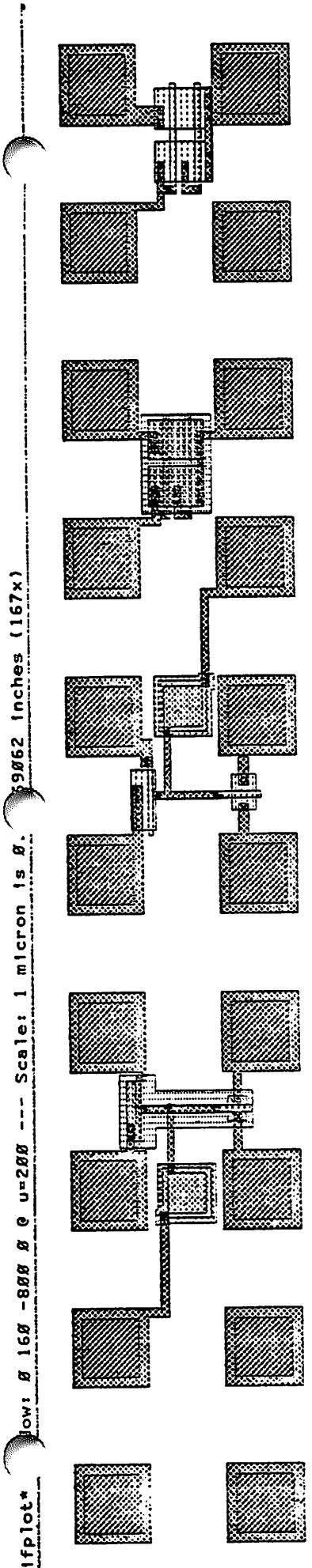
capacitor matching



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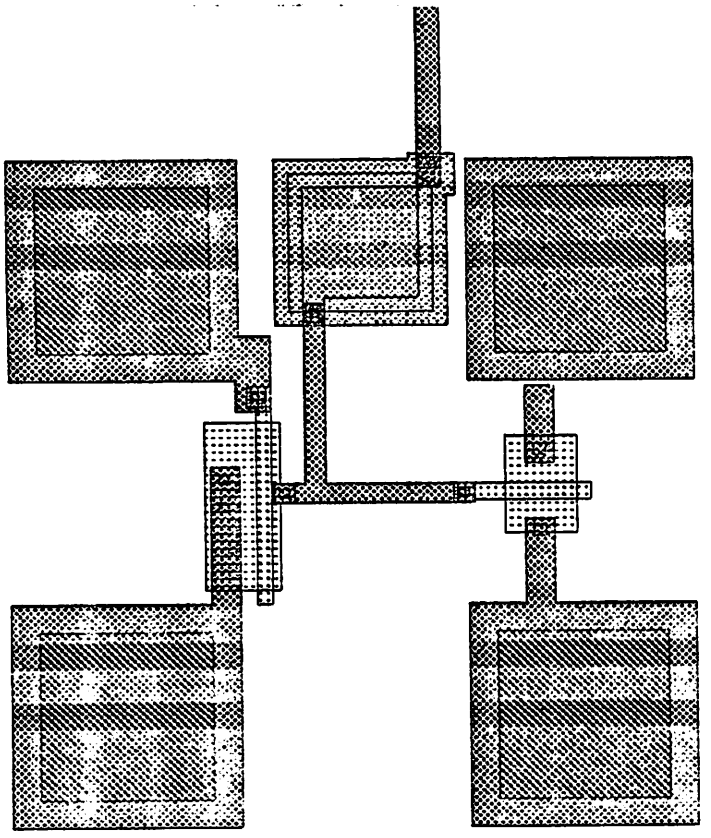
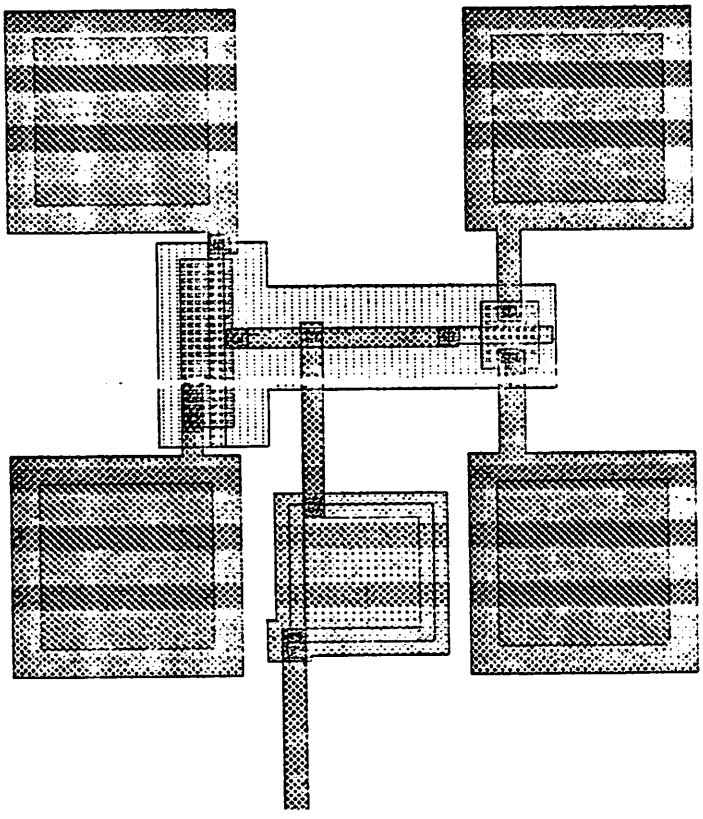
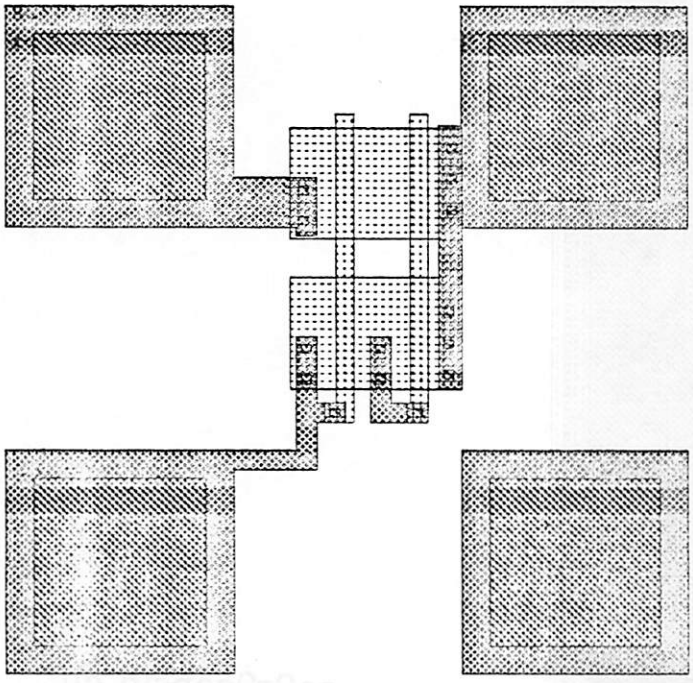
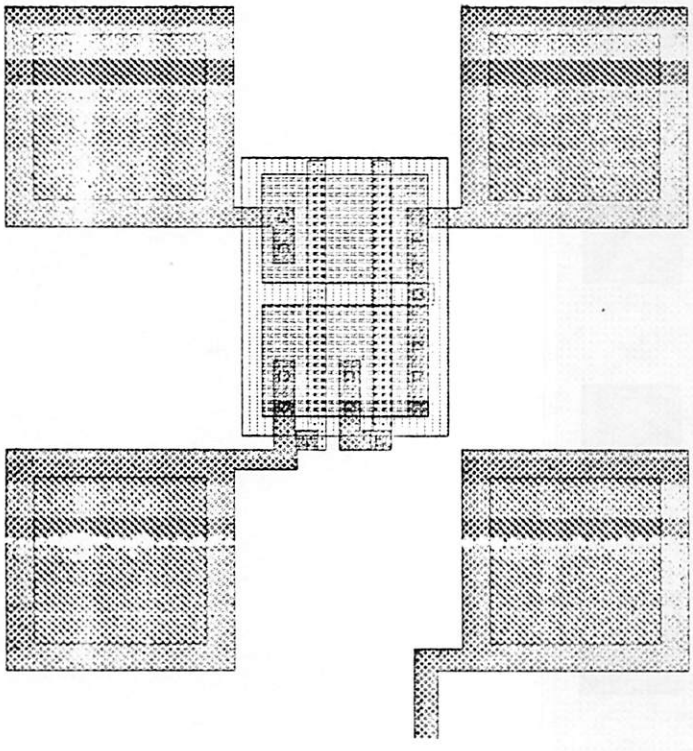


cc41imirro.cif
current mirrors





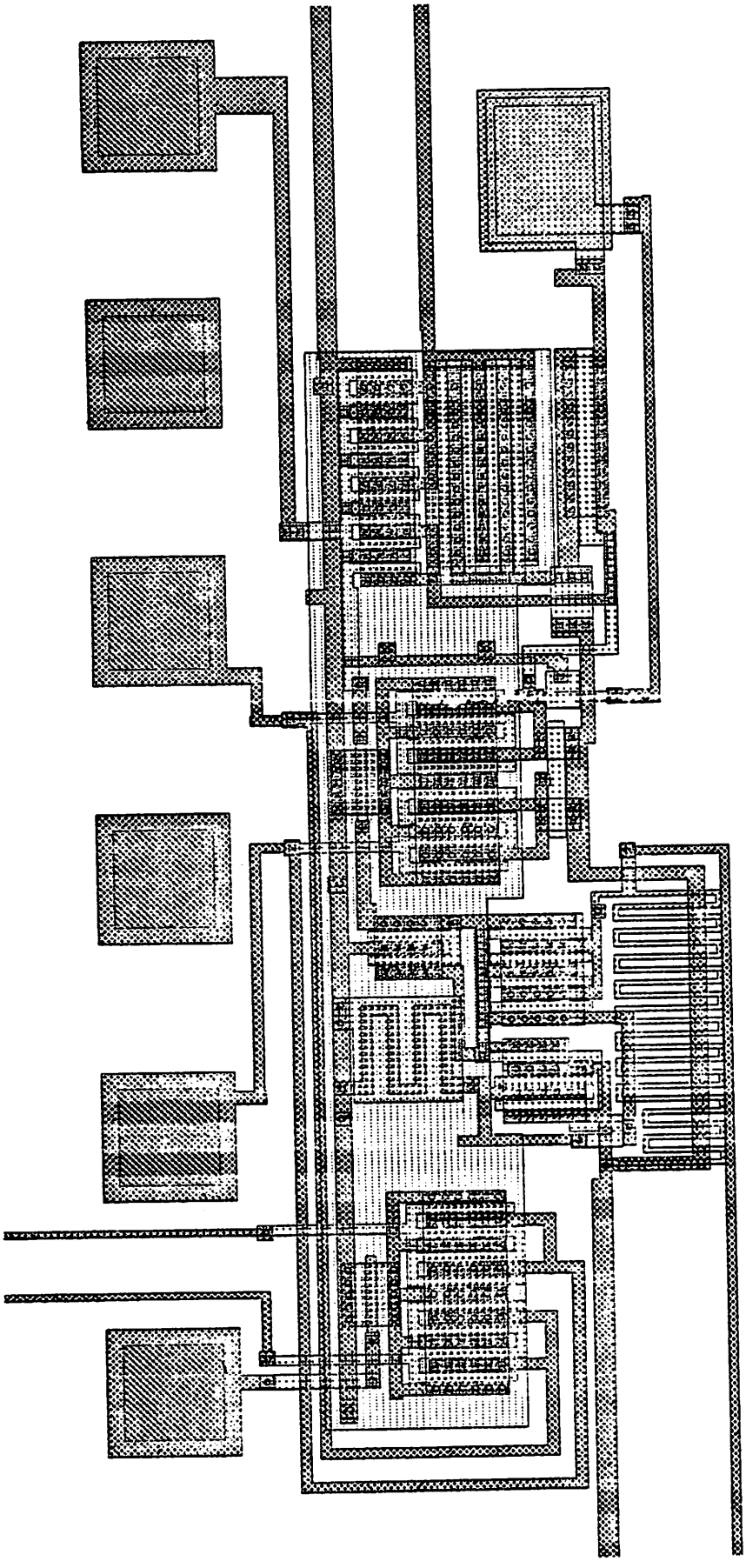
cc4r1imirro.cif
current mirrors



cc0r0capsin.cif
single capacitors

cc2r1noisem.cif

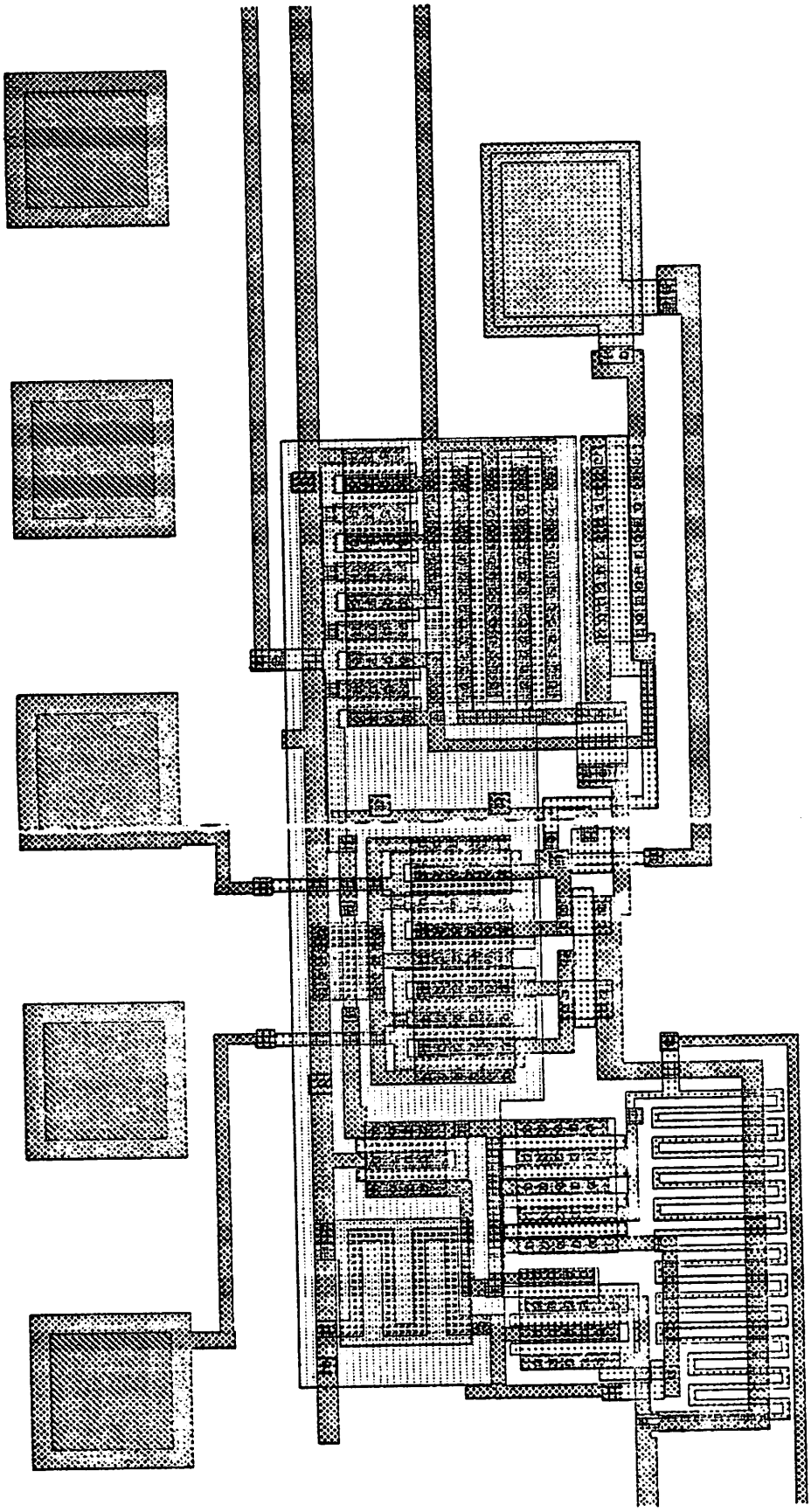
noise measurement



cc2r1noisem.cif
noise measurement

cc3r2opamp1.cif

opamp



cc3r2opamp1.cif
opamp

cc0r1resmat.cif
resistance matching

Analog Test Pattern (csubchip)
Cif File Cell Hierarchy

PAD.k

PADSET.k
  PAD.k

RESISTORA1.k
  PADSET.k

RESISTORB1.k
  PADSET.k

bias.k

cc0r0capsin.k
  PAD.k

cc0r1resmat.k
  RESISTORA1.k RESISTORB1.k

cc0r2qinjec.k
  PADSET.k bias.k comcap.k oa2.k switch.k

cc2r0capmat.k
  PADSET.k

cc2r1noisem.k
  PADSET.k bias.k comcap.k noise1.k oa2.k

cc3r0invert.k
  PADSET.k

cc3r2opamp1.k
  PADSET.k bias.k comcap.k oa2.k

cc4r1imirro.k
  PADSET.k

comcap.k

csubchip.k
  cc0r0capsin.k cc0r1resmat.k cc0r2qinjec.k cc2r0capmat.k
  cc2r1noisem.k cc3r0invert.k cc3r2opamp1.k cc4r1imirro.k

inv.k

noise1.k

oa2.k

switch.k
inv.k

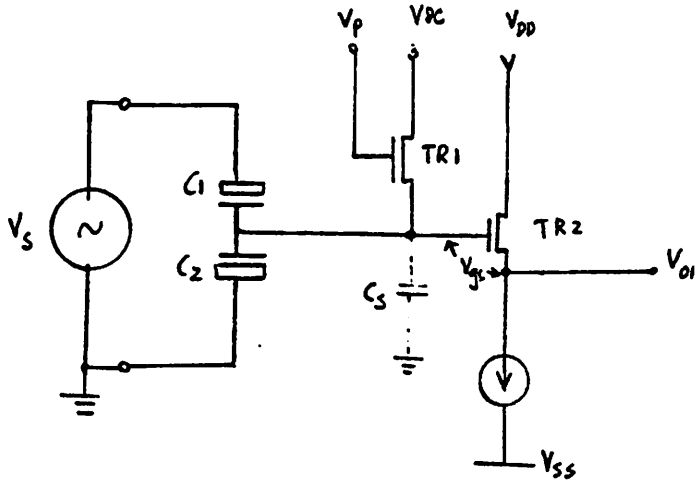


FIG 5.1 On-Chip Capacitance Ratio Measuring Technique

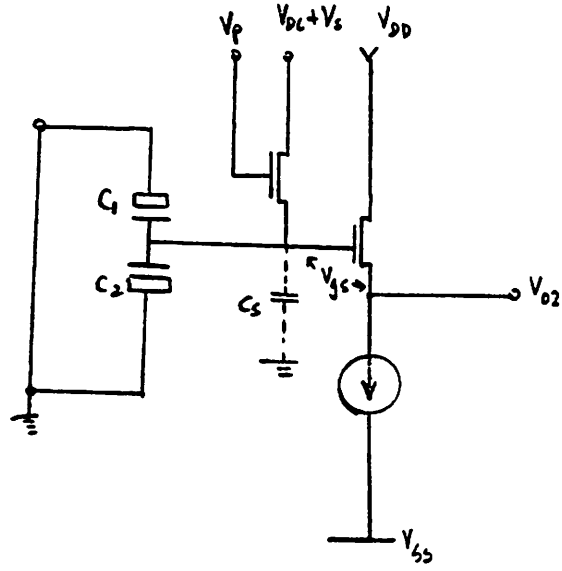


FIG 5.2 2nd Measurement to eliminate V_{gs}

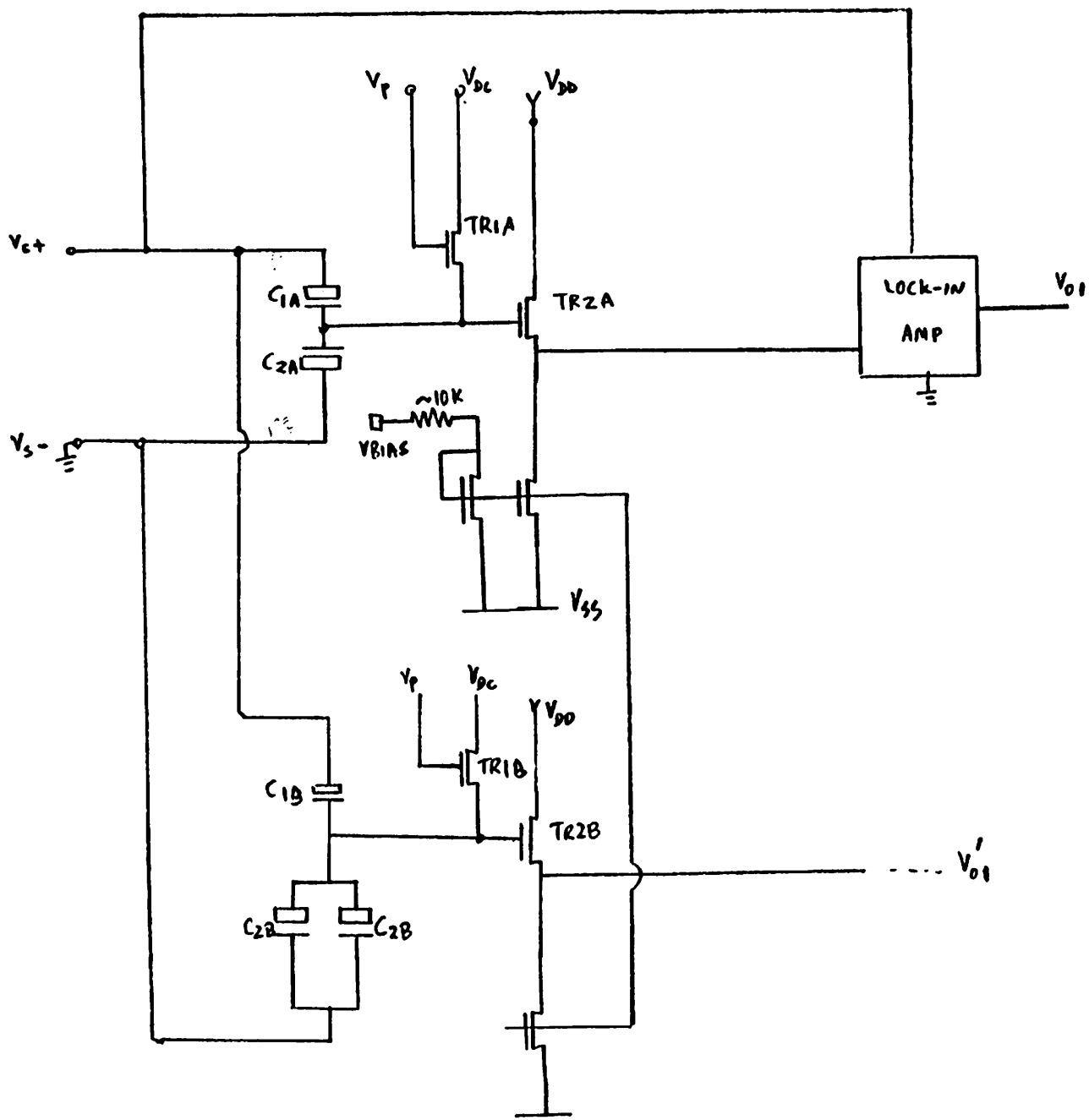


FIG 5.3 TEST CHIP AND TESTSET UP (ONLY ONE LOCK-IN AMPL CONNECTION SHOWN)

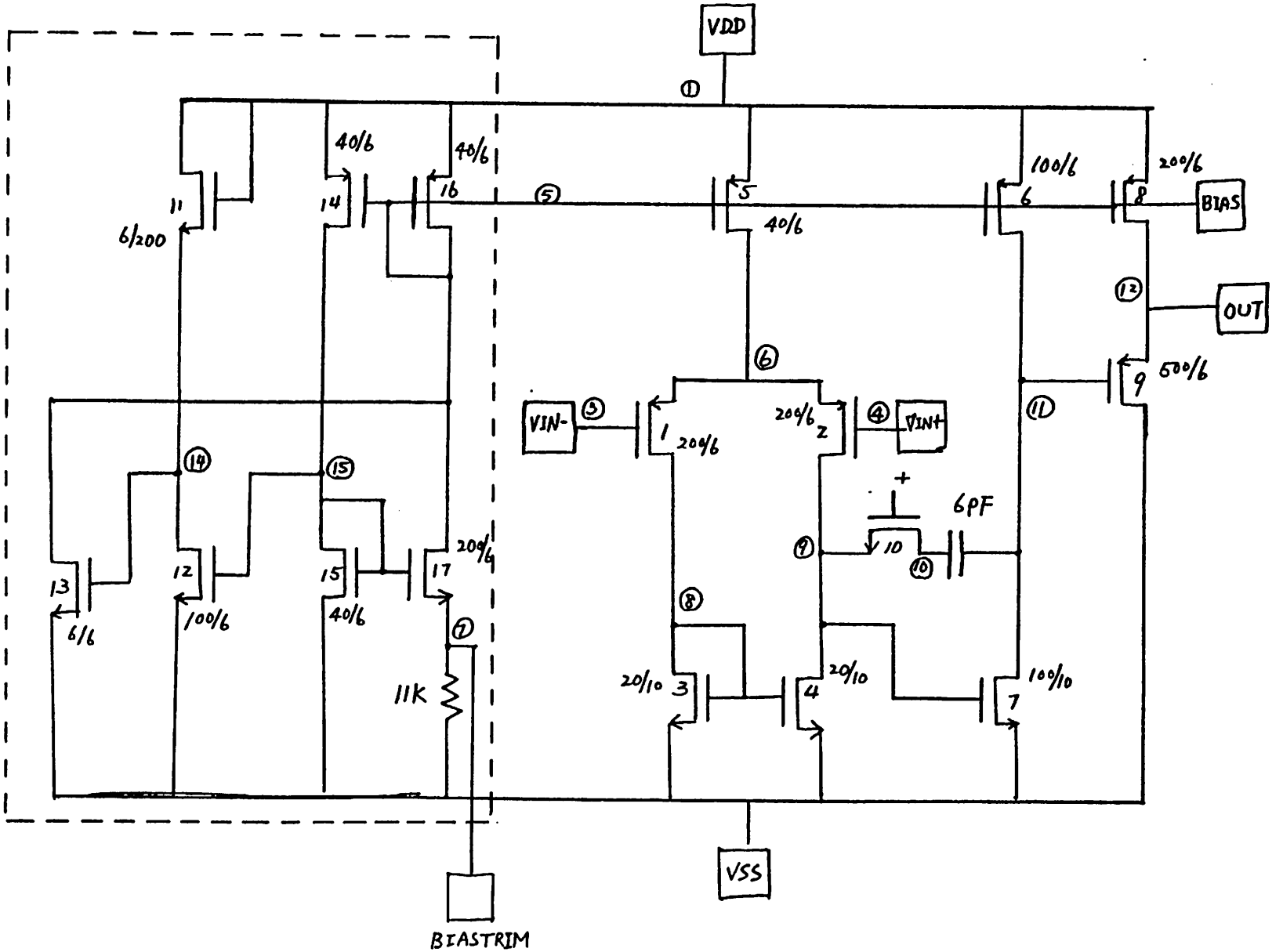


Figure. 7-1 Operational Amplifier

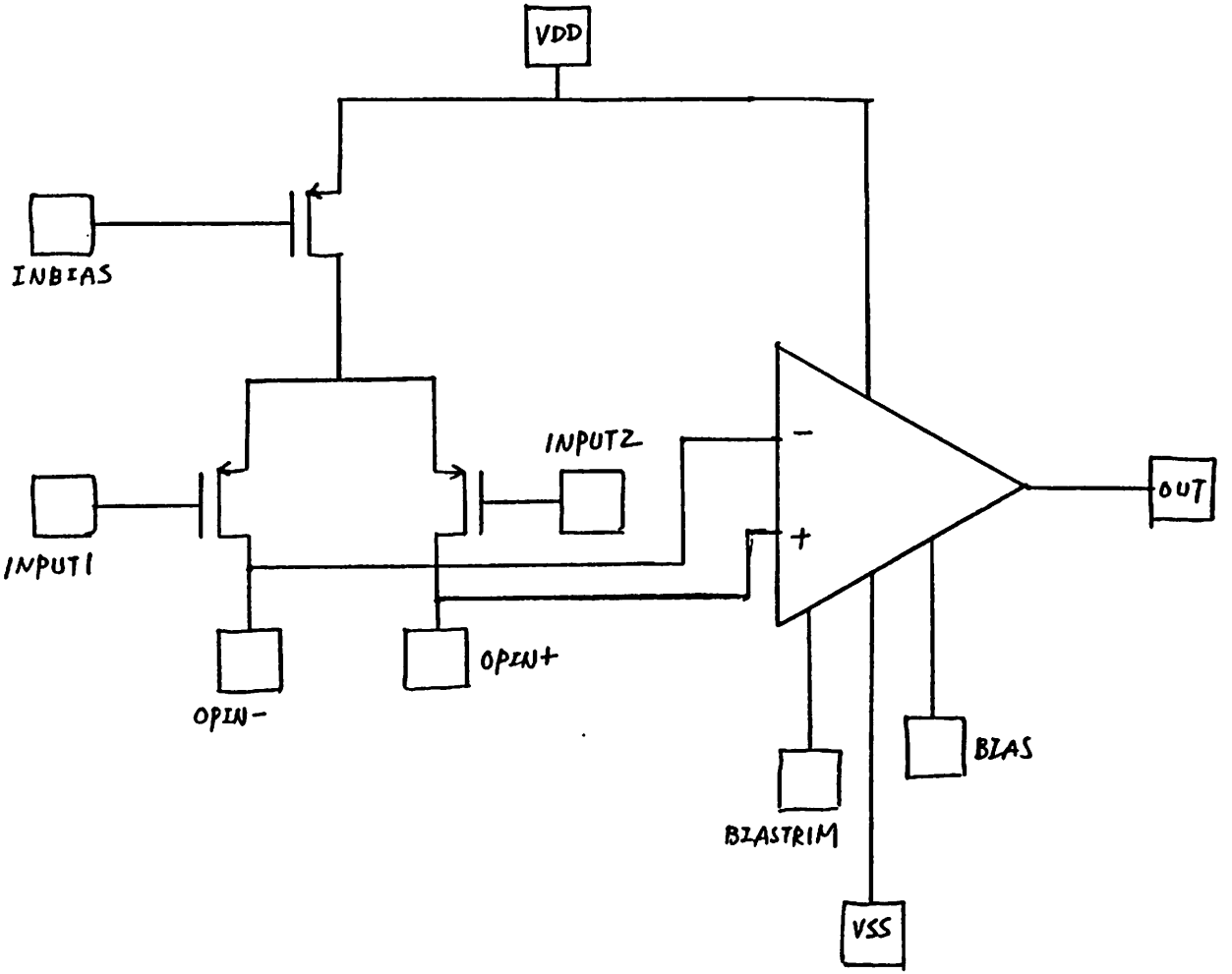


Figure 8-1. Noise Measurement Circuit Schematic

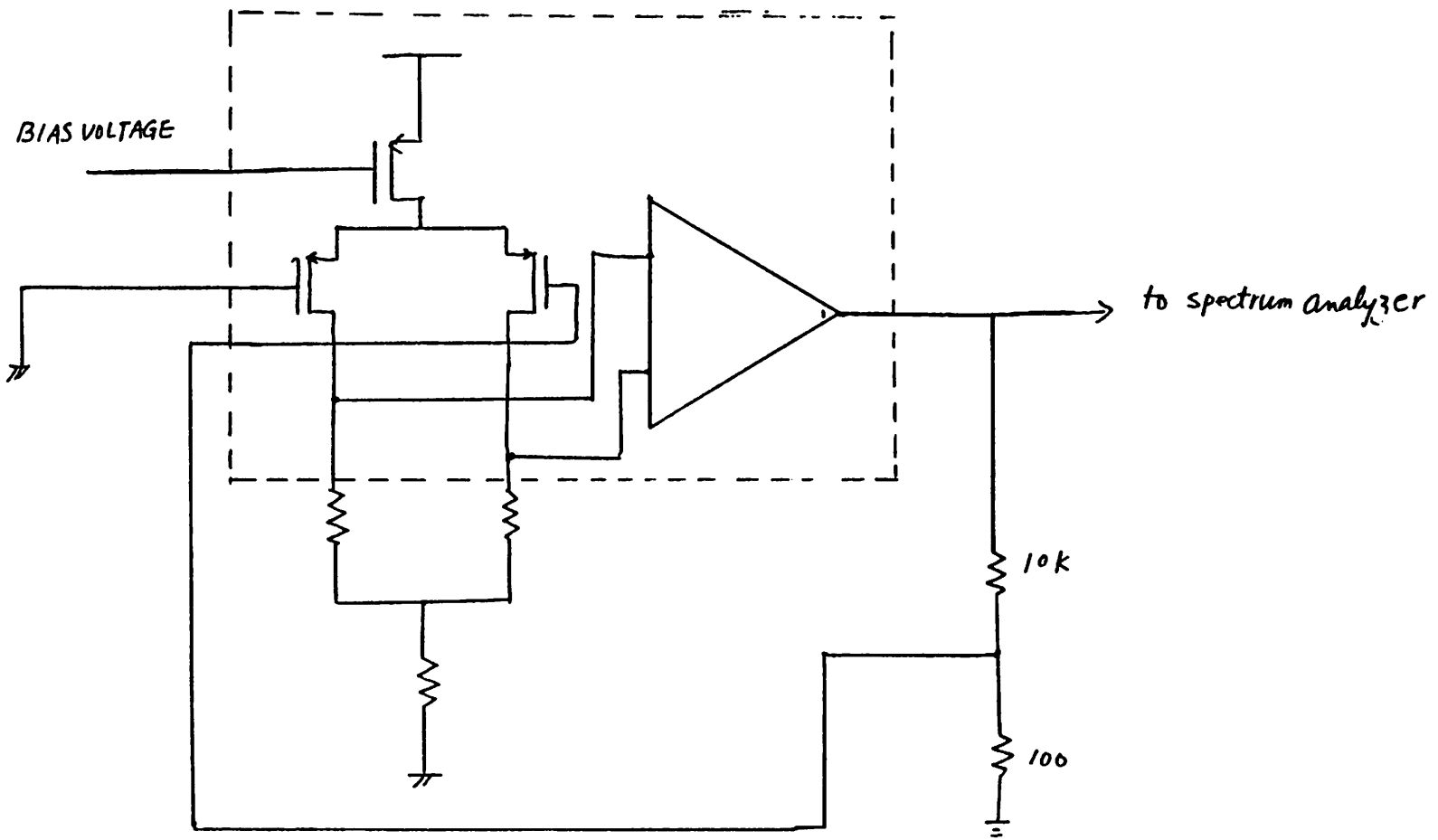


Figure 8-2 Noise Measurement Test Setup

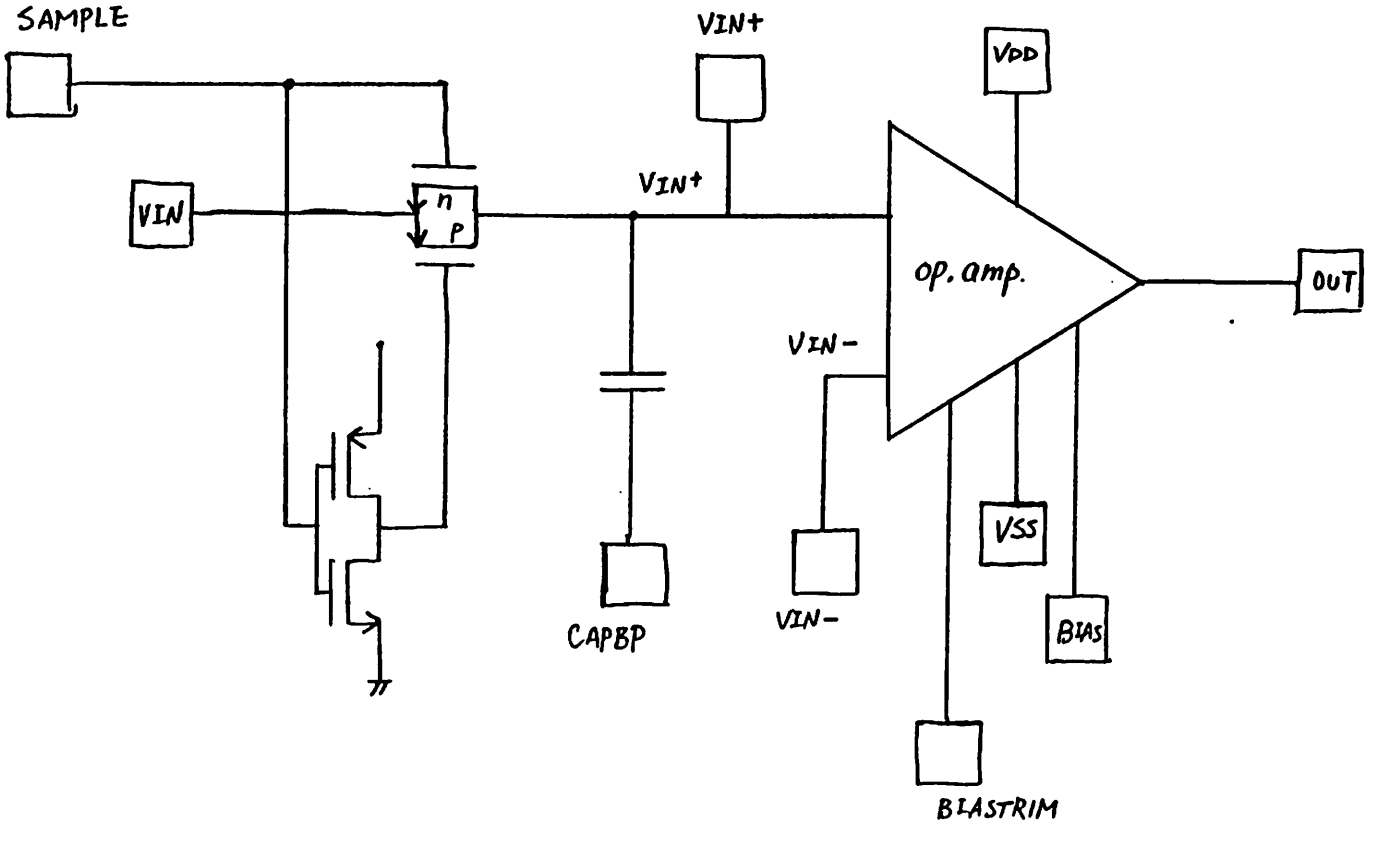


Figure 9-1. Charge Injection Circuit Schematic

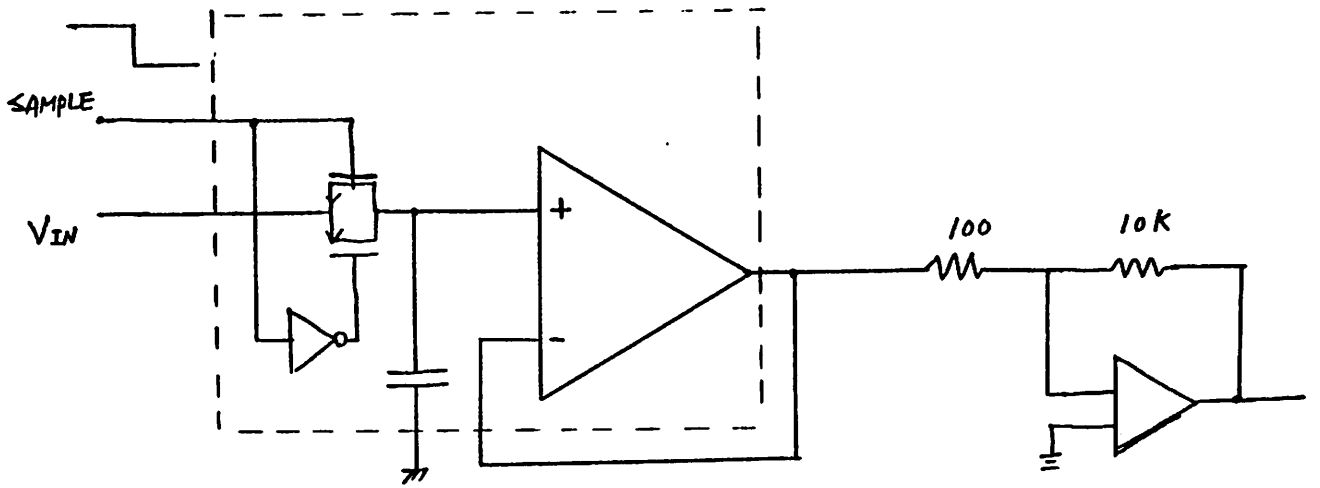


Figure 9-2 Test Setup for Charge Injection Measurement

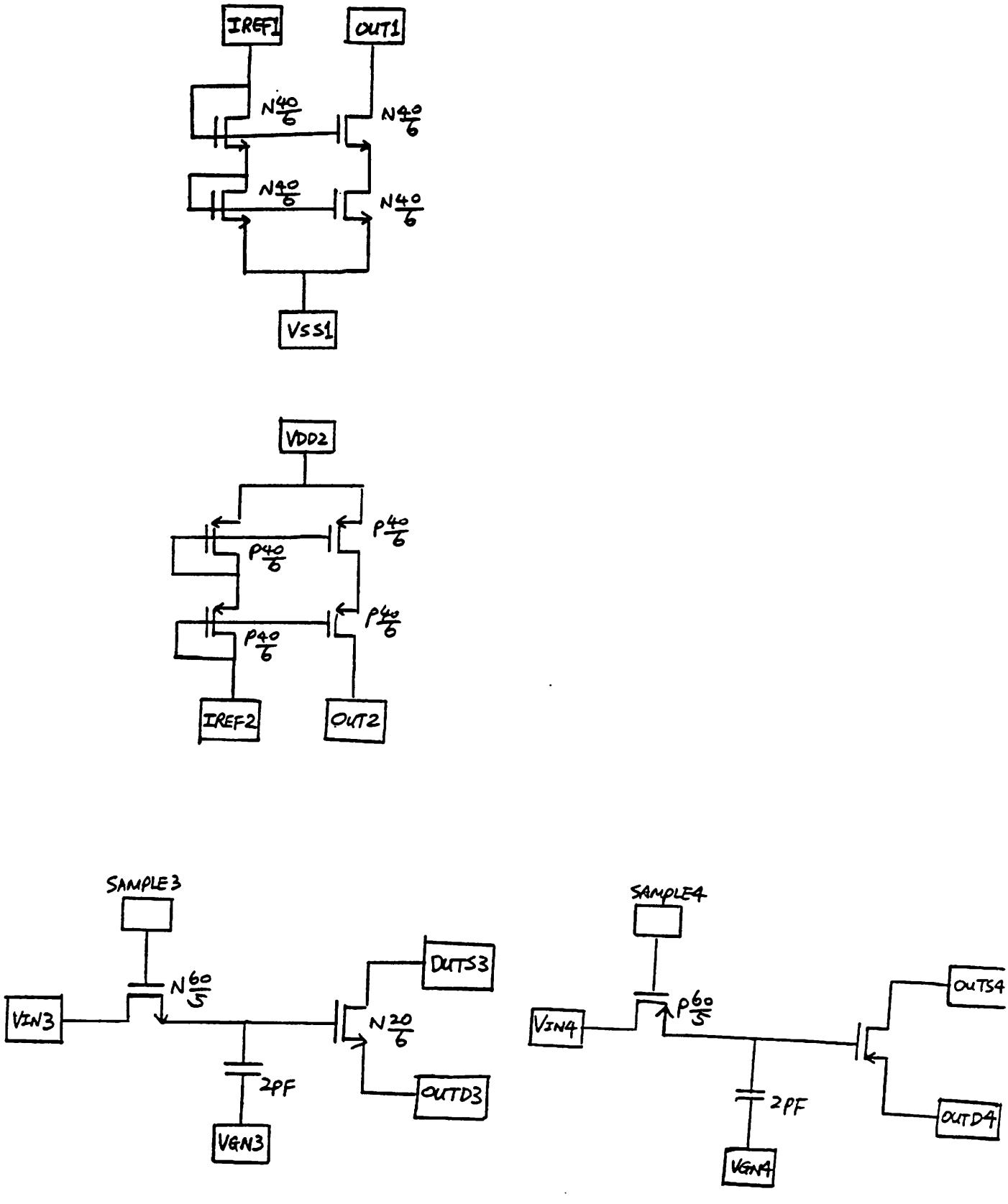


Fig. 10-1 Current mirrors and charge injection without Op-amp

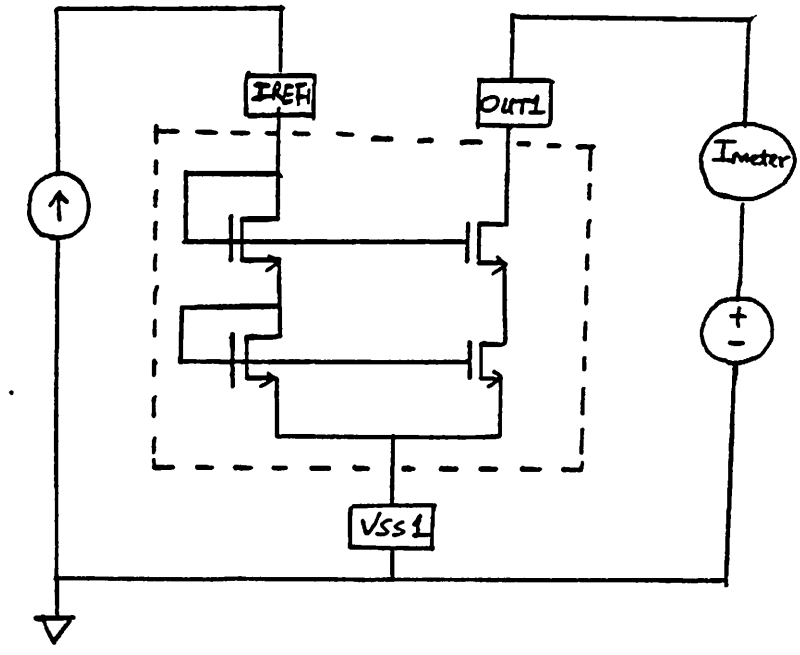
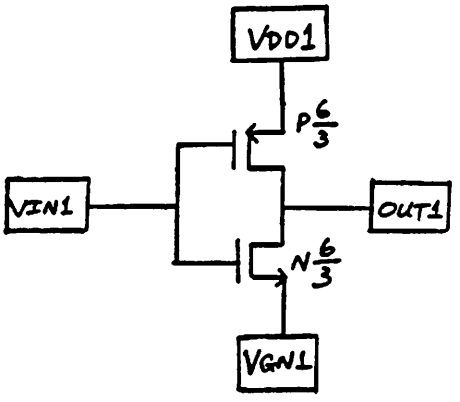
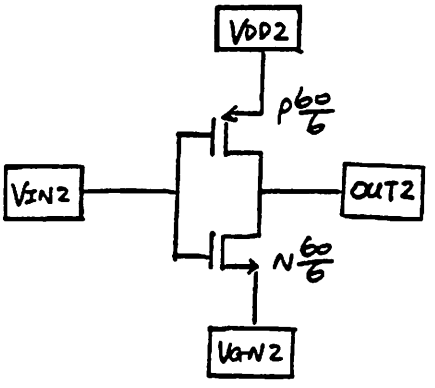


Fig. 10-2 Current Mirror Test Setup.





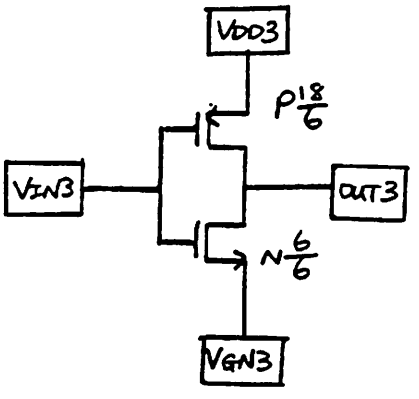


Fig. 11-1. Inverters

APPENDIX I

SPICE SIMULATIONS

1. Input deck of SPICE simulation of the bias circuit

2. Output of SPICE simulation of the bias circuit

3. Input deck of SPICE simulation of the operational amplifier

4. Output of SPICE simulation of the operational amplifier

```
1*******12/14/83 ********  SPICE 2G.6     3/15/83 ********20:07:08*****

OOPAMP

0****      INPUT LISTING                          TEMPERATURE =    27.000 DEG C

0******************************************************************************


 .MODEL N     NMOS LEVEL=2
+   VTO=0.7
+   CGSO=350P        CGDO=350P
+   CJ=80U           MJ=0.5          CJSW=500P       MJSW=0.55
+   TOX=40N          NSUB=1.0E15     TPG=+1
+   XJ=600N          LD=300N         UO=700
+   VMAX=50K         NEFF= 30
 .MODEL P     PMOS LEVEL=2
+   VTO=-0.7
+   CGSO=350P        CGDO=350P
+   CJ=200U           MJ=0.5          CJSW=1500P       MJSW=0.5
+   TOX=40N          NSUB=1.0E16     TPG=+1
+   XJ=600N          LD=300N         UO=350
+   VMAX=50K         NEFF= 30
M11 1 1 14 2 N W=6U L=200U
M12 14 15 2 2 N W=100U L=6U
M13 5 14 2 2 N W=6U L=6U
M15 15 15 2 2 N W=40U L=6U
M17 5 15 7 2 N W=200U L=6U
M14 1 5 15 1 P W=40U L=6U
M16 1 5 5 1 P W=40U L=6U
RR 7 2 11K
VDD 1 0 5
VSS 2 0 -5
 OP
 WIDTH OUT=80
 .END
1*******12/14/83 ********  SPICE 2G.6     3/15/83 ********20:07:08*****

OOPAMP

0****      MOSFET MODEL PARAMETERS                TEMPERATURE =    27.000 DEG C

0******************************************************************************


                  N              P
OTYPE             NMOS           PMOS
OLEVEL             2.000          2.000
OVTO               0.700         -0.700
OKP            6.04d-05       3.02d-05
OGAMMA             0.211          0.667
OPHI               0.576          0.695
OCGSO          3.50d-10       3.50d-10
OCGDO          3.50d-10       3.50d-10
OCJ            8.00d-05       2.00d-04
OMJ                0.500          0.500
OCJSW          5.00d-10       1.50d-09
OMJSW              0.550          0.500
```

Input of Bias Spice Simulation

```
ONEFF          30.000     30.000
1********12/14/83 ********  SPICE 2G.6     3/15/83 ********20:07:08*****

OOPAMP

0****      SMALL SIGNAL BIAS SOLUTION        TEMPERATURE =    27.000 DEG C

0******************************************************************************

  NODE    VOLTAGE     NODE    VOLTAGE     NODE    VOLTAGE     NODE    VOLTAGE

(  1)     5.0000    (  2)    -5.0000    (  5)     3.8292    (  7)    -4.7991

( 14)    -4.0384    ( 15)    -3.9848


     VOLTAGE SOURCE CURRENTS

     NAME         CURRENT

     VDD        -1.031d-04

     VSS         1.031d-04

     TOTAL POWER DISSIPATION   1.03d-03  WATTS
1********12/14/83 ********  SPICE 2G.6     3/15/83 ********20:07:08*****

OOPAMP

0****      OPERATING POINT INFORMATION       TEMPERATURE =    27.000 DEG C

0******************************************************************************


0
0**** MOSFETS

0              M11         M12         M13         M15         M17         M14         M16
0MODEL         N           N           N           N           N           P           P
 ID         5.85e-05    5.85e-05    2.93e-06    2.34e-05    1.83e-05    2.34e-05    2.12e-05
 VGS           9.038       1.015       0.962       1.015       0.814       7.814       0.
 VDS           9.038       0.962       8.829       1.015       8.628       8.985       1.171
 VBS          -0.962       0.          0.          0.         -0.201       8.985       1.171
 VTH           0.800       0.679       0.669       0.679       0.688      -0.651      -0.668
 VDSAT         7.638       0.291       0.257       0.292       0.114      -0.382      -0.367
 GM         1.43e-05    3.47e-04    2.00e-05    1.39e-04    2.90e-04    9.09e-05    8.49e-05
 GDS        2.65e-08    2.48e-06    3.81e-08    9.62e-07    4.01e-07    1.87e-07    5.34e-07
 GMB        6.91e-07    3.44e-05    1.89e-06    1.38e-05    2.49e-05    2.85e-05    2.74e-05
 CBD        0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00
 CBS        0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00
 CGSOVL     2.10e-15    3.50e-14    2.10e-15    1.40e-14    7.00e-14    1.40e-14    1.40e-14
 CGDOVL     2.10e-15    3.50e-14    2.10e-15    1.40e-14    7.00e-14    1.40e-14    1.40e-
 CGBOVL     0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00
 CGS        6.89e-13    3.11e-13    1.86e-14    1.24e-13    6.22e-13    0.  e+00    0.  e+00
 CGD        0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00    1.24e-13    1.24e-13
 CGB        0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00    0.  e+00
0
          JOB CONCLUDED
```

```
.MODEL N     NMOS LEVEL=2
+  VTO=0.7
+  CGSO=350P        CGDO=350P
+  CJ=80U           MJ=0.5          CJSW=500P       MJSW=0.55
+  TOX=40N          NSUB=1.0E15     TPG=+1
+  XJ=600N          LD=300N         UO=700
+  VMAX=50K         NEFF= 30
.MODEL P     PMOS LEVEL=2
+  VTO=-0.7
+  CGSO=350P        CGDO=350P
+  CJ=200U           MJ=0.5          CJSW=1500P       MJSW=0.5
+  TOX=40N          NSUB=1.0E16     TPG=+1
+  XJ=600N          LD=300N         UO=350
+  VMAX=50K         NEFF= 30
M1 6 3 8 1 P W=200U L=6U
+AD=2000P AS=600P PD=300U PS=300U
M2 6 4 9 1 P W=200U L=6U
+AD=2000P AS=600P PD=300U PS=300U
M3 5 8 2 2 N W=20U L=10U
+AD=200P AS=100P PD=30U PS=30U
M4 7 8 2 2 N W=20U L=10U
+AD=200P AS=100P PD=30U PS=30U
M5 1 5 6 1 P W=40U L=6U
+AD=400P AS=60P PD=60U PS=60U
M6 1 5 11 1 P W=100U L=6U
+AD=1000P AS=60P PD=150U PS=150U
M7 11 5 2 2 N W=100U L=10U
+AD=1000P AS=100P PD=150U PS=150U
M8 1 5 12 1 P W=200U L=6U
+AD=2000P AS=60P PD=300U PS=300U
M9 12 11 2 12 P W=500U L=6U
+AD=5000P AS=60P PD=750U PS=750U
M10 7 1 10 2 N W=6U L=20U
+AD=60P AS=200P PD=10U PS=10U
CC 10 11 6P
RI 10 11 10000MEG
VDD 1 0 5
VSS 2 0 -5
VBS 5 0 3.8292
V4 4 0 0
V3 3 0 0 AC 1
CL 12 0 20P
 AC DEC 5 100 10000MEG
.PLOT AC VDB(12,0)
.PLOT AC V(12,0) VP(12,0)
.NODESET V(10)=-3.8776
 WIDTH OUT=80
 END
```


Input of Opamp Simulation

1********12/14/83 ******** SPICE 2G.6 3/15/83 ********20:04:05******

OOPAMP

0**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

0**********

OLEGEND:

*: V(12)
+: VP(12)
X

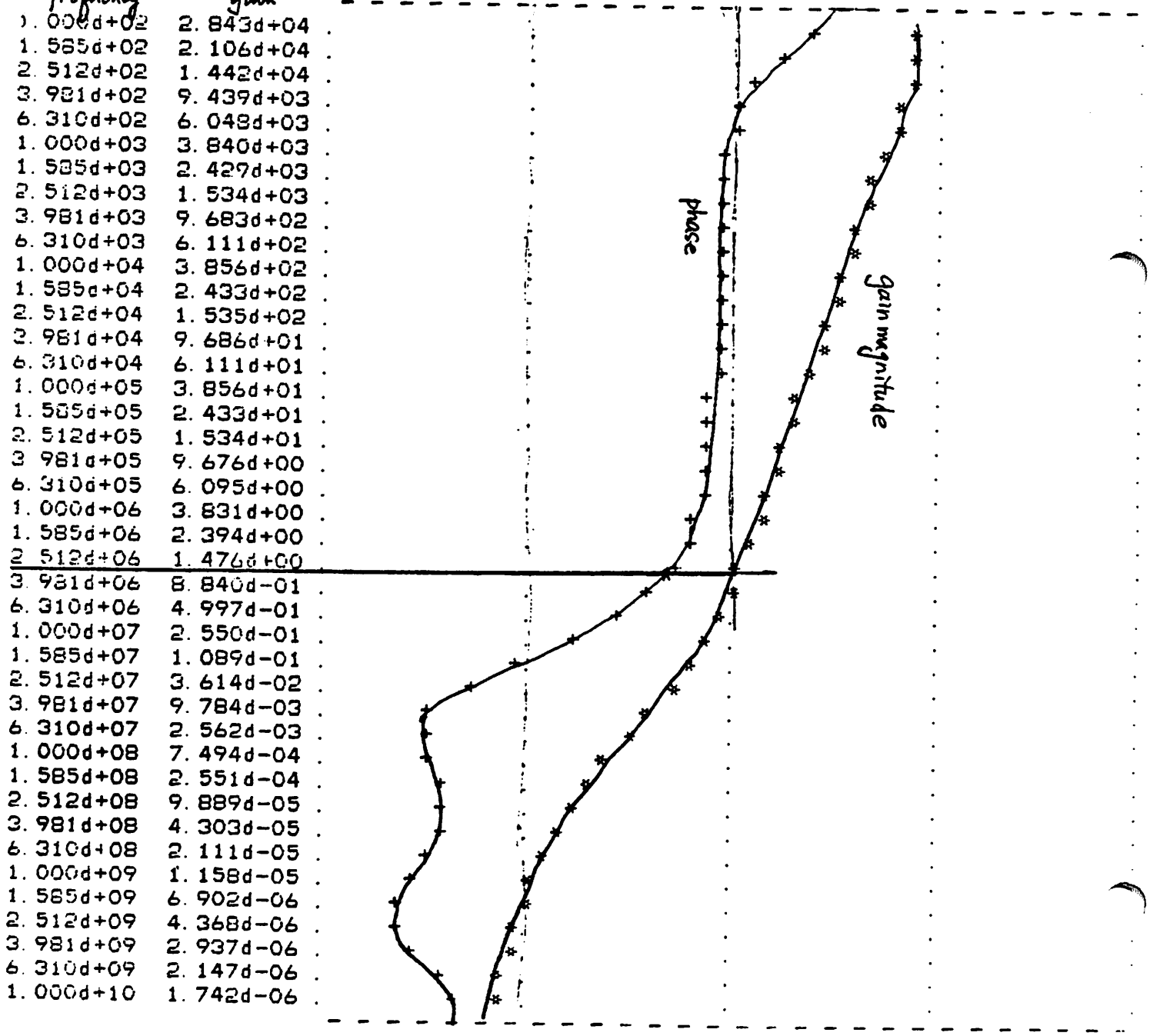
FREQ	V(12)
1.000d+02	2.843d+04
1.585d+02	2.106d+04
2.512d+02	1.442d+04
3.981d+02	9.439d+03
6.310d+02	6.048d+03
1.000d+03	3.840d+03
1.585d+03	2.429d+03
2.512d+03	1.534d+03
3.981d+03	9.683d+02
6.310d+03	6.111d+02
1.000d+04	3.856d+02
1.585d+04	2.433d+02
2.512d+04	1.535d+02
3.981d+04	9.686d+01
6.310d+04	6.111d+01
1.000d+05	3.856d+01
1.585d+05	2.433d+01
2.512d+05	1.534d+01
3.981d+05	9.676d+00
6.310d+05	6.095d+00
1.000d+06	3.831d+00
1.585d+06	2.394d+00
2.512d+06	1.476d+00
3.981d+06	8.840d-01
6.310d+06	4.997d-01
1.000d+07	2.550d-01
1.585d+07	1.089d-01
2.512d+07	3.614d-02
3.981d+07	9.784d-03
6.310d+07	2.562d-03
1.000d+08	7.494d-04
1.585d+08	2.551d-04
2.512d+08	9.889d-05
3.981d+08	4.303d-05
6.310d+08	2.111d-05
1.000d+09	1.158d-05
1.585d+09	6.902d-06
2.512d+09	4.368d-06
3.981d+09	2.937d-06
6.310d+09	2.147d-06
1.000d+10	1.742d-06

(*)---------- 1.000d-10 1.000d-05 1.000d+00 1.000d+05 1.000d+

(+)---------- -1.000d+02 0. d+00 1.000d+02 2.000d+02 3.000d+

frequency

gain



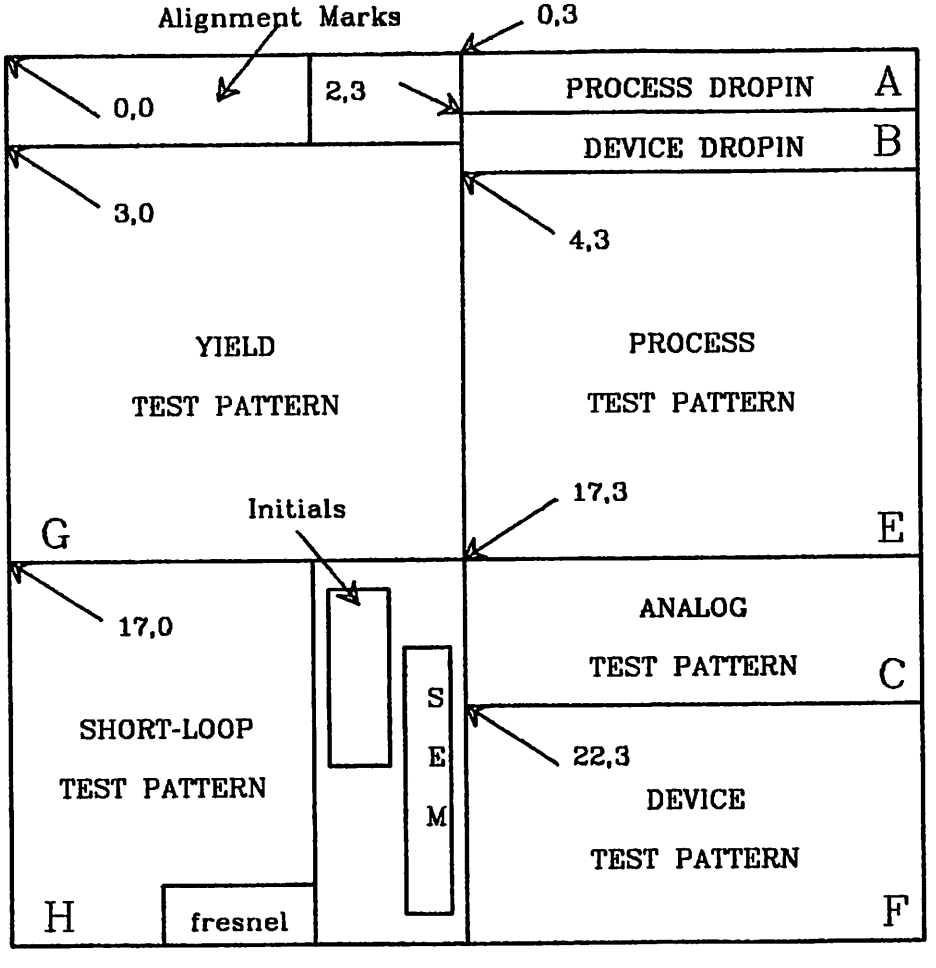
EE290 TEST CHIP ORGANIZATION

The EE290 test chip is made up of 7 Test Patterns plus a separate section for alignment marks. The 7 Test Patterns are: Device, Device Drop-in, Process, Process Drop-in, Shortloop, Yield, and Analog. Each test pattern consists of a collection of functional units. A functional unit is made up of several blocks which together accomplish a specific goal. These blocks are 320um x 1600um. Each block may contain a 2 x 10 array of 80um pads on 160um centers. A block does not always contain all 20 pads since some test structures require a large area, however the pads which are present will remain on the 160um grid. The pad numbering convention is shown below. Pad #1 contains a small notch in it to help distinguish top from bottom when viewing the chip through a microscope. The entire EE290 chip is a 6 row, 30 column array of blocks.

1	11
2	12
3	13
4	14
5	15
6	16
7	17
8	18
9	19
10	20

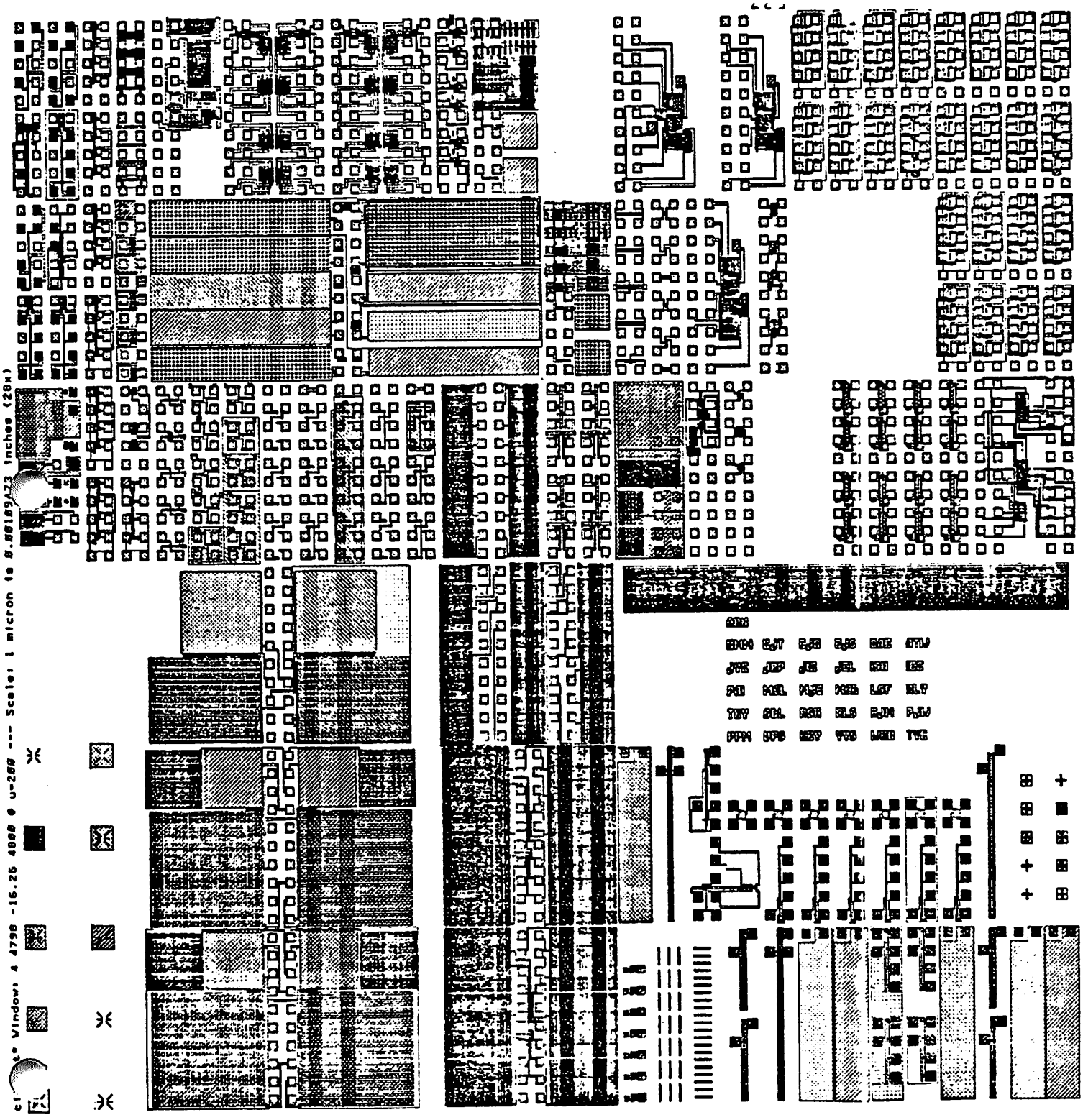
The testing of the devices can be accomplished with a 2 x 5 probe card. Some of the test patterns must be tested with a 2 x 10 probe card due to unconventional pad assignments and the inability to constrain the test structure to a 2 x 5 sub-block.

BERKELEY CMOS PROCESS TEST CHIP



testchip.cif

Entire EE290 Test Chip



BERKELEY CMOS PROCESS
YIELD TEST PATTERN

Long-Shen Fang
Kwang-Leei Konrad Young

(revised by)
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Steve Lester
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and Computer Sciences
Berkeley, California

REV 0.0
(Spring 1984)

Yield Test Pattern
Table of Contents

DISCUSSION

Yield Test Pattern

Gate Oxide Integrity

To evaluate gate oxide defect density, we assume that defects follow a Poisson distribution, then the probability of having n defects is

Pr(x=n) = [exp(-lambda) * (lambda**n)] / [n!]

where ** means "raised to the power of" . Lambda is the number of defects in that area, i.e. lambda = rho*A, where rho is the defect density per unit area and A is the area.

The probability that the gate oxide is defective is

Pr(x>0) = 1 - Pr(x=0)

= 1 - [exp(-lambda) * (lambda**0) / (0!)]

= 1 - exp(-rho*A)

Typical MOS processes have gate oxide defect density ranging from 10 to 100 defects/cm**2. In our test pattern, we choose a pattern of 500um by 500 um, which gives:

for rho = 10/cm**2 and lambda = 0.025

Pr(x>0) = 1 - exp(-0.025) = 0.0247

and for rho = 100/cm**2 and lambda = 0.25

Pr(x>0) = 1 - exp(-0.25) = 0.2212

Thus the probability of the gate oxide being defective ranges from 2.47% to 22.12%. This means that we should get one defective pattern out of five to forty patterns, which is a reasonable number.

PN Junction Leakage

In the integrated circuit process, junction leakage can be due to crystal defects and contamination. It is important to be able to identify leakage from different sources so that the cause of leakage can be traced. Typical leakage currents range from 1 nA/cm**2 to 10 nA/cm**2. The area chosen for the pn junction diode is 0.005075 cm**2 . This give currents of 5.075 to 50.75 pA, which is easily measured by an electrometer.

Metal Fault Density

A yield model should include the following facts:

1). Different defects from different mechanisms contribute to the whole yield function.

2). The defect density varies from chip to chip, and depends on its location on the wafer and other process factors.

3). The defect density depends on the design rules used in the design of a specific circuit.

4). The yield is a function of the circuit under discussion.

If we assume a binominal distribution and use a constant defect density (uniform defect density) and keep the defect number constant in the limiting process, we got a Poisson distribution, which is an exponentially decreasing function as was shown in an earlier section. But it is usually too pessimistic using this approach.

As pointed out by recent papers a more physical assumption is to use the Gamma function for the defect density distribution:

```
f(D) = [1 / {GAMMA(alpha) * (beta**alpha) }] *
                    [D**(alpha - 1)] * [exp(-D/beta)]
```

where alpha and beta are the two distribution parameters, and ** means "raised to the power of".

Thus the probability of having no defects on a chip is

```
Y = Po = [1 / {(A*beta + 1)**alpha}]

       = 1 / {(1 + S*A*Do)**(1/S) }
```

where S = 1/alpha .

The above formula is rather general. In the limiting case of S~0, it will become the Poisson yield function, which can be shown to be approximately true when we have extremely low defect densities.

To simplify the yield model without being pessimistic, and to meet requirement (2) above, we will assume a triangular density distribution which leads to the Murphy's law:

```
Y = { [(1 - exp(-Do*A)] / (Do*A) }**2
```

Thus a less pessimistic estimation of yield is obtained.

To meet requirement (1) above we must consider multiple types of defects with the gamma yield function, the overall yield is then the product of the yield for each type of defect:

```
Y = PROD [(1 + Sn*An*Dno)**(-1/Sn)]
```

where PROD means "the product of, from n=1 to n=N" . Fact (4) enters as the "An" terms. When the yield is high, Sn*An*Dno << 1, therefore,

```
ln(Y) = SUM [(-1 /Sn) * ln(1 + Sn*An*Dno)]
```

where SUM means "the sum of, from n=1 to n=N" .

Since $\ln(1 + Sn*An*Dno) \sim Sn*An*Dno$, we have

$\ln(Y) = SUM\ [-An*Dno]$

Thus

$Y = \exp[-SUM\ (An*Dno)] = \exp(-A*Dbar)$

SUMMARY TABLE
Yield Test Pattern

Filename Sz-(Blks)	Structure	Purpose	Coordinates within 290n chip	Test Pat.	Func. Unit
gc0r0OXNW 9	capacitors	Gate oxide integrity on N-well	c3r0	c0r0	c4r0
gc0r1OXPW 9	capacitors	Gate oxide integrity on P-well	c3r1	c0r1	c4r1
gc0r2PNLEAK1 9	PN junction	PN junction leakage N-well	c3r2	c0r2	c4r2
gc9r0MPA 5	Serpentine & Comb	detect opens & shorts metal over polysilicon	c12r0	c10r0	c10r0
gc9r1MP 5	Serpentine & Comb	detect opens & shorts metal over poly & diff.	c12r1	c12r1	c12r1
gc9r2MC 5	contact chain metal to poly metal to N+ metal to P+	contact fault density	c12r2	c9r2	c10r2 c12r2 c12r2

FUNCTIONAL DESCRIPTION

Yield Test Pattern

Gate Oxide Integrity on N-well & P-substrate

Filenames:

gc0r00XNW (Nwell bottom plate)

gc0r10XPW (P-substrate bottom plate)

Purpose:

To evaluate the gate oxide defect density

Description:

The gate oxide integrity test patterns are designed with different gate edge and isolation edge lengths. In this structures the effects of gate edge and isolation edge on the gate oxide integrity can be evaluated. Devices 1, 3, and 5 are to measure isolation edge effects, while devices 2, 4, and 6 are to measure gate edge effects.

In the following descriptions, the first name describes the P-substrate filename and the following name in ()'s describe the Nwell filename.

1) ox500.1 (ox5001N) is a large square capacitor (500um x 500um). In this structure, there will be no effect due to gate edge, and only isolation edge is possible.

2) ox500.2 (ox5002N) is also a large square capacitor (500um x 500um). However, only the gate edge is exposed.

3) ox500.3 (ox5003N) has 2500 squares with 10um a side. The total active area is the same as ox500.1 and 0x500.2, but the isolation edge length is increased from 2000 microns to 100,000 microns. There are also a lot of corners used to evaluate the effect of corners on gate oxide integrity.

4) ox500.32 (ox5003N.32) has 2500 squares with 5 um a side. The area is one quarter of the area of ox500.3. In this sturcture, only gate edge is exposed. There are a lot of corners to evaluate the corner effect on the gate oxide integrity.

5) ox500.4 (ox5004N) has the same periphery edge length as ox500.3, but there are less corners. The area is twice that of other test pattern due to the need to keep the periphery length the same as ox500.3.

6) ox500.42 (ox5004N.42) has the same periphery edge length as ox500.32 with less corners. The area is one quarter of the area of ox500.4.

Testing:

Standard Capacitance Measurement.

Pad Assignment:

PAD #	filename	AREA (sq um)	PERIMETER (um)
Nwell Capacitors (gc0r00XNW)			
14,3	ox5001N	250,000	2000
12,3	ox5002N	250,000	2000
18,8	ox5003N	250,000	100,000
13,3	ox5003N.32	62,500	50,000
19,8	ox5004N	495,000	100,000
11,3	0x5004N.42	123,750	50,000
P substrate Capacitors (gc0r10XPW)			
14,3	ox500.1	250,000	2000
12,3	ox500.2	250,000	2000
18,8	ox500.3	250,000	100,000
13,3	ox500.32	62,500	50,000
19,8	ox500.4	495,000	100,000
11,3	0x500.42	123,750	50,000

NOTE: Pad #'s 2, 10, 12, and 20 are contacts to the Nwell.

PN junction leakage test

Filename:

gc0r2PNLEAK1

Purpose:

To check junction leakage

Description:

The test patterns are described as follows:

1) pn712.5.1 (pn71251N) is a square pn junction diode (712.5um x 712.5um).

2) pn712.5.2 (pn71252N) has the same area as pn712.5.1, but is laid out in a finger-like manner to increase the periphery length of the isolation edge.

Pad Assignment:

PAD #	filename	AREA(sq um)	PERIMETER (um)
Nwell Capacitors			
16+,8- 19+,8-	pn71251N pn71252N	507656 507900	2850 101580
P substrate Capacitors			
7+,17- 7+,18-	pn712.5.1 pn712.5.2	507656 507900	2850 101580

Metal Fault Density

Filenames:

mop, msp, mopa, mspa

Purpose:

To determine the metal fault density.

Description:

The test pattern is made up of four parts:

1) mop consists of serpentined metal over polysilicon and field oxide with a total of 32,000 metal steps created by an array of poly lines. The metal is of minimum feature size according to our design rule (35 lambda), and the total length of metal is 101800 microns.

2) msp consists of two interwoven metal combs, and are made of minimum geometry metal wire as above and the spacing between adjacent lines is 65 lambda. The total adjacent parts of the two combs is made approximately the same length as in mop. This structure is dedicated to the test of shorts due to etching, patterning, etc.

3) mopa is also of serpentine metal with minimum features, the difference with mop is that it subjected to two steps of field oxide to poly and poly to diffusion, and thus has a more stringent test than mop. It has the same length as mop and has 16,660 pairs of steps.

4) mspa is a comparison to msp to see whether the added steps also influence the short fault density.

Testing:

OPENS:
A common reference point is chosen at the "end" of the serpentine. A current is forced through the serpentine at 4 possible locations. The voltage is sensed. If it is low, no opens have occurred. If it is high, opens exist in the structure, indicating a fault. Taps to the structure are placed at 1/8, 1/4, 1/2, and full distance from the reference tap.

SHORTS:
A common reference point is chosen at one side of the comb structure. A voltage is forced at the other end of the comb. Four different combs with varying number of "teeth" exist. The current is sensed. If it is low, no shorts have occurred. If it is high, this indicates a short has occured. Four different comb structures exist within each 2-block area. This allows areas of 1/8, 1/8, 1/4, and 1/2 of the total 2-block area to be tested.

Pad Assignment:

PAD #	DESCRIPTION	FUNCTION
OPENS		
2	Common Reference	Ground
11	10 Serpentines	Force I, Sense V
12	22 Serpentines	Force I, Sense V
13	~42 Serpentines	Force I, Sense V
14	~84 Serpentines	Force I, Sense V
SHORTS		
7	Common Reference	Ground
16	11 Combs	Force V, Sense I
17	11 Combs	Force V, Sense I
18	~22 Combs	Force V, Sense I
19	~44 Combs	Force V, Sense I

Metal Contact

Filenames:

mopl, mcnn, mcpp

Purpose:

To determine the fault density of metal contacts.

Description:

The following three stuctures are included:

1) mcpl is the metal to polysilicon contact test pattern. There are ~1664 poly pieces, each with two contacts. Thus, ~3328 poly to metal contacts are obtained. The contact size is 15 lambda (lambda = 0.1um), with 12 lambda metal and 16 lambda poly extention in all four directions.

2) mcmm is the metal to N+ contact. It also consists of ~1664 diffused areas with two contacts each, yielding ~3328 metal to diffusion contacts with 12 lambda metal and 8 lambda of N+ diffusion in all four directions.

3) mcpp is the same sa 2) above with P+ instead of N+ diffusion.

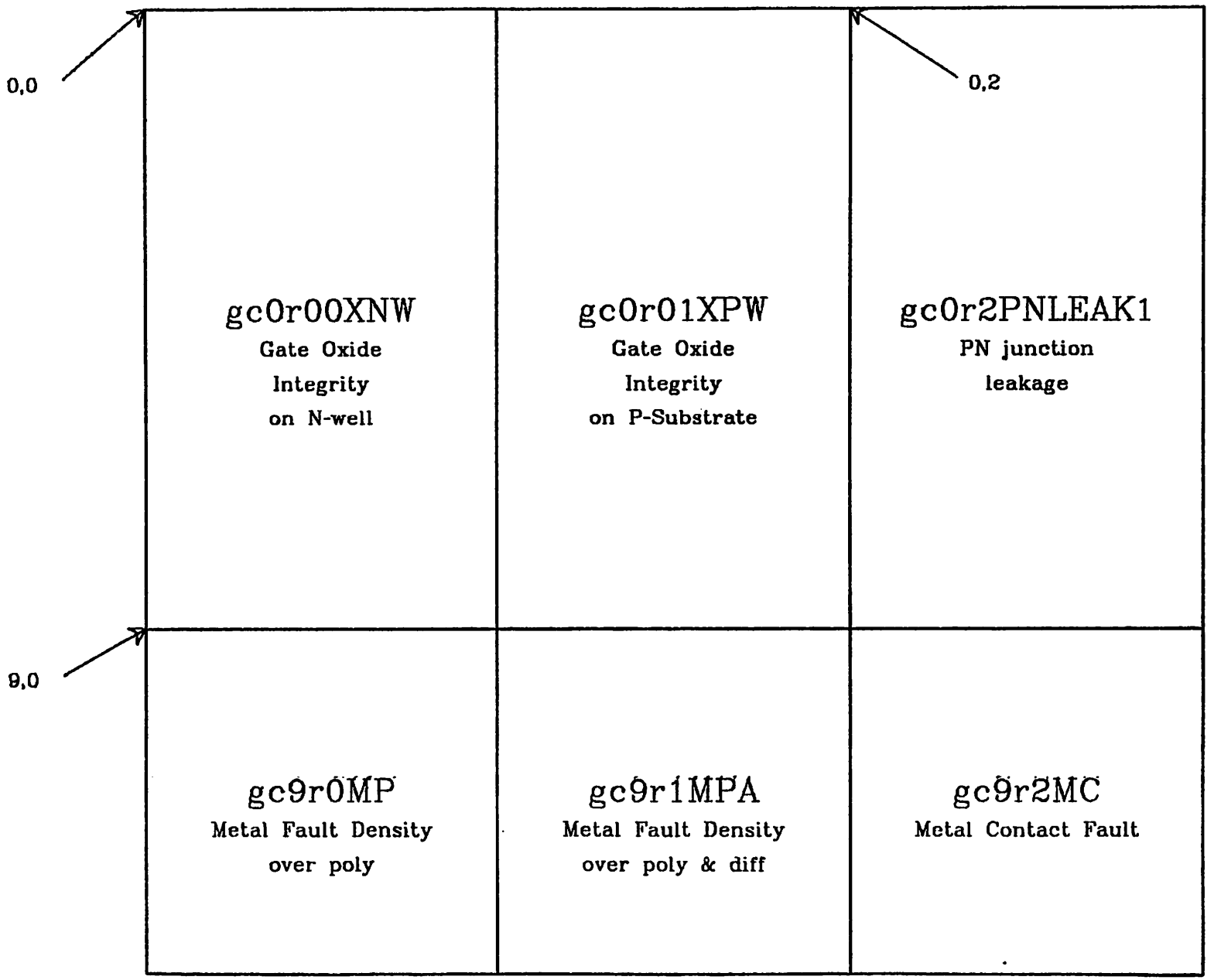
Testing:

A current is forced through the contact chain. If a high voltage results across the contact chain, an open circuit has occurred and hence a fault. A low voltage is expected for an operative chain.

Pad Assignment:

PAD #	DESCRIPTION	FUNCTION
POLY		
2	Reference Pad	Ground
11	416 contacts	Force I, Measure V
12	832 contacts	Force I, Measure V
13	1664 contacts	Force I, Measure V
14	3328 contacts	Force I, Measure V
N+		
2	Reference Pad	Ground
11	416 contacts	Force I, Measure V
12	832 contacts	Force I, Measure V
13	1664 contacts	Force I, Measure V
14	3328 contacts	Force I, Measure V
P+		
7	Reference Pad	Ground
19	416 contacts	Force I, Measure V
18	832 contacts	Force I, Measure V
17	1664 contacts	Force I, Measure V
16	3328 contacts	Force I, Measure V

YIELD TEST PATTERN FLOORPLAN



cifplot* \ ow: 112.5 2235.1 Ø 2396 @ u=2ØØ --- Scale: 1 micron Ø.ØØ19 inches (48x)

gsubchip.cif

Yield test pattern

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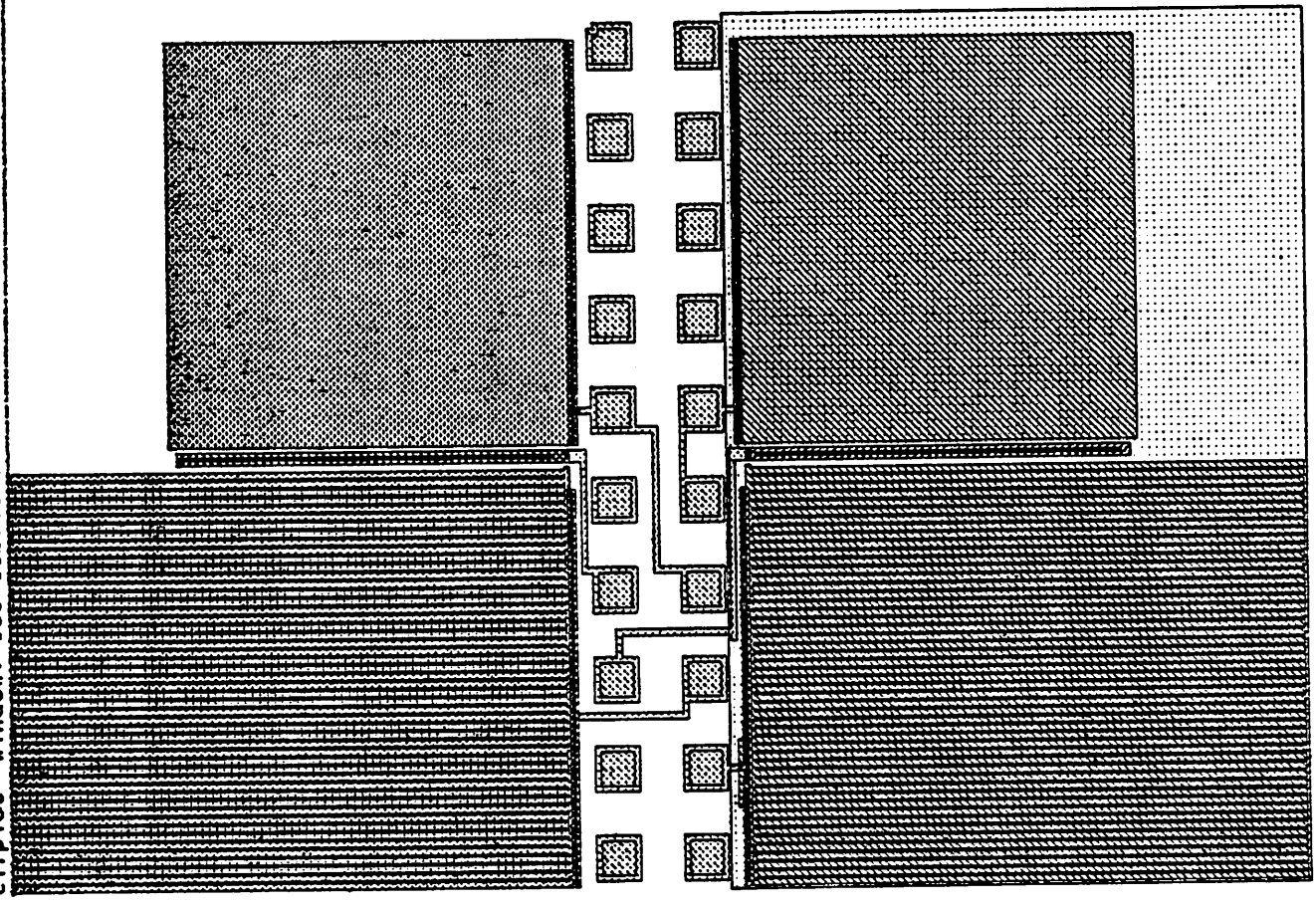
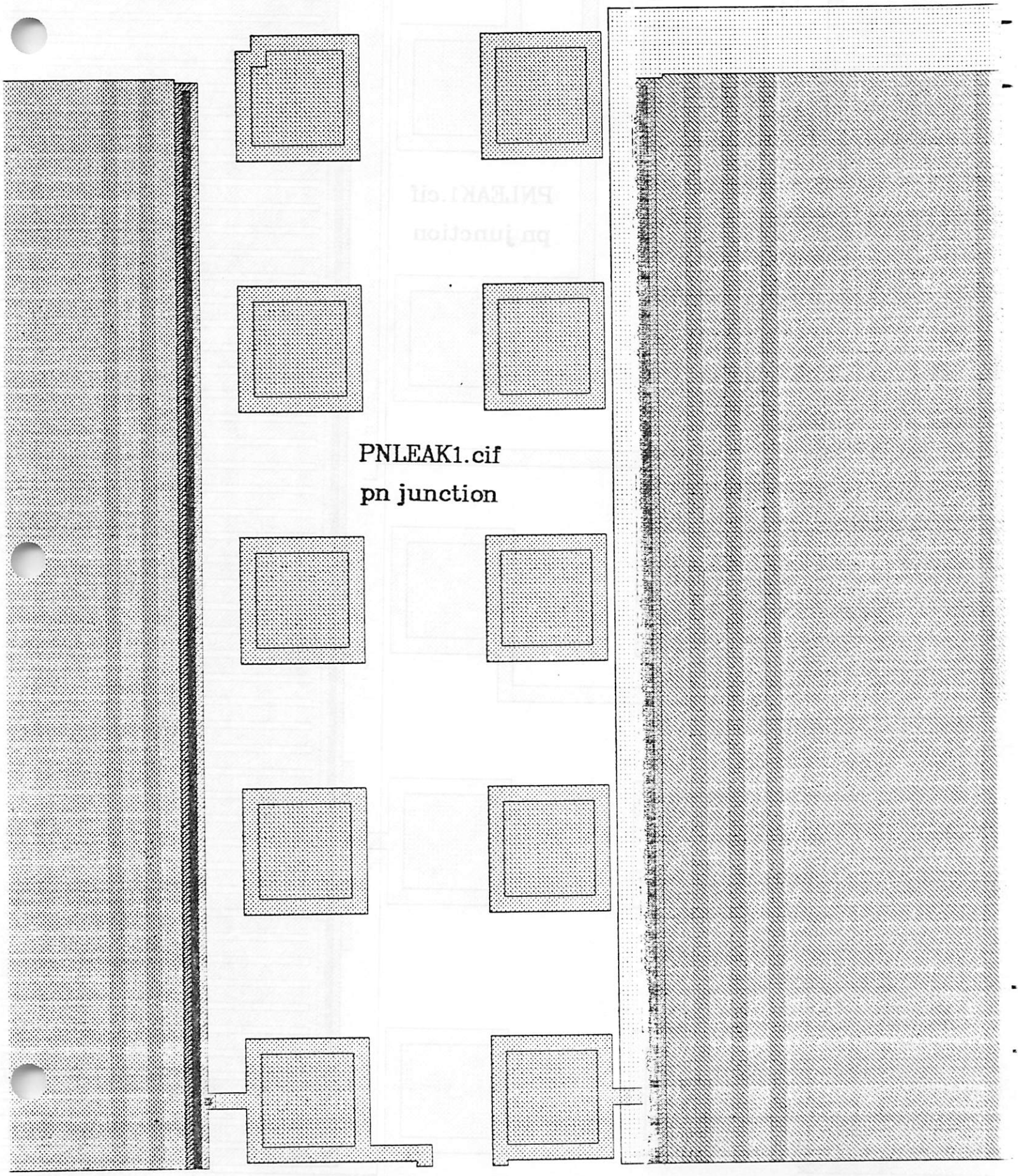
PNLEAK1.cif

pn junction




PNLEAK1.cif
pn junction

PNLEAK1.cif
pn junction

OXPW.cif

capacitors

OXPW.cif
capacitors

OXPW.cif
capacitors

OXNW.cif

capacitors

OXNW.cif
capacitors

OXNW.cif
capacitors

gc9r2

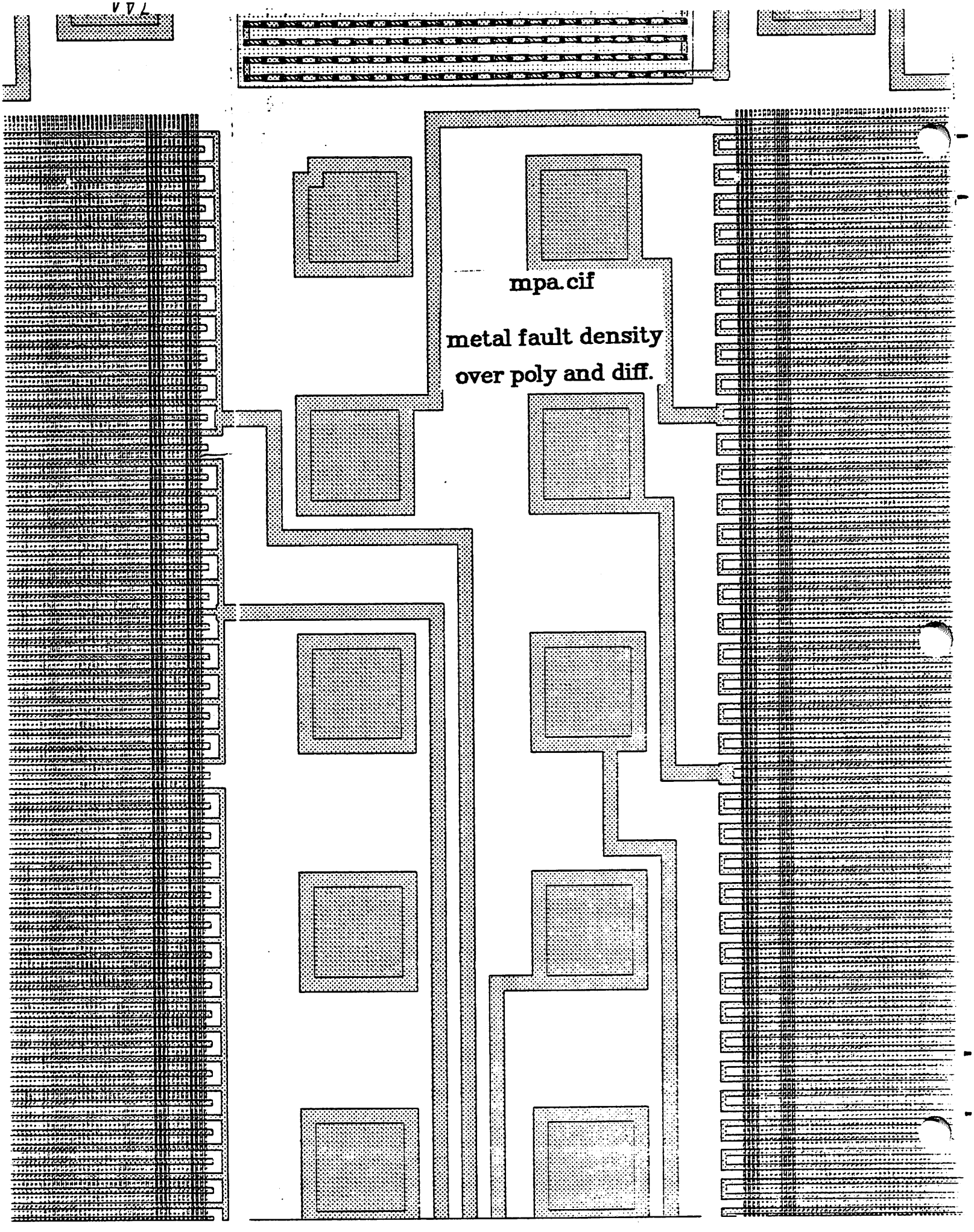
metal contact fault

gc9r2

metal contact fault

mpa.cif

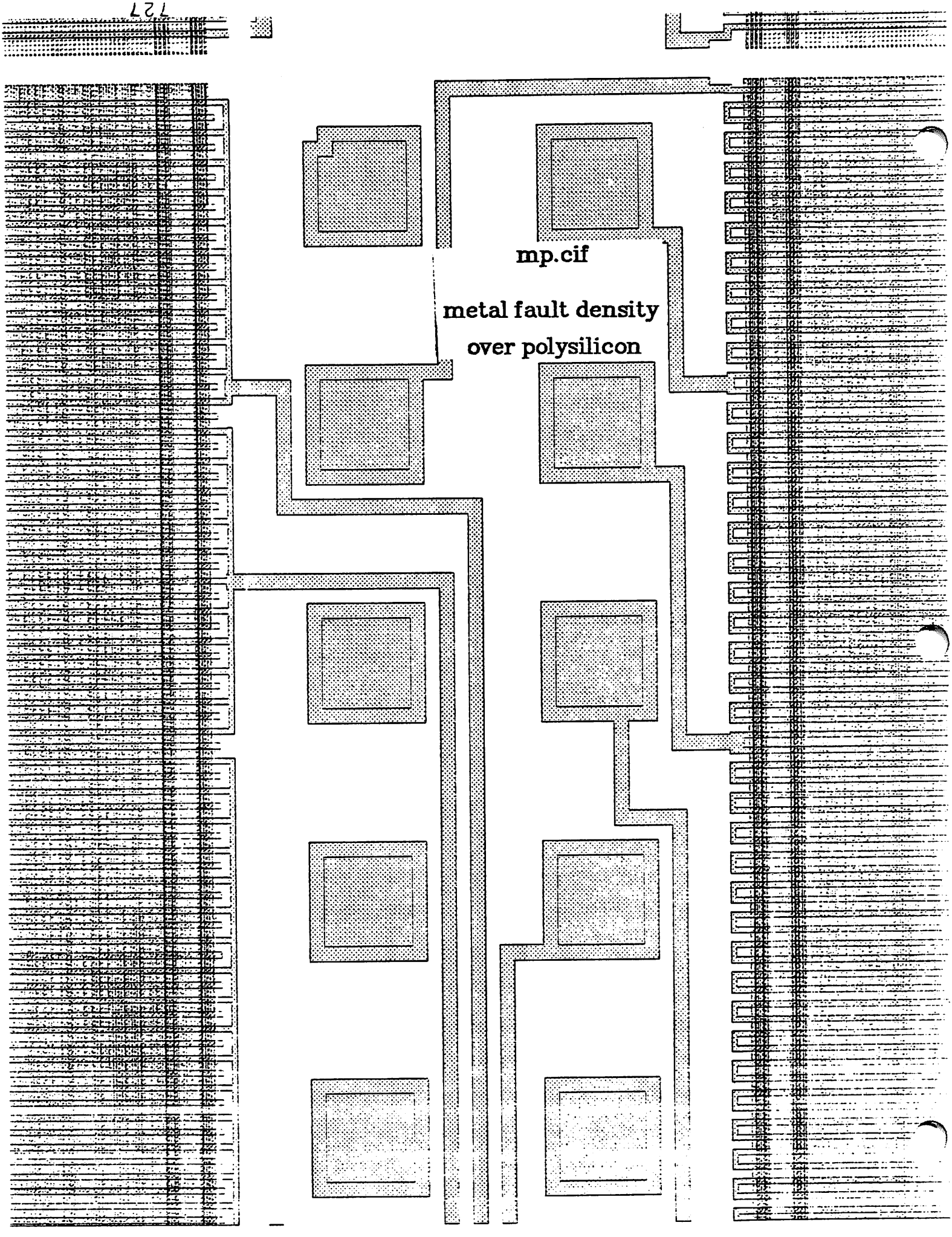
metal fault density
over poly and diff.


mpa.cif
metal fault density
over poly and diff.

mp.cif

metal fault density

over polysilicon


mp.cif
metal fault density
over polysilicon

Yield Test Pattern (gsubchip)
Cif File Cell Hierarchy

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  ox5003N.k ox5004N.42.k ox5004N.k

OXPW.k
  PADSET.k metlchange1.k ox500.1.k ox500.2.k
  ox500.3.k ox500.4.k ox500.42.k

PAD.k

PADSET.k
  PAD.k

PNLEAK1.k
  PADSET.k pn712.5.1.k pn712.5.2.k pn71251N.k pn71252N.k

actv.k

actv10.k

actv10n.k

actv10x.42.k

actv10x990.k

actv10x990n.k

actv10xn.42.k

actvzigzag.k

actvzigzagn.k

cont.k

contline.k
  pair.k

contlines.k
  contline.k pair.k

cpolyline.k
  polypair.k

cpolylines.k
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gsubchip.k
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konrad.k
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  polylines.k template.k

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mcpl.k
  PADSET.k contlines.k cpolylines.k

mcpp.k
  contlines.k plines.k

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pn71252N.k
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polyline.k

polylines.k
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polypair.k

ppair.k

template.k

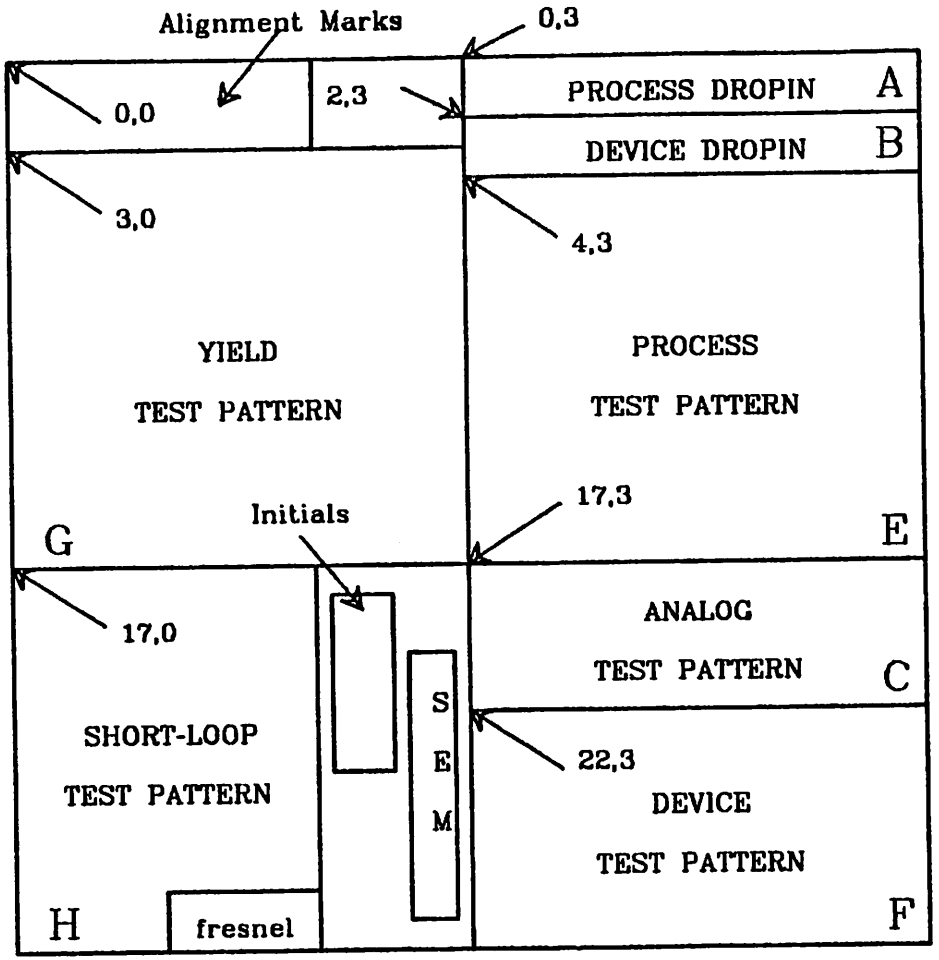
EE290 TEST CHIP ORGANIZATION

The EE290 test chip is made up of 7 Test Patterns plus a separate section for alignment marks. The 7 Test Patterns are: Device, Device Drop-in, Process, Process Drop-in, Shortloop, Yield, and Analog. Each test pattern consists of a collection of functional units. A functional unit is made up of several blocks which together accomplish a specific goal. These blocks are 320um x 1600um. Each block may contain a 2 x 10 array of 80um pads on 160um centers. A block does not always contain all 20 pads since some test structures require a large area, however the pads which are present will remain on the 160um grid. The pad numbering convention is shown below. Pad #1 contains a small notch in it to help distinguish top from bottom when viewing the chip through a microscope. The entire EE290 chip is a 6 row, 30 column array of blocks.

1	11
2	12
3	13
4	14
5	15
6	16
7	17
8	18
9	19
10	20

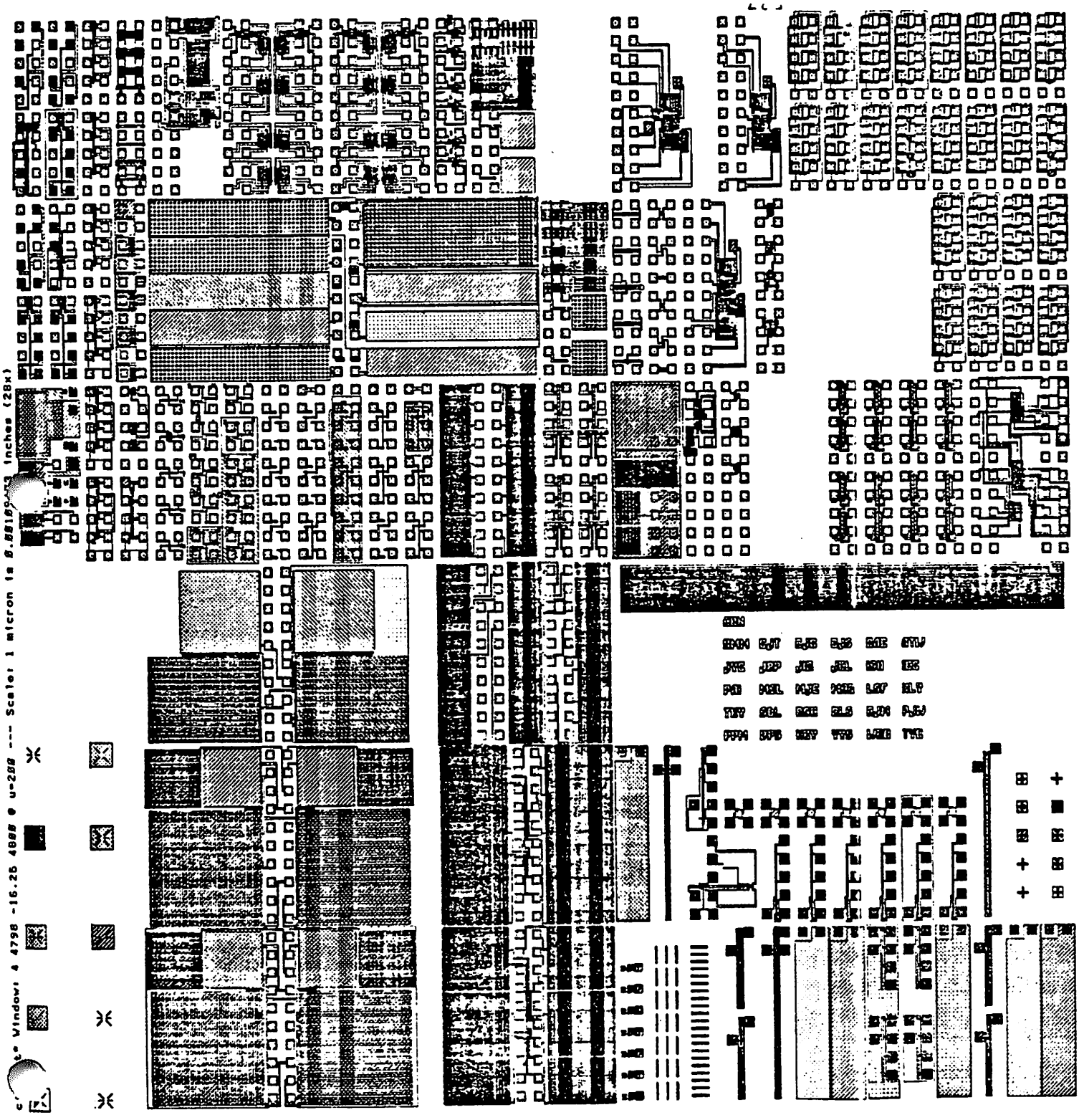
The testing of the devices can be accomplished with a 2 x 5 probe card. Some of the test patterns must be tested with a 2 x 10 probe card due to unconventional pad assignments and the inability to constrain the test structure to a 2 x 5 sub-block.

BERKELEY CMOS PROCESS TEST CHIP



testchip.cif

Entire EE290 Test Chip



Shortloop Test Pattern
Table of Contents

DISCUSSION

Short Loop Test Pattern

Abstract

A set of test patterns has been developed which allows "in process" evaluation of important physical parameters. Test categories include dielectric evaluation, linewidth and sheet resistance, layer alignment, and MOS device characteristics.

The purpose of the short loop test chip is twofold:

(1) to provide a way of evaluating critical physical and electrical parameters before a full process run is complete,

(2) and to make fully testable devices outside of the full process using as few masking steps as possible.

These abilities will enable process and device designers to evaluate their ideas without going to the trouble and expense of putting a wafer through the entire fab process.

Our goal in the project was to design a simple and versatile set of devices to use the short loop method while paying particular attention to the availability of automated test equipment.

The device types are categorized in two general groups, visual test sites and electrical test sites. Visual test patterns are particularly well suited to this chip because only one or two masking steps are required for their fabrication. They require no extra steps in the full process, and they may be inspected at any point in the process after they are made. However, their use is limited to resolution and alignment measurements. The main disadvantage of the visual tests is that we currently have no automated test equipment to perform the inspection. This means that testing enough sites to get a statistically meaningful sample size will be prohibitively time consuming.

The strengths of the electrical test sites are, fortunately, the weaknesses of the visual sites. The tests include alignment and resolution, sheet resistance, dielectric evaluation, surface state evaluation, and MOS device characteristics. However, the electrical test devices are harder to implement with the short loop method. One to four masking steps are generally required to produce a test site. Many sites require a special contact masking step before they may be tested. P-channel devices in our process are particularly poorly suited to the short loop method because the n-well fabrication necessary for their use is a major time burden. For this reason, n-channel devices have been used wherever possible. Of course the great advantage of the electrical test devices is that automated testing may be used.

Test Types

Following is a summary of the information which may be garnered from the devices. Listed with the general test areas are the names of the particular sites which are useful in measuring parameters related to that area. These tests cover the important aspects of process development. Detailed information on the individual test patterns is in the device catalogue.

ALIGNMENT

Verniers (optical): can determine the alignment between any two layers

Al-poly: finds the alignment of the polysilicon to the active areas.

Al-cont: finds the alignment of the metal contacts to the conducting layers.

CONTACT CHARACTERIZATION

Butting Contact: A chain of butting contacts to n-active regions.

Cont Chain: Active area to active area contact chain.

INSULATOR QUALITY

All Capacitor patterns: These are capacitor patterns which include all conducting layers and all oxide regions.

MOS DEVICE CHARACTERISTICS

Nmos1, Pmos1: 4 n-channel and 4 p-channel devices

Nmos2, Pmos2: same as Nmos1 and Pmos1 with the addition of a special mask which may be used to block implants, etch oxide, etc.

PATTERN CONTINUITY AND SHORTS

Metal continuity

Metal shorts

Poly continuity

Poly shorts

RESISTIVITY

All Van der Pauws: Will find sheet resistance (Rs) of each conducting layer.

SPACING/RESOLUTION

Elbows (optical): Measures the resolution of all layers

All Van der Pauws: finds the spacing and resolution of all conducting layers with the possible exception of metal.

These tests cover the important aspects of process development. Detailed information on the individual test patterns is given in the document.

Design notes

Many of the devices on this chip are similar to those on other test chips, particularly device and process characterization. The difference is that the layout of our devices enables them to be tested before processing is completed. Most contact pads are laid out in the material which is intended to be contacted. For example, the contacts for the gates of the MOS devices are made of poly. This may be done whenever the IR drop in the contact lines will not affect the accuracy of the testing, and it eliminates the necessity of the passivation, contact, and metallization procedures. It is questionable whether or not this will

work with the diffused layers, so an extra contact level, CON1, has been laid out for those layers. CON1 is also laid out for contact pads which are covered with a thin oxide at the time of their fabrication. Another additional mask, PROTECT, was laid out for half of the NMOS and PMOS devices. Using this mask the devices may be shielded from implants or have their oxide dipped back. They may then be compared with the non-masked devices.

For the p-channel devices there is no difference between the full and short loop processes, so no short loop plan is given. We tried to include only devices which could be made in a short loop, as anything which requires the full process really belongs on another test chip.

Conclusions

The devices on this chip should handle a large proportion of the process and device characterization needs. It is suggested that several more patterns which allow electrical inspection of the alignment of the n-well to the active areas and to the isolation be designed and added. Many of the patterns require the isolation and active area definition steps. Once the process has been finalized through those steps it would be a good idea to prepare several wafers up to that point and keep them on hand to be finished with the desired short loop steps. This will greatly reduce the short loop turnaround time.

Through some clever re-designing of devices on other test chips it may be possible to incorporate the short loop sites on those chips, thus saving a great deal of space. A short loop "drop in" may also be desirable.

SUMMARY TABLE
Shortloop Test Pattern

Filename Sz-(Blks)	Structure	Purpose	Coordinates within 290n chip	Test Pat.	Func. Unit
ELBOWS					
hc00r0 1	visual linewidth	measure vert. and horz. linewidth	c17r0	c0r0	c0r0
VERNIERS					
hc01r00 2	alignment verniers	visual alignment of 2 layers	c17r1	c1r0 c1r1	c1r0 c1r1
CAPACITORS					
hc05r0 1	metal-field capacitor	capacitance, edge effects	c22r0	c5r0	c5r0
hc06r0 1	metal-poly capacitors	capacitance, edge effects	c23r0	c6r0	c6r0
hc09r0 1	poly-diffused capacitor	capacitance, edge effects	c26r0	c9r0	c9r0
hc11r0 1	poly-field capacitors	capacitance, edge effects	c28r0	c11r0	c11r0
hc12r0 1	poly-n type gate oxide capacitor	capacitance, edge effects	c29r0	c12r0	c12r0
hc00r1 1	poly-p type gate oxide capacitor	capacitance, edge effects	c17r1	c0r1	c0r1

SUMMARY TABLE
Shortloop Test Pattern

Filename Sz-(Blks)	Structure	Purpose	Coordinates within 290n chip	Test Pat.	Func. Unit
SHORT DETECTION					
hc04r0 1	interlocking combs of metal	short circuit detection	c21r0	c4r0	c4r0
hc01r1 1	interlocking combs of metal & poly	short circuit detection	c18r1	c1r1	c1r1
CONTINUITY					
hc03r0 1	Serpentine w/ & w/o steps	continuity of metal layer	c20r0	c3r0	c3r0
hc10r0 1	Serpentine w/ & w/o steps	continuity of poly layer	c27r0	c10r0	c10r0
ALIGNMENT PATTERN					
hc02r1 1 & 1/2	long & narrow N-channel device	alignment of poly to active area	c19r1	c2r1	c2r1
DEVICES					
hc07r0 1	N and PMOS devices with PROTECT layer	various	c24r0	c7r0	c7r0
hc08r0 1	N and PMOS devices w/o PROTECT layer	various	c25r0	c8r0	c8r0
CONTACT CHAIN					
hc10r1 1	chain of butting contacts	check compat-ability of process for butting contacts	c27r1	c10r1	c10r1

SUMMARY TABLE
Shortloop Test Pattern

Filename Sz-(Blks)	Structure	Purpose	Coordinates within 290n chip	Test Pat.	Func. Unit
LINEWIDTH & SPACING, VAN DER PAUW PATTERN					
hc04r1 1	long, narrow piece of poly & VAN DER PAUW Pattern	linewidth and spacing, Sheet Resistance	c21r1	c4r1	c4r1
hc05r1 1	long, narrow piece of capacitor & VAN DER PAUW Pattern	linewidth and spacing Sheet Resistance	c22r1	c5r1	c5r1
hc06r1 1	long, narrow piece of metal & VAN DER PAUW Pattern	linewidth and spacing Sheet Resistance	c23r1	c6r1	c6r1
hc07r1 1	long, narrow piece of n+ diffusion & VAN DER PAUW Pattern	linewidth and spacing Sheet Resistance	c24r1	c7r1	c7r1
hc08r1 1	long, narrow piece of p+ diffusion & VAN DER PAUW Pattern	linewidth and spacing Sheet Resistance	c25r1	c8r1	c8r1
hc09r1 1	long, narrow piece of well & VAN DER PAUW Pattern	linewidth and spacing Sheet Resistance	c26r1	c9r1	c9r1

FUNCTIONAL DESCRIPTIONS

Short Loop Test Pattern

Elbows

Filename:

hc00r0

Purpose:

To measure both vertical and horizontal linewidth.

Description:

There are three sets of right angle elbows. One set has both variable linewidth and variable space. The other two are only variable space or variable linewidth.

There is one set of three for each layer.

Testing:

Visual Inspection.

Pad Assignment:

Non electrical test

Short Loop:

Each pattern can be inspected immediately after the completion of that processing step.

Verniers

Filename:

hc01r0

Purpose:

To determine alignment(visual) of two layers.

Description:

Two parallel rows of stripes which have slightly different ~10% different spacing. There are one pair for every layer to layer combination. There will be two sets on to measure both horizontal and the other to measure vertical alignment.

nwel -> aa
nwel -> pf
nwel -> poly
nwel -> n+
nwel -> p+
nwel -> cont
nwel -> metl
aa -> pf
aa -> poly
aa -> n+
aa -> p+
aa -> cont
aa -> metl
pf -> poly
pf -> n+
pf -> p+
pf -> cont
pf -> metl
poly -> n+
poly -> p+
poly -> cont
poly -> metl
n+ -> p+
n+ -> cont
n+ -> metl
p+ -> cont
p+ -> metl
cont -> metl

nwel = n well
aa = active area
pf = p field
poly = poly silicon
n+ = n+ source/drain
p+ = p+ source/drain
cont = contact
metl = metal

Testing:

Visual inspection to determine which stripes line up

Pad Assignment:

Non electrical test

Capacitors

Filenames:

hc05r0 metal-field
hc06r0 metal-poly
hc09r0 poly-diffused capacitor
hc11r0 poly-field
hc12r0 poly-n type gate oxide
hc00r1 poly-p type gate oxide

Purpose:

To measure capacitance and obtain C-V plots.

Description:

There are two capacitors in each block. One has an area of 202176 square microns and a perimeter of 2104 microns. The other has an area of 94656 square microns and a perimeter of 9912 microns. Edge effects can be calculated with the two devices of different area to perimeter ratios.

Testing:

Measure the capacitance with a capacitance meter across the plates.

$$C1=A1*Ca + P1*Cp$$
$$C2=A2*Ca + P2*Cp$$

Where Ca is the capacitance per unit area and Cb is the capacitance per unit length.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
1	GND	Large Cap Bottom Plate
11	VDD	Large Cap Top Plate
6	GND	Small Cap Bottom Plate
16	VDD	Small Cap Top Plate

Short Loop:

Each capacitor has its own short loop. The capacitors are formed when both plates have been formed. In some cases, (e.g. capacitors to the substrate), an addition implant is needed for an ohmic contact.

Short Detection

Filenames:

hc04r0 (metal)
hc01r1 (poly)

Purpose:

To check the poly and metal for short circuits

Description:

The structure is composed of two interlocking combs of minimum geometry wires.

Testing:

Pads 2 and 12 are connected, pad 11 is on the opposite comb. Force current into pad 11 and measure voltage. If there is a short then the voltage will be very low. Pads 2 and 12 can also be used to check for continuity of the other comb.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	Gnd	
12	Gnd	
11	Iin	Force I, Measure V

Continuity - With and Without Steps

Filenames:

hc03r0 (metal)
hc10r0 (poly)

Purpose:

To check the continuity of the layer.

Description:

There are two patterns on each block. One with steps and the other without. The metal pattern has poly steps and the poly pattern has n+ active area steps. The pattern is a serpentine pattern of 4 micron lines and 4 micron space. The steps are also 4 micron lines and spaces. The pattern is 5760 microns long.

Testing:

Force current from the universal pad and measure its voltage. If the voltage is low then the pattern is continuous.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	Gnd	With Steps
11	U1	With Steps
7	Gnd	Without Steps
16	U1	Without Steps

Gate to Active Area Alignment Pattern

Filename:

hc02r1

Purpose:

To examine the alignment of poly to the active area.

Description:

Two very long and narrow (440u x 4u) N channel devices aligned horizontally and vertically. Each source and drain has 4 taps, two to force current and two to sense voltage. The gate is left floating. The width of each source and drain is determined, and the mis-alignment of the gate to the active areas in two dimensions is found.

Also included is a Van der Pauw pattern made of N+.

Testing:

Define Va=Vs2-Vs1 and Vb=Vu3-Vu4.

Misalignment = IRs(440)(1/Va-1/Vb)u toward U3,U4 side.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
ALIGNMENT PATTERN (c02r1)		
2	G	Ground
4	E	Ground
5	S1	Voltage Tap
11	I	Current Source
13	U3	Voltage Tap
14	U4	Voltage Tap
15	S2	Voltage Tap
Van der Pauw PATTERN (co3r1)		
4	E	External
5	S1	Sense Voltage
14	U4	Universal
15	S2	Sense Voltage

Special Masks:

Short contact (CON1)

Completion Step:

Isolation, Gate Define, Poly, N+II, CON1

Linewidth and Spacing Test Pattern

Filenames:

hc04r1 (poly), hc05r1 (capacitor), hc06r1 (metal),
hc07r1 (N+II), hc08r1 (P+II), hc09r1 (nwell)

Purpose:

To measure the linewidth and spacing of the conducting layers.

Description:

Long, narrow (400u x 12u) forked sheet of conducting layers. The patterns are in the same block as the Van Der Pauw devices for that particular level.

Testing:

Force a known current, I. Rs is known from a Van Der Pauw pattern in the same block. The spacing, S, and the linewidth, L, are then:

$$S = (Rs)I(240V12 - 120V23)/(V12 \times V23)$$

$$W = Rs(L)I(240)/2V12$$

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
5	S1	Measure Voltage
11	U1	Force Current
12	U2	Measure Voltage
13	U3	Measure Voltage
14	U4	Sink Current
15	S2	Measure Voltage

Special Masks:

All implanted layers require the short contact mask.

Completion Point:

The structures are complete at any point after implantation or deposition and patterning.

Short Loop:

The short loop steps required are: metal and poly; deposit and pattern isolation, N+II, and nwell; implant and drive P+II; first form nwell, then implant and drive.

NMOS and PMOS Devices

Filenames: hc07r0 (PROTECT mask included), hc08r0

Purpose:

Primarily to allow measurement of the threshold voltage.

Description:

Two half blocks of NMOS and two half blocks of PMOS devices. Each half block has a common source and gate. hc07r0 is covered with a special mask to block the Vt adjust implant. There are four devices in each half block with W/L ratios of .6, 1.0, 2.0, 3.0. Included in the hc07r0 site is the additional mask layer, PROTECT.

Testing:

The testing procedure varies with the desired parameter measurement. It can include Id vs. Vds and sqrt(I) vs. Vgs plots.

Pad Assignment:

W/L	PAD NUMBER				
	G	S	D	B	SUB
NMOS					
0.6	1	2	11	none	none
1.0	1	2	12	none	none
2.0	1	2	13	none	none
3.0	1	2	14	none	none
PMOS					
0.6	6	7	16	none	none
1.0	6	7	17	none	none
2.0	6	7	18	none	none
3.0	6	7	19	none	none

Special Masks:

Short contact (CON1), PROTECT

Completion Step:

F-9

Short Loop:

There is no short process for the PMOS devices as they need the N-well. The short loop for the NMOS devices is: Gate Define, Source/Drain implant, CON1.

Van der Pauw Pattern

Filenames:

hc04r1 (poly), hc05r1 (capacitor), hc06r1 (metal),
hc07r1 (N+II), hc08r1 (P+II), hc09r1 (nwell)

Purpose:

To find the sheet resistance of each conducting layer including all implants.

Description:

A 60u square of each conducting layer with one contact on each side of the square. The JPL linewidth and spacing patterns are on the same block for each layer.

Testing:

$$Rs = ((Vs1 - Vs2)/Iu4) * pi/\ln 2$$

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
4	E	External
5	S1	Sense Voltage
14	U4	Universal
15	S2	Sense Voltage

Special Masks:

Short loop contacts for the implanted layers.

Completion Step:

Any point after implantation or deposition and patterning.

Short Loop:

The short loop steps required are: metal and poly; deposit and pattern isolation, N+II, and nwell; implant and drive P+II; first form nwell, then implant and drive.

Butting Contact Chain Test Pattern

Filename:

hc10r1

Purpose:

To study the compatibility of our process with butting contacts for the n-channel devices.

Description:

A chain of n+ active areas running up and down a full block joined by metal straps with butting contacts.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	G	Ground
14	U4	Universal

Special Masks:

none

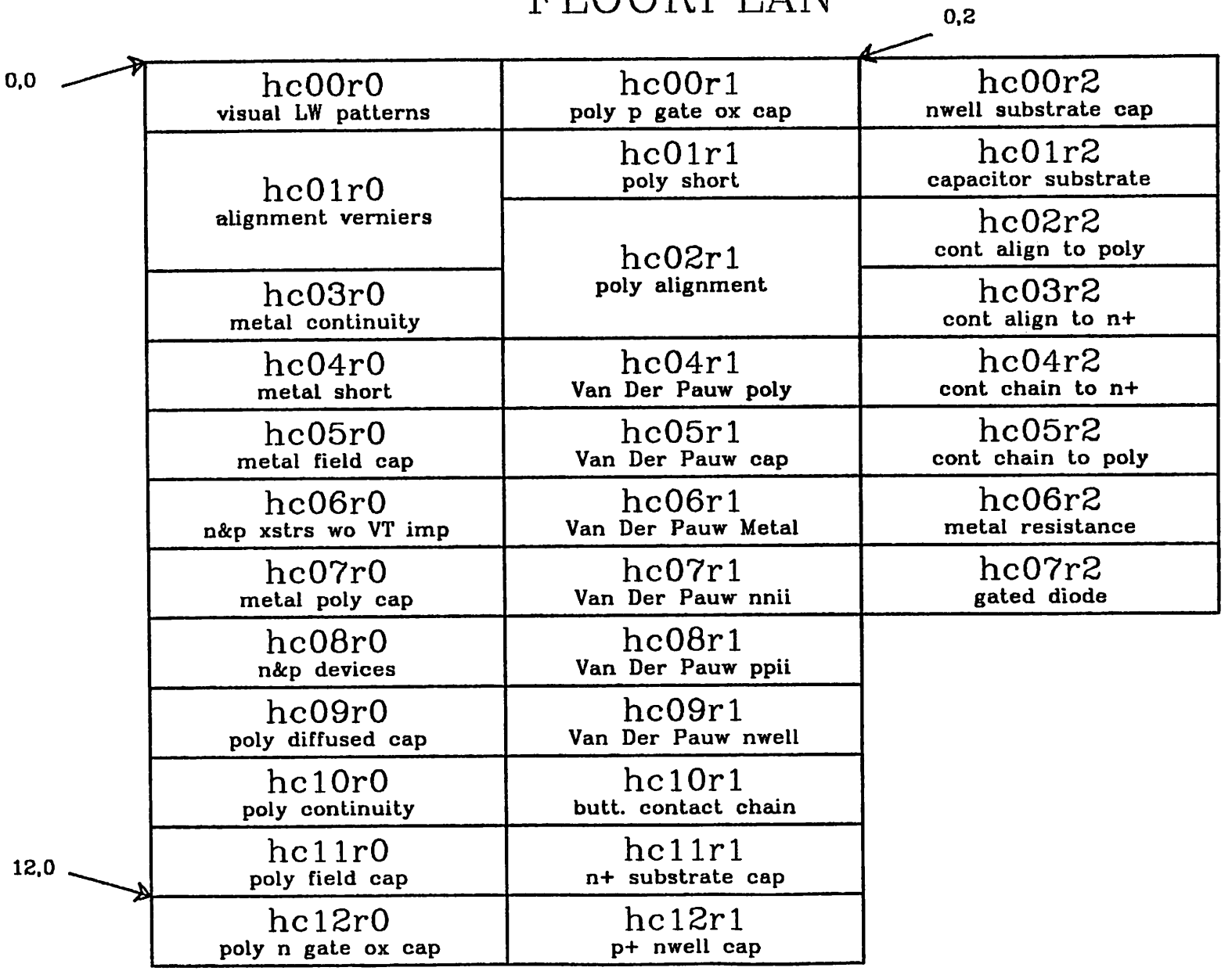
Completion Step:

Metallization

Short Loop:

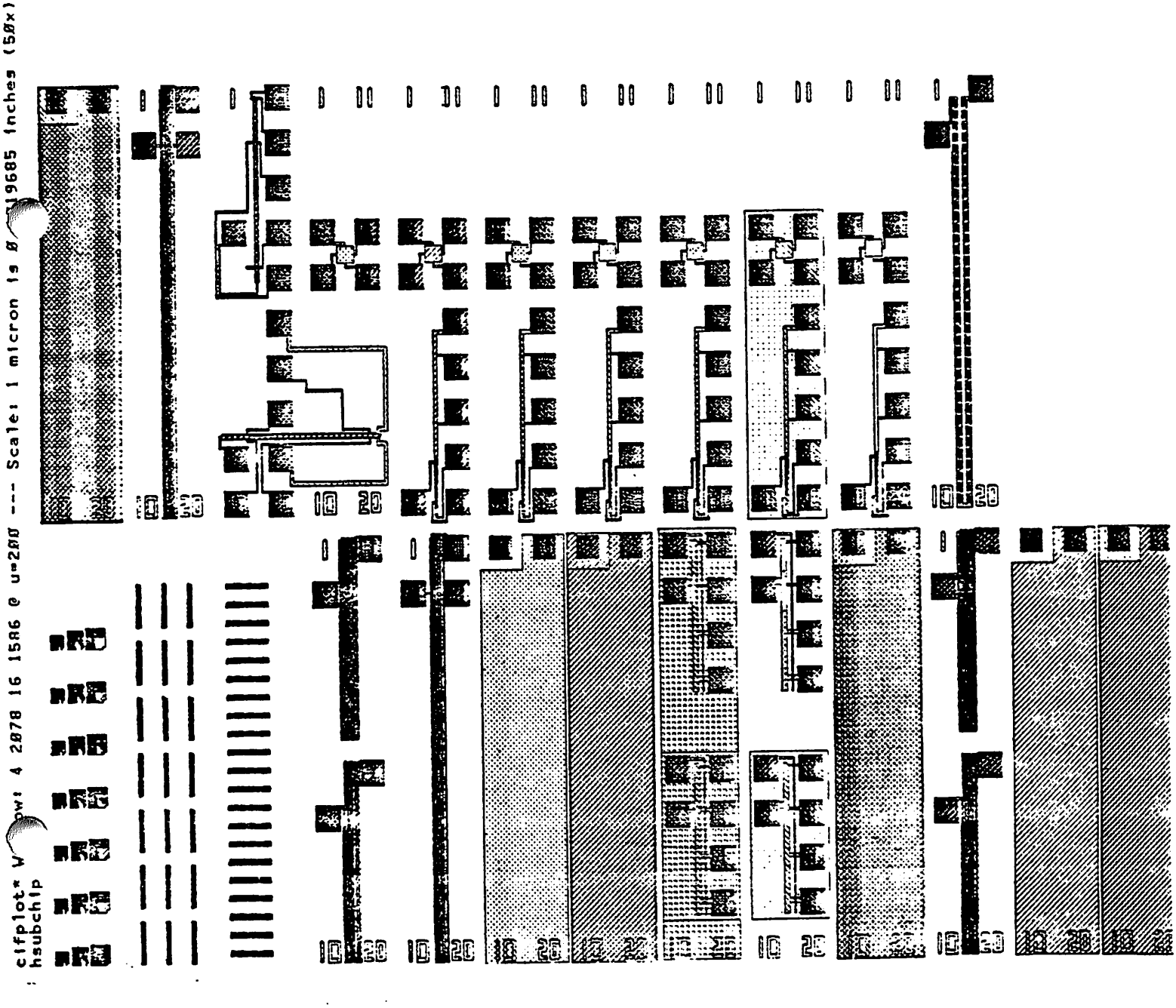
Isolation, N+II, contacts, metallization

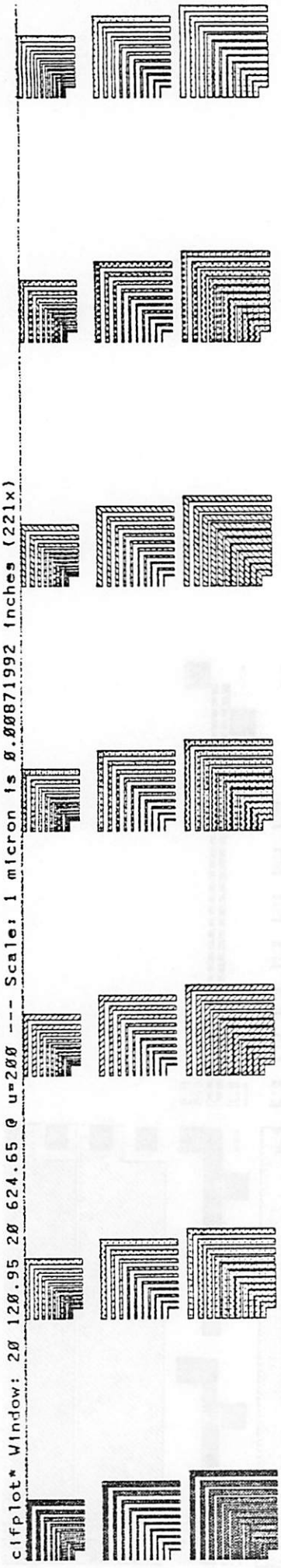
SHORTLOOP TEST PATTERN FLOORPLAN



hsubchip.cif

Shortloop Test Pattern

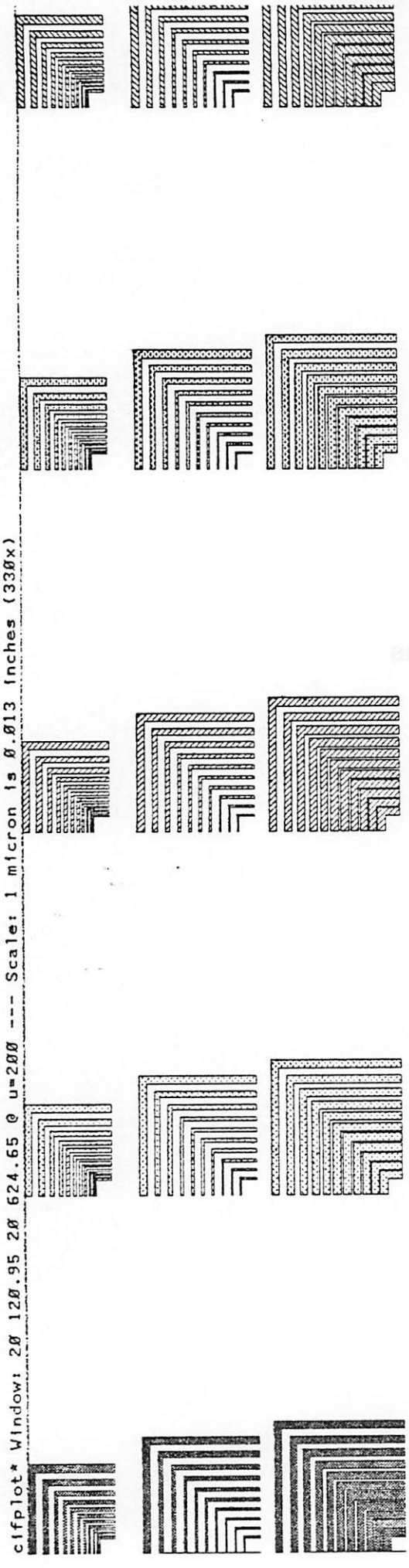




hc0r0.cif

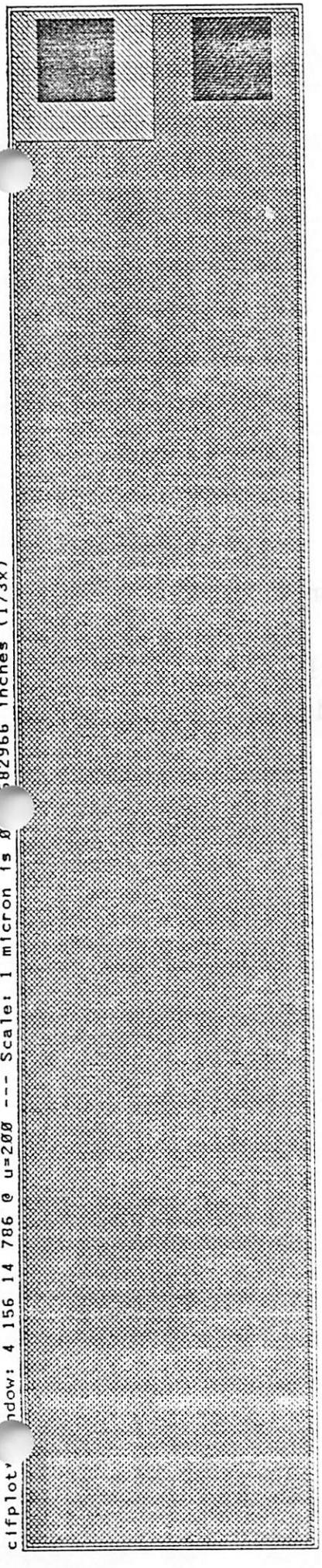
viual LW patterns

hc0r0.cif
viual LW patterns



hc0r0.cif

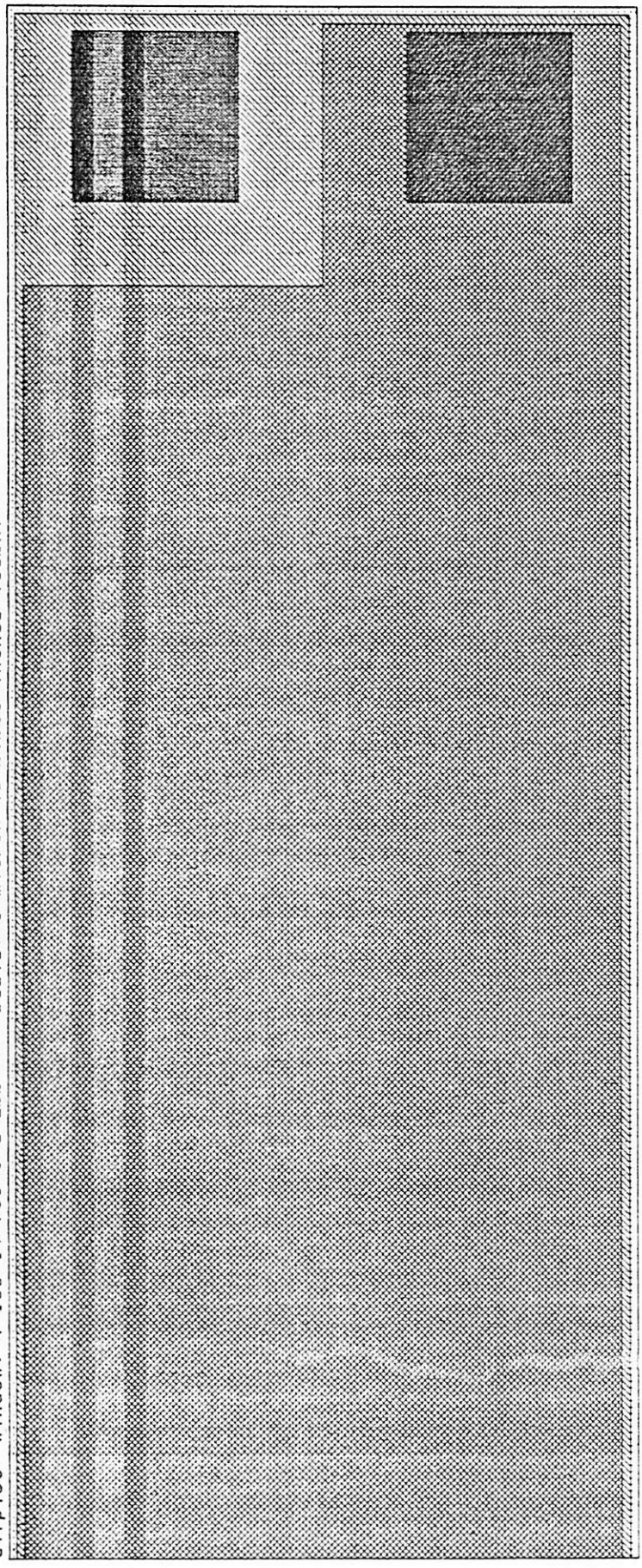
viual LW patterns



hc0r1.cif

poly p gate

oxide cap



hc0r1.cif

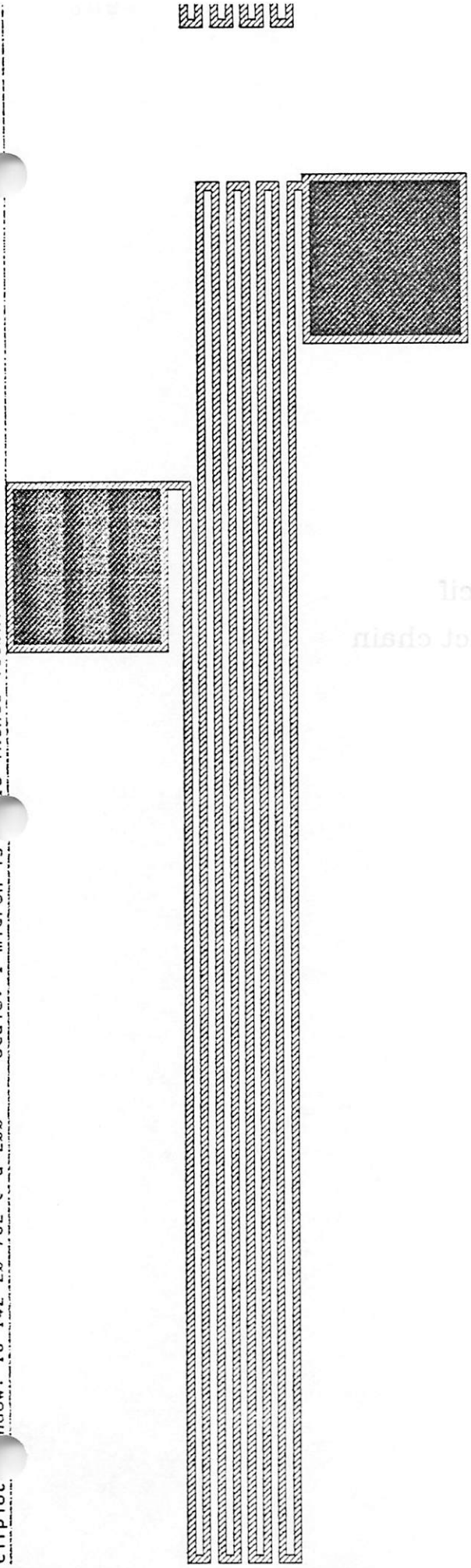
poly p gate

oxide cap

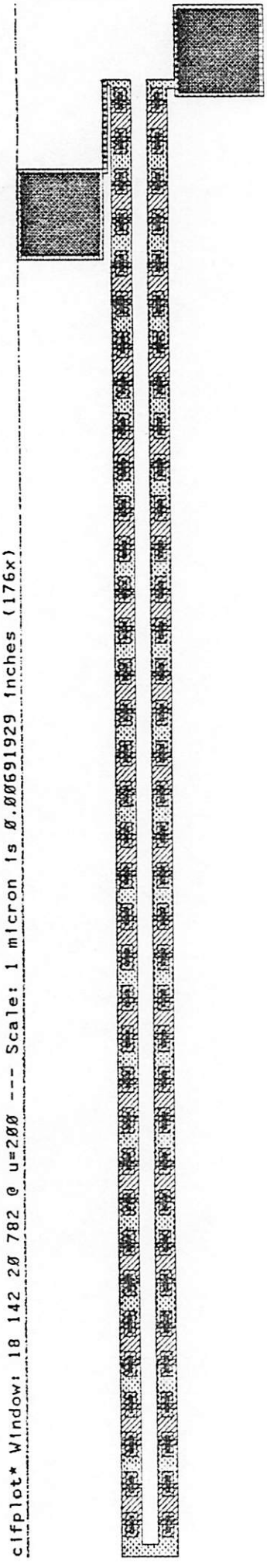
hc10r0.cif

poly continuity

hc10r0.cif
poly continuity



hc10r0.cif
poly continuity

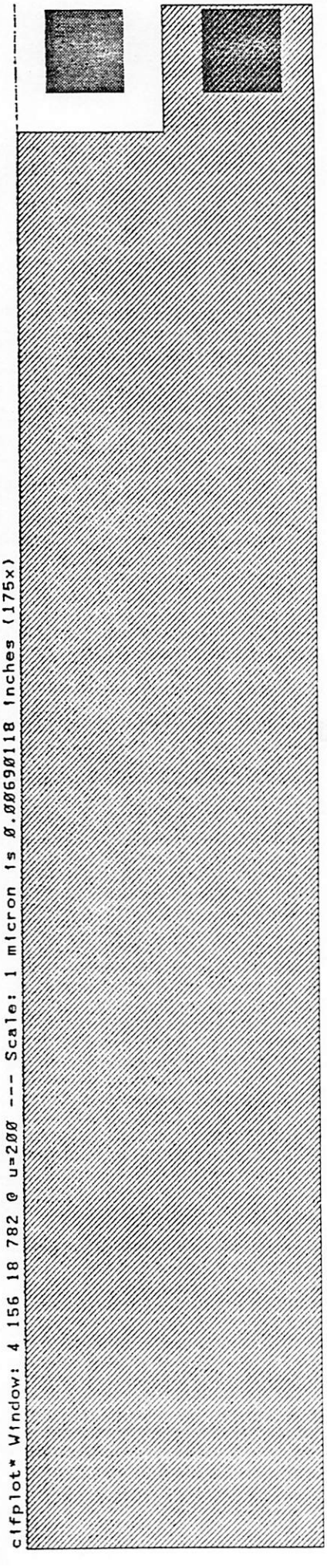


hc10r1.cif

butting contact chain

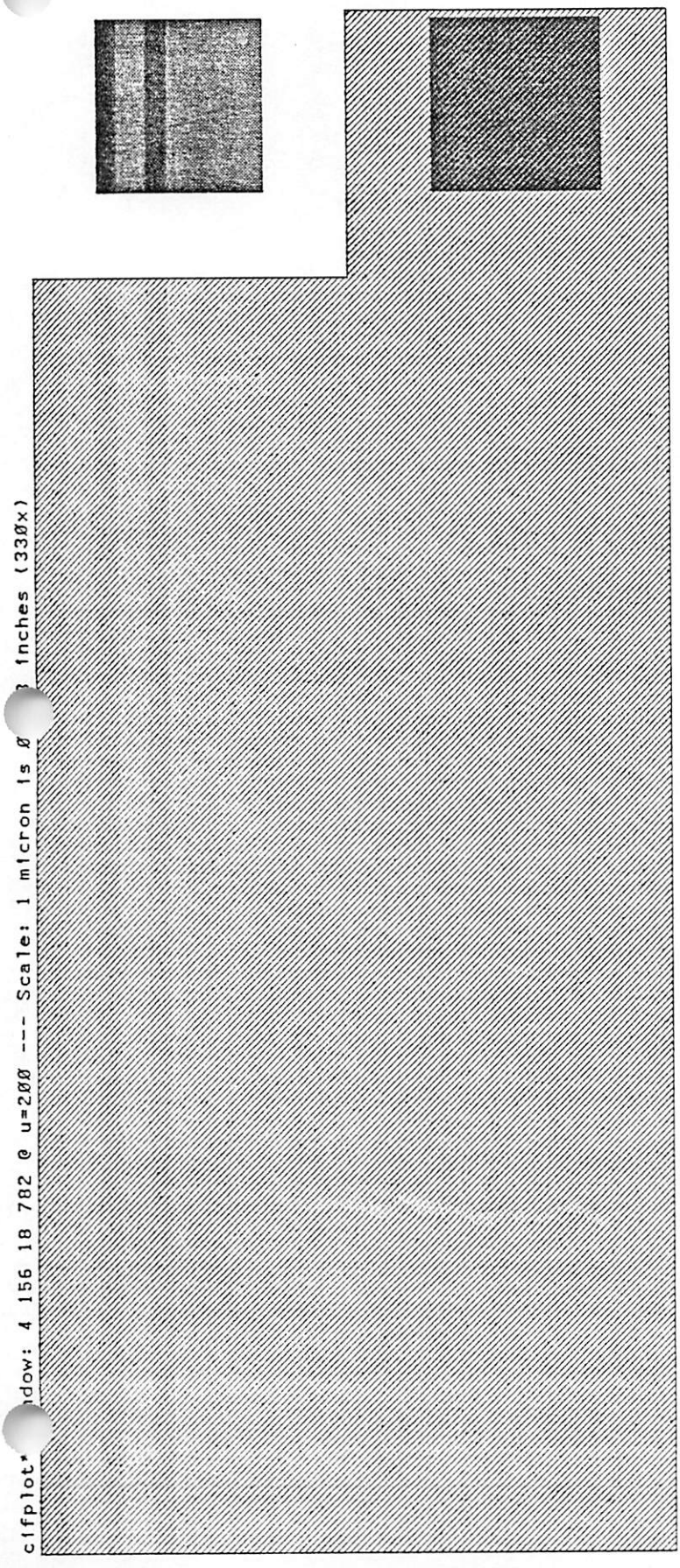
hc10r1.cif

butting contact chain

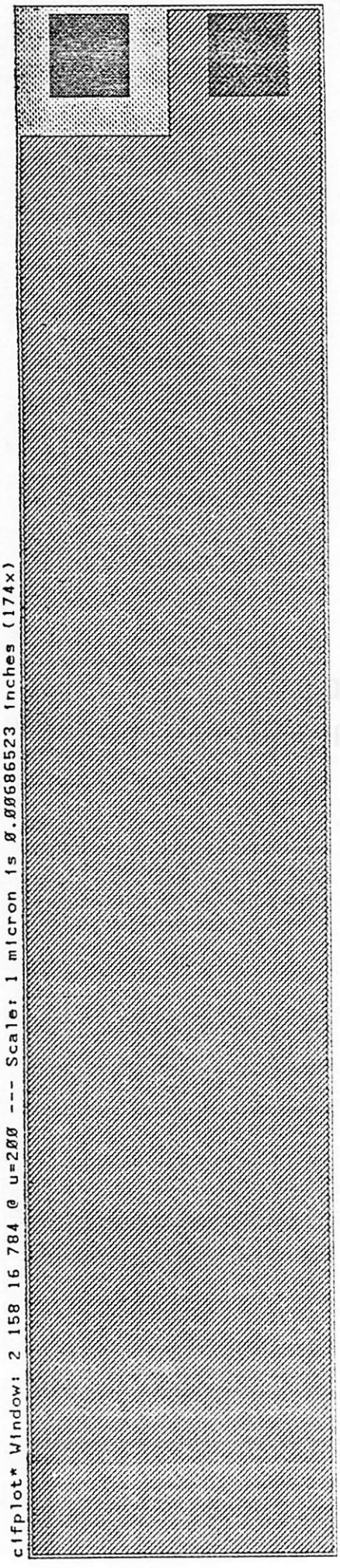


hc11r0.cif

poly field cap



hc11r0.cif
poly field cap



hc12r0.cif

poly n gate

oxide cap

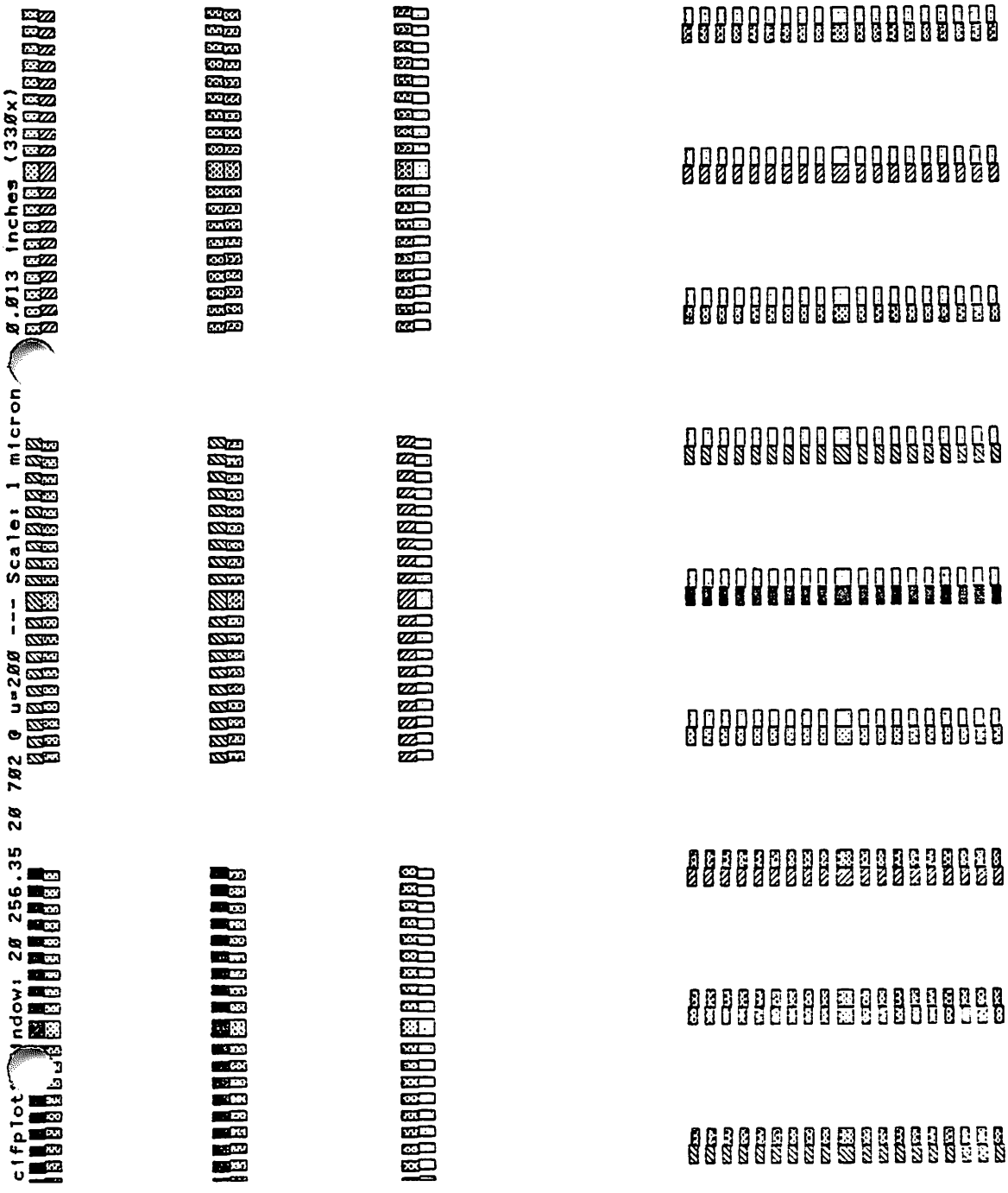
hc12r0.cif

poly n gate

oxide cap

hc1r0.cif
alignment verniers

hc1r0.cif
alignment verniers



hc1r0.cif

alignment verniers

hc1r1.cif
poly short

hc1r1.cif
poly short

hc2r1.cif
poly alignment

hc2r1.cif
poly alignment

clfplot: Window: 7.915 316.245 20 784 @ u=200 --- Scale: 1 mic ls Ø.Ø13 inches (33Øx)

hc3r0.cif

metal continuity

hc3r0.cif

metal continuity

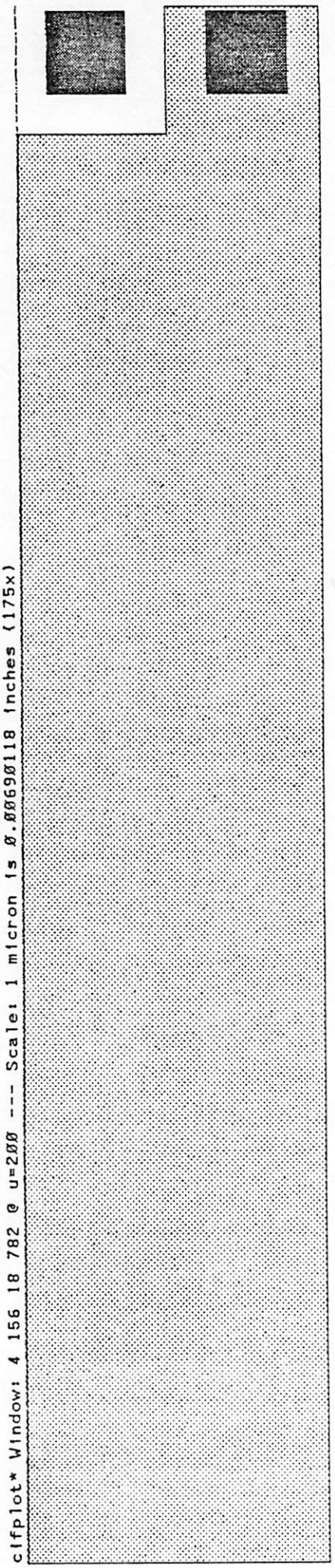
hc3r0.cif
metal continuity

hc4r0.cif
metal short

hc4r0.cif
metal short

hc4r1.cif

Van Der Pauw poly

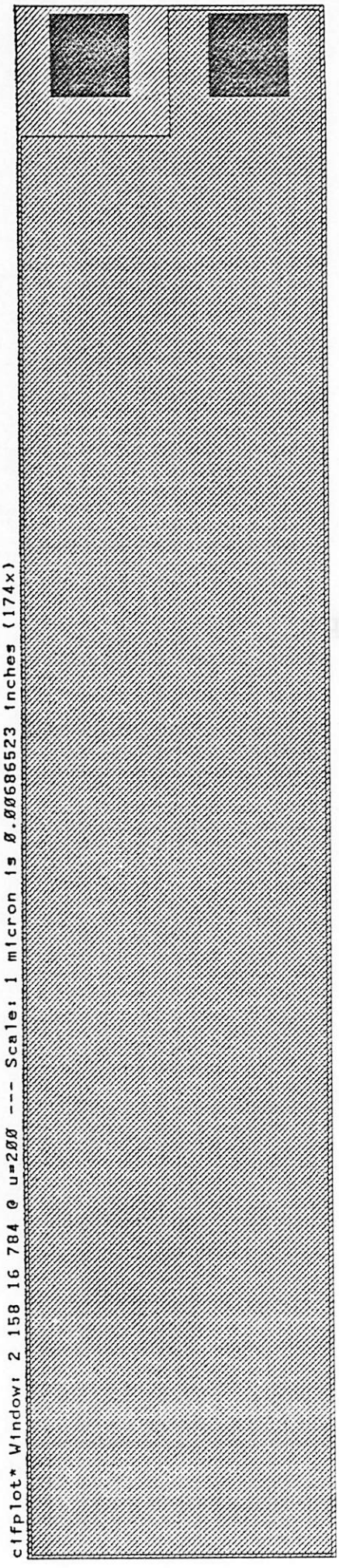


hc5r0.cif

metal field cap

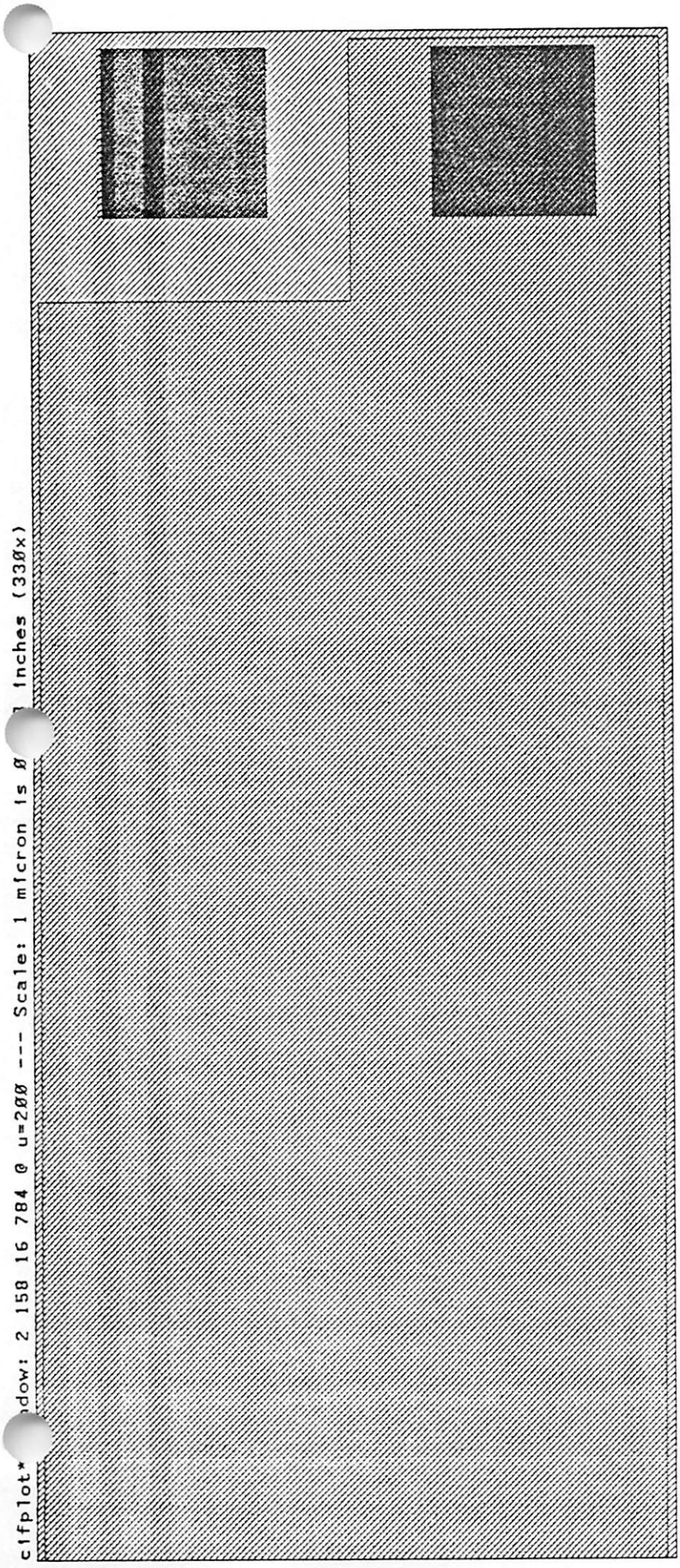
hc5r1.cif

Van Der Pauw cap



hc6r0.cif

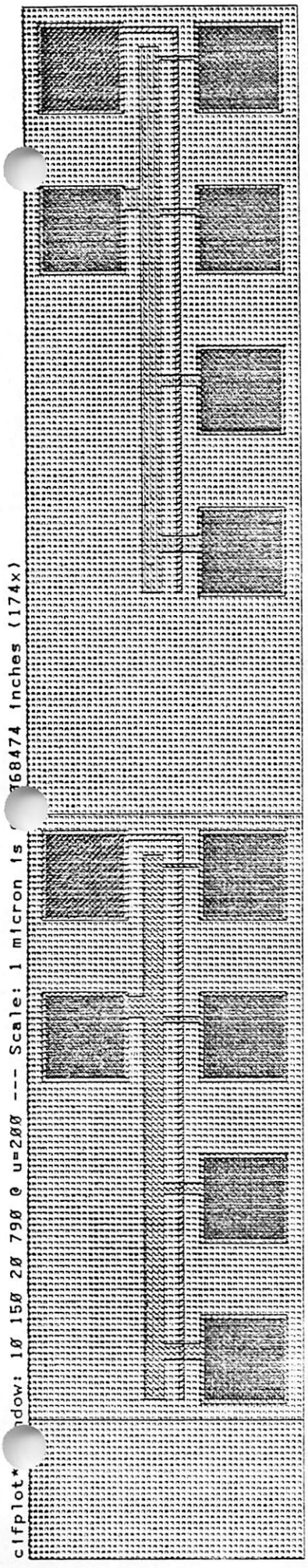
metal poly cap



hc6r0.cif
metal poly cap

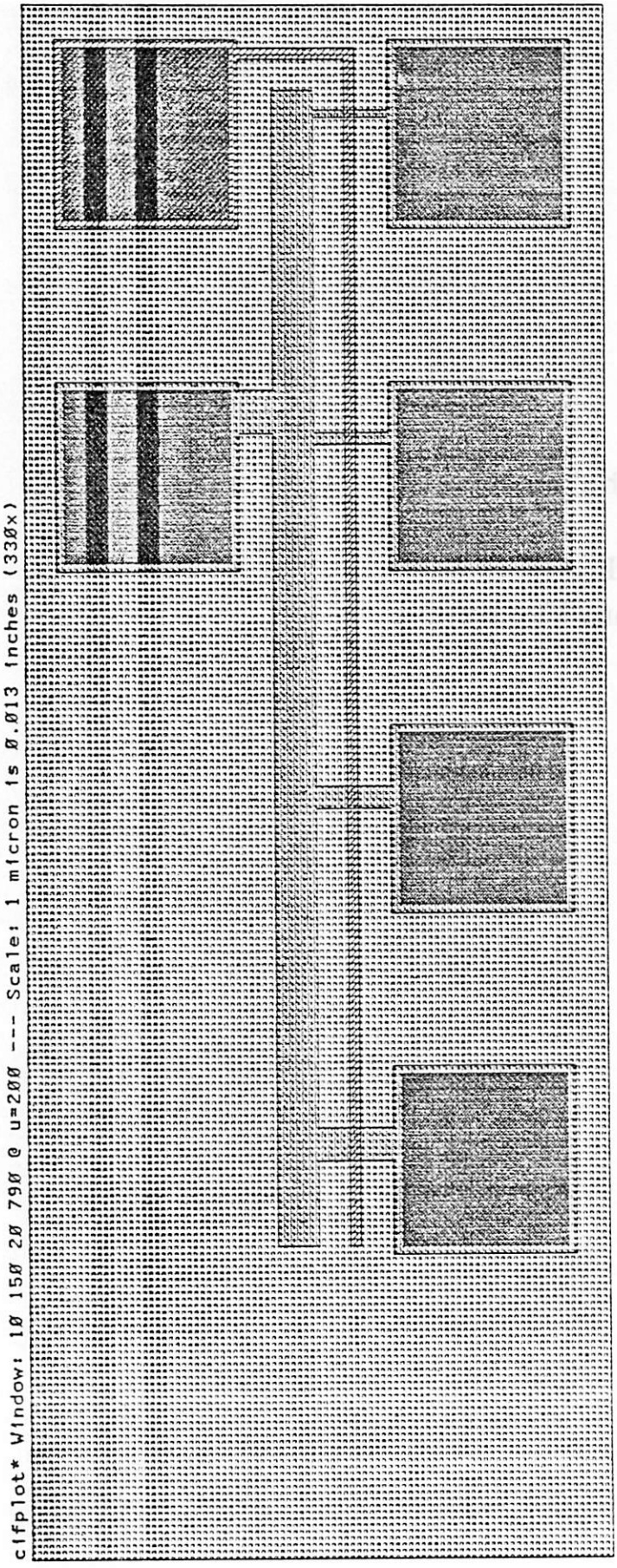
hc6r1.cif

Van Der Pauw metal



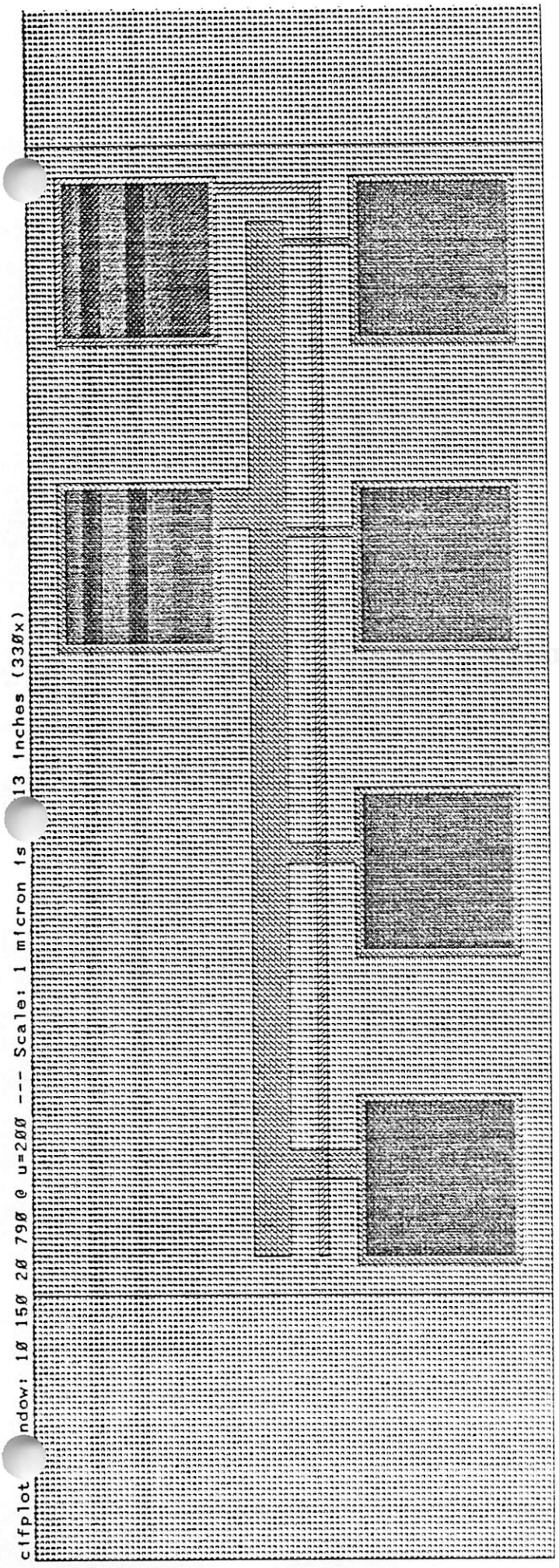
hc7r0.cif

n & p transistors
without VT implant



hc7r0.cif

n & p transistors
without VT implant



hc7r0.cif

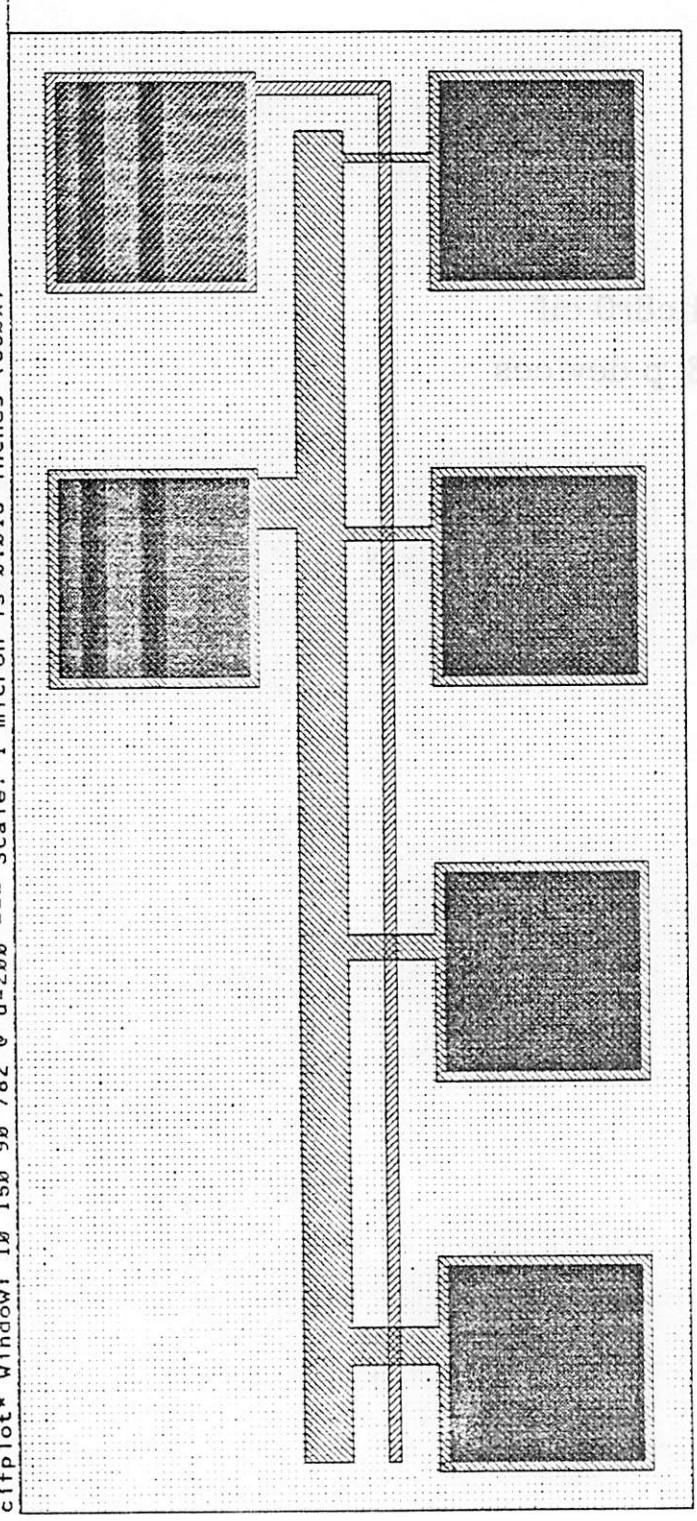
n & p transistors
without VT implant

hc7r1.cif

Van Der Pauw nnii

hc8r0.cif

n & p devices



hc8r0.cif

n & p devices

hc8r0.cif

n & p devices

hc8r1.cif

Van Der Pauw ppii

hc9r0.cif

poly diffused cap

hc9r1.cif

Van Der Pauw nwell

hc9r0.cif

poly diffused cap

Shortloop Test Pattern (hsubchip)
Cif File Cell Hierarchy

al-poly.k
  padblock.k

butting-cont.k
  padblock.k

contpad.k

elbows.k

hc0r0.k
  elbows.k

hc0r1.k
  polypgatecap.k

hc10r0.k
  poly-cont.k

hc10r1.k
  butting-cont.k

hc11r0.k
  polyfieldcap.k

hc12r0.k
  polyngatecap.k

hc1r0.k
  verniers.k

hc1r1.k
  poly-short.k

hc2r1.k
  al-poly.k

hc3r0.k
  metal-cont.k

hc4r0.k
  metal-short.k

hc4r1.k
  vp-poly.k

hc5r0.k
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hc5r1.k
  vp-fpii.k

hc6r0.k
  metlpolycap.k

hc6r1.k
  vp-metl.k

hc7r0.k
  np2.k

hc7r1.k
  vp-nii.k

hc8r0.k
  np1.k

hc8r1.k
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hc9r0.k
  poly-cap-cap.k

hc9r1.k
  vp-well.k

hsubchip.k
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  hc12r0.k hc1r0.k hc1r1.k hc2r1.k hc3r0.k
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  hc6r1.k hc7r0.k hc7r1.k hc8r0.k hc8r1.k
  hc9r0.k hc9r1.k

metal-cont.k
  padblock.k

metal-short.k
  padblock.k

metlfieldcap.k
  contpad.k padblock.k

metlpolycap.k
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np1.k
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np2.k
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padblock.k
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pads.k

poly-cap-cap.k
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polyngatecap.k
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polypgatecap.k
  contpad.k padblock.k

verniers.k

vp-fpii.k
  padblock.k

vp-metl.k
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vp-nii.k
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vp-pii.k
  padblock.k

vp-poly.k
  padblock.k

vp-well.k
  padblock.k

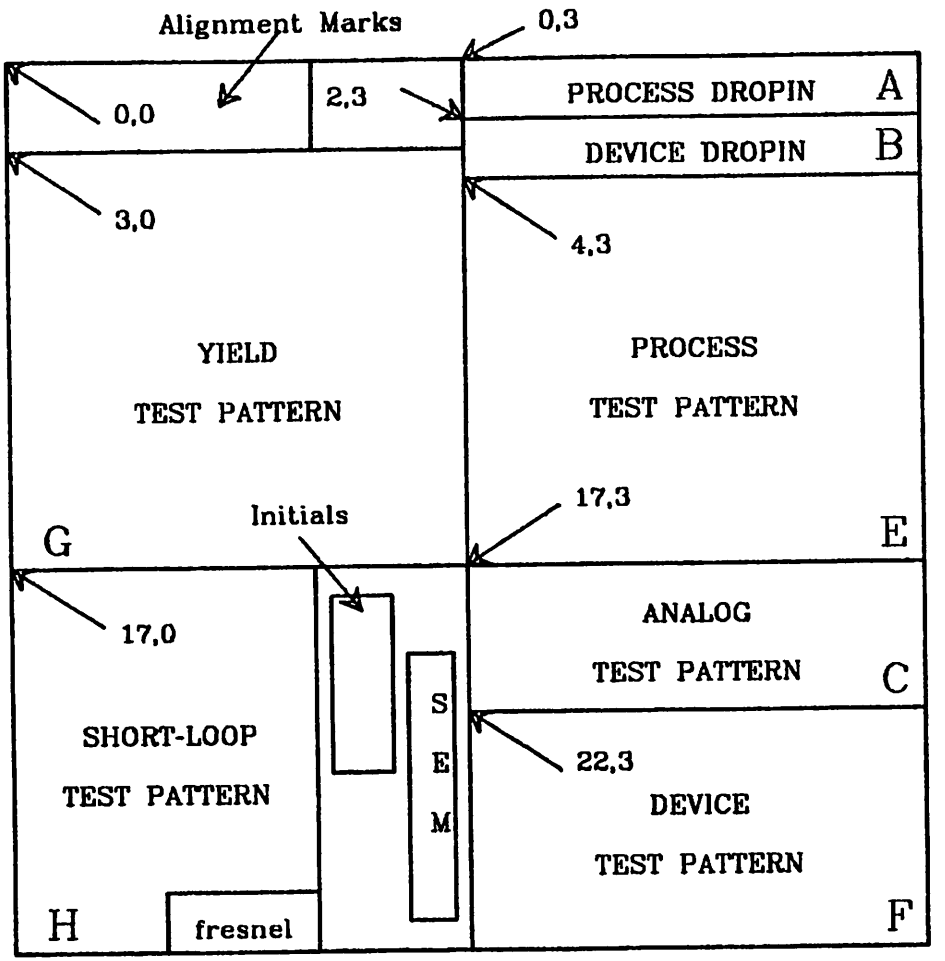
EE290 TEST CHIP ORGANIZATION

The EE290 test chip is made up of 7 Test Patterns plus a separate section for alignment marks. The 7 Test Patterns are: Device, Device Drop-in, Process, Process Drop-in, Shortloop, Yield, and Analog. Each test pattern consists of a collection of functional units. A functional unit is made up of several blocks which together accomplish a specific goal. These blocks are 320um x 1600um. Each block may contain a 2 x 10 array of 80um pads on 160um centers. A block does not always contain all 20 pads since some test structures require a large area, however the pads which are present will remain on the 160um grid. The pad numbering convention is shown below. Pad #1 contains a small notch in it to help distinguish top from bottom when viewing the chip through a microscope. The entire EE290 chip is a 6 row, 30 column array of blocks.

1	11
2	12
3	13
4	14
5	15
6	16
7	17
8	18
9	19
10	20

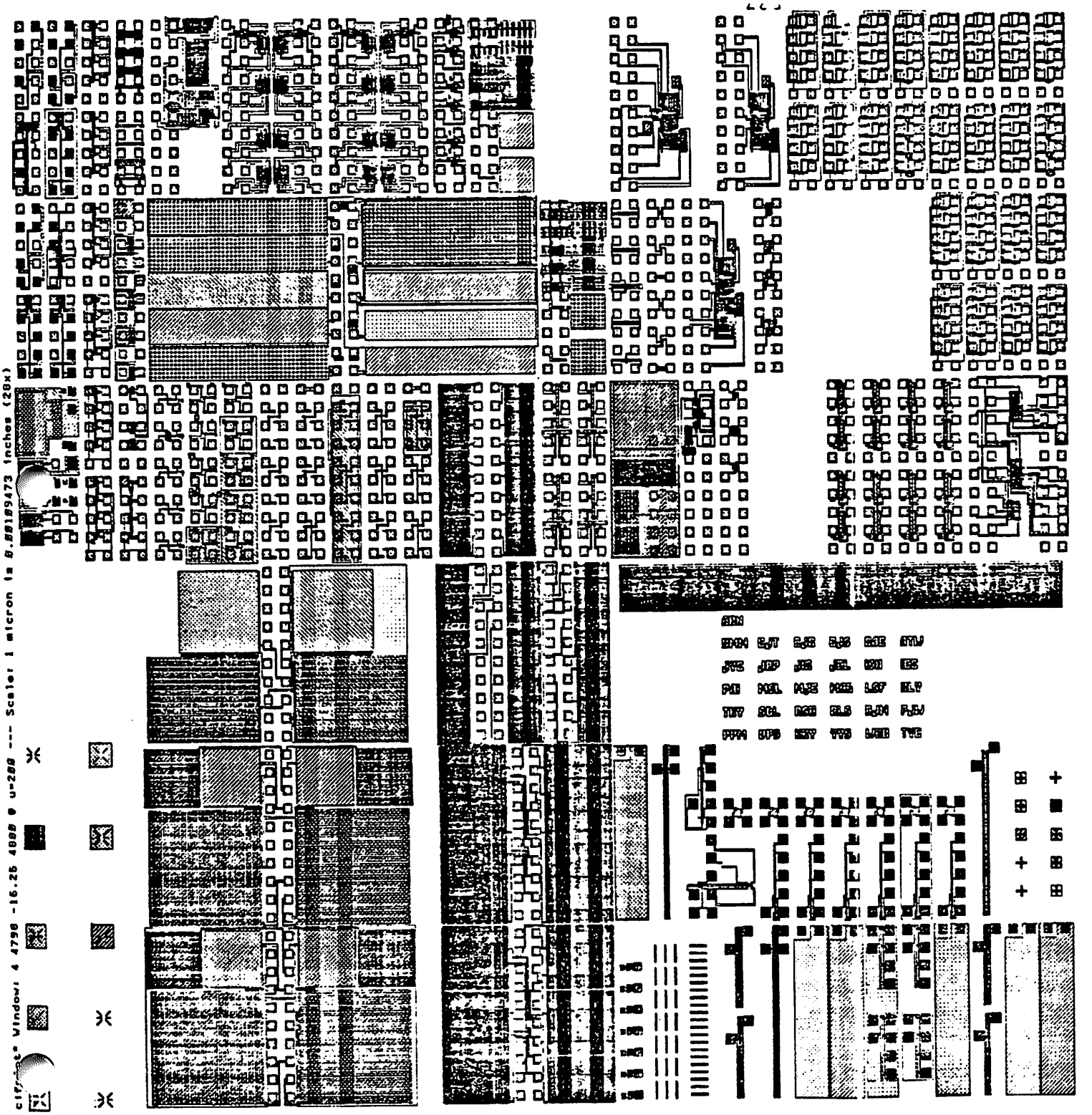
The testing of the devices can be accomplished with a 2 x 5 probe card. Some of the test patterns must be tested with a 2 x 10 probe card due to unconventional pad assignments and the inability to constrain the test structure to a 2 x 5 sub-block.

BERKELEY CMOS PROCESS TEST CHIP



testchip.cif

Entire EE290 Test Chip



BERKELEY CMOS PROCESS
PROCESS TEST PATTERN

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Process Test Pattern
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DISCUSSION
Process Test Pattern

Description

No formal introduction for the Process Test Pattern has been generated.

SUMMARY TABLE

Process Test Pattern

Filename Sz-(Blks)	Structure	Purpose	Coordinates within 280n chip	Test Pat.	Func. Unit
ec0r0rcon 1	Van der Pauw	contact resistance p+ S/D, n+ S/D, & poly	c4r3	c0r0	c0r0
ec1r0sr1 1	Van der Pauw	contact resistance p+ S/D, n+ S/D, poly, metal & n-well	c5r3	c1r0	c1r0
ec2r0sr2 1	Van der Pauw	contact resistance p+ in well, p+ in sub, n+ in well, n+ in sub	c6r3	c2r0	c2r0
ec3r0lwg 1	cross bridge	line width of poly lambda = 10, 13, 20	c7r3	c3r0	c3r0
ec4r0lwm 1	cross bridge	line width of metal lambda = 19, 26, 38	c8r3	c4r0	c4r0
ec5r0lwp 1	cross bridge	line width of p-active lambda = 17, 23, 34	c9r3	c5r0	c5r0
ec6r0lwn 1	cross bridge	line width of n-active lambda = 17, 23, 34	c10r3	c6r0	c6r0
ec7r0w 1	cross bridge	line width of poly, nwell, & p-active	c11r3	c7r0	c7r0

SUMMARY TABLE

Process Test Pattern

Filename Sz-(Blks)	Structure	Purpose	Coordinates within 290n chip	Test Pat.	Func. Unit
ec8r0chain 3	contact chain	contact resistance, poly, diffusion	c12r3 c12r3	c8r0 c10r0	c8r0 c10r0
ec11r0eapoly 1	potential divider	electrical alignment contact to poly & metal to poly	c15r3	c11r0	c11r0
ec12r0eadiff 1	potential divider	electrical alignment contact to diffusion & metal to poly	c16r3	c12r0	c12r0
ec0r2ring 2	ring oscillator	propagation delay	c4r5	c0r2	c0r2
ec2r2latchA 3	CMOS inverter with & without guard band	latch up	c6r5	c2r2	c2r2 and c4r2
ec5r2latchB 3	CMOS inverter with & without guard band	latch up	c9r5	c5r2	c5r2 and c7r2
ec8r2punch 1	CMOS inverter	punch through	c12r5	c8r2	c8r2

SUMMARY TABLE

Process Test Pattern

Filename Sz-(Blks)	Structure	Purpose	Coordinates within 290n chip	Test Pat.	Func. Unit
ec0r1cap1		capacitance			
		Cox(pMOS)	c4r4	c0r1	c5r1
		Cox(nMOS)	c4r4	c0r1	c5r1
		C(M-sub)	c4r4	c0r1	c5r1
		C(M-poly)	c4r4	c0r1	c5r1
	capacitors	Cjn+:area	c4r4	c0r1	c5r1
		Cjp+:area	c4r4	c6r1	c5r1
		C(M-well)	c4r4	c6r1	c5r1
		C(poly-well)	c4r4	c6r1	c5r1
11		C(poly-sub)	c4r4	c6r1	c5r1
cc11r1cap2		capacitance			
		Cfringe (M-sub)			
		Cfringe (poly-n+)			
		Cfringe (poly-p+)			
	capacitor	Cjedge:n+	c15r4	c11r1	c11r1
		Cjedge:p+			
		Cgate pMOS			
2		Cgate nMOS			
cc9r2cap3		capacitance			
		Cfringe (poly-well)			
		Cfringe (poly-sub)			
		Cfringe (met-n+S/D)			
	capacitor	Cfringe (met-p+S/D)	c13r5	c9r2	c9r2
		Cfringe (met-well)			
		Cfield(well)			
2		Cfield(sub)			

FUNCTIONAL DESCRIPTIONS

Process Complete Test Pattern

Contact Resistors

Filename:

ec0r0rcon

Purpose:

To measure the contact resistance of: 1) metal to p+ S/D, 2) metal to n+ S/D, 3) metal to poly, and 4) metal to poly

Description:

This is a Van Der Pauw like structure. The length and width of all structures is 4um.

Testing:

The test procedure is a standard Van Der Pauw measurement. The contact resistance is then, CR = (V*pi)/(I*ln2).

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
3	I+	Force Current Device 1
4	I-	Force Current Device 1
5	I+	Force Current Device 2
6	I-	Force Current Device 2
7	I+	Force Current Device 3
8	I-	Force Current Device 3
9	I+	Force Current Device 4
10	I-	Force Current Device 4
13	V+	Sense Voltage Device 1
14	V-	Sense Voltage Device 1
15	V+	Sense Voltage Device 2
16	V-	Sense Voltage Device 2
17	V+	Sense Voltage Device 3
18	V-	Sense Voltage Device 3
19	V+	Sense Voltage Device 4
20	V-	Sense Voltage Device 4

Sheet Resistance - 1

Filename:

ec1r0sr1

Purpose:

To measure the sheet resistivity of: 1) poly, 2) n-well, 3) metal, 4) n+ S/D, and 5) p+ S/D

Description:

The structure is a standard Van Der Pauw. The active area of each device is 40um x 40um.

Testing:

The test procedure is a standard Van Der Pauw measurement. The sheet resistance is then, SR = (V*pi)/(I*ln2).

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
1	I+	Force Current Device 1
2	I-	Force Current Device 1
3	I+	Force Current Device 2
4	I-	Force Current Device 2
5	I+	Force Current Device 3
6	I-	Force Current Device 3
7	I+	Force Current Device 4
8	I-	Force Current Device 4
9	I+	Force Current Device 5
10	I-	Force Current Device 5
11	V+	Sense Voltage Device 1
12	V-	Sense Voltage Device 1
13	V+	Sense Voltage Device 2
14	V-	Sense Voltage Device 2
15	V+	Sense Voltage Device 3
16	V-	Sense Voltage Device 3
17	V+	Sense Voltage Device 4
18	V-	Sense Voltage Device 4
19	V+	Sense Voltage Device 5
20	V-	Sense Voltage Device 5

Sheet Resistance - 2

Filename:

ec2r0sr2

Purpose:

To measure the sheet resistivity of: 1) n+ S/D, 2) n+ in n-well, 3) p+ S/D, 4) p+ in substrate, and 5) p+ in substrate.

Description:

The structure is a standard Van Der Pauw. The active area of each device is 40um x 40um.

Testing:

The test procedure is a standard Van Der Pauw measurement. The sheet resistance is then, SR = (V*pi)/(I*ln2).

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
1	I+	Force Current Device 1
2	I-	Force Current Device 1
3	I+	Force Current Device 2
4	I-	Force Current Device 2
5	I+	Force Current Device 3
6	I-	Force Current Device 3
7	I+	Force Current Device 4
8	I-	Force Current Device 4
9	I+	Force Current Device 5
10	I-	Force Current Device 5
11	V+	Sense Voltage Device 1
12	V-	Sense Voltage Device 1
13	V+	Sense Voltage Device 2
14	V-	Sense Voltage Device 2
15	V+	Sense Voltage Device 3
16	V-	Sense Voltage Device 3
17	V+	Sense Voltage Device 4
18	V-	Sense Voltage Device 4
19	V+	Sense Voltage Device 5
20	V-	Sense Voltage Device 5

Linewidth - 1

Filename:

ec3r01wg

Purpose:

To measure the linewidth of poly with the following drawn widths: 1) 1.0 um (10 lambda), 2) 1.3 um (13 lambda), and 3) 1.9 um (19 lambda).

Description:

The structure is a Cross Bridge. The bridge length is 160 um for each of the three linewidth bridges. These bridges also function as Van Der Pauw structures of drawn dimensions: 1) 1.0um x 1.0um, 2) 1.3um x 1.3um, and 3) 1.9um x 1.9um.

Testing:

The Van Der Pauw structures should be measured to obtain the sheet resistance. The sheet resistance is then used with the data from the cross bridge to calculate the linewidth. The linewidth is then, LW = length * sheet resistance * Ibot/(Vbot - V-).

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	I+	Force Current Device 1
3	I-	Force Current Device 1
4	Ibot	Force Current Device 1
5	I+	Force Current Device 2
6	I-	Force Current Device 2
7	Ibot	Force Current Device 2
8	I+	Force Current Device 3
9	I-	Force Current Device 3
10	Ibot	Force Current Device 3
12	V-	Sense Voltage Device 1
13	V+	Sense Voltage Device 1
14	Vbot	Sense Voltage Device 1
15	V-	Sense Voltage Device 2
16	V+	Sense Voltage Device 2
17	Vbot	Sense Voltage Device 2
18	V-	Sense Voltage Device 3
19	V+	Sense Voltage Device 3
20	Vbot	Sense Voltage Device 3

Linewidth - 2

Filename:

ec4r01wm

Purpose:

To measure the linewidth of poly with the following drawn widths: 1) 1.9 um (19 lambda), 2) 2.6 um (26 lambda), and 3) 3.8 um (38 lambda).

Description:

The structure is a Cross Bridge. The bridge length is 160 um for each of the three linewidth bridges. These bridges also function as Van Der Pauw structures of drawn dimensions: 1) 1.9um x 1.9um, 2) 2.6um x 2.6um, and 3) 3.8um x 3.8um.

Testing:

The Van Der Pauw structures should be measured to obtain the sheet resistance. The sheet resistance is then used with the data from the cross bridge to calculate the linewidth. The linewidth is then, LW = length * sheet resistance * Ibot/(Vbot - V-).

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	I+	Force Current Device 1
3	I-	Force Current Device 1
4	Ibot	Force Current Device 1
5	I+	Force Current Device 2
6	I-	Force Current Device 2
7	Ibot	Force Current Device 2
8	I+	Force Current Device 3
9	I-	Force Current Device 3
10	Ibot	Force Current Device 3
12	V-	Sense Voltage Device 1
13	V+	Sense Voltage Device 1
14	Vbot	Sense Voltage Device 1
15	V-	Sense Voltage Device 2
16	V+	Sense Voltage Device 2
17	Vbot	Sense Voltage Device 2
18	V-	Sense Voltage Device 3
19	V+	Sense Voltage Device 3
20	Vbot	Sense Voltage Device 3

Linewidth - 3

Filename:

ec5r01wp

Purpose:

To measure the linewidth of poly with the following drawn widths: 1) 1.7 um (17 lambda), 2) 2.3 um (23 lambda), and 3) 3.4 um (34 lambda).

Description:

The structure is a Cross Bridge. The bridge length is 160 um for each of the three linewidth bridges. These bridges also function as Van Der Pauw structures of drawn dimensions: 1) 1.7um x 1.7um, 2) 2.3um x 2.3um, and 3) 3.4um x 3.4um.

Testing:

The Van Der Pauw structures should be measured to obtain the sheet resistance. The sheet resistance is then used with the data from the cross bridge to calculate the linewidth. The linewidth is then, LW = length * sheet resistance * Ibot/(Vbot - V-).

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	I+	Force Current Device 1
3	I-	Force Current Device 1
4	Ibot	Force Current Device 1
5	I+	Force Current Device 2
6	I-	Force Current Device 2
7	Ibot	Force Current Device 2
8	I+	Force Current Device 3
9	I-	Force Current Device 3
10	Ibot	Force Current Device 3
12	V-	Sense Voltage Device 1
13	V+	Sense Voltage Device 1
14	Vbot	Sense Voltage Device 1
15	V-	Sense Voltage Device 2
16	V+	Sense Voltage Device 2
17	Vbot	Sense Voltage Device 2
18	V-	Sense Voltage Device 3
19	V+	Sense Voltage Device 3
20	Vbot	Sense Voltage Device 3

Linewidth - 4

Filename:

ec6r01wn

Purpose:

To measure the linewidth of poly with the following drawn widths: 1) 1.7 um (17 lambda), 2) 2.3 um (23 lambda), and 3) 3.4 um (34 lambda).

Description:

The structure is a Cross Bridge. The bridge length is 160 um for each of the three linewidth bridges. These bridges also function as Van Der Pauw structures of drawn dimensions: 1) 1.7um x 1.7um, 2) 2.3um x 2.3um, and 3) 3.4um x 3.4um.

Testing:

The Van Der Pauw structures should be measured to obtain the sheet resistance. The sheet resistance is then used with the data from the cross bridge to calculate the linewidth. The linewidth is then, LW = length * sheet resistance * Ibot/(Vbot - V-).

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	I+	Force Current Device 1
3	I-	Force Current Device 1
4	Ibot	Force Current Device 1
5	I+	Force Current Device 2
6	I-	Force Current Device 2
7	Ibot	Force Current Device 2
8	I+	Force Current Device 3
9	I-	Force Current Device 3
10	Ibot	Force Current Device 3
12	V-	Sense Voltage Device 1
13	V+	Sense Voltage Device 1
14	Vbot	Sense Voltage Device 1
15	V-	Sense Voltage Device 2
16	V+	Sense Voltage Device 2
17	Vbot	Sense Voltage Device 2
18	V-	Sense Voltage Device 3
19	V+	Sense Voltage Device 3
20	Vbot	Sense Voltage Device 3

Linewidth - 5

Filename:

ec7r01w

Purpose:

To measure the linewidth of: 1) p-channel active region (in well), 2) n-well, and 3) poly.

Description:

The structure is a Cross Bridge. The bridge length is 160 um for each of the three linewidth bridges. These bridges also function as Van Der Pauw structures of drawn dimensions of 4um x 4um each.

Testing:

The Van Der Pauw structures should be measured to obtain the sheet resistance. The sheet resistance is then used with the data from the cross bridge to calculate the linewidth. The linewidth is then, LW = length * sheet resistance * Ibot/(Vbot - V-).

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	I+	Force Current Device 1
3	I-	Force Current Device 1
4	Ibot	Force Current Device 1
5	I+	Force Current Device 2
6	I-	Force Current Device 2
7	Ibot	Force Current Device 2
8	I+	Force Current Device 3
9	I-	Force Current Device 3
10	Ibot	Force Current Device 3
12	V-	Sense Voltage Device 1
13	V+	Sense Voltage Device 1
14	Vbot	Sense Voltage Device 1
15	V-	Sense Voltage Device 2
16	V+	Sense Voltage Device 2
17	Vbot	Sense Voltage Device 2
18	V-	Sense Voltage Device 3
19	V+	Sense Voltage Device 3
20	Vbot	Sense Voltage Device 3

Contact Resistance

Filename:

ec8r0chain

Purpose:

To measure: 1) the contact resistance between metal and poly (left), and 2) the contact resistance between metal and diffusion (right) and to monitor the contact yield.

Description:

The structure is a chain of 2um x 2um contacts, The poly and diffusion segments are 12um x 4um and the metal segments are 12um x 6um.

Testing:

The test procedure is a simple resistance measurement. The resistance measured is made up of three components. The resistance of the poly or diffusion can be calculated from the sheet resistance and the dimensions of the segments. The resistance of the metal can be calculated in the same way. The total resistance is then the sum of the resistance due to poly or diffusion segments plus the resistance due to metal segments plus the resistance due to the contacts. The unknown contact resistance can then be determined from the test data and the sheet resistances of the poly, diffusion, and metal.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
1	1*20	Poly Contact Chain Tap
2	2*20	Poly Contact Chain Tap
3	26*20	Poly Contact Chain Tap
4	38*20	Poly Contact Chain Tap
5	50*20	Poly Contact Chain Tap
6	58*20	Poly Contact Chain Tap
7	70*20	Poly Contact Chain Tap
8	82*20	Poly Contact Chain Tap
9	106*20	Poly Contact Chain Tap
10	108*20	Poly Contact Chain Tap
11	1*20	Diffusion Contact Chain Tap
12	2*20	Diffusion Contact Chain Tap
13	26*20	Diffusion Contact Chain Tap
14	38*20	Diffusion Contact Chain Tap
15	50*20	Diffusion Contact Chain Tap
16	58*20	Diffusion Contact Chain Tap
17	70*20	Diffusion Contact Chain Tap
18	82*20	Diffusion Contact Chain Tap
19	106*20	Diffusion Contact Chain Tap
20	108*20	Diffusion Contact Chain Tap

Electrical Alignment - 1

Filename:

ec11r0eapoly

Purpose:

To measure the electrical alignment between: 1) contact to poly (vertical), 2) contact to poly (horizontal), 3) metal to poly (vertical), and 4) metal to poly (horizontal).

Description:

This is simply a potential divider. The resistor width is 24um. The taps to V+ and V- are 60um apart and the taps for V+ and Vref are 120um apart.

Testing:

To test the structure let current flow through I+ and I-, if tap to V+, and V- voltages are equal then the alignment is perfect. The misalignment is then, M = W*(voltage difference)/(2*Rs*I). Where W is the width, Rs the sheet resistance, and I is the current. The voltage difference is (V+ -Vtap) - (V- - Vtap).

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
1	Vref	Sense Voltage Device 1
2	V+	Sense Voltage Device 1
3	V-	Sense Voltage Device 1
4	I+	Force Current Device 2
5	V+	Sense Voltage Device 2
6	Vref	Sense Voltage Device 3
7	V+	Sense Voltage Device 3
8	V-	Sense Voltage Device 3
9	I+	Force Current Device 4
10	V+	Sense Voltage Device 4
11	I+	Force Current Device 1
12	Tap	Sense Voltage Device 1
13	I-	Force Current Device 1 & 2
14	V-	Sense Voltage Device 2
15	Tap	Sense Voltage Device 2
16	I+	Force Current Device 3
17	Tap	Sense Voltage Device 3
18	I-	Force Current Device 3 & 4
19	V-	Sense Voltage Device 4
20	Tap	Sense Voltage Device 4

Electrical Alignment - 2

Filename:

ec12r0eadiff

Purpose:

To measure the electrical alignment between: 1) contact to diff (vertical), 2) contact to diff (horizontal), 3) metal to diff (vertical), and 4) metal to diff (horizontal).

Description:

This is simply a potential divider. The resistor width is 24um. The taps to V+ and V- are 60um apart and the taps for V+ and Vref are 120um apart.

Testing:

To test the structure let current flow through I+ and I-, if tap to V+, and V- voltages are equal then the alignment is perfect. The misalignment is then, M = W*(voltage difference)/(2*Rs*I). Where W is the width, Rs the sheet resistance, and I is the current. The voltage difference is (V+ -Vtap) - (V- - Vtap).

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
1	Vref	Sense Voltage Device 1
2	V+	Sense Voltage Device 1
3	V-	Sense Voltage Device 1
4	I+	Force Current Device 2
5	V+	Sense Voltage Device 2
6	Vref	Sense Voltage Device 3
7	V+	Sense Voltage Device 3
8	V-	Sense Voltage Device 3
9	I+	Force Current Device 4
10	V+	Sense Voltage Device 4
11	I+	Force Current Device 1
12	Tap	Sense Voltage Device 1
13	I-	Force Current Device 1 & 2
14	V-	Sense Voltage Device 2
15	Tap	Sense Voltage Device 2
16	I+	Force Current Device 3
17	Tap	Sense Voltage Device 3
18	I-	Force Current Device 3 & 4
19	V-	Sense Voltage Device 4
20	Tap	Sense Voltage Device 4

Capacitors - 1

Filename:

ec0r1cap1

Purpose:

To measure the following capacitances:

1) C-gate (PMOS; poly-well) 2) C-gate (NMOS; poly-substrate)
3) C-thick (metal-substrate) 4) C-glass (metal-poly)
5) C-n+S/D (area) 6) C-p+S/D (area) 7) C-field (poly-well)
8) C-thick (metal-well) 9) C-field (poly-substrate)

Description:

This block contains 9 different capacitors as described above. The dimensions of these capacitors will be given with the pad assignment.

Testing:

Capacitance Measurement. C=eox/tox

Pad Assignment:

PAD #	DEVICE #	FUNCTION
1	1+	Well Top plate L=300um W=1600um
2	1-	Poly Bottom plate
3	2-	Substrate Bottom plate L=310um W=1610um
4	2+	Poly Top plate
5	3-	Substrate Bottom plate L=310um W=1610um
6	3+	Metal Top plate
7	4	Poly Plate L=300um W=1600um
8	4	Metal Plate
9	5-	Substrate Bottom plate L=300um W=1600um
10	5+	Top plate
11	6+	Well Top plate L=555um W=1540um
12	6-	Bottom plate
15	7+	Well Top plate L=240 W=1540um
16	7-	Poly Bottom plate
17	8+	Well Top plate L=250um W=1550um
18	8-	Metal Bottom plate
19	9-	Substrate Bottom plate L=240um W=1540um
20	9+	Poly Top plate

Capacitors - 2

Filename:

ec11r1cap2

Purpose:

To measure the following capacitances:

1) C-fringe (poly-p+) 2) C-fringe (poly-n+)
3) C-fringe (metal-substrate) 4) C-p+junc (edge-effect)
5) C-n+junc (edge effect) 6) C-gate (PMOS: C-V)
7) C-gate (NMOS: C-V)

Description:

This block contains 7 different capacitors of regular and comb-shape.

Testing:

Capacitance Measurement

(1)&(2) C-fringe=(Cmeasured - Cgate*L*W)/(2L)
(3) C-fringe=(Cmeasured - Cthick*L*W)/(2L)
(4)&(5) C-edge=(Cmeasured - Carea*L*W)/(2L)

(All of these capacitances are per unit length)

Pad Assignment:

PAD #	DEVICE#	FUNCTION
1	1-	P+ Bottom plate L=5680um W=3um
11	1+	Poly Top plate
2	2+	N+ Top plate L=5680um W=3um
12	2-	Poly Bottom plate
3	3-	Substrate Bottom plate L=4540um W=5um
13	3+	Metal Top plate
4	4+	Well Top plate L=5885um W=5um
14	4-	P+ Bottom Plate
5	5-	Substrate Bottom plate L=5885um W=5um
15	5+	N+ Top plate
6	6+	Well Top plate L=300um W=310um
16	6-	Poly Bottom plate
7	7-	Substrate Bottom plate L=300 W=310um
17	7+	Poly Top plate

Capacitors - 3

Filename:

ec9r2cap3

Purpose:

To measure the following capacitances:

1) C-fringe (poly-well)
2) C-fringe (poly-substrate)
3) C-fringe (metal-n+)
4) C-fringe (metal-p+)
5) C-fringe (metal-well)
6) C-field (poly-well)
7) C-field (poly-substrate)

Description:

This block contains 7 different capacitors of regular and comb-shape. Capacitors 1, 2, 6, and 7 are over field oxide while capacitors 3, 4, and 5 are over p-glass.

Testing:

Capacitance Measurement

(1)&(2) C-fringe=(Cmeasured - Carea*L*W)/(2L)
(3)&(4)&(5) C-fringe=(Cmeasured - Cthick*L*W)/(2L)

Pad Assignment:

PAD #	DEVICE#	FUNCTION
1	1-	P+ Bottom plate L=5680um W=3um
11	1+	Poly Top plate
2	2+	N+ Top plate L=5680um W=3um
12	2-	Poly Bottom plate
3	3-	Substrate Bottom plate L=4540um W=5um
13	3+	Metal Top plate
4	4+	Well Top plate L=5885um W=5um
14	4-	P+ Bottom Plate
5	5-	Substrate Bottom plate L=5885um W=5um
15	5+	N+ Top plate
6	6+	Well Top plate L=300um W=310um
16	6-	Poly Bottom plate
7	7-	Substrate Bottom plate L=300 W=310um
17	7+	Poly Top plate

Ring Oscillator

Filename:

ec0r2ring

Purpose:

To measure speed of 19 stages of CMOS ring oscillator.

Description:

The structure is a 19 stage ring oscillator. (channel length 2.5um)

Testing:

CMOS ring oscillator: Apply 5v to pads 14, ground pad 12, ring oscillator output can be measured at pad 11.

Buffer Speed: A buffer pair is provided to measure speed and attempt to latchup. Power is applied at pad 14, ground to pad 12. Input on pad 15 and measure prop delay to pad 16.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
11	RO	Ring Osc. Output
12	GND	Ground
14	V+	Power
17	BI	Buffer Input
18	BO	Buffer Output

CMOS Latch Up - 1

Filename:

ec2r2latchA

Purpose:

To test latch-up of inverters without guardband at 2.5um length.

Description:

This block is made up of four CMOS inverters in which the P and N channel transistors are connected in different ways.

The first device is set up such that the drain and source leads can be swapped for latch-up measurements in the four possible combinations.

The second device is the same as the first except that the drains are permanently connected.

The third device is the same as the second device except that the metal connections for inverter operation are present.

The fourth device is the same as the third device except that the positions of the source and drain are reversed on both transistors.

The width and length of all devices is 100um and 4um respectively. The distance from device to well is 4um.

Testing:

Latch-up can be accomplished by 1) raising N-well to P substrate voltage until avalanche-induced latch-up occurs, or 2) raising the drain above or below the supply-ground voltages.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
1	N-drn	NMOS drain Device 1
2	P-drn	PMOS drain Device 1
3	P-src	PMOS source Device 1
4	Sub	Substrate Device 1 & 2
5	Nwl	N-well Device 2
6	O/P	O/P Device 2
7	SubSrc	Source and Substrate of Device 3
8	NwlSrc	N-well and PMOS source of Device 3
9	SubSrc	Source and Substrate of Device 4
10	O/P	O/P Device 4
11	N-src	NMOS source Device 1
12	Nwl	N-well Device 1
13	Gate	Gate Device 1
14	Gate	Gate Device 2
15	P-src	PMOS source Device 2
16	N-src	NMOS source Device 2
17	Gate	Gate Device 3
18	O/P	O/P Device 3
19	NwlSrc	N-well and PMOS source of Device 4
20	I/P	I/P Device 4

CMOS Latch Up - 2

Filename:

ec2r2latchA

Purpose:

To test latch-up of inverters without guardband at 2.5um length.

Description:

This block is made up of four CMOS inverters in which the P and N channel transistors are connected in different ways.

The first device is set up such that the drain and source leads can be swapped for latch-up measurements in the four possible combinations.

The second device is the same as the first except that the drains are permanently connected.

The third device is the same as the second device except that the metal connections for inverter operation are present.

The fourth device is the same as the third device except that the positions of the source and drain are reversed on both transistors.

The width and length of all devices is 100um and 4um respectively. The distance from device to well is 4um.

Testing:

Latch-up can be accomplished by 1) raising N-well to P substrate voltage until avalanche-induced latch-up occurs, or 2) raising the drain above or below the supply-ground voltages.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
1	N-src	NMOS source Device 1
2	Nwl	N-well Device 1
3	Gate	Gate Device 1
4	O/P	Output Device 2
5	P-src	PMOS source Device 2
6	N-src	NMOS source Device 2
7	Gate	Gate Device 3
8	O/P	Output Device 3
9	NwlSrc	N-well and PMOS source of Device 4
10	I/P	Input Device 4
11	N-drn	NMOS drain Device 1
12	P-drn	PMOS drain Device 1
13	P-src	PMOS source Device 1
14	Sub	Substrate Device 1 & 2
15	Nwl	N-well Device 2
16	Gate	Gate Device 2
17	SubSrc	Source and Substrate of Device 3
18	NwlSrc	N-well and PMOS source of Device 3
19	SubSrc	Source and Substrate of Device 4
20	O/P	Output Device 4

CMOS Latch Up - 3

Filename:

ec5r2latchB

Purpose:

To test latch-up of inverters without guardband at 2.5um length.

Description:

This block is made up of four CMOS inverters in which the P and N channel transistors are connected in different ways.

The first device is set up such that the drain and source leads can be swapped for latch-up measurements in the four possible combinations.

The second device is the same as the first except that the drains are permanently connected.

The third device is the same as the second device except that the metal connections for inverter operation are present.

The fourth device is the same as the third device except that the positions of the source and drain are reversed on both transistors.

The width and length of all devices is 100um and 4um respectively. The distance from device to well is 8um.

Testing:

Latch-up can be accomplished by 1) raising N-well to P substrate voltage until avalanche-induced latch-up occurs, or 2) raising the drain above or below the supply-ground voltages.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
1	N-drn	NMOS drain Device 1
2	P-drn	PMOS drain Device 1
3	P-src	PMOS source Device 1
4	Sub	Substrate Device 1 & 2
5	Nwl	N-well Device 2
6	O/P	Output Device 2
7	SubSrc	Source and Substrate of Device 3
8	NwlSrc	N-well and PMOS source of Device 3
9	SubSrc	Source and Substrate of Device 4
10	O/P	Output Device 4
11	N-src	NMOS source Device 1
12	Nwl	N-well Device 1
13	Gate	Gate Device 1
14	Gate	Gate Device 2
15	P-src	PMOS source Device 2
16	N-src	NMOS source Device 2
17	Gate	Gate Device 3
18	O/P	Output Device 3
19	NwlSrc	N-well and PMOS source of Device 4
20	I/P	Input Device 4

CMOS Latch Up - 4

Filename:

ec5r2latchB

Purpose:

To test latch-up of inverters without guardband at 2.5um length.

Description:

This block is made up of four CMOS inverters in which the P and N channel transistors are connected in different ways.

The first device is set up such that the drain and source leads can be swapped for latch-up measurements in the four possible combinations.

The second device is the same as the first except that the drains are permanently connected.

The third device is the same as the second device except that the metal connections for inverter operation are present.

The fourth device is the same as the third device except that the positions of the source and drain are reversed on both transistors.

The width and length of all devices is 100um and 4um respectively. The distance from device to well is 8um.

Testing:

Latch-up can be accomplished by 1) raising N-well to P substrate voltage until avalanche-induced latch-up occurs, or 2) raising the drain above or below the supply-ground voltages.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
1	N-src	NMOS source Device 1
2	Nwl	N-well Device 1
3	Gate	Gate Device 1
4	O/P	Output Device 2
5	P-src	PMOS source Device 2
6	N-src	NMOS source Device 2
7	Gate	Gate Device 3
8	O/P	Output Device 3
9	NwlSrc	N-well and PMOS source of Device 4
10	I/P	Input Device 4
11	N-drn	NMOS drain Device 1
12	P-drn	PMOS drain Device 1
13	P-src	PMOS source Device 1
14	Sub	Substrate Device 1 & 2
15	Nwl	N-well Device 2
16	Gate	Gate Device 2
17	SubSrc	Source and Substrate of Device 3
18	NwlSrc	N-well and PMOS source of Device 3
19	SubSrc	Source and Substrate of Device 4
20	O/P	Output Device 4

CMOS Inverter

Filename:

ec8r2punch

Purpose:

To determine Punch-through characteristics.

Description:

8 various inverters.

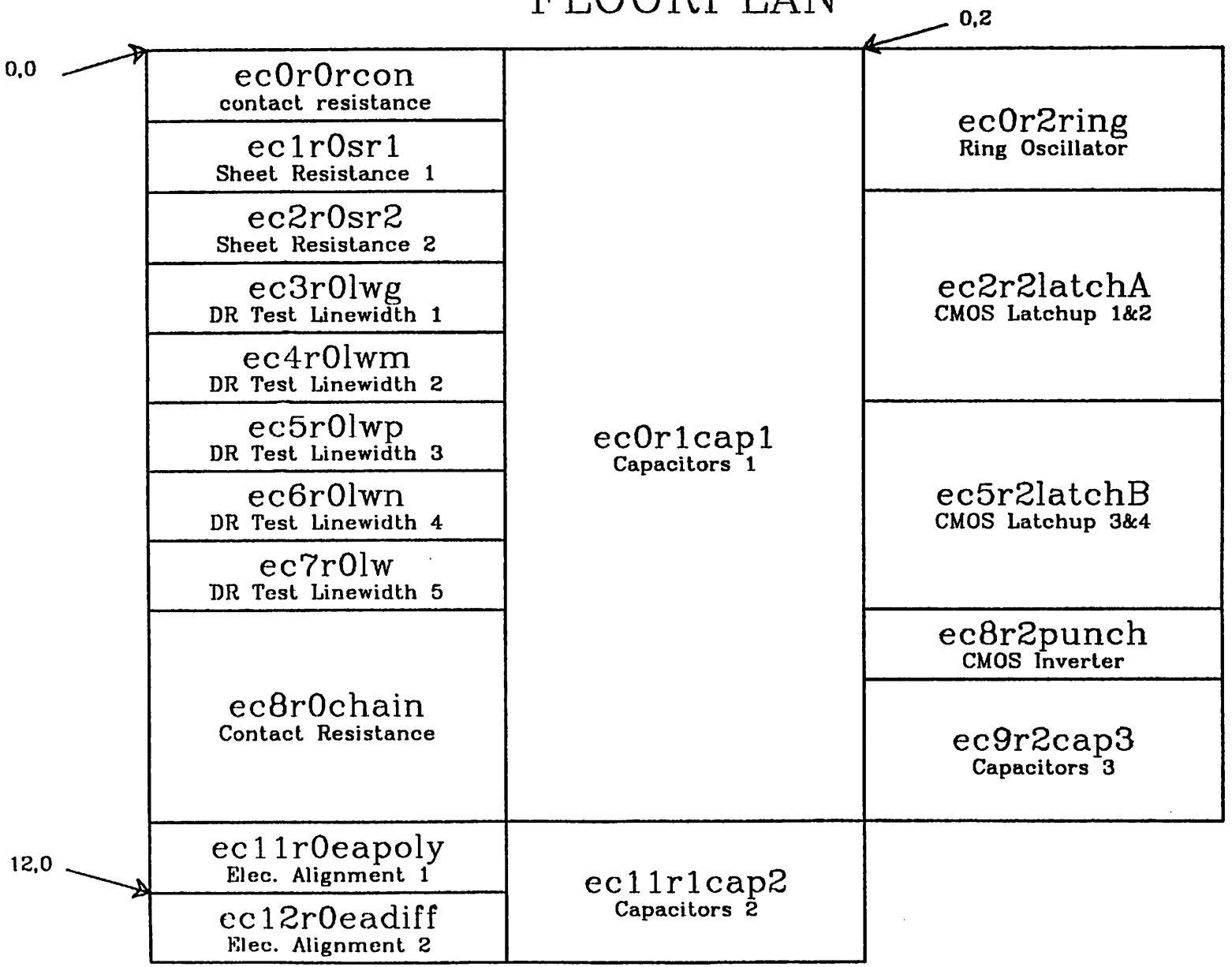
Testing:

Apply a High voltage to the input. Then all the voltage drop is across the PMOS device. Punch-through can be detected by monitoring the current. Similarily, apply a Low voltage to the input. Then all the voltage drop is across the NMOS device. Punch-through occurs if the output voltage drops suddenly.

Pad Assignment:

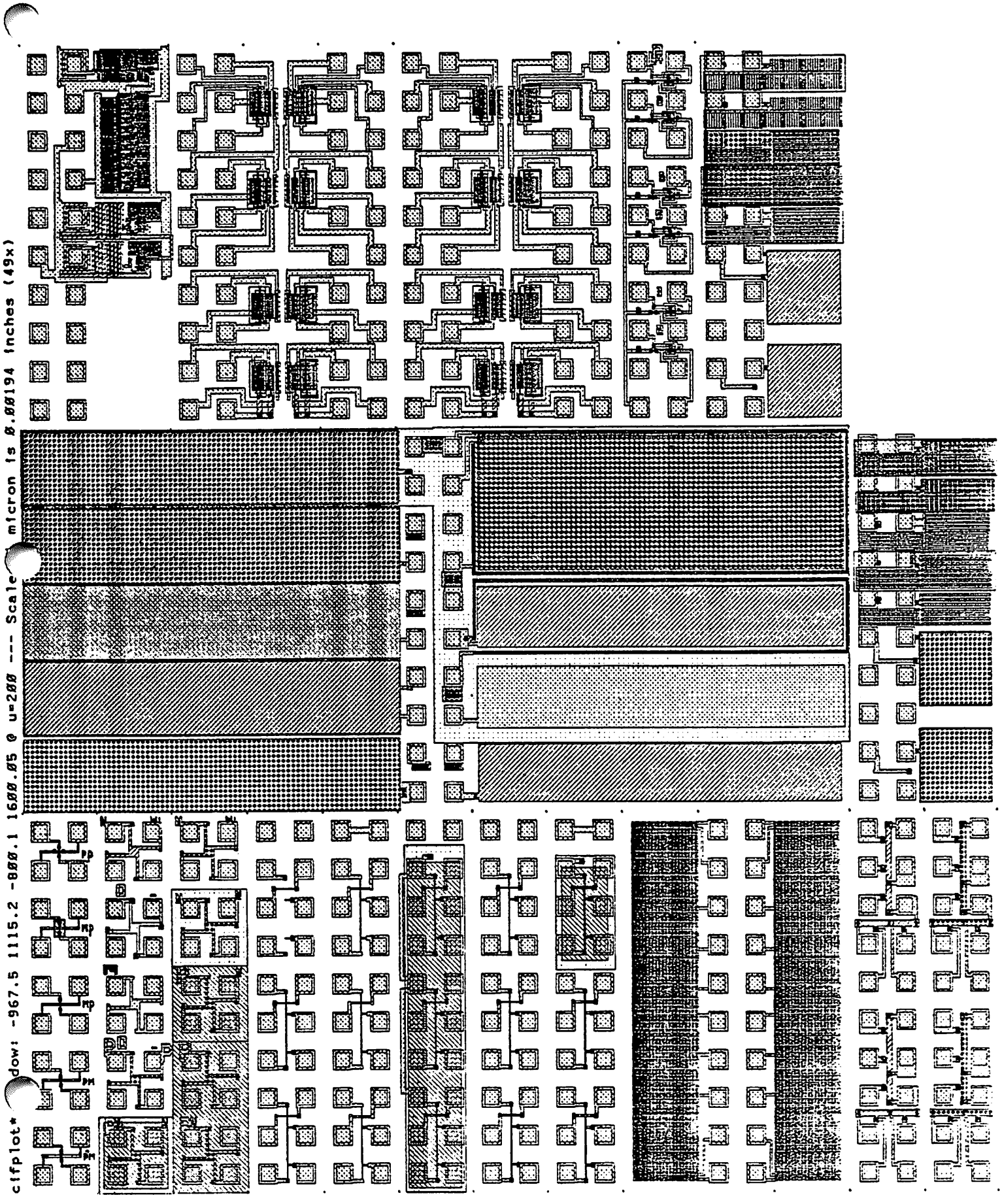
NMOS	PMOS	PAD NUMBER			
L/W	L/W	IN	OUT	VDD	GND
2/4	4/2	1	12	11	10
4/8	8/4	2	13	3	10
3/6	6/3	4	15	14	10
2.5/5	5/2.5	5	16	6	10
1.5/3	3/1.5	7	18	17	10
1/2	2/1	8	19	20	10

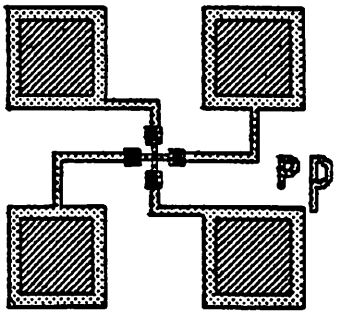
PROCESS COMPLETE TEST PATTERN FLOORPLAN



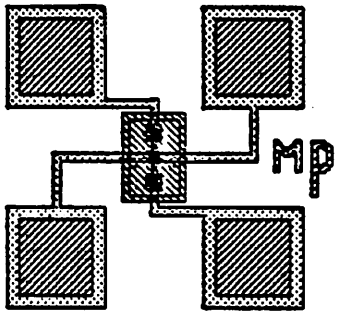
esubchip.cif

process test pattern

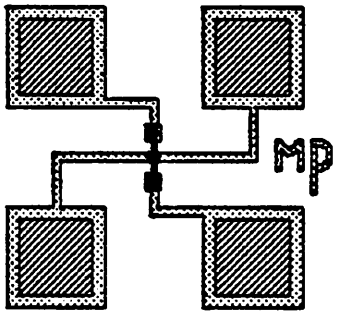




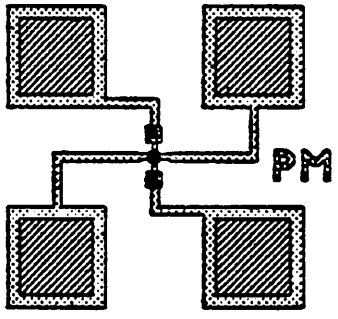
ec0r0con.cif
contact resistance



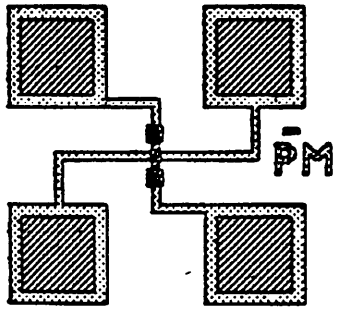
(a) metal – p+ S/D



(b) metal – n+ S/D



(c) metal - poly



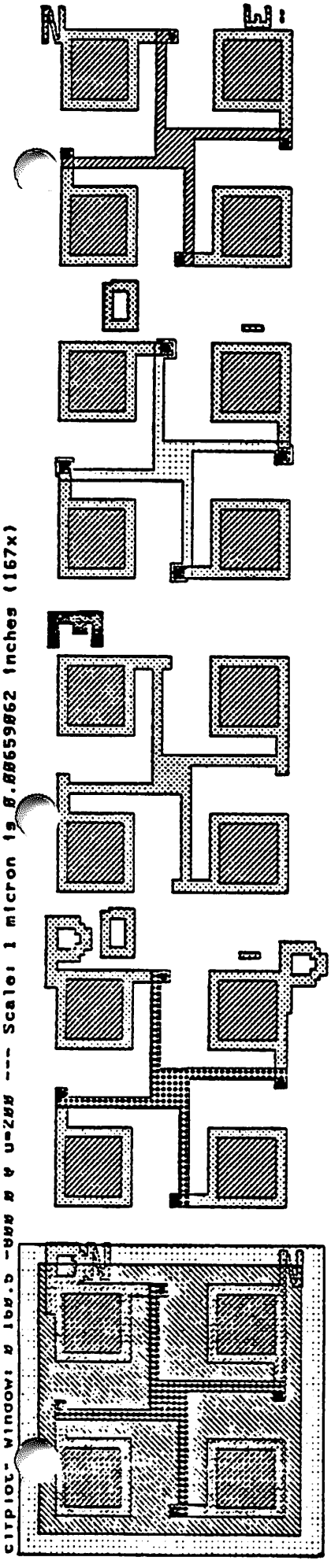
(d) metal - poly

ec0r0con.cif

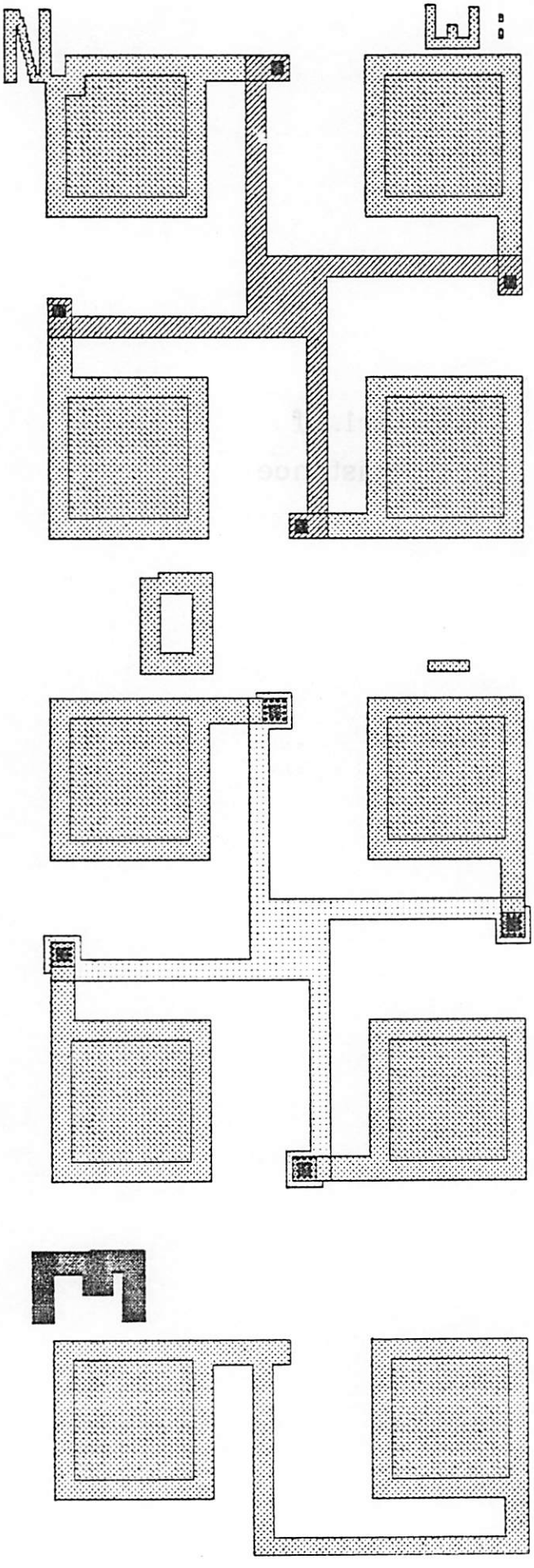
contact resistance

ec0r0con.cif

contact resistance



ec1r0sr1.cif
sheet resistance



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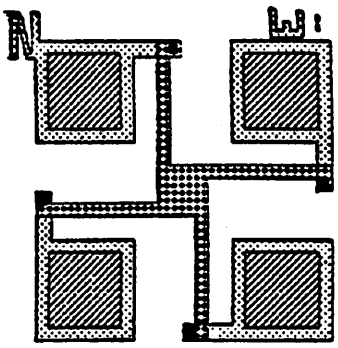
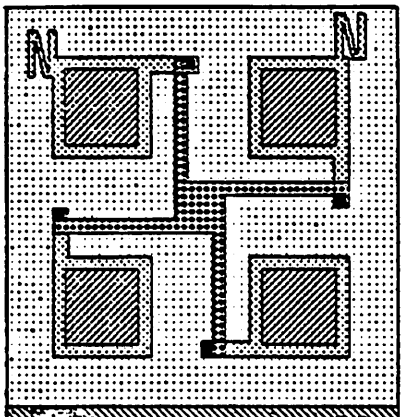
ec1r0sr1.cif

sheet resistance

ec1r0sr1.cif
sheet resistance



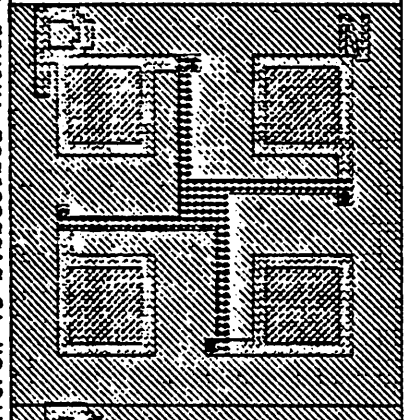
(a) n+ in sub



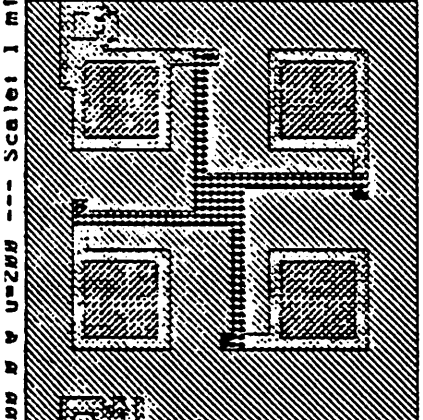
(b) n+ in well

ec2r0sr2

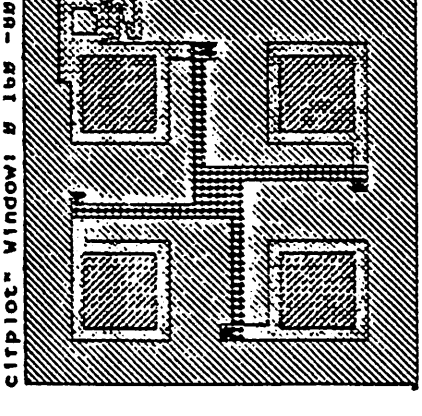
sheet resistance 2



(c) p+ in well



(d) p+ in sub



(e) p+ in sub

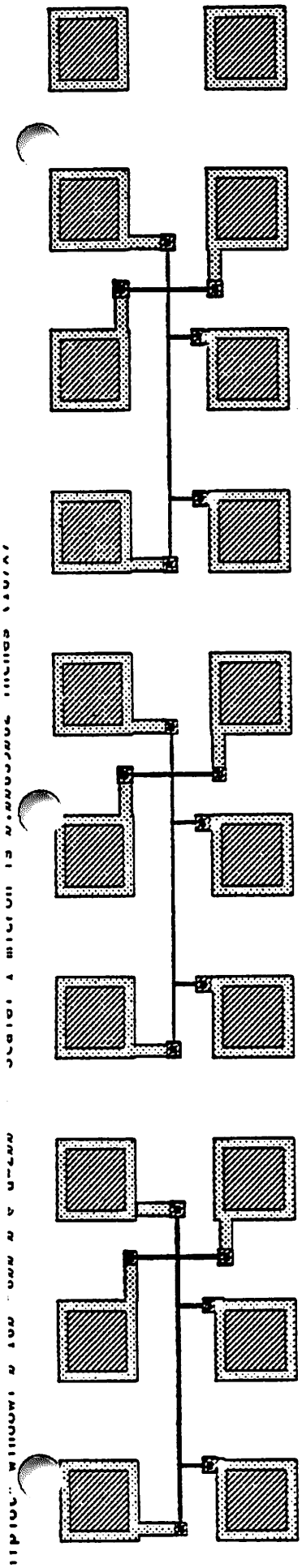
cirplot" Window: # 1bb -### -### # # u=##n --- Scale: 1 micron is #.##659862 inches (167x)

ec2r0sr2

sheet resistance 2

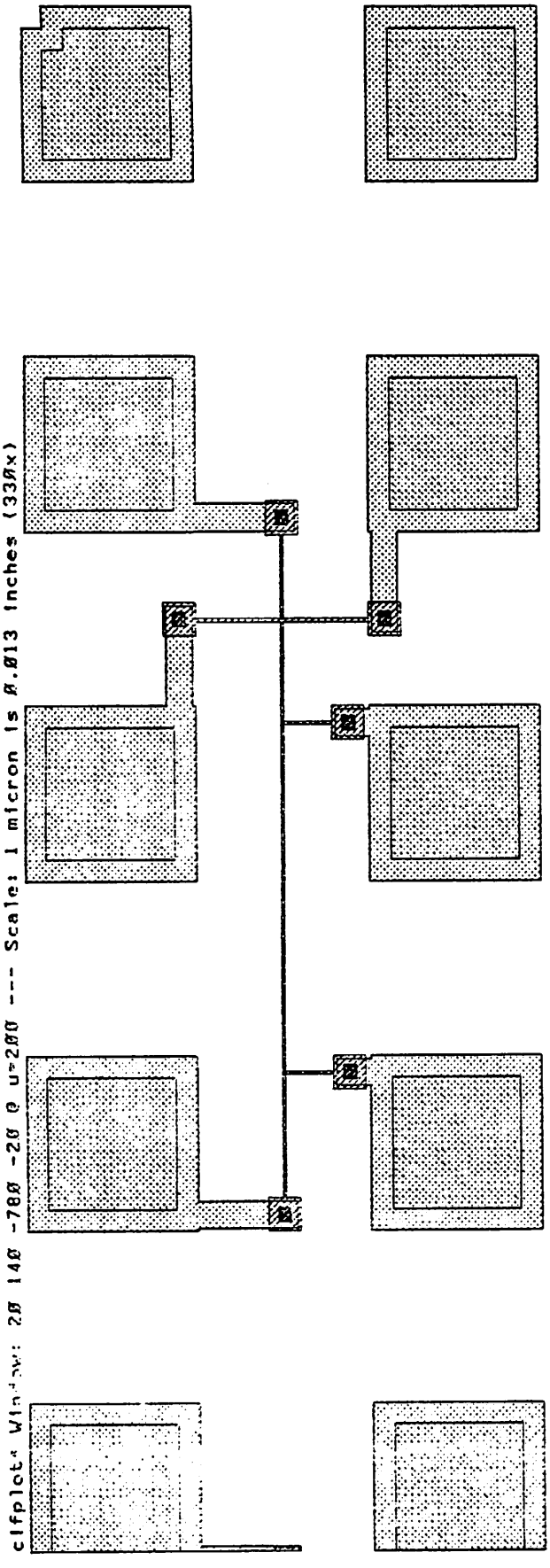
ec2r0sr2

sheet resistance 2



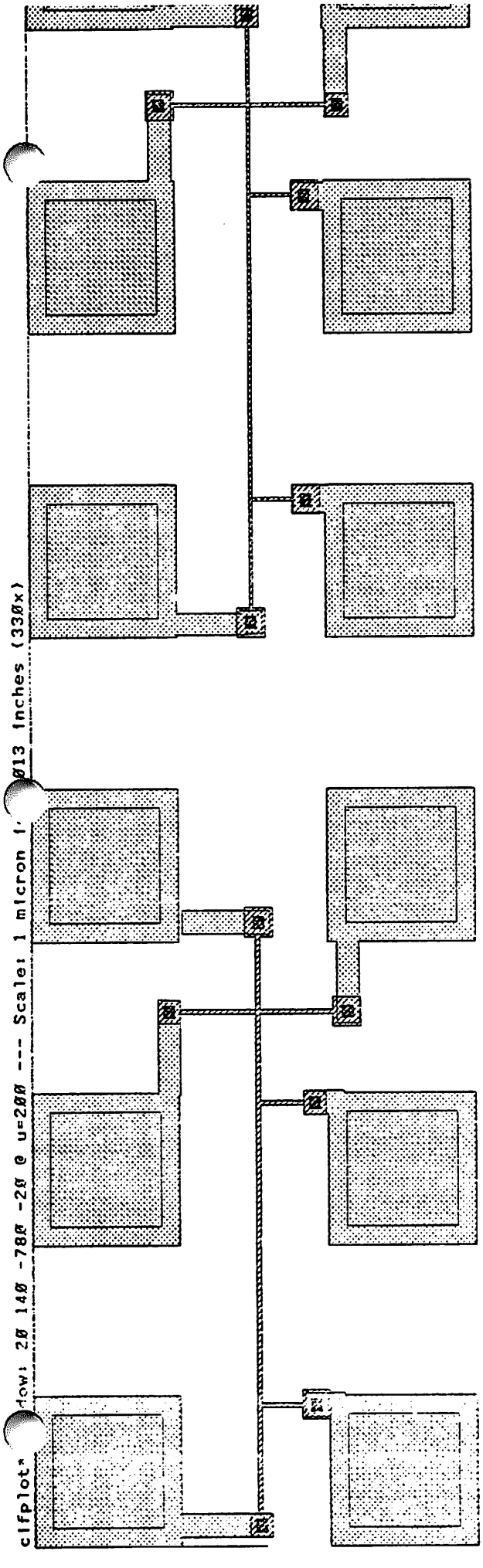
ec3r0lwg.cif

design rule testing
linewidth 1



ec3r0lwg.cif

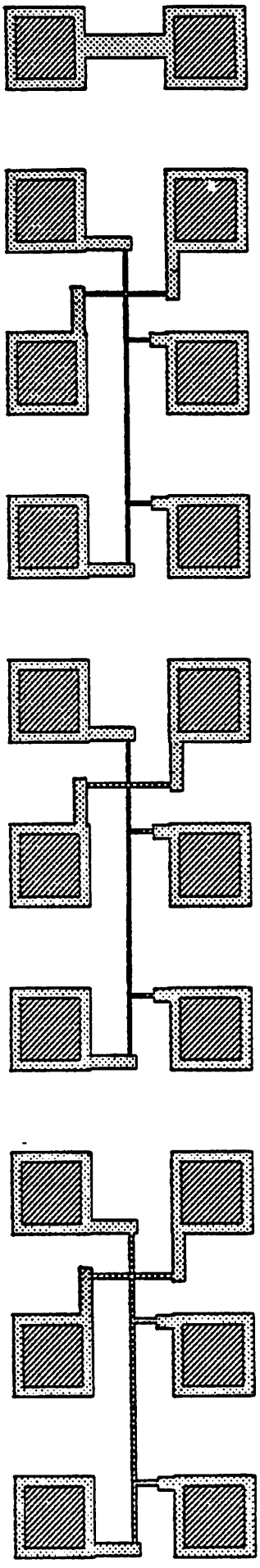
design rule testing
linewidth 1



ec3r0lwg.cif

design rule testing

linewidth 1

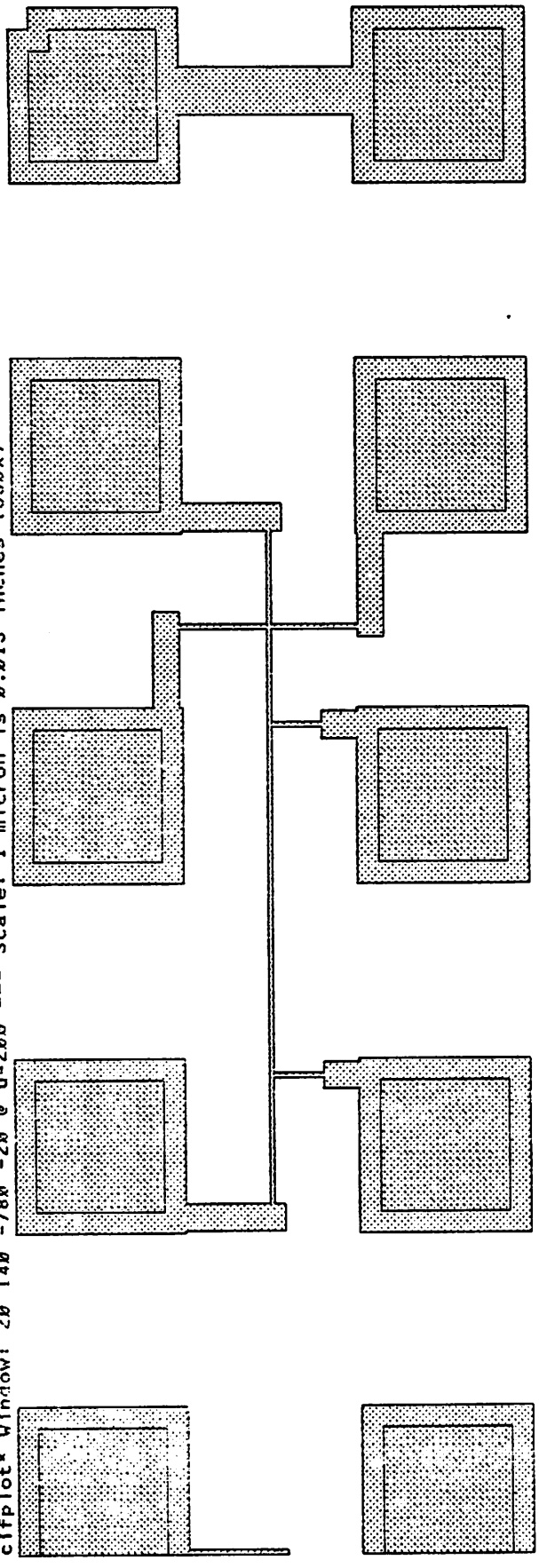


ec4r0lwm.cif

design rule testing
linewidth 2

ec4r0lwm.cif

design rule testing
linewidth 2



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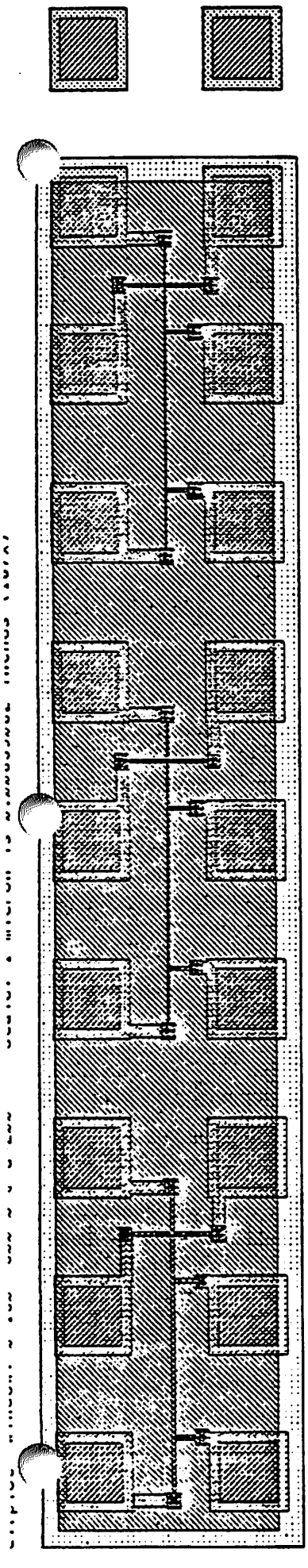
design rule testing
linewidth 2



ec5r0lwp.cif

design rule testing
linewidth 3

ec5r0lwp.cif

design rule testing
linewidth 3

ec5r0lwp.cif

design rule testing
linewidth 3

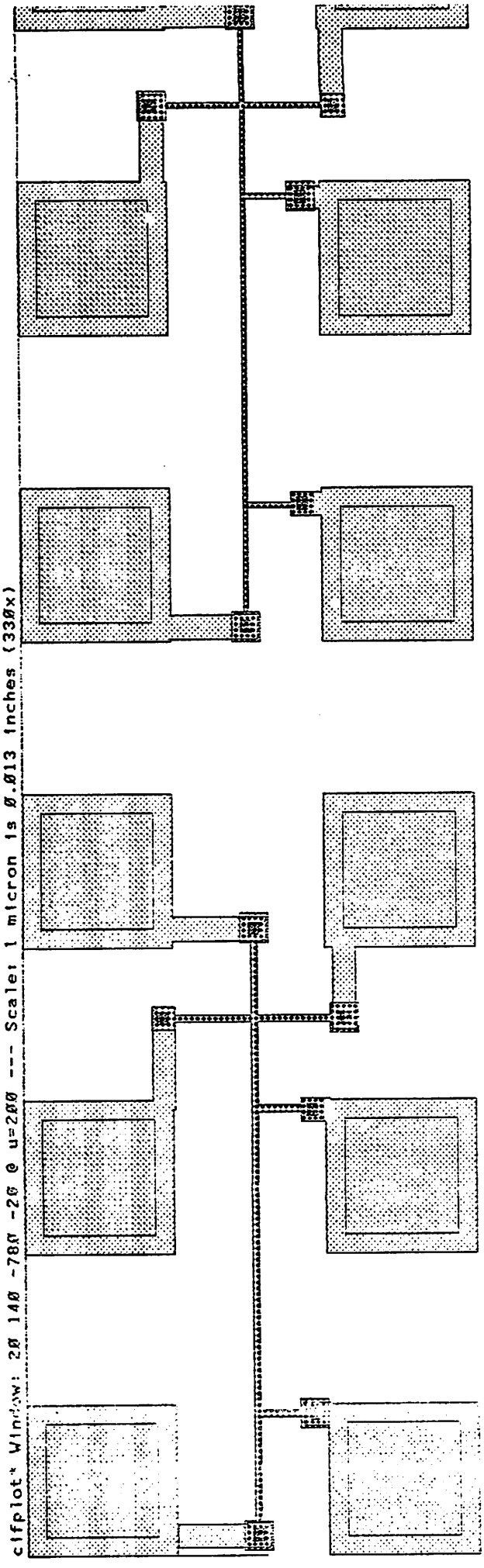
clfplot* Window: @ 168 -888 @ @ u=200 --- Scale: 1 micron is @.00659062 inches (167x)

ec6r0lw.cif

design rule testing
linewidth 4

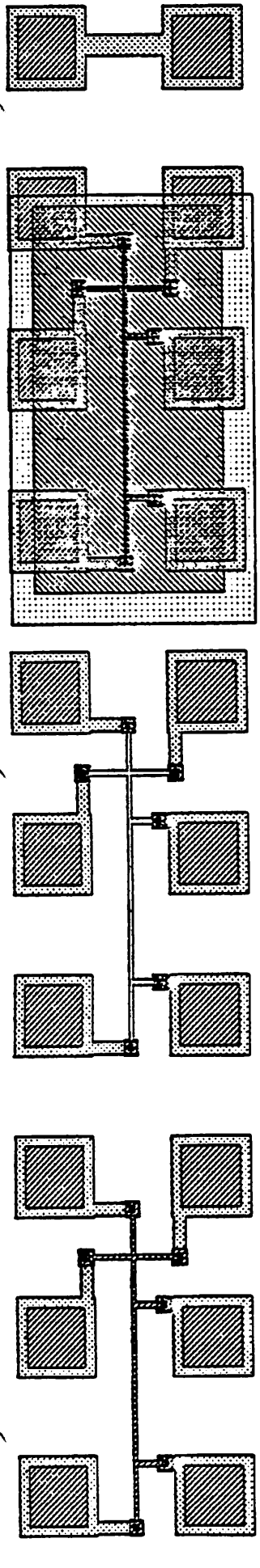
ec6r0lw.cif

design rule testing
linewidth 4



ec6r0lw.cif

design rule testing
linewidth 4



(a) p+ active

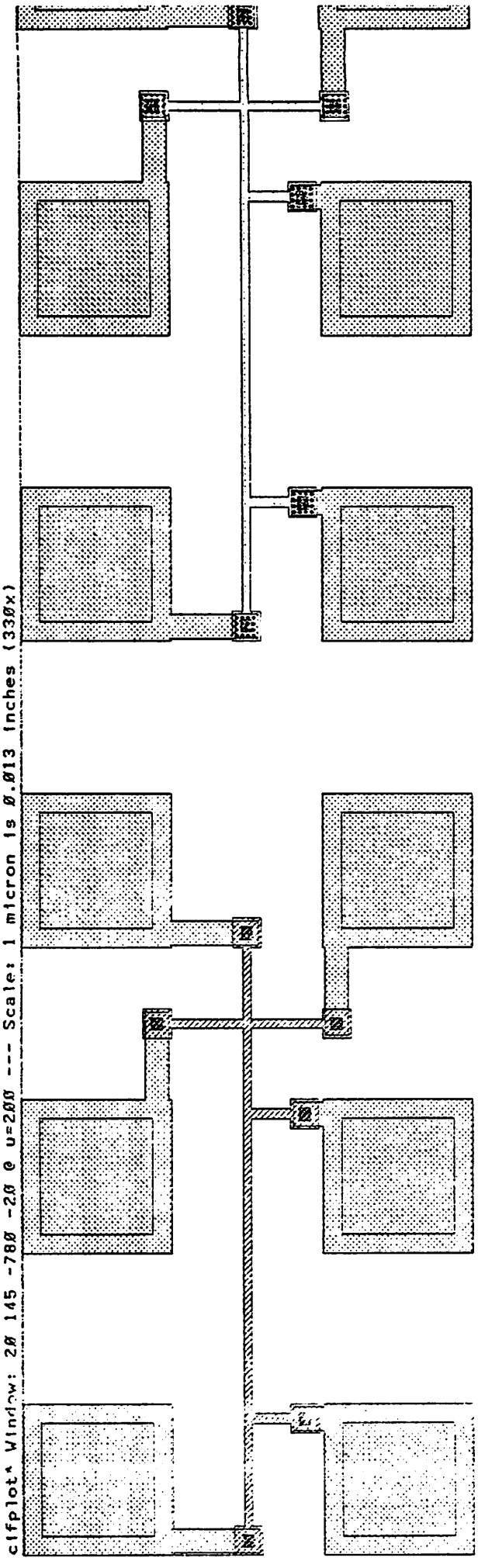
(b) n well

(c) poly

ec7r0lw.cif

design rule testing

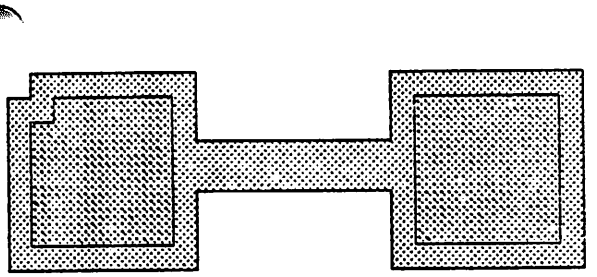
linewidth 5

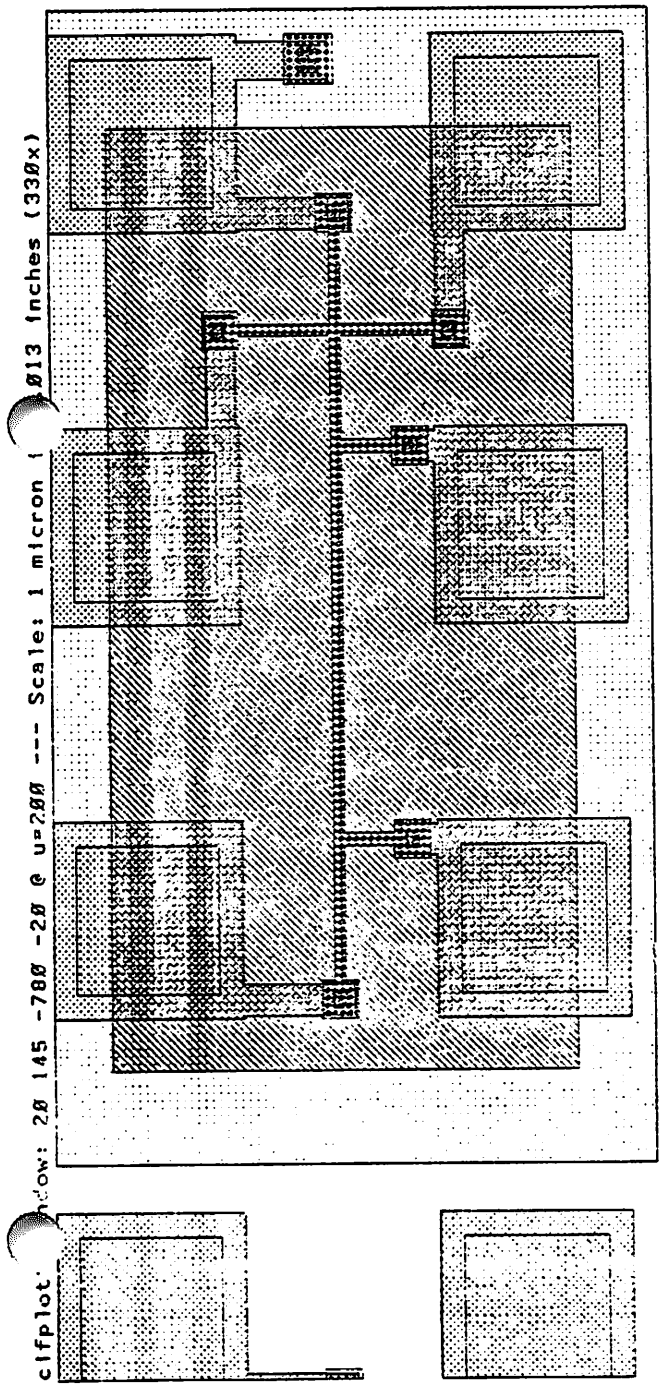


ec7r0lw.cif

design rule testing

linewidth 5



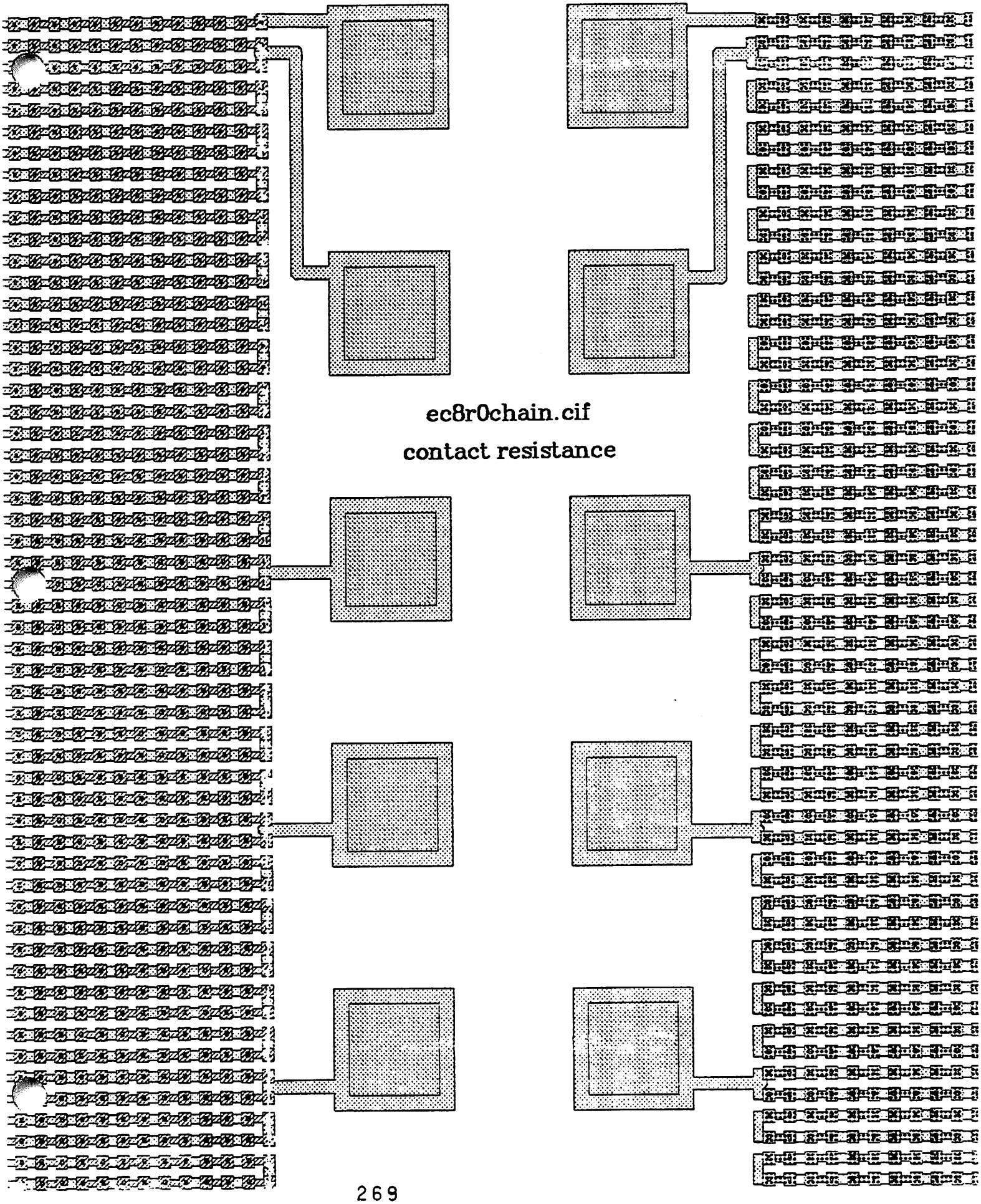


ec7r0lw.cif

design rule testing
linewidth 5

ec8r0chain.cif

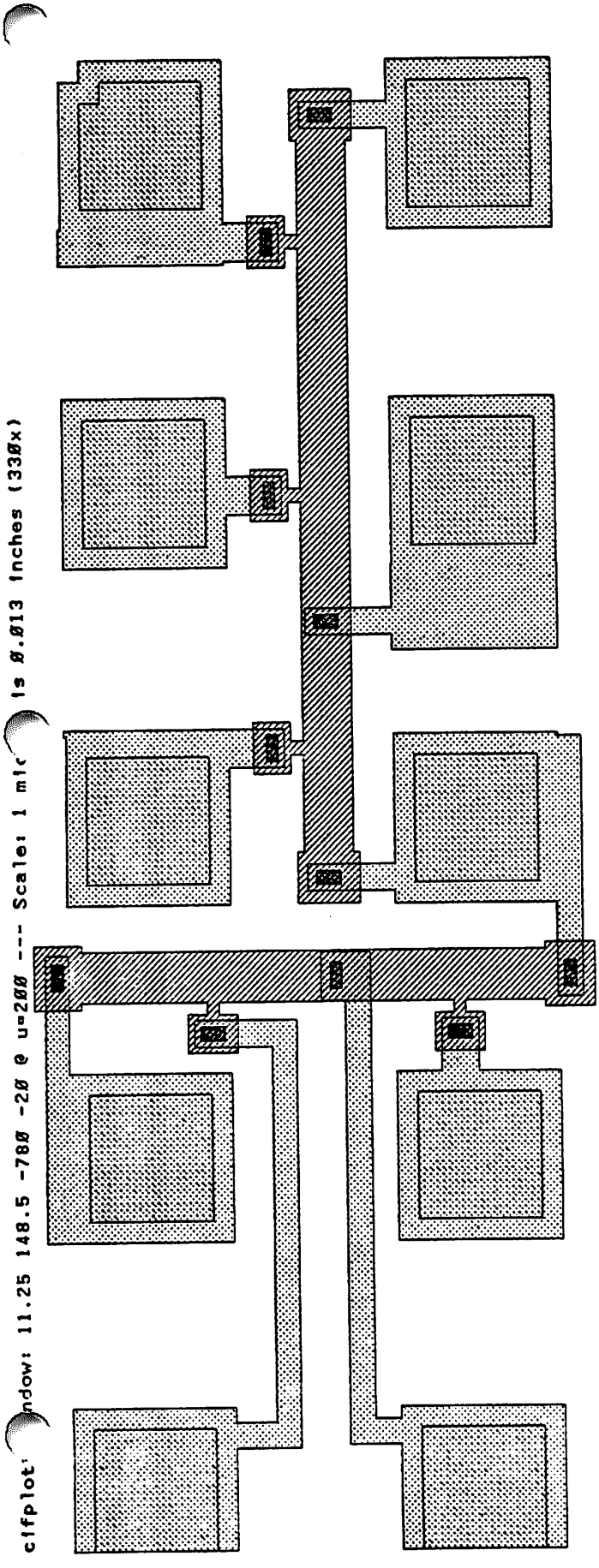
contact resistance



ec8r0chain.cif

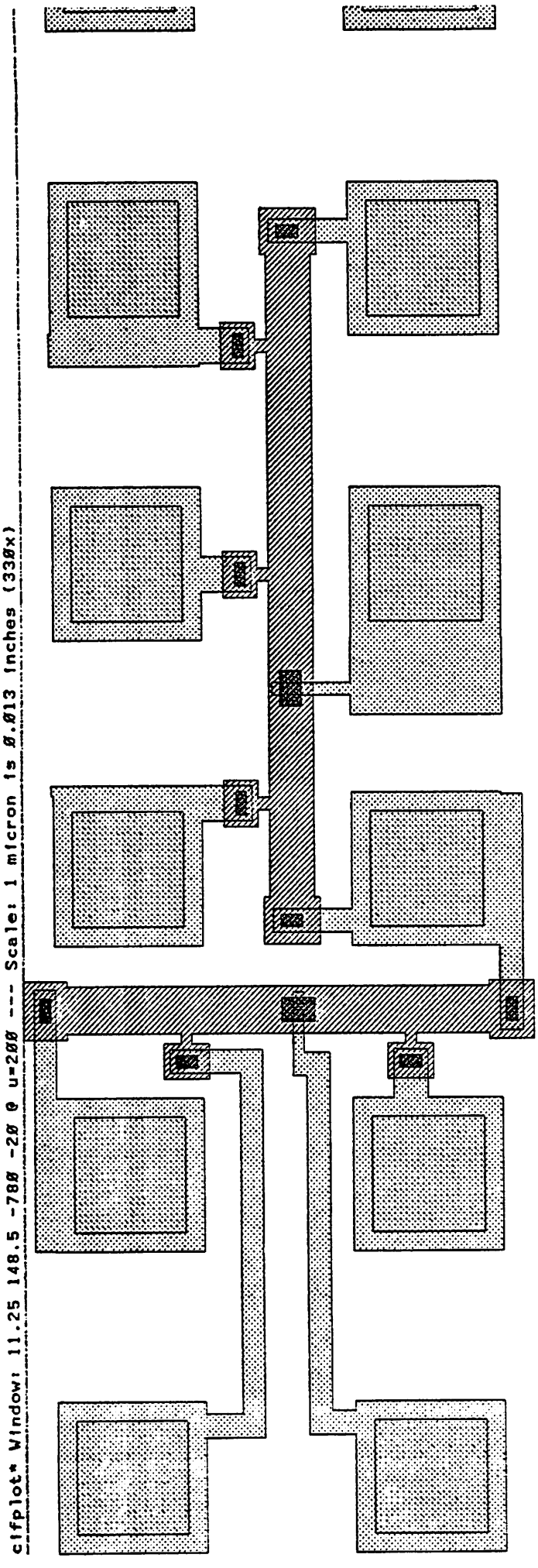
contact resistance

ec11r0eapoly.cif
electrical alignment 1

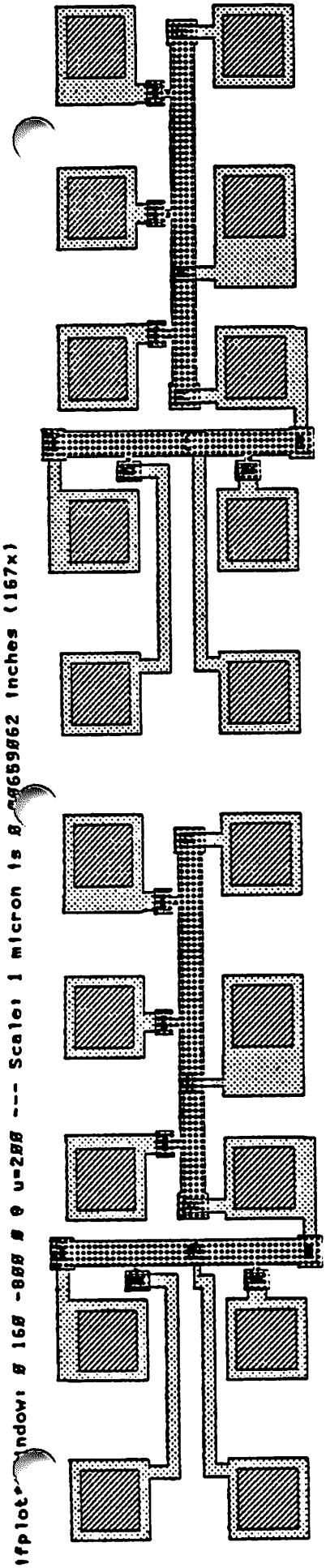


ec11r0eapoly.cif

electrical alignment 1

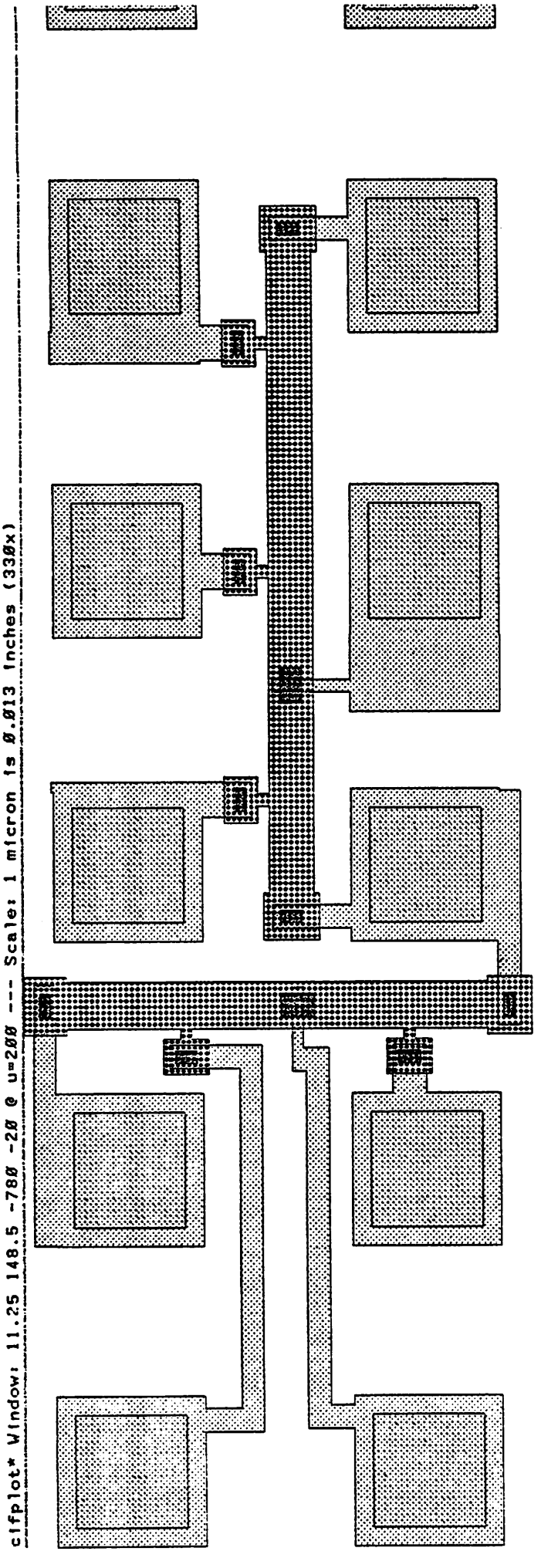


ec11r0eapoly.cif
electrical alignment 1



ec12r0eadiff.cif

electrical alignment 2

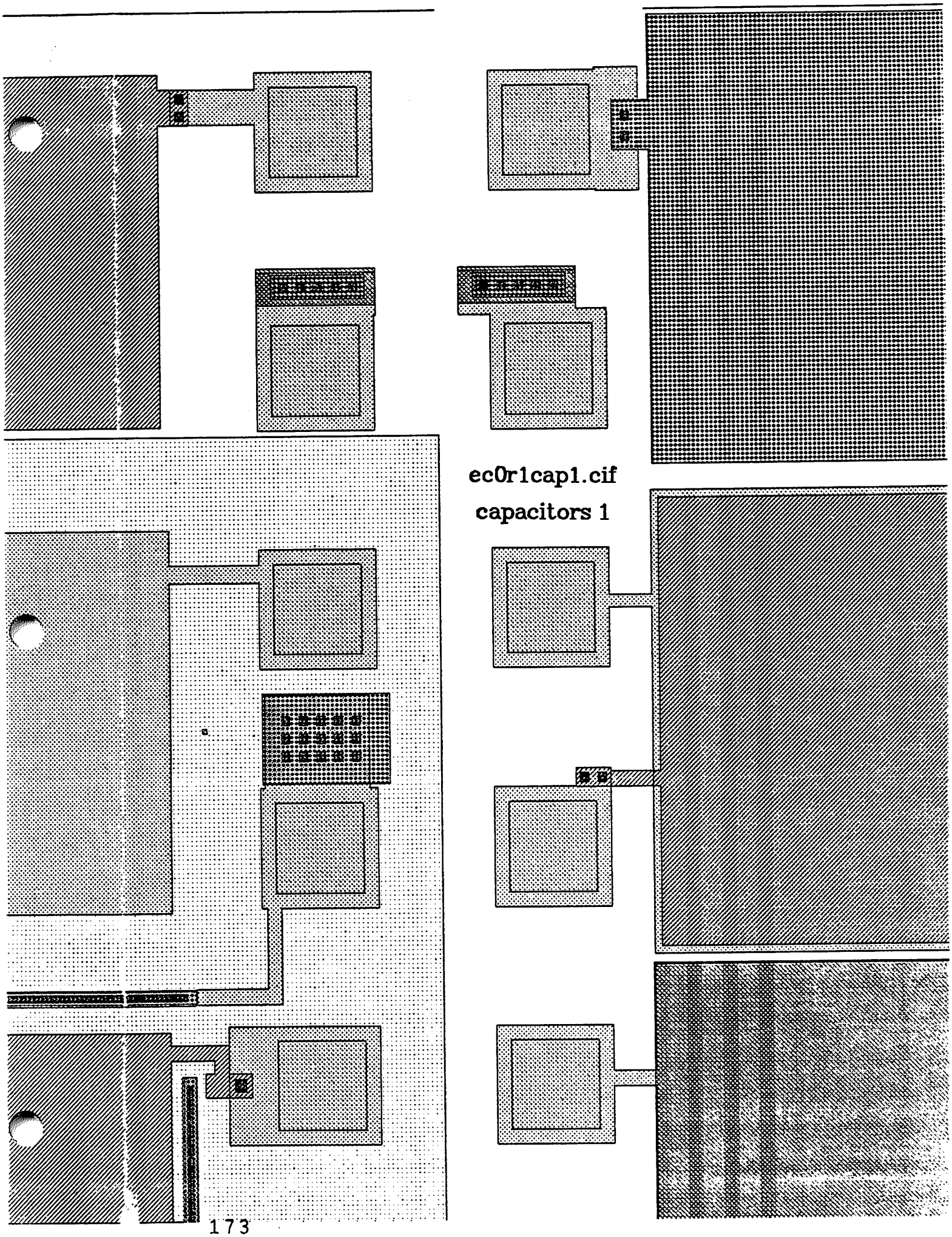


ec12r0eadiff.cif
electrical alignment 2

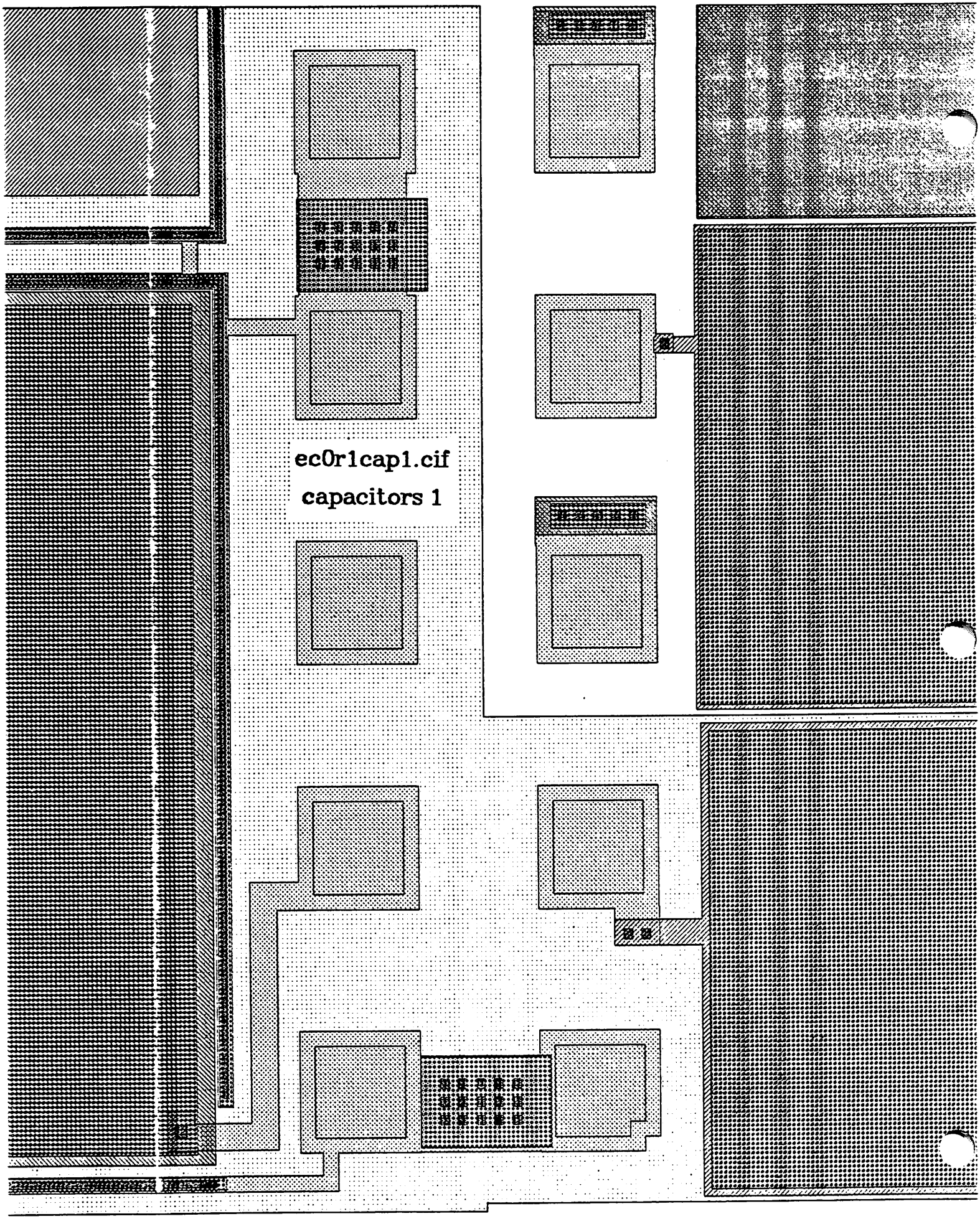
ec12r0eadiff.cif
electrical alignment 2

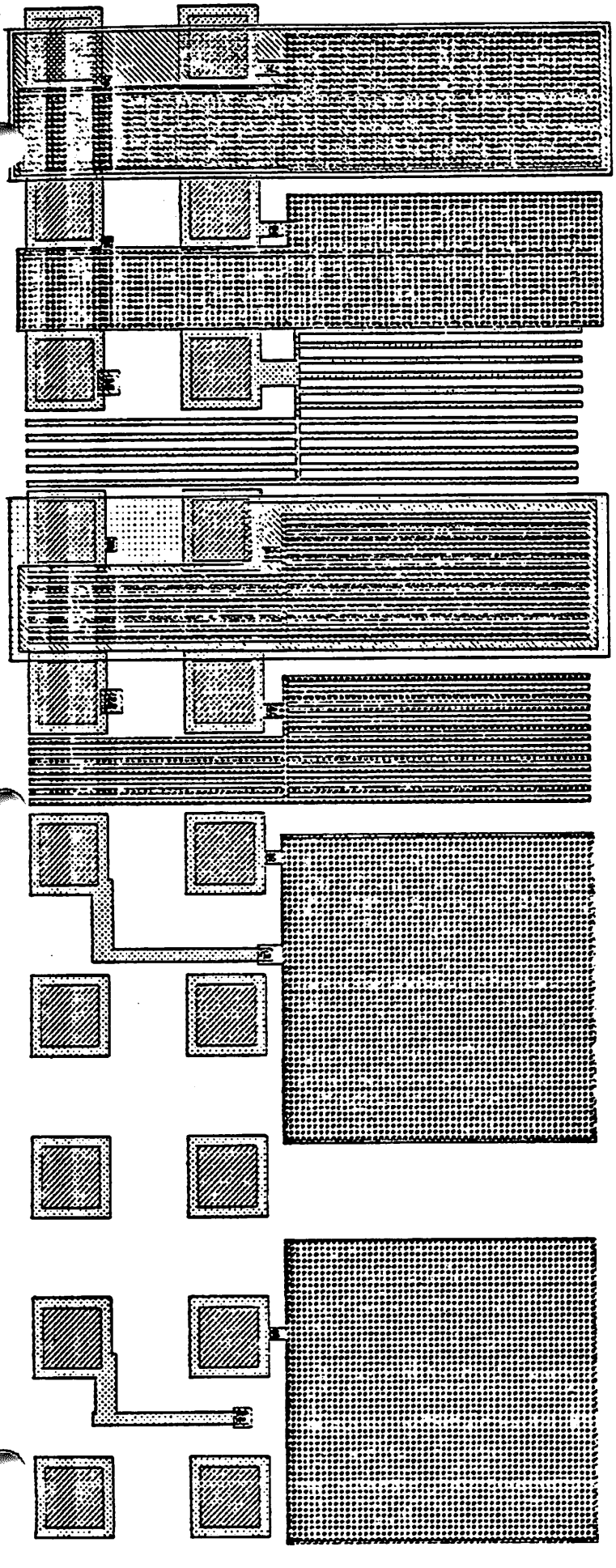
ec0r1cap1.cif

capacitors 1



ec0r1cap1.cif
capacitors 1


ec0r1cap1.cif
capacitors 1



cifplot: Window: @ 318.75 -888 @ @ u=200 --- Scale: 1 micron is 0.00659062 inches (167x)

ec11r1cap2.cif
capacitors 2

(a) C_{fringe} (poly-P+)

(b) C_{fringe} (poly-n+)

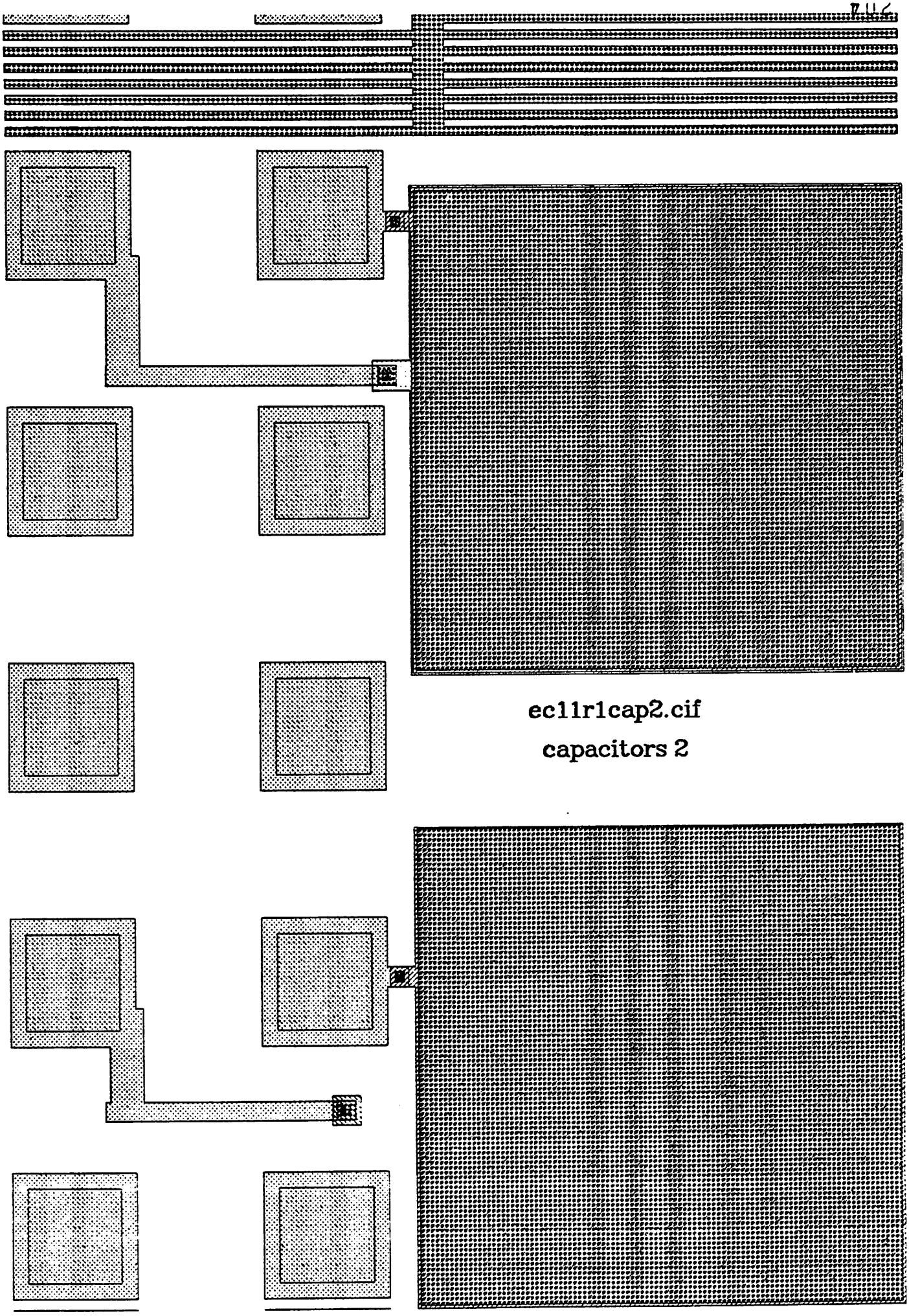
(c) C_{fringe} (Metal-sub)

(d) $C_{j\,edge}$ (p+)

(e) $C_{j\,edge}$ (n+)

(f) C_{gate} (pMOS C-V)

(g) C_{gate} (nMOS C-V)

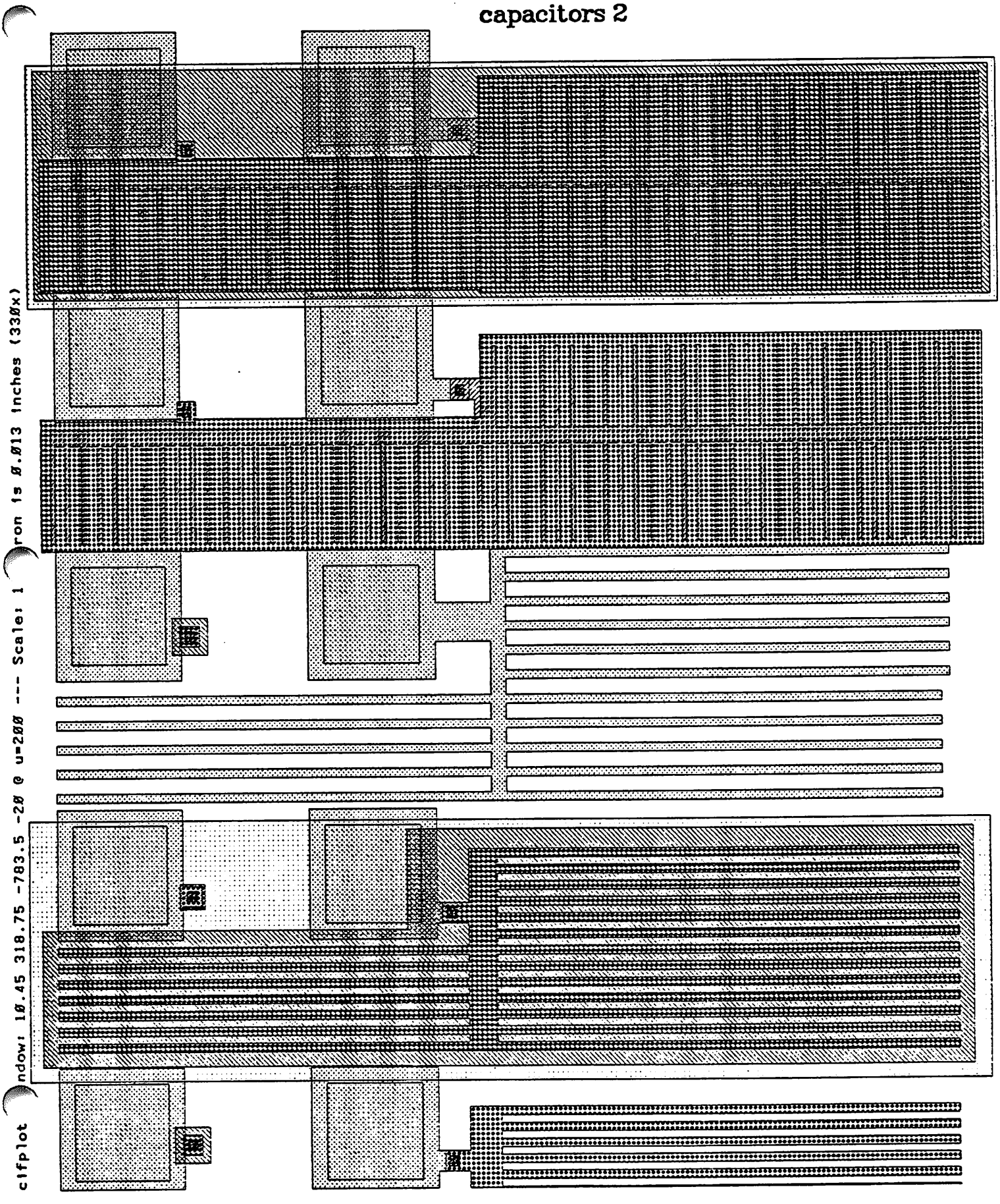


ec11r1cap2.cif

capacitors 2

ec11r1cap2.cif

capacitors 2



cifplot" Window: 20 346.5 -780 20 0 u=200 --- Scale: 1 micron is 0.00659062 inches (167x)

ec0r2ring.cif
ring oscillator

ec0r2ring.cif
clfplot* dow: 40 346.5 -760 16 @ u=200 --- Scale: 1 micron .013 inches (330x)

ec0r2ring.cif

clfplot* Window: 40 346.5 -760 16 0 u=200 --- Scale: 1 micron is 0.013 inches (330x)

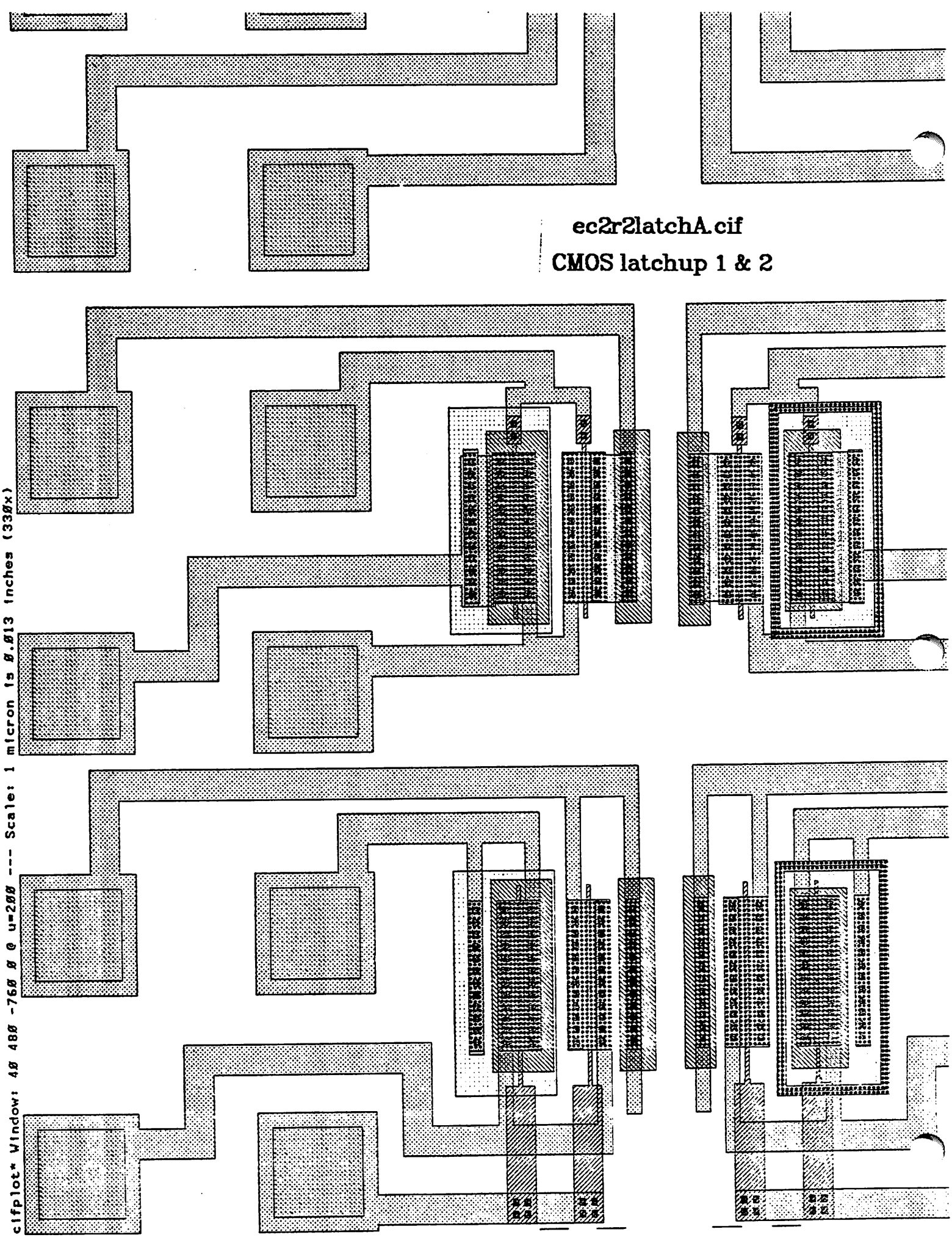
ec2r2latchA.cif

CMOS latchup 1

ec2r2latchA.cif
CMOS latchup 2

ec2r2latchA.cif

CMOS latchup 1 & 2


ec2r2latchA.cif
CMOS latchup 1 & 2
clfplot* Window: 40 480 -760 0 @ u=200 --- Scale: 1 micron is 0.013 inches (330x)

ec5r2latchB.cif

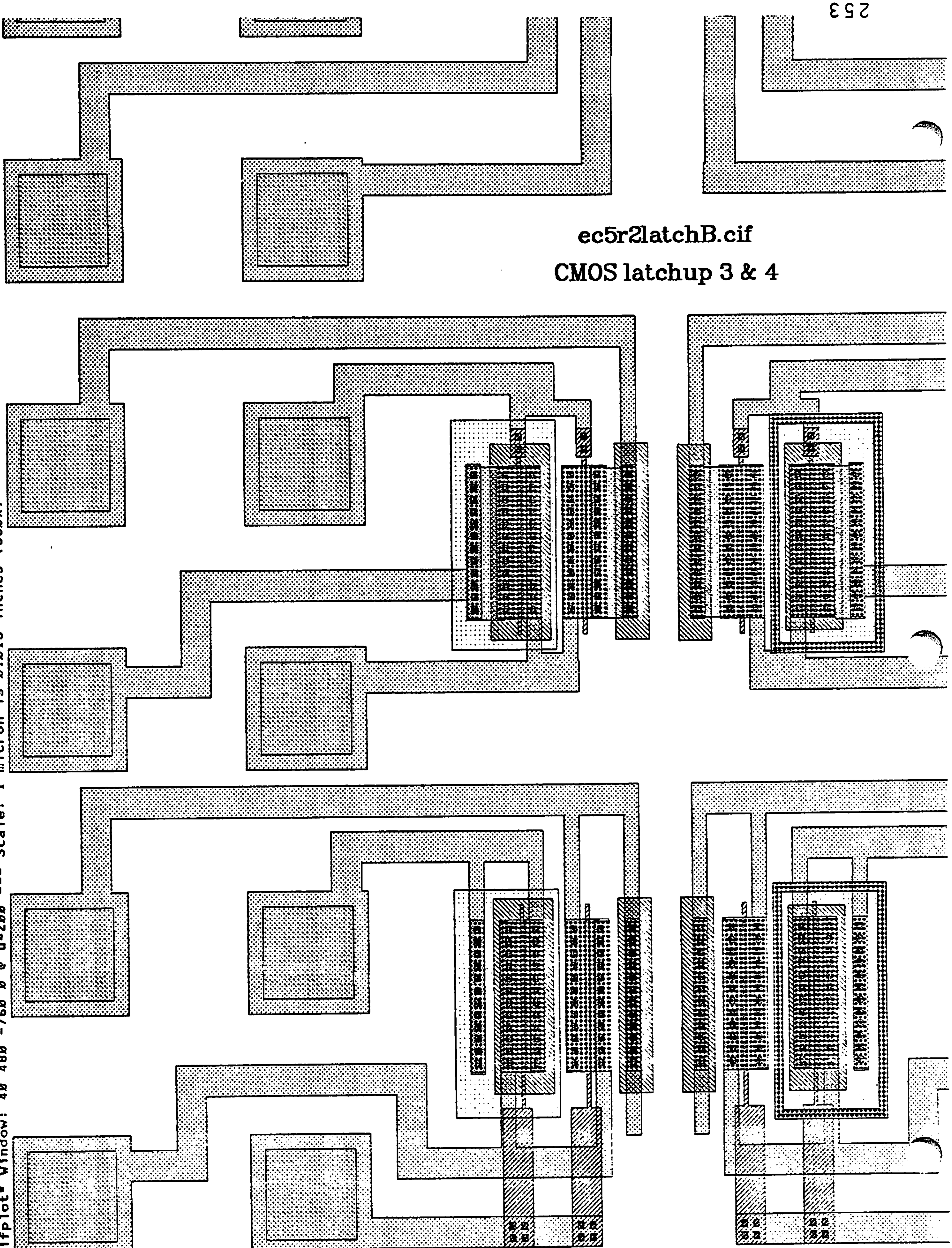
CMOS latchup 3

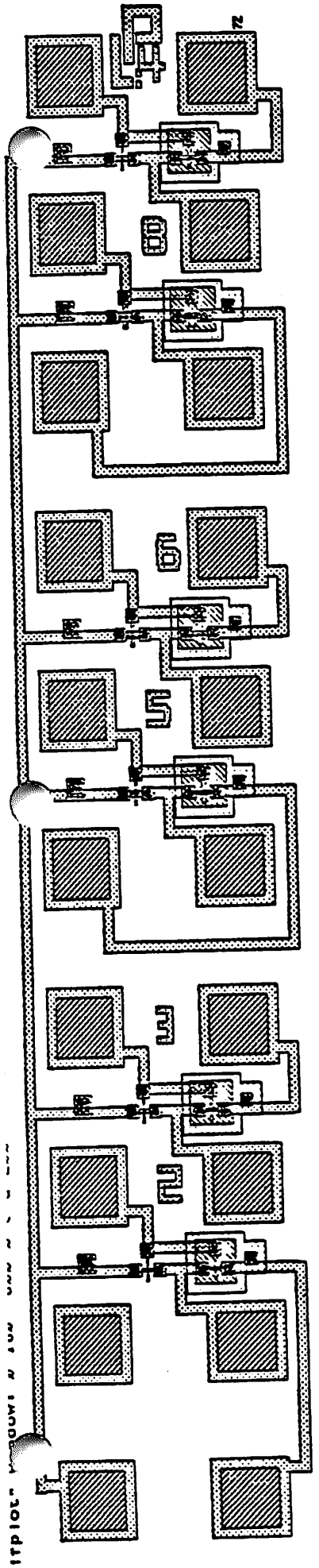
ec5r2latchB.cif

CMOS latchup 4

ec5r2latchB.cif

CMOS latchup 3 & 4


ec5r2latchB.cif
CMOS latchup 3 & 4
cifplot* Window: 40 480 -760 0 @ u=200 --- Scale: 1 micron is 0.013 inches (330x)



ec0r2punch.cif

CMOS inverter

ec0r2punch.cif
CMOS inverter

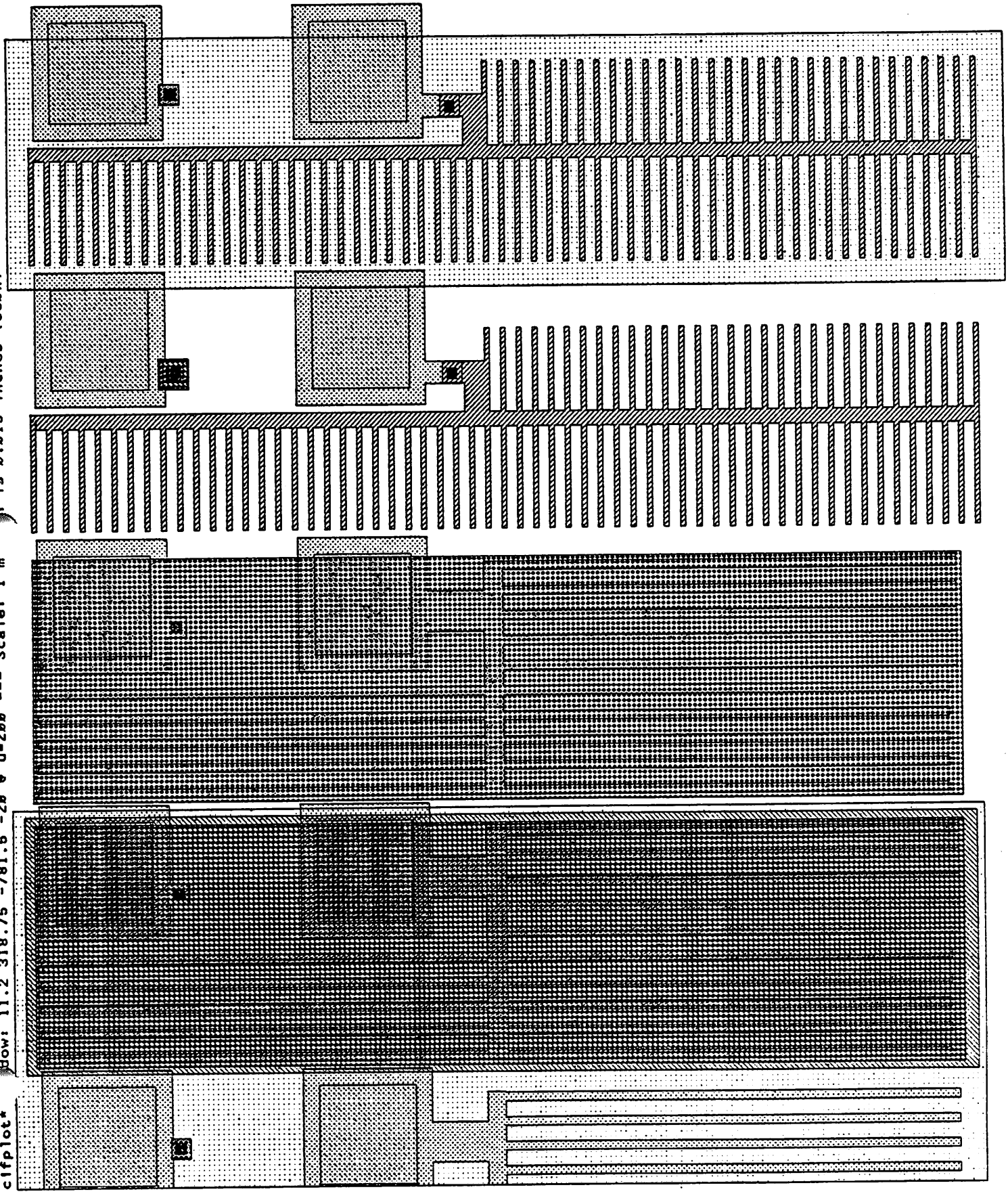
ec0r2punch.cif
CMOS inverter

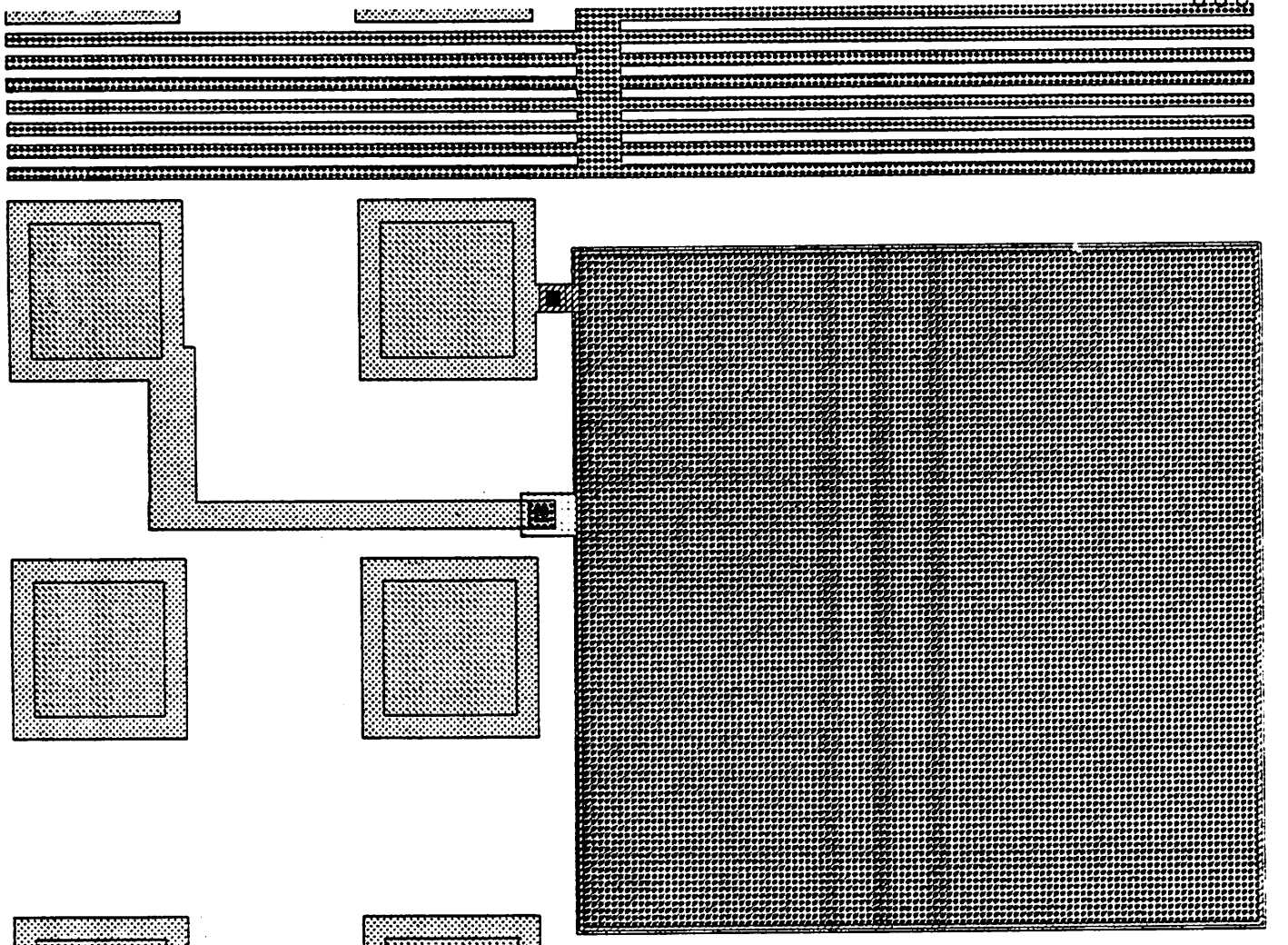
ec9r2cap3.cif

capacitors 3

ec9r2cap3.cif

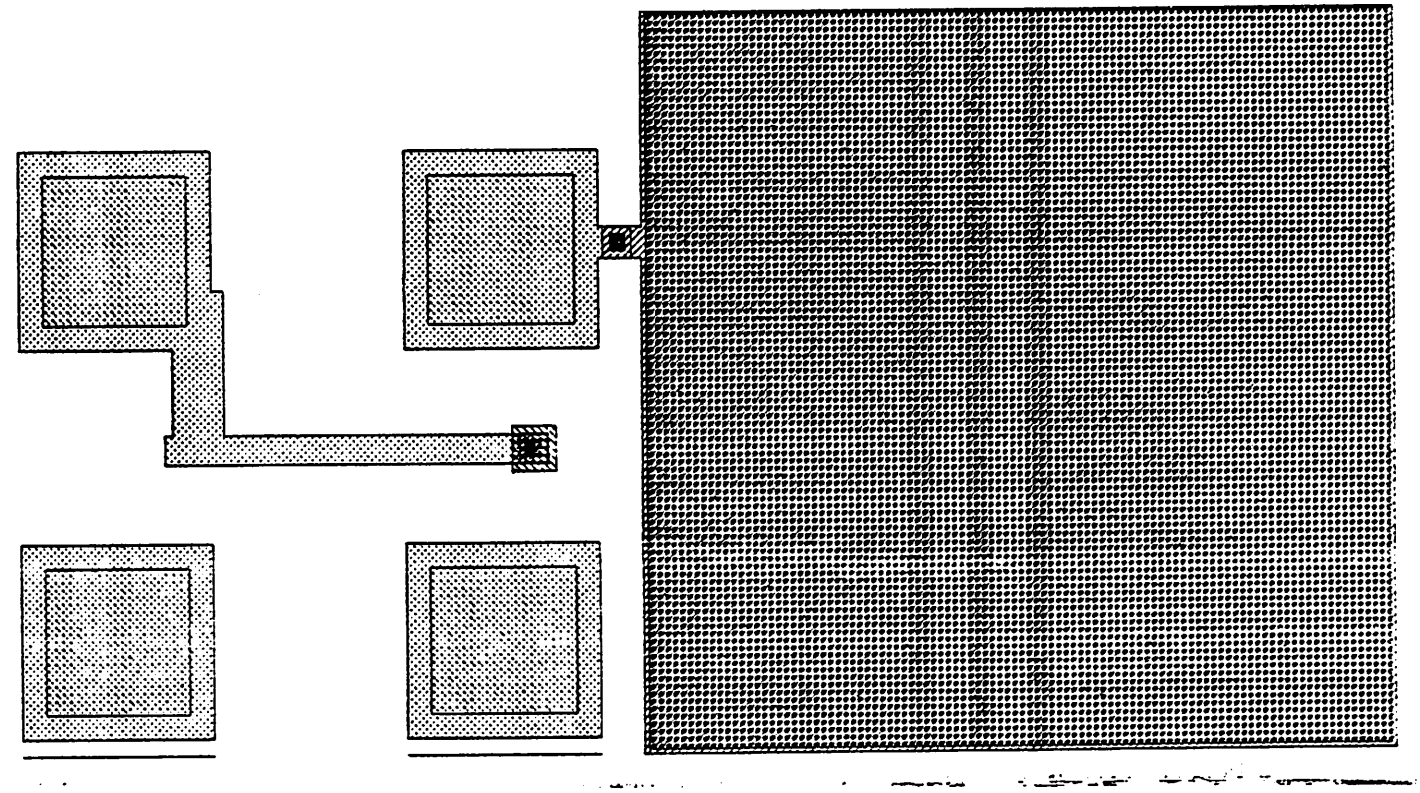
capacitors 3





ec9r2cap3.cif

capacitors 3



Process Test Pattern (esubchip)
Cif File Cell Hierarchy

272.k

372.k

472.k

51.k

52.k

53.k

54.k
  51.k 52.k CS5CONAR.k FRAME6.k

57.k

572.k

60.k
  51.k 52.k CSCUT2P5S.k CSCUT2S.k
  CSCUT3S.k CSCUT4S.k FRAME7.k

672.k

872.k

BTODIFFCON.k

BTOPOLYCON.k

CB1NTRN1P5X3.k
  BTODIFFCON.k BTOPOLYCON.k

CB1NTRN1X2.k
  BTODIFFCON.k BTOPOLYCON.k

CB1NTRN2P5X5.k
  BTODIFFCON.k BTOPOLYCON.k

CB1NTRN2X1P.k
  BTODIFFCON.k BTOPOLYCON.k

CB1NTRN2X4.k
  BTODIFFCON.k BTOPOLYCON.k

CB1NTRN3X1P5.k
  BTODIFFCON.k BTOPOLYCON.k

CB1NTRN3X6.k
  BT0DIFFCON.k BT0POLYCON.k

CB1NTRN4X2P.k
  BT0DIFFCON.k BT0POLYCON.k

CB1NTRN4X8.k
  BT0DIFFCON.k BT0POLYCON.k

CB1NTRN5X2P5.k
  BT0DIFFCON.k BT0POLYCON.k

CB1NTRN6X3P.k
  BT0DIFFCON.k BT0POLYCON.k

CB1NTRN8X4P.k
  BT0DIFFCON.k BT0POLYCON.k

CB2INVCONP.k
  BT0DIFFCON.k

CB3VDPPP.k
  BT0DIFFCON.k

CC3RING.k

CC3RINGS.k
  CC3RING.k

CONCUT6X6.k

CS5CONAR.k
  CSCUT2P5S.k CSCUT2S.k CSCUT3S.k CSCUT4S.k

CSCUT2.k

CSCUT2P5.k

CSCUT2P5S.k
  CSCUT2P5.k

CSCUT2S.k
  CSCUT2.k

CSCUT3.k

CSCUT3S.k
  CSCUT3.k

CSCUT4.k

CSCUT4S.k
  CSCUT4.k

D48.k

DWNINPAD.k
  CONCUT6X6.k DWNTRUPAD.k

DWNOUTPAD.k
  CONCUT6X6.k DWNTRUPAD.k

DWNPJMPAD.k
  CONCUT6X6.k

DWNTRUPAD.k

FRAME6.k
  53.k

FRAME7.k
  57.k

GBINVERT4.k
  NPLUSCON.k NTRANSA4.k PPLUSCON.k PTRANSA4.k

GBINVERT8.k
  NPLUSCON.k NTRANSA4.k PPLUSCON.k PTRANSA4.k

INVERT4.k
  NPLUSCON.k NTRANSA4.k PPLUSCON.k PTRANSA4.k

INVERT8.k
  NPLUSCON.k NTRANSA4.k PPLUSCON.k PTRANSA4.k

M48.k

N72.k

NPLUSCON.k
  CONCUT6X6.k

NTRANSA4.k
  CONCUT6X6.k

NTRANSB4.k
  CONCUT6X6.k

P48.k

P72.k

PAD.k

PADSET.k
  PAD.k

PGBINVERT4.k

```
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PGBINVERT8.k
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PINVERT4.k
  NPLUSCON.k  NTRANSB4.k  PPLUSCON.k  PTRANSB4.k

PINVERT8.k
  NPLUSCON.k  NTRANSB4.k  PPLUSCON.k  PTRANSB4.k

PPLUSCON.k
  CONCUT6X6.k

PTRANSA4.k
  CONCUT6X6.k

PTRANSB4.k
  CONCUT6X6.k

SB2CAPDIFPLY.k

SBPOLYCONT.k

ec0r0rcon.k
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  M48.k  P48.k  PADSET.k

ec0r1cap1.k
  BT0POLYCON.k  PADSET.k  SB2CAPDIFPLY.k
  SBPOLYCONT.k  sb2capmp.k  sb2cappol.k
  sbmetsub.k

ec0r2ring.k
  CC3RINGS.k  CONCUT6X6.k  DWNINPAD.k
  DWNOUTPAD.k  DWNPJMPAD.k  PAD.k

ec11r0eapoly.k
  PADSET.k

ec11r1cap2.k
  PAD.k

ec12r0eadiff.k
  PADSET.k

ec1r0sr1.k
  BT0POLYCON.k  CB3VDPPP.k  N72.k
  P72.k  PADSET.k

ec2r0sr2.k
  CB3VDPPP.k  N72.k  P72.k  PADSET.k

ec2r2latchA.k
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  PAD.k  PGBINVERT4.k  PINVERT4.k

ec3r0lwg.k
  BT0POLYCON.k  PADSET.k

ec4r0lwm.k
  PADSET.k

ec5r0lwp.k
  BT0DIFFCON.k  PADSET.k

ec5r2latchB.k
  CONCUT6X6.k  GBINVERT8.k  INVERT8.k
  PAD.k  PGBINVERT8.k  PINVERT8.k

ec6r0lwn.k
  BT0DIFFCON.k
  PADSET.k
ec7r0lw.k
  BT0DIFFCON.k
  PADSET.k

ec8r0chain.k
  54.k
  60.k  PADSET.k

ec8r2punch.k
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  CB1NTRN1P5X3.k  CB1NTRN1X2.k  CB1NTRN2P5X5.k
  CB1NTRN2X1P.k  CB1NTRN2X4.k  CB1NTRN3X1P5.k
  CB1NTRN3X6.k  CB1NTRN4X2P.k  CB1NTRN4X8.k
  CB1NTRN5X2P5.k  CB1NTRN6X3P.k  CB1NTRN8X4P.k
  CB2INVCONP.k  PADSET.k

ec9r2cap3.k
  PAD.k

esubchip.k
  ec0r0rcon.k  ec0r1cap1.k  ec0r2ring.k
  ec11r0eapoly.k  ec11r1cap2.k  ec12r0eadiff.k
  ec1r0sr1.k  ec2r0sr2.k  ec2r2latchA.k
  ec3r0lwg.k  ec4r0lwm.k  ec5r0lwp.k
  ec5r2latchB.k  ec6r0lwn.k  ec7r0lw.k
  ec8r0chain.k  ec8r2punch.k  ec9r2cap3.k

sb2capmp.k

sb2cappol.k

sbmetsub.k
```

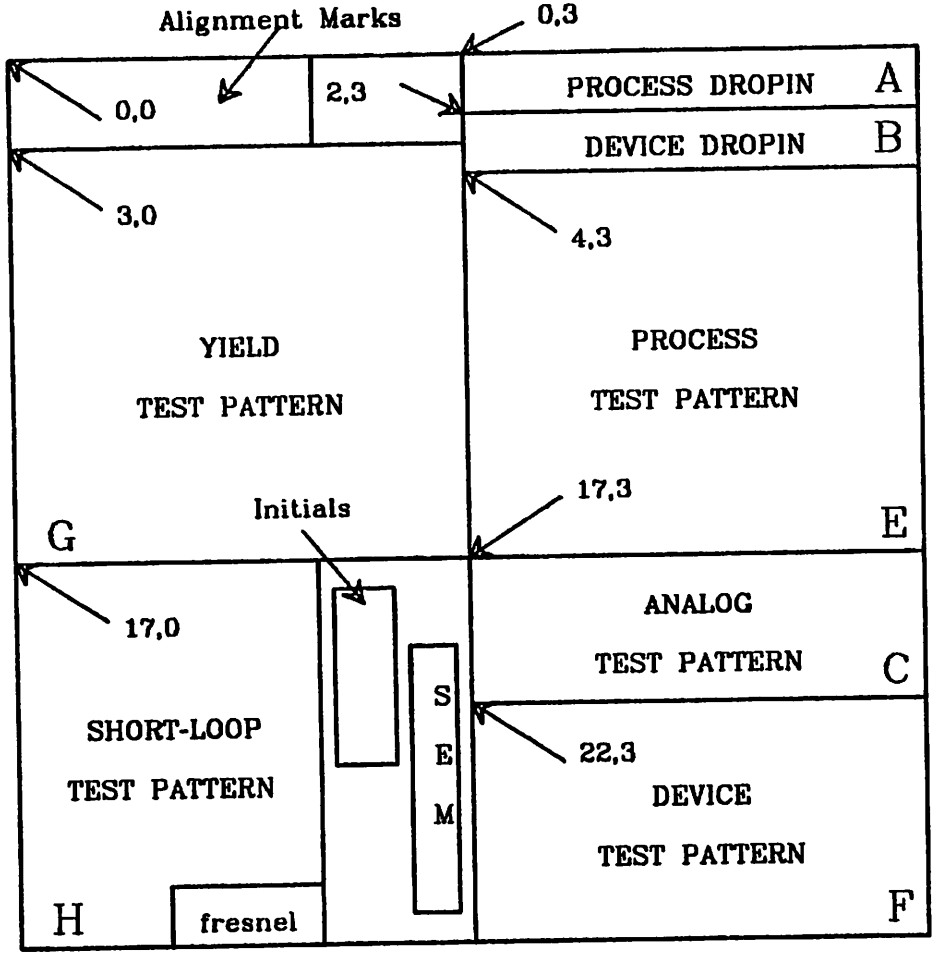
EE290 TEST CHIP ORGANIZATION

The EE290 test chip is made up of 7 Test Patterns plus a separate section for alignment marks. The 7 Test Patterns are: Device, Device Drop-in, Process, Process Drop-in, Shortloop, Yield, and Analog. Each test pattern consists of a collection of functional units. A functional unit is made up of several blocks which together accomplish a specific goal. These blocks are 320um x 1800um. Each block may contain a 2 x 10 array of 80um pads on 160um centers. A block does not always contain all 20 pads since some test structures require a large area, however the pads which are present will remain on the 160um grid. The pad numbering convention is shown below. Pad #1 contains a small notch in it to help distinguish top from bottom when viewing the chip through a microscope. The entire EE290 chip is a 6 row, 30 column array of blocks.

1	11
2	12
3	13
4	14
5	15
6	16
7	17
8	18
9	19
10	20

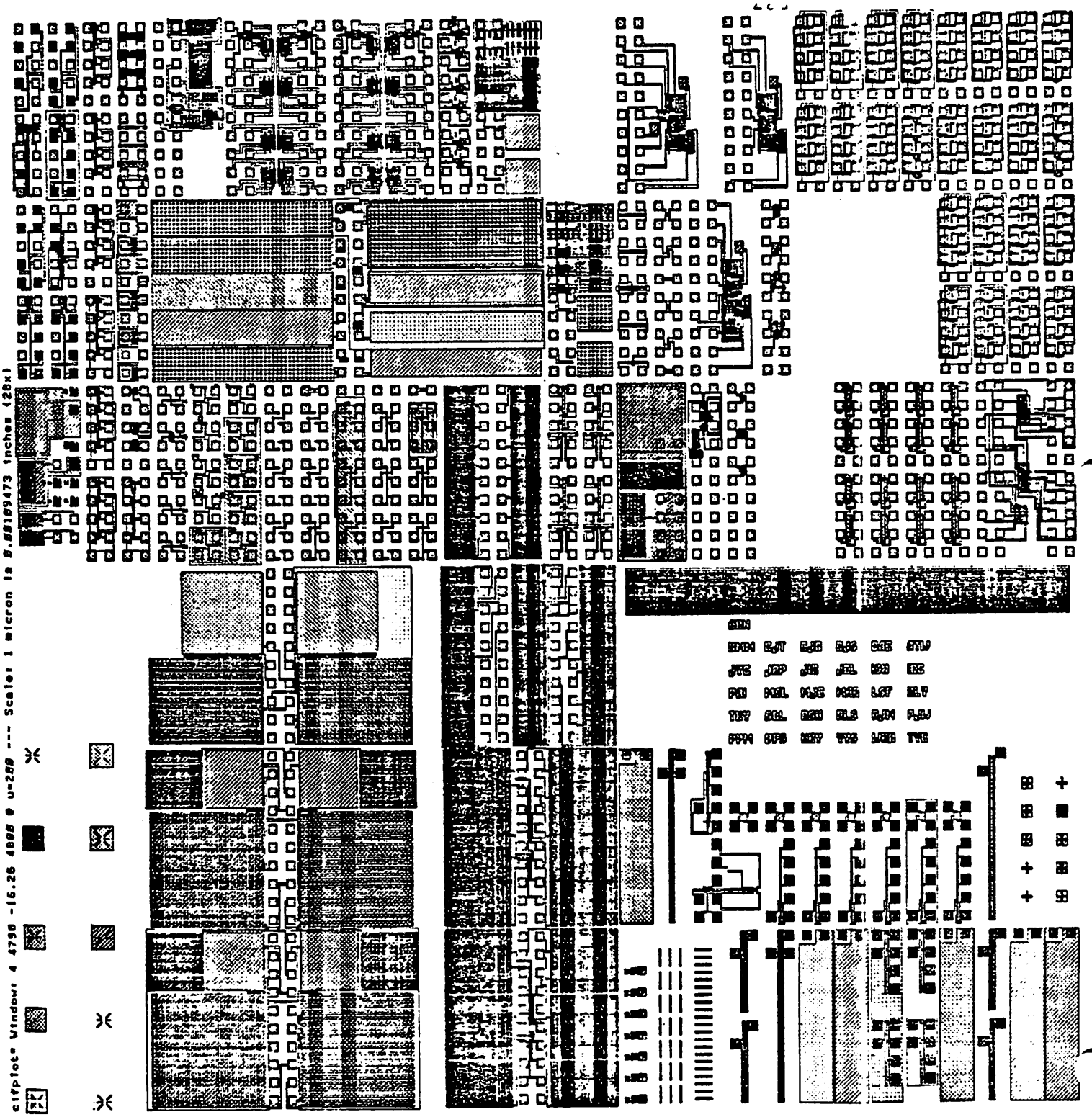
The testing of the devices can be accomplished with a 2 x 5 probe card. Some of the test patterns must be tested with a 2 x 10 probe card due to unconventional pad assignments and the inability to constrain the test structure to a 2 x 5 sub-block.

BERKELEY CMOS PROCESS TEST CHIP



testchip.cif

Entire EE290 Test Chip



BERKELEY CMOS PROCESS
PROCESS DROP-IN TEST PATTERN

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Bob Monteverde

(revised by)
Brian Childers
Steve Lester
Joseph Pierrat

UNIVERSITY OF CALIFORNIA
Department of Electrical Engineering
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Berkeley, California

REV 0.0
(Spring 1984)

Process Drop-In Test Pattern
Table of Contents

DISCUSSION

Process Drop-In Test Pattern

The process drop-in test chip (chip "a") consists of six 2 x 10 blocks. As the name suggests, the chip is intended to be "dropped in," or rather included, on every CMOS mask set to be processed in the electronics research laboratory. The benefits to such a test chip are three-fold. First, one can quickly determine many processing and electrical characteristics of a given lot because the test structures can be probed automatically. Secondly, due to the automatic testing capabilities, statistical sampling of various parameters both cross-wafer and cross-lot can be performed. Finally, and perhaps most importantly, a data base from which the quality of laboratory processing can be monitored constantly.

The process drop-in test structures and their purposes are:

Cross Bridge Structures for:	**Sheet Resistance & Line Width Bias Measurement for:	**polysilicon **p source/drain **n source/drain
Metal Meanders for:	**Sheet Res. & Linewidth Bias Meas. of metal	
Contact Chains for:	**Quick-check on continuity for:	**metal to poly contacts **metal to p-type source/drain **metal to n-type source/drain
Resistor Voltage Dividers for:	**Elec. Alignment Measurement for:	**metal to contact **contact to poly **contact to active **poly to active
Metal Comb Structure over poly/diffusion lines for:	**detecting metal short circuits	
Capacitors for:	**C-V and C-t measurements	

The capacitors include:

(a) poly/gate oxide/n-channel (p substrate)

(b) poly/gate oxide/p-channel (n well)

(c) poly/field oxide/n-channel

(d) metal/overglass-polyoxide/poly

All pad assignments except for the capacitor pads conform to the standard 2 x 5 pad assignment. The name and pad location of all the pads used appear in the detailed functional descriptions section in the Pad Configuration table. The capacitor probe pads are in pairs with the pad closest to each capacitor corresponding to the top electrode. Detailed documentation for each of the test structures is included in this report.

SUMMARY TABLE

Process Drop-In Test Pattern

Filename Sz-(Blks)	Structure	Purpose	Coordinates within 290n chip	Test Pat.	Func. Unit
ac1r2PACT 1/2	VD Pauw & Resistor	Sheet R, Line Width, (P-Src/Drn)	c1r2	c1r2	c1r2
ac1r1NACT 1/2	VD Pauw & Resistor	Sheet R, Line Width, (N-Src/Drn)	c1r1	c1r1	c1r1
ac0r2METL 1/2	Comb	Metal Shorts	c0r2	c0r2	c0r2
ac0r1POLY 1/2	VD Pauw & Resistor	Sheet R, Line Width, (Poly)	c0r1	c0r1	c0r1
ac0r2METL 1/2	Meander Resistor	Sheet R, Line Width, (Metal)	c0r2	c0r2	c0r2
ac1r1NACT 1/2	Voltage Divider	Align Poly>Actv	c1r1	c1r1	c1r1
ac1r2PACT 1/2	Voltage Divider	Align Cont>Actv	c1r2	c1r2	c1r2
ac0r1POLY 1/2	Voltage Divider	Align Cont>Poly	c0r1	c0r1	c0r1
ac0r2METL 1/2	Voltage Divider	Align Metal>Actv	c0r2	c0r2	c0r2
ac0r0CAP 3/5	Visuals	Process Monitors	c0r0	c0r0	c1r0
ac0r0CAP 2	Capacitors Al/BP-PolyOx/Poly Poly/Field/N-Well Poly/Gate/P-Chanl Poly/Gate/N-Chanl	Vfb, Vt Vbd, Nsub, Nss, Nit, Tox	c0r0 c0r0 c0r0 c0r0	c0r0 c0r0 c0r0 c0r0	c1r0 c1r0 c1r0 c1r0
ac0r1POLY 2 pads	Contact chain (Poly)	Contact Reliability	c0r1	c0r1	c0r1
ac1r1NACTI 2 pads	Contact chain (N-active)	Contact Reliability	c1r1	c1r1	c1r1
ac1r2PACTV 2 pads	Contact chain (P-active)	Contact Reliability	c1r2	c1r2	c1r2

FUNCTIONAL DESCRIPTION

Process Drop-in Test Pattern

Resistor Voltage Divider: Metl to Cont

Filename:

ac0r2METL (top 1/2)

Purpose:

Electrical Alignment Measurement

Description:

Two resistor voltage dividers, one for vertical alignment, one for horizontal alignment. Force current though resistors, horizontal alignment is perfect when voltage VTX is exactly half way between voltage V1 and V2, vertical alignment is perfect when voltage VTY is exactly half way between voltage V2 and V3.

Testing:

Two algorithms are possible. The best one is presently unknown. Both algorithms measure the difference in voltage between the two legs of a voltage divider.

Let,

Vn = the voltage across either leg when the alignment is perfect.

dV = the change in a legs voltage due to a misalignment.

Then, for the horizontal divider,

$$V1\text{-}VTX = Vn + dV$$
$$VTX\text{-}V2 = Vn - dV$$

and so,

$$dV = (1/2) * ((V1\text{-}VTX)-(VTX\text{-}V2))$$

The difference between the two algorithms is in how to compute the dX micron misalignment given the measured dV.

Note that,

$$(V1\text{-}VTX) = I * (Rs/w * (Lo + dL))$$
$$(VTX\text{-}V2) = I * (Rs/w * (Lo - dL))$$

so that,

$$dL = (w/Rsl) * dV \qquad \text{EQUATION 1}$$

where Rs = Sheet resistance of poly
w = resistor width
I = forced current
Lo = effective resistor length of either resistor leg when alignment is perfect.

However,

$$Vn = (RsLo/w) * I \quad \text{and so} \quad (w/Rsl) = Lo/Vn$$

so that,

$$dL = (Lo/Vn) * dV \qquad \text{EQUATION 2}$$

The test procedure is as follows:

1. Force current I+ = about 10 mA
2. Measure dV as described above.
3. Derive the ratio Rs/w from a separate test of the poly cross-bridge structure located in ac0r1POLY. Note that the nominal width of the poly resistor in ac0r1POLY is 20 um; the nominal width of the poly resistor in ac0r2METL is 15 um.
4. Knowing dV, Rs/w, and I, compute dX.

OR,

1. Force current I+ = about 10 mA.
2. Measure dV as described above.
3. Measure Vn.
   Vn = (V1-V2)/2 for horizontal.
   Vn = (V2-V3)/2 for vertical.
4. Knowing Lo, Vn, and dV, compute dX.
   Lo = 65 uM

The advantage of using equation 1 is that nothing is assumed: I and Rs/w are both measured. However, this may also be a disadvantage because it leads to more statistical error, especially since Rs/w is obtained from a different structure.

The advantage of using equation 2 is that the computation is entirely geometric and thus the exact value of Rs/w or I is not necessary. On the other

hand, the value of Lo is not know exactly because the "ends" of the resistor is not clearly defined. However any error is Lo is fixed and present only a scaling factor error. Furthermore, the Lo can be calibrated later by comparing electrical results with visual alignment structures such as verniers.

Mathematically, the two equations are identical; one can be derived from the other. The only difference is where the parameters are obtained.

Finally, due to unknown non-linearities and parasitic resistances, the calculated dX using either of the two procedures above may vary with the forcing current.

The accuracy of the dX measurement is better at higher test currents; however, too high of a current will alter the sheet resistivity (Eq. 2 is less sensitive to this effect since Rs is taken at that current) and eventually damage the structure. To optimize results, the test should be run at several different currents on the first few structures measured. The highest current which gives a consistent value of dX (per chip, not a consistent value of dX overall) should then be used of the remaining chips in the lot.

The structure is designed to resolve 0.1 uM misalignment. For the contact to poly structure at I = 10 mA, a .1 uM misalignment corresponds to dV = 1.67 mV centered of 2.16 volts.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	G	Ground
4	G	Ground
5	V3	Measure V
11	I+	Force I
12	V2	Measure V
13	VTX	Measure V
14	VTY	Measure V
15	V1	Measure V

Resistor Voltage Divider

Filename:

ac0r1POLY.cif (top 1/2)

Purpose:

Electrical Alignment Measurement

Description:

Two resistor voltage dividers, one for vertical alignment, one for horizontal alignment. Force current though resistors, horizontal alignment is perfect when voltage VTX is exactly half way between voltage V1 and V2, vertical alignment is perfect when voltage VTY is exactly half way between voltage V2 and V3.

Testing:

Two algorithms are possible. The best one is presently unknown. Both algorithms measure the difference in voltage between the two legs of a voltage divider.

Let Vn = the voltage across either leg when the alignment is perfect.

dV = the change in a legs voltage due to a misalignment.

Then, for the horizontal divider,

$$V1\text{-}VTX = Vn + dV$$
$$VTX\text{-}V2 = Vn - dV$$

and so,

$$dV = (1/2) * ((V1\text{-}VTX)-(VTX\text{-}V2))$$

The difference between the two algorithms is in how to compute the dX micron misalignment given the measured dV.

Note that,

$$(V1\text{-}VTX) = I * (Rs/w * (Lo + dL))$$
$$(VTX\text{-}V2) = I * (Rs/w * (Lo - dL))$$

so that,

$$dL = (w/Rsl) * dV \qquad \text{EQUATION 1}$$

where Rs = Sheet resistance of poly
w = resistor width
I = forced current

Lo = effective resistor length of
either resistor leg when
alignment is perfect.

However,

$$Vn = (RsLo/w) * I \quad \text{and so} \quad (w/Rsl) = Lo/Vn$$

so that,

$$dL = (Lo/Vn) * dV \qquad \text{EQUATION 2}$$

The test procedure is as follows:

1. Force current I+ = about 10 mA
2. Measure dV as described above.
3. Obtain the ratio Rs/w from a separate test of the cross-bridge structure located in the same block.
4. Knowing dV, Rs/w, and I, compute dX.

OR,

1. Force current I+ = about 10 mA.
2. Measure dV as described above.
3. Measure Vn.
   Vn = (V1-V2)/2 for horizontal.
   Vn = (V2-V3)/2 for vertical.
4. Knowing Lo, Vn, and dV, compute dX.
   Lo = ~70 uM

The advantage to using equation 1 is that nothing is assumed: I and Rs/w are both measured. However, this may also be a disadvantage because it leads to more statistical error, especially since Rs/w is obtained from a different structure.

The advantage to using equation 2 is that the computation is solely geometric and thus the exact value of Rs/w or I is not necessary. On the other hand, the value of Lo is not know exactly because the "ends" of the resistor is not clearly defined. However any error is Lo is fixed and present only a scaling factor error. Furthermore, the Lo can be calibrated later by comparing electrical results with visual alignment structures such as verniers.

Mathematically, the two equations are identical; one can be derived from the other. The only difference is where the parameters are obtained.

Finally, due to unknown non-linearities and parasitic resistances, the calculated dX using either of the two procedures above may vary with the forcing current.

The accuracy of the dX measurement is better at higher test currents; however, too high of a current will alter the sheet resistivity (Eq. 2 is less sensitive

to this effect since Rs is taken at that current) and eventually damage the structure. To optimize results, the test should be run at several different currents on the first few structures measured. The highest current which gives a consistent value of dX (per chip, not a consistent value of dX overall) should then be used of the remaining chips in the lot.

The structure is designed to resolve 0.1 uM misalignment. For the contact to poly structure at I = 10 mA, a .1 uM misalignment corresponds to dV = 1.25 mV centered of 1.75 volts.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	G	Ground
4	G	Ground
5	V3	Measure V
11	I+	Force I
12	V2	Measure V
13	VTX	Measure V
14	VTY	Measure V
15	V1	Measure V

Resistor Voltage Divider

Filename:

ac1r1NACTV (top 1/2)

Purpose:

Electrical Alignment Measurement

Description:

Two resistor voltage dividers, one for vertical alignment, one for horizontal alignment. Force current though resistors, horizontal alignment is perfect when voltage VTX is exactly half way between voltage V1 and V2, vertical alignment is perfect when voltage VTY is exactly half way between voltage V2 and V3.

Testing:

The position of a poly line changes the width, and thus the resistance, of two parallel diffusion resistors.

Let Vn = the voltage across either leg when the alignment is perfect.

dV = the change in a legs voltage due to a misalignment.

Then, for the horizontal divider,

$$V2\text{-}VTX = Vn + dV$$
$$VTX\text{-}V3 = Vn - dV$$

and so

$$dV = (1/2) * ((V2\text{-}VTX)\text{-}(VTX\text{-}V3))$$

For the vertical divider,

$$dV = (1/2) * ((V1\text{-}VTY)\text{-}(VTY\text{-}V3))$$

Note that,

$$(V2\text{-}VTX) = I * (R1 + Rp + Rp')$$
$$(VTX\text{-}V3) = I * (R2 + Rp + Rp')$$

(Rp, Rp' = Parasitic Resistances)

Where,

$$R1 = Rs * (L / Wo + dW)$$
$$R2 = Rs * (L / Wo - dW)$$

Solving:

$$dW = -(Wo^{**}2 / I * Rs * L) * dV$$

Rs = Sheet resistance of the material
I = forced current
L = resistor length
Wo = Nominal resistor width
dW = How much wider R1 gets, can be pos. or neg.

For our sign convention: dW = -dX

$$dX = (Wo^{**}2 / I * Rs * L) * dV$$

Wo, the nominal width of the diffusion resistor along L, needs to be calculated.

$$V2 - V3 = I * (2Rp + 2Rp' + R1 + R2)$$

Where,

$$R1 + R2 = Rs * L * (2/Wo)$$

$$Rp = Rs * Ns$$
$$Rp' = Rs * Ns'$$

(Ns, Ns'= Number of Squares)

Let Vn = (V2 - V3) / 2 be the nominal voltage drop.

Although we do not know Ns or Ns' very accurately, Rp and Rp' are small compared to R1 and R2, so a rough guess of Ns and Ns' should do.

$$Ns \sim 3, \quad Ns' \sim 1$$

Solving and Plugging in:

$$Wo = L / ((Vn / (Rs * I)) - 4)$$

The 4 is correction factor = Ns + Ns'

Finally,

$$dX = (L / ((((Vn / (Rs * I)) - 4)^{**}2) * Rs * I)) * dV$$

So the test procedure is as follows:

1. Force Voltage V = -0.5 volts to poly
2. Force current I+ = about 1 mA.
3. Measure dV as described above.
4. Measure Vn.
   Vn = (V2-V3)/2 for horizontal.

Vn = (V1-V2)/2 for vertical.

5. Obtain Rs for NACTV from cross-bridge structure.
6. Knowing L, Rs, Vn, and dV, compute dX.
   L = 120 um

The accuracy of the dX measurement is better at higher test currents; however, too high of a current will alter the sheet resistivity (Eq. 2 is less sensative to this effect since Rs is taken at that current) and eventually damage the structure. To optimize results, the test should be run at several different currents on the first few structures measured. The highest current which gives a consistent value of dX (per chip, not a consistent value of dX overall) should then be used of the remaining chips in the lot.

The structure is designed to resolve 0.1 um misalignments For the poly to active structure at I = 1 mA, a .1 um misalignment corresponds to a dV ~ 24 mV centered of 1.4 volts (Rs = 50 ohms/sq.).

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	G	Ground
3	Fv	(Force Voltage to Poly)
4	G	Ground
5	V3	Measure V
11	VTX	Measure V
12	V2	Measure V
13	VTY	Measure V
14	I+	Force I
15	V1	Measure V

Resistor Voltage Divider

Filename:

ac1r2PACTV

Purpose:

Electrical Alignment Measurement

Description:

Two resistor voltage dividers, one for vertical alignment, one for horizontal alignment. Force current though resistors, horizontal alignment is perfect when voltage VTX is exactly half way between voltage V1 and V2, vertical alignment is perfect when voltage VTY is exactly half way between voltage V2 and V3.

Testing:

Two algorithms are possible. The best one is presently unknown. Both algorithms measure the difference in voltage between the two legs of a voltage divider.

Let Vn = the voltage across either leg when the alignment is perfect.

dV = the change in a legs voltage due to a misalignment.

Then, for the horizontal divider,

$$V1\text{-}VTX = Vn + dV$$
$$VTX\text{-}V2 = Vn - dV$$

and so,

$$dV = (1/2) * ((V1\text{-}VTX)-(VTX\text{-}V2))$$

The difference between the two algorithms is in how to compute the dX micron misalignment given the measured dV.

Note that,

$$(V1\text{-}VTX) = I * (Rs/w * (Lo + dL))$$
$$(VTX\text{-}V2) = I * (Rs/w * (Lo - dL))$$

so that,

$$dL = (w/RsI) * dV \qquad \text{EQUATION 1}$$

where Rs = Sheet resistance of the active region
w = resistor width
I = forced current
Lo = effective resistor length of

either resistor leg when
alignment is perfect.

However,

$$Vn = (RsLo/w) * I \quad \text{and so} \quad (w/RsI) = Lo/Vn$$

so that,

$$dL = (Lo/Vn) * dV \qquad \text{EQUATION 2}$$

The test procedure is as follows:

1. Force current I+ = about 10 mA
2. Measure dV as described above.
3. Obtain the ratio Rs/w from a separate test of the cross-bridge structure located in the same block.
4. Knowing dV, Rs/w, and I, compute dX.

OR,

1. Force current I+ = about 10 mA.
2. Measure dV as described above.
3. Measure Vn.
   Vn = (V1-V2)/2 for horizontal.
   Vn = (V2-V3)/2 for vertical.
4. Obtain Lo from layout.
5. Knowing Lo, Vn, and dV, compute dX.

The advantage to using equation 1 is that nothing is assumed: I and Rs/w are both measured. However, this may also be a disadvantage because it leads to more statistical error, especially since Rs/w is obtained from a different structure.

The advantage of using equation 2 is that the computation is entirely geometric and thus the exact value of Rs/w or I is not necessary. On the other hand, the value of Lo is not know exactly because the "ends" of the resistor is not clearly defined. However any error is Lo is fixed and present only a scaling factor error. Furthermore, the Lo can be calibrated later by comparing electrical results with visual alignment structures such as verniers.

Mathematically, the two equations are identical; one can be derived from the other. The only difference is where the parameters are obtained.

Finally, due to unknown non-linearities and parasitic resistances, the calculated dX using either of the two procedures above may vary with the forcing current.

The accuracy of the dX measurement is better at higher test currents; however, too high of a current will alter the sheet resistivity (Eq. 2 is less sensative to this effect since Rs is taken at that current) and eventually damage the structure. To optimize results, the test should be run at several different currents on

the first few structures measured. The highest current which gives a consistent value of dX (per chip, not a consistent value of dX overall) should then be used of the remaining chips in the lot.

The structure is designed to resolve 0.1 uM misalignment For the contact to active structure at I = 10 mA, a .1 um misalignment corresponds to dV = 2.5 mV centered of 3.5 volts (Rs=50 ohms/sq.)

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	G	Ground
4	G	Ground
5	V3	Measure V
11	I+	Force I
12	V2	Measure V
13	VTX	Measure V
14	VTY	Measure V
15	V1	Measure V

Cross Bridge

Filename:

ac0r1POLY, ac1r1NACTI, ac1r2PACTV

Purpose:

Electrical Sheet Resistance and Linewidth Measurement

Description:

This structure is a Van der Pauw cross followed with a straight resistor. Both carry the same current. The sheet resistance is determined from the Van der Pauw cross; using this information, the linewidth of the straight resistor is determined.

Testing:

Sheet Resistance:

The equation for the Van der Pauw cross is,

$$Rs = ((V1 - V2) / I) * (pi / \ln 2)$$

$$(pi / \ln 2) \sim 4.53$$

The minimum resolution of the test equipment is 1 mV. If we choose this to correspond to a 5% change in Rs, we can guess at Rs and determine the proper current to use to test.

Material	Rs (est.)	Test Current
Poly	25	4 mA
Active	50	2 mA

Linewidth

The linewidth equation,

$$W = (I * Rs * L) / (VA - VB)$$

The test procedure is as follows:

1. Force current I+ = 2-4 mA.
2. Measure V1, V2.
3. Compute Rs from I, V1, V2.
4. Measure VA, VB.

5. Compute W from I, L, Rs, VA, VB.
   L = 160 um

   Note: Contact chains will be tested at the same time.

The currents suggested will give a resolution of Rs/20 for the sheet resistance measurement. The same currents will produce linewidth resolution of 0.025 um.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
7	G	Ground
9	G	Ground
10	V2	Measure V
17	VB	Measure V
18	VA	Measure V
19	I+	Force I
20	V1	Measure V

Note, pin 16 here is a current source for a contact chain. See contact chain documentation for a description.

Meander Resistors

Filename:

ac0r2METL

Purpose:

Electrical Sheet Resistance and Linewidth Measurement for Metal

Description:

This structure consists of two long meandering metal resistor; one is 9 microns wide and the other is 3 microns wide. Both are the same length. carry the same current. By comparing the voltage drops across the resistors, the linewidth bias and sheet resistance can be determined.

Testing:

There are two resistors, R and R',

$$R = (Rs * L) / (Wo + dW) = (V2 - V3) / I = V / I$$
$$R' = (Rs * L) / (Wo' + dW) = (V1 - V2) / I = V' / I$$

These are two equations in the two unknowns, dW and Rs.

$$dW = \frac{Wo'(R'/R) - Wo}{1 - (R'/R)}$$

$$Rs = R * ((Wo + dw) / L)$$

The test procedure is as follows:

1. Force current I+ = 1-5 mA.
2. Measure V1, V2, V3.
3. Compute dW from I, L, Wo, Wo', V1, V2, V3.
4. Compute Rs from I, L, V, Wo, dW.

Wo = 9.0 um
Wo' = 3.0 um
L = 1545um

Note: Metal Comb will be tested at the same time.

The currents suggested will give a resolution of about .1-.2 um for the line width measurement. The resolution of the sheet resistance measurement will be about .05-.1 ohms/sq.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
7	G	Ground
10	V3	Measure V
17	I+	Force I
18	V1	Measure V
20	V2	Measure V

Note, pin 18 here is a voltage source for a metal comb. See comb documentation for a description.

Contact Chains

Filename:

ac0r1POLY, ac1r1NACTI, ac1r2PACTV (bottom 1/2's)

Purpose:

Electrical Sheet Resistance and Linewidth Measurement

Description:

These structures consist of sixteen contacts between the levels indicated.

Testing:

Force a current; the sense voltage should be less than 5 volts.

The test procedure is as follows:

1. Force current I+ = 1 mA.
2. Measure V.

This structure is not intended to give statistical information. Rather, it is a check to make sure nothing is drastically wrong with the process.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
7	G	Ground
16	I/V	Force I/Measure V

Metal Comb

Filename:

ac0r2METL (bottom 1/2)

Purpose:

To check for electrical shorts

Description:

This structure consists of two interlocking but not connected metal patterns. The metal lines run over poly and field oxide steps at right angles.

Testing:

Force several different voltages. The current should be always zero. The test procedure is then to force voltage V= 1, 2, 3, 4, 5, and measure the resulting currents.

This structure is not intended to give statistical information. Rather, it is a check to see if any- thing is drastically wrong with the process.

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
7	G	Ground
16	V/I	Force I/Measure V

Visual Photolithography and Etch Monitors

Filename:

acOr0CAP

Purpose:

To indicate correct linewidth of photoresist lines or openings and etched lines or openings in different films.

Description:

Width to space, 4um/4um, 3/3, 2/2, 1/1, 3 lines and two spaces for each other at 6 um.

Type	Designation	Pad Location
NWELL	N	17
ACTIVE	A	16
POLY	P	15
PPII	I	14
CONTACT	C	13
METAL	M	12
PAD	O	11

Testing:

Visual inspection.

Pad Assignment:

Non Electrical Test

Flat Plate Capacitors

Filename:

ac0r0CAP

Purpose:

To measure the following data:

Nsub	substrate doping concentration at surface
Nwell	nwell doping concentration profile
Nss	fixed oxide charge
Nit	interface charge
Tox	gate oxide thickness
Fox	field oxide thickness

and thus derive Vfb, the flatband voltage, and Cox', the capacitance per unit area.

Description:

Four types of capacitors are included on this unit. They are:

1) poly/gate/n-channel
2) poly/gate/p-channel
3) poly/field/n-channel
4) met/BP-polyox/poly

Testing:

For Nit:

Do C-t measurement

For Nsub, Nnwell, Nss, Tox:

Do high frequency C-V measurement

For Tox:

Cox' = Cmax'

For Nsub, Nnwell:

$1/Cmin' = 1/Cox' + 1/Cd'$

$Cd' = \text{epsilon si}/xd$

$xd = \text{sqrt}\{[2*\text{epsilon si}*2\text{phi}]/qNsub\}$

$Nsub/ni = \exp(q\text{phi}/kT)$

Procedure:

Measure Cmin' and Cmax', solve for Cd'. Then solve the two previous equations iteratively such that xd satisfies the expression for Cd'.

For Vfb:

When V is equal to the Flat Band Voltage we have,

Cfb' = Cox'Cdo'/Cox'+Cdo'

Where,

Cdo' = epsilon si/Ld
Ld = sqrt{[2 *(epsilon si)* kT]/q^2 * Nsub}

Solve for Cdo', calculate Cfb' and determine Vfb from C-V Plot.

For Nss, NI2:

Vfb = phiMS(-qNss/Cox' + NI2/Cox')

To distinguish between Nss and NI2 charge, do several capacitors with different Vt implants each time. Then plot Ni2 vs. Vfb. The NI2 axis intercept is given by,

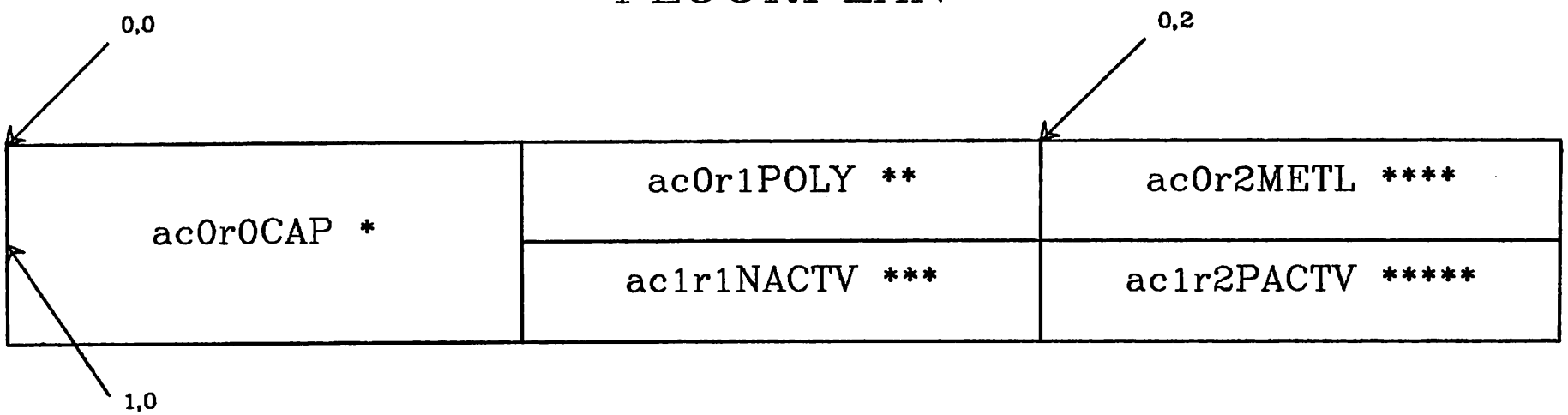
Y = qNss - phiMS Cox'

Nss = (Y + phiMS Cox')/q

Pad Assignment:

PAD NUMBER	NAME	FUNCTION
2	P1	top plate met/BP-polyox/poly cap
5	P1	top plate poly/fieldox/n-channel cap
8	P1	gate poly/gate/n-channel cap
9	P1	gate poly/gate/p-channel cap
12	P2	bottom plate met/BP-polyox/poly cap
15	P2	bottom plate poly/fieldox/n-channel cap
18	P2	bottom plate poly/gate/n-channel cap
19	P2	bottom plate poly/gate/p-channel cap

PROCESS DROP-IN TEST PATTERN
FLOORPLAN



* Capacitors and Visuals

** Van Der Pauw, Voltage Divider, Contact Chain, Resistor

*** Van Der Pauw, Voltage Divider, Contact Chain, Resistors

**** Comb, Meander Resistor, Voltage Divider

***** Van Der Pauw, Resistor, Voltage Divider, Contact Chain

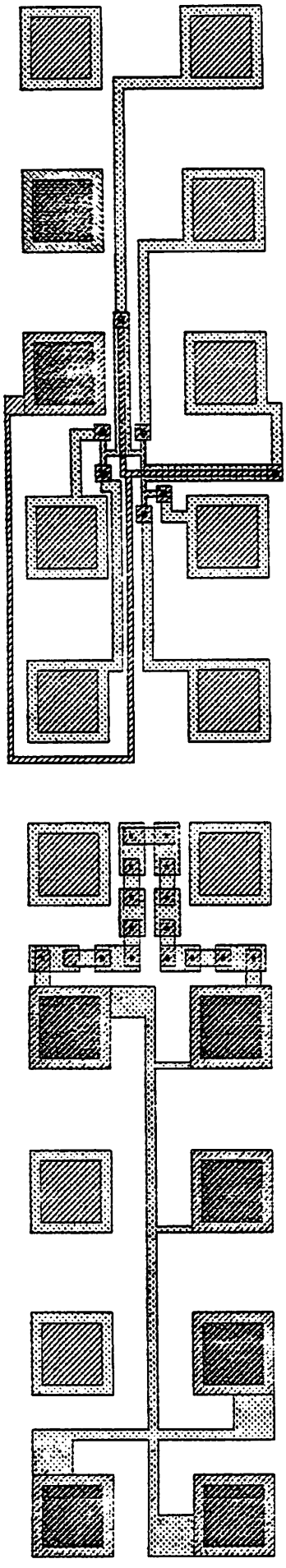
a subchip

Process drop-in

ac0r0CAP.cif

capacitors

visuals



ac1r1NACTV.cif

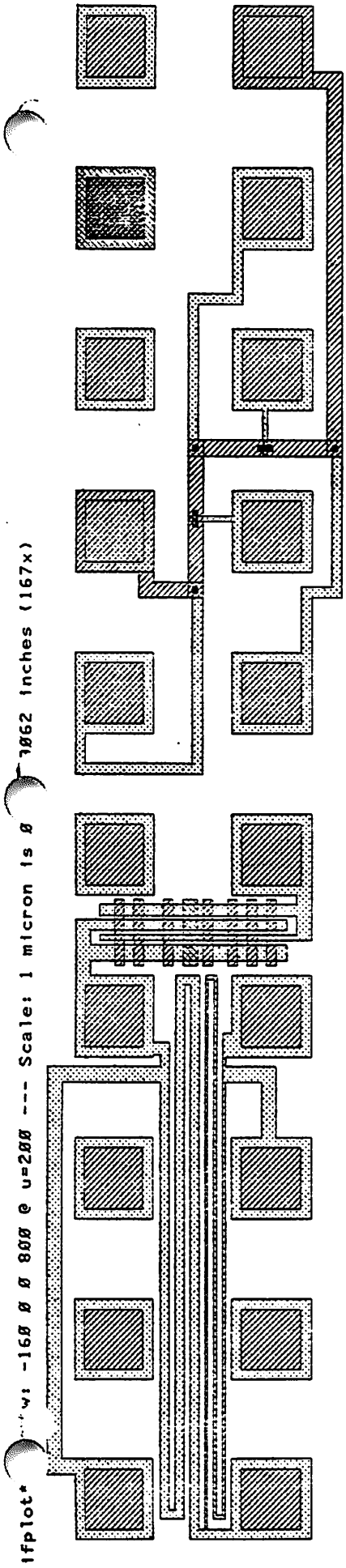
voltage divider

contact chain

Van Der Pauw & resistor

ac1r1NACTV.cif

ac1r1NACTV.cif



ac0r2METL.cif

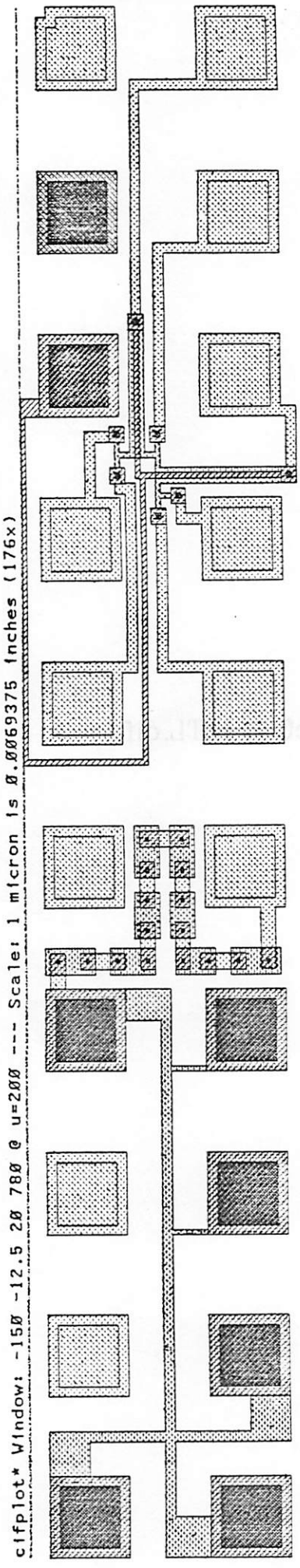
voltage divider

comb

meander resistor

ac0r2METL.cif

ac0r2METL.cif

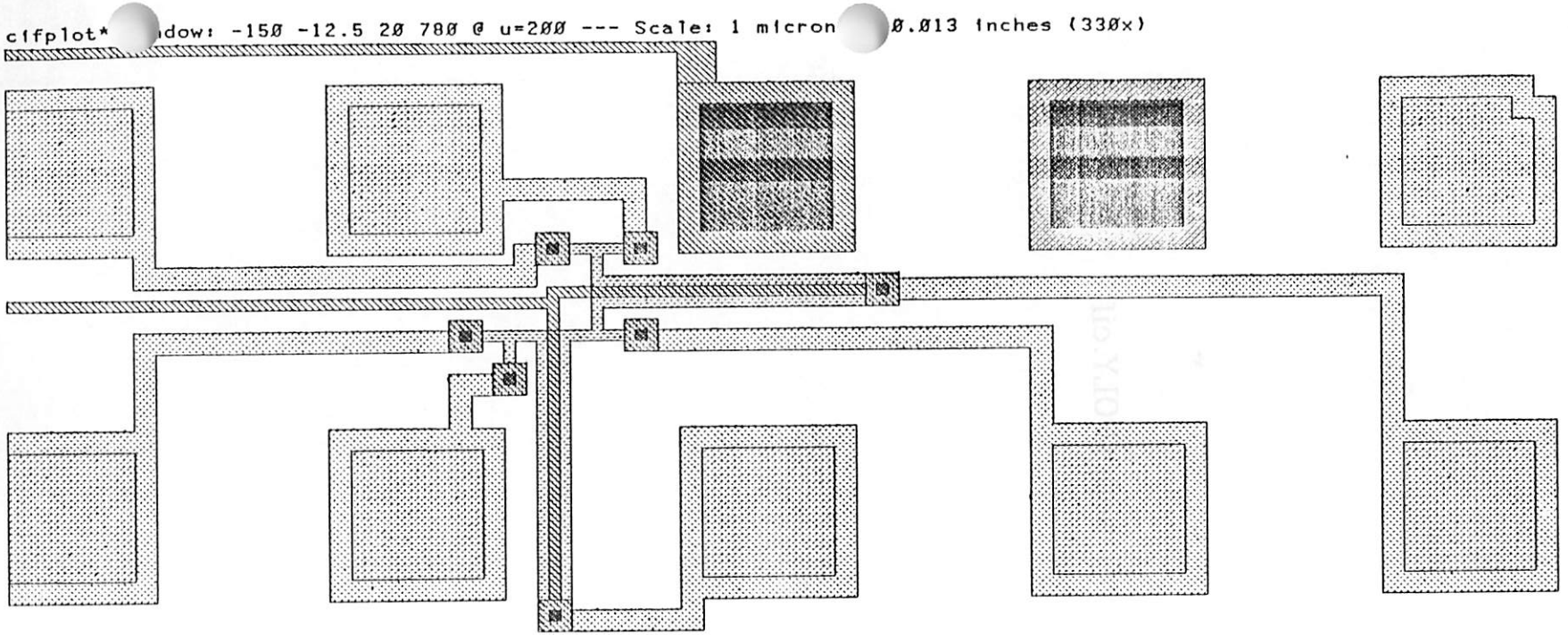


ac0r1POLY.cif

voltage divider

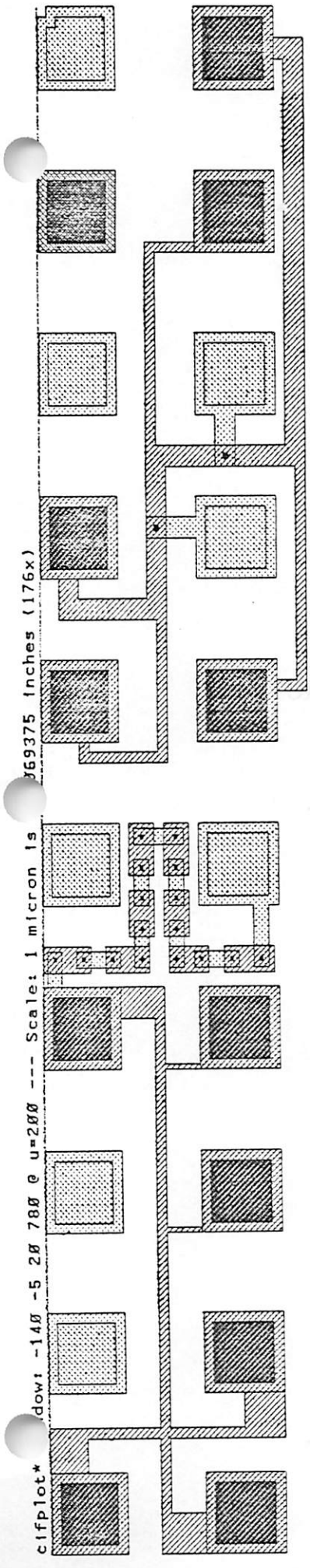
contact chain

Van Der Pauw & resistor



ac0r1POLY.cif

ac0r1POLY.cif



ac1r2PACTV.cif

voltage divider

Van Der Pauw & resistor

ac1r2PACTV.cif

ac1r2PACTV.cif

Process Drop-In Test Pattern (asubchip)
Cif File Cell Hierarchy

PAD.k

PADSET.k
  PAD.k

VISUAL.k

acOrOCAP.k
  PAD.k VISUAL.k visa.k viscont.k
  vismetl.k vispad.k vispoly.k

acOr1POLY.k
  PADSET.k contchainpol.k

acOr2METL.k
  PADSET.k

ac1r1NACTV.k
  PADSET.k

ac1r2PACTV.k
  PADSET.k contchain.k

asubchip.k
  acOrOCAP.k acOr1POLY.k acOr2METL.k
  ac1r1NACTV.k ac1r2PACTV.k

contchain.k

contchainpol.k

visa.k

viscont.k

vismetl.k

vispad.k

vispoly.k

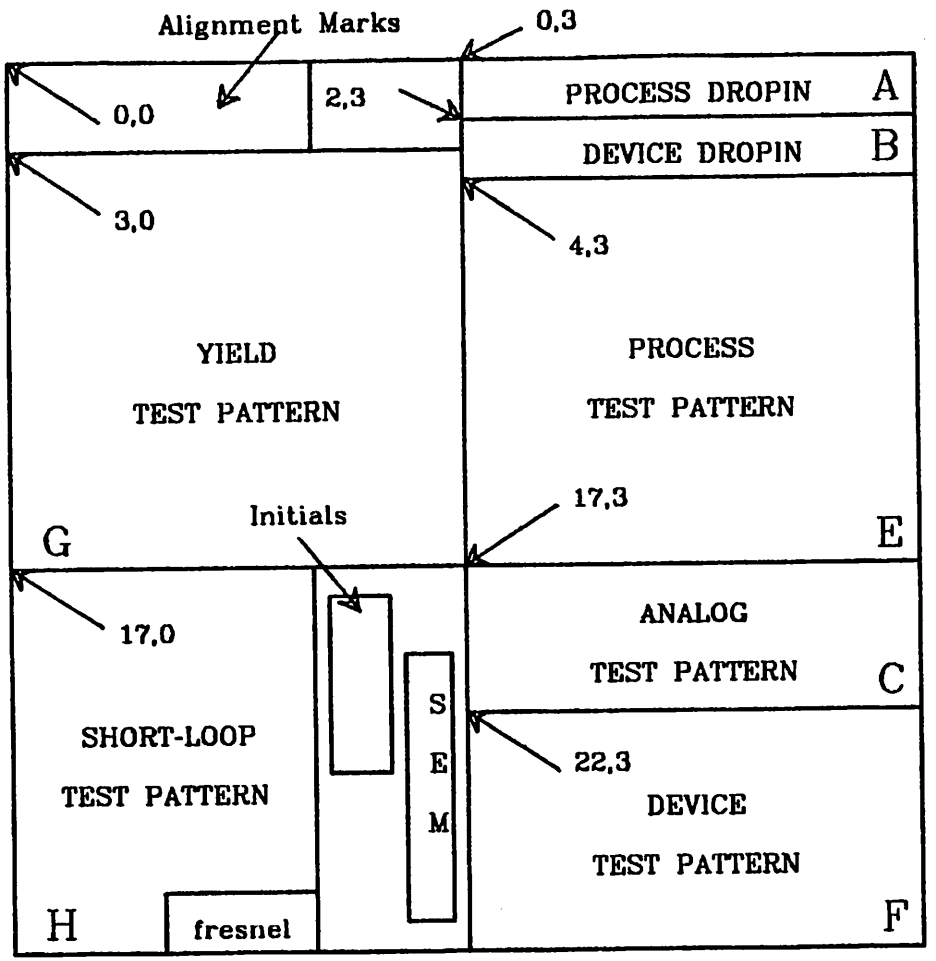
EE290 TEST CHIP ORGANIZATION

The EE290 test chip is made up of 7 Test Patterns plus a separate section for alignment marks. The 7 Test Patterns are: Device, Device Drop-in, Process, Process Drop-in, Shortloop, Yield, and Analog. Each test pattern consists of a collection of functional units. A functional unit is made up of several blocks which together accomplish a specific goal. These blocks are 320um x 1800um. Each block may contain a 2 x 10 array of 80um pads on 160um centers. A block does not always contain all 20 pads since some test structures require a large area, however the pads which are present will remain on the 160um grid. The pad numbering convention is shown below. Pad #1 contains a small notch in it to help distinguish top from bottom when viewing the chip through a microscope. The entire EE290 chip is a 6 row, 30 column array of blocks.

1	11
2	12
3	13
4	14
5	15
6	16
7	17
8	18
9	19
10	20

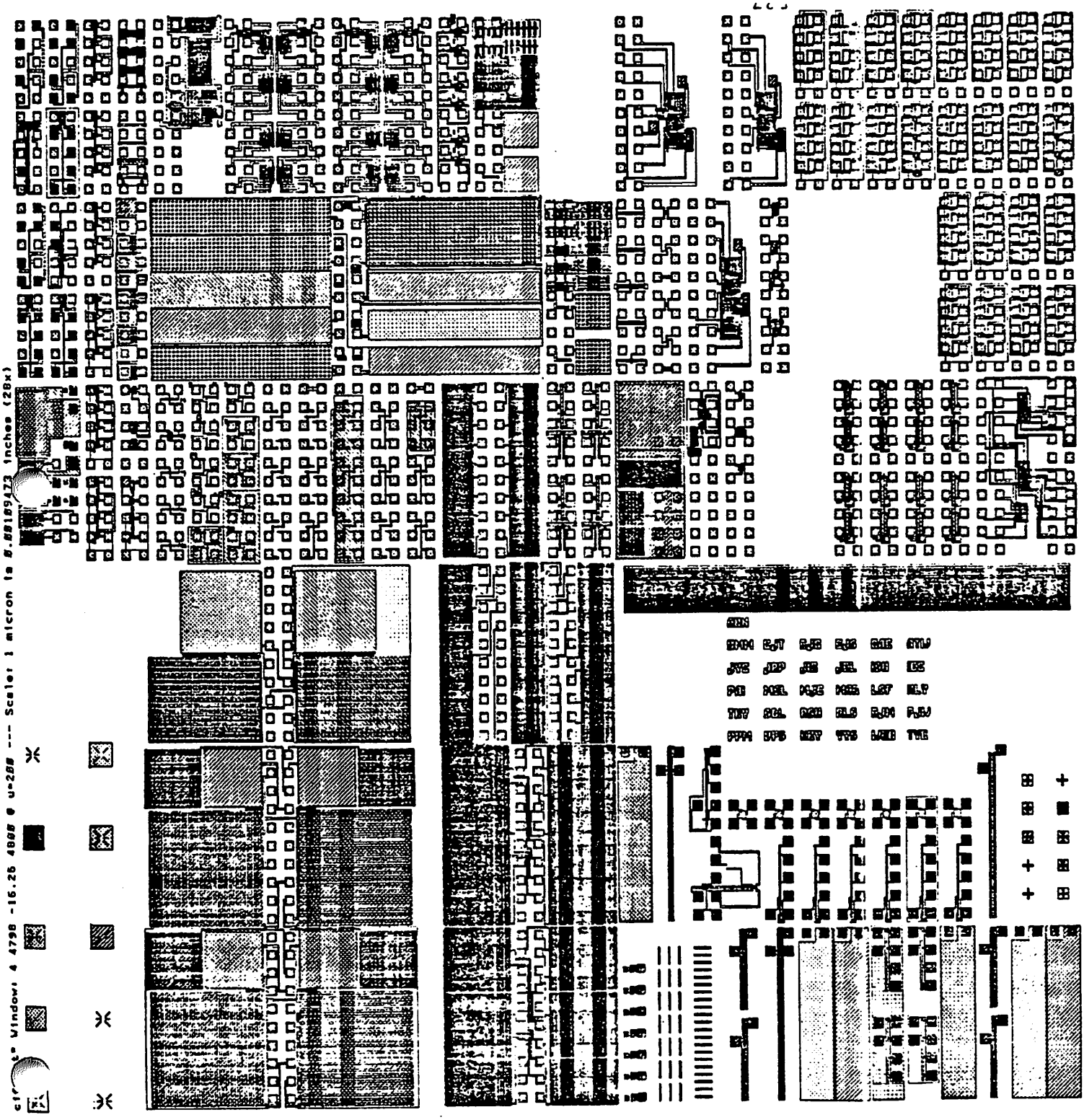
The testing of the devices can be accomplished with a 2 x 5 probe card. Some of the test patterns must be tested with a 2 x 10 probe card due to unconventional pad assignments and the inability to constrain the test structure to a 2 x 5 sub-block.

BERKELEY CMOS PROCESS TEST CHIP



testchip.cif

Entire EE290 Test Chip



BERKELEY CMOS PROCESS
DEVICE DROP-IN TEST PATTERN

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REV 0.0
(Spring 1984)

Device Drop-In Test Pattern
Table of Contents

DISCUSSION

Device Drop-In Test Pattern

Introduction

The goal of this project is to provide a minimum set of devices that can be used to extract the parameters needed for for circuit simulation.

The main consideration was given, naturally, to the MOS transistors but other types of devices such as bipolar transistors were also considered since some designs can use them. We focused our efforts to obtain the characteristics from a circuit point of view not from reliability (i.e. Latch-up) or other considerations.

Parasitics are tested for their effect on circuit performance. The parasitics considered are diffusion and poly resistances, diffusion, poly and metal capacitances and contact resistance. Some resistors (such as the N-well) can be used as circuit elements.

MOS Transistor Matrix

bc0r0bpmos1 bc0r0apmos2 bc0r1bpmos3
bc0r1anmos1 bc0r2bnmos2 bc0r2anmos3

The main purpose of the device drop-in chip is to characterize MOS transistors and therefore half of the total area is dedicated to this purpose. However, the total number of transistors is limited by the number of pads available to a total of 24, that were organized according to the following table:

Z and L in units of lambda = 1.2 microns

		Z			
		2	4	16	32
L	1	X	X	X	X
	2	X		X	
	4	X		X	
	16	X	X	X	X

This table contains 12 devices which are implemented both as N channel and P channel giving a total of 24. There are two complete columns (Z= 2 and 16) and two complete rows (L= 1,16). This is done to facilitate the extraction of parameters such as electrical length, source and drain resistance or mobility. The first row also characterizes the minimum gate length devices which will be preferred when trying to achieve maximum speed while the first column characterizes minimum width devices which draw the least power. The row and column at 16 is to provide a set of measurements in which we can assume that one of the two parameters of this matrix (Z,L) is sufficiently large to not consider short channel or narrow channel effects.

Field Threshold Devices

bc1r0bfield

This subblock is intended to measure field threshold. It contains two n-channel and two p-channel devices (poly-gate and Al-gate). Device size is 16x16 Lambda (Lambda = 1.2 microns).

SUMMARY TABLE

Device Drop-In Test Pattern

Filename Sz-(Blks)	Structure Z/L (lambda)	Coordinates within 290n chip	Test Pat.	Func. Unit
PMOS TRANSISTORS				
bc0r0bpmos1 1/2	2/16 2/4 2/2 2/1	c0r3	c0r0	c0r0
bc0r0apmos2 1/2	16/16 16/4 16/2 16/1	c0r3	c0r0	c0r0
bc0r1bpmos3 1/2	32/16 32/1 4/16 4/1	c0r4	c0r1	c0r1
NMOS TRANSISTORS				
bc0r1anmos1 1/2	2/16 2/4 2/2 2/1	c0r4	c0r1	c0r1
bc0r2bnmos2 1/2	16/16 16/4 16/2 16/1	c0r5	c0r2	c0r2
bc0r2nnmos3 1/2	32/16 32/1 4/16 4/1	c0r5	c0r2	c0r2
MOS FIELD & BIPOLAR TRANSISTORS				
bc1r0bfield 1/2	16/16 NMOS & PMOS poly & Al gate	c1r3	c1r0	c1r0
bc1r0abipolar 1/2	n+/p/nw nw/p/nw p+/nw/p	c1r3	c1r0	c1r0

SUMMARY TABLE
Device Drop-In Test Pattern

Filename Sz-(Blks)	Structure	Purpose	Coordinates within 290n chip	Test Pat.	Func. Unit
CAPACITORS					
bc1r1cap	P-region capacitor (a) poly/gate (b) N+/P (c) N+/P	Cox, Cj, & field (area) (perimeter)			
	N-region capacitor (a) poly/gate (b) P+/N (c) P+/N	Cox, Cj & field (area) (perimeter)	c1r4	c1r1	c1r1
1	Field (a) poly (b) poly (c) metal (d) metal	 (area) (perimeter) (area) (perimeter)			
RESISTORS & CONTACTS					
bc1r2bres 1/2	Resistors (a) N-Well (b) N+ poly (c) P+ poly (d) P+	Rs	c1r5	c1r2	c1r2
bc1r2acont 1/2	Contacts (a) N+ (b) Metal/poly (c) Metal/P+ (d) Metal/N+	Rs Rs contact resistance	c1r5	c1r2	c1r2

FUNCTIONAL DESCRIPTION

Device Dropin Test Pattern

MOS Transistor Matrix

Filename:

bc0r0bpmos1, bc0r0apmos2, bc0r1bpmos3
bc0r1anmos1, bc0r2bnmos2, bc0r2anmos3

Purpose:

The MOS transistor array will be used to characterize the electrical performance of the MOS devices.

Pad Assignment:

bc0r0bpmos1 (P-Channel Transistors)

W/L	PAD NUMBER				
	G	S	D	B	SUB
2/16	6	8	16	9	7
2/4	6	8	17	9	7
2/2	6	8	18	9	7
2/1	6	8	19	9	7

bc0r0apmos2 (P-Channel Transistors)

W/L	PAD NUMBER				
	G	S	D	B	SUB
16/16	1	3	11	4	2
16/4	1	3	12	4	2
16/2	1	3	13	4	2
16/1	1	3	14	4	2

bc0r1bpmos3 (P-Channel Transistors)

W/L	PAD NUMBER				
	G	S	D	B	SUB
32/16	6	8	16	9	7
32/1	6	8	17	9	7
4/16	6	8	18	9	7
4/1	6	8	19	9	7

bc0r1anmos1 (N-Channel Transistors)

W/L	PAD NUMBER				
	G	S	D	B	SUB
2/16	1	3	11	4	2
2/4	1	3	12	4	2
2/2	1	3	13	4	2
2/1	1	3	14	4	2

bc0r2bnmos2 (N-Channel Transistors)

W/L	PAD NUMBER				
	G	S	D	B	SUB
16/16	6	8	16	9	7
16/4	6	8	17	9	7
16/2	6	8	18	9	7
16/1	6	8	19	9	7

bc0r2anmos3 (N-Channel Transistors)

W/L	PAD NUMBER				
	G	S	D	B	SUB
32/16	1	3	11	4	2
32/1	1	3	12	4	2
4/16	1	3	13	4	2
4/1	1	3	14	4	2

Field Threshold Devices

Filename:

bc1r0bfield

Purpose:

To measure the field threshold.

Description:

This subblock is intended to measure field threshold. It contains two n-channel and two p-channel devices (poly-gate and Al-gate). Device size is 16x16 Lambda (Lambda = 1.2 microns).

Pad Assignment:

TYPE OF GATE	W/L	PAD NUMBER				
		G	S	D	B	SUB
Poly	16/16 NMOS	6	8	16	9	7
Al	16/16 NMOS	6	8	17	9	7
Poly	16/16 PMOS	6	8	18	9	7
Al	16/16 PMOS	6	8	19	9	7

Bipolar Devices

Filename:

bc1r0abipolar

Purpose:

To characterize the electrical performance of the bipolar transistors which may be used in circuit designs.

Description:

This subblock contains two npn and one pnp transistors. These are not intended to characterize undesirable parasitics, but rather devices which may be utilized in a circuit. They consist of one vertical pnp device and two lateral npn devices. The lateral devices were designed with minimum base width as determined by the appropriate design rule:

T1 : npn n+/p/n-well (Swp+ = 2.5 Lambda)

T2 : " n-well/p/n-well (Sww = 4.5 Lambda)

T3 : pnp p+/n-well/p

Pad Assignment:

Bipolar	PAD NUMBER		
	E	B	C
n+/p/nw	3	11	13
nw/p/nw	4	11	14
p+/nw/p	1	12	11

Capacitors

Filename:

bc1r1cap

Purpose:

Capacitors have been included in the drop-in to provide a way of measuring oxide thickness and flat band voltage. They also provide information to estimate delays due to parasitics.

Description:

There are a total of 10 capacitors which include 'area' and 'perimeter' capacitors arranged as follows:

P-Region

cap1 :	poly to active p-region	(area)
cap2 :	n+ diff to p-region/sub.	(area)
cap3 :	n+ diff to p-region/sub.	(perimeter)

N-Region (Well)

cap4 :	poly to active n-region	(area)
cap5 :	p+ diff to n-region/well	(area)
cap6 :	p+ diff to n-region/well	(perimeter)

Field
(over p-region only)

cap7 :	poly over thick ox	(area)
cap8 :	poly over thick ox	(perimeter)
cap9 :	metal over glass	(area)
cap10:	metal over glass	(perimeter)

Area capacitors are rectangles which have dimensions 180x140 = 25200 sq. microns with a perimeter of 640 microns. Perimeter capacitors are fin-shaped to increase the perimeter and have an area of 19300 sq. microns and a perimeter of 990 microns. They are intended to provide an estimate of edge capacitance.

Pad Assignment:

Structure	PAD NUMBER	
	Plate 1	Plate 2
P-Region		
poly/gate	1	11
N+/P	2	12
N+/P	3	13
N-Region		
poly/gate	4	14
P+/N	5	15
P+/N	6	16
Field		
poly	7	17
poly	8	18
Metal	9	19
Metal	10	20

Resistors & Contacts

Filename:

bc1r2bres, bc1r2acont

Purpose:

To measure the sheet and contact resistance.

Description:

This block contains three two-terminal resistors, two four-terminal resistors and three contact chains. Each resistor consists of a 17-square long bar (L=170 Lambda,W=10 Lambda), terminated with 2Wx2W squares containing 1Wx1W contacts. The four terminal resistor consists of a 14-square long bar between the two sense terminals.

The contact chains consist of an array of 20x5 minimum size contacts. They are formed with 50 bars (n+, p+ diffusions or poly) with connecting metal strips. Each diffused bar has dimensions L=15.5 and W=5.5 (in Lambda units). The minimum size contact (1.5x1.5) is placed 2 Lambda from the bar edge. The poly bars have dimensions L=17.5 and W=7.5, with the contact placed 3 Lambda from the edge.

Two-Terminal Resistors

n-well	(17 squares plus terminations)
n+ poly	"
n+p+ poly	"

Four-Terminal Resistors

p+	(14 squares center to center)
n+	(between sense terminals)

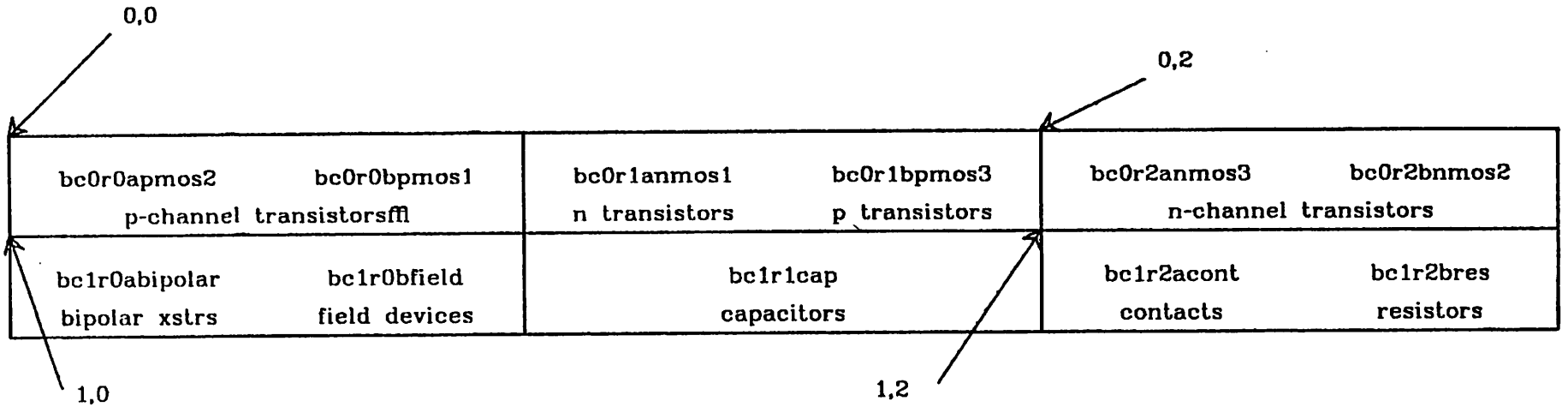
Contact Chains

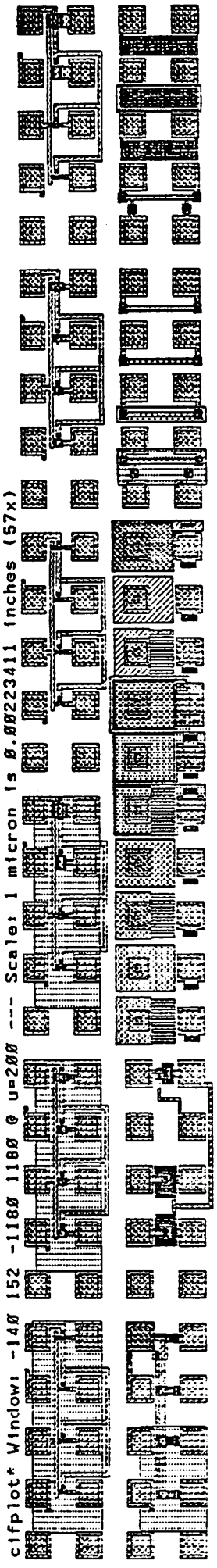
metal/poly	(100 minimum size contacts)
metal/p+	(")
metal/n+	(")

Pad Assignment:

Structure	PAD NUMBER	
	Pin 1	Pin 2
resistors		
N-well	6	16
N+Poly	7	17
P+Poly	8	18
P+	9,10	19,20
contacts		
N+	4,5	14,15
M/Poly	1	11
M/P+	2	12
M/N+	3	13

DEVICE DROP-IN TEST PATTERN FLOORPLAN

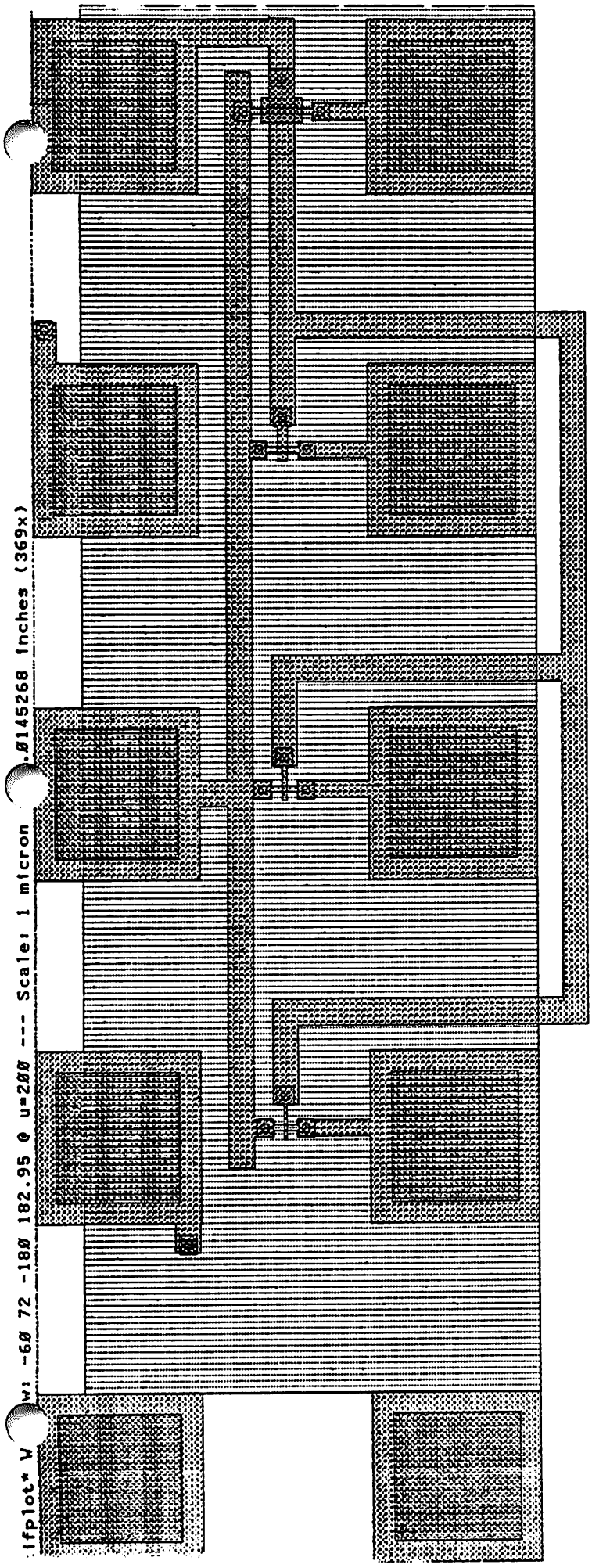




b subchip

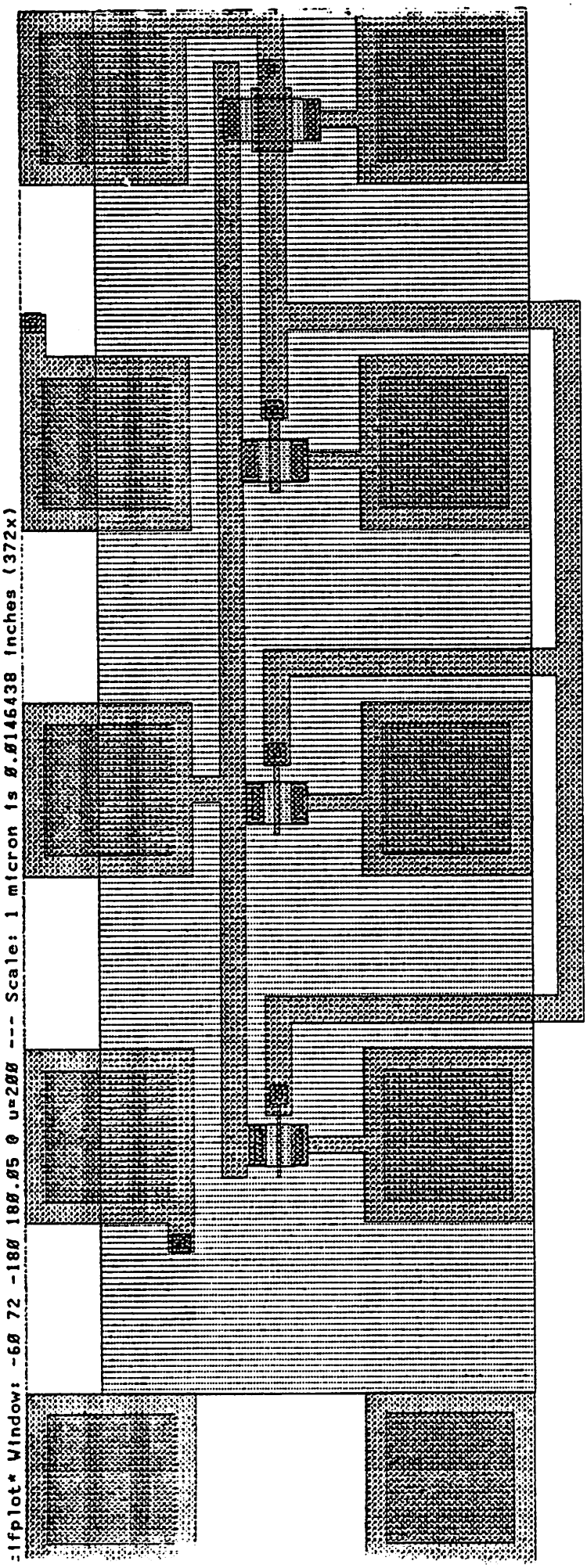
Device Drop-in

Test Pattern



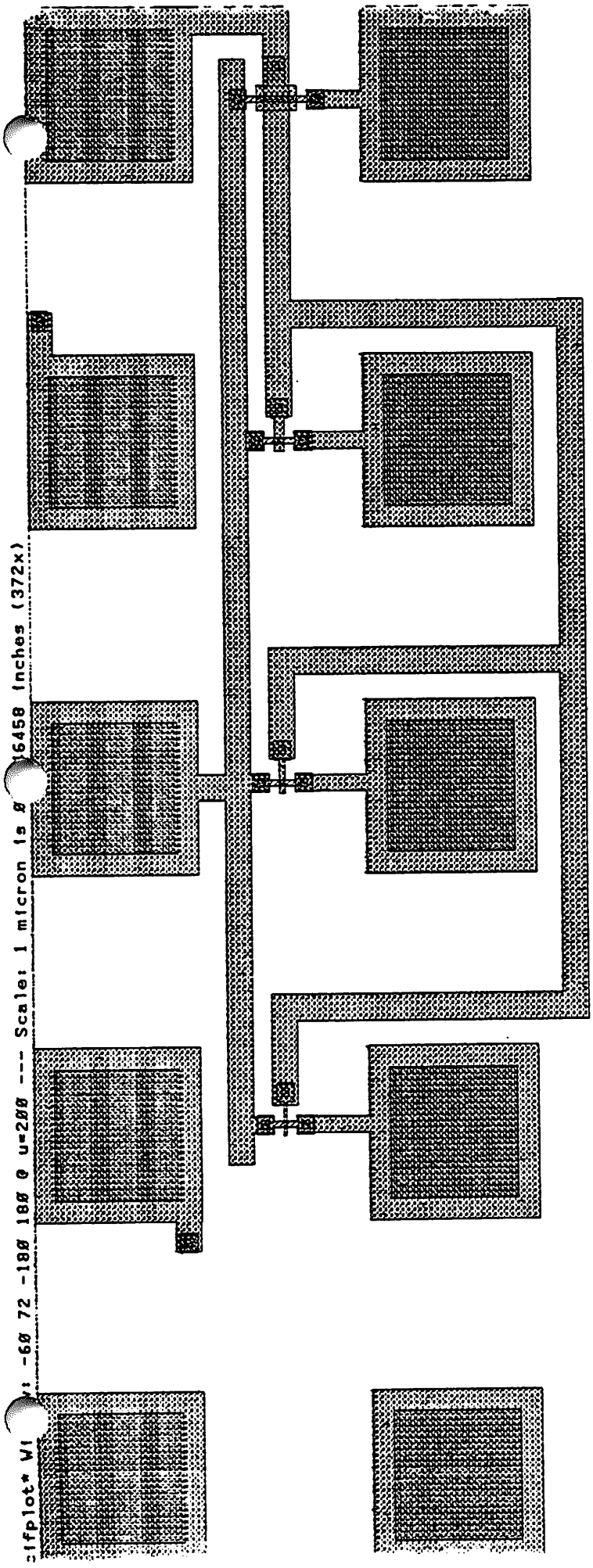
bc0r0bpmos1.cif

p-channel transistors



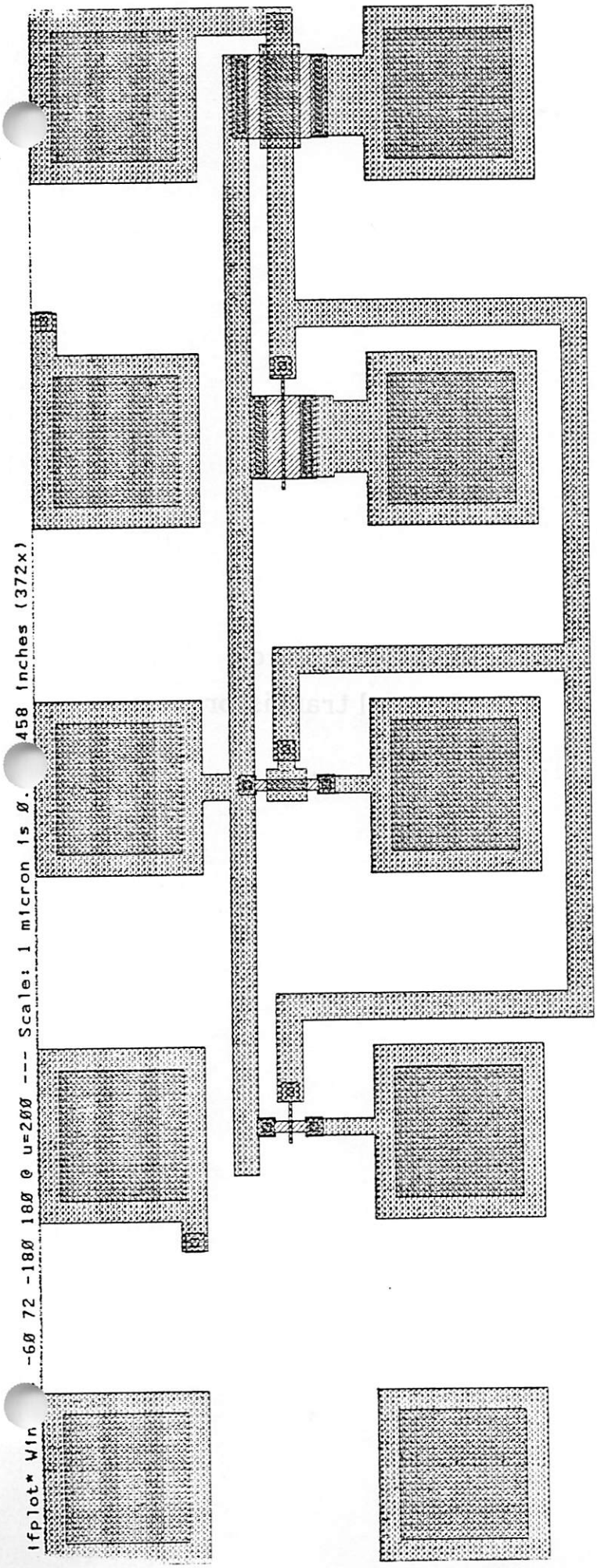
bc0r0apmos2.cif

p-channel transistors



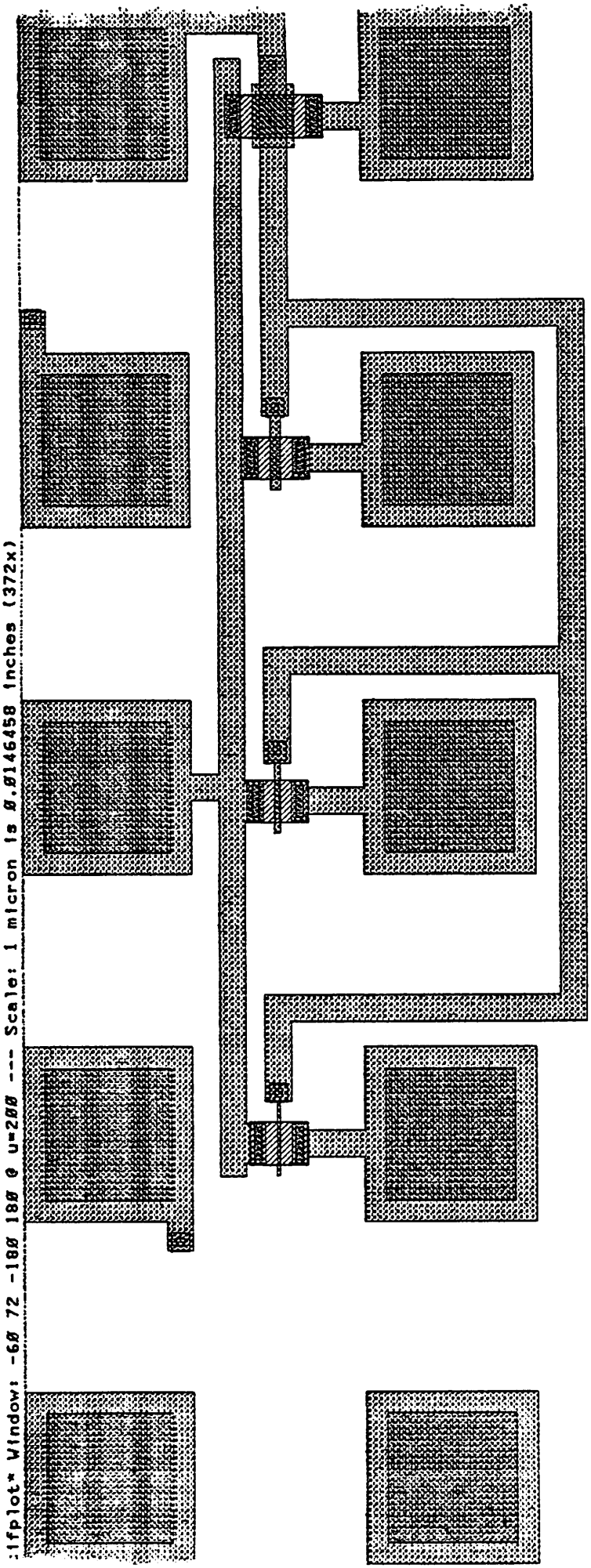
bc0r1anmos1.cif
n-channel transistors

bc0r1bpmos3.cif
p-channel transistors



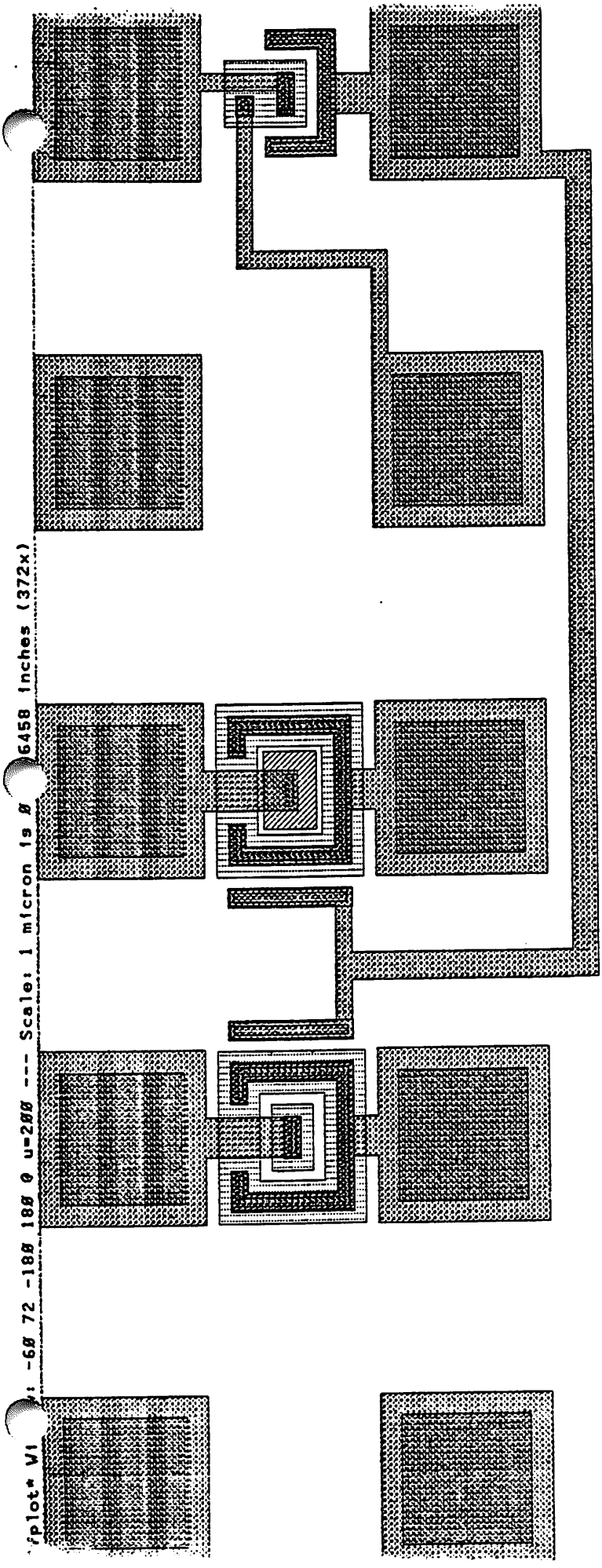
bc0r2anmos3.cif

n-channel transistors

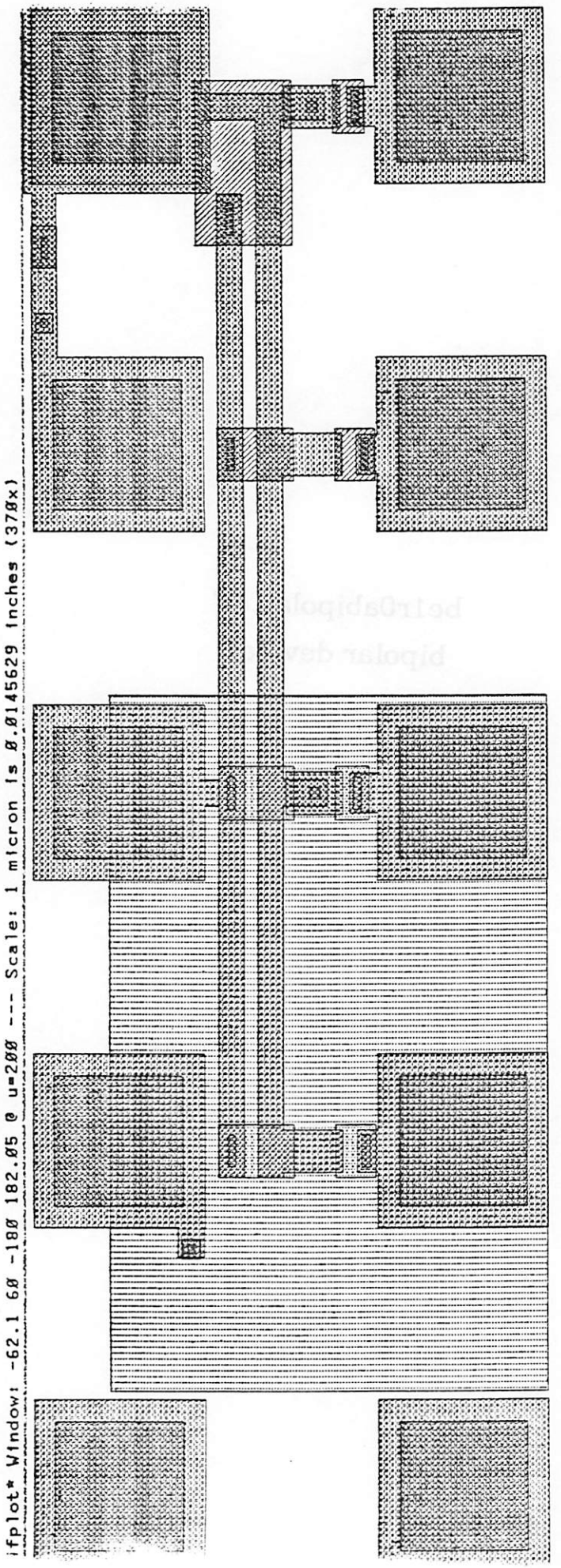


bc0r2anmos2.cif

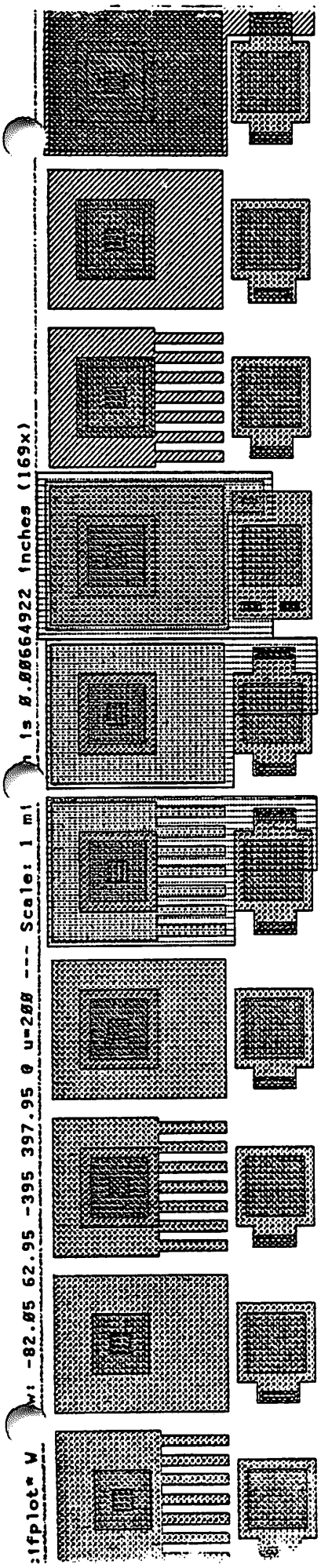
n-channel transistors



bc1r0abipolar.cif
bipolar devices



bc1r0bfield.cif
field devices



bc1r1cap.cif

capacitors

cap 1

bc1r1cap.cif

cap 2

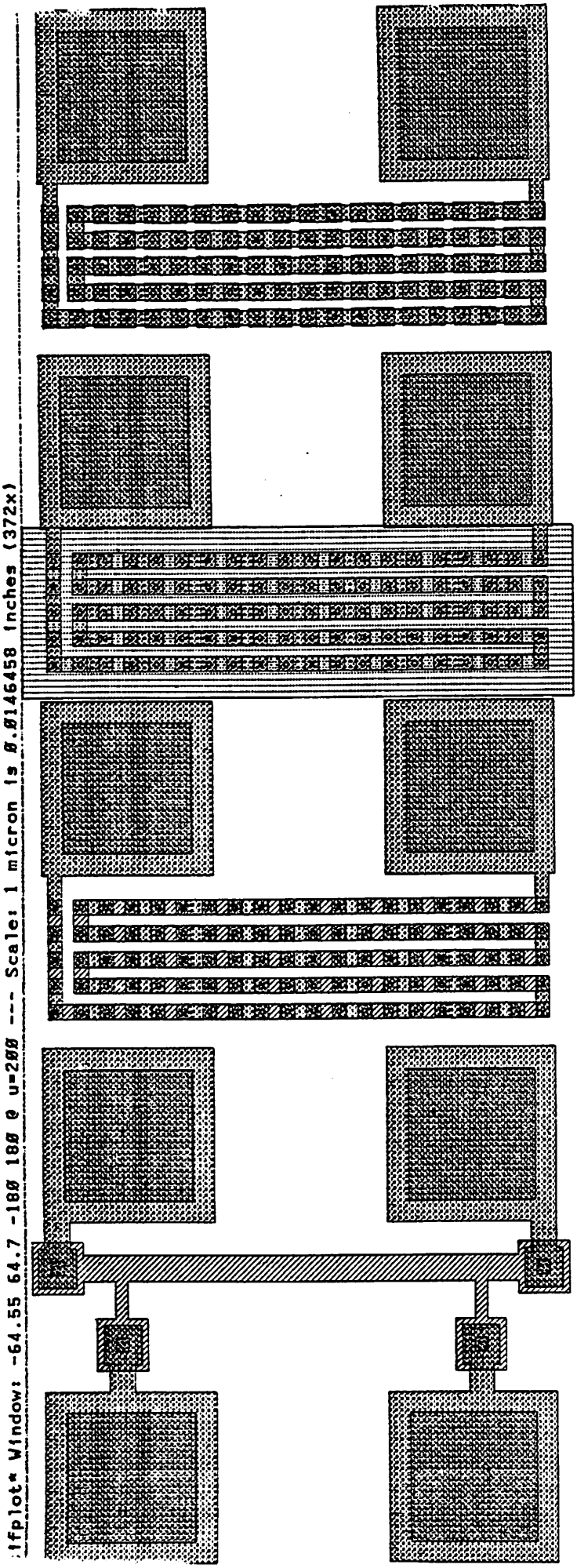
cap 3

clfplot* Window: -76.25 60.05 165 396.25 @ u=200 --- Scale: 1 micron is 0.0228 inches (579x)

cap 4
bc1r1cap.cif
cap 5
cap 6
cifplot* ow: -78.75 62.95 -77.5 158.75 @ u=200 --- Scale: 1 on is Ø.Ø223175 inches (567x)

cap 7
cap 8
bc1r1cap.cif
cap 9
cap 10
cifplot* Window: -75 60.05 -395 -85 @ u=200 --- Scale: 1 micron is 0.017000l Inches (432x)

bc1r2bres.cif
resistors



bc1r2bcont.cif

contacts

Device Drop-In Test Pattern (bsubchip)
Cif File Cell Hierarchy

PAD.k

PADSET.k
  PAD.k

bc0r0apmos2.k
  nncont.k polycont.k ppcont.k ppcont16.k

bc0r0bpmos1.k
  nncont.k polycont.k ppcont.k

bc0r1anmos1.k
  nncont.k polycont.k

bc0r1bpmos3.k
  nncont.k polycont.k ppcont.k ppcont32.k

bc0r2anmos3.k
  nncont.k nncont32.k polycont.k ppcont.k

bc0r2bnmos2.k
  nncont16.k polycont.k ppcont.k

bc1r0abiplr.k
  nncont16.k ppcont.k

bc1r0bfield.k
  nncont.k nncont16.k ppcont.k ppcont16.k

bc1r1cap.k
  cap1.k cap10.k cap2.k cap3.k
  cap4.k cap5.k cap6.k
  cap7.k cap8.k cap9.k

bc1r2acont.k
  nncontchain.k polycntchain.k ppcontchain.k

bc1r2bres.k

bsubchip.k
  PADSET.k bc0r0apmos2.k bc0r0bpmos1.k
  bc0r1anmos1.k bc0r1bpmos3.k bc0r2anmos3.k
  bc0r2bnmos2.k bc1r0abiplr.k bc1r0bfield.k
  bc1r1cap.k bc1r2acont.k bc1r2bres.k

cap1.k
  ppcont32.k

cap10.k
  ppcont32.k

cap2.k
  nncont32.k ppcont32.k

cap3.k
  nncont32.k ppcont32.k

cap4.k
  nncont16.k ppcont16.k

cap5.k
  nncont32.k ppcont32.k

cap6.k
  nncont32.k ppcont32.k

cap7.k
  ppcont32.k

cap8.k
  ppcont32.k

cap9.k
  ppcont32.k

nncont.k

nncont16.k

nncont32.k

nncontchain.k

polycntchain.k

polycont.k

ppcont.k

ppcont16.k

ppcont32.k

ppcontchain.k

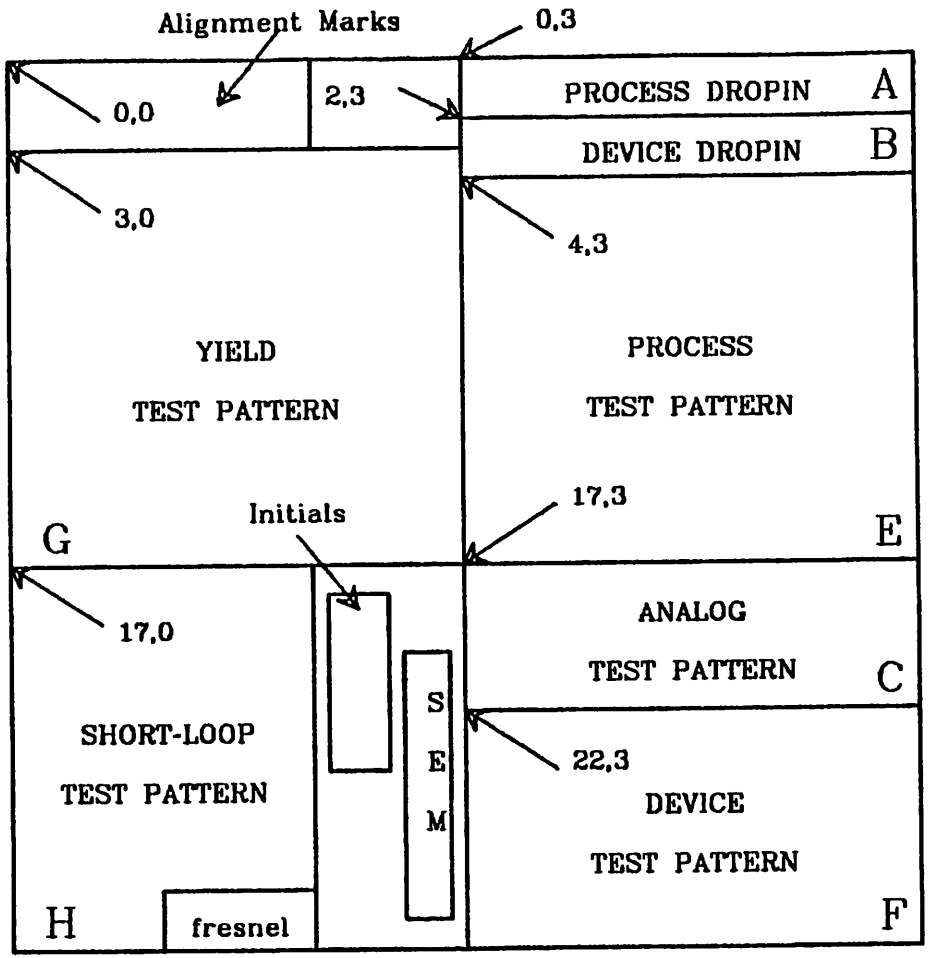
EE290 TEST CHIP ORGANIZATION

The EE290 test chip is made up of 7 Test Patterns plus a separate section for alignment marks. The 7 Test Patterns are: Device, Device Drop-in, Process, Process Drop-in, Shortloop, Yield, and Analog. Each test pattern consists of a collection of functional units. A functional unit is made up of several blocks which together accomplish a specific goal. These blocks are 320um x 1800um. Each block may contain a 2 x 10 array of 80um pads on 160um centers. A block does not always contain all 20 pads since some test structures require a large area, however the pads which are present will remain on the 160um grid. The pad numbering convention is shown below. Pad #1 contains a small notch in it to help distinguish top from bottom when viewing the chip through a microscope. The entire EE290 chip is a 6 row, 30 column array of blocks.

1	11
2	12
3	13
4	14
5	15
6	16
7	17
8	18
9	19
10	20

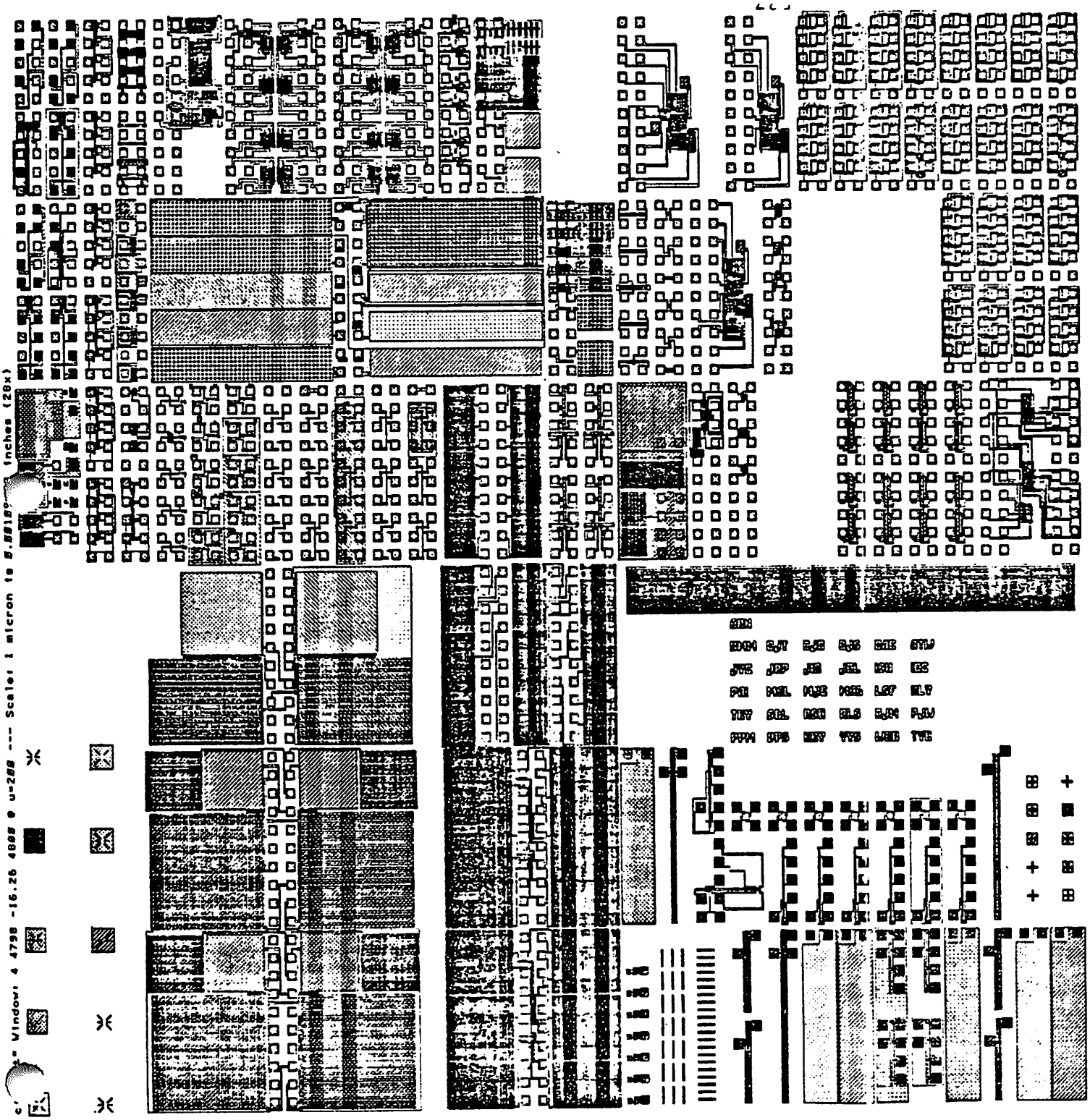
The testing of the devices can be accomplished with a 2 x 5 probe card. Some of the test patterns must be tested with a 2 x 10 probe card due to unconventional pad assignments and the inability to constrain the test structure to a 2 x 5 sub-block.

BERKELEY CMOS PROCESS TEST CHIP



testchip.cif

Entire EE290 Test Chip



BERKELEY CMOS PROCESS
DEVICE TEST PATTERN

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Joseph Pierret

(revised by)
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Berkeley, California

REV 0.0
(Spring 1984)

Device Test Pattern
Table of Contents

DISCUSSION

Device Test Pattern

NMOS & PMOS Transistors Description

Measurement of NMOS and PMOS devices will include the threshold voltage **Vth**, transconductance **k'**, body effect coefficient **gamma**, and channel length modulation parameter **lambda**.

A matrix with width (Z) and length (L) ranging from L = 0.6 um and Z = 0.6 um to L = 38.4 um and Z = 38.4 um will be included. These odd values correspond to a lambda=1.2 um. The matrix is repeated for NMOS and PMOS devices. Below is the matrix.

		L um							
		0.6	0.8	1.0	1.2	2.4	4.8	19.2	38.4
Z um	0.6				X	X			
	0.8				X	X			
	1.0				X	X			
	1.2				X	X			
	2.4	X	X	X	X	X	X	X	X
	4.8	X	X	X	X	X	X	X	X
	19.2				X	X	X	X	
	38.4				X	X		X	X

The matrix is made up of 32 transistors which have been chosen with specific purposes in mind:

(1) Any row (constant Z) can be tested to note the effects on **Vth** as **Leff** shrinks. In particular, the row with the minimum design rule width = 2.4 um can be tested. If this row fails, Z = 4.8 um has been included.

(2) Similarily, any column, (constant L) can be tested for narrow channel effects. The column with the minimum design rule width = 1.2 um can be tested to note the effects on **Vth** as **Leff** shrinks. If this row fails, L=2.4 um has been included.

(3) The diagonal can be tested to see how small the process can be made. As testing proceeds up the diagonal, and the devices fail, an obvious physical limitation has been reached.

To allow for the maximum density of devices on a chip, and to meet the requirements of fitting in the 2x5 pad convention, four devices will share 10 contacts. The four devices will have a common gate, source, substrate, and body connections. NOTE: The body connections on the NMOS devices is common with the substrate as they are one in the same.

The drop-in device chip has been designed as a subset of the matrix. There were some values in the matrix which were not originally included. However, with the drop-in transistors and our original transistors accounted for, some extra blocks existed, so we filled in the holds with extra transistors. There remains a few empty blocks which can be allocated to specific sub-chips appropriately.

Parasitic NMOS & PMOS Devices Description

Measurement of field devices will include **Vth** and verification of the design rule **Saa**. Both of these measurements can be made with a constant Z device. Z should be large enough to ensure working and testable devices. Therefore Z=12 um is chosen. L is made larger than the design rule to check **Vth** and smaller than the design rule to measure **Saa**. As L decreases and reaches its critical value, conduction will occur between non-associated source/drains and therefore failure occurs. L is varied from 1.2 to 12 um. The devices are repeated for both NMOS and PMOS devices. The devices are tested for poly gate over thick oxide and Aluminum gate over PSG over thick oxide. To assure that the transistors are operative, the poly overlaps the diffusion edge by 3 um on each side.

Design of the Layout for PMOS, NMOS, & Field Transistors

The poly runs for the gate connections are snaked around the outside of the pads instead of down the middle to allow the source/drain contacts to be as close as possible to the active transistor area. This reduces the series resistance of the n+ or p+ "diffusion" runs.

The metal run for the source connection is run outside the pad area instead of down the middle to allow for easier laying out of similar cells. For a small transistor, the metal run would fit between two rows of pads with no problem. However, for larger transistors, it would not. Since this would require two different layouts, a single general one was opted for.

Special MOS Devices Description

Provided are n+ to nwell (npnw), p-substrate to p+ (pmpp), & nwell to nwell (nwnw) special MOS devices. Polysilicon gate structures for 6 different channel lengths for each npnw & pmpp plus 4 for nwnw are provided, creating a total of 16 special MOS devices. A channel width of 5um is used.

All three types of devices are contained in a single block which is surrounded on either side by pads. The device block is fc11r00SMOS, the pad blocks are fc12r00SPAD & fc10r00SPAD.

Bipolar Devices Description

A 4 x 4 matrix of p+ in nwell stripes placed near stripes of n+ provide bipolar structures for diode, transistor, & latchup tests. The p+ to nwell (Ewp+) and n+ to nwell (Swn+) spacing are 15, 10, 2.3, and 1 um. These structures occupy 4 blocks, with each block including 4 devices of constant n+ separation.

SUMMARY TABLE

Device Test Pattern

Filename Sz-(Blks)	Structure Z/L (um)	Coordinates within 290n chip	Test Pat.	Func. Unit
PMOS TRANSISTORS				
fc0r2pmos 1	0.6/1.2 0.6/2.4 0.8/1.2 0.8/2.4 1.0/1.2 1.0/2.4 1.2/1.2 1.2/2.4	c22r2	c0r2	c0r2
fc1r2pmos 1	2.4/0.6 2.4/0.8 2.4/1 2.4/2 2.4/2.4 2.4/4.8 2.4/19.2 2.4/38.4	c23r2	c1r2	c1r2
fc2r2pmos 1	4.8/0.6 4.8/0.8 4.8/1 4.8/2 4.8/2.4 4.8/4.8 4.8/19.2 4.8/38.4	c24r2	c2r2	c2r2
fc3r2pmos 1	19.2/1.2 19.2/2.4 19.2/4.8 19.2/19.2 38.4/1.2 38.4/2.4 38.4/4.8 38.4/19.2	c25r2	c3r2	c3r2

SUMMARY TABLE

Device Test Pattern

Filename Sz-(Blks)	Structure Z/L (um)	Coordinates within 290n chip	Test Pat.	Func. Unit
NMOS TRANSISTORS				
fc4r2nmos 1	0.6/1.2 0.6/2.4 0.8/1.2 0.8/2.4 1.0/1.2 1.0/2.4 1.2/1.2 1.2/2.4	c26r2	c4r2	c4r2
fc5r2nmos 1	2.4/0.6 2.4/0.8 2.4/1 2.4/2 2.4/2.4 2.4/4.8 2.4/19.2 2.4/38.4	c27r2	c5r2	c5r2
fc6r2nmos 1	4.8/0.6 4.8/0.8 4.8/1 4.8/2 4.8/2.4 4.8/4.8 4.8/19.2 4.8/38.4	c28r2	c6r2	c6r2
fc7r2nmos 1	19.2/1.2 19.2/2.4 19.2/4.8 19.2/19.2 38.4/1.2 38.4/2.4 38.4/4.8 38.4/19.2	c29r2	c7r2	c7r2

SUMMARY TABLE

Device Test Pattern

Filename Sz-(Blks)	Structure Z/L (um)	Coordinates within 290n chip	Test Pat.	Func. Unit
PMOS FIELD TRANSISTORS				
fc4r1pfsi	12/1.2 12/1.8 12/2.4 12/3.0 12/3.6 12/4.8 12/9.6	c26r1	c4r1	c4r1
1	12/12			
fc5r1pfal	12/1.2 12/1.8 12/2.4 12/3.0 12/3.6 12/4.8 12/9.6	c27r1	c5r1	c5r1
1	12/12			
NMOS FIELD TRANSISTORS				
fc6r1nfsi	12/1.2 12/1.8 12/2.4 12/3.0 12/3.6 12/4.8 12/9.6	c28r1	c6r1	c6r1
1	12/12			
fc7r1nfal	12/1.2 12/1.8 12/2.4 12/3.0 12/3.6 12/4.8 12/9.6	c29r1	c7r1	c7r1
1	12/12			

SUMMARY TABLE

Device Test Pattern

Filename Sz-(Blks)	Structure	Coordinates within 290n chip	Test Pat.	Func. Unit
SPECIAL MOS DEVICES				
fc5r00SMOS	NMOS device with n+ in nwell source n+ in substrate drain–(npnw) l=1, 2.3, 4, 6, 10, 15 um	c27r0	c5r0	c5r0 c7r0
	PMOS device with p+ in nwell drain p+ in substrate source–(pmpp) L=0, 1 um 2.3, 3, 4, 5 um	c27r0	c5r0	c5r0 c7r0
	NMOS device with n+ in nwell drain n+ in substrate source–(nwnw)	c27r0	c5r0	
3	L=2.5, 5, 8, 10 um			c5r0
BIPOLAR DEVICES				
fc01r00BJTS	BJT with Swn+ = 15 Ewn+ = 1, 2.3, 10, & 15 um	c23r0	c1r0	c1r0
fc02r00BJTS	BJT with Swn+ = 10 Ewn+ = 1, 2.3, 10, & 15 um	c24r0	c2r0	c2r0
fc03r00BJTS	BJT with Swn+ = 2.3 Ewn+ = 1, 2.3, 10, & 15 um	c25r0	c3r0	c3r0
fc04r00BJTS	BJT with Swn+ = 1 Ewn+ = 1, 2.3, 10, & 15 um	c26r0	c4r0	c4r0

FUNCTIONAL DESCRIPTION

Device Test Pattern

NMOS & PMOS Transistors

Filenames:

fc0r2pmos, fc1r2pmos, fc2r2nmos, fc3r2pmos
fc4r2nmos, fc5r2nmos, fc6r2nmos, fc7r2nmos

Purpose:

To characterize the electrical parameters of the MOS devices.

Pad Assignment:

N-Channel Transistors:

fc4r2nmos

W/L	PAD NUMBER				
	G	S	D	B	SUB
0.6/1.2	1	3	11	2	4
0.6/2.4	1	3	12	2	4
0.8/1.2	1	3	13	2	4
0.8/2.4	1	3	14	2	4
1.0/1.2	6	8	16	7	9
1.0/2.4	6	8	17	7	9
1.2/1.2	6	8	18	7	9
1.2/2.4	6	8	19	7	9

fc5r2nmos

W/L	PAD NUMBER				
	G	S	D	B	SUB
2.4/0.6	1	3	11	2	4
2.4/0.8	1	3	12	2	4
2.4/1.0	1	3	13	2	4
2.4/2.0	1	3	14	2	4
2.4/2.4	6	8	16	7	9
2.4/4.8	6	8	17	7	9
2.4/19.2	6	8	18	7	9
2.4/38.4	6	8	19	7	9

fc6r2nmos

W/L	PAD NUMBER				
	G	S	D	B	SUB
4.8/0.6	1	3	11	2	4
4.8/0.8	1	3	12	2	4
4.8/1.0	1	3	13	2	4
4.8/2.0	1	3	14	2	4
4.8/2.4	6	8	16	7	9
4.8/4.8	6	8	17	7	9
4.8/19.2	6	8	18	7	9
4.8/38.4	6	8	19	7	9

fc7r2nmos

W/L	PAD NUMBER				
	G	S	D	B	SUB
19.2/1.2	1	3	11	2	4
19.2/2.4	1	3	12	2	4
19.2/4.8	1	3	13	2	4
19.2/19.2	1	3	14	2	4
38.4/1.2	6	8	16	7	9
38.4/2.4	6	8	17	7	9
38.4/4.8	6	8	18	7	9
38.4/19.2	6	8	19	7	9

P-Channel Transistors:

fc0r2pmos

W/L	PAD NUMBER				
	G	S	D	B	SUB
0.6/1.2	1	3	11	2	4
0.6/2.4	1	3	12	2	4
0.8/1.2	1	3	13	2	4
0.8/2.4	1	3	14	2	4
1.0/1.2	6	8	16	7	9
1.0/2.4	6	8	17	7	9
1.2/1.2	6	8	18	7	9
1.2/2.4	6	8	19	7	9

fc1r2pmos

W/L	PAD NUMBER				
	G	S	D	B	SUB
2.4/0.6	1	3	11	2	4
2.4/0.8	1	3	12	2	4
2.4/1.0	1	3	13	2	4
2.4/2.0	1	3	14	2	4
2.4/2.4	6	8	16	7	9
2.4/4.8	6	8	17	7	9
2.4/19.2	6	8	18	7	9
2.4/38.4	6	8	19	7	9

fc2r2pmos

W/L	PAD NUMBER				
	G	S	D	B	SUB
4.8/0.6	1	3	11	2	4
4.8/0.8	1	3	12	2	4
4.8/1.0	1	3	13	2	4
4.8/2.0	1	3	14	2	4
4.8/2.4	6	8	16	7	9
4.8/4.8	6	8	17	7	9
4.8/19.2	6	8	18	7	9
4.8/38.4	6	8	19	7	9

fc3r2pmos

W/L	PAD NUMBER				
	G	S	D	B	SUB
19.2/1.2	1	3	11	2	4
19.2/2.4	1	3	12	2	4
19.2/4.8	1	3	13	2	4
19.2/19.2	1	3	14	2	4
38.4/1.2	6	8	16	7	9
38.4/2.4	6	8	17	7	9
38.4/4.8	6	8	18	7	9
38.4/19.2	6	8	19	7	9

Parasitic NMOS & PMOS Devices

Filename:

fc4r1pfsi, fc5r1pfal,
fc8r1nfsi, fc7r1nfal

Purpose:

To characterize the electrical parameters of the MOS devices, espcially Vth for the field oxide and the design rule Saa.

Pad Assignment:

fc4r1pfsi (PMOS Silicon gate)

W/L	PAD NUMBER				
	G	S	D	B	SUB
12/1.2	1	3	11	2	4
12/1.8	1	3	12	2	4
12/2.4	1	3	13	2	4
12/3.0	1	3	14	2	4
12/3.6	6	8	16	7	9
12/4.8	6	8	17	7	9
12/9.6	6	8	18	7	9
12/12	6	8	19	7	9

fc5r1pfal (PMOS Aluminum gate)

W/L	PAD NUMBER				
	G	S	D	B	SUB
12/1.2	1	3	11	2	4
12/1.8	1	3	12	2	4
12/2.4	1	3	13	2	4
12/3.0	1	3	14	2	4
12/3.6	6	8	16	7	9
12/4.8	6	8	17	7	9
12/9.6	6	8	18	7	9
12/12	6	8	19	7	9

fc8r1nfsi (NMOS Silicon gate)

W/L	PAD NUMBER				
	G	S	D	B	SUB
12/1.2	1	3	11	2	4
12/1.8	1	3	12	2	4
12/2.4	1	3	13	2	4
12/3.0	1	3	14	2	4
12/3.6	6	8	16	7	9
12/4.8	6	8	17	7	9
12/9.6	6	8	18	7	9
12/12	6	8	19	7	9

fc7r1nfal (NMOS Aluminum gate)

W/L	PAD NUMBER				
	G	S	D	B	SUB
12/1.2	1	3	11	2	4
12/1.8	1	3	12	2	4
12/2.4	1	3	13	2	4
12/3.0	1	3	14	2	4
12/3.6	6	8	16	7	9
12/4.8	6	8	17	7	9
12/9.6	6	8	18	7	9
12/12	6	8	19	7	9

Special MOS Devices

Filename:

fc05r00SPADS

Purpose:

To find Vth for various parasitic MOS devices. In particular, this includes

(1) npnw which is NMOS with drain = n+ in nwell and source = n+ in substrate
(2) pmpp which is PMOS with drain = p+ in nwell and source = p+ in substrate
(3) nwnw which is NMOS with drain = n+ in nwell and source = n+ in nwell

Pad Assignment:

DEVICE	L=	PAD NUMBER				
		G	S	D	B	SUB
npnw	2.3	3	11	1	use 9	use 9
	1	3	12	1	use 9	use 9
pmpp	1	3	13	4	1	13
	0	3	14	4	1	14
nwnw	5	8	16	6	9	9
	2.5	8	17	6	9	9
	8	8	18	6	9	9
	10	8	19	6	9	9

Filename:

fc07r00SPADS

Pad Assignment:

DEVICE	L=	PAD NUMBER				
		G	S	D	B	SUB
npnw	4	3	11	1	4	4
	6	3	12	1	4	4
	10	3	13	1	4	4
	15	3	14	1	4	4
pmpp	2.3	8	6	16	9	16
	3	8	6	17	9	17
	4	8	6	18	9	18
	5	8	6	19	9	19

Bipolar Devices

Filename:

fc01r00BJTS to fc04r00BJTS

Purpose:

These are bipolar devices for diode, transistor, and latchup tests. The value of Swn+ and Ewp+ change to test the limitation on latchup.

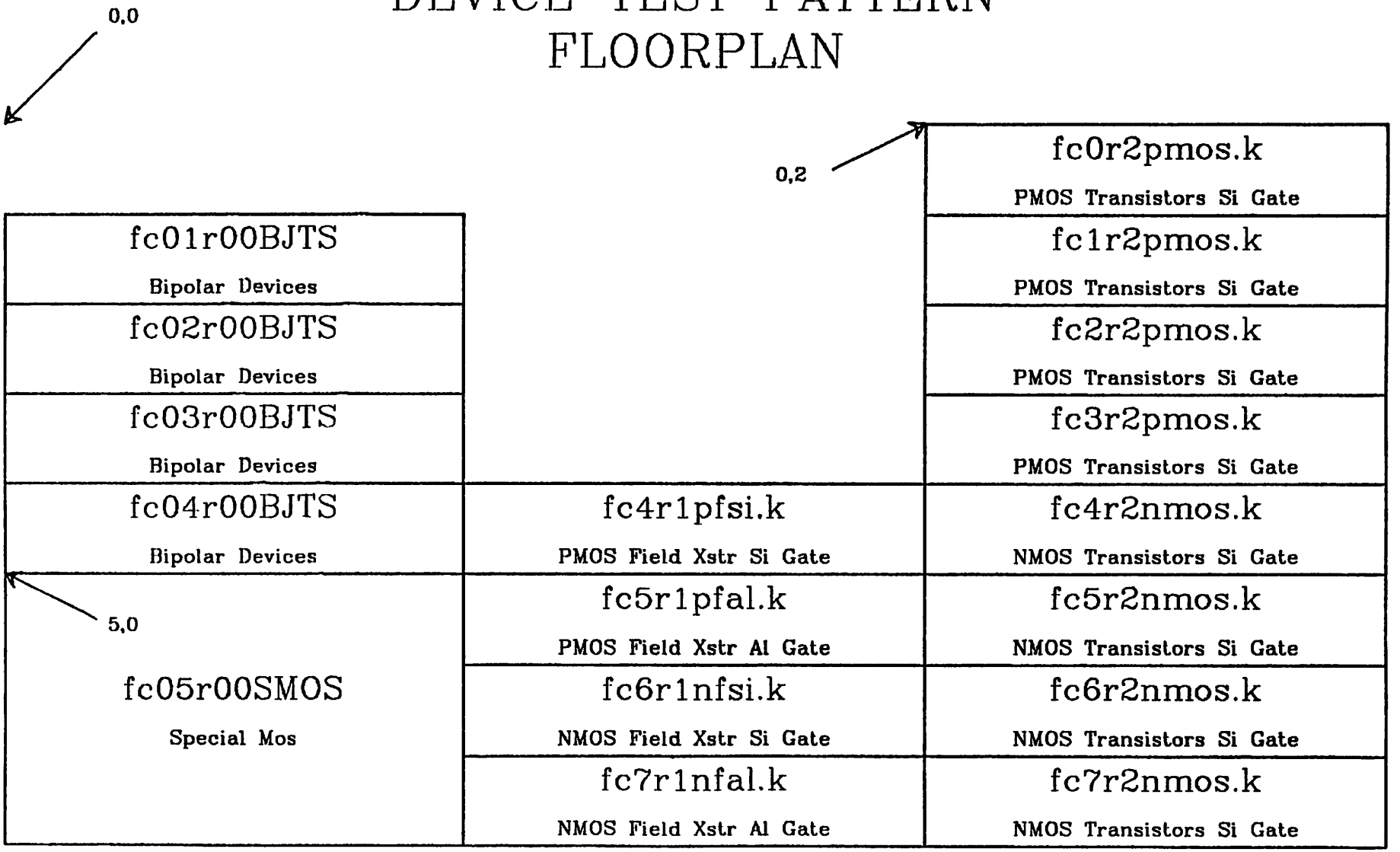
Description:

Each of the files fc01r00BJTS through fc04r00BJTS have the pad assignments described below. However each file has a different value for Swn+. fc01r00BJTS has Swn+ = 15um, fc02r00BJTS has Swn+ = 10um, fc03r00BJTS has Swn+ = 2.3um, and fc04r00BJTS has Swn+ = 1um.

Pad Assignment:

Ewp+	PAD NUMBER				
	p+ in nwell	well	n+ in sub.	sub.	gate
15	12	1	11	2	4
10	14	3	13	2	4
2.3	17	6	16	7	9
1	19	8	18	7	9

DEVICE TEST PATTERN FLOORPLAN



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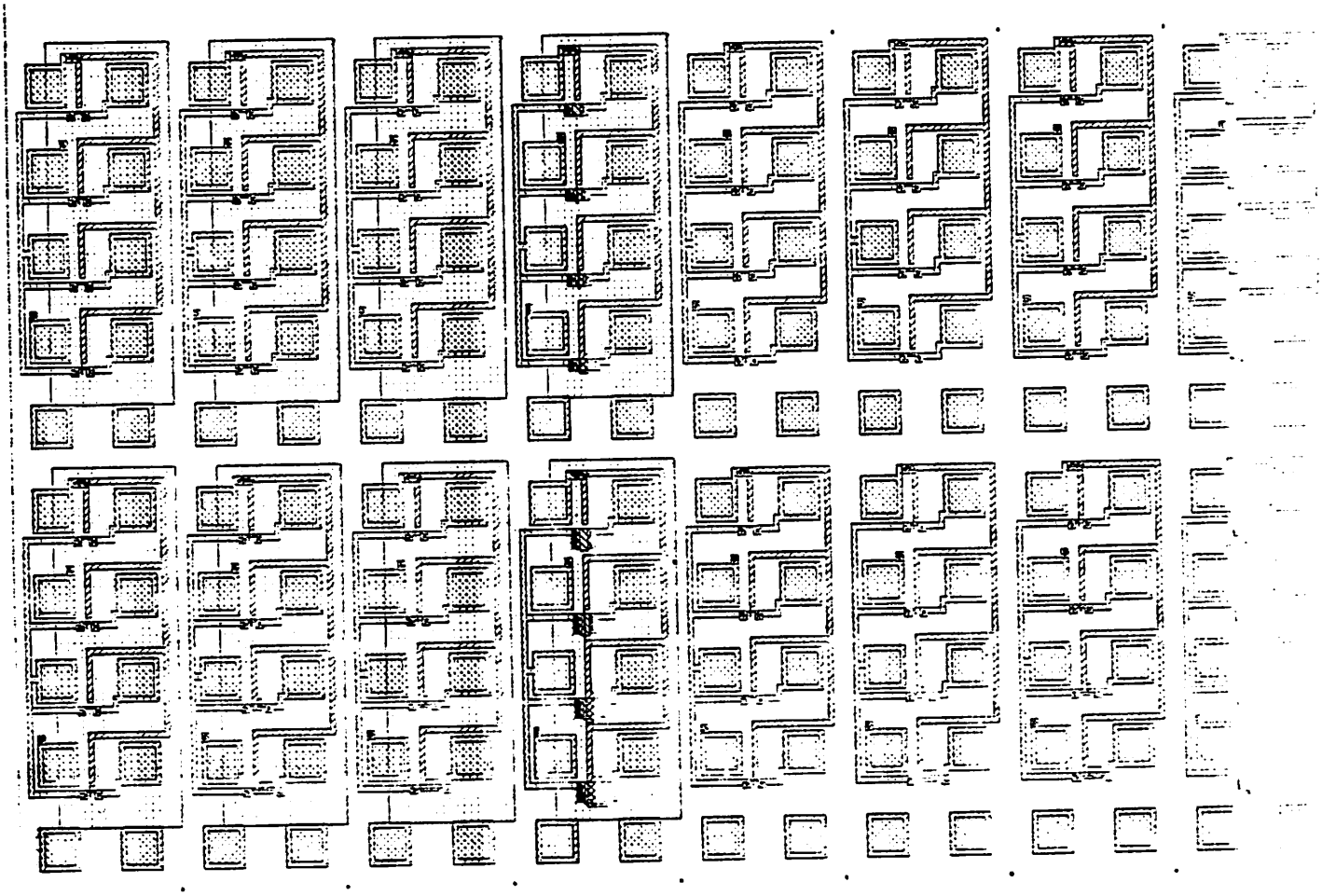
Device Test Pattern

DETAILED FLOOR PLAN – MOS TRANSISTORS

fc0r2nmos	fc1r2nmos	fc2r2nmos	fc3r2nmos	fc4r2pmos	fc5r2pmos	fc6r2pmos	fc7r2pmos
$\frac{Z}{L}(\mu m)$	$\frac{Z}{L}(\mu m)$	$\frac{Z}{L}(\mu m)$	$\frac{Z}{L}(\mu m)$	$\frac{Z}{L}(\mu m)$	$\frac{Z}{L}(\mu m)$	$\frac{Z}{L}(\mu m)$	$\frac{Z}{L}(\mu m)$
0.6/1.2	2.4/0.6	4.8/0.6	19.2/1.2	0.6/1.2	2.4/0.6	4.8/0.6	19.2/1.2
0.6/2.4	2.4/0.6	4.8/0.6	19.2/2.4	0.6/2.4	2.4/0.6	4.8/0.6	19.2/2.4
0.6/1.2	2.4/1	4.8/1	19.2/4.8	0.6/1.2	2.4/1	4.8/1	19.2/4.8
0.6/2.4	2.4/1.2	4.8/1.2	19.2/19.2	0.6/2.4	2.4/1.2	4.8/1.2	19.2/19.2
1/1.2	2.4/2.4	4.8/2.4	38.4/1.2	1/1.2	2.4/2.4	4.8/2.4	38.4/1.2
1/2.4	2.4/4.8	4.8/4.8	38.4/2.4	1/2.4	2.4/4.8	4.8/4.8	38.4/2.4
1.2/1.2	2.4/19.2	4.8/19.2	38.4/19.2	1.2/1.2	2.4/19.2	4.8/19.2	38.4/19.2
1.2/2.4	2.4/38.4	4.8/38.4	38.4/38.4	1.2/2.4	2.4/38.4	4.8/38.4	38.4/38.4



$$\frac{Z}{L} = \frac{0.6\mu m}{1.2\mu m}$$

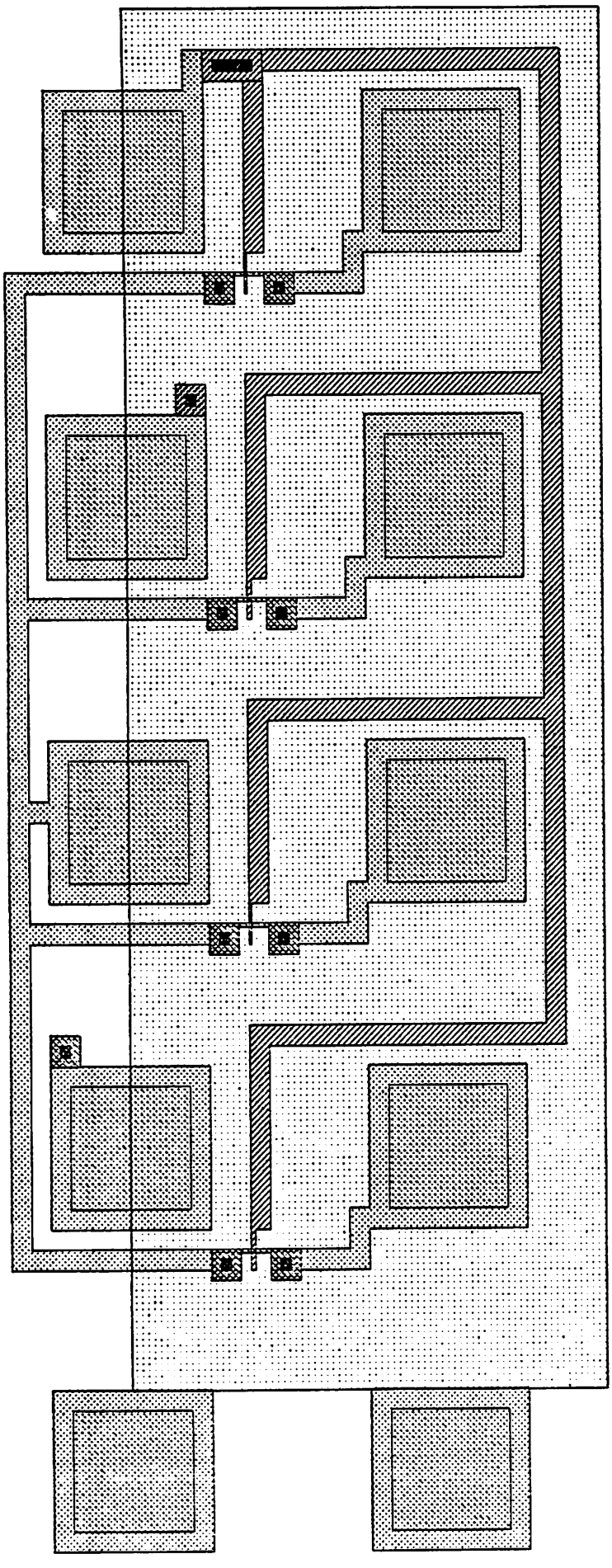
$$\frac{Z}{L} = \frac{0.6\mu m}{2.4\mu m}$$

fc0r2pmos.cif

pmos si gate transistors

$$\frac{Z}{L} = \frac{0.8\mu m}{1.2\mu m}$$

$$\frac{Z}{L} = \frac{0.8\mu m}{2.4\mu m}$$



cifplot* Window: 0 160 -800 0 @ u=200 --- Scale: 1 micron is 0.013 inches (330x)

$$\frac{Z}{L} = \frac{1\mu m}{1.2\mu m}$$

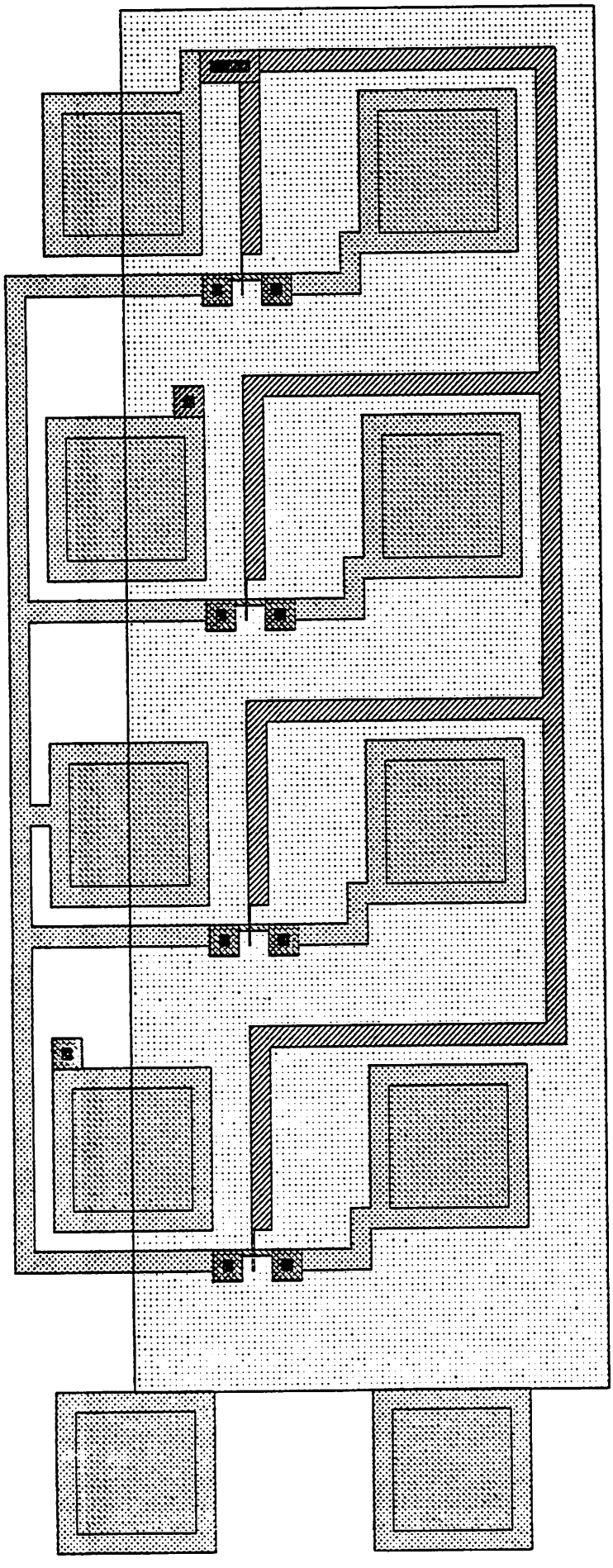
$$\frac{Z}{L} = \frac{1\mu m}{2.4\mu m}$$

fc0r2pmos.cif

pmos si gate
transistors

$$\frac{Z}{L} = \frac{1.2\mu m}{1.2\mu m}$$

$$\frac{Z}{L} = \frac{1.2\mu m}{2.4\mu m}$$



$$\frac{Z}{L} = \frac{2.4\mu m}{0.6\mu m}$$

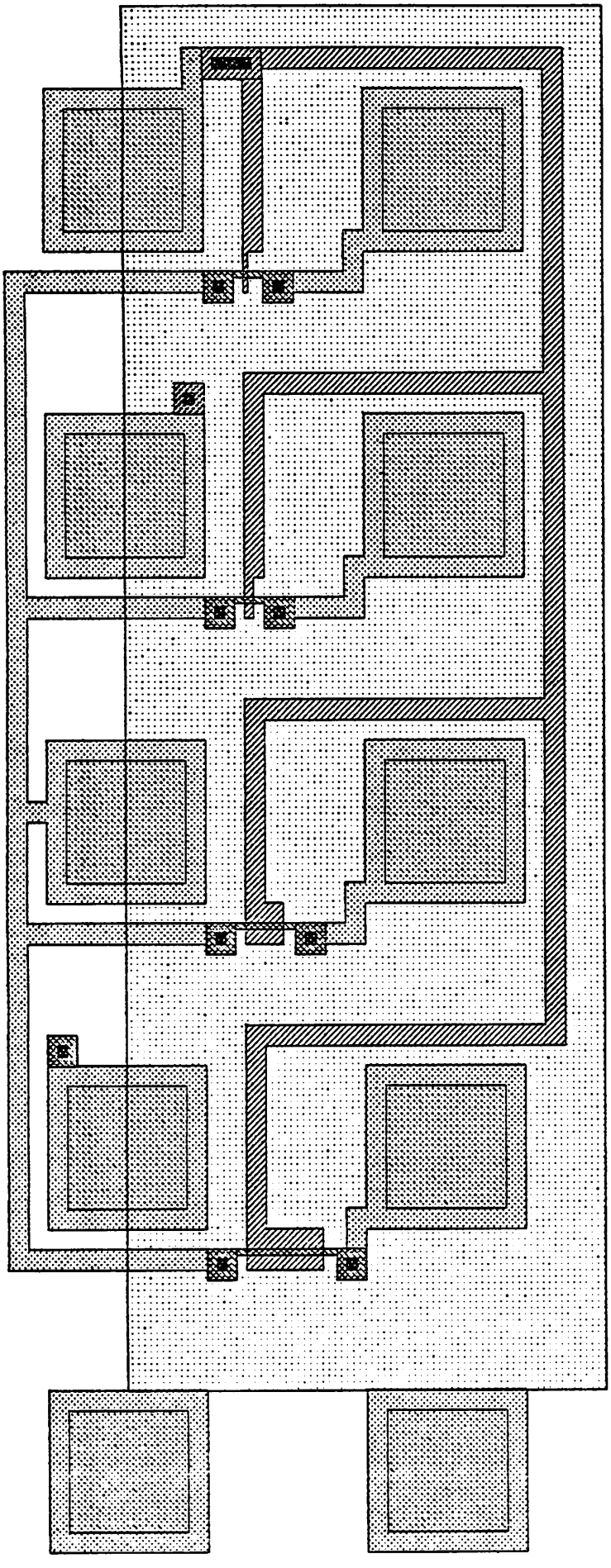
$$\frac{Z}{L} = \frac{2.4\mu m}{0.8\mu m}$$

fc1r2pmos.cif

pmos si gate transistors

$$\frac{Z}{L} = \frac{2.4\mu m}{1\mu m}$$

$$\frac{Z}{L} = \frac{2.4\mu m}{1.2\mu m}$$



$$\frac{Z}{L} = \frac{2.4\mu m}{2.4\mu m}$$

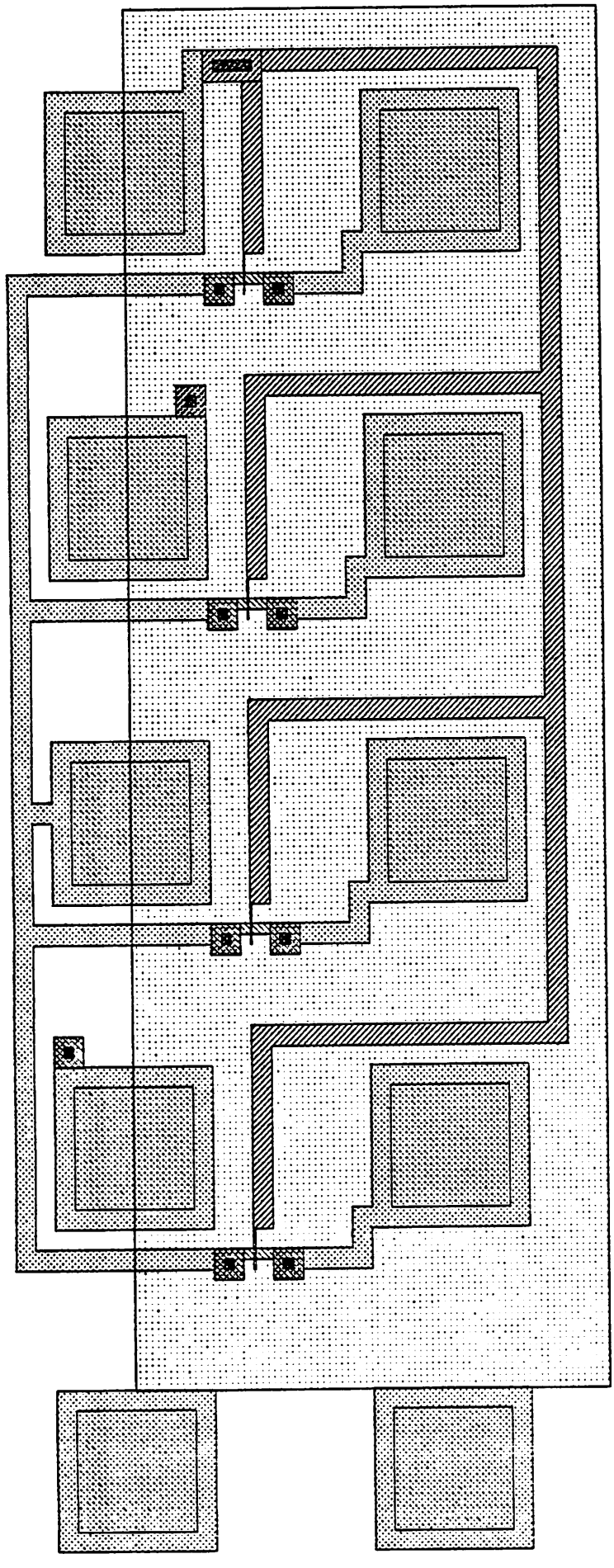
$$\frac{Z}{L} = \frac{2.4\mu m}{4.8\mu m}$$

fc1r2pmos.cif

pmos si gate
transistors

$$\frac{Z}{L} = \frac{2.4\mu m}{19.2\mu m}$$

$$\frac{Z}{L} = \frac{2.4\mu m}{38.4\mu m}$$



cifplot* dow: @ 160 -800 @ @ u=200 --- Scale: 1 micron is @ inches (3300x)

$$\frac{Z}{L} = \frac{4.8\mu m}{0.6\mu m}$$

$$\frac{Z}{L} = \frac{4.8\mu m}{0.8\mu m}$$

fc2r2pmos.cif

pmos si gate transistors

$$\frac{Z}{L} = \frac{4.8\mu m}{1\mu m}$$

$$\frac{Z}{L} = \frac{4.8\mu m}{1.2\mu m}$$

cifplot* Window: 0 160 -800 0 @ u=200 --- Scale: 1 micron is 0.013 inches (338x)

$$\frac{Z}{L} = \frac{4.8\mu m}{2.4\mu m}$$

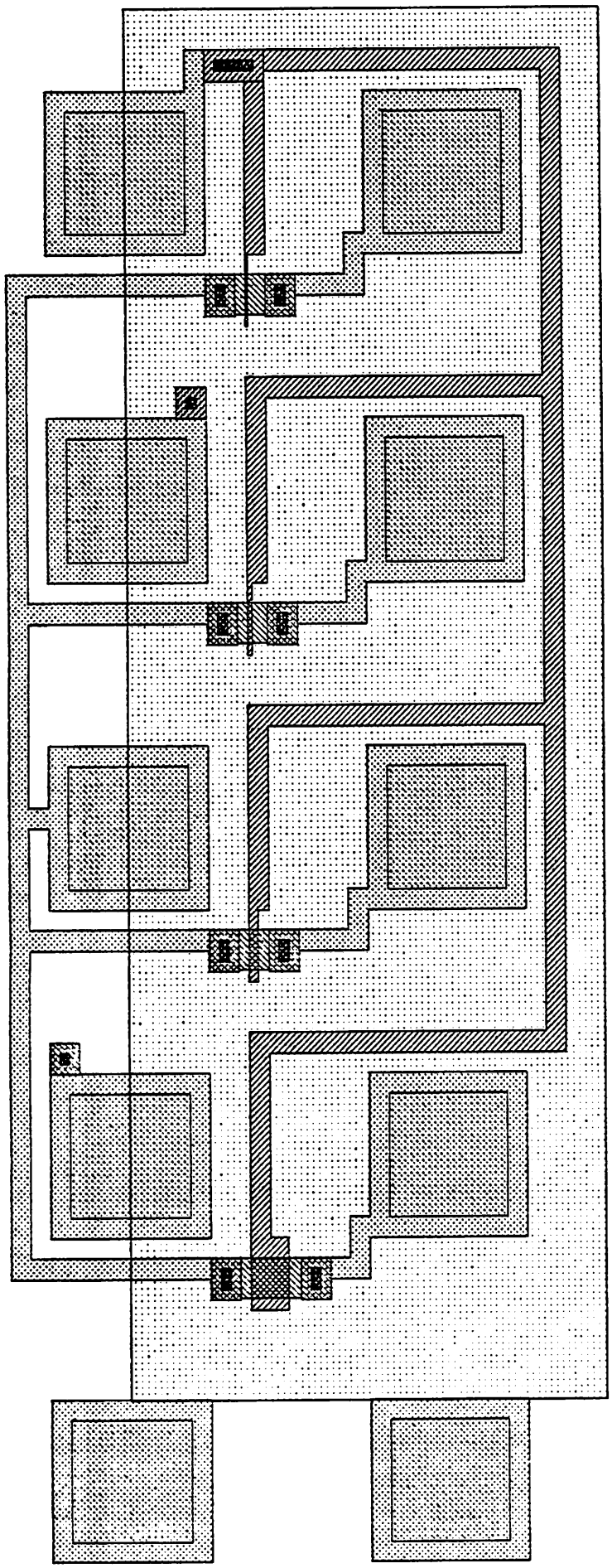
$$\frac{Z}{L} = \frac{4.8\mu m}{4.8\mu m}$$

fc2r2pmos.cif

pmos si gate
transistors

$$\frac{Z}{L} = \frac{4.8\mu m}{19.2\mu m}$$

$$\frac{Z}{L} = \frac{4.8\mu m}{38.4\mu m}$$



$$\frac{Z}{L} = \frac{19.2\mu m}{1.2\mu m}$$

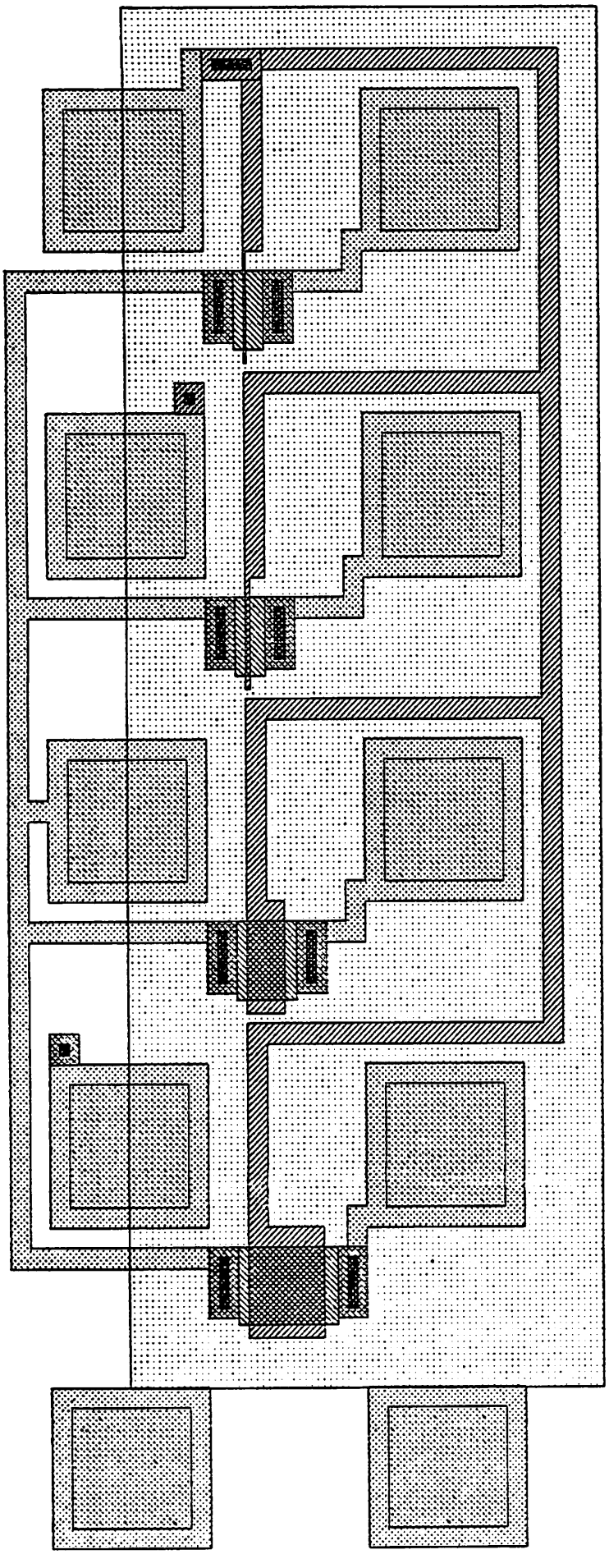
$$\frac{Z}{L} = \frac{19.2\mu m}{2.4\mu m}$$

fc3r2pmos.cif

pmos si gate transistors

$$\frac{Z}{L} = \frac{19.2\mu m}{4.8\mu m}$$

$$\frac{Z}{L} = \frac{19.2\mu m}{19.2\mu m}$$



cifplot* Window: Ø 16Ø -8ØØ Ø @ u=2ØØ --- Scale: 1 micron is Ø.Ø13 inches (33Øx)

$$\frac{Z}{L} = \frac{38.4\mu m}{1.2\mu m}$$

$$\frac{Z}{L} = \frac{38.4\mu m}{2.4\mu m}$$

fc3r2pmos.cif

pmos si gate transistors

$$\frac{Z}{L} = \frac{38.4\mu m}{19.2\mu m}$$

$$\frac{Z}{L} = \frac{38.4\mu m}{38.4\mu m}$$

$$\frac{Z}{L} = \frac{0.6\mu m}{1.2\mu m}$$

$$\frac{Z}{L} = \frac{0.6\mu m}{2.4\mu m}$$

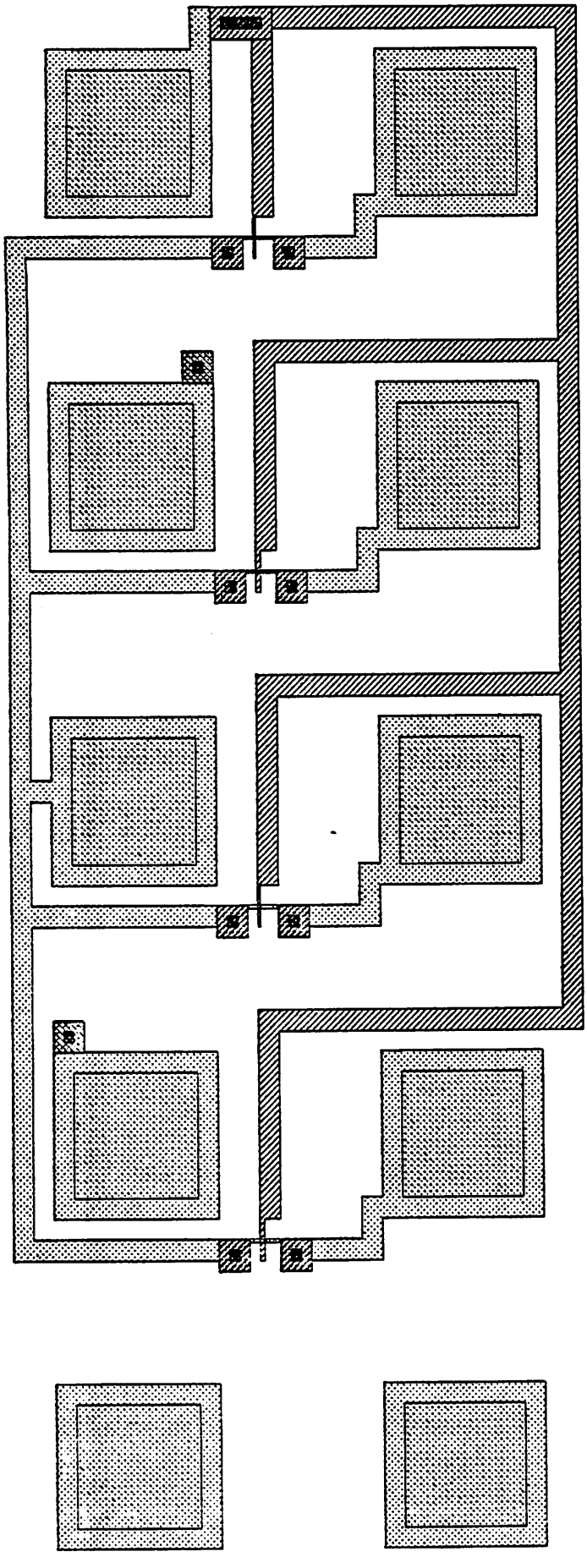
fc4r2nmos.cif

nmos si gate

transistors

$$\frac{Z}{L} = \frac{0.8\mu m}{1.2\mu m}$$

$$\frac{Z}{L} = \frac{0.8\mu m}{2.4\mu m}$$



cifplot* Window: Ø 16Ø -8ØØ Ø @ u=2ØØ --- Scale: 1 micron is Ø.Ø13 inches (33Øx)

$$\frac{Z}{L} = \frac{1\mu m}{1.2\mu m}$$

$$\frac{Z}{L} = \frac{1\mu m}{2.4\mu m}$$

fc4r2nmos.cif

nmos si gate transistors

$$\frac{Z}{L} = \frac{1.2\mu m}{1.2\mu m}$$

$$\frac{Z}{L} = \frac{1.2\mu m}{2.4\mu m}$$

$$\frac{Z}{L} = \frac{2.4\mu m}{0.6\mu m}$$

$$\frac{Z}{L} = \frac{2.4\mu m}{0.8\mu m}$$

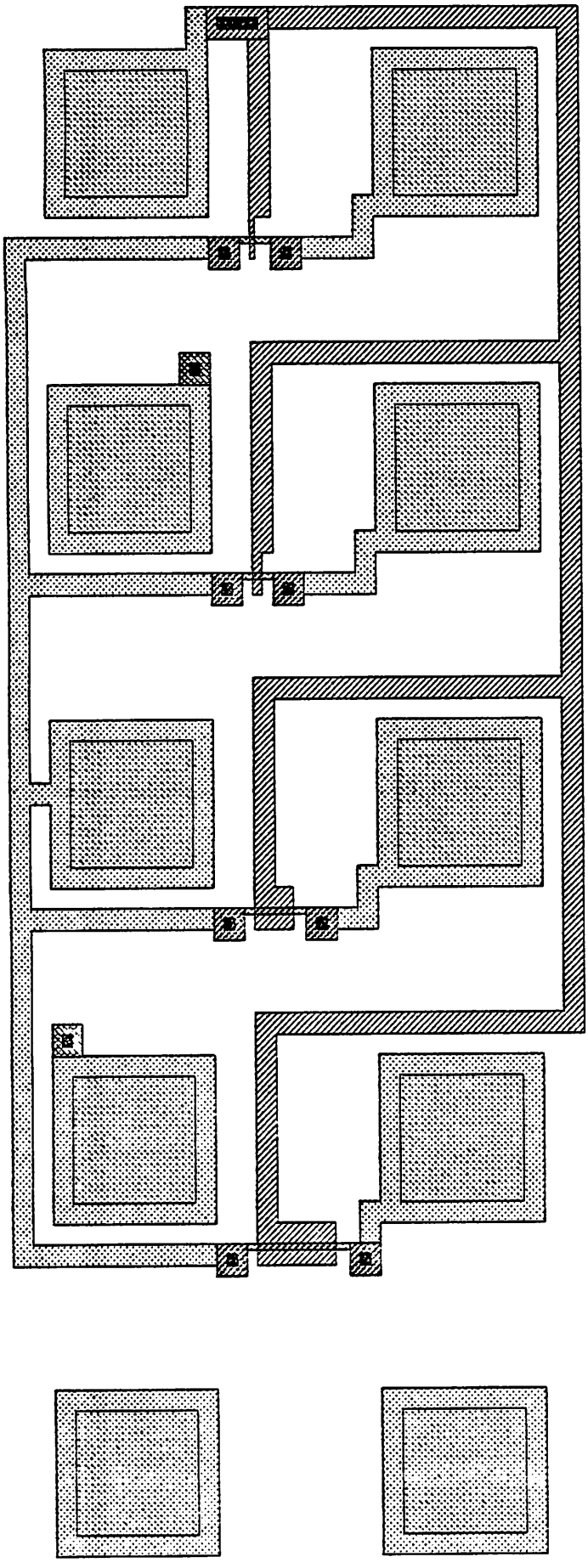
fr5r2nmos.cif

nmos si gate transistors

$$\frac{Z}{L} = \frac{2.4\mu m}{1\mu m}$$

$$\frac{Z}{L} = \frac{2.4\mu m}{1.2\mu m}$$

clfplot* dow: 0 160 -800 0 0 u=200 --- Scale: 1 micron is 0. Inches (330x)



cifplot* Window: @ 160 -800 @ @ u=200 --- Scale: 1 micron is @.013 inches (330x)

$$\frac{Z}{L} = \frac{2.4\mu m}{2.4\mu m}$$

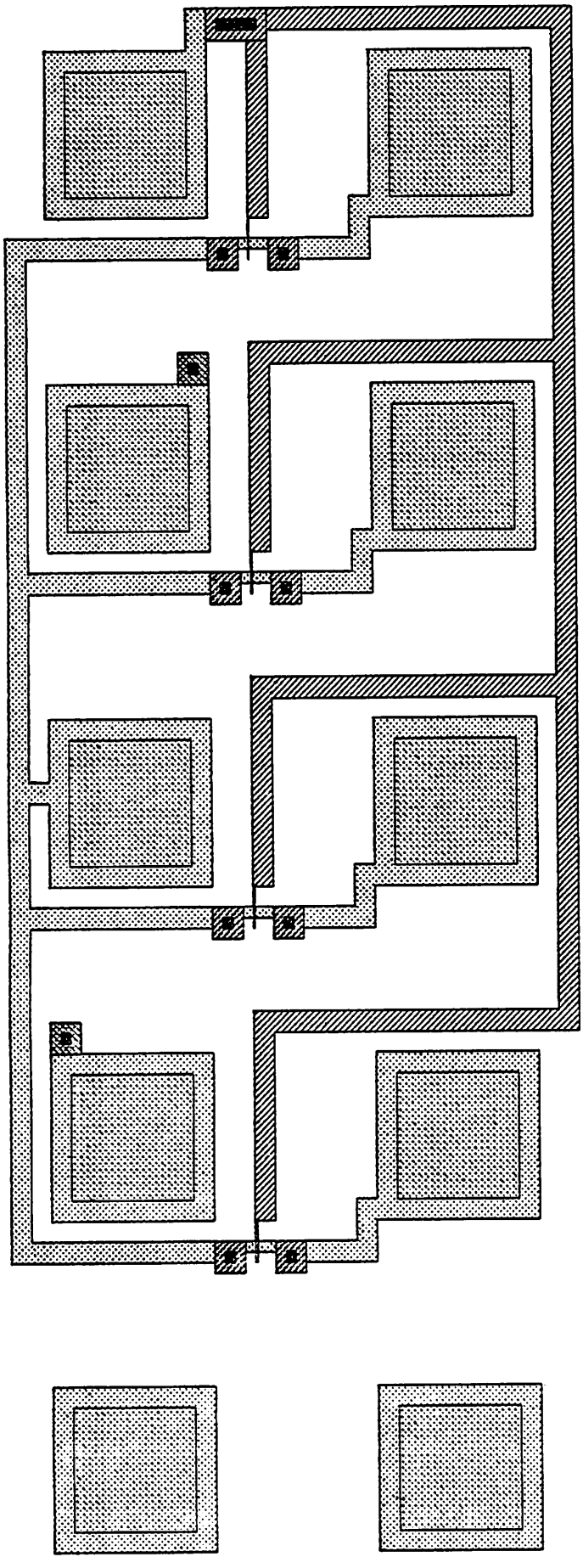
$$\frac{Z}{L} = \frac{2.4\mu m}{4.8\mu m}$$

fr5r2nmos.cif

nmos si gate transistors

$$\frac{Z}{L} = \frac{2.4\mu m}{19.2\mu m}$$

$$\frac{Z}{L} = \frac{2.4\mu m}{38.4\mu m}$$



$$\frac{Z}{L} = \frac{4.8\mu m}{0.6\mu m}$$

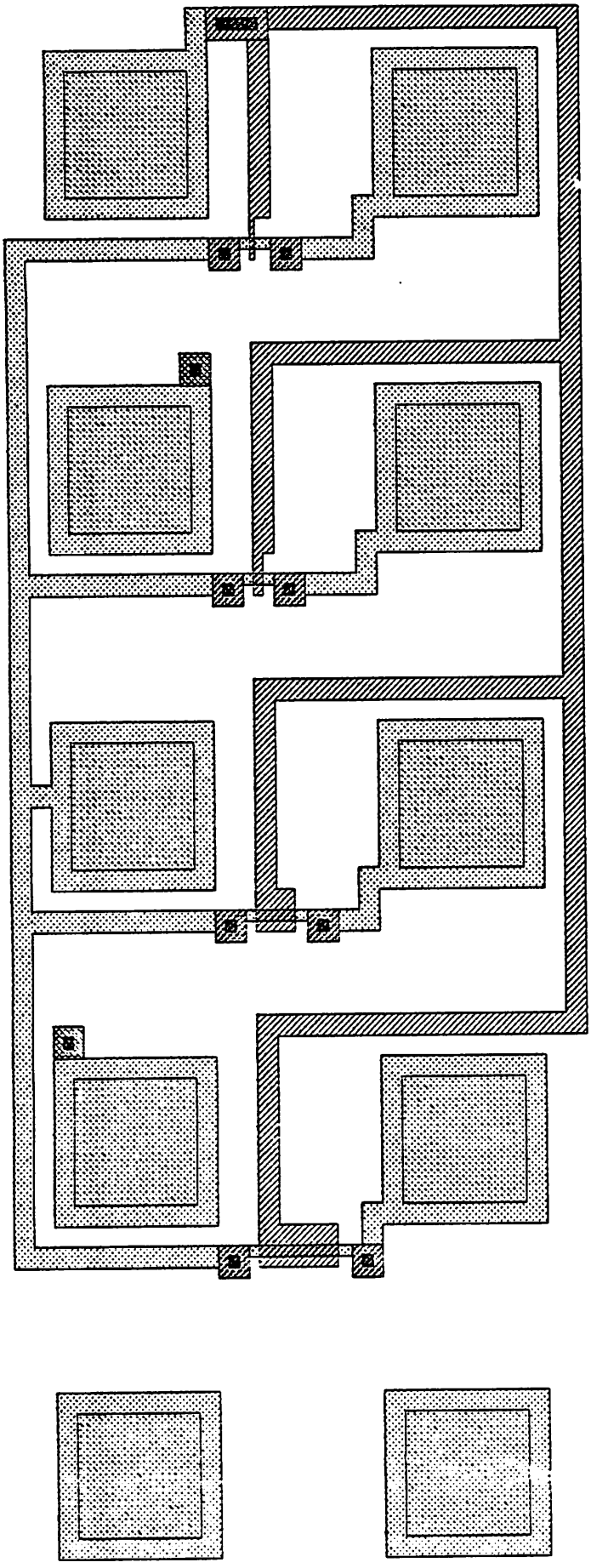
$$\frac{Z}{L} = \frac{4.8\mu m}{0.8\mu m}$$

fc6r2nmos.cif

nmos Si gate transistor

$$\frac{Z}{L} = \frac{4.8\mu m}{1\mu m}$$

$$\frac{Z}{L} = \frac{4.8\mu m}{1.2\mu m}$$



$$\frac{Z}{L} = \frac{4.8\mu m}{2.4\mu m}$$

$$\frac{Z}{L} = \frac{4.8\mu m}{4.8\mu m}$$

fc6r2nmos.cif

nmos Si gate transistor

$$\frac{Z}{L} = \frac{4.8\mu m}{19.2\mu m}$$

$$\frac{Z}{L} = \frac{4.8\mu m}{38.4\mu m}$$

cifplot* ndow: Ø 160 -800 Ø @ u=200 --- Scale: 1 micron is Ø 3 inches (330x)

$$\frac{Z}{L} = \frac{19.2\mu m}{1.2\mu m}$$

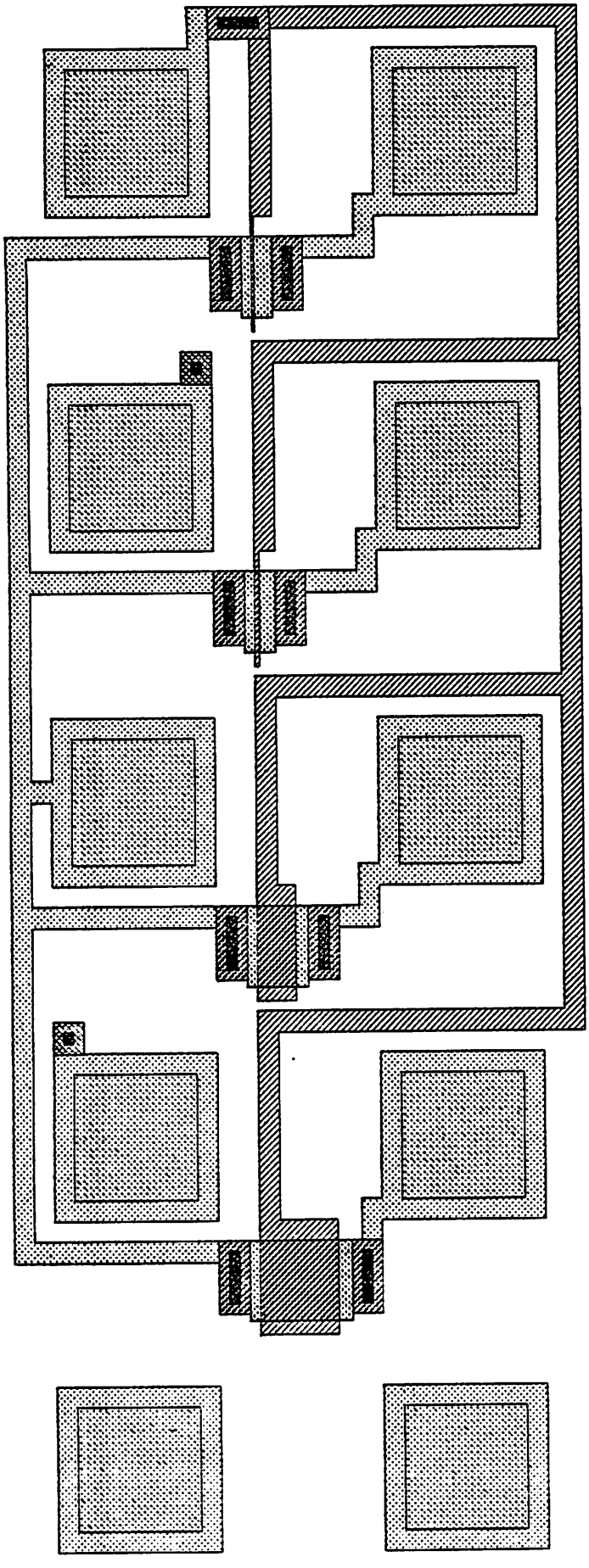
$$\frac{Z}{L} = \frac{19.2\mu m}{2.4\mu m}$$

fc7r2nmos.cif

nmos si gate transistors

$$\frac{Z}{L} = \frac{19.2\mu m}{4.8\mu m}$$

$$\frac{Z}{L} = \frac{19.2\mu m}{19.2\mu m}$$



clfplot* Window: Ø 160 -800 Ø Ø u=200 --- Scale: 1 micron is Ø.Ø13 inches (330x)

$$\frac{Z}{L} = \frac{38.4\mu m}{1.2\mu m}$$

$$\frac{Z}{L} = \frac{38.4\mu m}{2.4\mu m}$$

fc7r2nmos.cif

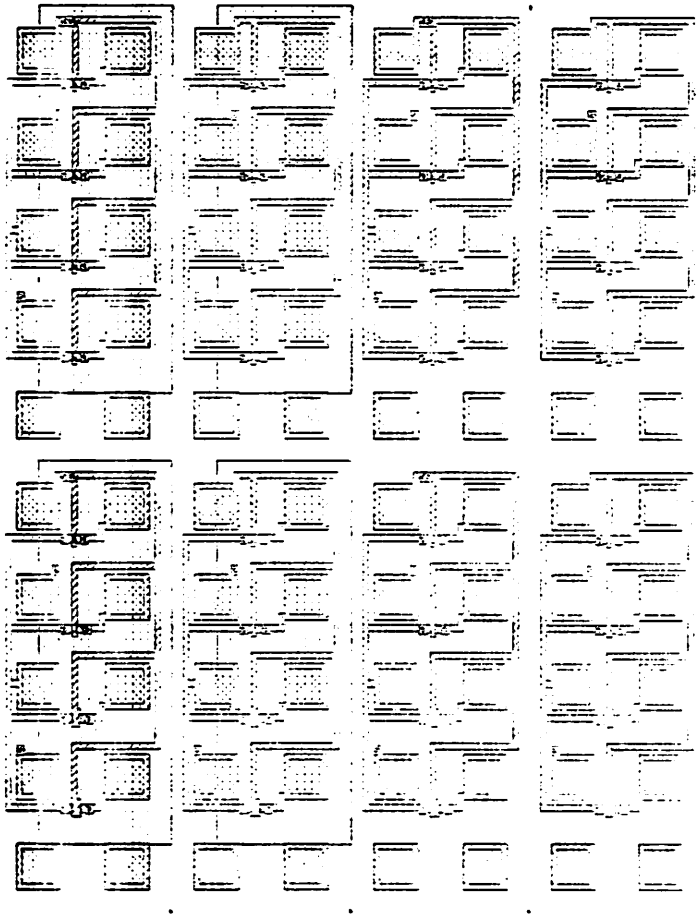
nmos si gate
transistors

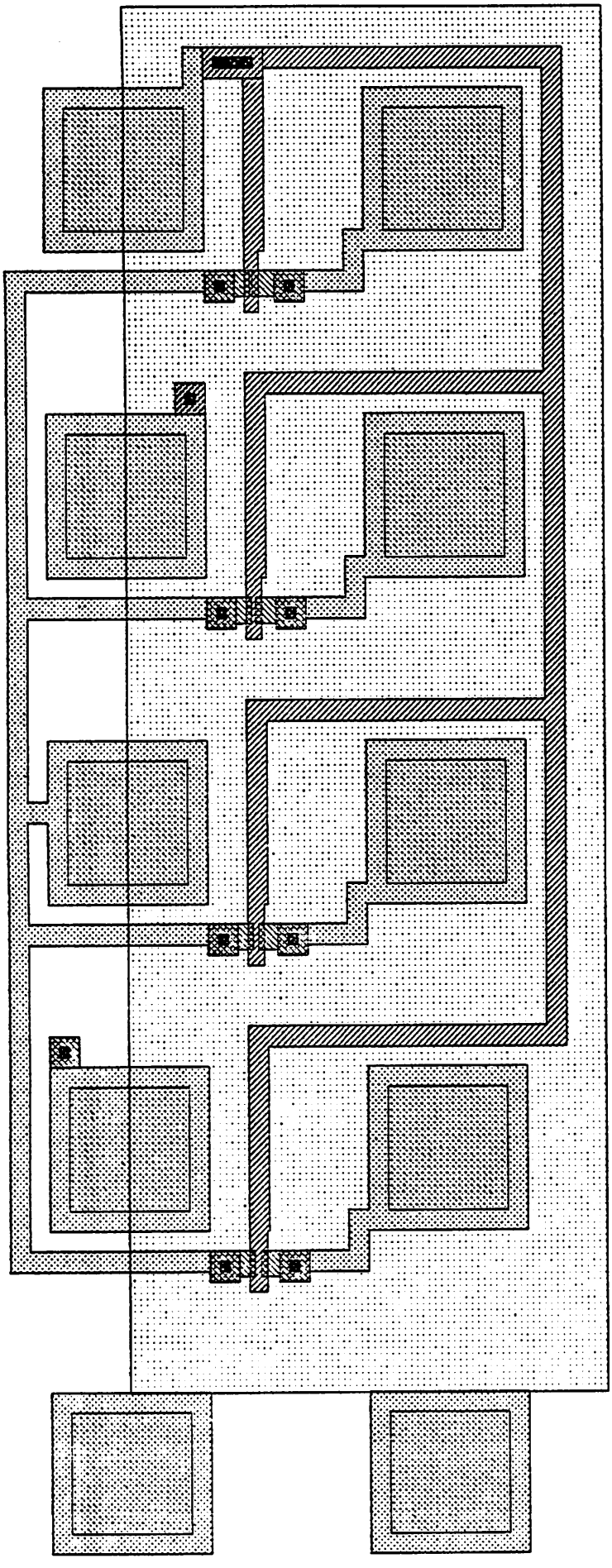
$$\frac{Z}{L} = \frac{38.4\mu m}{19.2\mu m}$$

$$\frac{Z}{L} = \frac{38.4\mu m}{38.4\mu m}$$

DETAILED FLOOR PLAN
MOS FIELD TRANSISTORS

fc4r1pfsi	fc5r1pfal	fc6r1nfsi	fc7r1nfal
$\frac{Z}{L}(\mu m)$	$\frac{Z}{L}(\mu m)$	$\frac{Z}{L}(\mu m)$	$\frac{Z}{L}(\mu m)$
12/1.2	12/1.2	12/1.2	12/1.2
12/1.8	12/1.8	12/1.8	12/1.8
12/2.4	12/2.4	12/2.4	12/2.4
12/3	12/3	12/3	12/3
12/3.6	12/3.6	12/3.6	12/3.6
12/4.8	12/4.8	12/4.8	12/4.8
12/9.6	12/9.6	12/9.6	12/9.6
12/12	12/12	12/12	12/12





clfplot* Window: Ø 160 -800 Ø 0 u=200 --- Scale: 1 micron is Ø.Ø13 inches (330x)

$$\frac{Z}{L} = \frac{12\mu m}{1.2\mu m}$$

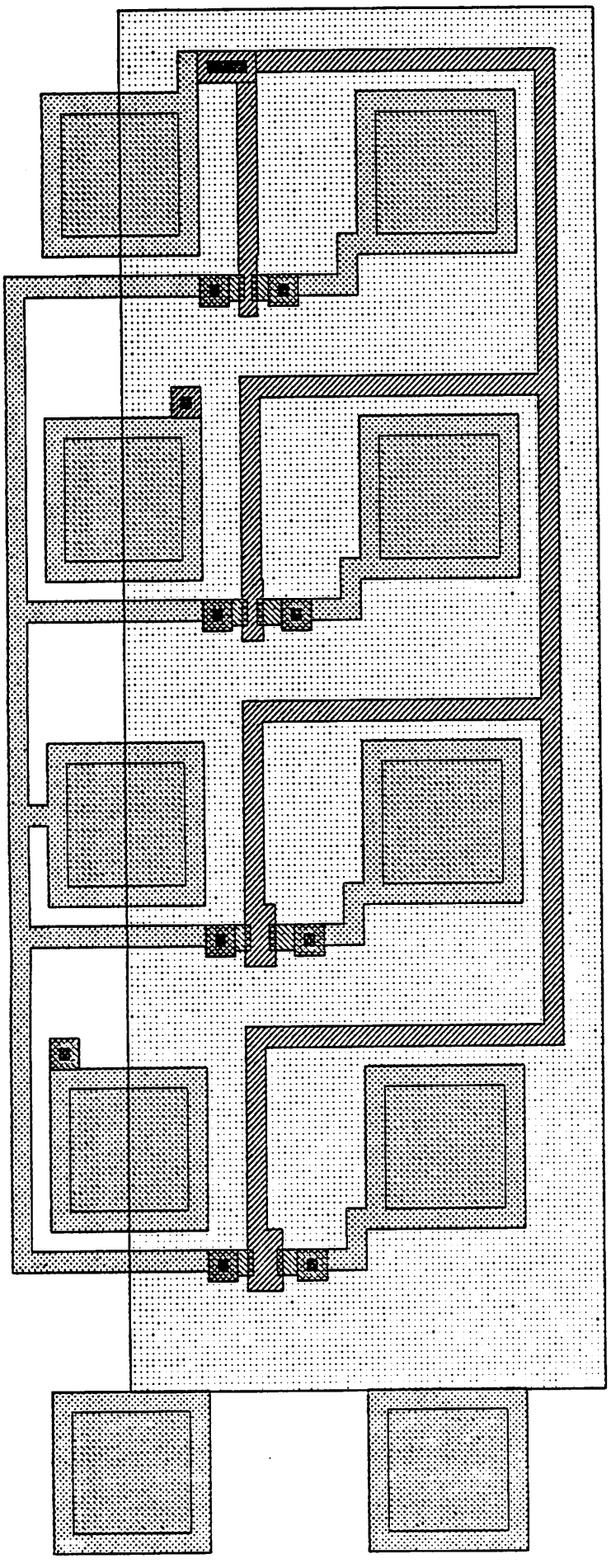
$$\frac{Z}{L} = \frac{12\mu m}{1.8\mu m}$$

fc4r1pfsi.cif

pmos field tran.
with Si gate

$$\frac{Z}{L} = \frac{12\mu m}{2.4\mu m}$$

$$\frac{Z}{L} = \frac{12\mu m}{3\mu m}$$



$$\frac{Z}{L} = \frac{12\mu m}{3.6\mu m}$$

$$\frac{Z}{L} = \frac{12\mu m}{4.8\mu m}$$

fc4r1pfsi.cif

pmos field tran.
with Si gate

$$\frac{Z}{L} = \frac{12\mu m}{9.6\mu m}$$

$$\frac{Z}{L} = \frac{12\mu m}{12\mu m}$$

cifplot* Window: 0 160 -800 0 @ u=200 --- Scale: 1 micron is 0.013 inches (330x)

$$\frac{Z}{L} = \frac{12\mu m}{1.2\mu m}$$

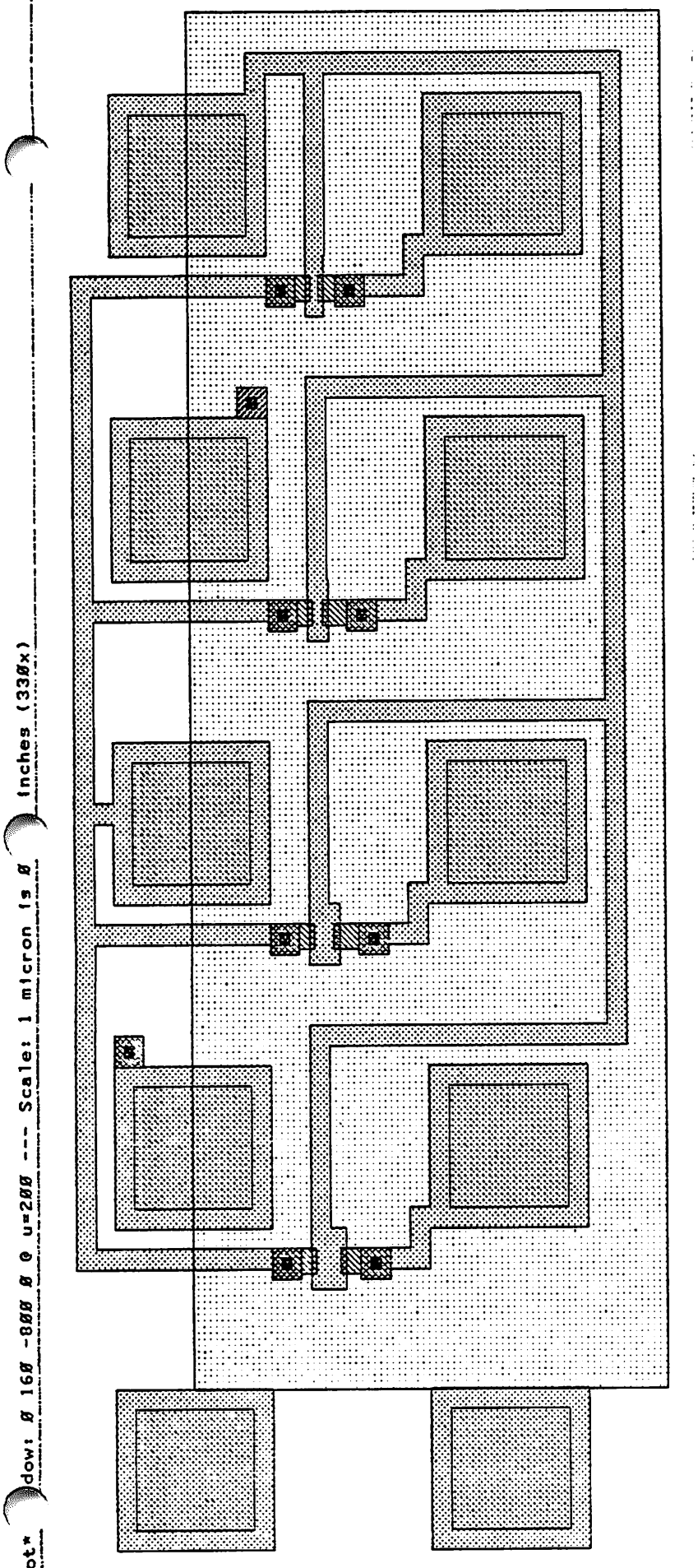
$$\frac{Z}{L} = \frac{12\mu m}{1.8\mu m}$$

fc5r1pfal.cif

pmos field tran.
with Al gate

$$\frac{Z}{L} = \frac{12\mu m}{2.4\mu m}$$

$$\frac{Z}{L} = \frac{12\mu m}{3\mu m}$$



$$\frac{Z}{L} = \frac{12\mu m}{3.6\mu m}$$

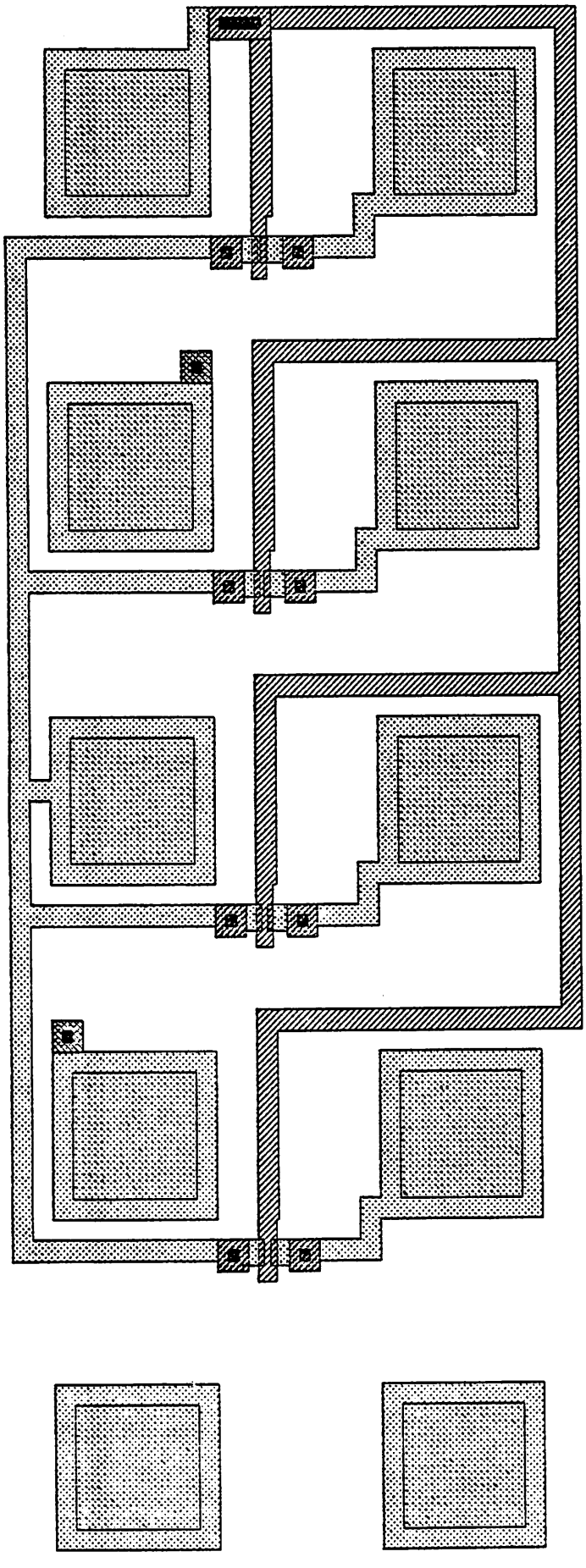
$$\frac{Z}{L} = \frac{12\mu m}{4.8\mu m}$$

fc5r1pfal.cif

pmos field tran.
with Al gate

$$\frac{Z}{L} = \frac{12\mu m}{9.6\mu m}$$

$$\frac{Z}{L} = \frac{12\mu m}{12\mu m}$$



$$\frac{Z}{L} = \frac{12\mu m}{1.2\mu m}$$

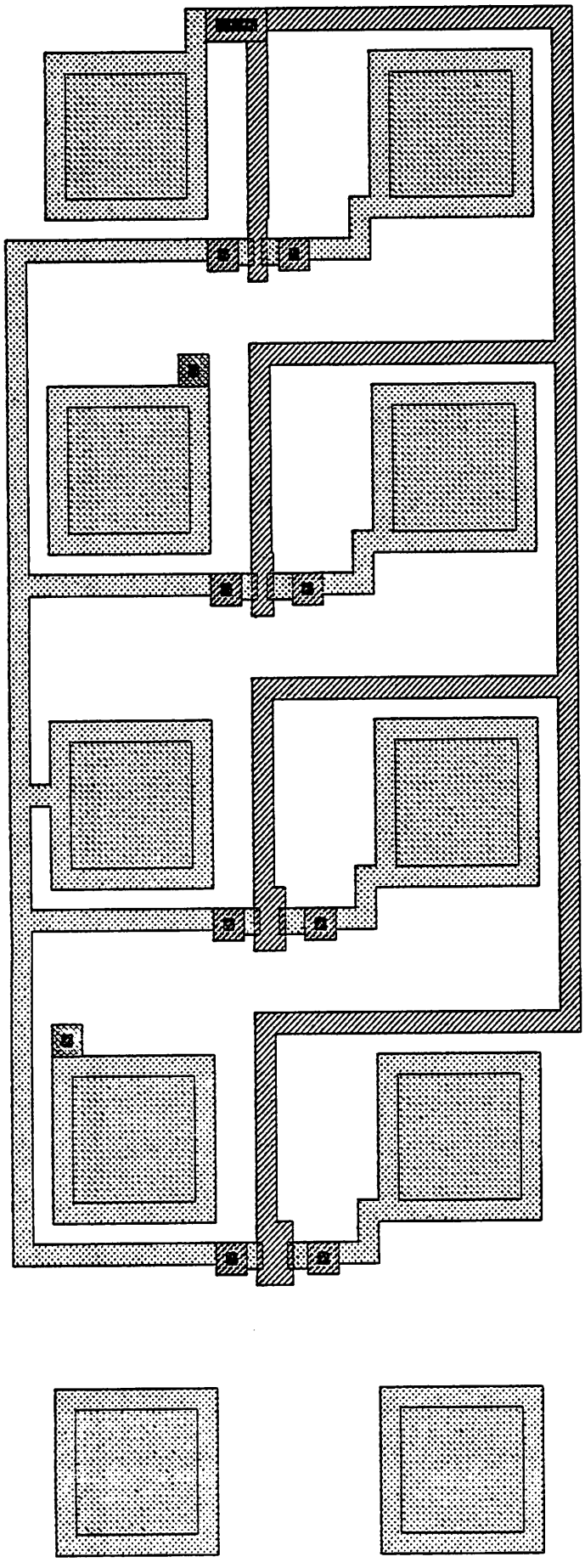
$$\frac{Z}{L} = \frac{12\mu m}{1.8\mu m}$$

fc6r1nfsi.cif

nmos field tran.
with Si gate

$$\frac{Z}{L} = \frac{12\mu m}{2.4\mu m}$$

$$\frac{Z}{L} = \frac{12\mu m}{3\mu m}$$



$$\frac{Z}{L} = \frac{12\mu m}{3.6\mu m}$$

$$\frac{Z}{L} = \frac{12\mu m}{4.8\mu m}$$

fc6r1nfsi.cif

nmos field tran.
with Si gate

$$\frac{Z}{L} = \frac{12\mu m}{9.6\mu m}$$

$$\frac{Z}{L} = \frac{12\mu m}{12\mu m}$$

clfplot* Window: 0 160 -800 0 0 u=200 --- Scale: 1 micron is 0.013 inches (330x)

$$\frac{Z}{L} = \frac{12\mu m}{1.2\mu m}$$

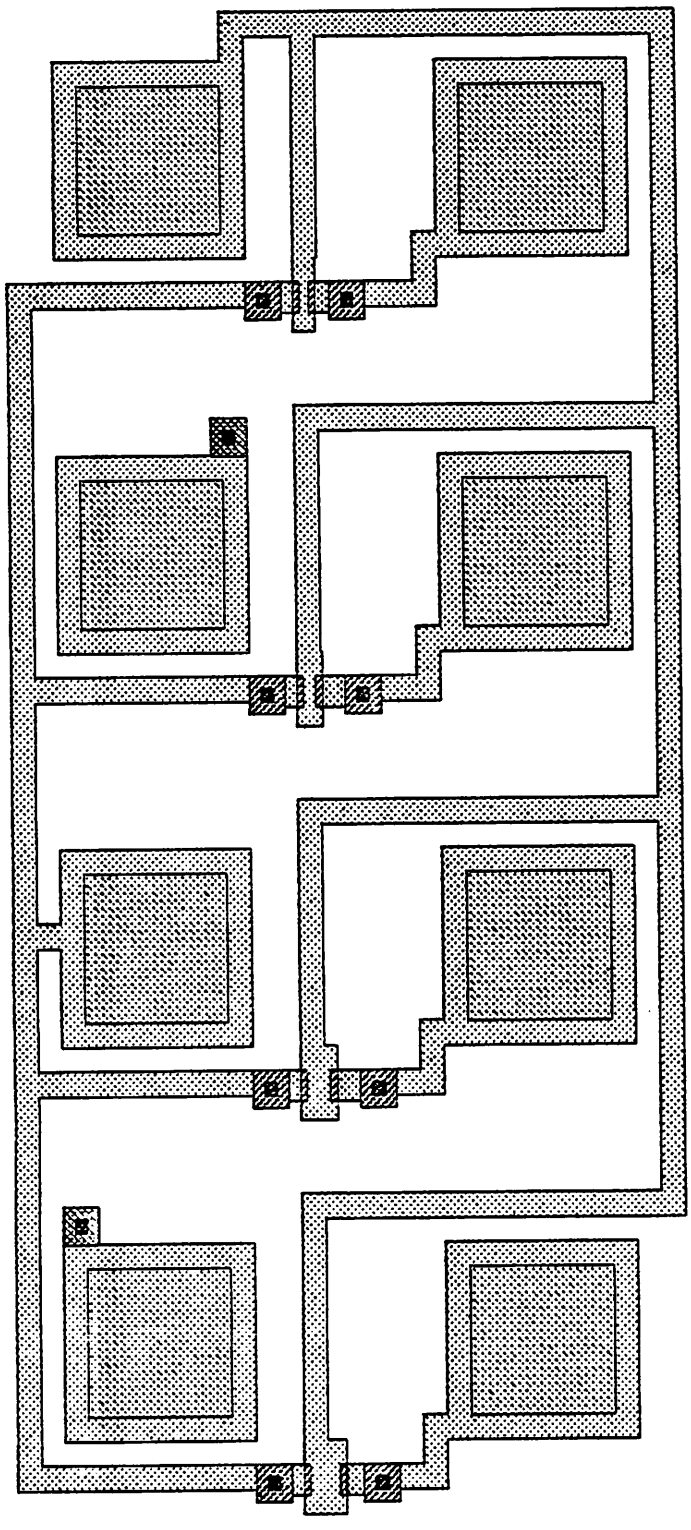
$$\frac{Z}{L} = \frac{12\mu m}{1.8\mu m}$$

fc7r1nfal.cif

nmos field tran.
with Al gate

$$\frac{Z}{L} = \frac{12\mu m}{2.4\mu m}$$

$$\frac{Z}{L} = \frac{12\mu m}{3\mu m}$$



$$\frac{Z}{L} = \frac{12\mu m}{3.6\mu m}$$

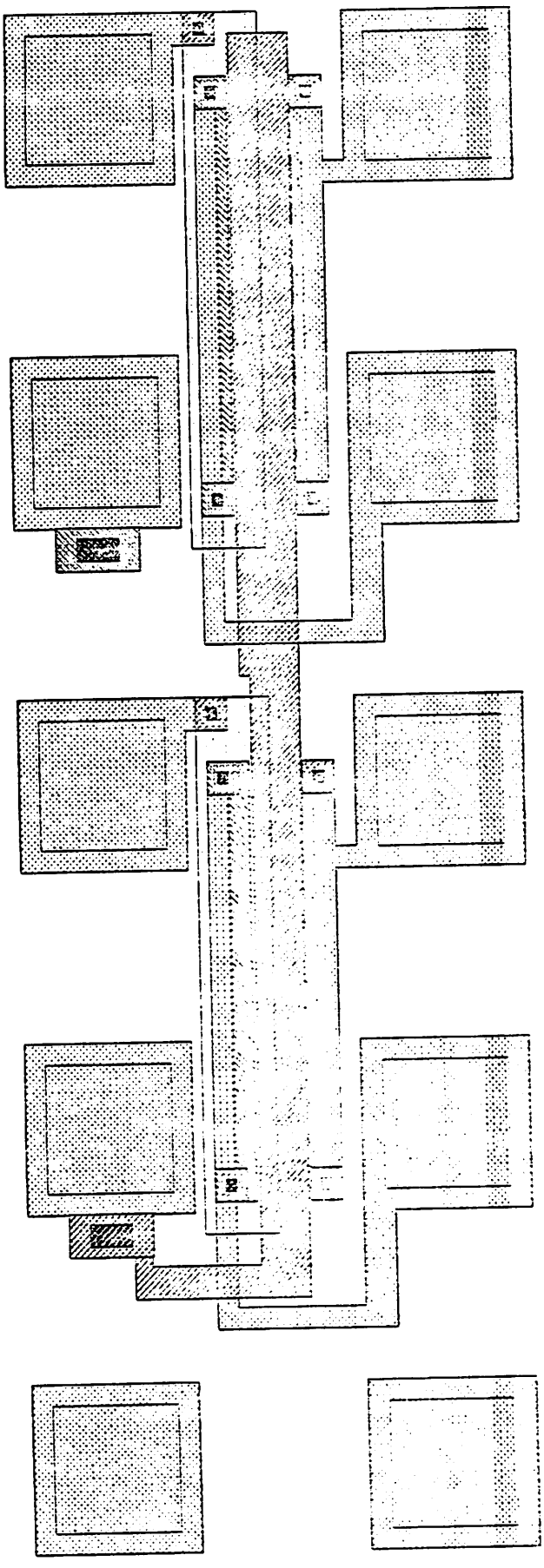
$$\frac{Z}{L} = \frac{12\mu m}{4.8\mu m}$$

fc7r1nfal.cif

nmos field tran.
with Al gate

$$\frac{Z}{L} = \frac{12\mu m}{9.6\mu m}$$

$$\frac{Z}{L} = \frac{12\mu m}{12\mu m}$$



fc4r1pfsi.cif

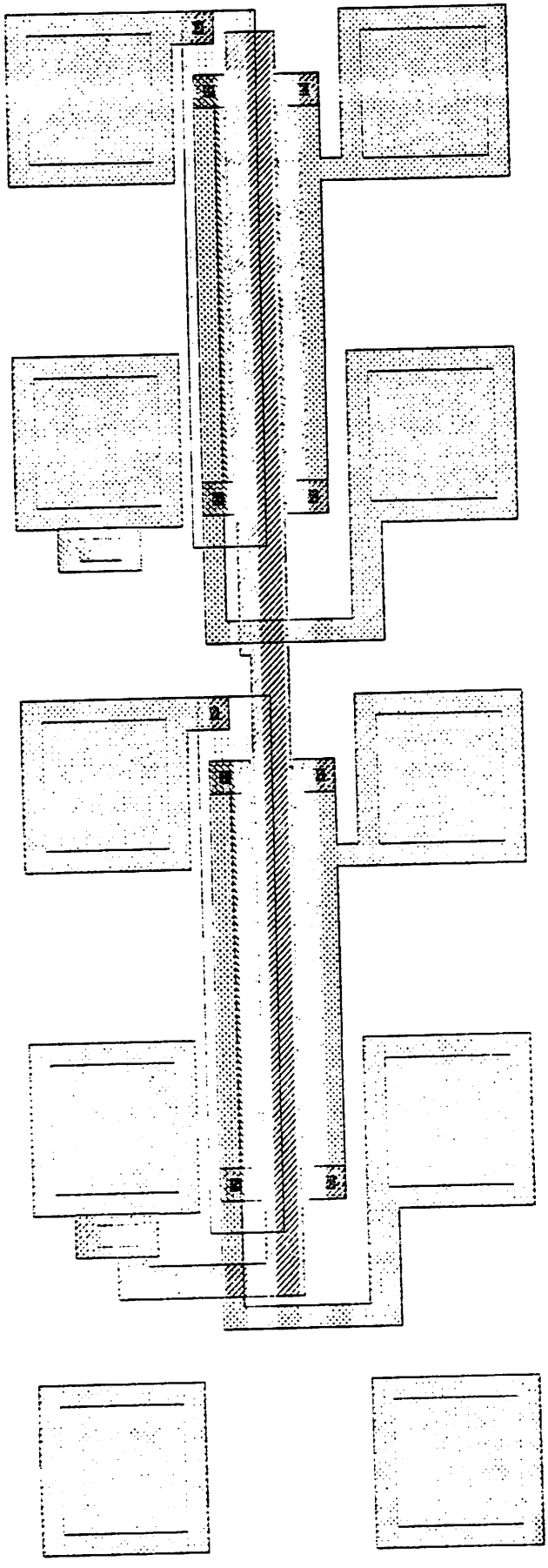
pmos field
si gate trans.

fc4r1pfsi.cif

pmos field
si gate trans.

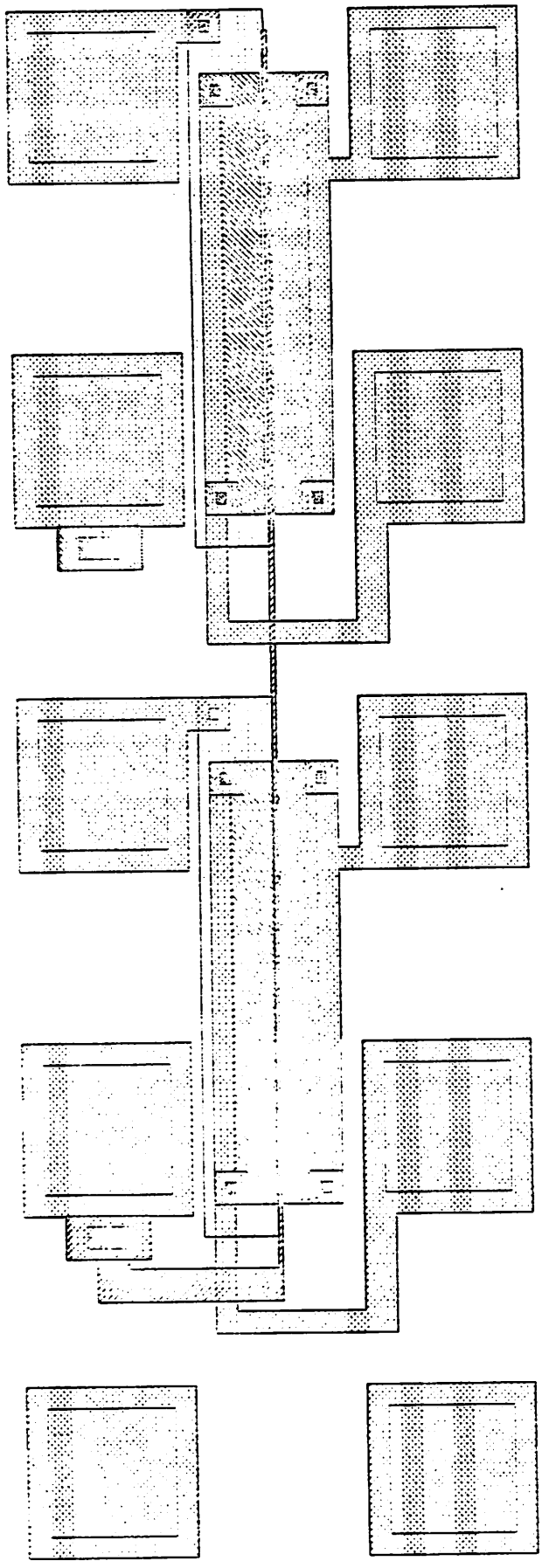
fc5r1pfal.cif

pmos field
Al gate trans.



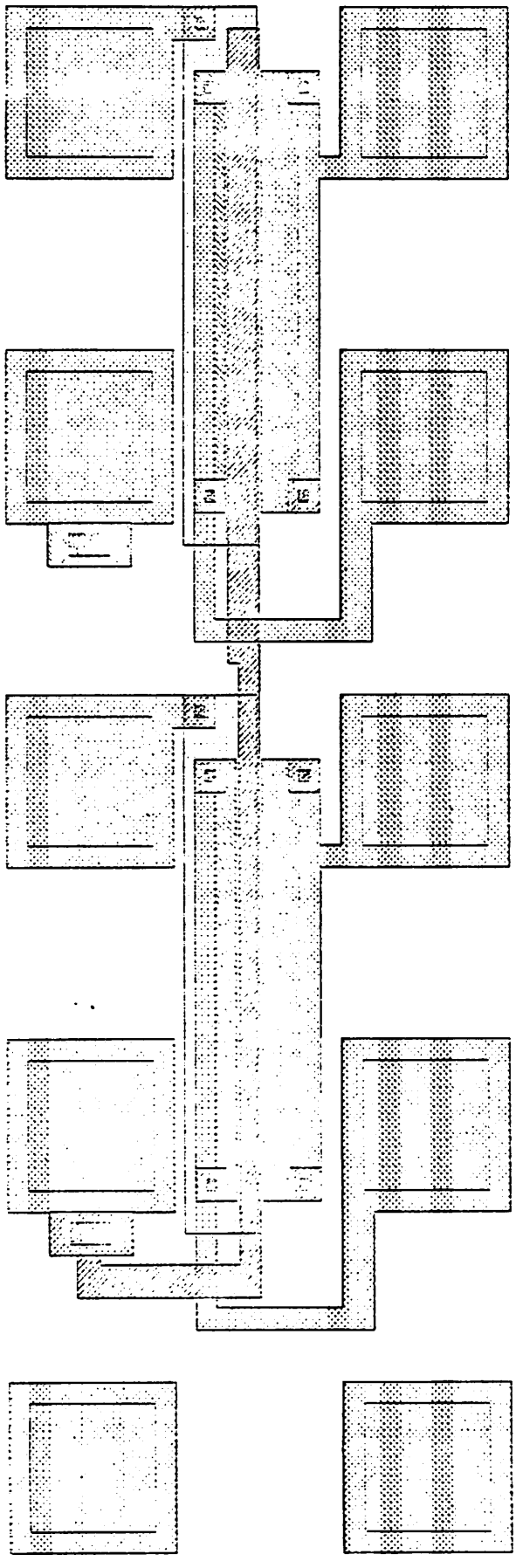
fc5r1pfal.cif

pmos field
Al gate trans.



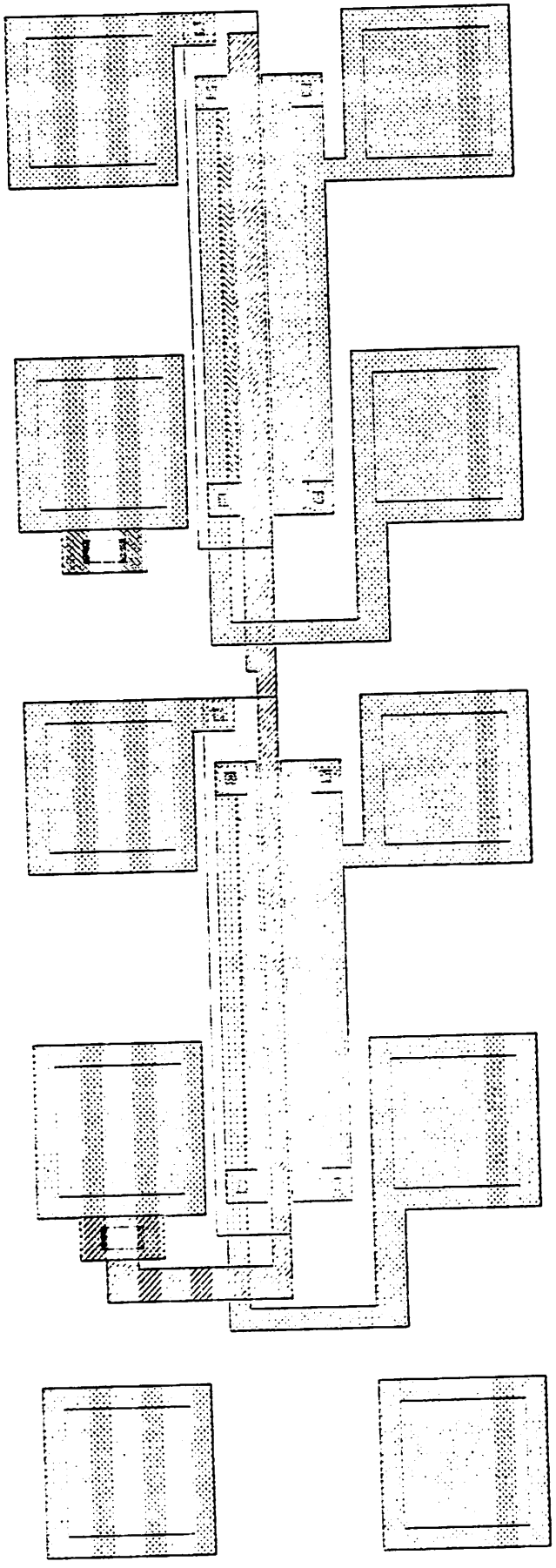
fc6r1nfsi.cif

nmos field
si gate trans.



fc6r1nfsi.cif

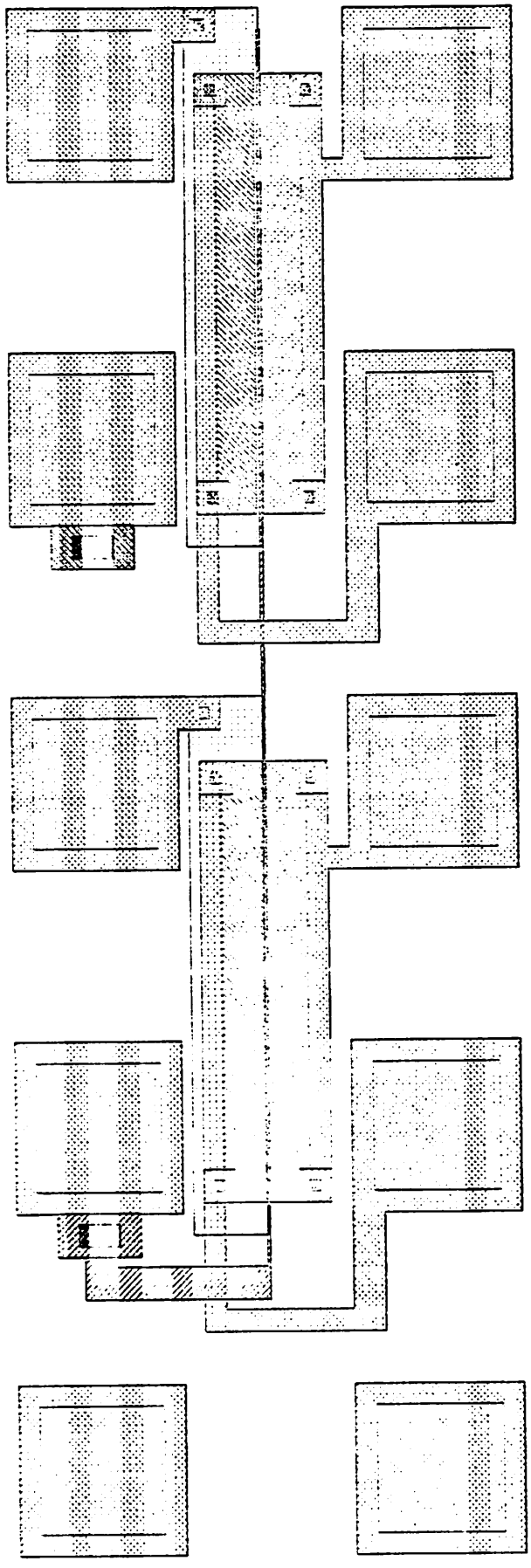
nmos field
si gate trans.



fc7r1nfal.cif

nmos field

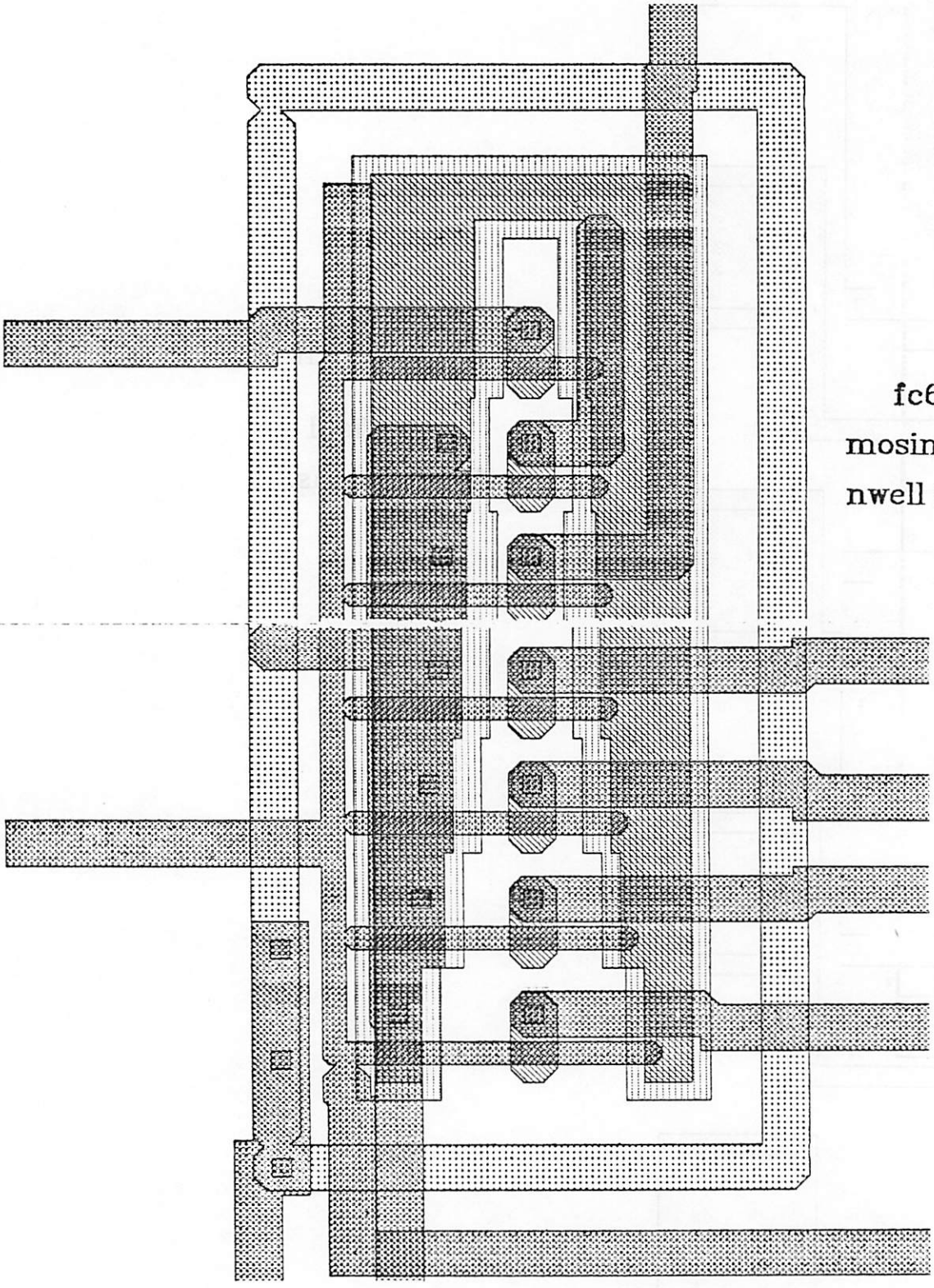
Al gate trans.



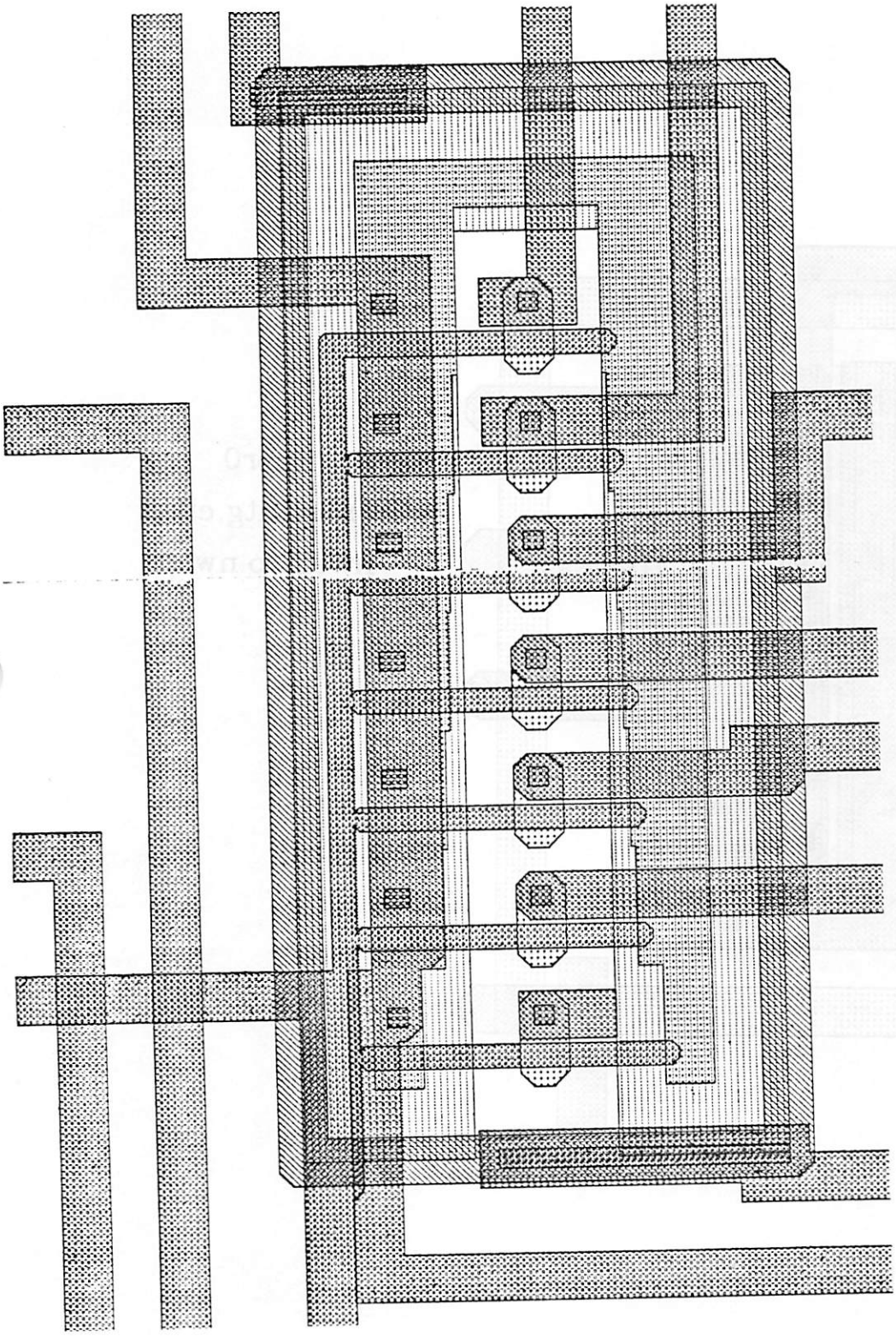
fc7r1nfal.cif

nmos field

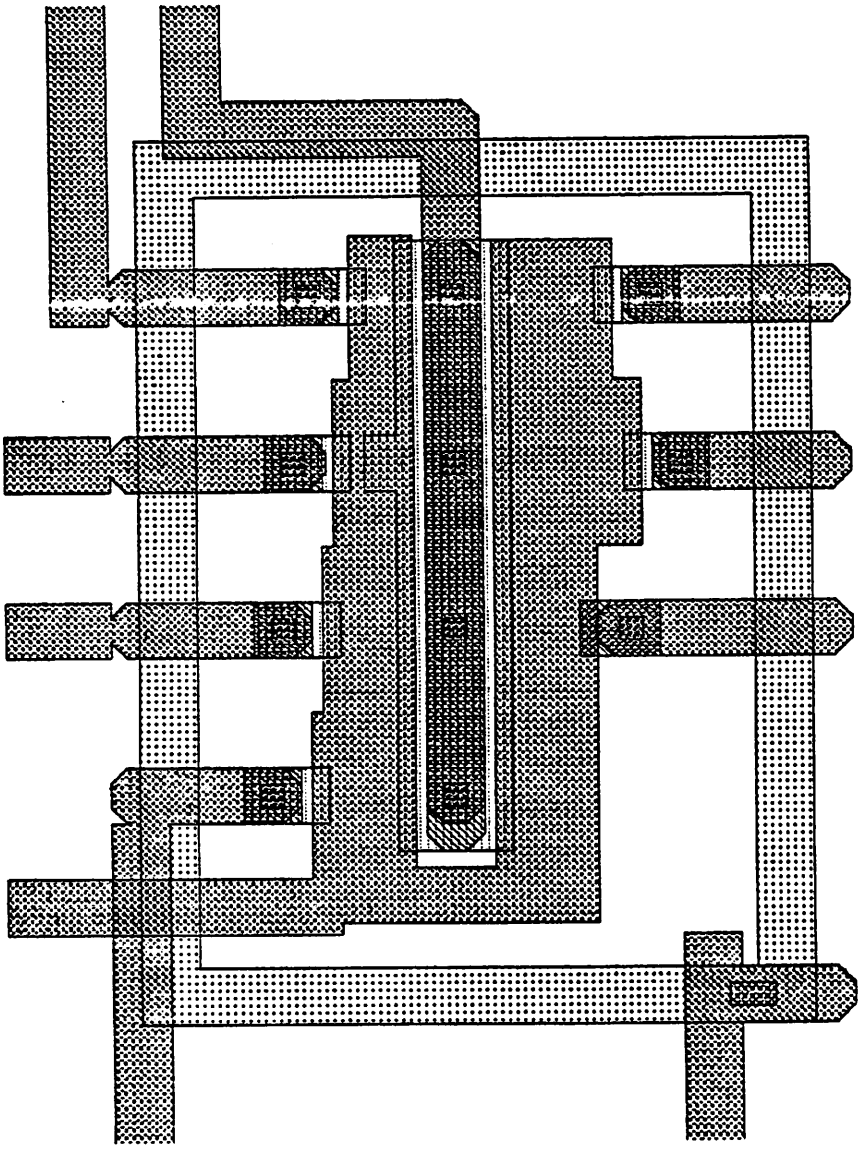
Al gate trans.



fc6r0
mosintg.cif
nwell to n+



fc6r0
mosintg.cif
p+ to p-



fc6r0
mosintg.cif
nwell to nwell

Device Test Pattern (fsubchip)
Cif File Cell Hierarchy

PAD.k

PADSET.k
  PAD.k

altern.k

alterp.k
  littlun.k

bjtintg.k
  altern.k alterp.k

f.psiwn.m.k

f.psiwp.m.k

f.pwwsi.k

fc0r2pmos.k
  nwellbase.k pcontact.k

fc1r2pmos.k
  nwellbase.k pcontact.k

fc2r2pmos.k
  nwellbase.k pcontact.k

fc3r2pmos.k
  nwellbase.k pcontact.k

fc4r1pfsi.k
  nwellbase.k pcontact.k

fc4r2nmos.k
  ncontact.k psubbase.k

fc5r1pfal.k
  nwellfbase.k pcontact.k

fc5r2nmos.k
  ncontact.k psubbase.k

fc6r1nfsi.k
  ncontact.k psubbase.k

fc6r2nmos.k
  ncontact.k psubbase.k

fc7r1nfal.k
  ncontact.k psubfbase.k

fc7r2nmos.k
  ncontact.k psubbase.k

fsubchip.k
  fc0r2pmos.k fc1r2pmos.k fc2r2pmos.k fc3r2pmos.k
  fc4r1pfsi.k fc4r2nmos.k fc5r1pfal.k fc5r2nmos.k
  fc6r1nfsi.k fc6r2nmos.k fc7r1nfal.k fc7r2nmos.k
  mosbjtintg.k

latchup.k

littlun.k
  PADSET.k quadlatch.k

mosbjtintg.k
  bjtintg.k mosintg.k

mosintg.k
  PADSET.k f.psiwn.m.k f.psiwp.m.k
  f.pwwsi.k polymetl.k

ncontact.k

nwellbase.k
  PADSET.k ncontact.k pcontact.k

nwellfbase.k
  PADSET.k ncontact.k pcontact.k

pcontact.k

polymetl.k

psubbase.k
  PADSET.k ncontact.k pcontact.k

psubfbase.k
  PADSET.k ncontact.k pcontact.k

quadlatch.k
  latchup.k

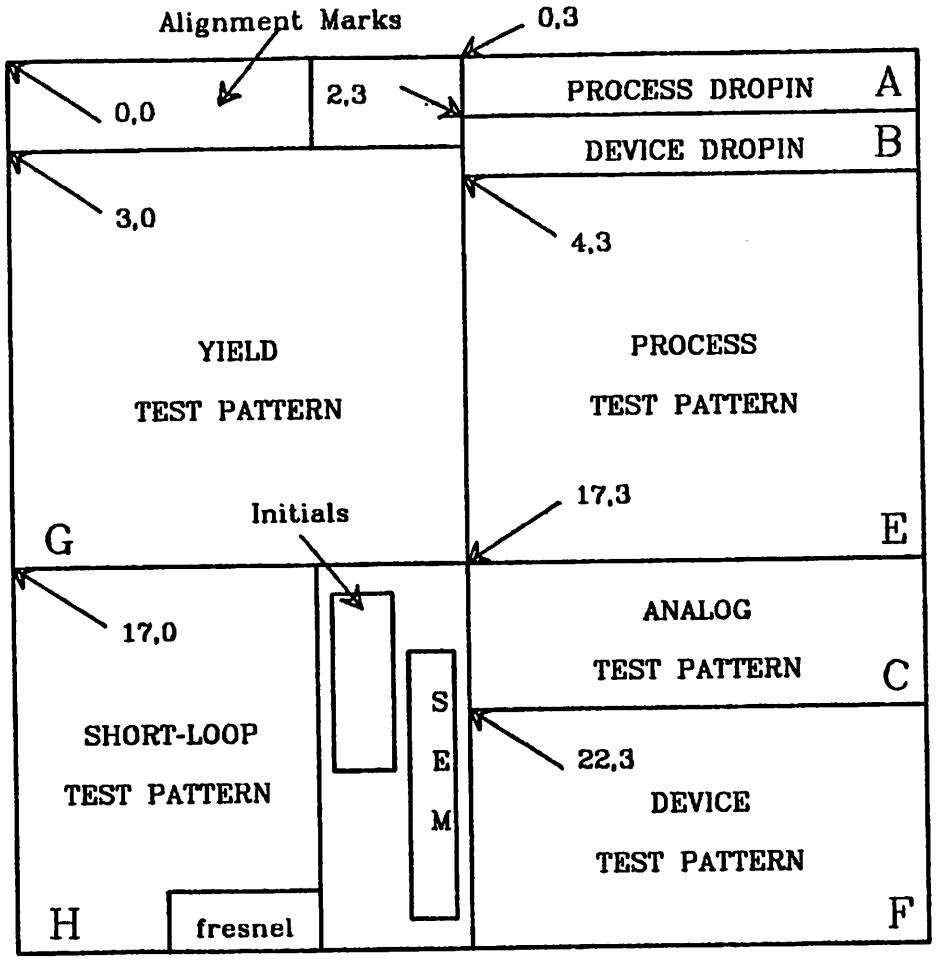
EE290 TEST CHIP ORGANIZATION

The EE290 test chip is made up of 7 Test Patterns plus a separate section for alignment marks. The 7 Test Patterns are: Device, Device Drop-in, Process, Process Drop-in, Shortloop, Yield, and Analog. Each test pattern consists of a collection of functional units. A functional unit is made up of several blocks which together accomplish a specific goal. These blocks are 320um x 1600um. Each block may contain a 2 x 10 array of 80um pads on 160um centers. A block does not always contain all 20 pads since some test structures require a large area, however the pads which are present will remain on the 160um grid. The pad numbering convention is shown below. Pad #1 contains a small notch in it to help distinguish top from bottom when viewing the chip through a microscope. The entire EE290 chip is a 6 row, 30 column array of blocks.

1	11
2	12
3	13
4	14
5	15
6	16
7	17
8	18
9	19
10	20

The testing of the devices can be accomplished with a 2 x 5 probe card. Some of the test patterns must be tested with a 2 x 10 probe card due to unconventional pad assignments and the inability to constrain the test structure to a 2 x 5 sub-block.

BERKELEY CMOS PROCESS TEST CHIP



testchip.cif

Entire EE290 Test Chip