NEGATIVE RESISTANCE CURVE TRACER

by

L. O. Chua and G-Q. Zhong

Memorandum No. UCB/ERL M84/29

9 April 1984

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

NEGATIVE RESISTANCE CURVE TRACER[†]

Leon O. Chua and Guo-Qun Zhong[††]

Department of Electrical Engineering and Computer Sciences
and the Electronics Research Laboratory
University of California, Berkeley, CA 94720

Abstract

Tracing the negative resistance characteristics of 2-terminal and 3-terminal devices often ended in failure due to jump phenomenon, hysteresis, and oscillation resulting from the tracing circuit. All of these problems are overcome in the curve tracer described in this paper. A detailed nonlinear dynamic circuit analysis is used to develop a simple method for quenching oscillations and other exotic phenomena.

Our curve tracer is designed to trace either voltage-controlled or current-controlled negative resistance characteristics of both 2-terminal and 3-terminal devices. All six representations which completely characterized a 3-terminal or 2-port nonlinear resistor are allowed. In particular, using a novel approach for implementing a nullator and norator, transmission (chain) characteristics of 3-terminal and 2-port devices have been successfully traced for the first time.

[†]Research sponsored in part by the Office of Naval Research under Contract N00014-76-C-0572 and National Science Foundation Grant ECS-8313278.

[††]Guo-Qun Zhong is a visiting scholar at the University of California, Berkeley, on leave from Guangzhou Research Institute of Electronic Technology, Academia Sinica. Guangzhou, People's Republic of China.

1. INTRODUCTION

A 2-terminal negative resistance device (Fig. 1(a)) is one whose voltage versus current (v-i) characteristics exhibits a negative slope over some region of the device's operating range. Since the v-i characteristic of any physical device must eventually lie in the first and third quadrant (i.e., they must be eventually passive) even if the device is biased by batteries,† a 2-terminal negative-resistance device characteristic is either voltage-controlled (type N) as shown by the hypothetical curve in Fig. 1(b), or current-controlled (type S) as shown by the hypothetical curve in Fig. 1(c).

A 3-terminal negative resistance device (Fig. 2(a)) is one whose family of characteristics has at least one curve in the $v_1 - i_1$ plane or $v_2 - i_2$ plane exhibiting a negative slope region. A hypothetical example of a family of 3-terminal negative-resistance device characteristics is shown in Fig. 2(b) for the voltage-controlled type, and in Fig. 2(c) for the current-controlled type.

Numerous 2-terminal negative resistance devices have been reported in the literature, the most well known being the tunnel diode, which is a type N device, and a glow tube, which is a type S device. An extensive catalog of such devices is listed in [1]. Indeed, with the systematic method for designing negative resistance devices using existing solid state devices developed in [1-2], there is now available virtually thousands of such 2-terminal negative resistance devices.

Examples of 3-terminal negative resistance devices are also frequently reported, specially in the recent literature. For example, a 2-μm gate length GaAs MESFET with $N_D = 6 \times 10^{16}$ cm^{-3} has been observed to exhibit a voltage-controlled negative resistance characteristic [3]. An older example is the unijunction transistor which has a current-controlled negative resistance characteristic [4]. Indeed, with the recent advances in material technology on GaAs and other materials having a negative differential drift velocity versus electric field characteristic [4], many more 3-terminal negative resistance devices are emerging over the horizon. In addition, a systematic circuit approach for generating new 3-terminal negative resistance devices having a "tailored" characteristic has just been reported [5].

In spite of the existence of a wide variety of negative resistance devices, very few scope tracings of such characteristics have appeared in the literature.

†This is because physical batteries have an internal resistance and are themselves eventually passive.

The reason is that the "negative resistance" often caused jump phenomenon, hysteresis, and oscillation in the tracing circuitry. Indeed, all commercially available curve tracers are based on the concept of applying a "sweeping" voltage source over the device's dynamic range and then monitoring the device current [6]. This technique will never work for current controlled devices because the load line representing the voltage source and its internal resistance will intersect their v-i characteristics (Figs. 1(c) and 2(c)) at several points during part of the tracing cycle, resulting at best in a jump phenomenon. This problem can be easily overcome by using a current source sweep instead. A much more serious problem is the perennial oscillation and instability that occur in many negative resistance devices.

Our objective in this paper is to design a curve tracer which is capable of tracing the voltage-controlled or current-controlled characteristics of both 2- and 3-terminal negative resistance devices. In the case of a 3-terminal device, our design will allow the device to be traced in any one fo the following six standard representations listed in Table 1.

Table 1. Equations for the six representations of a 3-terminal or 2-port device

Current-controlled representation	Voltage-controlled representation
$v_1 = \hat{v}_1(i_1,i_2)$ $v_2 = \hat{v}_2(i_1,i_2)$	$i_1 = \hat{i}_1(v_1,v_2)$ $i_2 = \hat{i}_2(v_1,v_2)$
Hybrid-1 representation	Hybrid-2 representation
$v_1 = \hat{v}_1(i_1,v_2)$ $i_2 = \hat{i}_2(i_1,v_2)$	$i_1 = \hat{i}_1(v_1,i_2)$ $v_2 = \hat{v}_2(v_1,i_2)$
Transmission-1 representation	Transmission-2 representation
$v_1 = \hat{v}_1(v_2,-i_2)$ $i_1 = \hat{i}_1(v_2,-i_2)$	$v_2 = \hat{v}_2(v_1,i_1)$ $-i_2 = \hat{i}_2(v_1,i_1)$

Whereas the methods for tracing the first 4 representations are a simple extension of the 2-terminal case, tracing the two transmission (chain) representations require some special techniques so that a voltage source and a current source can be simultaneously applied across the same pair of terminals! Indeed, to the best of our knowledge, no one has been able to trace the transmission characteristics of any 3-terminal or 2-port device before, let alone its negative resistance.

In order not to distract those readers interested only in using our tracer to trace negative resistance devices, the complete schematic diagram is first given in Section 2 along with numerous examples illustrating its use. The theory for quenching the oscillation and instability is developed in Section 3. This theory is crucial to the successful design of our tracer. The special technique developed for tracing the transmission representation is described in Section 4. Details on the design of the various components of the complete curve tracer circuit in Section 2 are described in Section 5 and in the Appendix.

2. THE CURVE TRACER: A USER'S GUIDE

A. External Description

In its simplest form, the circuit for tracing a 2-terminal negative resistor is shown in Fig. 3(a) for the voltage-controlled case, and in Fig. 3(b) for the current-controlled case. The series resistance R in Fig. 3(a) can be interpreted as the internal resistance of the voltage source $v_s(t)$ and should ideally be kept as small as possible. The shunt conductance G in Fig. 3(b) can be interpreted as the internal conductance of the current source $i_s(t)$ and should ideally be kept as small as possible.

The capacitance C in Fig. 3(a) and the inductance L in Fig. 3(b) are needed to quench any oscillation and other more complicated forms of instability. It will be shown in Section 3 that by choosing a large enough value of C and L, no instability will occur provided the tracing signal frequency is sufficiently small: The larger the value of C and L, the smaller the allowable frequency. Since too low a frequency would result in flicker in the oscilloscope tracing, a minimum frequency of 60 Hz is recommended. This implies that the value of C and L should be chosen as small as possible.

It will also be shown in Section 3 that there is a trade off between the values of R and C, and between G and L: increasing R over a limited range allows

us to decrease C and increasing G over a limited range allows us to decrease L. Since the trade off depends on the device characteristic itself, it is essential to allow both R and C in Fig. 3(a), and G and L in Fig. 3(b) to be adjustable externally.

The same basic circuits in Fig. 3 can be used to trace the negative resistance characteristics of a 3-terminal device (for the first 4 representations in Table 1) by simply applying a staircase voltage or current waveform to the other terminal. The increment in each step in the staircase signal determines the "spacing" between the curves in the family of characteristics. Since this choice depends on the nature of the device, the incremental step must also be externally adjustable.

Finally, since different devices have different dynamic ranges, the amplitude of the tracing signal $v_s(t)$ and $i_s(t)$ should also be adjustable.

To summarize, any general purpose curve tracer must have external switches and knobs for adjusting, at the very least, the following parameters:

Voltage-controlled device	Current-controlled device
1. R	1. G
2. C	2. L
3. incremental step Δi or Δv	3. incremental step Δv or Δi
4. amplitude of $v_s(t)$	4. amplitude of $i_s(t)$

In addition, the following external terminals are needed:

1. Device terminals: for connecting 2-terminal or 3-terminal device being traced.
2. Input signal terminals: to be connected to a periodic signal generator, usually a sinusoidal signal.
3. Output terminals: for connecting the device voltage signal to the horizontal plate and the device current signal to the vertical plate of the oscilloscope. A symbolic diagram illustrating how these terminals are connected in an actual measurement setup is shown in Fig. 4(a). A photograph of the curve tracer designed with the above features is shown in Fig. 4(b).

B. Complete Circuit Schematic Diagram

For users interested in building this curve tracer, a complete schematic diagram is shown in Figs. 5(a), (b), (c) and (d). For clarity purpose, this diagram is broken up into 3 parts and labelled as Figs. 5(b), (c) and (d), respectively. All components are clearly labelled for easy duplication. The complete list of components and their specifications are given in Appendix A.

The switches mounted on a common shaft are connected by dotted broken lines. For example, switch SW in Fig. 5(a) is a 2-pole 4-position switch mounted on a common shaft.

Fig. 5(a) is the block diagram of the curve tracer. It consists basically of three parts such as tracing signal generator, staircase signal generator and vertical and horizontal channel measurement circuit. There is a 2-pole 4-position switch sw which is used to switch the tracing signal and staircase signal to different terminals of the device being traced. Inductor L_s is used to adjust the inductance in series with current-controlled 2-terminal device. Potentiometer R_p is used to adjust the shunt resistance. Potentiometer R_s and capacitor C_p are used to adjust the resistance in series and capacitance in parallel with the voltage-controlled 2-terminal device being traced, respectively. The input signal for driving the tracer signal generator and the staircase signal generator are supplied by an external signal generator which is usually a sinusoidal signal generator. The output signals of the vertical and horizontal channel measurement circuit are applied to the vertical and horizontal terminals of the oscilloscope, respectively.

Figures 5(b), (c) and (d) form the complete circuitry of the curve tracer. Figure 5(b) shows the tracer signal generator circuit which transforms the input signal into a voltage source or current source having several optional waveforms (e.g., positive half sine wave, negative half sine wave, etc.) useful on various occasions.

Figure 5(c) shows the staircase signal generator circuit which is used to generate the voltage or current increment signals so that the family of characteristics describing a 3-terminal or 2-port device can be traced in a single measurement set up.

Figure 5(d) shows the vertical and horizontal channel measurement circuit which measures the current and the voltage associated with the device under test. Switch SW_2 switches the different tracer and staircase signals to the associated terminals of the 3-terminal device so that the families of

characteristics associated with any one of the 6 representations of the device may be traced in a single set up. Position 1 (present position of the arrow in Fig. 5(d)), 2, 3 or 4 corresponds to selecting the voltage-controlled, current-controlled, hybrid-2 or hybrid-1 (as shown in Table 1) representation of the device. Position 5 or 6 corresponds to selecting the transmission-1 or transmission-2 representation of the device.

When tracing a 2-terminal voltage-controlled (type N) device, SW_2 should be switched to position 1, and when tracing a 2-terminal current-controlled (type S) device, SW_2 should be switched to position 2.

The position of switch SW_{11} and SW_{12} depends on whether voltage or current is measured, respectively, i.e., to measure the voltage across the associated terminals of the device, we set SW_{11} to position v, and to measure the current through the associated terminals of the device, we set SW_{11} to position i.

The banks of capacitors and inductors in Fig. 5(d) correspond to C and L in Figs. 3(a) and (b), respectively. An extra position (ext.) in each switch allows the user to connect a capacitor or inductor (whose value is not available internally) across an external terminal pair.

C. Sample Tracings of 2-Terminal Negative Resistance Devices

Hundreds of negative resistance device characteristics have been successfully traced with our curve tracer. The following is a sample of some of these devices with interesting v-i characteristics. Most of these tracings require a "stabilizing" capacitance or inductance and could not have been traced by existing commercial curve tracers.

1. Voltage-controlled (type N) devices:

Figure 6(a) shows the scope tracing of a commercial 1N3717 tunnel diode (made by General Electric Co.) taken without the shunt capacitor in Fig. 3(a). Note that the negative resistance region looks like a mess although superficially its outline seems to suggest a smooth typical tunnel diode characteristic with a single peak and a single valley point [4]. Applying our theory from Section 3, we know the instability phenomenon in Fig. 6(a) can be quenched by connecting a sufficiently large capacitance C in parallel with the tunnel diode provided the frequency is low enough. The characteristic in Fig. 6(b) was successfully traced with a 40 Hz sinusoidal tracing signal and a 1 μF shunt capacitance. This v-i curve came as a big surprise as it differs drastically

from the expected conventional tunnel diode characteristic.

To ensure that this v-i curve is indeed the true device characteristic, we have made a point-by-point dc measurement and used multiple exposure to capture the points on film, as shown in Fig. 6(c). They coincide exactly with the "ac" tracing in Fig. 6(b). To ensure that the tracing circuit is not oscillating at a frequency beyond the bandwidth of our oscilloscope, we have checked the waveforms using a high frequency (200 MHz bandwidth) scope and found no discernible oscillation.

We have repeated our experiment with several other tunnel diodes (e.g., 1N3720) and found all of them to be characterized by a double-peak double-valley characteristic. We conclude therefore that at least for the batch of tunnel diodes we have traced, they are characterized by a v-i curve somewhat different from those published in textbooks. While this characteristic is more interesting and potentially more useful as a harmonic generator, any circuit design based on the conventional characteristic would clearly be in serious error!

Consider next the voltage-controlled negative resistance one-port shown in Fig. 7(a). The v-i curve in Fig. 7(b) is traced without a shunt capacitance. Note the instability near the negative resistance region. By adding a 0.1 μF shunt capacitance, we obtained the "clean" v-i curve in Fig. 7(c).

The preceding v-i characteristics lie in the first and third quadrants, as expected, since the devices are passive and unbiased.

Consider next the 2-transistor one-port shown in Fig. 8(a) which is biased by a 10 V battery. The v-i curve in Fig. 8(b) is again all messed up. The clean characteristic in Fig. 8(c) is traced with a 0.1 μF shunt capacitance. Note that unlike the previous characteristics, this device is not passive because there are points in the second and fourth quadrants. However, it is eventually passive, as expected.

To show that the parameters of some negative resistance devices, especially those made of op amps, are such that a stable v-i characteristic can be traced without the shunt capacitance, three different op amp one-ports are shown in Fig. 9, 10 and 11, along with their respective voltage-controlled negative resistance characteristics.

2. Current-controlled (type S) devices:

Consider the one-port shown in Fig. 12(a). Its v-i characteristic traced without a series inductance is shown in Fig. 12(b). Note the oscillation due to the tracing circuit wiped out the most interesting portion of the v-i

characteristic. The same one-port traced with a 2 mH series inductance and $G = 8.8 \times 10^{-6}$ mho is shown in Fig. 12(c).

Consider next the two-transistor one-port shown in Fig. 13(a). Its v-i characteristic traced in Fig. 13(b) without a series inductance leads to oscillation within the negative resistance region. By connecting a 3 mH inductance in series, we obtain the sharp v-i characteristic in Fig. 13(c).

Figures 14 through 17 show 4 different current-controlled negative resistance one-ports which were successfully traced without a series inductance. Observe that none of the current-controlled characteristics in Figs. 12-17 could be obtained by commerical curve tracers based on a voltage sweep.

D. Sample Tracings of 3-Terminal or 2-Port Negative Resistance Devices.

Numerous 3-terminal and 2-port negative resistance devices have been successfully traced using our curve tracer. The following is a sample of some of these devices.

Consider the 2-port shown in Fig. 18(a). Tracing the v-i characteristics with i_2 as a parameter (see hybrid-1 representation from Table 1) without a shunt capacitance, we obtain the messy characteristics in Fig. 18(b). Since each v-i curve in Fig. 18(b) is voltage-controlled, we can quench the oscillation by adding a shunt capacitance across port 1. The resulting family of characteristics $i_1 = \hat{i}_1(v_1, i_2)$ is shown in Fig. 18(c).

Consider next the 2-port shown in Fig. 19(a). Tracing the $i_1 - v_1$ characteristic with i_2 as a parameter (see hybrid-1 representation from Table 1) without a series inductance, we obtained the messed up characteristics in Fig. 19(b). Since each v-i curve in Fig. 19(b) is current-controlled, we can quench the oscillation by adding an inductance in series with port 1. The resulting family of characteristics is shown in Fig. 19(c).

To demonstrate that our curve tracer can indeed trace the characteristics of a 3-terminal or 2-port device in any of the 6 representations, consider the two-transistor 2-port shown in Fig. 20(a). The 2 families of characteristics corresponding to each of the 6 distinct representations in Table 1 are shown in Figs. 20(b), (c), (d), (e), (f) and (g), respectively. These characteristics are all traced without any shunt capacitance or series inductance. The two transmission (chain) representations shown in Figs. 29(f) and (g) are as clear as the others, thereby demonstrating the possibility of tracing these two families of characteristics. To the best of our knowledge, this measurement had never been made before.

Just as the chain matrix is extremely useful in analyzing and designing two or more linear 2-ports connected in cascades, the possibility of measuring the nonlinear transmission characteristics could be equally useful in analyzing and designing nonlinear 2-ports connected in cascades. The resulting transmission characteristics in this case will be just the composition of the respective transmission characteristics.

3. QUENCHING THE OSCILLATION

No physical device is purely resistive. The oscillation or other unstable behavior that often plagued the tracing circuitry is strictly a dynamic phenomenon and can only be quenched by carrying out a detailed analysis using a realistic dynamic circuit model for the device. Using a device physics approach [4] or a circuit-theoretic approach [7], we can derive the following basic result:

Negative Resistance Device Modeling Principle

1. Every voltage-controlled (type N) negative resistance device must be modelled with a capacitor in parallel with a type N negative resistor, as shown in Fig. 21(a), and possibly additional dynamic elements at higher frequencies.
2. Every current-controlled (type S) negative resistance device must modelled with an inductor in series with a type S negative resistor Fig. 21(b), and possibly additional dynamic elements at higher frequencies.

We have found the models given in Fig. 21 are adequate for our purpose in this paper.

In order to analyze and develop a method to quench oscillations and other instability phenomena frequently encountered in conventional curve tracers, we have found that it is necessary to include at least a series parasitic inductance L_p to the type N device model in Fig. 21(a), and a shunt parasitic capacitance C_p to the type S device model in Fig. 21(b), in order to account for the small but non-zero line inductance and stray capacitance of the connecting wires. Hence, the simplest realistic circuit model of our negative-resistance curve tracer is as shown in Fig. 22(a) for a type N curve tracer, and Fig. 22(b) for a type S curve tracer. Since these 2 circuits are dual of each other [8], we will analyze only the type N circuit.

The state equation for the type N curve tracer circuit model in Fig. 22(a) is given by

$$\frac{dVc}{dt} = \frac{1}{C}[i_L - \hat{i}_R(v_c)]$$
$$\frac{di_L}{dt} = \frac{1}{L}[v_s(t) - Ri_L - v_c] \qquad (1)$$

In order to uncover the source of the oscillation, it suffices to replace the voltage source $v_s(t)$ by a battery E so that we can analyze the stability of each equilibrium point. For the circuit in Fig. 22(a), the equilibrium points are identical to the dc operating points obtained by the load line method, as illustrated in Fig. 23 using a typical tunnel diode v-i characteristic. Observe that there are 3 equilibrium points in Fig. 23(a) but only one in Fig. 23(b). The bifurcation parameter is given by

$$R = \frac{1}{G_{max}} \qquad (2)$$

where

$$G_{max} \triangleq \text{magnitude of maximum negative slope of the } v_R\text{-}i_R \text{ characteristic} \qquad (3)$$

In order for the curve tracer to work properly, it is necessary that each equilibrium point be locally asymptotically stable [8-9] for all values of E within the dynamic range of interest. To derive the conditions for satisfying this requirement, consider the Jacobian matrix associated with (1) about an equilibrium point Q:

$$\underset{\sim}{J}_Q = \begin{bmatrix} -\frac{1}{C}\hat{i}'_R(V_Q) & \frac{1}{C} \\ -\frac{1}{L} & -\frac{R}{L} \end{bmatrix} \qquad (4)$$

where $\hat{i}'_R(V_Q)$ denotes the slope at $v_R = V_Q$. The necessary and sufficient conditions for the equilibrium point Q to be locally asymptotically stable are given by [8-9]:

$$T_Q \triangleq -\frac{R}{L} - \frac{1}{C}\hat{i}'_R(V_Q) < 0 \qquad (5)$$

$$\Delta_Q \triangleq \frac{R}{LC}\hat{i}'_R(V_Q) + \frac{1}{LC} > 0 \qquad (6)$$

Since $R > 0$, $L > 0$, and $C > 0$, conditions (5) and (6) are always satisfied if $\hat{i}'_R(V_Q) \geq 0$. Hence all equilibrium points falling on the non-negative

slope region of the $v_R - i_R$ characteristic are always loacally asymptotically stable. This explains why it is easy to trace monotone-increasing v-i characteristics.

However, both (5) and (6) are easily violated in negative resistance characteristics especially when the negative slope is steep, i.e., when $\hat{i}_R'(V_Q) << 0$. Since (5) and (6) must be satisfied at all operating points in the negative resistance region, the most critical situation occurs at the "steepest" point where the slope

$$\boxed{\hat{i}_R'(V_Q) = - G_{max}} \tag{7}$$

is most negative, where G_{max} as defined in (3) is a positive number. Using this notation, conditions (6) and (5) can be recast into (8) and (9), respectively, and restated in words as follows:

Stability Theorem

The necessary and sufficient conditions for all oeprating points of the type N curve tracer model in Fig. 22(a) to be locally asymptotically stable are:

$$\boxed{R < \frac{1}{G_{max}}} \tag{8}$$

$$\boxed{R > (LG_{max})\frac{1}{C}} \tag{9}$$

Since G_{max} is fixed for a given device and L, being the parasitic inductance, can not be reduced below some minimum value, the conflicting demands of (8) and (9) often can not be satisfied by adjusting only the parameter R alone, especially when the negative slope is steep, as in the examples in Figs. 6-8. Observe, however, that so long as $G_{max} < \infty$, conditions (8) and (9) can always be satisfied by choosing a sufficiently large value for C. This is easily met by connecting an adjustable capacitance C_1 in parallel with the device so that $C = C_0 + C_1$, as shown in Fig. 3(a).†

In the R-C parameter plane, conditions (8) and (9) define the stable region shown in Fig. 24(a) for a typical value of L. The minimum capacitance C_{min} needed to quench the oscillation occurs at the intersection between the

†Since C_0 is very small in a typical device, $C = C_0 + C_1 \approx C_1$. Hence we will neglect C_0 from our subsequent discussion for simplicity.

two bifurcation curves $\Delta = 0$ and $T = 0$. Note that the shaded region shifts to the right as L increases, as shown in Fig. 24(b) for a somewhat larger value of L. Hence C_{min} increases with L.

To minimize C_{min}, therefore, we must keep the connecting wires as short as possible.

Choosing the parameters R and C within the shaded region in Fig. 24 guarantees that the equilibrium point will be either a stable node or a stable focus [8] for each dc input voltage E.

For each equilibrium point $V_C = V_Q$ and each initial condition $V_C(0)$, the transient decay rate is determined by the real part σ of the eigenvalues

$$s_{1,2} = -\frac{1}{2}\left[\frac{R}{L} + \frac{\hat{i}'_R(V_Q)}{C}\right] \pm \frac{1}{2}\sqrt{\left[\frac{R}{L} + \frac{\hat{i}'_R(V_Q)}{C}\right]^2 - \frac{4}{LC}\left[R\hat{i}'_R(V_Q)+1\right]} \qquad (10)$$

if $V_C = V_Q$ is a focus, or by the smaller real natural frequency σ (corresponding to choosing the negative sign in (10)) if $V_C = V_Q$ is a node. A typical relationship between σ and C as calculated from (10) using a fixed value for R, L and $\hat{i}'_R(V_Q)$ is shown in Fig. 25. Note that $|\sigma|$ is largest at $C = C_{opt}$.

Now the transient will for all practical purposes be negligible after 5 time constants τ, where $\tau = \frac{1}{|\sigma|}$. Hence, it is possible to trace the v-i characteristic using a periodic ac voltage source $v_s(t)$ provided its frequency ω is chosen so that

$$\boxed{\omega < \frac{1}{5}|\sigma|} \qquad (11)$$

Since $\sigma = 0$ when $C = C_{min}$ in Fig. 25, where C_{min} corresponds to the intersection between the two bifurcation curves $T = 0$ and $\Delta = 0$ in Fig. 24(a), it follows from (11) that we must choose C greater than C_{min}. The maximum allowable frequency occurs when we choose $C = C_{opt}$. Any larger value of C must be accompanied by a decrease in ω. We can now summarize our preceding analysis as follows:

Oscillation Quenching Guidelines for Type N Device (Fig. 3(a))

1. Choose $R < \frac{1}{G_{max}}$.
2. Choose $C > C_{min}$.

3. Decreasing R must be accompanied by an increase in C.
4. Increasing C beyond C_{opt} must be accompanied by a decrease in the tracing frequency ω.

By duality, we can state:

Oscillation Quenching Guidelines for Type S Device (Fig. 3(b))

1. Choose $G < \frac{1}{R_{max}}$, where R_{max} is the magnitude of the slope of $\hat{v}'_R(i_R)$ at its steepest point.
2. Choose $L > L_{min}$, where L_{min} corresponds to C_{min} in Fig. 24(a).
3. Decreasing G must be accompanied by an increase in L.
4. Increasing L beyond L_{opt} must be accompanied by a decrease in the tracing frequency ω, where L_{opt} corresponds to C_{opt} defined above.

4. TRACING THE TRANSMISSION REPRESENTATION

The two transmission representations listed in Table 1 are the nonlinear generalization of the well-known chain matrix representations for linear time-invariant 2-ports, namely,

	transmission-1	transmission-2
linear 2-port	$\begin{bmatrix} V_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} t_{11} & t_{12} \\ t_{21} & t_{22} \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix}$ (12a)	$\begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} = \begin{bmatrix} t'_{11} & t'_{12} \\ t'_{21} & t'_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ i_1 \end{bmatrix}$ (12b)
nonlinear 2-port	$v_1 = \hat{v}_1(v_2,-i_2)$ $i_1 = \hat{i}_1(v_2,-i_2)$ (13a)	$v_2 = \hat{v}_2(v_1,i_1)$ $-i_2 = \hat{i}_2(v_1,i_1)$ (13b)

The two matrices in Eqs. (12a) and (12b) are called chain matrices.† The transmission representation is most conveniently used when two or more linear 2-ports are connected in cascade. In this case the transmission matrix of the composite 2-port is just the product of the respective chain matrices. Likewise, when two or more resistive 2-ports are connected in cascade, the transmission representation of the composite 2-port is just the composition of the respective transmission functions. This remarkable property is of immense help in both

†The chain matrix in Eq. (12a) is usually denoted by $\begin{bmatrix} A & B \\ C & D \end{bmatrix}$ in the literature.

analysis and design.

Unfortunately, manufacturers never specify a nonlinear 3-terminal device by its transmission representation. The reason is simple: no measurement technique, let alone a dedicated instrument, is available.

One obstacle here is due to the fact that both independent variables (v_2 and $-i_2$ in the transmission 1 representation; v_1 and i_1 in the transmission 2 representation) in Eqs. (13a) and (13b) pertain to the same port.

For example, to measure the transmission 2 representation, it is necessary to apply an independent voltage source $v_s(t)$ and an independent current source $i_s(t)$ to port 1 of the 3-terminal device $\mathcal{D}$ so that $v_1 = v_s(t)$ and $i_1 = i_s(t)$. The only two ways for connecting these two sources directly, as shown in Fig. 26, are not feasible because whereas $v_1 = v_s(t)$ in Fig. 26(a), $i_1 \neq i_s(t)$ unless $i_{in} \equiv 0$; and whereas $i_1 = i_s(t)$ in Fig. 26(b), $v_1 \neq v_s(t)$ unless $v_{in} \equiv 0$.

Another serious obstacle is encountered at port 2; namely, the load N in Fig. 26 must not present any constraint between the two dependent port variables v_2 and i_2 because both v_2 and i_2 are defined uniquely by the transmission functions via Eq. (13b). Note that open circuiting port 2 is not allowed because i_2 would then be constrained to zero. Likewise, short circuiting port 2 is not allowed because v_2 would then be constrained to zero. In fact, N can not be any ordinary one-port because such a one-port would be described by a relationship between v_2 and i_2, thereby creating an implicit constraint between these two dependent variables.

The first obstacle can be overcome by inserting a nullator[†] in series with the voltage source $v_s(t)$ as shown in Fig. 27(a), thereby clamping $i_{in} = 0$. Moreover, since the voltage across the nullator is zero, we still have $v_1 = v_s(t)$.

The second obstacle can be overcome by choosing the load N to be a norator,[††] as shown in Fig. 27(b). Since this element imposes no constraint in either v_2 or i_2, the port current i_2 and port voltage v_2 depend only on v_1 and i_1. Hence, the norator is functioning like a "slack" variable in linear programming.

Although individually, nullators and norators can not be realized by any physical circuit, together they can be simulated by an op amp operating in its linear region, as shown by the ideal op amp model in Fig. 27(b). Hence,

---

[†]The nullator is a singular circuit element defined by a single point at the origin, namely, $v = 0$, $i = 0$ [10-11].

[††]A norator is a singular circuit element defined by all points in the v-i plane [10-11].

replacing the nullator and norator in Fig. 27(b) by an op amp, we obtain the practical circuit in Fig. 27(c) for tracing the transmission 2 characteristics of a 3-terminal device $\mathcal{D}$.

To trace the transmission 2 characteristics of a 3-terminal device $\mathcal{D}$ using the circuit in Fig. 27(c), we first apply the signal $v_s(t)$ to the horizontal channel and the signal v_2 to the vertical channel of the oscilloscope. A staircase signal $i_s(t)$ is then applied to obtain the first family of characteristics; namely, $v_2 = \hat{v}_2(v_1, i_1)$. To obtain the second family of transmission characteristics, we repeat the above measurement but with $i_2(t)$ applied to the vertical channel through a small current sensing resistor.

To obtain the transmission 1 characteristics, we simply use the same circuit in Fig. 27(c) but with terminal 1 and 2 of the 3-terminal device $\mathcal{D}$ interchanged. The transmission characteristics shown in Figs. 19 and 20 are all measured using this simple tracing circuit. Our experience has shown that this circuit is rather robust and stable, in spite of the fact that the nullator and norator are highly pathological. This circuit is also interesting because it illustrates how a purely abstract concept can become indispensable in the design of a practical circuit. Indeed, we do not know of any other way for measuring the transmission characteristics.

5. DESIGN DETAILS

As mentioned above in Section 2, the complete circuit of the curve tracer consists basically of three parts: the tracer signal generator, the staircase signal generator and the vertical and horizontal channel measurement circuit. The tracer signal generator shown in Fig. 5(b) includes a full-wave rectifier, an amplifier, a voltage source, and a current source. Push-pull transformer T_1 is used to apply the signal from the external signal generator to the full-wave rectifier consisting of four diodes D_1, D_2, D_3 and D_4. Capacitors C_1 and C_2 are used to avoid potential parasitic oscillations. The load of the full-wave rectifier is a voltage amplifier IC_1 which has different gain for different waveforms so that the amplitudes of tis output voltages will be basically the same when the input voltage of the push-pull transformer T_1 is constant. The output stage IC_2 is a buffer.

The operational amplifier IC_3 amplifies the input signal from switch SW_2. The output voltage of IC_3 is applied to transistors Q_1 and Q_2. Transistor Q_1 will conduct when the input voltage of IC_3 is negative, and Q_2 will conduct

when the input voltage of IC_3 is positive, respectively. The feedback of IC_3 is from the output current of the tracer current source via resistor R_9.

The high-voltage op amp IC_4 amplifies the input signal from potentiometer R_6. Meanwhile, SW_2 will ground the input terminal of IC_3 so that the current source will not interfere with other circuits. Transistors Q_3 and Q_5 are the driver stages of the tracer voltage source, and transistors Q_4 and Q_6 are the power output stages of the tracer voltage source. Transistors Q_3 and Q_4 will conduct when the input signal of IC_4 is negative, and Q_5 and Q_6 will conduct when the input signal of IC_4 is positive, respectively. Diodes D_5, D_6, D_9 and D_{10} provide biasing for the output stages, and D_7, D_8, D_{11} and D_{12} are used for overload protection. Resistors R_{24} and R_{25} connected to the emitters of Q_4 and Q_6, respectively, are current-limiting resistors.

Figure 5(c) shows the circuit diagram of the staircase signal generator which consists of three parts: the staircase voltage generator, the staircase voltage source, and the staircase current source. IC_6, IC_7, IC_8, and IC_9 form the staircase voltage generator. The op amp IC_6 is used as a zero-crossing detector. The input signal of IC_6 is the same as that of transformer T_1 in the tracer signal generator so that the staircase signal is synchronized to the tracing signal.

The output pulses of the zero-crossing detector are used as triggers for the monostable multivibrators IC_7 and IC_8. The negative output pulses of IC_6 will be clipped by diode D_{13}. IC_5 is a +5 volt regulator that is used as a DC power supply for the monostable multivibrators IC_7 and IC_8. The output (positive) pulses of IC_7 charge capacitor C_{10} of the integrator (formed by IC_9, resistor R_{34} and capacitor C_{10}) to generate a staricase voltage between the output terminals of IC_9. The output (positive) pulses of IC_8 will discharge the integrator so that a periodic staircase voltage will be obtained. By adjusting the width of output pulses of IC_7 (by adjusting potentiometer R_{27}), we can change the "increment" in the steps. The "number" of steps can be changed by adjusting the width of the output pulses of IC_8 (by adjusting potentiometer R_{29}).

Diode D_{14} is used to avoid a premature discharge of the capacitor C_{10} while generating the step voltages. The network formed by resistor R_{35} and potentiometer R_{36} is used to adjust the zero step of the output staircase voltage of the integrator. Op amp IC_{10} and IC_{11} form a voltage source with positive and negative voltage output. In fact, IC_{10} is used as a phase

inverter and IC_{11} is a voltage follower. There is a voltage divider between IC_{10} and IC_{11} to change the step increment. The positive step voltage from the integrator is fed to the inverting input or non-inverting input of IC_{10} by switch SW_1 so that positive and negative step voltages can be obtained. Op amp IC_{12} and transistor Q_7 with the associated resistors form a positive staircase current source to which the positive staircase voltage from IC_{11} is applied through SW_1. Potentiometer R_{56} is used to adjust the zero step of the positive staircase current signal. Op amp IC_{13} and transistor Q_8 with the associated resistors form a negative staircase current source to which the negative staircase voltage from IC_{11} is applied through SW_1. Diode D_{15} and potentiometer R_{66} are used to adjust the zero step of the negative staircase current signal.

Figure 15(d) is the circuit diagram of the vertical and horizontal channel measurement circuit. In fact, the vertical and horizontal channels are basically the same. To improve the precision of the measurement circuit, we use JFET input quad op amp followers IC_{14}, IC_{15}, IC_{19} and IC_{20} as the input stages of these two channels so that the current through the device being traced will be almost equal to that through the current sensing resistor. There are four voltage dividers formed by resistors R_{75}-R_{78}, R_{79}-R_{82}, R_{96}-R_{99} and R_{100}-R_{103}, respectively, so that the op amp followers IC_{14}, IC_{15}, IC_{19} and IC_{20} would not saturate within the dynamic range of the device being traced. The division factors are 1, 2, 5 and 10, respectively. Hence, the input voltages of these followers will be reduced by 1, 2, 5 or 10 times so that the voltage amplitude displayed on the scope is equal to 1, $\frac{1}{2}$, $\frac{1}{5}$, or $\frac{1}{10}$ of the actual amplitude of the output voltage, depending on the positions of the switches SW_9 and SW_{10}. When measuring current through the device being traced, the voltage across the current sensing resistor R_{92}-R_{95} (or R_{71}-R_{74}) is applied to the differential amplifier IC_{21} (or IC_{16} for the horizontal channel). Current sensing resistors R_{71}-R_{74} and R_{92}-R_{95} are both chosen equal to 1 K, 500, 100 and 10 ohm, respectively. Hence, there is 1, 2, 10 and 100 mA of current through the device being traced for a 1 volt voltage across the resistors, respectively, depending on the positions of the switches SW_7 and SW_8. Op amp IC_{22} (or IC_{17}, for the horizontal channel), is a phase inverter. Op amp IC_{23} (or IC_{18} for the hosizontal channel) is a voltage follower serving as the output stage of the curve tracer. The polarities of the output signals of the vertical and horizontal channel can be changed by switches SW_{14} and SW_{13}, respectively. While measureing voltage, switch SW_{12} (or SW_{11} for the horizontal

channel) will ground the inverting input of the differential amplifier IC_{21} (or IC_{16}, in horizontal channel).

Op amp IC_{24} is playing the role of both nullator and norator when tracing the transmission characteristics of a 3-terminal device.

Potentiometer R_{68} is used as the shunt resistance in the tracing current source, and inductors L_1 through L_6 are connected in series with the device being traced, respectively. Both the shunt resistance and inductance are used to quench the oscillation when tracing a current-controlled 2-terminal device. Similarly, the potentiometer R_{112} connected in series and capacitors C_{11} through C_{16} connected in parallel with the device, respectively, are used to quench the oscillation when tracing a voltage-controlled 2-terminal device, as already described in Section 3.

REFERENCES

[1] L. O. Chua, J-B Yu, and Y-Y Yu, "Negative resistance devices," International Journal of Circuit Theory and Applications, Vol. 11, 1983, pp. 161-186.

[2] L. O. Chua, J-B Yu, and Y-Y Yu, "Bipolar-JFET-MOSFET negative resistance devices," IEEE Trans. on Circuits and Systems, to appear in 1985.

[3] J. J. Barnes, R. J. Lomax, and G. I. Haddad, "Finite element simulation of GaAs MESFET's with lateral doping profiles and submicron gates," IEEE Trans. on Electron Devices, Vol. ED-23, Sept., 1976, pp. 1042-1048.

[4] S. M. Sze, Physics of Semiconductor Devices, John Wiley & Sons, New York, 1981.

[5] J-B Yu, C-Q Zhang, and Z-S Kang, "Controlled negative resistance devices," International Symposium on Circuits and Systems, May 7-10, 1984, Montreal, Canada.

[6] J. Mulvey, Semiconductor Device Measurements, Tektronix, Inc., Beaverton, Oregon, 1968.

[7] L. O. Chua, "Device Modelling via Basic Nonlinear Circuit Elements," IEEE Trans. on Circuits and Systems, Vol. CAS-27, November, 1980, pp. 1014-1044.

[8] L. O. Chua, Introduction to Nonlinear Network Theory, McGraw Hill Book Company, New York, 1969.

[9] L. O. Chua, "Dynamic nonlinear network: state-of-the-art," IEEE Trans. on Circuits and Systems, Vol. CAS-27, Nov. 1980, pp. 1059-1087.

[10] H. J. Carlin and A. B. Giordano, Netowrk Theory, Prentice Hall, Inc., Englewood Cliffs, New Jersey, 1964.

[11] L. Bruton, RC Active Circuits: Theory and Design, Prentice Hall, Inc., Englewood Cliffs, New Jersey, 1980.

APPENDIX A: THE CATALOG OF COMPONENTS

Part No.	Model Description	Part No.	Model Description
R_1	10 KΩ ± 10% 1/4 W	R_{33}	3 KΩ ± 10% 1/4 W
R_2	10 KΩ ± 10% 1/4 W	R_{34}	30 KΩ ± 10% 1/4 W
R_3	62 KΩ ± 10% 1/4 W	R_{35}	2.2 KΩ ± 10% 1/4 W
R_4	330 KΩ ± 10% 1/4 W	R_{36}	10 KΩ potentiometer
R_5	20 KΩ ± 10% 1/4 W	R_{37}	100 KΩ ± 10% 1/4 W
R_6	10 KΩ potentiometer	R_{38}	100 KΩ ± 10% 1/4 W
R_7	10 KΩ ± 10% 1/4W	R_{39}	100 KΩ ± 10% 1/4 W
R_8	10 KΩ ± 10% 1/4 W	R_{40}	100 KΩ ± 10% 1/4 W
R_9	100 KΩ ± 10% 1/4 W	R_{41}	500 KΩ ± 1% 1/4 W
R_{10}	3.9 KΩ ± 10% 1/4 W	R_{42}	300 KΩ ± 1% 1/4 W
R_{11}	22 KΩ ± 10% 1/4 W	R_{43}	100 KΩ ± 1% 1/4 W
R_{12}	680 Ω ± 10% 1/2 W	R_{44}	50 KΩ ± 1% 1/4 W
R_{13}	10 KΩ ± 10% 1/4 W	R_{45}	30 KΩ ± 1% 1/4 W
R_{14}	22 KΩ ± 10% 1/4 W	R_{46}	10 KΩ ± 1% 1/4 W
R_{15}	3.9 KΩ ± 10% 1/4 W	R_{47}	5 KΩ ± 1% 1/4 W
R_{16}	680 Ω ± 10% 1/2 W	R_{48}	5 KΩ ± 1% 1/4 W
R_{17}	10 KΩ ± 10% 1/4 W	R_{49}	20 KΩ ± 10% 1/4 W
R_{18}	2.2 KΩ ± 10% 1/2 W	R_{50}	1 MΩ ± 10% 1/4 W
R_{19}	22 KΩ ± 10% 1/2 W	R_{51}	100 KΩ ± 10% 1/4 W
R_{20}	100 Ω ± 10% 1/2 W	R_{52}	1 MΩ ± 10% 1/4 W
R_{21}	100 Ω ± 10% 1/2 W	R_{53}	20 KΩ 1 10% 1/4 W
R_{22}	2.2 KΩ ± 10% 1/2 W	R_{54}	1KΩ ± 10% 1/4 W
R_{23}	22 KΩ ± 10% 1/2 W	R_{55}	91 KΩ ± 10% 1/4 W
R_{24}	1 Ω ± 10% 1 W	R_{56}	10 KΩ potentiometer
R_{25}	1 Ω ± 10% 1 W	R_{57}	1 MΩ ± 10% 1/4 W
R_{26}	20 KΩ ± 10% 1/4 W	R_{58}	20 KΩ ± 10% 1/4W
R_{27}	10 KΩ trimpot	R_{59}	1 MΩ ± 10% 1/4 W
R_{28}	100 Ω ± 10% 1/4 W	R_{60}	100 KΩ ± 10% 1/4 W
R_{29}	50 KΩ trimpot	R_{61}	1 MΩ ± 10% 1/4 W
R_{30}	1 KΩ ± 10% 1/4 W	R_{62}	20 KΩ ± 10% 1/4 W
R_{31}	10 KΩ ± 10% 1/4 W	R_{63}	1 KΩ ± 10% 1/4 W
R_{32}	5.6 KΩ ± 10% 1/4 W	R_{64}	1 MΩ ± 10% 1/4 W

Part No.	Model Description	Part No.	Model Description
R_{65}	91 KΩ ± 10% 1/4 W	R_{108}	30 KΩ ± 1% 1/4 W
R_{66}	10 KΩ potentiometer	R_{109}	30 KΩ ± 1% 1/4 W
R_{67}	20 KΩ ± 10% 1/4 W	R_{110}	30 KΩ ± 1% 1/4 W
R_{68}	1 MΩ potentiometer	R_{111}	30 KΩ ± 1% 1/4 W
R_{69}	30 KΩ ± 10% 1/4 W	C_1	0.1 µF 100V DC ceramic
R_{70}	30 KΩ ± 10% 1/4 W	C_2	0.1 µF 100V DC ceramic
R_{71}	1 KΩ ± 1% 1/2 W	C_3	0.1 µF 100V DC ceramic
R_{72}	500 Ω ± 1% 1/4 W	C_4	0.1 µF 100V DC ceramic
R_{73}	100 Ω ± 1% 1/4 W	C_5	0.01 µF 100V DC ceramic
R_{74}	10 Ω ± 1% 1/4 W	C_6	0.2 µF 100V DC ceramic
R_{75}, R_{79} R_{96}, R_{100}	5 MΩ ± 1% 1/4 W	C_7	0.1 µF 100V DC ceramic
		C_8	0.01 µF 100V DC ceramic
		C_9	10 µF 20V DC tantalum
R_{76}, R_{80} R_{97}, R_{101}	3 MΩ ± 1% 1/4 W	C_{10}	0.01 µF 100V DC ceramic
		C_{11}	0.01 µF 100V DC ceramic
R_{77}, R_{81} R_{98}, R_{102}	1 MΩ ± 1% 1/4 W	C_{12}	0.05 µF 100V DC ceramic
		C_{13}	0.1 µF 100V DC ceramic
R_{78}, R_{82} R_{99}, R_{103}	1 MΩ ± 1% 1/4 W	C_{14}	0.56 µF 100V DC orange drop
		C_{15}	1 µF 100V DC orange drop
R_{83}, R_{84}	30 KΩ ± 1% 1/4 W	C_{16}	2.2 µF 50V DC tantalum
R_{85}	30 KΩ ± 1% 1/4 W	L_1	0.01 mH fixed inductor
R_{86}	30 KΩ ± 1% 1/4 W	L_2	0.1 mH fixed inductor
R_{87}, R_{88}	30 KΩ ± 1% 1/4 W	L_3	0.47 mH fixed inductor
R_{89}, R_{90}	30 KΩ ± 1% 1/4 W	L_4	1 mH fixed inductor
R_{112}	1 KΩ precision potentiometer	L_5	2.2 mH fixed inductor
R_{91}	1 KΩ ± 10% 1/4 W	L_6	10 mH fixed inductor
R_{92}	1 KΩ ± 1% 1/2 W	T_1	1:1 push-pull transformer
R_{93}	500 Ω ± 1% 1/4 W	D_1-D_4	1N4448 100 mA 75 volt
R_{94}	100 Ω ± 1% 1/4 W	D_5-D_{12}	1N4003 1 A 200 volt
R_{95}	10 Ω ± 1% 1/4 W	D_{13}	1N34a Germanium diode
R_{104}	30 KΩ ± 1% 1/4 W	D_{14}	1N4448 100 mA 75 volt
R_{105}	30 KΩ ± 1% 1/4 W	D_{15}	1N4448 100 mA 75 volt
R_{106}	30 KΩ ± 1% 1/4 W	Q_1	2N4888 Si pnp transistor
R_{107}	30 KΩ ± 1% 1/4 W	Q_2	F2N5831 Si npn transistor

Part No.	Model Description	Part No.	Model Description
Q_3	2N3666 Si npn transistor	IC_{10}	LM741C
Q_4	2N5979 Si npn power trans.	IC_{11}	LM741C
Q_5	2N4033 Si pnp transistor	IC_{12}	1/4 LM2900n quad amp
Q_6	2N5976 Si pnp power trans.	IC_{13}	LM741C
Q_7	2N4249 Si pnp transistor	IC_{14}	1/4 TL074C quad amp
Q_8	F2N5831 Si npn transistor	IC_{15}	1/4 TL074c
IC_1	LM741C } general purpose	IC_{16}	1/4 TL074C
IC_2	LM741C } op amp	IC_{17}	1/4 TL074C
IC_3	LM143H high voltage op amp	IC_{18}	1/4 TL074C
IC_4	LM143H high voltage op amp	IC_{19}	1/4 TL074C
IC_5	LM340-5 $+5^V$ regulator	IC_{20}	1/4 TL074C
IC_6	LM741C	IC_{21}	1/4 TL074C
IC_7	74121 } monostable	IC_{22}	1/4 TL074C
IC_8	74121 } multivibrator	IC_{23}	1/4 TL074C
IC_9	1/4 LM2900n quad amp	IC_{24}	LM143H

FIGURE CAPTIONS

Fig. 1. (a) A 2-terminal device with associated reference directions for v and i.
(b) A hypothetical voltage-controlled negative resistance device.
(c) A hypothetical current-controlled negative resistance device.

Fig. 2. (a) A 3-terminal device with associated reference directions for v_1, v_2, i_1 and i_2.
(b) A hypothetical family of voltage-controlled negative resistance characteristics.
(c) A hypothetical family of current-controlled negative resistance characteristics.

Fig. 3. (a) Basic circuit for tracing a voltage-controlled negative resistance device.
(b) Basic circuit for tracing a current-controlled negative resistance device.

Fig. 4. (a) Set up for actual measurement.
(b) Photograph of curve tracer.

Fig. 5. (a) Block diagram of curve tracer.
(b) Tracer signal generator circuit.
(c) Staircase signal generator circuit.
(d) Vertical and horizontal measurement circuit.

Fig. 6. (a) Unstable tracing of a 1N3717 tunnel diode without shunt capacitor.
(b) v-i characteristic traced by a 40 Hz sinusoidal signal with a 1 μF shunt capacitance.
(c) v-i characteristic traced by a point-by-point dc measurement with a 1 μF shunt capacitance. All curves are traced with the same series resistance R = 6 Ω.
Horizontal scale: 0.2 volts per division,
Vertical scale: 3.3 mA per division.

Fig. 7. (a) One-port made of a pnp transistor and an n-channel JFET.
(b) Unstable tracing without shunt capacitor.
(c) Stable tracing with 0.1 μF shunt capacitance. All curves are traced with the same series resistance R = 5 Ω.
Horizontal scale: 2 volts per division,
Vertical scale: 20 mA per division.

Fig. 8. (a) One-port made of 2 npn transistors and a battery.
(b) Unstable tracing without shunt capacitor.
(c) Stable tracing with 0.1 μF shunt capacitance. All curves are traced with the same series resistance R = 5 Ω.
Horizontal scale: 0.4 volts per division,
Vertical scale: 4 mA per division.

Fig. 9. (a) One-op-amp negative-resistance one-port.
(b) v-i characteristic traced without shunt capacitance; R = 100 Ω.
Horizontal scale: 4 volts per division,
Vertical scale: 0.5 mA per division.

Fig. 10. (a) Two-op-amp negative resistance one-port.
(b) v-i characteristic traced without shunt capacitor; R = 100 Ω.
Horizontal scale: 4 volts per division.
Vertical Scale: 2.5 mA per division.

Fig. 11. (a) Three-op-amp negative resistance one-port.
(b) v-i characteristic traced without shunt capacitor; R = 100 Ω.

Horizontal scale: 4 volts per division.
Vertical scale: 0.5 mA per division.

Fig. 12. (a) A current-controlled negative resistance one-port made of an npn transistor and an n-channel JFET.
(b) v-i characteristic traced without series inductance.
(c) v-i characteristic traced with 2 mH series inductance.
All curves are traced with $G = 8.8 \times 10^{-6}$ mho.
Horizontal scale: 2 volts per division.
Vertical scale: 10 mA per division.

Fig. 13. (a) A current-controlled negative resistance one-port made of 2 npn transistors.
(b) v-i characteristic traced without series inductor.
(c) v-i characteristic traced with 3 mH series inductance.
All curves are traced with $G = 8.8 \times 10^{-6}$ mho.
Horizontal scale: 1 volt per division.
Vertical scale: 0.5 mA per division.

Fig. 14. (a) A current-controlled negative resistance one-port made of 2 pnp transistors.
(b) v-i characteristic traced without series inductance; $G = 8.8 \times 10^{-1}$ mho.
Horizontal scale: 0.4 volt per division.
Vertical scale: 2 mA per division.

Fig. 15. (a) A current-controlled negative resistance one-port made of an npn transistor and a pnp transistor.
(b) v-i characteristic traced without series inductor; $G = 8.8 \times 10^{-6}$ mho.
Horizontal scale: 2 volts per division.
Vertical scale: 0.5 mA per division.

Fig. 16. (a) A current-controlled negative resistance one-port made of an npn and a pnp transistor.
(b) v-i characteristic traced without series inductor; $G = 8.8 \times 10^{-6}$ mho.
Horizontal scale: 0.4 volts per division.
Vertical scale: 2 mA per division.

Fig. 17. (a) A current-controlled negative resistance one-port made of five op-amps
(b) v-i characteristic traced without series inductor; $G = 8.8 \times 10^{-6}$ mho.
Horizontal scale: 1 volt per division.
Vertical scale: 5 mA per division.

Fig. 18. (a) A voltage-controlled negative resistance 2-port.
(b) v_1-i_1 characteristics (with i_2 as parameter) traced without shunt capacitor.
(c) v_1-i_1 characteristics (with i_2 as parameter) traced with 0.1 μF capacitor; $R = 10\ \Omega$.
Horizontal scale: 2 volts per division.
Vertical scale: 20 mA per division.
Current step: -0.2 mA per step.

Fig. 19. (a) A current-controlled negative resistance 2-port.
(b) v_1-i_1 characteristics (with i_2 as parameter) traced without series inductance.
(c) v_1-i_1 characteristics (with i_2 as parameter) traced with 6.7 mH series inductance; $G = 8.8 \times 10^{-6}$ mho.
Horizontal scale: 1 volt per division.
Vertical scale: 2 mA per division.

Fig. 20. (a) A 2-port made of a pnp transistor and an npn transistor.
(b) Current-controlled representation.
Horizontal scale: 1 mA per division.
Vertical scale: 5 volts per division.
(c) Voltage-controlled representation.
Horizontal scale: 1 volt per division.
Vertical scale: i_1: 2 mA per division, i_2: 5 mA per division.
(d) Hybrid-1 representation.
Horizontal scale: v_1: 5 volts per division, i_2: 4 mA per division.
Vertical scale: i_1: 2 mA per division, v_2 = 2.5 volts per division.
(e) Hybrid-2 representation.
Horizontal scale: i_1: 4 mA per division, v_2: 2 volts per division.
Vertical scale: v_1: 2.5 volts per division, i_2: 1 mA per division.
(f) Transmission-1 representation.
Horizontal scale: v_2: 0.5 volt per division, i_2: 1 mA per division.
Vertical scale: v_1: 1 volt per division, i_1: 1 mA per division.
(g) Transmission-2 representation.
Horizontal scale: v_1: 0.5 volt per division, i_1: 1 mA per division.
Vertical scale: v_2: 1 volt per division, i_2: 1 mA per division.

Fig. 21. (a) Circuit model for a type N device.
(b) Circuit model for a type S device.

Fig. 22. (a) Curve tracer circuit model for type N device.
(b) Curve tracer circuit model for type S device.

Fig. 23. (a) When $R > \frac{1}{G_{max}}$, load line intersects the v_R-i_R characteristic at 3 points.
(b) When $R < \frac{1}{G_{max}}$, load line intersects the v_R-i_R characteristic at only one point.

Fig. 24. (a) Shaded region shows allowed parameter range for R and C for small L.
(b) Shaded region shows allowed parameter range for R and C for large L.

Fig. 25. Real part of s plotted as a function of C with all other parameters held constant.

Fig. 26. (a) Connecting a voltage source $v_s(t)$ and a current source $i_s(t)$ in parallel with port 1 is equivalent to just connecting the voltage source $v_s(t)$ alone.
(b) Connecting a current source $i_s(t)$ and a voltage source $v_s(t)$ in series with port 1 is equivalent to just connecting the current source $i_s(t)$ alone.

Fig. 27. (a) Connecting a nullator in series with the voltage source and a norator across port 2.
(b) Ideal op amp model in the linear region with infinite gain.
(c) Practical op amp circuit for tracing the transmission representation 2.

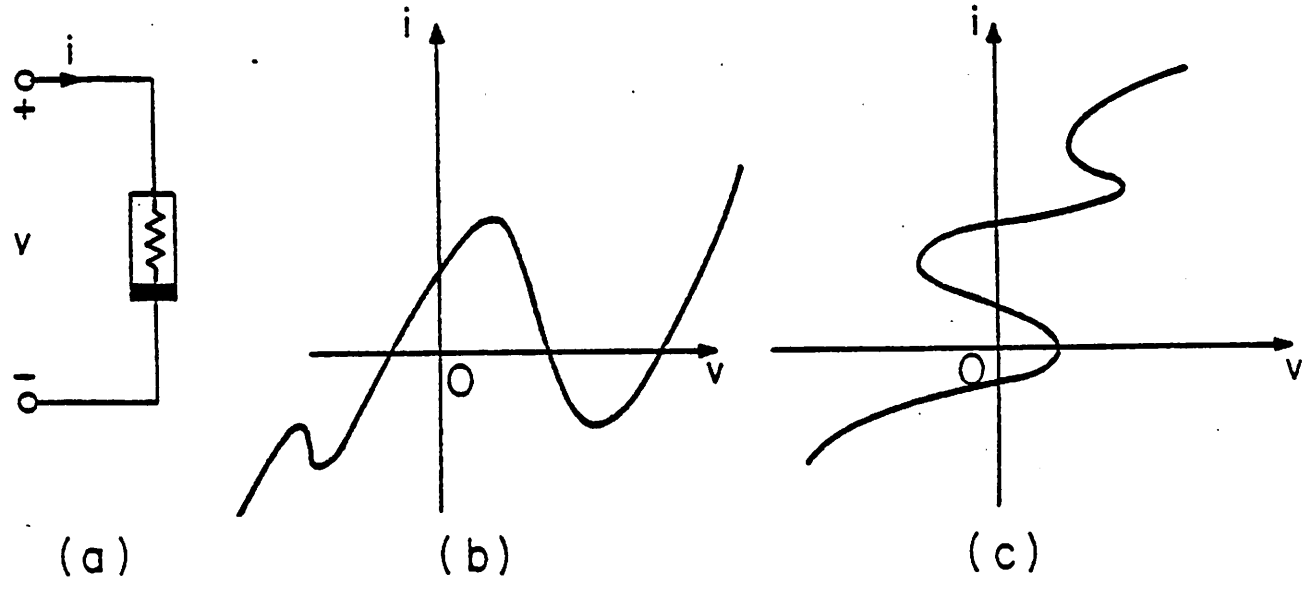


Fig. 1

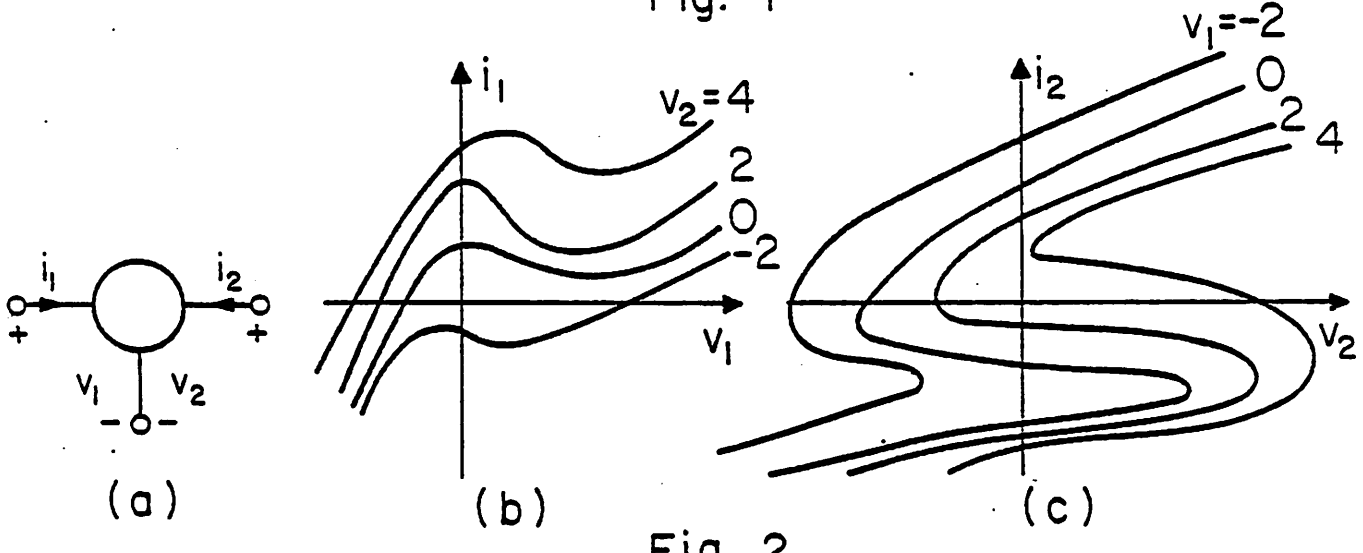


Fig. 2

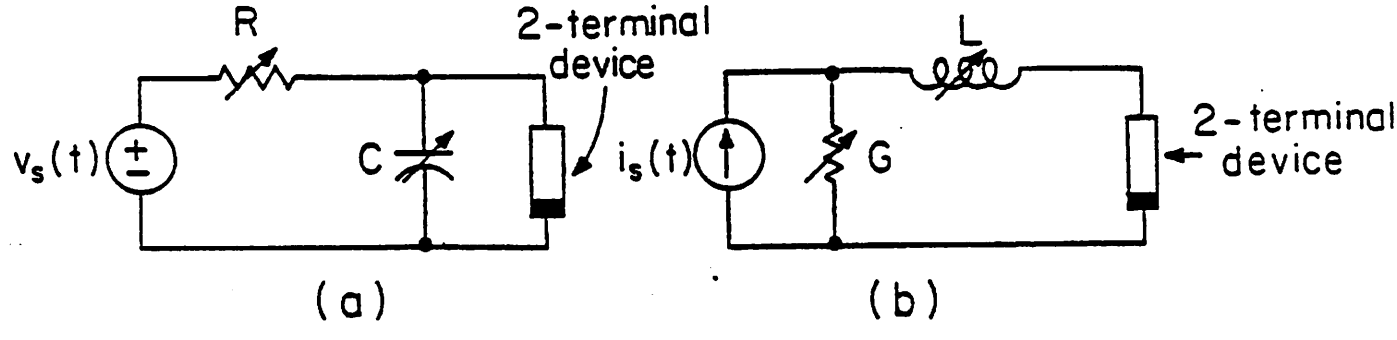
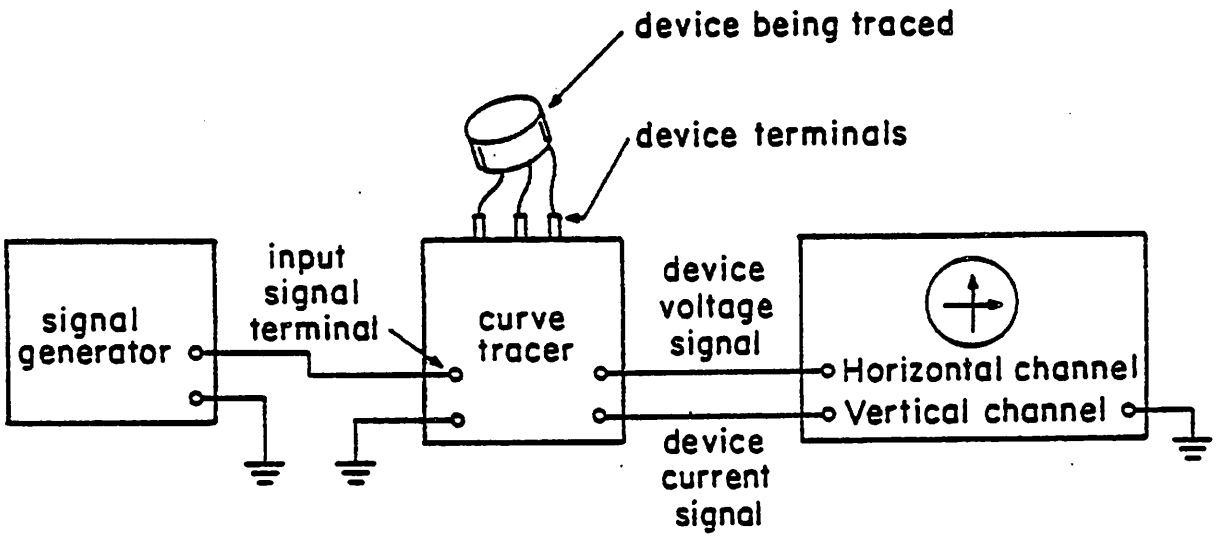
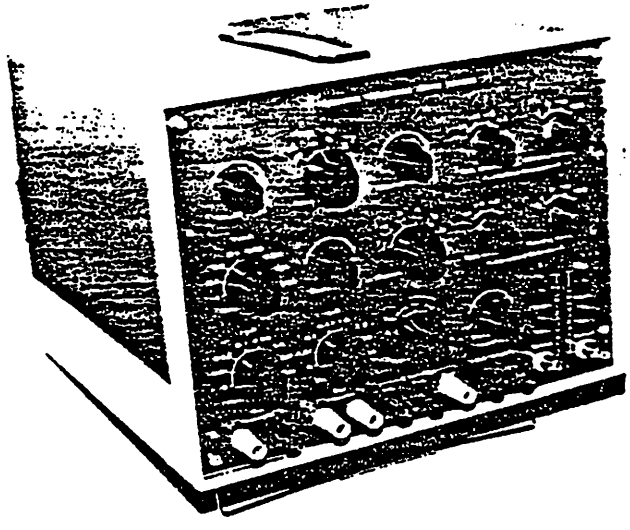


Fig. 3


device being traced
device terminals
signal generator
input signal terminal
curve tracer
device voltage signal
device current signal
Horizontal channel
Vertical channel

(a)



(b)

Fig. 4

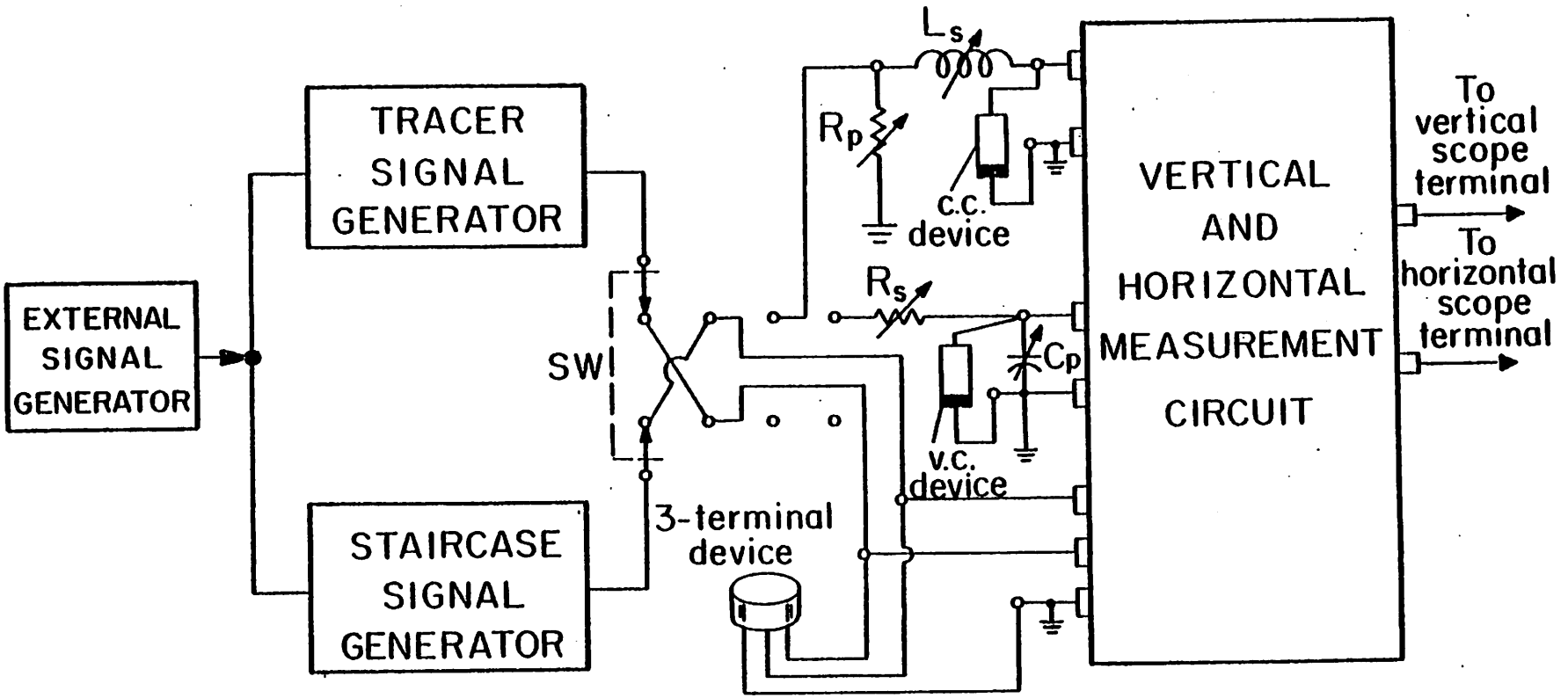

EXTERNAL SIGNAL GENERATOR
TRACER SIGNAL GENERATOR
STAIRCASE SIGNAL GENERATOR
SW
3-terminal device
L_s
R_p
C.C. device
R_s
C_p
V.C. device
VERTICAL AND HORIZONTAL MEASUREMENT CIRCUIT
To vertical scope terminal
To horizontal scope terminal

Fig. 5(a)

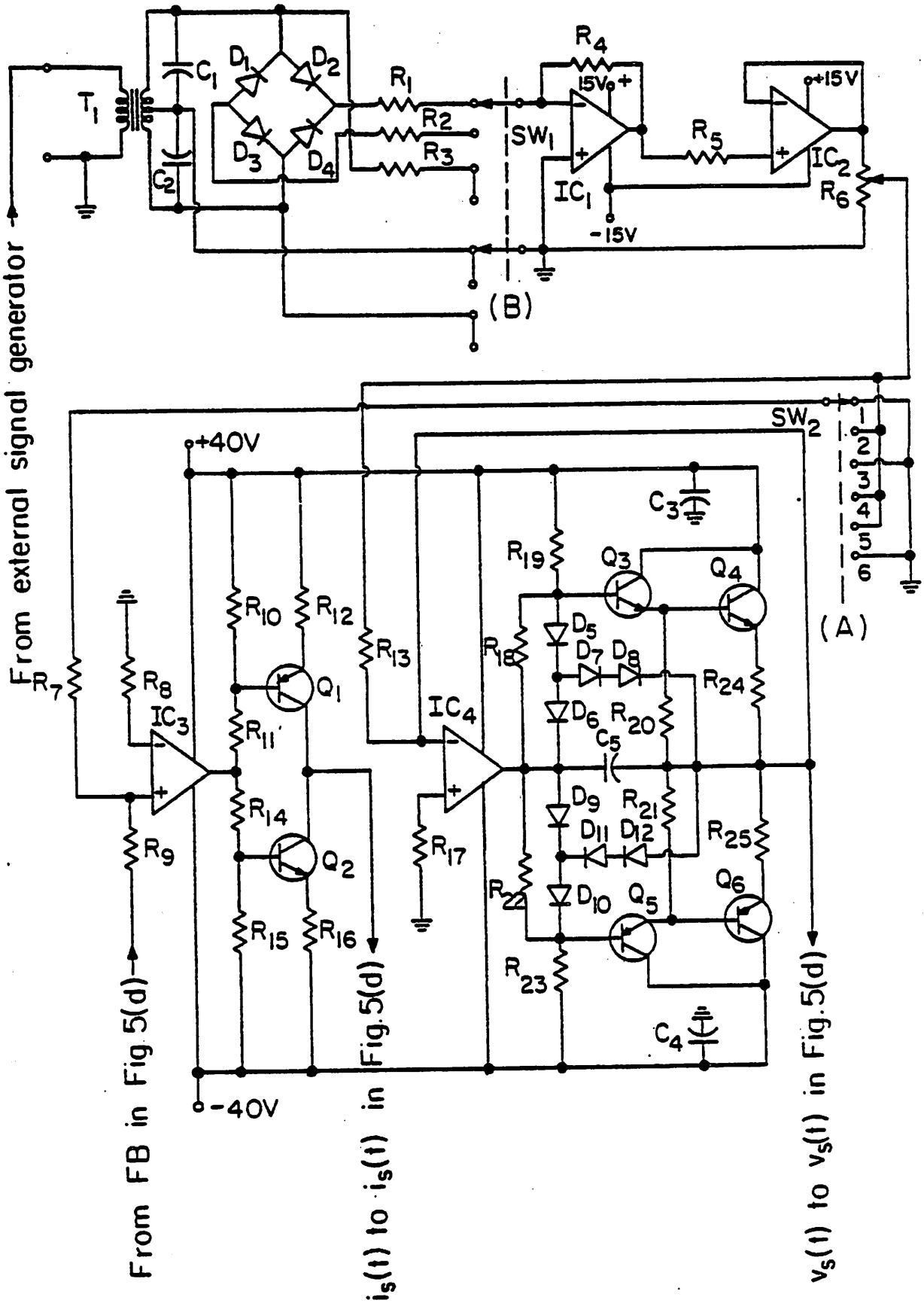

From external signal generator
T1
C1
C2
D1
D2
D3
D4
R1
R2
R3
R4
15V
+15V
SW1
IC1
IC2
R5
R6
-15V
(B)
SW2
(A)
+40V
-40V
C3
R19
Q3
Q4
D5
D7
D8
R18
R24
D6
R20
C5
R10
R12
R13
Q1
R8
R7
IC3
IC4
R11
R14
R9
Q2
R15
R16
R17
D9
R21
D11
D12
R25
R22
D10
Q5
Q6
R23
C4
From FB in Fig 5(d)
is(t) to is(t) in Fig.5(d)
vs(t) to vs(t) in Fig.5(d)

Fig. 5(b)

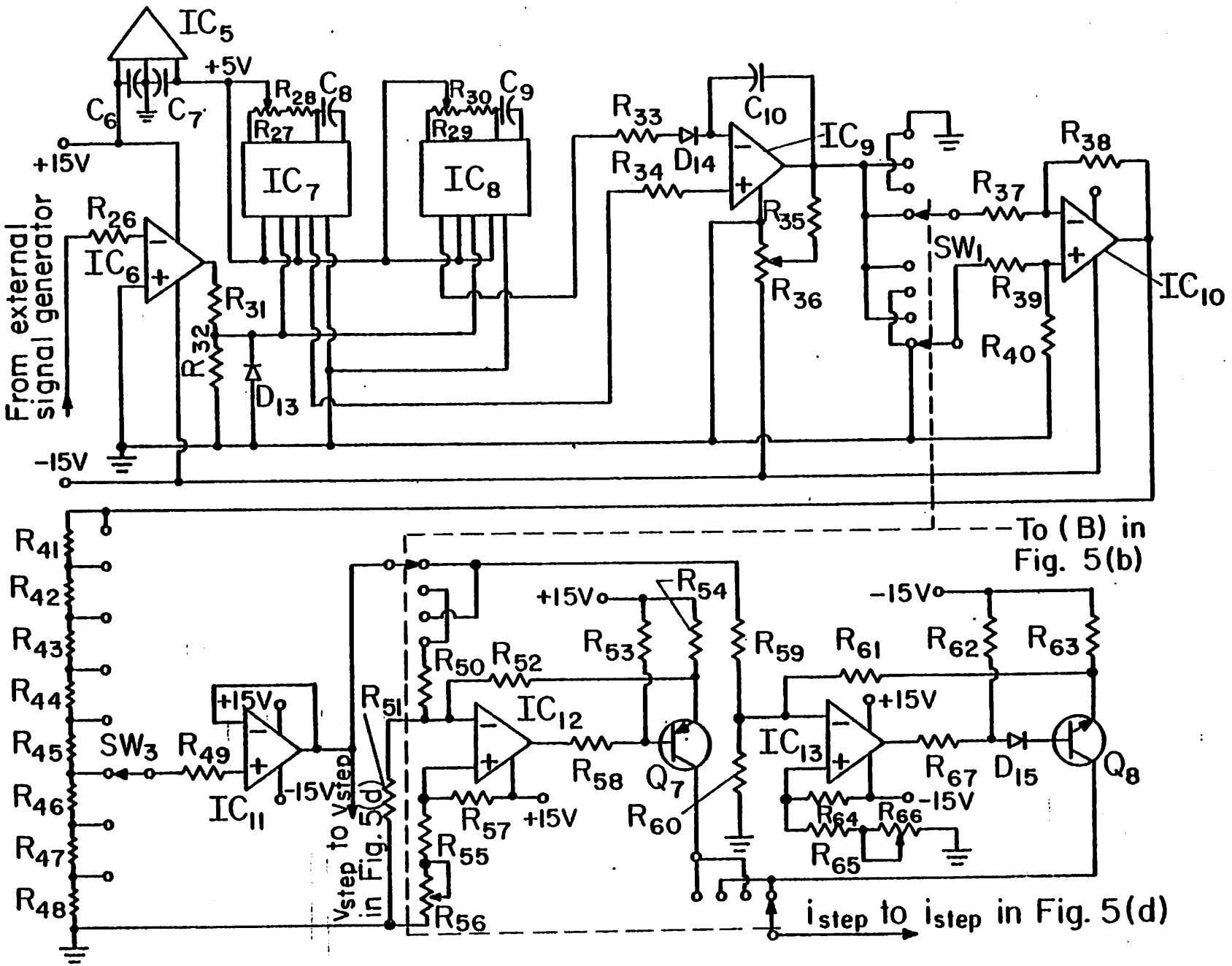

IC5
+5V
C6
C7
R28
C8
R27
IC7
R30
C9
R29
IC8
R33
R34
D14
C10
IC9
R38
R37
R35
R36
SW1
R39
R40
IC10
+15V
From external signal generator
R26
IC6
R31
R32
D13
-15V
To (B) in Fig. 5(b)
R41
R42
R43
R44
R45
R46
R47
R48
SW3
R49
+15V
IC11
-15V
Vstep to Vstep in Fig. 5(d)
R51
R50
R52
IC12
R57
+15V
R55
R56
R54
R53
R59
R58
Q7
R60
R61
R62
R63
IC13
R67
D15
Q8
R64
R66
R65
istep to istep in Fig. 5(d)

Fig. 5(c)

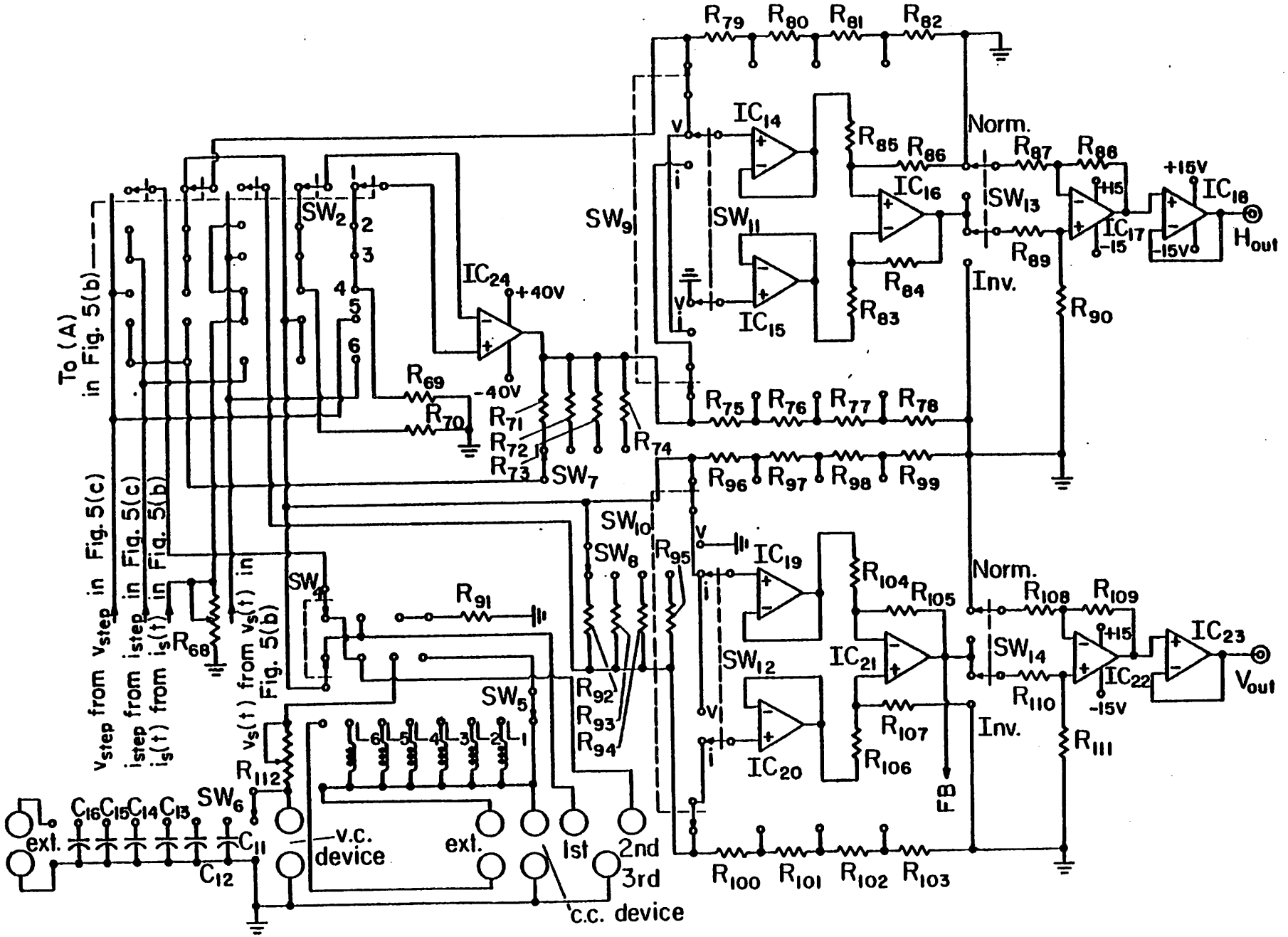

R79 R80 R81 R82
IC14
R85 R86
Norm.
R87 R88
+15V
IC16
SW13
IC18
SW2
SW9
SW11
IC17
Hout
IC24
+40V
R89
IC15
R84
Inv.
R83
R90
To (A) in Fig. 5(b)
R69
-40V
R70
R71
R72
R73
SW7
R74
R75 R76 R77 R78
R96 R97 R98 R99
SW10
SW8
R95
IC19
R104 R105
Norm.
R108 R109
IC23
SW14
IC22
Vout
SW12
IC21
R110
R107
Inv.
R111
IC20
R106
FB
R100 R101 R102 R103
R91
R68
SW5
R92
R93
R94
R112
SW6
C16 C15 C14 C13
C11
C12
ext.
v.c. device
ext.
1st
2nd
3rd
c.c. device
vstep from vstep in Fig. 5(c)
istep from istep in Fig. 5(c)
is(t) from is(t) in Fig. 5(b)
vs(t) from vs(t) in Fig. 5(b)

Fig. 5(d)

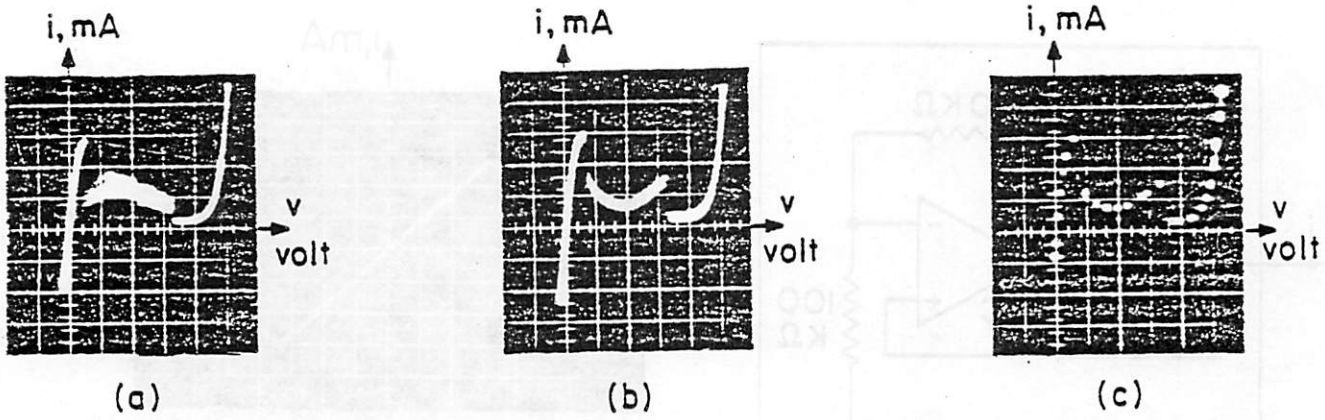


Fig. 6

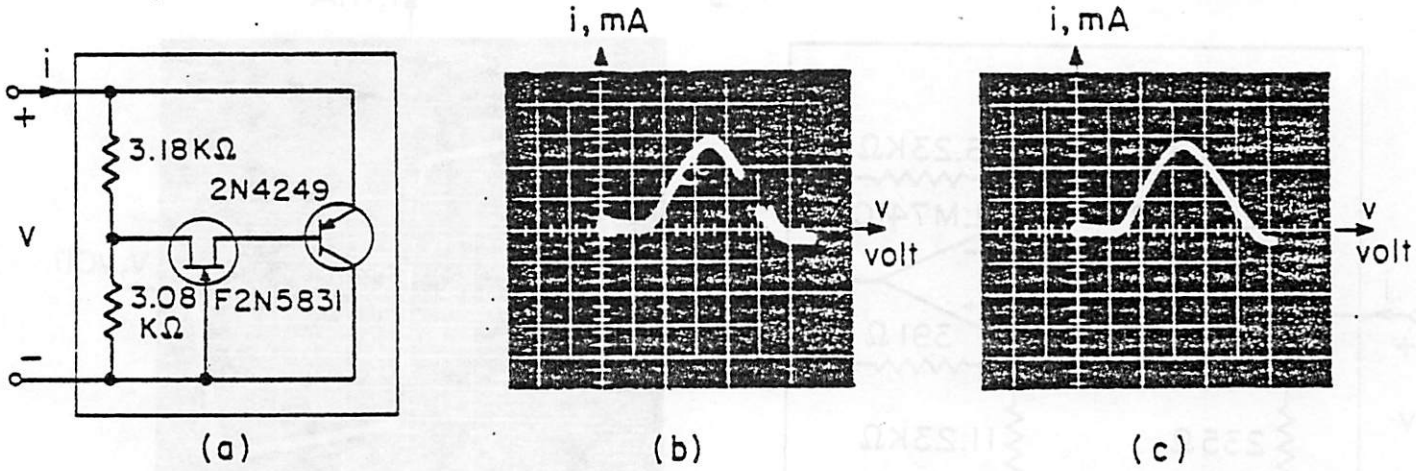


Fig. 7

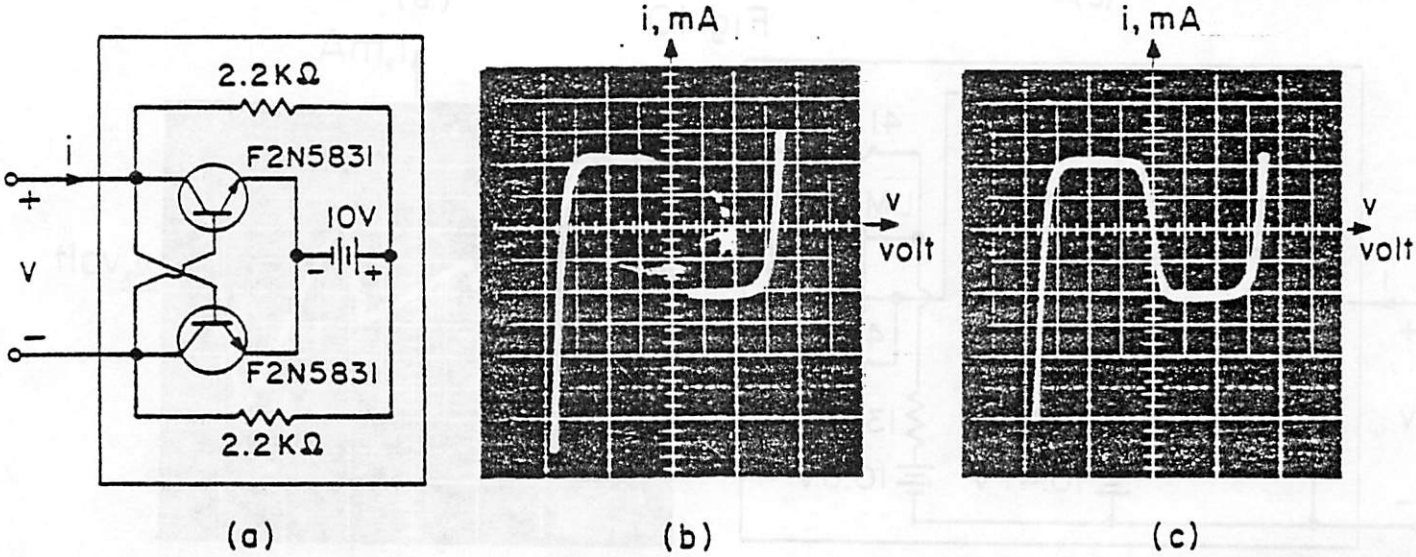
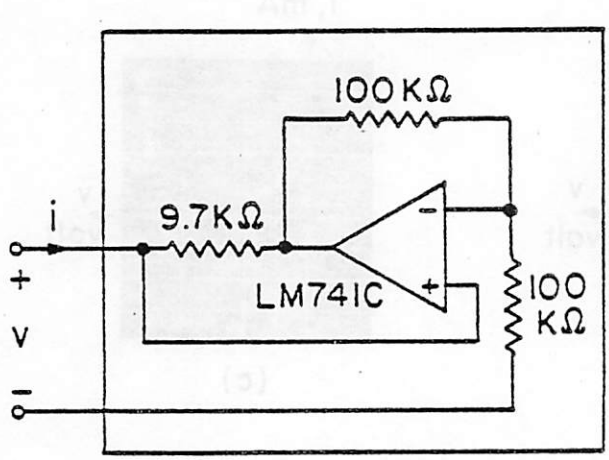
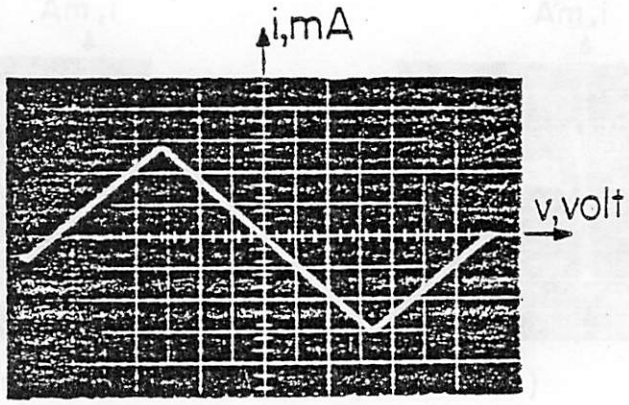


Fig. 8

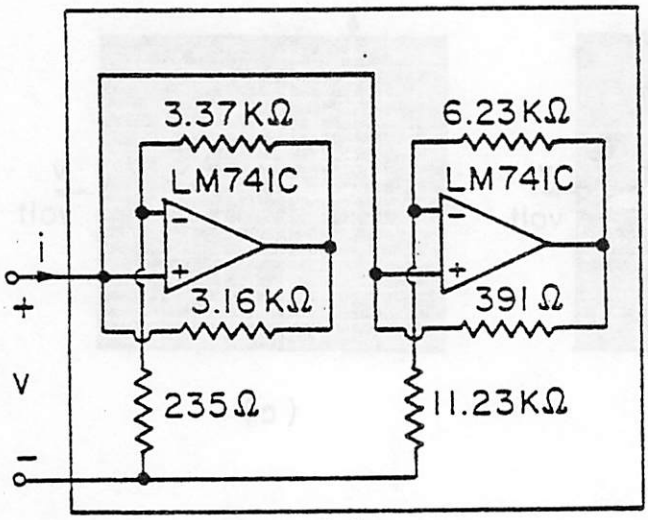


(a)

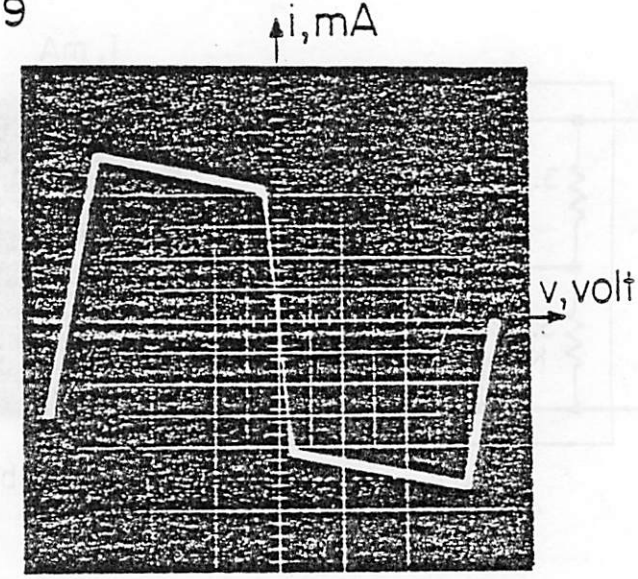


(b)

Fig. 9

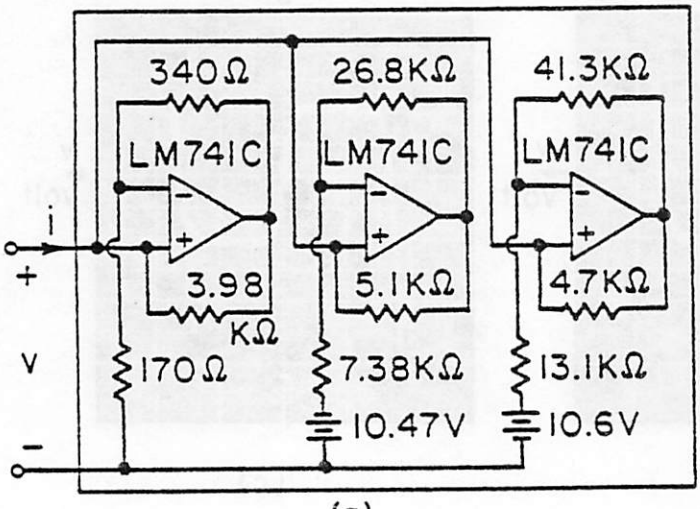


(a)

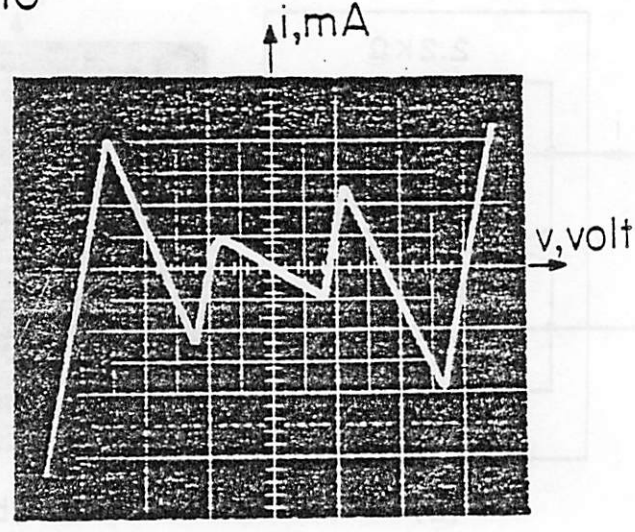


(b)

Fig. 10

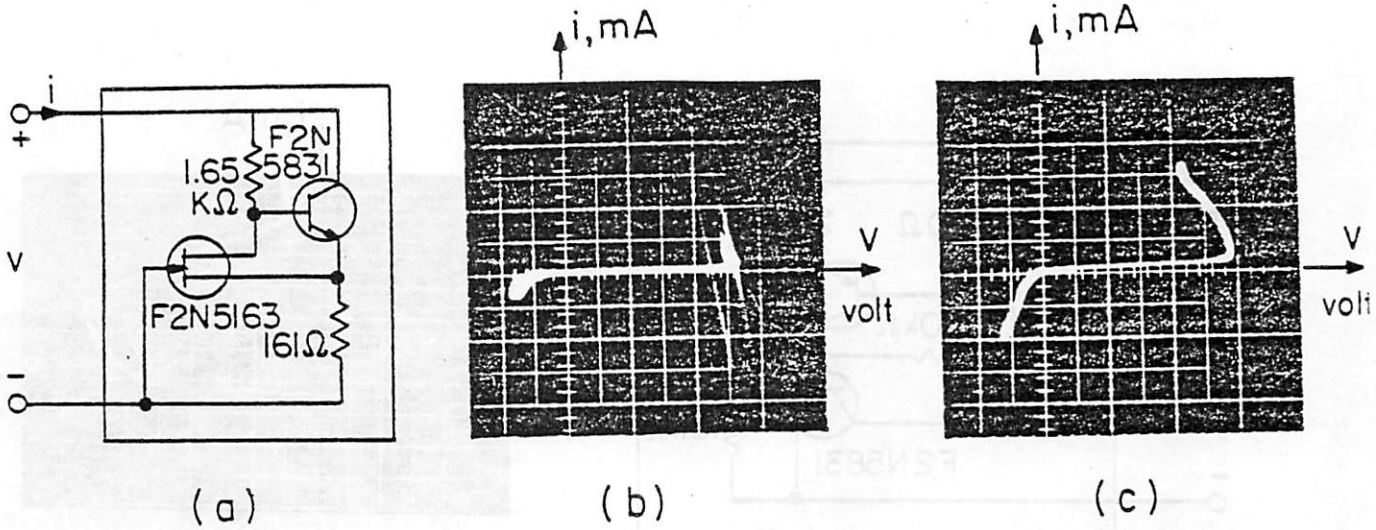


(a)



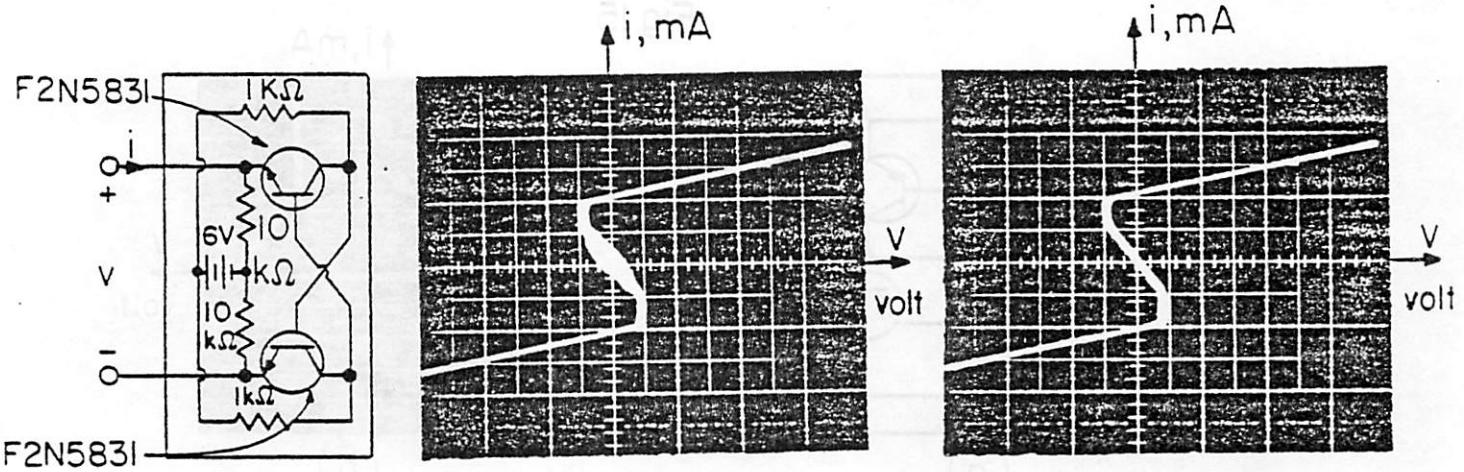
(b)

Fig. 11



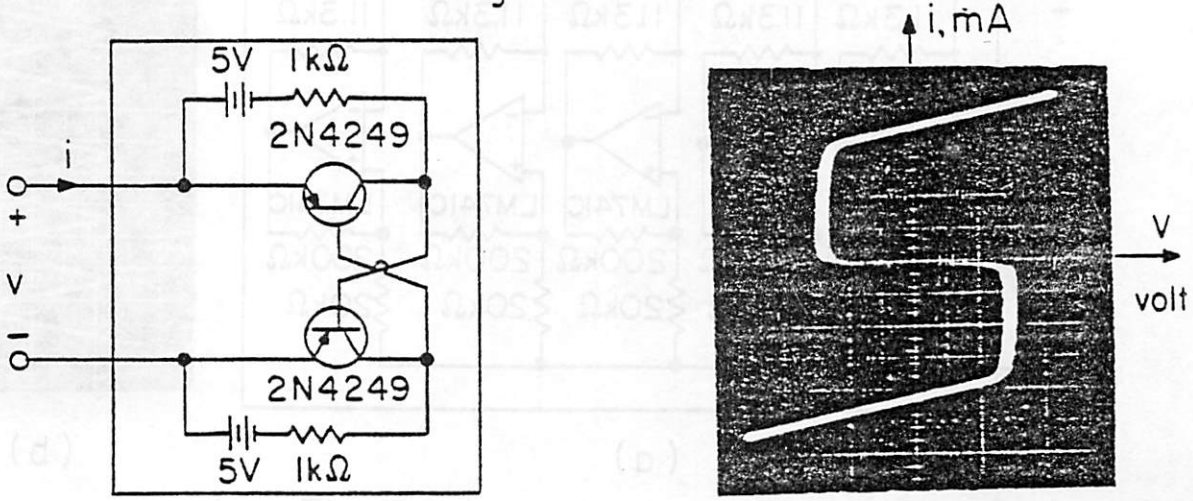
(a) (b) (c)

Fig. 12



(a) (b) (c)

Fig. 13



(a) (b)

Fig. 14

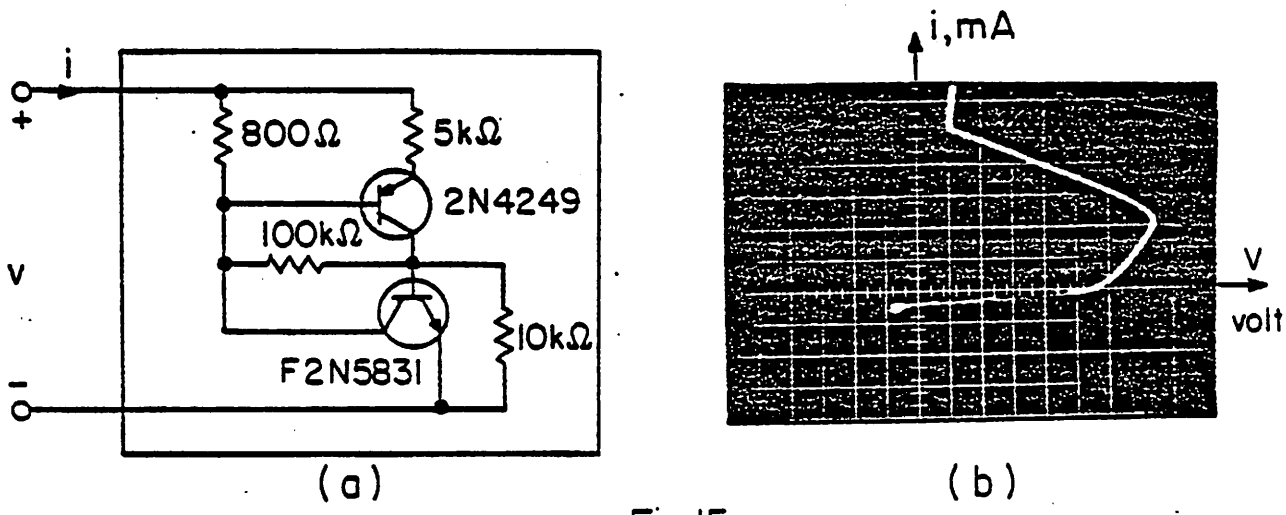


Fig.15

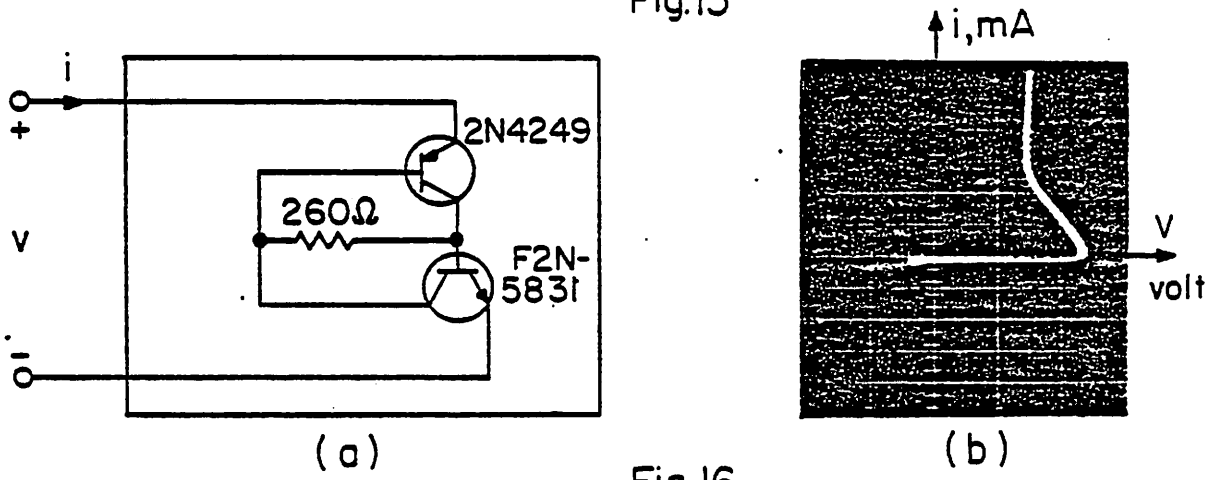


Fig.16

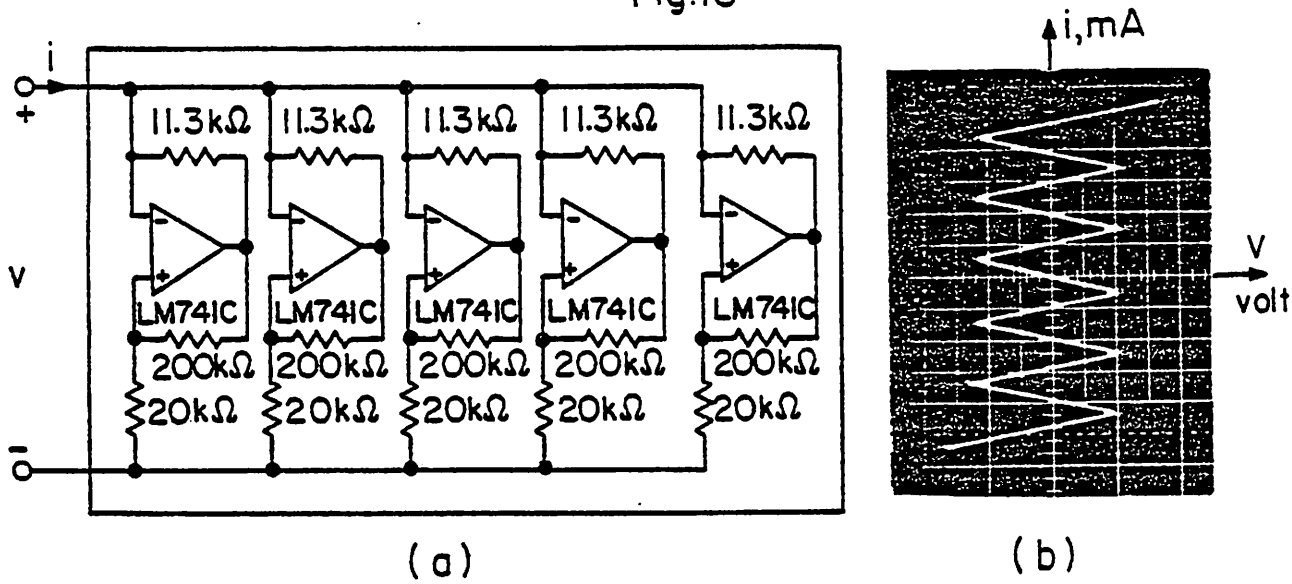


Fig. 17

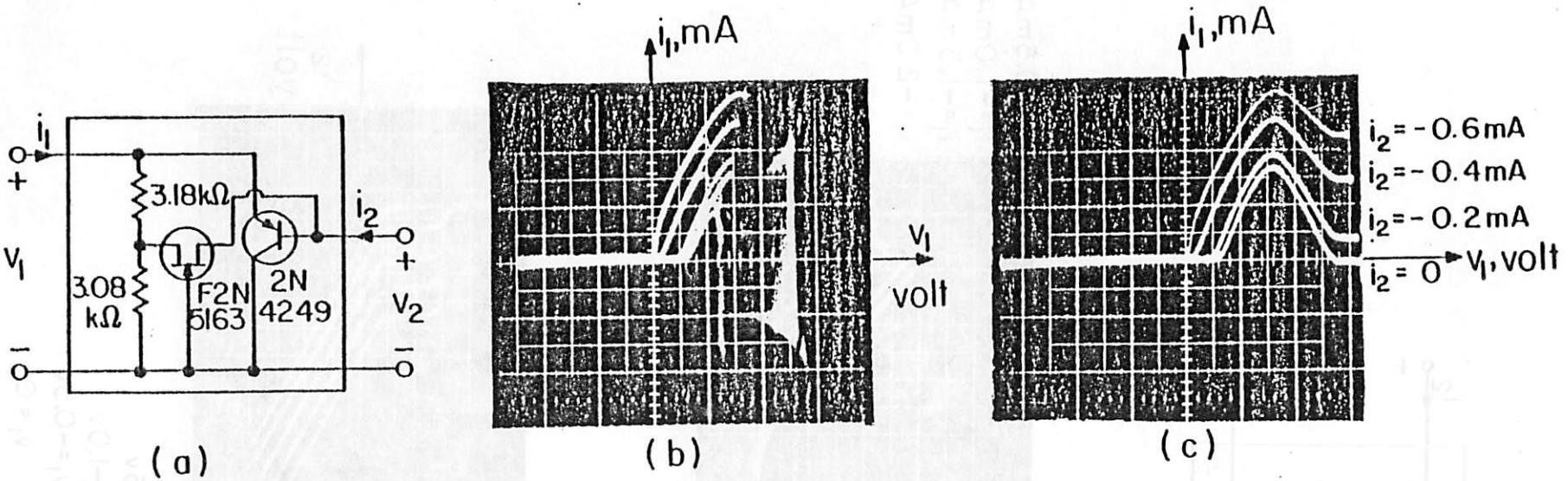

i1
+
V1
−
3.18kΩ
3.08
kΩ
F2N
5163
2N
4249
i2
+
V2
−
(a)
i1,mA
V1
volt
(b)
i1,mA
i2 = - 0.6mA
i2 = - 0.4mA
i2 = - 0.2mA
i2 = 0
V1, volt
(c)

Fig. 18

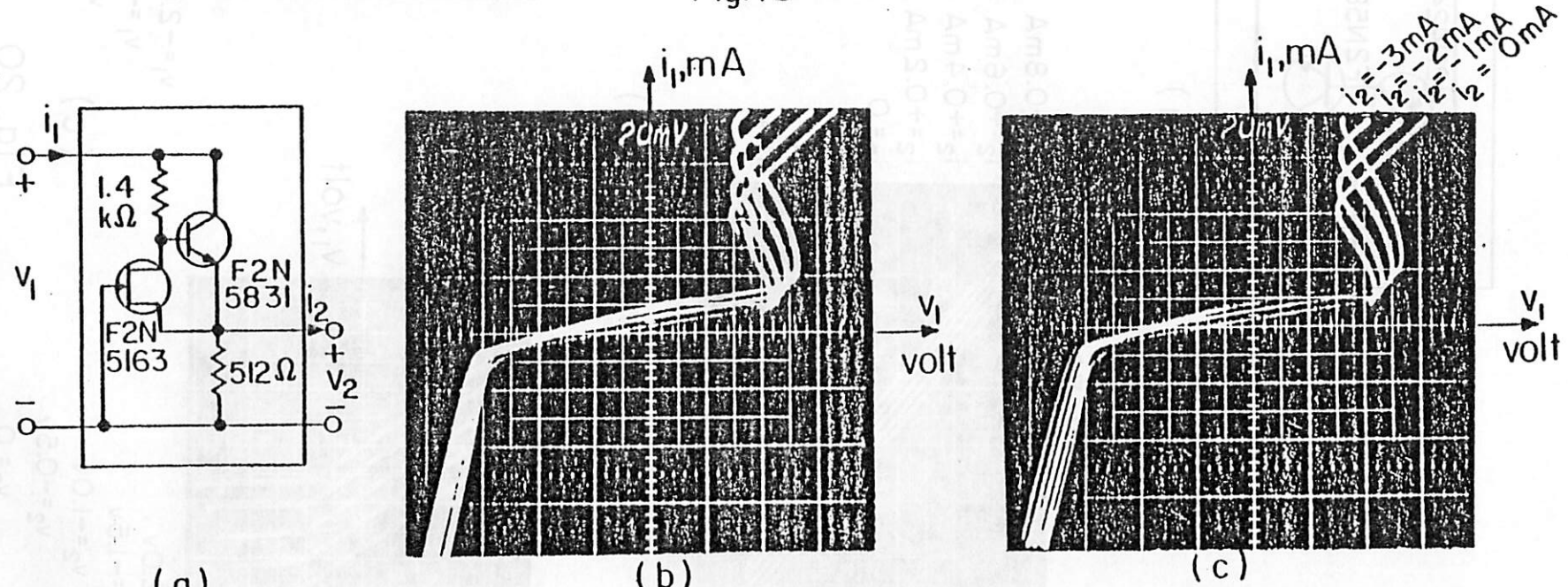
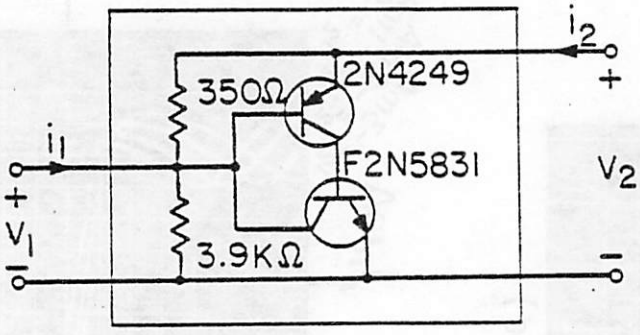
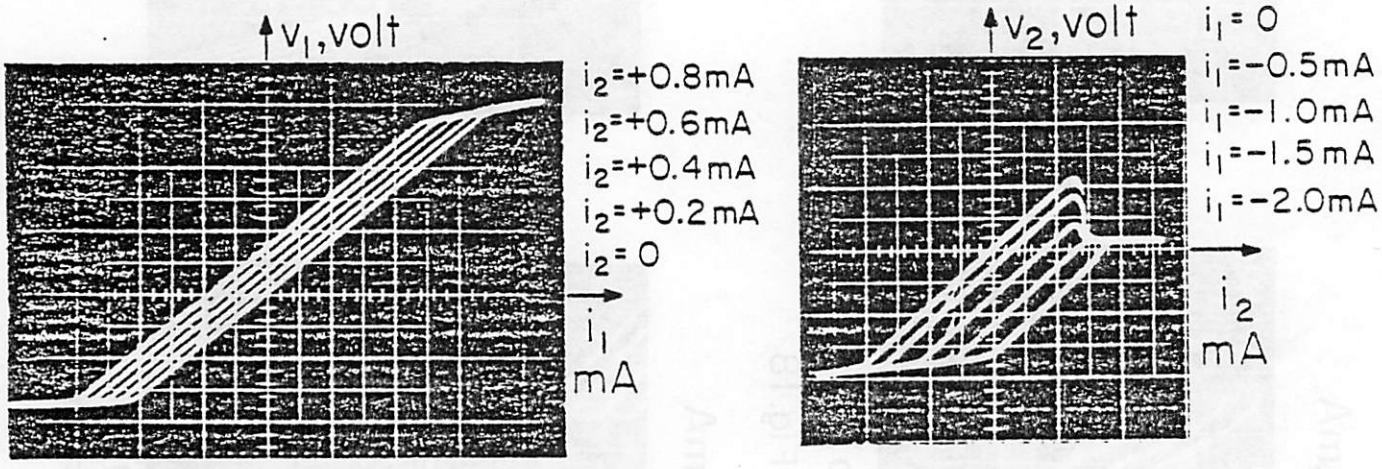

i1
+
V1
−
1.4
kΩ
F2N
5831
F2N
5163
512Ω
i2
+
V2
−
(a)
i1,mA
20mV
V1
volt
(b)
i1,mA
i2 = -3mA
i2 = -2mA
i2 = -1mA
i2 = 0mA
20mV
V1
volt
(c)

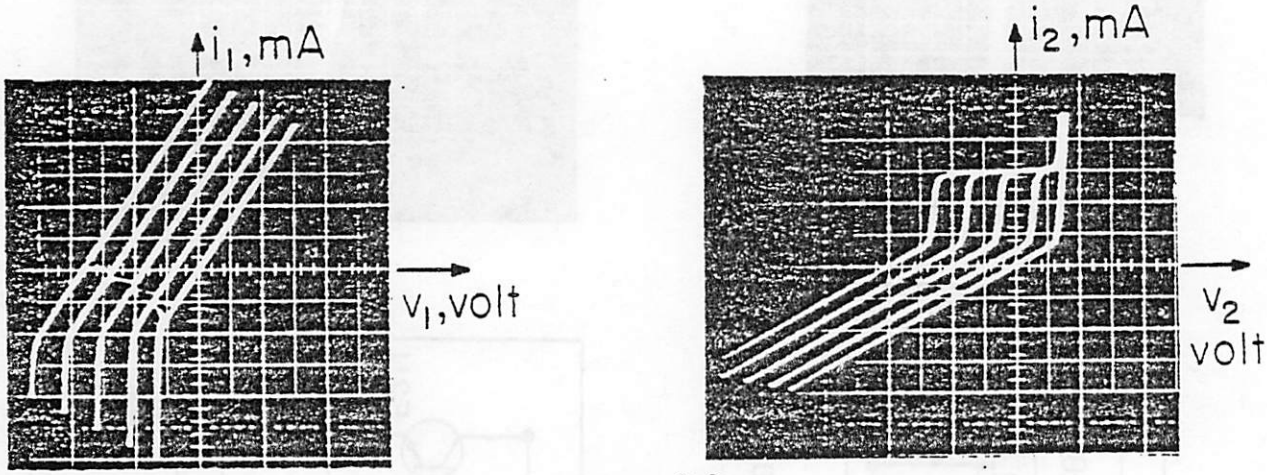
Fig. 19



(a)



(b)



v_2=−2.0v
v_2=−1.5v
v_2=−1.0v
v_2=−0.5v
v_2=0

(c)

v_1=−2.0v
v_1=−1.5v
v_1=−1.0v
v_1=−0.5v
v_1=0

Fig. 20

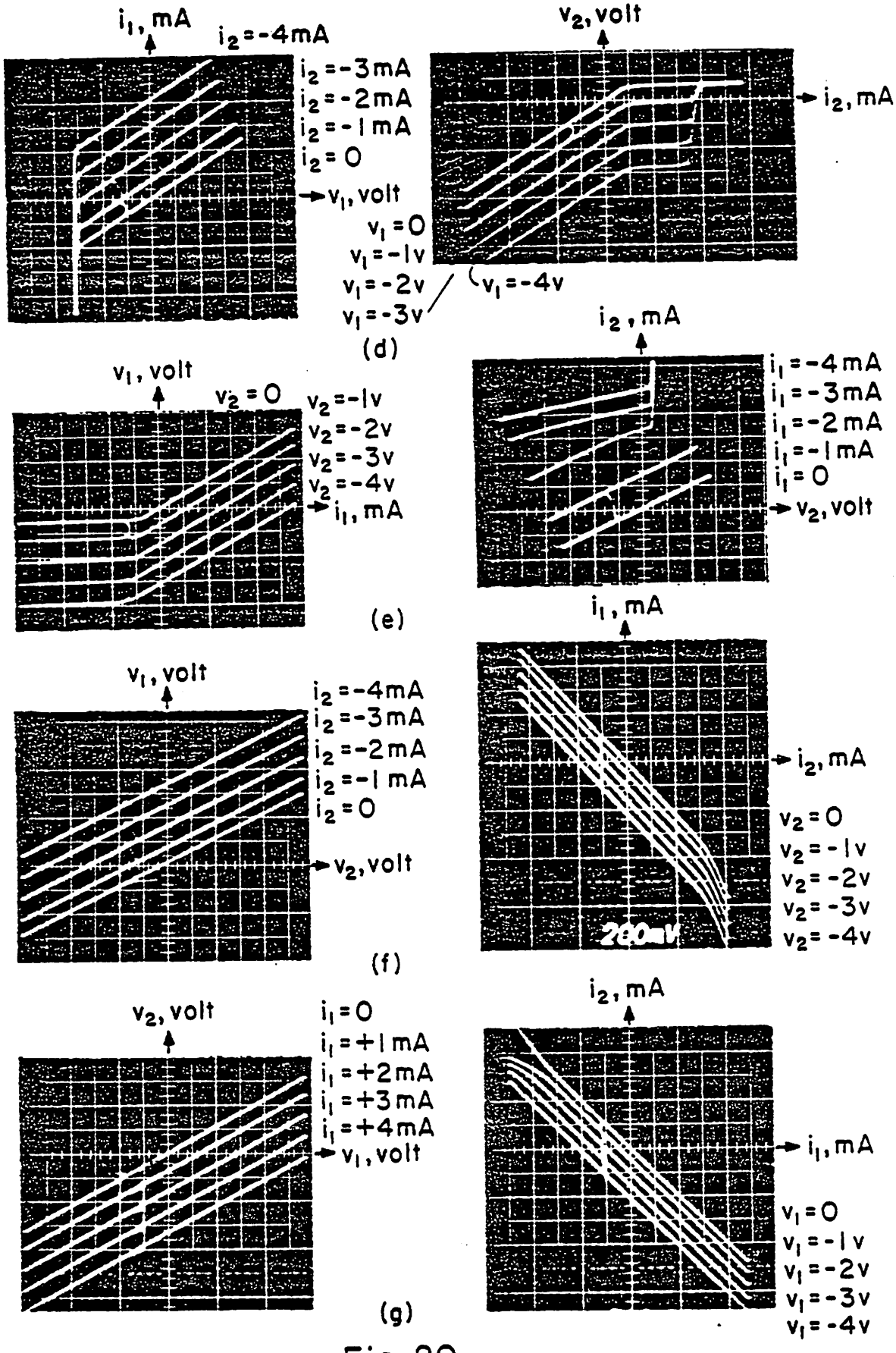

i1, mA
i2 = -4mA
i2 = -3mA
i2 = -2mA
i2 = -1mA
i2 = 0
v1, volt
v2, volt
i2, mA
v1 = 0
v1 = -1v
v1 = -2v
v1 = -3v
v1 = -4v
(d)
v1, volt
v2 = 0
v2 = -1v
v2 = -2v
v2 = -3v
v2 = -4v
i1, mA
i2, mA
i1 = -4mA
i1 = -3mA
i1 = -2mA
i1 = -1mA
i1 = 0
v2, volt
(e)
v1, volt
i2 = -4mA
i2 = -3mA
i2 = -2mA
i2 = -1mA
i2 = 0
v2, volt
i1, mA
i2, mA
v2 = 0
v2 = -1v
v2 = -2v
v2 = -3v
v2 = -4v
(f)
v2, volt
i1 = 0
i1 = +1mA
i1 = +2mA
i1 = +3mA
i1 = +4mA
v1, volt
i2, mA
i1, mA
v1 = 0
v1 = -1v
v1 = -2v
v1 = -3v
v1 = -4v
(g)

Fig. 20

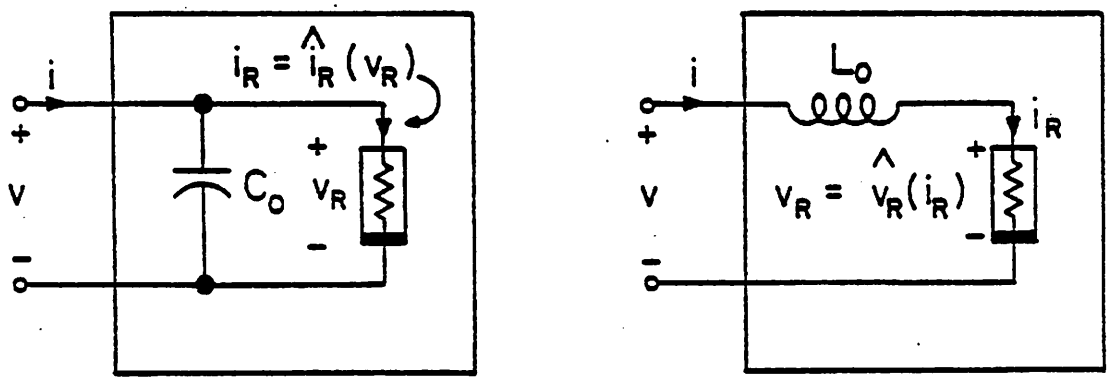
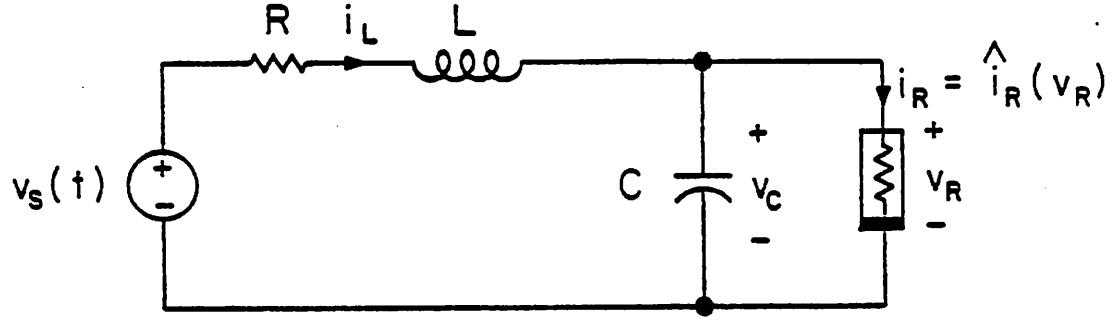
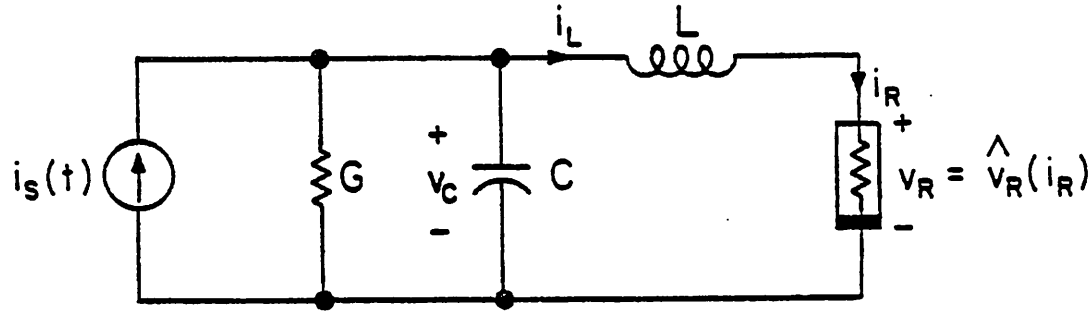


Fig. 21



(a)



(b)

Fig. 22

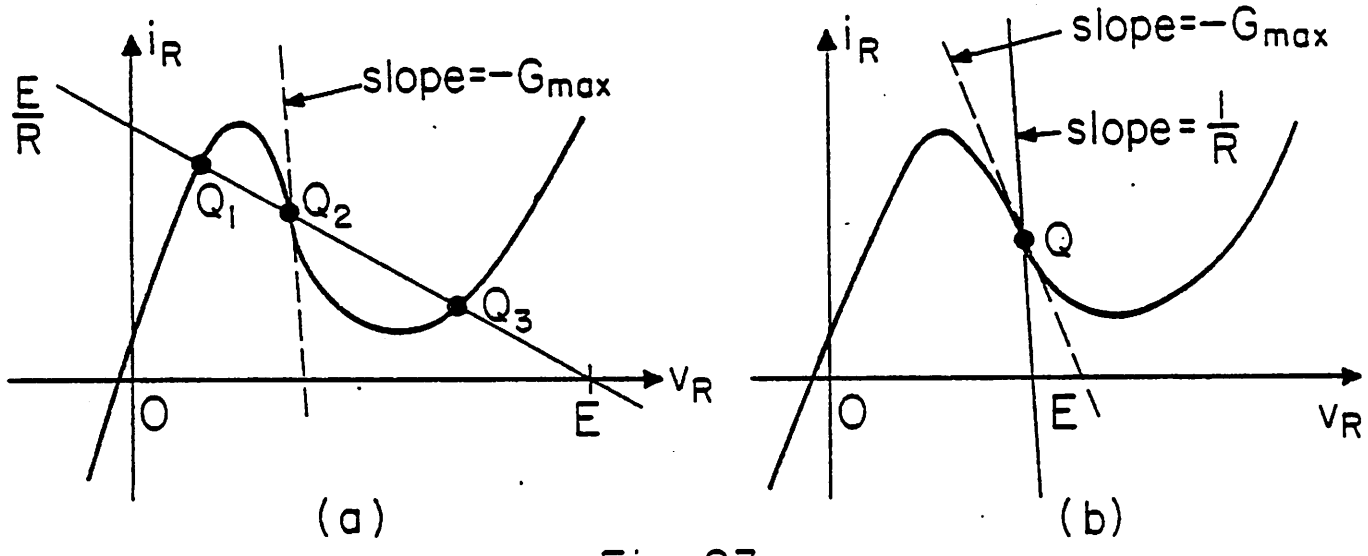
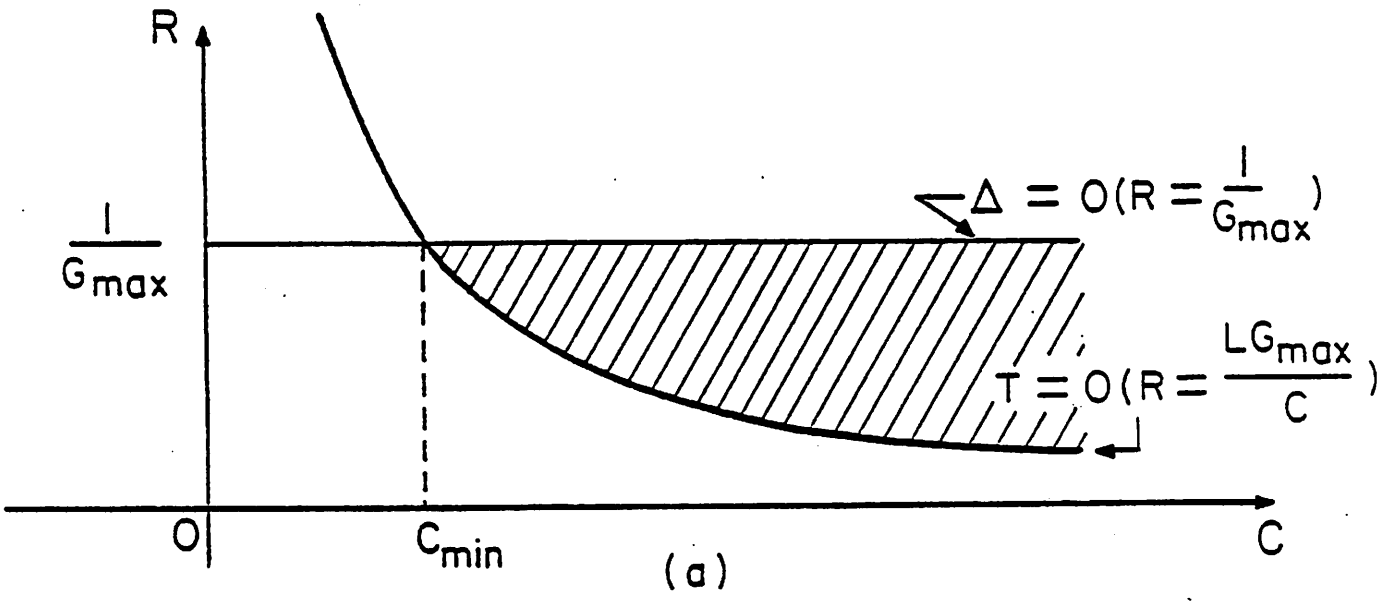
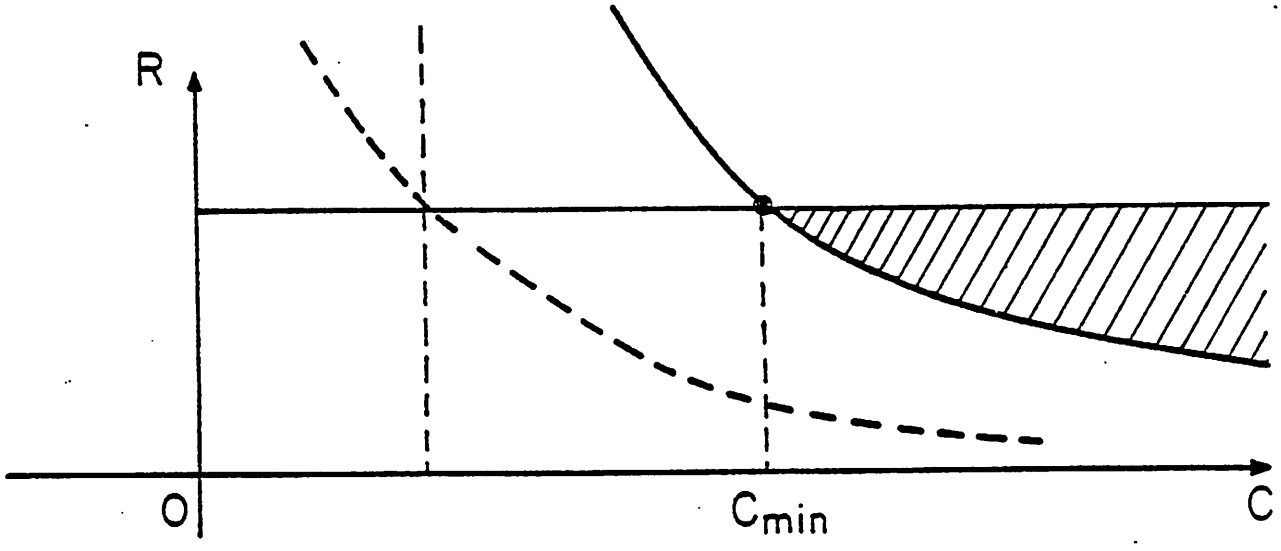

i_R
$\frac{E}{R}$
slope=$-G_{max}$
Q_1
Q_2
Q_3
O
E
V_R
(a)
i_R
slope=$-G_{max}$
slope=$\frac{1}{R}$
Q
O
E
V_R
(b)

Fig. 23



(a)



(b)

Fig.24

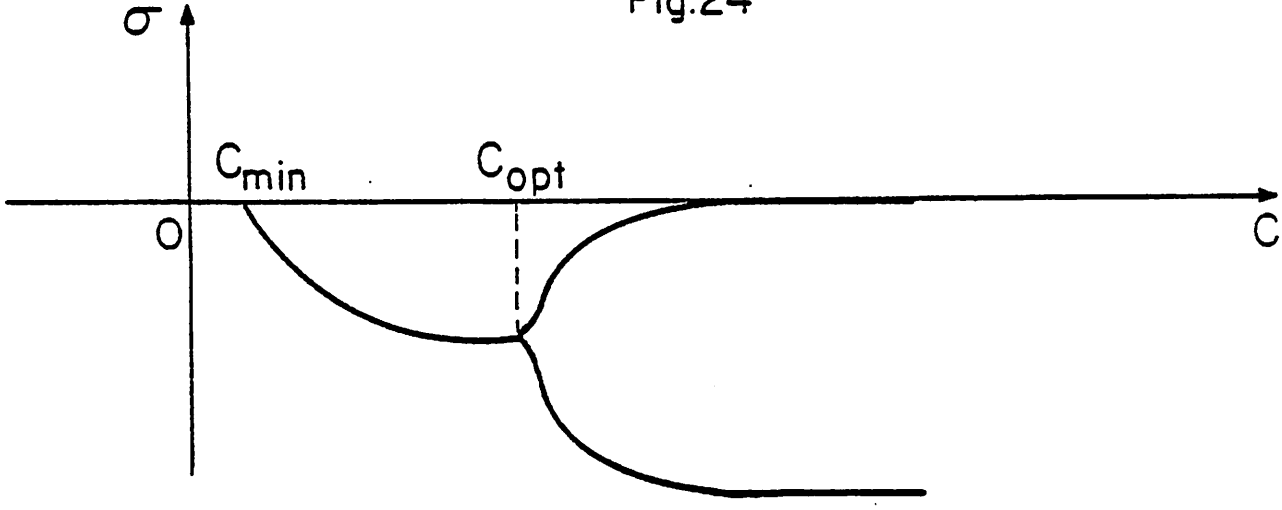
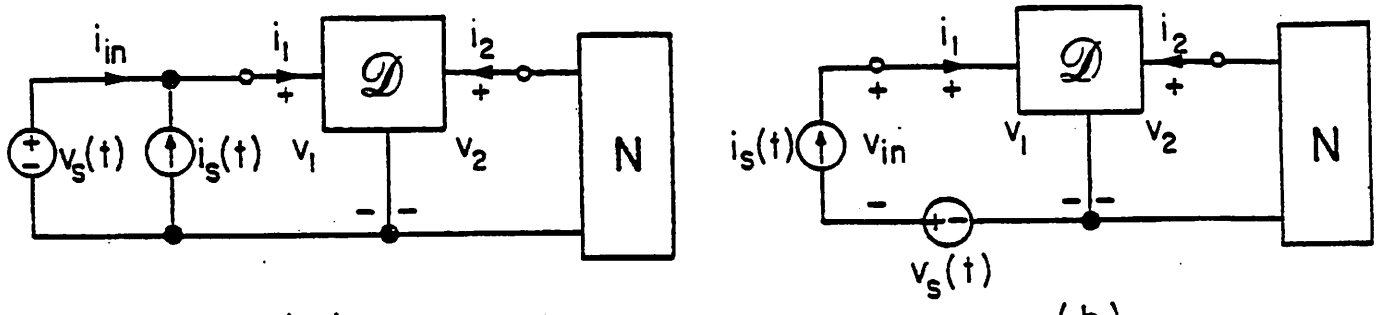
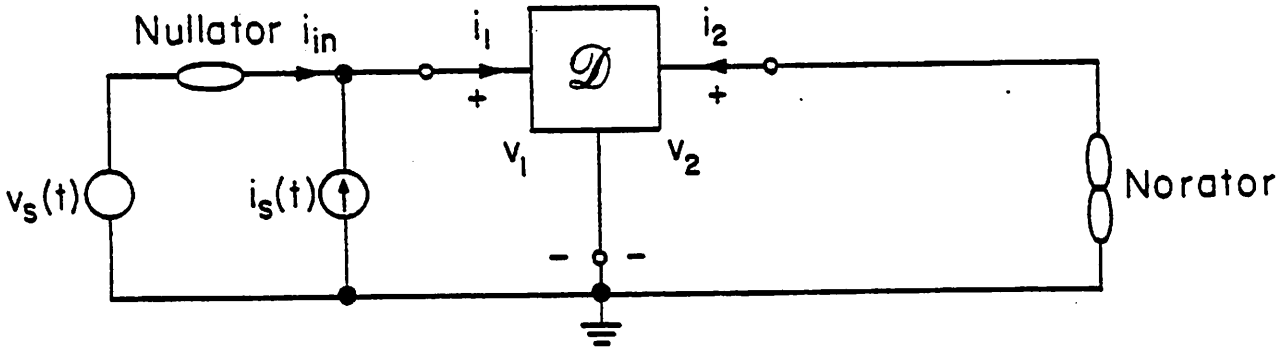


Fig. 25

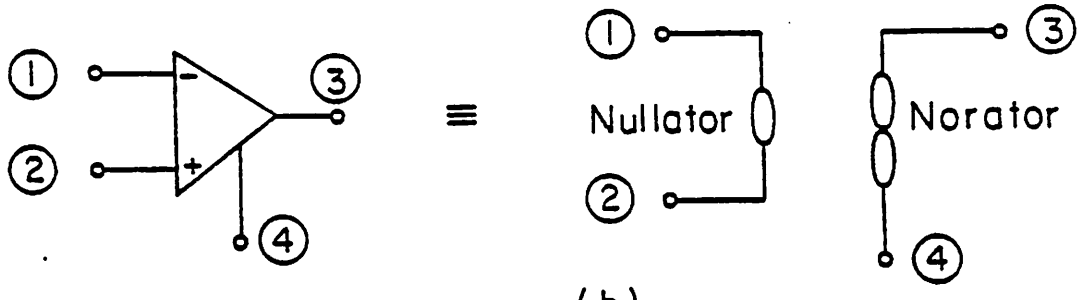


(a) (b)

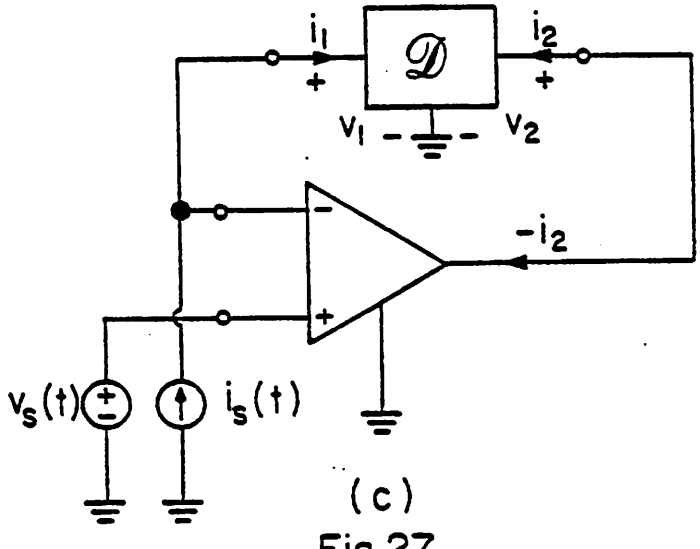
Fig.26



(a)



(b)



(c)

Fig.27