ON A CLASS OF SC RESISTORS AND ITS APPLICATION TO THE SYNTHESIS OF NONLINEAR DRIVING-POINT AND TRANSFER-CHARACTERISTIC PLOTS

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ABSTRACT The use of switched-capacitor components for designing nonlinear networks is discussed in this paper. We first introduce a new type of network component, the BESC-resistor, and consider its application to the design of nonlinear transfer characteristic and driving point plots. Systematic methods for designing piecewise-linear BESC-resistors using switched-capacitors are then given. Finally, experimental results showing the performance of the proposed circuits are included.

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1.INTRODUCTION

Since the mid seventies,linear switched capacitor (SC) networks have been receiving considerable attention because they offer an economical alternative in the design of precision filters and D/A and A/D converters [1,2].Extensive research has been done on the derivation of efficient design methods as well as specific simulation tools.One of the most striking features of SC networks is that they can be fully integrated in MOS technology [3]. This paves the way for implementing large scale integrated (LSI) analog circuits[4].

Interest in linear SC circuits has no counterpart in the nonlinear area.However,in many contexts where the need for a nonlinear transformation appears ,the question arises as to whether it is possible or not to design a complete analog sampled data system using SC circuits. For instance, some dynamic systems must be controlled in a nonlinear way and the use of SC methods is precluded because building blocks for a nonlinear transformation are not available.In fact,although a few recent papers have considered the synthesis of nonlinear functions for specific applications [5-8], nevertheless, it must be pointed out that a rational,general method for synthesizing nonlinear characteristics using SC networks has not yet been developed.

We have focused our attention during the last two years [14] on the realization of nonlinear building blocks which can allow the synthesis of any nonlinear transformation required for a given application.Our approach is also intended to develop a method of design which efficiently uses such building blocks.In this paper we will restrict ourselves to the consideration of piecewise-linear

characteristics.More general results will be reported elsewhere.

2. SOME PREVIOUS CONSIDERATIONS

For the sake of clarity in what follows we will only use a 2-phase nonoverlaping clock,even though it is not essential for the design method proposed here.We will designate the two clock phases as even and odd as is usual in the current literature [9].Switches in the networks can be even switches (S^e) when they are closed during the even clock phase. Alternatively, switches can be odd (S^o) when they are closed during the odd clock phase. In addition,switches can be controlled by the output of a comparator. This will be denoted by a subindex (S^i_j).Thus, a switch named S^e_j means that it may or may not be closed during the even phase,depending on the state of the j-th comparator used in the circuit.

Also, we will assume that the input voltage is sampled and held in synchronization with the internal clock.The sampling of the output variable takes place when hardly any current flows into the circuit and hence all voltages are practically constant.For convenience,we will call each electrical variable "even" if they occur at even instances;that is at n, n+1, n+2 ... and "odd" at instances n+1/2, n+3/2...As it was stated above for switches,we will use "e" and "o" as superscripts for specifying a variable defined in the even or in the odd phase,respectively.

3.ALGEBRAIC BESC-RESISTORS

The basis of the method in this paper is the extension of the equivalence between linear resistors and switched-capacitors,which has been proven to be useful for designing SC filters [2,9]. In

particular, we have paid attention to the analogy existing between a linear resistor and the SC circuit shown in Fig.1.This is only one of the many analogies we can define,but it has been popularized by SC filter designers [9].Strictly speaking,the network in Fig.1.b is a discretized capacitive model [13] of the linear resistor in Fig.1.a. Furthermore, it can be seen from the equations shown in Fig.1 that this discretized model has been derived by applying the Backward Euler numerical integration algorithm.This suggests a new concept,the BESC-resistor (BESC applies for Backward Euler Switched-Capacitor), which is defined as follows.

DEFINITION 1:BESC-resistor. The network element in Fig.2 is said to be a BESC-resistor if it can be characterized by the relation:

$$f(V^i , \hat{I}^i) = 0 \qquad (1)$$

where $f(\cdot,\cdot)$ is algebraic,V^i denotes the port voltage in phase "i",and $\hat{I}^i$ denotes the average of the current flowing through the network element during phase "i".

A BESC-resistor can be either "even"(i=e) or "odd"(i=o).In what follows we will only consider even BESC-resistors. We will say that such a BESC-resistors are voltage-controlled whenever $\hat{I}^e$ can be expressed as an explicit function of V^e,i.e.,

$$\hat{I}^e = g(V^e) \qquad (2)$$

Regarding voltage-controlled BESC-resistors, it will be interesting to consider the following definiton.

DEFINITION 2:Regional BESC-resistor. A voltage-controlled BESC-resistor is said to be regional inside an interval (a,b] if such

element can be described by,

$$\hat{I}^e = \begin{cases} g(V^e) & , \text{ for all } V^e \in (a,b] \\ 0 & , \text{ otherwise} \end{cases} \quad (3)$$

Current-controlled and regional current-controlled BESC-resistors can be defined in a similar way.

Using nonlinear BESC-resistors we can further extend the analogy shown in Fig.1 in order to synthesize nonlinear transfer characteristics.Let us consider the continuous network depicted in Fig.3.a,where all the 2-terminal resistors are explicitly shown.Let us assume that the remaining network N contains only interconnection paths. Assume further that the resistor connected across the k-th port is described by

$$i_k = f_k(v_k) \quad , \text{ for } k=1,2...p \quad (4)$$

and that the overall circuit realizes the following input-output transformation:

$$v_o = F(v_s) \quad (5)$$

If the BESC-resistor connected across the j-th port of the circuit in Fig.3.b is characterized by $\hat{I}_k^e = f_k(V_k^e)$, then, it should be clear that this circuit implements $V_o^e = F(V_s^e)$, where $F(\cdot)$ is the same functional dependence as in expression (5). Thus, the problem of synthesizing a nonlinear transfer characteristic using SC networks can be reduced to designing arbitrary BESC-resistors.

A word of caution must be said related to BESC-resistors (see [10] for the general case of SC-resistors). They are pseudo-resistive entities because they are capacitors whose memory is periodically

upset. Then, the $\hat{I}^e$ and V^e coordinates defining the DP plot associated with a BESC-resistor are not the instantaneous current and voltage measured at a physical port. Instead, they are average quantities that describe a symbolic port rather than a physical port. This may look surprising, but as it was clarified in [10], this kind of fictitious port allows the realization of TC plots with the same constraints that are typically used in linear SC filters. Namely:

1. Excitation signals are sampled and held until they change in synchronization with the clock waveform.
2. Electrical variables in the network are only of interest when no charge is flowing through any branch and all of the voltages are constant.

The problem of synthesizing continuous-time DP plots cannot be realized without resorting to mutators (see again [10] for technical details). Anyhow, the cornerstone is the finding of a systematic method for designing BESC-resistors. In that sense, we will devote the next Section to developing such a method for the realization of an interesting class of BESC-resistors.

4. SYNTHESIS OF MONOTONE PIECEWISE-LINEAR VOLTAGE-CONTROLLED BESC-RESISTORS

For our purposes, in what follows we will only treat voltage-controlled grounded BESC-resistors. Fig.4 shows a typical piecewise-linear(PL) monotone BESC-resistor characteristic. The segments have been labeled consecutively from "0" (leftmost segment) through "N" (righmost segment),and m denotes the slope of the j-th segment. Corresponding to the N+1 segments, the X-axis has been

partitioned into N+1 intervals defined by the knee voltages E_j. Then,for the j-th interval the element can be described by the following affine equation:

$$\hat{I}^e = m_j(V^e - E_j) + f(E_j) \quad , \quad E_j < V^e < E_{j+1} \qquad (6)$$

In the context of the synthesis it is interesting to consider two classes of PL monotone BESC-resistors.

DEFINITION 3:Extended concave BESC-resistors. A given PL monotone BESC-resistor is said to be an extended concave BESC-resistor if the following condition is fulfilled:

$$m_{j-1} < m_j < m_{j+1} \quad , \quad 1 \leq j \leq N-1 \qquad (7.a)$$

where

$$m_j > 0 \quad , \text{ for all } j \qquad (7.b)$$

DEFINITION 4:Extended convex BESC-resistors. A PL monotone BESC-resistor is said to be an extended convex BESC-resistor if

$$m_{j-1} > m_j > m_{j+1} \quad , \quad 1 \leq j \leq N-1 \qquad (8.a)$$

where

$$m_j > 0 \quad , \text{ for all } j \qquad (8.b)$$

REMARK 1. With the above definitions finite jump discontinuities are allowed for extended concave and extended convex BESC-resistors.

The synthesis of extended concave and extended convex BESC-resistors is what this paper is mainly concerned with.

4.1.SYNTHESIS OF EXTENDED CONCAVE BESC-RESISTORS

THEOREM 1. Each extended concave SC-resistor described by a PL function,$f(\cdot)$,can be synthesized by N+1 linear capacitors,2(N+1) analog switches,2N+1 voltage reference levels,N analog comparators and

N "AND" gates, interconnected as is shown in Fig.5 and where

$$C_j = m_j - m_{j-1} \quad , \quad \text{for} \quad j \neq 0 \tag{9}$$

$$C_o = m_o \tag{10}$$

$$E_j' = E_j - \frac{f(E_j^+) - f(E_j^-)}{C_j} \quad , \quad \text{for } j \neq 0 \tag{11}$$

$$E_o' = E_1 - \frac{f(E_1^-)}{C_o} \tag{12}$$

PROOF: Let us show the Theorem inductively.Clearly,it is fulfilled in the case of a BESC-resistor with only one interval.Then,let us assume that it is valid for a BESC-resistor with N intervals.Under this circumstances,C_N in Fig.5 will be eliminated and the last capacitor of the circuit will be C_{N-1}.

Now we need to prove that the circuit in Fig.5 is also valid when we introduce a new interval.Of course, this interval will be the rightmost one and be represented by a breakpoint at $V^e = E_N$ and a slope of value m_N for the charge-voltage characteristic when $V^e > E_N$.

The global characteristic for the BESC-resistor outside the new interval is the same as before

$$\hat{I}^e\Big|_{N+1} = \hat{I}^e\Big|_N \quad , \text{for} \quad V^e < E_N \tag{13.a}$$

and inside it

$$\hat{I}^e\Big|_{N+1} = \hat{I}^e\Big|_N + (m_N - m_{N-1})(V^e - E_N) + \Delta_N \quad , \quad \text{for } V^e > E_N \tag{13.b}$$

where $\hat{I}^e\Big|_N$ and $\hat{I}^e\Big|_{N+1}$ denote the port average currents for the BESC-resistors with N and N+1 intervals, respectively and where

$$\Delta_N = f(E_N^+) - f(E_N^-) \qquad (13.c)$$

denotes the measure of the jump at $V^e=E_N$ on $f(V^e)$.

On the other hand,the introduction of a new interval means adding one capacitor,one comparator,one "AND" gate and two switches.The charge flowing through the new capacitor will be denoted by $\hat{I}^e_{C_N}$ and fulfills the following conditions

$$\hat{I}^e\Big|_{N+1} = \hat{I}^e\Big|_N + H_N\hat{I}^e_{C_N} \qquad (14.a)$$

$$\hat{I}^e_{C_N} = C_N(V^e - E_N) \qquad (14.b)$$

where

$$H_N = \frac{1}{2}\{1 + \mathrm{sgn}(V^e-E_N)\} \qquad (15.a)$$

and

$$\mathrm{sgn}(x) = \begin{cases} 1 & , \quad x > 0 \\ -1 & , \quad \text{otherwise} \end{cases} \qquad (15.b)$$

After introducing (9) and (11) into (14.b) and then the resulting equation into (14.a),we obtain

$$\hat{I}^e\Big|_{N+1} = \hat{I}^e\Big|_N + H_N\{(m_N - m_{N-1})(V^e - E_N) + \Delta_N\} \qquad (16)$$

which corresponds to either (13.a) or (13.b) depending on he sign of $V^e - E_N$. This means that the addition of C_N and the associated circuitry allows the N+1 interval to be implemented. ▯

REMARK 2. An alternative implementation for extended concave BESC-resistors can be derived as shown in Fig.6. Theorem 1 is still valid for Fig.6.

4.2. SYNTHESIS OF EXTENDED CONVEX BESC-RESISTORS

THEOREM 2. Each extended convex BESC-resistor described by a piecewise-linear function $f(\cdot)$ with N+1 intervals can be synthesized by N+1 linear capacitors, 3N+2 analog switches, 2N+1 voltage reference levels, N analog comparators and N "NAND" gates interconnected as shown in Fig.7 and where

$$\frac{1}{C_j} = \frac{1}{m_j} - \frac{1}{m_{j-1}} \quad , \quad \text{for} \quad j \neq 0 \tag{17}$$

$$C_o = m_o \tag{18}$$

$$E_j' = -\frac{f(E_j^-)}{C_j} - \frac{\Delta_j}{m_j} \quad , \quad \text{for} \quad j \neq 0 \tag{19}$$

$$E_o' = E_o - \frac{f(E_1^-)}{m_o} \tag{20}$$

PROOF. Let us prove this Theorem by following the same steps as in Theorem 1. The only significant difference is that variables related to the added capacitor, C_N, now satisfy the following equations:

$$V^e\Big|_{N+1} = V^e\Big|_N + H_N V^e C_N \tag{21}$$

$$V^e_{C_N} = \frac{\hat{I}^e}{C_N} + E_N' \tag{22}$$

where $V^e_{C_N}$ is the voltage across the capacitor C_N.

Using expressions (17) and (19) we finally obtain the global representation for the voltage corresponding to the last interval. ▨

4.3. COMPLEMENTARY BESC-RESISTORS

Extended concave and convex BESC-resistors were treated separately in the previous sections as two unrelated classes of network elements. However, this two classes can be related by a simple geometrical transformation. Specifically, it is seen that when an extended convex (alternatively concave) characteristic is rotated 180° around the origin an extended concave (convex) characteristic is obtained. We can formalize this geometrical property by the following definition:

DEFINITION 5: Complementary BESC-resistors. Two BESC-resistors are said to be complementary if their respective characteristics can be reciprocally derived by making a rotation of 180° around the origin.

Clearly, given an extended concave (convex) BESC-resistor there always exists an extended convex (concave) one that is the complement of the other. We can put this fact to good use during the synthesis stage by applying the following Lemma:

LEMMA 1: Let us assume an extended concave (alternatively convex) BESC-resistor realized by the circuit in Fig.5 (Fig.7). Its complementary BESC-resistor can be implemented using the network in Fig.5(Fig.7) after making the following changes:

1) Interchanging input leads of each comparator.

2) Reversing the polarity of each reference voltage.

PROOF: Assume an arbitrary interval $H_j=(E_j, E_{j+1})$ lying between two adjacent breakpoints of the original characteristic. The corresponding interval of the complementary characteristic is $\overline{H}_j=(-E_{j+1}, -E_j)$.

Let us now consider the behaviour of the original network for an input $V^e|_{H_j}$ inside H_j. Since $V^e|_{H_j} > E_k$ $(k=1,2...j)$ and $V^e|_{H_j} < E_k$ $(k=j+1,...N)$, the outputs of the comparators ranging from k=1 to j are at the high state while the ones remaining are at the low state. Thus, the original network is modelled during the even phase of the clock (operating phase) by one of the equivalent networks in Fig.8. From these networks we obtain the following equation describing the interval H_j:

$$\hat{I}^e\Big|_{H_j} = m_j V^e\Big|_{H_j} + \sum_{k=1}^{j} a_k E_k' \qquad (23)$$

where m_j is given either by $m_j = \Sigma C_j$ (Fig.8.a) or by $m_j = \Sigma C_j^{-1}$ (fig.8.b) and the a_k's are real coefficients.

Consider next the behaviour of the complementary network for $V^e|_{\overline{H}_j} = -V^e|_{H_j} \in \overline{H}_j$. Taking into account point 1) of Lemma 1 and also that $-E_{j+1} < V^e|_{\overline{H}_j} < -E_j$, we conclude that the state of the comparators in the complementary network is the same as in the original one. Thus, the equivalent networks in Fig.8 can also be used for the complementary network provided that we change the sign of each reference voltage. With this change we obtain the following equation for the interval $\overline{H}_j$:

$$\hat{I}^e\Big|_{\overline{H}_j} = m\, V^e\Big|_{\overline{H}_j} + \sum_{k=1}^{j} a_k (-E_k') \qquad (24)$$

where m_j and a_k are the same as in equation (23) because the networks in Fig.8 are linear. Combining (23) and (24) we obtain

$$\begin{bmatrix} \hat{J}^e|_{H_j} \\ V^e|_{H_j} \end{bmatrix} = \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} \hat{J}^e|_{H_j} \\ V^e|_{H_j} \end{bmatrix} \qquad (25)$$

which corresponds to a rotation of 180°,as expected. ▨

It is interesting to note that from Theorems 1 and 2 and Lemma 1 it follows that any extended BESC-resistor (either concave or convex) can be realized by either a series capacitor configuration, or by a shunt capacitor configuration. For instance, the steps involved in designing an extended convex BESC-resistor using a parallel topology are as follows.First,we will obtain the complement of the given characteristic. Since this characteristic is concave,it can be realized by the circuit in Fig.5.Afterwards,the complementary network of the resulting circuit will be an implementation of the original convex characteristic.

4.4.SYNTHESIS OF REGIONAL SC-RESISTORS

As it was stated in equation (3), the behaviour of a regional BESC-resistor outside the interval in which it is regionalized [(a,b] in equation (3)] corresponds to an open circuit. Then, any extended concave (convex) BESC-resistor can be regionalised inside an arbitrary interval,$(E_h, E_k]$, by changing the logical control of switch S^e in Fig.5(Fig.7).We call the new switch S^e_{hk} and it must be controlled by making the "AND" operation between the clock phase and the output of two comparators,one which compares the input with E_h and the other which compares with E_k, as it is shown in Fig.9.

4.5. SYNTHESIS OF GENERAL PL MONOTONE BESC-RESISTORS

Let us assume a PL monotone BESC-resistor characterized by

$$\hat{I}^e = f(V^e) \qquad (26)$$

where $f(\cdot)$ contains N+1 segments with breakpoints at $E_1, E_2, \ldots E_N$ and assuming that finite jump discontinuities are allowed. From the above paragraphs we can propose a method for synthesizing such an BESC-resistor, although it is neither concave nor convex.

LEMMA 2: Each PL monotone BESC-resistor can be synthesized by shunting regional concave and regional convex BESC-resistors.

PROOF: A constructive procedure may be used to prove the Lemma. Starting from the left, let us divide the characteristic $f(\cdot)$ into the smallest number of regions possible, all of them being either extended concave or extended convex. For each one of these regions let us synthesize a regional BESC-resistor whose characteristic corresponds exactly to $f(\cdot)$ inside that region. Then, shunt all of these regional BESC-resistors. It is clear that the global characteristic of the resulting network is equivalent to $f(\cdot)$. ▨

It is important to mention that since each interval shares a breakpoint with its neighbors, the total number of comparators required to synthesize a monotone BESC-resistor is equal to the number of breakpoints.

5. APPLICATION TO NONMONOTONE BESC-RESISTORS

It is well-known from the Theory of Nonlinear Networks [11] that any nonmonotone "continuous-time" PL resistor can be realized by the appropriate interconnection of a monotone PL resistor and a negative

one.It has been shown in [10] that the same technique can be used with BESC-resistors. In this paper we will only consider this classical approach. Thus, it will be enough for us to describe a procedure for designing negative-slope BESC-resistors.

Fig.10 shows the basic circuit for implementing a negative slope BESC-resistor.During the even phase the charge conservation equations are

$$V_1^e = 2V^e \tag{27.a}$$

$$\hat{I}^e = C(V^e - V_1^e) \tag{27.b}$$

Substituting (27.a) into (27.b), we obtain

$$\hat{I}^e = -CV^e \tag{28}$$

Since C is an arbitrary positive number and the circuit is voltage-controlled, we can synthesize an arbitrary nonmonotone PL BESC-resistor by shunting a suitable negative BESC-resistor to a monotone PL BESC-resistor.Guidelines for selecting both elements for a given nonmonotone characteristic are similar to the ones reported for "continuous-time" resistors [11] .

6.SYNTHESIS OF TRANSFER CHARACTERISTICS USING BESC-RESISTORS

As it was previously stated in Section 3,BESC-resistors can be efficiently used to synthesize a transfer characteristic.As an example, consider Fig.11 where the following outputs can be obtained:

$$V_1^e(n) = V^e(n) + \frac{f\{V^e(n)\}}{C} \tag{29.a}$$

$$V_1^o(n+1/2) = \frac{f\{V^e(n)\}}{C} \qquad (29.b)$$

Thus, two nonlinear transfer characteristics are obtained,whose functional dependences upon V^e are directly related to the one describing the nonlinear BESC-resistor.

Observe that in Fig.11 the BESC-resistor is driven by a voltage source via the virtual ground of the operational amplifier A1. More general driving schemes must be considered carefully due to instability troubles provoked by the comparator delay. For instance, the simple SC nonlinear voltage divider shown in Fig.12 can perform in an erroneous way due to the influence of those delays [10].Fortunately,such troubles can be avoided by adding a memory device to each comparator output in Figs.5,6.,7 and 9.Fig.13 depicts a practical way to do that.The block labelled "D" in this figure is a type D flip-flop which is trigered by the falling edge of the clock ϕ^e.

7.EXPERIMENTAL RESULTS.

The efficiency of the procedure developed in this papers has been checked by synthesizing different examples. Theorems 1 and 2 in conjunction with expression (29.b) were applied for implementing the TC plot characteristics shown in Fig.14.a and 15.a, respectively.The corresponding experimental results are shown in Fig.14.b and 15.b. On the other hand,Lemma 2 was applied in conjunction with equation (29.a) to synthesize the transfer characteristic shown in Fig.16.a. The experimental result is shown in Fig.16.b. In this figure, two residual traces due to the transient response of the comparators in

each operating cycle can be observed.

The characteristic in Fig.17 is used to illustrate the use of complementary components.To this end, it is decomposed as shown in Fig.18. Fig.18.a shows a regional convex characteristic and is realized by the network in Fig.19. On the other hand, the characteristic in Fig.18.b is the complement of the one in Fig.18.a. Thus, it can be realized by Lemma 1 using the complementary network of the one in Fig.19.The complete realization is obtained by shunting these two networks.Fig.20 shows the measured experimental characteristic.

Finally, Fig.21 depicts an experimental absolute value characteristic. It was realized by shunting one positive and a one negative BESC-resistor and illustrates the design of nonmonotone elements. In all the experiments, discrete capacitors with a 10% tolerance and values ranging from 1nF to 5nF were used. For the comparators we have utilized μA709 operational amplifiers. The remaining components were μA741 operational amplifiers, MC14066 analog switches and MC14011 NAND gates.

8.DISCUSSION OF RESULTS

We have introduced the concept of "BESC-resistor" as a basic building block for synthesizing SC nonlinear networks. Emphasis has been placed on the physical realization of transfer functions, the reason being twofold.First, this emphasis is in line with the general practice in SC filters, where only transfer characteristics are obtained. Secondly, as it was discussed in Section 3, the synthesis of driving-point characteristics using BESC-resistor is straigthforward requiring the use of mutators as it has been

extensively shown in [10] .

The main result here is that we can implement any monotone TC plot by using monotone extended concave and extended convex BESC-resistors. Also, with the addition of the negative BESC-resistor the method is useful for synthesizing any nonmonotone TC.Moreover,since the absolute value function can be easily implemented (see Fig.19), extension of the procedure to multidimensional TC characteristics is straightforward in view of the technique given in [12] .

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CAPTIONS TO FIGURES

Figure 1:Switched-capacitor simulated resistor.

Figure 2:Circuit symbol for a BESC-resistor.

Figure 3:(a)Continuous-time nonlinear network to be simulated

(b)Simulation network using BESC-resistors.

Figure 4:Typical PL monotone characteristic.

Figure 5:Network realization for an extended concave BESC-resistor.

Figure 6:Alternative realization for an extended concave BESC-resistor.

Figure 7:Network realization for an extended convex BESC-resistor.

Figure 8:Equivalent networks during the even phase for:

(a)Extended concave BESC-resistors.

(b)Extended convex BESC-resistors.

Figure 9:Circuit used for regionalising a BESC-resistor.

Figure 10:Network realization for a negative slope BESC-resistor.

Figure 11:Transfer function realization using a grounded voltage-controlled BESC-resistor.

Figure 12:Nonlinear SC voltage divider.

Figure 13:Example of a comparator with memory.

Figure 14:(a)Theoretical extended concave BESC-resistor characteristic.

(b)Experimental result.

vertical signal:V_2^o ,scale 1v/div (C =1nF)

horizontal signal:V^e ,scale 0.5v/div

Figure 15:(a)Theoretical extended convex BESC-resistor characteristic.

(b)Experimental result.

vertical signal:V_2^o ,scale 0.5v/div (C =1nF)

horizontal signal:V^e ,scale 0.5v/div

Figure 16:(a)Theoretical PL monotone TC characteristic.

(b)Experimental result.

vertical signal:V_1^e ,scale 1v/div

horizontal signal:V^e ,scale 0.5v/div

Figure 17:Theoretical PL characteristic used for illustrating the utilization of complementary elements.

Figure 18:Component curves for the characteristic in Fig.17.

Figure 19:Network realization for the characteristic in Fig.18.a.

Figure 20:Experimental result for the characteristic in Fig.17.

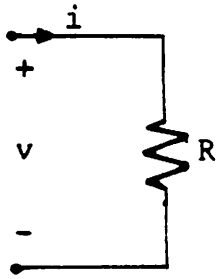
vertical signal:V_2^o ,scale 1v/div (C =lnF)

horizontal signal:V^e ,scale 1v/div

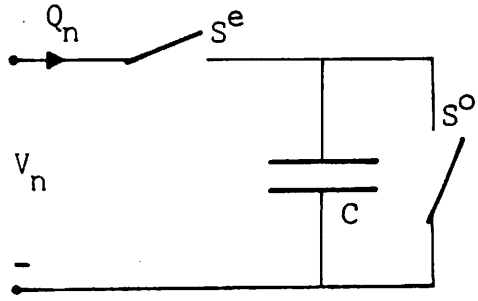
Figure 21:Experimental absolute value characteristic.

vertical signal:V_2^o ,scale 1v/div

horizontal signal:V^e ,scale 2v/div



$dq = \frac{v}{R}\, dt$



$Q_n - Q_{n-1} = \Delta Q_n = CV_n$

Fig.1

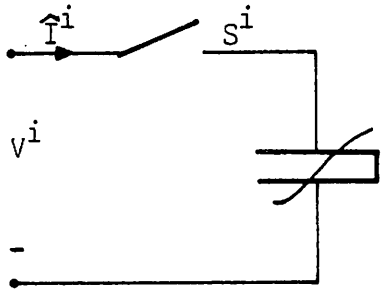
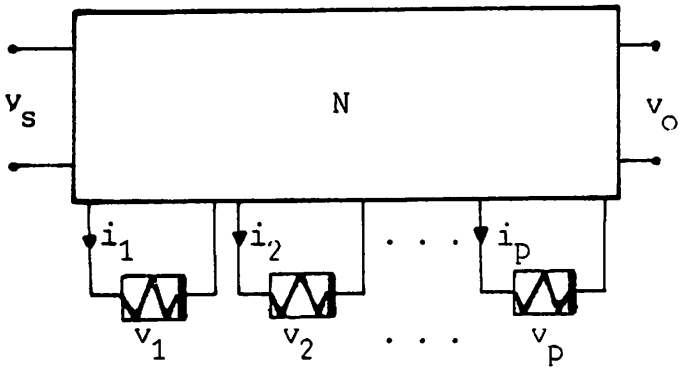
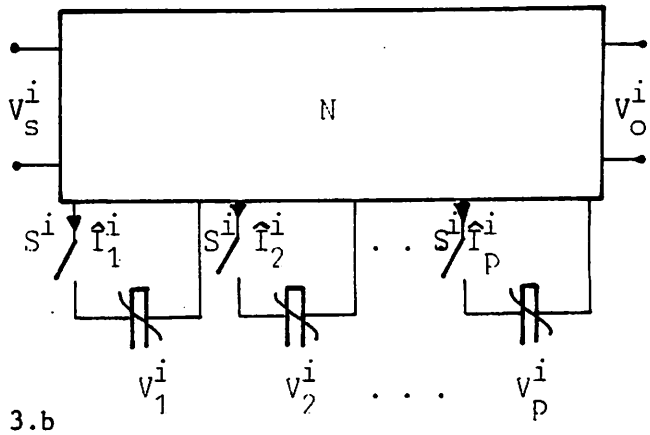


Fig.2



3.a



3.b

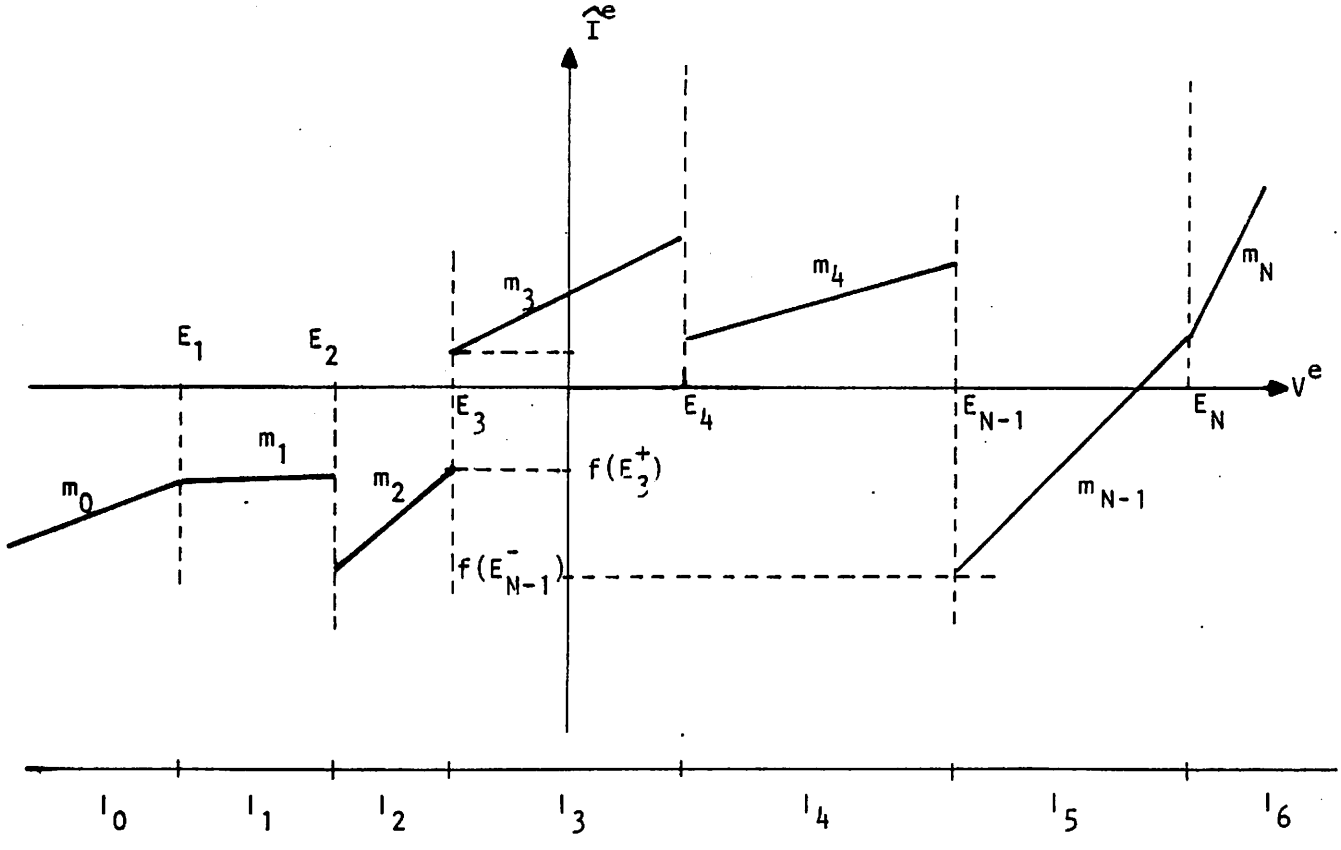

$\tilde{I}^e$
V^e
E_1
E_2
E_3
E_4
E_{N-1}
E_N
m_0
m_1
m_2
m_3
m_4
m_{N-1}
m_N
$f(E_3^+)$
$f(E_{N-1}^-)$
I_0
I_1
I_2
I_3
I_4
I_5
I_6

Fig.4

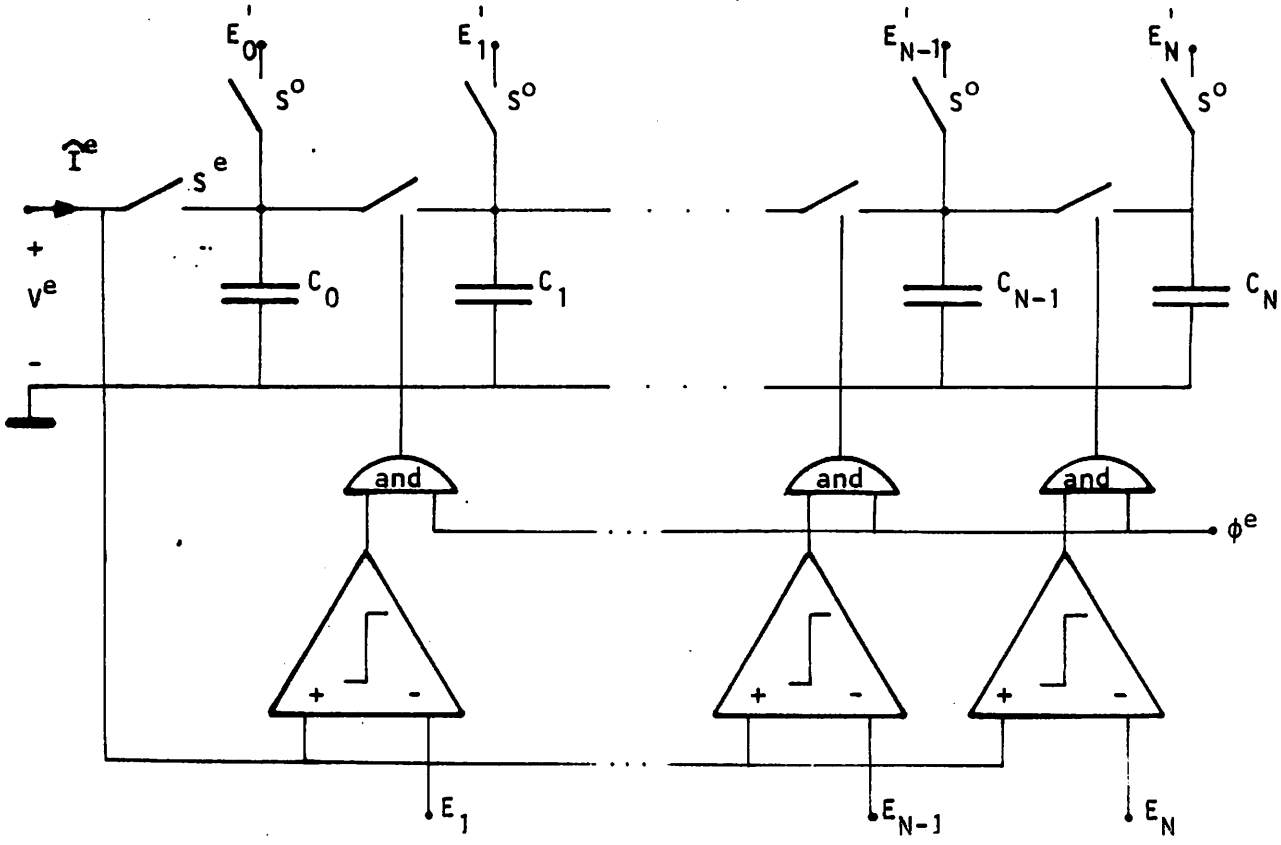


Fig.5

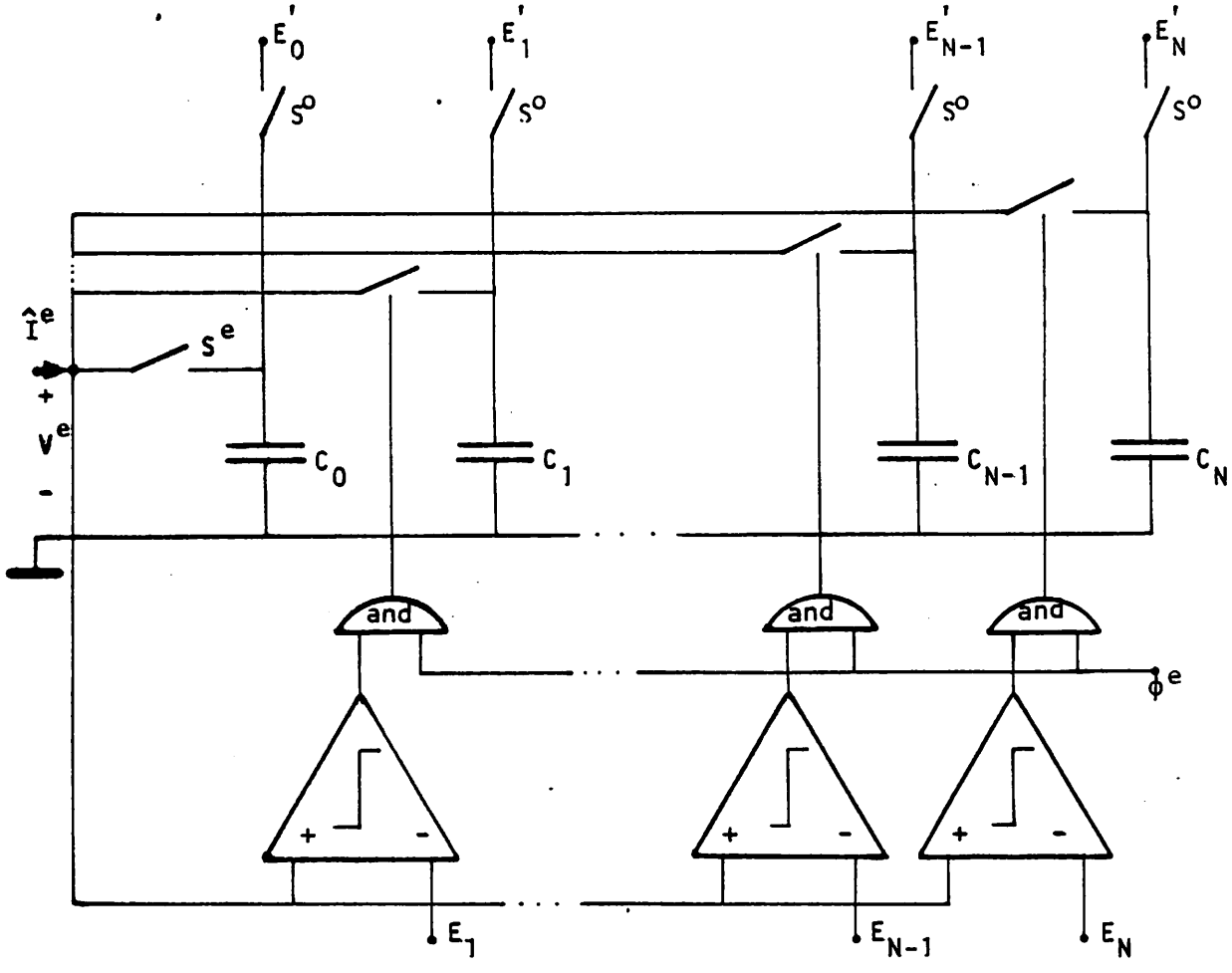


Fig.6

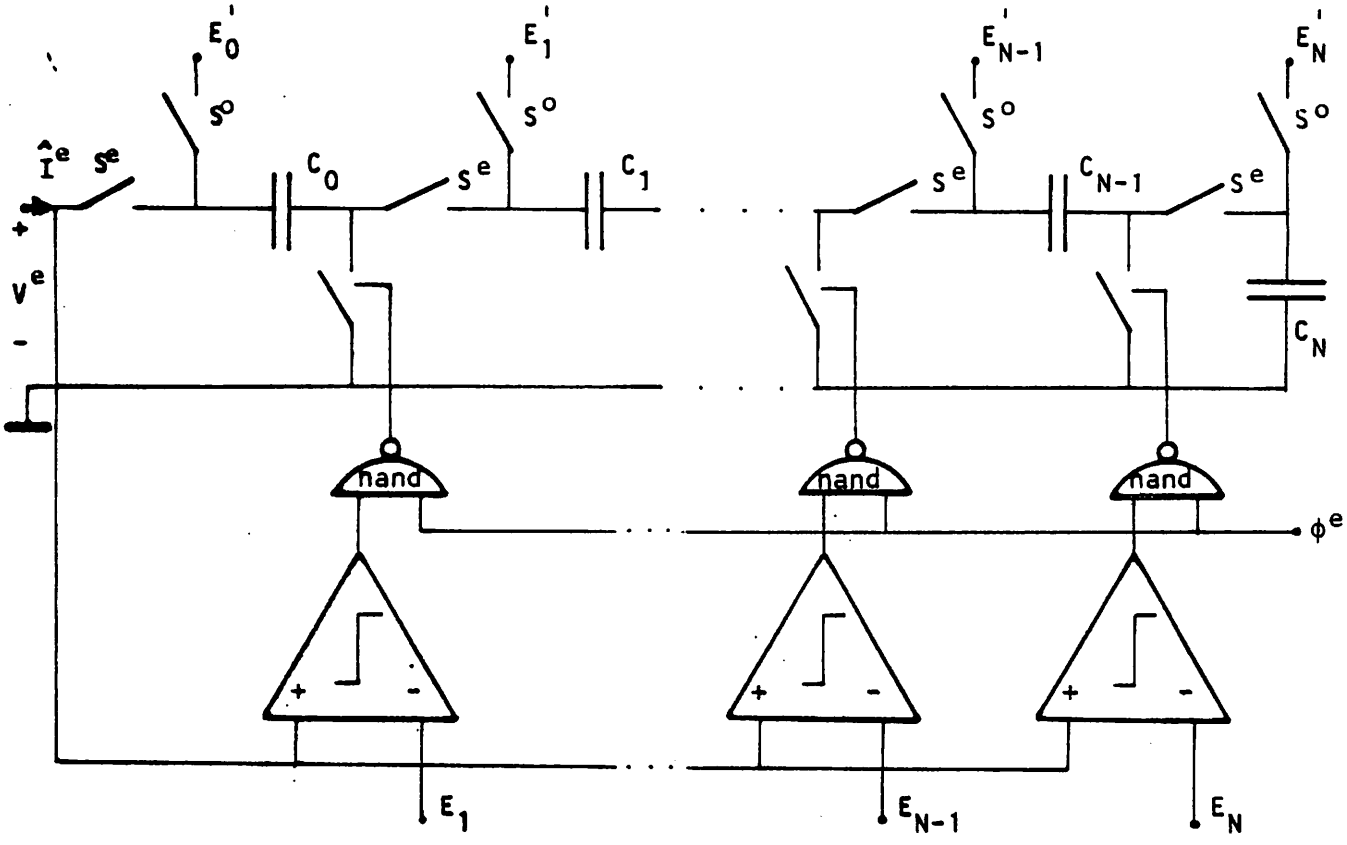
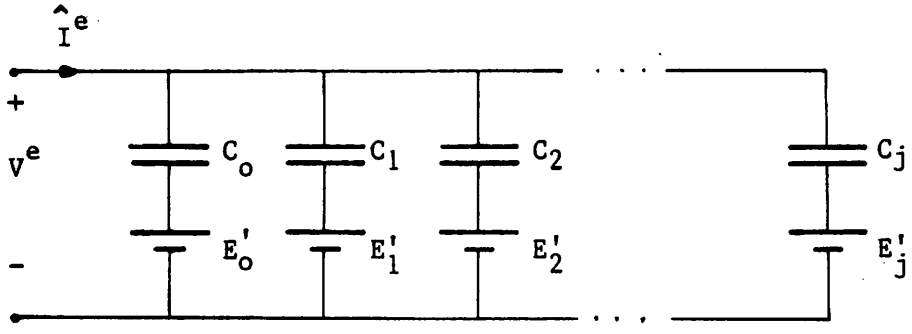
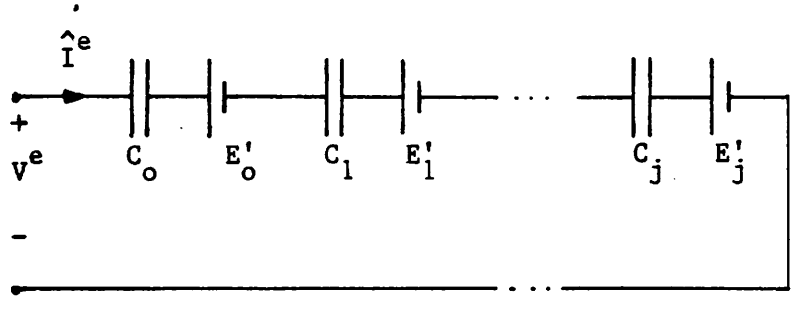


Fig.7



8.a



8.b

Fig.8

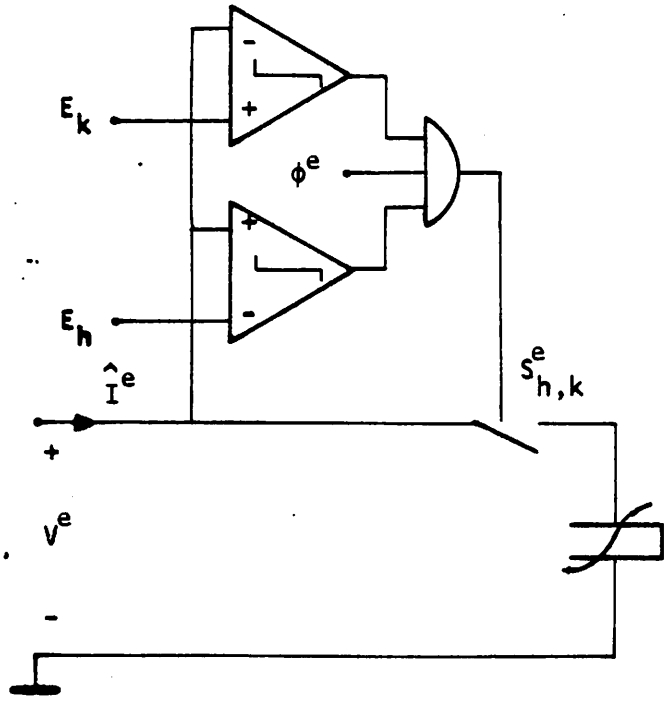


Fig.9

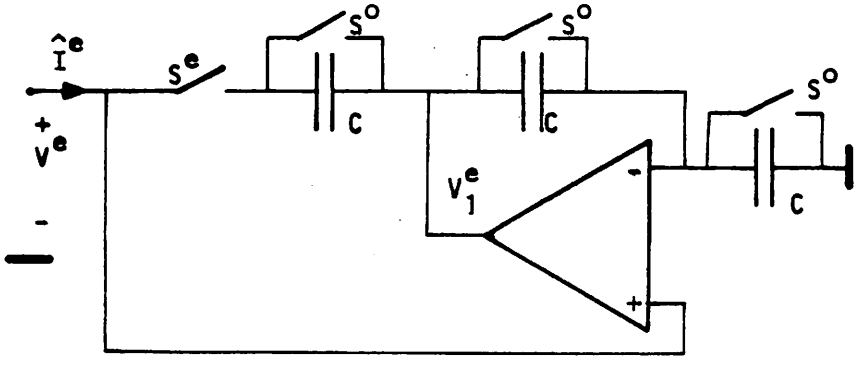


Fig.10

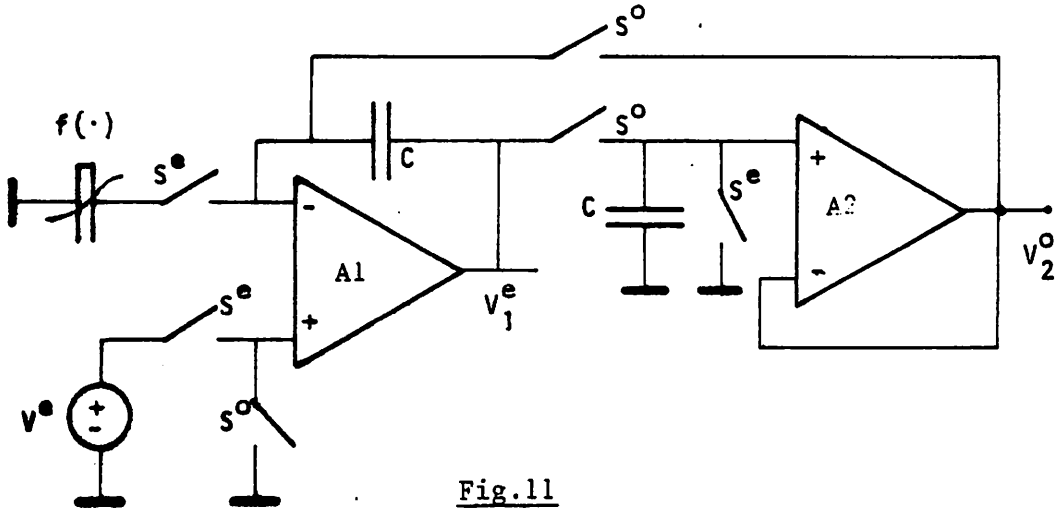


Fig.11

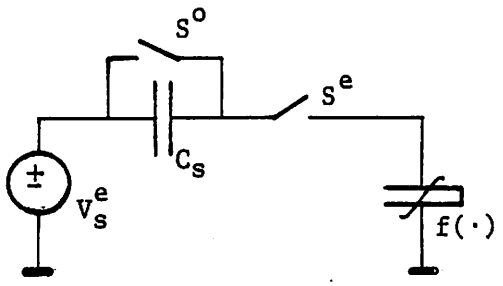


Fig.12

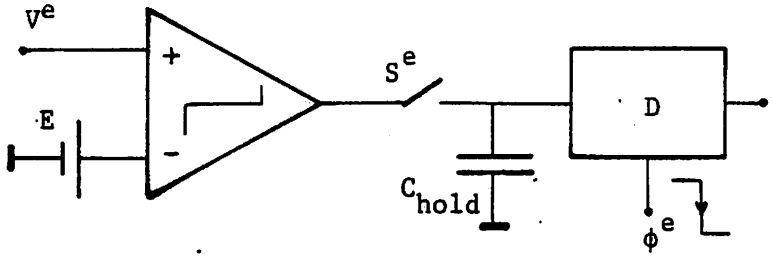
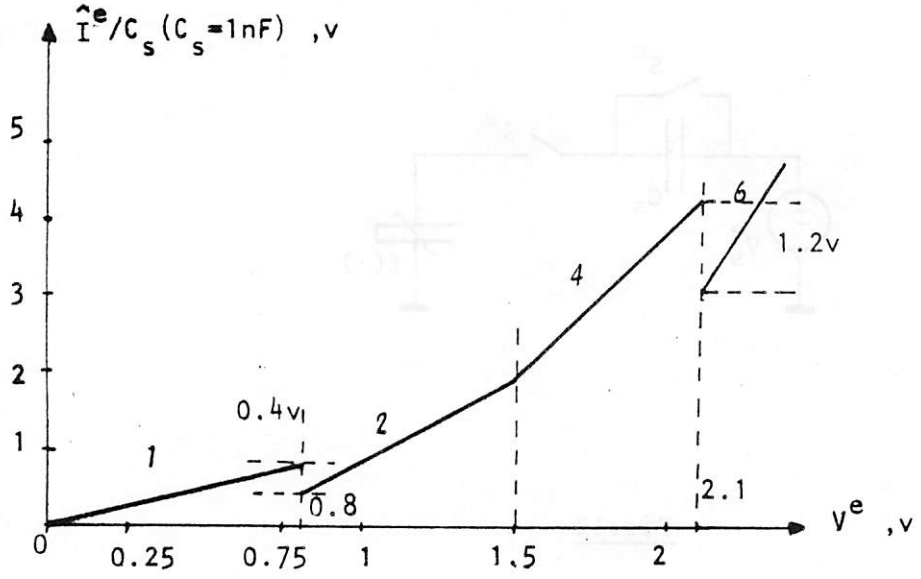
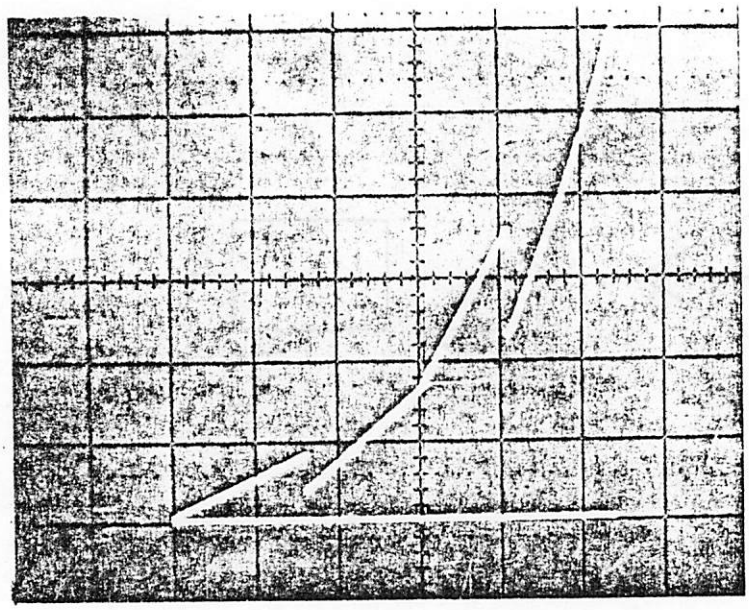


Fig.13

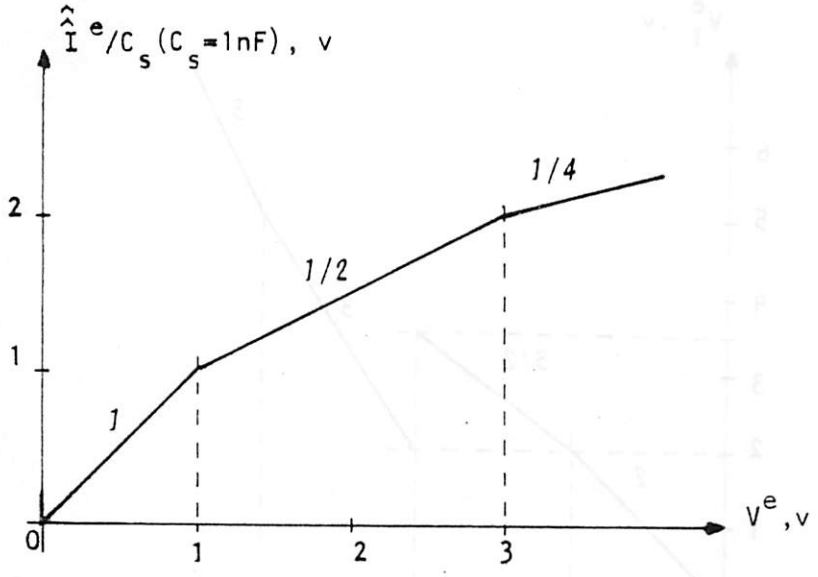


14.a



14.b

Fig. 14



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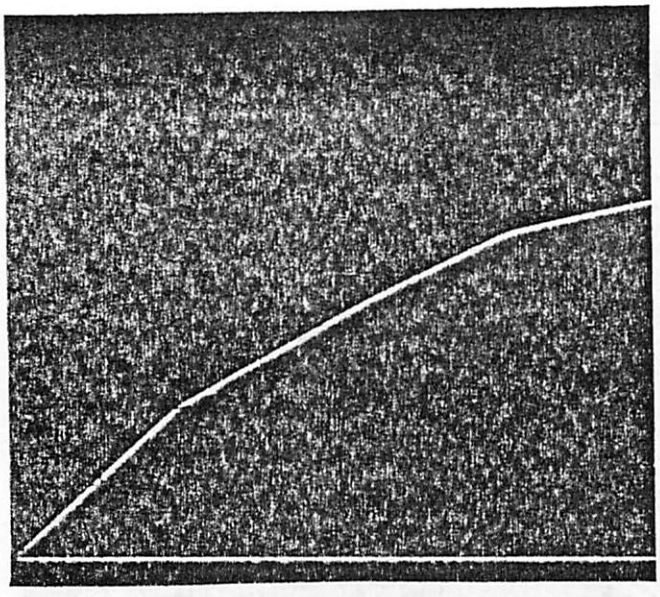
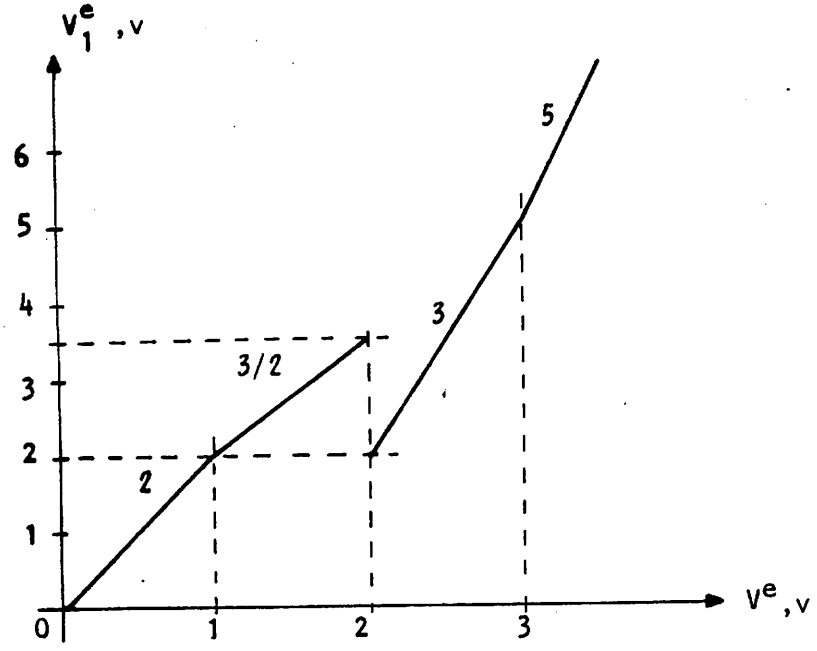
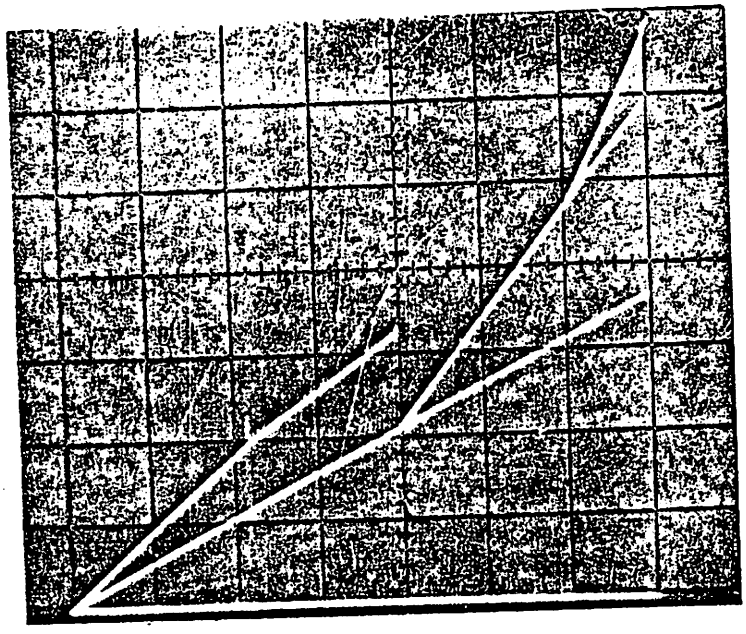


15.b

Fig.15

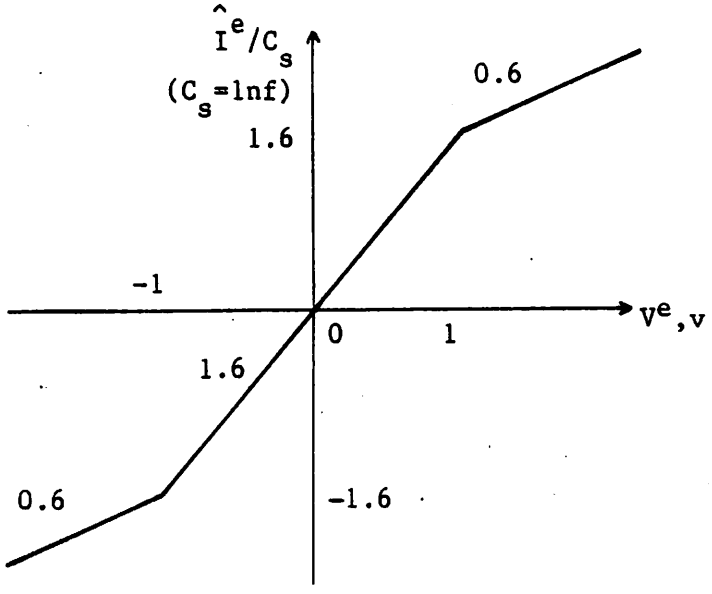


16.b



16.a

Fig.16


$\hat{I}^e/C_s$
$(C_s=1nf)$
1.6
0.6
-1
0
1
V^e,v
1.6
0.6
-1.6

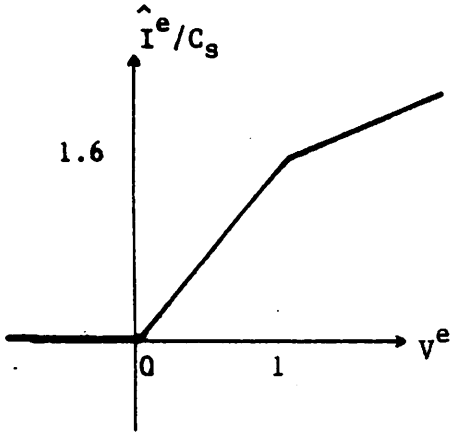

$\hat{I}^e/C_s$
1.6
0
1
V^e

Fig.17

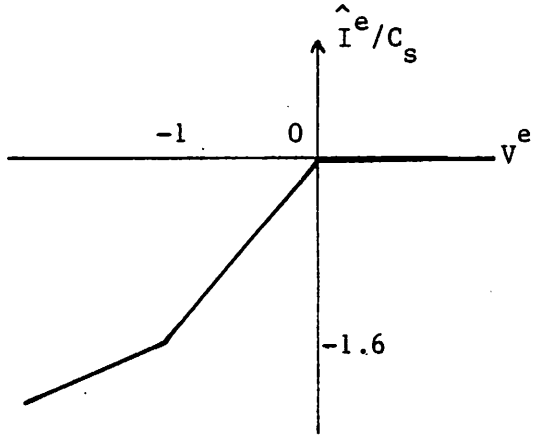
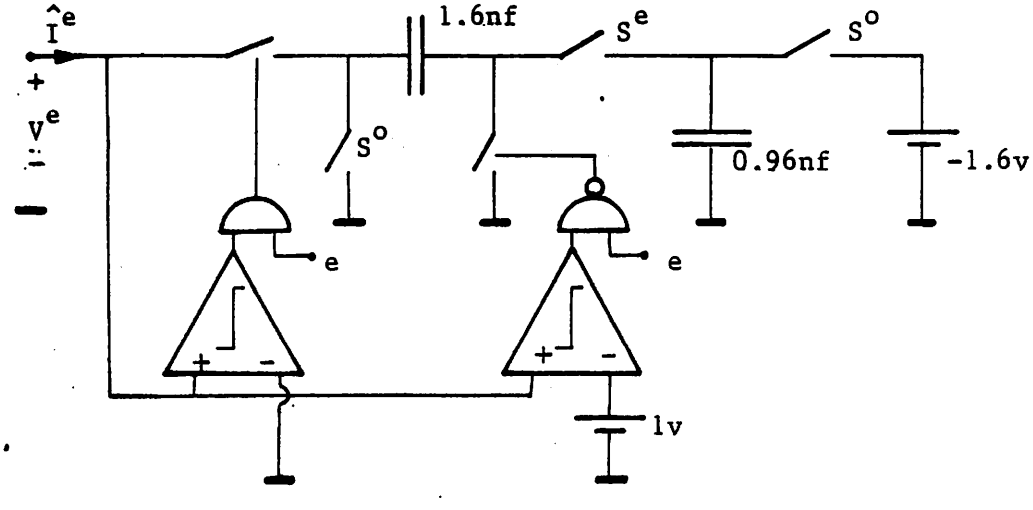

$\hat{I}^e/C_s$
-1
0
V^e
-1.6

Fig.18


$\hat{I}^e$
+
V^e
-
1.6nf
S^e
S^o
S^o
0.96nf
-1.6v
e
e
1v

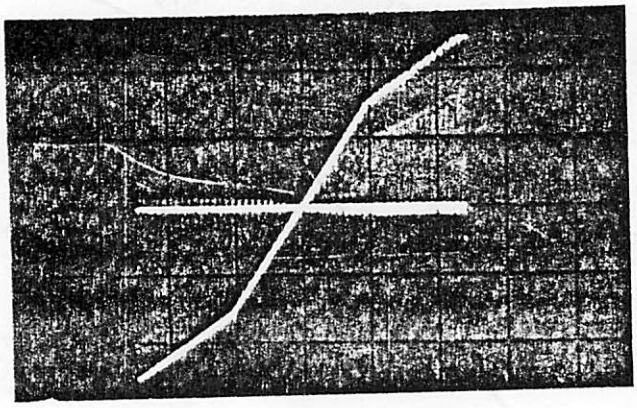


Fig.20

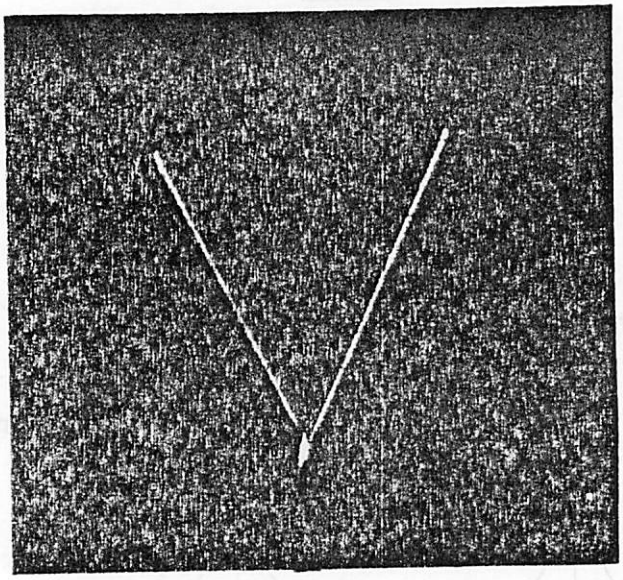


Fig.21