HIGH-FREQUENCY CMOS CONTINOUS TIME FILTERS

by

H. Khorramabadi

Memorandum No. UCB/ERL M85/19

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High-Frequency CMOS Continuous Time Filters

By

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DISSERTATION

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Chairman Date
Robert W. Brodersen 2/20/85
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High-Frequency CMOS Continuous Time Filters

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ABSTRACT

The extension of fully-integrated continuous time filtering technique to high frequencies would allow a higher level of integration in systems such as communication receivers. In the past, the practical implementation of high-frequency continuous time filters have been hindered by problems such as the sensitivity of high frequency filters to the integrator nonidealities and center frequency control. In this dissertation these problems are investigated.

A simple fully-differential integrator, optimized for phase-error cancellation, forms the basic element; a complete filter consists of intercoupled integrators. The center frequency of the filter is locked to an external reference frequency by a modified phase-locked loop. Instead of the voltage controlled oscillator of the conventional phase-locked loop, an exact replica of the second order section of the main filter is used.

To prove the viability of this technique, a fully-integrated sixth-order bandpass filter was designed and fabricated. The prototype dissipates 55 mW and occupies 4 mm^2 in a 6 μm CMOS technology.

ACKNOWLEDGEMENTS

I wish to express my deepest appreciation to my research advisor Professor Paul Gray for his guidance, patience and continuous support throughout the course of my graduate studies. I feel privileged for the opportunity to work with him.

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CHAPTER 1

INTRODUCTION

High-precision, high-order monolithic filters in the frequency range of 100KHz to 10MHz have many applications in communication receivers such as AM & FM IF filtering and video processing in T.V. circuits. Additional applications include data communications and local area networks.

Monolithic filters have been previously successfully applied to voice band applications both by utilizing the switched-capacitor technique and the continuous-time filtering method [1] [2]. However, the extension of both techniques to higher frequencies has been delayed due to many problems.

One promising approach for the implementation of high-frequency filters is the switched-capacitor technique. Recently a switched-capacitor bandpass filter at the center frequency of $260KHz$ has been designed which has shown excellent performance [3] . Another switched-capacitor filter with low-pass characteristics was reported at a roll-off frequency of $2.8MHz$ [4] . One major drawback to this approach is the requirement of continuous-time prefilters to band limit the input spectrum to reduce the aliasing effects. Another problem peculiar to the implementation of high-frequency switched capacitor filters is that due to settling time limitations in state of the art operational amplifiers, the extension of this technique to higher frequencies requires the lowering of the ratio of clock rate to center frequency of the filter which brings about the necessity of higher selectivity for the anti-aliasing prefilters.

Another alternative is to use continuous-time filtering techniques, which do not have the aliasing problem of sampled-data systems. However, due to the dependence of the center frequency of the filter on the absolute values of monolithic components such

as capacitors and transistor transconductances, which are both process and temperature dependent, some extra circuitry is required to control the center frequency of this type of filters.

This dissertation describes a high-frequency CMOS continuous-time bandpass filtering technique which utilizes a modified version of the phase-locked loop scheme introduced by Tan [1], to precisely control the center frequency of the filter [5].

In Chapter 2, Tan's approach is reviewed and the problems involved in the direct extension of this technique to higher frequencies are discussed.

Solutions to the problems hindering the filter design are proposed in Chapter 3, where a very simple fully differential integrator is described and a sixth-order bandpass filter is implemented.

In Chapter 4, the limitations of the designed filter are discussed. This includes finding an upper bound for the filter quality factor as a function of frequency. Noise and dynamic range considerations are presented in detail followed by a study of the effect of transistor mismatches on the filter behavior. In the final section, the results obtained in the previous sections are used to design a 500 *KHz* filter.

In Chapter 5, the center frequency control circuit is studied and and the design of the required building blocks is described.

In Chapter 6, experimental results obtained from a monolithic CMOS prototype is presented. The prototype includes a sixth order bandpass filter with an on-chip phase-locked loop.

A summary of this research project is presented in Chapter 7.

In Appendix A, the high-frequency characteristics of MOS transistors which are required for the design of the integrator are studied.

In Appendix B. the total output noise power of an active ladder type bandpass filter is derived.

CHAPTER 2

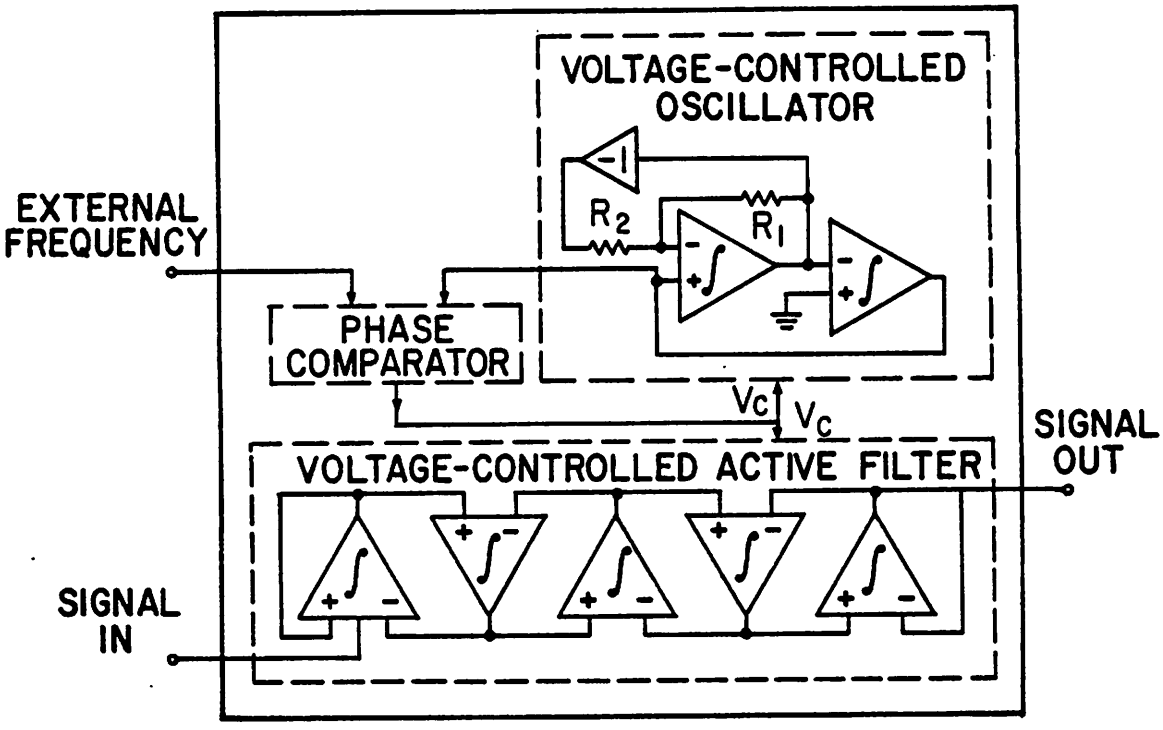
EXTENSION OF LOW-FREQUENCY FREQUENCY-LOCKED FILTERING TECHNIQUES TO HIGHER FREQUENCIES

The frequency-locked continuous-time filtering technique was first introduced in 1977 [1]. A low-pass voice-band filter was designed by using an integrator as the principle building block. The roll-off frequency of the filter is determined by the time constant of the integrators. This in turn is a function of the absolute values of monolithic components, in this case capacitors and transistor transconductances, which are both process and temperature dependent. To achieve an accurate filter roll-off frequency, a phase-locked loop scheme was utilized to lock the roll-off frequency to an external reference frequency. Because the frequency characteristics of the filter depend only on the matching accuracy of monolithic components, using this technique eliminates the requirement of any external trimming.

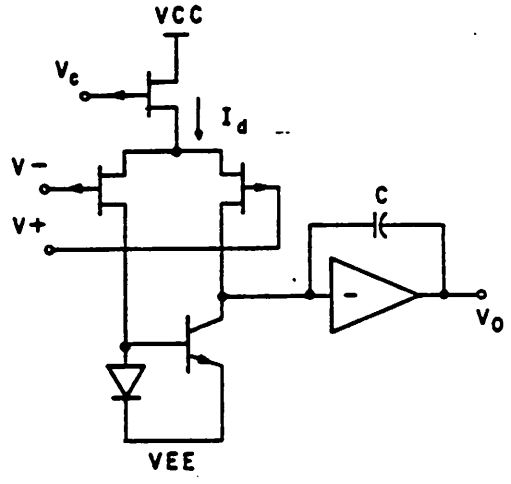
Fig. 2.1(a) shows the block diagram of the system. The integrator consists of a JFET transconductance stage followed by a multi-stage bipolar operational amplifier and a feedback integrating capacitor, as shown in Fig. 2.1(b). The time constant of the integrators are controlled through the control voltage, V_c. A voltage-controlled oscillator, VCO, in conjunction with a phase-comparator functions as a phase-locked loop. By choosing the same type of integrator for both the filter and the VCO, the bandwidth of the filter tracks the frequency of the oscillator.

The extension of this approach to higher frequencies involves several problems:

1) The main problem is that the behavior of high-frequency filters is highly sensitive to analog integrator non-idealities, particularly the phase shift at the unity-gain



(a)



(b)

Figure 2.1

(a)- Block diagram of Tan's approach to the design of a low-frequency low-pass continuous-time filter. (b)- Monolithic JFET input integrator.

frequency.

2) The second problem is the realization of a CMOS VCO with stable and repeatable center frequency in the *MHz* range.

3) Because the desired filters are often highly selective (high Q), the power supply rejection (PSRR) is a critical problem.

4) Finally the feed-through of the reference signal to the output of the filter can result in the degradation of the dynamic range.

The solution to the first problem will be discussed in detail in Chapter 3. To overcome the second problem, an alternative scheme is presented in Chapter 5 which utilizes a voltage-controlled filter VCF instead of the conventional VCO. The last two problems are minimized by using fully differential architecture for the circuit design.

CHAPTER 3

PRACTICAL IMPLEMENTATION OF CONTINUOUS-TIME HIGH-FREQUENCY FILTERS

In the monolithic implementation of continuous-time high-frequency filters, the most important consideration is the effect of the finite integrator quality factor on the filter performance. This chapter begins with a study of the effect of the integrator non-idealities on filter behavior. The results of this study are used to design a simple source-coupled pair integrator. In the final sections, the considerations for the design of a resonator and the implementation of a sixth-order bandpass filter are discussed.

3.1. Effect of Integrator Non-Idealities on Filter Behavior

As mentioned earlier, the main building block for ladder type active filters is an integrator. In this section, the quality factor of the integrator is defined in terms of integrator non-idealities. The effect of the finite integrator quality factor on the filter behavior is demonstrated through an example.

3.1.1. The Ideal Integrator

The transfer function of the ideal integrator is given by

$$H(s) = \frac{\omega_0}{s} \tag{3.1}$$

It has a pole at the origin and exactly 90 degree phase shift at the unity-gain frequency. In Fig. 3.1 the amplitude and phase response of an ideal integrator is illustrated.

For the purpose of the design of active filters, one useful measure of the integrator behavior is its quality factor, Q_{intg}.

Ideal Integrator

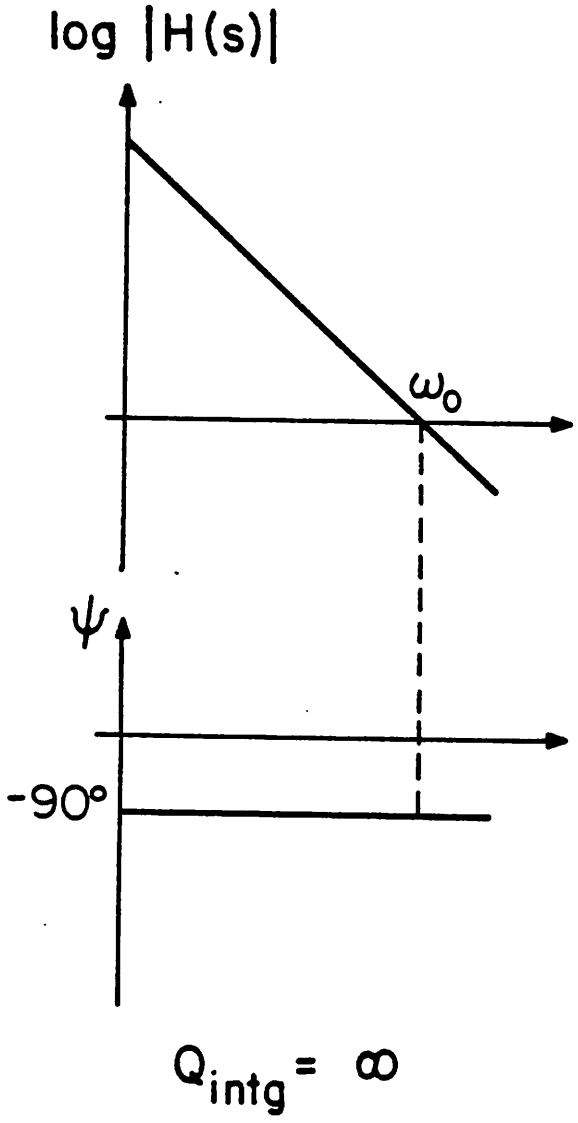


Figure 3.1

Amplitude and phase response of an ideal integrator.

For any component with a transfer function of

$$H(j\omega) = \frac{1}{R(\omega)+jX(\omega)} \tag{3.2}$$

the quality factor is defined as [6]

$$Q = \frac{X(\omega)}{R(\omega)} \tag{3.3}$$

Using the above concept and equation (3.2) , the Q of the ideal integrator is found to be

$$Q_{intg}^{ideal} = \infty \tag{3.4}$$

3.1.2. The Real Integrator

For a real integrator, with a finite DC gain of a , the dominant pole is pushed from the origin to a frequency equal to $p_1 = \frac{\omega_0}{a}$, where ω_0 is the unity-gain frequency of the integrator. Also, it may have one or more high-frequency non-dominant poles, p_2, p_3, . . ., as illustrated in Fig. 3.2. The finite DC gain causes phase lead at the unity-gain frequency and the non-dominant poles result in excess phase shift.

The transfer function of the real integrator is given by

$$H(s) = \frac{a}{\left|1 + s\frac{a}{\omega_0}\right| \left|1 + \frac{s}{p_2}\right| \left|1 + \frac{s}{p_3}\right| \ldots\ldots} \tag{3.5}$$

To find the quality factor of the real integrator Q_{intg} , the transfer function should be transformed to the form of the equation (3.2) . The denominator is multiplied and $j\omega$ is substituted for s

$$H(j\omega) = \tag{3.6}$$

$$\frac{a}{1+j\omega\left|\frac{a}{\omega_0}+\sum_{i=2}^{i=\infty}\frac{1}{p_i}\right|-\omega^2\left|\frac{a}{\omega_0}\sum_{j=2}^{j=\infty}\frac{1}{p_j}+\frac{1}{p_2}\sum_{k=3}^{k=\infty}\frac{1}{p_k}+\ldots\right|+j\omega^3\left|\frac{a}{\omega_0}\frac{1}{p_2p_3}+\ldots\right|+\ldots}$$

Real Integrator

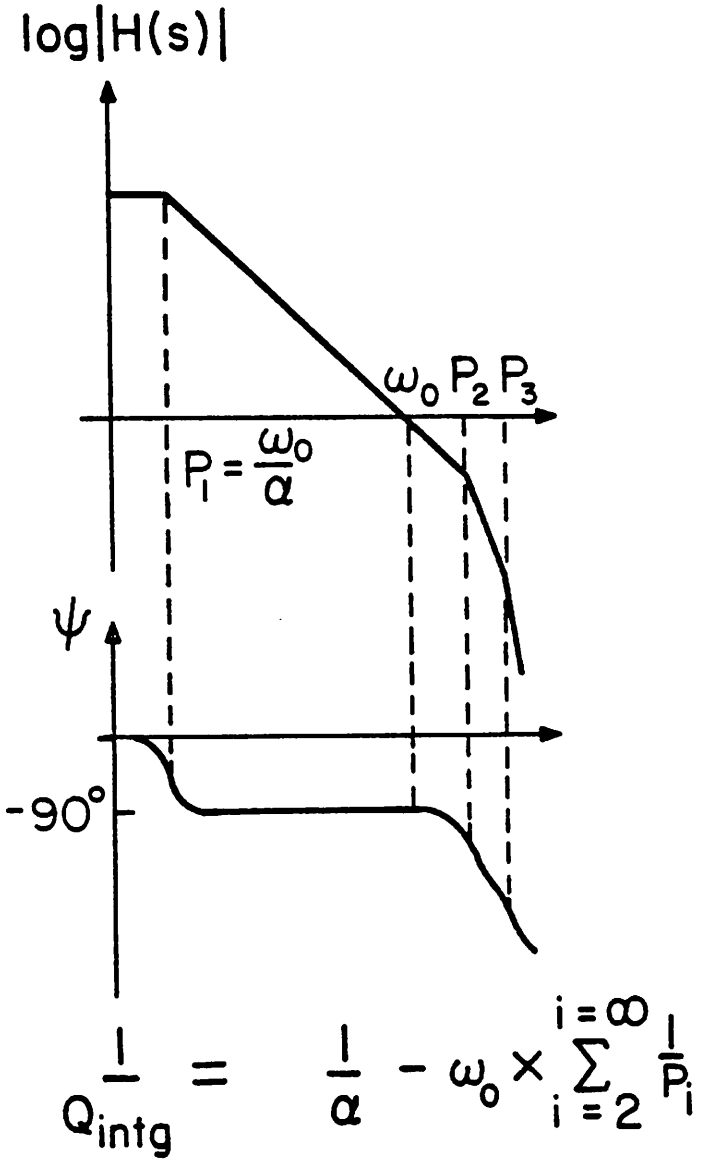


Figure 3.2

Amplitude and phase response of a non-ideal integrator.

thus

$$Q_{intg} = \frac{\omega \left| \frac{a}{\omega_0} + \sum_{i=2}^{i=\infty} \frac{1}{p_i} \right| + \omega^3 \left| \frac{a}{\omega_0} \frac{1}{p_2 p_3} + \ldots \right| + \ldots\ldots}{1 - \omega^2 \left| \frac{a}{\omega_0} \sum_{j=2}^{j=\infty} \frac{1}{p_j} + \frac{1}{p_2} \sum_{k=3}^{k=\infty} \frac{1}{p_k} + \ldots \right| + \ldots\ldots} \tag{3.7}$$

Assuming that all the non-dominant poles p_i are at a much higher frequency than the frequency of interest: that is $\frac{\omega}{p_i} \ll 1$, and that $a \gg 1$, the quality factor of the real integrator in the vicinity of the unity-gain frequency, could be simplified as

$$Q_{intg} \approx \frac{1}{\frac{\omega_0}{\omega} \left| \frac{1}{a} - \omega_0 \sum_{i=2}^{i=\infty} \frac{1}{p_i} \right|} \tag{3.8}$$

Note that the quality factor of the real integrator is frequency dependent whereas the Q of the ideal integrator is equal to infinity for all frequencies.

For $\omega = \omega_0$

$$Q_{intg} \approx \frac{1}{\left| \frac{1}{a} - \omega_0 \sum_{i=2}^{i=\infty} \frac{1}{p_i} \right|} \tag{3.9}$$

substituting for $p_1 = \frac{\omega_0}{a}$ from Fig. 3.2 , it can be found that

$$Q_{intg} \approx \frac{1}{\left| \frac{p_1}{\omega_0} - \omega_0 \sum_{i=2}^{i=\infty} \frac{1}{p_i} \right|} \tag{3.10}$$

The first term is equal to the phase lead at the unity-gain frequency in radians and the second term corresponds to the excess phase at the same frequency. Note that as ω_0 is increased the excess phase term becomes larger.

3.1.3. Effect of Finite Integrator Q on Filter Behavior

The quality factor of the basic element for the implementation of active ladder filters, the integrator, was found in equation (3.10) . This equation suggests that the quality factor of the integrator, at a given unity-gain frequency, could be positive, negative or infinity depending upon the location of the frequency response singularities with respect to ω_0 .

In the following example the effect of the three possible cases of integrator Q on the filter behavior is examined (Fig. 3.3). The bold curve in all three figures shows the frequency response of a sixth order bandpass filter, with an overall Q of 10 constructed with ideal integrators. The broken line in Fig. 3.3(a) shows the frequency response of the same filter made with integrators which have about a 0.56 degree phase lead at their unity-gain frequency. This corresponds to a DC gain of 100 for the integrators. The Q is degraded in this case. In Fig. 3.3(b) the effect of a 0.56 degree excess-phase at the unity-gain frequency of the integrators, which corresponds to a non-dominant pole 100 times larger than the unity-gain frequency, is shown. In this case the Q is enhanced and as mentioned earlier, as ω_0 is increased the excess phase becomes larger and may result in oscillation. Note that the error in the passband of the filter is directly proportional to $\frac{Q_{filter}}{Q_{intg}}$, where Q_{filter} is the overall quality factor of the filter. Fig. 3.3(c) shows the effect of exactly equal amount of phase lead and excess phase at unity-gain frequency of the integrators, which results in phase error cancellation at this frequency. Interestingly enough, the frequency response of the filter in this case is very close to the ideal case.

These considerations suggest that it is very desirable to design the integrator in such a way that the two phase error components cancel each other right at the unity-gain frequency. For this purpose, using equation (3.10) , p_1 and $\sum_{i=2}^{i=\infty} p_i$ should be chosen

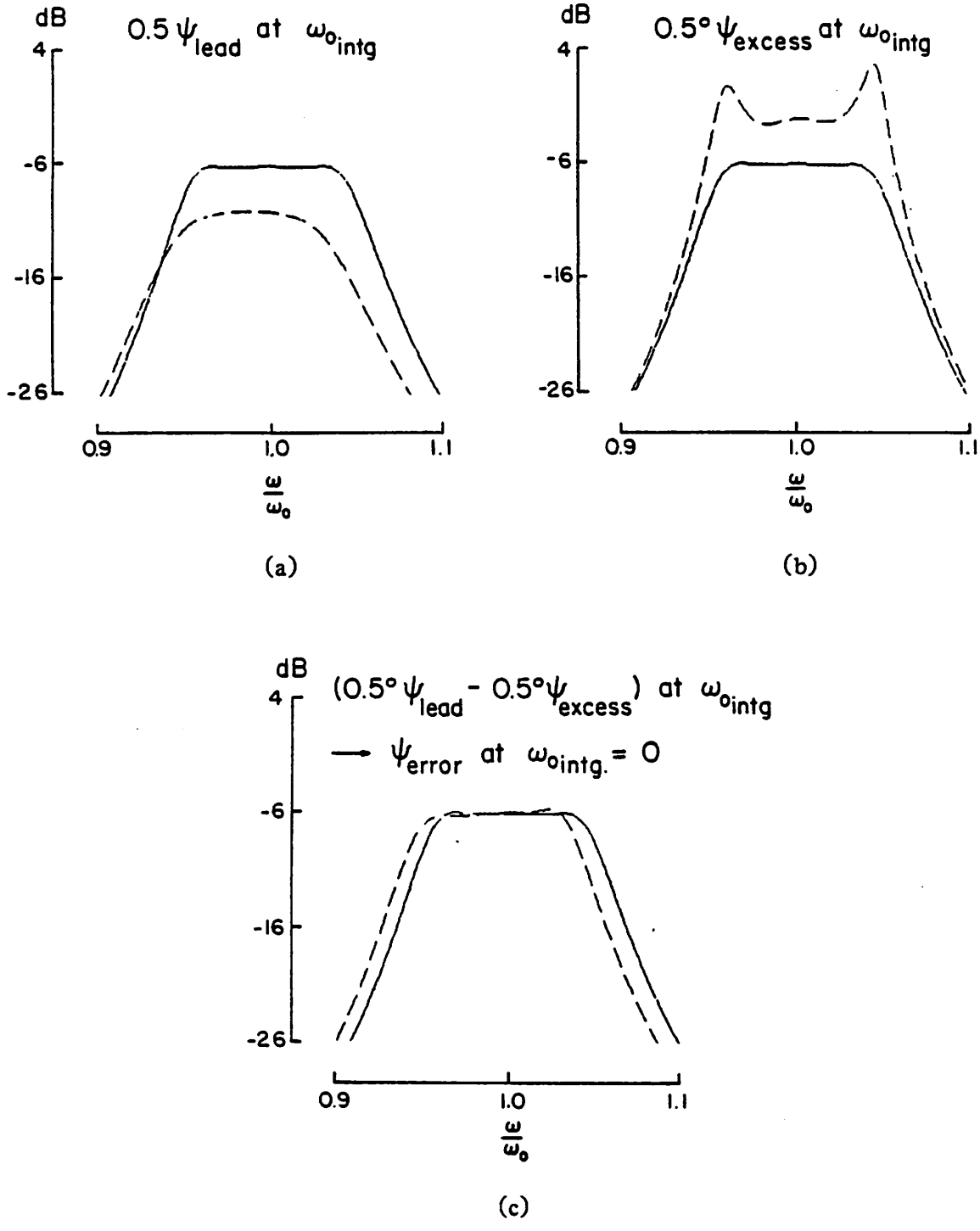


Figure 3.3

Effect of integrator non-idealies on the filter behavior.
(a)- Effect of 0.5 degree phase lead at ω_0 of integrators.
(b)- Effect of 0.5 degree excess phase at ω_0 of integrators.
(c)- Effect of 0.5 degree phase lead and excess phase at ω_0 of integrators.

so that

$$\frac{p_1}{\omega_0} = \omega_0 \sum_{i=2}^{i=\infty} \frac{1}{p_i} \tag{3.11}$$

However, the dependence of the two phase error components on temperature and process variations limits the accuracy of such phase error cancellation in high-frequency filtering applications; and thus, in conjunction with the maximum allowable error in the passband, dictates an upper limit for the maximum Q of the filter. This will be further explored in section 4.1 .

The passive components, used in the design of conventional LC filters, exhibit a frequency dependent loss; in other words a finite Q which is always positive. This results in Q degradation and limits the maximum achievable quality factor of the filter. Hence, by using the phase-error cancellation technique, the active implementation of high-frequency filters might have the capability of successfully achieving higher Q's compared to their passive counterparts.

3.2. Integrator Design

An $R-C$ integrator is typically constructed of a multi-stage operational amplifier connected in the feedback configuration shown in Fig. 3.4 . In the previous section, it was shown that the frequency response of high-frequency filters is very sensitive to extra phase-shift in the integrator. The high-frequency poles of the multi-stage operational amplifier tend to contribute large amounts of excess phase causing a large error in the filter response. An important objective, then, is to design an integrator with preferably no non-dominant poles.

To achieve this goal, a one-stage source-coupled differential pair configuration was chosen to minimize the Q enhancement effects, as shown in Fig. 3.5 . The unity gain frequency ω_0 of this integrator is given by

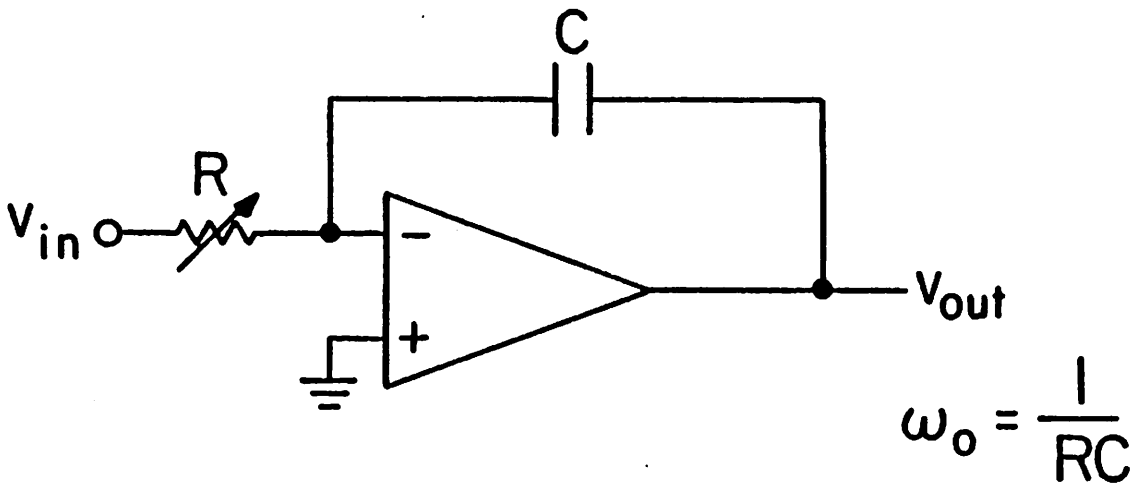


Figure 3.4

Typical integrator configuration

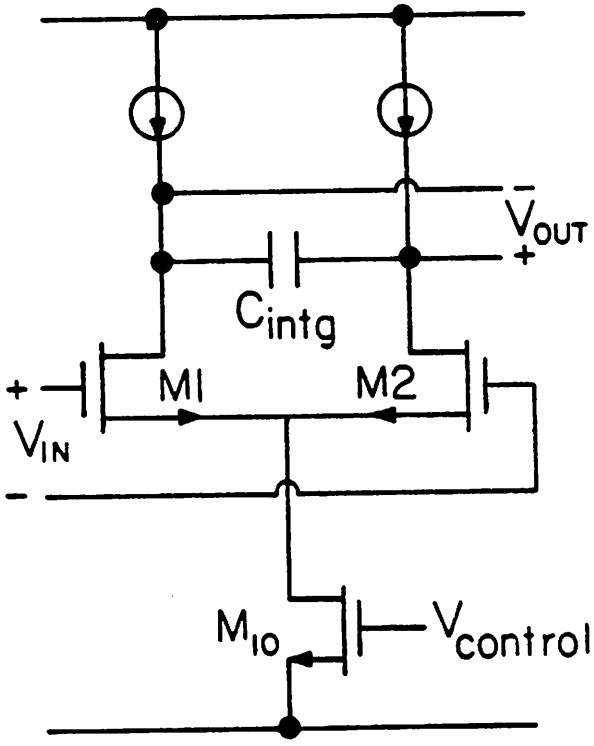


Figure 3.5

Simple differential pair integrator.

$$\omega_0 = \frac{G_{m_{(M1,2)}}}{2C_{intg}} \tag{3.12}$$

where C_{intg} corresponds to the integrating capacitor and $G_{m_{(M1,2)}}$ is the transconductance of the input transistors, and for small signals is given by

$$G_{m_{(M1,2)}} = 2 \left| \tfrac{1}{2} \mu C_{ox} \times \left(\frac{W}{L}\right)_{(M1,2)} \times I_{d_{(M1,2)}} \right|^{1/2} \tag{3.13}$$

where μ is the average carrier mobility in the channel, C_{ox} is the gate oxide capacitance per unit area, W and L are the channel width and length of the input devices and $I_{d_{(M1,2)}}$ corresponds to the drain currents. It is evident that ω_0 is process dependent and can be controlled through $G_{m_{(M1,2)}}$ by varying the drain current of the input transistors through $V_{control}$ as described in chapter 5 .

3.2.1. Quality Factor of the Simple Source-coupled Pair Integrator

The quality factor of the integrator Q_{intg} , is found by using equation (3.9). The first term is derived by finding the DC gain of the integrator. The second term is estimated by finding an effective non-dominant pole $p_{2_{effective}}$ for the integrator.

The DC gain is found to be

$$a = \frac{g_{m_{(M1,2)}}}{g_{0_{(M1,2)}} + g_{0_{load}}} \tag{3.14}$$

where $g_{0_{(M1,2)}}$ and $g_{0_{load}}$ are the small signal output conductance of the input transistors and the load transistors. Assuming that the output resistance of the load transistors is much larger than the output resistance of the input transistors and by substituting for

$$g_{m_{(M1,2)}} = \frac{2I_D}{V_{GS} - V_{th}}$$

and

$$g_{0_{(M1,2)}} = \lambda I_D$$

the gain is found to be

$$a = \frac{2}{\lambda\,(V_{GS}-V_{th})_{(M1,2)}} \tag{3.15}$$

where λ is the channel-length modulation coefficient. In practice λ is estimated from experimental data and is inversely proportional to the channel length neglecting the short-channel effects. Here, for simplicity, a new parameter θ is introduced

$$\lambda = \frac{\theta}{L} \tag{3.16}$$

where θ is in the order of 0.1 $\left[\frac{\mu}{V}\right]$.

Substituting for λ gives

$$a = \frac{2\,L}{\theta\,(V_{GS}-V_{th})_{(M1,2)}} \tag{3.17}$$

Fig. 3.6 shows the small-signal equivalent differential mode half-circuit of the integrator. The circuit has only two nodes, an input node and an output node. The simple IGFET model predicts no non-dominant poles for this integrator; in other words, for a transistor biased in the saturation region, a constant drain current as a function of frequency is predicted when the gate is driven by a voltage source (Fig. 3.7(a)). However, a more detailed consideration of the distributed nature of the channel resistance and gate capacitance, as illustrated in Fig. 3.7(b) and Fig. 3.7(c), shows that the frequency response of the transconductance falls off at high-frequencies. It can be shown that this phenomena gives rise to an infinite number of high-frequency poles. In the previous chapter, it was shown that as long as the non-dominant poles are much higher in frequency than the unity-gain frequency of the integrator, it is enough to find the effective non-dominant pole which is at

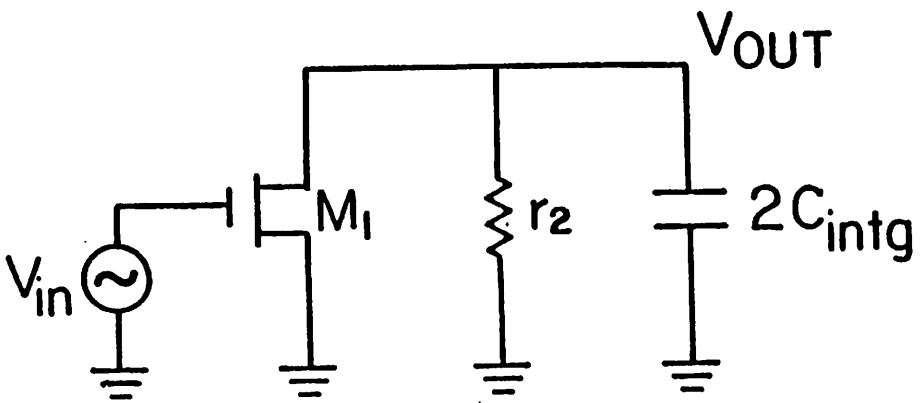
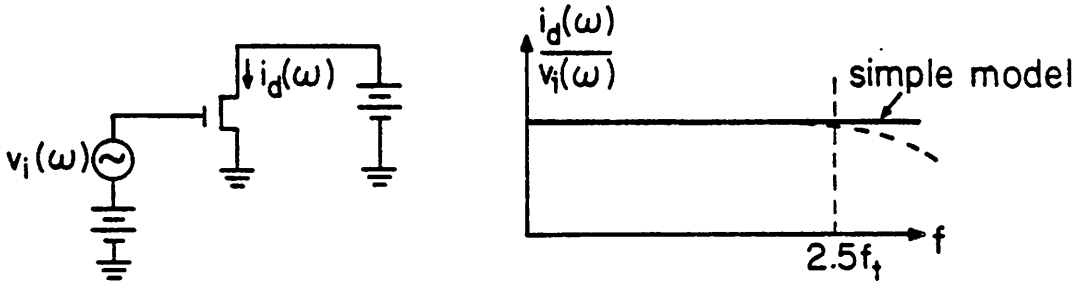
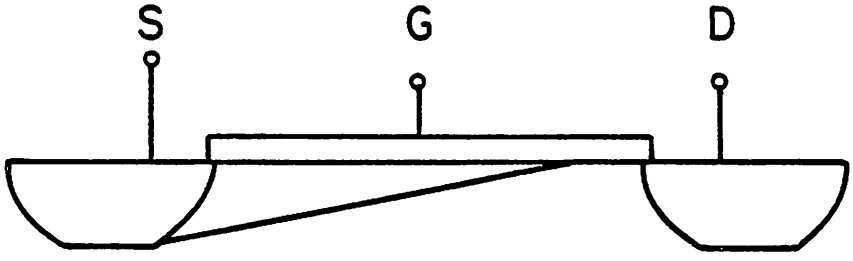


Figure 3.6

Small signal equivalent differential mode
half-circuit of the integrator.



(a)



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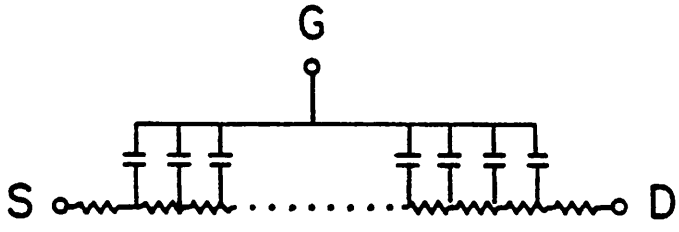


(c)

Figure 3.7

The high-frequency behavior of an MOS transistor.
(a)-Drain current as a function of frequency.
(b)-Cross-section view of an MOS transistor in saturation.
(c)-The distributed channel resistance and gate capacitance.

$$p2_{effective} \approx \frac{1}{\sum_{i=2}^{i=\infty} \frac{1}{p_i}} \tag{3.18}$$

rather than the exact location of each individual pole. In appendix A. it is proven that in this case

$$p2_{effective} \approx 2.5\ \omega_{t_{(M1,2)}} \tag{3.19}$$

where ω_t is the frequency at which the current gain of the input transistor is equal to one and is given by

$$\omega_{t_{(M1,2)}} = \frac{g_{m_{(M1,2)}}}{\frac{2}{3} C_{ox} WL} = \frac{3}{2} \frac{\mu (V_{GS} - V_{th})}{L^2} \tag{3.20}$$

Note that the integrator effective non-dominant pole is at a much higher frequency than for a typical operational amplifier type integrator. The contribution of this phenomena to the integrator phase shift at the unity gain frequency is

$$\phi_{lag} \approx \frac{\omega_0}{2.5\ \omega_{t_{(M1,2)}}} = \frac{4}{15} \frac{\omega_0 L^2}{\mu (V_{GS} - V_{th})_{(M1,2)}} \tag{3.21}$$

Substituting from (3.17) and (3.21) in (3.10)

$$Q_{intg} \approx \frac{1}{\frac{\theta (V_{GS} - V_{th})_{(M1,2)}}{2L} - \frac{4}{15} \frac{\omega_0 L^2}{\mu (V_{GS} - V_{th})_{(M1,2)}}} \tag{3.22}$$

Here it is assumed that the Q of the integrating capacitor is much larger than the other components quality factor and can be neglected, which is usually the case. The above equation shows that the excess phase-shift is proportional to $L^2_{(M1,2)}$. whereas the phase lead due to the finite DC gain is proportional to $\frac{1}{L_{(M1,2)}}$. From this the conclusion can be drawn, that for a well-characterized well-controlled process, an optimum input transistor channel-length can be chosen for first order phase error cancellation at

a given frequency which makes the realization of high-Q filters possible. The optimum input channel length will be derived in the next section, where the contribution of the loading integrator to the quality factor of the integrator is also accounted for.

Inspecting the differential mode half circuit, it can be seen that there is a feed forward path between the input and the output through the C_{gd} of the input transistors (a right half plane zero). In the next section, it will be shown that connecting the integrators in a resonator configuration results in the disappearance of the right half plane zero.

3.3. Resonator Design Considerations

In Fig. 3.8, a resonator is implemented by connecting two integrators back to back. In this part, first the effect of the parasitic capacitances on the resonator behavior is discussed; then, the quality factor of the resonator is found, and in the last part the design of a terminated resonator is discussed.

3.3.1. Effect of Parasitic Capacitance on the Resonator Behavior

The parasitic capacitance at the output of each integrator consists of:

a) Gate-source capacitance of the input transistors, C_{gs}, of the next stage integrator and is equal to

$$C_{gs} = \frac{2}{3}(WL)_{M1,2}C_{ox} \tag{3.23}$$

plus the gate-source overlap capacitance (same as part (b)).

b) Gate-drain capacitance, C_{gd}, of the integrator input transistors due to the overlap of the gate oxide and the drain diffusion.

$$C_{gd} = W\ L_d\ C_{ox} \tag{3.24}$$

c) Drain-substrate capacitance of the input transistor, C_{db}, which is the junction depletion capacitance between the drain and substrate for these transistors.

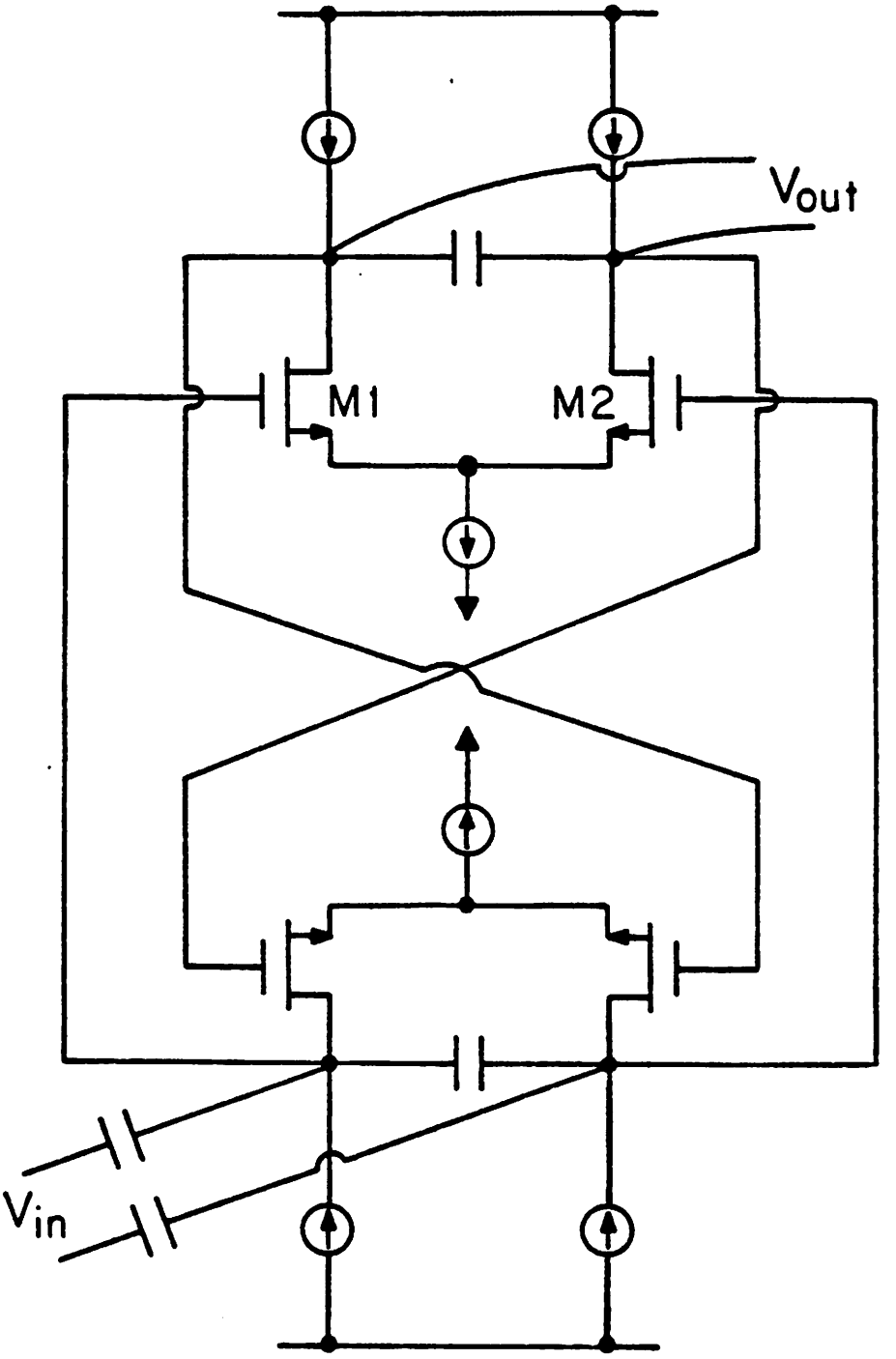


Figure 3.8

Circuit configuration of a resonator.

d) Load transistor capacitance, $C_{J_{load}}$, which is the capacitance of the load current sources.

e) Parasitic capacitance of the integrating capacitor, $C_{par_{C_{intg}}}$, which for a single poly process is the junction depletion capacitance between the capacitor bottom plate diffusion and the substrate.

All of the above capacitances tend to increase the effective value of the integrating capacitor and therefore increase ω_0.

$$C_{intg_{total}} = C_{intg} + \frac{1}{2}\sum_{all} C_{par} \tag{3.25}$$

For low frequency applications, where $C_{intg} \gg C_{par}$, the parasitic capacitances could be neglected. At high frequencies, where the size of the integrating capacitors is not significantly larger than the input transistors, parasitic capacitances should be accounted for.

3.3.2. Resonator Quality Factor

The resonator quality factor is given be

$$\frac{1}{Q_{res}} = \frac{2}{Q_{intg}} + \frac{2}{Q_{C_{par}}} \tag{3.26}$$

It can be shown that the overall Q is determined by the larger capacitors and the effect of the smaller ones is negligible. The largest parasitic capacitance at the output node is the gate-source capacitance of the input transistors of the next stage. In Appendix A, it is found that the input impedance of an MOS transistor biased in the saturation region behaves as a lossy capacitor with a quality factor, $Q_{C_{gs}}$, of

$$Q_{C_{gs}} \approx \frac{5\,\omega_t}{\omega} \tag{3.27}$$

substituting from (3.22) and (3.27) in (3.26), the resonator quality factor is found to

be

$$\frac{1}{Q_{res}} \approx \frac{\theta\,(V_{GS}-V_{th})_{(M1,2)}}{L} - \frac{4}{15}\,\frac{\omega_0 L^2}{\mu\,(V_{GS}-V_{th})_{(M1,2)}} \tag{3.28}$$

It is interesting to note that the phase lag term is cut by exactly half due to the loss in the gate-source capacitances. From the equation above, by equating the two terms, an optimum channel length for the input transistor is found for which the phase error is canceled

$$L_{opt} \approx \left[\frac{15}{4}\,\frac{\theta\,\mu\,(V_{GS}-V_{th})^2_{(M1,2)}}{\omega_0} \right]^{1/3} \tag{3.29}$$

The above equation suggests that the optimum input transistor channel length is a function of the center frequency of the filter. As the center frequency is increased, L_{opt}, for which the phase error is canceled, tends to decrease. Values for L_{opt} as a function of the center frequency, are calculated in section 4.1.

One interesting aspect of this resonator circuit configuration is that the right-half plane zero due to the gate-drain capacitances of the input transistors cancel out. This can be more clearly understood by inspecting Fig. 3.9 . Let's consider node C. There are two signal feed-through paths to this node. One is from node A through the gate-drain capacitance of M_1 ; the other path runs from node B through the C_{gd} of M_3 . As the circuit is fully balanced, the signals at nodes A and B are equal and of opposite signs, resulting in signal cancellation at node C.

3.3.3. Terminated Resonator Design

Fig. 3.10 shows the flow-graph of a terminated resonator. Here the termination is realized by feeding back a fraction equal to $1/Q$ of the output of the resonator to its input.

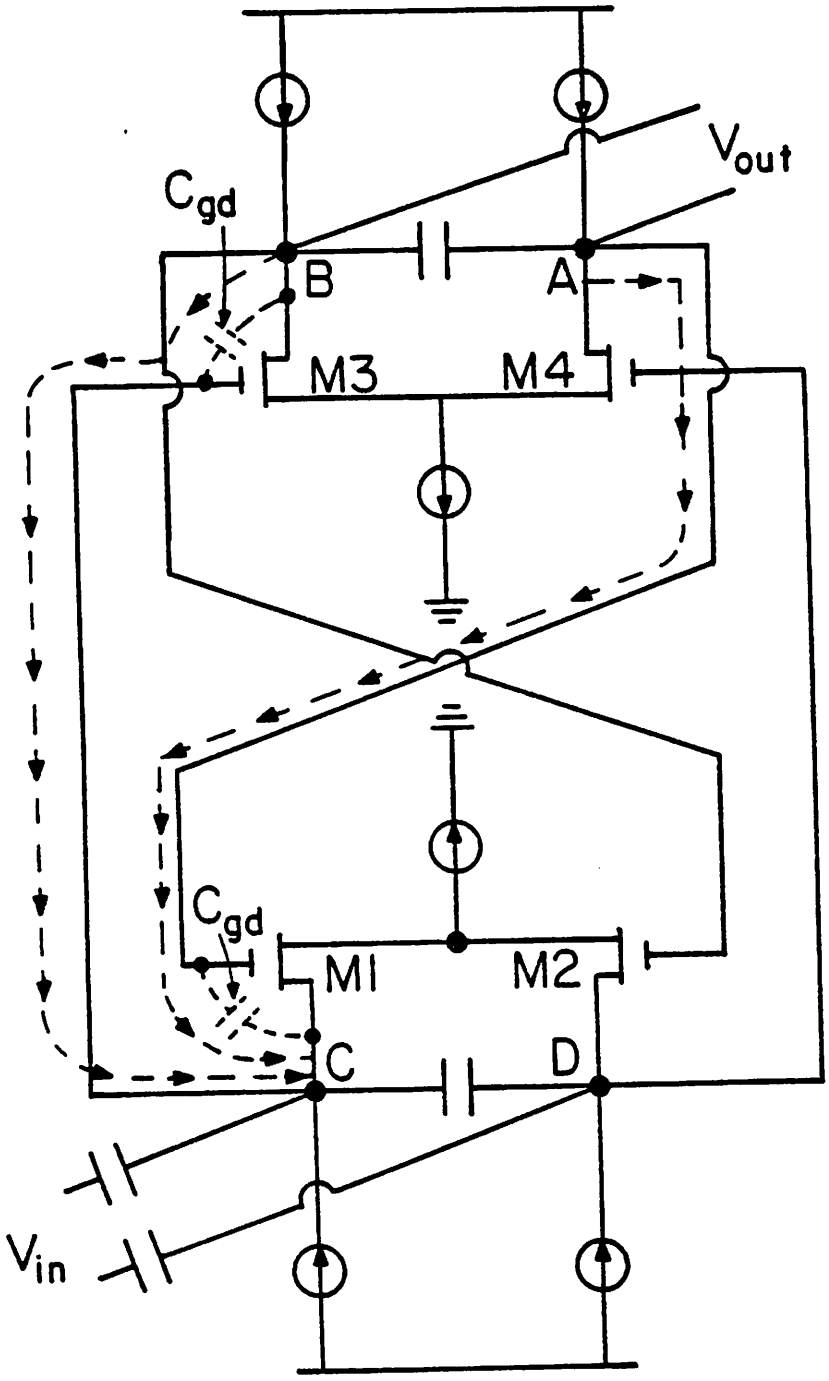


Figure 3.9

Feed-through paths to node C of the resonator

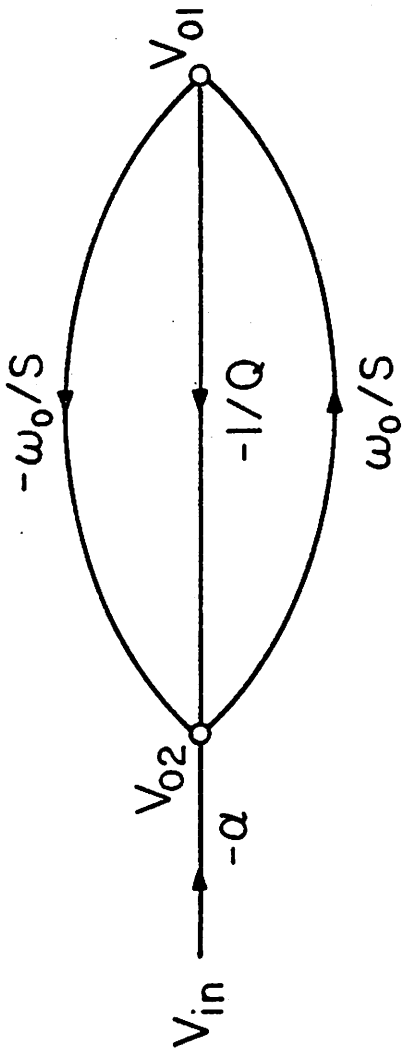


Figure 3.10

Flow-graph of a terminated resonator.

One approach to this is shown in Fig. 3.11 where the feedback is provided through a buffer at the output and the capacitor C_Q.

Using this configuration the Q is given by

$$Q = \frac{2C_{int}}{C_Q} \tag{3.30}$$

This scheme works well for resonators with low center frequencies . However, at higher frequencies, the inherent phase-shift between the input and the output of the buffer distorts the frequency response of the filter.

To overcome this problem the conventional flow-graph is transformed to the one shown in Fig. 3.12 . This new flow-graph can be realized by adding a resistive load to the output of one of the integrators. Fig. 3.13 shows a simple implementation of the resistive load. The equivalent load resistance seen in parallel with the corresponding integrating capacitor is equal to

$$R_{eq} = \frac{2}{G_{m(M3,4)}} \tag{3.31}$$

which results in

$$Q = \frac{G_{m(M1,2)}}{G_{m(M3,4)}} \tag{3.32}$$

Thus, the Q is set by scaling the $\frac{W}{L}$ ratios of $M_{1,2}$ and $M_{3,4}$ as well as the current sources. This will be discussed further in section 3.5.

3.4. Filter Design

The classical doubly-terminated LC ladder structure was used in the experimental chip described in chapter 6 due to its low sensitivity to component variations (Fig. 3.14)[7],[8]. The flow-graph for such a filter is shown in Fig. 3.15 [9] which is constructed of three resonators interconnected through unilateral coupling paths. All

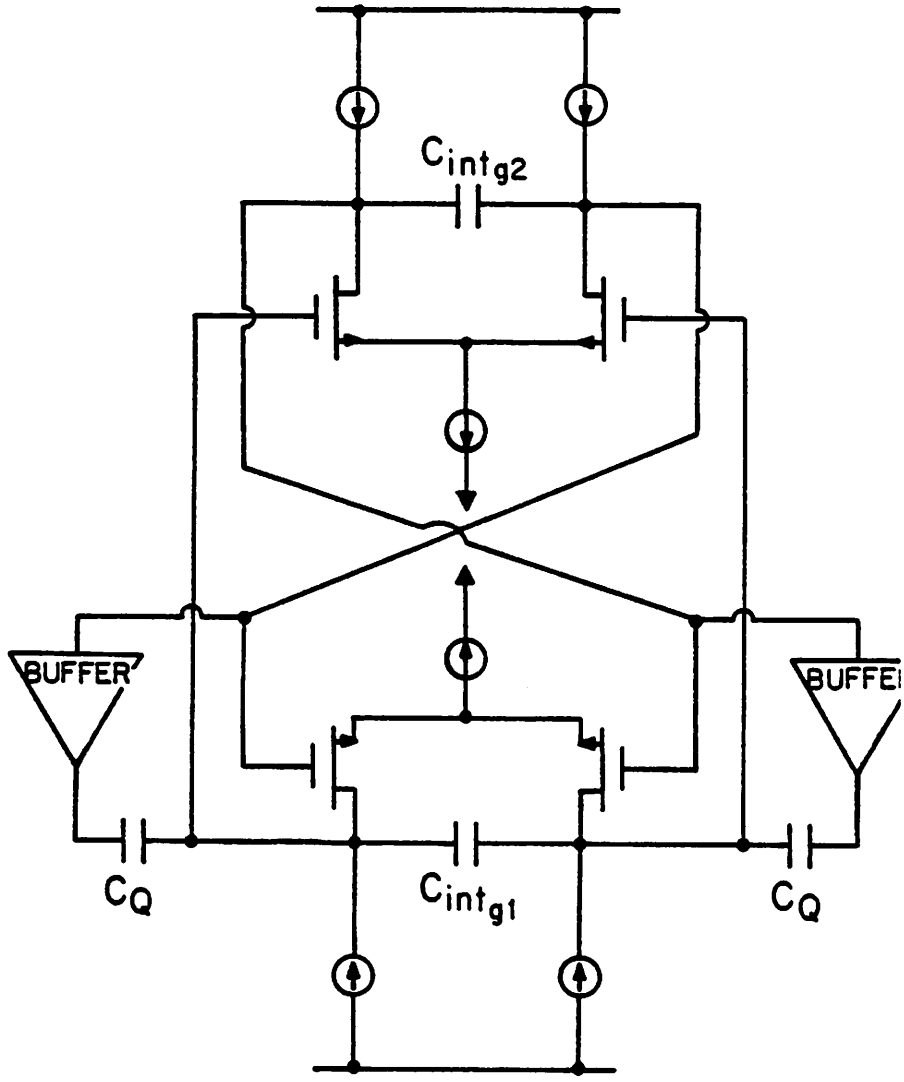


Figure 3.11

Direct termination implementation.

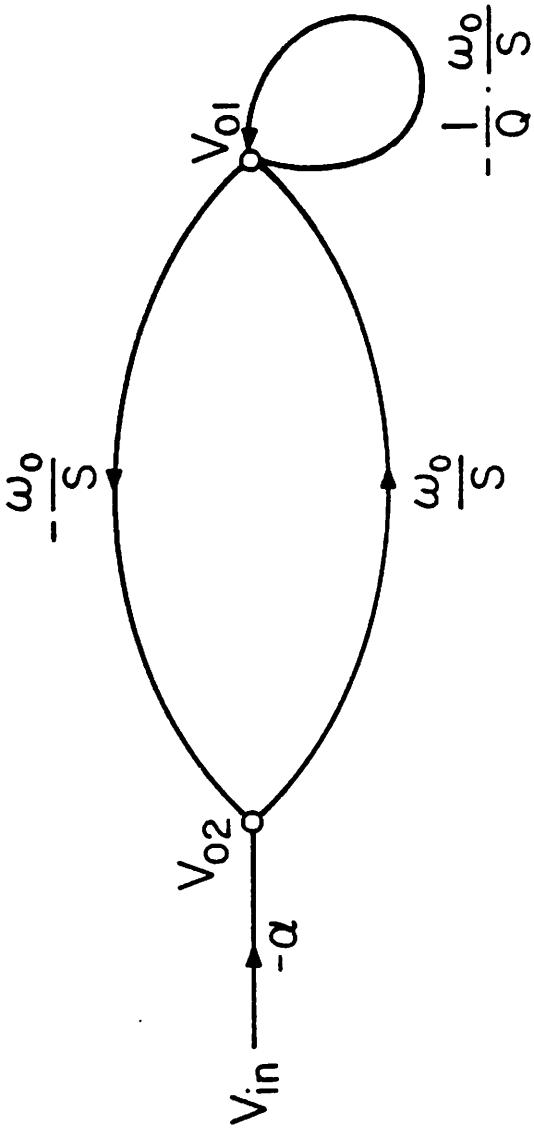


Figure 3.12

Modified flow-graph for termination implementation.

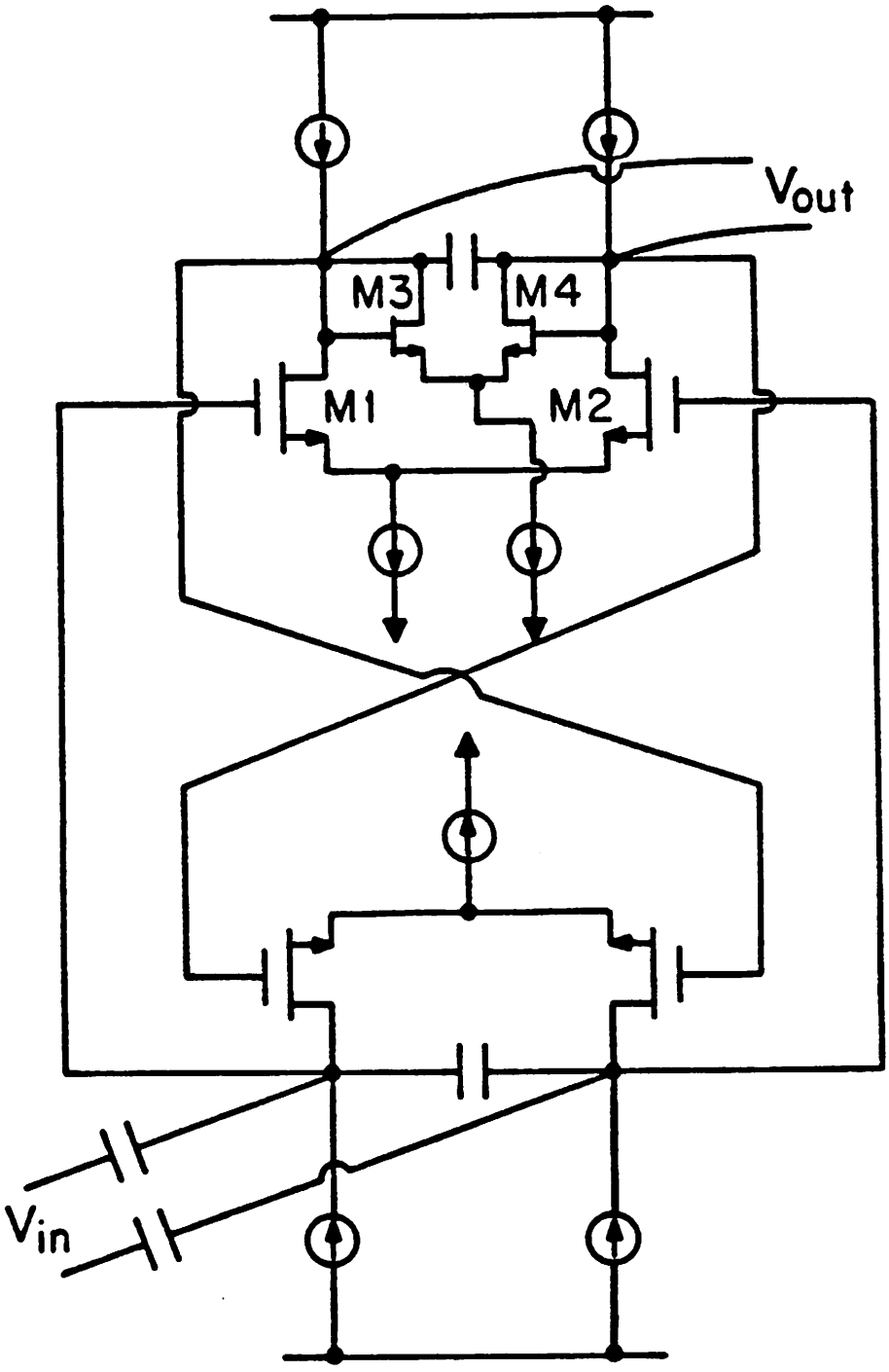


Figure 3.13

Circuit implementation of the termination.

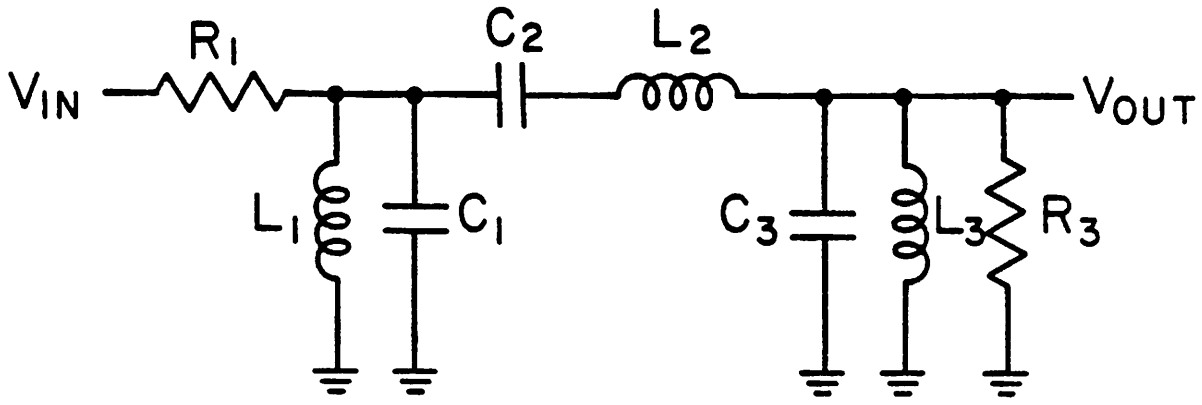


Figure 3.14

Sixth order LC ladder filter.

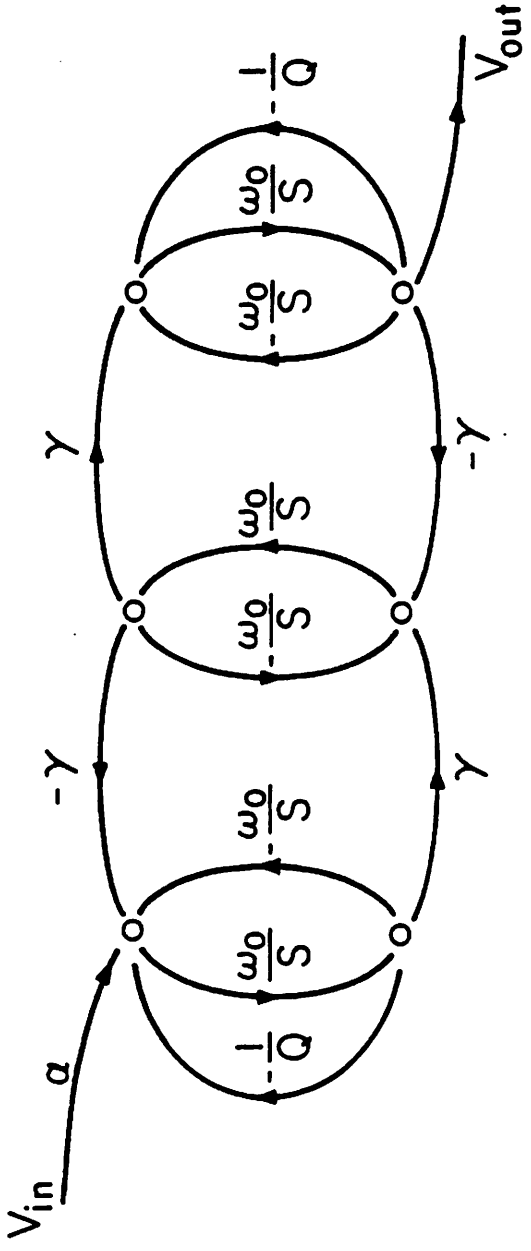


Figure 3.15

Flow-graph of the sixth order ladder filter.

integrators are chosen to have the same time constant for optimum sensitivity [3]. Using the resonator designed in the previous section, the implementation of the filter brings about the requirement of buffers at the resonator outputs for the unilateral coupling paths. This results in an increased die area and increased power consumption. Moreover, for filters with high center frequencies, the extra phase-shift caused by the buffer may result in a significant distortion in the filter frequency response . This problem can be alleviated by converting the flow-graph to the configuration shown in Fig. 3.16. Note that for narrow-band filters, the following assumption is true within the passband of the filter

$$\frac{\omega_0^2}{s^2} \approx -1 \tag{3.33}$$

Using this approximation the coupling paths are transformed to bilateral paths with equal values as shown in Fig. 3.17. This approximation is called the narrow-band approximation which exhibits a reasonable passband shape for a Q greater than about 4 [10]. Fig. 3.18 shows the frequency response of a bandpass filter using the conventional flow-graph and the frequency response for the narrow-band approximated filter. By inspecting the frequency response, it can be seen that the narrow-band approximation causes the filter frequency response to be slightly unsymmetrical .

Fig. 3.19 shows the active implementation of a narrow-band approximated sixth-order bandpass filter using the designed integrator. Note that using the above approximation, the active realization is simply done by using three resonators coupled through capacitors (C_k). The coupling coefficient is given by

$$\gamma = \frac{2C_{intg}}{C_k} \tag{3.34}$$

The center frequency of the filter is controlled by $V_{control}$ by varying the transconductance of all input transistors which makes the matching of these transistors critical as

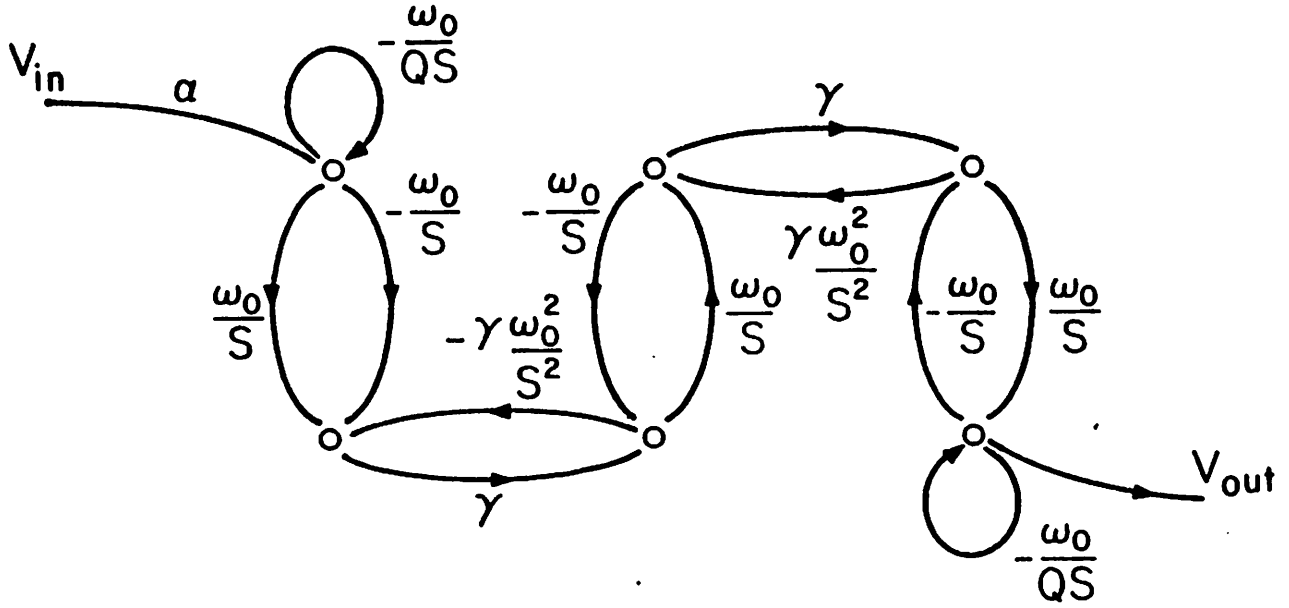


Figure 3.16

Modified flow-graph of the sixth-order filter.

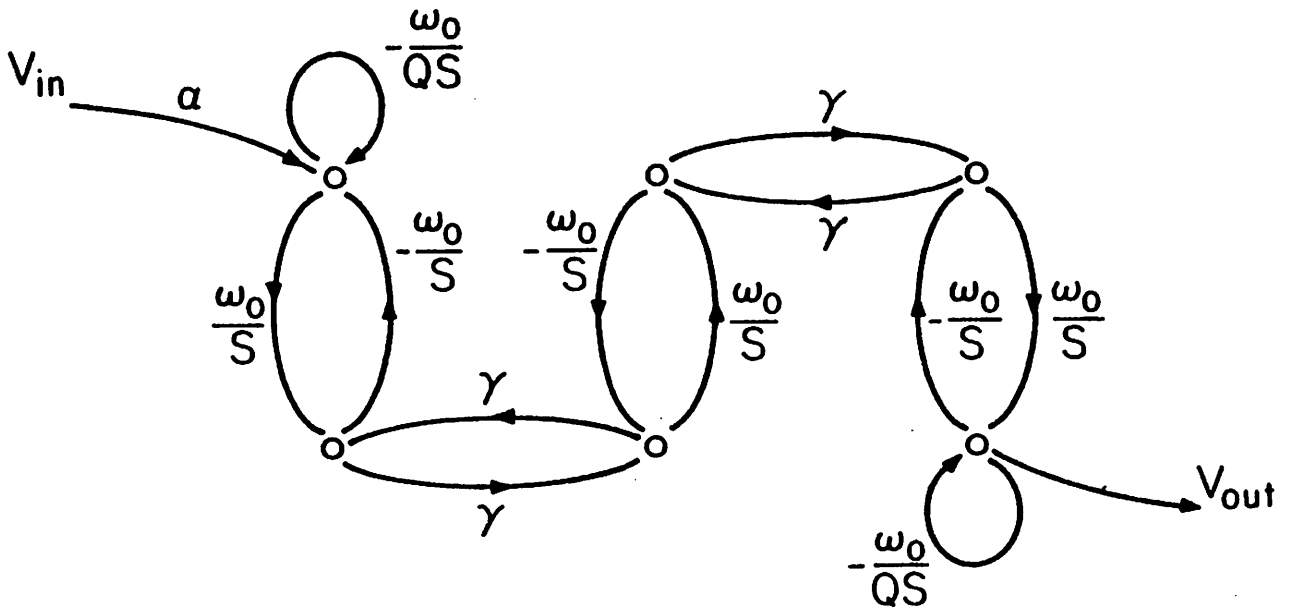


Figure 3.17

Modified flow-graph of the sixth-order filter.

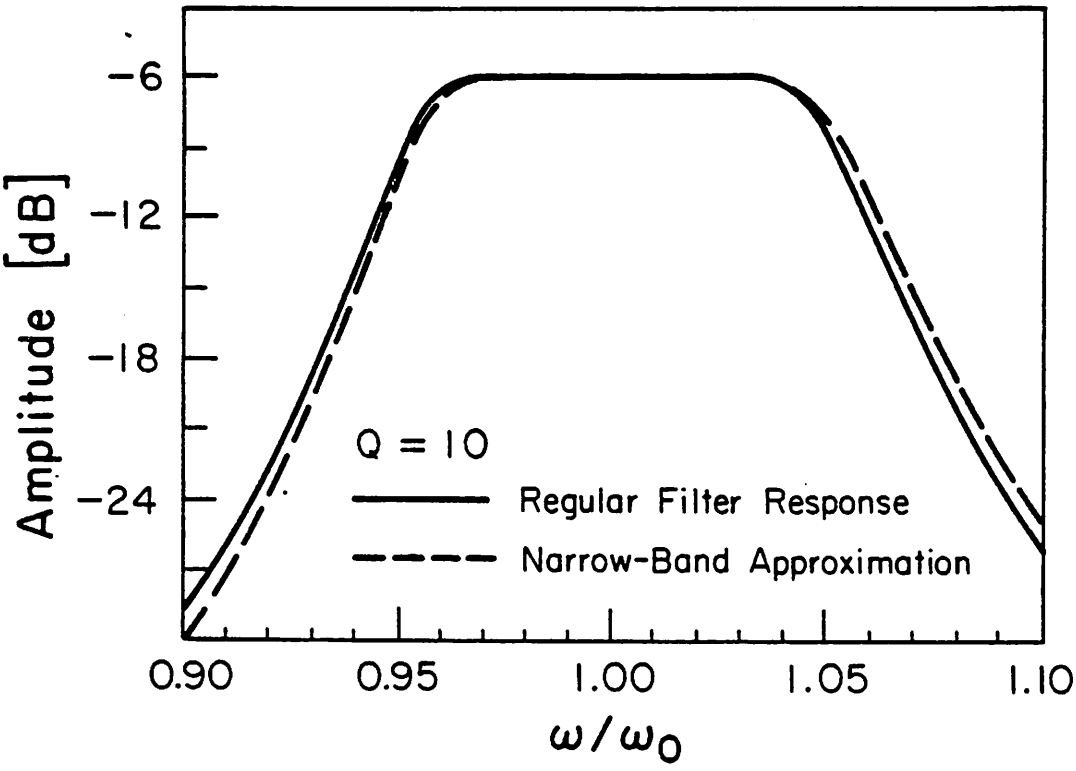


Figure 3.18

Frequency response of a conventional sixth-order bandpass filter and the narrow-band approximated version.

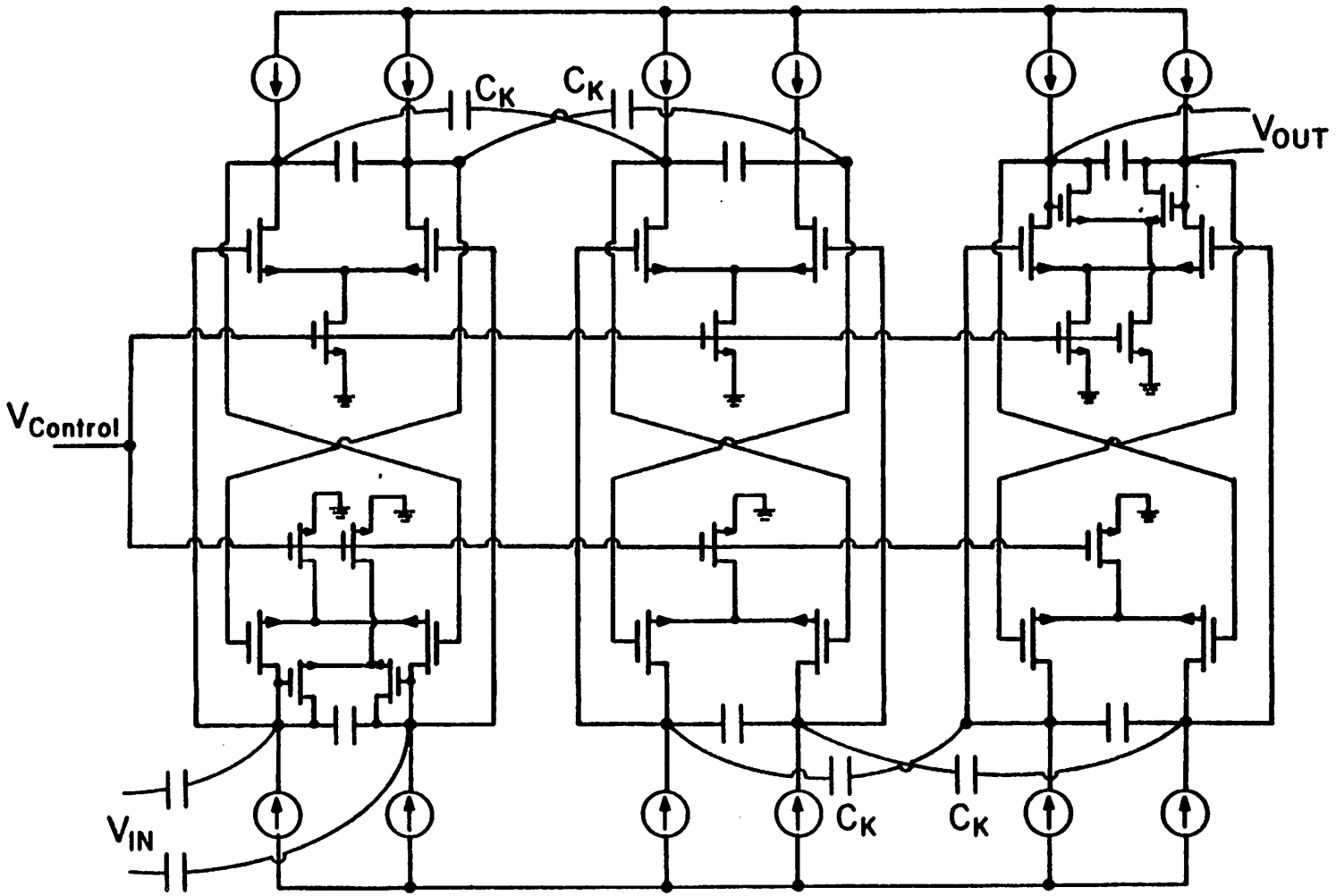


Figure 3.19

Active implementation of the sixth order ladder filter.

discussed in section 4.3.

The fully differential architecture immunizes the filter response to the power supply variations and parasitic couplings and the reference signal feed-through to the output of the filter.

3.5. Final Integrator Design

The complete schematic of the integrator is shown in Fig. 3.20. The common mode output voltage is stabilized by M_5,M_6 which operate in the triode region. M_3,M_4 are the termination devices and are connected in the $(A-A')$ configuration for terminated integrators: $(B-B')$ connection is made for unterminated integrators for matching purposes.

The quality factor of a terminated integrator Q_{intg}^{term} was found in section 3.3.

$$Q_{intg}^{term} = \frac{G_{m(M1,2)}}{G_{m(M3,4)}} = \frac{\left[\left(\frac{W}{L}\right)_{(M1,2)} \times I_{d(M1,2)} \right]^{1/2}}{\left[\left(\frac{W}{L}\right)_{(M3,4)} \times I_{d(M3,4)} \right]^{1/2}} \tag{3.35}$$

where

$$\frac{I_{d(M1,2)}}{I_{d(M3,4)}} = \frac{\left(\frac{W}{L}\right)_{(M10)}}{\left(\frac{W}{L}\right)_{(M11)}} \tag{3.36}$$

By chosing equal channel lengths for $M_{1,2}$, $M_{3,4}$ and M_{10} , M_{11} , the Q can be implemented by scaling the channel widths of these transistors. To achieve high accuracy for the Q implementation, the termination transistor is chosen as a unit transistor and the input transistors are constructed of an array of Q unit transistors connected in parallel.

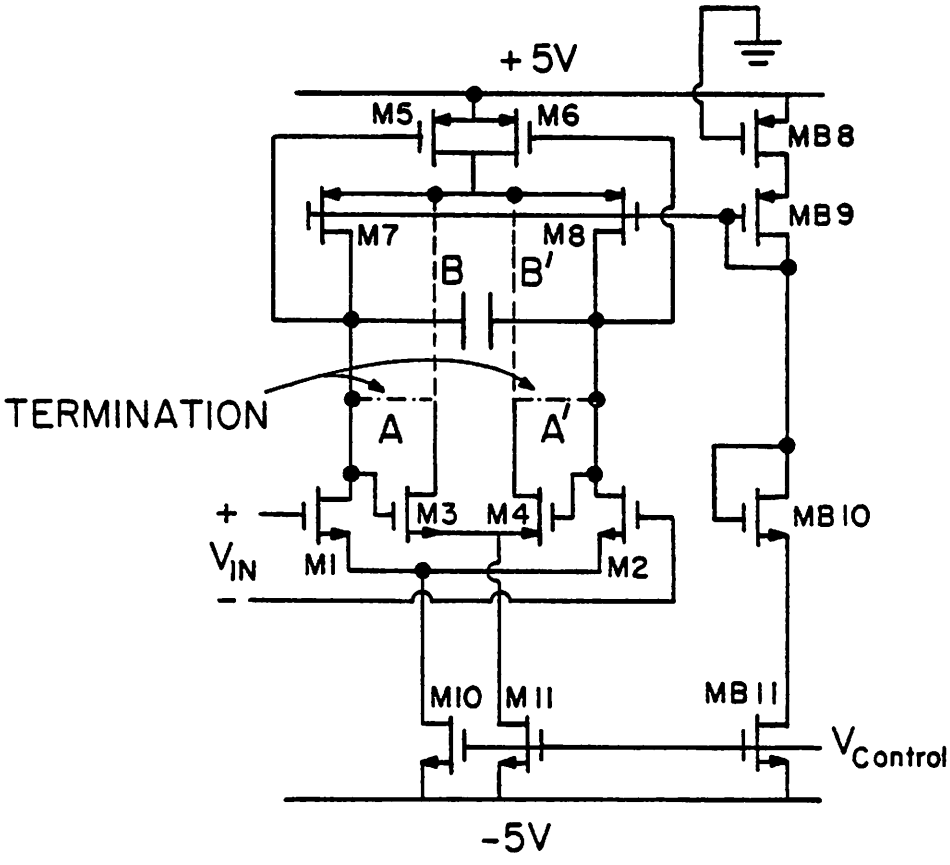


Figure 3.20

Complete schematic of the integrator.

CHAPTER 4

LIMITATIONS OF THE IMPLEMENTATION OF MONOLITHIC CONTINUOUS-TIME FILTERS

In chapter 3, a simple integrator was designed and used to construct a sixth-order continuous-time bandpass filter. In this chapter, the fundamental limitations of such an approach are investigated.

In the first section, the maximum achievable quality factor of the filter as a function of process parameter variations and the center frequency is discussed in detail.

In the second section, the dynamic range of the filter is determined by finding an upper and lower limit for an acceptable output signal.

The third section deals with the effect of transistor mismatches on the behavior of the filter.

Finally, the design of a bandpass filter at the center frequency of 500 KHz is discussed.

4.1. Quality Factor Limitations as a Function of Frequency

In this section the limitations of the quality factor of the filter, imposed by the process and temperature variations, are studied in detail.

The error in the filter passband is directly proportional to the ratio of $\frac{Q_{filter}}{Q_{intg}}$; in other words, the maximum achievable filter quality factor, Q_{filter}, is dictated by the maximum allowable passband error and the minimum integrator quality factor Q_{intg}.

In chapter 3, the phase error cancellation technique was proposed to be utilized in the integrator design. For this purpose, an optimum input transistor channel length

was derived. Ideally, by using this technique, there should be no restrictions on the filter quality factor. However, process and temperature variations limit the accuracy of such phase error cancellation which results in a finite integrator quality factor and thus, dictates an upper limit for the maximum Q of the filter.

In this section the optimum input transistor channel length is first found as a function of frequency followed by the derivation of the worst case integrator quality factor; and then, the maximum quality factor of the filter is derived for different frequencies.

4.1.1. Optimum Input Transistor Channel Length as a Function of Frequency

In chapter 3, the optimum input transistor channel length was found to be

$$L_{opt} \approx \left| \frac{15}{4} \frac{\theta \mu (V_{GS}-V_{th})^2_{(M1,2)}}{\omega_0} \right|^{1/3} \tag{4.1}$$

To find realistic values for L_{opt}, we will assume that the process has the typical parameters that are summarized in Table 4.1. For $L_{opt} > 6\mu$, the gate overdrive factor $(V_{GS}-V_{th})$ is set equal to $1V$ and for $L_{opt} \leq 6\mu$ the $(V_{GS}-V_{th})$ is chosen to be about $0.7V$. The optimum channel length is calculated and listed in the second row of Table 4.2 and is sketched in Fig. 4.1.

4.1.2. Worst Case Integrator Quality Factor

In chapter 3, the resonator quality factor was found to be

$$\frac{1}{Q_{res}} \approx \frac{\theta (V_{GS}-V_{th})_{(M1,2)}}{L} - \frac{4}{15} \frac{\omega_0 L^2}{\mu (V_{GS}-V_{th})_{(M1,2)}} \tag{4.2}$$

The integrator quality factor, connected in a resonator configuration, is found by multiplying the resonator Q by a factor of 2

$$\frac{1}{Q_{intg}} \approx \frac{\theta (V_{GS}-V_{th})_{(M1,2)}}{2L} - \frac{2}{15} \frac{\omega_0 L^2}{\mu (V_{GS}-V_{th})_{(M1,2)}} \tag{4.3}$$

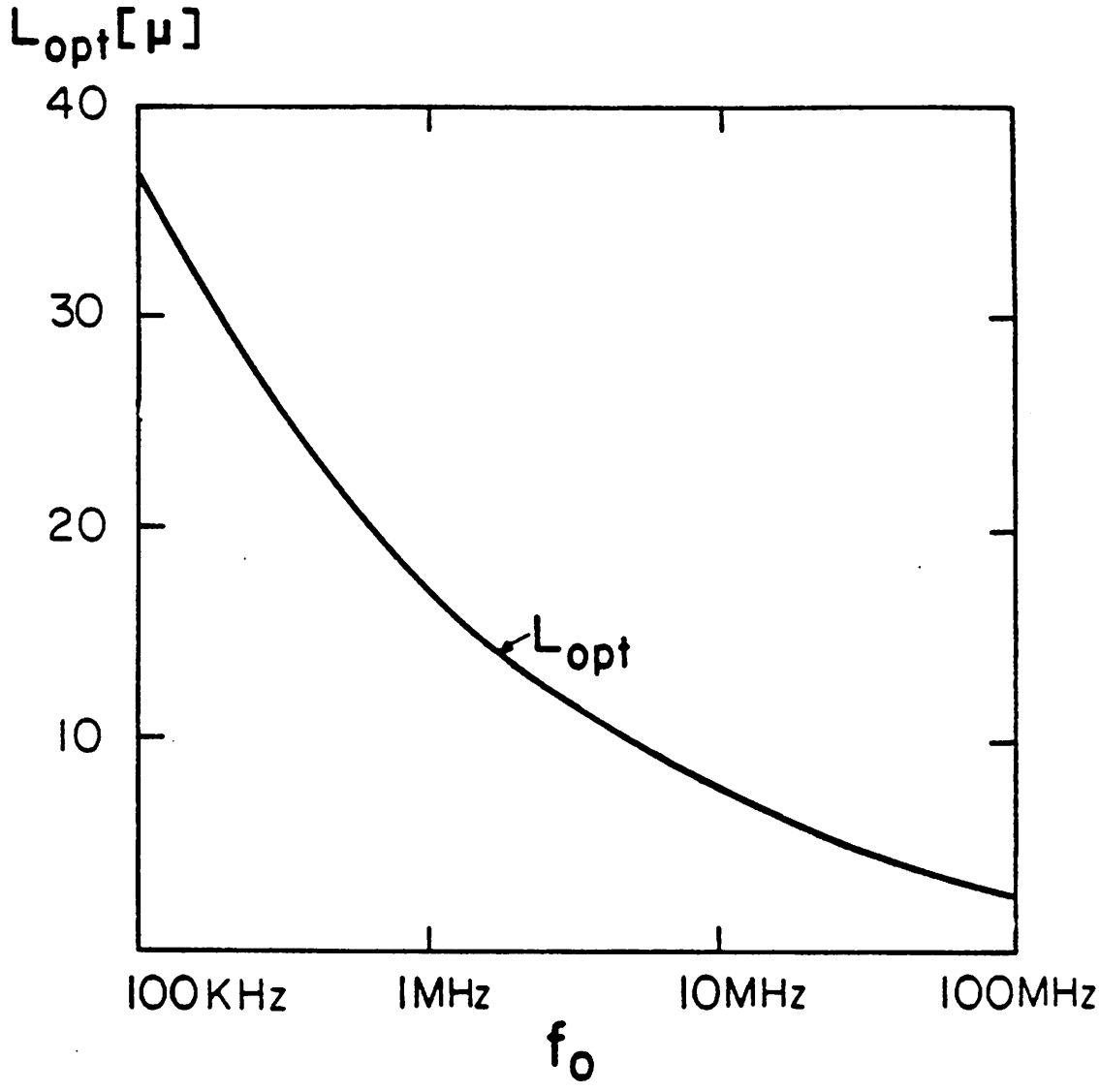


Figure 4.1

Optimum input transistor channel length as a function of frequency.

Parameter	Symbol	Average Value	Tolerance	Units
Gate Oxide Thickness	t_{ox}	400	±10%	*Angstroms*
Channel Mobility n-type	μ_n	700	∓10%	$cm^2/\ v-sec$
Channel Mobility p-type	μ_p	350	∓10%	$cm^2/\ v-sec$
Channel Length Modulation Factor n-type	$\theta_n = \frac{\lambda_n}{L}$	0.1	±15%	*Microns / v*
Channel Length Modulation Factor p-type	$\theta_p = \frac{\lambda_p}{L}$	0.13	±15%	*Microns / v*
Uncertainty in Poly-Silicon Etching	ΔL		±0.5	*Microns*

Table 4.1. Summary of Process Parameters and Tolerances for a Typical N-Well Silicon-Gate CMOS Process

substituting for $(V_{GS}-V_{th})_{(M1,2)} = \dfrac{\omega_0 C_{intg}}{\frac{\mu C_{ox}}{2}\frac{W}{L}}$ in the above equation

$$\frac{1}{Q_{intg}} \approx \frac{\theta\ \omega_0 C_{intg}}{\mu C_{ox} W} - \frac{1}{15}\frac{WL\ C_{ox}}{C_{intg}} \qquad (4.4)$$

Assuming that the integrating capacitor is constructed of an array of m unit capacitors connected in parallel

$$C_{intg} = m\ W_{cap}\ L_{cap}\ C_{ox_{cap}} \tag{4.5}$$

where W_{cap} and L_{cap} are the width and length of the unit capacitor and are usually chosen to have equal values and $C_{ox_{cap}}$ is the capacitor oxide capacitance per unit area. Substituting for C_{intg} in (4.4)

$$\frac{1}{Q_{intg}} \approx \frac{\theta\ \omega_0}{\mu}\ \frac{m\ W_{cap}\ L_{cap}}{W}\ \frac{C_{ox_{cap}}}{C_{ox}} - \frac{1}{15}\ \frac{WL}{m\ W_{cap}\ L_{cap}}\ \frac{C_{ox}}{C_{ox_{cap}}} \tag{4.6}$$

For the ideal case, both terms in the above equation are equal thus it is assumed that each term is equal to $\frac{1}{Q_a}$. Now the quality factor can be estimated in terms of Q_a and the process parameter tolerances by

$$\frac{1}{Q_{intg}} \approx \frac{1}{Q_a}\left| + \frac{\Delta\theta}{\theta} - \frac{\Delta\mu}{\mu} + 2\frac{\Delta W_{cap}}{W_{cap}} + 2\frac{\Delta L_{cap}}{L_{cap}} - 2\frac{\Delta W}{W} + 2\frac{\Delta C_{ox_{cap}}}{C_{ox_{cap}}} - 2\frac{\Delta C_{ox}}{C_{ox}} - \frac{\Delta L}{L}\right| \tag{4.7}$$

The fact that the terms corresponding to the capacitor oxide capacitance and the gate oxide capacitance are of opposite signs suggests that it is desirable to have a process for which the gate oxide and the capacitor oxide are grown simultaneously. In this case, independent of their absolute values, the oxide thickness of the transistor gates and the capacitors tracks and thus, $\frac{\Delta C_{ox_{cap}}}{C_{ox_{cap}}} = \frac{\Delta C_{ox}}{C_{ox}}$ and the two correlated oxide capacitance errors would cancel each other. The term corresponding to the channel width of the input transistors could be neglected as usually $W >> \Delta W$. Thus Q_{intg} is simplified and

$$\frac{1}{Q_{intg}} \approx \frac{1}{Q_a}\left| + \frac{\Delta\theta}{\theta} - \frac{\Delta\mu}{\mu} + 2\frac{\Delta W_{cap}}{W_{cap}} + 2\frac{\Delta L_{cap}}{L_{cap}} - \frac{\Delta L}{L}\right| \tag{4.8}$$

To find a worst case value for Q_{intg}, Q_a should be estimated from equation (4.3)

$$Q_a = \frac{2\,L_{opt}}{\theta\,(V_{GS}-V_{th})_{(M1,2)}} \tag{4.9}$$

substituting for L_{opt} from (4.1)

$$Q_a = \left[\frac{30\,\mu}{\theta^2\,(V_{GS}-V_{th})_{(M1,2)}\,\omega_0} \right]^{1/3} \tag{4.10}$$

Substituting for Q_a, Q_{intg} is found to be

$$Q_{intg} \approx \frac{\left[\frac{30\,\mu}{\theta^2\,(V_{GS}-V_{th})_{(M1,2)}\,\omega_0} \right]^{1/3}}{\left[+ \frac{\Delta\theta}{\theta} - \frac{\Delta\mu}{\mu} + 2\frac{\Delta W_{cap}}{W_{cap}} + 2\frac{\Delta L_{cap}}{L_{cap}} - \frac{\Delta L}{L} \right]} \tag{4.11}$$

Both the numerator and the denominator, in the above equation, are frequency dependent. The numerator, Q_a, is proportional to $\frac{1}{\omega_0^{1/3}}$. In the denominator, L_{opt}, W_{cap} and L_{cap} are functions of frequency and decrease as frequency is increased. Thus the worst case integrator Q decreases as the frequency is increased.

To find a general idea for the value of Q_{intg}, for simplicity it is assumed that

$$W_{cap} = L_{cap} \approx 4L_{opt} \tag{4.12}$$

Using the process parameters and the corresponding tolerances from Table 4.1

$$Q_{intg} \approx \frac{32212}{f_0^{1/3}} \left[0.25 + \frac{2\times 0.5\mu}{L_{opt}} \right]^{-1} \tag{4.13}$$

Using the above equation, the calculated values for Q_{intg} for different frequencies is listed in the third row of Table 4.2.

In the next part, this results are used to find an upper limit for the quality factor of the filter.

f_0	L_{opt} [μ]	Q_{intg}	Q_{filter}
100 *KHz*	34.7	2489	50
200 *KHz*	27.5	1923.5	38.5
500 *KHz*	20.3	1356.2	27.1
1 *MHz*	16.1	1032	20.6
2 *MHz*	12.8	779.2	15.6
5 *MHz*	9.4	528.6	10.6
10 *MHz*	7.5	390	7.8
20 *MHz*	4.7	289	5.8
50 *MHz*	3.9	194.5	3.9
100 *MHz*	2.7	126	2.5

Table 4.2. Optimum Channel Length - Minimum Integrator Q - Maximum Filter Q as a Function of Frequency

4.1.3. Maximum Quality Factor of the Filter as a Function of Frequency

As mentioned earlier, the maximum achievable quality factor of the filter depends on the minimum integrator Q and the maximum allowable error in the passband of the filter.

For a resistively terminated LC filter, the fractional change in the magnitude within the passband could be expressed as [11]

$$\frac{\Delta T(\omega)}{T(\omega)} \approx \frac{1}{2} \left| \frac{1}{Q_L} + \frac{1}{Q_C} \right| \omega\tau(\omega) \tag{4.14}$$

where Q_L and Q_C are the quality factors of the filter inductor and capacitors; $\tau(\omega)$ is the filter group delay, and ω is the frequency of interest. Similarly for a filter constructed with integrators

$$\frac{\Delta T(\omega)}{T(\omega)} \approx \frac{1}{Q_{intg}} \omega\tau(\omega) \tag{4.15}$$

The group delay $\tau(\omega)$ of a sixth order bandpass filter is at its maximum at the lower and upper edges of the passband. Using the filter simulation program FILSYN [12], it can be shown that for a sixth order bandpass filter designed to have about 0.1 dB ripple in the passband

$$\frac{\omega\tau(\omega)}{Q_{filter}} = 7.16 \tag{4.16}$$

substituting in (4.15)

$$\frac{\Delta T(\omega)}{T(\omega)} \approx \frac{Q_{filter}}{Q_{intg}} \times 7.16 \tag{4.17}$$

To find an estimate for the maximum achievable Q_{filter}, as an example it is assumed that the maximum allowable passband error is about 1.2 dB. Substituting in the above equation it is found that

$$\frac{Q_{filter}}{Q_{intg}} \approx \frac{1}{48.3} \tag{4.18}$$

Thus, the integrator Q must be at least about 50 times larger than the filter quality factor. From the above results and the minimum value found for Q_{intg} (third row of Table 4.2), the maximum Q_{filter} is calculated and is tabulated in the fourth row of Table 4.2. The maximum filter Q as a function of frequency is sketched in Fig. 4.2.

The maximum quality factor for a 100 KHz filter is about 50 and the upper limit of the quality factor of a 100 MHz filter is about 2.5.

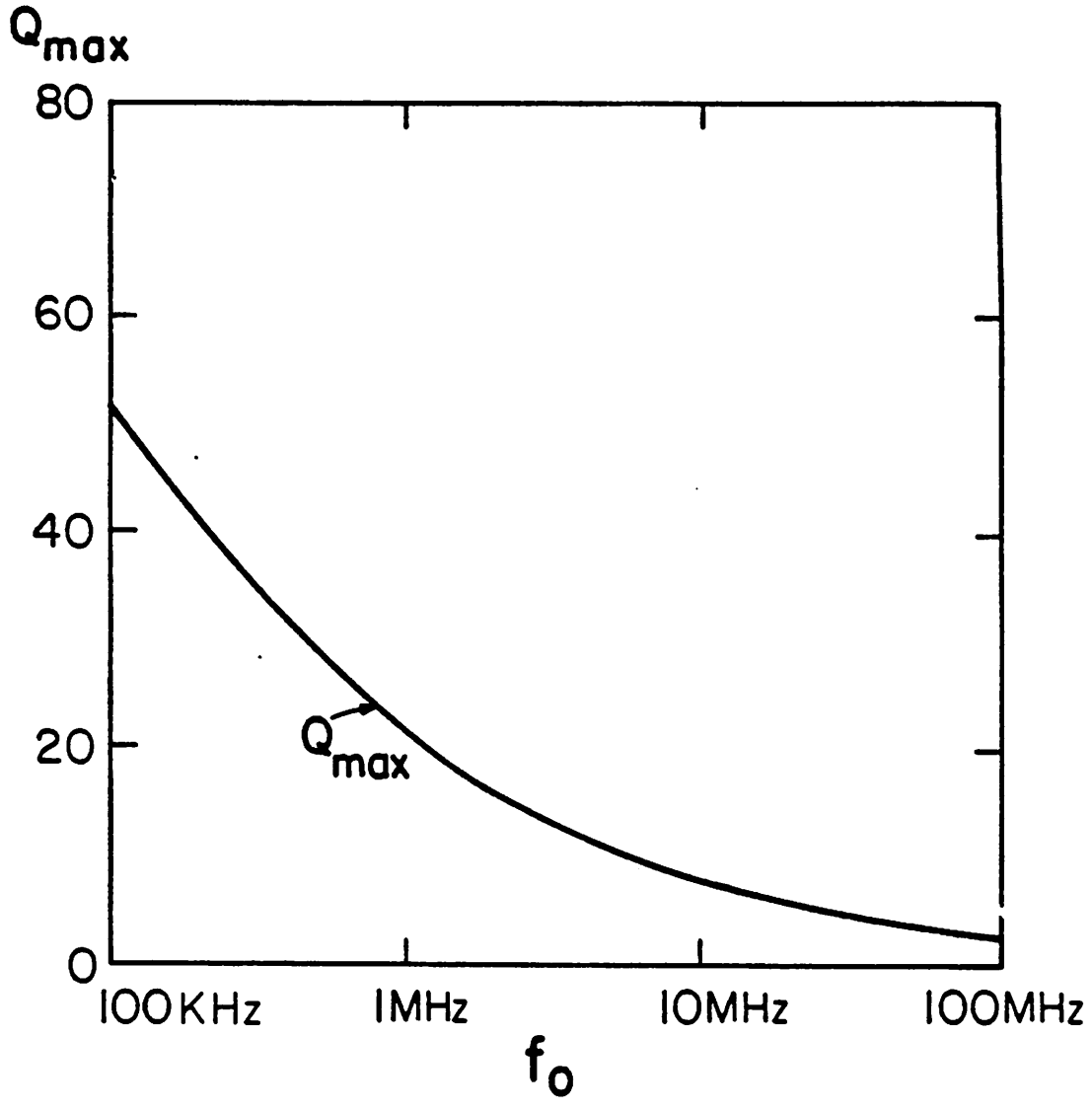


Figure 4.2

Maximum filter Q as a function of frequency.

4.2. Filter Dynamic Range Considerations

The dynamic range of the filter is defined as the ratio of the total RMS output voltage at a given distortion level to the total RMS noise voltage within the passband of the filter.

For bandpass filters, the maximum signal level is usually defined at a 1% third-order intermodulation distortion as this is the only distortion component which in most cases may fall within the passband of the filter, the other distortion components are filtered out.

The noise at the output of the filter is determined by the sum of the noise contribution from each of the integrators.

In the following section, the output signal distortion of the integrator and it's effect on the filter distortion is discussed first. Some techniques are presented to improve the dynamic range of the filter. In the next part the noise performance of the integrator is discussed and the total output noise of second and sixth order bandpass filters are found.

4.2.1. Distortion in the Integrator Output Signal

The nonlinear behavior of the integrator gives rise to two problems:

1) As the signal level is increased the transfer function becomes more nonlinear and in the presence of unwanted signals this may result in spurious signals being generated within the pass-band of the filter.

2) The fact that the input transistor transconductance decreases as the signal level is increased, results in the lowering of the unity-gain frequency of the integrator (center frequency down shift of the filter). This is especially critical for high-Q filters.

To evaluate the distortion in the output signal of the integrator, it is assumed that the nonlinearity due to the load transistors is negligible compared to the input

transistors. Fig. 4.3(b) shows the DC transfer characteristics of the integrator input source-coupled pair of Fig. 4.3(a). The differential output current is found to be

$$\Delta I_d = I_{ss} \left| \frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}} \right| \left\{ 1 - \frac{1}{4} \left| \frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}} \right|^2 \right\}^{1/2} \qquad (4.19)$$

Note that ΔI_d reaches its limit, I_{ss}, when $\Delta v_i \geq \sqrt{2}(V_{GS}-V_{th})$.

Using the series expansion of $(1-x^2)^{1/2}$, the differential output current could be transformed to

$$\Delta I_d = I_{ss} \left\{ \left| \frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}} \right| - \frac{1}{8} \left| \frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}} \right|^3 - \frac{1}{128} \left| \frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}} \right|^5 - \frac{1}{1024} \left| \frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}} \right|^7 \cdots\cdots \right\} \qquad (4.20)$$

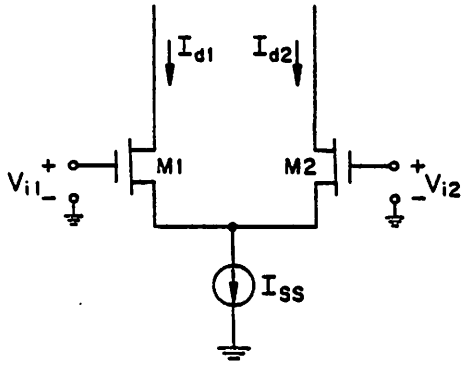
For small input signals, $\Delta v_i \ll (V_{GS}-V_{th})$, the first term is much larger than the higher order terms and the output current is a linear function of the input voltage. For input signals comparable to $(V_{GS}-V_{th})$, the higher order terms become more significant which results in nonlinear behavior in the output current.

4.2.1.1. Intermodulation Distortion

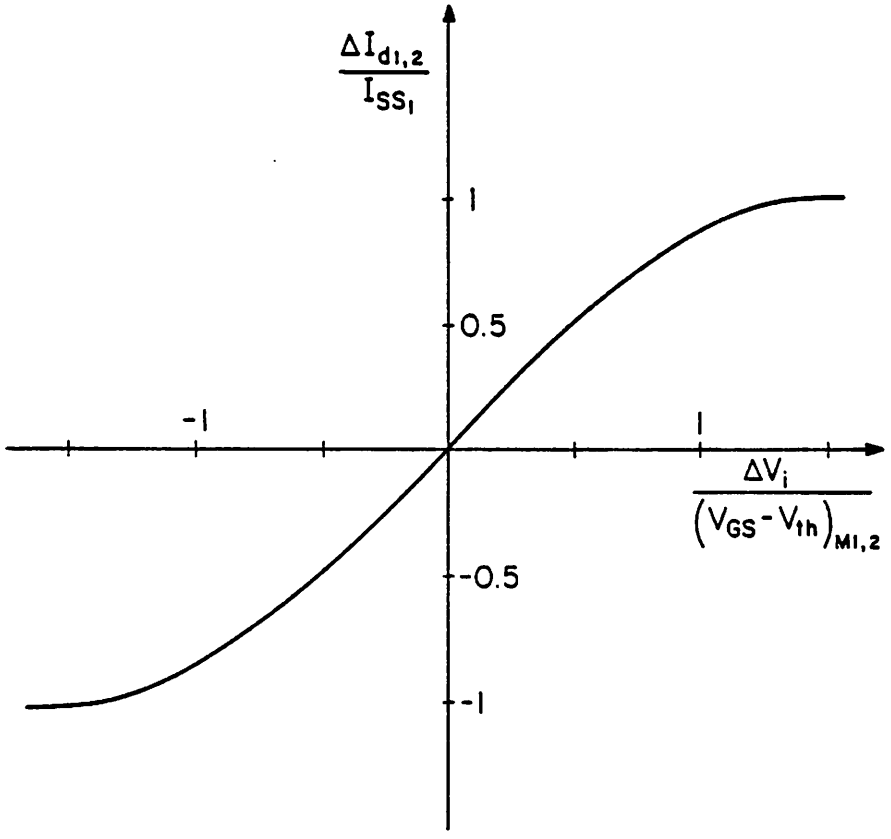
As mentioned earlier, for bandpass filters the third order intermodulation, $IM3$, component is the only distortion component which may fall within the passband of the filter. To calculate $IM3$, the coefficients in the following equation must be found [13]

$$\Delta I_d = a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + a_4 v_i^4 + a_5 v_i^5 + a_6 v_i^6 + \cdots\cdots \qquad (4.21)$$

from equation (4.20)



(a)



(b)

Figure 4.3

(a)- The source coupled pair.
(b)- The DC transfer curve of the source-coupled pair.

$$a_1 = \frac{I_{ss}}{(V_{GS} - V_{th})} \qquad a_2 = 0$$
$$a_3 = -\frac{I_{ss}}{8\,(V_{GS} - V_{th})^3} \qquad a_4 = 0 \qquad (4.22)$$
$$a_5 = -\frac{I_{ss}}{128\,(V_{GS} - V_{th})^5} \qquad a_6 = 0$$

the third order intermodulation component, $IM3$, is generated by the odd coefficients and can be shown to be equal to

$$IM3 \approx \frac{3}{4}\frac{a_3}{a_1}\hat{v}_i^2 + \frac{25}{8}\frac{a_5}{a_1}\hat{v}_i^4 + \ldots\ldots \qquad (4.23)$$

using the values found for a_1 and a_3 and a_5

$$IM3 \approx -\frac{3}{32}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^2 - \frac{25}{1024}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^4 - \ldots\ldots (4.24)$$

for small values of $IM3$, the first term is dominant and

$$\hat{v}_{i\,max} \approx 4\,(V_{GS}-V_{th})\left|\frac{2}{3}\,IM3\right|^{1/2} \qquad (4.25)$$

As expected, the maximum voltage is increased as the gate overdrive voltage $(V_{GS}-V_{th})$ is increased.

For example for $IM3 = 1\%$ and $(V_{GS}-V_{th}) = 1\ V$

$$\hat{v}_{i\,max} = 327\ mV \quad or \quad v_{i\,RMS} = 231\ mV \qquad (4.26)$$

The maximum voltage is quite low and can be increased by increasing $(V_{GS}-V_{th})$. The other factors that limit the choice of this parameter will be discussed later.

4.2.1.2. Center Frequency Shift

The center frequency shift of the filter for large input signals is a particularly critical problem for the design of high Q filters.

The unity-gain frequency of the integrator is given by

$$\omega_0 = \frac{G_m}{2C_{intg}} \tag{4.27}$$

Let's assume G_m is the large signal transconductance of the integrator and g_m is the small signal transconductance

$$G_m = \frac{d\,\Delta I_d}{d\,\Delta v_i} \tag{4.28}$$

differentiating equation (4.20)

$$G_m = \frac{I_{ss}}{(V_{GS}-V_{th})}\left\{1 - \frac{3}{8}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^2 - \frac{5}{128}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^4 - \frac{7}{1024}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^6 \cdots\cdots\right\} \tag{4.29}$$

but $\frac{I_{ss}}{(V_{GS}-V_{th})} = g_m$, thus

$$G_m = g_m\left\{1 - \frac{3}{8}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^2 - \frac{5}{128}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^4 - \frac{7}{1024}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^6 \cdots\cdots\right\} \tag{4.30}$$

or

$$\frac{\Delta G_m}{g_m} = -\frac{3}{8}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^2 - \frac{5}{128}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^4 - \frac{7}{1024}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^6 \cdots\cdots \tag{4.31}$$

For small values of $\frac{\Delta G_m}{g_m}$, the first term is dominant and

$$\hat{v}_{i\,max} \approx 2\,(V_{GS}-V_{th})\left|\frac{2}{3}\,\frac{\Delta G_m}{g_m}\right|^{1/2} \tag{4.32}$$

Comparing the above result to (4.25), it is evident that the maximum input voltage is twice as much for $IM3$ than $\frac{\Delta G_m}{g_m}$ for equal error percentage. This is verified by inspecting Fig. 4.4 which shows the normalized large signal transconductance versus normalized differential input voltage. For the above example, the input voltage which

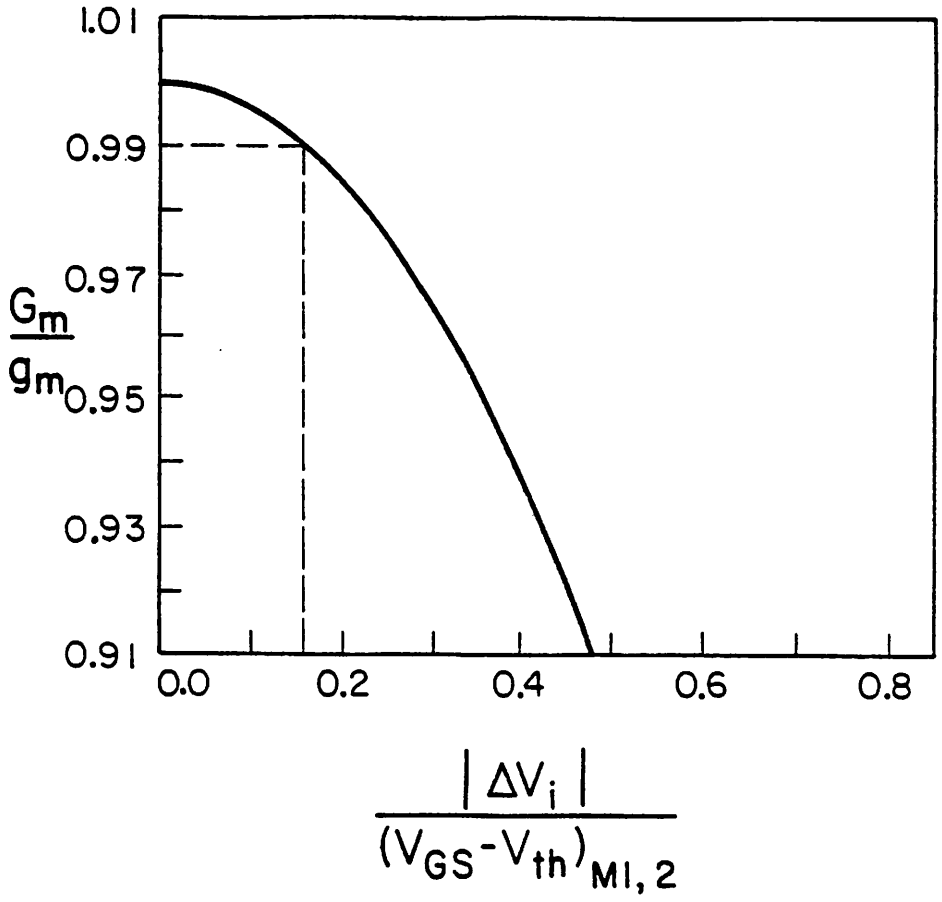


Figure 4.4

Normalized large signal transconductance of a source-coupled pair as a function of the differential input voltage.

resulted in $IM3 = 1\%$ corresponds to $\left|\frac{G_m}{g_m} = 0.96\right|$ or a 4% shift in the center frequency of the filter. For the same example, a 1% center frequency shift occurs for

$$\hat{v}_{i\,max} = 163\ mV \quad or \quad v_{i\,RMS} = 115\ mV \tag{4.33}$$

4.2.1.3. Circuit Techniques to Improve the Integrator Linearity

Both equations (4.25) and (4.32) suggest that the upper limit of the output signal could be increased by choosing large values for the input transistor gate overdrive voltage,$(V_{GS}-V_{th})_{M1,2}$. The major limiting factor in this case is the maximum available supply voltage. By inspecting equation (4.32), it is obvious that the worst case Q_{inig} and thus the maximum achievable filter quality factor, is proportional to $\frac{1}{(V_{GS}-V_{th})^{1/3}_{M1,2}}$. Therefore, achieving high Q with low passband error dictates low values for $(V_{GS}-V_{th})_{M1,2}$. The above considerations suggests that the choice of the gate overdrive voltage is based not only on maximizing the dynamic range, but also upon the maximum power supply voltage and the filter quality factor.

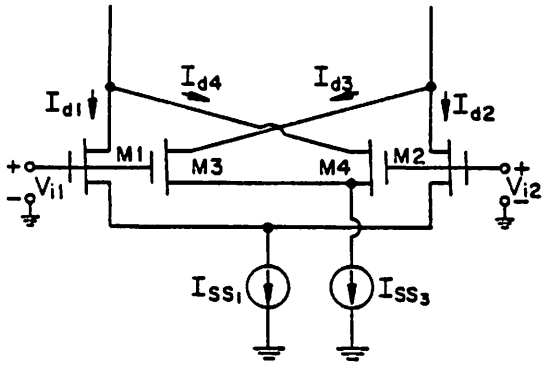
Here a simple circuit technique is proposed to linearize the output current of the integrator.

To compensate for the non-linearity of the output current, a cross-coupled source-coupled pair is added to the input of the integrator (Fig. 4.5(a)) . The function of the cross-coupled pair is to subtract a small amount of current, $\Delta I_{d_{3,4}}$, which becomes nonlinear more rapidly as compared to $\Delta I_{d_{1,2}}$ as shown in Fig. 4.5(b).

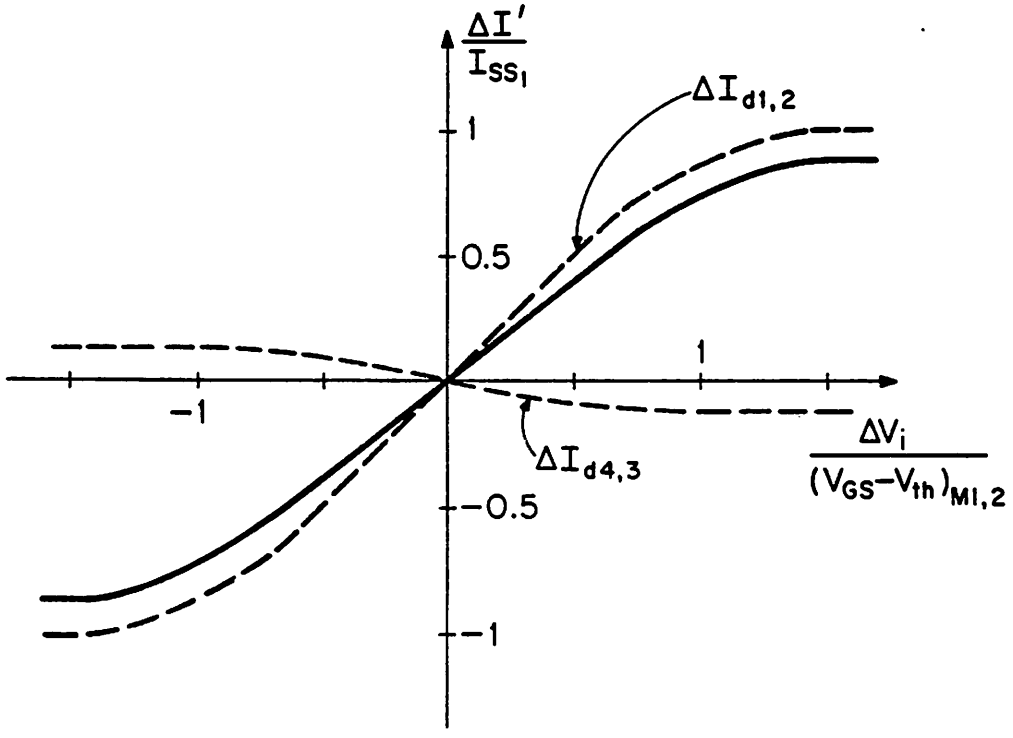
The total output current is given by

$$\Delta I' = \Delta I_{d_{1,2}} - \Delta I_{d_{3,4}} \tag{4.34}$$

where $\Delta I_{d_{1,2}}$ is given by equation (4.20) and $\Delta I_{d_{3,4}}$ is



(a)



(b)

Figure 4.5

(a)- A cross-coupled pair is added to the input stage source-coupled pair to linearize the output current.
(b)- The normalized output current.

$$\Delta I_{d_{3,4}} = I_{ss3}\left\{ \left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M3,4}}\right| - \frac{1}{8}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M3,4}}\right|^3 - \frac{1}{128}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M3,4}}\right|^5 - \frac{1}{1024}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M3,4}}\right|^7 \cdots\cdots \right\} \tag{4.35}$$

Let's assume that $\frac{I_{ss1}}{I_{ss3}} = b$ and $\frac{(V_{GS}-V_{th})_{M1,2}}{(V_{GS}-V_{th})_{M3,4}} = a$ and thus

$$\frac{(\frac{W}{L})_{M1,2}}{(\frac{W}{L})_{M3,4}} = \frac{b}{a^2} \tag{4.36}$$

It can be shown that

$$\Delta I_{d_{3,4}} = I_{ss1}\left\{ \left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|\left|\frac{a}{b}\right| - \frac{1}{8}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^3\left|\frac{a^3}{b}\right| - \frac{1}{128}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^5\left|\frac{a^5}{b}\right| \cdots\cdots \right\} \tag{4.37}$$

Substituting from the above equation and (4.20) in (4.34) the total output current is found

$$\Delta I = I_{ss1} \times\left\{ \left|1-\frac{a}{b}\right|\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right| - \frac{1}{8}\left|1-\frac{a^3}{b}\right|\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^3 - \frac{1}{128}\left|1-\frac{a^5}{b}\right|\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^5 - \frac{1}{1024}\left|1-\frac{a^7}{b}\right|\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^7 \cdots\cdots \right\} \tag{4.38}$$

The output current coefficients are given by

$$a_1 = \left|1 - \frac{a}{b}\right| \left|\frac{I_{ss1}}{(V_{GS} - V_{th})}\right| \qquad a_2 = 0$$
$$a_3 = -\left|1 - \frac{a^3}{b}\right| \left|\frac{I_{ss1}}{8\,(V_{GS} - V_{th})^3}\right| \qquad a_4 = 0 \qquad (4.39)$$
$$a_5 = -\left|1 - \frac{a^5}{b}\right| \left|\frac{I_{ss1}}{128\,(V_{GS} - V_{th})^5}\right| \qquad a_6 = 0$$

Using the derived values in (4.23)

$$IM3 \approx -\frac{3}{32}\frac{\left|1 - \frac{a^3}{b}\right|}{\left|1 - \frac{a}{b}\right|}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^2 - \frac{25}{1024}\frac{\left|1 - \frac{a^5}{b}\right|}{\left|1 - \frac{a}{b}\right|}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^4 - \cdots\cdots \qquad (4.40)$$

The interesting aspect of the above equation is that for $\frac{a^3}{b} = 1$, the first term, which is the main source of third order intermodulation, disappears.

For the new configuration the transconductance is found to be

$$G_m' = \frac{I_{ss1}}{(V_{GS}-V_{th})_{M1,2}} \times \left\{ \left|1 - \frac{a}{b}\right| - \frac{3}{8}\left|1 - \frac{a^3}{b}\right|\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^2 \right. \qquad (4.41)$$
$$\left. - \frac{5}{128}\left|1 - \frac{a^5}{b}\right|\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^4 - \frac{7}{1024}\left|1 - \frac{a^7}{b}\right|\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^6 \cdots\cdots\cdots \right\}$$

Note that the small signal transconductance, g_m', is reduced to

$$g_m' = g_{m_{M1,2}}\left|1 - \frac{a}{b}\right| \qquad (4.42)$$

This results in a lower DC gain for the integrator. It can be shown that

$$\frac{\Delta G_m}{g_m} \approx -\frac{3}{8}\frac{\left|1-\frac{a^3}{b}\right|}{\left|1-\frac{a}{b}\right|}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^2 - \frac{5}{128}\frac{\left|1-\frac{a^5}{b}\right|}{\left|1-\frac{a}{b}\right|}\left|\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}}\right|^4 - \cdots\cdots \tag{4.43}$$

To choose values for a and b, several considerations must be taken into account:

1) To keep the DC gain high $\frac{a}{b} \ll 1$

2) The range of the input voltage over which the linearity correction performed by M_3 and M_4 is effective is approximately $\sqrt{2}(V_{GS}-V_{th})_{M3,4}$ or $\frac{\sqrt{2}}{a}(V_{GS}-V_{th})_{M1,2}$. Therefore a must be kept as small as possible.

3) To reduce $IM3$ and $\frac{\Delta G_m}{g_m}$, it was concluded that $b \approx a^3$.

As an example, accounting for the above considerations, a is chosen to be equal to two. Let's first try $\left|b = a^3 = 8\right|$ for which the first term of both $\frac{\Delta G_m}{g_m}$ and $IM3$ is zero. Fig. 4.6 shows that the normalized transconductance in this case increases as the input voltage increases. The input voltage for which $\left|\frac{G_m}{g_m} = 1.01\right|$ is $\Delta v_i \approx 0.47(V_{GS}-V_{th})$ and for $(V_{GS}-V_{th}) = 1\ V$ $\Delta v_i \approx 0.47\ V$. Comparing this number to, $\Delta v_i = 0.163\ V$ found in the previous section, an improvement of 9.2 dB is predicted for the dynamic range. For this input voltage $IM3$ is found from equation (4.20). The first term is zero and the second term gives

$$IM3 \approx 0.46\ \% \tag{4.44}$$

It can be shown that for $a = 2$ and $b = 8$, the $IM3 = 1\ \%$ occurs at

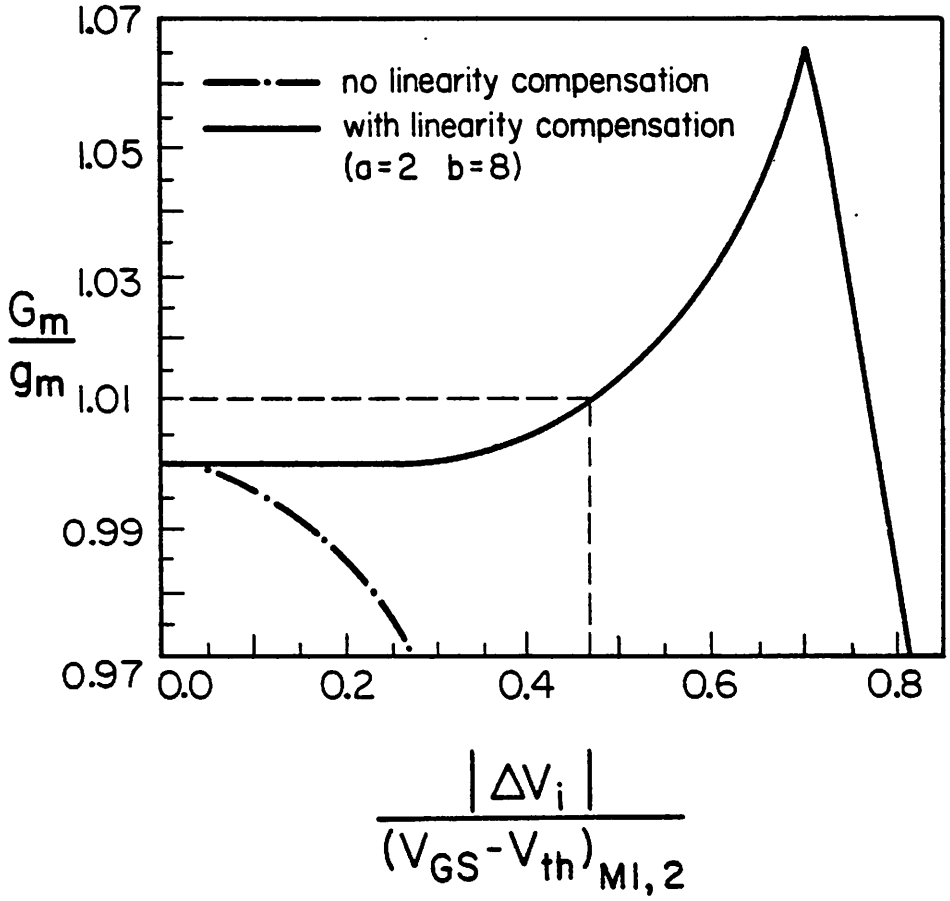


Figure 4.6

The normalized transconductance for $a = 2$, $b = 8$.

$\frac{\Delta v_i}{(V_{GS}-V_{th})_{M1,2}} \approx 0.599\ V$. Comparing this to the result of the previous section shows an improvement of $5\ dB$.

For both the $IM3$ and $\frac{\Delta G_m}{g_m}$ equations, the first and the second terms are proportional to $\left|1-\frac{a^3}{b}\right|$, and $\left|1-\frac{a^5}{b}\right|$, respectively. In the previous example a and b were chosen to set the first term coefficients to zero. By choosing a larger value for b, the two terms will be of opposite signs which helps linearize the performance of the circuit. The first term is dominant for smaller Δv_i and as the input signal is increased the second term becomes more significant.

As an example b is chosen so that G_m stays within ± 1 % of its small signal value. Fig. 4.7 demonstrates the normalized transconductance for $a = 2$ and $b = 9.5$. As Δv_i is made larger G_m decreases (the second term which has a negative sign dominates), it has a minimum of $0.99\ g_m$. At this point the third term which has a positive sign becomes significant. The two terms are equal for $\frac{\Delta v_i}{(V_{GS}-V_{th})} \approx 0.64\ V$; that is, $G_m = g_m$. For $\frac{\Delta v_i}{(V_{GS}-V_{th})} \approx 0.69\ V$ $\frac{G_m}{g_m} = 1.01\ V$. This translates to an improvement of $12.5\ dB$. For this input voltage, the third order intermodulation, $IM3$, is calculated to be about 0.76 %. Using equation (4.40), the signal level for which $IM3 = 1$ % is found to be $\frac{\Delta v_i}{(V_{GS}-V_{th})} \approx 0.72\ V$ that results in a $6.8\ dB$ increase in the dynamic range.

In this example a and b were optimized for ± 1% center frequency shift: in other words, $\frac{G_m}{g_m} = 1 \pm 0.01$, which resulted in a $12.5\ dB$ improvement in the dynamic range. The same criterion could be applied to optimize the filter performance for the required intermodulation specifications.

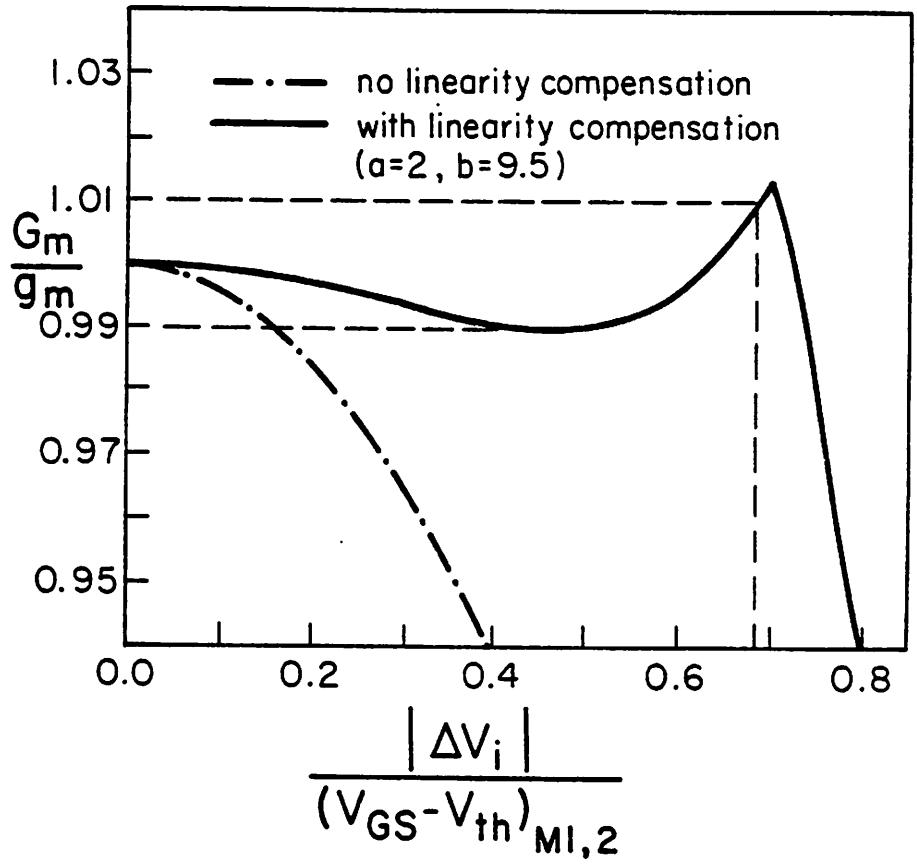


Figure 4.7

The normalized transconductance for $a = 2$, $b = 9.5$.

4.2.2. Distortion in the Filter Output Signal

As was mentioned earlier, the identical resonator filter architecture was adopted for optimum sensitivity. However, due to the fact that the maximum signal of some of the internal nodes of the filter is a factor of two higher than the output node signal [14], the maximum filter output with acceptable distortion is half the value found for the integrator in the previous section. This results in a $6\,dB$ loss in the overall dynamic range of the filter.

4.2.3. Noise Performance of the Integrator

The equivalent input noise of the integrator can be calculated to be

$$\overline{v_{eq_T}^2} = \overline{v_{eq_{M1}}^2} + \overline{v_{eq_{M2}}^2} + \left| \frac{g_{m\,M7,8}}{g_{m\,M1,2}} \right|^2 \left[\overline{v_{eq_{M7}}^2} + \overline{v_{eq_{M8}}^2} \right] \tag{4.45}$$

where $\overline{v_{eq_{M1}}^2}$, $\overline{v_{eq_{M2}}^2}$, $\overline{v_{eq_{M7}}^2}$, $\overline{v_{eq_{M8}}^2}$, are, the equivalent input voltage noise generators of the input transistors and the load transistors, respectively.

Assuming that the lower band edge of the filter is at a much higher frequency than the flicker noise "corner" frequency and therefore the contribution of this noise component is negligible; the noise of all MOS transistors are thermal and

$$\overline{v_{eq}^2} = 4kT \left| \frac{2}{3g_m} \right| \Delta f \tag{4.46}$$

substituting in equation (4.45)

$$\overline{v_{eq_T}^2} = 8kT \left| \frac{2}{3\,g_{m\,M1,2}} \right| \left| 1 + \frac{g_{m\,M7,8}}{g_{m\,M1,2}} \right| \Delta f \tag{4.47}$$

Assuming $\frac{g_{m\,M7,8}}{g_{m\,M1,2}} = \frac{1}{2}$, the input referred noise spectral density of the integrator is found to be

$$S_i(f)_{intg} = 8kT\frac{1}{g_{m\,M1,2}} \tag{4.48}$$

substituting for $g_{m\,M1,2} = 2\omega_0 C_{intg}$

$$S_i(f)_{intg} = \frac{4kT}{\omega_0 C_{intg}} \tag{4.49}$$

It can be demonstrated that the same integrator implemented with operational amplifier type fully differential integrators of Fig. 4.8 (b) would exhibit four times more output noise power for equal total integration capacitance. This is due to the bridge connection of the integrating capacitance as illustrated in Fig. 4.8 (a).

4.2.4. Noise Performance of the Filter

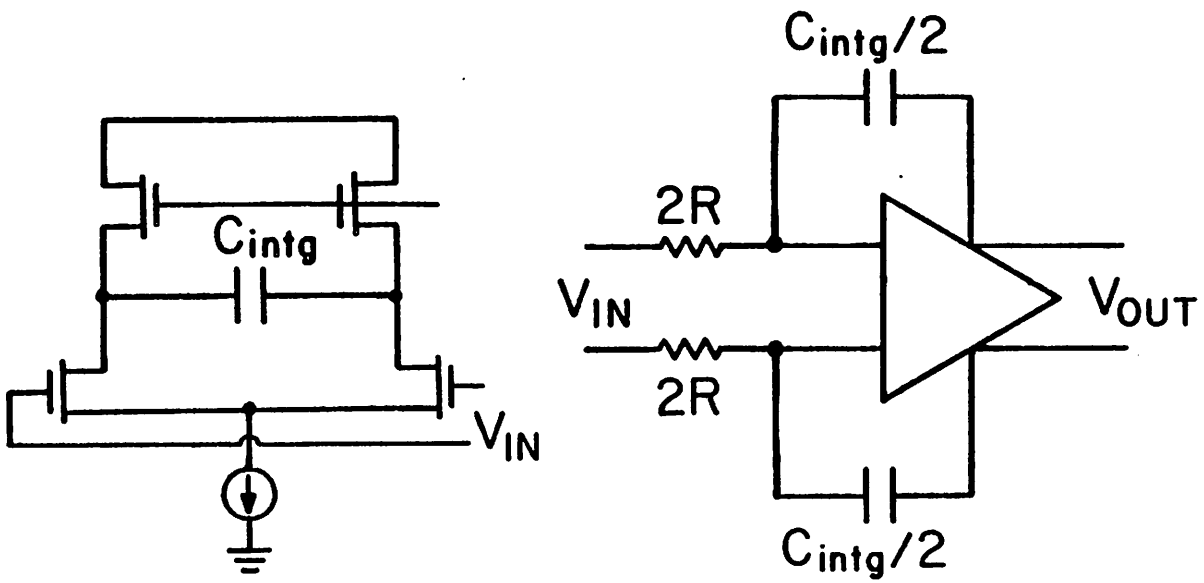
The total output noise power of a typical doubly-terminated sixth order ladder bandpass filter implemented with identical integrators is found in Appendix B to be

$$\overline{v_{out}^2} = S_i(f)_{intg} \times \frac{3\pi}{2} \times Q_{res}^{term} \times f_0 \tag{4.50}$$

where $S_i(f)_{intg}$ is assumed to be frequency independent, f_0 corresponds to the center frequency of the filter and Q_{res}^{term} is the quality factor of the terminated resonators which depending upon the desired shape of the filter frequency characteristics ranges from one to two times the overall Q of the filter. Substituting for $S_i(f)$ and f_0, the total output noise power is found to be

$$\overline{v_{out}^2} = 3\,\frac{kT}{C_{intg}}\,Q_{res}^{term} \tag{4.51}$$

Since in recursive bandpass filters the output noise power is inversely proportional to the integrating capacitor value, for the above integrator the noise can be drastically reduced by choosing higher values for the integrating capacitors and paying a price in terms of higher power consumption and die area. Whereas in switched-capacitor technique the dependence of the operational amplifier settling time on the integrating capa-



(a) (b)

Figure 4.8

(a)-The simple differential pair integrator.
(b)-An operational amplifier type fully differential integrator.

citance limits the integrating capacitance to relatively small values for high frequency filters. This in turn makes the achievement of low values of output noise easier in this technique than in switched-capacitor filters.

4.3. Effect of Transistor Mismatches

The matching of the integrator transistors is an important factor to consider because of the following reasons.

The matching of the unity-gain frequency, ω_0, of all the integrators, which directly affects the frequency response of the filter, is of particular importance. It can be shown that the unity-gain frequency mismatch is given by

$$\frac{\Delta\omega_0}{\omega_0} = \frac{\Delta G_{m_{(M1,2)}}}{G_{m_{(M1,2)}}} + \frac{\Delta C_{intg}}{C_{intg}} \tag{4.52}$$

In MOS processes the MOS capacitors can typically be matched within a few tenths of a percent, whereas the MOS transistor transconductances matching is more difficult to achieve. The mismatch of the input transistor transconductance from one integrator to another is found to be

$$\frac{\Delta G_{m_{(M1,2)}}}{G_{m_{(M1,2)}}} \approx \frac{1}{2}\left|\frac{\Delta(\frac{W}{L})}{(\frac{W}{L})}\right|_{M1,2} + \frac{1}{2}\left|\frac{\Delta(\frac{W}{L})}{(\frac{W}{L})}\right|_{M10} + \left|\frac{\Delta V_{th}}{(V_{GS}-V_{th})}\right|_{M10} \tag{4.53}$$

The first two terms are geometry dependent and independent of bias point. The third term is dependent on the threshold voltage mismatch and the gate overdrive voltage of the current sources, $M10$. One way to reduce this term is by choosing a large value for the current source gate overdrive voltage; as an example, a threshold mismatch of $\Delta V_{th} = 5\ mV$ and $(V_{GS}-V_{th})_{M10} = 1\ V$ results in 0.5% mismatch for ω_0.

The second critical factor to consider, is the power supply rejection, PSRR, of the integrator. For the circuit configuration of the designed integrator, the PSRR is strongly

dependent on the matching of the two input transistors, $M1$ and $M2$, of each individual integrator [15].

The above considerations suggest that for both the unity-gain frequency matching and PSRR improvement, the matching of the input transistors, $M1$ and $M2$, and the current sources, $M10$, are more critical than the other integrator transistors. By physically locating these devices close to each other better matching can be achieved. The matching of the current sources threshold voltage can be substantially improved by the use of common-centroid geometries [16].

4.4. Design of a 500KHz Filter

In this section, the studies performed in chapter 3 and chapter 4 are used to design a sixth-order bandpass filter for an experimental prototype. The filter is designed for a center frequency of 500 KHz and a quality factor of five.

The simplified circuit schematic of the filter is shown in Fig. 3.19. The filter is chosen to have a chebychev characteristic with about 0.1 dB ripple in the passband. The coupling coefficient and the termination quality factor are found from the corresponding tables to be [10]

$$\gamma \approx 7.6 \qquad Q_{res}^{term} \approx 8 \tag{4.54}$$

As discussed earlier, for the integrator design (Fig. 3.20), choosing a high $(V_{GS}-V_{th})_{(M1,2)}$ results in higher dynamic range but lowers the intergrator Q. Thus, considering the fact that the total power supply voltage is 10 V and there is a stack of four transistors with threshold voltages of 1 V, the $(V_{GS}-V_{th})_{(M1,2)}$ was chosen to be 1 V. Table 4.2 is used to extract the optimum input channel length for $f_0 = 500\ KHz$.

$$L_{opt} = 20\ \mu \tag{4.55}$$

In section (4.2) it was shown that the output noise power of the filter is inversely pro-

portional to C_{intg}. Thus, it is desirable to choose a high value for the integrating capacitor. The center frequency is

$$f_0 = \frac{\left[\frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{th})\right]_{(M1,2)}}{2\pi C_{intg}} \tag{4.56}$$

which suggest that for a given center frequency, a high value for C_{intg} requires choosing a high value for W which both tend to increase the die area and power consumption. Hence, considering the tradeoff between the die area, power consumption and the filter noise, it was decided to choose

$$C_{intg} = 38\ pF$$

using the above equation the input transistor channel width is found to be

$$W_{M1,2} = 80\ \mu$$

The drain current for M 1,2 is calculated to be

$$I_{d_{M1,2}} = 120\ \mu A$$

or

$$I_{d_{M10}} = 240\ \mu A$$

As discussed in section (4.3), for the matching of the unity-gain frequency of the integrators, $(V_{GS}-V_{th})_{(M10)}$ should be chosen to have a high value. Considering the total supply voltage, it was chosen to be about 1 V which results in

$$\left[\frac{W}{L}\right]_{M10} = 8$$

thus, for $L_{M10} = 10\ \mu$ the channel width is $W_{M10} = 80\ \mu$.

For the termination implementation, in section (3.5) it was shown that to achieve an accurate Q, the channel lengths of $M_{1,2}$ and $M_{3,4}$ as well as M_{10} and M_{11} should be chosen to be equal, and thus

$$Q_{res}^{term} = \frac{W_{M1,2}}{W_{M3,4}} = \frac{W_{M10}}{W_{M11}}$$

which for $Q_{res} = 8$ results in $W_{M3,4} = 10\ \mu$ and $W_{M11} = 10\ \mu$

Integrator			
Transistor No.	W [μ]	L [μ]	I_d [μA]
M1,2	80	20	120
M3,4	10	20	15
M5,6	20	7.5	120
M7,8	80	40	120
M10	80	10	240
M11	10	10	30
MB8	20	7.5	120
MB9	80	40	120
MB10	80	20	120
MB11	40	10	120

Table 4.3. Integrator Device Sizes and Currents

In Table 4.3 the device sizes as well as the currents for the integrator and the biasing circuit shown in Fig. 3.20 is listed. The total integrating capacitor was chosen to be $C_{intg_{total}} = 38\ pF$. The parasitic capacitances should be calculated and subtracted from this value to obtain a value for C_{intg}. Note that for a fully balanced integrator, C_{intg} should be connected to the two output nodes in such a way that the two nodes get an equal share of the capacitor bottom plate parasitic capacitance.

The last parameter to decide is a value for the coupling capacitor C_k (Fig. 3.19). Since $\gamma \approx 7.6$ and

$$\gamma = \frac{2C_{intg}}{C_k}$$

substituting for γ and C_{intg} results in

$$C_k = 10pF$$

For the layout, special attention should be paid to the problem of equalizing the effect of the coupling capacitor parasitic capacitance on all nodes.

CHAPTER 5

CENTER FREQUENCY CONTROL CIRCUIT

As was mentioned earlier, the center frequency of continuous-time filters is dependent on the absolute values of monolithic components. For the filter described in chapter 3, these components are capacitors and transistors transconductances which are both temperature and process dependent. Thus, the center frequency must be either tuned externally or some extra circuitry should be added to eliminate the necessity of the external tuning. To overcome this problem a modified version of the phase-locked loop scheme, introduced by Gray and Tan in 1977, is proposed and described in this chapter.

5.1. The Modified Phase-Locked Loop Concept

Figure 5.1 shows the block diagram of the filter and the center frequency control circuit. The center frequency can either be controlled through an external voltage source or an on-chip phase-locked loop locks the center frequency to an external reference frequency. The phase-locked loop differs from the conventional PLL as it utilizes an exact replica of the main filter's second order section (voltage controlled filter, VCF) instead of the conventional voltage controlled oscillator, or VCO. The reason for this modification is that the realization of a CMOS VCO with stable center frequency at *KHz* and *MHz* range is quite complicated. It will be proven that the maximum error due to this is negligible.

The phase detector compares the phase difference ϕ between the input and output of the filter and generates an error voltage proportional to the phase difference. The error voltage is then amplified and used to change the center frequency of the filter in a direction which reduces the difference between the two frequencies.

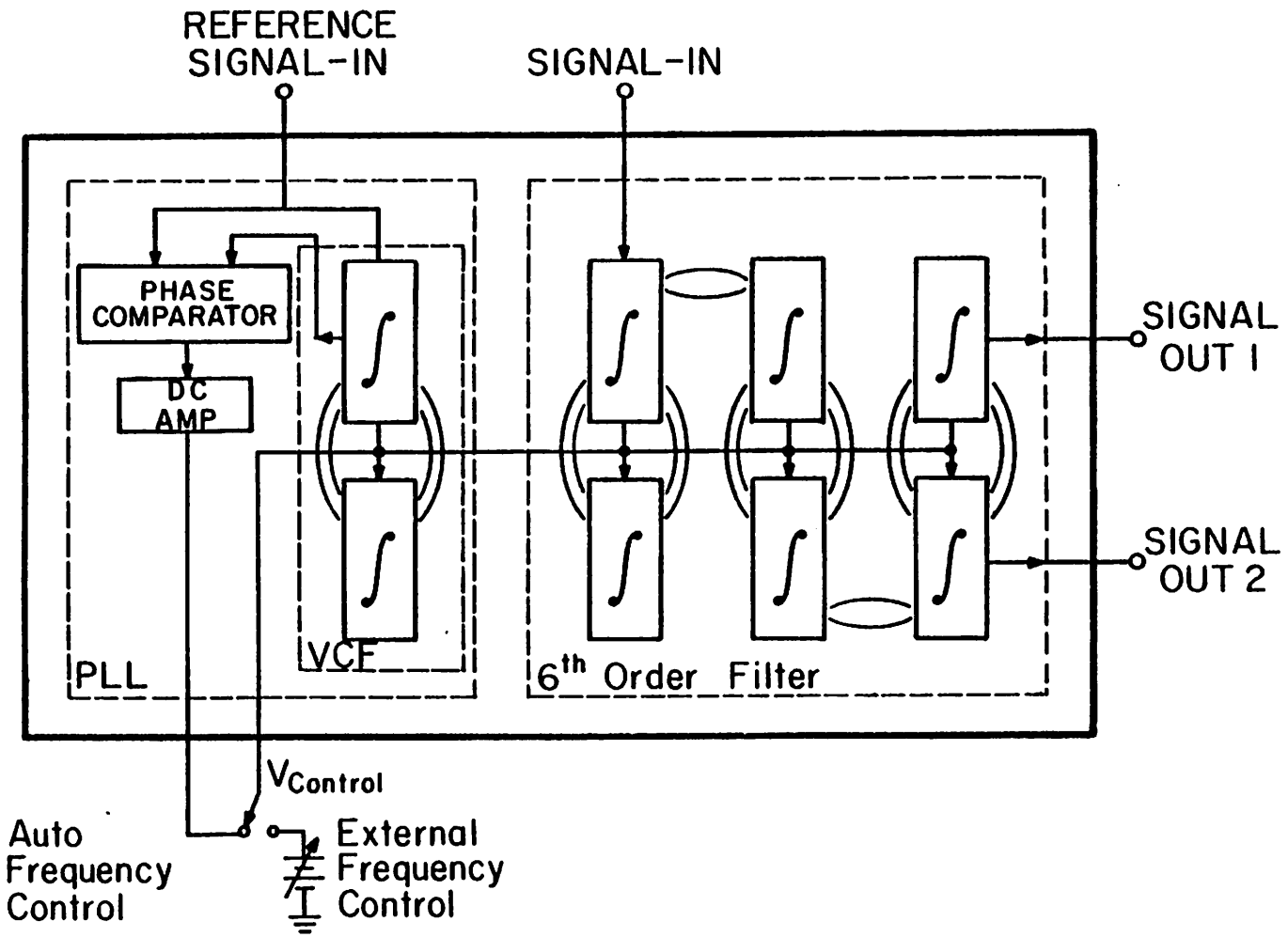


Figure 5.1

Block diagram of the filter and the center frequency control circuit.

5.2. The Phase-Locked Loop in the Locked Condition

The PLL circuit can be treated as a linear feedback system while in lock (Fig. 5.2). The closed loop transfer function is [17]

$$\frac{V_{out}}{\omega_i} = \frac{1}{K_o} \frac{K_v F(s)}{s + K_v F(s)} \tag{5.1}$$

where ω_i is the reference signal angular frequency and

$$K_v = K_D K_o A$$

where

K_D is the phase detector gain factor and is measured in units of V / rad

K_o is the VCF conversion factor in $radians / sec\ per\ volt$

A is the DC gain of the amplifier

$F(s)$ is the low-pass loop filter transfer function

K_v is called the loop bandwidth and has the dimension of $(sec)^{-1}$

5.2.1. Effect of the Loop Filter on the PLL Behavior

To understand the significance of the loop filter in the behavior of the phase-locked loop, let's first consider the case in which the loop filter is removed ($F(s)=1$). The transfer function is of the first-order type

$$\frac{V_{out}}{\omega_i} = \frac{1}{K_o} \frac{K_v}{s + K_v} \tag{5.2}$$

Fig. 5.3(a) shows the open-loop response of the PLL with no loop filter. The loop bandwidth in this case is equal to K_v. As it will be shown later, in order to keep the error between the reference frequency and the locked center frequency low, a high DC loop gain $\left| A_{PLL} = \frac{K_v}{\omega_0} \right|$ is desirable. This results in a wide loop bandwidth which gives rise to the following problem. Since the phase detector is a multiplier, it produces a sum frequency component as well as the difference frequency component. This

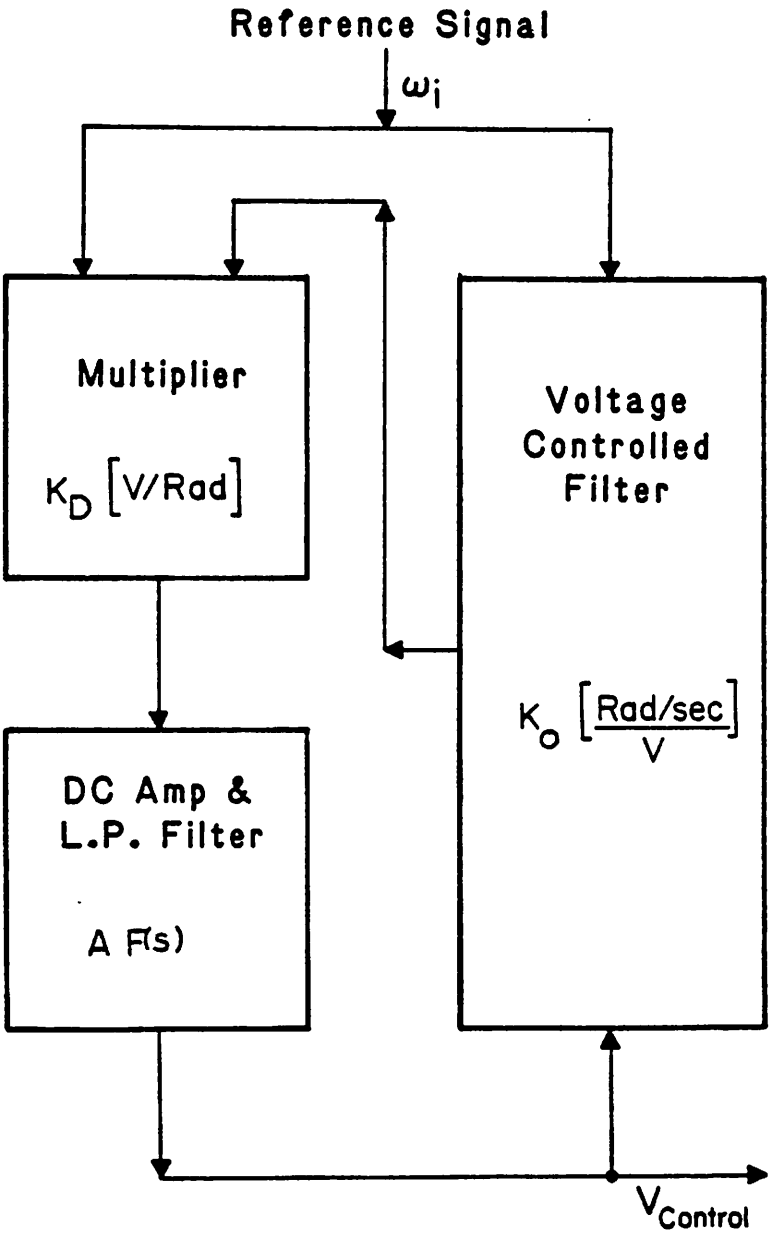


Figure 5.2

Block diagram of PLL system.

unwanted component which is at twice the reference frequency plus all interfering signals present at the input will appear at the output. Thus, a low-pass loop filter is required to filter out these unwanted signals.

One filter configuration which lowers the bandwidth of the loop while maintaining enough phase-margin to ensure stability is [18]

$$F(s) = \frac{1 + \frac{s}{\omega_2}}{1 + \frac{s}{\omega_1}} \tag{5.3}$$

where ω_1 corresponds to a pole at a frequency much less than K_v and results in an additional 90 degree phase shift as shown in Fig. 5.3(b). To increase the phase margin, a left half-plane zero, ω_2, is added in the loop filter at a frequency close to the cross over frequency.

By using the loop filter, the loop bandwidth and the *DC* loop gain can be set independently.

5.2.2. Error Between the Locked Frequency and the Reference Frequency

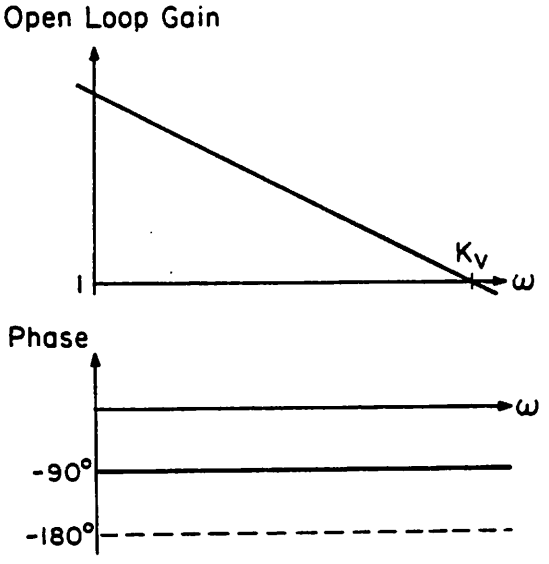
The major drawback to the modified PLL, which utilizes a voltage controlled filter instead of the conventional voltage controlled oscillator, is that there exists an error between the locked center frequency, f_0^{locked}, and the reference frequency, f_{ref}, which tends to increase as the difference between the unlocked center frequency, $f_0^{unlocked}$, and the reference signal is increased. It can be shown that

$$f_0^{locked} = f_{ref} + \frac{f_0^{unlocked} - f_{ref}}{A_{PLL}} \tag{5.4}$$

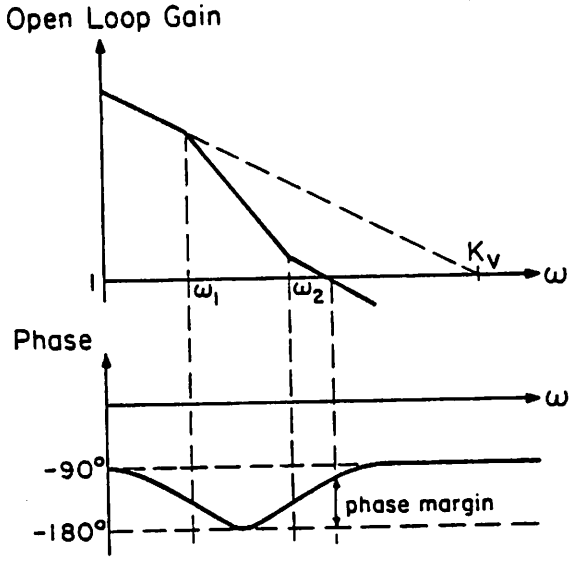
For a conventional phase-locked loop, the following equation is always true while in lock

$$f_0^{locked} = f_{ref} \tag{5.5}$$

whereas for the modified PLL the above equation is true only when $f_0^{unlocked} = f_{ref}$.



(a)



(b)

Figure 5.3

a) PLL open-loop response with no loop filter.
b) PLL open-loop response with a lag-lead type loop filter.

By choosing high values for A_{PLL}, the error can be kept within acceptable limits: as an example for a capture range of ±15% and loop gain of 300, the maximum error is only 0.05% of the center frequency which in most cases is tolerable.

5.3. The Phased-Locked Loop Building Blocks

In this section the design of the building blocks of the PLL on the circuit level is discussed.

5.3.1. Phase Comparator Design

The phase comparator configuration is chosen to be a CMOS version of the Gilbert four-quadrant multiplier circuit as shown is Fig. 5.4 [20]. The bias circuit for all PLL circuits is demonstrated in Fig. 5.5.

The small signal differential output current of this circuit is found to be [19]

$$\Delta I_o = \mu C_{ox} \left[\frac{1}{2}\left(\frac{W}{L}\right)_{MP1,2}\left(\frac{W}{L}\right)_{MP3,4,5,6}\right]^{1/2} V_{in\,1} V_{in\,2} \tag{5.6}$$

The differential output voltage of the multiplier is given by

$$\Delta V_o = \Delta I_o r_o \tag{5.7}$$

To find the phase detector gain, K_D, let's assume

$$V_{in\,1}(t) = V_{pk_1} \sin\omega t \tag{5.8}$$

and

$$V_{in\,2}(t) = V_{pk_2} \sin(\omega t + \phi) \tag{5.9}$$

substituting for $V_{in\,1}$ and $V_{in\,2}$ in (5.6)

$$\Delta V_o = \mu C_{ox} \left[\frac{1}{2}\left(\frac{W}{L}\right)_{MP1,2}\left(\frac{W}{L}\right)_{MP3,4,5,6}\right]^{1/2} r_o\, V_{pk_1} \sin\omega t\; V_{pk_2} \sin(\omega t + \phi) \tag{5.10}$$

or

$$\Delta V_o = \frac{\mu C_{ox}}{2} \left[\frac{1}{2}\left(\frac{W}{L}\right)_{MP1,2}\left(\frac{W}{L}\right)_{MP3,4,5,6}\right]^{1/2} r_o V_{pk_1} V_{pk_2} \left[\cos\phi + \cos(2\omega t + \phi)\right] \tag{5.11}$$

As the above equation suggests, the output voltage consists of a DC component which

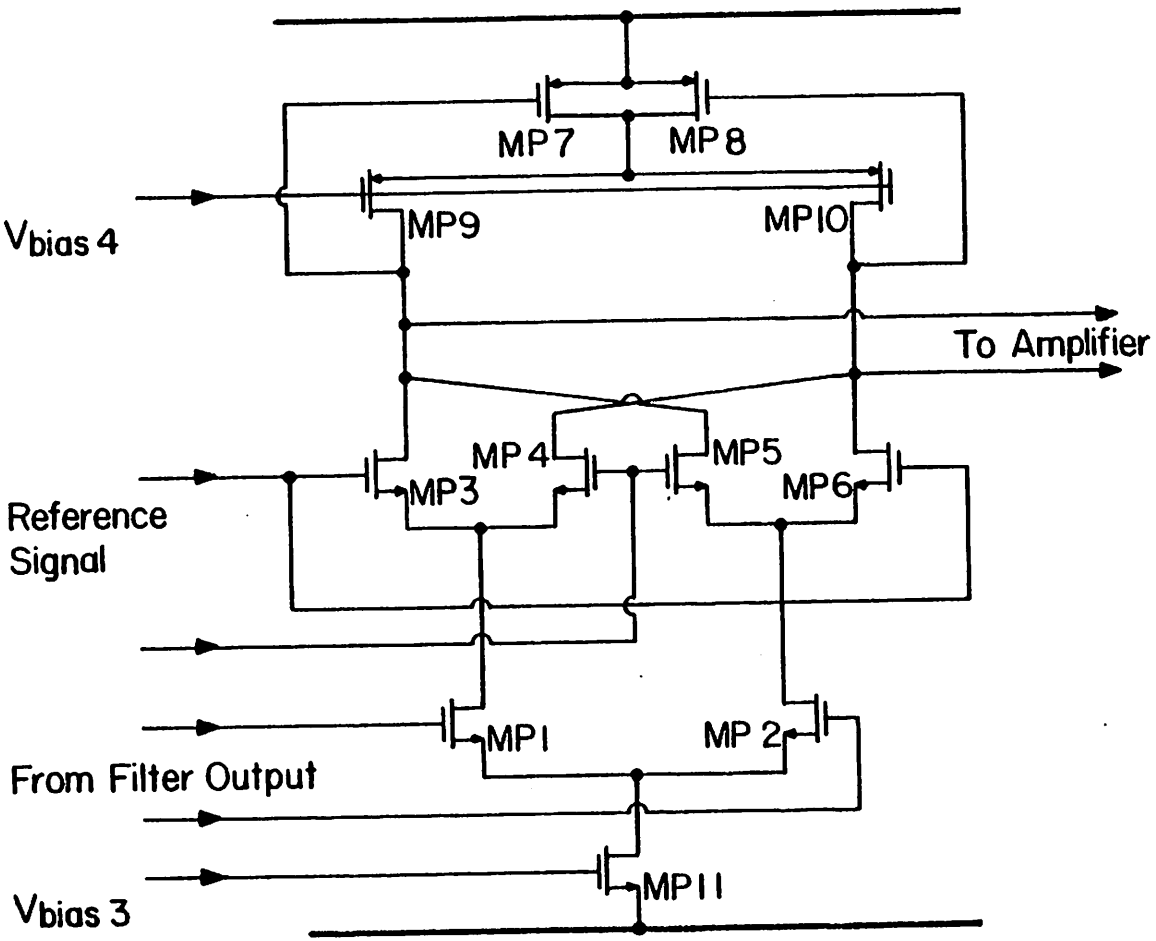


Figure 5.5

Bias circuit for all PLL circuits.

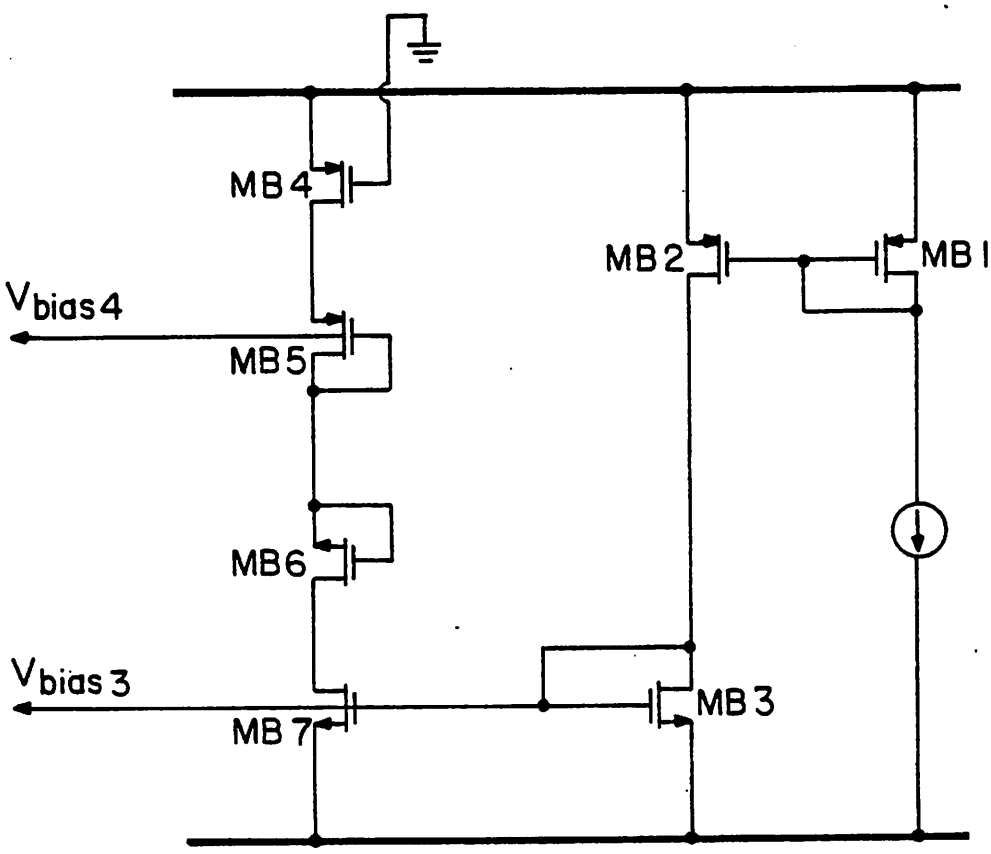


Figure 5.5

Bias circuit for all PLL circuits.

is a function of the phase difference between the two signals and an AC component at twice the original frequency. The AC component is filtered out by the loop low-pass filter and the average output voltage $\Delta V_{o_{average}}$ is given by

$$\Delta V_{o_{average}} = \frac{\mu C_{ox}}{2} \left[\frac{1}{2} \left(\frac{W}{L}\right)_{MP1,2} \left(\frac{W}{L}\right)_{MP3,4,5,6} \right]^{1/2} r_o V_{pk_1} V_{pk_2} \cos\phi \qquad (5.12)$$

Note that ΔV_o is at it's maximum for $\phi = 0$ and $\phi = \pi$ and $\Delta V_o = 0$ for $\phi = \frac{\pi}{2}$. But

$$\cos\phi = \sin\left(\frac{\pi}{2} - \phi\right) \qquad (5.13)$$

and for ϕ close to $\frac{\pi}{2}$

$$\cos\phi \approx \left(\frac{\pi}{2} - \phi\right) \qquad (5.14)$$

Substituting (5.14) in (5.12)

$$\Delta V_{o_{average}} \approx \frac{\mu C_{ox}}{2} \left[\frac{1}{2} \left(\frac{W}{L}\right)_{MP1,2} \left(\frac{W}{L}\right)_{MP3,4,5,6} \right]^{1/2} r_o V_{pk_1} V_{pk_2} \left(\frac{\pi}{2} - \phi\right) \qquad (5.15)$$

To find K_D

$$K_D = \frac{d\,\Delta V_o}{d\,\phi} \qquad (5.16)$$

differentiating (5.15) gives

$$K_D \approx \frac{\mu C_{ox}}{\pi} \left[\frac{1}{2} \left(\frac{W}{L}\right)_{MP1,2} \left(\frac{W}{L}\right)_{MP3,4,5,6} \right]^{1/2} r_o V_{pk_1} V_{pk_2} \qquad (5.17)$$

where r_o is given by

$$r_o = \left| \frac{2}{\frac{\theta_n}{L_{MP3}} + \frac{\theta_p}{L_{MP9}}} \right| \frac{1}{I_{MP11}} \qquad (5.18)$$

5.3.2. Voltage Controlled Filter

The VCF is chosen to be the exact replica of the main filter's second order section for matching purposes. Fig. 5.6 shows the flow-graph of the filter. The transfer functions of the two outputs are given by

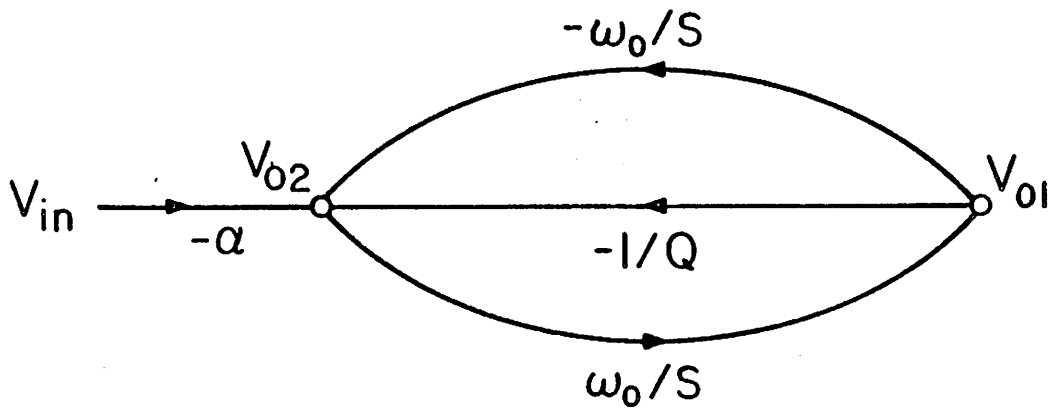


Figure 5.6

Flow-graph of a second order filter.

$$\frac{v_{o_1}}{v_{in}} = \frac{-\frac{s}{\omega_0}\alpha}{\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1} \tag{5.19}$$

$$\frac{v_{o_2}}{v_{in}} = \frac{-\frac{s^2}{\omega_0^2}\alpha}{\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1} \tag{5.20}$$

The bandpass output, v_{o_1}, has a 180 degree phase shift at the center frequency ($s = j\omega$) with respect to the input signal. The second output, v_{o_2}, has a high-pass characteristic with a peaking at the center frequency and a -90 degree phase shift at this frequency. Considering the phase-detector characteristics, v_{o_2} seems to have the desirable phase response to generate the error voltage. Fig. 5.7(a) shows the amplitude and phase response of v_{o_2}. To verify that choosing v_{o_2} as the input to the phase detector does indeed produce a suitable error voltage for center frequency control, the *DC* component generated by the multiplication of v_{in} and v_{o_2} which turns out to be equal to

$$v_{pk_m} v_{pk_{o_2}} \cos\phi \tag{5.21}$$

is shown in Fig. 5.7(b) . The error voltage is zero for $f = f_0$ and is at its maximum for $f = f_0(1 \pm \frac{1}{2Q})$. Note that this corresponds to the error voltage when the loop is broken. Once the loop is closed, this voltage changes the center frequency of the filter and reduces the difference between the two frequencies.

In this part the VCF gain, K_o, which is defined as the variation of the center frequency in response to the output voltage of the DC amplifier, is found. Fig. 5.8 shows the circuit diagram of the VCF and the voltage to current converter. Note that K_o also includes the contribution of the voltage to current converter

$$K_o = \frac{d\omega}{dv_i} \tag{5.22}$$

Since

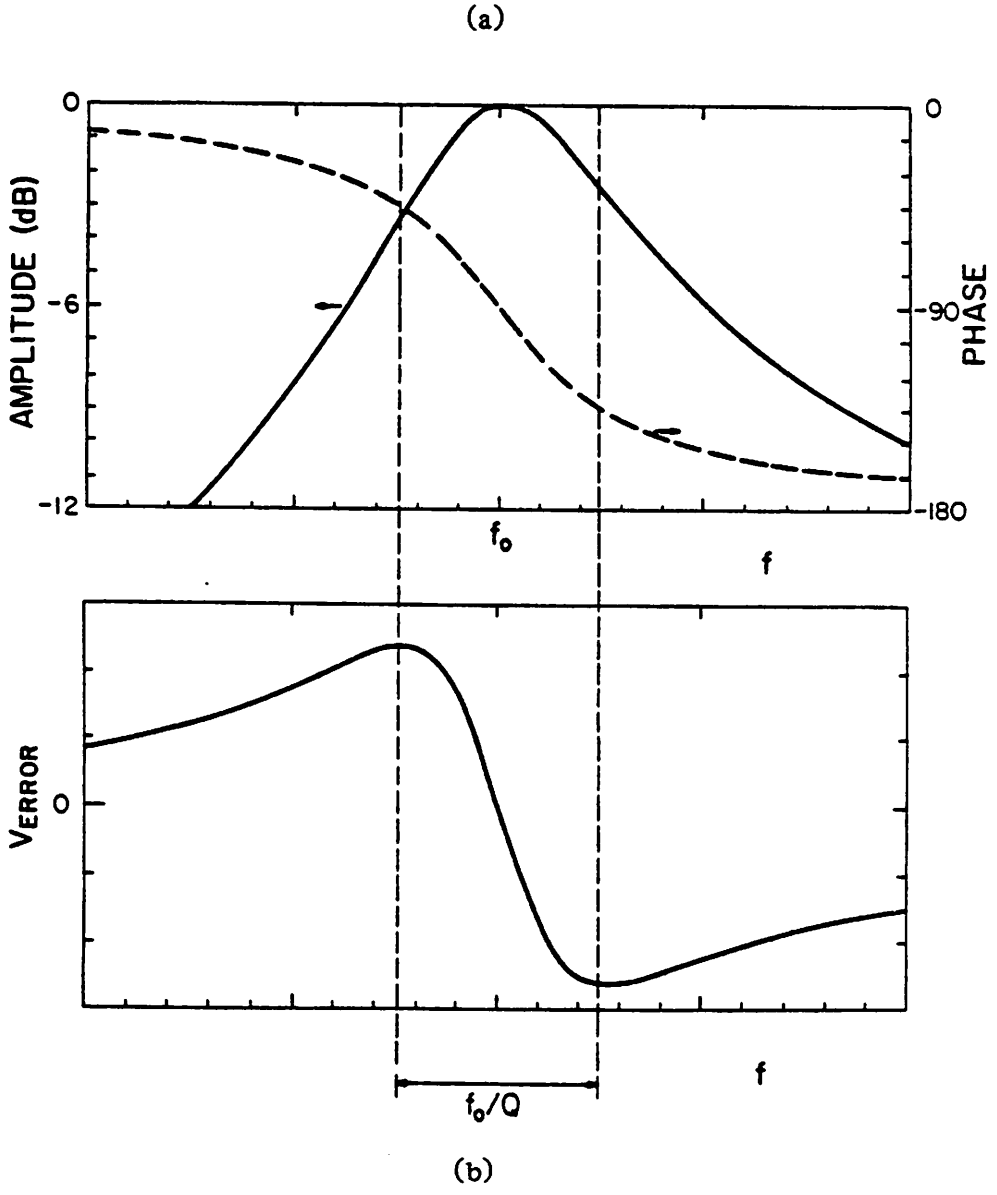


Figure 5.7

(a)- Amplitude and phase response of the filter output.
(b)- Open loop error voltage.

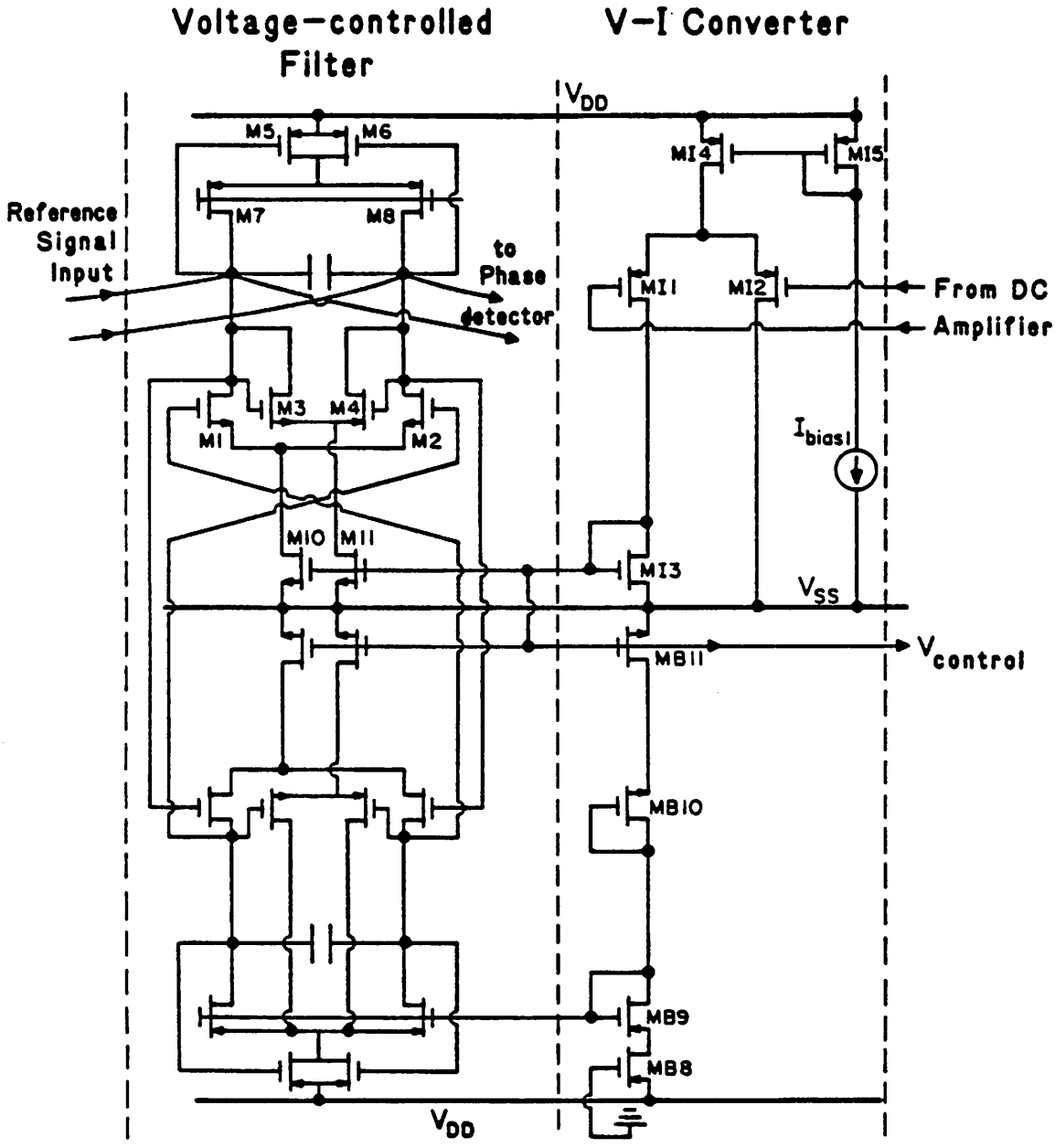


Figure 5.8

Circuit diagram of the VCF and the voltage to current converter.

$$\omega = \frac{d\phi}{dt} \tag{5.23}$$

then

$$\omega(s) = s\phi(s) \tag{5.24}$$

and

$$K_o = s\frac{d\phi}{dv_i} \tag{5.25}$$

To find the phase variation in response to the control voltage, equation (5.20) is transformed to

$$\frac{v_{o_2}}{v_{in}} = \frac{\alpha}{1 - \frac{\omega_0^2}{\omega^2} - j\frac{\omega_0}{\omega Q}} \tag{5.26}$$

and thus

$$\phi = \tan^{-1} \frac{\frac{\omega_0}{\omega Q}}{1 - \frac{\omega_0^2}{\omega^2}} = \tan^{-1} \frac{1}{Q\left|\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right|} \tag{5.27}$$

but

$$\left|\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right| = \frac{(\omega-\omega_0)(\omega+\omega_0)}{\omega\omega_0} \tag{5.28}$$

for ω close to ω_0

$$\left|\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right| \approx 2\frac{\Delta\omega}{\omega_0} \tag{5.29}$$

thus

$$\phi \approx \tan^{-1} \frac{1}{2Q}\frac{\omega_0}{\Delta\omega} \tag{5.30}$$

The series expansion of $\tan^{-1}x$ is

$$\tan^{-1} x = \frac{\pi}{2} - \frac{1}{x} + \frac{1}{3x^3} - \ldots . \tag{5.31}$$

for $x \ll 1$

$$\tan^{-1} x \approx \frac{\pi}{2} - \frac{1}{x} \tag{5.32}$$

that is for $\Delta\omega \ll \frac{2\omega_0}{Q}$

$$\phi \approx \frac{\pi}{2} - 2Q \frac{\Delta\omega}{\omega_0} \tag{5.33}$$

To derive K_o as a function of the control voltage. we need to find $\frac{\Delta\omega}{\omega_0}$ in terms of $v_{control}$. The center frequency of the filter is given by

$$\omega_0 = \frac{G_{m_{M1,2}}}{2C_{intg}} \tag{5.34}$$

where

$$G_{m_{M1,2}} = 2\left[\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{M1,2}\frac{I_{M10}}{2}\right]^{1/2} \tag{5.35}$$

but

$$I_{M10} = I_{MI3}\frac{\left(\frac{W}{L}\right)_{M10}}{\left(\frac{W}{L}\right)_{MI3}} \tag{5.36}$$

and

$$I_{MI3} = \frac{I_{MI4}}{2} - \frac{1}{2}\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}\Delta v_i\left[\frac{2I_{MI4}}{\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}} - \Delta v_i^{\,2}\right]^{1/2} \tag{5.37}$$

for $\Delta v_i \ll \left[\frac{2I_{MI4}}{\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}}\right]^{1/2}$ then

$$I_{MI3} = \frac{I_{MI4}}{2} - \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}\frac{\Delta v_i}{2}\left[\frac{2I_{MI4}}{\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}}\right]^{1/2} \tag{5.38}$$

substituting (5.38) and (5.36) in (5.35)

$$G_{m_{M1,2}} = \tag{5.39}$$

$$2\left\{\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{M1,2}\frac{\left(\frac{W}{L}\right)_{M10}}{\left(\frac{W}{L}\right)_{MI3}}\left|\frac{I_{MI4}}{2}-\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}\frac{\Delta v_i}{2}\left|\frac{2I_{MI4}}{\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}}\right|^{1/2}\right|\right\}^{1/2}$$

For $\Delta v_i = 0$, the filter center frequency is at its initial, unlocked value ($\omega_0 = \omega_{0_{initial}}$). Considering this and equation (5.34) and (5.39) , it can be found that

$$\omega_0 = \omega_{0_{initial}}\left\{1 - 2\Delta v_i\left|\frac{\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}}{2I_{MI4}}\right|^{1/2}\right\}^{1/2} \tag{5.40}$$

for small Δv_i

$$\omega_0 \approx \omega_{0_{initial}}\left\{1 - \Delta v_i\left|\frac{\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}}{2I_{MI4}}\right|^{1/2}\right\} \tag{5.41}$$

or

$$\frac{\omega_0}{\omega_{0_{initial}}} \approx 1 - \Delta v_i\left|\frac{\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}}{2I_{MI4}}\right|^{1/2} \tag{5.42}$$

by manipulating the above equation and setting $\left|\omega_0 - \omega_{0_{initial}} = \Delta\omega\right|$

$$\frac{\Delta\omega}{\omega_{0_{initial}}} \approx \Delta v_i\left|2\frac{\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}}{2I_{MI4}}\right|^{1/2} \tag{5.43}$$

Substituting the above equation in equation (5.33) gives

$$\phi \approx \frac{\pi}{2} - 2Q\,\Delta v_i\left|\frac{\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}}{2I_{MI4}}\right|^{1/2} \tag{5.44}$$

The VCF gain is found from differentiating the above equation and substituting in equation (5.25) then

$$K_o = 2Q\ \omega \left[\frac{\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MI1}}{2I_{MI4}} \right]^{1/2} \tag{5.45}$$

Note that the VCF gain is directly proportional to the filter quality factor. The term in the brackets is equal to $\frac{1}{2(V_{GS}-V_{th})_{MI1}}$. This suggests that to achieve a high gain, a low gate overdrive voltage for $MI1$ is required.

5.3.3. DC Amplifier Design

The DC amplifier is chosen to have a simple one stage configuration. Fig. 5.9 shows that the phase detector output is directly connected to the P-channel input transistors and the same signals are level shifted and applied to the N-channel input transistors, in order to have all four transistors operate in the saturation region. The common mode output voltage is stabilized by $MA5$ and $MA6$ which operate in the triode region.

The gain of the amplifier is given by

$$A = \frac{g_{m(MA1,2)} + g_{m(MA3,4)}}{g_{o(MA1,2)} + g_{o(MA3,4)}} \tag{5.46}$$

Substituting for $g_{m(MA1,2)}$, $g_{m(MA3,4)}$, $g_{o(MA1,2)}$, $g_{o(MA3,4)}$

$$A = \frac{2}{\lambda_{MA1,2} + \lambda_{MA3,4}} \frac{\left[\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{MA1,2}\right]^{1/2} + \left[\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{MA3,4}\right]^{1/2}}{\left[\frac{I_{MA7}}{2}\right]^{1/2}} \tag{5.47}$$

or

$$A = \frac{2}{\frac{\theta_n}{L_{MA1,2}} + \frac{\theta_p}{L_{MA3,4}}} \left[\frac{1}{(V_{GS}-V_{th})_{(MA1,2)}} + \frac{1}{(V_{GS}-V_{th})_{(MA3,4)}} \right] \tag{5.48}$$

From the above equation it is evident that to achieve a large gain, the transistors MA 1,2 and MA 3,4 should be chosen to have long channel lengths while the gate over-

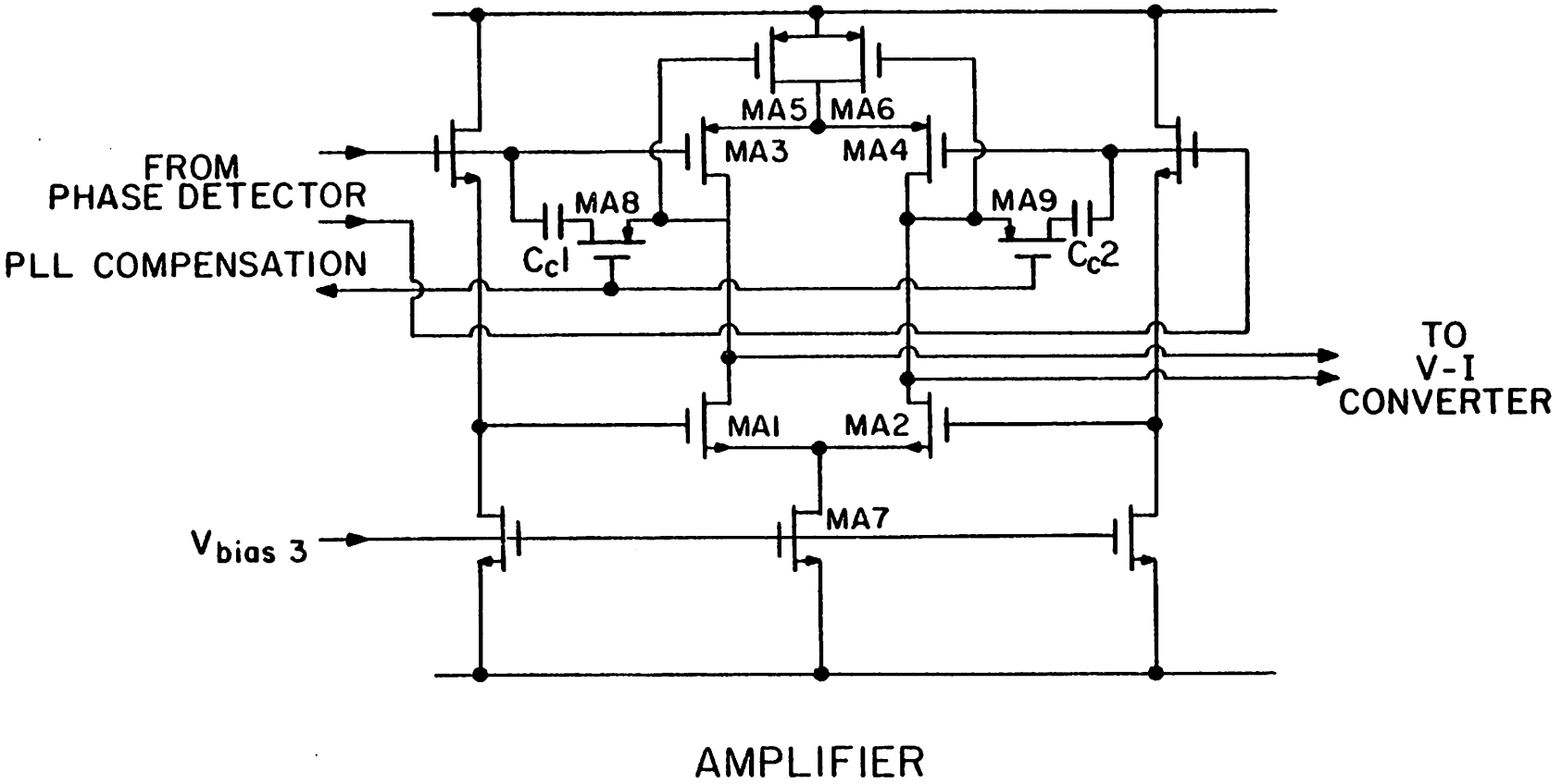


Figure 5.9

DC amplifier and the loop filter.

drive voltages ($V_{GS}-V_{th}$) must be chosen to be low. On the other hand, for the PLL to be able to handle relatively high signal levels, high ($V_{GS}-V_{th}$) is required. The choice of transistor channel lengths is limited by the fact that larger size transistors have higher parasitic capacitance which results in the degradation of the PLL phase margin. These considerations must be accounted for the design of the amplifier.

5.3.4. Loop Filter

The loop filter consists of C_{c1} , C_{c2} and MA_8 , MA_9 (Fig. 5.9). It performs as a lag-lead type filter which generates a pair of left-hand plane pole and zero. The compensation capacitor $C_{c1,2}$ is *Miller* multiplied and the frequency response of the loop benefits from the pole-splitting effect of this configuration [16] . The dominant pole is located at

$$\omega_{pole} = -\frac{1}{r_{o_{mult}} A \; C_{c1,2}} \tag{5.49}$$

where A is the amplifier DC gain and is given by equation (5.47) and $r_{o_{mult}}$ is given by

$$r_{o_{mult}} = \frac{2}{\left|\lambda_{MP9,10} + \lambda_{MP3,4,5,6}\right| I_{MP11}} \tag{5.50}$$

The pole location of the loop filter controls the bandwidth and thus, the capture range of the PLL. Hence, the value of $C_{c1,2}$ is dictated by the desired capture range.

The zero is located at

$$\omega_{zero} = -\frac{1}{\left|\frac{1}{g_{o_{MA\,8,9}}} - \frac{1}{g_{m_{(MA\,1,2)}} + g_{m_{(MA\,3,4)}}}\right| C_{c1,2}} \tag{5.51}$$

MA_8 and MA_9 operate in the triode region and the $\left|\frac{W}{L}\right|$ ratio is chosen so that $g_{o_{MA\,8,9}} \ll \left|g_{m_{(MA\,1,2)}} + g_{m_{(MA\,3,4)}}\right|$. This causes the right half plane zero, due to the direct propagation of the signal through the compensation capacitor, to move into the left hand plane to improve the loop phase margin. The zero location can be approximated

by

$$\omega_{zero} \approx -\frac{2\left|\frac{\mu_p C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{th})\right|_{MA\,8,9}}{C_{c\,1,2}} \tag{5.52}$$

As mentioned earlier, $C_{c\,1,2}$ is determined by the pole location and the desired zero location is achieved by the proper choice of $\left|\frac{W}{L}\right|_{MA\,8,9}$. To compensate for process variations the zero location can be controlled externally by changing the gate voltage of *MA* 8 and *MA* 9.

A significant source of extra phase shift, which can result in instability, is that $V_{control}$ has to drive a relatively high capacitance (in this case eight current source transistor gates). To overcome this problem $g_{m_{MI3}}$ must be chosen to be sufficiently high.

5.4. Analysis of the Monolithic Phase-Locked Loop

In the previous section, the PLL building blocks were designed and analyzed. In this section the overall behavior of the PLL will be evaluated. This is best achieved by analyzing the PLL portion of the experimental prototype.

In Table 5.1 the device sizes chosen for the prototype as well as the drain currents are listed. The process parameters of Table 4.1 are used for all the calculations.

First the phase comparator gain is calculated by using equation (5.17) and (5.18)

$$K_D = \frac{\mu C_{ox}}{\pi}\left[\frac{1}{2}\left(\frac{W}{L}\right)_{MP1,2}\left(\frac{W}{L}\right)_{MP3,4,5,6}\right]^{1/2}\left|\frac{2}{\frac{\theta_n}{L_{MP3}}+\frac{\theta_p}{L_{MP9}}}\right|\frac{1}{I_{MP11}}V_{pk\,1}V_{pk\,2} \tag{5.53}$$

It is assumed that $V_{pk\,1} = V_{pk\,2} = 100\ mV$ thus

$$K_D \approx 0.224\ \ V/rad$$

The VCF gain was found as

Phase Detector			
Transistor No.	W [μ]	L [μ]	I_d [μA]
MP1,2	35	10	100
MP3,4,5,6	27	10	50
MP7,8	40	7.5	100
MP9,10	80	15	100
MP11	80	10	200

PLL Bias Circuit			
Transistor No.	W [μ]	L [μ]	I_d [μA]
MB1	80	10	100
MB2	80	10	100
MB3	40	10	100
MB4	25	7.5	100
MB5	80	15	100
MB6	80	15	100
MB7	40	10	100

Voltage to Current Converter			
Transistor No.	W [μ]	L [μ]	I_d [μA]
MI1,2	60	7.5	300
MI3	100	10	300
MI4	390	10	600
MI5	130	10	200

DC Amplifier			
Transistor No.	W [μ]	L [μ]	I_d [μA]
MA1,2	80	15	100
MA3,4	80	15	100
MA5,6	25	7.5	100
MA7	80	10	100
MA8,9	10	40	

Table 5.1. Device Sizes and Current Levels for PLL Building Blocks

$$K_o = 2Q\ \omega \left| \frac{\frac{\mu_p C_{ox}}{2} \left(\frac{W}{L}\right)_{MI1}}{2I_{MI4}} \right|^{1/2} \tag{5.54}$$

The designed second order filter has a quality factor of eight thus

$$K_o \approx 5\ \omega_0 \quad rad / V-sec$$

The DC amplifier gain is given by equation (5.47) as

$$A = \frac{2}{\frac{\theta_n}{L_{MA\,1,2}} + \frac{\theta_p}{L_{MA\,3,4}}} \frac{\left| \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_{MA\,1,2} \right|^{1/2} + \left| \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L}\right)_{MA\,3,4} \right|^{1/2}}{\left| \frac{I_{MA\,7}}{2} \right|^{1/2}} \quad (5.55)$$

substituting for the parameters

$$A \approx 280$$

Thus the open loop gain is given by

$$K_v = K_D K_o A \approx 320\,\omega_0$$

and the DC open loop gain is found to be

$$A_{PLL} = \frac{K_v}{\omega_0} \approx 320$$

Substituting for A_{PLL} in (5.4)

$$f_0^{locked} = f_{ref} + \frac{f_0^{unlocked} - f_{ref}}{320}$$

which results in an extremely small error between the locked center frequency and the reference frequency.

In this part the open-loop frequency response of the PLL is analyzed to ensure the stability of the loop.

The center frequency of the designed filter is at $f_0 = 500\ KHz$ thus

$$K_v \approx 320\,\omega_0 \approx 1GHz$$

The loop filter singularities are found by using equations (5.49) and (5.52).

$$\omega_{pole} = -\frac{\left(\lambda_{MP\,9,10} + \lambda_{MP\,3,4,5,6}\right) I_{MP\,11}}{2} \frac{1}{A\ C_{c\,1,2}} \quad (5.56)$$

$C_{c\,1,2}$ was chosen to have a value of 50 pF, therefore

$$f_{pole} \approx -22\ Hz$$

and

$$\omega_{zero} \approx -\frac{2\left[\frac{\mu_p C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{th})\right]_{MA\,8,9}}{C_{c\,1,2}} \qquad (5.57)$$

substituting for the parameters

$$f_{zero} \approx -100\ KHz$$

Using the open loop gain and the pole and zero locations found in the above analysis, the bode plot of the loop gain is sketched in Fig. 5.10 . The unity-gain frequency is at about 250 KHz. Note that the zero has increased the phase-margin by about 60 degrees which ensures closed loop stability.

As was mentioned in section (4.3), the fact that $MI3$ has to drive eight current sources may result in phase margin degradation. To calculate the pole due to this, the information is Table 5.1 is used to find

$$g_{m_{MI3}} = \frac{1}{1667}\ \ mho$$

In Table 4.3 the sizes of M_{10} and M_{11} where given to be $\frac{80}{10}$ and $\frac{10}{10}$. Thus the total gate capacitances is

$$8\,C_{gs} = 8 \times \frac{2}{3} \times WLC_{ox}$$

which turns out to be equal to

$$8\,C_{gs} \approx 4.2\ pF$$

To find the total capacitance of this node, the C_{gs} of $MI3$ and $MB3$ should also be calculated

$$C_{gs_{MI3}} + C_{gs_{MB3}} \approx 0.8\ pF$$

Assuming 1 pF for all the other parasitic capacitances

$$C_{total} \approx 6\ pF$$

and the resulting pole is located at about

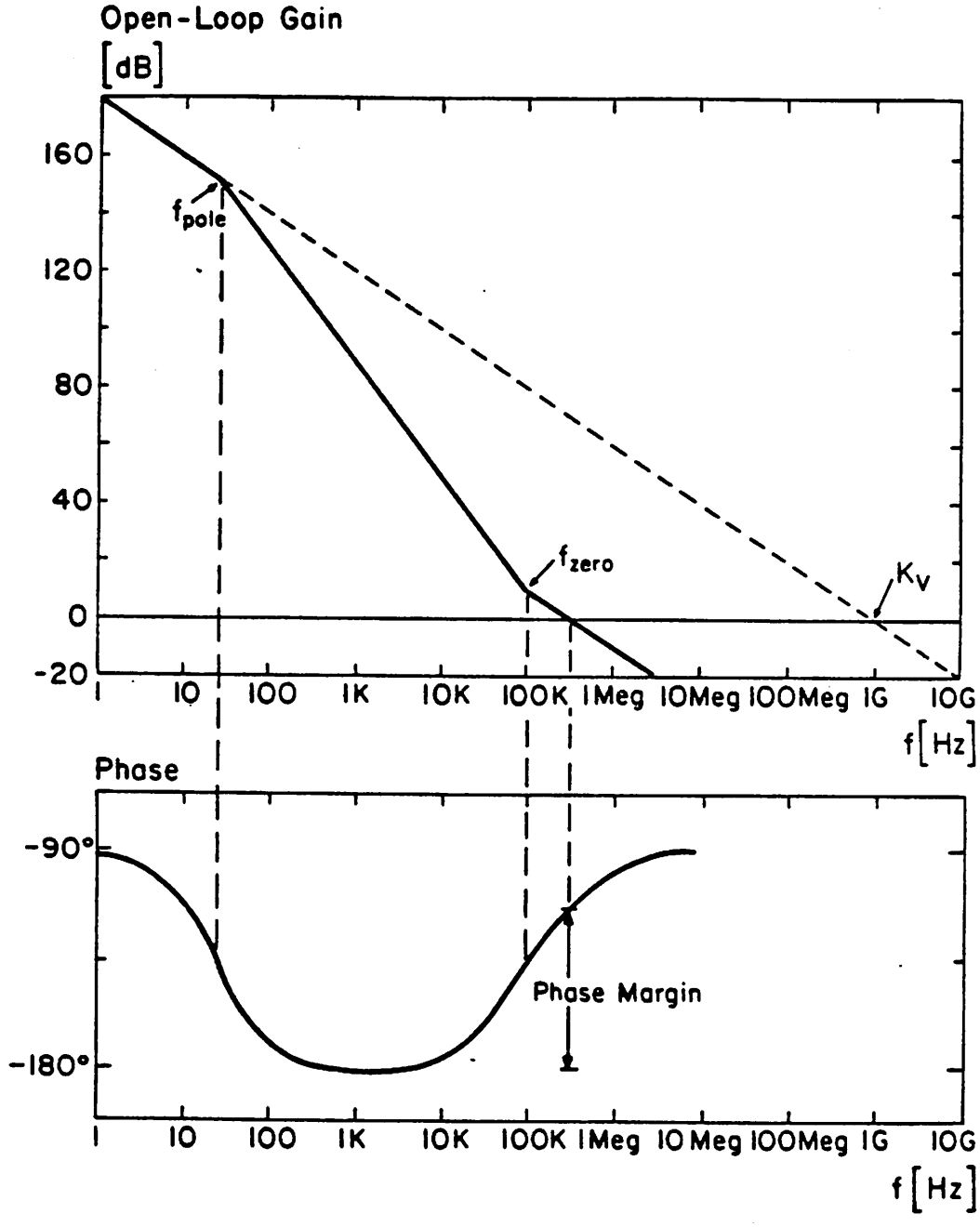


Figure 5.10

PLL open-loop amplitude and frequency response.

$$f_{pole} = \frac{g_{m_{MI3}}}{2\pi C_{total}} \approx 16\ MHz$$

which results in about 1 degree extra phase shift at the unity-gain frequency of the open-loop gain.

In the next chapter, the experimental results of the PLL analyzed in this section are presented.

CHAPTER 6

EXPERIMENTAL RESULTS

In this chapter, the results from an experimental prototype are presented. A sixth-order bandpass filter with an on-chip center frequency control phase-locked loop with a center frequency of $500KHz$ and a quality factor of five was designed and fabricated. The design of a bandpass filter with the above specifications was discussed in chapter 4 and the phase-locked loop was explained in chapter 5. Fig. 6.1 shows the microphotograph of the experimental chip. A $6-micron$ single-poly n-well CMOS technology was used and the die area is about $4mm^2$.

In Fig. 6.2(a) the overall frequency response of the filter is shown. The detailed passband of the two different outputs of the filter is seen in Fig. 6.2(b). The frequency response of the filter is very close to the shape simulated with the program SPICE and a $\pm$ 10% variation in the power supply voltage produced no significant change in the filter frequency response.

The functionality of the PLL is shown in Fig. 6.3, note that the markers are added externally to indicate the reference frequency. First a reference frequency at $450KHz$ is applied, the filter frequency response locks to this frequency. Then the reference frequency is changed to $500KHz$, the filter follows this change. The last curve is for a reference frequency at $550KHz$. This corresponds to a 20% lock range for the phase-locked loop.

The maximum output voltage with acceptable distortion is measured in Fig. 6.4 . The measurement is performed for 1 % third order intermodulation distortion, $IM\,3$. The output voltage for this condition is about 300 $mVP-P$ or 106 $mVrms$. The maximum output voltage for the integrator was calculated in section (4.2.1.1) to be

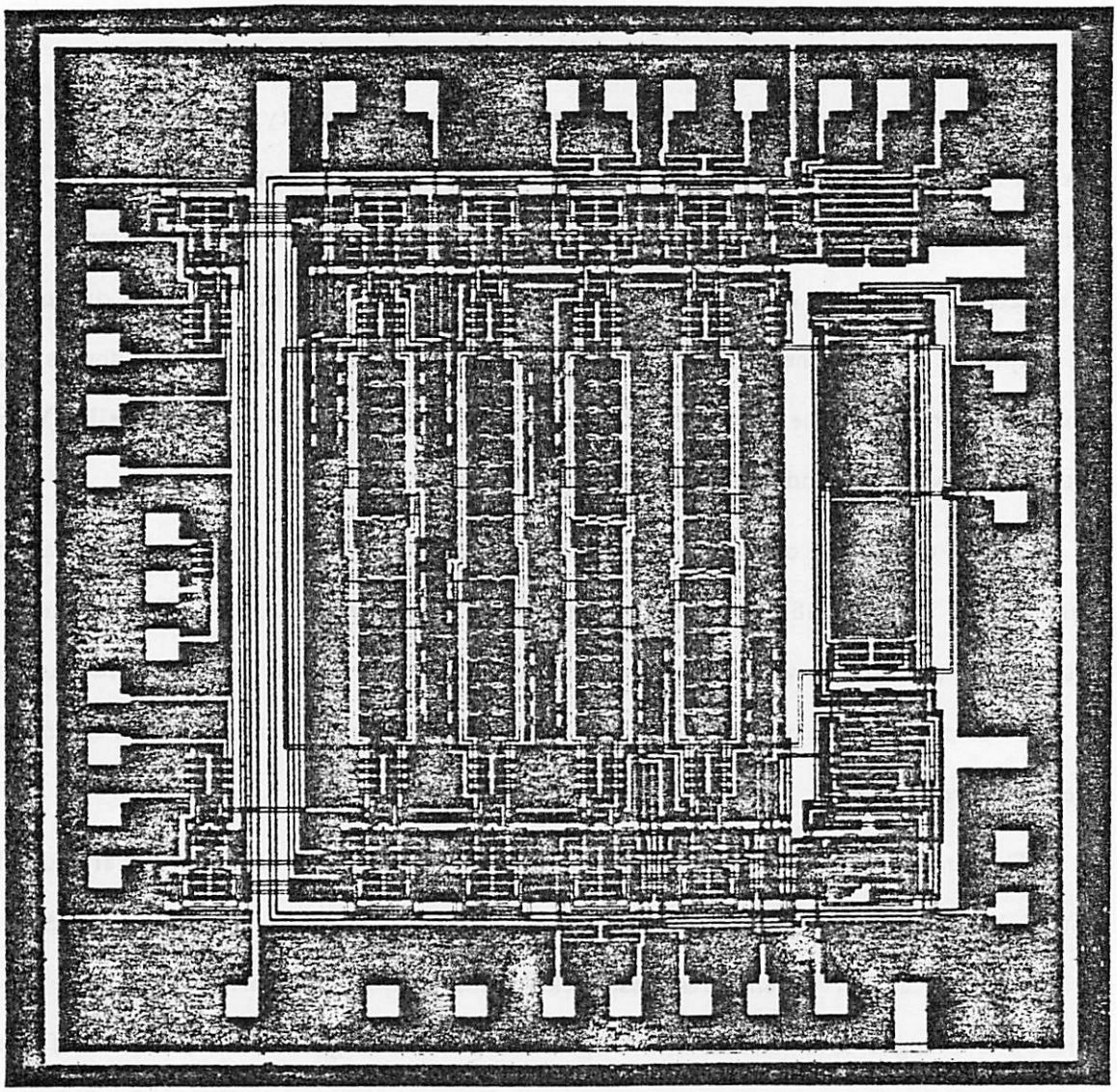
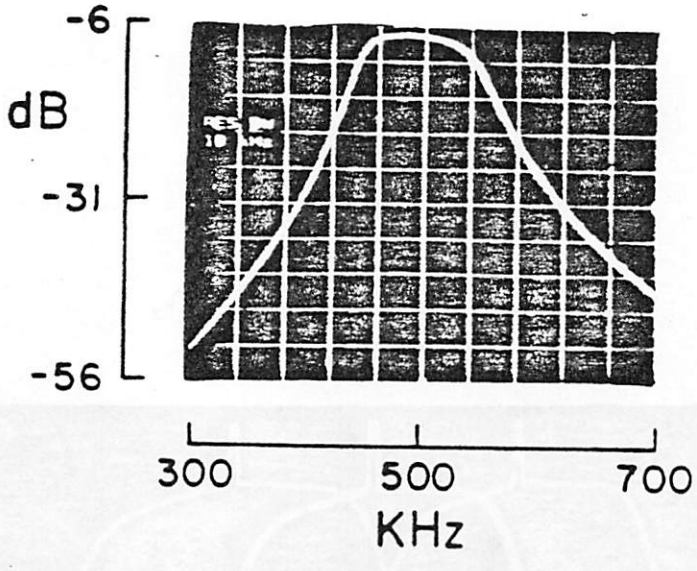
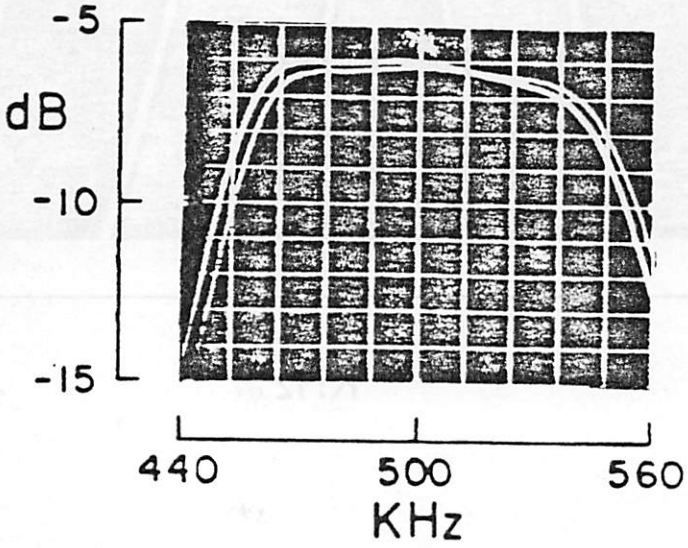


Figure 6.1

Microphotograph of the experimental chip.



(a)



(b)

Figure 6.2

(a) -Overall frequency response of the prototype.
(b) -Detailed passband of two outputs of the filter.

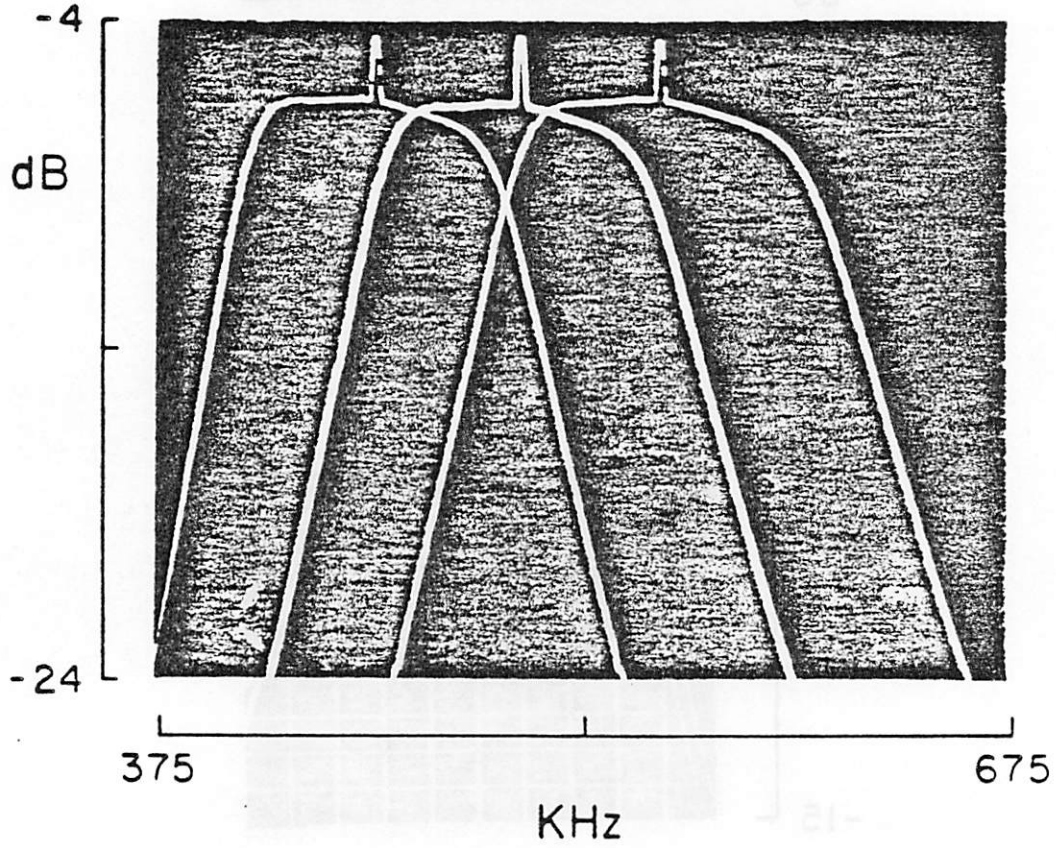


Figure 6.3

PLL functionality test.

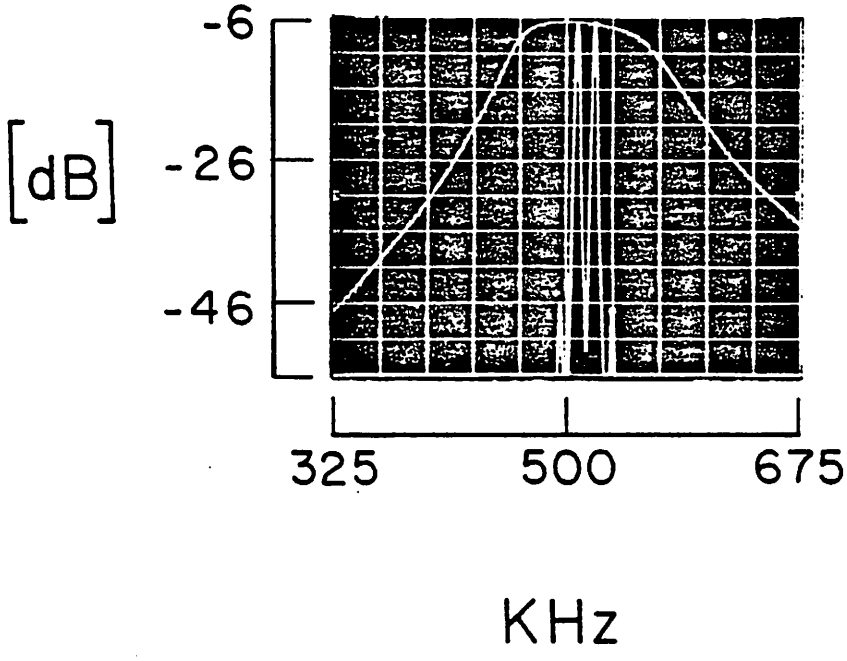


Figure 6.4

Maximum output voltage for $IM\,3 = 1\%$.

230 mV. Considering the fact that for the identical integrator filter architecture there exits a 6 dB loss in the dynamic range (section 4.2.2), the theoretical maximum voltage turns out to be about 115 $mVrms$ which is consistent with the measured 106 $mVrms$.

The total in-band noise is found from Fig. 6.5 to be about $30\mu Vrms$ for a bandwidth of $96KHz$. In order to compare the experimental noise to the theoretical noise, the prototype values of $C_{intg} = 38pf$ and $Q_{res} = 8$ are substituted in equation (4.51)

$$\overline{v_{out}^2} = 3\,\frac{kT}{C_{intg}}\,Q_{res}^{term}$$

which gives a total output noise of $50\mu Vrms$. Note that the experimental value is for the total "in-band" noise whereas the calculated value includes noise over the whole frequency range. The results are reasonably consistent considering the fact that most of the noise power falls within the passband of the filter. The center frequency of the filter was controlled externally for the noise measurement. The reference signal feed-through at the output of the filter was measured by controlling the center frequency through the phase-locked loop. As can be seen in Fig. 6.6 the feed-through is about 100 $\mu Vrms$ which exceeds the output noise and degrades the dynamic range by $10dB$. The relatively high reference signal feed-through is partly due to the fact that for debugging purposes, some extra nodes were connected to bonding pads which increased the parasitic couplings. Another reason for this is due to some asymmetry in the filter layout.

Using the above measurements the dynamic range of the filter could be calculated: For the stand-alone filter (external center frequency control), the dynamic range is found to be

$$Dynamic\ Range = \frac{100\ mV}{30\ \mu V} = 70.5\ dB$$

The dynamic range of the filter while controlled by the PLL, is determined by the

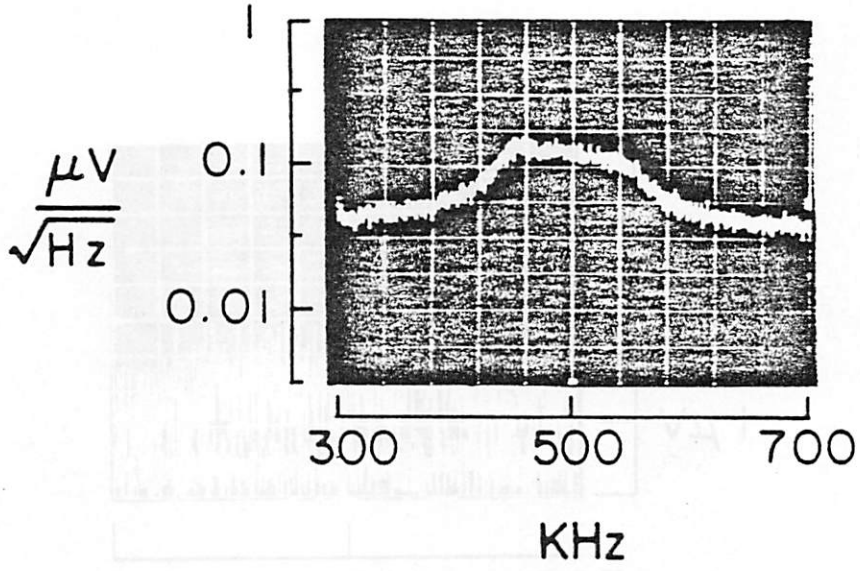


Figure 6.5

Measured noise response of the filter.

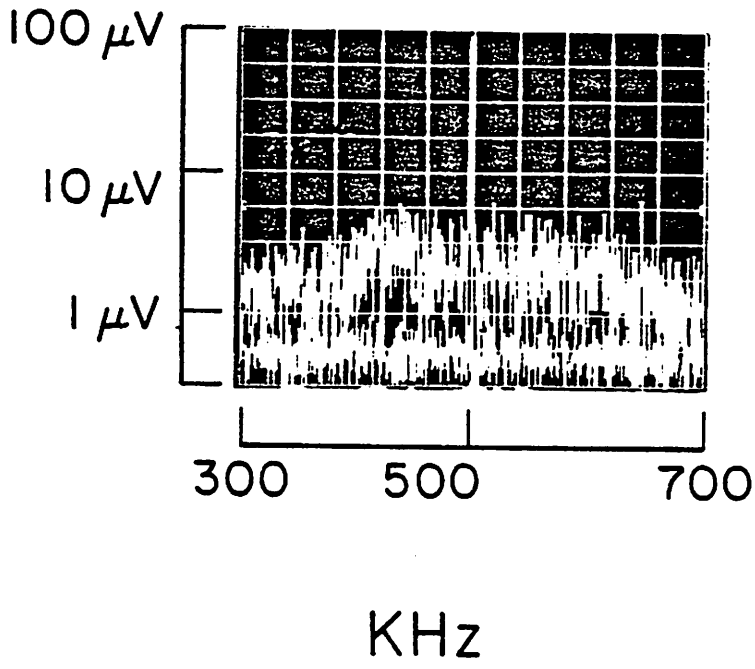


Figure 6.6

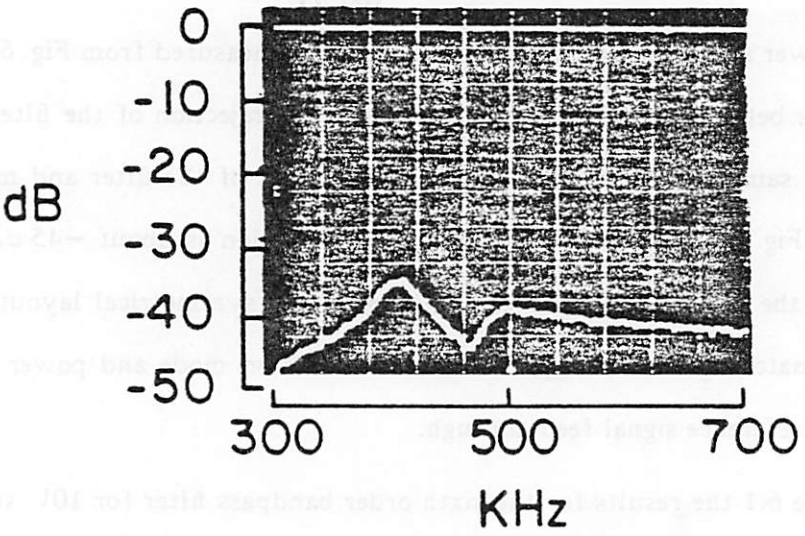
Reference signal feed-through to the output of the filter.

reference signal feed-through rather than the output noise.

$$Dynamic\ Range = \frac{100\ mV}{100\ \mu V} = 60\ dB$$

The power supply rejection for both supplies is measured from Fig. 6.7(a) and Fig. 6.7(b) and is better than $35dB$. The common mode rejection of the filter is tested by applying the same signal to the two differential input of the filter and monitoring the output. As Fig. 6.8 shows, the common mode rejection is about $-45\ dB$ within the passband of the filter. It is believed that a perfectly symmetrical layout and a better component matching should improve both the common mode and power supply rejection and the reference signal feed-through.

In Table 6.1 the results for the sixth order bandpass filter for $10V$ supply voltage is summarized.



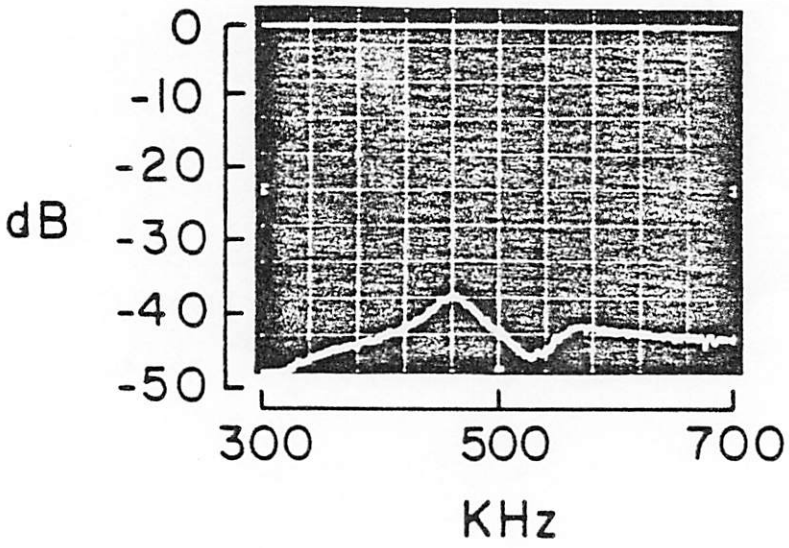


Figure 6.7

Power supply rejection with respect to the positive and negative supply.

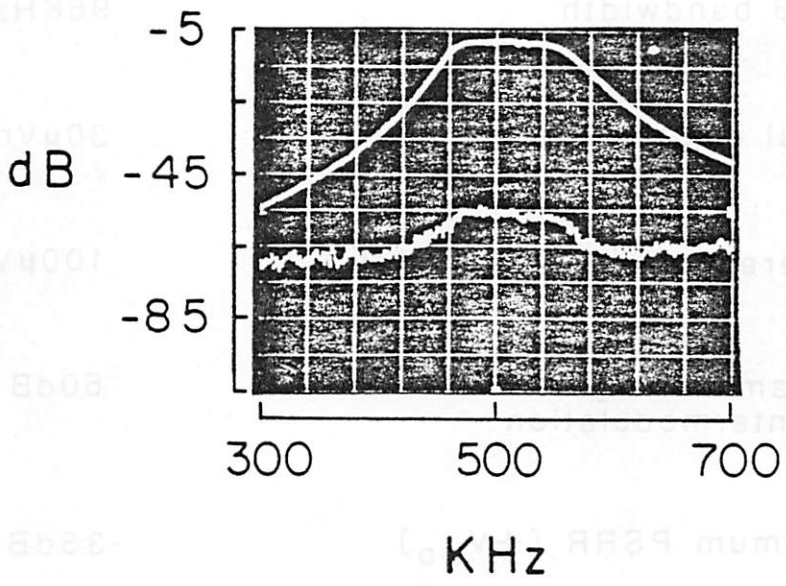


Figure 6.8

Common mode rejection measurement.

Experimental results of the sixth order bandpass filter for 10V supply voltage

Center frequency	500KHz
-3dB bandwidth	96KHz
Total in-band noise	30μVrms
Reference signal feed-thru	100μVrms
Dynamic Range 1% intermodulation	60dB
Minimum PSRR ($+V_{DD}$)	-35dB
Minimum PSRR ($-V_{SS}$)	-38dB
Power dissipation	55mW

Table 6.1- Experimental results of the six order bandpass filter for 10V supply voltage

CHAPTER 7

CONCLUSION

A design approach to implement high-frequency continuous-time filters was presented. From the experimental performance of the filter it can be concluded that this technique is indeed a viable method for the implementation of high-frequency filters.

The problems hindering the extension of the low-frequency frequency-locked filtering techniques were overcome by 1) using a simple circuit configuration for the integrator design and utilizing the phase error cancellation technique. 2) Modifying the conventional phase-locked loop scheme for controlling the center frequency of the filter. Instead of the VCO a voltage controlled filter, VCF, was utilized. Detailed analysis proved that the error due to this is very small. 3) Fully differential architecture was employed to improve the power supply and common mode rejection and thus minimized the reference signal feed-through to the output of the filter.

The fundamental limitations of this approach were studied in chapter 4. In Fig.7.1 the capability of this technique in a scaled technology is projected. Here the maximum filter Q and the optimum transistor channel length is sketched as a function of center frequency for typical process variations. It shows that a maximum Q of about 50 can be achieved at the center frequency of $100KHz$ and drops down to about 2.5 for $100MHz$. With the progress of processing technology, (e.g., more accurate poly-silicon etching), the maximum achievable Q can be improved. The other curve shows the optimum input transistor channel length for different frequencies. From this curve it can be concluded that the implementation of filters with center frequencies up to $20MHz$ can be realized in a $6-micron$ technology, and a $100MHz$ filter requires a

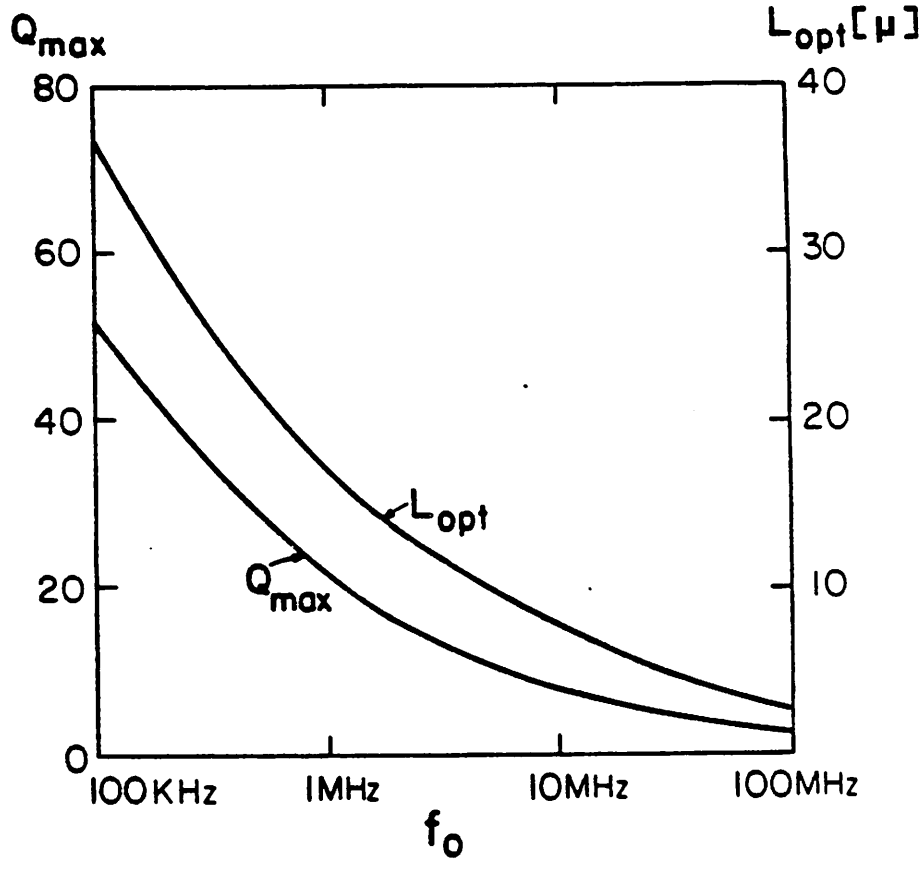


Figure 7.1

Maximum Q and optimum input transistor channel length as a function of frequency

3—*micron* technology.

One major shortcoming of this approach is the relatively low dynamic range. This is due to two facts; one is the nonlinear behavior of the integrator which limits the upper bound of the signal. The second problem is the reference signal feed-through which determines the lower limit of the signal. Improving the dynamic range of the filter is an area where future work may be directed.

APPENDIX A

HIGH-FREQUENCY CHARACTERISTICS OF MOS TRANSISTORS

The objective of this section is to investigate the high-frequency small-signal behavior of the transconductance and input admittance of the MOS transistor operating in the saturation region.

A.1. High-frequency transconductance of the MOS transistor

Due to the distributed nature of the gate capacitance and channel resistance, the MOS transistor behaves as a nonlinear RC transmission line. This phenomena gives rise to an infinite number of high-frequency poles in the frequency response of the transconductance [22].

The high-frequency performance of the MOS transistor is best analyzed as an array of series combination of n transistors as shown in Fig. A.1 . These transistors have the same channel width as the original transistor but their channel length is equal to $\frac{L}{n}$. Note that M_1 through M_{n-1} operate in the triode region and M_n is in saturation region. Fig. A.2 shows the small signal equivalent circuit of the transistors. To simplify the analysis, the gate-drain capacitance as well as the small signal output resistance of the transistor is neglected.

It can be shown that for such a circuit

$$\frac{i_d}{v_{gs}} = \frac{g_{m_0}}{1 + b_1 s + b_2 s^2 + b_3 s^3 \ldots\ldots} \qquad (A.1)$$

where g_{m_0} is the DC small signal transconductance of the transistor.

Finding the value of each and every pole of the above equation is not a trivial task. For most applications, the infinite number of poles can be approximated by a

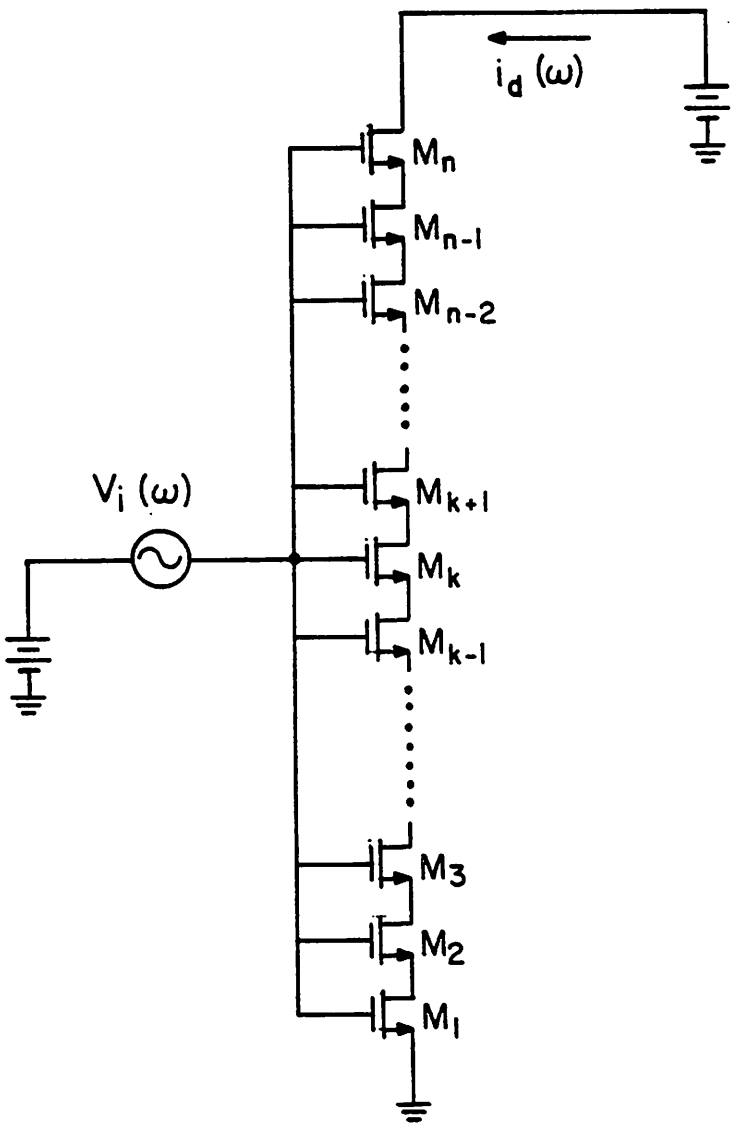


Figure A.1

An MOS transistor as an array of n transistors in series.

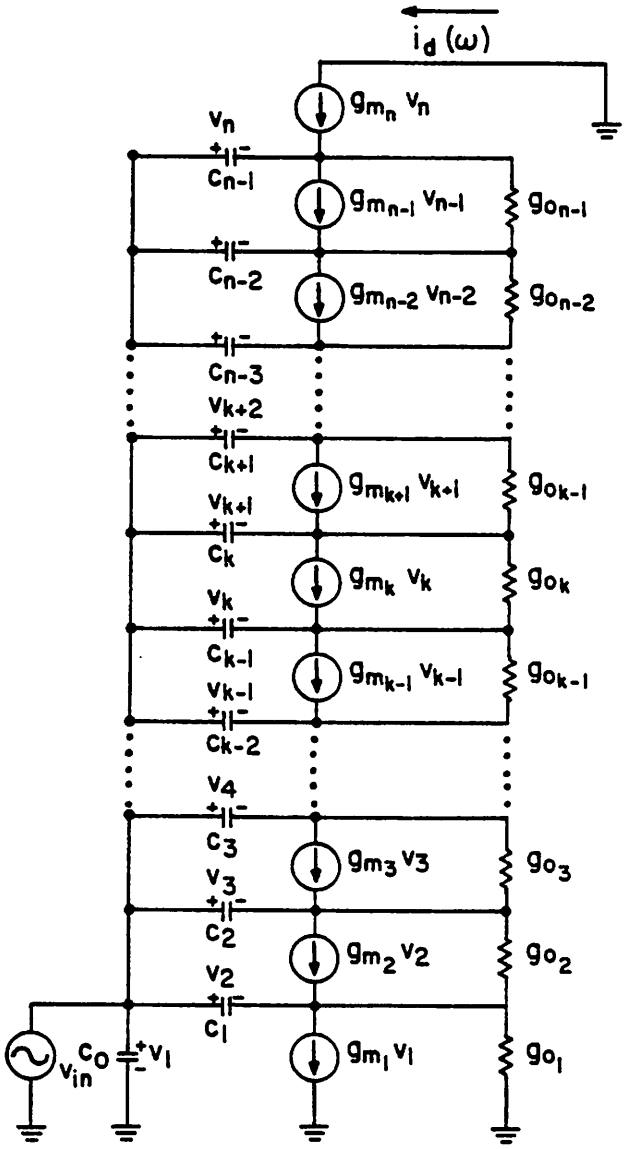


Figure A.2

Small signal equivalent circuit of an MOS transistor simulated as an array of n transistors in series.

single effective pole at the frequency

$$p_{2_{effective}} \approx \frac{1}{\sum_{i=0}^{i=\infty} \frac{1}{p_i}} \tag{A.2}$$

It can be shown that

$$b_1 = \sum_{i=0}^{i=\infty} \frac{1}{p_i} \tag{A.3}$$

thus

$$p_{2_{effective}} \approx \frac{1}{b_1} \tag{A.4}$$

b_1 can be found by using the *Zero-Value Time Constant* [16] method for which

$$b_1 = \sum_{i=0}^{i=\infty} T_{0_i} \tag{A.5}$$

and

$$T_{0_k} = R_{o_k} C_k \tag{A.6}$$

where R_{o_k} is the driving point resistance at the C_k node pair with all other capacitors set to zero.

To find the driving point resistance of the k^{th} capacitor nodes, all the other capacitors are set to zero and a test current, i_x, is applied to the corresponding nodes as shown in Fig. A.3(a). The resulting v_x is calculated as

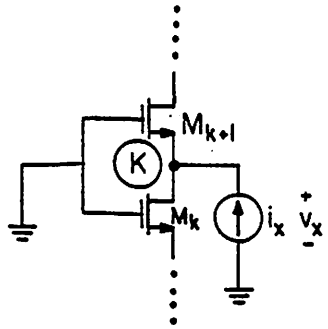
$$R_{o_k} = \frac{v_x}{i_x} \tag{A.7}$$

In order to find this we need to know the output conductance and transconductance of each transistor. These parameters are found to be equal to

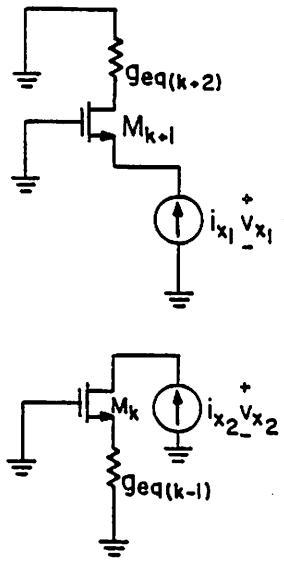
$$g_{o_{(M_k)}} = g_{m_0} \sqrt{n\,(n-k)} \tag{A.8}$$

$$g_{m_{(M_k)}} = g_{m_0} \sqrt{n} \left[\sqrt{n-k+1} - \sqrt{n-k} \right] \tag{A.9}$$

$$C_0 = \frac{C_{ox} WL}{2n} \tag{A.10}$$



(a)



(b)

Figure A.3

Equivalent circuit for the calculation of R_{o_k}.

$$C_1 = C_2 = \ldots\ldots = C_{n-2} = \frac{C_{ox} WL}{n} \tag{A.11}$$

$$C_{n-1} = \frac{7}{6n} C_{ox} WL \tag{A.12}$$

where $g_{m_{(M_k)}}$ and $g_{o_{(M_k)}}$ are the transconductance and output conductance of the k_{th} transistor. It is easier to break the connection at node k and find the contribution of M_{k+1} and M_k separately. Fig. A.3(b) shows the equivalent circuit for the calculation of R_{o_k}. In this case

$$\frac{1}{R_{o_k}} = \frac{i_{x1}}{v_{x1}} + \frac{i_{x2}}{v_{x2}} \tag{A.13}$$

Let's define $\frac{i_{x1}}{v_{x1}}$ as $g_{S_{M_{k+1}}}$ and $\frac{i_{x2}}{v_{x2}}$ as $g_{D_{M_k}}$, thus

$$g_{o_k} = g_{S_{M_{k+1}}} + g_{D_{M_k}} \tag{A.14}$$

It can be found that

$$\frac{1}{g_{S_{M_{k+1}}}} = \frac{1}{g_{o_{M_{k+1}}} + g_{m_{M_{k+1}}}} \left| 1 + \frac{g_{o_{M_{k-1}}}}{g_{eq_{k+2}}} \right| \tag{A.15}$$

and

$$\frac{1}{g_{D_{M_k}}} = \frac{1}{g_{o_{M_k}}} \left| 1 + \frac{g_{m_{M_k}} + g_{o_{M_k}}}{g_{eq_{k-1}}} \right| \tag{A.16}$$

note that $g_{eq_{k-1}} = g_{D_{M_{k-1}}}$ and $g_{eq_{k+2}} = g_{S_{M_{k+2}}}$

Substituting for (A.8) and (A.9) and manipulating the above equation

$$g_{S_{M_{k+1}}} = g_{m_0} \frac{\sqrt{n}}{\sqrt{n-k}} \tag{A.17}$$

and

$$g_{D_{M_k}} = g_{m_0} \frac{\sqrt{n(n-k)}}{k} \tag{A.18}$$

substituting from (A.17) and (A.18) in (A.14)

$$g_{o_k} = g_{m_0}\sqrt{n}\left[\frac{1}{\sqrt{n-k}} + \frac{\sqrt{n-k}}{k}\right] \tag{A.19}$$

or

$$g_{o_k} = g_{m_0}\frac{n\sqrt{n}}{k\sqrt{n-k}} \qquad 0<k\leqslant n-1 \tag{A.20}$$

to find the *Zero-Value Time Constant*

$$b_1 = \sum_{i=1}^{i=n-1}\frac{C_i}{g_{o_i}} \tag{A.21}$$

substituting from (A.11) and (A.12)

$$b_1 = \left[\frac{C_{ox}WL}{n}\sum_{k=1}^{k=n-2}\frac{1}{g_{o_k}}\right] + \left[\frac{7}{6}\frac{C_{ox}WL}{n}\frac{1}{g_{o_{n-1}}}\right] \tag{A.22}$$

substituting from (A.20)

$$b_1 = \frac{C_{ox}WL}{n^2\sqrt{n}\ g_{m_0}}\left[\sum_{k=1}^{k=n-2} k\sqrt{n-k} + \frac{7}{6(n-1)}\right] \tag{A.23}$$

for $n \rightarrow \infty$ the above series could be transformed to

$$b_1 = \frac{C_{ox}WL}{g_{m_0}}\left[\frac{\Gamma(\frac{3}{2})\,\Gamma(2)}{\Gamma(\frac{7}{2})}\right] \tag{A.24}$$

or

$$b_1 = \frac{C_{ox}WL}{g_{m_0}}\frac{4}{15} \tag{A.25}$$

but

$$\frac{C_{ox}WL}{g_{m_0}} = \frac{3}{2}\frac{1}{\omega_t} \tag{A.26}$$

Thus b_1 is found to be

$$b_1 = \frac{2}{5}\frac{1}{\omega_t} \tag{A.27}$$

or

$$p2_{effective} \approx 2.5\,\omega_t \tag{A.28}$$

This implies that the transconductance of an MOS transistor has a value lower by

$-3dB$ at $2.5\omega_t$ compared to it's DC value. Fig. A.4(a) gives the approximate location of the poles and Fig. A.4(b) shows the location of the effective pole.

To verify this result an MOS transistor was simulated by the computer circuit simulation program SPICE [21] by modeling the transistor as 36 transistors in series which is a more accurate analysis than the above one-pole approximation. The result is shown in Fig.A.5 which proves that the *Zero-Value Time Constant* method is a relatively reasonable method to find the effective pole of the response for frequencies up to about $2\ \omega_t$ of the MOS transistor.

A.2. High-Frequency Input Admittance of the MOS transistor

For low frequencies the input admittance of the MOS transistor is capacitive and

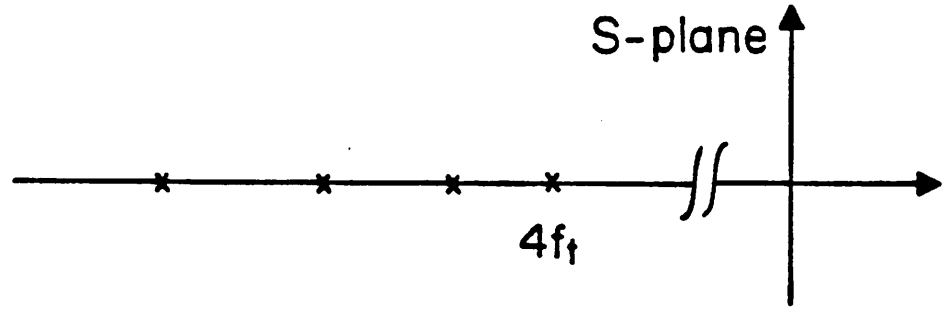
$$Y_{in} = s \times \frac{2}{3} C_{ox} WL \tag{A.29}$$

At high-frequencies, the distributed capacitance and channel resistance results in some more singularities in the input admittance.

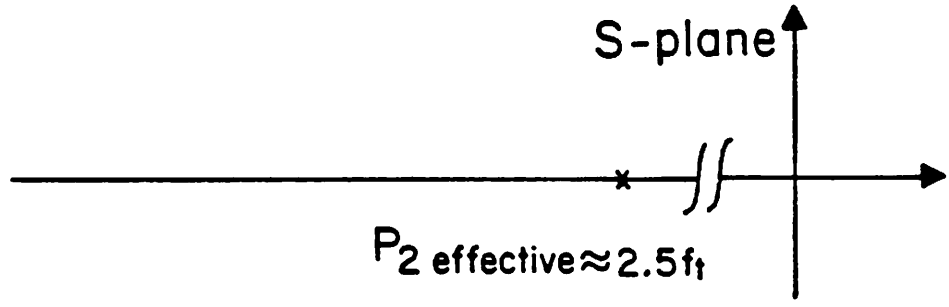
Analyzing the small signal equivalent circuit shown in Fig. A.2, it can be shown that the input admittance has the form [23]

$$Y_{in} = sC_{gs} \frac{\prod_{i=1}^{i=\infty}(1+\frac{s}{z_i})}{\prod_{i=1}^{i=\infty}(1+\frac{s}{p_i})} \tag{A.30}$$

By inspection it can be shown that the poles are exactly at the same locations as the transconductance poles and the zeros are located in between the poles. The first singularity is a pole as shown in Fig. A.6 . For frequencies lower than about ω_t of the transistor, finding the exact locations of all the poles and zeros is not necessary and the input admittance can be well approximated by



(a)



(b)

Figure A.4

(a) -Approximate location of the drain current poles.
(b) -Location of the effective pole.

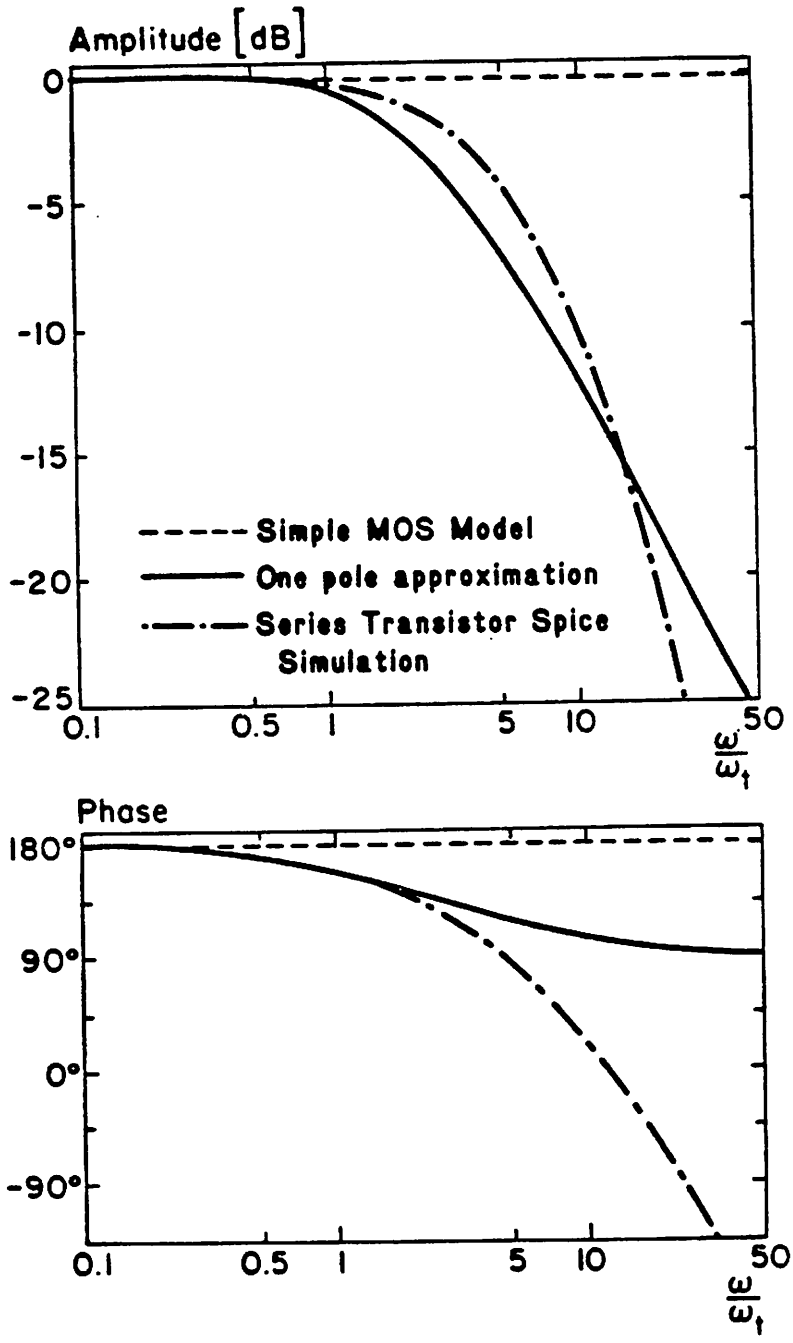
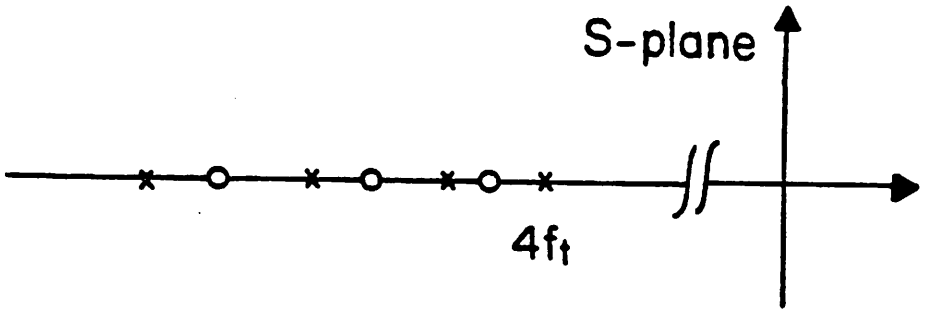
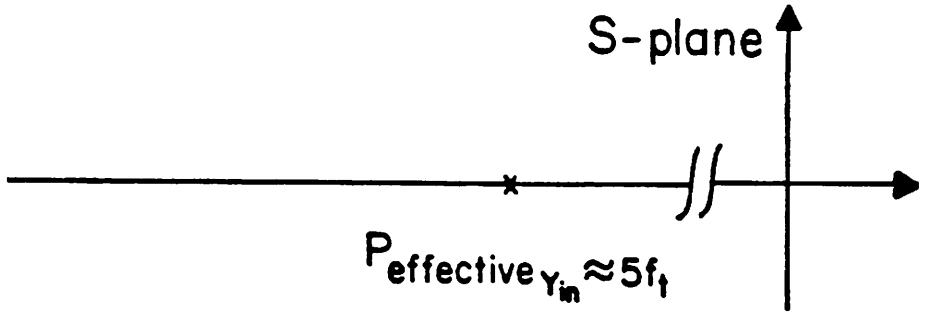


Figure A.5

Amplitude and phase of the drain current as a function of the frequency. 1) simple transitor model 2) one pole approximation 3) SPICE simulation.



(a)



(b)

Figure A.6

The poles and zeros of the input admittance of an MOS transistor.

$$Y_{in} \approx sC_{gs} \frac{(1+s\sum_{i=1}^{i=\infty}\frac{1}{z_i})}{(1+s\sum_{i=1}^{i=\infty}\frac{1}{p_i})} \tag{A.31}$$

It can be shown that Y_{in} can be approximated as

$$Y_{in} \approx sC_{gs} \frac{1}{1+s\sum_{i=1}^{i=\infty}\frac{1}{p_i} - s\sum_{i=1}^{i=\infty}\frac{1}{z_i}} \tag{A.32}$$

and

$$p_{effective} \approx \frac{1}{\sum_{i=1}^{i=\infty}\frac{1}{p_i} - \sum_{i=1}^{i=\infty}\frac{1}{z_i}} \tag{A.33}$$

The easiest way to find $p_{effective_{Y_m}}$ is by SPICE simulation of a single transistor modeled as many transistors in series which is shown in Fig. A.7. The 45 degree phase shift point is found to be at about $5\omega_t$. thus

$$p_{effective} \approx 5\,\omega_t \tag{A.34}$$

As mentioned earlier the pole locations of Y_{in} is exactly the same as the transconductance. That is,

$$\sum_{i=0}^{i=\infty}\frac{1}{p_i} = \frac{1}{2.5\,\omega_t} \tag{A.35}$$

from (A.33) (A.34) and (A.35), it can be concluded that

$$\sum_{i=0}^{i=\infty}\frac{1}{z_i} \approx \frac{1}{5\,\omega_t} \tag{A.36}$$

therefore

$$Y_{in} \approx sC_{gs}\frac{1+\frac{s}{5\,\omega_t}}{1+\frac{s}{2.5\,\omega_t}} \tag{A.37}$$

For all singularities represented by one effective pole.

$$Y_{in} \approx sC_{gs}\frac{1}{1+\frac{s}{5\,\omega_t}} \tag{A.38}$$

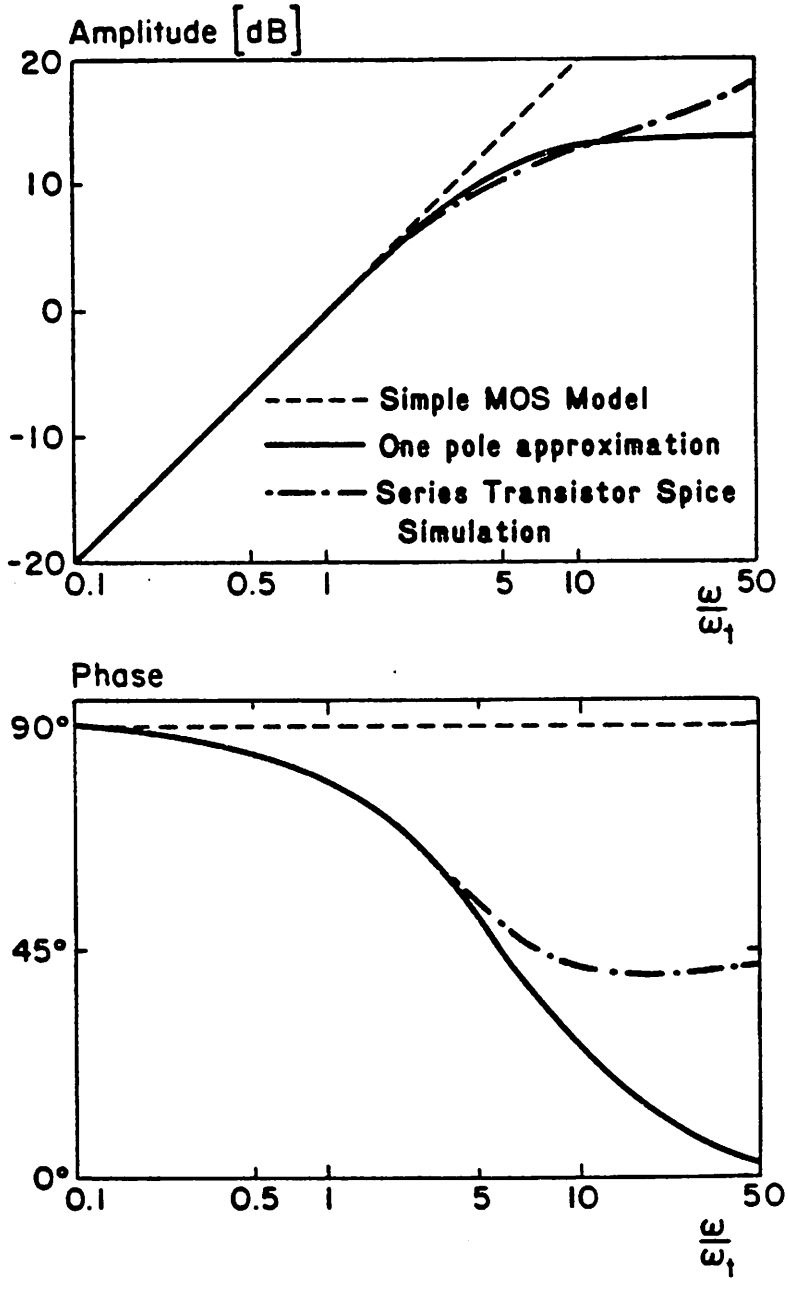


Figure A.7

Amplitude and phase of the input admittance as a function of frequency given by 1) simple transistor model 2) one pole approximation 3) SPICE simulation

In Fig. A.7 the result of the SPICE simulation of the input admittance of an MOS transistor is compared to the one-pole approximation.

The quality factor of the input capacitance is found to be

$$Q_{C_m} \approx \frac{5\,\omega_t}{\omega} \tag{A.39}$$

Fig. A.8 shows an approximate equivalent circuit for the input admittance.

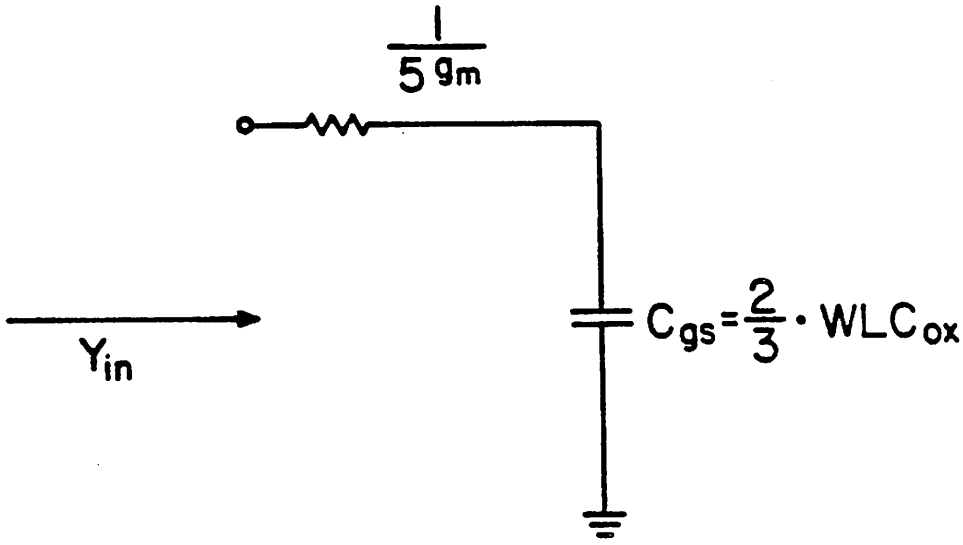


Figure A.8

Equivalent circuit for the input admittance of an MOS transistor.

APPENDIX B

TOTAL OUTPUT NOISE POWER OF THE BANDPASS FILTER

To evaluate the filter noise performance, the total output noise power of a second and sixth order bandpass filter is derived in this section.

For an n^{th} order bandpass filter, made of n identical integrators, there exists n independent noise sources. The total output noise power of the filter, $\overline{v_{OT}^2}$, is given by

$$\overline{v_{OT}^2} = \int_0^{+\infty} S_o(f)\,df = \sum_{m=1}^{m=n} \int_0^{+\infty} |H_m(jf)|^2 S_i(f)_{intg}\,df \qquad \text{(B.1)}$$

where

$S_o(f)$ is the output noise spectral density.

$S_i(f)_{intg}$ is the input referred noise spectral density of an integrator.

$H_m(jf)$ is the transfer function of the m^{th} node to the output of the filter.

The derivation of $\overline{v_{OT}^2}$ could be drastically simplified by assuming that the input referred noise spectral density of the integrator $S_i(f)_{intg}$ is frequency independent. In chapter 4 it was shown that this assumption is indeed true for MOS integrators at high frequencies. Thus the above equation simplifies to

$$\overline{v_{OT}^2} = S_{i_{intg}} \sum_{m=1}^{m=n} \int_0^{+\infty} |H_m(jf)|^2\,df \qquad \text{(B.2)}$$

To find the total output noise, the transfer function from each integrator input to the output of the filter should be derived.

B.1 Total Output Noise of a Second Order Bandpass Filter

In Fig. B.1 the flow-graph of a second order bandpass filter with the corresponding noise sources is demonstrated. It can be shown that

$$H_1(j\omega) = \frac{v_{out}}{v_{n_1}} = \frac{\left|\frac{\omega_0}{s}\right|^2}{1 + \frac{\omega_0}{s}\frac{1}{Q} + \left|\frac{\omega_0}{s}\right|^2} \tag{B.3}$$

$$H_2(j\omega) = \frac{v_{out}}{v_{n_2}} = \frac{\left|\frac{\omega_0}{s}\right|}{1 + \frac{\omega_0}{s}\frac{1}{Q} + \left|\frac{\omega_0}{s}\right|^2} \tag{B.4}$$

and

$$|H_1(jf)|^2 = \frac{Q^2\left|\frac{f_0}{f}\right|^2}{1 + Q^2\left|\frac{f_0}{f} - \frac{f}{f_0}\right|^2} \tag{B.5}$$

$$|H_2(jf)|^2 = \frac{Q^2}{1 + Q^2\left|\frac{f_0}{f} - \frac{f}{f_0}\right|^2} \tag{B.6}$$

substituting from the above equations in (B.2)

$$\overline{v_{OT}^2} = S_{i_{mag}} Q^2 \int_0^{+\infty} \frac{1 + \left|\frac{f_0}{f}\right|^2}{1 + Q^2\left|\frac{f_0}{f} - \frac{f}{f_0}\right|^2}\, df \tag{B.7}$$

changing the variable to x, where x is given by

$$x = \left|\frac{f_0}{f} - \frac{f}{f_0}\right|$$

then

$$\overline{v_{OT}^2} = S_{i_{mag}} Q^2 f_0 \int_{-\infty}^{+\infty} \frac{1}{1 + Q^2 x^2}\, dx \tag{B.8}$$

and the integration yields

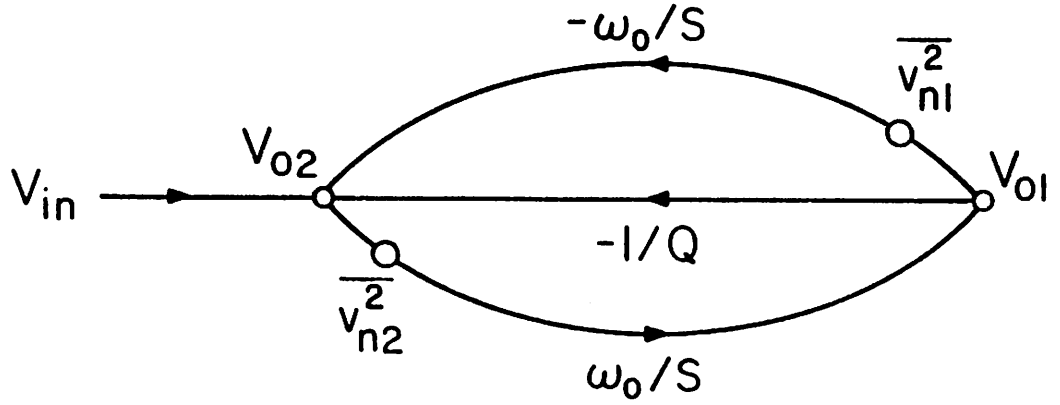


Figure B.1

The flow-graph of a second order bandpass filter with equivalent input referred integrator noise generators.

$$\overline{v_{OT}^2} = S_{i_{mg}} Q^2 f_0 \left| \frac{1}{Q} \tan^{-1} Q x \right|_{x=-\infty}^{+\infty} \tag{B.9}$$

and finally

$$\overline{v_{OT}^2} = S_{i_{mg}} Q f_0 \pi \tag{B.10}$$

B.2. Total Output Noise of a Sixth Order Bandpass Filter

The flow-graph of a sixth order bandpass filter, with the corresponding input referred noise sources is shown in Fig. B.2. To find the transfer functions, the Mason's theorem is used [24]

$$H_k(s) = \frac{P_k \Delta_k}{\Delta} \tag{B.11}$$

where Δ is the graph determinant, P_k is the direct path from node k to the output and Δ_k is the sum of those terms without any constituent loops touching P_k.

The denominator of all the transfer functions is equal to Δ and is found to be

$$\Delta = 1 + \frac{2}{Q}\frac{\omega_0}{s} + \left[3 + 2\gamma^2 + \frac{1}{Q^2}\right]\left[\frac{\omega_0}{s}\right]^2 + \frac{2}{Q}\left[2 + \gamma^2\right]\left[\frac{\omega_0}{s}\right]^3 + \left[3 + 2\gamma^2 + \frac{1}{Q^2}\right]\left[\frac{\omega_0}{s}\right]^4 + \frac{2}{Q}\left[\frac{\omega_0}{s}\right]^5 + \left[\frac{\omega_0}{s}\right]^6 \tag{B.12}$$

and the transfer functions are found to be

$$H_1(j\omega) = \frac{v_{out}}{v_{n_1}} = \frac{\gamma^2 \left[\frac{\omega_0}{s}\right]^3}{\Delta} \tag{B.13}$$

$$H_2(j\omega) = \frac{v_{out}}{v_{n_2}} = \frac{\gamma^2 \left[\frac{\omega_0}{s}\right]^4}{\Delta} \tag{B.14}$$

$$H_3(j\omega) = \frac{v_{out}}{v_{n_3}} = \frac{\gamma^2 \left[\frac{\omega_0}{s}\right]^2 \left\{1 + \frac{1}{Q}\frac{\omega_0}{s} + \left[\frac{\omega_0}{s}\right]^2\right\}}{\Delta} \tag{B.15}$$

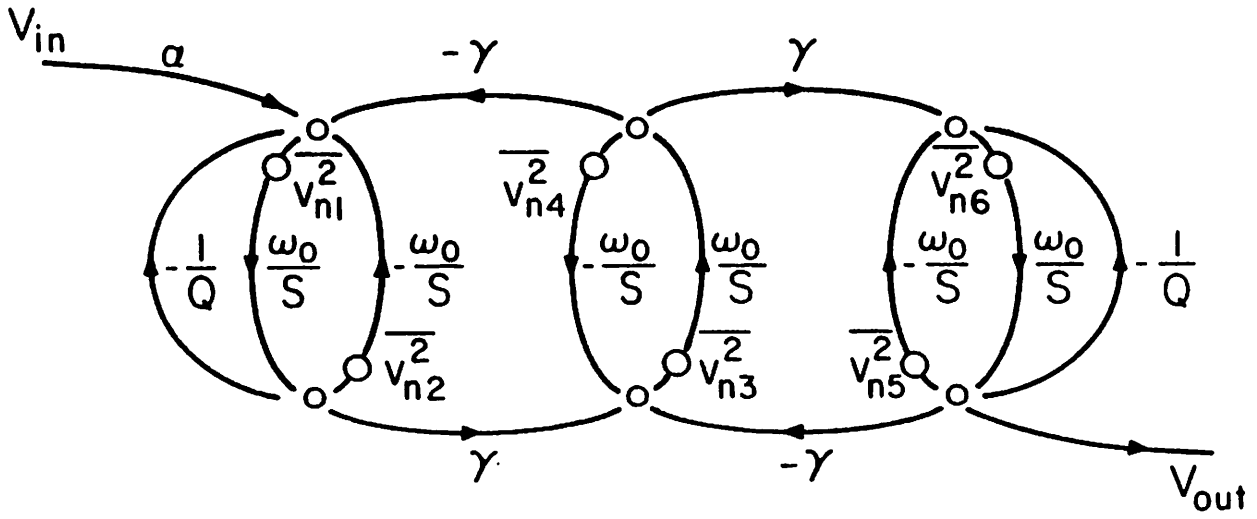


Figure B.2

The flow-graph of a sixth order bandpass filter with equivalent input referred integrator noise generators.

$$H_4(j\omega) = \frac{v_{out}}{v_{n_4}} = \frac{\gamma \left[\frac{\omega_0}{s}\right]^3 \left\{1 + \frac{1}{Q}\frac{\omega_0}{s} + \left[\frac{\omega_0}{s}\right]^2\right\}}{\Delta} \tag{B.16}$$

$$H_5(j\omega) = \frac{v_{out}}{v_{n_5}} \tag{B.17}$$

$$= \frac{\frac{\omega_0}{s}\left\{1 + \frac{1}{Q}\frac{\omega_0}{s} + \left(2+\gamma^2\right)\left[\frac{\omega_0}{s}\right]^2 + \frac{1}{Q}\left[\frac{\omega_0}{s}\right]^3 + \left[\frac{\omega_0}{s}\right]^4\right\}}{\Delta}$$

$$H_6(j\omega) = \frac{v_{out}}{v_{n_6}} \tag{B.18}$$

$$= \frac{\left[\frac{\omega_0}{s}\right]^2 \left\{1 + \frac{1}{Q}\frac{\omega_0}{s} + \left(2+\gamma^2\right)\left[\frac{\omega_0}{s}\right]^2 + \frac{1}{Q}\left[\frac{\omega_0}{s}\right]^3 + \left[\frac{\omega_0}{s}\right]^4\right\}}{\Delta}$$

using the derived transfer functions, it can be shown that

$$\sum_{m=1}^{m=6} |H_m(jf)|^2 = \frac{Q^2\left[1 + \left[\frac{f_0}{f}\right]^2\right]}{1 + Q^2\left[\frac{f_0}{f} - \frac{f}{f_0}\right]^2} \tag{B.19}$$

$$\times \frac{\left[\frac{f_0}{f} - \frac{f}{f_0}\right]^4 + \left[\frac{1}{Q^2} - \gamma^2\right]\left[\frac{f_0}{f} - \frac{f}{f_0}\right]^2 + \gamma^2\left[\frac{1}{Q^2} + 2\gamma^2\right]}{\left[\frac{f_0}{f} - \frac{f}{f_0}\right]^4 + \left[\frac{1}{Q^2} - 4\gamma^2\right]\left[\frac{f_0}{f} - \frac{f}{f_0}\right]^2 + 4\gamma^4}$$

or

$$\sum_{m=1}^{m=6} |H_m(jf)|^2 =$$

$$\frac{Q^2\left|1+\left|\frac{f_0}{f}\right|^2\right|}{1+Q^2\left|\frac{f_0}{f}-\frac{f}{f_0}\right|^2} + \left\{\frac{3\gamma^2Q^2\left|1+\left|\frac{f_0}{f}\right|^2\right|}{1+Q^2\left|\frac{f_0}{f}-\frac{f}{f_0}\right|^2}\right\} \times \left\{\frac{3\left|\frac{f_0}{f}-\frac{f}{f_0}\right|^2-\left|2\gamma^2-\frac{1}{Q^2}\right|}{\left|\frac{f_0}{f}-\frac{f}{f_0}\right|^4+\left|\frac{1}{Q^2}-4\gamma^2\right|\left|\frac{f_0}{f}-\frac{f}{f_0}\right|^2+4\gamma^4}\right\} \tag{B.20}$$

Integrating both sides over the frequency range

$$\int_0^{+\infty}\sum_{m=1}^{m=6}|H_m(jf)|^2\,df =$$

$$\int_0^{+\infty}\left\{\frac{Q^2\left|1+\left|\frac{f_0}{f}\right|^2\right|}{1+Q^2\left|\frac{f_0}{f}-\frac{f}{f_0}\right|^2}\right\}df + \int_0^{+\infty}\left\{\frac{\gamma^2Q^2\left|1+\left|\frac{f_0}{f}\right|^2\right|}{1+Q^2\left|\frac{f_0}{f}-\frac{f}{f_0}\right|^2}\right\} \times \left\{\frac{3\left|\frac{f_0}{f}-\frac{f}{f_0}\right|^2-\left|2\gamma^2-\frac{1}{Q^2}\right|}{\left|\frac{f_0}{f}-\frac{f}{f_0}\right|^4+\left|\frac{1}{Q^2}-4\gamma^2\right|\left|\frac{f_0}{f}-\frac{f}{f_0}\right|^2+4\gamma^4}\right\}df \tag{B.21}$$

Note that the first term on the right side is exactly the same as the equation found for the second order filter, analyzed in the previous section, and is equal to $\left|Q\,f_0\,\pi\right|$. To find the second term let's assume

$$B = \gamma^2 Q^2 \int_0^{+\infty} \left\{ \frac{\left| 1 + \left| \frac{f_0}{f} \right|^2 \right|}{1 + Q^2 \left| \frac{f_0}{f} - \frac{f}{f_0} \right|^2} \right\} \times \left\{ \frac{3 \left| \frac{f_0}{f} - \frac{f}{f_0} \right|^2 - \left| 2\gamma^2 - \frac{1}{Q^2} \right|}{\left| \frac{f_0}{f} - \frac{f}{f_0} \right|^4 + \left| \frac{1}{Q^2} - 4\gamma^2 \right| \left| \frac{f_0}{f} - \frac{f}{f_0} \right|^2 + 4\gamma^4} \right\} df. \tag{B.22}$$

changing the variable according to the following equation

$$x = \left| \frac{f_0}{f} - \frac{f}{f_0} \right|$$

ther.

$$B = \gamma^2 f_0 \int_{-\infty}^{+\infty} \left\{ \frac{1}{x^2 + \frac{1}{Q^2}} \times \frac{3x^2 - \left| 2\gamma^2 - \frac{1}{Q^2} \right|}{x^4 + \left| \frac{1}{Q^2} - 4\gamma^2 \right| x^2 + 4\gamma^4} \right\} dx \tag{B.23}$$

The above equation can be transformed to the form

$$B = f_0 \frac{Q^2}{4\gamma^2} \left| 2\gamma^2 - \frac{1}{Q^2} \right| \times \int_{-\infty}^{+\infty} \frac{\left| \frac{3x^2}{2\gamma^2 - \frac{1}{Q^2}} - 1 \right|}{\frac{Q^2}{4\gamma^4} \left| 2\gamma^2 - \frac{1}{Q^2} \right|^2 x^2 \left| \frac{x^2}{\left| 2\gamma^2 - \frac{1}{Q^2} \right|} - 1 \right|^2 + 1} dx \tag{B.24}$$

changing variable

$$u = \left[2\gamma^2 - \frac{1}{Q^2} \right] \left\{ \frac{x^2}{\left[2\gamma^2 - \frac{1}{Q^2} \right]} - 1 \right\} x$$

Then

$$B = f_0 \frac{Q^2}{2} \int_{-\infty}^{+\infty} \frac{1}{Q^2 u^2 + 1} \, du \tag{B.25}$$

or

$$B = f_0 \frac{Q^2}{2} \left| \frac{1}{Q} \tan^{-1} Q \, u \right|_{u=-\infty}^{+\infty} \tag{B.26}$$

yields to

$$B = f_0 Q \frac{\pi}{2} \tag{B.27}$$

Adding the above value to the value found from the integration of the first term from equation (B.21)

$$\int_0^{+\infty} \sum_{m=1}^{m=6} \left| H_m (jf) \right|^2 df = f_0 Q \frac{3\pi}{2} \tag{B.28}$$

and substituting in equation (B.2)

$$\overline{v_{OT}^2} = S_{i_{mg}} f_0 Q \frac{3\pi}{2} \tag{B.29}$$

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