INSTABILITY AND GEOMETRIC TRANSIENCE OF THE ALOHA PROTOCOL

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Instability and Geometric Transience of the Aloha Protocol[†]

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ABSTRACT

In this paper, we give a simple probabilistic proof to show that the discrete time Markov chain underlying the slotted uncontrolled Aloha protocol is geometrically transient. Let P be the $(\infty \times \infty)$ transition matrix of this Markov chain. Let P_n denote the northwest $(n \times n)$ corner truncation of P and β_n its largest eigenvalue. We establish that, as a consequence of geometric transience, $\beta = \lim \beta_n$, as $n \to \infty$, exists and that $0 < \beta < 1$. Note that the largest eigenvalue of P equals 1. We propose $1/(1-\beta)$ as a performance measure which we show to be the limit of certain expected exit times.

September 5, 1986

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APPENDIX C: SPICE IMPLEMENTATION OF THE BSIM SUBSTRATE CURRENT AND DEGRADATION MODELS

1. Introduction

The BSIM substrate current model has been implemented into SPICE3 and the BSIM version of SPICE2G.6. The analysis is carried out in a pre- and post-processor fashion so that the actual SPICE code remains untouched. Because of this fact, simulator operation is independent of the exact drain-current model implemented in SPICE, and minimal setup time is required.

In addition to the substrate current model, a simple parametric device degradation model has been added to calculate device lifetime in a circuit environment. With this addition, the circuit designer can isolate areas within his circuit susceptible to adverse hot-electron and degradation effects.

The following sections will introduce the degradation model, summarize the basic operation of the pre- and post-processors, and offer a guide to users wanting to implement these models in their circuit simulations.

2. Degradation Model

2.1 Basic Equations

Device degradation is typically measured by the amount of threshold voltage shift (ΔV_{th}) that occurs. In DC static stressing, the device lifetime can be modelled by two basic equations dependent on I_{ds} , I_{bs} , and other parameters [1]:

$$\Delta V_{th} = At^n \tag{1.1}$$

$$\tau = WBI_{bs}^{-m} I_{ds}^{m-1} \tag{1.2}$$

$$m = \frac{\phi_{it}}{\phi_i}$$

where n and B are extracted parameters (B being a constant dependent on device processing technology), τ is the device lifetime, and $q\phi_i$ and $q\phi_{it}$ are the critical energies required for impact ionization and the creation of interface traps, respectively. Typical log - log plots of ΔV_{th} versus time and τ versus I_{bs} are shown in Figs. C1 and C2. These equations can then be combined with numerical calculations to find device lifetime.

2.2 Analytical Analysis

Using a quasi-static analysis, equations (1.1) and (1.2) can be extended to model the dynamic stressing behavior in a circuit for which the substrate current of a device is a function of time. Let $\Delta V_{tho} = \Delta V_{th}\,|_{t=\tau}$ be the threshold voltage shift defined at device failure. By solving for A in equation (1.1) using (1.2), we get:

$$\Delta V_{tho} = A\tau^n = A[WBI_{bs}^{-m} I_{ds}^{m-1}]^n$$

$$A = \Delta V_{tho}[WBI_{bs}^{-m} I_{ds}^{m-1}]^{-n}$$

Thus equation (1.1) becomes

$$\Delta V_{th} = \Delta V_{tho}(WB)^{-n} I_{bs}^{mn} I_{ds}^{n(1-m)} t^n$$

or

$$\Delta V_{th}^{\frac{1}{n}} = \Delta V_{tho}^{\frac{1}{n}} (WB)^{-1} I_{bs}^{m} I_{ds}^{(1-m)} t \tag{1.3}$$

Since $\Delta V_{th}^{\frac{1}{n}}$ is a linear function of time, this quantity can simply be summed over the time period of the SPICE analysis. If $t_1, \ldots, t_P$ are the individual time points of SPICE, then

$$\Delta V_{th\,(tot)}^{\frac{1}{n}} = \Delta V_{th}(t_1)^{\frac{1}{n}} + \cdots + \Delta V_{th}(t_P)^{\frac{1}{n}}$$

Moreover, to find the device lifetime assuming a periodic signal, a simple linear extrapolation in terms of $\Delta V_{th}^{\frac{1}{n}}$ is all that is necessary. The number of time intervals of the SPICE analysis needed so that $\Delta V_{th} = \Delta V_{tho}$ is simply

$$N = [\frac{\Delta V_{tho}}{\Delta V_{th\,(tot)}}]^{\frac{1}{n}}$$

Thus, if the length of the SPICE analysis is $t_P = T$ and is equal to the period of the signal, the lifetime is found from

$$\tau = NT$$

or

$$\tau = T[\frac{\Delta V_{tho}}{\Delta V_{th\,(tot)}}]^{\frac{1}{n}} \tag{1.4}$$

2.3 Additional Parameters

Additional parameters needed for the process file are summarized as follows:

(1) B: an extracted process dependent parameter which is the intercept of the log τ versus log I_{bs} curve (Fig. C2).

(2) n: slope of logΔV_{th} versus log t curve (Fig. C1). This generally ranges from 0.5 to 0.75 depending on the mechanism limiting interface trap density formation.

(3) m: the ratio of the trap energy and impact ionization energy $\frac{\phi_{it}}{\phi_i}$ which is approximately the slope of the log τ versus log I_{bs} curve (Fig. C2). Typically, m is equal to 2.9 [1].

(4) ΔV_{tho}: threshold voltage shift defined at device failure.

These parameters should be appended to the process file directly after the substrate

current parameters in two rows and in the order mentioned above (B, n, m, ΔV_{tho}). Fig. C3 shows the location of all BSIM parameters in the process file for proper SPICE read-in.

3. Using the Pre- and Post-Processor

The following new commands have been added for substrate current and degradation analysis:

.PRINT ISUB(MXXX) ISUB(MYYY) ... <(MIN,MAX)>

.PRINT ISUB(SXXX) ISUB(SYYY) ... <(MIN,MAX)>

.PLOT ISUB(MXXX) ISUB(MYYY) ... <(MIN,MAX)>

.PLOT ISUB(SXXX) ISUB(SYYY) ... <(MIN,MAX)>

These cards are used to either print or plot out the substrate current. SXXX is used to follow SPICE2 convention, while MXXX is used for SPICE3. MIN and MAX are optional parameters specifiying the minimum and maximum substrate current plotted.

.ISUBWIDTH=XX

This card controls the width of the substrate current output printout. This is independent of the usual .WIDTH or .OPTIONS WIDTH card used in SPICE. In SPICE3, all non-substrate current analysis printout is outputted in 90 column format, regardless of the .OPTIONS WIDTH card. This was done to insure proper voltage read-in when none of the four nodes of the specified transistor are grounded.

.PROCESS processname FILENAME=processfilename

This card is new only for SPICE3. The format is identical to that already implemented in SPICE2. It is important to realize that ".MODEL" cards are no longer necessary for SPICE3, but that a ".PROCESS" card is now mandatory.

In an UNIX environment, the following should be executed for proper simulator operation:

presub -x deck | spice | postsub > outfile

where x is either "2" or "3" depending on whether SPICE2 or SPICE3 is used, "deck" is the input deck file, and "outfile" is the output file desired. If no "-x" option is specified, the simulator defaults to SPICE2.

Figs. C4 and C5 illustrate sample SPICE2 and SPICE3 input decks respectively for a CMOS EEPROM sense amplifier shown in Fig. C6. M1 and M7 are EEPROM reference and memory cells, and M3 and M5 are the sense amplifier's NMOS devices of which substrate current simulations are requested. The essential difference between the two input decks is the BSIM transistor designations (SXXX for SPICE2, MXXX for SPICE3). Fig. C7 shows the resulting output for SPICE2 with a 5 volt input pulse of 4ns rise and fall time, and 25ns pulse width applied at $V_{in} = V(6)$ at $t = 0$ns. Output for SPICE3 is virutally identical to the one shown here.

Work is presently being done to port the simulator to the VMS operating system and will be available in the near future.

4. More About The Processors

To calculate the substrate current, appropriate node voltages for the specified transistors are printed out, and these voltages are read in by the post-processor to do the necessary calculations. Thus, the basic need for the pre-processor is to add the appropriate ".PRINT" cards to the input deck. Besides this basic task, the operation of the simulators differ somewhat for SPICE2 and SPICE3. This was necessary because of the fact that SPICE2 reads in the process file created by the BSIM extraction program directly, while presently SPICE3 needs ".MODEL" cards with all parameters appended to the input deck.

The configuration was designed to retain as much commonality as possible between the two schemes (see Figs. C8 and C9). In both, an input deck and a process file must be present for read-in, the input deck is filtered of all substrate current command cards, and substrate current output is added to the SPICE output file in similar fashion. A "rawsub" file is created for communication between the two processors, and a "rawmodel" file is made for storing model parameters for housekeeping purposes. The differences can be seen from the two figures and are listed below:

(1) In SPICE2, a "RAWPROC" file is created which is identical to the original process file except that the substrate current and degradation parameters are commented out for compatibility with present SPICE2 code. The input deck's ".PROCESS" card is modified accordingly by the pre-processor to read in "RAWPROC". Otherwise, the input deck is unaltered.

(2) In SPICE3, no "RAWPROC" file is created, but the "rawmodel" file is appended to the input deck with the substrate current parameters commented out. Because appending of the model parameters is done automatically, a ".PROCESS" card has been introduced in similarity with present SPICE2 convention as mentioned in the previous section.

REFERENCE

[1] C. Hu, S. Tam, F-C Hsu, P.K. Ko, T.Y. Chan, K.W. Terrill, "Hot-Electron-Induced MOSFET Degradation - Model, Monitor, Improvement," IEEE Trans. Electron. Devices, Vol. ED-32, pp. 375-385, February 1985.

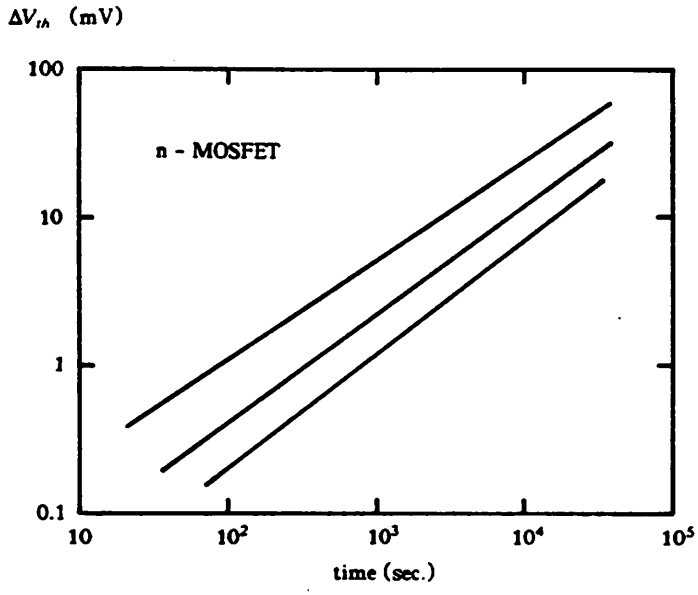

Fig. C1 Typical log - log plots of ΔV_{th} versus time for various device technologies (from Hu et al [1]).

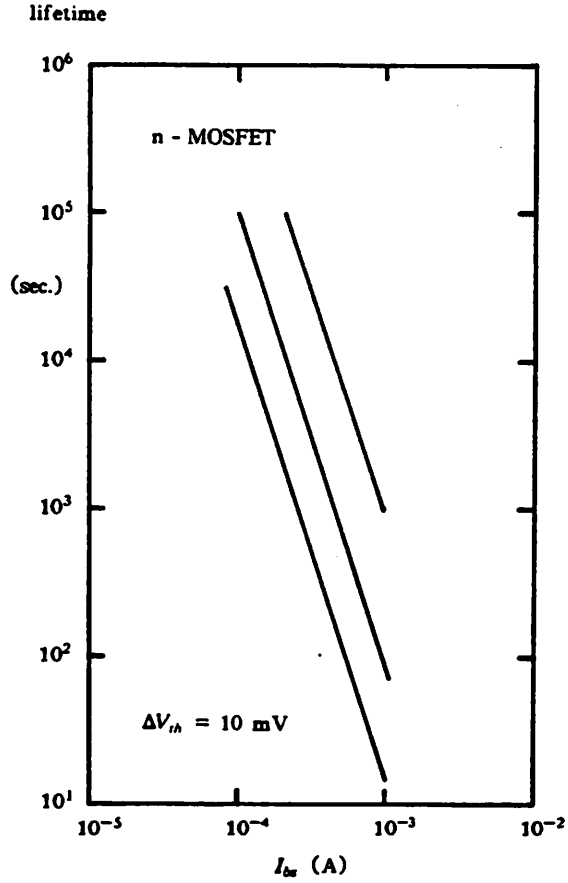

Fig. C2 Typical log - log plots of device lifetime τ versus I_{bs} for various device technologies (from Hu et al [1]).

	Name	L sens. factor	W sens. factor	Units of basic parameter
1	V_{FB} (VFB)	V_{FBl} (LVFB)	V_{FBw} (WVFB)	V
2	ϕ_S (PHI)	ϕ_{Sl} (LPHI)	ϕ_{Sw} (WPHI)	V
3	K_1 (K1)	K_{1l} (LK1)	K_{1w} (WK1)	$V^{1/2}$
4	K_2 (K2)	K_{2l} (LK2)	K_{2w} (WK2)	-
5	η_0 (ETA)	η_{0l} (LETA)	η_{0w} (WETA)	-
6	μ_Z (MUZ)	δ_l (DL)	δ_w (DW)	cm^2/V-s, μm, μm
7	U_{0Z} (U0)	U_{0Zl} (LU0)	U_{0Zw} (WU0)	V^{-1}
8	U_{1Z} (U1)	U_{1Zl} (LU1)	U_{1Zw} (WU1)	μm V^{-1}
9	μ_{ZB} (X2MZ)	μ_{ZBl} (LX2MZ)	μ_{ZBw} (WX2MZ)	cm^2/V^2-s
10	η_B (X2E)	η_{Bl} (LX2E)	η_{Bw} (WX2E)	V^{-1}
11	η_D (X3E)	η_{Dl} (LX3E)	η_{Dw} (WX3E)	V^{-1}
12	U_{0B} (X2U0)	U_{0Bl} (LX2U0)	U_{0Bw} (WX2U0)	V^{-2}
13	U_{1B} (X2U1)	U_{1Bl} (LX2U1)	U_{1Bw} (WX2U1)	μm V^{-2}
14	μ_S (MUS)	μ_{Sl} (LMS)	μ_{Sw} (WMS)	cm^2/V^2-s
15	μ_{SB} (X2MS)	μ_{SBl} (LX2MS)	μ_{SBw} (WX2MS)	cm^2/V^2-s
16	μ_{SD} (X3MS)	μ_{SDl} (LX3MS)	μ_{SDw} (WX3MS)	cm^2/V^2-s
17	U_{1D} (X3U1)	U_{1Dl} (LX3U1)	U_{1Dw} (WX3U1)	μm V^{-2}
18	T_{ox} (TOX)	T_{emp} (TEMP)	V_{dd} (VDD)	μm, $^\circ C$, V
19	CGDO	CGSO	CGBO	F/m
20	XPART	DUM1	DUM2	-
21	N0	LN0	WN0	-
22	NB	LNB	WNB	-
23	ND	LND	WND	-
24	$E_{crit\,0}$ (ECRIT0)	$E_{crit\,0l}$ (LECRIT0)	$E_{crit\,0w}$ (WECRIT0)	V/cm
25	E_{critg} (ECRITG)	E_{critgl} (LECRITG)	E_{critgw} (WECRITG)	1/cm
26	E_{critb} (ECRITB)	E_{critbl} (LECRITB)	E_{critbw} (WECRITB)	1/cm
27	$l_{c\,0}$ (LC0)	$l_{c\,0l}$ (LLC0)	$l_{c\,0w}$ (WLC0)	$\mu m^{1/2}$
28	$l_{c\,1}$ (LC1)	$l_{c\,1l}$ (LLC1)	$l_{c\,1w}$ (WLC1)	$\mu m^{1/2} - V$
29	$l_{c\,2}$ (LC2)	$l_{c\,2l}$ (LLC2)	$l_{c\,2w}$ (WLC2)	$\mu m^{1/2} - V^{-1}$
30	$l_{c\,3}$ (LC3)	$l_{c\,3l}$ (LLC3)	$l_{c\,3w}$ (WLC3)	$\mu m^{1/2}$
31	$l_{c\,4}$ (LC4)	$l_{c\,4l}$ (LLC4)	$l_{c\,4w}$ (WLC4)	$\mu m^{1/2} - V$
32	$l_{c\,5}$ (LC5)	$l_{c\,5l}$ (LLC5)	$l_{c\,5w}$ (WLC5)	$\mu m^{1/2} - V^2$
33	$l_{c\,6}$ (LC6)	$l_{c\,6l}$ (LLC6)	$l_{c\,6w}$ (WLC6)	$\mu m^{1/2}$
34	$l_{c\,7}$ (LC7)	$l_{c\,7l}$ (LLC7)	$l_{c\,7w}$ (WLC7)	$\mu m^{1/2} - V$
35	B	n	m	A-sec/μm , -, -
36	ΔV_{tho} (DVTHO)	DUM3	DUM4	V, -, -

Fig. C3 BSIM process file format.

```
SIMPLE CMOS SENSE AMPLIFIER
s1 2 5 0 0 PC1_nm1_du1 w=3u l=2u
s2 2 2 5 5 PC1_pm1_du1 w=140u l=2u
s3 3 2 1 0 PC1_nm1_du1 w=20u l=2u
s4 3 2 5 5 PC1_pm1_du1 w=60u l=2u
s5 4 1 0 0 PC1_nm1_du1 w=5u l=2u
s6 4 3 5 5 PC1_pm1_du1 w=10u l=2u
s7 1 6 0 0 PC1_nm1_du1 w=3u l=2u
vdd 5 0 5 dc
vin 6 0 pulse(0,5,0ns,4ns,4ns,25ns,58ns)
.process PC1 filename=PF.SUB
.plot isub(s3) isub(s5)
c1 1 0 2pf
c2 4 0 0.2pf
.tran 1ns 58ns
.isubwidth=80
.width in=80 out=80
.end
```

Fig. C4 Sample SPICE2 input deck.

```
SIMPLE CMOS SENSE AMPLIFIER
m1 2 5 0 0 PC1_nm1_du1 w=3u l=2u
m2 2 2 5 5 PC1_pm1_du1 w=140u l=2u
m3 3 2 1 0 PC1_nm1_du1 w=20u l=2u
m4 3 2 5 5 PC1_pm1_du1 w=60u l=2u
m5 4 1 0 0 PC1_nm1_du1 w=5u l=2u
m6 4 3 5 5 PC1_pm1_du1 w=10u l=2u
m7 1 6 0 0 PC1_nm1_du1 w=3u l=2u
vdd 5 0 5 dc
vin 6 0 pulse(0,5,0ns,4ns,4ns,25ns,58ns)
.process PC1 filename=PF.SUB
.plot isub(m3) isub(m5)
c1 1 0 2pf
c2 4 0 0.2pf
.tran 1ns 58ns
.isubwidth=80
.end
```

Fig. C5 Sample SPICE3 input deck.

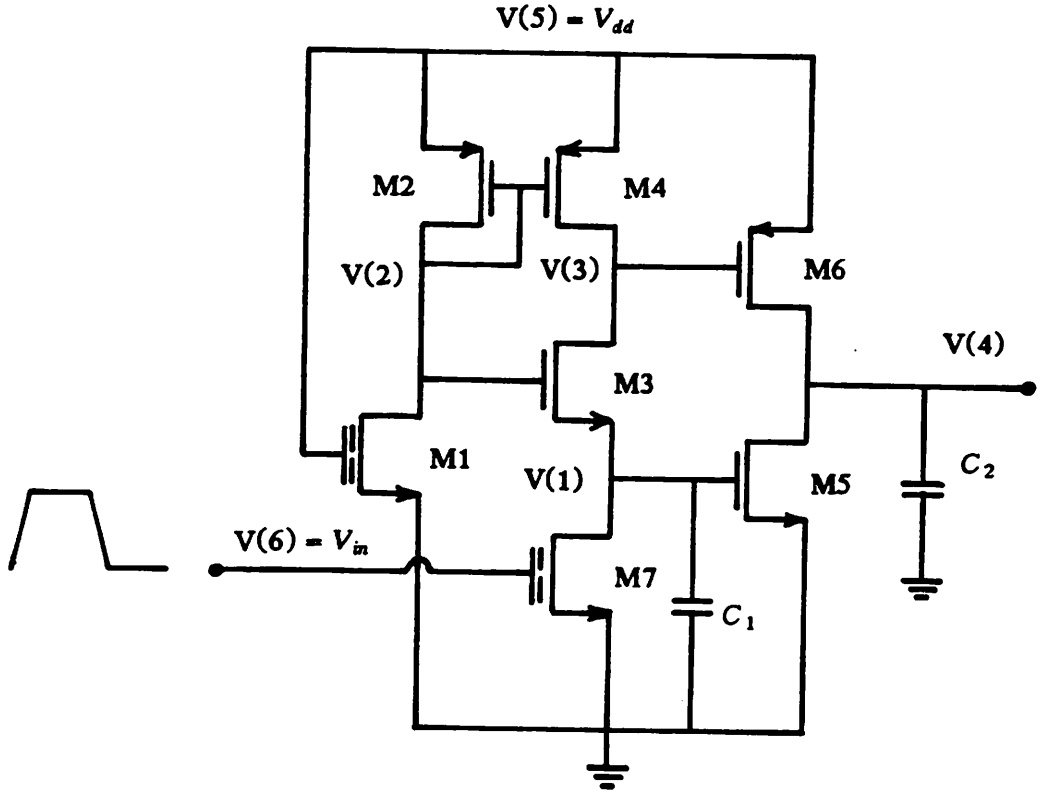

Fig. C6 CMOS sense amplifier circuit used for sample SPICE simulations.

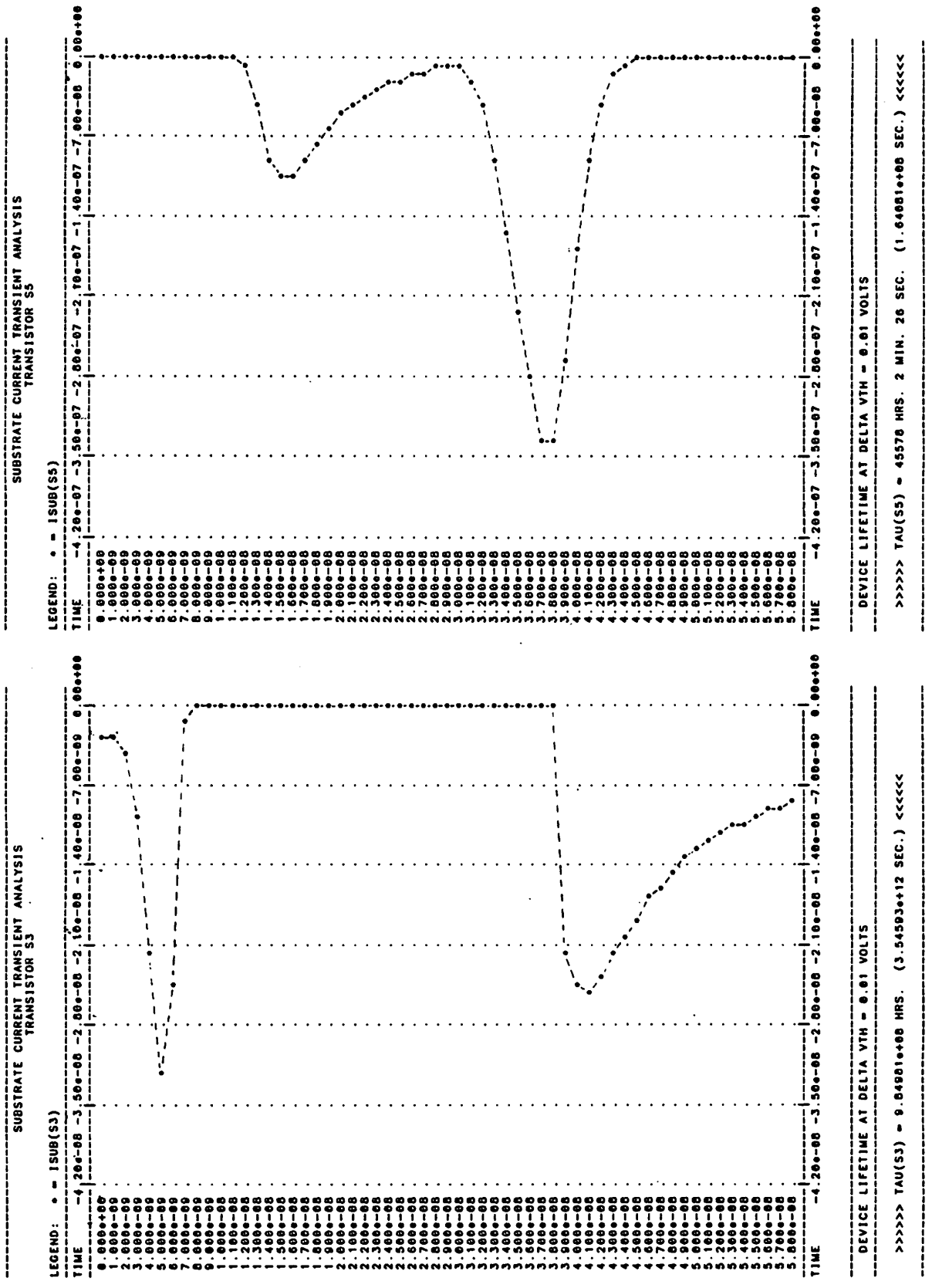

Fig. C7 SPICE2 output file.

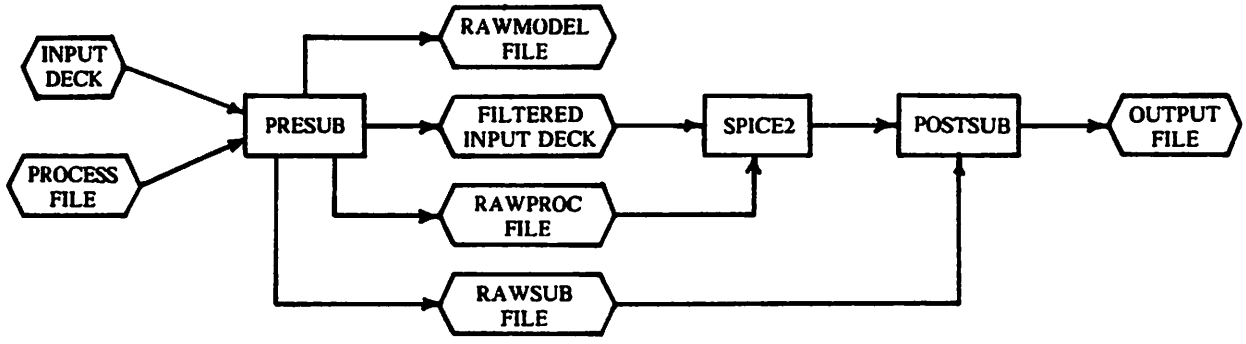

Fig. C8 SPICE2 processor configuration.

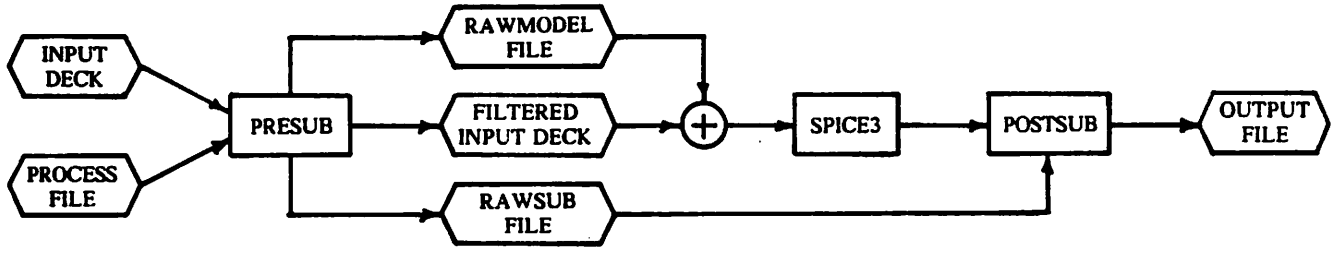

Fig. C9 SPICE3 processor configuration.