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SPICE3 VERSION 3C1 USERS GUIDE

by

Thomas L. Quarles

Memorandum No. UCB/ERL M89/46

24 April 1989

THE SPICE3 IMPLEMENTATION GUIDE

by

Thomas L. Quarles

Memorandum No. UCB/ERL M89/44

24 April 1989

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
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TITLE PAGE

Preface

This memo is one of six containing the text of the Ph.D. dissertation *Analysis of Performance and Convergence Issues for Circuit Simulation.* The dissertation itself is available as UCB/ERL Memorandum M89/42. The other appendices are available as:

Memo number	Title
UCB/ERL M89/43	The Front End to Simulator Interface
UCB/ERL M89/44	The SPICE3 Implementation Guide
UCB/ERL M89/45	Adding Devices to SPICE3
UCB/ERL M89/47	Benchmark Circuits: Results for SPICE3

This memo was originally Appendix F of the dissertation and details the language used to describe circuits and analyses to SPICE3. This memo was last updated to reflect the language at the time SPICE3, version 3C1 was released.

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CHAPTER 1

SPICE2 compatible input language

SPICE3 Version 3C1 User's Guide

April 24, 1989

T. Quarles
A.R.Newton, D.O.Pederson, A.Sangiovanni-Vincentelli

Department of Electrical Engineering and Computer Sciences
University of California
Berkeley, Ca., 94720

Please Note

This is the third major release of SPICE3. This release incorporates many new features not available in SPICE3B, as well as some performance improvements. We believe that all of the features described here are fully functional; however, since the development of SPICE and its algorithms is ongoing at Berkeley, not all of the intended capabilities of the program have been implemented in full yet. Please mail any reports of suspected bugs in the program or suggested enhancements to the program to:

EECS/ERL Industrial Support Office
479 Cory Hall
U.C. Berkeley
Berkeley, Ca. 94720

or by electronic mail to:

spice@cad.BERKELEY.EDU (Internet)
ucbvax!ucbcad!spice (UUCPnet)

Please include input to the program, output, suggestions as to where the problem may be, and if possible, a suggested fix!

SPICE is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analyses. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, transmission lines, switches, and the five most common semiconductor devices: diodes, BJTs, JFETs, MESFETs, and MOSFETs.

The SPICE3 version is based directly on SPICE 2G.6. While SPICE3 is being developed to include new features, it will continue to support those capabilities and models which remain in extensive use in the SPICE2 program.

SPICE has built-in models for the semiconductor devices, and the user need specify only the pertinent model parameter values. The model for the BJT is based on the integral charge model of Gummel and Poon; however, if the Gummel- Poon parameters are not specified, the model reduces to the simpler Ebers-Moll model. In either case, charge storage effects, ohmic resistances, and a current-dependent output conductance may be included. The diode model can be used for either junction diodes or Schottky barrier diodes. The JFET model is based on the FET model of Shichman and Hodges. Four MOSFET models are implemented: MOS1 is described by a square-law I-V characteristic, MOS2[1] is an analytical model, while MOS3[1] is a semi-empirical model, and MOS4[2, 3] is the new BSIM (Berkeley Short-channel IGFET Model). MOS2, MOS3, and MOS4 include second-order effects such as channel length modulation, subthreshold conduction, scattering limited velocity saturation, small-size effects, and charge-controlled capacitances.

1.1. TYPES OF ANALYSIS

1.1.1. DC Analysis

The dc analysis portion of SPICE determines the dc operating point of the circuit with inductors shorted and capacitors opened. A dc analysis is automatically performed prior to a transient analysis to determine the transient initial conditions, and prior to an ac small-signal analysis to determine the linearized, small-signal models for nonlinear devices. If requested, the dc small-signal value of a transfer function (ratio of output variable to input source), input resistance, and output resistance will also be computed as a part of the dc solution. The dc analysis can also be used to generate dc transfer curves: a specified independent voltage or current source is stepped over a user-specified range and

the dc output variables are stored for each sequential source value. The dc analysis options are specified on the .DC, .TF, and .OP control cards.

1.1.2. AC Small-Signal Analysis

The ac small-signal portion of SPICE computes the ac output variables as a function of frequency. The program first computes the dc operating point of the circuit and determines linearized, small-signal models for all of the nonlinear devices in the circuit. The resultant linear circuit is then analyzed over a user-specified range of frequencies. The desired output of an ac small- signal analysis is usually a transfer function (voltage gain, transimpedance, etc). If the circuit has only one ac input, it is convenient to set that input to unity and zero phase, so that output variables have the same value as the transfer function of the output variable with respect to the input.

1.1.3. Transient Analysis

The transient analysis portion of SPICE computes the transient output variables as a function of time over a user-specified time interval. The initial conditions are automatically determined by a dc analysis. All sources which are not time dependent (for example, power supplies) are set to their dc value. The transient time interval is specified on a .TRAN control line.

1.1.4. Pole-Zero Analysis

The pole-zero analysis portion of SPICE computes the poles and/or zeros in the small-signal ac transfer function. The program first computes the dc operating point and then determines the linearized, small-signal models for all the nonlinear devices in the circuit. This circuit is then used to find the poles and zeros.

Two types of transfer functions are allowed : one of the form (output voltage)/(input voltage) and the other of the form (output voltage)/(input current). These two types of transfer functions cover

all the cases and one can find the poles/zeros of functions like input/output impedance and voltage gain. The input and output ports are specified as two pairs of nodes.

The pole-zero analysis works with resistors, capacitors, inductors, linear-controlled sources, independent sources, BJTs, MOSFETs, JFETs and diodes. Transmission lines are not supported.

1.1.5. Analysis at Different Temperatures

All input data for SPICE is assumed to have been measured at a nominal temperature of 27°C, which can be changed by use the the TNOM paramèter on the .OPTION control line. This value can further be overridden for any device which models temperature effects by specifying the TNOM parameter on the model itself. The circuit simulation will also be performed at a temperature of 27°C, unless overridden by a TEMP parameter on the .OPTION control line. Individual instances may further override the circuit temperature through the specification of a TEMP parameter on the instance.

Temperature dependent support is provided for resistors, diodes, JFET's, BJT's, and level 1, 2, and 3 MOSFET's. BSIM (level 4) MOSFET's have an alternate temperature dependency scheme which adjusts all of the model parameters before input to SPICE. For details of the BSIM temperature adjustment, see [1] or [2].

Temperature appears explicitly in the exponential terms of the BJT and diode model equations. In addition, saturation currents have a built-in temperature dependence. The temperature dependence of the saturation current in the BJT models is determined by:

IS(T1) = IS(T0)*((T1/T0)**XTI)*exp(q*EG*(T1-T0)/(k*T1*T0))

where k is Boltzmann's constant, q is the electronic charge, EG is the energy gap which is a model parameter, and XTI is the saturation current temperature exponent (also a model parameter, and usually equal to 3). The temperature dependence of forward and reverse beta is according to the formula:

beta(T1)=beta(T0)*(T1/T0)**XTB

where T1 and T0 are in degrees Kelvin, and XTB is a user-supplied model parameter. Temperature effects on beta are carried out by appropriate adjustment to the values of BF, ISE, BR, and ISC. Temperature dependence of the saturation current in the junction diode model is determined by:

IS(T1) = IS(T0)*((T1/T0)**(XTI/N))*exp(q*EG*(T1-T0)/(k*N*T1*T0))

where N is the emission coefficient, which is a model parameter, and the other symbols have the same meaning as above. Note that for Schottky barrier diodes, the value of the saturation current temperature exponent, XTI, is usually 2.

Temperature appears explicitly in the value of junction potential, PHI, for all the device models. The temperature dependence is determined by:

PHI(TEMP) = k*TEMP/q*log(Na*Nd/Ni(TEMP)**2)

where k is Boltzmann's constant, q is the electronic charge, Na is the acceptor impurity density, Nd is the donor impurity density, Ni is the intrinsic concentration, and EG is the energy gap.

Temperature appears explicitly in the value of surface mobility, UO, for the MOSFET model. The temperature dependence is determined by:

UO(TEMP) = UO(TNOM)/(TEMP/TNOM)**(1.5)

The effects of temperature on resistors is modeled by the formula:

value(TEMP) = value(TNOM)*(1+TC1*(TEMP-TNOM)+TC2*(TEMP-TNOM)**2))

where TEMP is the circuit temperature, TNOM is the nominal temperature, and TC1 and TC2 are the first- and second-order temperature coefficients.

[1] Soyeon Park, "Analysis and SPICE implementation of High Temperature Effects on MOSFET", Master's thesis, U.C. Berkeley, December 1986.

[2] Clement Szeto, "Simulator of Temperature Effects in MOSFETs (STEIM)", Master's thesis, U.C. Berkeley, May 1988.

1.2. CONVERGENCE

Both dc and transient solutions are obtained by an iterative process which is terminated when both of the following conditions hold:

1) The nonlinear branch currents converge to within a tolerance of 0.1 percent or 1 picoamp (1.0E-12 Amp), whichever is larger.

2) The node voltages converge to within a tolerance of 0.1 percent or 1 microvolt (1.0E-6 Volt), whichever is larger.

Although the algorithm used in SPICE has been found to be very reliable, in some cases it will fail to converge to a solution. When this failure occurs, the program will terminate the job.

Failure to converge in dc analysis is usually due to an error in specifying circuit connections, element values, or model parameter values. Regenerative switching circuits or circuits with positive feedback probably will not converge in the dc analysis unless the OFF option is used for some of the devices in the feedback path, or the .NODESET card is used to force the circuit to converge to the desired state.

1.3. INPUT FORMAT

The input format for SPICE is of the free format type. Fields on a card are separated by one or more blanks, a comma, an equal (=) sign, or a left or right parenthesis; extra spaces are ignored. A card may be continued by entering a + (plus) in column 1 of the following card; SPICE continues reading beginning with column 2.

A name field must begin with a letter (A through Z) and cannot contain any delimiters.

A number field may be an integer field (12, -44), a floating point field (3.14159), either an integer or floating point number followed by an integer exponent (1E-14, 2.65E3), or either an integer

or a floating point number followed by one of the following scale factors:

T=1E12	G=1E9	MEG=1E6	K=1E3	MIL=25.4E-6
M=1E-3	U=1E-6	N=1E-9	P=1E-12	F=1E-15

Letters immediately following a number that are not scale factors are ignored, and letters immediately following a scale factor are ignored. Hence, 10, 10V, 10VOLTS, and 10HZ all represent the same number, and M, MA, MSEC, and MMHOS all represent the same scale factor. Note that 1000, 1000.0, 1000HZ, 1E3, 1.0E3, 1KHZ, and 1K all represent the same number.

1.4. CIRCUIT DESCRIPTION

The circuit to be analyzed is described to SPICE by a set of element cards, which define the circuit topology and element values, and a set of control cards, which define the model parameters and the run controls. The first card in the input deck must be a title card, and the last card must be a .END card. The order of the remaining cards is arbitrary (except, of course, that continuation cards must immediately follow the card being continued).

Each element in the circuit is specified by an element card that contains the element name, the circuit nodes to which the element is connected, and the values of the parameters that determine the electrical characteristics of the element. The first letter of the element name specifies the element type. The format for the SPICE element types is given in what follows. The strings XXXXXXX, YYYYYYY, and ZZZZZZZ denote arbitrary alphanumeric strings. For example, a resistor name must begin with the letter R and can contain one or more characters. Hence, R, R1, RSE, ROUT, and R3AC2ZY are valid resistor names.

Data fields that are enclosed in less than and greater than signs '< >' are optional. All indicated punctuation (parentheses, equal signs, etc.) is optional and merely indicate the presence of any delimiter. A consistent style such as that shown here will make the input easier to understand. With respect

to branch voltages and currents, SPICE uniformly uses the associated reference convention (current flows in the direction of voltage drop).

Nodes names may be arbitrary character strings. The datum (ground) node must be named '0'. Note the difference in SPICE3 where the nodes are treated as character strings and not evaluated as numbers, thus '0' and '00' are distinct nodes in SPICE3 but not in SPICE2. The circuit cannot contain a loop of voltage sources and/or inductors and cannot contain a cutset of current sources and/or capacitors. Each node in the circuit must have a dc path to ground. Every node must have at least two connections except for transmission line nodes (to permit unterminated transmission lines) and MOSFET substrate nodes (which have two internal connections anyway).

1.5. TITLE CARD, COMMENT CARDS AND .END CARD

1.5.1. Title Card

Examples:

```
POWER AMPLIFIER CIRCUIT
TEST OF CAM CELL
```

This card must be the first card in the input deck. Its contents are printed verbatim as the heading for each section of output.

1.5.2. .END Card

Examples:

```
.END
```

This card must always be the last card in the input deck. Note that the period is an integral part of the name.

1.5.3. Comment Card

General Form:

* <any comment>

Examples:

```
* RF=1K      GAIN SHOULD BE 100
* MAY THE FORCE BE WITH MY CIRCUIT
```

The asterisk in the first column indicates that this card is a comment card. Comment cards may be placed anywhere in the circuit description. Note that SPICE3 will also consider any line with leading white space to be a comment.

1.6. ELEMENT CARDS

1.6.1. Resistors

General form:

RXXXXXXX N1 N2 VALUE

Examples:

```
R1 1 2 100
RC1 12 17 1K
```

N1 and N2 are the two element nodes. VALUE is the resistance (in ohms) and may be positive or negative but not zero.

1.6.2. Capacitors and Inductors

General form:

CXXXXXXX N+ N- VALUE <IC=INCOND>

LYYYYYYY N+ N- VALUE <IC=INCOND>

Examples:

```
CBYP 13 0 1UF
COSC 17 23 10U IC=3V
LLINK 42 69 1UH
LSHUNT 23 51 10U IC=15.7MA
```

N+ and N- are the positive and negative element nodes, respectively. VALUE is the capacitance in Farads or the inductance in Henries.

For the capacitor, the (optional) initial condition is the initial (time-zero) value of capacitor voltage (in Volts). For the inductor, the (optional) initial condition is the initial (time-zero) value of inductor current (in Amps) that flows from N+, through the inductor, to N-. Note that the initial conditions (if any) apply 'only' if the UIC option is specified on the .TRAN card.

1.6.3. Coupled (Mutual) Inductors

General form:

KXXXXXXX LYYYYYYY LZZZZZZZ VALUE

Examples:

```
K43 LAA LBB 0.999
KXFRMR L1 L2 0.87
```

LYYYYYYY and LZZZZZZZ are the names of the two coupled inductors, and VALUE is the coefficient of coupling, K, which must be greater than 0 and less than or equal to 1. Using the 'dot' convention, place a 'dot' on the first node of each inductor.

1.6.4. Transmission Lines (Lossless)

General form:

```
TXXXXXXX N1 N2 N3 N4 Z0=VALUE <TD=VALUE> <F=FREQ <NL=NRMLEN>>
+                <IC=V1, I1, V2, I2>
```

Examples:

T1 1 0 2 0 Z0=50 TD=10NS

N1 and N2 are the nodes at port 1; N3 and N4 are the nodes at port 2. Z0 is the characteristic impedance. The length of the line may be expressed in either of two forms. The transmission delay, TD, may be specified directly (as TD=10ns, for example). Alternatively, a frequency F may be given, together with NL, the normalized electrical length of the transmission line with respect to the wavelength in the line at the frequency F. If a frequency is specified but NL is omitted, 0.25 is assumed (that is, the frequency is assumed to be the quarter-wave frequency). Note that although both forms for expressing the line length are indicated as optional, one of the two must be specified.

Note that this element models only one propagating mode. If all four nodes are distinct in the actual circuit, then two modes may be excited. To simulate such a situation, two transmission-line elements are required. (see the example in the final section of this chapter for further clarification.)

The (optional) initial condition specification consists of the voltage and current at each of the transmission line ports. Note that the initial conditions (if any) apply 'only' if the UIC option is specified on the .TRAN card.

1.6.5. Linear Dependent Sources

SPICE allows circuits to contain linear dependent sources characterized by any of the four equations

i=g*v v=e*v i=f*i v=h*i

where g, e, f, and h are constants representing transconductance, voltage gain, current gain, and transresistance, respectively.

1.6.6. Linear Voltage-Controlled Current Sources

General form:

GXXXXXXX N+ N- NC+ NC- VALUE

Examples:

G1 2 0 5 0 0.1MMHO

N+ and N- are the positive and negative nodes, respectively. Current flow is from the positive node, through the source, to the negative node. NC+ and NC- are the positive and negative controlling nodes, respectively. VALUE is the transconductance (in mhos).

1.6.7. Linear Voltage-Controlled Voltage Sources

General form:

EXXXXXXX N+ N- NC+ NC- VALUE

Examples:

E1 2 3 14 1 2.0

N+ is the positive node, and N- is the negative node. NC+ and NC- are the positive and negative controlling nodes, respectively. VALUE is the voltage gain.

1.6.8. Linear Current-Controlled Current Sources

General form:

FXXXXXXX N+ N- VNAM VALUE

Examples:

F1 13 5 VSENS 5

N+ and N- are the positive and negative nodes, respectively. Current flow is from the positive node, through the source, to the negative node. VNAM is the name of a voltage source through which the controlling current flows. The direction of positive controlling current flow is from the positive node, through the source, to the negative node of VNAM. VALUE is the current gain.

1.6.9. Linear Current-Controlled Voltage Sources

General form:

HXXXXXXX N+ N- VNAM VALUE

Examples:

HX 5 17 VZ 0.5K

N+ and N- are the positive and negative nodes, respectively. VNAM is the name of a voltage source through which the controlling current flows. The direction of positive controlling current flow is from the positive node, through the source, to the negative node of VNAM. VALUE is the transresistance (in ohms).

1.6.10. Non-linear Dependent Sources

General form:

BXXXXXXX N+ N- <I=EXPR> <V=EXPR>

Examples:

```
B1 0 1 I=cos(v(1))+sin(v(2))
B1 0 1 V=ln(cos(log(v(1)-v(2)^2)))-v(3)^4+v(2)^v(1)
B1 3 4 I=17
B1 3 4 V=exp(pi^i(vdd))
```

N+ is the positive node, and *N-* is the negative node. The values of the V and I parameters determine the voltages and currents across and through the device, respectively. If I is given then the device will be a current source, and if V is given the device will be a voltage source. One and only

one of these parameters must be given.

The expressions given for V and I may be any function of voltages and currents through voltage sources in the system. The following functions of real variables are defined:

abs	asinh	cosh	sin
acos	atan	exp	sinh
acosh	atanh	ln	sqrt
asin	cos	log	tan

The following operations are defined:

\+ - * / ^ unary -

If the values of the circuit variables used in the expressions enter a region where the value of the expression or of any of its partial derivatives becomes undefined, an error will result.

1.6.11. Independent Sources

General form:

VXXXXXXX N+ N- <<DC> DC/TRAN VALUE> <AC <ACMAG <ACPHASE>>>
IYYYYYYY N+ N- <<DC> DC/TRAN VALUE> <AC <ACMAG <ACPHASE>>>

Examples:

```
VCC 10 0 DC 6
VIN 13 2 0.001 AC 1 SIN(0 1 1MEG)
ISRC 23 21 AC 0.333 45.0 SFFM(0 1 10K 5 1K)
VMEAS 12 9
```

N+ and N- are the positive and negative nodes, respectively. Note that voltage sources need not be grounded. Positive current is assumed to flow from the positive node, through the source, to the negative node. A current source of positive value, will force current to flow out of the N+ node, through the source, and into the N- node. Voltage sources, in addition to being used for circuit excitation, are the 'ammeters' for SPICE, that is, zero valued voltage sources may be inserted into the circuit for the purpose of measuring current. They will, of course, have no effect on circuit operation

since they represent short-circuits.

DC/TRAN is the dc and transient analysis value of the source. If the source value is zero both for dc and transient analyses, this value may be omitted. If the source value is time-invariant (e.g., a power supply), then the value may optionally be preceded by the letters DC.

ACMAG is the ac magnitude and ACPHASE is the ac phase. The source is set to this value in the ac analysis. If ACMAG is omitted following the keyword AC, a value of unity is assumed. If ACPHASE is omitted, a value of zero is assumed. If the source is not an ac small-signal input, the keyword AC and the ac values are omitted.

Any independent source can be assigned a time-dependent value for transient analysis. If a source is assigned a time-dependent value, the time-zero value is used for dc analysis. There are five independent source functions: pulse, exponential, sinusoidal, piece-wise linear, and single-frequency FM. If parameters other than source values are omitted or set to zero, the default values shown will be assumed. (TSTEP is the printing increment and TSTOP is the final time (see the .TRAN card for explanation)).

1. Pulse PULSE(V1 V2 TD TR TF PW PER)

Examples:

VIN 3 0 PULSE(-1 1 2NS 2NS 2NS 50NS 100NS)

parameters	default values	units
V1 (initial value)		Volts or Amps
V2 (pulsed value)		Volts or Amps
TD (delay time)	0.0	seconds
TR (rise time)	TSTEP	seconds
TF (fall time)	TSTEP	seconds
PW (pulse width)	TSTOP	seconds
PER(period)	TSTOP	seconds

A single pulse so specified is described by the following table:

time	value
0	V1
TD	V1
TD+TR	V2
TD+TR+PW	V2
TD+TR+PW+TF	V1
TSTOP	V1

Intermediate points are determined by linear interpolation.

2. Sinusoidal SIN(VO VA FREQ TD THETA)

Examples:

VIN 3 0 SIN(0 1 100MEG 1NS 1E10)

parameters	default value	units
VO (offset)		Volts or Amps
VA (amplitude)		Volts or Amps
FREQ (frequency)	1/TSTOP	Hz
TD (delay)	0.0	seconds
THETA (damping factor)	0.0	1/seconds

The shape of the waveform is described by the following table:

time	value
0 to TD	VO
TD to TSTOP	VO + VA*exp(-(time-TD)*THETA)*sine(twopi*FREQ*(time+TD))

3. Exponential EXP(V1 V2 TD1 TAU1 TD2 TAU2)

Examples:

VIN 3 0 EXP(-4 -1 2NS 30NS 60NS 40NS)

parameters	default values	units

V1 (initial value)		Volts or Amps
V2 (pulsed value)		Volts or Amps
TD1 (rise delay time)	0.0	seconds
TAU1 (rise time constant)	TSTEP	seconds
TD2 (fall delay time)	TD1+TSTEP	seconds
TAU2 (fall time constant)	TSTEP	seconds

The shape of the waveform is described by the following table:

time	value
0 to TD1	V1
TD1 to TD2	V1+(V2-V1)*(1-exp(-(time-TD1)/TAU1))
TD2 to TSTOP	V1+(V2-V1)*(1-exp(-(time-TD1)/TAU1)) +(V1-V2)*(1-exp(-(time-TD2)/TAU2))

4. Piece-Wise Linear PWL(T1 V1 <T2 V2 T3 V3 T4 V4 ...>)

Examples:

VCLOCK 7 5 PWL(0 -7 10NS -7 11NS -3 17NS -3 18NS -7 50NS -7)

Parameters and default values

Each pair of values (Ti, Vi) specifies that the value of the source is Vi (in Volts or Amps) at time=Ti. The value of the source at intermediate values of time is determined by using linear interpolation on the input values.

5. Single-Frequency FM SFFM(VO VA FC MDI FS)

Examples:

V1 12 0 SFFM(0 1M 20K 5 1K)

parameters	default values	units
VO (offset)		Volts or Amps
VA (amplitude)		Volts or Amps
FC (carrier frequency)	1/TSTOP	Hz
MDI (modulation index)		
FS (signal frequency)	1/TSTOP	Hz

The shape of the waveform is described by the following equation:

value = VO + VA*sine((twopi*FC*time) + MDI*sine(twopi*FS*time))

1.6.12. Switches

General form:

SXXXXXXX N+ N- NC+ NC- MODEL <ON><OFF>
WYYYYYYY N+ N- VNAM MODEL <ON><OFF>

Examples:

s1 1 2 3 4 switch1 ON
s2 5 6 3 0 sm2 off
Switch1 1 2 10 0 smodel1
w1 1 2 vclock switchmod1
W2 3 0 vramp sm1 ON
wreset 5 6 vclck lossyswitch OFF

Nodes 1 and 2 are the nodes between which the switch terminals are connected. The model name is mandatory while the initial conditions are optional. For the voltage controlled switch, nodes 3 and 4 are the positive and negative controlling nodes respectively. For the current controlled switch, the controlling current is that through the specified voltage source. The direction of positive controlling current flow is from the positive node, through the source, to the negative node.

1.7. SEMICONDUCTOR DEVICES

The elements described to this point typically require only a few parameter values. However, the models for the semiconductor devices that are included in the SPICE program require many parameter values. Often, many devices in a circuit are defined by the same set of device model parameters. For these reasons, a set of device model parameters is defined on a separate .MODEL card and assigned a unique model name. The device element cards in SPICE then refer to the model name.

This scheme alleviates the need to specify all of the model parameters on each device element card.

Each device element card contains the device name, the nodes to which the device is connected, and the device model name. In addition, other optional parameters may be specified for some devices: geometric factors and an initial condition.

The area factor used on the diode, BJT, JFET, and MESFET device cards determines the number of equivalent parallel devices of a specified model. The affected parameters are marked with an asterisk under the heading 'area' in the model descriptions below. Several geometric factors associated with the channel and the drain and source diffusions can be specified on the MOSFET device card.

Two different forms of initial conditions may be specified for some devices. The first form is included to improve the dc convergence for circuits that contain more than one stable state. If a device is specified OFF, the dc operating point is determined with the terminal voltages for that device set to zero. After convergence is obtained, the program continues to iterate to obtain the exact value for the terminal voltages. If a circuit has more than one dc stable state, the OFF option can be used to force the solution to correspond to a desired state. If a device is specified OFF when in reality the device is conducting, the program will still obtain the correct solution (assuming the solutions converge) but more iterations will be required since the program must independently converge to two separate solutions. The .NODESET card serves a similar purpose as the OFF option. The .NODESET option is easier to apply and is the preferred means to aid convergence.

The second form of initial conditions are specified for use with the transient analysis. These are true 'initial conditions' as opposed to the convergence aids above. See the description of the .IC card and the .TRAN card for a detailed explanation of initial conditions.

1.7.1. Semiconductor Resistors

General form:

RXXXXXXX N1 N2 <VALUE> <MNAME> <L=LENGTH> <W=WIDTH> <TEMP=T>

Examples:

```
RLOAD 2 10 10K
RMOD 3 7 RMODEL L=10u W=1u
```

This is the more general form of the resistor presented in section 6.1, and allows the modeling of temperature effects and for the calculation of the actual resistance value from strictly geometric information and the specifications of the process. If VALUE is specified, it overrides the geometric information and defines the resistance. If MNAME is specified, then the resistance may be calculated from the process information in the model MNAME and the given LENGTH and WIDTH. If VALUE is not specified, then MNAME and LENGTH **must** be specified. If WIDTH is not specified, then it will be taken from the default width given in the model. The (optional) TEMP value is the temperature at which this device is to operate, and overrides the temperature specification on the .OPTION card.

1.7.2. Semiconductor Capacitors

General form:

CXXXXXXX N1 N2 <VALUE> <MNAME> <L=LENGTH> <W=WIDTH> <IC=VAL>

Examples:

```
CLOAD 2 10 10P
CMOD 3 7 CMODEL L=10u W=1u
```

This is the more general form of the Capacitor presented in section 6.2, and allows for the calculation of the actual capacitance value from strictly geometric information and the specifications of the process. If VALUE is specified, it defines the capacitance. If MNAME is specified, then the capacitance is calculated from the process information in the model MNAME and the given LENGTH and WIDTH. If VALUE is not specified, then MNAME and LENGTH **must** be specified. If WIDTH is not specified, then it will be taken from the default width given in the model. Either VALUE or MNAME, LENGTH, and WIDTH may be specified, but not both sets.

1.7.3. Uniform Distributed RC Lines (Lossy)

General form:

UXXXXXXX N1 N2 N3 MNAME L=LEN <N=LUMPS>

Examples:

U1 1 2 0 URCMOD L=50U
URC2 1 12 2 UMODL l=1MIL N=6

N1 and N2 are the two element nodes the RC line connects, while N3 is the node to which the capacitances are connected. MNAME is the model name, LEN is the length of the RC line in meters. LUMPS, if specified, is the number of lumped segments to use in modeling the RC line (see the model description for the action taken if this parameter is omitted).

1.7.4. Junction Diodes

General form:

DXXXXXXX N+ N- MNAME <AREA> <OFF> <IC=VD> <TEMP=T>

Examples:

DBRIDGE 2 10 DIODE1
DCLMP 3 7 DMOD 3.0 IC=0.2

N+ and N- are the positive and negative nodes, respectively. MNAME is the model name, AREA is the area factor, and OFF indicates an (optional) starting condition on the device for dc analysis. If the area factor is omitted, a value of 1.0 is assumed. The (optional) initial condition specification using IC=VD is intended for use with the UIC option on the .TRAN card, when a transient analysis is desired starting from other than the quiescent operating point. The (optional) TEMP value is the temperature at which this device is to operate, and overrides the temperature specification on the .OPTION card.

1.7.5. Bipolar Junction Transistors (BJT's)

General form:

QXXXXXXX NC NB NE <NS> MNAME <AREA> <OFF> <IC=VBE, VCE> <TEMP=T>

Examples:

Q23 10 24 13 QMOD IC=0.6, 5.0
Q50A 11 26 4 20 MOD1

NC, NB, and NE are the collector, base, and emitter nodes, respectively. NS is the (optional) substrate node. If unspecified, ground is used. MNAME is the model name, AREA is the area factor, and OFF indicates an (optional) initial condition on the device for the dc analysis. If the area factor is omitted, a value of 1.0 is assumed. The (optional) initial condition specification using IC=VBE, VCE is intended for use with the UIC option on the .TRAN card, when a transient analysis is desired starting from other than the quiescent operating point. See the .IC card description for a better way to set transient initial conditions. The (optional) TEMP value is the temperature at which this device is to operate, and overrides the temperature specification on the .OPTION card.

1.7.6. Junction Field-Effect Transistors (JFET's)

General form:

JXXXXXXX ND NG NS MNAME <AREA> <OFF> <IC=VDS, VGS> <TEMP=T>

Examples:

J1 7 2 3 JM1 OFF

ND, NG, and NS are the drain, gate, and source nodes, respectively. MNAME is the model name, AREA is the area factor, and OFF indicates an (optional) initial condition on the device for dc analysis. If the area factor is omitted, a value of 1.0 is assumed. The (optional) initial condition specification, using IC=VDS, VGS is intended for use with the UIC option on the .TRAN card, when a transient analysis is desired starting from other than the quiescent operating point. See the .IC card

for a better way to set initial conditions. The (optional) TEMP value is the temperature at which this device is to operate, and overrides the temperature specification on the .OPTION card.

1.7.7. MOSFET's

General form:

MXXXXXXX ND NG NS NB MNAME <L=VAL> <W=VAL> <AD=VAL> <AS=VAL>
+ <PD=VAL> <PS=VAL> <NRD=VAL> <NRS=VAL> <OFF> <IC=VDS, VGS, VBS> <TEMP=T>

Examples:

M1 24 2 0 20 TYPE1
M31 2 17 6 10 MODM L=5U W=2U
M1 2 9 3 0 MOD1 L=10U W=5U AD=100P AS=100P PD=40U PS=40U

ND, NG, NS, and NB are the drain, gate, source, and bulk (substrate) nodes, respectively. MNAME is the model name. L and W are the channel length and width, in meters. AD and AS are the areas of the drain and source diffusions, in sq-meters. Note that the suffix U specifies microns (1E-6 m) and P sq-microns (1E-12 sq-m). If any of L, W, AD, or AS are not specified, default values are used. The use of defaults simplifies input deck preparation, as well as the editing required if device geometries are to be changed. PD and PS are the perimeters of the drain and source junctions, in meters. NRD and NRS designate the equivalent number of squares of the drain and source diffusions; these values multiply the sheet resistance RSH specified on the .MODEL card for an accurate representation of the parasitic series drain and source resistance of each transistor. PD and PS default to 0.0 while NRD and NRS to 1.0. OFF indicates an (optional) initial condition on the device for dc analysis. The (optional) initial condition specification using IC=VDS, VGS, VBS is intended for use with the UIC option on the .TRAN card, when a transient analysis is desired starting from other than the quiescent operating point. See the .IC card for a better and more convenient way to specify transient initial conditions. The (optional) TEMP value is the temperature at which this device is to operate, and overrides the temperature specification on the .OPTION card. The temperature specification is ONLY valid for level 1, 2, and 3 MOSFET's, not for level 4 or BSIM devices.

1.7.8. MESFET's

General form:

ZXXXXXXX ND NG NS MNAME <AREA> <OFF> <IC=VDS, VGS>

Examples:

Z1 7 2 3 ZM1 OFF

ND, NG, and NS are the drain, gate, and source nodes, respectively. MNAME is the model name, AREA is the area factor, and OFF indicates an (optional) initial condition on the device for dc analysis. If the area factor is omitted, a value of 1.0 is assumed. The (optional) initial condition specification, using IC=VDS, VGS is intended for use with the UIC option on the .TRAN card, when a transient analysis is desired starting from other than the quiescent operating point. See the .IC card for a better way to set initial conditions.

1.7.9. .MODEL Card

General form:

.MODEL MNAME TYPE(PNAME1=PVAL1 PNAME2=PVAL2 ...)

Examples:

.MODEL MOD1 NPN (BF=50 IS=1E-13 VBF=50)

The .MODEL card specifies a set of model parameters that will be used by one or more devices. MNAME is the model name, and type is one of the following fourteen types:

R	resistor model
C	capacitor model
URC	Uniform Distributed RC model
D	diode model
NPN	NPN BJT model
PNP	PNP BJT model
NJF	N-channel JFET model
PJF	P-channel JFET model
NMOS	N-channel MOSFET model

PMOS	P-channel MOSFET model
NMF	N-channel MESFET model
PMF	P-channel MESFET model
SW	voltage controlled switch
CSW	current controlled switch

Parameter values are defined by appending the parameter name, as given below for each model type, followed by an equal sign and the parameter value. Model parameters that are not given a value are assigned the default values given below for each model type.

1.7.10. Resistor Model

The resistor model consists of process-related device data that allow the resistance to be calculated from geometric information and to be corrected for temperature. The parameters available are:

name	parameter	units	default	example
TC1	first order temperature coeff.	Ω/°C	0.0	-
TC2	second order temperature coeff.	$\Omega/°C^2$	0.0	-
RSH	sheet resistance	Ω/□	-	50
DEFW	default width	meters	1e-6	2e-6
NARROW	narrowing due to side etching	meters	0.0	1e-7
TNOM	parameter measurement temperature	°C	27	50

The sheet resistance is used with the narrowing parameter and L and W from the resistor card to determine the nominal resistance by the formula

$$R=RSH\times\frac{L-NARROW}{W-NARROW}$$

DEFW is used to supply a default value for W if one is not specified on the device card. If either RSH or L is not specified, then the standard default resistance value of 1k Ω is used. TNOM is used to override the circuitwide value given on the .OPTIONS card where the parameters of this model have been measured at a different temperature. After the nominal resistance is calculated, it is adjusted for temperature by the formula:

$$RES(temp)=RES(tnom)\times(1+TC1\times(temp-tnom)+TC2*(temp-tnom)^2)$$

1.7.11. Capacitor Model

The capacitor model contains process information that may be used to compute the capacitance from strictly geometric information.

name	parameter	units	default	example
CJ	junction bottom capacitance	F/meters^2	-	5e-5
CJSW	junction sidewall capacitance	F/meters	-	2e-11
DEFW	default device width	meters	1e-6	2e-6
NARROW	narrowing due to side etching	meters	0.0	1e-7

The capacitor has a capacitance computed as

CAP=CJ×(LENGTH–NARROW)×(WIDTH–NARROW)+2×CJSW×(LENGTH+WIDTH–2*NARROW)

1.7.12. Uniform Distributed RC Model

The URC model is derived from a model proposed by L. Gertzberrg in 1974. The model is accomplished by a subcircuit type expansion of the URC line into a network of lumped RC segments with internally generated nodes. The RC segments are in a geometric progression, increasing toward the middle of the URC line, with K as a proportionality constant. The number of lumped segments used, if not specified on the URC line card, is determined by the following formula:

$$N=\frac{\log\left[F_{max}\times\frac{R}{L}\times\frac{C}{L}\times 2\times\pi\times l^2\times\left[\frac{(K-1)}{K}\right]^2\right]}{\log K}$$

The URC line will be made up strictly of resistor and capacitor segments unless the ISPERL parameter is given a non-zero value, in which case the capacitors are replaced with reverse biased diodes with a zero-bias junction capacitance equivalent to the capacitance replaced, and with a saturation current of ISPERL amps per meter of transmission line and an optional series resistance equivalent to RSPERL ohms per meter.

	name	parameter	units	default	example	area
1	K	Propagation Constant	-	2.0	1.2	-
2	FMAX	Maximum Frequency of interest	Hz	1.0G	6.5MEG	-
3	RPERL	Resistance per unit length	Ohm/m	1000	10	-
4	CPERL	Capacitance per unit length	F/m	1.0E-15	1PF	-
5	ISPERL	Saturation Current per unit length	Amp/m	0	-	-
6	RSPERL	Diode Resistance per unit length	Ohm/m	0	-	-

1.7.13. Switch Model

The switch model allows an almost ideal switch to be described in SPICE. The switch is not quite ideal, in that the resistance can not change from 0 to infinity, but must always have a finite positive value. By proper selection of the on and off resistances, they can be effectively zero and infinity in comparison to other circuit elements. The parameters available are:

name	parameter	units	default	switch
VT	threshold voltage	Volts	0.0	S
IT	threshold current	Amps	0.0	W
VH	hysteresis voltage	Volts	0.0	S
IH	hysteresis current	Amps	0.0	W
RON	on resistance	Ω	1.0	both
ROFF	off resistance	Ω	1/GMIN*	both

*(See the .OPTIONS card for a description of GMIN, its default value results is a off resistance of 1.0e+12 ohms.)

The use of an ideal element that is highly non-linear such as a switch can cause large discontinuities to occur in the circuit node voltages. A rapid change such as that associated with a switch changing state can cause numerical roundoff or tolerance problems leading to erroneous results or timestep difficulties. The user of switches can improve the situation by taking the following steps:

First of all it is wise to set ideal switch impedances only high and low enough to be negligible with respect to other circuit elements. Using switch impedances that are close to "ideal" in all cases will aggravate the problem of discontinuities mentioned above. Of course, when modeling real dev-

ices such as MOSFETS, the on resistance should be adjusted to a realistic level depending on the size of the device being modelled.

If a wide range of ON to OFF resistance must be used in the switches (ROFF/RON >1e+12), then the tolerance on errors allowed during transient analysis should be decreased by using the .OPTIONS card and specifying TRTOL to be less than the default value of 7.0. When switches are placed around capacitors, then the option CHGTOL should also be reduced. Suggested values for these two options are 1.0 and 1e-16 respectively. These changes inform SPICE3 to be more careful around the switch points so that no errors are made due to the rapid change in the circuit.

1.7.14. Diode Model

The dc characteristics of the diode are determined by the parameters IS and N. An ohmic resistance, RS, is included. Charge storage effects are modeled by a transit time, TT, and a nonlinear depletion layer capacitance which is determined by the parameters CJO, VJ, and M. The temperature dependence of the saturation current is defined by the parameters EG, the energy and XTI, the saturation current temperature exponent. The nominal temperature at which these parameters were measured is TNOM, which defaults to the circuitwide value specified on the .OPTIONS card. Reverse breakdown is modeled by an exponential increase in the reverse diode current and is determined by the parameters BV and IBV (both of which are positive numbers).

	name	parameter	units	default	example	area
1	IS	saturation current	A	1.0E-14	1.0E-14	*
2	RS	ohmic resistance	Ohm	0	10	*
3	N	emission coefficient	-	1	1.0	
4	TT	transit-time	sec	0	0.1Ns	
5	CJO	zero-bias junction capacitance	F	0	2PF	*
6	VJ	junction potential	V	1	0.6	
7	M	grading coefficient	-	0.5	0.5	
8	EG	activation energy	eV	1.11	1.11 Si 0.69 Sbd 0.67 Ge	
9	XTI	saturation-current temp. exp	-	3.0	3.0 jn	

					2.0 Sbd
10	KF	flicker noise coefficient	-	0	
11	AF	flicker noise exponent	-	1	
12	FC	coefficient for forward-bias depletion capacitance formula	-	0.5	
13	BV	reverse breakdown voltage	V	infinite	40.0
14	IBV	current at breakdown voltage	A	1.0E-3	
15	TNOM	parameter measurement temperature	°C	27	50

1.7.15. BJT Models (both NPN and PNP)

The bipolar junction transistor model in SPICE is an adaptation of the integral charge control model of Gummel and Poon. This modified Gummel-Poon model extends the original model to include several effects at high bias levels. The model will automatically simplify to the simpler Ebers-Moll model when certain parameters are not specified. The parameter names used in the modified Gummel-Poon model have been chosen to be more easily understood by the program user, and to reflect better both physical and circuit design thinking.

The dc model is defined by the parameters IS, BF, NF, ISE, IKF, and NE which determine the forward current gain characteristics, IS, BR, NR, ISC, IKR, and NC which determine the reverse current gain characteristics, and VAF and VAR which determine the output conductance for forward and reverse regions. Three ohmic resistances RB, RC, and RE are included, where RB can be high current dependent. Base charge storage is modeled by forward and reverse transit times, TF and TR, the forward transit time TF being bias dependent if desired, and nonlinear depletion layer capacitances which are determined by CJE, VJE, and MJE for the B-E junction , CJC, VJC, and MJC for the B-C junction and CJS, VJS, and MJS for the C-S (Collector-Substrate) junction. The temperature dependence of the saturation current, IS, is determined by the energy-gap, EG, and the saturation current temperature exponent, XTI. Additionally base current temperature dependence is modeled by the beta temperature exponent XTB in the new model. The values specified are assumed to have been measured at the temperature TNOM, which can be specified on the .OPTIONS card or overridden by a specification on the .MODEL card.

The BJT parameters used in the modified Gummel-Poon model are listed below. The parameter names used in earlier versions of SPICE2 are still accepted.

Modified Gummel-Poon BJT Parameters.

	name	parameter	units	default	example	area
1	IS	transport saturation current	A	1.0E-16	1.0E-15	*
2	BF	ideal maximum forward beta	-	100	100	
3	NF	forward current emission coefficient	-	1.0	1	
4	VAF	forward Early voltage	V	infinite	200	
5	IKF	corner for forward beta high current roll-off	A	infinite	0.01	*
6	ISE	B-E leakage saturation current	A	0	1.0E-13	*
7	NE	B-E leakage emission coefficient	-	1.5	2	
8	BR	ideal maximum reverse beta	-	1	0.1	
9	NR	reverse current emission coefficient	-	1	1	
10	VAR	reverse Early voltage	V	infinite	200	
11	IKR	corner for reverse beta high current roll-off	A	infinite	0.01	*
12	ISC	B-C leakage saturation current	A	0	1.0E-13	*
13	NC	B-C leakage emission coefficient	-	2	1.5	
14	RB	zero bias base resistance	Ohms	0	100	*
15	IRB	current where base resistance falls halfway to its min value	A	infinite	0.1	*
16	RBM	minimum base resistance at high currents	Ohms	RB	10	*
17	RE	emitter resistance	Ohms	0	1	*
18	RC	collector resistance	Ohms	0	10	*
19	CJE	B-E zero-bias depletion capacitance	F	0	2PF	*
20	VJE	B-E built-in potential	V	0.75	0.6	
21	MJE	B-E junction exponential factor	-	0.33	0.33	
22	TF	ideal forward transit time	sec	0	0.1Ns	
23	XTF	coefficient for bias dependence of TF	-	0		
24	VTF	voltage describing VBC dependence of TF	V	infinite		
25	ITF	high-current parameter for effect on TF	A	0		*
26	PTF	excess phase at freq=1.0/(TF*2PI) Hz	deg	0		
27	CJC	B-C zero-bias depletion capacitance	F	0	2PF	*
28	VJC	B-C built-in potential	V	0.75	0.5	
29	MJC	B-C junction exponential factor	-	0.33	0.5	
30	XCJC	fraction of B-C depletion capacitance connected to internal base node	-	1		
31	TR	ideal reverse transit time	sec	0	10Ns	
32	CJS	zero-bias collector-substrate capacitance	F	0	2PF	*
33	VJS	substrate junction built-in potential	V	0.75		

34	MJS	substrate junction exponential factor	-	0	0.5
35	XTB	forward and reverse beta temperature exponent	-	0	
36	EG	energy gap for temperature effect on IS	eV	1.11	
37	XTI	temperature exponent for effect on IS	-	3	
38	KF	flicker-noise coefficient	-	0	
39	AF	flicker-noise exponent	-	1	
40	FC	coefficient for forward-bias depletion capacitance formula	-	0.5	
41	TNOM	Parameter measurement temperature	°C	27	50

1.7.16. JFET Models (both N and P Channel)

The JFET model is derived from the FET model of Shichman and Hodges. The dc characteristics are defined by the parameters VTO and BETA, which determine the variation of drain current with gate voltage, LAMBDA, which determines the output conductance, and IS, the saturation current of the two gate junctions. Two ohmic resistances, RD and RS, are included. Charge storage is modeled by nonlinear depletion layer capacitances for both gate junctions which vary as the -1/2 power of junction voltage and are defined by the parameters CGS, CGD, and PB.

	name	parameter	units	default	example	area
1	VTO	threshold voltage	V	-2.0	-2.0	
2	BETA	transconductance parameter	A/V**2	1.0E-4	1.0E-3	*
3	LAMBDA	channel length modulation parameter	1/V	0	1.0E-4	
4	RD	drain ohmic resistance	Ohm	0	100	*
5	RS	source ohmic resistance	Ohm	0	100	*
6	CGS	zero-bias G-S junction capacitance	F	0	5PF	*
7	CGD	zero-bias G-D junction capacitance	F	0	1PF	*
8	PB	gate junction potential	V	1	0.6	
9	IS	gate junction saturation current	A	1.0E-14	1.0E-14	*
10	KF	flicker noise coefficient	-	0		
11	AF	flicker noise exponent	-	1		
12	FC	coefficient for forward-bias depletion capacitance formula	-	0.5		
13	TNOM	parameter measurement temperature	°C	27	50	

1.7.17. MOSFET Models (both N and P channel)

SPICE provides four MOSFET device models, which differ in the formulation of the I-V characteristic. The variable LEVEL specifies the model to be used:

LEVEL=1 ->	Shichman-Hodges
LEVEL=2 ->	MOS2 (as described in [1])
LEVEL=3 ->	MOS3, a semi-empirical model(see [1])
LEVEL=4 ->	BSIM (as described in [2])

The dc characteristics of the level 1 through level 3 MOSFETs are defined by the device parameters VTO, KP, LAMBDA, PHI and GAMMA. These parameters are computed by SPICE if process parameters (NSUB, TOX, ...) are given, but user-specified values always override. VTO is positive (negative) for enhancement mode and negative (positive) for depletion mode N-channel (P-channel) devices. Charge storage is modeled by three constant capacitors, CGSO, CGDO, and CGBO which represent overlap capacitances, by the nonlinear thin-oxide capacitance which is distributed among the gate, source, drain, and bulk regions, and by the nonlinear depletion-layer capacitances for both substrate junctions divided into bottom and periphery, which vary as the MJ and MJSW power of junction voltage respectively, and are determined by the parameters CBD, CBS, CJ, CJSW, MJ, MJSW and PB. Charge storage effects are modeled by the piecewise linear voltages-dependent capacitance model proposed by Meyer. The thin-oxide charge storage effects are treated slightly different for the LEVEL=1 model. These voltage-dependent capacitances are included only if TOX is specified in the input description and they are represented using Meyer's formulation.

There is some overlap among the parameters describing the junctions, e.g. the reverse current can be input either as IS (in A) or as JS (in A/m**2). Whereas the first is an absolute value the second is multiplied by AD and AS to give the reverse current of the drain and source junctions respectively. This methodology has been chosen since there is no sense in relating always junction characteristics with AD and AS entered on the device card; the areas can be defaulted. The same idea applies also to the zero-bias junction capacitances CBD and CBS (in F) on one hand, and CJ (in F/m**2) on the other. The parasitic drain and source series resistance can be expressed as either RD

and RS (in ohms) or RSH (in ohms/sq.), the latter being multiplied by the number of squares NRD and NRS input on the device card.

SPICE level 1 to level 3 parameters.

	name	parameter	units	default	example
1	LEVEL	model index	-	1	
2	VTO	zero-bias threshold voltage	V	0.0	1.0
3	KP	transconductance parameter	A/V**2	2.0E-5	3.1E-5
4	GAMMA	bulk threshold parameter	V**0.5	0.0	0.37
5	PHI	surface potential	V	0.6	0.65
6	LAMBDA	channel-length modulation (MOS1 and MOS2 only)	1/V	0.0	0.02
7	RD	drain ohmic resistance	Ohm	0.0	1.0
8	RS	source ohmic resistance	Ohm	0.0	1.0
9	CBD	zero-bias B-D junction capacitance	F	0.0	20FF
10	CBS	zero-bias B-S junction capacitance	F	0.0	20FF
11	IS	bulk junction saturation current	A	1.0E-14	1.0E-15
12	PB	bulk junction potential	V	0.8	0.87
13	CGSO	gate-source overlap capacitance per meter channel width	F/m	0.0	4.0E-11
14	CGDO	gate-drain overlap capacitance per meter channel width	F/m	0.0	4.0E-11
15	CGBO	gate-bulk overlap capacitance per meter channel length	F/m	0.0	2.0E-10
16	RSH	drain and source diffusion sheet resistance	Ohm/sq.	0.0	10.0
17	CJ	zero-bias bulk junction bottom cap. per sq-meter of junction area	F/m**2	0.0	2.0E-4
18	MJ	bulk junction bottom grading coef.	-	0.5	0.5
19	CJSW	zero-bias bulk junction sidewall cap. per meter of junction perimeter	F/m	0.0	1.0E-9
20	MJSW	bulk junction sidewall grading coef.	-	0.50(level1) 0.33(level2, 3)	
21	JS	bulk junction saturation current per sq-meter of junction area	A/m**2		1.0E-8
22	TOX	oxide thickness	meter	1.0E-7	1.0E-7
23	NSUB	substrate doping	1/cm**3	0.0	4.0E15
24	NSS	surface state density	1/cm**2	0.0	1.0E10
25	NFS	fast surface state density	1/cm**2	0.0	1.0E10
26	TPG	type of gate material: +1 opp. to substrate -1 same as substrate 0 Al gate	-	1.0	
27	XJ	metallurgical junction depth	meter	0.0	1U
28	LD	lateral diffusion	meter	0.0	0.8U
29	UO	surface mobility	cm**2/V-s	600	700

30	UCRIT	critical field for mobility degradation (MOS2 only)	V/cm	1.0E4	1.0E4
31	UEXP	critical field exponent in mobility degradation (MOS2 only)	-	0.0	0.1
32	UTRA	transverse field coef (mobility) (deleted for MOS2)	-	0.0	0.3
33	VMAX	maximum drift velocity of carriers	m/s	0.0	5.0E4
34	NEFF	total channel charge (fixed and mobile) coefficient (MOS2 only)	-	1.0	5.0
35	KF	flicker noise coefficient	-	0.0	1.0E-26
36	AF	flicker noise exponent	-	1.0	1.2
37	FC	coefficient for forward-bias depletion capacitance formula	-	0.5	
38	DELTA	width effect on threshold voltage (MOS2 and MOS3)	-	0.0	1.0
39	THETA	mobility modulation (MOS3 only)	1/V	0.0	0.1
40	ETA	static feedback (MOS3 only)	-	0.0	1.0
41	KAPPA	saturation field factor (MOS3 only)	-	0.2	0.5
42	TNOM	parameter measurement temperature	°C	27	50

The level 4 parameters are all values obtained from process characterization, and can be generated automatically. J. Pierret [3] describes a means of generating a 'process' file, and the program Proc2Mod provided with SPICE3 will convert this file into a sequence of .MODEL cards suitable for inclusion in a SPICE deck. Parameters marked below with an * in the l/w column also have corresponding parameters with a length and width dependency. For example, VFB is the basic parameter with units of Volts, and LVFB and WVFB also exist and have units of Volt-μmeter The formula

$$P=P_0+\frac{P_L}{L_{effective}}+\frac{P_W}{W_{effective}}$$

is used to evaluate the parameter for the actual device specified with

$$L_{effective}=L_{input}-DL$$

and

$$W_{effective}=W_{input}-DW$$

Note that unlike the other models in SPICE, the BSIM model is designed for use with a process characterization system that provides all the parameters, thus there are no defaults for the parameters, and leaving one out is considered an error. For an example set of parameters and the format of a process file, see the SPICE2 implementation notes[2].

SPICE BSIM (level 4) parameters.

name	parameter	units	l/w
VFB	flat-band voltage	V	*
PHI	surface inversion potential	V	*
K1	body effect coefficient	$V^{1/2}$	*
K2	drain/source depletion charge sharing coefficient	-	*
ETA	zero-bias drain-induced barrier lowering coefficient	-	*
MUZ	zero-bias mobility	$cm^2/V–s$	
DL	shortening of channel	µm	
DW	narrowing of channel	µm	
U0	zero-bias transverse-field mobility degradation coefficient	V^{-1}	*
U1	zero-bias velocity saturation coefficient	µm/V	*
X2MZ	sens. of mobility to substrate bias at v_{ds}=0	$cm^2/V^2–s$	*
X2E	sens. of drain-induced barrier lowering effect to substrate bias	V^{-1}	*
X3E	sens. of drain-induced barrier lowering effect to drain bias at $V_{ds}=V_{dd}$	V^{-1}	*
X2U0	sens. of transverse field mobility degradation effect to substrate bias	V^{-2}	*
X2U1	sens. of velocity saturation effect to substrate bias	μmV^{-2}	*
MUS	mobility at zero substrate bias and at $V_{ds}=V_{dd}$	$cm^2/V^2–s$	
X2MS	sens. of mobility to substrate bias at $V_{ds}=V_{dd}$	$cm^2/V^2–s$	*
X3MS	sens. of mobility to drain bias at $V_{ds}=V_{dd}$	$cm^2/V^2–s$	*
X3U1	sens. of velocity saturation effect on drain bias at $V_{ds}=V_{dd}$	μmV^{-2}	*
TOX	gate oxide thickness	µm	
TEMP	temperature at which parameters were measured	°C	
VDD	measurement bias range	V	
CGDO	gate-drain overlap capacitance per meter channel width	F/m	
CGSO	gate-source overlap capacitance per meter channel width	F/m	
CGBO	gate-bulk overlap capacitance per meter channel length	F/m	
XPART	gate-oxide capacitance charge model flag	-	
N0	zero-bias subthreshold slope coefficient	-	*
NB	sens. of subthreshold slope to substrate bias	-	*
ND	sens. of subthreshold slope to drain bias	-	*
RSH	drain and source diffusion sheet resistance	Ω/□	
JS	source drain junction current density	A/m^2	
PB	built in potential of source drain junction	V	
MJ	Grading coefficient of source drain junction	-	
PBSW	built in potential of source, drain juntion sidewall	V	
MJSW	grading coefficient of source drain junction sidewall	-	
CJ	Source drain junction capacitance per unit area	F/m^2	
CJSW	source drain junction sidewall capacitance per unit length	F/m	
WDF	source drain junction default width	m	
DELL	Source drain junction length reduction	m	

XPART = 0 selects a 40/60 drain/source charge partition in saturation, while XPART=1 selects a 0/100 drain/source charge partition.

1.7.18. MESFET Models (both N and P Channel)

The MESFET model is derived from the GaAs FET model of Statz et al. as described in [4]. The dc characteristics are defined by the parameters VTO, B, and BETA, which determine the variation of drain current with gate voltage, ALPHA, which determines saturation voltage, and LAMBDA, which determines the output conductance. The formula are given by

$$I_d = \frac{\beta (V_{gs}-V_T)^2}{1 + b(V_{gs} - V_T)} \left[1 - \left[1-\alpha\frac{V_{ds}}{3}\right]^3\right](1 + \lambda V_{ds}) \quad \text{for } 0<V_{ds}<\frac{3}{\alpha}$$

$$I_d = \frac{\beta (V_{gs}-V_T)^2}{1 + b(V_{gs} - V_T)}(1 + \lambda V_{ds}) \quad \text{for } V_{ds}>\frac{3}{\alpha}$$

Two ohmic resistances, RD and RS, are included. Charge storage is modeled by total gate charge as a function of gate-drain and gate-source voltages and is defined by the parameters CGS, CGD, and PB.

	name	parameter	units	default	example	area
1	VTO	pinch-off voltage	V	-2.0	-2.0	
2	BETA	transconductance parameter	A/V**2	1.0E-4	1.0E-3	*
3	B	doping tail extending parameter	1/V	0.3	0.3	*
4	ALPHA	saturation voltage parameter	1/V	2	2	*
5	LAMBDA	channel length modulation parameter	1/V	0	1.0E-4	
6	RD	drain ohmic resistance	Ohm	0	100	*
7	RS	source ohmic resistance	Ohm	0	100	*
8	CGS	zero-bias G-S junction capacitance	F	0	5PF	*
9	CGD	zero-bias G-D junction capacitance	F	0	1PF	*
10	PB	gate junction potential	V	1	0.6	
11	KF	flicker noise coefficient	-	0		
12	AF	flicker noise exponent	-	1		
13	FC	coefficient for forward-bias depletion capacitance formula	-	0.5		

[1] A. Vladimirescu and S. Liu, "The Simulation of MOS Integrated Circuits Using SPICE2", ERL Memo No. ERL M80/7, Electronics Research Laboratory, University of California, Berkeley, Oct. 1980.

[2] B. J. Sheu, D. L. Scharfetter, and P. K. Ko, "SPICE2 Implementation of BSIM" ERL Memo No. ERL M85/42, Electronics Research Laboratory, University of California, Berkeley, May 1985.

[3] J. R. Pierret, "A MOS Parameter Extraction Program for the BSIM Model" ERL Memo Nos. ERL

M84/99 and M84/100, Electronics Research Laboratory, University of California, Berkeley, Nov. 1984.

[4] H.Statz et al., "GaAs FET Device and Circuit Simulation in SPICE", IEEE Transactions on Electron Devices, V34, Number 2, February, 1987 pp160-169.

1.8. SUBCIRCUITS

A subcircuit that consists of SPICE elements can be defined and referenced in a fashion similar to device models. The subcircuit is defined in the input deck by a grouping of element cards; the program then automatically inserts the group of elements wherever the subcircuit is referenced. There is no limit on the size or complexity of subcircuits, and subcircuits may contain other subcircuits. An example of subcircuit usage is given in the final section of this chapter.

1.8.1. .SUBCKT Card

General form:

.SUBCKT subnam N1 <N2 N3 ...>

Examples:

.SUBCKT OPAMP 1 2 3 4

A circuit definition is begun with a .SUBCKT card. SUBNAM is the subcircuit name, and N1, N2, ... are the external nodes, which cannot be zero. The group of element cards which immediately follow the .SUBCKT card define the subcircuit. The last card in a subcircuit definition is the .ENDS card (see below). Control cards may not appear within a subcircuit definition; however, subcircuit definitions may contain anything else, including other subcircuit definitions, device models, and subcircuit calls (see below). Note that any device models or subcircuit definitions included as part of a subcircuit definition are strictly local (i.e., such models and definitions are not known outside the sub-

circuit definition). Also, any element nodes not included on the .SUBCKT card are strictly local, with the exception of 0 (ground) which is always global.

1.8.2. .ENDS Card

General form:

.ENDS <SUBNAM>

Examples:

.ENDS OPAMP

This card must be the last one for any subcircuit definition. The subcircuit name, if included, indicates which subcircuit definition is being terminated; if omitted, all subcircuits being defined are terminated. The name is needed only when nested subcircuit definitions are being made.

1.8.3. Subcircuit Calls

General form:

XYYYYYYY N1 <N2 N3 ...> SUBNAM

Examples:

X1 2 4 17 3 1 MULTI

Subcircuits are used in SPICE by specifying pseudo-elements beginning with the letter X, followed by the circuit nodes to be used in expanding the subcircuit.

1.9. CONTROL CARDS

1.9.1. .OPTIONS Card

General form:

.OPTIONS OPT1 OPT2 ... (or OPT=OPTVAL ...)

Examples:

.OPTIONS RELTOL=.005 TRTOL=8

This card allows the user to reset program control and user options for specific simulation purposes. Additional options for Nutmeg may be specified as well and take effect when Nutmeg reads the input deck. Options specified to Nutmeg via the 'set' command are also passed on to SPICE3 as if specified on a .OPTIONS card. See the Nutmeg manual for the Nutmeg parameters which may be set with a .OPTIONS card and the format of the Nutmeg 'set' command. Any combination of the following options may be included, in any order. 'x' (below) represents some positive number.

option	effect
GMIN=x	resets the value of GMIN, the minimum conductance allowed by the program. The default value is 1.0E-12.
RELTOL=x	resets the relative error tolerance of the program. The default value is 0.001 (0.1 percent).
ABSTOL=x	resets the absolute current error tolerance of the program. The default value is 1 picoamp.
VNTOL=x	resets the absolute voltage error tolerance of the program. The default value is 1 microvolt.
TRTOL=x	resets the transient error tolerance. The default value is 7.0. This parameter is an estimate of the factor by which SPICE overestimates the actual truncation error.
CHGTOL=x	resets the charge tolerance of the program. The default value is 1.0E-14.
PIVTOL=x	resets the absolute minimum value for a matrix entry to be accepted as a pivot. The default value is 1.0E-13.
PIVREL=x	resets the relative ratio between the largest column entry and an acceptable pivot value. The default value is 1.0E-3. In the numerical pivoting algorithm the allowed minimum pivot value is determined by EPSREL=AMAX1(PIVREL*MAXVAL, PIVTOL) where MAXVAL is the maximum element in the column where

	a pivot is sought (partial pivoting).
TNOM=x	resets the nominal temperature at which device parameters are measured. The default value is 27 deg C (300 deg K). TNOM can be overridden by a specification on any temperature dependent device model.
TEMP=x	Resets the operating temperature of the circuit. The default value is 27 deg C (300 deg K). TEMP can be overridden by a temperature specification on any temperature dependent instance.
ITL1=x	resets the dc iteration limit. The default is 100.
ITL2=x	resets the dc transfer curve iteration limit. The default is 50.
ITL5=x	resets the transient analysis total iteration limit. the default is 5000. Set ITL5=0 to omit this test.
DEFL=x	resets the value for MOS channel length; the default is 100.0 micrometer.
DEFW=x	resets the value for MOS channel width; the default is 100.0 micrometer.
DEFAD=x	resets the value for MOS drain diffusion area; the default is 0.0.
DEFAS=x	resets the value for MOS source diffusion area; the default is 0.0.

1.9.2. .OP Card

General form:

.OP

The inclusion of this card in an input deck will force SPICE to determine the dc operating point of the circuit with inductors shorted and capacitors opened. Note: a dc analysis is automatically performed prior to a transient analysis to determine the transient initial conditions, and prior to an ac small-signal analysis to determine the linearized, small-signal models for nonlinear devices.

1.9.3. .DC Card

General form:

.DC SRCNAM VSTART VSTOP VINCR [SRC2 START2 STOP2 INCR2]

Examples:

.DC VIN 0.25 5.0 0.25
.DC VDS 0 10 .5 VGS 0 5 1
.DC VCE 0 10 .25 IB 0 10U 1U

This card defines the dc transfer curve source and sweep limits. SRCNAM is the name of an independent voltage or current source. VSTART, VSTOP, and VINCR are the starting, final, and incrementing values respectively. The first example will cause the value of the voltage source VIN to be swept from 0.25 Volts to 5.0 Volts in increments of 0.25 Volts. A second source (SRC2) may optionally be specified with associated sweep parameters. In this case, the first source will be swept over its range for each value of the second source. This option can be useful for obtaining semiconductor device output characteristics. See the second example data deck in that section of the guide.

1.9.4. .NODESET Card

General form:

.NODESET V(NODNUM)=VAL V(NODNUM)=VAL ...

Examples:

.NODESET V(12)=4.5 V(4)=2.23

This card helps the program find the dc or initial transient solution by making a preliminary pass with the specified nodes held to the given voltages. The restriction is then released and the iteration continues to the true solution. The .NODESET card may be necessary for convergence on bistable or astable circuits. In general, this card should not be necessary.

1.9.5. .IC Card

General form:

.IC V(NODNUM)=VAL V(NODNUM)=VAL ...

Examples:

.IC V(11)=5 V(4)=-5 V(2)=2.2

This card is for setting transient initial conditions. It has two different interpretations, depending on whether the UIC parameter is specified on the .TRAN card. Also, one should not confuse this card with the .NODESET card. The .NODESET card is only to help dc convergence, and does not affect final bias solution (except for multi-stable circuits). The two interpretations of this card are as follows:

1. When the UIC parameter is specified on the .TRAN card, then the node voltages specified on the .IC card are used to compute the capacitor, diode, BJT, JFET, and MOSFET initial conditions. This is equivalent to specifying the IC=... parameter on each device card, but is much more convenient. The IC=... parameter can still be specified and will take precedence over the .IC values. Since no dc bias (initial transient) solution is computed before the transient analysis, one should take care to specify all dc source voltages on the .IC card if they are to be used to compute device initial conditions.

2. When the UIC parameter is not specified on the .TRAN card, the dc bias (initial transient) solution will be computed before the transient analysis. In this case, the node voltages specified on the .IC card will be forced to the desired initial values during the bias solution. During transient analysis, the constraint on these node voltages is removed. This is the preferred method since it allows SPICE to compute a consistent dc solution.

1.9.6. .TF Card

General form:

.TF OUTVAR INSRC

Examples:

.TF V(5, 3) VIN
.TF I(VLOAD) VIN

This card defines the small-signal output and input for the dc small- signal analysis. OUTVAR is the small-signal output variable and INSRC is the small-signal input source. If this card is included, SPICE will compute the dc small-signal value of the transfer function (output/input), input resistance, and output resistance. For the first example, SPICE would compute the ratio of V(5, 3) to VIN, the small-signal input resistance at VIN, and the small-signal output resistance measured across nodes 5 and 3.

1.9.7. .AC Card

General form:

```
.AC DEC ND FSTART FSTOP
.AC OCT NO FSTART FSTOP
.AC LIN NP FSTART FSTOP
```

Examples:

```
.AC DEC 10 1 10K
.AC DEC 10 1K 100MEG
.AC LIN 100 1 100HZ
```

DEC stands for decade variation, and ND is the number of points per decade. OCT stands for octave variation, and NO is the number of points per octave. LIN stands for linear variation, and NP is the number of points. FSTART is the starting frequency, and FSTOP is the final frequency. If this card is included in the deck, SPICE will perform an ac analysis of the circuit over the specified frequency range. Note that in order for this analysis to be meaningful, at least one independent source must have been specified with an ac value.

1.9.8. .TRAN Card

General form:

```
.TRAN TSTEP TSTOP <TSTART <TMAX>>
```

Examples:

```
.TRAN 1NS 100NS
.TRAN 1NS 1000NS 500NS
.TRAN 10NS 1US
```

TSTEP is the printing or plotting increment for line-printer output. For use with the post-processor, TSTEP is the suggested computing increment. TSTOP is the final time, and TSTART is the initial time. If TSTART is omitted, it is assumed to be zero. The transient analysis always begins at time zero. In the interval <zero, TSTART>, the circuit is analyzed (to reach a steady state), but no outputs are stored. In the interval <TSTART, TSTOP>, the circuit is analyzed and outputs are stored. TMAX is the maximum stepsize that SPICE will use (for default, the program chooses either TSTEP or (TSTOP-TSTART)/50.0, whichever is smaller. TMAX is useful when one wishes to guarantee a computing interval which is smaller than the printer increment, TSTEP.

UIC (use initial conditions) is an optional keyword which indicates that the user does not want SPICE to solve for the quiescent operating point before beginning the transient analysis. If this keyword is specified, SPICE uses the values specified using IC=... on the various elements as the initial transient condition and proceeds with the analysis. If the .IC card has been specified, then the node voltages on the .IC card are used to compute the initial conditions for the devices. Look at the description on the .IC card for its interpretation when UIC is not specified.

1.9.9. .PZ Card

General form:

```
.PZ NODE1 NODE2 NODE3 NODE4 CUR POL
.PZ NODE1 NODE2 NODE3 NODE4 CUR ZER
.PZ NODE1 NODE2 NODE3 NODE4 CUR PZ
.PZ NODE1 NODE2 NODE3 NODE4 VOL POL
.PZ NODE1 NODE2 NODE3 NODE4 VOL ZER
.PZ NODE1 NODE2 NODE3 NODE4 VOL PZ
```

Examples:

```
.PZ 1 0 3 0 CUR POL
```

```
.PZ 2 3 5 0 VOL ZER
.PZ 4 1 4 1 CUR PZ
```

CUR stands for a transfer function of the type (output voltage)/(input current) while VOL stands for a transfer function of the type (output voltage)/(input voltage). POL stands for pole analysis only, ZER for zero analysis only and PZ for both. This feature is provided mainly because if there is a nonconvergence in finding poles or zeros, then, at least the other can be found. Finally, NODE1 and NODE2 are the two input nodes and NODE3 and NODE4 are the two output nodes. Thus, there is complete freedom regarding the output and input ports and the type of transfer function.

In interactive mode, the command syntax is the same except that the first field is PZ instead of .PZ. To print the results, one should use the command 'print all'.

1.9.10. .FOUR Card

The .FOUR card used by SPICE2 to request fourier analysis of outputs has been replaced by the fourier command in Nutmeg, the interactive SPICE3 front end. For details of this command, see the manual for Nutmeg.

1.10. Parameter description summary

The following tables summarize the parameters available on each of the devices and models in SPICE3. There are up to four tables for each type of device supported by SPICE3. Input parameters to instances and models are simply parameter that can occur on an instance or model definition line in the form "keyword=value" where "keyword" is the parameter name as given in the tables. Output parameters are those additional parameters which are available for many types of instances for the output of operating point and debugging information. These parameters are specified as "@device[keyword]" and are available for the most recent point computed or, if specified in a

".save" statement, for an entire simulation as a normal output vector. Thus, to monitor the gate to source capacitance of a MOSFET, a command

save @m1[cgs]

given before a transient simulation will cause the specified capacitance value to be saved at each timepoint, and a subsequent command such as

plot @m1[cgs]

will produce the desired plot.

Some variables are listed as both input and output, and their output will simply return the previously input value, or the default value after the simulation has been run. Some parameter are input only because the output system can not handle variables of the given type yet, or the need for them as output variables has not been apparent. Many such input variables are available as output variables in a different format, such as the initial condition vectors that can be retrieved as individual initial condition values. Finally, internally derived values are output only and are provided for debugging and operating point output purposes.

Please note that these tables do not provide the detailed information available about the parameters provided in the section on each device and model, but are provided as a quick reference guide.

1.10.1. Arbitrary Source

Input only instance parameters for Arbitrary Source (ASRC)

Parm. name	Description
i	Current source
v	Voltage source

Output only instance parameters for Arbitrary Source (ASRC)

Parm. name	Description
pos_node	Positive Node
neg_node	Negative Node

1.10.2. Bipolar Junction Transistor

Input only instance parameters for Bipolar Junction Transistor (BJT)

Parm. name	Description
ic	Initial condition vector
sens_area	flag to request sensitivity WRT area

Output only instance parameters for Bipolar Junction Transistor (BJT)

Parm. name	Description
colnode	Number of collector node
basenode	Number of base node
emitnode	Number of emitter node
substnode	Number of substrate node
colprimenode	Internal collector node
baseprimenode	Internal base node
emitprimenode	Internal emitter node
vbe	B-E voltage
vbc	B-C voltage
cc	Current at collector node
cb	Current at base node
gpi	Small signal input conductance - pi
gmu	Small signal conductance - mu
gm	Small signal transconductance
go	Small signal output conductance
qbe	Charge storage B-E junction
cqbe	Cap. due to charge storage in B-E jct.
qbc	Charge storage B-C junction
cqbc	Cap. due to charge storage in B-C jct.
qcs	Charge storage C-S junction
cqcs	Cap. due to charge storage in C-S jct.
qbx	Charge storage B-X junction
cqbx	Cap. due to charge storage in B-X jct.
gx	Conductance from base to internal base
cexbc	Total Capacitance in B-X junction
geqcb	d(Ibe)/d(Vbc)
gccs	Internal C-S cap. equiv. cond.
geqbx	Internal C-B-base cap. equiv. cond.
ce	Emitter current
cs	Substrate current
p	Power dissipation
sens_dc	dc sensitivity
sens_real	real part of ac sensitivity
sens_imag	dc sens. & imag part of ac sens.
sens_mag	sensitivity of ac magnitude
sens_ph	sensitivity of ac phase
sens_cplx	ac sensitivity

Input/Output instance parameters for Bipolar Junction Transistor (BJT)

Parm. name	Description
off	Device initially off
icvbe	Initial B-E voltage
icvce	Initial C-E voltage
area	Area factor
temp	instance temperature

Model parameters for Bipolar Junction Transistor (BJT)

Parm. name	Description
off	Device initially off
icvbe	Initial B-E voltage
icvce	Initial C-E voltage
area	Area factor
ic	Initial condition vector
sens_area	flag to request sensitivity WRT area
colnode	Number of collector node
basenode	Number of base node
emitnode	Number of emitter node
substnode	Number of substrate node
colprimenode	Internal collector node
baseprimenode	Internal base node
emitprimenode	Internal emitter node
vbe	B-E voltage
vbc	B-C voltage
cc	Current at collector node
cb	Current at base node
gpi	Small signal input conductance - pi
gmu	Small signal conductance - mu
gm	Small signal transconductance
go	Small signal output conductance
qbe	Charge storage B-E junction
cqbe	Cap. due to charge storage in B-E jct.
qbc	Charge storage B-C junction
cqbc	Cap. due to charge storage in B-C jct.
qcs	Charge storage C-S junction
cqcs	Cap. due to charge storage in C-S jct.
qbx	Charge storage B-X junction
cqbx	Cap. due to charge storage in B-X jct.
gx	Conductance from base to internal base
cexbc	Total Capacitance in B-X junction
geqcb	d(Ibe)/d(Vbc)
gccs	Internal C-S cap. equiv. cond.
geqbx	Internal C-B-base cap. equiv. cond.
ce	Emitter current
cs	Substrate current
p	Power dissipation
sens_dc	dc sensitivity

Model parameters for Bipolar Junction Transistor (BJT)

Parm. name	Description
sens_real	real part of ac sensitivity
sens_imag	dc sens. & imag part of ac sens.
sens_mag	sensitivity of ac magnitude
sens_ph	sensitivity of ac phase
sens_cplx	ac sensitivity
temp	instance temperature
npn	NPN type device
pnp	PNP type device
is	Saturation Current
bf	Ideal forward beta
nf	Forward emission coefficient
vaf	Forward Early voltage
va	Forward Early voltage
ikf	Forward beta roll-off corner current
ik	Forward beta roll-off corner current
ise	B-E leakage saturation current
c2	Obsolete parameter name
ne	B-E leakage emission coefficient
br	Ideal reverse beta
nr	Reverse emission coefficient
var	Reverse Early voltage
vb	Reverse Early voltage
ikr	reverse beta roll-off corner current

1.10.3. Berkeley Short Channel IGFET Model

Input only instance parameters for Berkeley Short Channel IGFET Model (BSIM)

Parm. name	Description
ic	Vector of DS,GS,BS initial voltages

Input/Output instance parameters for Berkeley Short Channel IGFET Model (BSIM)

Parm. name	Description
l	Length
w	Width
ad	Drain area
as	Source area
pd	Drain perimeter
ps	Source perimeter
nrd	Number of squares in drain
nrs	Number of squares in source
off	Device is initially off

Input/Output instance parameters for Berkeley Short Channel IGFET Model (BSIM)

Parm. name	Description
vds	Initial D-S voltage
vgs	Initial G-S voltage
vbs	Initial B-S voltage

Model parameters for Berkeley Short Channel IGFET Model (BSIM)

Parm. name	Description
l	Length
w	Width
ad	Drain area
as	Source area
pd	Drain perimeter
ps	Source perimeter
nrd	Number of squares in drain
nrs	Number of squares in source
off	Device is initially off
vds	Initial D-S voltage
vgs	Initial G-S voltage
vbs	Initial B-S voltage
ic	Vector of DS,GS,BS initial voltages
vfb	Flat band voltage
lvfb	Length dependence of vfb
wvfb	Width dependence of vfb
phi	Strong inversion surface potential
lphi	Length dependence of phi
wphi	Width dependence of phi
k1	Bulk effect coefficient 1
lk1	Length dependence of k1
wk1	Width dependence of k1
k2	Bulk effect coefficient 2
lk2	Length dependence of k2
wk2	Width dependence of k2
eta	VDS dependence of threshold voltage
leta	Length dependence of eta
weta	Width dependence of eta
x2e	VBS dependence of eta
lx2e	Length dependence of x2e
wx2e	Width dependence of x2e
x3e	VDS dependence of eta
lx3e	Length dependence of x3e
wx3e	Width dependence of x3e
dl	Channel length reduction in um
dw	Channel width reduction in um
muz	Zero field mobility at VDS=0 VGS=VTH
x2mz	VBS dependence of muz
lx2mz	Length dependence of x2mz
wx2mz	Width dependence of x2mz

Model parameters for Berkeley Short Channel IGFET Model (BSIM)

Parm. name	Description
mus	Mobility at VDS=VDD VGS=VTH, channel length modulation
lmus	Length dependence of mus
wmus	Width dependence of mus
x2ms	VBS dependence of mus
lx2ms	Length dependence of x2ms
wx2ms	Width dependence of x2ms
x3ms	VDS dependence of mus
lx3ms	Length dependence of x3ms
wx3ms	Width dependence of x3ms
u0	VGS dependence of mobility
lu0	Length dependence of u0
wu0	Width dependence of u0
x2u0	VBS dependence of u0
lx2u0	Length dependence of x2u0
wx2u0	Width dependence of x2u0
u1	VDS depence of mobility, velocity saturation
lu1	Length dependence of u1
wu1	Width dependence of u1
x2u1	VBS depence of u1
lx2u1	Length depence of x2u1
wx2u1	Width depence of x2u1
x3u1	VDS depence of u1
lx3u1	Length dependence of x3u1
wx3u1	Width depence of x3u1
n0	Subthreshold slope
ln0	Length dependence of n0
wn0	Width dependence of n0
nb	VBS dependence of subthreshold slope
lnb	Length dependence of nb
wnb	Width dependence of nb
nd	VDS dependence of subthreshold slope
lnd	Length dependence of nd
wnd	Width dependence of nd
tox	Gate oxide thickness in um
temp	Temperature in degree Celcius
vdd	Supply voltage to specify mus
cgso	Gate source overlap capacitance per unit channel width(m)
cgdo	Gate drain overlap capacitance per unit channel width(m)
cgbo	Gate bulk overlap capacitance per unit channel length(m)

1.10.4. Fixed capacitor

Input only instance parameters for Fixed capacitor (Capacitor)

Parm. name	Description
sens_cap	flag to request sens. WRT cap.

Output only instance parameters for Fixed capacitor (Capacitor)

Parm. name	Description
c	Device current
p	Instantaneous device power
sens_dc	dc sensitivity
sens_real	real part of ac sensitivity
sens_imag	dc sens. & imag part of ac sens.
sens_mag	sensitivity of ac magnitude
sens_ph	sensitivity of ac phase
sens_cplx	ac sensitivity

Input/Output instance parameters for Fixed capacitor (Capacitor)

Parm. name	Description
capacitance	Device capacitance
ic	Initial capacitor voltage
w	Device width
l	Device length

Model parameters for Fixed capacitor (Capacitor)

Parm. name	Description
capacitance	Device capacitance
ic	Initial capacitor voltage
w	Device width
l	Device length
sens_cap	flag to request sens. WRT cap.

1.10.5. Current controlled current source

Input only instance parameters for Current controlled current source (CCCS)

Parm. name	Description
sens_gain	flag to request sensitivity WRT gain

Output only instance parameters for Current controlled current source (CCCS)

Parm. name	Description
neg_node	Negative node of source
pos_node	Positive node of source
c	CCCS current
p	CCCS current
sens_dc	dc sensitivity
sens_real	real part of ac sensitivity
sens_imag	imag part of ac sensitivity
sens_mag	sensitivity of ac magnitude
sens_ph	sensitivity of ac phase
sens_cplx	ac sensitivity

Input/Output instance parameters for Current controlled current source (CCCS)

Parm. name	Description
gain	Gain of source
control	Name of controlling source

1.10.6. Linear current controlled current source

Input only instance parameters for Linear current controlled current source (CCVS)

Parm. name	Description
sens_trans	flag to request sens. WRT transimpedance

Output only instance parameters for Linear current controlled current source (CCVS)

Parm. name	Description
pos_node	Positive node of source
neg_node	Negative node of source
c	Device current
p	Device power
sens_dc	dc sensitivity
sens_real	real part of ac sensitivity
sens_imag	imag part of ac sensitivity
sens_mag	sensitivity of ac magnitude
sens_ph	sensitivity of ac phase
sens_cplx	ac sensitivity

Input/Output instance parameters for Linear current controlled current source (CCVS)

Parm. name	Description
gain	Transresistance (gain)
control	Controlling voltage source

1.10.7. Current controlled ideal switch

Input only instance parameters for Current controlled ideal switch (CSwitch)

Parm. name	Description
on	Initially closed
off	Initially open

Output only instance parameters for Current controlled ideal switch (CSwitch)

Parm. name	Description
pos_node	Positive node of switch
neg_node	Negative node of switch
c	Switch current
p	Instantaneous power

Input/Output instance parameters for Current controlled ideal switch (CSwitch)

Parm. name	Description
control	Name of controlling source

Model parameters for Current controlled ideal switch (CSwitch)

Parm. name	Description
control	Name of controlling source
on	Initially closed
off	Initially open
pos_node	Positive node of switch
neg_node	Negative node of switch
c	Switch current
p	Instantaneous power

1.10.8. Junction Diode model

Input only instance parameters for Junction Diode model (Diode)

Parm. name	Description
sens_area	flag to request sensitivity WRT area

Output only instance parameters for Junction Diode model (Diode)

Parm. name	Description
voltage	Diode voltage
current	Diode current
charge	Diode capacitor charge
capcur	Diode capacitor current
cond	Diode conductance
p	Diode power
c	Diode current
sens_dc	dc sensitivity
sens_real	dc sens. and real part of ac sensitivity
sens_imag	imag part of ac sensitivity
sens_mag	sensitivity of ac magnitude
sens_ph	sensitivity of ac phase
sens_cplx	ac sensitivity

Input/Output instance parameters for Junction Diode model (Diode)

Parm. name	Description
off	Initially off
temp	Instance temperature
ic	Initial device voltage
area	Area factor

Model parameters for Junction Diode model (Diode)

Parm. name	Description
off	Initially off
temp	Instance temperature
ic	Initial device voltage
area	Area factor
sens_area	flag to request sensitivity WRT area
voltage	Diode voltage
current	Diode current
charge	Diode capacitor charge
capcur	Diode capacitor current
cond	Diode conductance
p	Diode power
c	Diode current
sens_dc	dc sensitivity
sens_real	dc sens. and real part of ac sensitivity
sens_imag	imag part of ac sensitivity
sens_mag	sensitivity of ac magnitude

1.10.9. Inductors

Input only instance parameters for Inductors (Inductor)

Parm. name	Description
sens_ind	flag to request sensitivity WRT inductance

Output only instance parameters for Inductors (Inductor)

Parm. name	Description
flux	Flux through inductor
volt	Terminal voltage of inductor
current	Current through the inductor
p	instantaneous power dissipated by the inductor
sens_dc	dc sensitivity sensitivity

Output only instance parameters for Inductors (Inductor)

Parm. name	Description
sens_real	real part of ac sensitivity
sens_imag	dc sensitivity and imag part of ac sensitivty
sens_mag	sensitivity of AC magnitude
sens_ph	sensitivity of AC phase
sens_cplx	ac sensitivity

Input/Output instance parameters for Inductors (Inductor)

Parm. name	Description
inductance	Inductance of inductor
ic	Initial current through inductor

1.10.10. Independent current source

Input only instance parameters for Independent current source (Isource)

Parm. name	Description
pulse	Pulse description
sine	Sinusoidal source description
sin	Sinusoidal source description
exp	Exponential source description
pwl	Piecewise linear description
sffm	single freq. FM description
ac	AC magnitude,phase vector
p	Power supplied by the source
c	Current through current source

Output only instance parameters for Independent current source (Isource)

Parm. name	Description
neg_node	Negative node of source
pos_node	Positive node of source
acreal	AC real part
acimag	AC imaginary part
function	Function of the source
order	Order of the source function
coeffs	Coefficients of the source

Input/Output instance parameters for Independent current source (Isource)

Parm. name	Description
dc	DC value of source
acmag	AC magnitude
acphase	AC phase

1.10.11. Junction Field effect transistor

Output only instance parameters for Junction Field effect transistor (JFET)

Parm. name	Description
drain-node	Number of drain node
gate-node	Number of gate node
source-node	Number of source node
drain-prime-node	Internal drain node
source-prime-node	Internal source node
vgs	Voltage G-S
vgd	Voltage G-D
cg	Current at gate node
cd	Current at drain node
cgd	Current G-D
gm	Transconductance
gds	Conductance D-S
ggs	Conductance G-S
ggd	Conductance G-D
qgs	Charge storage G-S junction
cqgs	Capacitance due to charge storage G-S junction
qgd	Charge storage G-D junction
cqgd	Capacitance due to charge storage G-D junction
cs	Source current
p	Power dissipated by the JFET

Input/Output instance parameters for Junction Field effect transistor (JFET)

Parm. name	Description
off	Device initially off
ic	Initial VDS,VGS vector
area	Area factor
ic-vds	Initial D-S voltage
ic-vgs	Initial G-S volrage
temp	Instance temperature

Model parameters for Junction Field effect transistor (JFET)

Parm. name	Description
off	Device initially off
ic	Initial VDS,VGS vector
area	Area factor
ic-vds	Initial D-S voltage
ic-vgs	Initial G-S volrage
temp	Instance temperature
drain-node	Number of drain node
gate-node	Number of gate node
source-node	Number of source node
drain-prime-node	Internal drain node
source-prime-node	Internal source node
vgs	Voltage G-S
vgd	Voltage G-D
cg	Current at gate node
cd	Current at drain node
cgd	Current G-D

1.10.12. GaAs MESFET model

Output only instance parameters for GaAs MESFET model (MES)

Parm. name	Description
off	Device initially off
dnode	Number of drain node
gnode	Number of gate node
snode	Number of source node
dprimenode	Number of internal drain node
sprimenode	Number of internal source node
vgs	Gate-Source voltage
vgd	Gate-Drain voltage
cg	Gate capacitance
cd	Drain capacitance
cgd	Gate_Drain capacitance
gm	Transconductance
gds	Drain-Source conductance
ggs	Gate-Source conductance
ggd	Gate-Drain conductance
qgs	Gate-Source charge storage
cqgs	Capacitance due to gate-source charge storage
qgd	Gate-Drain charge storage
cqgd	Capacitance due to gate-drain charge storage
cs	Source current
p	Power dissipated by the mesfet

Input/Output instance parameters for GaAs MESFET model (MES)

Parm. name	Description
area	Area factor
icvds	Initial D-S voltage
icvgs	Initial G-S voltage

Model parameters for GaAs MESFET model (MES)

Parm. name	Description
off	Device initially off
area	Area factor
icvds	Initial D-S voltage
icvgs	Initial G-S voltage
dnode	Number of drain node
gnode	Number of gate node
snode	Number of source node
dprimenode	Number of internal drain node
sprimenode	Number of internal source node
vgs	Gate-Source voltage
vgd	Gate-Drain voltage
cg	Gate capacitance
cd	Drain capacitance
cgd	Gate_Drain capacitance
gm	Transconductance
gds	Drain-Source conductance
ggs	Gate-Source conductance
ggd	Gate-Drain conductance
qgs	Gate-Source charge storage

1.10.13. Level 1 MOSfet model with Meyer capacitance model

Input only instance parameters for Level 1 MOSfet model with Meyer capacitance model (Mos1)

Parm. name	Description
off	Device initially off
ic	Vector of D-S, G-S, B-S voltages
sens_l	flag to request sensitivity WRT length
sens_w	flag to request sensitivity WRT width

Output only instance parameters for Level 1 MOSfet model with Meyer capacitance model (Mos1)

Parm. name	Description
cgs	Gate-Source capacitance
cgd	Gate-Drain capacitance
dnode	Number of the drain node
gnode	Number of the gate node
snode	Number of the source node
bnode	Number of the node
dnodeprime	Number of int. drain node
snodeprime	Number of int. source node
sourceconductance	Conductance of source
drainconductance	Conductance of drain
von	
vdsat	Saturation drain voltage
sourcevcrit	Critical source voltage
drainvcrit	Critical drain voltage
cd	Drain current
cbs	B-S junction capacitance
cbd	B-D junction capacitance
gmbs	Bulk-Source transconductance
gm	Transconductance
gds	Drain-Source conductance
gbd	Bulk-Drain conductance
gbs	Bulk-Source conductance
capbd	Bulk-Drain capacitance
capbs	Bulk-Source capacitance
cbd0	Zero-Bias B-D junction capacitance
cbdsw0	
cbs0	Zero-Bias B-S junction capacitance
cbssw0	
vbd	Bulk-Drain voltage
vbs	Bulk-Source voltage
vgs	Gate-Source voltage
vds	Drain-Source voltage
capgs	Gate-Source capacitance
qgs	Gate-Source charge storage
cqgs	Capacitance due to gate-source charge storage
capgd	Gate-Drain capacitance
qgd	Gate-Drain charge storage
cqgd	Capacitance due to gate-drain charge storage
capgb	Gate-Bulk capacitance
qgb	Gate-Bulk charge storage
cqgb	Capacitance due to gate-bulk charge storage
qbd	Bulk-Drain charge storage
cqbd	Capacitance due to bulk-drain charge storage
qbs	Bulk-Source charge storage
cqbs	Capacitance due to bulk-source charge storage
cs	Source current
cg	Gate current
cb	Bulk current
p	Instaneous power
sens_l_dc	dc sensitivity wrt length

Output only instance parameters for Level 1 MOSfet model with Meyer capacitance model (Mos1)

Parm. name	Description
sens_l_real	real part of ac sensitivity wrt length
sens_l_imag	imag part of ac sensitivity wrt length
sens_l_mag	sensitivity wrt l of ac magnitude
sens_l_ph	sensitivity wrt l of ac phase
sens_l_cplx	ac sensitivity wrt length
sens_w_dc	dc sensitivity wrt width
sens_w_real	real part of ac sensitivity wrt width
sens_w_imag	imag part of ac sensitivity wrt width
sens_w_mag	sensitivity wrt w of ac magnitude
sens_w_ph	sensitivity wrt w of ac phase
sens_w_cplx	ac sensitivity wrt width

Input/Output instance parameters for Level 1 MOSfet model with Meyer capacitance model (Mos1)

Parm. name	Description
l	Length
w	Width
ad	Drain area
as	Source area
pd	Drain perimeter
ps	Source perimeter
nrd	Drain squares
nrs	Source squares
icvds	Initial D-S voltage
icvgs	Initial G-S voltage
icvbs	Initial B-S voltage
temp	Instance temperature

Model parameters for Level 1 MOSfet model with Meyer capacitance model (Mos1)

Parm. name	Description
l	Length
w	Width
ad	Drain area
as	Source area
pd	Drain perimeter
ps	Source perimeter
nrd	Drain squares
nrs	Source squares
off	Device initially off
icvds	Initial D-S voltage
icvgs	Initial G-S voltage
icvbs	Initial B-S voltage
temp	Instance temperature

Model parameters for Level 1 MOSfet model with Meyer capacitance model (Mos1)

Parm. name	Description
ic	Vector of D-S, G-S, B-S voltages
sens_l	flag to request sensitivity WRT length
sens_w	flag to request sensitivity WRT width
cgs	Gate-Source capacitance
cgd	Gate-Drain capacitance
dnode	Number of the drain node
gnode	Number of the gate node
snode	Number of the source node
bnode	Number of the node
dnodeprime	Number of int. drain node
snodeprime	Number of int. source node
sourceconductance	Conductance of source
drainconductance	Conductance of drain
von	
vdsat	Saturation drain voltage
sourcevcrit	Critical source voltage
drainvcrit	Critical drain voltage
cd	Drain current
cbs	B-S junction capacitance

1.10.14. Level 2 MOSfet model with Meyer capacitance model

Input only instance parameters for Level 2 MOSfet model with Meyer capacitance model (Mos2)

Parm. name	Description
off	Device initially off
ic	Vector of D-S, G-S, B-S voltages
sens_l	flag to request sensitivity WRT length
sens_w	flag to request sensitivity WRT width

Output only instance parameters for Level 2 MOSfet model with Meyer capacitance model (Mos2)

Parm. name	Description
cgs	Gate-Source capacitance
cgd	Gate-Drain capacitance
dnode	Number of drain node
gnode	Number of gate node
snode	Number of source node
bnode	Number of bulk node
dnodeprime	Number of internal drain node
snodeprime	Number of internal source node
sourceconductance	Source conductance
drainconductance	Drain conductance

Output only instance parameters for Level 2 MOSfet model with Meyer capacitance model (Mos2)

Parm. name	Description
von	
vdsat	Saturation drain voltage
sourcevcrit	Critical source voltage
drainvcrit	Critical drain voltage
cd	Drain current
cbs	B-S junction capacitance
cbd	B-D junction capacitance
gmbs	Bulk-Source transconductance
gm	Transconductance
gds	Drain-Source conductance
gbd	Bulk-Drain conductance
gbs	Bulk-Source conductance
capbd	Bulk-Drain capacitance
capbs	Bulk-Source capacitance
cbd0	Zero-Bias B-D junction capacitance
cbdsw0	
cbs0	Zero-Bias B-S junction capacitance
cbssw0	
vbd	Bulk-Drain voltage
vbs	Bulk-Source voltage
vgs	Gate-Source voltage
vds	Drain-Source voltage
capgs	Gate-Source capacitance
qgs	Gate-Source charge storage
cqgs	Capacitance due to gate-source charge storage
capgd	Gate-Drain capacitance
qgd	Gate-Drain charge storage
cqgd	Capacitance due to gate-drain charge storage
capgb	Gate-Bulk capacitance
qgb	Gate-Bulk charge storage
cqgb	Capacitance due to gate-bulk charge storage
qbd	Bulk-Drain charge storage
cqbd	Capacitance due to bulk-drain charge storage
qbs	Bulk-Source charge storage
cqbs	Capacitance due to bulk-source charge storage
cs	Source current
cg	Gate current
cb	Bulk current
p	Instantaneous power
sens_l_dc	dc sensitivity wrt length
sens_l_real	real part of ac sensitivity wrt length
sens_l_imag	imag part of ac sensitivity wrt length
sens_l_cplx	ac sensitivity wrt length
sens_l_mag	sensitivity wrt l of ac magnitude
sens_l_ph	sensitivity wrt l of ac phase
sens_w_dc	dc sensitivity wrt width
sens_w_real	dc sensitivity and real part of ac sensitivity wrt width
sens_w_imag	imag part of ac sensitivity wrt width
sens_w_mag	sensitivity wrt w of ac magnitude
sens_w_ph	sensitivity wrt w of ac phase
sens_w_cplx	ac sensitivity wrt width

Output only instance parameters for Level 2 MOSfet model with Meyer capacitance model (Mos2)

Parm. name	Description

Input/Output instance parameters for Level 2 MOSfet model with Meyer capacitance model (Mos2)

Parm. name	Description
l	Length
w	Width
ad	Drain area
as	Source area
pd	Drain perimeter
ps	Source perimeter
nrd	Drain squares
nrs	Source squares
icvds	Initial D-S voltage
icvgs	Initial G-S voltage
icvbs	Initial B-S voltage
temp	Instance operating temperature

Model parameters for Level 2 MOSfet model with Meyer capacitance model (Mos2)

Parm. name	Description
l	Length
w	Width
ad	Drain area
as	Source area
pd	Drain perimeter
ps	Source perimeter
nrd	Drain squares
nrs	Source squares
off	Device initially off
icvds	Initial D-S voltage
icvgs	Initial G-S voltage
icvbs	Initial B-S voltage
temp	Instance operating temperature
ic	Vector of D-S, G-S, B-S voltages
sens_l	flag to request sensitivity WRT length
sens_w	flag to request sensitivity WRT width
cgs	Gate-Source capacitance
cgd	Gate-Drain capacitance
dnode	Number of drain node
gnode	Number of gate node
snode	Number of source node
bnode	Number of bulk node
dnodeprime	Number of internal drain node
snodeprime	Number of internal source node
sourceconductance	Source conductance
drainconductance	Drain conductance
von	
vdsat	Saturation drain voltage
sourcevcrit	Critical source voltage

Model parameters for Level 2 MOSfet model with Meyer capacitance model (Mos2)

Parm. name	Description
drainvcrit	Critical drain voltage
cd	Drain current
cbs	B-S junction capacitance
cbd	B-D junction capacitance
gmbs	Bulk-Source transconductance
gm	Transconductance
gds	Drain-Source conductance
gbd	Bulk-Drain conductance
gbs	Bulk-Source conductance
capbd	Bulk-Drain capacitance

1.10.15. Level 3 MOSfet model with Meyer capacitance model

Input only instance parameters for Level 3 MOSfet model with Meyer capacitance model (Mos3)

Parm. name	Description
off	Device initially off
sens_l	flag to request sensitivity WRT length
sens_w	flag to request sensitivity WRT width

Output only instance parameters for Level 3 MOSfet model with Meyer capacitance model (Mos3)

Parm. name	Description
cgs	Gate-Source capacitance
cgd	Gate-Drain capacitance
dnode	Number of drain node
gnode	Number of gate node
snode	Number of source node
bnode	Number of bulk node
dnodeprime	Number of internal drain node
snodeprime	Number of internal source node
sourceconductance	Source conductance
drainconductance	Drain conductance
von	
vdsat	Saturation drain voltage
sourcevcrit	Critical source voltage
drainvcrit	Critical drain voltage
cd	Drain current
cbs	B-S junction capacitance
cbd	B-D junction capacitance
gmbs	Bulk-Source transconductance
gm	Transconductance
gds	Drain-Source conductance

Output only instance parameters for Level 3 MOSfet model with Meyer capacitance model (Mos3)

Parm. name	Description
gbd	Bulk-Drain conductance
gbs	Bulk-Source conductance
capbd	Bulk-Drain capacitance
capbs	Bulk-Source capacitance
cbd0	Zero-Bias B-D junction capacitance
cbdsw0	
cbs0	Zero-Bias B-S junction capacitance
cbssw0	
vbd	Bulk-Drain voltage
vbs	Bulk-Source voltage
vgs	Gate-Source voltage
vds	Drain-Source voltage
capgs	Gate-Source capacitance
qgs	Gate-Source charge storage
cqgs	Capacitance due to gate-source charge storage
capgd	Gate-Drain capacitance
qgd	Gate-Drain charge storage
cqgd	Capacitance due to gate-drain charge storage
capgb	Gate-Bulk capacitance
qgb	Gate-Bulk charge storage
cqgb	Capacitance due to gate-bulk charge storage
qbd	Bulk-Drain charge storage
cqbd	Capacitance due to bulk-drain charge storage
qbs	Bulk-Source charge storage
cqbs	Capacitance due to bulk-source charge storage
cs	Source current
cg	Gate current
cb	Bulk current
p	Instantaneous power
sens_l_dc	dc sensitivity wrt length
sens_l_real	real part of ac sensitivity wrt length
sens_l_imag	imag part of ac sensitivity wrt length
sens_l_cplx	ac sensitivity wrt length
sens_l_mag	sensitivity wrt l of ac magnitude
sens_l_ph	sensitivity wrt l of ac phase
sens_w_dc	dc sensitivity wrt width
sens_w_real	real part of ac sensitivity wrt width
sens_w_imag	imag part of ac sensitivity wrt width
sens_w_mag	sensitivity wrt w of ac magnitude
sens_w_ph	sensitivity wrt w of ac phase
sens_w_cplx	ac sensitivity wrt width

Input/Output instance parameters for Level 3 MOSfet model with Meyer capacitance model (Mos3)

Parm. name	Description
l	Length
w	Width
ad	Drain area
as	Source area
pd	Drain perimeter
ps	Source perimeter
nrd	Drain squares
nrs	Source squares
icvds	Initial D-S voltage
icvgs	Initial G-S voltage
icvbs	Initial B-S voltage
ic	Vector of D-S, G-S, B-S voltages
temp	Instance operating temperature

Model parameters for Level 3 MOSfet model with Meyer capacitance model (Mos3)

Parm. name	Description
l	Length
w	Width
ad	Drain area
as	Source area
pd	Drain perimeter
ps	Source perimeter
nrd	Drain squares
nrs	Source squares
off	Device initially off
icvds	Initial D-S voltage
icvgs	Initial G-S voltage
icvbs	Initial B-S voltage
ic	Vector of D-S, G-S, B-S voltages
temp	Instance operating temperature
sens_l	flag to request sensitivity WRT length
sens_w	flag to request sensitivity WRT width
cgs	Gate-Source capacitance
cgd	Gate-Drain capacitance
dnode	Number of drain node
gnode	Number of gate node
snode	Number of source node
bnode	Number of bulk node
dnodeprime	Number of internal drain node
snodeprime	Number of internal source node
sourceconductance	Source conductance
drainconductance	Drain conductance
von	
vdsat	Saturation drain voltage
sourcevcrit	Critical source voltage
drainvcrit	Critical drain voltage

Model parameters for Level 3 MOSfet model with Meyer capacitance model (Mos3)

Parm. name	Description
cd	Drain current
cbs	B-S junction capacitance
cbd	B-D junction capacitance
gmbs	Bulk-Source transconductance
gm	Transconductance
gds	Drain-Source conductance
gbd	Bulk-Drain conductance
gbs	Bulk-Source conductance
capbd	Bulk-Drain capacitance
capbs	Bulk-Source capacitance
cbd0	Zero-Bias B-D junction capacitance

1.10.16. Simple linear resistor

Input only instance parameters for Simple linear resistor (Resistor)

Parm. name	Description
sens_resist	flag to request sensitivity WRT resistance

Output only instance parameters for Simple linear resistor (Resistor)

Parm. name	Description
sens_dc	dc sensitivity
sens_real	dc sensitivity and real part of ac sensitivity
sens_imag	dc sensitivity and imag part of ac sensitivity
sens_mag	ac sensitivity of magnitude
sens_ph	ac sensitivity of phase
sens_cplx	ac sensitivity

Input/Output instance parameters for Simple linear resistor (Resistor)

Parm. name	Description
resistance	Resistance
w	Width
l	Length
c	Current
p	Power
temp	Instance operating temperature

Model parameters for Simple linear resistor (Resistor)

Parm. name	Description
resistance	Resistance
w	Width
l	Length
c	Current
p	Power
sens_resist	flag to request sensitivity WRT resistance
sens_dc	dc sensitivity

1.10.17. Ideal voltage controlled switch

Input only instance parameters for Ideal voltage controlled switch (Switch)

Parm. name	Description
on	Switch initially closed
off	Switch initially open

Output only instance parameters for Ideal voltage controlled switch (Switch)

Parm. name	Description
cont_p_node	Positive contr. node of switch
cont_n_node	Positive contr. node of switch
c	Switch current
p	Switch power

Input/Output instance parameters for Ideal voltage controlled switch (Switch)

Parm. name	Description
pos_node	Positive node of switch
neg_node	Negative node of switch

Model parameters for Ideal voltage controlled switch (Switch)

Parm. name	Description
on	Switch initially closed
off	Switch initially open
pos_node	Positive node of switch
neg_node	Negative node of switch

Model parameters for Ideal voltage controlled switch (Switch)

Parm. name	Description
cont_p_node	Positive contr. node of switch
cont_n_node	Positive contr. node of switch
c	Switch current

1.10.18. Lossless transmission line

Input only instance parameters for Lossless transmission line (Tranline)

Parm. name	Description
ic	Initial condition vector:v1,i1,v2,i2

Output only instance parameters for Lossless transmission line (Tranline)

Parm. name	Description
rel	Rel. rate of change of deriv. for bkpt
abs	Abs. rate of change of deriv. for bkpt
pos_node1	Positive node of end 1 of t. line
neg_node1	Negative node of end 1 of t. line
pos_node2	Positive node of end 2 of t. line
neg_node2	Negative node of end 2 of t. line
delays	Delayed values of excitation

Input/Output instance parameters for Lossless transmission line (Tranline)

Parm. name	Description
z0	Characteristic impedance
zo	Characteristic impedance
f	Frequency
td	Transmission delay
nl	Normalized length at frequency given
v1	Initial voltage at end 1
v2	Initial voltage at end 2
i1	Initial current at end 1
i2	Initial current at end 2

1.10.19. Uniform R.C. line

Output only instance parameters for Uniform R.C. line (URC)

Parm. name	Description
pos_node	Positive node of URC
neg_node	Negative node of URC
gnd	Ground node of URC

Input/Output instance parameters for Uniform R.C. line (URC)

Parm. name	Description
l	Length of transmission line
n	Number of lumps

Model parameters for Uniform R.C. line (URC)

Parm. name	Description
l	Length of transmission line
n	Number of lumps
pos_node	Positive node of URC
neg_node	Negative node of URC
gnd	Ground node of URC
k	Propagation constant
fmax	Maximum frequency of interest

1.10.20. Voltage controlled current source

Input only instance parameters for Voltage controlled current source (VCCS)

Parm. name	Description
sens_trans	flag to request sensitivity WRT transconductance
ic	Initial condition of controlling source

Output only instance parameters for Voltage controlled current source (VCCS)

Parm. name	Description
pos_node	Positive node of source
neg_node	Negative node of source
cont_p_node	Positive node of contr. source
cont_n_node	Negative node of contr. source
c	Current
p	Power
sens_dc	dc sensitivity
sens_real	real part of ac sensitivity
sens_imag	imag part of ac sensitivity
sens_mag	sensitivity of ac magnitude
sens_ph	sensitivity of ac phase
sens_cplx	ac sensitivity

Input/Output instance parameters for Voltage controlled current source (VCCS)

Parm. name	Description
gain	Transconductance of source (gain)

1.10.21. Voltage controlled voltage source

Input only instance parameters for Voltage controlled voltage source (VCVS)

Parm. name	Description
sens_gain	flag to request sensitivity WRT gain
ic	Initial condition of controlling source

Output only instance parameters for Voltage controlled voltage source (VCVS)

Parm. name	Description
pos_node	Positive node of source
neg_node	Negative node of source
cont_p_node	Positive node of contr. source
cont_n_node	Negative node of contr. source
c	Current
p	Power
sens_dc	dc sensitivity
sens_real	real part of ac sensitivity
sens_imag	imag part of ac sensitivity
sens_mag	sensitivity of ac magnitude
sens_ph	sensitivity of ac phase

Output only instance parameters for Voltage controlled voltage source (VCVS)

Parm. name	Description
sens_cplx	ac sensitivity

Input/Output instance parameters for Voltage controlled voltage source (VCVS)

Parm. name	Description
gain	Voltage gain

1.10.22. Independent voltage source

Input only instance parameters for Independent voltage source (Vsource)

Parm. name	Description
pulse	Pulse description
sine	Sinusoidal source description
sin	Sinusoidal source description
exp	Exponential source description
pwl	Piecewise linear description
sffm	Single freq. FM descripton
ac	AC magnitude, phase vector

Output only instance parameters for Independent voltage source (Vsource)

Parm. name	Description
pos_node	Positive node of source
neg_node	Negative node of source
function	Function of the source
order	Order of the source function
coeffs	Coefficients for the function
acreal	AC real part
acimag	AC imaginary part
c	Voltage source current
p	Instantaneous power

Input/Output instance parameters for Independent voltage source (Vsource)

Parm. name	Description
dc	D.C. source value
acmag	A.C. Magnitude
acphase	A.C. Phase

1.11. EXAMPLE DATA DECKS

1.11.1. Circuit 1

The following deck determines the dc operating point of a simple differential pair. In addition, the ac small-signal response is computed over the frequency range 1Hz to 100MEGHz.

```
SIMPLE DIFFERENTIAL PAIR
VCC 7 0 12
VEE 8 0 -12
VIN 1 0 AC 1
RS1 1 2 1K
RS2 6 0 1K
Q1 3 2 4 MOD1
Q2 5 6 4 MOD1
RC1 7 3 10K
RC2 7 5 10K
RE 4 8 10K
.MODEL MOD1 NPN BF=50 VAF=50 IS=1.E-12 RB=100 CJC=.5PF TF=.6NS
.TF V(5) VIN
.AC DEC 10 1 100MEG
.END
```

1.11.2. Circuit 2

The following deck computes the output characteristics of a MOSFET device over the range 0-10V for VDS and 0-5V for VGS.

```
MOS OUTPUT CHARACTERISTICS
.OPTIONS NODE NOPAGE
VDS 3 0
VGS 2 0
M1 1 2 0 0 MOD1 L=4U W=6U AD=10P AS=10P
.MODEL MOD1 NMOS VTO=-2 NSUB=1.0E15 UO=550
* VIDS MEASURES ID, WE COULD HAVE USED VDS, BUT ID WOULD BE NEGATIVE
VIDS 3 1
.DC VDS 0 10 .5 VGS 0 5 1
.END
```

1.11.3. Circuit 3

The following deck determines the dc transfer curve and the transient pulse response of a simple RTL inverter. The input is a pulse from 0 to 5 Volts with delay, rise, and fall times of 2ns and a pulse width of 30ns. The transient interval is 0 to 100ns, with printing to be done every nanosecond.

```
SIMPLE RTL INVERTER
VCC 4 0 5
VIN 1 0 PULSE 0 5 2NS 2NS 2NS 30NS
RB 1 2 10K
Q1 3 2 0 Q1
RC 3 4 1K
.MODEL Q1 NPN BF 20 RB 100 TF .1NS CJC 2PF
.DC VIN 0 5 0.1
.TRAN 1NS 100NS
.END
```

1.11.4. Circuit 4

The following deck simulates a four-bit binary adder, using several subcircuits to describe various pieces of the overall circuit.

```
ADDER - 4 BIT ALL-NAND-GATE BINARY ADDER

   *** SUBCIRCUIT DEFINITIONS

.SUBCKT NAND 1 2 3 4
   *  NODES:  INPUT(2), OUTPUT, VCC
Q1 9 5 1 QMOD
D1CLAMP 0 1 DMOD
Q2 9 5 2 QMOD
D2CLAMP 0 2 DMOD
RB 4 5 4K
R1 4 6 1.6K
Q3 6 9 8 QMOD
R2 8 0 1K
RC 4 7 130
Q4 7 6 10 QMOD
DVBEDROP 10 3 DMOD
Q5 3 8 0 QMOD
.ENDS NAND
.SUBCKT ONEBIT 1 2 3 4 5 6
```

```
    *  NODES:  INPUT(2), CARRY-IN, OUTPUT, CARRY-OUT, VCC
X1 1 2 7 6 NAND
X2 1 7 8 6 NAND
X3 2 7 9 6 NAND
X4 8 9 10 6 NAND
X5 3 10 11 6 NAND
X6 3 11 12 6 NAND
X7 10 11 13 6 NAND
X8 12 13 4 6 NAND
X9 11 7 5 6 NAND
.ENDS ONEBIT
.SUBCKT TWOBIT 1 2 3 4 5 6 7 8 9
    *  NODES:  INPUT - BIT0(2) / BIT1(2), OUTPUT - BIT0 / BIT1,
    *          CARRY-IN, CARRY-OUT, VCC
X1 1 2 7 5 10 9 ONEBIT
X2 3 4 10 6 8 9 ONEBIT
.ENDS TWOBIT

.SUBCKT FOURBIT 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
   *  NODES:  INPUT - BIT0(2) / BIT1(2) / BIT2(2) / BIT3(2),
   *          OUTPUT - BIT0 / BIT1 / BIT2 / BIT3, CARRY-IN, CARRY-OUT, VCC
X1 1 2 3 4 9 10 13 16 15 TWOBIT
X2 5 6 7 8 11 12 16 14 15 TWOBIT
.ENDS FOURBIT

   *** DEFINE NOMINAL CIRCUIT

.MODEL DMOD D
.MODEL QMOD NPN(BF=75 RB=100 CJE=1PF CJC=3PF)
VCC 99 0 DC 5V
VIN1A 1 0 PULSE(0 3 0 10NS 10NS   10NS   50NS)
VIN1B 2 0 PULSE(0 3 0 10NS 10NS   20NS  100NS)
VIN2A 3 0 PULSE(0 3 0 10NS 10NS   40NS  200NS)
VIN2B 4 0 PULSE(0 3 0 10NS 10NS   80NS  400NS)
VIN3A 5 0 PULSE(0 3 0 10NS 10NS  160NS  800NS)
VIN3B 6 0 PULSE(0 3 0 10NS 10NS  320NS 1600NS)
VIN4A 7 0 PULSE(0 3 0 10NS 10NS  640NS 3200NS)
VIN4B 8 0 PULSE(0 3 0 10NS 10NS 1280NS 6400NS)
X1 1 2 3 4 5 6 7 8 9 10 11 12 0 13 99 FOURBIT
RBIT0 9 0 1K
RBIT1 10 0 1K
RBIT2 11 0 1K
RBIT3 12 0 1K
RCOUT 13 0 1K

   *** (FOR THOSE WITH MONEY (AND MEMORY) TO BURN)
.TRAN 1NS 6400NS

.END
```

1.11.5. Circuit 5

The following deck simulates a transmission-line inverter. Two transmission-line elements are required since two propagation modes are excited. In the case of a coaxial line, the first line (T1) models the inner conductor with respect to the shield, and the second line (T2) models the shield with respect to the outside world.

```
TRANSMISSION-LINE INVERTER
V1 1 0 PULSE(0 1 0 0.1N)
R1 1 2 50
X1 2 0 0 4 TLINE
R2 4 0 50
 .SUBCKT TLINE 1 2 3 4
T1 1 2 3 4 Z0=50 TD=1.5NS
T2 2 0 4 0 Z0=100 TD=1NS
 .ENDS TLINE
 .TRAN 0.1NS 20NS
 .END
```