

Copyright © 1990, by the author(s).  
All rights reserved.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission.

**NOVEL ROUTING SCHEMES FOR  
IC LAYOUT PART II: THREE-LAYER  
CHANNEL ROUTING**

by

Deborah Wang and E. S. Kuh

Memorandum No. UCB/ERL M90/102

2 November 1990

**NOVEL ROUTING SCHEMES FOR  
IC LAYOUT PART II: THREE-LAYER  
CHANNEL ROUTING**

by

Deborah Wang and E. S. Kuh

Memorandum No. UCB/ERL M90/102

2 November 1990

**ELECTRONICS RESEARCH LABORATORY**

College of Engineering  
University of California, Berkeley  
94720

**NOVEL ROUTING SCHEMES FOR  
IC LAYOUT PART II: THREE-LAYER  
CHANNEL ROUTING**

by

Deborah Wang and E. S. Kuh

Memorandum No. UCB/ERL M90/102

2 November 1990

COVER PAGE

**NOVEL ROUTING SCHEMES FOR  
IC LAYOUT PART II: THREE-LAYER  
CHANNEL ROUTING**

by

Deborah Wang and E. S. Kuh

Memorandum No. UCB/ERL M90/102

2 November 1990

**ELECTRONICS RESEARCH LABORATORY**

College of Engineering  
University of California, Berkeley  
94720

TITLE PAGE

# Novel Routing Schemes for IC Layout

## Part II: Three-Layer Channel Routing

### ABSTRACT

We present new three-layer channel routing algorithm and theory involving  $60^\circ$  wires. The routing strategy is based on the river routing techniques. Vertical constraints no longer exist. The final solution contains a minimal set of net crossings which leads to a small number of vias. The lower- and upper- bounds of the channel height are  $2d/5$  and  $d$  respectively, where  $d$  is the density. Preliminary results are promising.

# 1 Introduction

Channel routing is one of the key steps in the layout of integrated circuits. It has been extensively studied and applied to many different design styles such as gate array, standard cell and building blocks. The original channel-routing problem assumes two interconnect layers are available. Recent advance in the manufacturing technology has made multi-layer interconnect a reality. Therefore, it is important to design channel router to handle multi-layer regions. This development is also meaningful for other technologies such as multi-chip modules and hybrid packages. We shall focus on the 3-layer channel routing problem in this paper.

Most of the 3-layer routing algorithms [9, 6, 3, 7, 8, 10] extend the layer per direction paradigm of Manhattan routing : the top and bottom layers are used for horizontal wires and the middle layer is used for vertical wires (HVH model). The vertical constraints are the major performance- degrading factor under such model. Other algorithms use knock-knee model [13] or overlapping wires [2, 1, 11] to warrant worst case performance. For example, the knock-knee router [13] routes any channel in height equal to the density using 3 alyers. However, these methods may introduce excess vias.

In this paper, we propose a new 3-layer channel routing algorithm using  $60^\circ$  wires.  $60^\circ$  wires not only provide more degrees of freedom for completing the interconnections but also shorten interconnect length. The algorithm is implemented in a router called *Overture*. *Overture* is designed to route two-terminal nets across a channel, and will also be extended to handle multi-terminal nets. The routing strategy is based on the river routing technique and is very different from the Manhattan approach. In particular, vertical constraints no longer exist. Furthermore, the solution produced by *Overture* consists of a minimal set of net crossings which leads to a small number of vias. These characteristics contribute to the effectiveness of *Overture*.

The remainder of this paper is organized as follows. Section 2 defines the channel routing problem. Section 3 describes the Steiner ( $60^\circ$ ) wiring grid. The routing algorithm is given in Section 4. Section 5 contains performance analysis. Routing results are presented in Section 6. Concluding remarks and future work are given in Section 7.

## 2 The Problem

A channel is a pair of vectors of nonnegative integers - TOP and BOT - of the same dimension.

$$\text{TOP} = t(1), t(2), \dots, t(n)$$

$$\text{BOT} = b(1), b(2), \dots, b(n)$$

We assume that these numbers are the labels of grid points located along the top and

bottom edge of a rectangle. Points having the same positive label have to be interconnected, i.e. they define nets. Given three interconnect layers and the design rules, a 100% routing completion is required. The primary objective is to minimize the channel height. The secondary objectives are to minimize the number of vias and the wire length of each net.

**Definition 1** A channel is dense iff  $t(i) \neq 0$  and  $b(i) \neq 0$  for all  $i$ , that is, every grid point on the top and bottom boundaries is occupied by a terminal.

**Definition 2** A non-trivial 2-terminal net is a net that has exactly two terminals, one on the top and another on the bottom.

Let  $\{ 1, 2, \dots, N \}$  denote the set of nets. Then in a dense 2-terminal net channel, TOP and BOT are permutations of  $\{ 1, 2, \dots, N \}$ . Without loss of generality, we may assume that nets are arbitrarily ordered on the bottom and are naturally ordered on the top. This is stated as:

**Definition 3** A dense 2-terminal net (D2TN) channel routing problem is specified by:

$TOP = 1, 2, 3, \dots, N$

$BOT = \text{a permutation of } \{ 1, 2, \dots, N \}$

We denote the top and bottom terminals of net  $i$  by  $(i, q_i)$ .

The design rules specify the wire width, the line-to-line spacing and size of a via. The sum of the line width and line-to-line spacing is called the pitch. Technology limits typically require that vias be larger than the wire widths, the corresponding design rules are called the contact-to-line and contact-to-contact spacing.

### 3 The Steiner Grid

The Steiner grid, first proposed by [4, 5], is composed of three types of grid lines: the horizontal tracks, the right ( $+60^\circ$ ) tracks and the left ( $-60^\circ$ ) tracks (Figure 1). In principle, three interconnect layers are required: one layer per direction [5, 12]. In contrast to the layer-per-direction Steiner model, we allow wires on different layers to overlap. The only restriction is that wires must lie on the Steiner grid, thereby imposing a uniform unit separation design rule. At each grid point, at most one via is present. Figure 2 shows three sample nets routed on the Steiner grid.

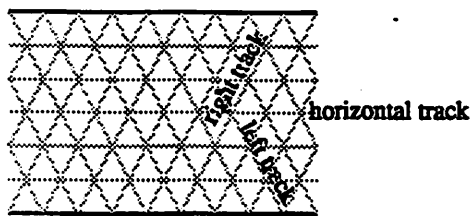


Figure 1. The Steiner Grid

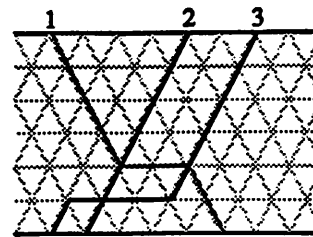


Figure 2. Sample nets



Let us now examine the design rules for the Steiner grid. If the terminals on TOP or BOT are separated by the contact-to-contact spacing,  $D$ , the distance between parallel tracks is  $\sqrt{3}D/2$ . If this is greater than or equal to the pitch, the spacing requirement is satisfied. Otherwise, the the spacing between terminals need to be enlarged. Since the contact-to-contact spacing is typically larger than the pitch, it is highly likely that the spacing rule is satisfied without magnifying the terminal spacing. We also note the spacing between grid points where vias are located, remains design-rule correct.

## 4 Routing Algorithm

In order to align terminals on TOP and BOT on vertical lines, the channel must have odd number of horizontal tracks. Let the horizontal tracks be labeled by  $t_w, t_{w-1}, \dots, t_0, \dots, t_{-w}$  (Figure 3). Consider a D2TN channel routing problem specified by Definition 3. Let us define the following terms.

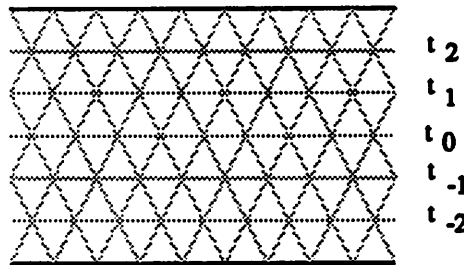


Figure 3. Label horizontal tracks

**Definition 4** Given a net  $i$  with terminals  $(i, q_i)$ ,

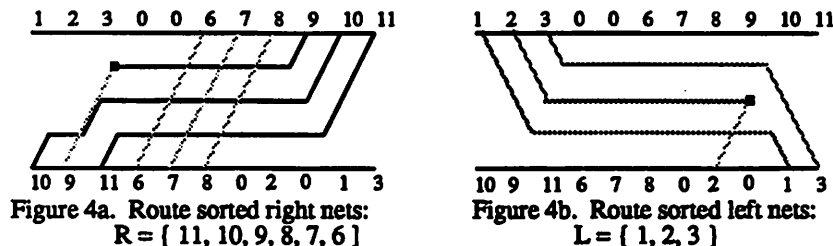
- $i$  is a right net iff  $i \geq q_i$ .
- $i$  is a left net iff  $i < q_i$ .

We partition the nets into two disjoint subsets:  $R = \{\text{rightnets}\}$  and  $L = \{\text{leftnets}\}$  and route each set independently. The routing strategy is based on the river routing techniques. It is an extension of the 2-layer channel router presented in [14]. A top level description of the algorithm is given below:

### *Top-Level Routing Algorithm*

- step 1) Nets are divided into two sets:  $R = \text{right nets}$  ;  $L = \text{left nets}$
- step 2) Sort  $R$  in decreasing order of their top terminals. Route  $R$ .
- step 3) Sort  $L$  in increasing order of their top terminals. Route  $L$ .

The solution for the D2TN channel is constructed in a bottom- to-top net-by-net fashion. Let us demonstrate the algorithm on the example shown in Figure 4. The right nets are sorted and routed sequentially in a river routing fashion. The procedure begins by constructing a wiring path on the Steiner grid for the first right net. The path begins at its bottom terminal and ends at its top terminal (detail of path finding will be given later). The wiring path for the second right net simply follows the path of the first right net and ends at the top terminal. This process continues until all right nets are routed. Step 3 is identical to step 2, except that this time the left nets are routed.



The layer assignment scheme is as follows. The first interconnect layer is used for horizontal and right tracks; the third layer is used for horizontal and left tracks. If a channel has more right nets than left nets, the middle interconnect layer is used exclusively for the right ( $+60^\circ$ ) tracks. Otherwise, it is used for the left ( $-60^\circ$ ) tracks.

To find the wiring path for each individual net on the Steiner grid, we classify the nets according to the following definition.

**Definition 5** Given a channel of height  $h = 2(w+1)$  and net  $i$  with terminals  $(i, q_i)$ ,

- $i$  is a right long net iff  $i - q_i > w + 1$
- $i$  is a right short net iff  $0 \leq i - q_i \leq w + 1$
- $i$  is a left long net iff  $q_i - i > w + 1$
- $i$  is a left short net iff  $0 \leq q_i - i \leq w + 1$

For channels with more right nets, the wiring paths for sample nets are shown in Figure 5. A short net with  $|i - q_i| = h + 1$  is also called a *direct net*. A direct net is routed with a single segment on the right or left track and requires no via. A short net bends on the horizontal track  $i - q_i$ . A long net is routed with one horizontal segment and two  $60^\circ$  segments. Direct nets are routed on a single layer and do not require vias. Short and long nets change layer only once and require one via per net. The layer assignment scheme in Figure 5 uses the second layer for right tracks. On the other hand, if there are more left nets, ie. the second

layer is used for the left tracks, the wiring patterns and layer assignment scheme shown in Figure 6 are suitable for this class of channel routing problems.

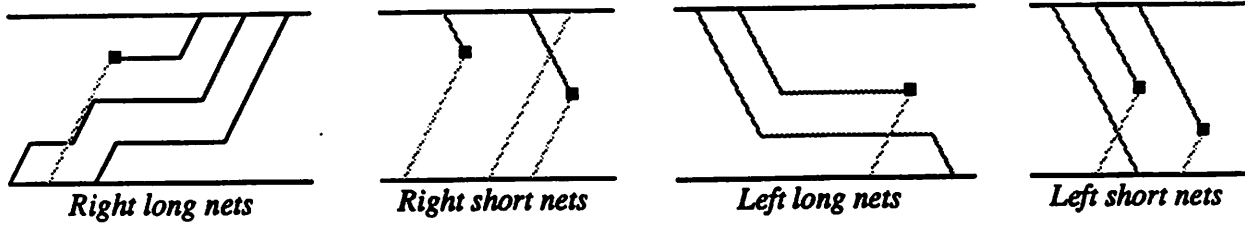


Figure 5. Wiring Method I:

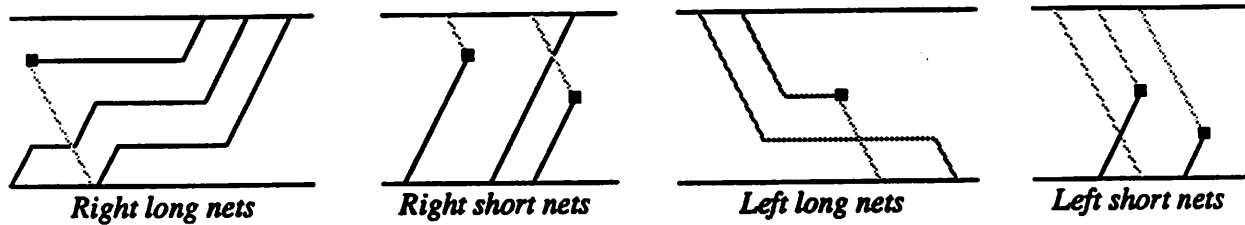
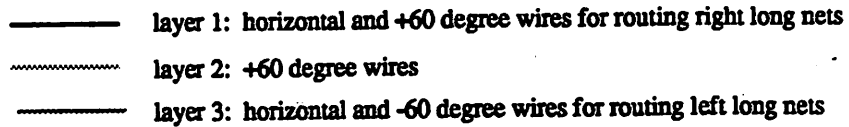
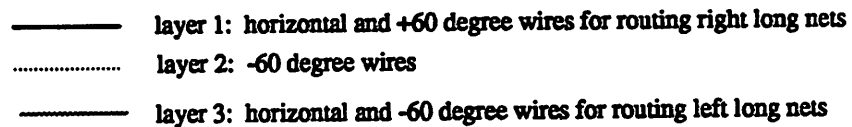


Figure 6. Wiring Method II:



## 5 Performance Analysis

In this section, we establish four results associated with Overture: (1) lower bound on the channel height, (2) upper bound on the channel height, (3) total number of vias, and (4) wire length. In particular, we prove the final channel height,  $h$ , produced satisfies  $2d/5 \leq h \leq d$ , where  $d$  is the Manhattan density.

For the 3-layer HVH Manhattan model,  $d/2$  is an obvious lower bound on the channel height, since as many as  $d/2$  tracks are necessary on each horizontal layer to complete routing. When overlap between wires is allowed, Hambrusch [11] showed that the lower bound is also  $d/2$  using 3 layers. We improve this lower bound to  $2d/5$  for the 3-layer  $60^\circ$  model. In particular, the example shown in Figure 7 is routed by Overture in a channel of height equal to the lower bound.

**Theorem 1** *The lower bound on the channel height produced by Overture is  $2d/5$ , where  $d$  is the global density of the channel.*

**Proof:** Given a channel routing problem and a channel of height  $h = 2w + 1$ , consider a vertical line  $L$  as shown in Figure 8. The horizontal tracks are labeled as  $t_w, t_{w-1}, \dots, t_0, \dots, t_{-w}$ . Suppose  $w$  is even. Then each of the  $w$  grid points located at the intersection of  $L$  and the odd numbered tracks allows three distinct wires to pass through. Similarly, each of the  $(w + 1)$  grid points located at the intersection of  $L$  and the even numbered tracks allows two distinct wires to pass through. Hence the total number of distinct wires cut by  $L$  is  $3w + 2(w + 1) = 5w + 2 \geq d$ . The channel height,  $h = 2w + 1$ , is then  $\geq (2d - 1)/5$ . The proof for even  $w$  is similar. ■

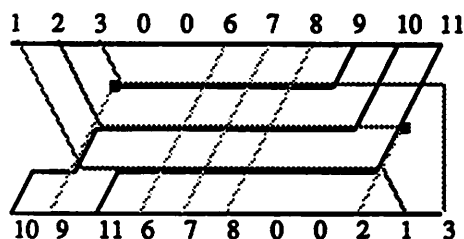


Figure 7. This example is routed in a channel of height equal to the lower bound

density = 8  
tracks = 3  
vias = 2

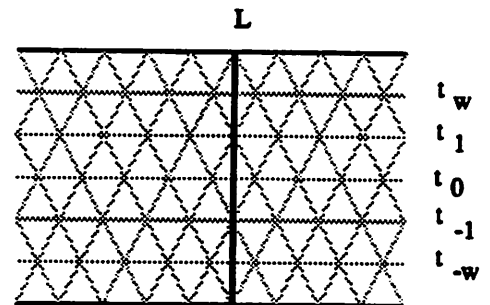


Figure 8. For proof of Theorem 1

The final channel height,  $h$ , is  $\max\{h(i) \mid 1 \leq i \leq 3\}$ , where  $h(i)$  denote the number of tracks required in the  $i$ th interconnect layer. The values of  $h(i)$  depend on the density of wires on layer  $i$ . Recall the Manhattan density is the maximum of nets that are split by any vertical cut of the channel. We now introduce the notion of the *Steiner density* by considering the number of nets split by any  $+60^\circ$  or  $-60^\circ$  cut of the channel.

**Definition 6** *Given a channel of height  $h$  and a set of nets,  $S$ ,*

$d(S, h, +60^\circ)$  = the maximum number of nets in  $S$  split by any  $+60^\circ$  cut of the channel

$d(S, h, -60^\circ)$  = the maximum number of nets in  $S$  split by any  $-60^\circ$  cut of the channel

For a given  $h$ , let  $R_l, R_s, L_l, L_s$  denote the sets of *right long nets*, *right short nets*, *left long nets*, and *left short nets* respectively. Since layer 1 contains only right long nets and each such net intersects any  $-60^\circ$  cut line once, the number of tracks required on layer 1,  $h(1)$ , is the Steiner density,  $d(R_l, h, -60^\circ)$ . The number of tracks required on layer 2 and 3,  $h(2)$  and  $h(3)$  can be calculated similarly. This is summarized in the following lemma.

**Lemma 1** *Given a channel routing problem, assume wiring method I is used, the channel height produced by Overture is  $h = \max\{h(i) \mid 1 \leq i \leq 3\}$ , where*

$$h(1) = d(R_l, h, -60^\circ)$$

$$h(2) = d(R_s \cup L_s, h, -60^\circ)$$

$$h(3) = d(L_l \cup L_s \cup R_s, h, -60^\circ)$$

To find the value of channel height and to construct the final solution, we propose an iterative method. We start with  $h = 2d/5$ , the lower bound. Given  $h$ , we can construct the sets  $R_l$ ,  $R_s$ ,  $L_l$ ,  $L_s$  and calculate  $h(i)$  by Lemma 1. If  $\max\{h(i)\} > h$ , we repeat the procedure with  $h + 1$ . Otherwise, the algorithm terminates and the final solution is found. This iteration procedure is summarized below.

*Overture Routing Procedure*

initialize  $h = 2d/5$

repeat

    build  $R_l, R_s, L_l, L_s$

    calculate  $h(i)$  by Lemma 1

while (  $h < \max\{h(i) \mid 1 \leq i \leq 3\}$  )

construct wiring paths ( described in Section 4 )

To find the upper bound on the channel height,  $h$ , and to compare it with the Manhattan density, we analyze the worst case performance of Overture in the following theorem.

**Theorem 2** *Overture can route any D2TN channel routing problem in at most  $d$  tracks, where  $d$  is the Manhattan density of the channel.*

**Proof:** Suppose a D2TN channel routing problem with Manhattan density  $d$  is routed in a height  $h$  by Overture (Figure 9). Consider layer 1 and any  $-60^\circ$  cut line  $L$ . The number of tracks required on layer 1 is  $d(R_l, h, -60^\circ)$  (Lemma 1).

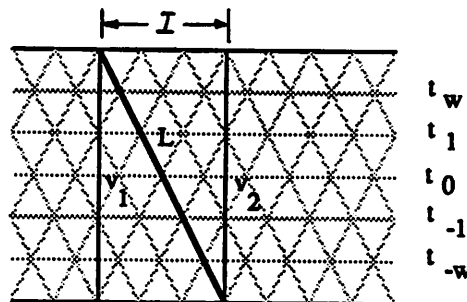


Figure 9. For proof of Theorem 2

- i) number of grid points on  $L = h$
- ii) each right net split by the vertical line  $v_1$  is also split by  $L$ . At most  $d/2$  right nets are split by  $v_1$ .
- iii) If all of the  $d/2$  right nets split by  $v_1$  are also split by the vertical line  $v_2$ , then there can not be additional right nets in the interval  $I$ . Hence  $h = d(R_1, h, -60^\circ) = d/2$ .
- iv) If not all of the  $d/2$  right nets split by  $v_1$  span the interval  $I$ , i.e. say  $m$  right nets have top terminals in  $I$ , then at most  $m$  additional right long nets can be split by  $L$ . Since there are  $h/2$  grid points on  $I$ ,  $m \leq h/2$ . Hence in the worst case  $d(R_1, h, -60^\circ) = d/2 + m = d/2 + h/2 =$  number of grid points on  $L = h$ . Hence  $h = d$ .

The proof for layer 2 and layer 3 is similar. ■

This upper bound is rather pessimistic because it is the channel height of a pathological case. Experimental results show that Overture performs well on practical channels.

The number of vias required by Overture is small because the solution consists of a minimal number of net crossings. In particular, at most one via is required per net for any D2TN channel routing problem. The number of vias can be calculated by the following Lemma.

**Lemma 2** *Given a D2TN channel routing problem specified by Definition 3. Let  $R =$  right nets ;  $L =$  left nets. Given nets  $i, j$  and  $S$ , a set of nets, we define  $NOTORDER(i,j,S)$  as the number of indices  $p \in S$  such that  $i < p \leq j$  and  $q_p \leq q_i$ , or such that  $j \leq p < i$  and  $q_i \leq q_p$ . Then, for any non-direct right (left) net  $i$ , if  $NOTORDER(i,1,R) = 0$  (  $NOTORDER(i,N,L) = 0$  ), then net  $i$  has no via in the final solution produced by Overture. Otherwise, net  $i$  has one via. The total number of vias can be precisely calculated by evaluating  $NOTORDER(i,1,R)$  or  $NOTORDER(i,N,L)$  for all  $i$ .*

When wiring method I is used, i.e. layer 2 is used for  $+60^\circ$  tracks, the wiring paths for the right nets are monotonic in both the horizontal and vertical directions; while the paths for the left nets are monotonic in the vertical direction only. The wire length of each net can be calculated by the following lemma.

**Lemma 3** *The exact wire length of net  $i$ ,  $L(i)$ , is calculated by:*

$$L(i) = span(i) + h/2 \text{ if net } i \text{ is a right net}$$

$$L(i) = span(i) + h/2 + NOTORDER(i,N,L) \text{ if net } i \text{ is a left net}$$

$$\text{where } span(i) = |i - b(i)|, h = \text{final channel height}$$

## 6 Results

Overture is implemented in the C language on a DEC3100 running Ultrix Worksystem V2.1. Figure 9 shows the routing result of a channel with 48 nets. We have attempted to run this example using other routers available[chameleon,trigger] but they produced substantially worse results. Table I lists the channels tested with 100% routing completion in all cases.

Table 1. Experimental results

Examples	density	Result of [12]		Our results		
		height	vias	height	vias	CPU
Ex1	9	7	31	5	4	0.1
Ex2	8	7	15	3	2	0.1
Ex3	8	8	8	5	0	0.1
Ex4	18	N/A	N/A	11	34	1.0

N/A: Not Available

All examples are two-terminal net channels

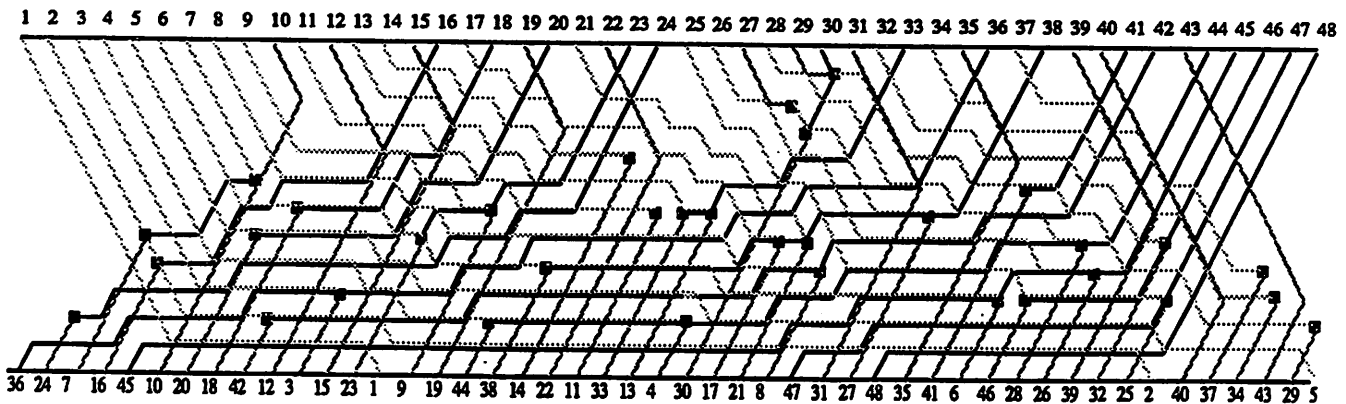


Figure 9. Routing results of Ex4.

## 7 Conclusion and Future Work

In this paper, we have proposed a new 3-layer channel routing scheme by exploiting the additional degrees of freedom offered by the  $60^\circ$  Steiner grid. The routing strategy is based on the river routing technique. Wires on different layers are allowed to overlap. The routing solution produced by Overture has unambiguous layer assignment and is design-rule correct. We prove that the channel height,  $h$ , produced by Overture satisfies  $2d/5 \leq h \leq d$ , where  $d$  is the Manhattan density. Compared to the Manhattan routers, Overture has the following advantages: (1) It does not need to deal with vertical constraints, (2) The wire length is expected to be shorter due to the use of  $60^\circ$  wires. (3) A small number of vias is required because the routing solution contains a minimal number of net crossings. In particular, at most one via per net is required for routing two-terminal nets across a channel. (4) Due to the simplicity of the river routing technique, it is very fast. We plan to extend Overture to handle multi-terminal nets and larger number of layers.

## References

- [1] M.L. Brady and D.J. Brown. An algorithm for three layer channel routing using restricted overlap. In *Proc. 23rd Annual Allerton Conference on Communication, Control and Computing*, pages 674–675, 1985.
- [2] M.L. Brady and D.J. Brown. Optimal multilayer channel routing with overlap. In *Proc. 4th MIT Conference on Advanced Research in VLSI*, pages 281–296, 1986.
- [3] P. Bruell and P. Sun. A greedy three layer channel router. In *Proc. of the International Conference on Computer-Aided Design*, pages 298–300, 1985.
- [4] P. Chaudhuri. An ecological approach to wire routing. In *Proc. of the IEEE International Symposium on Circuits and Systems*, pages 854–857, 1979.
- [5] P. Chaudhuri. Routing multilayer boards on steiner metric. In *Proc. of the IEEE International Symposium on Circuits and Systems*, pages 961–964, 1980.
- [6] Y.K. Chen and M.L. Liu. Three-layer channel routing. In *IEEE Trans. on CAD of Integrated Circuits and Systems, V. CAD-3*, pages 156–163, 1984.
- [7] J. Cong, D.F. Wong, and C.L. Liu. A new approach to three- or four-layer routing. In *IEEE Trans. on CAD of Integrated Circuits and Systems, V. CAD-3*, pages 1094–1104, 1988.
- [8] R.J. Enbody and H.C. Du. Near-optimal n-layer channel routing. In *Proc. of the 23rd Design Automation Conference*, pages 709–714, 1986.



- [9] D. Braun et al. Techniques for multilayer channel routing. In *IEEE Trans. on CAD of Integrated Circuits and Systems, V. CAD-7*, pages 698–712, 1988.
- [10] R.I. Greenberg et al. Mulch: A multi-layer channel router using one, two and three layer partitions. In *Proc. of the International Conference on Computer-Aided Design*, pages 88–91, 1988.
- [11] S.E. Hambrusch. Using overlap and minimizing contact points in channel routing. In *Proc. 21st Annual Allerton Conference on Communication, Control and Computing*, pages 256–257, 1983.
- [12] E. Lodi, F. Luccio, and L. Pagli. Routing in the times square mode. Technical report, dipartimento di informatica, Universita Degli Studi Di Pisa, Italy, 1989.
- [13] F.P. Preparata and W. Lipski. Three layers are enough. In *Proc. 23rd Annual Symposium on Foundations of Computer Science*, pages 350–357, 1982.
- [14] D. Wang and E.S. Kuh. Novel routing schemes for ic layout, part i: Two-layer channel routing. Technical report, Department of Electrical Engineering, Electronics Research Laboratory, University of California, Berkeley, 1990.