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HOT-WALL SILICON EPITAXY

by

Carl Johan Galewski

Memorandum No. UCB/ERL M90/122

20 December 1990

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20 December 1990

ELECTRONICS RESEARCH LABORATORY

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Dedicated to my parents

&

Judy

Hot-Wall Silicon Epitaxy

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Carl J. Galewski

Abstract

A low-pressure hot-wall epitaxial reactor is proposed as a possible low-cost alternative to standard cold-wall epitaxial reactors. Fundamental limitations for the removal of native oxides inside the reactor guided the design. The reactor was built by modifying a commercial LPCVD furnace tube, retaining as much as possible of its original structure. The reactor can accommodate as many as 50 wafers of 100 mm diameter. Defect-free epitaxial deposition is obtained at temperatures ranging from 950° to 830° C after a 1000° C bake in H_2. The use of an HF vapor etch before the wafers are loaded into the reactor allows the H_2 bake temperature to be decreased to 900° C. Input concentrations from 3.9% to 17% SiH_2Cl_2 in H_2 were used and all resulted in selective epitaxial deposition.

Basic issues and experimental results pertaining to epitaxial silicon interface quality, background impurities, selective epitaxy, and electrical properties are discussed. It is found that the oxide at the interface is not uniform, that the interface does not have to be perfect in order to grow defect-free epitaxial layers, and that the presence of H_2O inside the reactor is most likely due to adsorption from air on parts exposed to air while the reactor is open. An improved cleaning procedure is found that reduces oxide nucleation. Electrical evaluation of MOS devices fabricated on both standard and epitaxial material shows essentially identical behavior for the two materials.

A complete model is presented for deposition uniformity in the hot-wall reactor. Radial depletion is modeled successfully with a first-order reaction rate and diffusion.

Longitudinal modeling requires a more complicated reaction rate expression, and also must include both convection and diffusion. Good fit between the model and data is found over a wide range of gas composition, pressure, and temperature. The model is used to explore improvements to the existing hot-wall reactor, and also to design a hypothetical production-sized reactor.

Prof. W. G. Oldham
Committee Chairman

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Chapter 1
Introduction

The past trend for integrated circuits has been to continuously increase the functionality of each chip by decreasing the size of the structures that make up the circuits. As the trend towards more complex integrated circuits continues, it will become increasingly difficult to fabricate the compact structures that can fully utilize the ever smaller dimensions that can be defined by microlithography. Epitaxial deposition provides a means of forming single crystal layers with an impurity concentration independent of the substrate, and under certain conditions epitaxial deposition can be selective with respect to a masking layer. Both of these epitaxial deposition characteristics can be used to make integrated circuits more compact. Deposition of a lightly doped epitaxial layer on top of a heavily doped substrate reduces parasitic substrate resistance, allowing, for example, CMOS transistors to be placed more closely together [1,2]. Selective epitaxial deposition can be used to fabricate compact structures that take better advantage of a given surface area [3,4]. However, the high-cost of the current method of depositing epitaxial layers in cold-wall reactors is an obstacle for many applications. For example, the high cost of producing epitaxial substrates with conventional cold-wall reactors has limited the use to a few percent of the total number of substrates used for MOS circuits [5]. Furthermore, compact structures often require shallow and abrupt junctions which preclude the high temperatures above 1000° C that are used for traditional epitaxy. The above reasons suggest that there is a need for less costly methods to deposit epitaxial silicon, and that low temperature operation is important.

Deposition of many layers important to integrated circuit fabrication, such as polysilicon, silicon nitride, and low temperature oxides, are performed economically by

low-pressure chemical vapor deposition (LPCVD) in tubular hot-wall systems. Deposition rates are low, but 100-200 coaxially placed wafers can be processed per batch. The high temperatures used traditionally for epitaxial deposition are not compatible with a hot-wall tubular reactor because of excessive depletion due to deposition of silicon on the heated walls. Epitaxial cold-wall reactors are designed for high temperatures and high growth rates by heating only an internal susceptor. The disadvantage of the cold-wall reactor approach is that the the number of wafers that can be processed per batch is limited by each wafers having to fully contact the heated susceptor. As growth rates decrease due to the desired reductions in the growth temperature, the high packing density of wafers in tubular hot-wall reactors will make them more cost effective with respect to cold-wall reactors. Tubular reactor also scale more efficiently than cold-wall reactors when wafer diameters increase. This thesis, therefore, proposes to examine the use of a low-pressure hot-wall reactor for epitaxial silicon deposition.

Chapter 2 reviews the past work on hot-wall silicon epitaxy, and then describes the design, construction, and typical operation of our reactor. Chapter 3 presents a collection of empirical information obtained from operation of the reactor. Chapter 4 concerns the use of HF vapor cleaning to reduce the amount of surface oxide to a minimum before wafers are inserted into the reactor. Chapter 5 describes a computer model for predicting the deposition uniformity inside our reactor, and also proposes a hypothetical production-sized reactor. The Appendix contains drawings of the completed system, control recipes, maintenance procedures, procedure on processing selective epitaxy wafers, operating procedure for the reactor, and the process flow that was used to make devices for electrical characterization.

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Chapter 2
Hot-Wall Reactors and Silicon Epitaxy

Tubular hot-wall furnaces are characterized by their simplicity and homogeneous temperature. This makes them suitable for low cost vapor deposition of many materials. The same reasons make them suited for studies concerning the equilibrium and kinetics of vapor deposition. Such studies concerning silicon deposition have, for example, been done by Ban et. al. [1], Nishizawa et. al. [2], and Woodruff et. al. [3]. The chronological review in the first part of this chapter examines the less common topic of epitaxial silicon deposition in hot-wall reactors. The second part of this chapter describes how we approached the design, construction, and operation of our hot-wall reactor.

2.1 Historical Perspective

It was realized early in the development of vapor phase epitaxial reactors that hot-wall heating is less complex and expensive than the induction heating necessary to build a cold-wall reactor. The first investigation of hot-wall silicon epitaxy was published only about a year after epitaxial silicon deposited in a cold-wall reactor was first used to fabricate a transistor. Despite this early beginning there has been surprisingly little published on hot-wall silicon epitaxy in the last 30 years. The review contains only six projects dealing with the feasibility of using hot-wall reactors to deposit epitaxial silicon. The paucity of work is no doubt due in part to the very high deposition temperatures that epitaxy traditionally has required. Most of the work on hot-wall epitaxy struggles with the depletion effects due to high temperatures. This is likely to change with a better understanding of the factors that limit epitaxial deposition temperatures, and also the need

for thin layers with sharp doping transitions. Our work and recent work by Meyerson et. al. described in the last section is indicative of this trend.

2.1.1 Deal

The article published by Deal in 1962 is the first to propose the use of the hot-wall configuration as an alternative to the more expensive cold-wall technique [4]. The project was undertaken to determine if the cold-wall configuration was necessary to deposit epitaxial silicon, or if the simpler hot-wall approach was a practical alternative. Feasibility of the hot-wall approach was demonstrated by using a modified atmospheric diffusion tube to deposit epitaxial silicon. However, because of the high temperatures used in this system there were severe depletion problems.

The furnace used by Deal was 26 inches long with 3 heat zones using quartz or Mullite reaction tubes of 45 mm ID. Prior to deposition the wafers were exposed to 15 min of pure H_2. During deposition the gas composition was 0.025 mole fraction $SiCl_4$ in about 3 l/min of H_2. Both the H_2 bake and deposition were performed at atmospheric pressure using temperatures around 1250° C. A single wafer system was built first, and then later modified to accommodate 3 wafers. In both cases the wafers were placed horizontally. In the 3 wafer system the wafers were placed next to each other under a cover which concentrated the gas flow. Because of premature gas phase decomposition of the $SiCl_4$ above 1000° C, an injector cooled by N_2 was necessary to deliver the gas to the wafers. The deposition rate for the 3 wafer system was about 1.3 μm/min ± 10%. Undoped resistivity was between 3.0 and 0.2 ohm-cm. The need to control water vapor and air entering in to the system was acknowledged but not connected with the very high temperatures needed to grow epitaxially. The electrical performance of bipolar transistors manufactured in the epitaxial layers were found to be worse than those made on non-

epitaxial wafers.

This paper by Deal is important because it demonstrates that the concern for the high cost and complexity of cold-wall deposition systems has been around since the beginning of epitaxy. The paper does verify that epitaxial deposition is possible with hot-wall heating. The results on the other hand do not show any advantage of hot-wall over cold-wall for the high temperatures used in the experiments. Injectors and wafers laying next to each other, just as in a cold-wall system, were both necessary because of the strong depletion effects.

2.1.2 Lombos and Somogyi

To counteract the depletion due to deposition, Lombos and Somogyi proposed the use of a sloped temperature profile instead of injectors [5]. This simplifies the design and construction of the furnace but makes process control more difficult because the temperature profile necessary for uniform growth can be affected by many parameters.

An atmospheric pressure system consisting of a 125 cm long quartz tube with a 40 mm diameter was used. The wafers were prepared for deposition by a bake in pure H_2. Source gas composition during deposition was 0.03 mole fraction $SiCl_4$ in 8 l/min H_2. The temperature during baking and deposition was sloped, increasing in the direction of the gas flow. Across the 8 cm long zone where 4 wafers were placed the temperature increased from 1200° C to 1300° C in the direction of gas flow. With this temperature profile of 12.5° C/cm the deposition rate for the 4 wafers was 0.25 µm/min ± 5%. From diodes the impurity concentration of the undoped deposition was measured to be $9 \cdot 10^{16}$ cm^{-3} ± 30% n-type.

It was demonstrated that deposition could be made uniform along the reaction zone without having to control the gas flow pattern inside the reactor if the temperature

profile was adjusted to compensate for the depletion. However, the high temperatures used in the experiments required a large gradient limiting the length of the zone where deposition is practical. The overall growth rate was by this scheme much lower than in the approach used by Deal. The wafers were laying flat next to each other so the system resulted in a low growth rate and a low packing density.

2.1.3 Bloem et. al.

The uniformity of deposition can also be improved by adjusting the composition of the input gas so that the overall reaction rate is reduced. This approach was used by Bloem et. al. in a series of publications on growth near equilibrium [6, 7, 8, 9]. Equilibrium calculations were emphasized to predict the the growth rate uniformity and deposition selectivity. The goal of the research was to investigate the possibility of growing epitaxial silicon cheaply for solar cells by using a hot-wall tube furnace by densely packing the wafers perpendicularly to the gas flow. The low-cost deposition of polycrystalline silicon in hot-wall tubes was used as the motivation for their research.

The experimental reactor was a 260 cm long quartz tube with 45 mm ID operating at atmospheric pressure. Wafers were loaded by cutting 5 cm diameter wafers in half and placing them perpendicularly to the gas stream with a spacing of 5 cm. The heated length was 135 cm with the unheated portion acting as a "load-lock" by allowing the wafers to be purged with H_2 before inserted into the hot zone. Once inside the hot zone the wafers are prepared for deposition by using a 0.5% HCl etch for 5 min (etch rate 0.02 μm/min). The oxygen and water content of the H_2 gas was specified to be below 1 ppm at all times and the total flow was fixed at 3.5 l/min. The silicon source gas was either $SiHCl_3$, or SiH_2Cl_2, in H_2 with HCl added to bring the composition closer to the desired input supersaturation. Deposition temperatures were between 950° C and 1100° C but

1000° C was reported to be the minimum required for acceptable epitaxial quality. Published micrographs would show a smooth surface only for temperatures above 1080° C. For the smooth films the micrographs indicate about 2000 hillocks/cm^2.

Using a temperature gradient of 2° C/cm in the direction of gas flow, the deposition rate would first increase at the front of the reactor, and then become almost constant at 0.1 to 0.3 μm/min for part of the distance along the reactor. This behavior is explained by the gas attaining equilibrium, and that the imposed temperature gradient increases the supersaturation by just enough to compensate for any decrease due to deposition. The calculated supersaturation was based on the total silicon solubility at equilibrium. According to this definition the authors report that for a supersaturation less than 10% the deposition is selective with respect to the quartz walls in the furnace and oxide present on the wafers. The data shows, however, that initial supersaturations of at least 10% are required to get a substantial region with constant deposition rate. The deposition uniformity across each slice is reported to be about ± 40%.

This work first stresses the importance of high packing density in a hot-wall reactor to decrease the cost of epitaxy. It showed that, despite using high temperatures and atmospheric pressures, large amounts of HCl (10-25%) could be added to reduce the net deposition rate so that a moderate gas flow and temperature profile was sufficient to achieve uniform deposition. However, since the system is operating at atmospheric pressure mass transport effects are evident, despite the large spacing the, uniformity across each slice was poor. By insisting that the deposition is entirely determined by the thermodynamic equilibrium kinetic effects were not addressed. It is not clear from the thermodynamic calculations how depletion affects the supersaturation because a Cl/H parameter is used to predict the necessary temperature gradient. Further, according to thermodynamics, there should be no dependence on which source gas is used if the Si/Cl and Cl/H

ratios are the same. The authors state that this is the case, but their data indicate that for identical conditions the growth rate for $SiHCl_3$ is at least 35% lower than that for SiH_2Cl_2. The epitaxial films grown using $SiHCl_3$ were also smoother and could be deposited at lower temperatures than those using SiH_2Cl_2.

2.1.4 Langlais et. al.

If the pressure inside the reactor is reduced, growth rates decrease and diffusion rates increase, both of which help improve deposition uniformity. Langlais et. al. were the first to propose and demonstrate reduced pressure hot-wall silicon epitaxy [10]. Their goal was to show the feasibility of a high packing density system that would benefit from the improved gas transport and homogeneous temperature that a reduced pressure hot-wall system could offer.

The experimental reactor consisted of a 50 mm diameter horizontal quartz tube heated by a furnace to give a 25 cm long zone of constant temperature. A mechanical rotary pump was connected at the rear of the system to maintain operating pressures in the 1-100 torr range. One sample at a time was processed by laying it horizontally on a quartz holder and inserting it into the hot zone from a load-locked chamber at the front of the system. Gas was injected at the front of the system and consisted of SiH_2Cl_2 in H_2 for a total flow rate of about 100 l/h (measured at atmospheric pressure). The relative amounts of SiH_2Cl_2 and H_2 were adjusted to achieve Cl/H ratios in the range of 10^{-3} to 10^{-1}. Monocrystalline films were grown at rates of of 0.1-0.2 μm/min above 1000° C and a system pressure of 1 torr. The depletion of source species at the output due to silicon deposits on the reactor walls and the sample holder did not exceed 30%. The apparent activation energy of the monocrystalline depositions above 1000° C was zero, or negative. The authors do not consider that their results indicate that depletion is a significant effect.

Depletion is not accounted for when using thermodynamically calculated values for $SiCl_2$ to determine the kinetics for the deposition.

This work demonstrated that SiH_2Cl_2 in H_2 at pressures of 1 torr in a hot-wall reactor can be used to deposit epitaxial silicon. It also demonstrates, even though not explicitly stated, that depletion effects are still significant at 1000° C despite the increased gas transport rates and reduced deposition rates that the low pressure operation provides. The important issue of multiple wafer deposition needed for an economical system was not addressed by their experiments.

2.1.5 Ogirima and Takahashi

At this point it can be concluded that because of the large amount of heated areas in a hot-wall reactor the growth rates must be lower than in a cold-wall system. This loss in through-put would have to be compensated for by increasing the packing density of the wafers inside the reactor. It is conveniently done by placing the wafers perpendicularly to the axis of the tube. The densely packed wafers require a reduced system pressure to achieve uniform deposition across each wafer. Ogirima et. al. designed and built such a high capacity hot-wall reduced pressure reactor for epitaxial silicon deposition [11, 12].

The 100 mm diameter quartz tube reactor was heated by a 3 zone heater. The hot zone accommodated 20-30 wafers of 3 inch diameter placed perpendicularly to the tube axis and main gas flow. The pumping system was connected to the water cooled front end and consisted of a 3800 l/min Roots pump backed by a 1000 l/min rotary pump. Gas was injected at the rear using an injector set-up referred to as a "nozzle". The silicon source was SiH_2Cl_2 in H_2 with doping possible by the addition of PH_3. Data presented from a series of experiments on 9 wafers at unspecified spacing shows that for a H_2 flow rate of 16 l/min and a mole fraction of 0.02 SiH_2Cl_2 the deposition rate was 0.22 μm/min

at 900° C and 11 torr. The uniformity across each wafer and along the reactor for these conditions was ± 4%. If the temperature and pressure were increased to 950° C and 25 torr the uniformity degraded to ± 14%. Increasing the pressure to 100 torr at the same temperature of 950° C the uniformity degraded further, becoming ± 40%. The quality of the epitaxial layers were dependent on the pre-epitaxial treatment and loading conditions. With the use of a new loading system under low pressure the authors state that less than 100 OSF/cm^2 were obtained.

The reactor presented by Ogirima et. al. is the first hot-wall system that looks practical. The data presented shows how strongly uniformity is affected by temperature and pressure. Hot-wall epitaxy on large number of wafers at a time cannot be achieved unless both low temperatures and pressures are used. The growth rates will be low but that may not be a disadvantage for applications where thin layers are desired.

2.1.6 Meyerson et. al.

Silicon epitaxy has traditionally required temperatures above 1000° C. This limit is related to the high sensitivity of epitaxial deposition to contamination on the starting surface. Lower epitaxial deposition temperatures are possible if a reactor is designed to reduce the presence of contamination below standard reactors. This approach was used by Meyerson et. al. to build a hot-wall reactor able to deposit epitaxial silicon at temperatures as low as 750° C [13, 14]. The temperature range was later extended to 550° C, and high level boron doping was shown to be possible [15]. Good quality IC devices have been built using layers deposited at 550° C [16, 17].

Based on the results published by Ghidini and Smith on the critical pressures of O_2 and H_2O that would cause clean silicon surfaces to oxidize [18, 19], Meyerson et. al. designed their reactor specifically to reduce the background pressure of these contam-

inants. The reactor consists of a furnace heated quartz tube with a separately pumped load chamber at the front, allowing the reactor itself to be kept under vacuum at all times. The reaction area is evacuated by a turbopump backed by a Roots blower and rotary pump system. An external RF coil is used to clean the reaction chamber prior to depositions by inducing an H_2 plasma. After such a treatment it is reported that the background pressure of H_2O is 10^{-10} torr. The hot zone can accommodate up to 35 wafers of 3.25 inch diameter with the wafers placed perpendicularly to the axis of the tube in a 6 inch long carrier. The wafers are prepared for deposition with a standard RCA clean followed by 10 sec dip in dilute HF to remove all oxides and passivate the surface [20]. No final rinse in water is mentioned. Loading of the furnace is accomplished by placing the wafers in a carrier inside the load chamber. After a 30 min 100° C pre-bake in the load chamber the wafers are introduced into the reaction chamber under a 600 sccm H_2 flow and pressure of 200 mtorr. This purge is continued for 5 min prior to a pumpdown to the base pressure of 10^{-9} torr "to remove the passivating hydrogen" from the HF dip in an atmosphere with a minimum of contamination present [20]. The deposition is performed at a pressure of 1-2 mtorr using 2 sccm SiH_4 and 20 sccm H_2. Reported growth rates vary from 40-120 Å/min over the 550-775° C range. Uniformity across the load of wafers and across each wafer is reported to be ± 2%. The silicon source is SiH_4, and the deposition of silicon is not selective with respect to oxide. The use of HCl in the system as an in-situ etch to clean the substrates was reported to raise the base pressure from 10^{-10} torr to 10^{-5} torr because of the presence of chlorosilanes that could not be removed by baking [13].

TEM and x-ray topography was used to evaluate the crystallographic quality of 550° C deposited films and revealed less than 10^3 defects/cm^2. Fully activated Boron doping as high as $1.5 \cdot 10^{20}$ cm^{-3} is possible at 550° C without affecting the crystallographic defect count, and the transition width is reported to be only 3-10 Å. Background

doping of carbon and oxygen was measured with SIMS[13]. The carbon level was about $6 \cdot 10^{16}$ cm^3 in the bulk of the film with a 10^{19} cm^3 peak at the substrate interface. Oxygen was at the SIMS background limit of 10^{17} cm^3 in the bulk and $3 \cdot 10^{18}$ cm^3 at the substrate interface. The bulk levels are impressively low but no mention is made of the rather large peaks at the substrate interface. Neither the source nor impact on epitaxial quality is discussed.

A significant aspect of the work by Meyerson et. al. in comparison to the prior work in this review is that they designed their furnace from fundamental requirements rather than just following standard practices. By operating at much lower pressures than conventional reduced pressure epitaxy (100-20 torr) the sensitivity to source gas contamination content was decreased. The use of a separately evacuated load chamber prevented the exposure of the reactor to air. Contribution to the background concentration of water adsorbed to surfaces inside the reactor after exposure to air was found to be significant. Operation of the reactor without using the vacuum loading technique resulted in the background pressure of H_2O rising 3 orders of magnitude to 10^{-7} torr and epitaxial deposition was not possible even if the temperature was raised to 850° C [13]. The disadvantage, if any, of an evacuated load chamber is that it adds significantly to the complexity of scaling such a system to production size. The operation at very low pressures also did not seem compatible with chlorosilanes which precludes selective deposition.

2.2 Our Hot-Wall Reactor Approach

Our reactor was designed and built before the work described in the previous section by Meyerson et. al. was published, but we followed a similar fundamental approach. From the other published results on hot-wall epitaxy it was clear to us that the

feasibility had been demonstrated, but the use of high temperatures was limiting the ability to deposit uniformly on enough wafers at a time to make it a practical process. Polycrystalline deposition of silicon is in contrast a highly successful and economical process performed in tubular hot-wall reactors. Polycrystalline silicon is routinely deposited in high volume production on 200 wafers of 6 inch diameter with better than ± 10% (3σ) uniformity. This performance is accomplished by depositing at a low rate of 100-200 Å/min under low pressure conditions so that gas transport is not limiting the growth rate. Our approach was, therefore, to design a system similar to those used for polycrystalline silicon deposition by starting with a standard low-pressure tubular furnace, and then modifying it in accordance with our understanding of epitaxial deposition requirements.

2.2.1 Surface Oxide Removal Limits

The fundamental problem of epitaxy, and what distinguishes it from polycrystalline deposition, is that an almost perfect template is necessary to ensure defect free crystal structure of the deposited film. In practical terms this means that at the start of the deposition phase inside an epitaxial reactor the substrate must be free of any surface contamination. Bare silicon is very reactive and has a strong tendency to oxidize. Wafers inserted into the reactor will always have some film on their surface, e.g. as formed by reaction with the air ("native oxide") and/or during the pre-epitaxial cleaning step ("chemical oxide"). Thus the reactor cycle must incorporate an "oxide removal" step before the deposition can begin. Because of our desire for low cost and complexity, the traditional method of removing surface oxides by heating the wafers under vacuum in H_2 has been chosen. Other approaches such as plasma cleaning are possible, but difficult and expensive to implement in a tightly packed tubular geometry.

The two components of air that are responsible for surface oxide formation are

O_2 (20%) and H_2O (3% max. at 25° C). Inevitably some O_2 and H_2O will also find their way into the reactor, where they can prevent the removal of the surface oxide if present at a high enough level. With an understanding of the maximum levels that can be tolerated without the formation of SiO_2, the reactor can be designed around the fundamental constraint of avoiding surface oxide formation. The oxidizing contamination constraint can be obtained from either thermodynamic calculations, or the work on critical pressures to form SiO_2 by Ghidini and Smith [19, 18]. The two methods are not equivalent and will give different answers. Since it cannot be determined a priori which method is more valid, both methods will be examined when considering the design of the reactor in this chapter. In the next chapter the ideas developed in this section will be used to examine actual oxide removal results obtained from the hot-wall reactor.

Inside the reactor following reactions can be used to describe the interaction between the contaminated H_2 ambient and the wafers:

$$O_2 + 2H_2 \rightarrow 2H_2O \tag{2.1}$$

$$2H_2O + Si(s) \rightarrow SiO_2(s) + 2H_2 \tag{2.2}$$

$$H_2O + Si(s) \rightarrow SiO\uparrow + H_2 \tag{2.3}$$

$$H_2 + SiO_2(s) \rightarrow SiO\uparrow + H_2O \tag{2.4}$$

$$Si(s) + SiO_2(s) \rightarrow 2SiO\uparrow \tag{2.5}$$

Reaction (2.1) is highly favored thermodynamically, but has a large kinetic barrier. For example, O_2 and H_2 can be mixed at room temperature without reaction unless a spark or other source of energy initiates the reaction (i.e. explosion). For design purposes it is

desirable to consider the worst case which assumes that reaction (2.1) has completely converted all present O_2 to H_2O. The conversion to H_2O is a worst case because it oxidizes silicon faster than O_2, and H_2O is more difficult to remove from the inside of the reactor since it can adsorb on the walls. The H_2O can either oxidize or etch the silicon surface via reactions (2.2) and (2.3). At low partial pressures of H_2O the effect of reaction (2.3) will become stronger and pitting of the silicon surface is possible. Removal of SiO_2 can occur both from reduction by the H_2 in reaction (2.4), and by reduction along the silicon interface according to reaction (2.5). Kinetically reaction (2.4) is very slow and the removal occurs preferentially along the silicon interface via reaction (2.5) [21]. The important implications of reaction (2.5) on selective epitaxy will be discussed further in Chapter 4.

To calculate the thermodynamic limit to the complete removal of any surface oxide reaction (2.5) is used together with any one of reactions (2.2)-(2.4) (equivalent thermodynamically). For example if reaction (2.5) and (2.3) are used, the following equilibrium expressions are obtained:

$$K_1 = P_{SiO}{}^2 = e^{-\Delta G_1(T)/RT} \tag{2.6}$$

$$K_2 = \frac{P_{H_2} P_{SiO}}{P_{H_2O}} = e^{-\Delta G_2(T)/RT} \tag{2.7}$$

Eliminating the SiO pressure between (2.6) and (2.7) gives us the desired relationship:

$$\frac{[H_2O]}{[H_2]} = \frac{P_{H_2O}}{P_{H_2}} = \frac{K_1{}^{1.5}}{K_2} = A\,e^{-E_a/kT} \tag{2.8}$$

From formation energies listed in the JANAF tables [22] A = 28.6 and E_a = 2.06 eV in equation (2.8). This result is plotted as the solid line in Fig. 2.1. The total contribution

of H_2O from the reactor and gas source must be below the solid line for the desired operating temperature in order to obtain oxide free surfaces inside the reactor during the H_2 bake. The allowable amount of H_2O is only dependent on its relative concentration with respect to H_2. It is not dependent on the total pressure.

The thermodynamic result is quite different from the experimental results obtained by Ghidini and Smith [19, 18]. They measured the critical pressure of H_2O that would result in SiO_2 forming on bare silicon surfaces. The experiments were performed in a ultra high vacuum system (UHV) with only the sample heated by flowing a current through it. Temperatures were measured with an optical pyrometer to an accuracy of ± 10° C. Inside the UHV system the silicon samples were first cleaned by heating them for 5-10 min at 1350° C and 10^{-7} torr. A large amount of SiO was detected inside the system while the surface oxide was being removed. Once cleared of oxide the sample was cooled to a temperature in the range of 890-1150° C before H_2O was admitted through a leak valve. The onset of oxidation was observed by the change of emissivity recorded with the pyrometer. Two distinct regions of emissivity were detected, one corresponding to a surface partially covered with SiO_2, and another corresponding to complete SiO_2 coverage. The region of incomplete coverage was explained by H_2O etching the silicon surface via reaction (2.3). The critical H_2O pressures data was observed to fit well to a standard Arrhenius relationship of the form:

$$P_{c(H_2O)} = P_o \, e^{-E_a/kT} \tag{2.9}$$

For the upper boundary $P_0 = 2.3 \cdot 10^{13}$ torr and $E_a = 3.9$ eV was obtained, and for the lower boundary $P_0 = 5.6 \cdot 10^7$ torr and $E_a = 3.0$ eV. These two equation are plotted as the solid lines in Fig. 2.2. According to these results the reactor must be designed so that the

H_2O pressure due to all source of contamination is below the lower solid line at the desired operating temperature.

The O_2 and H_2O get inside the reactor in four ways: gas supply contamination, leaks, permeation, and outgassing. The background concentration of H_2O (assuming full conversion of O_2 to H_2O) is the sum of these sources. Contamination of the gas supply can be the most significant and difficult to control unless the gas is purified at the point of use. Besides the purity limitations due to the actual source such as a gas bottle there is also the problem of contamination introduced anywhere along the usually long path that the gas must travel to get to the reactor. Consistently obtaining 1 ppm or less of H_2O could be difficult. Epitaxy results depend strongly on the purity of the H_2 and an important decision was to install a palladium diffusion cell H_2 purifier just prior to the mass flow controller that injects H_2 into the reactor. The purifier isolates the reactor from the possibly contaminated gas source, and supplies H_2 that can be assumed to contain insignificant amounts of H_2O.

The sources of H_2O inside the reactor that must still be considered are leaks, permeation (diffusion), and outgassing associated with the gas control plumbing, injectors, and reactor vessel. In the following discussion the amount of H_2O due to each of these sources will be estimated for nominal conditions of a 1 sl/min flow of H_2 at 1 torr. The reactor configuration is assumed to be a 100 cm long quartz tube of 15.5 cm ID and 3 mm wall thickness. The estimated values can easily be scaled for other conditions and configurations according to the equations that estimate the contribution to the background concentration for each effect.

Air leaks into the reactor add O_2 and H_2O in a straightforward manner. The contribution to the background amount of water can be expressed as:

$$\frac{[H_2O]}{[H_2]} = \frac{L_{air}\,(C_{O_2} + C_{H_2O})}{F_{H_2}} \tag{2.10}$$

where L_{air} is the volumetric leak rate of air in to the system, C denotes the concentration of O_2 and H_2O in air, and F_{H_2} is the molar flow rate of H_2. The contribution of a 10^{-6} cm^3/sec leak of air in to the a system with a flow rate of 1 sl/min of H_2 (1 mole = 22.4 sl) is shown by dashed line (1) in Figs. 2.1 and 2.2. Note that for Fig. 2.2. the total system pressure (nominally 1 torr) must be used to convert the background concentration to a pressure of H_2O. According to the thermodynamic limit curve in Fig. 2.1 such a leak would lead to a lower temperature limit of about 840° C, and for Fig. 2.2 the lower limit would be 690° C.

Since diffusion coefficients are exponentially dependent on temperature, permeation of O_2 and H_2O from the air in to the reactor through the heated walls by diffusion is a concern. This contribution can be expressed as:

$$\frac{[H_2O]}{[H_2]} = \frac{(D_{O_2}C_{O_2} + D_{H_2O}C_{H_2O})\,(\pi dL)}{\delta\, F_{H_2}} \tag{2.11}$$

where D is the diffusion coefficient of O_2 and H_2O through the reactor wall at the given temperature, and δ is the wall thickness. The heated area for a tubular reactor of diameter d and heater length L is assumed. A common material for the reactor wall is quartz (crystalline SiO_2) for which the permeation rate is supposed to be less than for glass (noncrystalline SiO_2) [23]. By using the diffusion coefficients for SiO_2 as given in Sze's VLSI Technology [24] a worst case estimate can be obtained. The resulting diffusion contribution versus temperature for a quartz tube of 100 cm heated length, diameter of 15.5 cm, and 3 mm wall thickness is plotted as dotted line (2) in Figs. 2.1 and 2.2 for a flow rate

of 1 sl/min of H_2 at 1 torr reactor pressure. The dimensions are those of the original quartz tube and heater that were present in the system that was modified for epitaxial deposition. The resulting lower limit in Fig. 2.2 for this tube and conditions would be 750° C, while according to the thermodynamic limit in Fig. 2.1 epitaxial deposition would not be possible at all. As an example of how possible options can be evaluated, the dashed line (3) in Fig. 2.1 shows the reduction in H_2O due to increasing the wall thickness of the quartz tube to 6 mm and increasing the H_2 flow rate to 10 sl/min. The resulting minimum temperature is now 850° C.

The final and most poorly understood contributor is outgassing. This is a phenomenon usually only of great concern for UHV systems [23]. For reactors operating only at reduced or low pressures (down to about 1 torr) it is not often considered to be significant. However, epitaxial deposition, as shown in Figs. 2.1 and 2.2, is very sensitive to the presence of H_2O. Adsorption of H_2O to the inside surfaces of the reactor and its subsequent release is a very temperature sensitive process but does not have a single activation energy [25,26,27,28]. Instead it depends strongly on the surface treatment of the surface and microscopic structure of the material. The measured water release rate consists of both water desorbing from the surface and water diffusing to the surface before desorbing from the surface. The total amount of water desorbed can be as high as the equivalent of 100 monolayers/cm^2 [27]. The rate will be strongly dependent on temperature with a combination of several activation energies and the resulting release rate will decrease only slowly with time (first order or less). These characteristics make the water desorption rates specific to the materials in the system and the operation of the system. The longer a surface is exposed to air after being outgassed in vacuum the longer it will relase water because water has had time to diffuse further in to the surface. In our case, unheated areas exposed to air during the loading and unloading of wafers are a concern.

Especially the stainless steel door, cantilever suspension block, and injection tubing have to be considered. The contribution to the background of H_2O inside the system can be expressed as:

$$\frac{[H_2O]}{[H_2]} = \frac{A\, G_{H_2O}(T)}{R\, T\, F_{H_2}} \tag{2.12}$$

where R is the gas constant, T the temperature, and G the outgassing rate usually given in the units of torr-l/sec-cm^2 or equivalent. Published values for G at room temperature after one hour pumping range from around 10^{-7} (untreated) to 10^{-9} torr-l/sec-cm^2 (after surface treatments), decreasing about an order of magnitude after 10 hours [23]. We will assume as a worst case that all of the outgassing is H_2O. According to equation (2.13) these rates would result in $[H_2O]/[H_2]$ levels of $7{\cdot}10^{-9}$ to $7{\cdot}10^{-11}$ per cm^2 of surface area for a H_2 flow rate of 1 sl/min. A 1 meter long section of 1/4 inch stainless steel tubing has an internal surface area of 143 cm^2 so the outgassing levels can quickly become significant in Figs. 2.1 and 2.2. Keeping the system under vacuum as much as possible and exposing it to air for as short time as possible will be important. The use of a N_2 purged load station as proposed in Chapter 6 eliminates the exposure of the system to air reducing the potential for outgassing.

Before describing the actual system that has been built, the differences between the thermodynamically calculated limit in Fig. 2.1 and the experimentally measured limit in Fig. 2.2 should be examined. The most important difference is that the measured limit depends on the absolute pressure of H_2O, as opposed to the thermodynamically calculated limit which depends on the concentration of H_2O relative to H_2. For the experimental results in Fig. 2.2 the minimum temperature that removes a surface oxide according to the kinetic limit decreases not only by an increase in the flow rate of H_2, but also by a

decrease in the total reactor pressure. In the case of the thermodynamically calculated limit there is no benefit from decreasing the reactor pressure. It is not clear, however, how applicable the experimentally measured limit is to our conditions. Ghidini and Smith measured their critical pressures by admitting only H_2O into a system where only the silicon sample was heated. In our reactor there is a great excess of H_2 which can alter the oxidation limit by both being part of the overall reactions (2.2)-(2.4), and by competing for surface sites. Furthermore, in Ghidini and Smith's system the cold reactor walls act as a sink to SiO, preventing equilibrium from being attained for reaction (2.5). It could, therefore, be argued that the conditions in a hot-wall system with an excess of H_2 and a low flow-rate is closer to the thermodynamic equilibrium case.

The hot-wall reactor results by Meyerson et. al. agree with the limit measured by Ghidini and Smith. Meyerson et. al. quote their background pressure of H_2O to be 10^{-10} torr and report epitaxial deposition down to 550° C. Extrapolating the data measured by Ghidini and Smith would give a lower temperature limit of 578° C. The 200 mtorr of H_2 during the loading and beginning of the bake results in a $[H_2O]/[H_2]$ equal to $5 \cdot 10^{-10}$ which according to the thermodynamic limit results in a minimum temperature of 692° C. The reported successful use of a base pressure bake at 10^{-9} torr should not work at all according to the thermodynamic limit if the H_2O pressure is 10^{-10} torr. The validity of the thermodynamic equilibrium assumption may also not be true at such extremely low pressures.

There is also other data published concerning epitaxial silicon deposition that agrees with a kinetic limit such as measured by Ghidini and Smith, but obtained in cold-wall systems. An example of such data is the work of Duchemin et. al. [29]. which contains an often referenced table showing how the transition temperature in their system between polycrystalline and monocrystalline decreased from 1000° C at 760 torr to 800°

C at 10 torr. A more recent example has been presented by Borland[30,31] where system pressure is raised to 100 torr in order to grow selective polysilicon rather than selective epitaxial silicon. A pressure below 50 torr normally results in epitaxial deposition, but when, for the same flow rates, the pressure is raised to 100 torr, polysilicon deposition occurs because there is an interfacial oxide layer remaining on the substrate after the H_2 bake.

2.2.2 Design and Construction

The system was designed and built by modifying an existing Tylan low-pressure chemical vapor deposition (LPCVD) furnace. At the time the reactor was designed and built we did not know which of the two limits discussed in the previous section would restrict our ability to achieve epitaxial deposition. The thermodynamic limit is a worst case, and from it we made the important decision to use a silicon carbide furnace tube. Quartz tubes cannot tolerate vacuum operation above about 1000° C without deforming due to the pressure of the atmosphere, and diffusion through a quartz tube wall could also be a limitation. Because silicon carbide is brittle and conducts heat well its use adds complexity to the mating of the furnace to the rest of the system. It can, however, be machined to make smooth sealing surfaces, and will tolerate very large temperature gradients. It is also very strong and well matched to the expansion coefficient of silicon, making it suitable for a silicon deposition environment. Quartz tubes often crack if cooled when coated with a thick layer of silicon.

A schematic of the reactor that was designed and built is shown in Fig. 2.3. The reactor consists of a cylindrical resistive heater surrounding a 7 inch ID silicon carbide furnace tube. At each end of the furnace tube water cooled stainless steel flanges are used to make a door at the front and a connection to the vacuum pump at the rear. The stain-

less steel flanges use a compression seal to a smooth surface machined to the ends of the tube. Cooling water flows in direct contact with the silicon carbide between two o-rings. The 1.5 gallon/min cooling water flow removes about 2.5 kW when the furnace is operating at 850° C, and no part of the flanges gets hotter than 40°-50° C. The door at the front is also made of stainless steel and suspended from the cantilever mount at its center with a ball joint to allow it to seal reliably with the front flange. The cantilever rods are held inside the cantilever mount with teflon bushings. In retrospect this a potentially large source of outgassing, but is simple, reliable, and leak tight. The flanges together with the door and cantilever suspension assembly were designed by us, and were fabricated by the department machine shop. After careful assembly the furnace system did not reveal any leaks down to the 10^{-10} cm^3/sec detection limit of our helium leak detector.

Another important design decision was to try to ensure the highest possible purity of H_2 delivered to the reactor. Therefore, a palladium diffusion cell purifier was mounted as close as possible to the shelf in the furnace cabinet which contains the mass flow controllers. On this shelf the output from mass flow controllers for H_2, SiH_2Cl_2, and N_2 are mixed in to a single 1/4 inch stainless steel injector tube which leads to the front flange of the system. The N_2 is used to vent and purge the system during loading. The wafers are suspended inside the hot zone on a pair of cantilever rods. The wafers are placed in "boats" which holds them upright and perpendicular to main gas flow. The spacing between the wafers depends on how closely the slots in the boats can be cut. The minimum spacing is about 2.4 mm, which means that 100 wafers can be placed in the approximately 9 inch long hot-zone. Wafers of up to 5 inch diameter can be accommodated, but concentric placement results only for 4 inch wafers. Quartz baffles are used to reduce the radiative heat losses at each end of the furnace. The vacuum pump is ballasted with N_2 to reduce backstreaming of oil.

The finished reactor, as shown in Fig. 2.4, looks very much like a standard LPCVD furnace. It is operated with the same computerized controller as the rest of the Tylan furnace system, and is in that sense a prototype system rather than a purely experimental reactor. More detailed drawings and information on the system are given in the Appendix.

2.2.3 Typical Deposition Cycle

The operation of the reactor will be illustrated by considering a typical deposition cycle. We have often operated with variations on the cycle to learn more about the system; especially the bake cycle has been the subject of many experiments. Avoiding an undercut along the silicon/oxide interface dictates that the lowest possible temperature during the bake must be used. The minimum bake temperature has decreased from 1085° C in early experiments to to 900° C as described in Chapter 4. Deposition is performed at 850° C which has been found to give good quality growth with manageable depletion for the present system (quality and uniformity will be considered in the following chapters). The temperature, pressure, and input flow rates are shown versus time in Fig. 2.5 starting from the standard standby temperature of 525° C under vacuum with N_2 flowing at 500 sccm (standard cm^3/min). The 525° C temperature is a compromise between minimizing oxide growth on the wafers and minimizing water adsorption inside the reactor during loading. The deposition cycle consists of 7 major parts which have been labeled A-E in Fig. 2.5.

During the loading step (A) the gate valve is closed and the system is vented for 7.5 min with 5000 sccm N_2. The door and cantilever rods are then pulled out as a unit allowing wafers to be loaded. During the time the system is open an additional 10 lpm (rotometer liters/min) of N_2 flows through the purge inlet shown in Fig. 2.3. We want to

absolutely minimize time the system is exposed air in order to reduce the amount of H_2O that can be adsorbed inside the reactor. Maximum load time is 10 min, but typically loading or unloading is completed in 5 min or less. The system is then closed by pushing the door and cantilever rods unit in again. The N_2 purge flow is terminated and the injected N_2 flow is reduced as the gate valve is opened. Pumping down to less than 1 torr takes about 20 sec after which the system is kept at about 800 mtorr for 10 min with 500 sccm of N_2.

The temperature ramp to the bake temperature (B) is preceded by a a pumpdown to the N_2 ballasted base pressure of about 70-80 mtorr for 30 sec after which the gate valve is closed for 30 sec and the pressure rise is monitored to ensure that there are no large leaks. If the pressure rise is smaller than 100 mtorr (resolution limited by Tylan controller), the H_2 is turned on and a full power ramp to the bake temperature is initiated. The flow rate of H_2 is currently 8 slpm (standard liter/min) during the bake portion of the cycle. It takes about 50 min to reach the baking temperature of 900° C with no temperature overshoot or stabilization problems. External thermocouples (spikes) are used for controlling the furnace temperature, resulting in the internal temperature always approaching the set point monotonically as shown in Fig. 2.5. To make the internal temperature correspond to the set point, the external thermocouples must be calibrated to the internal temperatures for the specific operating conditions. This is a minor inconvenience compared to the difficulties in controlling the reactor temperature directly from internal thermocouples. The maximum rate during the bake ramp is about 10° C/min. The large thermal mass of a hot-wall system is a disadvantage because a large portion of the total cycle time is taken up by temperature changes.

Another important consequence of the slow temperature response is that the silicon surface that has been cleared of surface oxides by the bake must be kept stable,

reformation of an oxide or pitting along the oxide sidewalls cannot be tolerated. Marginal conditions for the silicon surface cannot be overcome by a rapid transition to the deposition stage. Results for H_2 baking below 950° C improves if a small amount of SiH_2Cl_2 is turned on at a time T_1 during the bake (C) as shown in Fig. 2.5.† The SiH_2Cl_2 initiates a small amount of silicon deposition during the bake (C), and ramp down to deposition (D).

The ramp down from the bake temperature of 900° C to the deposition temperature of 850° C takes about 18 min (D). The standard condition during deposition (E) is 400 sccm of H_2 and 32 sccm of SiH_2Cl_2. These conditions have been chosen as a compromise between epitaxial quality and deposition uniformity. The system pressure is limited by the size of the current pump and for the standard deposition conditions in Fig. 2.5 the pressure is about 600 mtorr. Deposition rates for these conditions are 60-80 Å/min, depending on the number of wafers and where they are located. There is nothing magical about the standard conditions, and, in fact, results for both quality and uniformity would probably improve with the higher flow rates and lower pressures that a larger capacity pumping system would provide. These improvements would result from the dilution of the background contamination and improved gas transport.

After the desired deposition time, 100 min for the cycle shown in Fig. 2.5, the temperature is ramped down to 525° C (F). A flow of 1 slpm H_2 is used during the cool down until a temperature of about 600° C is reached. The temperature is ramped down before unloading the wafers so that a new set of wafers can be loaded, and to minimize the stress on the o-rings at the front of the reactor. The wafers are ready to unload (G) after 10 min of N_2 flow by the same procedure as the load at the beginning of the cycle.

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† Results to be published J. C Lou. Mentioned here in order to fully describe the currently used process cycle.

2.3 Summary

Only 6 projects were found since the beginning of hot-wall vapor phase epitaxial growth around 1960. Presented chronologically, the first three by Deal, Lombos and Somogyi, and Bloem et. al. were atmospheric systems. In all cases depletion of the gas stream was severe even if a cooled injector, temperature ramp, or the addition of HCl was used respectively in the three different reactors. In a system with the wafers stacked perpendicularly to the gas stream Bloem et. al. were able to obtain a region of uniform deposition along the length of the reactor but the gas transport limitations caused a 40% variation across wafers. Operation at low pressures enhances gas transport by increasing the diffusion rate, and reduces the growth rate so that there is less rapid depletion. Low pressure reactors were used by the second group of three investigations published by Langlais et. al., Ogirima and Takahashi, and Meyerson et. al. The work by Langlais et. al. demonstrated feasibility on a single slice system, and also that operation at 1000° C even at as low a pressure as 1 torr still leads to significant depletion when SiH_2Cl_2 is used as the source gas. The first practical looking multiple wafer reactor is presented by Ogirima et. al. which when operated with SiH_2Cl_2 as a source gas at 900° C and 11 torr. For these conditions their reactor is capable of deposition on 9 wafers standing perpendicularly to the gas flow with a uniformity of $\pm$ 4% if an injector is used. These results suggest that a production sized reactor would have to operate at still lower pressures and temperatures in order to deposit uniformly on 100 to 200 densely packed wafers as in the case of polycrystalline silicon deposition. Meyerson et. al. took this idea to an extreme by building a reactor able to deposit epitaxial silicon at temperatures as low as 550° C at 1 mtorr with a preceding oxide removal step using 10^{-9} pressure. The high vacuum operation and low temperatures requires the use of SiH_4 as a source gas, and the deposition is no longer selective. The most important aspect of the Meyerson et. al. project is their fundamental

approach to the design of the reactor. Up to this point, the design and construction of epitaxial reactors acknowledged that the presence of impurities such as O_2 and H_2O interfere with epitaxial growth, but were not connected specifically to the traditional use of high temperatures and high flow rates. By using the experimental data obtained by Ghidini and Smith for the critical pressures of O_2 and H_2O that oxidize silicon Meyerson et. al. designed their reactor specifically to get below these critical pressures.

We built our reactor before the publication of the results by Meyerson et. al. but happened to use a similar fundamental approach. By plotting the thermodynamic limitation for SiO_2 removal, and the critical pressures measured by Ghidini and Smith, we estimated the lower limit in temperature due gas supply contamination, leaks, permeation, and outgassing. Since it is not possible to a priori determine which limitation is most appropriate the thermodynamic limitation was used as the worst case. The system was built by modifying an existing Tylan furnace tube in an LPCVD bank according to our understanding of the limitations to epitaxial deposition. In retrospect, the design of the reactor minimizes leaks and permeation problems at the expense of increasing outgassing. Important design decisions were the use of a silicon carbide furnace tube and purification of the H_2 gas as close to the point of use as possible. The typical deposition cycle for best selective epitaxial growth results was used to describe the operation of the finished reactor. The cycle has two major steps, a 8 sl/min H_2 bake at 900° C and 5.6 torr, and deposition using 7.4% SiH_2Cl_2 in H_2 at 850° C and 0.6 torr.

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29. J. P. Duchemin, M. Bonnet, and F. Koelsch, "Kinetics of Silicon Growth under Low Hydrogen Pressure," *J. Electrochem. Soc.*, vol. 125, no. 4, pp. 637-644, April 1978.
30. J. O. Borland, April 9, 1990. Presentation given in seminar at U. C. Berkeley
31. J. O. Borland and I. Beinglass, "Selective Silicon Deposition for the Megabit Age," *Solid State Technology*, pp. 73-78, January 1990.

Fig. 2.1 Thermodynamic limit for the presence of H_2O versus temperature inside the reactor is plotted as a solid line. Dashed line (1) represents contribution of H_2O from a leak for conditions described in the text. Dashed lines (2) and (3) represent contribution from diffusion through furnace wall for conditions described in the text.

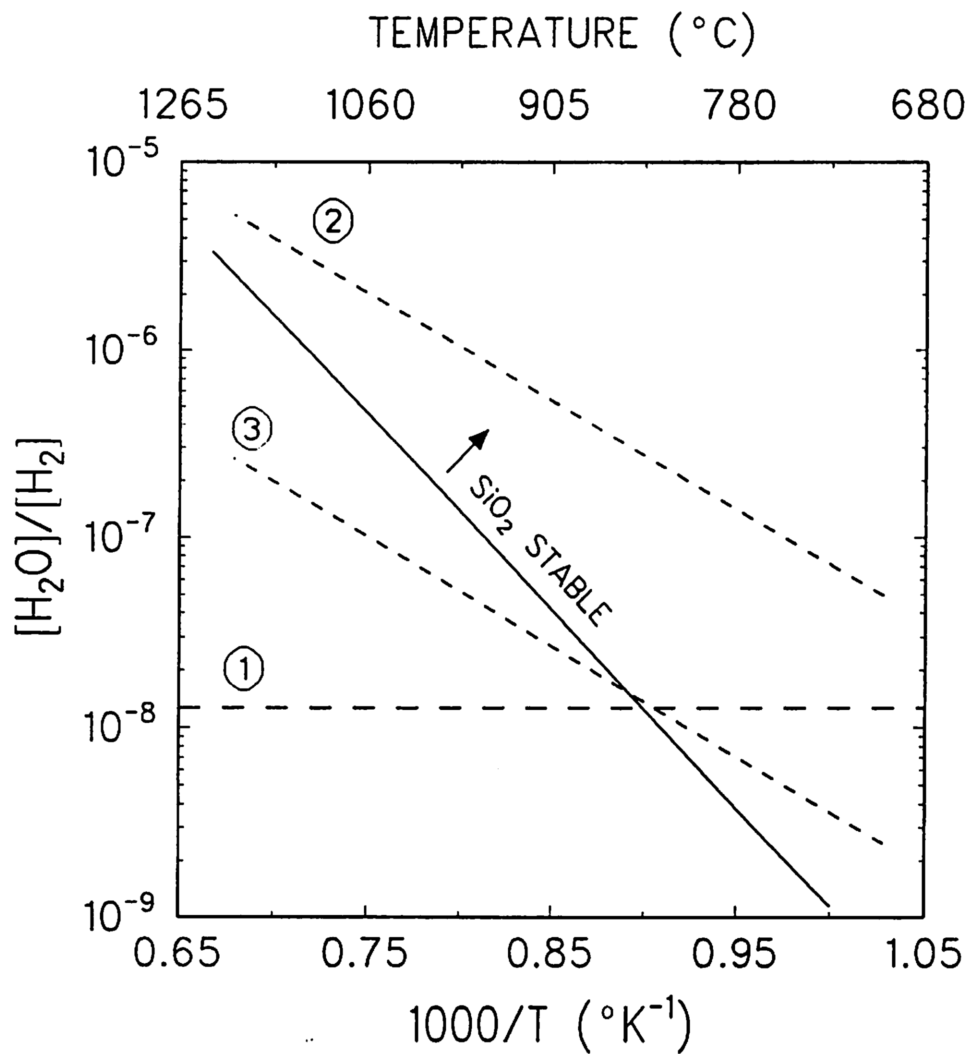


Fig. 2.2 The critical pressure of H_2O versus temperature measured by Ghidini and Smith are plotted as solid lines. Dashed line (1) represents contribution of H_2O from a leak for conditions described in the text. Dashed line (2) represents contribution from diffusion through the furnace wall for conditions described in the text.

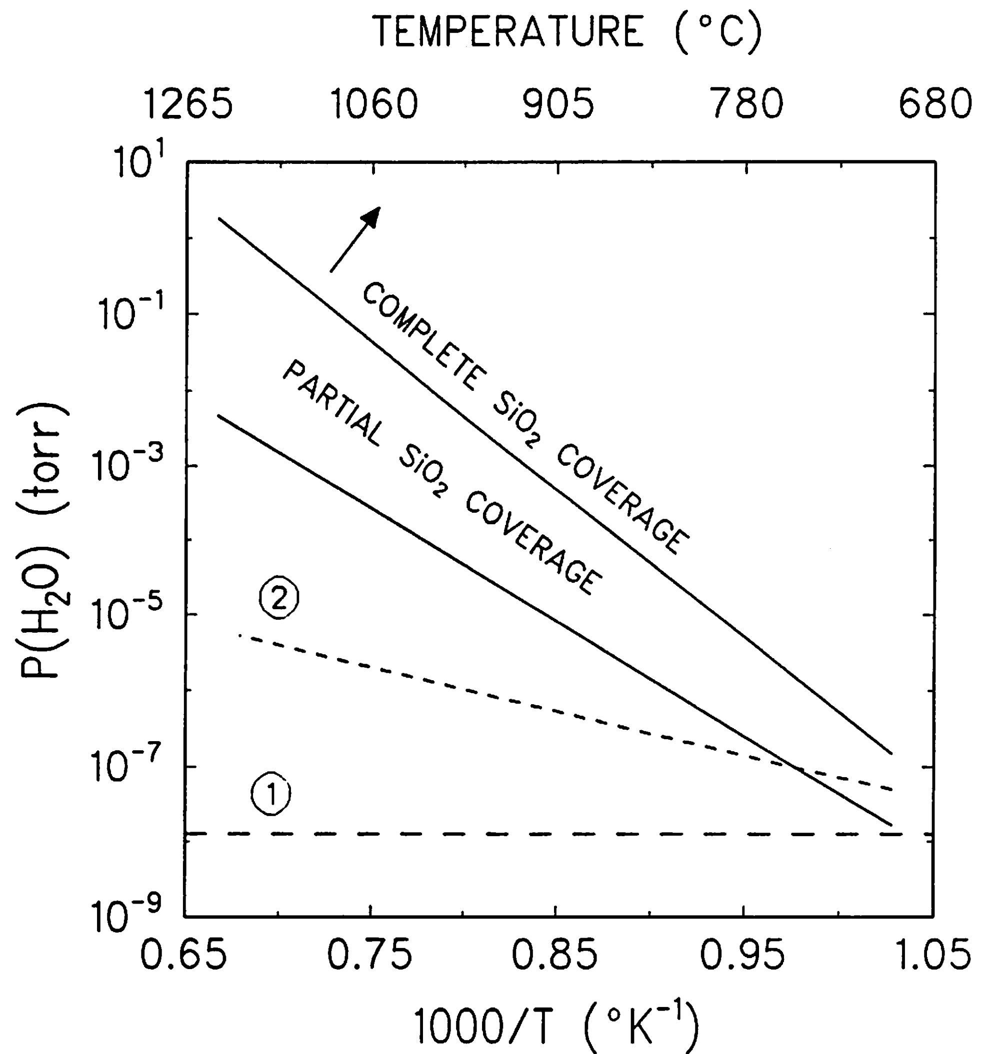


Fig. 2.3 Schematic diagram of our hot-wall low-pressure silicon epitaxy reactor.

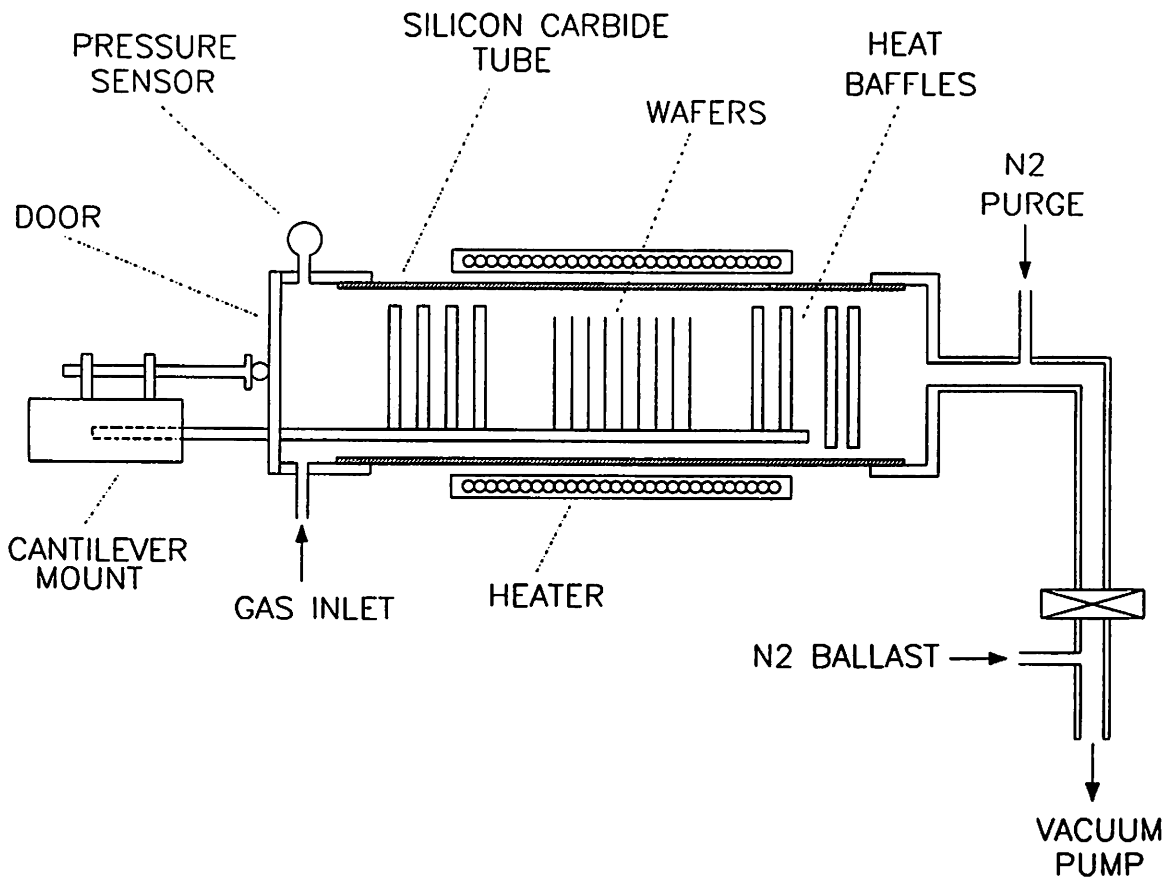
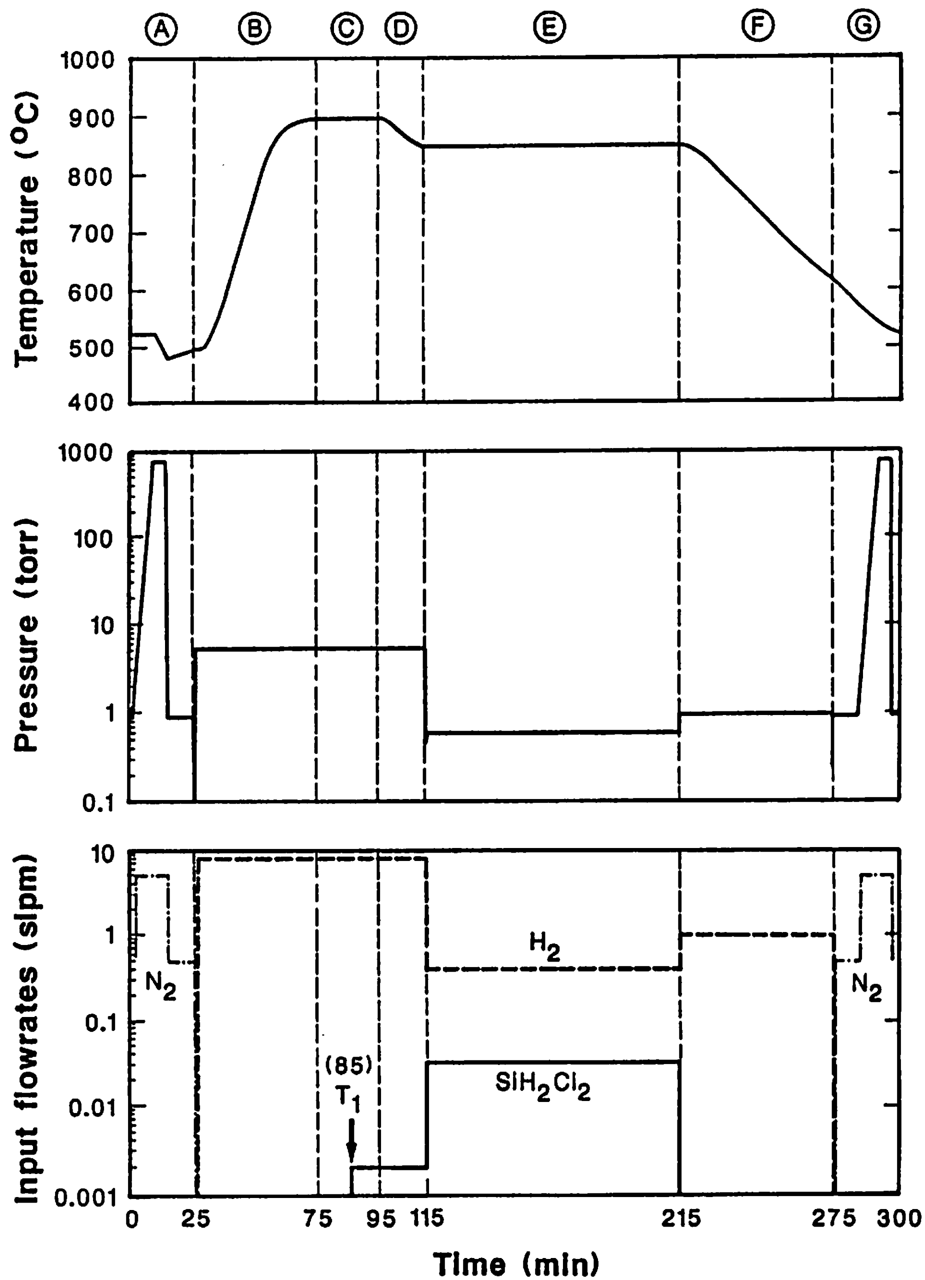


Fig. 2.4 Picture of our hot-wall low-pressure silicon epitaxy reactor. The reactor is the second tube from the top of the LPCVD furnace bank, and is shown open for loading of wafers.

Fig. 2.5 Typical reactor cycle used for deposition of selective epitaxy requiring a low-temperature bake. Used in conjunction with the HF vapor clean described in Chapter 4.



Chapter 3
Basic Issues and Experimental Results

This chapter addresses some of the basic issues pertaining to silicon epitaxy. These include the quality of the silicon interface at the start of deposition, oxygen and carbon contamination, impurity autodoping, conditions that determines the quality of selective growth, and electrical properties. Because of the empirical nature of the topics presented in this chapter it is somewhat open ended with an emphasis on communicating as many of the results as possible so that future researchers can perhaps benefit.

3.1 Hydrogen Baking and Epitaxial Quality

One of the most important factors that determine the quality of the epitaxial growth is the condition of the starting interface. Epitaxial growth requires that deposited atoms are able to align themselves to the atoms of the substrate. From our experience an atomically perfect surface is fortunately not necessary. Essentially defect-free epitaxial films can be deposited even though small patches of oxide and carbon contamination are present at the interface. The presence of adsorbed atoms such as hydrogen apparently also do not interfere with the epitaxial alignment of the depositied atoms. Nevertheless, the amount of surface contamination that can be tolerated at the start of the epitaxial deposition is less than most other process steps used for integrated circuit manufacturing. Very small levels of contamination inside the reactor able to deposit on the substrate, or to prevent the removal of contamination already present on the substrate, can interfere with epitaxial deposition.

Once the film growth has been initiated, impurities represent a much smaller part

of the total flux impinging on the substrates and can be buried before forming large enough clusters to interfere with the epitaxial deposition. We have observed this reduced sensitivity experimentally by reducing the deposition temperature after growth has been initiated. For example, high quality films were obtained if the deposition was initiated at a temperature of 835° C, and then while the deposition was occurring the temperature was reduced to 750° C [Expt.92]. We have not otherwise been able to grow low-defect epitaxial layers at constant temperatures lower than 820° C.

The strong tendency of silicon to oxidize, even if only exposed to room temperature air, makes it necessary to include an oxide removal step inside the reactor before epitaxial deposition can begin. Two possible limitations for the removal of the surface oxide by heating in the presence of hydrogen were described in the previous chapter. The concentration limits of O_2 and H_2O imposed by thermodynamic calculations, or direct measurements by Ghidini and Smith [1,2], are both low, and decrease strongly with decreasing temperature. This section will compare results obtained from operation of the reactor to the behavior predicted by the two models.

An ideal epitaxial film should replicate the crystal structure of the substrate exactly. Since the starting substrate is a flat <100> oriented silicon surface, a similar surface should result after epitaxial deposition. During surface-rate-limited conditions, different crystallographic directions of the silicon grows at different rates, the <100> direction growing fastest, and <111> the slowest. If a disruption to the growth occurs so that a slower growing direction is exposed it may persist and cause a deviation from a flat surface. The persistence of slow-growing facet planes will be maximized under surface rate-limited-conditions such as those in our reactor. The mass-flow-controlled conditions often encountered in conventional cold-wall reactors can make the difference in growth rates between the crystallographic planes less distinct.

Deviations from an ideally flat surface can be observed by using a collimated beam of intense light, a phase contrast enhanced optical microscope (Nomarski method), or a scanning electron microscope (SEM). The light method deserves some special attention since it is a traditional and convenient method to quickly evaluate epitaxial wafer surfaces. A well collimated and intense beam of light is used to observe by eye the light scattered from the surface as shown in Fig. 3.1. Because of the high sensitivity of the human eye, features as small as 0.5 μm can easily be detected by this method. However, because this method involves the human eye, we must resort to verbal descriptions to classify the observations with words such as "sparkles" and "haze". Sparkles appear as point sources of light on the surface. They can vary from faint to very bright, the brightest usually being particles on top of the surface. Haze is more difficult to quantify. Its appearance can vary from a slight cloudiness of the surface to a very strong frosted glass appearance, and a stronger appearance of haze usually correlates with more textured surfaces. Faint haze usually appears milky white, and when stronger looks somewhat brownish. There is an imprecise transition, depending on the observer, between what can be described as a faint uniformly dense distribution of sparkles, or as a light haze.

For epitaxial films deposited in our reactor at a standard temperature of 850° C, deviations from flatness most often appear in the form of a heavily textured surface, or a flat surface containing pits shaped like inverted pyramids when observed with a Nomarski microscope. The sides of the pyramidal defects are always aligned parallel to the {110} planes, and can be used to verify that deposited silicon films are indeed monocrystalline. Examples of the two surface types are shown in the micrographs of Figs. 3.2(a) and 3.2(b). The epitaxial films shown in these two figures contrast the results obtained using a 1060° C hydrogen bake before a standard 850° C deposition with an increase of the H_2 flow rate from 2 slpm (standard liters per minute) to 8 slpm [Expt.36, Expt.37] as the only

variable. For the 2 slpm flow rate the surface is very textured, whereas for the 8 slpm flow rate the surface is smooth with 10^4-10^5 cm^{-2} of pyramidal pits. When observed with collimated light, the film in Fig. 3.2(a) appears uniformly covered with a very strong haze, and the surface in Fig. 3.2(b) is covered with faint sparkles. The presence of these defects is correlated with the amount of oxygen detected by secondary ion mass spectrometry (SIMS) at the interface between the epitaxial layer and the substrate. The SIMS depth profile for the respective samples are shown in Figs. 3.3(a) and 3.3(b). For the sample grown using the 8 slpm H_2 bake the peak of oxygen is an order of magnitude lower and much sharper, indicating that the amount of oxide at the start of deposition was less for that sample. The above results correlates with the expectation from Chapter 2 that a higher flow rate of uncontaminated H_2 should dilute contributions to the background of O_2 and H_2O from other sources.

According to the two scenarios for oxide removal discussed in the previous chapter, the maximum allowable concentration of O_2 and H_2O decreases strongly with decreasing temperature. A fixed background concentration of O_2 and H_2O will, therefore, make the oxide removal less complete as the temperature during the H_2 bake is decreased. The SIMS results shown in Fig. 3.4 corroborate this interpretation. In the experiments of Fig. 3.4., all conditions were kept the same except for the bake temperature which was decreased from 1060° C to 900° C in approximately 50° C increments [Expt.39, Expt.44, Expt.46, Expt.48]. As perhaps expected from the discussion of oxide removal in the Chapter 2, the oxygen peak becomes progressively larger as the bake temperature drops. However, some aspects of these results are puzzling.

The first puzzling result is that the conditions for the experiment in Fig. 3.3(b) [Expt.37] and Fig. 3.4(a) [Expt.39] are almost identical except for the addition of a 3 minute step at the beginning of the deposition during which a maximum flow of SiH_2Cl_2

(100 sccm) and a minimum flow of H_2 (100 sccm) are used. We call this step a "predep". This step eliminates the 10^{19} cm^{-3} peak of oxygen completely, but it is not presently understood how. One possibility is that the introduction of a large amount of SiH_2Cl_2 can somehow reduce the amount of surface oxide, perhaps by etching of silicon, or by direct attack of the oxide. Another possibility is that there is a transient of contamination released when the SiH_2Cl_2 source is turned on. This contamination would become diluted for a higher flow rate. Further experiments would be necessary to fully understand why there is an improvement when a predep step is included†. It is also likely that the improved results described below which are obtained with a small addition of SiH_2Cl_2 during low temperature bakes is related in some way to the predep phenomenon.

The second puzzling result is the ability to cool the reactor to temperatures below those that remove oxides during the bake cycle, and still be able to deposit defect-free epitaxial layers. The size of the oxygen peak for each experiment in Fig. 3.4 seems to depend primarily on the bake temperature, implying that the oxide observed at the interface is that which was not removed during the bake. One possibility is that the regrowth rate of oxide during the cool-down is so low that very little forms, even though it takes up to 35 min to change the temperature to 850° C. Another possibility is a bake-out effect. The higher the temperature at the center of the reactor, the warmer the ends become, increasing the outgassing rate of H_2O that adsorbed during the loading step. As these surfaces cool, their outgassing rate drops below what it would have been without the bake-out, reducing the background pressure of H_2O. The flanges at each end of the reactor are water cooled, but the temperatures of the door assembly can increase because of radiation

† About a week later corrosion was discovered in the dichlorosilane mass flow controller due to a small leak at the bypass sensor seal. An experiment involving only the predep was regrettably not repeated afterwards.

heating when the center of the reactor is above about 800° C. For example, the temperature of the door, which is very susceptible to H_2O adsorption during the load step, rises from 27° C at a reactor temperature of 600° C to 50° C at reactor temperature of 1050° C. Even such a small temperature increase can significantly increase the outgassing rate of H_2O adsorbed on the door (e.g. the rate increases by a factor of 15 if the activation energy is 1 eV).

Examination of the results from an earlier set of four experiments, using a bake temperature of 1085° C, provide further information on the effect of system pressure, and the possibility of a bake-out effect. [Expt.27, Expt.28, Expt.29, Expt.30]. In the first, and fourth experiment, an H_2 flow rate of 2 slpm was used with good results. The SIMS analysis for the interface of the first experiment [Expt.27] is shown in Fig. 3.5(a). The results are similar to the experiment where a 1060° C bake and 8 slpm of H_2 was used as shown in Figs. 3.2(b) and 3.3(b) [Expt.37]. During the bake of the second experiment a throttle valve was used to raise the pressure during the H_2 bake from the normal 1.6 torr (fully open) to 8 torr (almost closed) while keeping the flow rate constant at 2 slpm. The result was a film almost identical to the one shown in Figs. 3.2(a) and 3.3(a), indicating the presence of a large amount of oxide at the interface. If it is assumed that the rates discussed in Chapter 2 that contribute to the background contamination are not affected significantly by the relatively small increase in pressure, the sensitivity of the oxide removal process to the pressure increase makes a kinetic limit, such as the critical pressures measured by Ghidini and Smith, a more likely limitation than thermodynamic calculations. The thermodynamic limit does not depend on the system pressure, contrary to the experimental result.

The possibility that the background pressure of H_2O decreases during the cool-down to the deposition temperature is suggested by the third experiment of the series. In

this experiment the turbo pump normally used for the mass spectrometer was used to evacuate the system during the bake portion of the cycle [Expt.29]. The SIMS analysis of the epitaxial film grown after the low-pressure bake is shown in Fig. 3.5(b). In comparison to Fig. 3.5(a) the oxygen peak is smaller but the carbon peak is larger. The source of the carbon peak is likely to be oil backstreaming from the pump, demonstrating that maintaining a flow of H_2 during a standard bake can serve to both dilute background contamination, and to reduce backstreaming from the pump. For the low pressure bake experiment [Expt.29] the system was transferred to the turbo pump as a part of the ramp up from the loading temperature of 525° C to the bake temperature of 1085° C. The pressure of the system when pumped with the turbo, and no gas flow, reached $2 \cdot 10^{-4}$ torr after 8 min. For the following 48 min of ramp-up and 10 min of baking at 1085° C the pressure reduced to only 10^{-4} torr. As the temperature was ramped down to the 850° C deposition the pressure reduced to $8 \cdot 10^{-7}$ torr after 24 min (916° C). The pressure remained constant at this level until the deposition temperature of 850° C was reached 15 min later. At that point the system was connected back to the regular mechanical pump, and the H_2 gas flow was turned on just prior to starting the deposition step. If it is assumed that the background pressure is mostly due to H_2O these results can be plotted together with the limit measured by Ghidini and Smith as shown in Fig. 3.6. The pressure during the cool down to deposition decreases rapidly enough that it is still below the lower limit at the deposition temperature of 850° C. The possibility that the decrease in pressure is due to a bake-out effect is consistent with the behavior for a typical vacuum system when a bake-out is used as a part of the pump down [3]. The intercept of the $8 \cdot 10^{-7}$ torr pressure with the measured limit of Ghidini and Smith is 819° C, closely matching our observation that epitaxial deposition is possible only above 820° C.

Assuming that the limits measured by Ghidini and Smith are valid for a conventional H_2 bake, the H_2O pressures calculated from direct measurements of the H_2O background can be included in Fig. 3.6. With a mass spectrometer connected to the output of our reactor it was possible to qualitatively measure the composition of the gas exiting the reactor. Quantitative measurements of the H_2O background concentration, however, were not possible without the access to a source supplying a known concentration of H_2O at the same pressure and gas mixture as the unknown reactor output. With a portable calibrated source lent to us by Union Carbide, Linde Division, it was possible to estimate the background concentration of H_2O to be 200 ppm with a 289 sccm flow of N_2 and a pressure of 562 mtorr. Direct measurements using H_2 were not possible for safety reasons, but assuming that the N_2 and H_2 are not significantly contaminated by H_2O themselves, the H_2O pressure can be calculated from the ratios of flows and pressures. The calculated pressures for the bake conditions discussed so far are shown in Fig. 3.6 with dotted lines. In all cases the minimum temperature predicted by the intercept with the lower critical H_2O pressure is much higher than the eventual deposition temperature. Unless a bake-out effect is postulated, the bake cycle would have to move along the horizontal dotted line, requiring that the regrowth of oxide be slow enough that none is formed during the up to 35 min spent in the regions of partial and complete oxide coverage. Furthermore, because the pressure increases from 1.6 torr to 5.4 torr when the flow rate is increased from 2 slpm to 8 slpm (pump limitation), there is a only a slight reduction from 978° C to 970° C in the minimum temperature predicted by the intercept with the critical pressure data. The large improvement observed in Figs. 3.2 and 3.3 for an increased H_2 flow from 2 slpm to 8 slpm does not correlate well with the small change seen in Fig. 3.6.

There are some caveats associated with the previously described mass spectrometer measurements that should be mentioned before continuing. Any one of them can

cause the H_2O pressure calculated from the direct measurement to appear higher than it would actually be during a H_2 bake. The H_2O measurements were done at a constant reactor temperature of 525° C, not after a bake cycle. However, the reactor had not been opened for at least 10 days prior to the measurements. Theoretically this should have been long enough for outgassing to be reduced several orders of magnitude. At room temperature the first order of magnitude of outgassing reduction takes about 10 hrs [3]. In order to connect the calibrated H_2O source, the N_2 supply line just prior to the mass flow controller had to be opened and exposed to air. This could have contributed a source of additional H_2O to the N_2. The laboratory N_2 supply itself is also not completely free of H_2O as assumed in the calculation. Plastic tubing is used to supply the N_2 to the Tylan furnace system, and it is well known that plastic tubing is more porous than stainless steel. Furthermore, plastic connectors are also routinely used in the laboratory on the N_2 supply, any one of these could have a leak, allowing H_2O to enter the N_2 supply. However, in order to reduce the calculated H_2O pressure to the 10^{-6} torr level compatible with 850° C deposition the N_2 supply would have to contribute 190 ppm of the measured 200 ppm. According to the staff of the Microfabrication Laboratory this amount is much larger than can be present according to their experience from other pieces of equipment in the laboratory. In any case, a N_2 purifier would seem to be a worthwhile addition to guard against the chance of contamination entering the reactor because of accidents elsewhere in the laboratory.

The low pressure bake matches the conditions under which Ghidini and Smith measured their critical H_2O pressures more closely than the standard H_2 bake. The effect that the addition of H_2 could have on the critical H_2O pressure cannot be deduced from their measurements or model. As a product in both a reaction that etches silicon and one that oxidizes silicon, increasing the amount of H_2 could conceivably either decrease or

increase the critical H_2O pressure. A well controlled study similar to the one conducted by Ghidini and Smith under the conditions of a typical H_2 bake would be necessary to fully understand the H_2 bake process. As it stands presently, the release of adsorbed H_2O from the loading step seems the most likely cause for the observed temperature limitations. This explanation is consistent with the results of Meyerson et. al. when they operate without using a vacuum load [4].

How the oxide is distributed along the interface will determine its effect on the epitaxial deposition. For example, in Fig. 3.2(a) the silicon surface is textured, but continuous, despite the presence of a large amount of oxide at the interface according to the SIMS profile. Under most conditions in our reactor deposition is completely selective with respect to oxide. Therefore, if there is a continuous silicon film present, as shown in Fig. 3.2(a), it must have nucleated on silicon and grown laterally to cover the oxide present on the starting surface.

Besides predicting that the limit for removing the interfacial oxide is the H_2O pressure, the experiments conducted by Ghidini and Smith also imply that the oxide is removed laterally rather than vertically. Their data suggest strongly that the dominating mechanism for oxide removal is due to reduction along the oxide-silicon interface. The practical implication of this is that the removal proceeds laterally by starting from holes, or weak spots, in the thin surface oxide.

Even bare silicon wafers that have not seen any processing are usually covered with a surface film of about 20 Å according to ellipsometer measurements (assuming an index of refraction of 1.45). This surface film has formed due to air exposure and/or chemical cleaning, and is, therefore, most likely a very imperfect oxide with numerous weak spots. If the lateral removal is incomplete, the resulting surface should contain silicon patches where the oxide was perhaps a little stronger.

A surface of SiO_2 patches partially covering the underlying silicon substrate is revealed by the SEM pictures shown in Fig. 3.7. These surfaces were subjected to a 10 min bake at 1050° C using only 600 sccm of H_2 because of the low capacity of the pump connected to the system at that time [Expt.4]. The wafers were cooled in H_2 after the bake, and unloaded without depositing any silicon. Visual inspection revealed a uniformly hazy surface on the first wafer. On the second wafer the haze was concentrated around the perimeter with the central areas displaying a much less hazy surface, possibly due to a depletion of H_2O by oxidation of the backside of the first wafer 4.8 mm in front of it. The SEM's shown in Fig. 3.7 were taken without gold coating the samples, corresponding to a hazy area in Fig. 3.7(a), and an area with very faint haze in Fig. 3.7(b). Without a gold coating oxide areas appear whitish due to charging in the SEM, allowing us to distinguish SiO_2 from silicon. The hazy area in Fig. 3.7(a) reveals a surface mostly covered by oxide, but with many small holes and some larger openings that both could nucleate silicon growth. A silicon surface after deposition on such a surface can easily be imagined to look like that in Fig. 3.2(a). The faintly hazy surface in Fig. 3.7(b) reveals many small oxide patches that are surprisingly uniform in size and spacing. The spacing and shape maybe due to a similar process as observed by Ghidini and Smith. They observed the formation of oriented oxide islands each surrounded by an area clear of oxide where the silicon area had been etched forming a slight depression around each island. Their hypothesis is that the silicon has been etched by H_2O producing volatile SiO. Such a cleared area is most obvious at the extreme left in Fig. 3.7(b) where a corner of a large oxide feature is showing. No oxide patches are present in a 0.2 μm wide region along the edge of the large oxide feature.

As mentioned earlier, the deposition in our reactor is highly surface-rate controlled, and selective with respect to oxide. An oxide distributed as a number of discrete

patches would force the epitaxial film to nucleate on the bare silicon areas and then laterally overgrow the oxide patches. Depending on the size of an oxide patch the film can completely overgrow it, or be in a stage of incomplete overgrowth when the deposition is stopped. This type of situation is suggested by Fig. 3.8 which shows an originally smooth epitaxial layer containing square base pits, similar to those shown in Fig. 3.2(b), that has been etched with a dilute Schimmel etch [5]. This type of etch is supposed to reveal crystallographic defects such as dislocations by an enchanced etch rate producing round pits where defects are present. The sample shown in Fig. 3.8 [Expt.155] has been etched until only about 3000 Å of the originally 1 μm thick epitaxial film remained. The square base pits remain undistorted, but between them small mounds have appeared (Nomarski reveals polarity). Some of the larger mounds have a depression at the center, like the caldera of a volcano. The dilute Schimmel etch removes SiO_2 almost as fast as silicon (0.2 μm/min versus 0.3 μm/min) so these depressions can be the remains of an oxide patch or a defect in the overgrowth. The possibility that square base pits represent incomplete overgrowth is suggested by Fig. 3.9 which shows a large square pit in a 4 μm thick film [Expt.50]. The bottom of the large pit appears to have overgrown an underlying feature. Notice also that the size of the square base is larger than the ones shown in Fig. 3.2(b), corresponding to the increase in thickness of the epitaxial film from 1 μm to 4 μm.

The orientation of the sides of the square pits is parallel to {110}. This would agree with the formation of a {111} facet as shown in Fig. 3.10. In our test pattern used for selective epitaxy evaluation the {111} oriented facet starts to dominate as lateral growth over oxide squares proceeds unless the sides of the squares are aligned almost exactly parallel to {100}, forcing the {111} facet to occur only in convex corners. The persistence of {111} facets can be explained by <111> being the slowest direction of

growth. A more surprising result than the appearance of the {111} facet is the uniform size of the square pits when they occur, and that their size corresponds to the thickness of the film. This would be the case if all of the oxide patches were of exactly the same size, but, as shown in Fig. 3.8, oxide patches can be found that were smoothly overgrown among the square base pits. Another possibility is that all of the oxide patches are small enough to be overgrown fully but that a few of them nucleate a stacking fault bounded by {111} planes. These could slowly fill in, forming the flat bottom seen in the thick layer in Fig. 3.9, but would all remain the same size and depth irrespective of the relative growth rate between the <100> and <111> directions. A variation on this hypothesis is that after the growth fronts meet on top of an oxide patch, a fast growing {100} plane forms at the bottom of the pit. The bottom of the pit could grow faster than the top surface because of additional adsorbed molecules diffusing to it from the {111} facets, and in this way also slow the growth of the {111} facet. In this case the size at the surface would be the same even if the overgrown oxide patches are of different sizes, but some pits would have their bottoms at different levels depending on the size of the original oxide patch. The result of this hypothesis is shown in Fig. 3.10 where for the smallest oxide patch the bottom of that pit has grown up to be level with the top surface. A final possibility is that the pits are not as distinct as they appear in a Nomarski microscope, but instead only a slight depression, perhaps as before revealing an underlying stacking fault, or an uneveness in the starting surface caused by the oxide removal similar to the undercut observed along oxide pattern sidewalls. The Nomarski technique makes visible variations in height as small as 200 Å. The SEM in Fig. 3.11 of an epitaxial film shows 2 distinct pits in the foreground. The pits look rather smooth as viewed in the SEM, and are difficult to find unless the sample is viewed at a shallow angle as in Fig. 3.11. In a Nomarski microscope the same pits look much more delineated as in Fig. 3.2(b).

Figure 3.11 also shows a facet overgrowing the sloping oxide profile (HF etched) that is very uneven. Because a <111> facet corresponds to the slowest growing plane ideal circumstances should lead to a smooth <111> facet forming along the <110> oriented oxide sidewalls as in Fig. 3.11. The uneveness of the epitaxial surface along the edge is perhaps due to the undercut of the oxide caused by the high temperature H_2 bake used on this sample (1085° C), but it also suggests that the <111> oriented facet maybe is not as stable a structure as commonly assumed. For example, it would be very useful for certain selective epitaxy applications if a particular oxide profile could be used to minimize the formation of {111} facet planes.

Pyramidal pit formation appears to be related to the surface-rate-controlled conditions in our reactor at 850° C. In epitaxial layers grown under the more conventional mass flow limitations in cold-wall reactors pyramidal pits are discussed and described only in conjunction with crystallographic defect etches (e.g. the Wright-Jenkins etch). Pyramidal pits are particularly interesting because the same crystallographically orientation dependent growth processes that govern the pit morphology control selective epitaxy and subsequent oxide overgrowth. A strongly surface limited growth is a good vehicle for studying the fundamental sensitivity to the oxide profile, oxide orientation, substrate condition, etc. Experiments closely examining selective epitaxy overgrowth for differently shaped and oriented patterns of oxide on various substrate orientations would both improve the understanding of selective epitaxy, and surface defect formation.

3.2 Background Impurities and Outdiffusion

This section examines the incorporation of impurities from the reactor background, and from the substrate itself (autodoping). The goal is to differentiate between

fundamental limitations associated with the hot-wall approach, and effects that are specific to our system. As a point of reference for evaluating the films grown in our reactor, epitaxial films were grown on identical substrates in a commercially available AMC 7810 cold-wall reactor modified slightly to operate at lower than standard pressures for better selective results.† The reactor is a radiantly heated cold-wall system using a single pass laminar injector system (turbulent is standard). A schematic for this type of reactor is shown in Fig. 3.12. The wafers are placed in circular depressions on a rotating susceptor (barrel) which is heated by infra-red radiation from lamps placed outside of the quartz bell jar. Gas is injected at the top of the reactor vessel, and exhausted at the bottom by a vacuum pump. Hydrogen is injected both through two injectors outside the barrel (H_2 main), and one injector leading to the inside of the rotating barrel (H_2 rotation), but SiH_2Cl_2 added only to the H_2 of the main injectors. There are a few holes along the corners of the barrel that allow H_2 from the rotation injector to flow out of the barrel, but the major portion probably exits through much larger holes in the bottom. Because of this very complex configuration it is difficult to model and analyze the growth conditions inside the reactor. For this discussion it will be assumed that the wafers are exposed only to the main injector flow, and the rotation injector only contributes to the total pressure.††

The deposition cycle used in the cold-wall reactor, and the SIMS analysis of the resulting epitaxial film, are shown in Table 3.1 and Fig. 3.13, respectively. The type of substrate used for the deposition is the same as used for Figs. 3.3, 3.4, and 3.5. These substrates are wafers donated to us by Dr. John Rossi at Monsanto, and are identical to those that are used in their production of epitaxial substrate wafers. The wafers are Czo-

† John Borland at Applied Materials provided the reactor.

†† John Borland feels that this is the case for the laminar flow injector in the AMI 7810. This assumption also makes the growth rate in the AMI 7810 consistent with the rate model in Chapter 5.

chralski grown with 20-30 ppm oxygen, heavily antimony doped, and backside gettered with polysilicon. We use these wafers directly out of the box without further cleaning since the cleaning performed at Monsanto is superior to what we can accomplish. These wafers serve the dual purpose of allowing us to evaluate our epitaxial results on a consistent substrate, and to locate the substrate interface because of the low diffusion rate of antimony.

Comparing the deposition cycle shown in Table 3.1 to the one of our system shown in Chapter 2, there are several differences that will become important when comparing the two systems. First of all, temperature ramping is much faster in the cold-wall system. In the hot-wall system the temperature can be increased at a maximum rate of 12° C/min, and decreased at a maximum rate of 4° C/min, compared to over 50° C/min in either direction for the cold-wall system. The slow transitions between temperatures add significantly to the time the wafers spend at a given temperature, increasing dopant redistribution. Secondly, gas flow rates and system pressure during deposition are both much higher in the cold-wall system which affects the amount of background impurities.

The choice of flow rates and system pressure are dictated by the design limitations of each system. In the cold-wall reactor high growth rates are necessary to compensate for the low packing density resulting from placing the wafers in contact with a susceptor. In the hot-wall reactor growth rates must be low enough that the diffusion rate that supplies the centers of the densely stacked wafers does not limit the growth rate. The net effect is that for a 1 μm thick epitaxial film the total cycle time is 45 minutes in the cold-wall reactor, versus 300 minutes in the hot-wall reactor. On the other hand, the hot-wall reactor can hold more wafers per cycle. For example, up to 100 wafers of 100 mm, or 125 mm, diameter can be accommodated in the current configuration of our hot-wall reactor, versus 24, or 12, for the same size wafers in the AMI cold-wall reactor.

The flow and pressure are factors that also affect the incorporation of contamination in the epitaxial films. Comparing the carbon level inside the epitaxial film grown in the AMI reactor, as shown in Fig. 3.13, and the carbon levels seen for films grown in our reactor, as shown in Figs. 3.3, 3.4, and 3.5, it is found that the film grown in the AMI reactor contains about $8 \cdot 10^{16}$ cm^{-3} (1.6 ppm) versus $3 \cdot 10^{17}$ - $6 \cdot 10^{17}$ cm^{-3} (6 - 12 ppm). For both reactors the carbon content is above the substrate level, and the SIMS background measurement limit. Carbon occupies substitutional sites, and for concentrations as high as $5 \cdot 10^{17}$ cm^{-3} it does not precipitate, nor is it electrically active [6]. However, carbon can aid in the formation of defects, and it has been linked to the precipitation kinetics of oxygen. Minimizing the carbon content requires knowledge of the sources of carbon and its incorporation mechanism. Without knowledge of the later the amount of carbon in the gas phase that corresponds to a given level as measured by SIMS cannot be inferred. Direct mass-spectrometer measurements of the carbon background inside our reactor were not very effective for the want of a calibration source, and the poor reliability of the turbo pump used for the analyzer. The presence of pump oil could be detected, but the source could not be identified from the cracking pattern. The amount of oil detected increased after each of the frequent shutdowns of the turbo pump. We will, therefore, assume that the incorporation of carbon is identical to silicon (i.e. 1 ppm of carbon in SiH_2Cl_2 in the gas phase corresponds to 1 ppm in the epitaxial film), which leads to two equally possible explanations for the carbon background level in the two reactors. One is that the carbon is injected from the SiH_2Cl_2 source itself, which is specified by Matheson Gas Products to contain less than 10 ppm carbon for the ULSI grade that is used in our reactor. The other is that there are sources inside both systems that add carbon contamination to the total flow at similar rates (e.g. a surface contaminated with pump oil). For internal sources the different operating conditions of the two reactors result in a ratio of partial pressures close

to the ratio calculated from the carbon content measured by SIMS (29 vs. 14-26). The two possibilities can be distinguished with experiments where the total flow rate is varied while the pressure is kept constant. A larger capacity pumping system than currently connected to the reactor will be necessary to vary the residence time over a significant enough range for this experiment.

More recent data indicate that the carbon levels in our reactor have decreased somewhat compared to the earlier data shown in Figs. 3.3 through 3.5. This decrease is perhaps due to the present use of a Unit mass flow controller with a higher flow rate sensor compared to the previous Tylan controller, and an Ultraline gas bottle which is lined with an inert material preventing exposure of the metal wall directly to the corrosive SiH_2Cl_2, as was the case in previous gas bottles. Shown in Fig. 3.14 is a SIMS analysis of the dummy wafer D2-8 that was the furthest downstream wafer in Expt.156-Expt.167. It was inside the reactor for 25 days, and present during 12 experiments, and one coating run, resulting in a total deposit of about 6 μm of silicon. The carbon level fluctuates between $1 \cdot 10^{17}$ cm^{-3} to $2 \cdot 10^{17}$ cm^{-3} during deposition. The oxygen measurement for this particular analysis session was unfortunately limited by the SIMS background of about $5 \cdot 10^{17}$ cm^{-3}.

The data shown in Fig. 3.14 also contain an intriguing series of peaks. Since the dummy wafers are not removed between experiments, the peaks suggests that carbon is accumulated either inside the reactor between experiments, while the reactor is open, during the steps leading up to deposition, or from carbon transported into the reactor on the surfaces of loaded experimental wafers. Matching the observed peaks to the experiments as shown in Table 3.2, it is found that peak A corresponds to the break of 158-159, B to 159-160, C to 161-162, and the two peaks at D to 164-165 and 165-166. The same basic recipe was used for all of these runs (EPI.18T), and experiments were performed by

adjusting the variables indicated in Table 3.2. There is no clear pattern to the operation of the reactor except that there are no peaks observed after 1000° C bakes except for the coating run performed after the reactor had been broken down for 12 days with temperature control problems. Experiments 158 through 162 using 900° C bakes were run mostly in order to make the HF vapor treatment described in Chapter 4 more reliable by using SiH_2Cl_2 during the ramp down to deposition temperature. The liability of using SiH_2Cl_2 before the surface is completely cleared of residual oxide by the H_2 bake is that the oxide gets buried and cannot be removed. The experimental wafers in this set of runs are as a result not good indicators of epitaxial quality, but it is expected that an accumulation of carbon at the epitaxial interface can only be detrimental, and should be avoided. Carbon could be injected into the reactor via bursts in the nitrogen during idle, or from the SiH_2Cl_2 during the low flow ramp down, but it seems more likely that the carbon could have been introduced into the reactor as a result of uncontrolled factors associated with the loading step. Carbon contamination can also occur because of oil backstreaming just as the gate valve opens, and during the 30 sec leak check step that precedes the start of the bake ramp. This type of contamination would affect both run and dummy wafers, but no SIMS data were taken from the run wafers for Expt.158 through Expt.166 so this hypothesis remains to be tested. A mechanical pump should ideally be base-pressure-limited to a minimum of 130 mtorr to eliminate backstreaming oil [3] but due to the already limited pump capacity the base pressure can only be limited to 70 mtorr. A larger capacity pumping system and/or the use of a blower will be necessary to reduce possible oil backstreaming further.

Examining closely the differences between experiments 158 through 161 leads to the possibility that moisture on the loaded wafers can transport volatile carbon into the reactor. In Chapter 4 the generation of surface moisture is correlated to the amount of

exposure to HF vapor, and for exposures above about 5 seconds there is visible formation of water on the surface. We do not presently have any means of controlling the accumulation of water except by keeping the exposure to HF vapor as short as possible. It is also expected that the amount of water accumulated on the HF etched surface also depends on the humidity inside the lab which varies between 40 to 60 percent according to the laboratory hygrograph. During the cleaning of the wafer used in Expt.159, peak A, one of the experimental wafers picked up 2 water droplets from the rim of the beaker used to perform the vapor etch. Since the reactor was ready to load, the wafer was dried hurriedly in the spin dryer. This was just before it was discovered that the spin dryer was not cleaned regularly, contributing enough contamination to selective epitaxy wafers to be a cause for unwanted oxide nucleation. Experiment 160, peak B, included experimental wafers with varying times of exposure to HF vapor, and some were exposed long enough to accumulate a visible mist of water. Experiments 158 and 161 used wafers with only 5 second exposures. Surprisingly, poor deionized water quality because of water supply malfunction during the preparation of wafers for Expt.161 did not cause a problem.

The last set of peaks at D are from Expt.165 through Expt.167, during which raised source/drain structures were grown on wafers made and cleaned by Jim Moon. These wafers had been exposed to many more process steps than our standard test wafers, and, therefore, can have contributed to to the carbon contamination Furthermore, since Jim Moon had a large investment of effort in these wafers, he cleaned and loaded his own wafers which may have contributed to the observed results due perhaps to a subtle difference in technique of the vapor etch leading to more water on the surface, or the longer reactor load time resulting from doing it for the first time.

Water evaporating from the wafer surfaces during the loading step that has been contaminated with carbon-containing compounds can release both oxidizing and carbon

species that deposit on the dummy wafers. The correlation between oxide peaks and carbon peaks in Fig. 3.14 can, therefore, be consistent with both the water source hypothesis, or a hypothesis that carbon and oxygen accumulate on the dummies as a part of the load cycle. The results from the SIMS analysis of the dummy wafer D2-8 are far from conclusive, but show that analysis of dummy wafers can be an important source of information to solve problems with the preparation of epitaxial substrate wafers, and the operation of the reactor. Further experiments are needed to investigate methods to obtain more consistent results between runs. The addition of a nitrogen purged loading station, and perhaps an improved HF vapor process that minimizes water droplet formation†, are both worthwhile experiments.

Controlling the incorporation of background impurities is primarily a practical problem of good vacuum system design not directly related to the type of reactor, but the slow temperature response of a hot-wall reactor compared to a cold-wall system presents a fundamental limitation. The long temperature cycles in a hot-wall system will make a significant impact on the distribution of impurities. This is compounded by the reduced growth rates necessary in the hot-wall system to reduce source gas depletion. The goal of the remainder of the section will be to examine the impact on autodoping by hot-wall versus cold-wall.

The SIMS analyses shown in Fig. 3.15 contrasts two wafers, one with an epitaxial film grown in the previously described AMC 7810 cold-wall reactor using a 950° C bake, and one with an epitaxial film grown in our reactor using a 1060° C bake. The starting substrate in each case is a Monsanto standard wafer taken directly from the shipping box, and onto which an approximately 1 μm thick epitaxial film was grown at

† For example, commercially available systems from FSI International and Advantage Production Technology perform HF vapor etching with close control of the moisture content.

similar temperatures close to 850° C. The hot-wall wafer [M2-9, Expt.39] reveals a much larger amount of oxygen outdiffusion as a result of the H_2 bake (T>1050° C for 20 min) in comparison to the cold-wall wafer (T=950° C for 7 min). The region denuded of oxygen for the AMI wafer is only about 1 μm versus 5 μm for the hot-wall wafer. Another interesting result is that the oxygen profile is continuous through the epitaxial to substrate transition which is consistent with the high diffusivity of oxygen in silicon. Using published diffusion constants, the calculated $\sqrt{Dt}$ for oxygen after a 100 minute 850° C deposition is 60 times larger than the $\sqrt{Dt}$ for boron, and 350 times larger than the $\sqrt{Dt}$ for antimony [6]. The presence of this oxygen inside the epitaxial silicon can contribute to the formation of thermal donors. These donors are poorly understood, but it has been found that they form most rapidly in the temperature range of 400°-500° C, dissolve in the range 600°-700° C, and can form at a lower rate in the range of 700°-900° C [6, 7]. The rate of formation of thermal donors at 700° C is in the range of 10^{14} /cm^3-hr.

The formation of thermal donors can explain the n-type background doping observed for our undoped epitaxial films when analyzed with the spreading resistance profiling (SRP) technique. In Fig. 3.16 an SRP profile is contrasted with a SIMS measurement of the antimony profile for a 1 μm thick epitaxial film grown in our hot-wall reactor at 850° C. The SRP profile shows that the background doping of the epitaxial film is n-type with a slowly decreasing donor concentration, reaching $5\cdot10^{14}$ cm^{-3} at the surface. For a 4 μm thick film shown in Fig. 3.17 [M3-8, Expt.50] the tail becomes exponentially decreasing, reaching $7\cdot10^{12}$ cm^{-3} at the surface. Note that the value at 3 μm (1μm of epi) for the thicker film is almost identical to the value at the surface for the 1 μm film. According to the theory of thermal donor formation, the concentration of donors is exponentially dependent on time [7] which predicts that the thermal donor concentration should fall of exponentially versus thickness since the thickness increases linearly with

time. With SIMS it was not possible to identify any dopant species that could directly explain the SRP data, suggesting thermal donors. However, the exponentially decreasing tail of the SRP measurements could also be an artifact from attempting to measure a very lightly doped film, on top of a heavily doped substrate. Carriers from the heavily doped layer can affect the conductivity measured in the lightly doped layer at least for a distance up to 1 μm [8]. Dave Dickey of Solecon Labs where the SRP analysis was performed warned that his measurements are not calibrated below 10^{14} cm^{-3}, and that he typically sees this sloping concentration profile in undoped epitaxial films, but had no explanation for it. An interesting experiment to distinguish between measurement artifact and possible thermal donors would be to compare SRP measurements of samples taken from a wafer like the one shown in Fig. 3.17 that have been put through various anneal cycles designed to minimize, or maximize, thermal donors, and then measure them with SRP. Without further investigation the actual background doping in our epitaxial film can only be identified as n-type, with a concentration that is possibly as low as 10^{13} cm^{-3}. This agrees well with the Matheson Gas Products specified minimum resistivity for SiH_2Cl_2 of 275 ohm-cm n-type ($2 \cdot 10^{13} cm^{-3}$).

Besides effects due to the presence of oxygen, a critical parameter for the construction of compact devices that use epitaxial layers is the abruptness of the dopant profiles. In particular, chemical or diffusive transport of dopants from the substrate is of great concern. Both the bake cycle, and deposition cycle, are important in determining the final dopant profile. A transition width is often used in order to characterize the abruptness of the profile with a single number. The definition of this transition width is somewhat arbitrary and depends on the application. A commonly used definition is to measure the distance it takes the concentration profile to decrease 2 orders of magnitude from some level based on the maximum concentration, which in this work will be chosen to be 75%

of the maximum. Defined in this way the transition width will combine effects due both to outgassing of dopant during the bake step, and diffusion into the growing epitaxial film during the deposition step.

Antimony profiles measured with SIMS are shown in Fig. 3.18 together with profiles simulated by using SUPREM-3 (ver. 1B, rev. 8520).† The SIMS profile in Fig. 3.18(a) is the same one as in Fig. 3.13, grown in a cold-wall reactor with the cycle shown in Table 3.1. The SIMS profile in Fig. 3.18(b) is the same one as in Fig. 3.16, obtained from an epitaxial layer deposited at 850° C after a high temperature bake at 1085° C [Expt.27]. The concentration levels that are used to measure the transition width are shown with dashed lines. Because of the higher growth rate in the cold-wall reactor at the same temperature as the hot-wall reactor, it is not surprising to find that the transition width measured by SIMS is 450 Å for the cold-wall reactor, and 700 Å for the hot-wall reactor. To get good agreement between simulation with SUPREM and the measured curves it was important to include as a part of the simulation an accurate representation of both the deposition step and the preceding bake step. The SUPREM simulation for the hot-wall with the bake step included predicts a profile with a transition width of 650 Å that closely resembles the the profile measured with SIMS. Simulation of the cold-wall case, however, predicts a profile with a transition width of 110 Å that matches the slope of the SIMS profile well, but with a much sharper transition at the top of the profile. This disagreement can be caused either by limitations in the SIMS measurement, and/or the SUPREM model not accurately predicting the outgassing behavior of antimony.

According to Charles Evans & Associates, where the SIMS analysis was performed, an atomically abrupt transition would be measured by their SIMS machines as

† Simulation was provided Dr. Ginetto Addiego of Lawrence Livermore Labs.

having a transition width of 100-200 Å. That assumes that the machine is working perfectly, and has been set up to maximize the depth resolution at the expense of other parameters such as sensitivity, which is usually not the case. As an example of the repeatability of the SIMS technique in this regard, the same cold-wall sample measured on a different machine by a different operator was measured to have a transition width of 950 Å, more than two times larger than the one shown in Fig. 3.18(a). In contrast, the repeatability of the antimony concentration inside the substrate was within 20%. This difference in repeatability reflects that calibration of the concentration level can be performed objectively with a standard, whereas the depth resolution depends on how the operator has chosen to balance the limitations of the machine in order to achieve a suitable measurement.

Simulation with SUPREM is also limited in its ability to accurately predict the profile. For example, it was found that outgassing of dopant during the bake must be included in order to obtain profiles that agree well with the measured profiles. The rate at which dopants leave the surface is expected to be to some extent dependent on the pressure and composition of the surrounding gas. However, the profiles predicted by SUPREM were not dependent on the specified pressure, nor was there any option to use anything but nitrogen as the non-oxidizing gaseous ambient. Similar problems exist with the deposition step, which for SiH_2Cl_2 can only be modeled by a deposition rate and time, not a more detailed model involving the pressure and gas composition. Despite these reservations, SUPREM simulations do allow us to quickly evaluate different conditions with reasonable accuracy considering the approximate nature of the models. For example, epitaxial films of identical thicknesses must be used for the two types of reactors in order to isolate the effects that the low growth rate and slow temperature response of a hot-wall reactor will have on the abruptness of the dopant profile.

The effect of reactor configuration on antimony autodoping is shown in Fig. 3.19 for a fixed epitaxial thickness of 1 μm. A cold-wall type system is simulated in Fig. 3.19(a) by using short bake times of 5 minutes, and a high growth rate of 0.1 μm/min for 10 minutes at 850° C. Profiles for no bake, 900° C bake, and 1000° C bake are shown so that the effect of the bake is made obvious (cannot be done experimentally). We find that the transition widths for each of these cases is 120 Å, 90 Å, and 120 Å, respectively. A hot-wall type system is simulated in Fig. 3.19(b) by using a longer duration bake of 50 min, corresponding to the slower temperature response, and a low growth rate of 100 Å/min for 100 minutes at 850° C. The transition widths for no bake, 900° C bake, and 1000° C bake are 200 Å, 180 Å, and 430 Å, respectively. The no-bake case allows us to compare the amount of redistribution directly attributable to the reduced deposition rate. The profile for the hot-wall system is about a factor of 2 less steep with a concomitant increase in transition width from 120 Å to 200 Å. The reduced slope causes the antimony autodoping to extend about twice as far into the epitaxial film for the hot-wall case. When the bake is included in the simulation the situation becomes more complicated with the antimony autodoping profile shifting towards the substrate because of the dopant outgassing from the surface during the bake. The effect of the bake is demonstrated more clearly by Fig. 3.20, where the profile for the hot-wall case is shown before and after deposition for both the no-bake and the 1000° C bake conditions. The effect of the bake is to deplete the top surface of the substrate by outgassing of antimony. The model in SUPREM-3 predicts that there is a sharp dip at the surface because of the low diffusion rate relative to the outgassing rate. In fact, for antimony the surface is so depleted by outgassing that the concentration at the interface actually increases during the deposition. The antimony slope inside the epitaxial layer is determined by the the magnitude of the diffusion constant relative to the growth rate, and is not changed by the bake. The net

effect of the bake is, therefore, a shift of the concentration profile towards the substrate.

Whereas antimony is the slowest diffusing dopant commonly used for silicon, boron is the fastest. The $\sqrt{Dt}$ of boron at 850° C is about one order of magnitude larger than for antimony. Since boron is the only commonly available p-type dopant the constraints imposed by boron diffusion are important. The boron doping profile resulting from depositing a 0.9 μm thick undoped epitaxial silicon film at 850°C after a 1000° C bake is shown in Fig. 3.21. The 2 order transition width is about 0.26 μm for the SIMS profile, and is 0.21 μm when simulated with SUPREM-3. In order to obtain a good fit with a SUPREM simulation for boron it is even more important than for antimony to use a realistic temperature cycle. SUPREM provides only linear temperature ramps but the real temperature ramps are far from linear when close to the set points. Increasing the number of temperature segments that simulate the bake cycle from 3 to 5 improved the fit considerably, increasing the calculated transition width from 0.19 μm to 0.21 μm.

Hot-wall system impact is again assessed by simulating the dopant profile for a fixed epitaxial thickness of 1 μm with the same parameters that were used previously for antimony. The resulting profiles are shown in Fig. 3.22(a) for a simulated cold-wall where for no bake, a 900° C bake, and a 1000° C bake the transition widths are 270 Å, 350 Å, and 350 Å, respectively. The same conditions simulated for a hot-wall system are shown in Fig. 3.22(b), and the transition widths are 710 Å, 800 Å, and 1360 Å, respectively. As expected in comparison to antimony, the boron profiles are less steep, and there is a larger change when the growth rate is decreased. Less expected perhaps is the lower amount of boron depletion at the surface compared to antimony, resulting in less shift of the dopant profile towards the substrate. This effect is shown more clearly in Fig. 3.23 were the boron profile is plotted before and after epitaxial deposition using either no bake or a 1000° C bake. In contrast to antimony the boron diffuses quickly enough so

that the surface is not strongly depleted during the bake, and the concentration at the interface is higher at the surface after the bake than after the deposition. Consequently, the shift of the profile towards the substrate is reduced. On the other hand, the higher diffusion rate causes the depletion of boron to extend further into the substrate because of the higher diffusion rate, and the transition widths, therefore, increase quickly.

From the simulations of dopant redistribution it can be concluded that a hot-wall system will not provide profiles as abrupt as cold-wall systems because of the slower temperature response, and the lower growth rate. Whether the less abrupt profiles are significant or not depends on the specific application, but for critical applications it is obviously important to do an accurate simulation, including accurate temperature cycles for both baking and deposition. It should also be noted that the transition width by itself is not sufficient to fully characterize a dopant profile, since the profile position is sensitive to changes in the deposition cycle. The sensitivity of the dopant distribution to the bake cycle is a strong incentive to reduce the bake temperature and time as much as possible. If in the future, the hot-wall reactor is improved allowing a constant temperature to be used instead of the high-low cycle, improvements in both throughput and dopant redistribution would ensue.

3.3 Selective Epitaxy

Selective deposition has been investigated since the beginnings of epitaxial silicon growth [9], and it adds considerable complexity to an already difficult task. However, the continuing interest in increasingly dense integrated circuits, and improvements in process control, have more recently contributed to making the use of selective epitaxy a promising alternative for future integrated circuit fabrication [10]. The topic is relevant to this thesis

because hot-wall type reactors operating at low growth rates in the surface-rate-limited regime have the potential of providing epitaxial silicon that is both deposited selectively, and at low cost. Suitable applications are, for example, elevated source drains, and first level contact filling, both requiring thin layers of epitaxy with an emphasis on low cost.

Fundamentally, an atom or molecule approaching a surface of a solid always experiences a net attractive potential [11]. There is, thus, a finite probability that it will be trapped and adsorbed on the surface long enough for further reaction to take place. This probability will vary, depending on the environmental conditions (pressure, temperature, gas composition, etc.), and the nature of the surface. The sensitivity to the nature of the surface is exploited by the selective silicon deposition technique as illustrated schematically by Fig. 3.24. The reactor conditions are adjusted so that epitaxial silicon is deposited only where a masking SiO_2 layer has been etched away to expose the underlying silicon surface. Molecules landing on the masking oxide will not form a silicon nucleate on the oxide unless there is some contamination or defect present that can make the adsorption of silicon more favorable as shown on the left in Fig. 3.24. If the contamination on the surface allows the nucleus to reach a critical size, determined by its surface energy, it is stable and will continue to grow. An example of oxide nucleation is shown in the SEM picture of Fig. 3.25 from a wafer subjected to a 1085° C H_2 bake before a standard epitaxial deposition at 850° C [CG4-5, Expt.31]. There is a very sharp delineation of the area where the oxide nucleation occurred which corresponds well to the hypothesis of a local adsorption enhancement such as contamination.

The reactor conditions that are most likely to result in selective growth are those for which the net accumulation of silicon on the oxide is low. Low net rates can be achieved either by increasing the removal rate, by decreasing the impingment rate, decreasing the affinity of the gaseous species for the oxide (shorter residence time), or by

using a gaseous species with low oxide affinity. Quantifying such basic kinetic dependencies is often difficult because of mass transport effects, uncertainty of the reaction mechanism, and limitations in analytical techniques. Published selective epitaxy data measured in large multiple-wafer reactors are, therefore, not often related to the basic kinetic phenomena, making the results specific to the conditions, and the reactor that was used. Despite the maturity of epitaxial technology there is further need for basic studies in small experimental reactors where all relevant parameters can be controlled and measured.

The common method of achieving selective epitaxial silicon deposition by adding HCl to the gas mixture is an example of a process that is useful, but not well understood in detail. An increased removal rate is probably the predominant kinetic effect, but the actual deposition mechanism is not well known in the Si-Cl-H system because of the large number of different gaseous species that are present [12, 13, 14]. Drowley and Hammond have summarized the addition of HCl to a mixture of SiH_2Cl_2 and H_2 in a commercial Gemini reactor, and found that nucleation on the oxide decreases with higher Cl/Si ratios, lower pressures, and lower concentrations of the silicon source gas [15]. They also found that for a fixed Cl/Si ratio, selectivity is enhanced at lower pressures and lower temperatures. The authors found optimum amounts of HCl for their range of temperatures (950°-1000° C), pressures (50-300 torr), and composition (~0.3% SiH_2Cl_2). Unless an optimum amount of HCl is used, the silicon growth will not be flat, but instead enhanced (too little HCl), or retarded (too much HCl), along the oxide edges. The conditions for which the silicon profile is flat result in a silicon growth rate in oxide windows that is independent of the amount of surrounding oxide. The optimum amount of HCl not only depends on the deposition conditions, but also, as the authors point out, on the type of reactor. Without more understanding of the basic kinetics and reactor behavior, it is impossible to

predict the selectivity using HCl without doing the actual experiment. For example, in the case of Drowley and Hammond, kinetic understanding could help explain if there is a fundamental reason for all of the optimum conditions resulting in similar silicon growth rates (~0.14 μm/min). If there is such a reason then it would provide a more general result that could be used in a model to predict the onset of selectivity.

The drawback to using HCl is that it is an independent reverse reaction that is used to balance the forward deposition reaction. Using a source gas that by itself facilitates selective deposition may be preferable from a control standpoint, particularly when dealing with strong depletion effects. The onset of selectivity depends on the source gas, and the balance between the kinetic effects. For example, SiH_4 in an H_2 ambient generally results in non-selective growth, and is widely used for polysilicon deposition on oxide. However, Mercier et. al. have recently shown that, without the addition of HCl, a mixture of 0.4% SiH_4 in H_2 at 5 torr resulted in selective deposition at 1000° C in a rapid thermal processing system [16]. From a kinetic point of view this result can be due to the shorter residence times of adsorbed molecules on the oxide because of the high temperature, or the formation of gaseous species with less affinity for oxide.

From a practical perspective, improvement in selectivity with an increase in temperature is not often desirable because of mass transport limitations (higher growth rates on silicon areas), or the increase in thermal cycle for the processed wafers. Lower growth rates and lower selective temperatures are possible using chlorosilanes. The mixtures of 7% SiH_2Cl_2 in H_2 at 0.6 torr used in our reactor exhibit selective deposition (except for cases of contamination) over the temperature range of 800°-950° C without the addition of any HCl. It is not clear whether the selectivity is due to the formation of HCl, or because the dominant gaseous species $SiCl_2$ [12, 13, 14] has a low affinity for the oxide.

As shown in Figs. 3.24 and 3.25, contamination on the oxide can result in silicon nuclei forming. The exposure to H_2 at high temperatures can reduce the contamination on the wafer surfaces, but, as discussed in Chapter 4, for selective epitaxial growth applications it is necessary to operate at the lowest possible temperatures to reduce oxide undercut and dopant diffusion. In our system, an increase in oxide nucleation is observed due to oxide contamination when temperatures lower than 1000° C are used during the H_2 bake. Oxide nucleation that result after a standard lab clean and a 950° C H_2 bake can be seen as white dots in the micrograph of Fig. 3.26(a) [Expt.54]. The oxide nucleation forms distinct circular patterns that suggest that the contamination was deposited on the surface by water droplets. Observation under a collimated light source clearly reveals radial streaks of oxide nucleation. Preferential oxide nucleation is also often observed along the edges of oxide patterns. These observations have led us to suspect the contamination source to be the wet clean and spin dry that are performed just prior to the loading of the wafers into the reactor.

We have been able to drastically reduce the amount of oxide nucleation by modifying the sequence of the standard lab clean shown in the left column of Table 3.3 to the one in the right column. The micrographs in Fig. 3.26 show two wafers that were treated exactly the same, including being in the same reactor run using a 950° C H_2 bake [Expt.54], except that the wafer in Fig. 3.26(a) [CG5-14] was put through the standard lab clean, and the wafer in Fig. 3.26(b) [CG5-15] was put through the improved clean. The amount of improvement is actually larger than the micrographs indicate because they were both taken in areas with a high density of oxide nucleation. Areas with a high density of oxide nucleation were much less common on the wafer that received the improved clean. The distribution on the wafer with the improved clean was also not distinctly distributed as droplets or radial streaks.

The residual amount of oxide nucleation seen in Fig. 3.26(b) can almost be totally eliminated even for wafers subjected to only a 900° C H_2 bake if the spin dryer is cleaned at least once a week. The dryer consists of a rotating stainless steel fixture enclosed in a chamber that is purged with heated N_2 while the fixture is spinning. To dry a batch of wafers the cassette used to hold the wafers during the wet clean is transferred from the last rinse tank directly to the stainless steel fixture, the door is closed, and the automatic drying cycle is started. The method to clean the spin dryer that has been found to work well consists of a careful wipe down of all internal surfaces of the spin dryer with methanol, followed by a thorough rinse using deionized water from the deck hose connected to sink 6. When the rotating stainless steel fixture is clean the water should bead on it.

There are several possible contamination sources associated with the wet cleaning step, including the water, the wafer holder, the chemicals, the air, the spin dryer, and contamination due to previous users of the wet sink. The difference between the two cleaning cycles is the addition of a second Piranha clean (1 gallon 120° C H_2SO_4 and 100 ml H_2O_2) after the HF dip that clears the oxide on the silicon areas. An additional short rinse after the HF dip ensures that the field oxide is not etched by residual HF during the second Piranha clean. We think the improved cleaning cycle works because the second Piranha removes contamination introduced by the HF dip, and also by passivating the otherwise reactive silicon areas with a thin chemical oxide. The resistivity of the deionized water as it enters the wet sink usually reads close to the maximum 18.2 Mohm-cm but can contribute non-ionic contamination such as silicon from dissolved silica which is not blocked by the reverse osmosis membranes, and carbon from chemicals leached from the plastic tubing and/or from bacteria growing inside the deionized water system (sterilized twice a year). Non-ionic contamination may attach to the wafer surface rather than

dissolve in the water, and be left behind after drying. The wafer holders (cassettes) are made of teflon which is a porous material, and they have a tendency to degrade with time. As the holders age the time it takes to get the resistivity close to the empty tank reading during the final rinse starts to increase. The characteristic behavior of this problem is that resistivity first increases rapidly and then decreases to a lower value before increasing slowly again, suggesting that some contamination is leaching out of the teflon. The resistivity measurement responds to ions such as those in Piranha and/or other contamination perhaps picked up from the common practice of transporting cleaned wafers to the furnaces by carrying them in the cleaning cassettes (for epi wafers a dedicated clean box is used as a transport vehicle). The cleaning of the spin dryer helps by reducing the amount of contamination resulting from water hitting its internal surfaces and splashing back on the wafers. It should be noted that the spin dryer was intended to also rinse the wafers, but in the lab it is only operated in the drying mode, perhaps allowing contamination to accumulate. The wet sink (sink 6) is used for both the pre-epitaxial clean, and all other pre-furnace cleans. It is, therefore, one of the more heavily used sinks in the lab, and, therefore, subject to much potential contamination. Problems are the common use of metal tweezers in the lab, and the large amount of handling wafer cassettes are subjected to. Sink 9 is dedicated for the cleaning of wafers for especially sensitive experiments, but has no spin dryer, or other method to quickly dry a batch of wafers. Attempts using a portable single-wafer spinner and sink 9 have only given much worse results than using the more heavily used sink 6 and its associated spin dryer.

The recently published work by Mishima et. al. [17] demonstrates that standard wet cleaning combined with a spin dry is not a very effective way to remove contamination present on wafer surfaces. Wafers intentionally contaminated with simulated organic particles (polystyrene latex) and inorganic particles (silica latex) were used in a careful

evaluation of different cleaning dips, and also in a comparison between drying with a spinner versus isopropanol (IPA) vapor. The best dip was a 0.25:1:5 mixture of $NH_4OH:H_2O_2:H_2O$ which was able to remove more than 95% of both kinds of particles. Note that this mixture is more dilute than standard RCA 1 (1:1:5) which was found to be less effective for polystyrene, and to cause an increase in haze due to surface etching. A 4:1 mixture of $H_2SO_4:H_2O_2$ removed at best 85% of the polystyrene particles, and a 1:100 $HF:H_2O$ mixture removed 95% of only the silica particles. Their presumed removal mechanism for the NH_4OH mixture explains the result by lift-off due to native oxide etching for the polystyrene-latex particles, and native oxide etching and particle etching for the silica-latex particles. Since H_2SO_4 does not etch oxide this explains why it most effectively removes particles it can oxidize such as polystyrene. But the presumed mechanism does not explain why the HF mixture was not able to remove the polystyrene particles by lift-off. Perhaps the answer is that the particles were not removed because of the positive electrostatic surface-potential of 1 kV that the authors measure when a wafer is immersed in the HF mixture. In contrast, other dips result in negative electrostatic surface-potentials as large as 15 kV. An even larger surface-potential of negative 25 kV resulted from the spin dry cycle. Mishima et. al., therefore, propose an IPA vapor drying method which does not induce a surface-potential, and has the ability to neutralize charges left on the wafer surfaces by previous cleaning steps. It is found that, for the optimum conditions of 82° C IPA with water content of less than 1000 ppm and a vapor velocity of 5 cm/sec, the worst set of dips still only result in 3.5 particles larger than 0.5 μm for 125 mm wafers. The less than 1000 ppm water content specification ensures that no water droplets form on the wafer surfaces. Even under the very carefully controlled conditions of these experiments, the authors observed contamination spots if water droplets where allowed to form during the drying step. One of the authors, T. Ohmi, has previously sug-

gested that carbon dioxide from the air can dissolve in water droplets on the wafer surface and leave residues.

Because our lab has so many users with different requirements, it would be difficult to duplicate the controlled conditions of Mishima et. al., but their work does indicate that our wet cleaning methods can be improved. In particular the standard RCA cycle [18] according to the data of Mishima et. al. does not seem as effective as more dilute mixtures. If the present cleaning cycle using the standard sink 6 becomes a limitation to obtaining reasonable results for H_2 bakes at temperatures less than 900° C, sink 9 can be equipped with a spin dryer and used for more controlled cleaning methods. Sink 9 is currently the cleanest, and least used (only 3 qualified users), sink in the lab. Further improvements can be attained by using vapor cleaning methods as discussed in Chapter 4.

Whereas the cleaning of wafers is mostly a practical issue, the quality of the selective epitaxial deposition along the oxide boundaries has fundamental limitations dependent on the growth kinetics. For example, by orienting the oxide boundaries parallel to the {100} planes of the silicon crystal it has been found that the selectively grown silicon surface becomes level with the oxide surface with no facets except in outside corners, and with a low defect density along the oxide sidewall [19, 20]. The location of the facets and their relationship to the crystallographic directions is shown for the case of a square pattern oriented along the {110} planes in Fig. 3.27(a), and for one along the {100} planes in Fig. 3.27(b). Cliff Drowley et. al. [21] have proposed an atomistic model explaining the pattern orientation result by the interaction between the sidewall oxide and the crystal plane responsible for growth in the sidewall direction. According to their model the faceting and defects along the edges of {110} oriented oxide sidewalls occur because of the slow growing {111} and {113} crystal planes. There is an energetically favored formation of twin planes at the oxide boundary causing the formation of very thin

twin plane defects, which, according to Drowley et. al., would look similar in transmission electron microscopy (TEM) analysis to the stacking faults that Endo et. al. [22] claim to be the predominant defect along {110} oxide sidewalls.

The flat on standard wafers is traditionally ground parallel to {110} for wafers with {100} oriented surfaces. The flat is used to register the patterns defined on the wafers so that their sides are oriented parallel to {110}. The reason for this choice of orientation is mostly the historical convenience of being able to use {110} cleavage planes to separate integrated circuits with sides parallel to the patterns. After rotating the patterns 45° so that their sides are parallel of the {100}, a wafer saw is necessary to extract pieces with sides parallel to the pattern. The most convenient way to rotate the patterns is to get wafers with the flat ground parallel to {100}, but most vendors will require the purchase of the whole ingot because it is a non-standard flat orientation. Another method is to rotate the pattern on the mask. We use this method on the EPI test mask which has patterns that are rotated 0° (parallel to {110}), 15°, 30°, and 45° (parallel to {100}). This method is very accurate but complicated in our facility because the computer program that translates the pattern to the format that drives the pattern generator does not allow rotated geometries. There is a final possibility of generating rotated patterns which involves actually rotating the mask when installing it in to the GCA Wafer Stepper. This method allows the angle to be varied quickly to any value desired. However, it can only be used for single layer exposures, and repeatability could be a problem. The sensitivity to misalignment of the oxide pattern to the {100} orientation is an issue which has not been addressed frequently in the literature, but recent data published by Terada et. al. [23] suggests that it depends on the growth conditions, and can be as small as 6°. Corner sharpness and oxide sidewall angle are likewise fundamental issues that might be important in determining selective epitaxial quality but have not been specifically addressed in the

literature.

Most of our selective epitaxy evaluations so far have mostly been visual, including some defect etching. The observations focus on the edge quality of the selective epitaxy, classifying good quality selective epitaxy as having smooth edges. It is not fully understood presently what causes the selective epitaxy edges to become uneven ("rough"), and what crystallographic defects are present in conjunction with the surface roughness. An example of rough edges is shown in the SEM pictures of Fig. 3.28 for a wafer subjected to a 1085° C bake before the standard at 850° C deposition [Expt.31]. The oxide pattern was aligned along the {100} crystallographic planes as illustrated in Fig. 3.28(b) by using a wafer with a {100} major flat provided by Cliff Drowley. Under a Nomarski microscope the epitaxial edges look very rough, but again as in Fig. 3.11 the SEM reveals smooth depressions. For the small 10 μm square in Fig. 3.28(a) the most obvious depressions are those associated with each of the {111} facets present in the convex corners. These depressions are also present for facet free concave corners as shown in Fig. 3.28(b). The depressions look very much like those discussed earlier in conjunction with residual oxide, but it seems unlikely that every corner should have interfacial oxide present at similar locations. It is more likely that the depressions are associated with some type of defect induced by the geometry of the corner.

The continuing work on selective epitaxy by J. C. Lou including analysis with transmission electron microscopy (TEM) should add considerable insight to the conditions that lead to roughness, and the identification of associated crystallographic defects. The TEM cross section shown in Fig. 3.29(a) was prepared by J. C. Lou from the same wafer as shown in Fig. 3.28. It reveals that the field oxide has been removed along the substrate interface for a distance of about 0.8 μm because of the high temperature during the H_2 bake. This undercut is thought to arise from the formation of volatile SiO by the reaction

of Si and SiO_2 as discussed in Chapter 4. We have found that the presence of this undercut correlates to the appearance of a rough selective epitaxy surface along the oxide edges oriented along the {100} directions. The dotted line in Fig. 3.29(b) represents the simplest possibility for the starting interface but it is more likely that the amount of silicon removed during the H_2 bake is greater where more oxide is removed. This would lead to the starting surface ending up at a lower level under the field oxide as represented by the dotted line in Fig. 3.29(c). The change in substrate level exposes slower growing crystallographic planes which can in turn cause the uneven epitaxial surface. However, even when it is believed that the undercut has been eliminated by using H_2 baking at 900° C, as in Chapter 4, there are instances of rough epitaxial edges appearing together with smooth edges on the same wafers. This may result from the epitaxy being very sensitive to the presence of even a very small undercut. Another explanation may be that the plasma etching used to define the vertical oxide sidewalls leaves residues and/or erodes the silicon surface close to the oxide. Cross sections of samples after plasma etching, H_2 baking, and deposition of a thin epitaxial layer would be helpful in further exploring the mechanism causing the edge roughness.

The effect of pattern orientation on the epitaxial edge quality is shown before and after defect etching in Figs. 3.30 and 3.31, respectively. Selective epitaxy on this wafer was grown at a 850° C after a 1000° C H_2 bake, resulting in a field oxide undercut of about 0.2 μm [Expt.155]. The field oxide thickness is 1 μm, and the thickness of the epitaxial film is 0.8 μm. The Nomarski micrographs in Figs. 3.30 and 3.31 were taken after the field oxide was removed with buffered HF. The pattern in Fig. 3.30(a) consists of selective epitaxy lines oriented along the {110} direction, and a similar pattern in Fig. 3.30(b) is oriented along the {100} direction. After growth the edge along the {100} is much rougher than along the {110} which may be caused by edges along the fastest

growing {100} direction being more susceptible to the uneveness of the starting surface that was postulated earlier. Edges along the {110} direction are already dominated by a slow growing facet.

Preferential etching is a very useful technique to quickly evaluate the quality of an epitaxial layer by enhancing the etch rates at defects. The Nomarski micrographs in Fig. 3.31 were taken after a 158 second dilute Schimmel etch [5] has removed about 0.5 μm of silicon from the sample shown in Fig. 3.30. The dilute Schimmel etch is supposed to reveal defects such as dislocations by producing a round etch pit. In Fig. 3.31, pits are observed along only the edges of the epitaxial patterns, not on the substrate or epitaxial surfaces. The pattern oriented along the {110} direction in Fig. 3.31(a) reveals an almost continuous line of etch pits along the epitaxial patterns. The pattern with edges oriented 15° away from the {110} direction in Fig. 3.31(b) displays discrete pits at a density of about 400 pits/mm. For patterns oriented along {100}, as shown in Fig. 3.31(c), the pit density drops an order of magnitude to 35 pits/mm. There is also a pit at each of the corners for the {100} oriented patterns that is perhaps related to the corner facet and pits that are observed in SEM micrograph of Fig. 3.28. The appearance of these pits after defect etching, and their decrease in number as the patterns are oriented towards {100}, correlates well with the published observations of improved epitaxial edge quality of edges along {100} versus {110}. It is surprising, however, that the edge that looks most uneven after deposition results in the fewest etch pits, and that the etch does not enhance the roughness of the surface. It is also surprising that the standard Wright-Jenkins defect etch did not result in the appearance of any etch pits even if etched long enough to remove all of the epitaxial layer. More work is necessary to explore what type of defects the dilute Schimmel etch is decorating.

3.4 Electrical Performance

Electrical parameter evaluation of the epitaxial layers is the proverbial "proof-of-the-pudding" since these are the parameters that will affect fabricated devices. What constitutes an electrical evaluation depends strongly on the application. For our purposes it is important to verify that the hot-wall deposited epitaxy does not have some inherent problems that would limit its practical application. Such limitations would arise from excessive recombination or generation of carriers, and poor oxide quality such as leakage, breakdown, interface states, etc. The deposition of simple metal dot capacitors on oxidized epitaxial wafers have verified that good quality oxides can be grown, and that the effective lifetime is around 50 μsec for 4 μm thick undoped epitaxial films. Jim Moon has also successfully fabricated elevated source/drain devices using selective epitaxy grown in our hot-wall reactor.

However, the most sensitive test of an epitaxial layer is to use it as part of the active region in a device, and a set of discrete n-channel MOS devices have been fabricated for this purpose. In order to isolate any degradation due to the epitaxial layer versus standard substrates, processing conditions were made as identical as possible. Identical prime wafers from the same shipping box were used, and the only variable between the two sets of wafers was the initial epitaxial step that some received. The epitaxial layer was grown on the wafers directly out of the shipping box without further cleaning. Conditions for the epitaxial deposition were the standard 400 sccm of H_2 and 32 sccm of SiH_2Cl_2 at 600 mtorr and 850° C preceded by a H_2 bake at 1000° C [Expt.205]. After the epitaxial deposition step, the wafers were transferred directly back to the shipping box, and from then on processed together with the non-epitaxial wafers as a batch. The complete process following the epitaxial deposition is given in the appendix. It is a modified version of an uncomplicated 4 mask process designed for the EECS 143 undergraduate IC

fabrication course [24]. This course uses 2 inch wafers, and many processing steps are performed in a dedicated laboratory. To ensure the best possible results all processing steps, except for the two ion-implants, were performed in the Class 100 U. C. Berkeley Microfabrication Research Facility on 4 inch wafers. Other modifications to the EECS 143 process include the use of arsenic implanted source/drains, and a 1000° C gate oxidation.

The process flow was simulated with SUPREM-3 (ver. 1B, rev. 8520).† Input files for the epitaxial case are given in the appendix. The simulated boron profile under the gate oxide at the end of the process is shown in Fig. 3.32(a). LOCOS isolation is not used in this process so the initial $3 \cdot 10^{12}$ cm^{-2}, 60 keV boron implant serves as both field and gate threshold dopant. The solid line in Fig. 3.32(a) shows that at the end of the process thermal diffusion has reduced the maximum boron concentration to $8.0 \cdot 10^{15}$ cm^{-3}, and the remaining 1.1 μm thick epitaxial film has been completely doped with boron. The initial epitaxial layer was 1.4 μm thick and its undoped state was simulated as lightly n-type according to the previously presented results in this chapter. The only autodoping effect that could be included with the applicable epitaxy model was diffusion. Because of the boron extending uniformly to the surface for the standard wafer there is a small increase in the boron doping density by the substrate amount to a maximum of $8.5 \cdot 10^{15}$ cm^{-3} as shown by the dotted line in Fig. 3.32(a). The dopant profile of the implanted source/drain regions at the end of the process cycle for an epitaxial wafer is shown in Fig. 3.32(b). The junction depth is 0.30 μm which should ensure that the properties of the epitaxial layer dominates the device characteristics for devices built on the epitaxial wafers. In the absence of a junction depth measurement, the SUPREM simulated value will be

† Provided by Dr. Ginetto Addiego at Lawrence Livermore National Laboratory.

assumed to be the actual junction depth.

The device characteristics were measured on a probing station provided by Dr. Steve Holland at Lawrence Berkeley Laboratory. The largest available devices on the EECS 143 mask set were used to minimize the effect of dimensional variations, and to maximize the measured signals. A 100x100 μm MOS transistor, a 200x200 μm gate oxide capacitor, and a 300x140 μm source/drain junction diode where measured on a center die on a wafer from each of the epitaxial and standard substrate groups. Initial thickness of the epitaxial layer was 1.4 μm which at the end of the process has been reduced to about 1.1 μm by the oxidations steps. Equations and graphs from S. M. Sze's book on semiconductor device physics [25] where used to evaluate the parameters summarized in the Table 3.4, and the remainder of this section is used to discuss the analysis.

The drain current characteristics of the two MOS transistor are shown in Fig. 3.33. Both transistors behave similarly except for the difference in the amounts of saturation current. The saturation current for the epitaxial substrate is larger by a factor of 1.033 which can completely be accounted for by using the slightly thicker gate oxide, and slightly higher threshold voltage, in the familiar first-order equation

$$I_{DS} = \frac{W}{L}\frac{\mu_n C_{ox}}{2}\left[V_{GS} - V_T\right]^2 \tag{3.1}$$

where W/L is the width to length ratio, μ_n is the electron mobility, C_{ox} is the oxide capacitance $\varepsilon_{ox} / t_{ox}$, and V_T is the threshold voltage.

Threshold voltages were measured by extrapolating the slopes of the drain current versus the gate voltage in the linear region shown in Fig. 3.34(a). The threshold voltages for the epitaxial wafer and standard wafer are 0.328 V and 0.344 V, respectively. The larger threshold voltage for the standard wafer agrees with the slightly thicker gate oxide

and higher doping level. The characteristics in Fig. 3.34(a) can also be used to calculate the mobility by first calculating the transconductance g_m from its definition

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W}{L} \mu_n C_{ox} V_{DS} \tag{3.2}$$

and then solving (3.2) for the mobility as

$$\mu_n = \frac{g_m}{(W/L) C_{ox} V_{DS}} \tag{3.3}$$

The resulting mobility versus gate voltage curves are shown in Fig. 3.34(b). The maximum mobility is 656 cm^2/V-sec and 648 cm^2/V-sec for the epitaxial and standard wafers, respectively. The reduction with increasing gate voltage is the same, indicating that the oxide interface of the epitaxial wafer is of the same quality as the standard wafer.

If the data in Fig. 3.34(a) is plotted logarithmically, as in Fig. 3.35(a), the subthreshold swing S can be obtained from the inverse slope of the curve for gate voltages less than the threshold voltage. The subthreshold swing is 88.1 mV/decade for the epitaxial wafer, and 88.8 mV/decade for the standard wafer. The ideal subthreshold swing depends on the gate oxide thickness and the doping level, and can be approximated by the following equation

$$S_{ideal} = \frac{\partial V_{GS}}{\partial(\log I_{DS})} \approx \frac{kT}{q} \ln 10 \left[1 - \frac{C_D}{C_{ox}} \right] \tag{3.4}$$

where C_D is the depletion layer capacitance. Interface traps increases the measured subthreshold swing, and can be modeled as an additional capacitance C_{it} in parallel with the the depletion layer capacitance

$$S_{traps} = S_{ideal} \cdot \frac{1+(C_D+C_{it})/C_{ox}}{1+C_D/C_{ox}} \tag{3.5}$$

Combining (3.4) and (3.5), the interface trap density D_{it} is derived as

$$C_{it} = q\,D_{it} = C_{ox}\left[\frac{S_{traps}}{S_{ideal}} - 1\right]\left[\frac{S_{ideal}}{\frac{kT}{q}\ln 10}\right] \tag{3.6}$$

The necessary oxide thickness and doping level can be obtained from a gate oxide capacitor curve as shown in Fig. 3.35(b). Because of a large metal pad over the field oxide there is substantial parasitic capacitance that must be considered in the calculations. Additionally, the field oxide is thinner than for the standard EECS 143 process because of the implanted rather than spin-on-glass doped source/drains, resulting in a field oxide thickness of 3721 Å and 3325 Å for the epitaxial and standard substrates, respectively. Subtracting out the field oxide component from the accumulation capacitance in Fig. 3.35(b), the respective gate oxide thicknesses are 494 Å and 507 Å for the epitaxial and standard wafers. The capacitance measured at inversion C'_{min} is the series combination of the gate oxide capacitance, and the depletion capacitance corresponding to the maximum depletion depth W_m. The maximum depletion depth can, therefore, be calculated from

$$W_m = \varepsilon_{si}\left[\frac{1}{C'_{min}} - \frac{1}{C_{ox}}\right] \tag{3.7}$$

The maximum depletion width is also related to the doping density N_A according to the approximate relationship given by

$$W_m \approx \left[\frac{4\,\varepsilon_{si}\,k\,T\ln(N_A/n_i)}{q^2 N_A}\right]^{1/2} \tag{3.8}$$

where n_i is the intrinsic carrier density. Solving equations (3.7) and (3.8) by iteration results in doping levels of $8.2 \cdot 10^{15}$ cm^{-3} and $8.7 \cdot 10^{15}$ cm^{-3} for the epitaxial and standard wafer, respectively. These results match closely those from the SUPREM simulation shown in Fig. 3.32(a) at the calculated maximum depletion depth of 0.3 μm. From the gate oxide thickness and doping level the ideal subthreshold swing can be obtained graphically from Sze's book to be 87.2 mV/decade for the epitaxial wafer, and 87.9 mV/decade for the standard wafer. This corresponds to interface densities calculated according to equation (3.6) of $6.7 \cdot 10^{12}$ cm^{-2} and $6.5 \cdot 10^{12}$ cm^{-2}, respectively. It should be noted that analysis of the gate capacitor is more sensitive to interface states but requires a variable measurement frequency which was not available at the time of measurement. However, it can be concluded from the capacitor data there is no significant difference between the epitaxial and standard wafer, either in interface states or fixed charges. Interface states would have resulted in a decreased slope in the transition from accumulation to inversion, and fixed charges in a shift of the whole curve along the voltage axis.

The capacitance-voltage characteristic of the junction diode is shown in Fig. 3.36(a). It can be used to obtain a depth scale, and the doping density profile. The depletion width W is related to the capacitance-voltage characteristic C(V) by the dielectric constant of silicon ε_{si}

$$W = \frac{\varepsilon_{si}}{C(V)} \tag{3.9}$$

Assuming that the junction is one sided the depth scale is obtained scale by adding the 0.3 μm junction depth obtained from SUPREM to the depletion width from equation (3.9). The derivative of $1/C^2$ is related to the doping density according to following equation

$$\frac{d(1/C^2)}{dV} = \frac{2}{q\,\varepsilon_{si}\,N(W)} \tag{3.10}$$

which can be rearranged to allow the calculation of the doping profile N(W)

$$N(W) = \frac{2}{q\,\varepsilon_{si}\, d(1/C^2)/dV} \tag{3.11}$$

The dopant profile obtained from (3.9) and (3.11) is shown in Fig. 3.36(b) together with the profile obtained from SUPREM. There is excellent agreement between simulation and measured data except for the different substrate doping levels. The specification for the substrate doping is a p-type resistivity of 30 to 15 ohm-cm, corresponding to a boron doping level of $4.5\cdot10^{14}$ to $9\cdot10^{14}$ cm^{-3}. A low doping level was used as a worst case in the SUPREM simulation. The experimentally measured doping levels are higher but still within the wafer manufacturers resistivity specification.

The forward current characteristic of the diode is shown in Fig. 3.37. Empirically the forward characteristic can be represented by

$$J_F \sim \exp\left[\frac{qV}{nkT}\right] \tag{3.12}$$

where the ideality factor n equals 1 if diffusion dominates, and 2 if recombination dominates. Equation (3.12) can be arranged in terms of the inverse slope of the forward characteristic

$$\frac{dV}{d(\log J_F)} = \frac{nkT}{q}\ln 10 \tag{3.13}$$

The ideality factor can, thus, be obtained from the ratio of the measured slope to the ideal slope calculated according to (3.13) by setting n equal to 1. For the measurement temperatures given in Table 3.4 the ideal slope is 58.1 mV/decade, and the slopes measured from Fig. 3.37 are 61.3 mV/decade for the epitaxial wafer, and 58.7 mV/decade for the

standard wafers. These slopes correspond to respective ideality factors of 1.06 and 1.01. Ideality factors observed on the epitaxial wafer varied from 1.03 to 1.06 versus an almost constant 1.01 for the standard wafer. More data would be necessary to establish whether this represents a significant difference, or experimental variation.

The reverse-current characteristic of the diode is shown in Fig. 3.38(a). For semiconductors that have a small intrinsic carrier concentration n_i, such as silicon, generation dominates the reverse leakage current as long as the temperature is low enough to not increase n_i significantly. From the assumption that generation dominates the reverse characteristic, the reverse current density J_R can be written as

$$J_R = \frac{q\, n_i\, W}{\tau_e} \tag{3.14}$$

where τ_e is the effective lifetime. Rearranging (3.14) and substituting equation (3.9) for the depletion width W results in

$$\tau_e = \frac{q\, n_i\, \varepsilon_{si}}{J_R(V)\, C(V)} \tag{3.15}$$

Combining the data from Fig. 3.36(a) and Fig. 3.38(a) the result is the effective lifetime profile shown in Fig. 3.38(b). The rapid increase of the lifetime closest to the junction may be and artifact of the current becoming lower than than the measurement limit of about 0.5 pA. The rapid decrease in lifetime past 3.5 μm may be related to defects due to oxygen precipitation in the substrate, or the onset of junction breakdown. variation between substrates. Aside from the lifetime measured at the extremes, the profile decreases slowly from about 55 μsec at 0.8 μm to about 20 μsec at 3.0 μm for both wafers. A more detailed plot of the data from the epitaxial region shown in Fig. 3.38(c) does not reveal a decrease in the lifetime either inside the epitaxial film, or at the substrate

interface.

A summary of the results are shown in Table 3.4. From these results it can be concluded that the properties of the epitaxial layer grown in our hot-wall reactor are not limiting factors in processing environment of our Microlab. More extensive measurements would be necessary to gather enough statistics to discern a possible increase in the defect density resulting from the epitaxial layer.

3.5 Summary

Basic issues and experimental results pertaining to epitaxial silicon in the areas of interface quality, background impurities, autodoping, selective epitaxy, and electrical properties were discussed. It was found that the interface does not have to be atomically perfect in order to deposit essentially defect-free epitaxial layers. Oxide remaining on the starting surface will generate defects either in the form of pits or a rough textured surface, depending on the amount of oxide at the interface. The amount of oxygen detected by SIMS profiling proved to be a more sensitive method for detecting interfacial oxide than visual defects, indicating that small enough oxide patches can be completely and smoothly overgrown. The removal of oxide during the H_2 bake appears from the experimental results to be limited by a reaction between Si and SiO_2 that forms volatile SiO, rather than by a thermodynamic equilibrium limitation. Water adsorbed to the unheated surfaces of the reactor seems to be the most likely source of water contamination that limit the H_2 bake effectiveness. The distribution of interfacial oxide after the H_2 bake in the form of discrete patches was verified with SEM and agrees with the hypothesis of lateral oxide removal by the reaction along the silicon interface. One of the remaining mysteries is the formation of crystallographically oriented pits when large oxide patches are present.

These pits appear as sharply delineated inverted pyramids with a Nomarski microscope, but in an SEM they appear as shallow depressions.

SIMS profiles reveal that the epitaxial films contain more carbon, but less oxygen, than the substrates. The level of carbon observed is no larger than specified as the maximum concentration by the SiH_2Cl_2 supplier. Oxygen profiles are continuous from the level of the substrate indicating that a diffusion from the substrate is a possible source. Thermal donors forming as a result of the presence of oxygen can explain the n-type background doping observed for the undoped epitaxial films. Analysis of dummy wafers that are not removed from the reactor between experiments indicate that carbon and oxygen can accumulate on the wafers between experiments. The sources of this contamination has not been identified but their presence indicates that the procedures surrounding the loading/unloading of the reactor can be improved.

The slow temperature response and low growth rate of the hot-wall reactor causes increased outdiffusion from the substrate when compared to a cold-wall reactor. The result is a less abrupt dopant profile. SUPREM results were found to agree well with data as long as the temperature ramps during the bake and depositions were accurately represented. More abrupt profiles would result for the hot-wall system if the same temperature can be used for both the bake and deposition steps, eliminating the time consuming ramp from bake to deposition temperature.

Selective epitaxy introduces the additional constraint of avoiding oxide nucleation while depositing high quality epitaxial layers. A reduction in temperature during the H_2 bakes enhances the epitaxial quality along the oxide edges by reducing the undercut of the field oxide, but increases the amount of oxide nucleation. Below 1000° C streaks and droplet shaped areas of oxide nucleation appear implicating the pre-epitaxial cleaning procedure. Oxide nucleation can almost be eliminated even for bakes of 900° C if a double

Piranha cleaning cycle is used, and if the spin dryer is cleaned regularly. Dilute Schimmel defect etching of selective epitaxial patterns oriented in various directions revealed the fewest defect pits along edges oriented parallel to the {100} crystallographic planes. This agrees well with other published results, but it was also found that before defect etching the edges parallel to {100} looked less smooth than for patterns parallel to {110} (the worst direction). This surprising result remains to be explained, but identifying the mechanisms that cause the appearance of such non-uniform epitaxial edges are important for improving the quality and control of selective deposition.

Finally, electrical evaluation of MOS devices fabricated on epitaxial layers depositied in the hot-wall reactor revealed no degradation compared to standard substrates processed in our Microlab facility.

References

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Experiments Discussed in Chapter 3

Expt.4: Bake: H_2=600 sccm, 1050° C, 700 mtorr, 10 min

Expt.27: Bake: H_2=2000 sccm, 1080° C, 1.6 torr, 10 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850 °C, 100 min

Expt.28: Bake: H_2=2000 sccm, 1080° C, 8.0 torr, 10 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850 deC, 100 min

Expt.29: Bake: H_2=0 sccm, 1080° C, 10^{-4} torr, 10 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.30: Bake: H_2=2000 sccm, 1080° C, 1.6 torr, 10 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 120 min

Expt.31: Bake: H_2=2000 sccm, 1080° C, 1.6 torr, 10 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 120 min

Expt.36: Bake: H_2=2000 sccm, 1060° C, 1.6 torr, 10 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.37: Bake: H_2=8000 sccm, 1060° C, 5.4 torr, 10 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.39: Bake: H_2=8000 sccm, 1060° C, 5.4 torr, 10 min
Predep: SiH_2Cl_2=100 sccm, H_2=100 sccm, 850° C, 3 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.44: Bake: H_2=8000 sccm, 1000° C, 5.4 torr, 10 min
Predep: SiH_2Cl_2=100 sccm, H_2=100 sccm, 850° C, 5 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.46: Bake: H_2=8000 sccm, 950° C, 5.4 torr, 10 min
Predep: SiH_2Cl_2=100 sccm, H_2=100 sccm, 850° C, 5 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.48: Bake: H_2=8000 sccm, 900° C, 5.4 torr, 10 min
Predep: SiH_2Cl_2=100 sccm, H_2=100 sccm, 850° C, 5 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.50: Bake: H_2=8000 sccm, 1000° C, 5.4 torr, 10 min
Predep: SiH_2Cl_2=100 sccm, H_2=100 sccm, 850° C, 5 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 500 min

Expt.54: Bake: H_2=8000 sccm, 950° C, 5.4 torr, 10 min
Predep: SiH_2Cl_2=100 sccm, H_2=100 sccm, 850° C, 5 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.92: Bake: H_2=8000 sccm, 1000° C, 5.4 torr, 10 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 830°→750° C, 160 min

Expt.155: Bake: H_2=8000 sccm, 1000° C, 5.4 torr, 10 min
Predep: SiH_2Cl_2=100 sccm, H_2=100 sccm, 850° C, 1 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.156: Bake: H_2=8000 sccm, 1000° C, 5.4 torr, 10 min
Predep: SiH_2Cl_2=100 sccm, H_2=100 sccm, 850° C, 1 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.158: Bake: H_2=8000 sccm, 900° C, 5.4 torr, 10 min
Predep: SiH_2Cl_2=100 sccm, H_2=100 sccm, 850° C, 1 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.159: Bake: H_2=8000 sccm, 900° C, 5.4 torr, 10 min
Depramp: SiH_2Cl_2=2 sccm, H_2=8000 sccm, 900°→850° C, 18 min
Predep: SiH_2Cl_2=100 sccm, H_2=100 sccm, 850° C, 1 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.161: Bake: H_2=8000 sccm, 900° C, 5.4 torr, 10 min
Depramp: SiH_2Cl_2=2 sccm, H_2=8000 sccm, 900°→850° C, 18 min
Predep: SiH_2Cl_2=100 sccm, H_2=100 sccm, 850° C, 1 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 100 min

Expt.165: Bake: H_2=8000 sccm, 900° C, 5.4 torr, 10 min
Depramp: SiH_2Cl_2=2 sccm, H_2=8000 sccm, 900°→850° C, 18 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 14.3 min

Expt.166: Bake: H_2=8000 sccm, 900° C, 5.4 torr, 10 min
Depramp: SiH_2Cl_2=2 sccm, H_2=8000 sccm, 900°→850° C, 18 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 14.3 min

Expt.167: Bake: H_2=8000 sccm, 900° C, 5.4 torr, 10 min
Depramp: SiH_2Cl_2=2 sccm, H_2=8000 sccm, 900°→850° C, 18 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 20 min

Expt.205: Bake: H_2=8000 sccm, 900° C, 5.4 torr, 10 min
Predep: SiH_2Cl_2=100 sccm, H_2=100 sccm, 850° C, 2 min
Deposition: SiH_2Cl_2=32 sccm, H_2=400 sccm, 850° C, 200 min

Table 3.1 Deposition Cycle for AMI 7810

Step	Time (min)	Function	Press (torr)	Temp (°C)	H_2 Rot. (slpm)	H_2 Main (slpm)	DCS (slpm)
Pump /Purge		purge with N_2					
Low Heater							
5	3	flow H_2 before T > 500 °C	atm.		11.0	10.9	
10	10	pump down heater on	9.8	850	11.0	10.9	
15	2	ramp to bake	9.8	950	11.0	10.9	
20	5	bake	9.8	950	11.0	10.9	
25	3	ramp to deposition	9.8	860	11.0	10.9	210 bypass
30	10	deposition	9.8	860	11.0	10.9	210
35	1	end deposition	9.8	860	11.0	10.9	
40	5	cool down	9.8		11.0	10.9	
45	3	post purge & backfill	atm.				

Table 3.2 Experiment Summary for Dummy Wafer D2-8

Date	Expt.	Bake Temp. (°C)	Bake Time (min)	DCS depramp (sccm)	Predep Time (min)	Depositio n Temp. (°C)	Depositon Time (min)	SIMS depth (μm)
9/28/89	167	900	20	2	0	850	20	0.1
9/28/89	166	900	20	2	0	850	14.33	0.2
9/28/89	165	900	20	2	0	850	14.33	0.3 <D>
9/26/89	164	900	20	2	0	850	18	0.5
9/25/89	163	1000	20	0	1	850	100	1.2
9/23/89	Bake & Coat	1075	45	0	1	850	100	1.8 <C>
9/18/89	162	900	20	0	0	850	0	1.8 <C>
9/9/89	161	900	10	2	1	850	100	2.6
9/8/89	160	900	10	2	1	850	100	3.3 <B>
9/7/89	159	900	10	2	1	850	100	4.0 <A>
9/6/89	158	900	10	0	1	850	100	4.7
9/4/89	157	1000	10	0	1	850	100	5.4
9/3/89	156	1000	10	2	1	850	100	6.1

Table 3.3 Pre-Epitaxial Cleaing Procedures

Standard Lab Clean	Improved Clean
Refreshed Piranha [1] (10 min)	Refreshed Piranha (10 min)
DI water rinse, first 2 tanks (2 min each minimum)	DI water rinse, first 2 tanks (2 min each minimum)
DI water rinse, resistivity tank (within 2 Mohm-cm of empty tank)	DI water rinse, resistivity tank (within 2 Mohm-cm of empty tank)
10:1 HF dip (until dewet)	10:1 HF dip (until dewet)
DI water rinse, first 2 tanks (2 min each minimum)	DI water rinse, first 2 tanks (30 sec each maximum)
DI water rinse, resistivity tank (within 2 Mohm-cm of empty tank)	Refreshed Piranha (5 min)
Spin dry (2 min)	DI water rinse, first 2 tanks (2 min each minimum)
	DI water rinse, resistivity tank (within 2 Mohm-cm of empty tank)
	Spin dry (2 min)
	Optional 2:1 HF vapor etch [2] (5sec)

1. Made by adding 100 ml of hydrogen peroxide to hot sulfuric acid tank.

2. To remove chemical oxide for low temperature bakes [Ch. 4].

Table 3.4 Electrical Characterization Results

	Epitaxial Substrate	Standard Substrate
field oxide (Å)	3721	3325
gate oxide (Å)	494	507
V_T (V)	0.328	0.344
μ_n (cm^2/V-sec), max	656	648
N_A (cm^{-3}), threshold	$8.2 \cdot 10^{15}$	$8.7 \cdot 10^{15}$
S_{ideal} (mV/decade)	87.2 (21.4° C)*	87.9 (20.3° C)*
S_{meas} (mV/decade)	88.1	88.8
D_{it} (cm^{-2})	$6.7 \cdot 10^{12}$	$6.5 \cdot 10^{12}$
diode $_{ideal}$ (mV/decade)	58.1 (19.8° C)*	58.1 (19.2° C)*
diode $_{meas}$ (mV/decade)	61.3	58.7
n (ideality factor)	1.06	1.01
τ_e (μsec), @1 μm	47.3	42.9

* Measurement temperature

Fig. 3.1 Wafer surface inspection using an intense collimated light source. The source used in our case is a slide projector mounted in a service area so as not to generate particles that would affect the observations. Deviations from a flat wafer surface generate scattered light that can be observed by holding the wafer at a shallow angle.

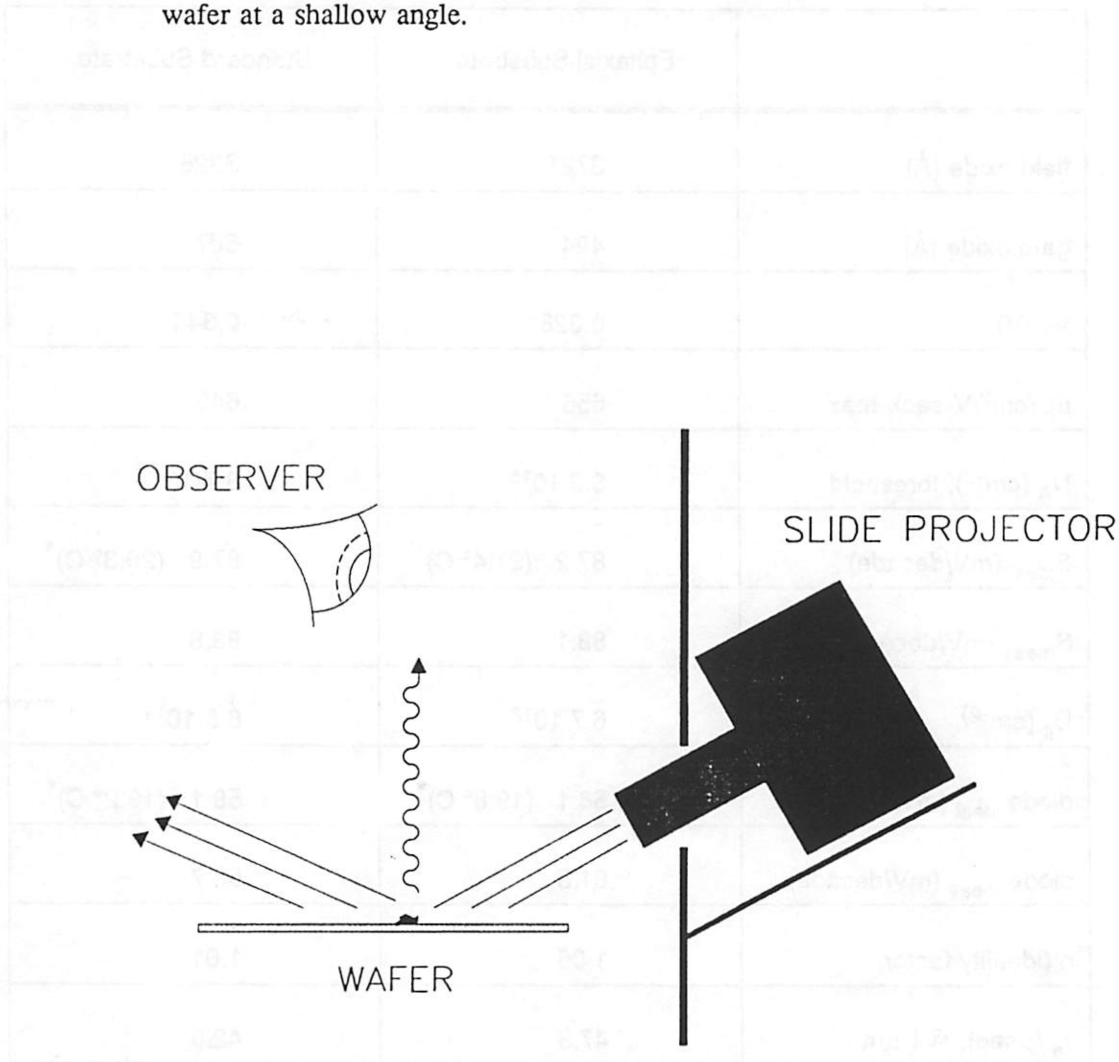


Fig. 3.2 Nomarski micrographs of epitaxial films grown at 850° C after a 1060° C bake in (a) 2 slpm H_2 and (b) 8 slpm H_2.

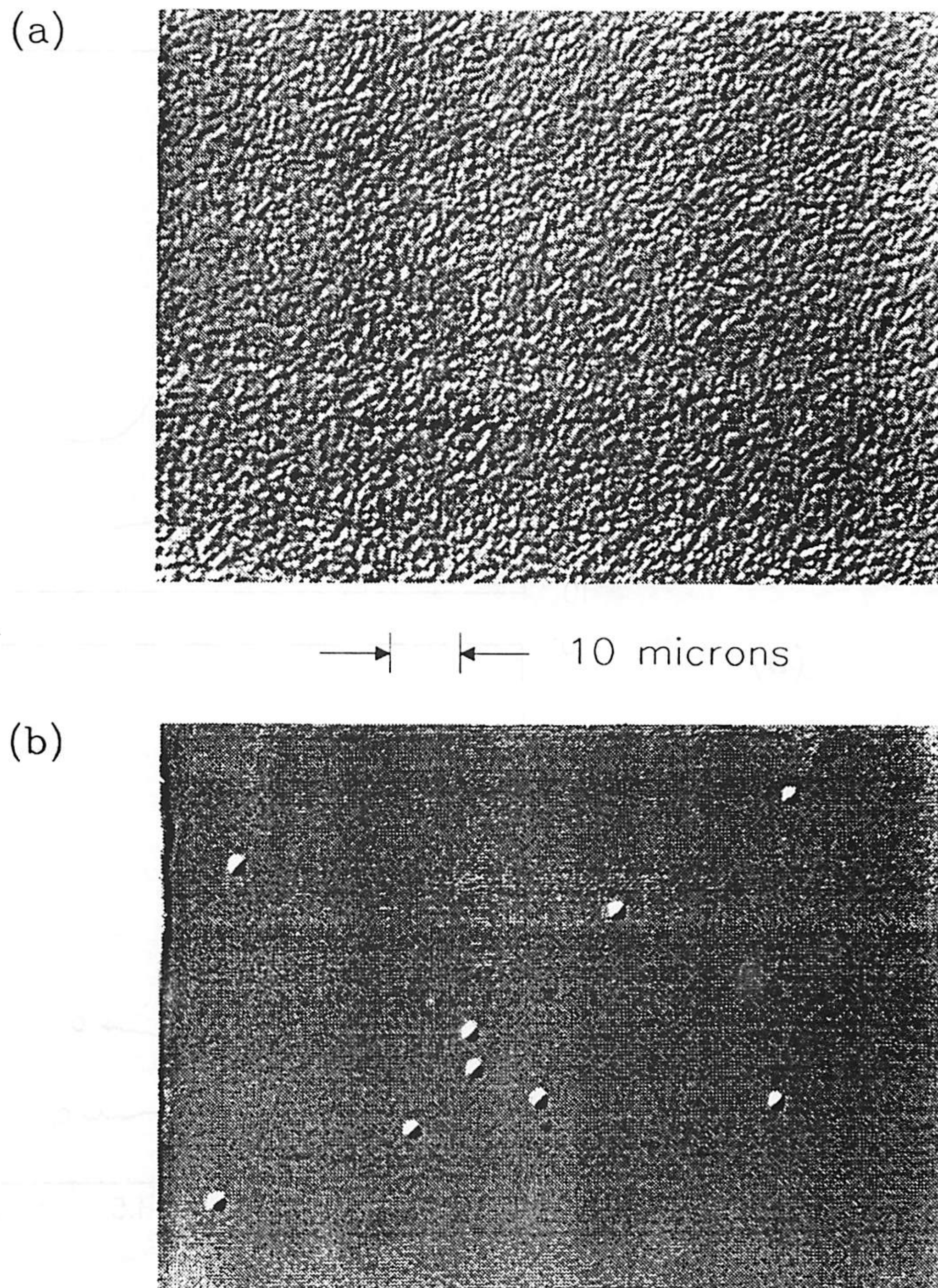


Fig. 3.3 SIMS profiles of oxygen and carbon measured on the same samples as shown in Fig. 3.2. The epitaxial films were grown at 850° C after a 1060° C bake in (a) 2 slpm H_2 and (b) 8 slpm H_2.

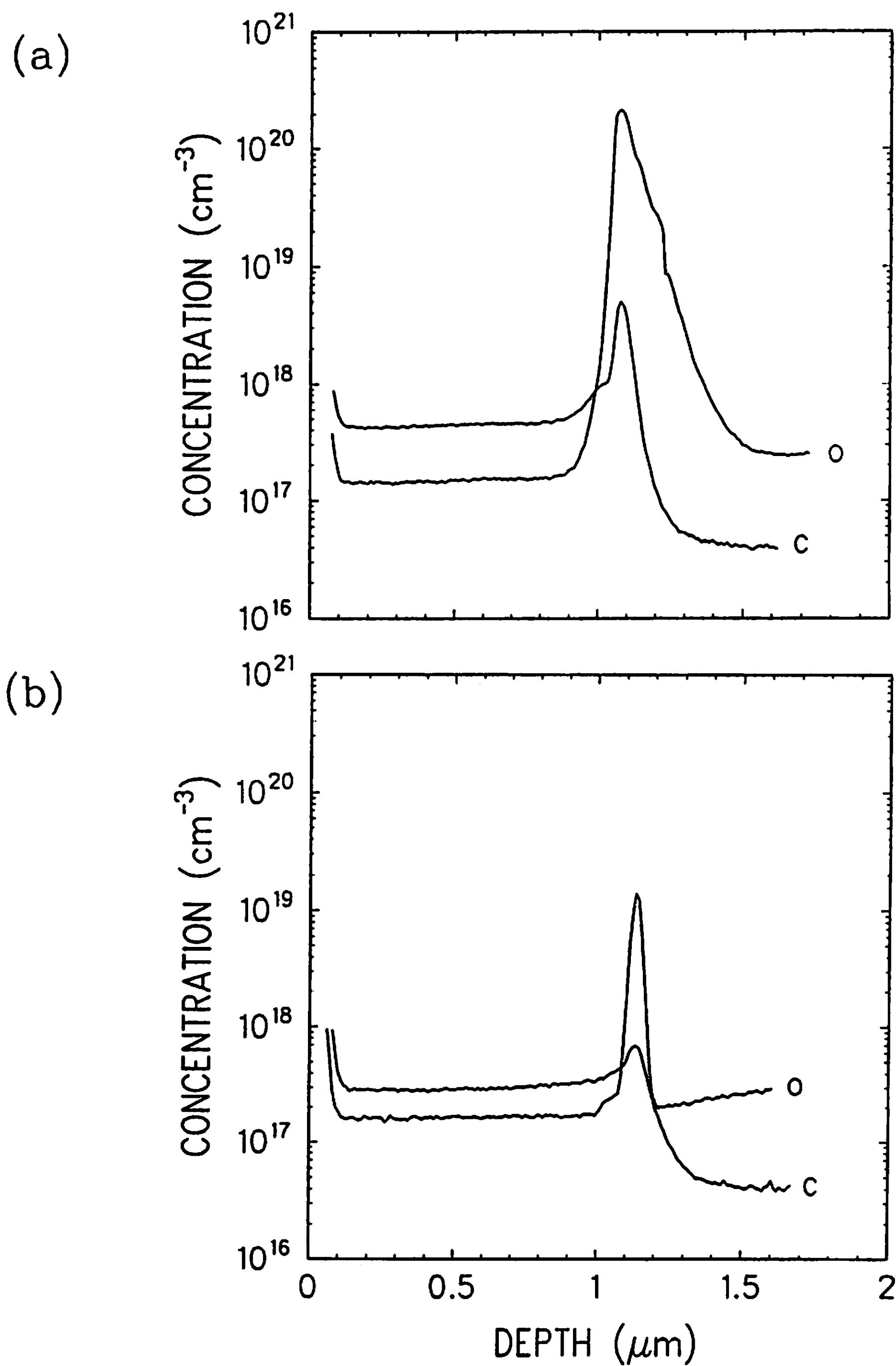


Fig. 3.4 SIMS profiles of carbon and oxygen in a series of epitaxial films. For each sample the nominal baking duration was 10 minutes at the following temperatures: (a) 1050° C, (b) 1000° C, (c) 950° C, and (d) 900° C.

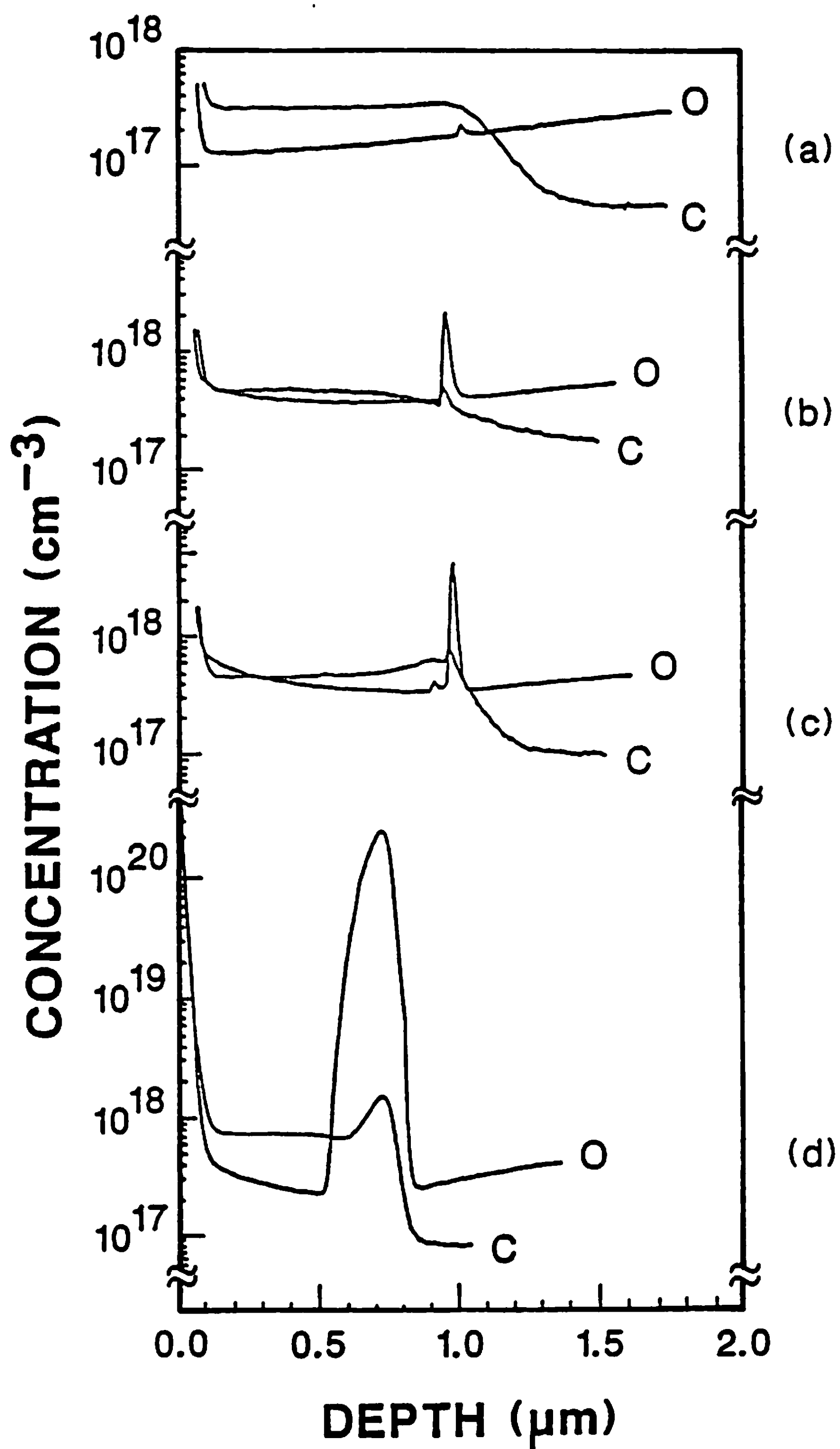


Fig. 3.5 SIMS profiles of carbon and oxygen for epitaxial films deposited at 850° C after baking at 1085° C using either (a) 2 slpm H_2 and 1.6 torr, or (b) no H_2 and 10^{-4} torr (turbo pumped).

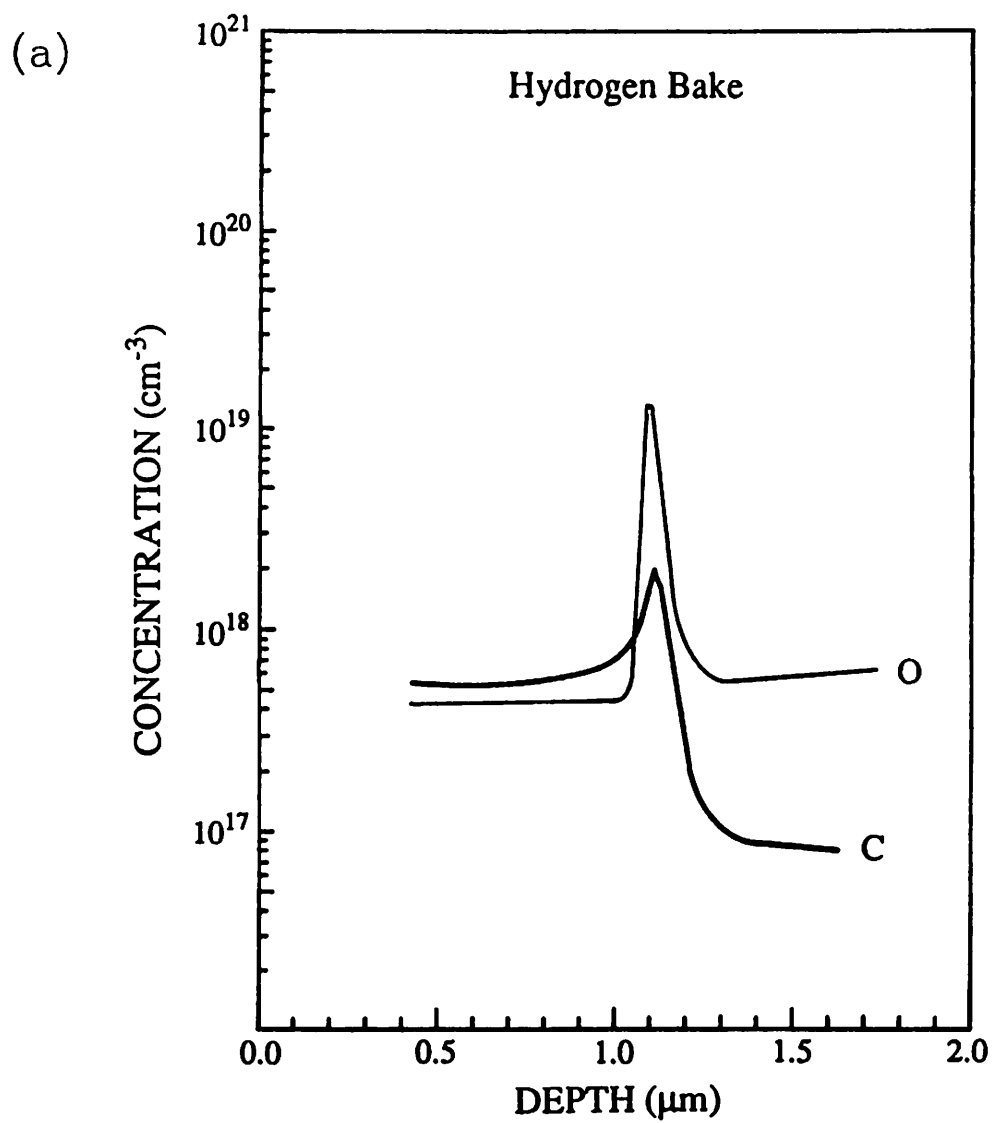


Fig. 3.5 (cont.)

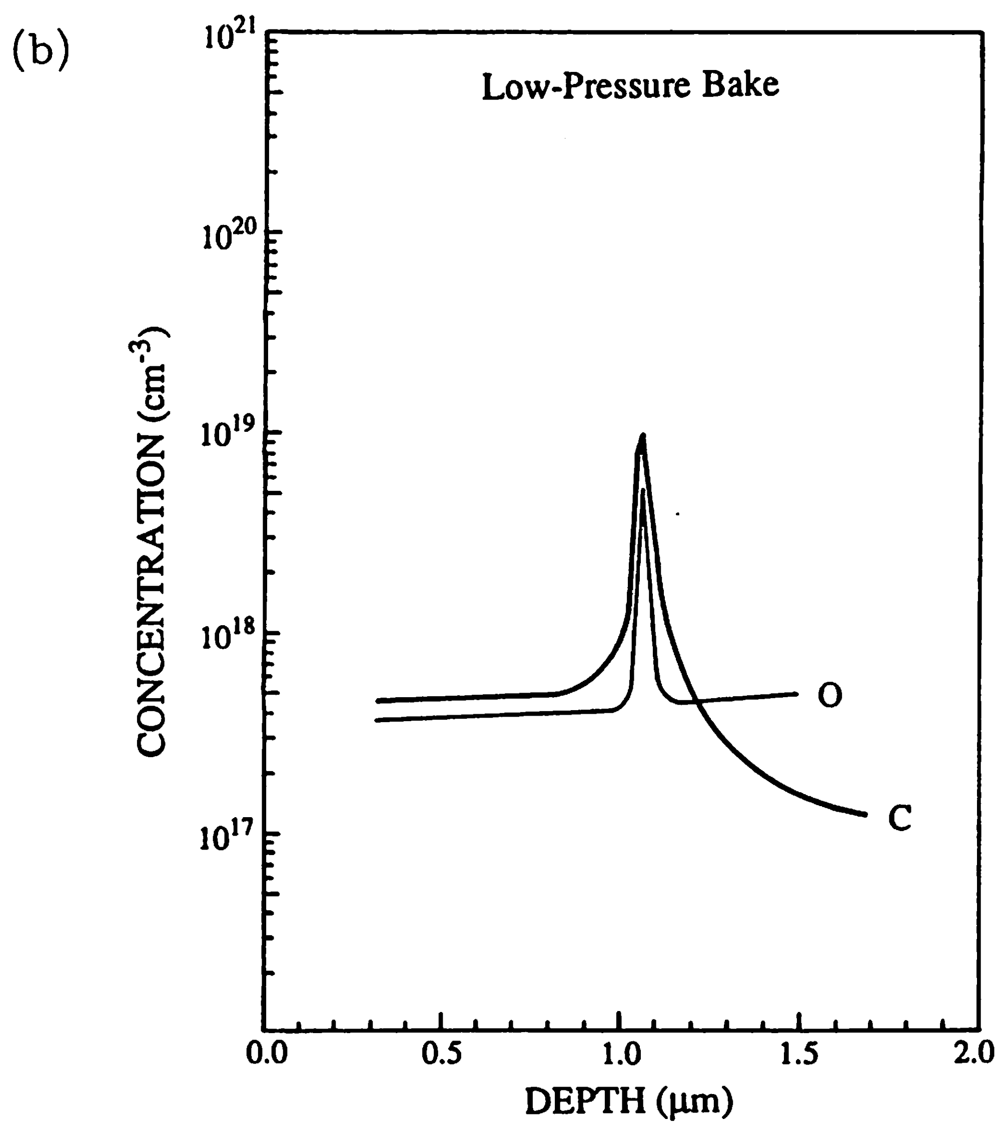


Fig. 3.6 The critical H_2O pressures versus temperature measured by Ghidini and Smith are shown plotted with solid lines. The dashed lines show the H_2O pressures for the indicated H_2 baking conditions using the background concentration of H_2O inferred from mass-spectrometer measurements. The experiment 29 curve shows the reactor pressure measured during the turbo pumped bake and cool-down to deposition.

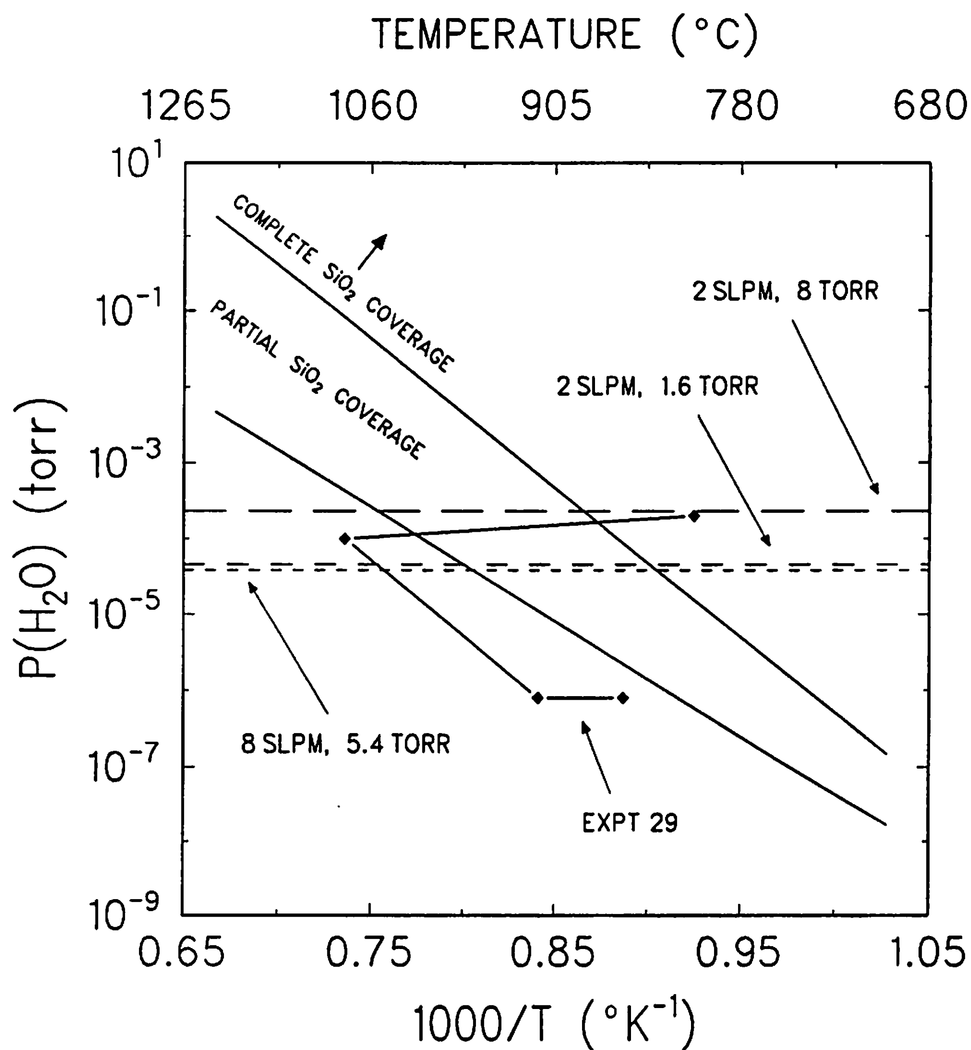


Fig. 3.7 SEM pictures of silicon surfaces baked at 1050° C in H_2 without deposition. Samples were not gold coated so oxide areas appear whitish. Pictures show where taken from a strongly hazy area (a), and a lightly hazy area (b).

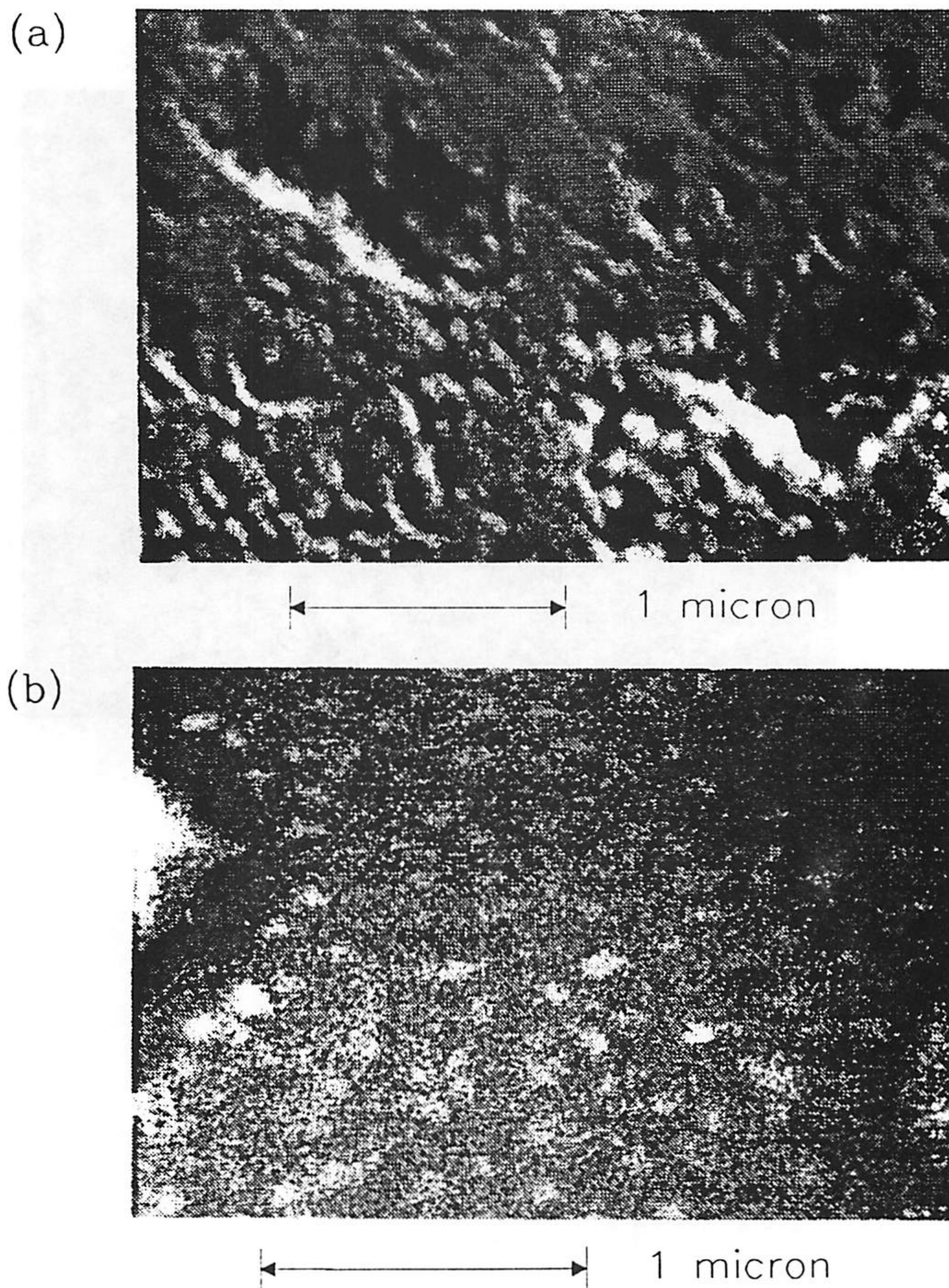


Fig. 3.8 Epitaxial film originally 1 μm thick that has been etched to a thickness of 0.3 μm with a dilute Schimmel. Area shown was originally smooth with square pits.

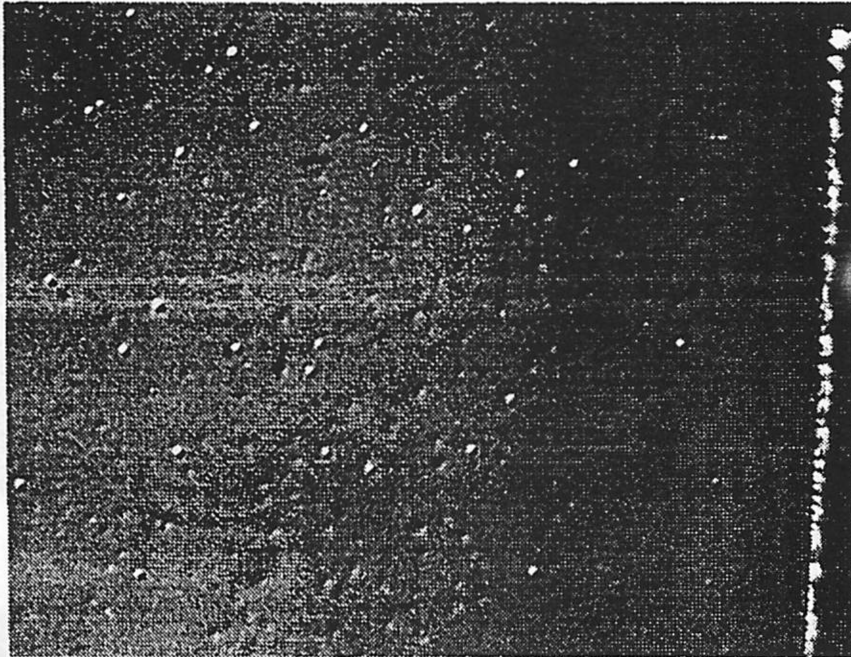


Fig. 3.9 A large pit in a 4 μm thick epitaxial film suggesting that square pits result from incomplete overgrowth.

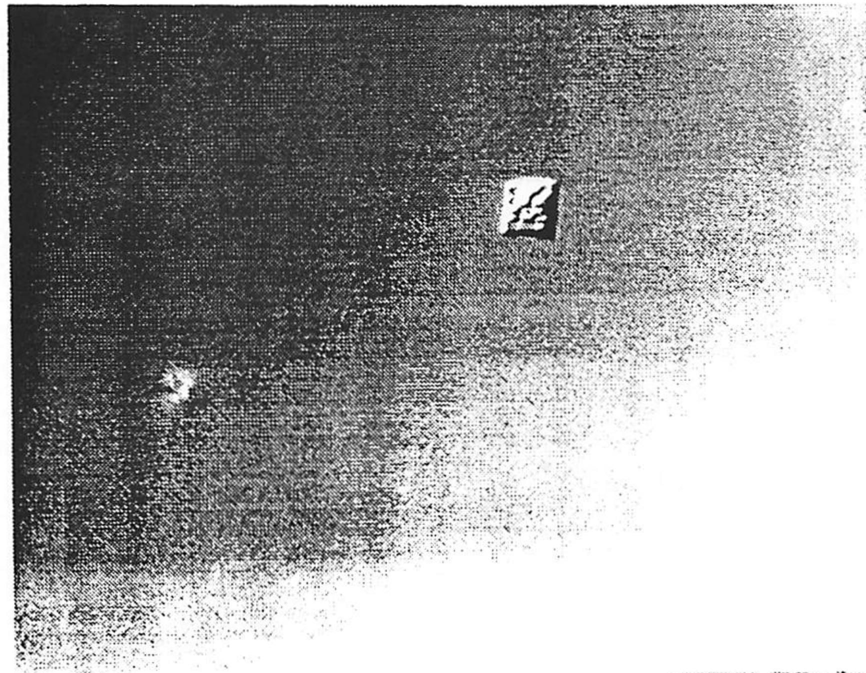
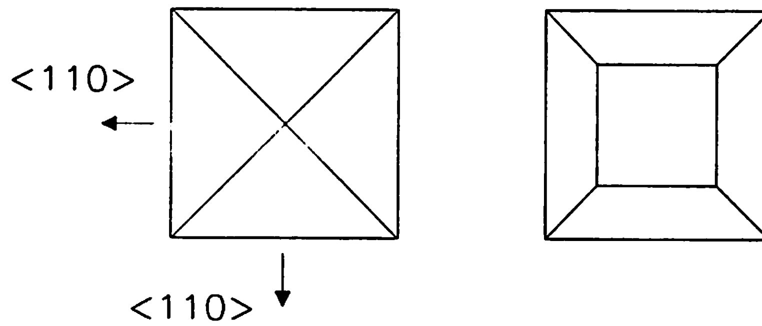


Fig. 3.10 Illustration of the hypothesis that once overgrowth fronts meet on top of an oxide patch the pit starts to fill in from the bottom, slowing the growth of the <111> facets.



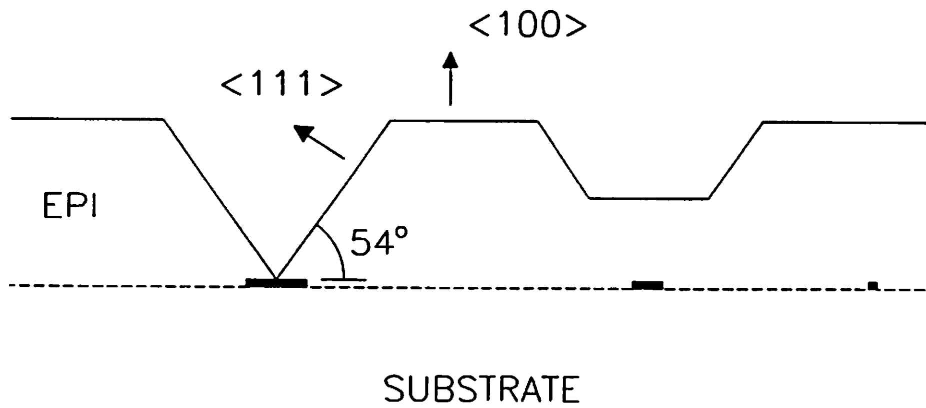


Fig. 3.11 SEM picture showing the selective epitaxy around a wet etched oxide pattern (light area) oriented along the {110}. Square pits in the foreground are only visible at a shallow angle in the SEM, revealing that they are quite shallow.

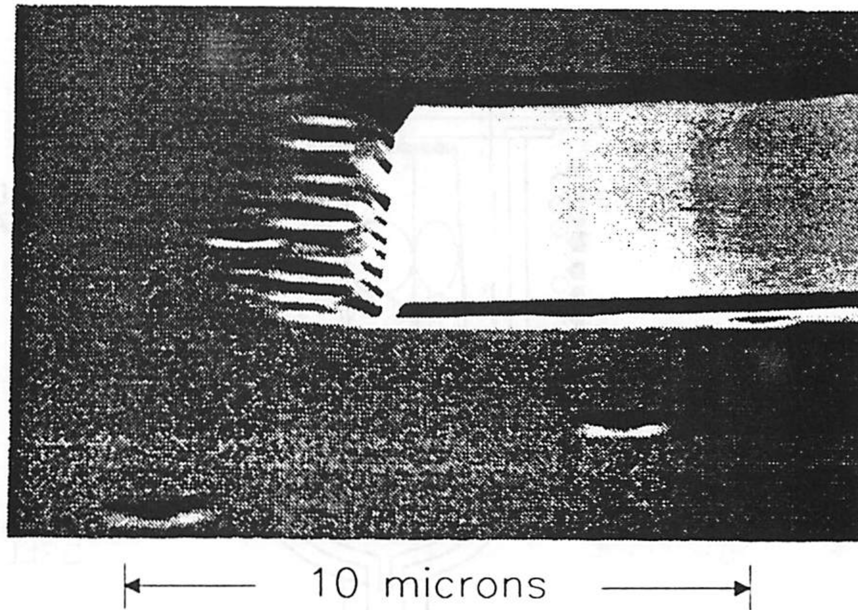


Fig. 3.12 Schematic of a radiantly heated barrel-type epitaxial reactor such as the Applied Materials 7810. [Modified from an illustration in "*Handbook on Semiconductors*", North-Holland Publishing Co., 1980].

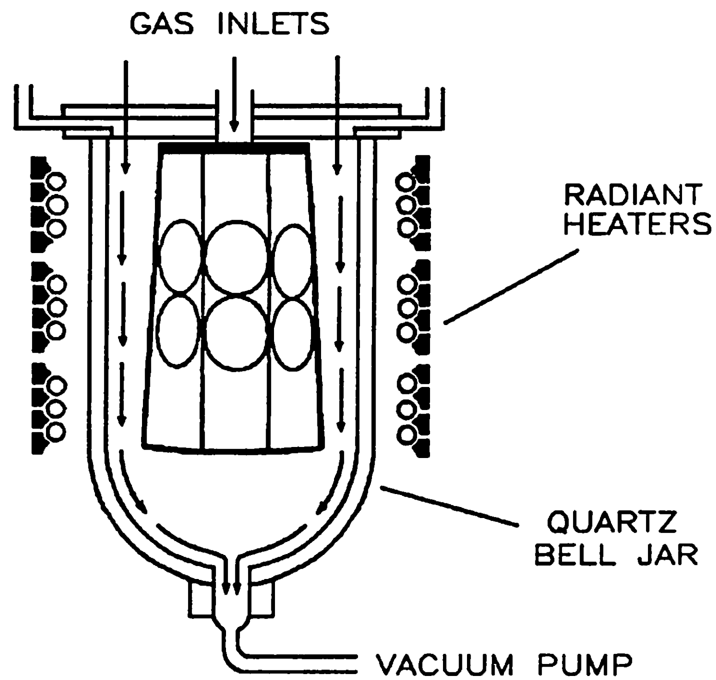


Fig. 3.13 SIMS profiles of carbon, oxygen, and antimony for an epitaxial film grown in a cold-wall Applied Materials 7810 reactor.

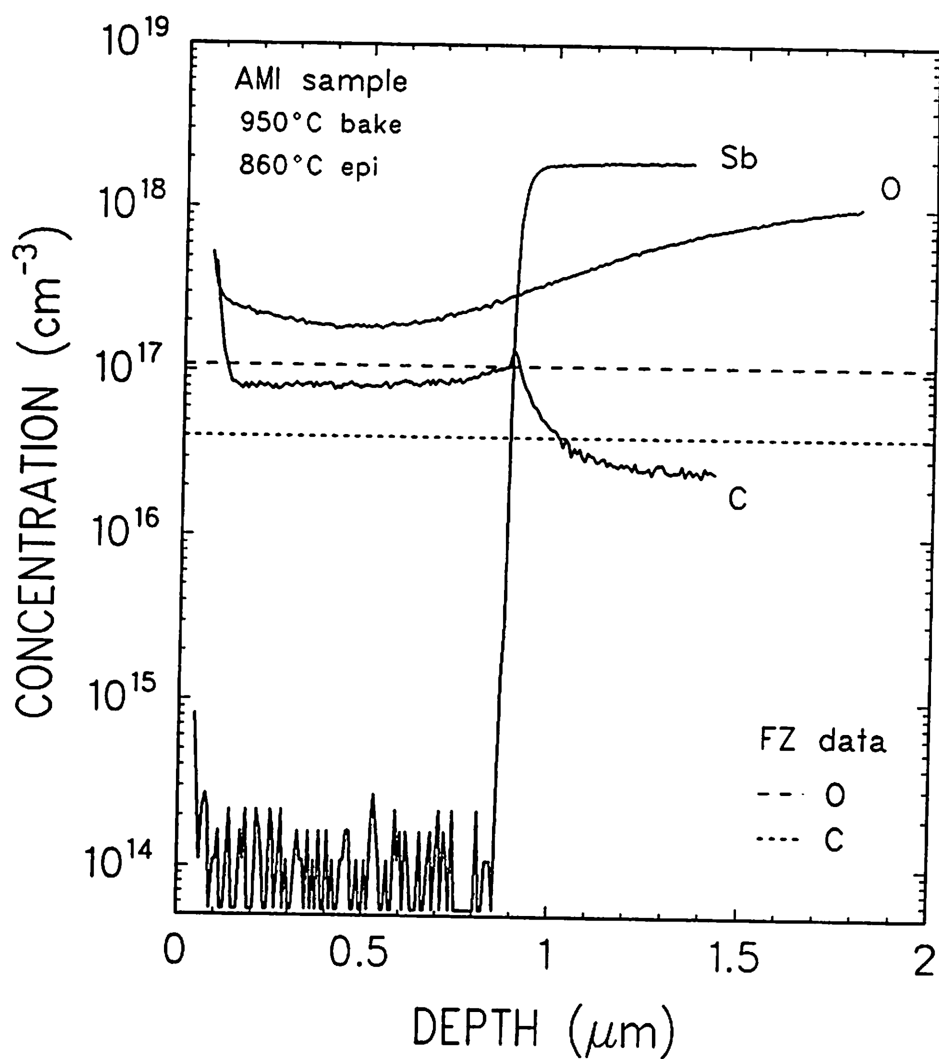


Fig. 3.14 SIMS profiles of carbon and oxygen for the dummy wafer D2-8. The float zone (FZ) levels for carbon and oxygen are shown with a dotted line and indicate the measurement limit for that session. The labeled peaks correspond to the experiments indicated with the same labels in Table 3.2.

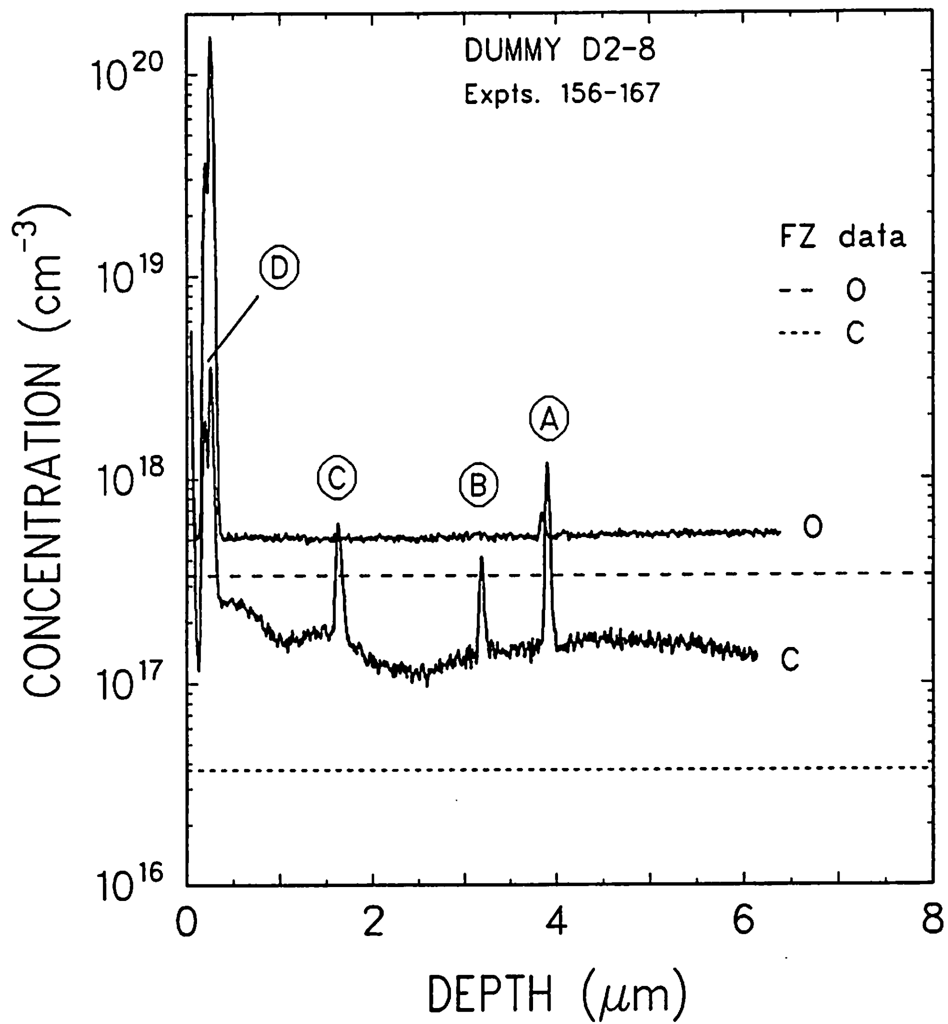


Fig. 3.15 SIMS profiles of oxygen after a 1 μm thick epitaxial films were grown in the Applied Material 7810 (AMI sample) and our reactor (M2-9 sample). Oxygen measurement limit was $1 \cdot 10^{17}$ cm^{-3} for this session.

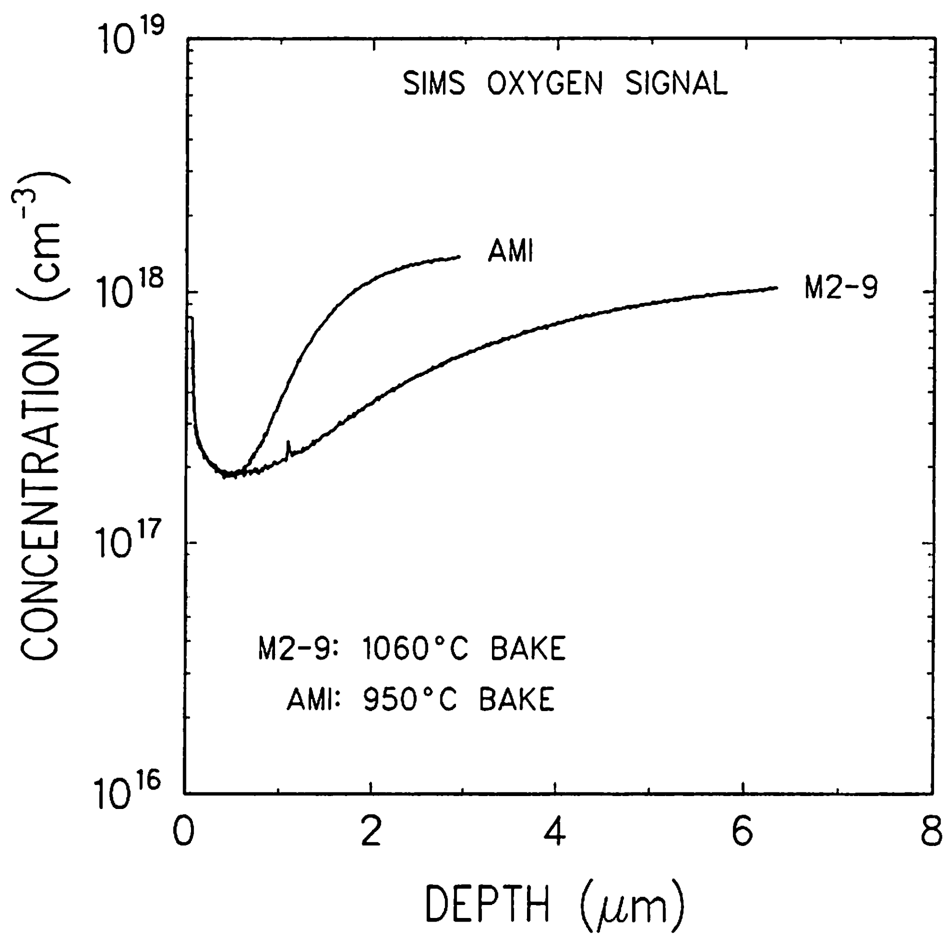


Fig. 3.16 SIMS profile of antimony and SRP n-type carrier concentration profile for a 1 μm thick epitaxial film.

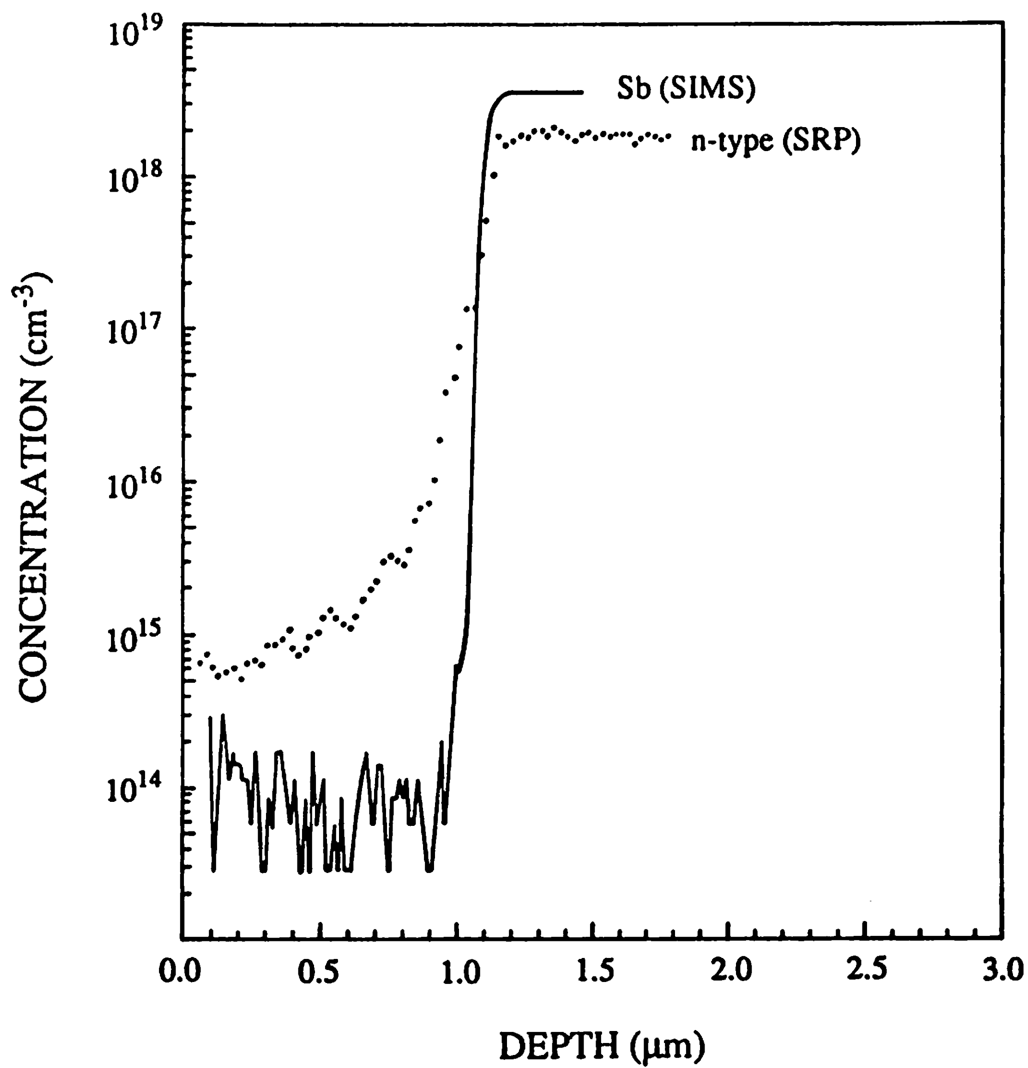


Fig. 3.17 SRP n-type carrier concentration profile for a 4 μm thick epitaxial film.

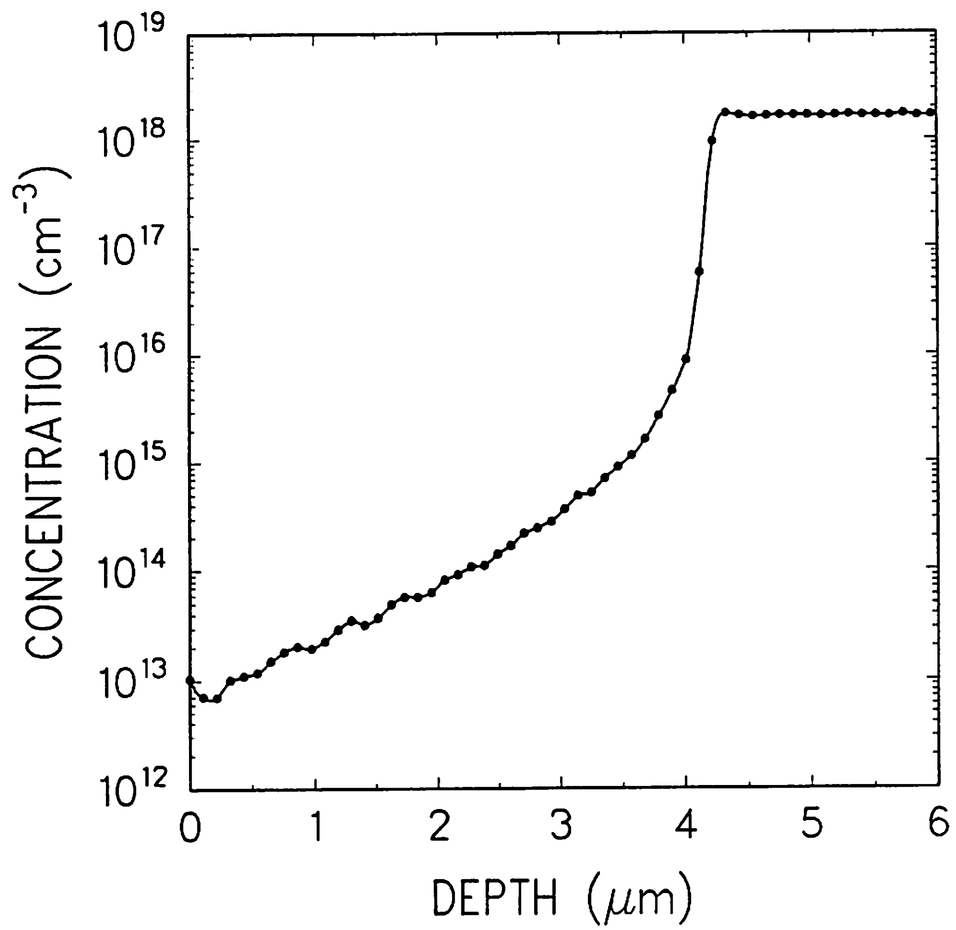


Fig. 3.18 Comparison between the measured SIMS profile for antimony and the antimony profile simulated with SUPREM for (a) the Applied Materials 7810 cold-wall reactor, and (b) our hot-wall reactor.

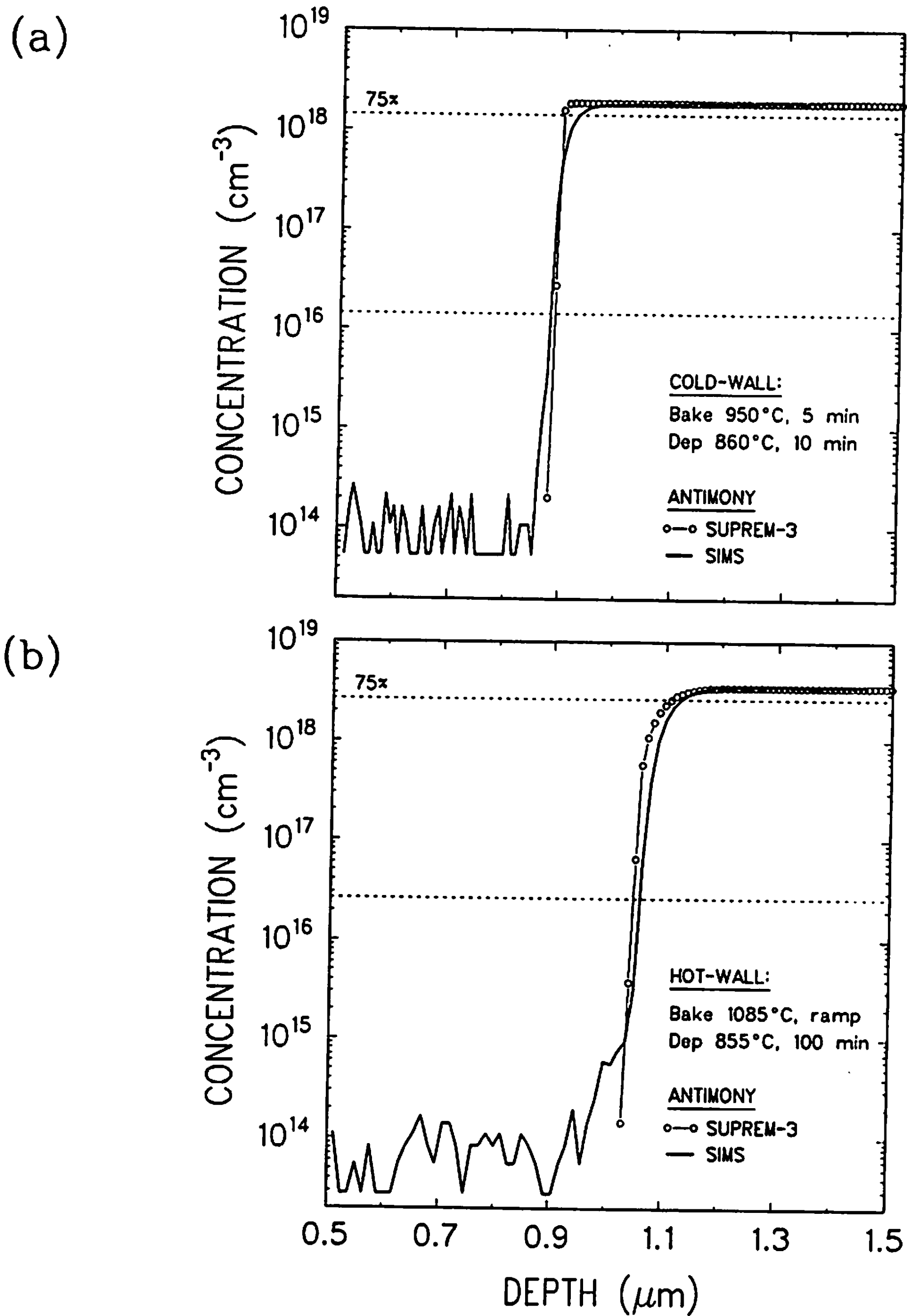


Fig. 3.19 SUPREM simulated antimony profiles for a 1 μm thick epitaxial deposition using a typical cold-wall cycle in (a), and a typical hot-wall cycle in (b). The effect of outgassing due to the bake is demonstrated by including a simulated deposition without a prior bake (not possible in the real world).

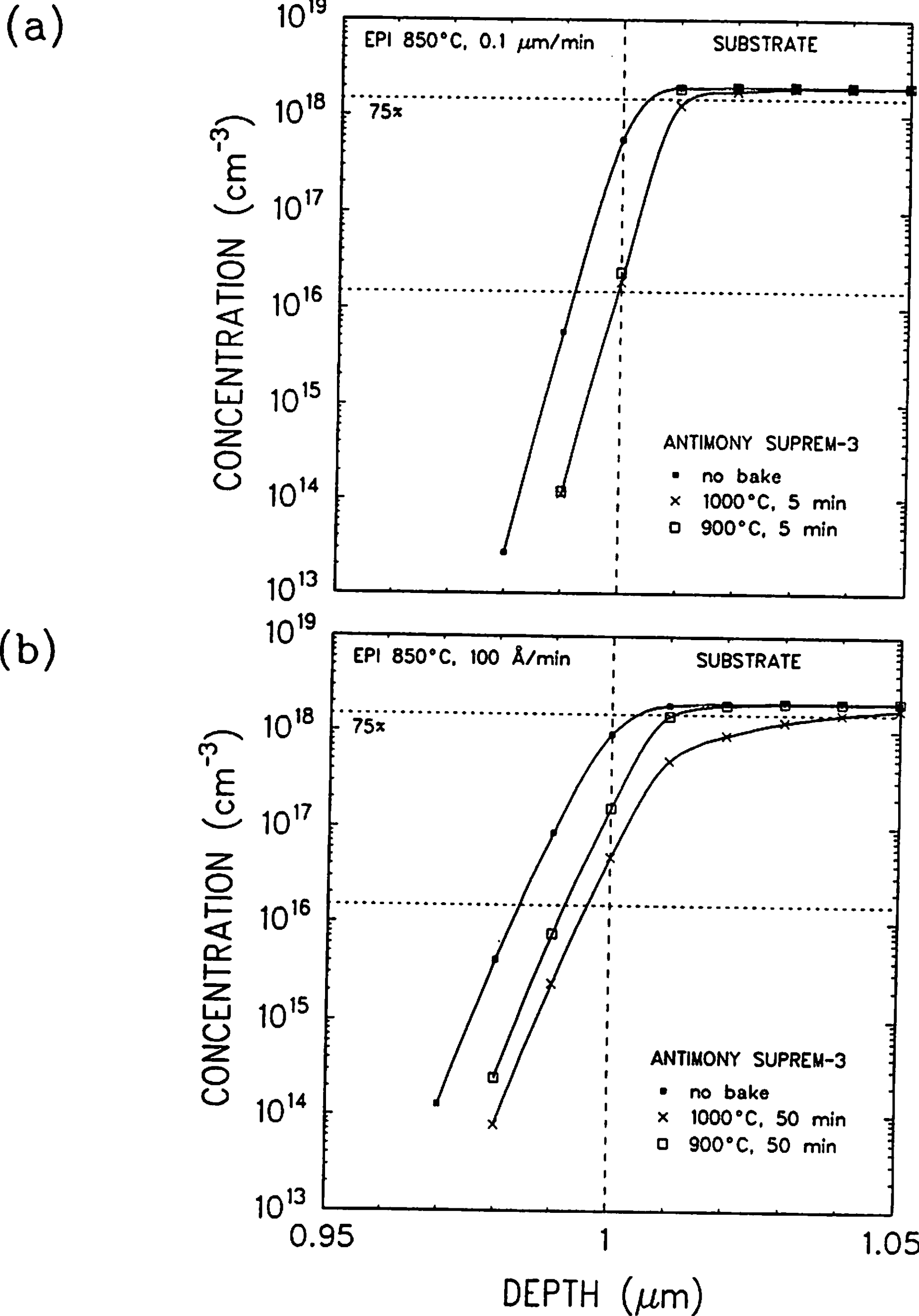


Fig. 3.20 Simulated antimony profiles before and after a typical hot-wall deposition of a 1 μm thick epitaxial film. The effect of outgassing due to the bake is demonstrated by including a simulated deposition without a prior bake (not possible in the real world).

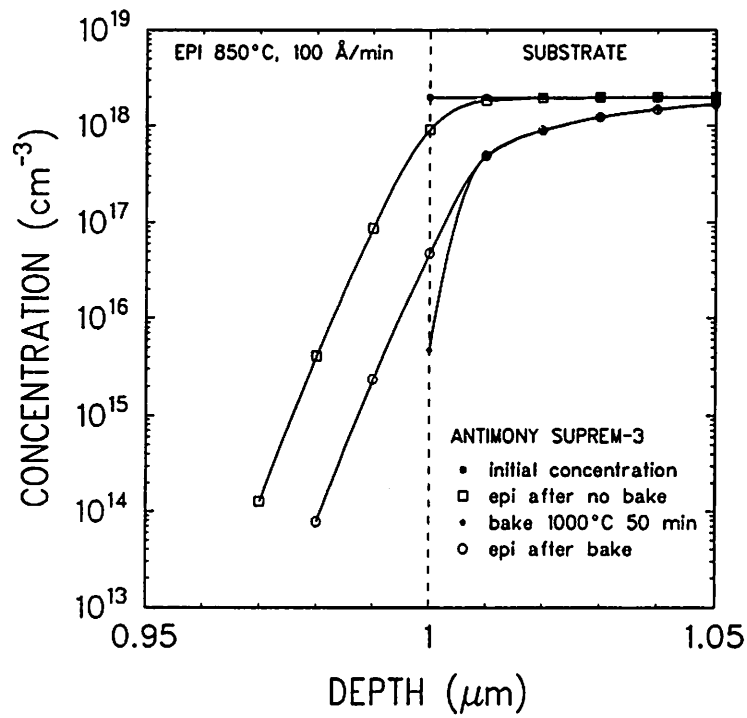


Fig. 3.21 Comparison between the measured SIMS profile for boron, and the boron profile simulated with SUPREM for our hot-wall reactor.

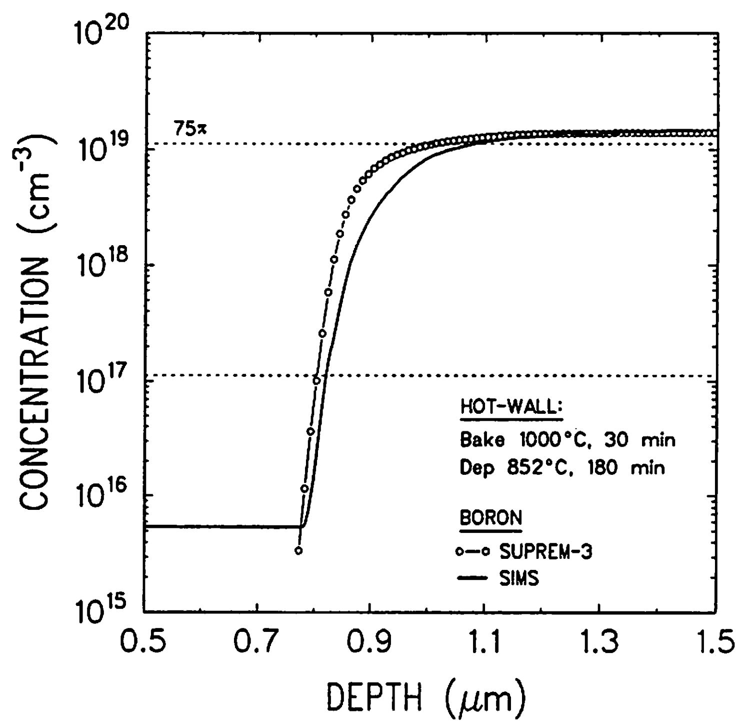


Fig. 3.22 SUPREM simulated boron profiles for a 1 μm thick epitaxial deposition using a typical cold-wall cycle in (a), and a typical hot-wall cycle in (b). The effect of outgassing due to the bake is demonstrated by including a simulated deposition without a prior bake (not possible in the real world).

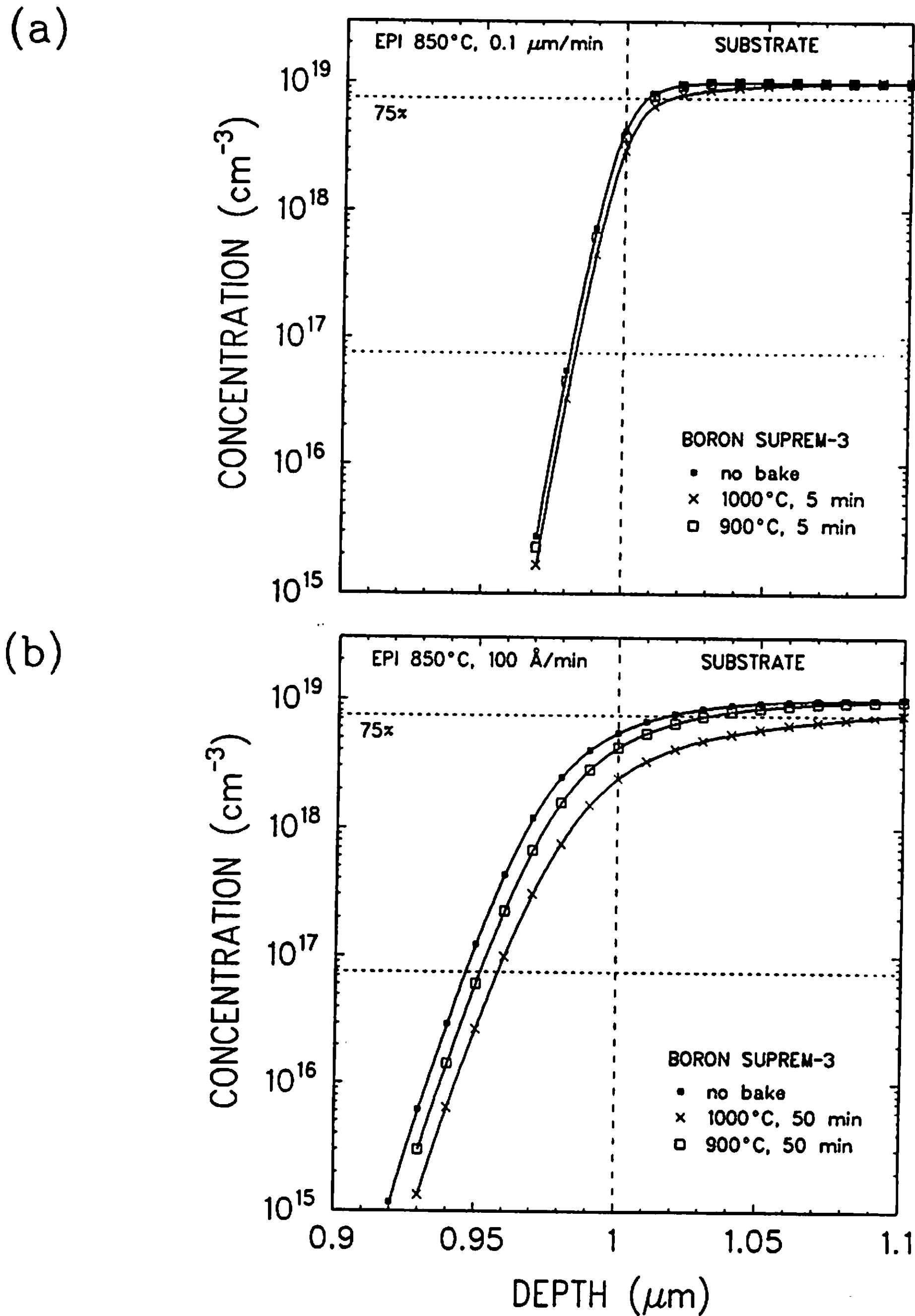


Fig. 3.23 Simulated boron profiles before and after a typical hot-wall deposition of a 1 μm thick epitaxial film. The effect of outgassing due to the bake is demonstrated by including a simulated deposition without a prior bake (not possible in the real world).

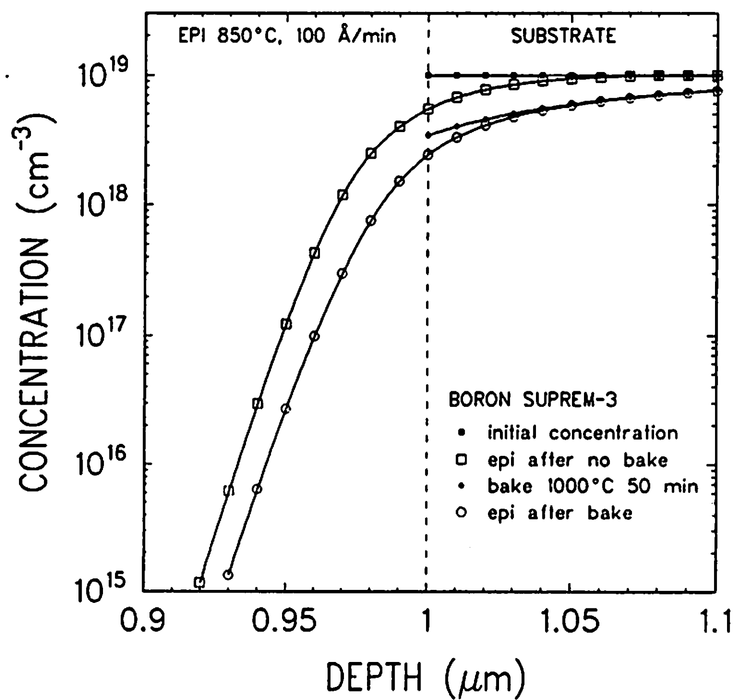


Fig. 3.24 Illustration of the selective epitaxy process. Molecules are impinging on all of the wafer surface but only react to form silicon deposits on exposed substrate and oxide imperfections that allow silicon nuclei to form.

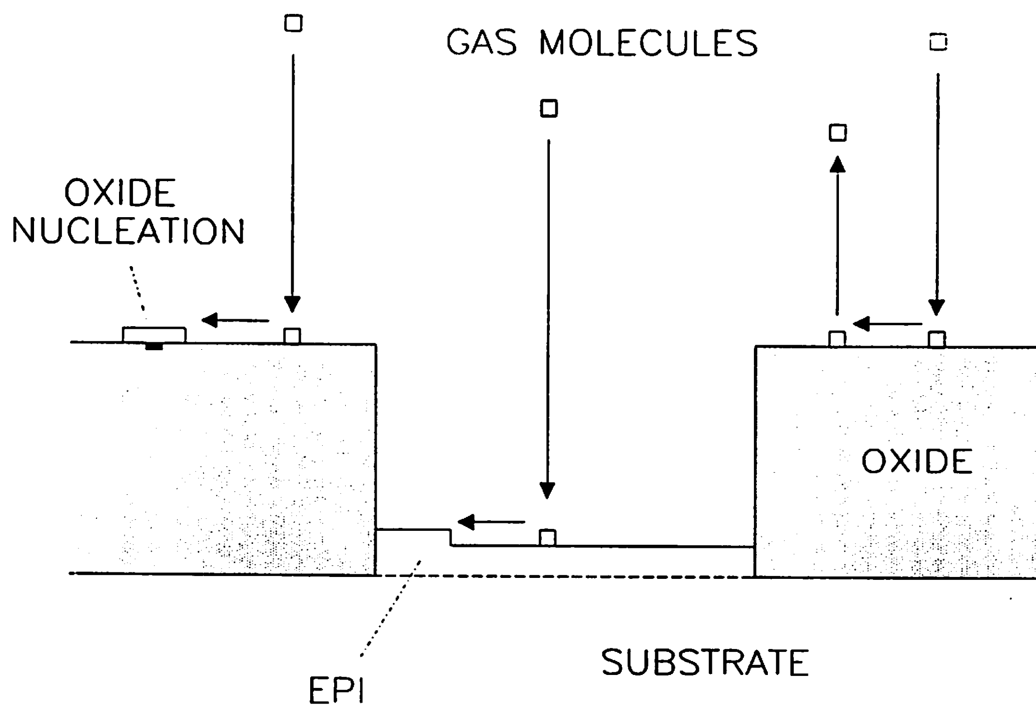


Fig. 3.25 SEM picture showing the sharp delineation between clean oxide and a circular patch of silicon nucleation.

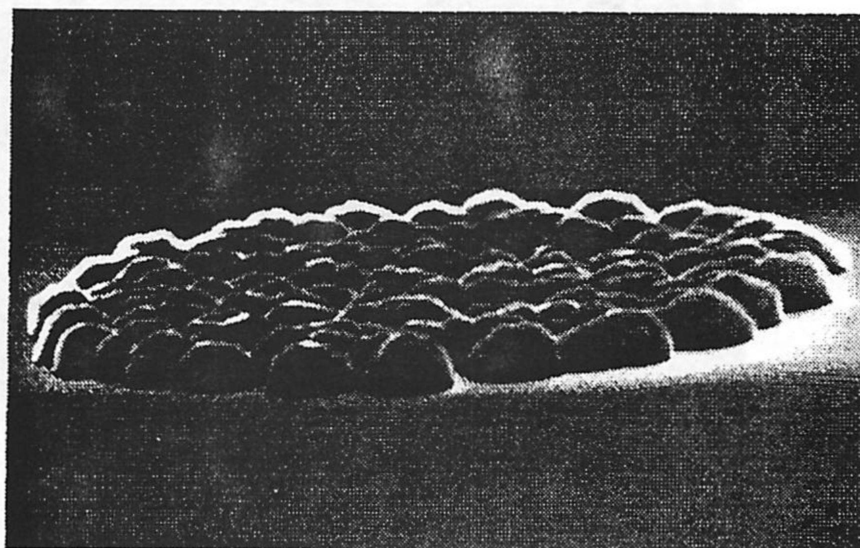


Fig. 3.26 Nomarski micrographs of unwanted oxide nucleation resulting from a selective epitaxial deposition. The samples where processed identically except for using the two different pre-epitaxial cleans shown in Table 3.3. Sample (a) received standard lab cleaning, and sample (b) received improved cleaning.

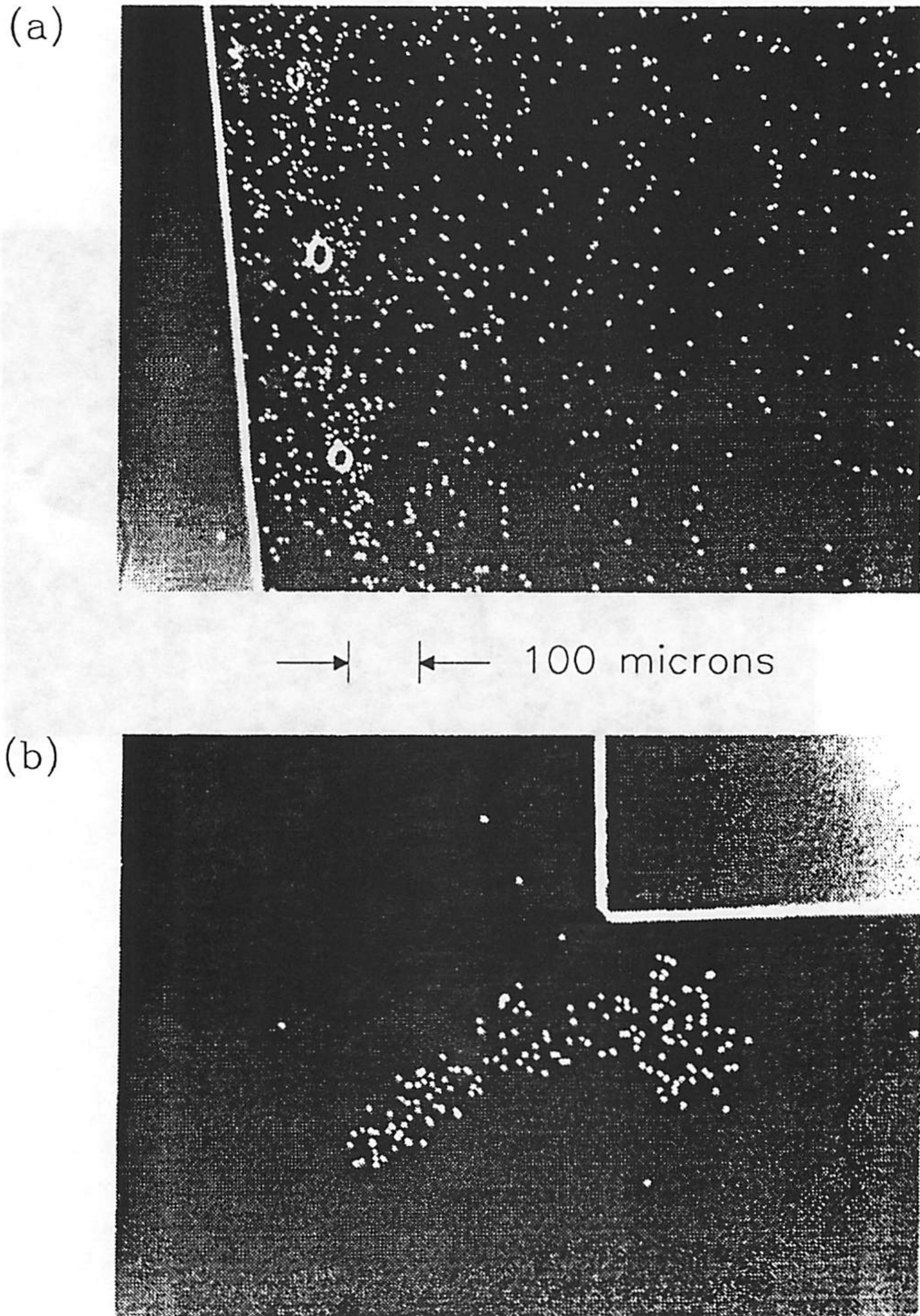


Fig. 3.27 Illustrating the effect of oxide pattern orientation on facet formation. In (a) the oxide pattern is oriented with the sidewalls parallel to the {110} planes of silicon substrate, and in (b) the oxide sidewalls are oriented parallel to {100}.

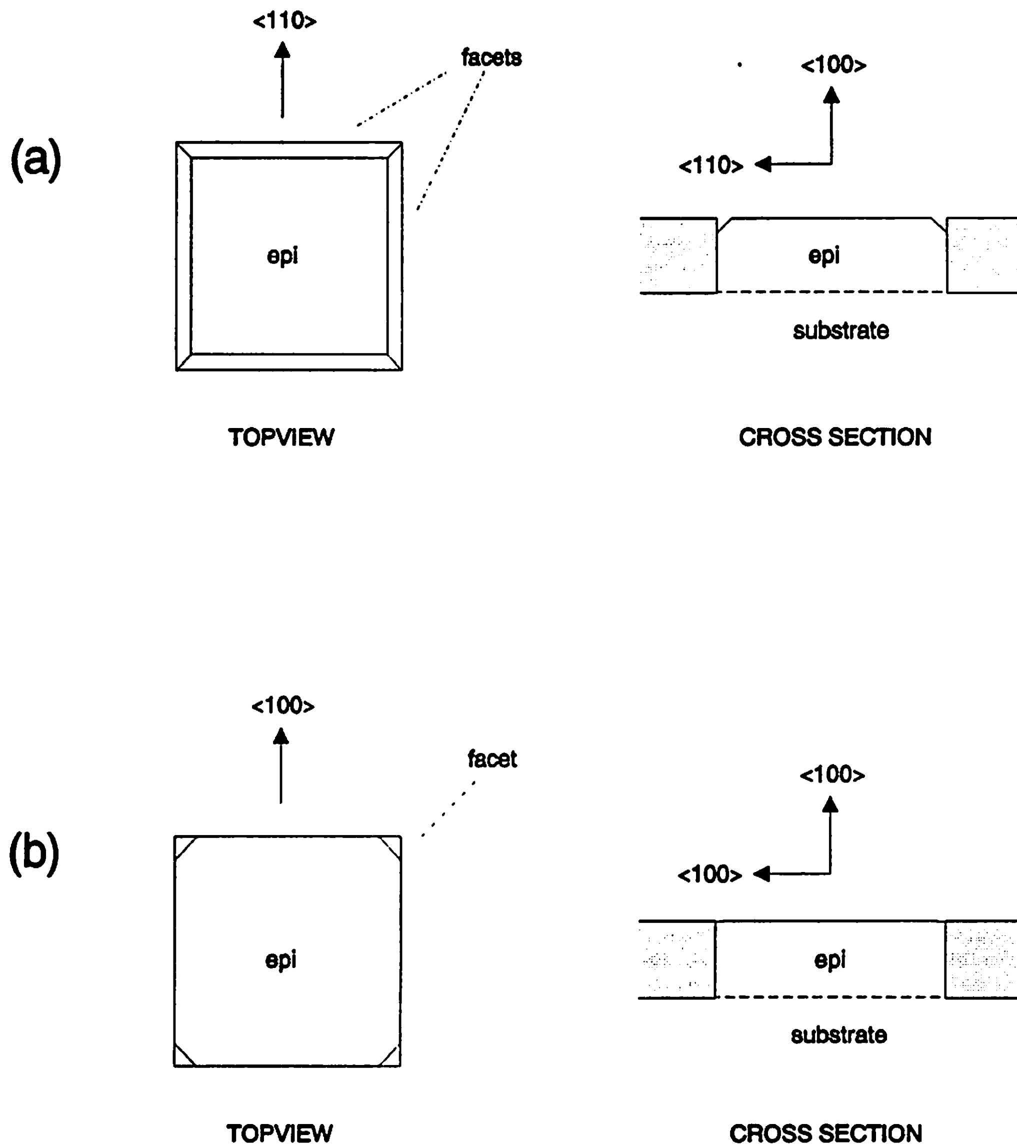
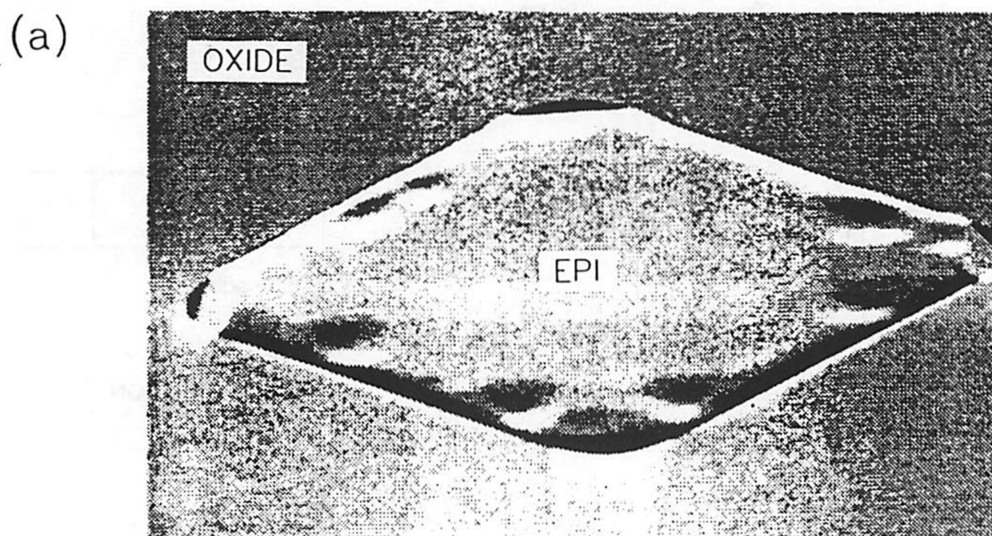


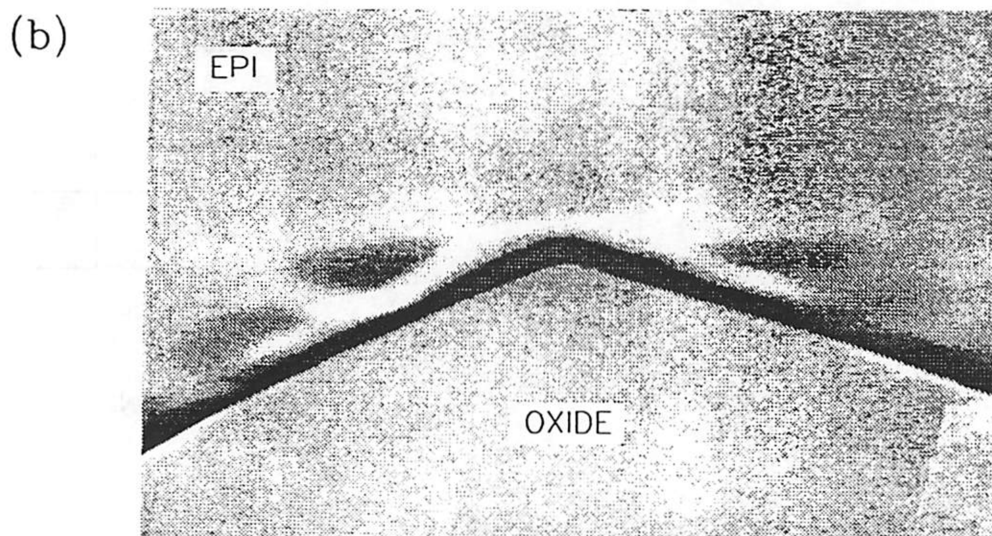
Fig. 3.28 SEM pictures of a 1 μm thick epitaxy layer with the oxide sidewalls oriented parallel to {100}. Facets form in the outside corners (a), but not in an inside corner (b).

(a)



10 microns

(b)



1 micron

Fig. 3.29 TEM cross section shown in (a) was prepared by J. C. Lou, revealing defect free epitaxy and H_2 bake induced oxide undercut. The assumption that silicon is removed uniformly along the substrate during the H_2 bake is shown in (b), and is contrasted with the hypothesis that silicon removal is enhanced by the proximity of oxide in (c).

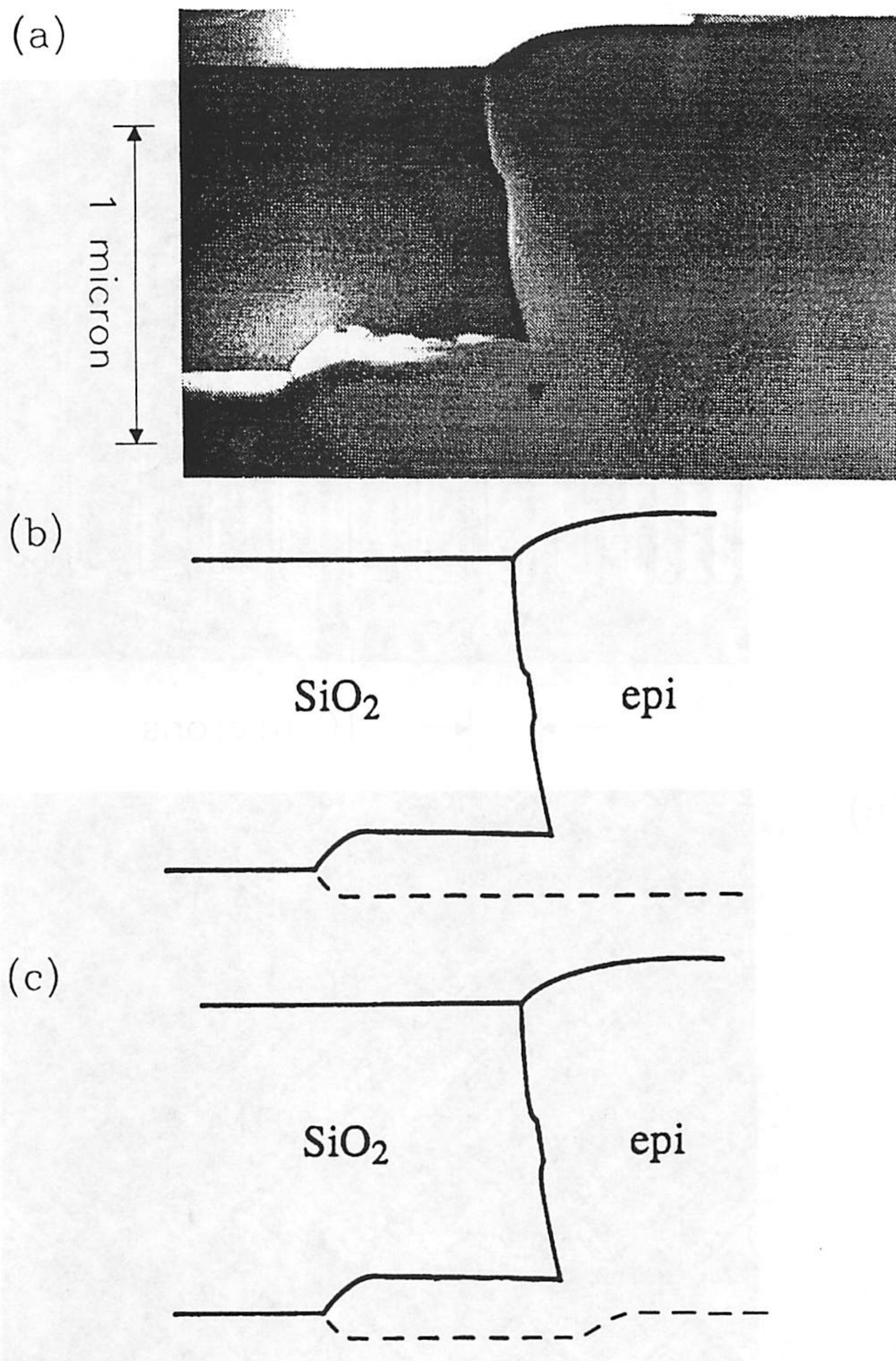


Fig. 3.30 Stripes of selectively grown epitaxy after removal of the masking oxide. The epitaxial thickness is about 0.8 μm. In (a) the sidewalls are oriented along {110}, and in (b) they are oriented along {100}.

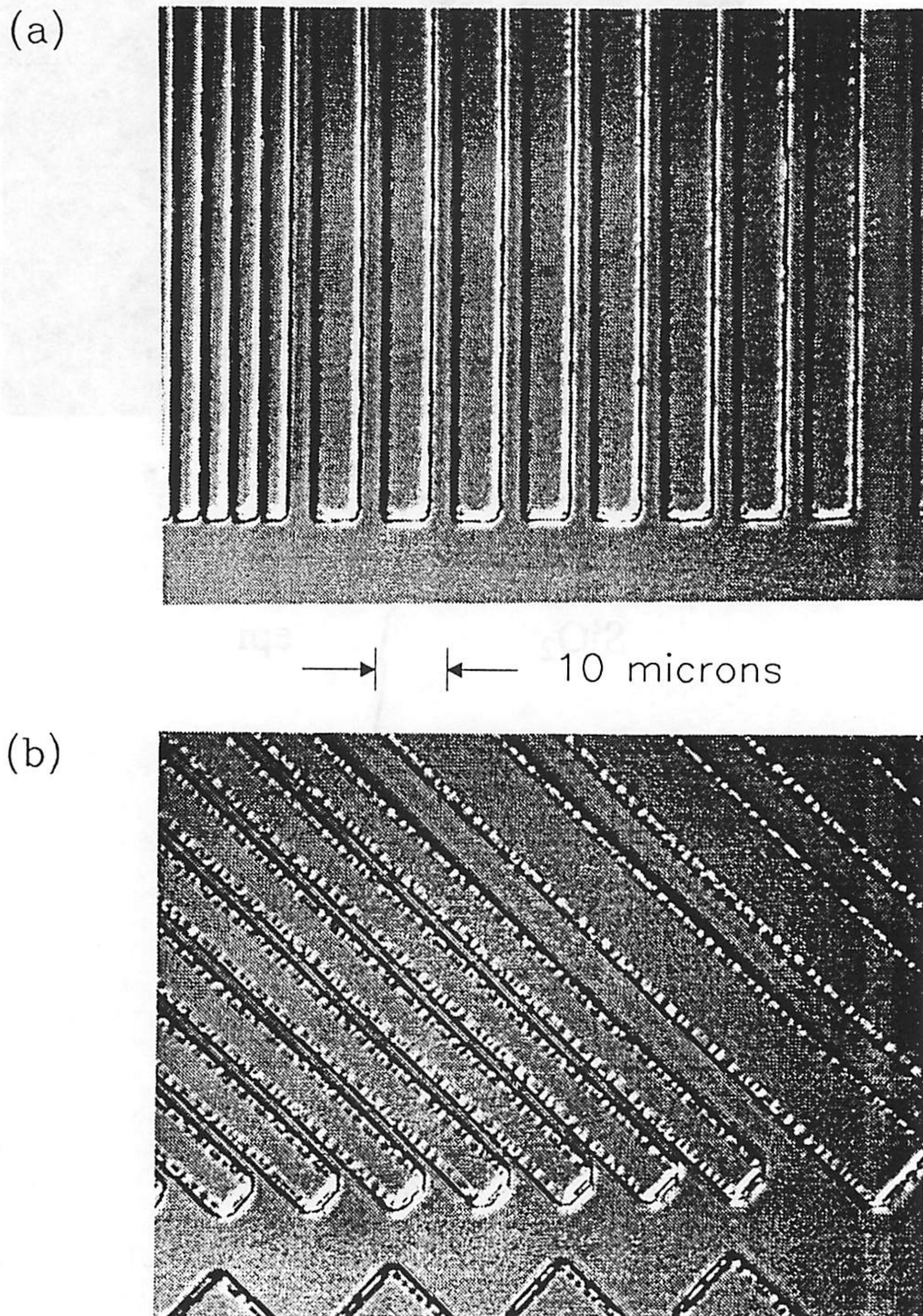
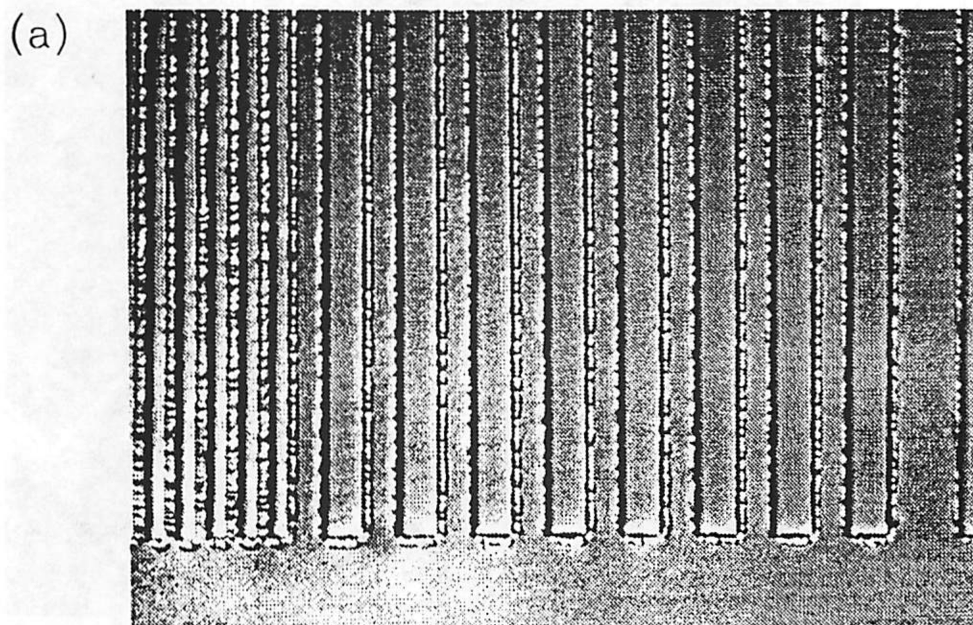


Fig. 3.31 The same sample shown in Fig. 3.30 after a dilute Schimmel etch was used to remove about 0.5 μm of the silicon, decorating defects along the sides of the patterns. In (a) the sidewalls are oriented along {110}, in (b) they are oriented 15° away from {110}, and in (c) they are oriented along {100}.

(a)



→| |← 10 microns

(b)

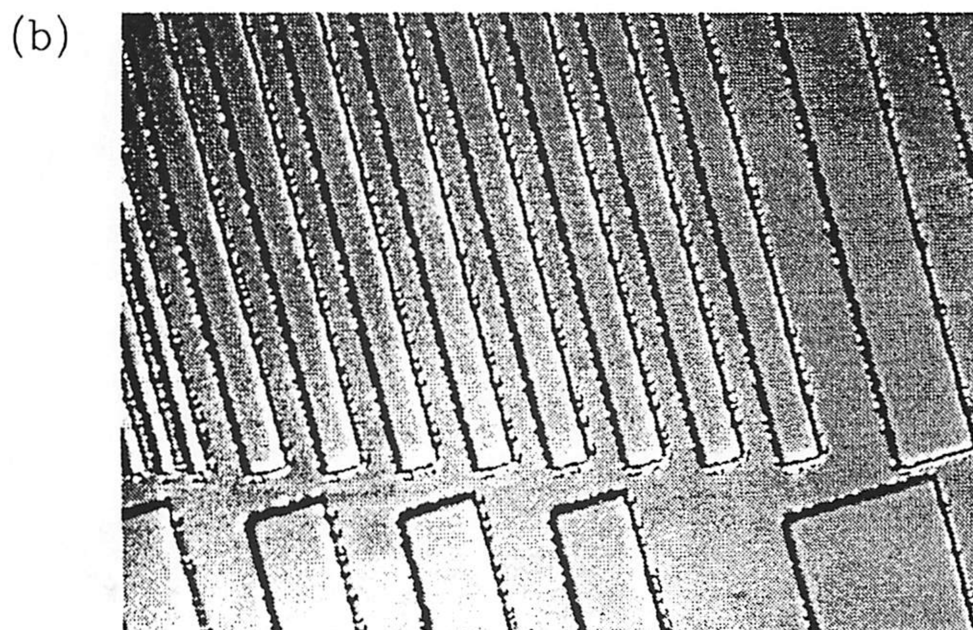
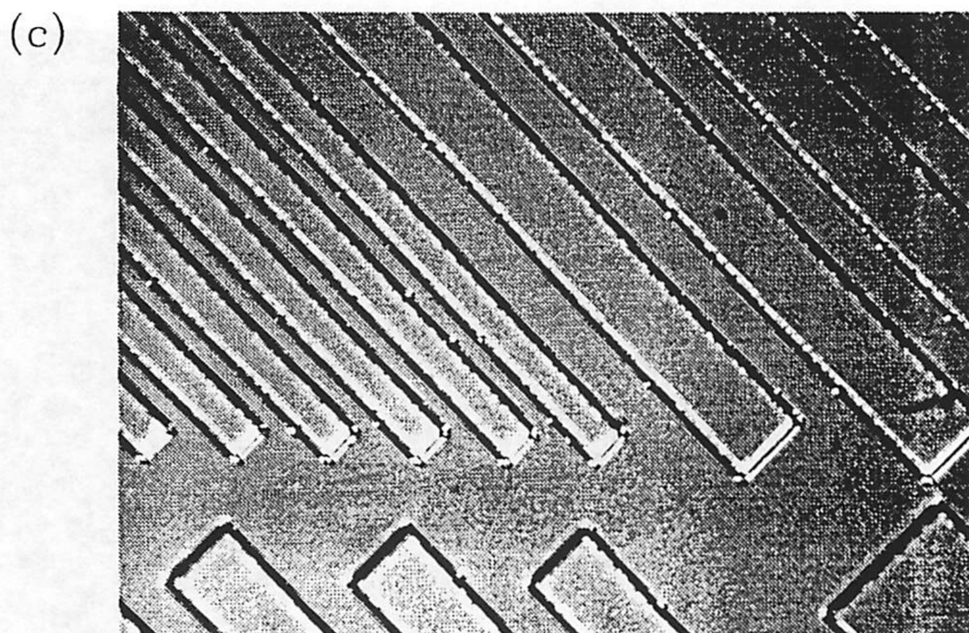


Fig. 3.31 (cont.)



→| |← 10 microns

Fig. 3.32 SUPREM simulation of the impurity profiles that result from the Modified EECS 143 Process. The profile under the gate is shown in (a), and the source/drain profile is shown in (b).

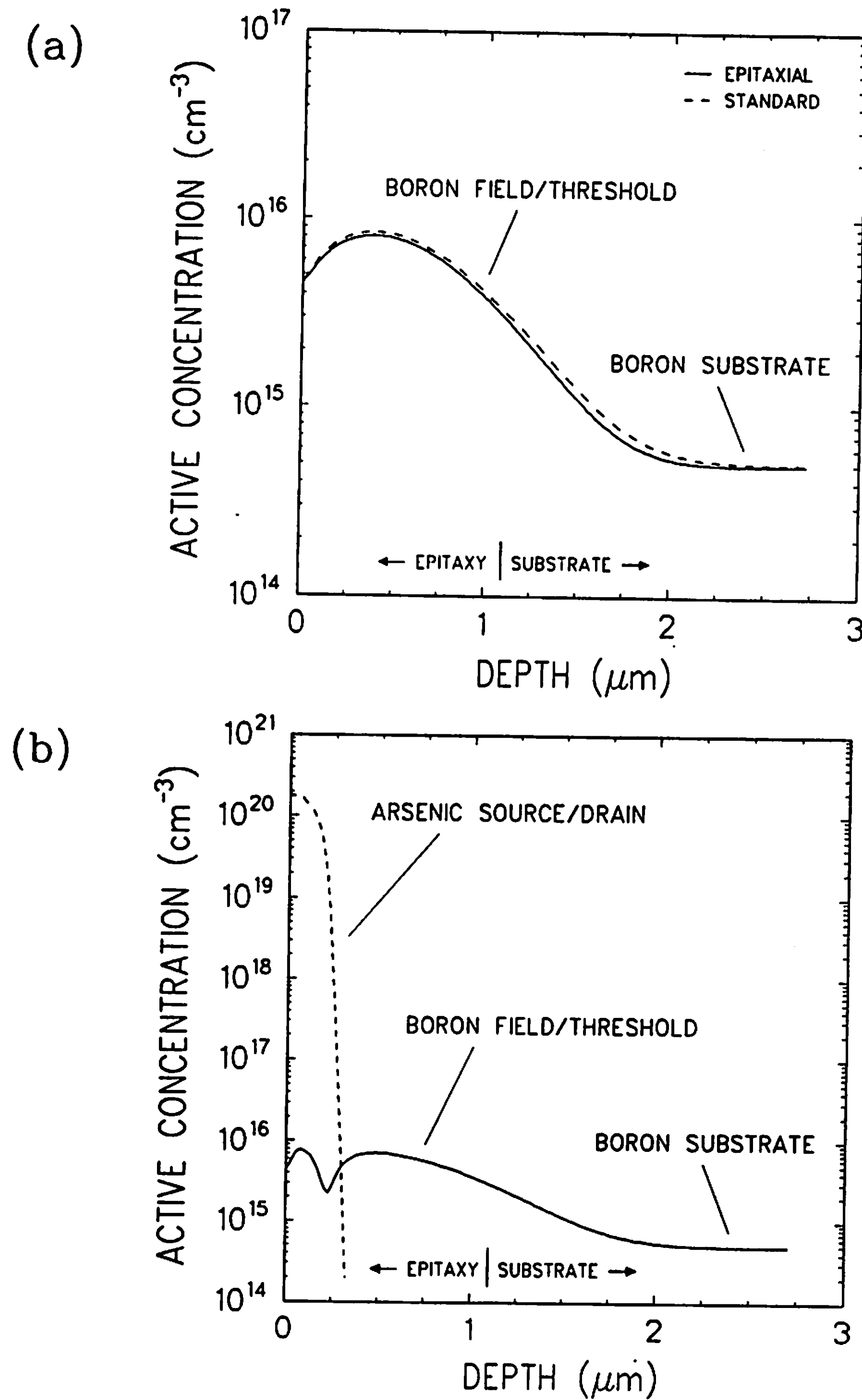


Fig. 3.33 Comparison of the drain current characteristics of a 100/100 μm MOS transistor fabricated on an epitaxial wafer versus one fabricated on a standard (non-epitaxial) wafer.

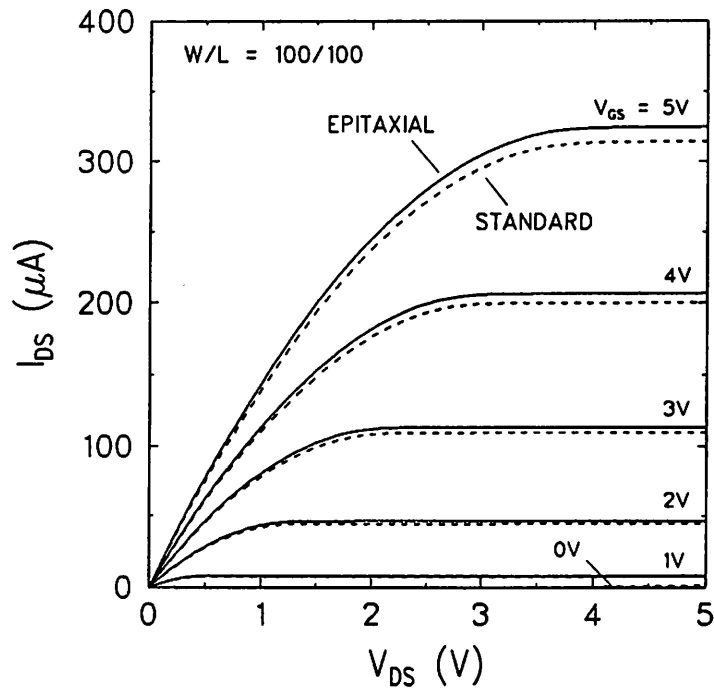


Fig. 3.34 Comparison of the drain current characteristic in the linear region for a 100/100/ MOS transistor fabricated on an epitaxial versus a standard wafer is shown in (a). The mobility versus V_{GS} characteristics extracted from (a) are compared in (b).

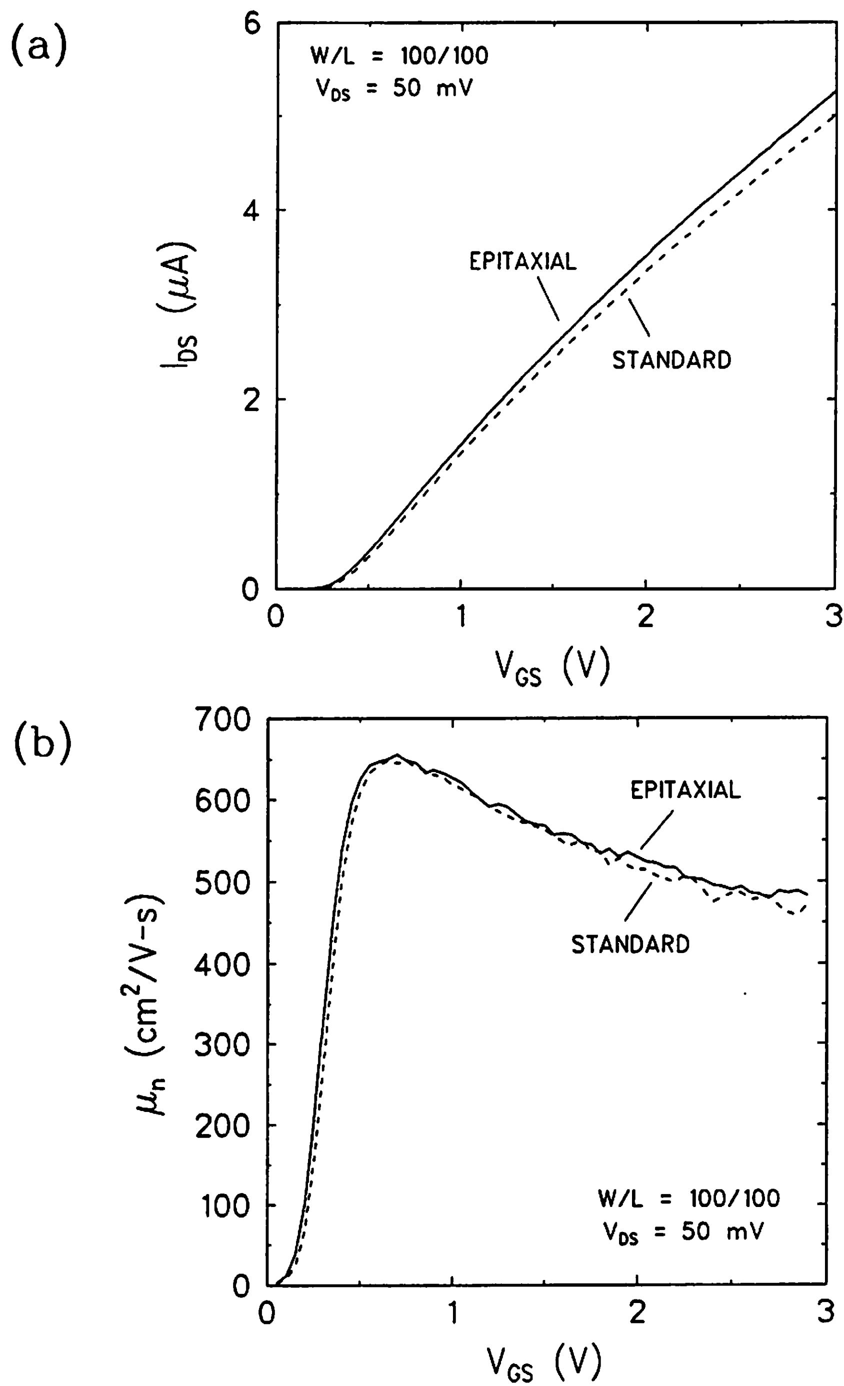


Fig. 3.35 Comparison of subthreshold drain current characteristic for a 100/100 MOS transistor fabricated on an epitaxial versus a standard wafer is shown in (a). The capacitance versus voltage characteristics for a large gate oxide capacitor are compared in (b).

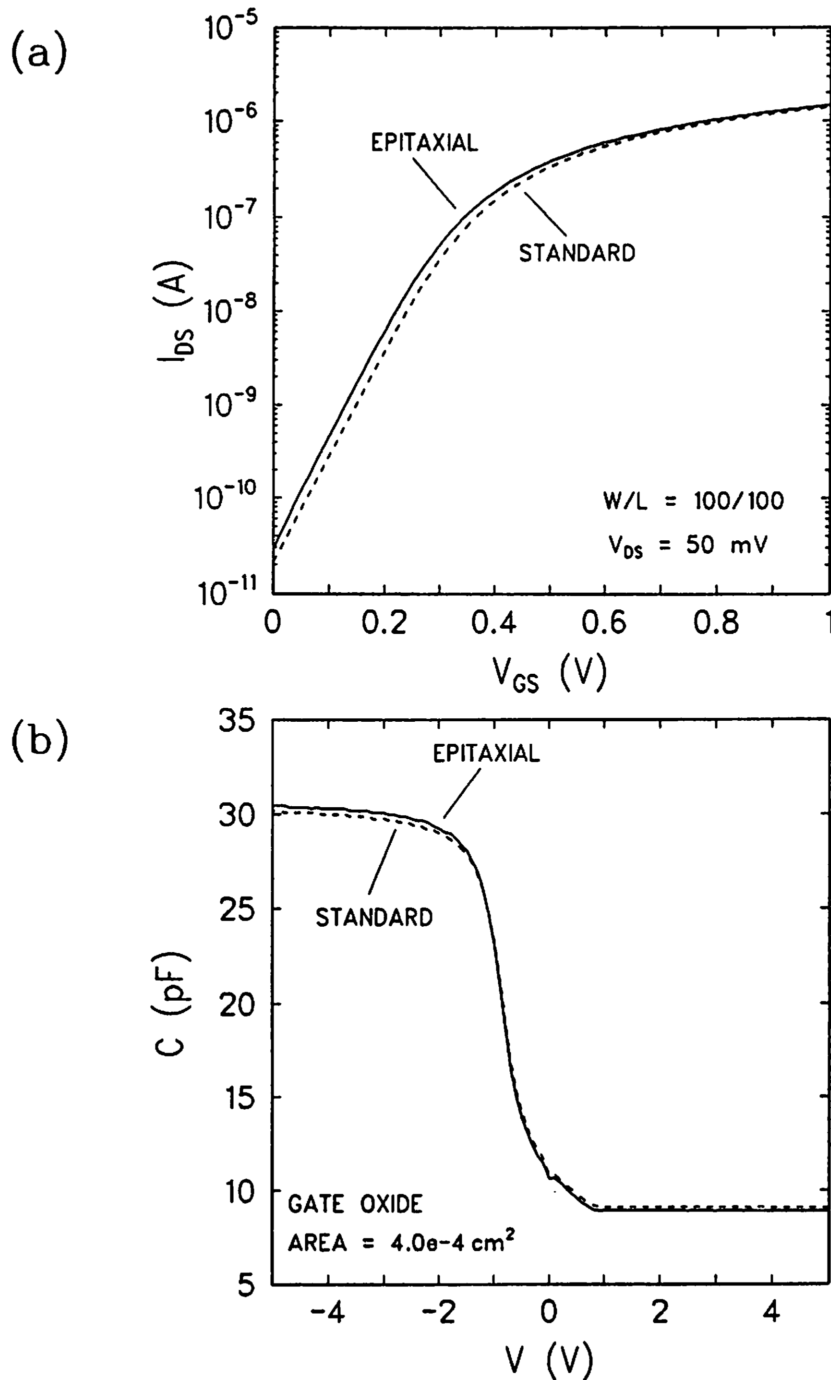


Fig. 3.36 Comparison of the source/drain junction capacitance versus voltage characteristics for a large source/drain junction capacitor fabricated on an epitaxial versus a standard wafer is shown in (a). The dopant profiles extracted from the characteristics in (a) are shown in (b) together with the SUPREM simulated dopant profile.

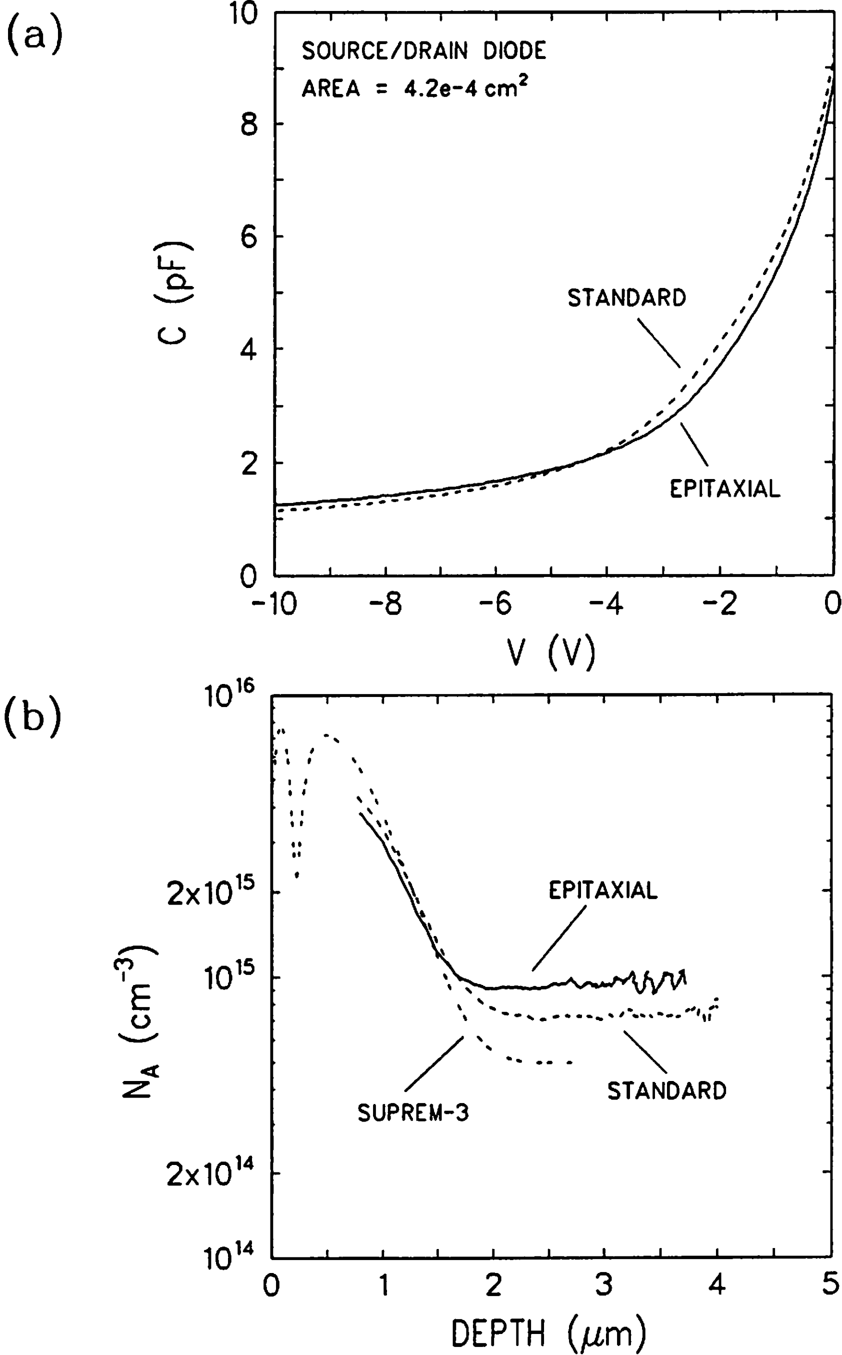


Fig. 3.37 Comparison of the forward-biased current characteristics of source/drain junctions fabricated on an epitaxial versus a standard wafer.

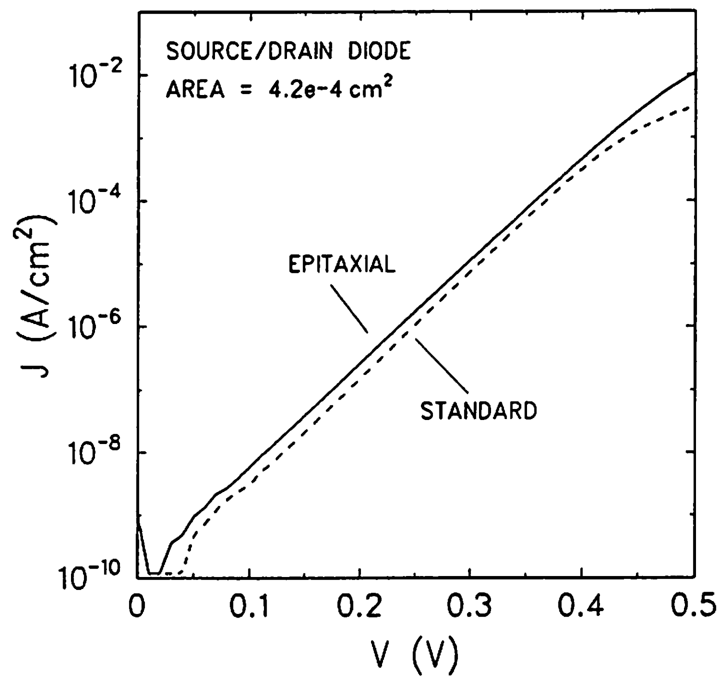


Fig. 3.38 Comparison of the reverse-biased current characteristics of source/drain junctions fabricated on an epitaxial versus a standard wafer. The effective lifetime profiles extracted from the data in (a) are compared in (b) and (c).

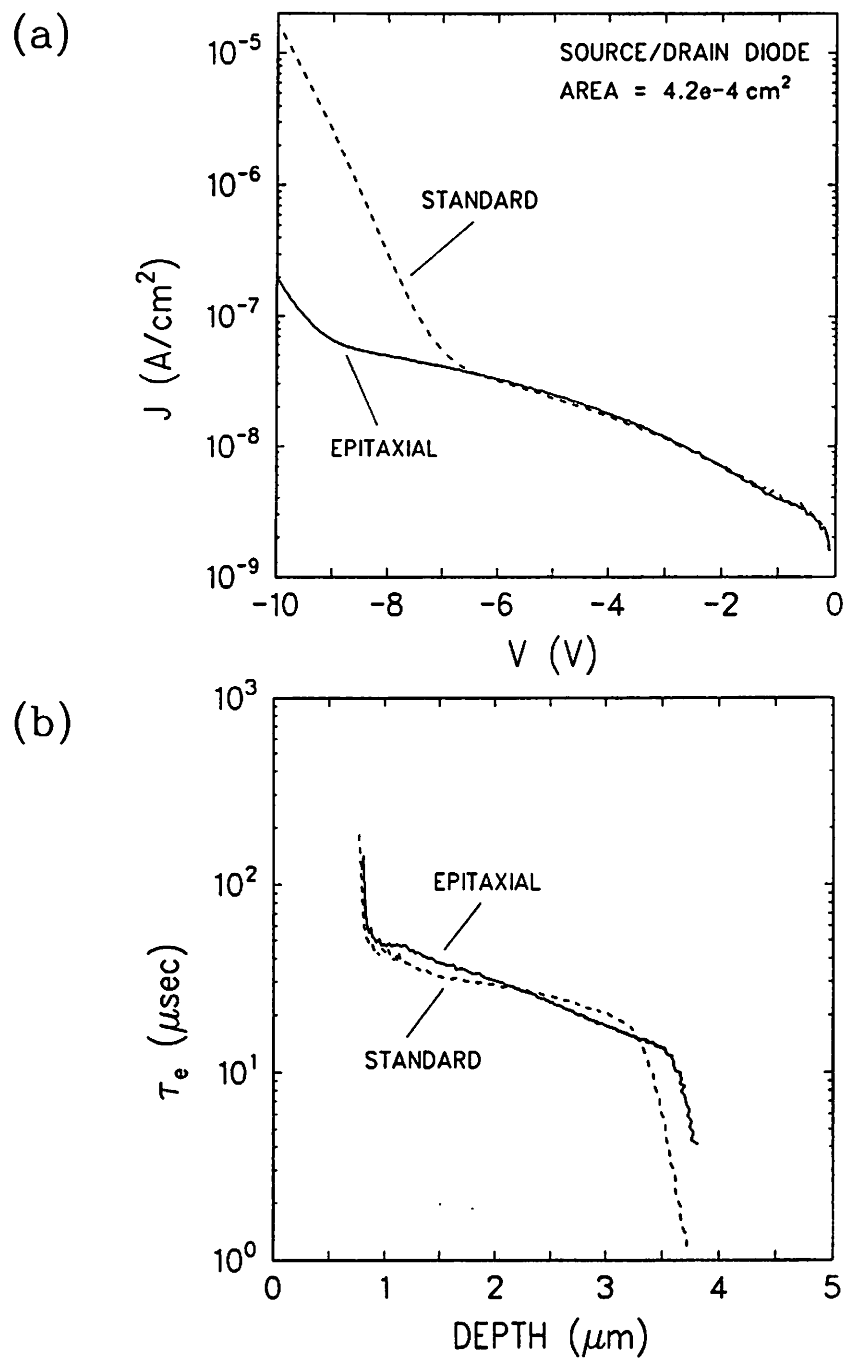
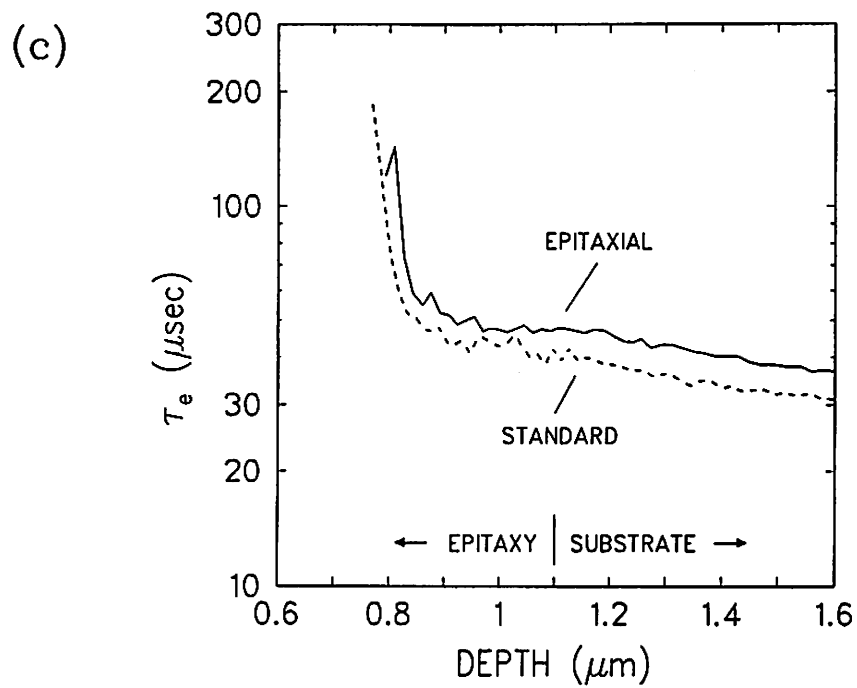


Fig. 3.38 (cont.)



Chapter 4
Wafer Preparation for Selective Epitaxy†

Selective epitaxy is becoming an increasingly important means by which compact structures can be made for the dense integrated circuits that will be necessary in the future [1]. These compact structures often require that abrupt and shallow junctions be maintained, which precludes the utilization of high temperatures during the epitaxial step. Further complication for the case of selective epitaxial deposition is provided by the sensitivity of the epitaxial quality to the condition of the oxide sidewalls that delineate the selective deposition areas.

This chapter addresses the specific problem of generating an oxide-free substrate surface for selective epitaxy applications without using a higher temperature than 900° C during the H_2 bake. The effect of the H_2 bake on the formation of an undercut along the bottom of oxide sidewall is examined first. It is determined that the amount of surface oxide must be reduced to a minimum before the wafers are loaded into the reactor. The second half of the chapter investigates the use of HF vapor etching to accomplish this task.

4.1 Hydrogen Baking Limitations

To achieve high quality epitaxial silicon it is necessary to start the deposition on a clean single-crystal silicon surface [2]. This is not an easy task because bare silicon surfaces are highly reactive. Many undesired impurities, such as metals, carbon, and oxygen,

† The work presented in this chapter was performed together with J. C. Lou and was published in the August 1990 issue of IEEE Transactions on Semiconductor Manufacturing.

are easily adsorbed. The most pervasive contamination is oxygen; a layer of 1-2 nm thick native oxide will form on any bare silicon surface exposed to air. Chemical oxides of similar thickness are also formed as a part of cleaning procedures such as the RCA [3]. Such oxides passivate the reactive silicon surface, reducing the accumulation of other impurities like metals and carbon [4]. Thin oxide removal is conventionally performed inside the epitaxial reactor by heating the wafers in the presence of H_2 before starting the deposition. This H_2 bake generally requires a temperature above 1000° C, a temperature not compatible with manufacturing compact structures with abrupt junctions.

Selective applications introduce the additional problem of an *undercut* forming along the substrate interface of the isolation oxide during the H_2 bake [5]. An example of an oxide undercut resulting from a 1000° C H_2 bake is shown in Fig. 4.1. The effective duration of the bake, including temperature ramps, was about 20 minutes and has resulted in the formation of an 0.17 μm deep undercut. From our experience, the presence of an oxide undercut is associated with defects and nonuninform growth along the oxide sidewalls. These problems are especially evident when films are grown thicker than the masking oxide, as in the case of epitaxial overgrowth.

Lower temperatures during the epitaxial process decrease both the dopant diffusion and undercut rates, but with the reduction in temperature the process becomes more sensitive to disruption by background impurities inside the reactor, such as O_2 and H_2O. The H_2 bake step, and the initiation of growth, are particularly sensitive, and generally benefit from using the highest possible temperature. Using high temperatures counteracts the presence of the background because of the increased rates of removal. As discussed in chapter 2, thermodynamics can be used to obtain a worst case limit by by calculating the dividing line between between conditions that result in a clean silicon surface or one covered by oxide [6]. Using available thermodynamic constants [7], the result is a

that the amount of H_2O allowed in the H_2 ambient decreases from 0.9 ppm at 1150° C to 0.07 ppm at 950° C.

4.1.1 Oxide Removal Efficiency

The decrease in oxide removal efficiency with lower temperatures is demonstrated by the experiments summarized in Fig. 4.2. The SIMS profiles in Fig. 4.2(a) through 4.2(d) reveal an increase in the interfacial oxide peak as the bake temperature is reduced from 1050° C to 900° C, while the deposition temperature was held constant at 850° C. The flow rate and pressure of the H_2 during each of the bakes was 8 slpm and 5.6 torr. We use a Matheson 8373 Pd diffusion cell to purify the hydrogen gas source. This purifier is mounted just before the hydrogen mass flow controller to minimize contamination injected into the reactor from all prior sources. Accurately measuring the low background concentration of water inside the reactor during the H_2 bake is difficult. A lower limit estimate is provided by the minimum temperature of 1050° C needed to completely eliminate the oxide peak which, according to the thermodynamic relationship for maximum H_2O content, indicates a H_2O background concentration of 0.2 ppm.

Epitaxial layers in Fig. 4.2 that were deposited at 850° C after bakes from 1050° C to 950° C do not have any visual defects unless revealed with a defect etch. Removing the epitaxial layers down to the interface with a dilute Schimmel etch [8] reveals a dislocation pit density of about 30 cm^{-2} at 950° C, versus essentially zero for bakes at 1000° C and 1050° C. When the bake temperature is reduced to 900° C the deposited film is very rough, but continuous and single-crystalline. Since the deposition is highly selective, the 900° C bake result suggests a "patchy" interfacial oxide that has been laterally overgrown by epitaxial deposition from areas where the silicon was exposed during the bake. For higher bake temperatures these patches of oxide are smaller and/or fewer in number, and

do not always result in visible surface defects. Visual inspection in this case is not as sensitive as a SIMS profile through the interface.

A pre-epitaxial surface consisting of oxide patches agrees with the observations of Ghidini and Smith [9] investigating the interaction of gaseous H_2O with bare silicon surfaces. Their results show that H_2O can both oxidize and etch silicon, and that the removal of oxide occurs by solid silicon reduction. The proposed set of reactions can be written as:

$$2H_2O + Si \rightarrow SiO_2 + 2H_2 \quad (1)$$

$$H_2O + Si \rightarrow SiO\uparrow + H_2 \quad (2)$$

$$Si + SiO_2 \xrightarrow{H_2} 2SiO\uparrow \quad (3)$$

An activation energy calculation for the equilibrium pressure of SiO according to reaction (3) results in 3.3 eV, while a calculation for the equilibrium H_2O pressure by either reaction (1) or (2) gives an activation energy of 2.0 eV [7]. Ghidini and Smith experimentally measured the maximum H_2O pressure that maintains an oxide-free silicon surface; it decreases from 10^{-4} torr at 1050° C to $5 \cdot 10^{-6}$ torr at 900° C, corresponding to an activation energy of 3.0 eV. This indicates that the most likely rate limiting step for ensuring oxide-free surfaces is the removal of the oxide by reaction (3).

The implication for epitaxy from these observations is to quantify the maximum background pressure of H_2O allowed inside a reactor for a given temperature to maintain oxide-free silicon surfaces during the H_2 bake. These pressures for H_2O are also lower than those for O_2 by about an order of magnitude [10]. The high sensitivity to H_2O, together with the ability of H_2O to adsorb on internal surfaces of the reactor if opened to air, makes H_2O a major concern for low temperature epitaxy. Once adsorbed, H_2O will

evaporate at a rate determined by the temperature of the surface, and can be present for long periods of time in systems that otherwise have no detectable external leaks. The desorbing H_2O mixes with the source gas, and the background pressure will depend on the relative rates of desorption and source gas flow. Therefore, background contamination by adsorbed H_2O, unlike source gas contamination, is not reduced by decreasing the operating pressure, but must instead be controlled by designing the reactor to minimize water adsorption, or by increasing the total flow through the system. In our case, flow rate experiments indicate that the background water concentration during the bake results from sources inside the reactor and not from the injected hydrogen.

4.1.2 Oxide Undercut

For selective epitaxy, reaction (3) has also been proposed by Liu et. al. [11] to cause isolation oxide undercut. It is reported that H_2 is necessary for the reaction to proceed, and the proposed mechanism involves H_2 as a catalyst. Their measured undercutting rate decreased from 850 nm/min at 1150° C to 100 nm/min at 1050 ° C, corresponding to an activation energy of 3.2 eV. Extrapolating these results to a 900° C H_2 bake, the rate is reduced to only 2 nm/min. This strong temperature dependence is advantageous for minimizing the undercut resulting from the H_2 bake step, but, since it appears from our previous discussion that the same reaction is also involved in the removal of oxide, there will be a similar reduction in the rate at which native oxide can be removed.

According to the mechanism described by reaction (3), the native oxide removal would start at defects, such as "pinholes", and, then, proceed laterally at the same rate as the oxide undercut forms. Completely removing a given native oxide will, therefore, give the same amount of undercut, independent of temperature. The consequence for selective

epitaxy is that an H_2 bake cannot be used to remove more than a small amount of oxide if the formation of an undercut is to be avoided. If the removal is incomplete, the remaining oxide patches can cause defects. Methods that allow wafers to be loaded into the reactor with a minimum of oxide are necessary, unless other methods, such as a plasma clean [12], are incorporated into the reactor. An HF dip can remove any oxide present on the wafers, but it is well known that exposure to aqueous HF results in surfaces highly attractive to heavy metals or hydrocarbons [13]. It is also very difficult to remove the wafers from the HF solution without contaminating the surfaces. A final rinse can add further contamination, both from the water itself, and the surrounding air. Rinsing in water also removes some of the adsorbed fluorine species that otherwise may be able to reduce the rate of native oxide regrowth [14]. We have, therefore, chosen to investigate the exposure to gaseous HF as an alternative to aqueous HF for the removal of oxides on pre-epitaxial substrates.

4.2 HF Vapor Etch Characterization

Reactors for anhydrous HF exposure are commercially available [15, 16], but a simpler method was chosen instead since our objective is a preliminary study of the effectiveness of an HF vapor treatment. Instead of anhydrous HF, the experimental method uses the vapor above a room temperature solution of HF in a plastic beaker. The size of the beaker is chosen so that the the perimeter of the wafer can rest securely on the rim. Vapor treatment is accomplished by using a vacuum wand to hold wafers face down on the rim of the beaker. Thermally oxidized wafers were used by J. Liu to characterize the etch rates by measuring the amount of removed oxide after each exposure. The etch results for 3 different concentrations of H_2O:49%HF are shown in Fig. 4.3. The etch rate

decreases with dilution of the aqueous HF solution; for 49%HF it is 106 nm/min, decreasing to 32 nm/min for a 1:2 mixture, and 16 nm/min for a 1:1 mixture.

A set of reactions has been proposed by Novak and Thompson[15] for the vapor etching of SiO_2:

$$SiO_2 + 2H_2O \rightarrow Si(OH)_4 \quad (4)$$

$$Si(OH)_4 + 4HF \rightarrow SiF_4\uparrow + 4H_2O \quad (5)$$

According to this set of reactions, H_2O is both a reactant and a product. As a reactant H_2O is necessary to initiate the etching, but as a product it can also inhibit it. In fact, the appearance of water droplets was observed on oxide-covered wafer surfaces exposed for long times to HF vapor when measuring the etch rates for Fig. 4.3. Scattered light from a collimated beam of light can reveal the presence of even submicroscopic water droplets resulting from short exposures. By measuring the time it takes the water droplets to evaporate after exposure to HF vapor, estimate is obtained for the amount of water on the wafer surface. The water evaporation time after each exposure is plotted in Fig. 4.4 versus the amount of oxide removed by the same exposure. There is a direct relationship between the amount of oxide removed and the evaporation time for both concentrations of HF, suggesting that the water forming on the wafer surfaces is indeed a result of the oxide etching as predicted by reaction (5).

To avoid the formation of water droplets one might consider heating the wafers before exposing them to the HF vapor. The result of such an experiment is also shown in Fig. 4.3. In this experiment an IR (infra-red) lamp was used to heat the wafer for 10 seconds before exposure to the HF vapor. The result is an induction period during which there is no etching, and then, once etching starts, the etching behavior is similar to that of

the unheated wafer, including droplet formation. This induction effect was observed in all of our attempts at preheating wafers. The initiation of etching, as predicted by reaction (4), cannot occur without some adsorbed H_2O on the surface. Preheating the wafers with the IR lamp apparently desorbs enough H_2O from the wafer surface that significant etching does not occur until the wafer cools down, allowing H_2O to adsorb again.

4.3 Selective Epitaxy Results

Our standard pre-epitaxial clean includes two piranha treatments. The exposed silicon areas end up with an effective chemical oxide thickness of 2.0 nm according to ellipsometer measurements (assuming 1.5 for the index of refraction). This clean has the advantage of not exposing a bare Si surface to water during the final rinse, but it limits our ability to do low-temperature epitaxial deposition because of the oxide that needs to be removed inside the reactor. From our prior characterization the 5 second exposure to the vapor above a 1:2 mixture was selected. About 2.5 nm of thermal oxide is removed by this etch. The chemical oxide in patterned areas should etch faster since it is more porous and contains more moisture [15].

When using HF vapor exposure it is important to avoid the formation of water droplets on oxide covered areas due to overetching. Water droplets on the surface can dissolve impurities in the air that leave residues as sites for unwanted nucleation on the oxide. An example of such nucleation is shown in Fig. 4.5(a). The sample was etched for 45 seconds over a 1:2 mixture. Nucleation of silicon on the oxide separating the epitaxial areas is in the distinctive circular shape of a droplet. There is also considerable roughness of the epitaxial film along the oxide edges.

Using our standard pre-epitaxial clean together with the 5 second 1:2

H_2O:49%HF vapor etch, we are able to deposit defect-free epitaxial films at 850° C after an H_2 bake at only 900° C. A selectively grown film using this process is shown in Fig. 4.5(b). There are no visible defects in the epitaxial areas, and the edges are smooth. The edge quality is especially evident in the smooth overgrowth achieved for the narrow lines. Oxide nucleation is also not present, indicating that impurities on the oxide areas can be avoided for HF treatments that result in a minimal amount of surface moisture. SIMS analysis gives further indication of the effectiveness of the HF vapor treatment. As shown in Fig. 4.6, there is no evidence of an oxygen peak at the substrate interface for the sample that received an HF vapor treatment. Using the HF vapor treatment and a low temperature bake complete removal of interfacial oxide is accomplished, absence of oxide undercut, and lack of oxide nucleation.

Because of these improvements to the process it is possible to grow thick epitaxial films that can grow laterally over the masking oxide without the formation of defects. A TEM cross section of such an epitaxial film is shown in Fig. 4.7, where a 3.2 μm thick film has overgrown a 0.4 μm masking oxide. Even though the sample was carefully aligned to allow high contrast imaging of any defects, no defects are found in the epitaxial layer that has seamlessly covered the masking oxide.

4.4 Summary

To make selective epitaxy possible with a minimum of undercut there must be a minimal amount of native, or chemical, oxide to remove during an H_2 bake. This constraint, together with the decreased effectiveness of H_2 baking at the reduced temperatures that minimize diffusion in compact structures, precludes the use of H_2 baking alone as the means of thin oxide removal for selective epitaxial growth. A simple HF vapor treatment

is explored for the removal of thin oxides before loading wafers into an epitaxial reactor. The vapor removal minimizes adsorption of impurities on the wafers, and reduces the rate of native oxide formation. The HF vapor treatment permits a dramatic reduction of the temperature during the hydrogen bake. For short H_2 bakes at 900° C using this treatment SIMS profiles indicate no interfacial oxide, and cross sectional TEM reveals the absence of an oxide undercut. The growth of high quality epitaxial films further demonstrates that clean single crystal silicon surfaces are obtained using the vapor treatment process.

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Fig. 4.1 Cross-section TEM prepared by J. C. Lou of a selective epitaxial layer grown at 850° C after a 1000° C H_2 bake. The epitaxy is defect-free but a 0.17 μm deep undercut has formed along the substrate interface of the 0.20 μm thick oxide during the bake.

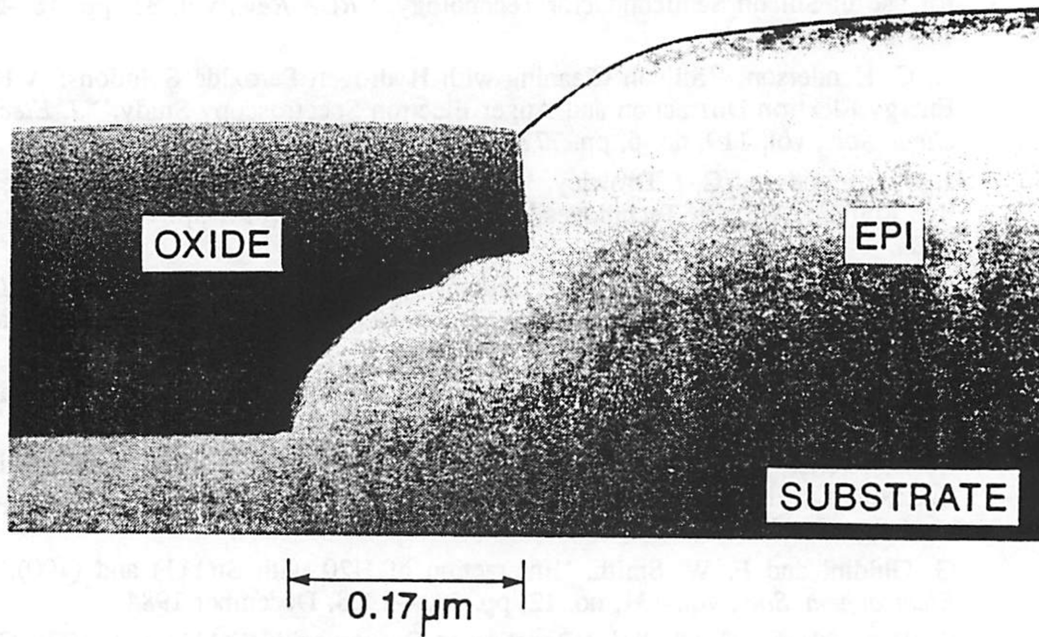


Fig. 4.2 SIMS profiles of carbon and oxygen for epitaxial films deposited at 850°C in our hot-wall reactor. For each sample the nominal baking duration was 10 minutes at the following temperatures: (a) 1050° C, (b) 1000° C, (c) 950° C, and (d) 900° C.

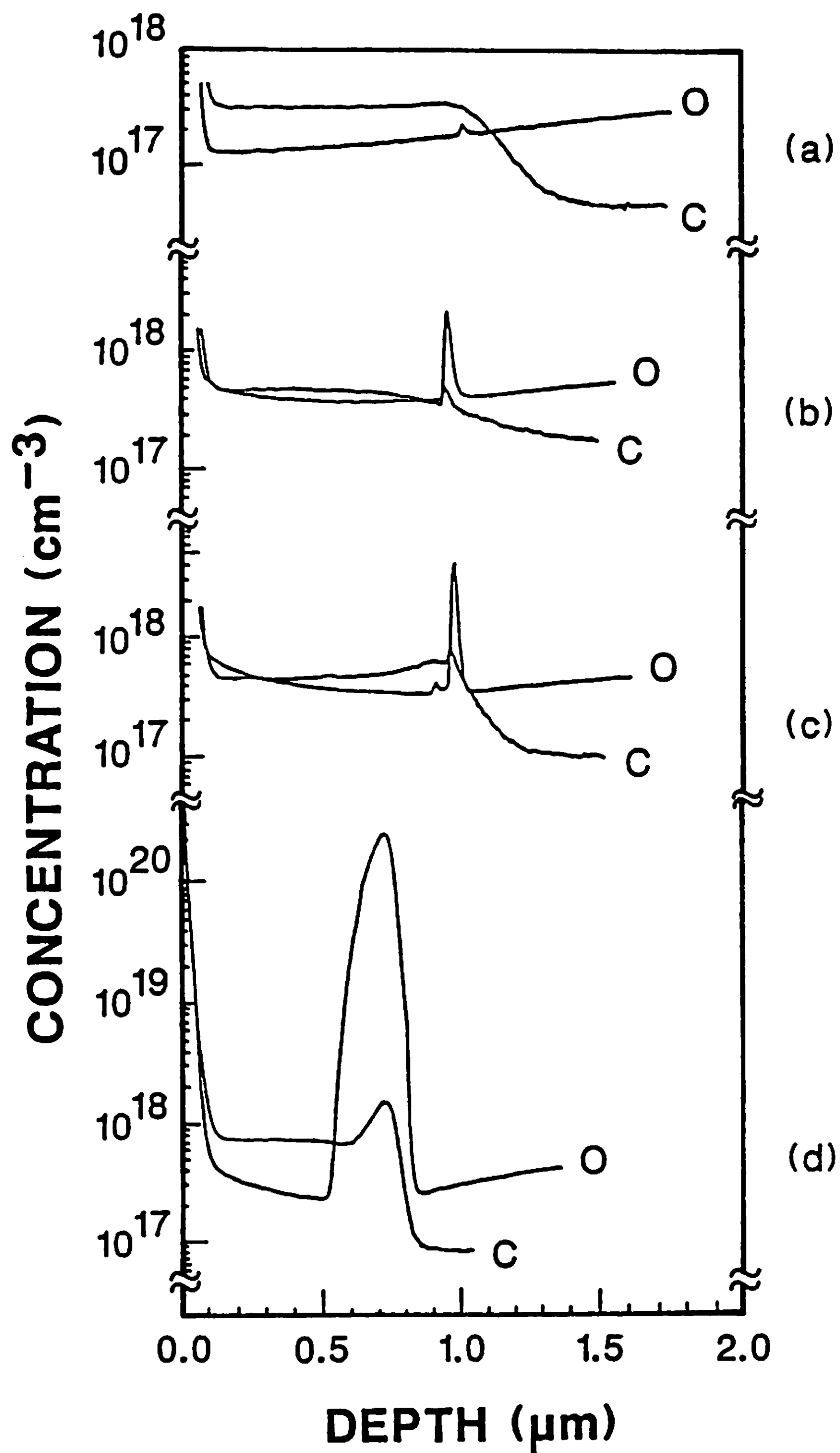


Fig. 4.3 Amount of thermal oxide removed versus exposure time to the vapor above three mixtures of H_2O:49%HF. The wafer preheated for 10 seconds with an IR lamp only starts to etch after a 50 second delay.

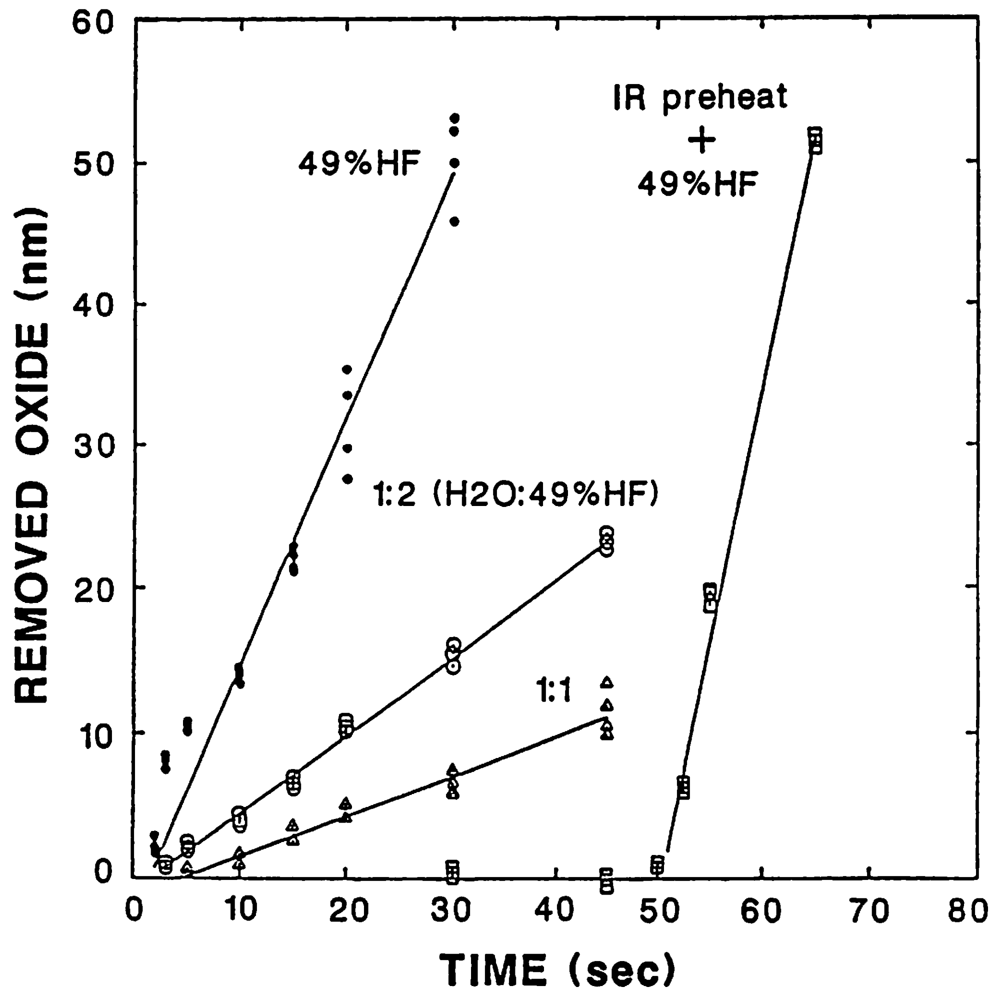


Fig. 4.4 The relationship between the amount of oxide removed and the time for accumulated water droplets to evaporate for two mixtures of H_2O and HF.

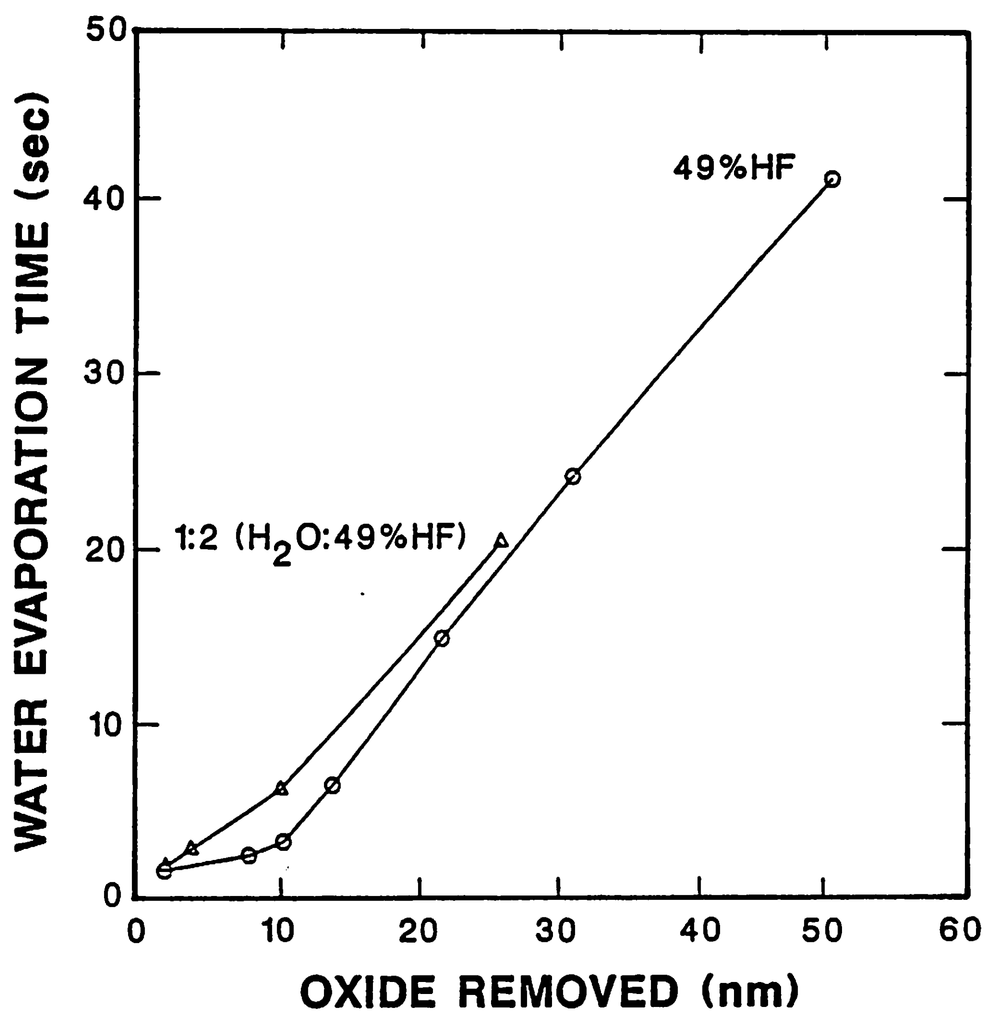


Fig. 4.5 Photomicrographs of selective epitaxy deposited at 850° C using a 900° C hydrogen bake. After the standard pre-epitaxial clean each sample was exposed to the vapor over 1:2 H_2O:49%HF for (a) 45 seconds, and (b) 5 seconds. In each case the epitaxial film is about 1.5 μm thick and the masking oxide 0.5 μm thick.

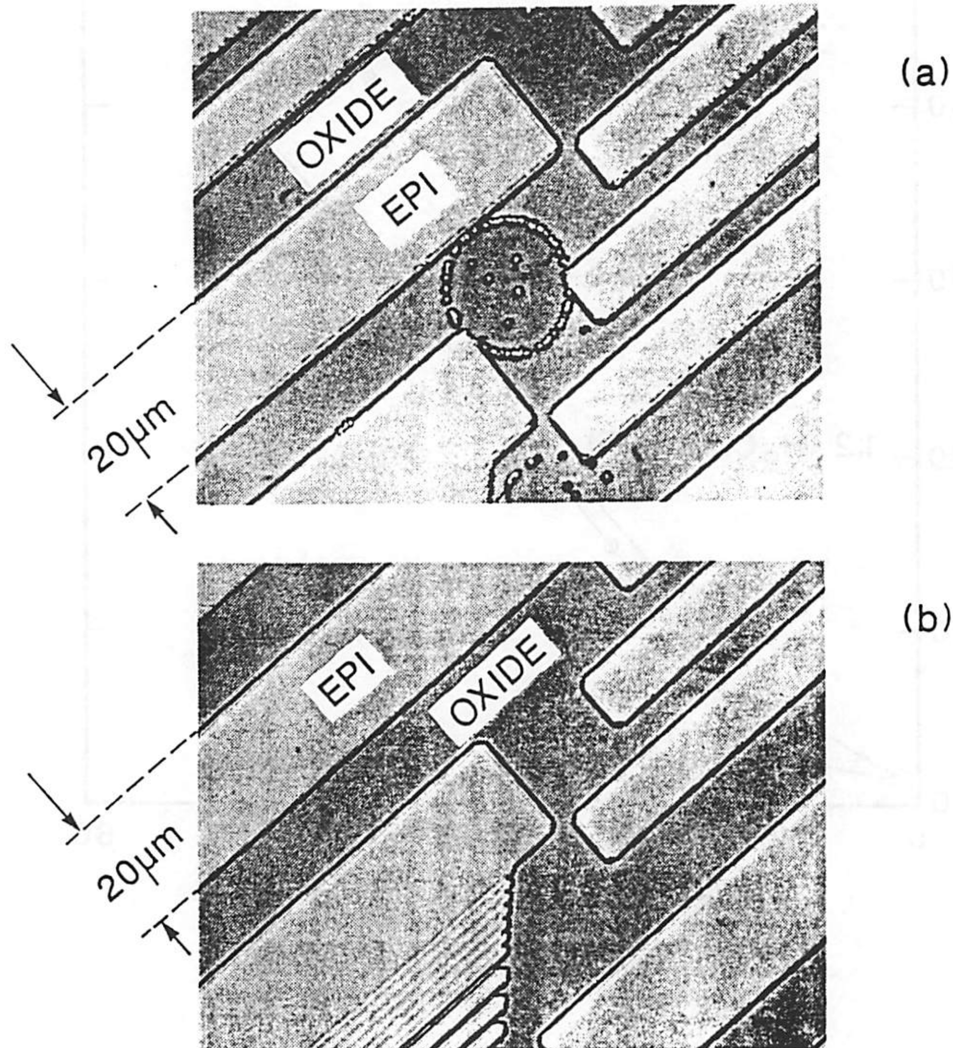


Fig. 4.6 Comparison of the SIMS profiles obtained from two wafers in an experiment where sample (a) did not receive an HF vapor treatment, and sample (b) was exposed to 5 seconds over 1:2 H_2O:49%HF. The two wafers otherwise received identical treatment. The H_2 prebake was at 900° C and the epitaxial silicon was deposited at 850° C.

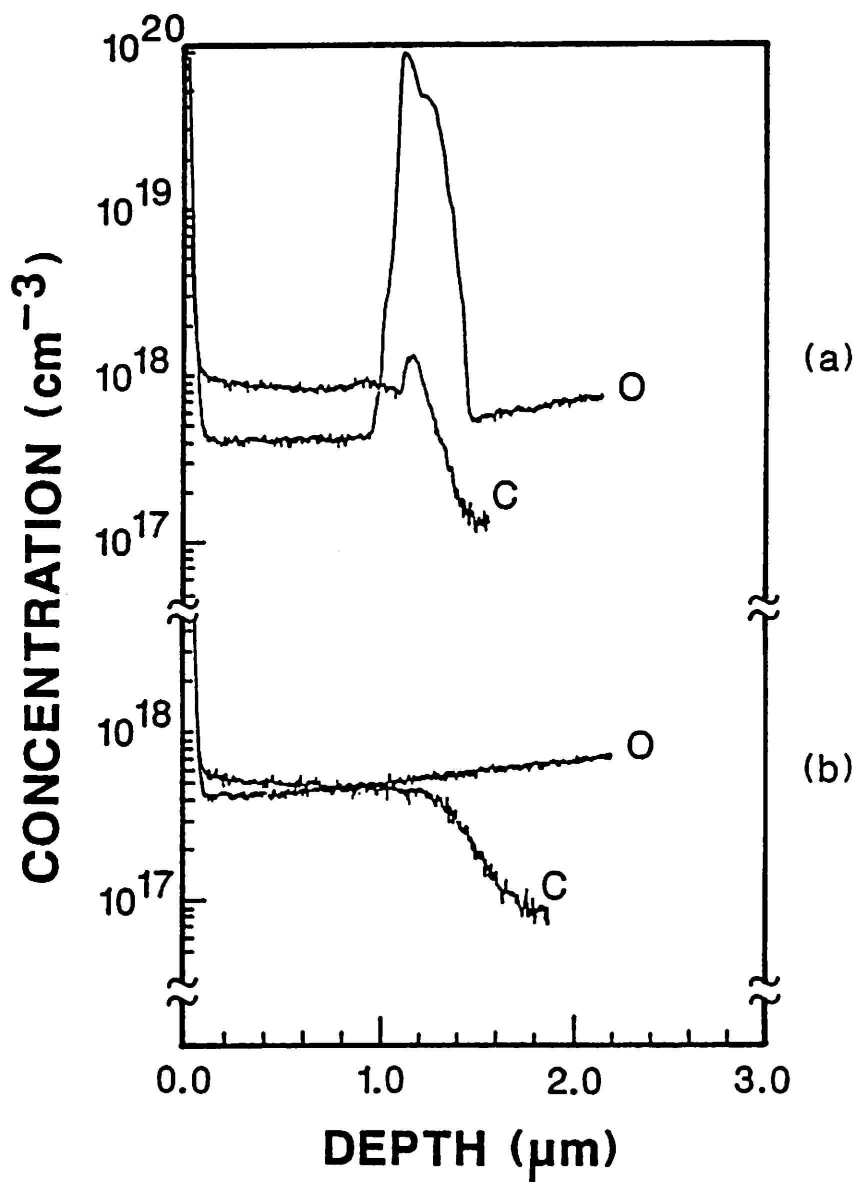
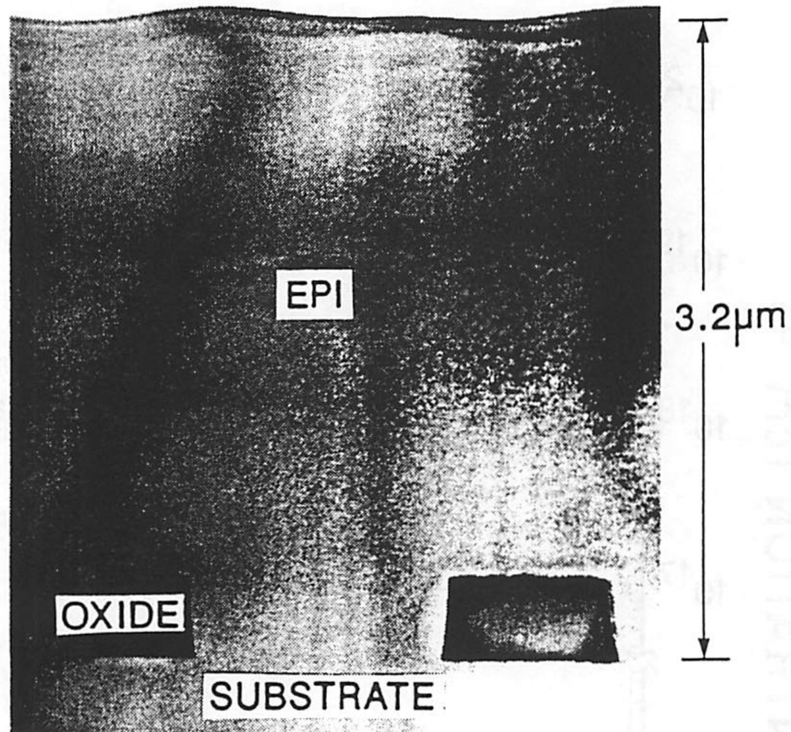


Fig. 4.7 Cross-sectional TEM of selective epitaxy grown using the same bake conditions as in Fig. 4.5(b). The overgrown oxide strips are about 0.4 μm thick and 0.9 μm wide. The epitaxial thickness is 3.2 μm.



Chapter 5
Modeling of Deposition Uniformity

As described in the previous chapter dealing with the historical perspective of hot-wall silicon epitaxy, an obstacle to the development of practical hot-wall systems has been excessive depletion and the resulting non-uniform growth. This chapter describes a physically based model for the deposition rate uniformity in our hot-wall epitaxial silicon system that predicts the amount of depletion in both the radial, and axial directions. The goal of this effort is the ability to quickly find conditions that result in uniform growth, including a larger production-sized system.

5.1 Modeling Hot-Wall Tubular Deposition Systems

The motivation to construct a physically based model of a system consists of two parts. First, system understanding is enhanced by the ability to examine the contribution of each of the physical processes to the overall system behavior. Second, extrapolation outside the realm of the original system is possible if there are no changes in the physical processes.

In order to model our hot-wall tubular system, two physical processes will be included: (1) molecular transport by convection and diffusion, and (2) chemical reactions. The interactions of these mechanisms are illustrated schematically by Fig. 5.1 for a simple system involving one gaseous species that reacts to form a solid deposit on hot surfaces. The reactants in Fig. 5.1 are transported along the axis of the tube from left to right by convection and diffusion. As a result of solid material forming on the wafers and reactor walls, the gaseous concentration of reactant decreases along the tube by an amount deter-

mined by the balance between transport and deposition rates. If the transport rate is increased relative to the deposition rate more of the reactants will be transported down the tube before being removed by deposition. The deposition rate at the front of the reactor will be reduced, and the rate at the back of the reactor will decrease less because more reactants are available.

An important feature is that the wafers are stacked perpendicularly to the axis and gas flow in order to maximize the number of wafers that can be placed inside the reactor. With such an arrangement the mass flow down the tube cannot interact strongly with the centers of the wafers. The uniformity across each wafer will, therefore, be strongly dependent on radial transport by diffusion. Unless the ratio of growth rate to radial diffusion is much less than one, the growth rate at the center will be reduced relative to the edge, as shown in the lower portion of Fig. 5.1. In most cases the radial constraint determines the design and operation of the whole system. For example, low pressure operation improves radial uniformity by simultaneously reducing the deposition rate and increasing the diffusion rate. The net effect is that a reduced growth rate is accepted in order to increase the number of wafers that can be processed per deposition cycle. Optimization of this tradeoff would maximize the number of wafers that can be processed per unit time (throughput), and is a task that can benefit from reactor modeling.

Low-pressure tubular hot-wall type reactors are presently used to deposit many different materials. There is, therefore, considerable impetus for improving the understanding and control of such reactors. Reactor models for polysilicon [1,2,3,4,5,6], silicon nitride [7], and oxide from tetraethoxysilane (TEOS) [8] have been described in the literature. None of these studies, however, has presented any data or included the actual entrance region of the reactor as a part of the model. The models published by Joshi [3] and Yeckel et. al. [5] include an entrance region, but only as an empty tube of constant

temperature. As shown in the schematic representation of our system in Fig. 5.2, the entrance region is quite complicated. Besides a rapidly changing temperature there is also a set of "baffles" that are used to reduce radiative heat loss. These baffles reduce the open cross-section of the tube, and also provide considerable surface area for deposition. The result of ignoring the end zones of the reactor is shown at the bottom of Fig. 5.2. Standard boundary conditions assuming no reaction outside the wafer region are obviously not correct, causing difficulty matching the measurement to simulation. In order to use the above boundary conditions, our modeling will extend the simulated region far enough to the extremes of the reactor that the amount of reaction outside of it can be ignored.

5.2 Radial Depletion Model

Yeckel et. al. [9] have shown that, under the typical conditions encountered for low-pressure chemical vapor deposition (LPCVD) in a tubular hot-wall system, the dominant transport mechanism between the wafers is diffusion, and the concentration gradient across the wafer space in the longitudinal direction can be ignored. The model will be further simplified by assuming that the concentration in the annular region outside the wafers is constant for each space and that the reaction is first order in SiH_2Cl_2. These assumptions can be justified by noting that our interest is in uniform conditions, implying that concentration variations are small. It will also be assumed that the wafers are placed concentrically with the tube without the use of any cantilevers and "boats" to hold them in place. This is, of course, impossible in reality; it will be found later that the obstruction provided by the boat and cantilever improves uniformity rather than making it worse, and so excluding their effect is a worst case condition.

The one-dimensional mass balance in cylindrical coordinates for the simplified

problem, shown in Fig. 5.3, can be written as

$$\delta \frac{d}{dr}\left[rD\frac{dC}{dr} \right] - \alpha r k_s' C = 0 \tag{5.1}$$

in which δ is the space between the wafers, C is the concentration of SiH_2Cl_2, and α is a silicon coverage factor equal to the total area of silicon on the two wafers that bound the space divided by the total area of a wafer. The silicon coverage factor is included because deposition is selective with respect to SiO_2. If the deposition was not selective, or if no oxide present on the silicon surfaces, then $\alpha = 2$.

The binary diffusion constant D for SiH_2Cl_2 and H_2 can be estimated from Chapman-Enskog kinetic theory [10] from

$$D_{AB} = 0.0018583 \frac{\sqrt{T^3 \left[\frac{1}{M_A} + \frac{1}{M_B} \right]}}{P\, \sigma_{AB}^2\, \Omega_{D,AB}} \tag{5.2a}$$

$$\approx D_o \left[\frac{P_o}{P} \right] \left[\frac{T}{T_o} \right]^{1.65} \tag{5.2b}$$

Equation (5.2a) assumes that the ideal gas law is valid, and that the variables are defined as follows: P is the pressure, T is the absolute temperature, M is the respective molecular weights, σ is a characteristic diameter of the molecules, and $\Omega_{D,AB}$ is a slowly varying function of the dimensionless temperature kT/ε. A more convenient representation for our purposes is shown in (5.2b) were D_o at a temperature T_o and pressure P_o is calculated according to (5.2a). It is then assumed that the overall temperature dependence of (5.2a) can be approximated by the power 1.65 in the temperature range in which the reactor

operates [10]. If Lennard-Jones parameters for CH_2Cl_2 are used as an analog to SiH_2Cl_2, D_o is equal to 5700 cm^2/sec at our standard operating conditions of 850° C and 0.6 torr.

The deposition rate in units of cm/sec is assumed to be of the form

$$r_{dep} = k_s P_{DCS} = k_{so} e^{-E_a/kT} P_{DCS} \quad (5.3)$$

where P_{DCS} is the SiH_2Cl_2 pressure, and k_s is a reaction rate constant exponentially dependent on temperature via an Arrhenius relationship with activation energy E_a. The conversion of the rate to units of moles/sec-cm^2 as used in (5.1) is accomplished by defining an alternate surface rate constant k_s' as

$$k_s' = k_s \, m_{Si} \, RT \quad (5.4)$$

where R is the ideal gas constant, T is the absolute temperature, and m_{Si} is the molar density of silicon equal to $8.31 \cdot 10^{-2}$ moles/cm^3. The boundary conditions for (5.1) are:

$$C(R_w) = C_i \quad (5.5)$$

$$\frac{dC}{dr}(0) = 0 \quad (5.6)$$

The concentration in the annular region for the ith wafer is C_i, and the symmetry of the problem forces the gradient to zero at the center.

To obtain a general solution to (5.1) it is useful to define the following dimensionless transformations:

$$\psi \equiv \frac{C}{C_i} \quad (5.7)$$

$$\xi \equiv \frac{r}{R_w} \quad (5.8)$$

After transformation (5.1) becomes

$$\frac{1}{\xi}\frac{d}{d\xi}\left[\xi\frac{d\psi}{d\xi}\right]-\phi^2\psi=0 \tag{5.9}$$

with boundary conditions

$$\psi(1)=1 \tag{5.10}$$

$$\frac{d\psi}{d\xi}(0)=0 \tag{5.11}$$

The dimensionless factor ϕ in (5.9) is defined by†

$$\phi \equiv R_w\sqrt{\frac{\alpha k_s'}{\delta D}} \tag{5.12}$$

The solution to (5.9) can now be found by inspection to be a Bessel function of zero-order and parameter ξ. If the boundary conditions (5.10) and (5.11) are applied to the series form of the Bessel function, the solution can be written as

$$\psi(\phi,\xi)=\frac{1+\dfrac{\phi^2\xi^2}{2^2(1!)^2}+\dfrac{\phi^4\xi^4}{2^4(2!)^2}+\dfrac{\phi^6\xi^6}{2^6(3!)^2}+\cdots}{1+\dfrac{\phi^2}{2^2(1!)^2}+\dfrac{\phi^4}{2^4(2!)^2}+\dfrac{\phi^6}{2^6(3!)^2}+\cdots} \tag{5.13}$$

At the center of the wafers ξ=1 and the normalized concentration reduces to

$$\psi(\phi,0)=\frac{1}{1+\dfrac{\phi^2}{2^2(1!)^2}+\dfrac{\phi^4}{2^4(2!)^2}+\dfrac{\phi^6}{2^6(3!)^2}+\cdots} \tag{5.14}$$

† This parameter is analogous to the Thiele parameter used in chemical engineering to characterize diffusion transport inside catalyst pellets [11].

Because a linear reaction rate expression was assumed, the normalized concentration at the center corresponds directly to the reduction in deposition rate at the center with respect to the edge. An analytic expression accurate to 1% for depletion up to 20% can be obtained by neglecting the high-order terms in (5.14)

$$\psi(\phi,0) \approx \left[1+\frac{\phi^2}{4}\right]^{-1} = \left[1+\frac{R_w^2}{4}\frac{\alpha}{\delta}\frac{k_s'}{D}\right]^{-1} \tag{5.15}$$

According to this expression it should be possible to predict the uniformity if the ratio k_s'/D is known. Note also that because of the first-order rate assumption there is no dependence on the concentration of SiH_2Cl_2.

In order to obtain k_s'/D, and to test the model represented by (5.15), a series of epitaxial silicon depositions shown in Table 5.1 were performed on <100> oriented substrates. The experiments varied the temperature, pressure, composition, and wafer diameter around the standard set of conditions indicated by experiment 177 and 182. To maximize depletion across the wafers, and to maintain radial symmetry, wafers with a 1 μm thick oxide were patterned with concentric oxide circles spaced 4 mm apart as shown in Fig. 5.4 for a 100 mm diameter wafer. The pattern shown in Fig. 5.4 was printed on a transparency with a laser printer, and then transferred to the wafer by using positive photoresist and a 20 sec flood exposure. After development and etching with 5:1 BHF the resulting oxide pattern consisted of 200 μm wide oxide lines corresponding to a silicon coverage ratio of 0.95 independent of wafer diameter. Since the epitaxial deposition is selective, the thickness can simply be measured after each experiment by removing the oxide rings with HF and using a stylus profiler.

The placement of the wafers in the reactor during the radial deposition experiments is shown in Fig. 5.5. Wafers that are not labeled were blank dummy wafers. A

boat with slots cut at 2.4 mm intervals was used to obtain data for spacings of 2.4, 4.8, 7.2, and 9.6 mm. Since the backs of the wafers were bare the corresponding α was 1.95 for the variably spaced wafers. An oxidized wafer was in front of an extra wafer placed at the narrowest 2.4 mm spacing to obtain data for a reduced α of 0.95. The standard boat was used for standard 100 mm diameter wafers and 3 inch diameter wafers. A specially made low-profile boat was used to accommodate 125 mm diameter wafers. The low-profile boat was stored at the back of the furnace when not in use. When necessary the positions of the standard and the low-profile boats could quickly be exchanged by using a clean quartz fork.

Experiment 177 was an initial exploratory experiment that differed from 182 only in that two sets of variably spaced wafers were used. This experiment was used to evaluate the sensitivity of the experiment to loading and symmetry effects. The raw deposition rate data versus radial position from experiment 177 is shown for the upstream and downstream wafer sets in Fig. 6(a) and 6(b), respectively. The radial position axis corresponds to a left (negative) to right (positive) diameter as viewed facing the wafer from an upstream position inside the reactor. It is difficult to discern a trend from the data in this form except for a decrease in growth rate due to depletion for downstream wafers. If, however, the growth rate is normalized to the growth rate at the left (negative) radial position the influence of spacing and α becomes more clear as shown in Fig. 7(a) and 7(b). The left radial deposition rate is used to normalize the growth rate because the injection of gas at the front flange of the reactor occurs through a hole on that side, and this left side is, therefore, expected to show less transport effects. The measured normalized growth rate corresponds directly to the normalized concentration in (5.15) because a first order reaction was assumed in the model. Comparing Fig. 7(a) to 7(b) the effect of depletion is less than the normalized rate uncertainty that varies between ± 0.016 and ± 0.022 depending

on the deposited thickness. The small effect caused by depletion agrees with the model of (5.15) which predicts that radial depletion is independent of the concentration outside the wafers.

The uncertainty of the growth rate data is calculated from the 3σ variation of the thickness measurements which spanned 8,080 Å to 6,090 Å. From measurements of a designated standard step before, and after, each measurement session, it was found that the 3σ uncertainty of the thickness measured by the stylus profiler was ±110 Å for single measurements, and ±70 Å for the average of 4 consecutive scans. To reduce the uncertainty in this work, only thickness measurements from 4 averaged scans are used.

The effect of the boat and cantilevers that support the wafers is shown in Fig. 5.8 which contrasts the depletion across the symmetric left-to-right diameter versus the non-symmetric top-to-bottom diameter. The 4 slotted rods in the boat that hold the wafers, and the 2 cantilevers, block transport to the bottom edge. Because of reduced growth rate at the bottom edge there is less depletion, and uniformity with respect to the bottom edge is improved. This result agrees with the work of Yeckel et. al. [12] which demonstrates that improvement in radial uniformity for polysilicon deposition is possible by using wafer carriers that reduce the growth rate at the edge of the wafers. In our work the model does not include blocking the gas transport to the edges, and measurements across the left-to-right diameter are used to measure the depletion.

Figures 9 through 12 summarize the results of the radial experiments and compare the fit of (5.15) to the data for variations in wafer diameter, pressure, temperature, and composition, respectively. The measured profiles across the narrowest 2.4 mm spacing are shown together with the relationship for the rate at the center versus spacing. The rate data at the center are shown with error bars calculated by assuming a 3σ variation of ±70 Å in the thickness measurement. The prediction of the model is shown with a solid

line. By including an expression for k_s'/D in (5.15), square error was minimized between calculated values and data for the rate at the center by using a downhill simplex algorithm. Best fit tc the data resulted from the following expression for k_s'/D

$$\frac{k_s'}{D} = 1.02 \cdot 10^{11} \left[\frac{P\,(\mathrm{atm})\; R_w\,(\mathrm{cm})}{[T\,(^\circ K)]^{0.65}} \right] e^{-2.05\,\mathrm{eV}/kT}\ \mathrm{cm}^{-1} \tag{5.16}$$

The dependence on pressure and temperature was derived by using the form that would be expected from dividing (5.3) by (5.2). The two fitting parameters in (5.16) can be judged to be reasonable from other published data. The activation energy of the reaction rate is about 2 eV which is within the range of activation energies of 1.3 to 2.2 eV that have been reported in the literature for deposition from SiH_2Cl_2 according to the review by Dudukovic [13]. Values of k_s'/D calculated from (5.16) is within an order of magnitude of values reported by Kuiper et. al. [14] that resulted in uniform deposition for polysilicon.

Equation (5.16) includes a dependence on radius that was found to improve the fit versus wafer diameter. The additional dependence on R may be due to flow effects resulting from the non-central placement for wafers that are not 100 mm in diameter. As can be seen in Fig. 9(a), the growth rate across the 125 mm diameter wafer is reduced on the right (positive) side versus the left (negative) side. Gas enters the system through a hole to the left side of the front flange. The reactor tube of the system was sized for 100 mm wafers resulting in only 5 mm of clearance between the top of the 125 mm wafers and the tube wall. Reduced depletion could have resulted from the small clearance at the top by a blocking effect analogously to the effect observed in Fig. 5.8. The additional radial dependence can also be the result of over simplifying other aspects of the model, such as the reaction rate expression. Experiments in a properly sized tube would be

necessary to resolve this issue.

The fit of the model represented by (5.15) and (5.16) to the data is within the error bars except for a few cases involving the smallest 2.4 mm spacing. The lower than predicted growth rate at the center for narrowly spaced 3 inch diameter wafers in Fig. 9(b) may have been caused by the standard boat not holding the thinner and smaller 3 inch wafers as securely as 100 mm diameter wafers. Also an important consideration in connection with the narrowest spacing is that the mean free path calculated from

$$\lambda = \frac{1}{\sqrt{2}\pi\sigma^2 C_T} \approx 3.4 \cdot 10^{-8} \frac{T\,(^\circ K)}{P\,(atm)} \text{ cm} \tag{5.17}$$

is 0.5 mm at 850° C and 0.6 torr. When the mean free path becomes almost as large as the spacing between wafer, collisions with the wafer surface become almost as frequent as those with other gas molecules. As a result, the growth rate at the edge and the depletion may be larger than predicted by (5.15). The lower than predicted growth at the center in the experiments with the lowest pressure in Fig. 10(b), and the lowest SiH_2Cl_2 concentration in Fig. 12(b), can both be related to the long mean free path. Flow effects or a more complex reaction rate expression are also likely candidates for discrepancies between the model and the data.

As mentioned previously, the deposition of the epitaxial silicon from H_2 and SiH_2Cl_2 is selective with respect to SiO_2, and accordingly depletion across the wafers can be reduced by using wafers with SiO_2 on their back surfaces. According to the model in (5.15), the depletion across wafers should be the same as long as the ratio of the silicon coverage ratio (α) to wafer spacing (δ) stays constant. To test this prediction an oxidized wafer was included in each of the radial experiments to simulate the effect of using wafers with oxide covered back surfaces. Wafers with oxide on their back surfaces are easily

obtained if a plasma is used to etch the oxide patterns on the front surfaces. However, for these experiments the etching of the silicon substrate by the plasma after the oxide in the patterns is removed would have introduced increased uncertainty in the thickness measurements. The oxide covered wafer in front of another wafer, as shown Fig. 5.5, reduced the silicon coverage ratio from 1.95 to 0.95. Dividing the silicon coverage ratios with their respective spacings of 4.8 and 2.4 mm, the model predicts that the difference should be less than 0.003 for each of the experiments. Comparing the difference predicted by the model to the measured differences shown in Fig. 5.13(b), the differences revealed by the data are an order of magnitude larger than predicted by the model, and in each case the rate at the center is less for the narrower spacing with an oxidized wafer. Increased transport to the edge for wider spacings due to a flow effect is a possible explanation for the difference. There is also an uncertainty due to the thickness measurement repeatability of ±70 Å that is significant in comparison to the observed difference as shown in Fig. 5.13(b). Only for experiments 191 and 194 is the difference larger than the uncertainty. These experiments involve the highest temperature, and lowest concentration of SiH_2Cl_2, respectively, and would be most sensitive to an overly simplistic reaction rate expression. More precise measurement methods, or thicker epitaxial films, would be required to resolve the real difference and to justify a more complex model.

An effectiveness factor η can be used to incorporate the effect of radial depletion in the longitudinal deposition rate model that will be described in the next section. The formal definition of the effectiveness factor is the ratio of the actual deposition rate for the whole wafer to the rate evaluated at the concentration at the edge of the wafer.† If the simple linear reaction rate expression defined by (5.3) and (5.4) is used the following

† The definition of this effectiveness factor is analogous to those used in chemical engineering to relate reaction rates in catalyst pellets to external concentrations [11].

expression for the effectiveness factor is obtained

$$\eta = \frac{\int_0^{R_w} k_s' C(r)\, 2\pi r\, dr}{k_s' C_i \cdot \pi R_w^2} \tag{5.18}$$

Simplifying the expression, and substituting the definition for the normalized variables defined in (5.7) and (5.8), results in

$$\eta = 2 \int_0^1 \psi(\phi,\xi)\, d\xi \tag{5.19}$$

Using the first two terms in (5.13) to integrate (5.19), we obtain the following simple expression

$$\eta = \frac{1 + \frac{\phi^2}{8}}{1 + \frac{\phi^2}{4}} \tag{5.20}$$

which can be evaluated independently of the concentration by using the model described in this section. If a more complex reaction rate expression was used then the effectiveness factor could still be used, but it would not be independent of concentration.

5.3 Longitudinal Uniformity Model

The flow regime in the reactor can be characterized by the non-dimensional Reynolds and Peclet numbers. The Reynolds number characterizes the transition from laminar to turbulent flow and is defined by

$$R_e \equiv \frac{L u \rho}{\mu} \tag{5.21}$$

where u is the linear velocity, ρ is the density, μ is the viscosity, and L is a characteristic length of the problem. Using the ideal gas law, the density can be calculated according to

$$\rho = M C_T = M \left[\frac{P}{RT}\right] \tag{5.22}$$

where M is the molecular weight of the gas mixture. The viscosity can be estimated from

$$\mu = 2.6693 \cdot 10^{-5} \frac{\sqrt{MT}}{\sigma^2 \Omega_\mu} \tag{5.23}$$

where σ is a characteristic diameter of the molecule and Ω_μ is a slowly varying function of the dimensionless temperature kT/ε [10]. As in the case of diffusion, the Lennard-Jones parameters σ and kT/ε can be approximated for SiH_2Cl_2 by using values for CCl_2H_2 [10]. The linear velocity u is related to the volumetric flow rate v by dividing it with the cross-sectional area A. The volumetric flow rate v can be related to a standard condition volumetric flow rate v_{std} by using the ideal gas law. The result is the following equation

$$u = \frac{v}{A} = \frac{v_{std}}{A} \left[\frac{T}{273°K}\right] \left[\frac{1\ \text{atm}}{P}\right] \tag{5.24}$$

It is convenient for our purposes to relate the linear velocity to a standard volume of gas per unit time since the mass flow controllers used to determine the gas flow input to the reactor also use these units.

For our typical condition of a total flow of 432 sccm (standard cm^3/min), 7.4% SiH_2Cl_2 in H_2, 850° C, and 0.6 torr, it can be calculated that the linear velocity is 280 cm/sec, the density is $8.0 \cdot 10^{-8}$ g/cm^3, and the viscosity is $3.6 \cdot 10^{-4}$ g/cm-sec. The resulting Reynolds number for the 25 cm long region where the wafers are located is 1.5. For the 75 cm long hot zone, assuming no obstructions, the Reynolds number is 3.7. Both of

the calculated Reynolds numbers are smaller than 1000 which signifies the transition to turbulent flow, and larger than 0.1 which characterizes a transition away from creep flow around objects in the path of the gas. The flow is, therefore, expected to be laminar, but with vortices forming at the edges of objects in the reactor. For simplicity only laminar flow is included in the present model.

The Peclet number is a measure of the relative importance of convection versus diffusion, and is defined by

$$P_e \equiv \frac{u L}{D} \tag{5.25}$$

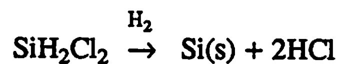
If the Peclet number is much greater than one, convection dominates, and if the Peclet number is much less than one, diffusion dominates. The same reactor conditions used for the Reynolds number calculation result in a Peclet number for the 25 cm long wafer region of 1.2, and for an open 75 cm long hot-zone the Peclet number is 2.3. These Peclet values indicate that diffusion is of equal importance to convection in determining the transport inside the reactor, and that both transport mechanisms must be included in the longitudinal model.

It is interesting to note at this point that if (5.2), (5.22), (5.23), and (5.24) are substituted in the definitions for the Reynolds and Peclet numbers, the dependence on pressure cancels out. This suggests that the main reason the Reynolds and Peclet numbers are small is that volumetric flow rate is low relative to the size of the reactor, not because of low pressure operation.

Because of the low pressure and the high temperature, radiation is assumed to be the dominant heat transfer mechanism, and heat of reaction is assumed to be insignificant. These assumptions can be justified by noting the low gas density at our typical operation

pressure of 0.6 torr, and the low growth rate. The assumed reactor temperature will, therefore, be radially uniform and determined by the reactor temperature profile. Furthermore, the radial concentration profile outside of the wafer spaces is assumed to be uniform. The results from the previous section indicate that for typical operating conditions the radial diffusion rate is about 10^3 larger than the growth rate, making this a reasonable assumption.

Because the temperature and concentration will vary significantly in the longitudinal direction, a simple first order reaction rate expression, such as (5.3), is not expected to be a good approximation. The thermodynamics of the Si-Cl-H system [15, 16, 17, 18], and the kinetics of silicon deposition from chlorosilanes [18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29] have been extensively researched. Measurements by mass spectrometer [21, 22] and IR spectroscopy [26, 27, 23, 29] have indicated the presence of $SiCl_4$, $SiHCl_3$, SiH_2Cl_2, HCl, SiH_3 (only in Nishizawa et. al.), and $SiCl_2$ in the gas phase. There is, however, no consensus on a definite reaction mechanism. The large number of gaseous species that are formed, and the significant reverse component due to etching by HCl, makes it unlikely that a single reaction mechanism is responsible. Even for simple heterogeneous reactions, different and quite complex reaction rate equations result from assuming reactions in the gas phase, adsorption, surface reaction, or desorption to be rate limiting step [30]. To avoid the reaction mechanism problem, a power-law rate expression that relates to the overall reaction is used which can be written as



$$SiH_2Cl_2 \xrightarrow{H_2} Si(s) + 2HCl$$

Hydrogen is not consumed or generated by the reaction but can affect both the forward and reverse rates so that the general deposition rate expression becomes

$$r_{dep} = k_s\, P_{DCS}^{a}\, P_{H2}^{b} - k_r\, P_{HCl}^{c}\, P_{H2}^{d} \tag{5.26}$$

where the two reaction rate constants are given by:

$$k_s = k_{so}\, e^{-E_a/kT} \tag{5.27}$$

$$k_r = k_{ro}\, e^{-E_{ar}/kT} \tag{5.28}$$

Because this expression does not describe a single mechanism, it is not expected that the powers will be integers or half-integers. Instead, all 8 reaction parameters (k_{so}, E_a, k_{ro}, E_{ar}, a, b, c, d) will be chosen to best fit the deposition rate data. Unless an accurate reaction mechanism is known, this approach should be at least as accurate as an expression derived from a postulated mechanism.

Evaluation of equation (5.26) along the reactor requires that the concentration profiles of SiH_2Cl_2 and HCl be calculated. A model using two coupled mass balances will require much more computation time to solve than a single mass balance. If it is assumed that HCl is in equilibrium with the SiH_2Cl_2 at each point in the reactor (or equivalently that their respective transports are not significantly different), the HCl concentration can be calculated from the amount of SiH_2Cl_2 that has reacted, avoiding the need for two mass balances. The amount of SiH_2Cl_2 that has reacted can be expressed by a conversion factor χ along the reactor defined by

$$\chi = 1 - \frac{C}{C_{noreac}} \tag{5.29}$$

where C is the concentration of SiH_2Cl_2 and C_{noreac} is a concentration calculated from setting the reaction rate to zero. The HCl concentration along the reactor is then given by

$$C_{HCl} = 2\,\chi\, C_{noreac} \tag{5.30}$$

where the factor 2 results from the stoichiometry of the overall reaction.

According to the previous results and assumptions the model becomes a one-dimensional mass balance for a single reactant such as discussed by Levenspiel [31] for a plug-flow reactor with longitudinal dispersion due to diffusion. The differential equation describing the reactor is derived by dividing the reactor into N elements for which a steady-state mass-balance is written which states that the mass flow into the element is equal to the mass flow out of it. For the ith element, as shown in Fig. 5.14, mass enters the element by convection, diffusion, and by the possible use of an injector at that point. Mass leaves by convection, diffusion, and reaction due to deposition. Each element has a length Δz, temperature T, surface area per unit length S_L, and cross-sectional area X_A. Also associated with each element is the molecular concentration C and volumetric flow rate v. In the limit of $\Delta z \rightarrow 0$ the following differential equation is derived

$$\frac{d}{dz}\left[vC\right] - \frac{d}{dz}\left[X_A D \frac{dC}{dz}\right] + \left[r_{dep} - r_{inj}\right] S_L = 0 \tag{5.31}$$

where the first term is due to convection by the volumetric flow rate, the second term is due to diffusion, and the last term represents the loss due to the net deposition rate r_{dep} and the gain due to injection at a rate r_{inj}. The boundary conditions for (5.31) are:

$$C(0) = C_o \tag{5.32}$$

$$\frac{dC}{dz}(L) = 0 \tag{5.33}$$

where the simulated region from distance 0 to L is chosen so that deposition outside of the region can be ignored. The concentration C_o in (5.32) is the input concentration of SiH_2Cl_2 at the front of the reactor. Equation (5.33) results from assuming that no reaction

takes place beyond the distance L (i.e. C cannot change past L), and was shown by Wehner and Wilhelm [32] to be correct as long as the Peclet number is greater than zero.

For the case of first order kinetics with constant temperature and no volume expansion due to reaction, equation (5.31) can be solved analytically for C as a function of distance z [32]. However, in our case the reaction rate is not first-order, and the extremes of the reactor where the temperature is not constant are included. A numerical solution of (5.31) for C(z) will be performed instead by using a finite difference approach to approximate the differential equation, resulting in a tridiagonal set of non-linear equations that can be solved by the Newton-Raphson algorithm.

The pressure drop can be estimated from the analysis performed by Hitchman et. al. for LPCVD of polysilicon [33]. From their analysis we estimate that at our typical reactor conditions of 850° C and 0.6 torr the pressure drop is 14 mtorr over the length of the hot-zone. Because of the small magnitude of the drop, we assume that the pressure is constant, forcing instead the volumetric flow rate to vary in order to compensate for volume changes due to temperature and reaction. According to this assumption the volumetric flow rate becomes

$$v = v_{std} \left[\frac{T}{273^\circ K}\right] \left[\frac{1\,atm}{P}\right] \left[1 + \chi f\right] \tag{5.34}$$

where v_{std} is the input volumetric flow rate in standard cm^3/sec, χ is the previously defined conversion factor, and f is the volumetric expansion factor at full conversion (i.e. @ χ=1). The other factors in (5.31) have been discussed previously. Diffusivity is dependent on temperature and pressure according to (5.2a), and can be approximated by (5.2b) where D_o is 5700 cm^2/sec at 850° C and 0.6 torr. The reaction rate is dependent on temperature and pressure according to (5.26), which can be converted to a concentra-

tion dependence and molar flux by using the ideal gas law and the molar density of silicon as shown by (5.4) for the radial case.

Seven epitaxial silicon deposition experiments on <100> oriented substrates were conducted in order to evaluate the longitudinal model described by (5.31) and to find appropriate parameters for the reaction rate expression in (5.26). The deposition conditions used for the longitudinal uniformity experiments are shown in Table 5.2. The temperature, pressure, and composition were varied around the typical deposition conditions represented by experiment 196. Wafers with a 1 μm thick oxide were patterned with our selective epitaxy test mask and then etched in 5:1 BHF. The epitaxial thickness was measured with a stylus profiler by removing the masking oxide after each experiment. Six patterned wafers were included in each run, and placed inside the reactor at the locations shown in Fig. 5.15. The other 23 wafers were blank dummy wafers. To obtain deposition rate data from the front of the reactor, two wafers were placed directly on the cantilever rods, and one wafer was placed between the last set of baffles.

Deposition is selective with respect to the oxide on wafers but the quartzware accumulates a coating of silicon because of the repeated exposures. Inspection of the quartzware inside the reactor reveals an abrupt beginning and end of the deposition zone. Using a coordinate system with the center of the reactor at zero as shown in Fig. 5.15, the positions where deposition starts and ends are located at -15 and +15 inches, respectively. Simulation is confined to this region by assuming that the boundary conditions in (5.32) and (5.33) apply at the observed deposition boundaries. A grid of 120 uniformly spaced points along the reaction zone was found to produce a smooth deposition profile even through regions with abrupt transitions. The simulator can also accommodate a non-uniform grid to increase the number of points in regions with abrupt transitions. Cross-sectional area, surface area per unit length, and temperature are input as a function of z by

as shown in Fig. 5.16. The cross-sectional area and surface area per unit length were calculated from the dimensions and locations of the various pieces of quartzware inside the furnace. The large reduction in cross-sectional area in Fig. 5.16(a) at each end is caused by the baffles. The surface area per unit length profile in Fig. 5.16(b) was calculated using the total surface areas before radial depletion was incorporated for the different reactor conditions by multiplying the radial surface areas of wafers and baffles with the effectiveness factor defined by (5.20). The temperature profile in Fig. 5.16(c) was measured with a movable thermocouple at 1 inch intervals. The accuracy of the temperature profile is estimated to be ±1/8 inch and ±0.4° C. Interpolation was used to obtain temperatures for grid points between temperature measurement points.

A downhill simplex algorithm was used to minimize the squared error between simulated deposition rates and the data. The reaction rate parameters obtained by this method are shown in Table 5.3. From our previous discussion on the complexity of the real reaction mechanism it would be dangerous to infer too much information from these parameters. It is reassuring, however, to find that, as in the case of the radial model, the activation energies fall in the range of those reported in the literature. The approximately half-order dependence on both SiH_2Cl_2 and H_2 is surprising. It is commonly believed that H_2 only acts to reduce the deposition rate by occupying surface sites, resulting in an inverse half-order H_2 dependence instead. One possibility is that hydrogen plays an active role in the deposition mechanism, either by generating an active intermediate in the gas phase, or by arriving from the gas phase to complete the surface reaction to form solid silicon. However, the excess H_2 that is present makes it unlikely that such a dependence is observed. Another possibility, therefore, is that the unusual H_2 dependence occurs because the reaction mechanism changes when the total pressure changes.

Simulated deposition rate profiles using the parameters of Table 5.2 are plotted together with the corresponding experimental data in Fig. 5.17. Overall the agreement between data and simulation is good; the predicted decrease in reaction rate because of depletion agrees especially well with the data, only for the simulation of experiment 199 (3.4% SiH_2Cl_2) in Fig 5.17(c) is there significant disagreement. Experiment 199 involves the lowest concentration of SiH_2Cl_2 and is, therefore, most susceptible to any inaccuracies of the mass flow controllers. Accuracy of the mass flow controllers is worse when operating close to the bottom of their range, which is the case here since the range of the controller is 0-100 sccm. As shown in Fig. 5.17(c), a small increase in the flow of SiH_2Cl_2 during the simulation of experiment 199 from the nominal 16 sccm to 20 sccm can account for the discrepancy. However, it is also possible that the reaction mechanism for the lowest concentration of SiH_2Cl_2 is different enough that a single set of parameters in an overall reaction rate expression like (5.26) cannot fit all of the data. More experiments are necessary to distinguish between these two possibilities.

The difference between simulation and data in the entrance region is much larger than in the region where the wafers are located. There are two significant effects occurring in the entrance region which the model does not include. One effect is that the gas squeezed through the small annulus surrounding the baffles is suddenly free to expand into the much larger cross-section of the open tube. The Reynolds number predicts that vortices will form when the gas enters the open tube from the annular region surrounding the front baffles. These vortices cause back mixing that increases the concentration, and the deposition rate, in the region just following the baffles. Since the reactor model does not include back flow, the predicted growth rate, as can be seen in Fig. 5.17, is less than the data in the region just following the front baffles. The other effect is that the gas heats up slower than the rapidly changing wall temperature at the front of the reactor. The

increased linear velocity in the annulus around the front baffles only helps to contribute to that effect. As can be in Fig. 5.17, the simulated growth rate decreases less rapidly than the data towards the front of the reactor in the heat up region where the front baffles are located. This may indicate that the wall temperature used in the model is larger than the gas temperature in the front region where the temperature is increasing rapidly. Because no deposition was observed on the quartzware past -15 inches from the center of the reactor, the front boundary condition was imposed at that distance, so the effect of the discrepancy due to the difference between gas temperature and wall temperature is less than if simulation was extended further towards the front of the reactor. Because of the entrance effect, the fitting parameters and boundary conditions now include properties specific to our system. Whether this results in a significant loss in generality for the model has not yet been determined.

5.4 Modeling as a Design Aid

In this section it will be assumed that the models derived in the previous sections adequately represent the behavior of our system, and that it is possible to extend the models to scaled systems. Possible applications of the models will be illustrated by two examples: (1) an evaluation of possible improvements to our existing system, and (2) a design approach to a production-sized system able to process 100 wafers of 200 mm diameter.

5.4.1 Improvements to Existing Reactor

For the typical conditions, represented by experiment 196, the mean growth rate is 61 Å/min with a variation of ±32% across the 10 inch long zone in the center of the reactor where the boats are located. The typical reactor conditions was chosen as a

convenient tradeoff between epitaxial quality, growth rate, and radial uniformity to serve as a point of reference for our experiments. The operating window is currently constrained by the 80 cfm (cubic feet/min) rotary-vane pump that evacuates the reactor. Its limited capacity in our pressure range does not allow for an increase in flow without a concomitant pressure increase. The planned addition of a roots blower to the rotary vane pump should provide a significant increase in capacity, allowing for more flexibility in the choices of flow rate and pressure. In particular it is hoped that higher flow rates can be used to demonstrate the feasibility of the hot-wall epitaxial reactor approach by producing a more uniform growth rate profile.

Assuming that constant pressure is maintained, the reactor model can be used to quickly evaluate the effect on the growth rate profile by the 3 different permutations for increasing the flow rate. The flow of SiH_2Cl_2 or H_2 can be increased individually or together. For the simulated growth rates shown in Fig. 5.18(a), the ratio of SiH_2Cl_2/H_2 is changed by only increasing one of the flow rates at a time, maintaining otherwise the conditions of experiment 196. An increase in the SiH_2Cl_2 flow increases the mean growth, but the variation across the 10 inch center region is not reduced in comparison to experiment 196. An increase in the H_2 flow rate decreases the growth rate and improves the uniformity. These two simulation results suggest that an increase in only the SiH_2Cl_2 flow rate at the front of the reactor will not be beneficial for controlling the growth rate uniformity. An increase in only the H_2 flow reduces the partial pressure of SiH_2Cl_2 and increases the total flow rate in the system, improving the uniformity at the expense of reducing the overall growth rate. As shown in Fig. 5.18(a), a variation of ±8.5% can be obtained if the H_2 rate is increased 7.5 times that of experiment 196, but the mean growth rate is reduced to 40 Å/min. For an increase in the H_2 flow rate to result in a reduction of depletion it is necessary that the pump and tubing that connect it to the reactor is of

sufficient capacity that a constant pressure can be maintained. The large effect produced by a small increase in pressure from 0.6 torr to 1.0 torr is shown in Fig. 5.18(b). Depletion is considerably increased as demonstrated by the ±49% variation across the 10 inch center section for the growth rate profile calculated from the same flow rates as experiment 196. The H_2 flow rate that results in a uniformity similar to to the 0.6 torr case is increased from 3000 to 8000 sccm. It is interesting to note that not only is the uniformity similar, but the actual growth rates are also similar. This suggests that the ratio between growth rate and mass transport determines the uniformity as proposed by Kuiper and Brekel [14]. If the pressure can be kept constant, both an increased growth rate and less variation can be attained by increasing the SiH_2Cl_2 and H_2 rates together, as shown in Fig. 18(c). For a factor of 10 increase in the flow rates of experiment 196 the mean growth rate is 131 Å/min ±5.0%. The results shown in Fig. 5.18 imply that improving the growth rate uniformity by injecting more gas from the front is inefficient because of the large flow of gasses that become necessary. In addition to the cost of gas and vacuum pumps, local variations in growth rates due to vortices will also become a larger effect as the total flow rate of the system is increased. The Reynolds number is directly related to the flow rate according to (5.21) and (5.24).

Injectors placed along the length of the reactor increases the complexity of the reactor, but makes more efficient use of the available pumping speed by adding SiH_2Cl_2 directly where it is needed to compensate for loss due to depletion. The ability to place an individually controlled injector at every grid point along the reactor is included in the simulator. In Fig. 5.19, 3 injectors each adding 32 sccm of SiH_2Cl_2 have been placed 5 inches apart at the rear of the reactor. Adding this set of injectors to a simulation of experiment 196 increases the mean growth rate from 61 Å/min to 88 Å/min, and the variation in growth rate simultaneously decreases from ±32% to ±7%, while only increasing

the total flow by a factor 1.2. Optimizing the results with injectors is a trial-and-error process that can accomplished much more quickly if a reactor model is available. The increase in complexity with injectors results from adding the extra hardware to the reactor, and maintaining the injector tubes which are likely to plug up periodically because silicon deposits. Improved control and flexibility is afforded by using three individual injectors each with their own mass flow controller. Such an implementation allows the positions and flow rate at each injection point to be adjusted with minimal disruption to the reactor. The mass flow controller for each will be able to compensate for the gradual narrowing of the injector tube because of deposition. A simpler implementation uses a single mass flow controller feeding an injector manifold with multiple holes placed at the desired locations. More injection points can be implemented by this method but the amount of injection at a given point will vary as deposition gradually plugs up the injector manifold. For a production-sized reactor some kind of injector system will almost certainly be required because of the large number of wafers in each batch, but in the case of our reactor the need for injectors depends on the future goals for the project. For basic studies of epitaxial growth properties, involving only a few wafers in each batch, injectors are not necessary.

Besides predicting the results due to changes in the operating conditions, the reactor simulator can also be used to analyze the effect of changes to the structural features of the reactor. A particular concern is the effect of the quartz baffles used at the ends of the reactor to block radiative heat losses. These baffles affect the growth rate profile of the reactor by reducing the cross-sectional area and increasing the surface area. Three possible changes to these baffles will be simulated: (1) reducing the surface area with a solid baffle,† (2) increasing the cross-sectional area by perforating the baffles with

† Usually made by constructing a quartz container and stuffing it with an opaque material.

staggered holes so that radiation is still blocked, and (3) reducing the cross-sectional area by scaling the baffles to the smallest practical clearance to the tube wall. Simulated growth-rate profiles for the three modified types of baffles are shown in Fig. 5.20 by using the typical deposition conditions of experiment 196. Reducing the surface area with a solid baffle while maintaining the same cross sectional area is found to have a barely perceptible effect on the growth rate profile, suggesting that the depletion occurring at the baffles is not a significant factor in determining the growth rate profile. The cross-sectional area and surface area of the perforated baffle was calculated by assuming that 36 holes with 1 cm diameters have been made in each plate, making the effective cross-sectional area 2.4 times larger. For this increase in cross-sectional area, the mean growth rate for the 10 inch center region is predicted to increase with respect to experiment 196 by 14%. A maximally sized larger baffle was calculated by assuming that the minimum clearance between the tube wall and baffle could be decreased to 4 mm (optimistic), resulting in a 35% reduction in the cross-sectional area with respect to the current baffles. The result of the reduced cross-sectional area is predicted to decrease with the mean growth rate by 5% with respect to experiment 196. It was hypothesized that a larger baffle would perhaps improve the uniformity along the reactor by reducing the growth rate at the front analogously to the radial effect seen in Fig. 5.8. The negative result to this hypothesis suggests that the improvement in radial uniformity at the bottom of the wafers in Fig. 5.8 is not due to a reduction in the diffusion rate, but rather to a reduction of the increased growth rate at the edges due to vortices. According to these simulations, perforated baffles can be proposed as a worthwhile improvement to increase the overall growth rate in our existing reactor. Perforated baffles provide an additional benefit of a less abrupt transition from the baffles to the open tube, reducing the discrepancy between the model and data in that region.

5.4.2 Design Approach to a Production-Sized Reactor

The design of a production-sized hot-wall silicon epitaxial deposition system is difficult to generalize because of the large number of decisions specific to the application that are involved. However, with the reactor model derived in previous sections it is possible to quickly try various options and then refine a design to a particular set of constraints. A design for a hypothetical production sized reactor for 200 mm diameter wafers will be described to illustrate such an approach.

It will be assumed that the hypothetical reactor should use a compact furnace design like our existing reactor so that the temperature profiles at the end zones will be similar. The goal for the reactor capacity is 100 wafers per load at a growth rate of 100 Å/min. The thickness tolerance will be assumed to be ±2.5% per wafer and ±7.5% total. It will further be assumed that the intended application is selective epitaxial deposition with no more than 70% of the surface consisting of silicon. Because selective epitaxy requires vertical oxide side-walls, it will be assumed that a plasma etch is used to etch the oxide pattern, resulting in an oxide covering the back surfaces of the wafers.

Furnaces using a compact design are commercially available with heaters of 10 inch diameter and 100 cm long zones capable of maintaining a flat temperature profile within ±0.5° C. Once the furnace has been chosen the spacing is determined by the number of wafers that are to be accommodated. A spacing of 9.6 mm is chosen to allow the use of two standard 50 wafer boats. From equation (5.15) the relationship between the spacing δ and the other parameters is

$$\delta = R_w^2 \frac{\alpha}{4} \left[\frac{1}{\psi} - 1 \right]^{-1} \frac{k_s'}{D} \tag{5.35}$$

From the specified design goals all of the parameters have been determined except for the

temperature and pressure. The relationship between spacing, temperature, and pressure according to (5.35) is shown in Fig. 5.21. An operating point towards high temperature is chosen because epitaxial quality is easier to maintain. The chosen temperature of 840° C corresponds to a pressure of 0.4 torr in order to satisfy the the spacing requirement of 9.6 mm.

Specified dimensions of the tube and internally placed items determine the calculated cross-section and surface area per unit length profiles. Assuming that the hypothetical reactor can be made by scaling up our existing reactor to a tube of 24.5 cm ID, the calculated profiles for cross-sectional area and surface area become those shown in Fig. 5.22(a) and 5.22(b). A temperature profile must also be determined either by assumption or measurement. For this design an ideal temperature profile is constructed from a flat temperature of 840° C in the center zone that is joined to end zone temperature profiles obtained from our existing reactor.

The design is evaluated by using the longitudinal model to try various combinations of flows and injector placements to determine if the specifications for growth rate and uniformity can be met for that particular configuration. For a production-sized system, with a large amount of surface area, an important observation from our simulations, involving a large range of input flow combinations, is that the amount of H_2 flow is important for maintaining a flat growth rate profile towards the rear of the reactor. For conditions that lead to HCl concentrations large enough at the rear of the reactor that the reduction in growth rate is due mainly to the reverse rate, an increased H_2 is necessary to decrease the growth rate at the front and increase the rate at rear of the reactor. The impact of this effect on the design process is that for a given surface area per unit length there is a an inverse relationship between the length of the reactor and the maximum flat growth rate that can be maintained. For the reactor design example in this section a flat

growth rate at 100 Å/min can only be maintained for about half the required reactor length of 100 cm.

The growth rate profile for the reactor designed in this section is shown in Fig. 5.23 for which it was assumed a the capacity of the pumping system is able to maintain 0.4 torr at a total flow rate of 2500 sccm. An injector system capable of injecting 30 sccm of SiH_2Cl_2 at 6 places is included in the design. All of the specified design goals could be met except for the mean growth rate which is 53 Å/min. For the current design a growth rate of 100 Å/min is only attainable for a reactor of half the size. Changes to the design and further simulations would be necessary to explore the possibility of a 100 wafer system capable of 100 Å/min on 200 mm diameter wafers. In addition to injectors it is likely that a sloped temperature profile will also be necessary for such a system.

Even with a growth rate of only 50 Å/min, a system capable of uniform deposition on 100 wafers of 200 mm diameter wafers is interesting. Because it is required to place the wafers side by side on a heated susceptor in most cold-wall reactor, the number of wafers per batch decreases rapidly as the wafer diameter increases. The commercially available 78 series Applied Materials reactor can normally accommodate 4 wafers of 200 mm diameter per batch, and an expansion kit can increase this to 8 wafers per batch. Assuming 1 μm thick selective epitaxy layers the reactor cycle would be the same as in Chapter 3, resulting in a throughput of 10.7 wafers/hour with an expansion kit. Assuming a deposition cycle for the hot-wall reactor that is similar to the one described in Chapter 2, the total cycle time for a 1 μm thick layer would be 400 min, resulting in a throughput of 15 wafers/hour for the hot-wall reactor described in Fig. 5.23.

5.5 Summary

A complete model was presented for the deposition uniformity in our low-pressure hot-wall epitaxial silicon. Radial depletion was modeled successfully with a simple first-order reaction-rate expression leading to an analytic solution which is independent of the concentration. A successful longitudinal depletion model was found to require a more complicated reaction rate expression, and also both convective and diffusive transport. To avoid the controversy and inaccuracies introduced by stipulating a reaction mechanism, a simple power law rate expression was used, for which the parameters were chosen for best fit to the data. The resulting parameters are physically reasonable except for a surprising half-order H_2 dependence.

To illustrate the use of the model, improvements to our existing reactor were analyzed, and the design of a production-sized reactor that accommodates 100 wafers of 200 mm diameter was proposed. For our existing system it was found that a significant increase in total flow rate by a factor of 5-10, or injectors would be necessary to improve the deposition uniformity without reducing the growth rate. A perforated baffle was proposed as an addition to our system that could under typical conditions increase the growth rates by more than 10%. The example illustrating the design process for a production-sized reaction was able to achieve a growth uniformity of better than ±7% but at a lower rate than the desired 100 Å/min. However, even at growth rates of 50 Å/min, a hot-wall reactor of the proposed size was found to have higher wafer throughput than a typical cold-wall reactor.

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Table 5.1 Radial Uniformity Experiments

Expt. #	Temp. (°C)	Press. (mtorr)	H_2 (sccm)	DCS (sccm)	Wafer dia. (mm)
177	852	620	400	32	100
182	852	622	400	32	100
183	852	622	400	32	75
184	851	621	400	32	125
186	851	393	200	16	100
188	851	1003	800	64	100
191	901	607	400	32	100
192	803	596	400	32	100
193	852	601	312	64	100
194	852	605	452	16	100

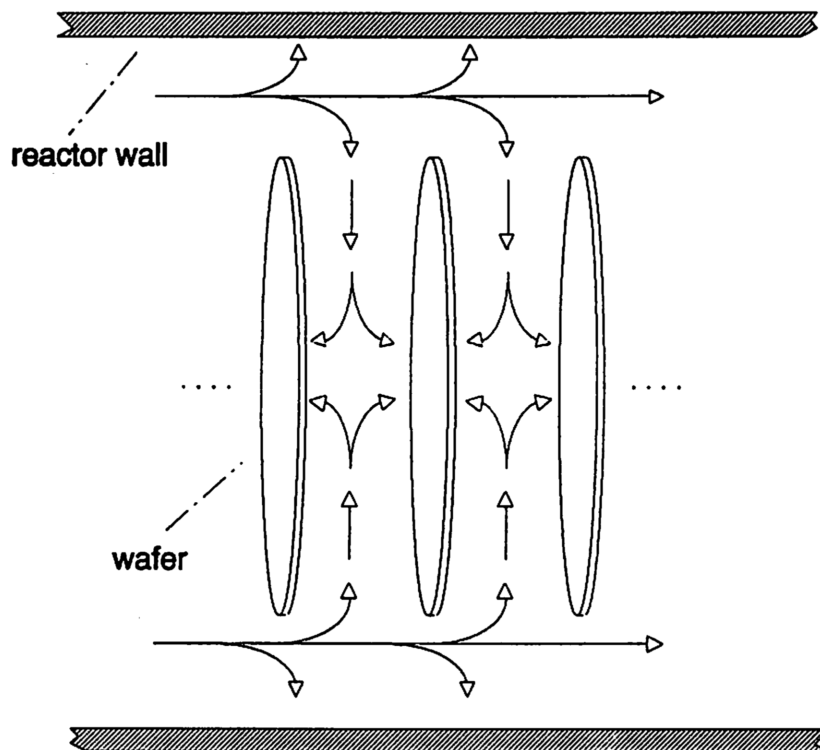
Table 5.2 Longitudinal Uniformity Experiments

Expt. #	Temp. (°C)	Press. (mtorr)	H_2 (sccm)	DCS (sccm)
195	901	609	400	32
196	853	604	400	32
197	852	387	200	16
198	853	986	800	64
199	852	604	452	16
200	853	602	312	64
201	804	602	400	32

Table 5.3 Longitudinal Model Parameters

k_{so} (cm/sec)	$4.930 \cdot 10^5$
E_a (eV)	2.037
k_{ro} (cm/sec)	$4.922 \cdot 10^4$
E_{ar} (eV)	1.763
a (DCS)	0.583
b (H_2,forward)	0.551
c (HCl)	1.129
d (H_2,reverse)	-0.097

Fig. 5.1 Schematic representation of the physical processes that lead to non-uniform deposition in a tubular hot-wall deposition system.



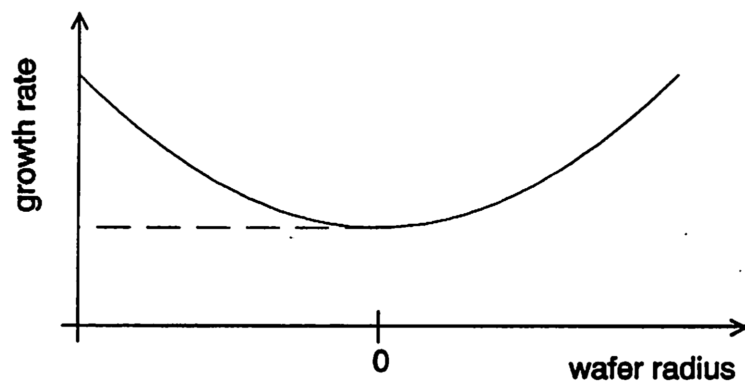


Fig. 5.2 Schematic representation of our tubular reactor illustrating that the end zones can contribute significantly to the growth rate profile across the region where the wafers are placed. Confining the simulation to only the wafer region, assuming no reaction occurring in the end zones, results in a curved profile that does not match measured profiles.

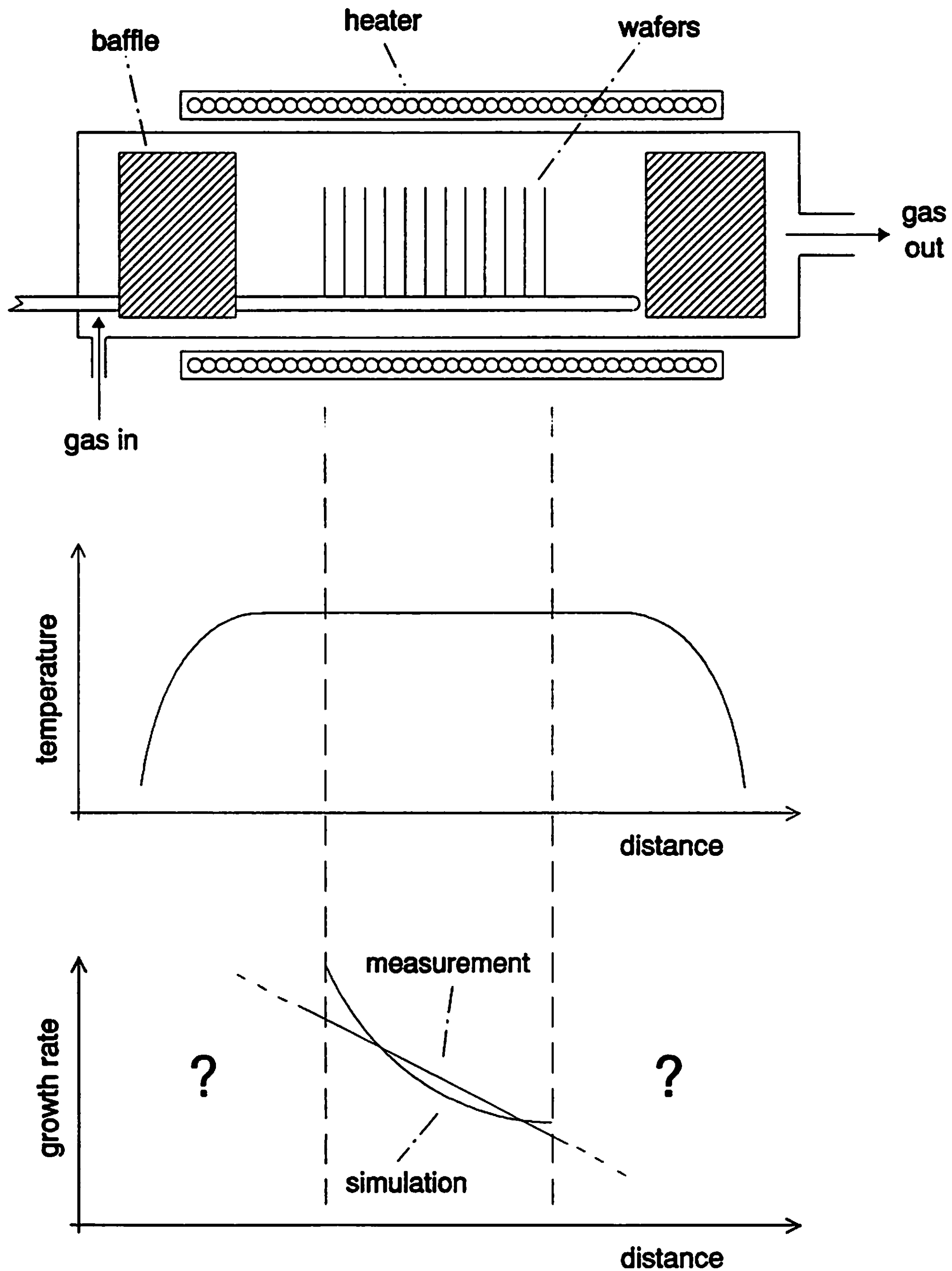


Fig. 5.3 Simplified situation that results from the assumption that transport of reactants to the centers of the wafers occurs by diffusion from a uniform annular concentration.

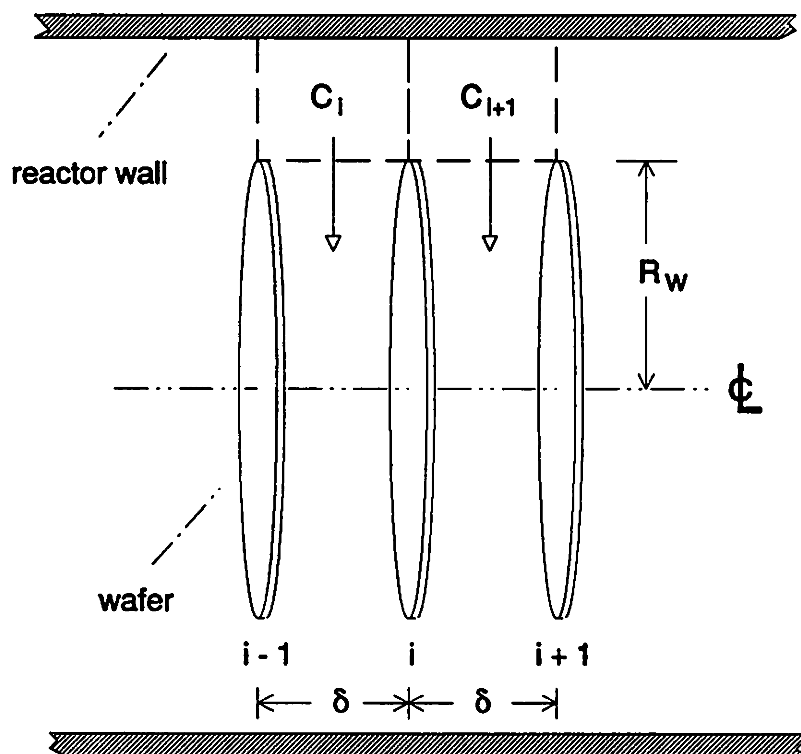


Fig. 5.4 Pattern that was used to generate wafers with concentric narrow circles of oxide spaced 4 mm apart for the radial uniformity experiments. Pattern used for the 100 mm diameter wafers is shown in this figure.

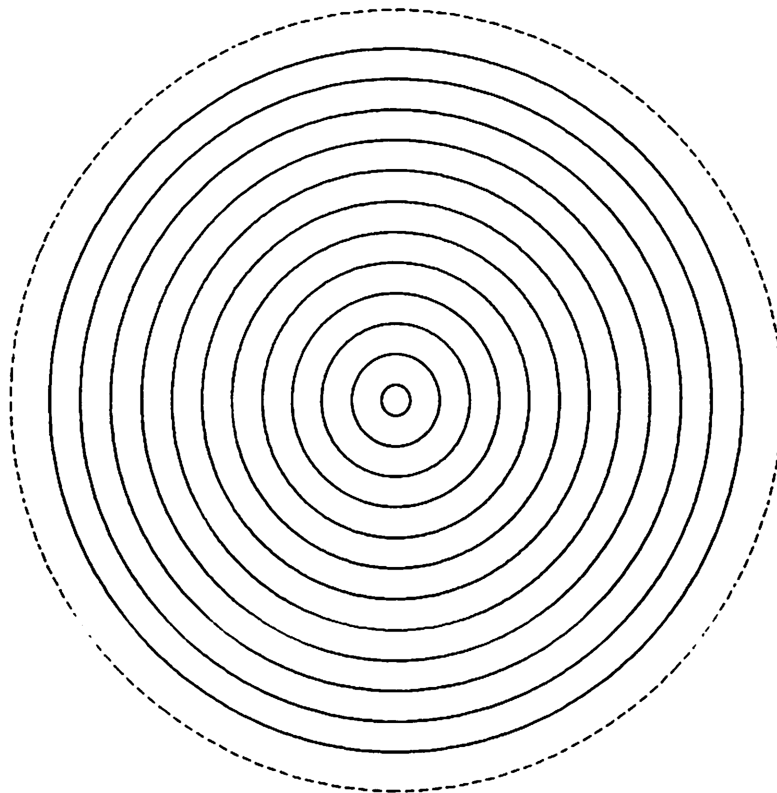


Fig. 5.5 Wafer locations inside the reactor for the radial uniformity experiments. Unlabeled wafers are blank dummy wafers. The front of the reactor is in the negative direction.

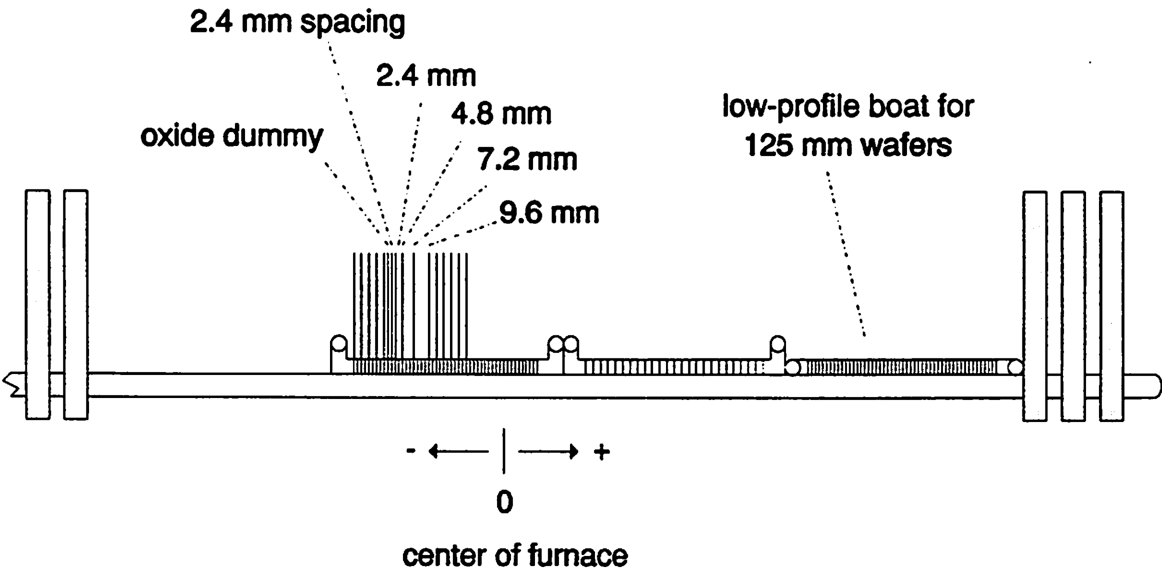


Fig. 5.6 Data from experiment 177 showing growth rate versus radial position across each wafer in the two sets of variably space wafers that had been placed (a) upstream, and (b) downstream.

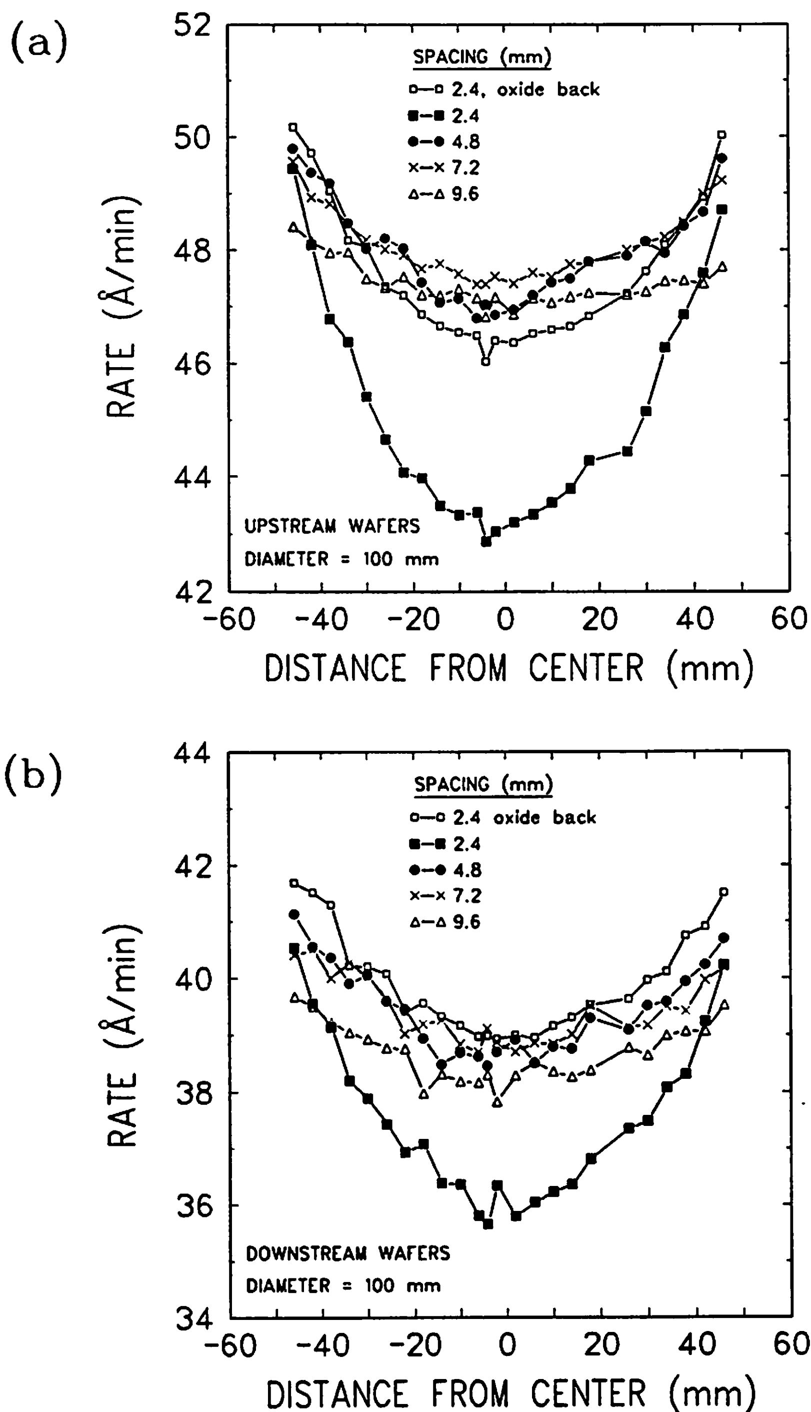
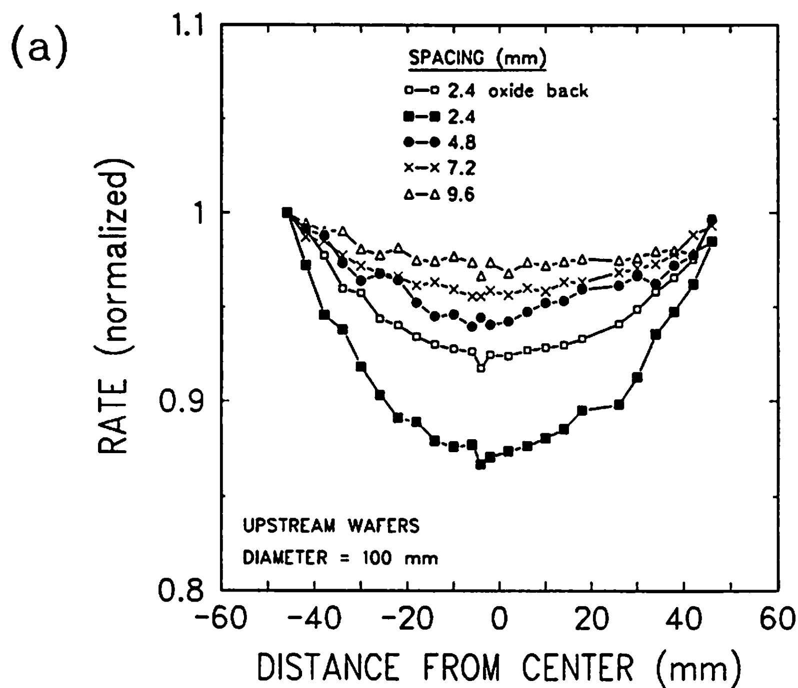


Fig. 5.7 Same data as in Fig. 5.6, except that the growth rate across each wafer is normalized to the rate at the left (negative distance) radial position. Left side of the wafer is expected to be less sensitive to flow effects.



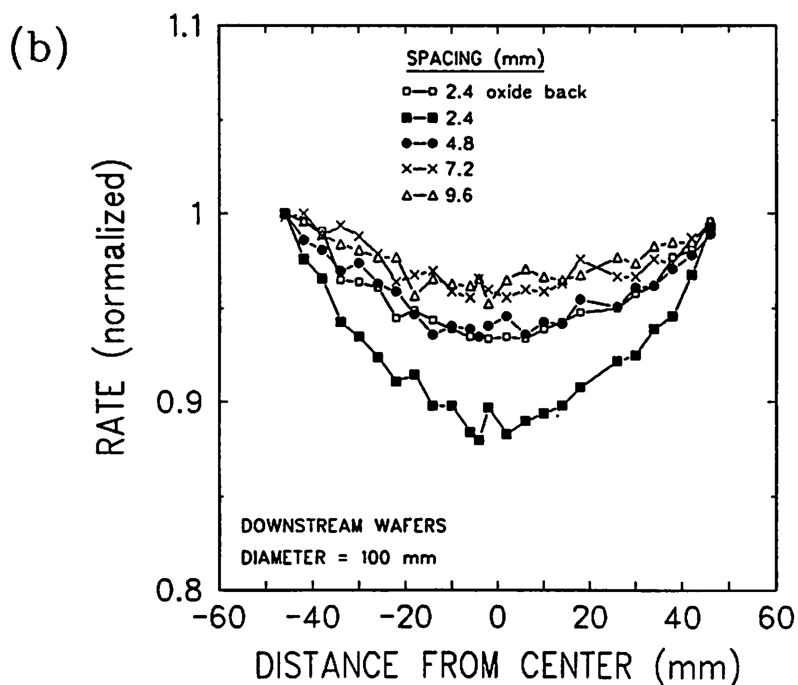


Fig. 5.8 Normalized growth rate versus position for the 2.4 mm spaced upstream wafer in experiment 177. Data across the left (negative) to right (positive) diameter are plotted together with the data from the top (negative) to bottom (positive) diameter, revealing the effect of the structure that supports the wafer at the bottom edge.

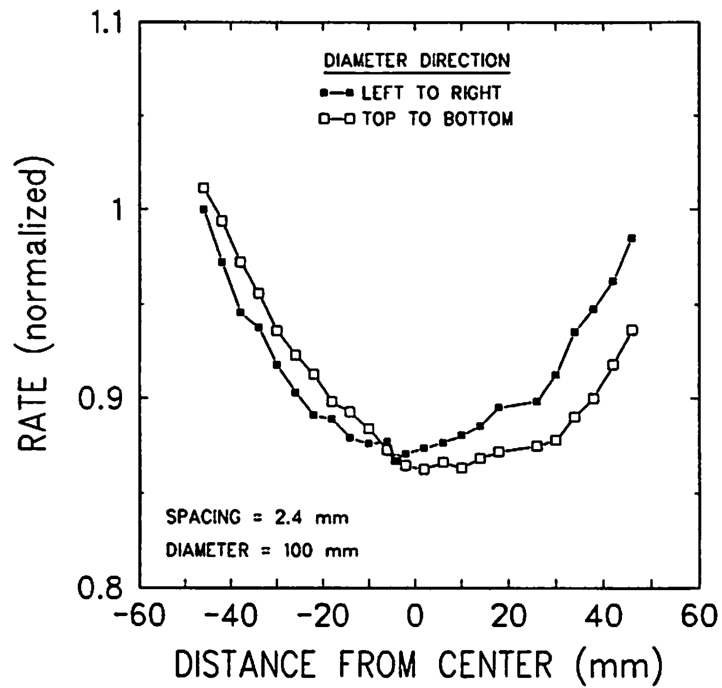


Fig. 5.9 Radial uniformity versus wafer diameter. Normalized growth rate profiles obtained from the 2.4 mm spaced wafers are shown in (a). The normalized growth rate at the center for each wafer is plotted versus spacing in (b). The model obtained by substituting (5.16) into (5.15) is shown by the solid line in (b).

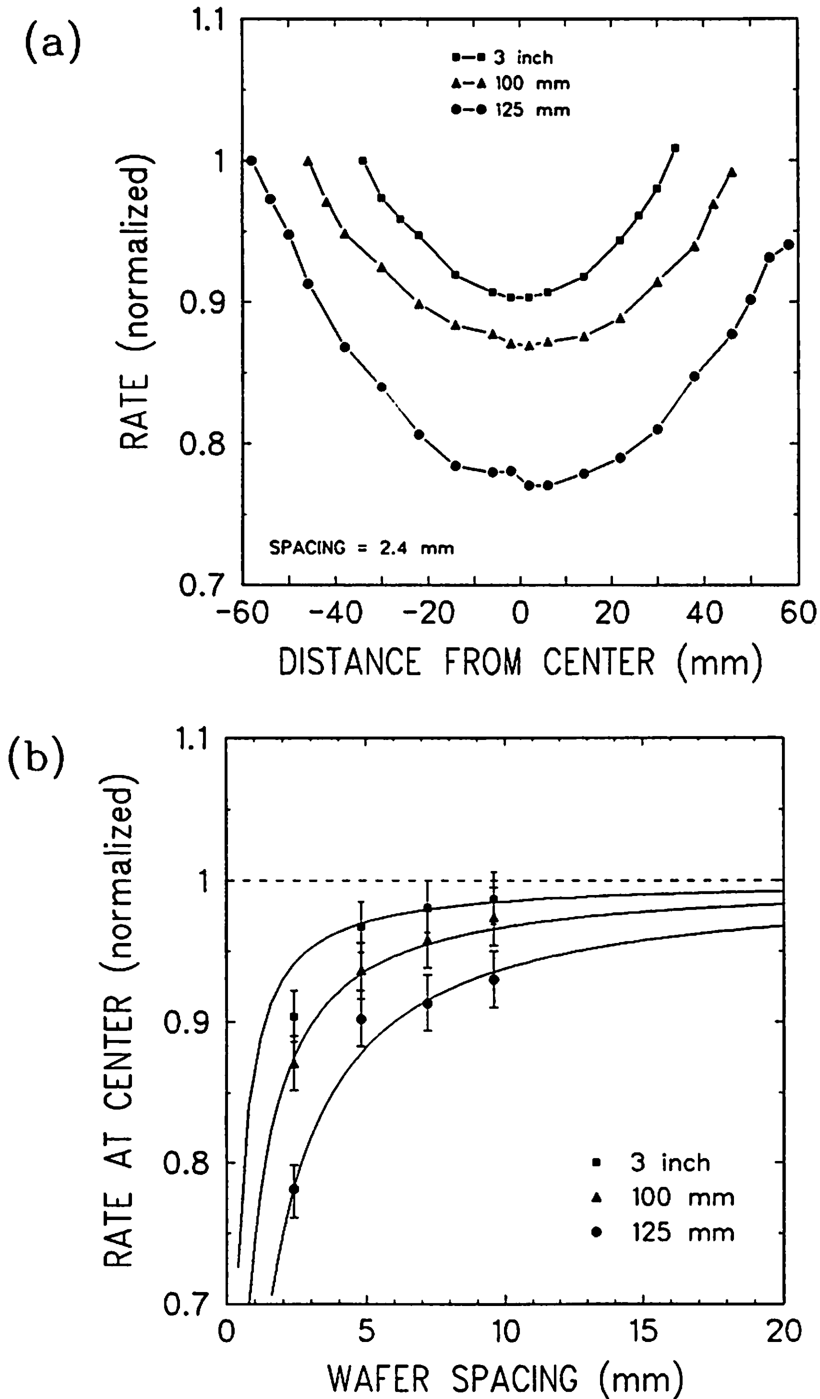


Fig. 5.10 Radial uniformity versus total pressure. Normalized growth rate profiles obtained from the 2.4 mm spaced wafers are shown in (a). The normalized growth rate at the center for each wafer is plotted versus spacing in (b). The model obtained by substituting (5.16) into (5.15) is shown by the solid lines in (b).

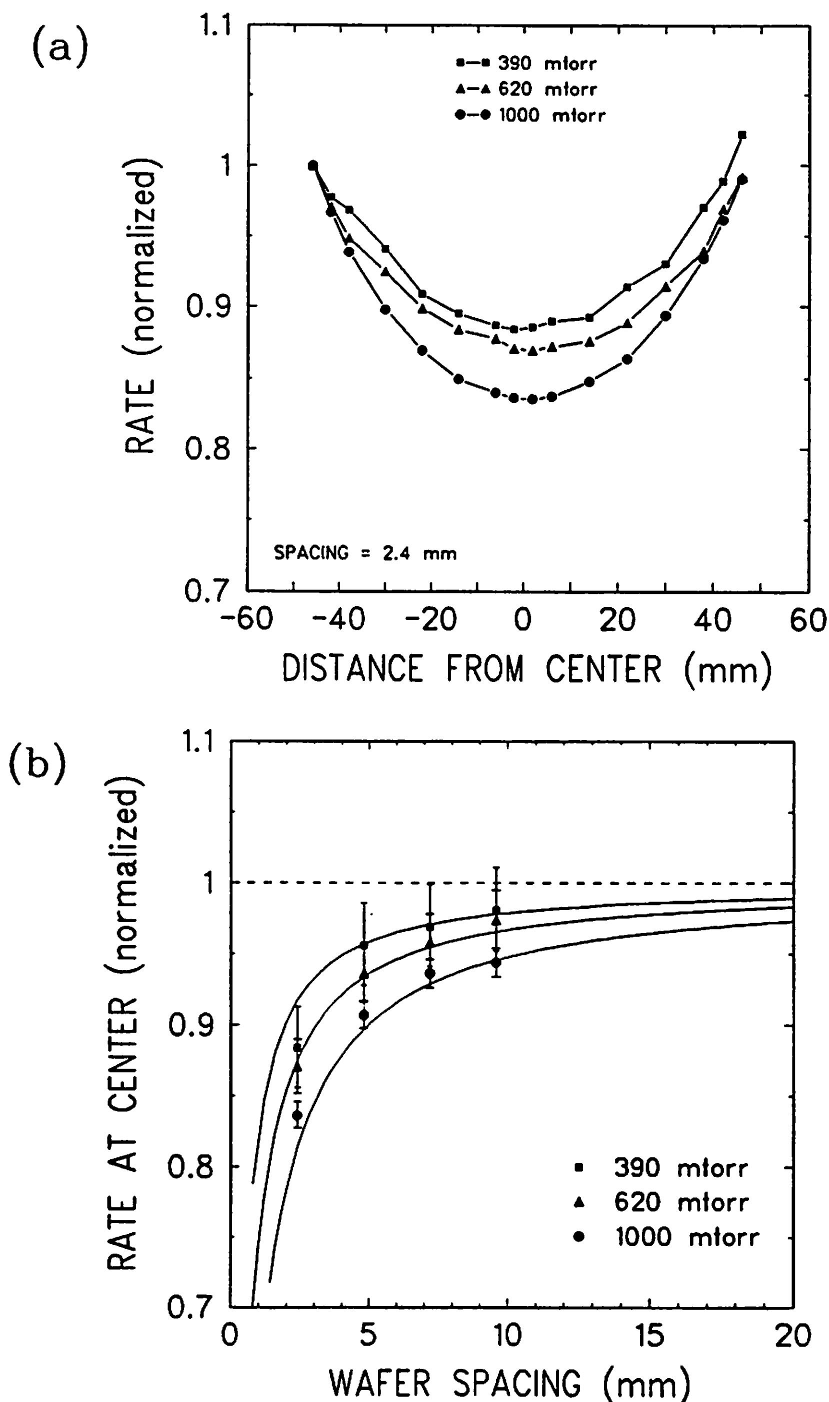


Fig. 5.11 Radial uniformity versus temperature. Normalized growth rate profiles obtained from the 2.4 mm spaced wafers are shown in (a). The normalized growth rate measured at the center for each wafer is plotted versus spacing in (b). The model obtained by substituting (5.16) into (5.15) is shown by the solid lines in (b).

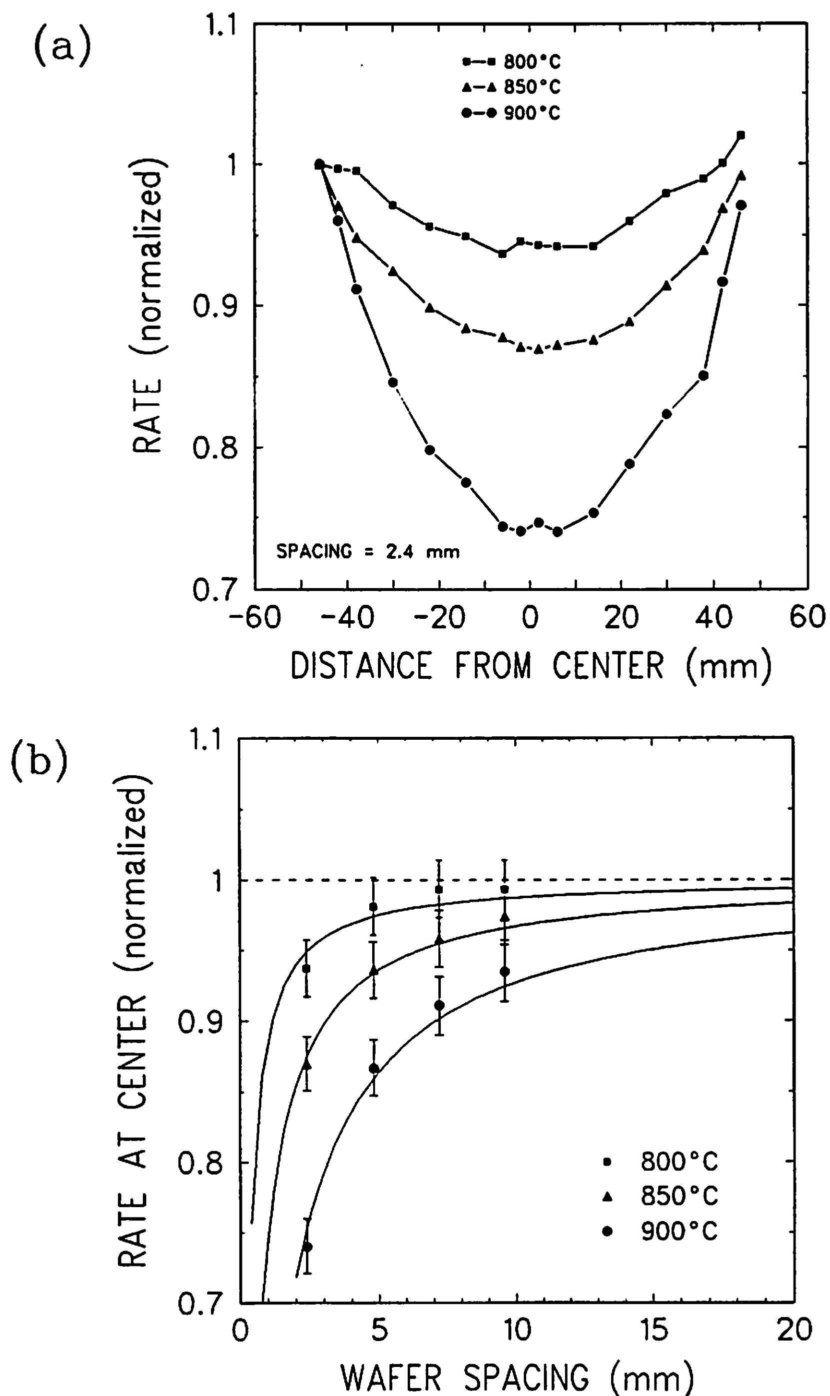


Fig. 5.12 Radial uniformity versus percent concentration of SiH_2Cl_2 (DCS) in H_2. Normalized growth rate profiles obtained from the 2.4 mm spaced wafers are shown in (a). The normalized growth rate measured at the center for each wafer is plotted versus spacing in (b). The model obtained by substituting (5.16) into (5.15) is shown by the solid lines in (b).

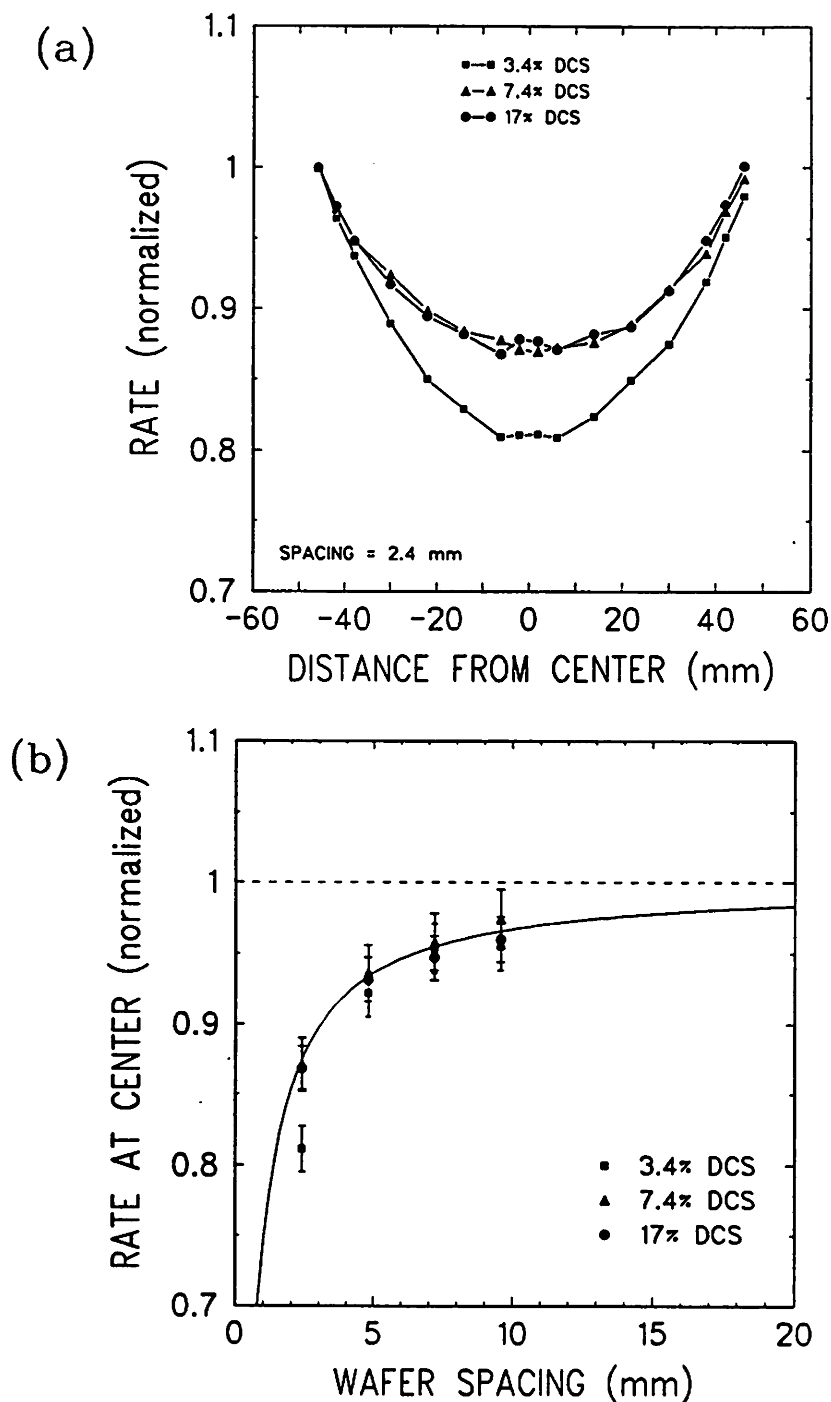


Fig. 5.13 Comparison between uniformity observed with an oxide coated wafer (α=0.95, spacing=2.4 mm) and a bare wafer (α=1.95, spacing=4.8 mm) in front of the measured wafer. Histogram (a) shows the rates for each of the cases versus experiment. Histogram (b) compares the observed difference and measurement uncertainty versus experiment.

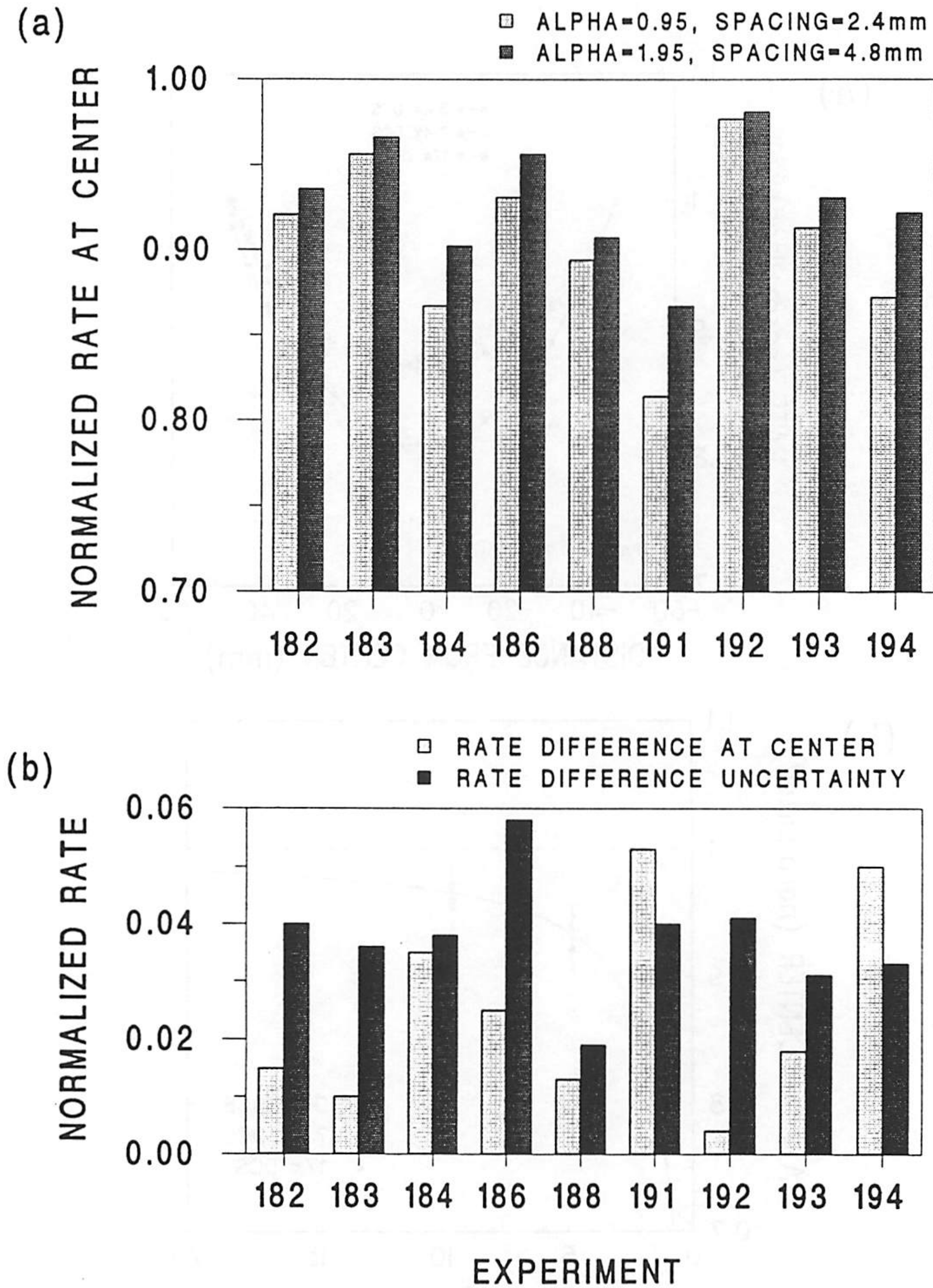
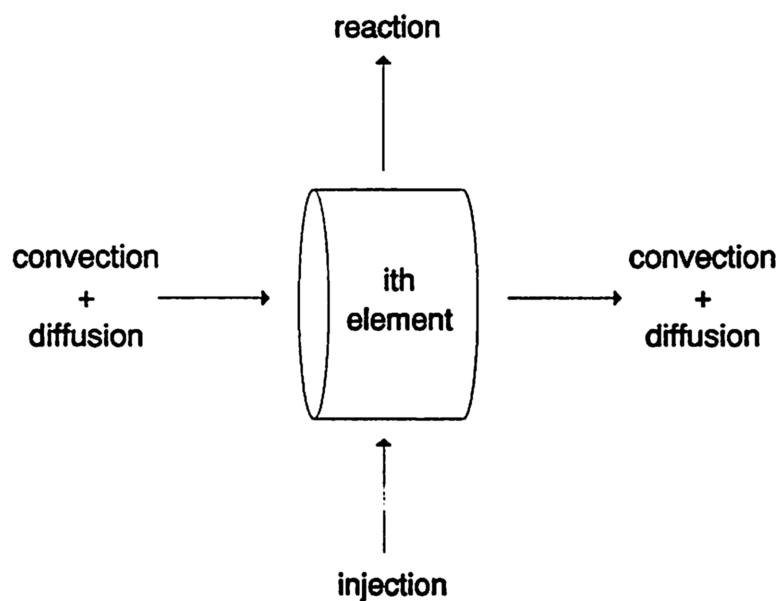


Fig. 5.14 Mass flows and reactor properties associated with the ith reactor element. The differential equation is obtained by taking the limit of $\Delta z \rightarrow 0$.



$\Delta Z(i)$ = length

$T(i)$ = temperature

$SL(i)$ = surface area / unit length

$XA(i)$ = cross sectional area

Fig. 5.15 Wafer locations inside the reactor for the longitudinal uniformity experiments. Unlabeled wafers are blank dummy wafers. The front of the reactor is in the negative direction.

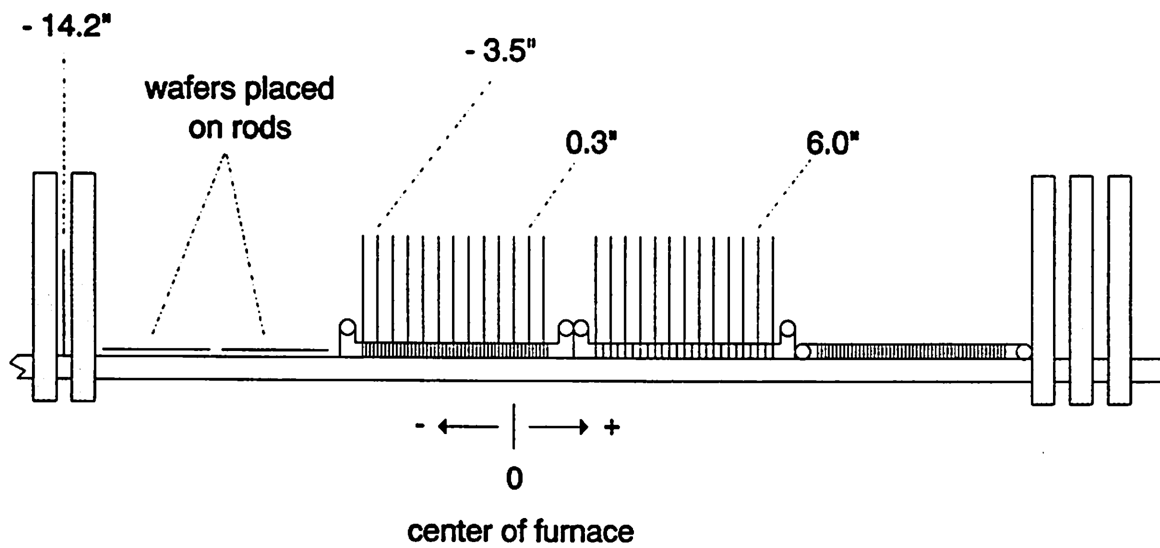


Fig. 5.16 Parameter profiles that describe our reactor during simulation of the longitudinal experiments. Cross sectional area is shown in (a), surface area per unit length is shown in (b), and measured temperature profiles for the three nominal set points are shown in (c).

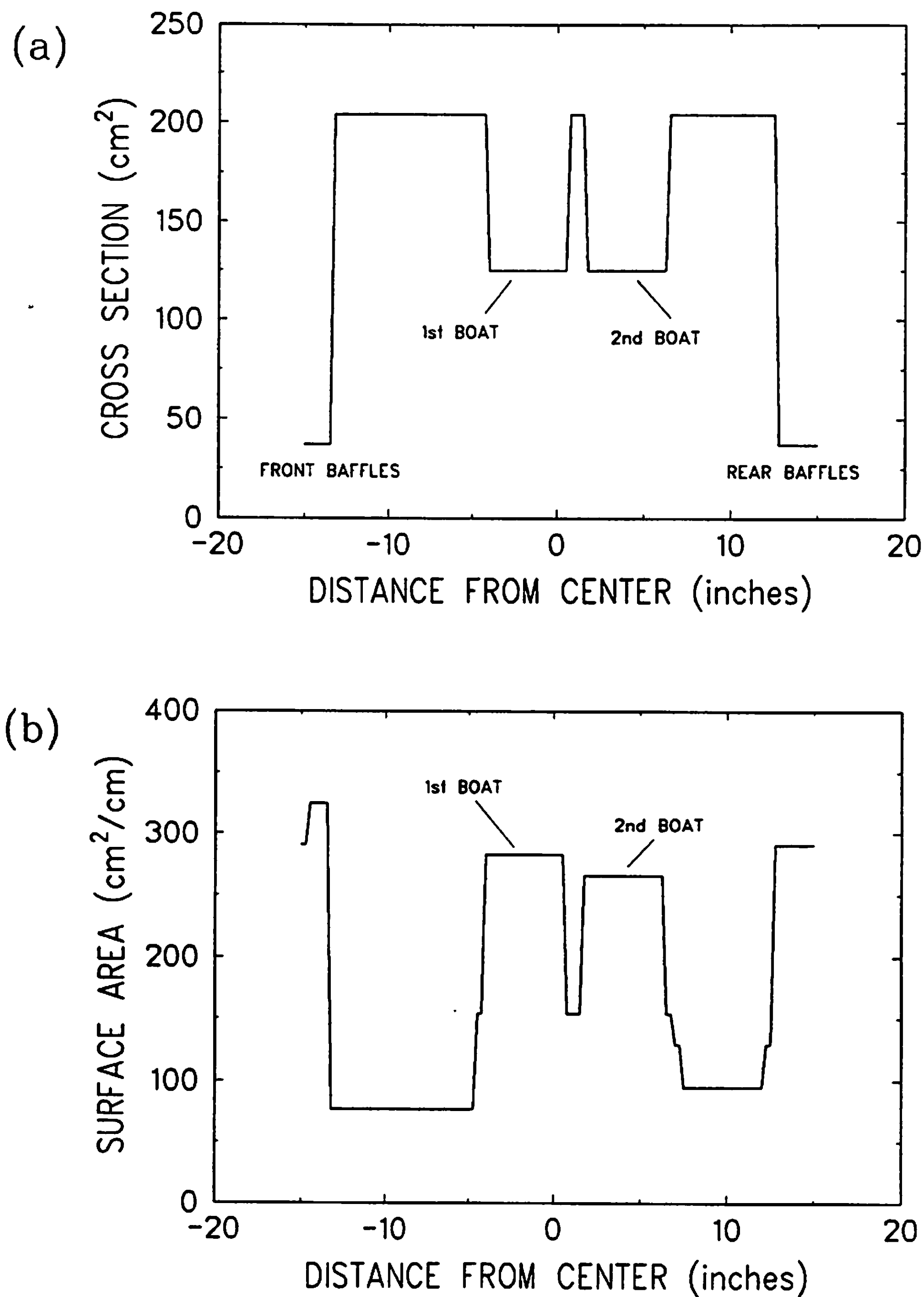


Fig. 5.16 (cont.)

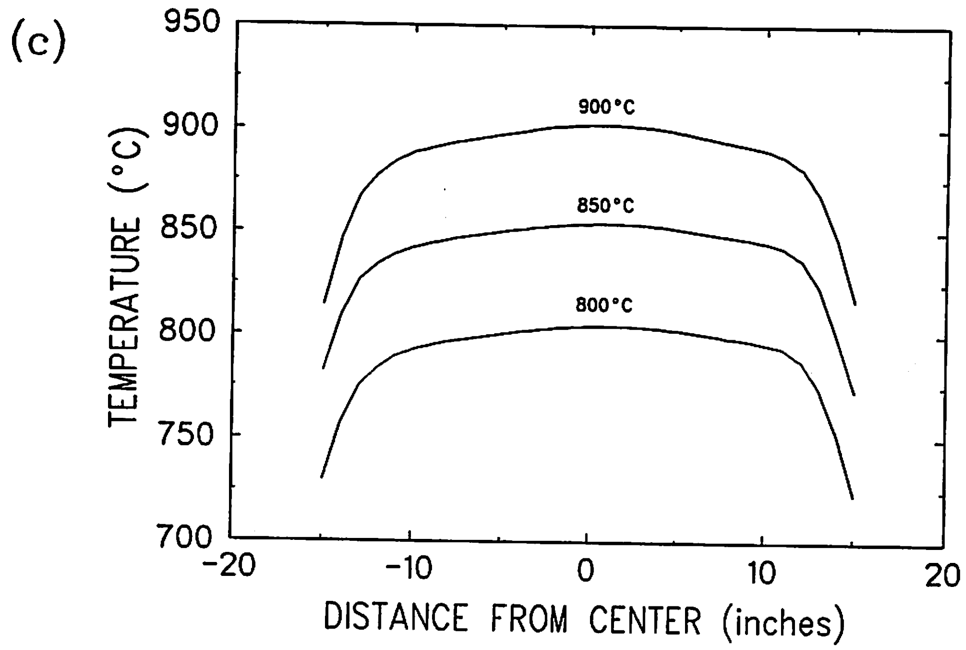


Fig. 5.17 Measured growth rate profiles are plotted together with simulated profiles for experiments varying: (a) temperature, (b) total pressure, and (c) percent concentration of SiH_2Cl_2 (DCS) in H_2. In (c) the simulated curve for DCS=16 represents the nominal concentration of 3.4%, and DCS=20 the result of a possible inaccuracy of the flow controller.

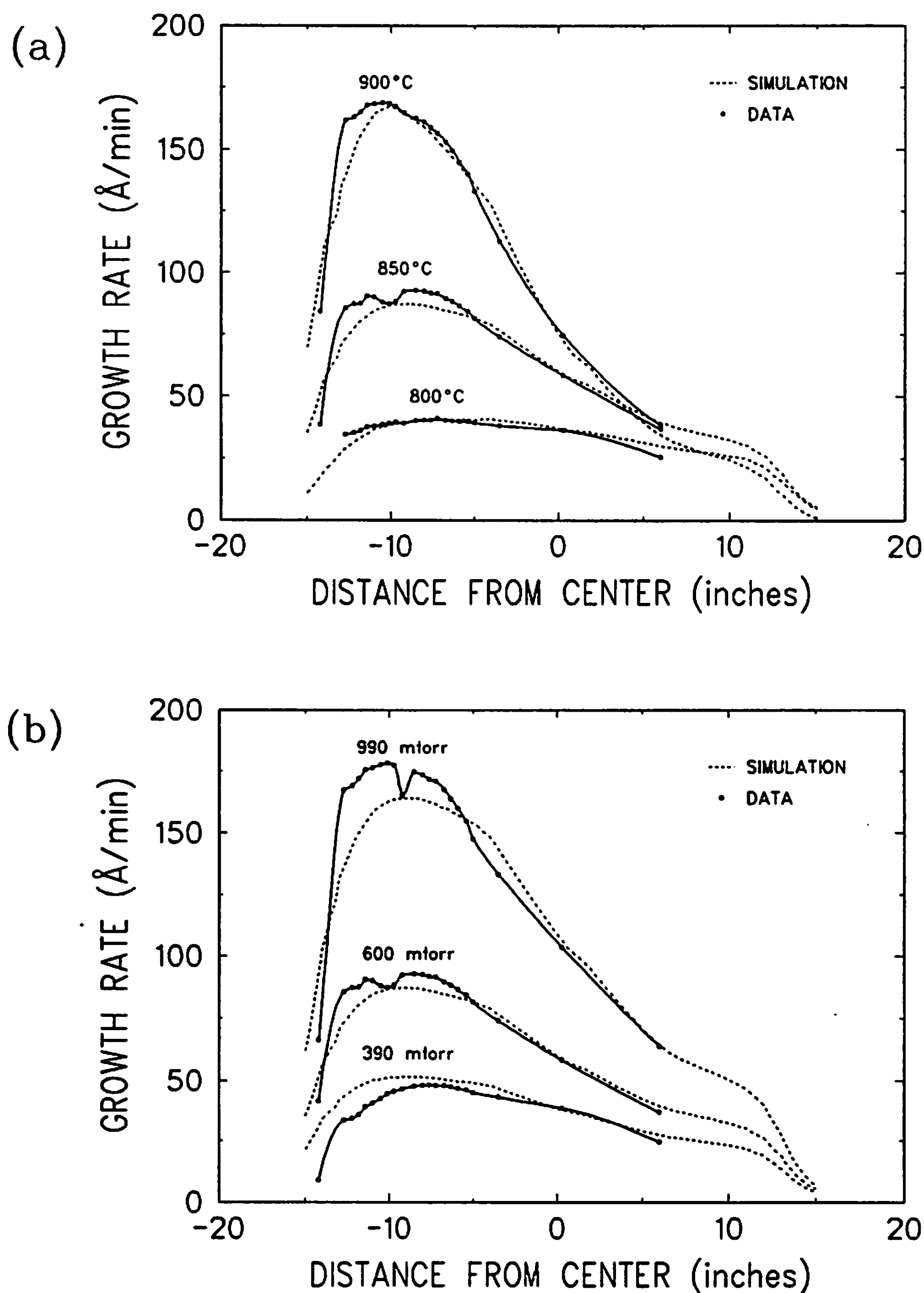


Fig. 5.17 (cont.)

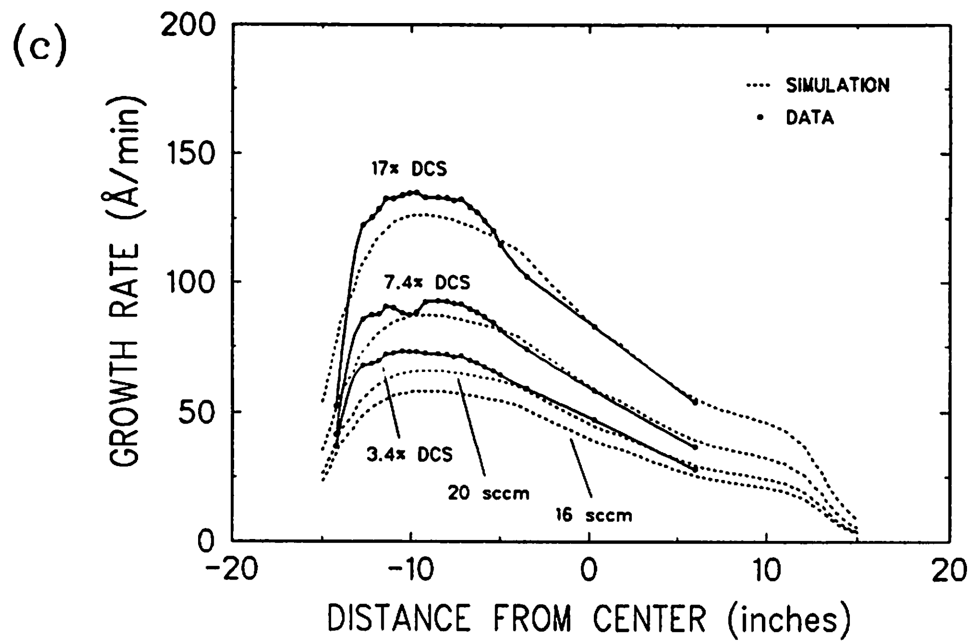
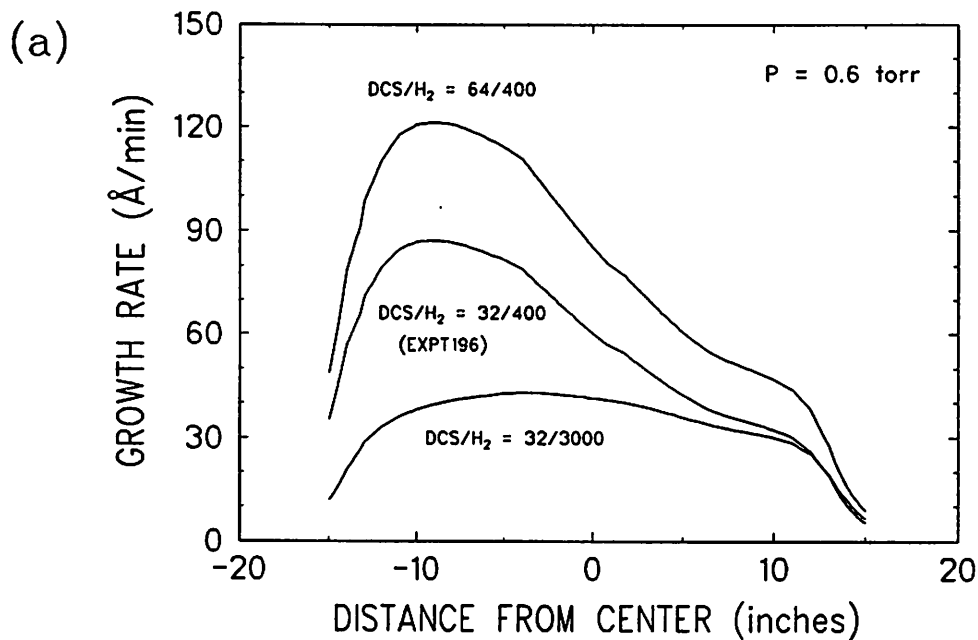


Fig. 5.18 Exploring possible changes to the conditions represented by experiment 196 (DCS/H_2=32/400, P=0.6 torr) that would result in a more uniform growth rate. The simulated cases are: (a) SiH_2Cl_2 or H_2 flow increased at a constant pressure of 0.6 torr, (b) H_2 flow increased at a constant pressure of 1.0 torr, and (c) SiH_2Cl_2 and H_2 flows increased together at constant pressure of 0.6 torr.



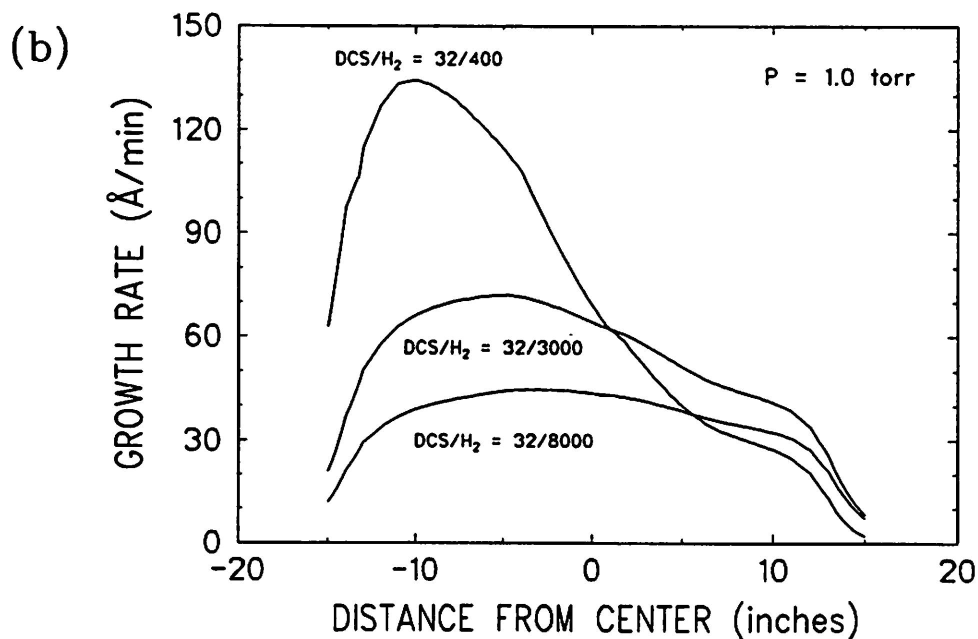


Fig. 5.18 (cont.)

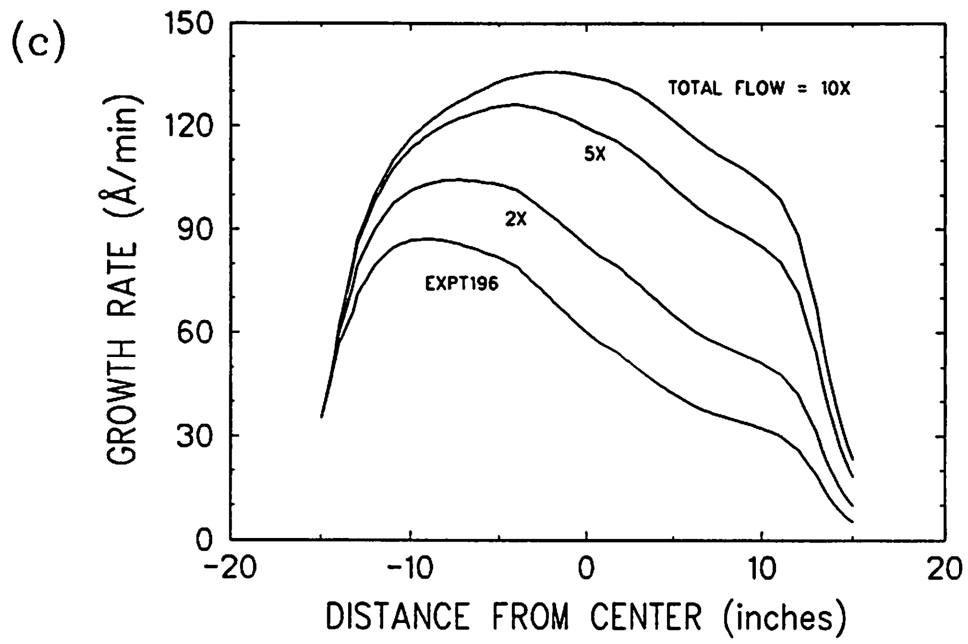


Fig. 5.19 Simulated growth profile illustrating the predicted effect on experiment 196 results by adding 3 injectors each supplying 32 sccm SiH_2Cl_2 (DCS).

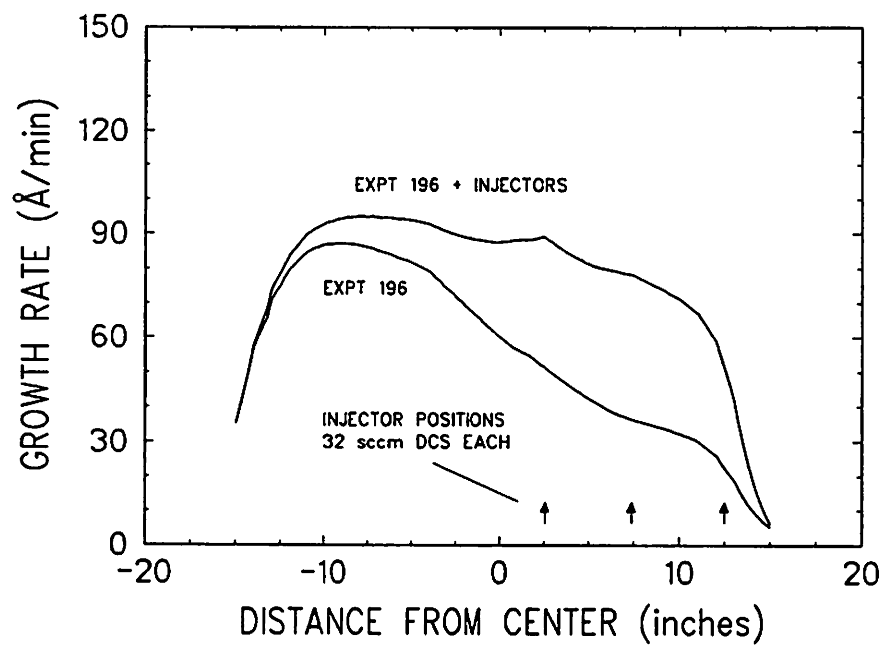


Fig. 5.20 Simulated growth profiles illustrating the predicted effects of changing the type of baffle that is used at the end zones of the reactor.

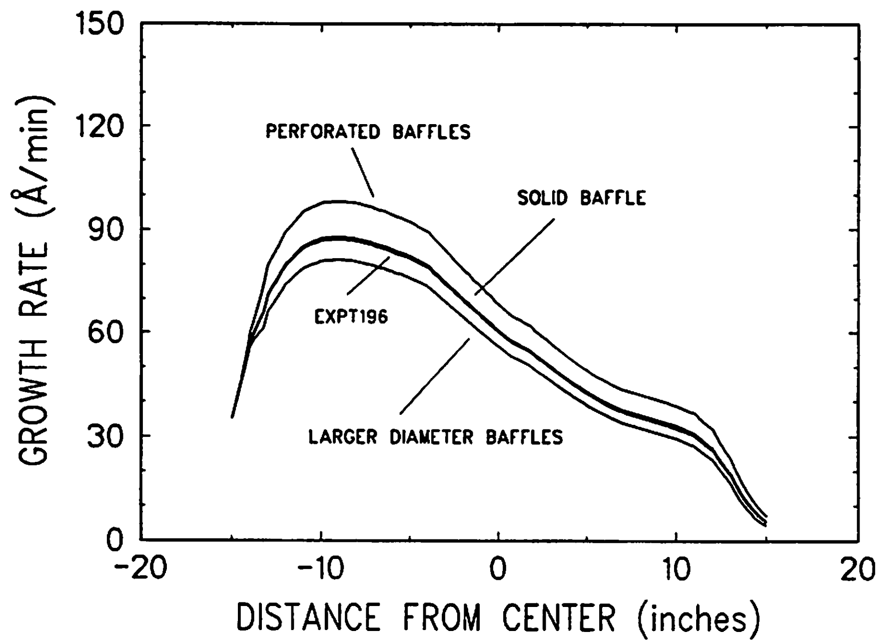


Fig. 5.21 Relationship between wafer spacing, temperature, and pressure for the specified R_w, ψ, and α of the hypothetical production-sized reactor.

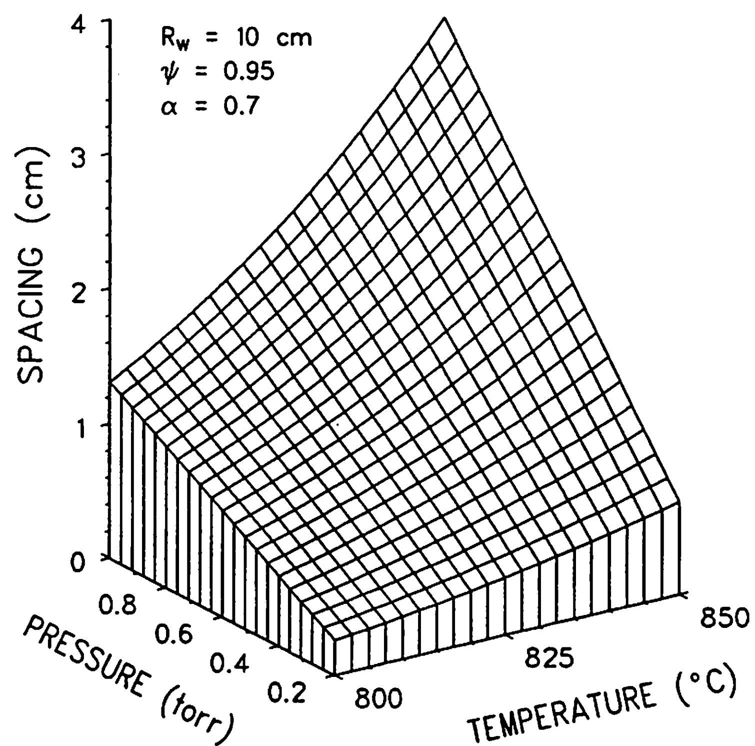


Fig. 5.22 Parameter profiles for the hypothetical production-sized reactor when loaded with 100 wafers 200 mm in diameter. The cross-sectional area (a), and surface area per unit length (b) are calculated by scaling our existing reactor. The temperature profile (c) is obtained by combining end zone profiles from our existing reactor with an ideally flat 840° C center profile.

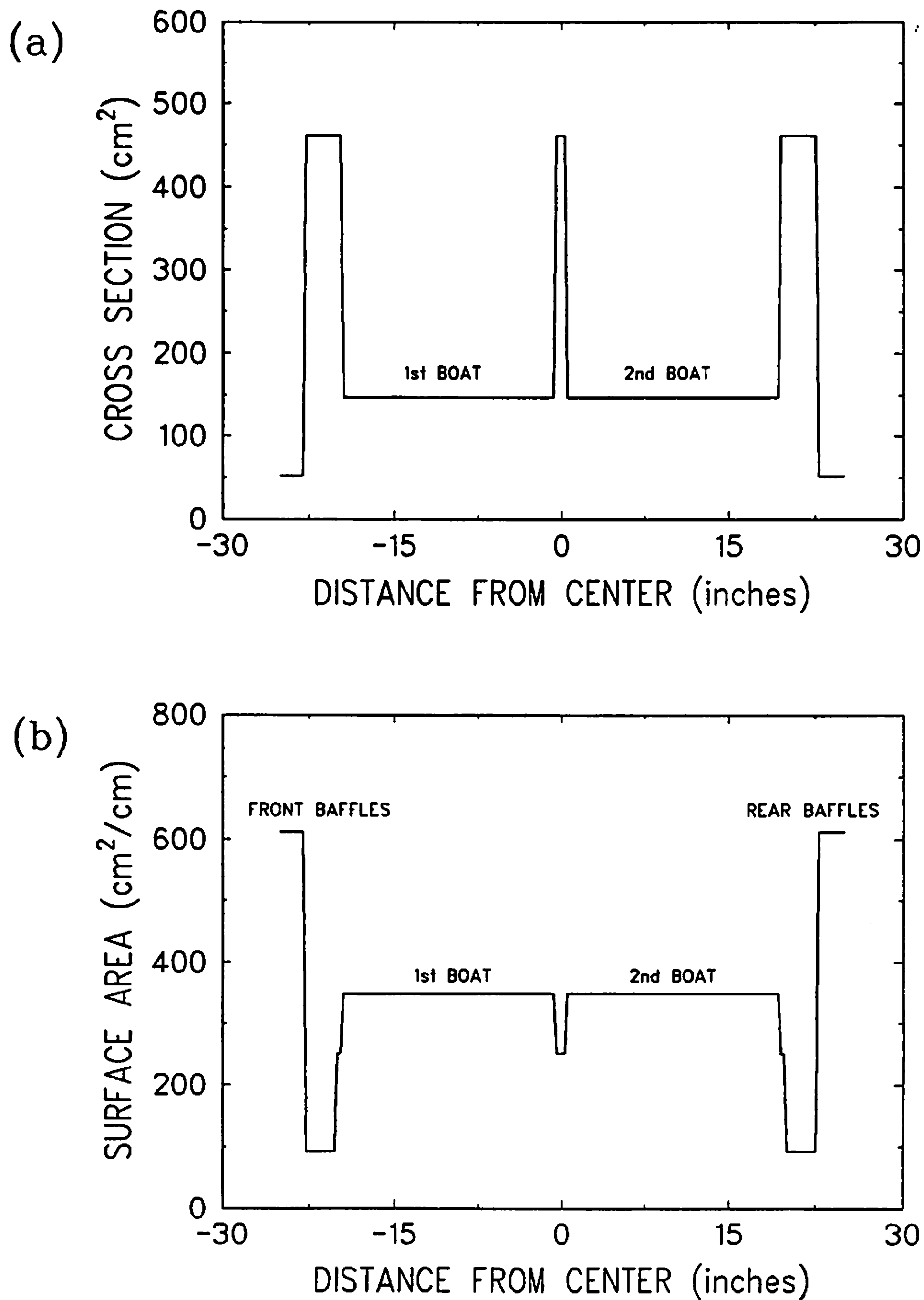


Fig. 5.22 (cont.)

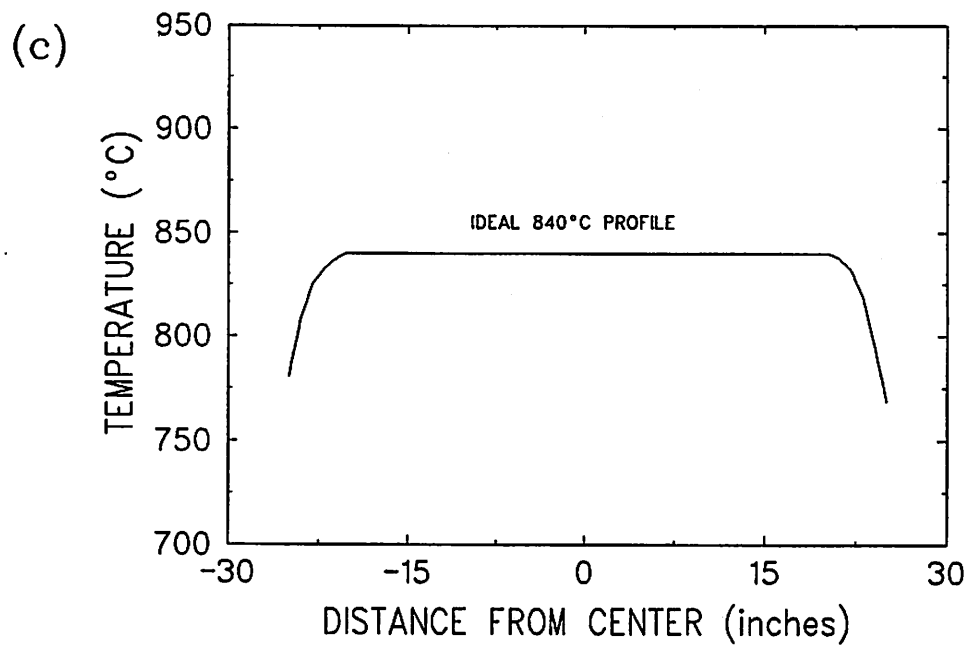
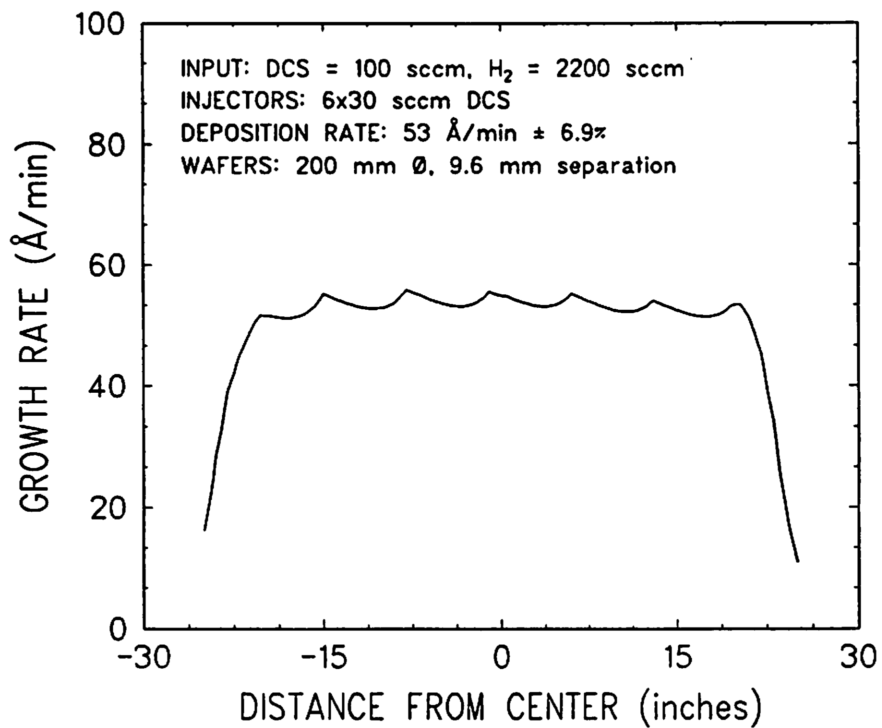


Fig. 5.23 Predicted growth rate profile for the hypothetical production-sized reactor when loaded with 100 wafers of 200 mm diameter.



Chapter 6
Future Work

6.1 Reactor Improvements

The capacity of the currently used rotary vane pump limits the total flow to 432 sccm at 0.6 torr. Increased pumping capacity by a factor of 4 to 7 is possible by the installation of a Roots blower in series with the currently used rotary vane pump. The Roots blower allows the rotary vane pump to operate at higher pressures where it is more efficient, providing the additional benefit of reducing the chance that backstreaming oil from the rotary vane pump will contaminate the reactor.

The reduction in total pressure after the low-pressure bake described in Chapter 3 suggests the presence of adsorbed H_2O inside the reactor. An increase in H_2O that is adsorbed from the air during loading was also observed qualitatively by using a mass spectrometer. The signal of peak 18, which corresponds mostly to H_2O, is shown in Fig. 6.1(a) versus time after the reactor was opened and then evacuated to 0.5 torr. The N_2 flow rate was 500 sccm and the reactor temperature was 525° C. A much larger signal for mass peak 18 is seen if the system is open longer, and if rear injected N_2 is not used while the reactor is open. The signal for mass peak 32, corresponding mainly to O_2 which is not expected to adsorb, decreases more quickly. A load-locked system reduces the amount of H_2O and O_2 that enter the system as a result of exposure to air. However, a true load-lock would be very difficult to implement on our system, but there exists the alternative of building a nitrogen purged box that would surround the door and cantilever while extracted from the reactor tube. To reduce adsorption of H_2O, the loading box could incorporate a UV light source in addition to the nitrogen purge.

Before a loading box is built, there are two more easily implemented improvements that can be made to the system. In the current system the mass flow controllers (MFC's) are located on a gas shelf approximately 5 m from the front injection point. There is no provision for protecting this tubing from exposure to air other than purging it with N_2 during loading. The first proposed improvement would be to modify the gas injection system as illustrated in Fig. 6.2. A pair of manual 2-way valves on each side of the MFC allows it to be serviced and purged without contaminating the injection tubing. An automatically actuated 2 way-valve mounted as close as possible to the injection point at the front of the reactor prevents the injection tubing from exposure to air when the reactor is open. Furthermore, the ability to bypass the reactor allows turn-on transients to be eliminated by establishing the flow in the injector before connecting it to the reactor. The ideal situation would be to use 3 separate injection tubes, one for N_2, one for the high flow of H_2 during bakes, and one for a mixture of SiH_2Cl_2 and H_2 during deposition. A second improvement to the system would be to install heaters on the door and cantilever block to raise their temperature above the maximum temperature reached during reactor operation (approximately 50° C). The heaters would be turned on by the controller before venting the system, remain on while the reactor is open, and then be turned off as the system is pumped down. This would ensure that the door and cantilever block do not release any adsorbed H_2O during reactor operation.

6.2 Mass Spectrometer Measurements

Mass spectrometer measurements in the pressure range of 0.5 to 5 torr turned out to be more difficult than anticipated. It was initially hoped that concentrations as low as a few ppm of H_2O could be measured by using an enclosed ion-source on the mass spec-

trometer. The mass spectrometer was installed as closely as possible to the output of the reactor as shown in Appendix A.1.

A practical problem was the poor reliability of the turbo pump connected to the mass-spectrometer. The frequent shut-downs would not allow the analyzer to reach stable operation in terms of its background level of H_2O and pump oil, making consistent measurements difficult. More fundamental difficulties were encountered with the enclosed ion-source and chemistry of SiH_2Cl_2. To achieve an increased sensitivity to the sampled gas versus the background in the analyzer, the enclosed ion-source is operated at a pressure approximately two orders of magnitude higher than the analyzer portion. The effect of this type of ion-source is that the amount of background concentration contributed by the analyzer during measurements cannot be measured by closing the sampling port. Furthermore, the readings obtained by the analyzer depend strongly on the pressure of the enclosed ion-source, which in turn depends on the conductance of the sampling port and the pressure that is sampled. The pressure of the enclosed ion-source cannot be measured directly, and the ion-source must be operated close to saturation for the main components in order to resolve 1 ppm for background values. Calibration must, therefore, be made at each pressure that will be sampled. An additional consideration with the enclosed ion-source is increased ionic shielding effects due to easily ionized species, which makes calibration dependent on the gaseous species involved (i.e. H_2O in N_2 is not equivalent to H_2O in H_2). The relative amounts of ions (cracking pattern) generated by the source also depend on the pressure of the source and will be different than the commonly tabulated values that have been obtained in mass spectrometers operating with standard ion-source. Analysis of the gas composition during deposition is especially difficult because the cracking pattern of SiH_2Cl_2 is extremely complicated, and products such as HCl adsorb inside the analyzer.

If mass spectrometer analysis is to be attempted in future experiments the following features should be incorporated in the installation: a more reliable pump that should be able to run a year between maintenance shut-downs; calibrated sources of the same composition at the same pressure as the reactor; and the ability to sample both feed and exhaust in order to monitor the effect of the reactor as the difference between the two complex SiH_2Cl_2 cracking patterns.

6.3 Epitaxial Deposition Experiments

The addition of a larger capacity vacuum pump as proposed previously would allow more latitude in designing experiments that can be used to establish both fundamental epitaxial deposition characteristics and practical aspects of the hot-wall reactor approach. As seen in Chapter 2 and 3, internal sources of H_2O are likely causes of the current temperature limitations. The ability to conduct experiments with higher total flow rates at constant pressure would allow the contribution of these H_2O sources to be determined. Deposition temperatures could also be reduced because the H_2O background is diluted by the larger flow. Likewise, internal sources of carbon versus carbon contamination of the gas source could be distinguished by varying the flow rate at constant pressure. Finally, higher total flow rates could be used to further evaluate the proposed model in Chapter 5, and to produce more uniform growth along the reactor.

There are several unresolved issues introduced in Chapter 3 that require further investigation. For example, the role of oxide in influencing the growth rate, defect formation, and background doping remains to be established. Square pits of uniform size are commonly observed in association with interfacial oxide. It is not understood how they form. As shown in Chapter 3, it is difficult to explain their uniform size if it is simply

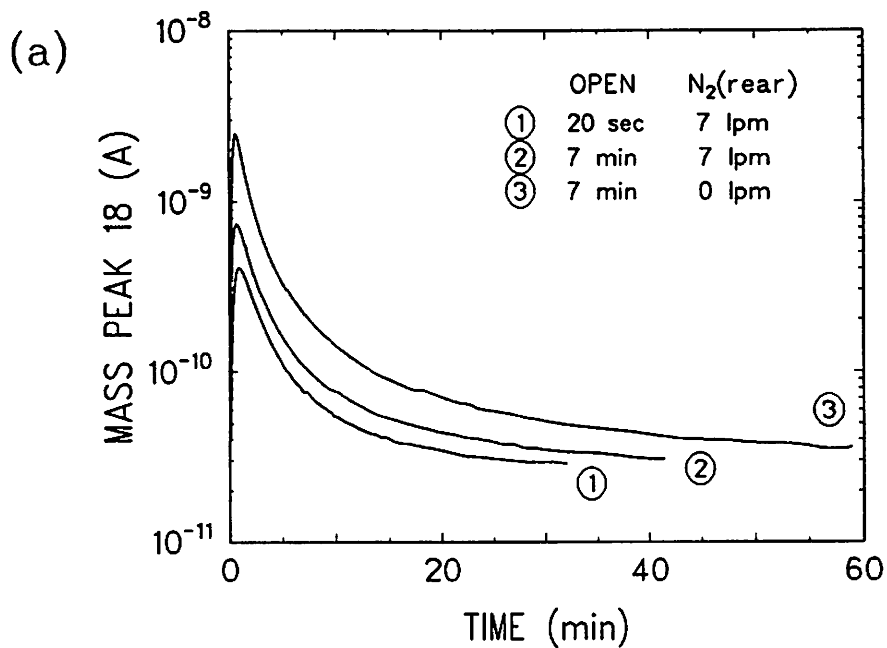
assumed that they result from incomplete overgrowth. It is also difficult to explain the smoothly overgrown oxide patches that are revealed by defect etching in regions that also contain the square pits. If square pits are related to overgrowth, then their characteristics can be explored by using lateral overgrowth experiments. Chapter 3 also showed that oxygen diffuses significantly and could be the cause of the background doping by formation of thermal dopant formation. The effect of significant amounts of oxygen diffusing from oxide patches on the substrate and oxide sidewalls may affect the growth kinetics in those regions.

Another area which needs future work is the kinetics of the oxide removal process, and the passivation (if any) that results from the HF vapor etch. The data presented by Ghidini and Smith presented in Chapters 2 and 3 was measured by introducing only H_2O. The effect of H_2O in an excess of H_2 remains to be investigated. The oxide removal process appears to proceed along the silicon interface, as discussed in Chapter 4, but it this does not explain the width of the oxide undercut without also invoking some gaseous or surface diffusion process that allows for silicon and oxygen transport between oxide and silicon areas. The common belief is that silicon surfaces form a native oxide within minutes after exposure to air which seems to require that the HF vapor treatment in Chapter 4 prevents native oxide formation, yet the published data on surface coverage has found very little fluorine on the surface. The amount of time that an HF vapor versus HF dip protects a silicon from native oxide formation should be measured to help explain the reduction in bake temperature that this process allows.

Finally, the topic of in-situ doping for epitaxial films has not been addressed in this work, but will eventually have to be investigated. The surface-rate controlled regime of a hot-wall reactor may make it difficult to independently vary the doping level, and uniformity problems may occur because of depletion effects.

Fig. 6.1 Mass spectrometer signals measured after the reactor was open for 20 seconds with N_2 rear on, 7 minutes with N_2 rear on, and 7 minutes with N_2 rear off. The signals were monitored versus time at 0.5 torr and an N_2 flow rate of 500 sccm. Signal at mass peak 18 corresponding to the presence of H_2O is shown in (a), and signal for mass peak 32 corresponding to the presence of O_2 is shown in (b).

(a)



(b)

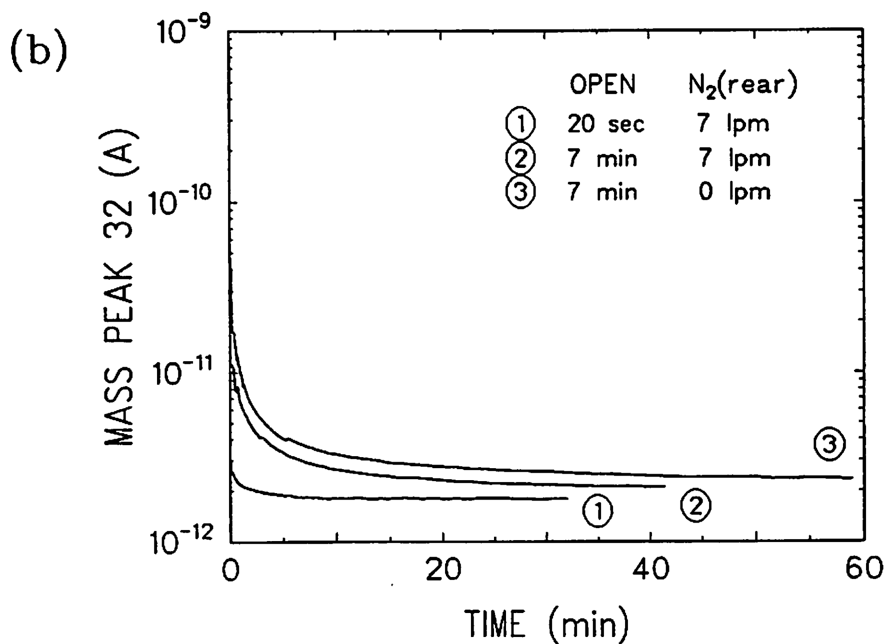
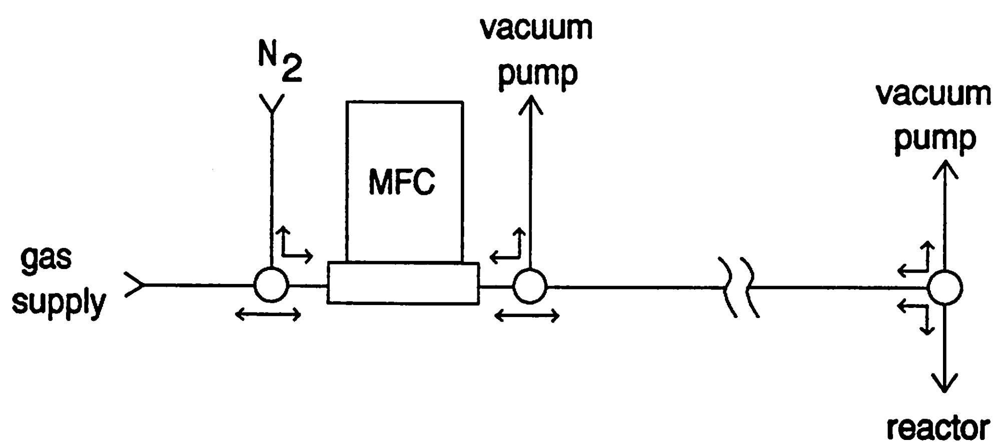


Fig. 6.2 Proposed improvement to gas injection system. Three 2-way valves would be added as shown, allowing replacement of the mass flow controller (MFC) and opening of the reactor without exposing the injection tubing to air. Turn on transients can also be avoided by bypassing the reactor until the flow is stable.



Chapter 7
Conclusion

A low-pressure hot-wall epitaxial silicon reactor has been designed, constructed, and successfully operated. Defect-free epitaxial layers are deposited at 850° C. Electrical evaluation of MOS devices fabricated on epitaxial layers deposited in the hot-wall reactor reveal no degradation compared to standard substrates processed in our Microlab facility. The reactor was built as a prototype system by modifying an existing LPCVD furnace, using as much of the original structure and control circuitry as possible. The reactor is, therefore, a strong statement for the feasibility of the hot-wall reactor approach.

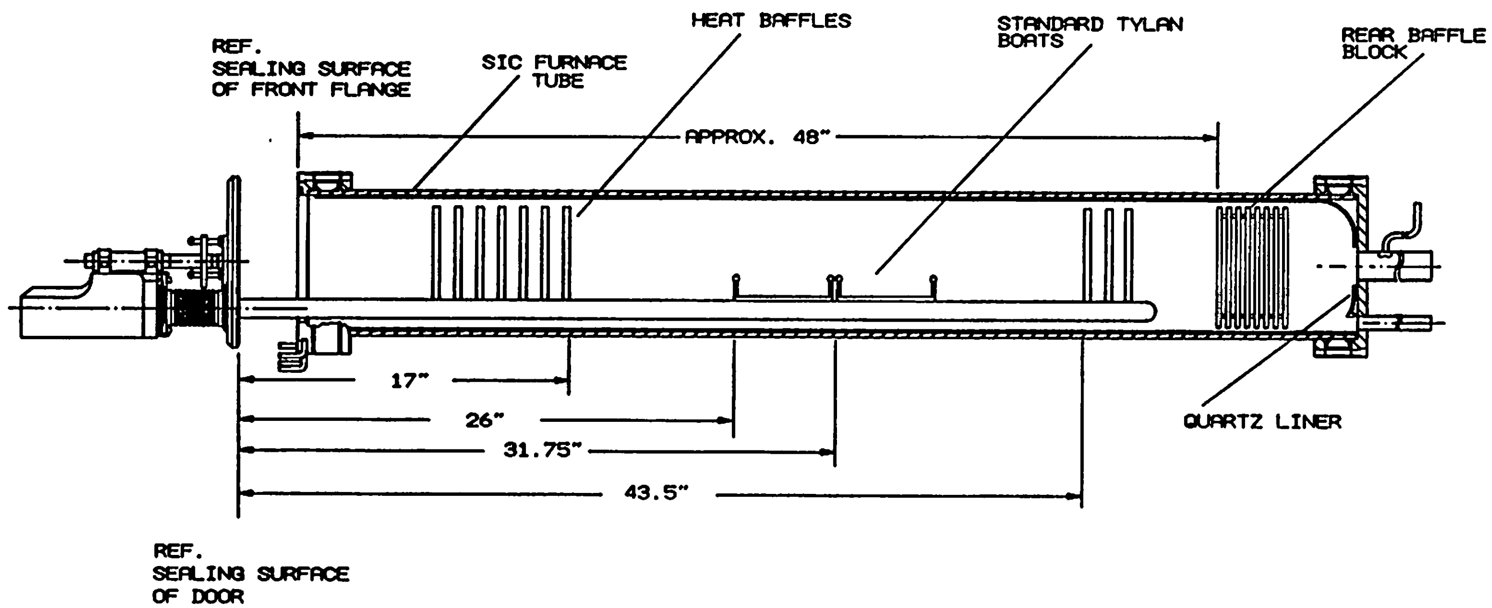
The reactor in its current configuration has two limitations that can be improved. Adsorption of H_2O to internal surfaces of the door assembly while the reactor is open causes a bake-out effect, releasing H_2O inside the reactor during the H_2 bake. The vacuum pump capacity is currently not large enough to demonstrate uniform deposition rate along the reactor. A fundamental problem that cannot be changed is the increase in $\sqrt{Dt}$ resulting from the slow changes in temperature and low growth rate in the hot-wall system.

A one-dimensional mass-transport model can predict observed growth rate profiles over a wide range of temperature, pressure, and composition. The model predicts that a production-sized reactor accommodating 100 wafers with 200 mm diameter is feasible.

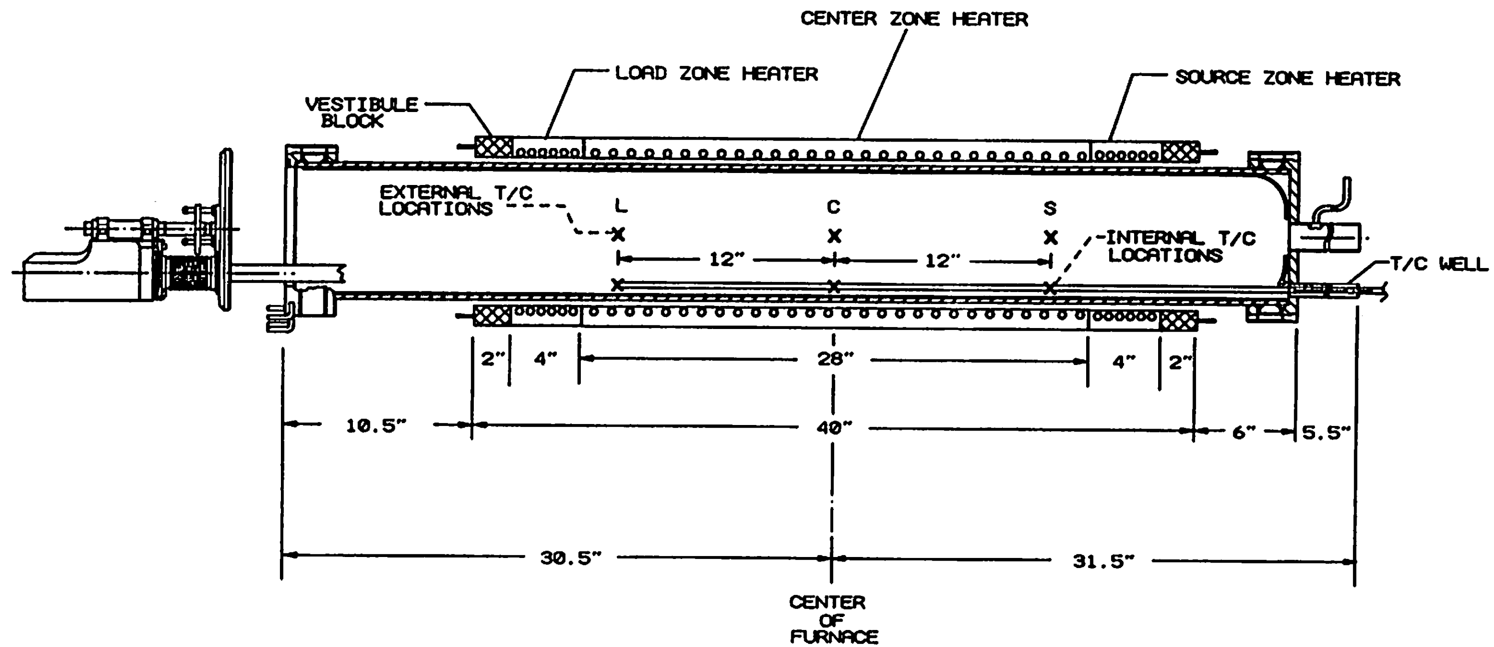
Appendix

A.1

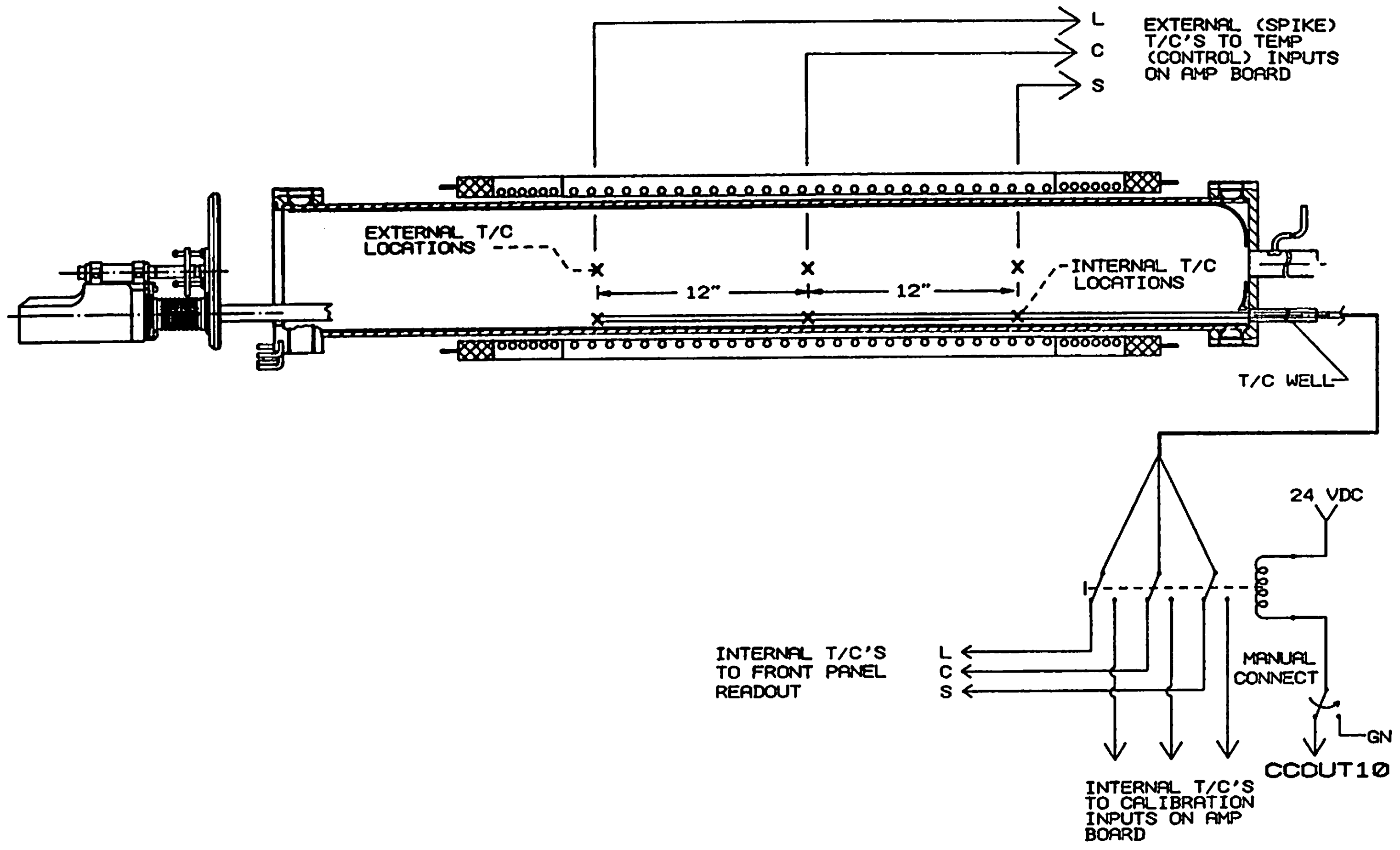
Epitaxial System Drawings



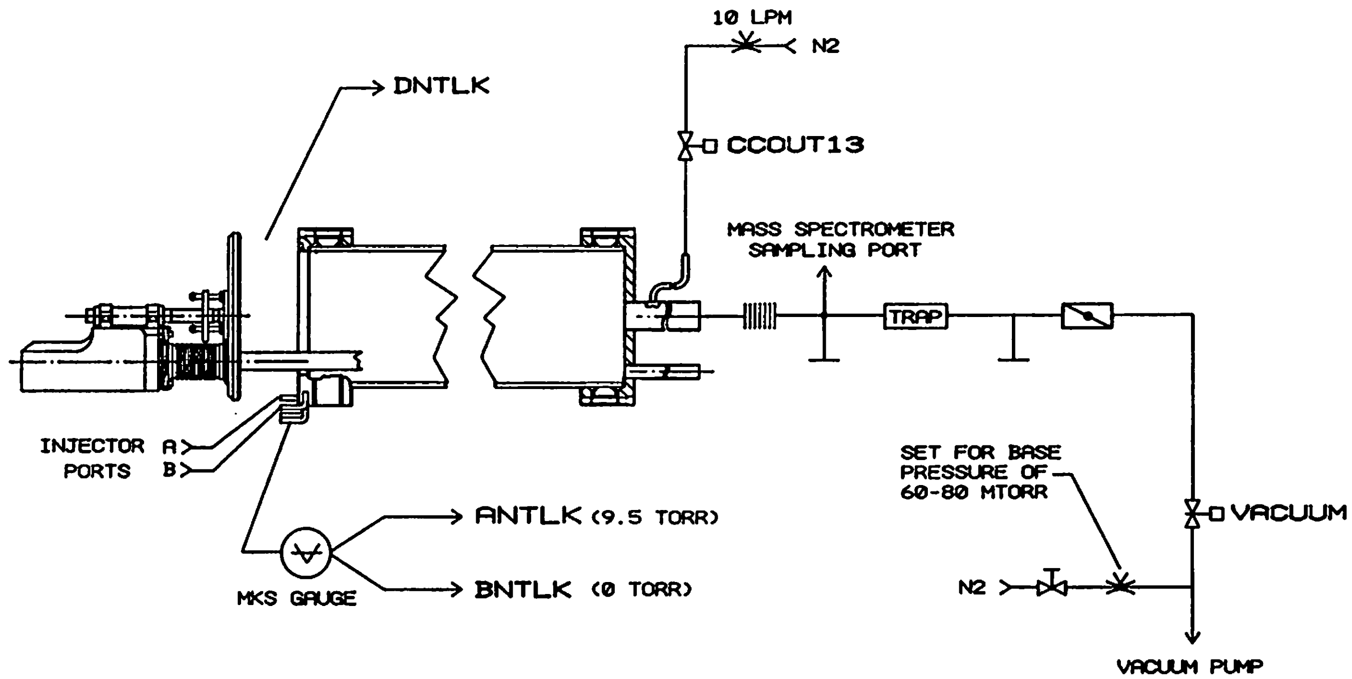
Drw. 1: Quartzware locations inside reactor.



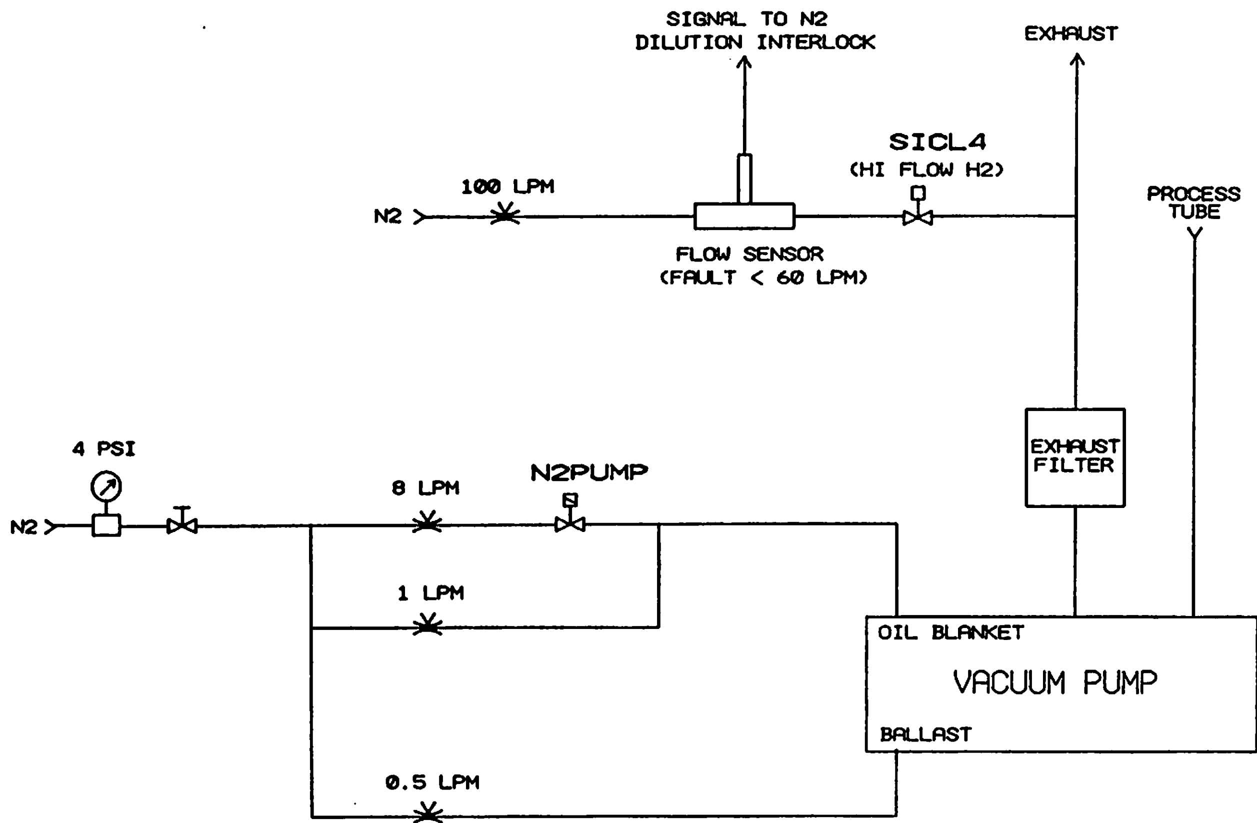
Drw. 2: Heater and thermocouple locations with respect to the reactor tube.



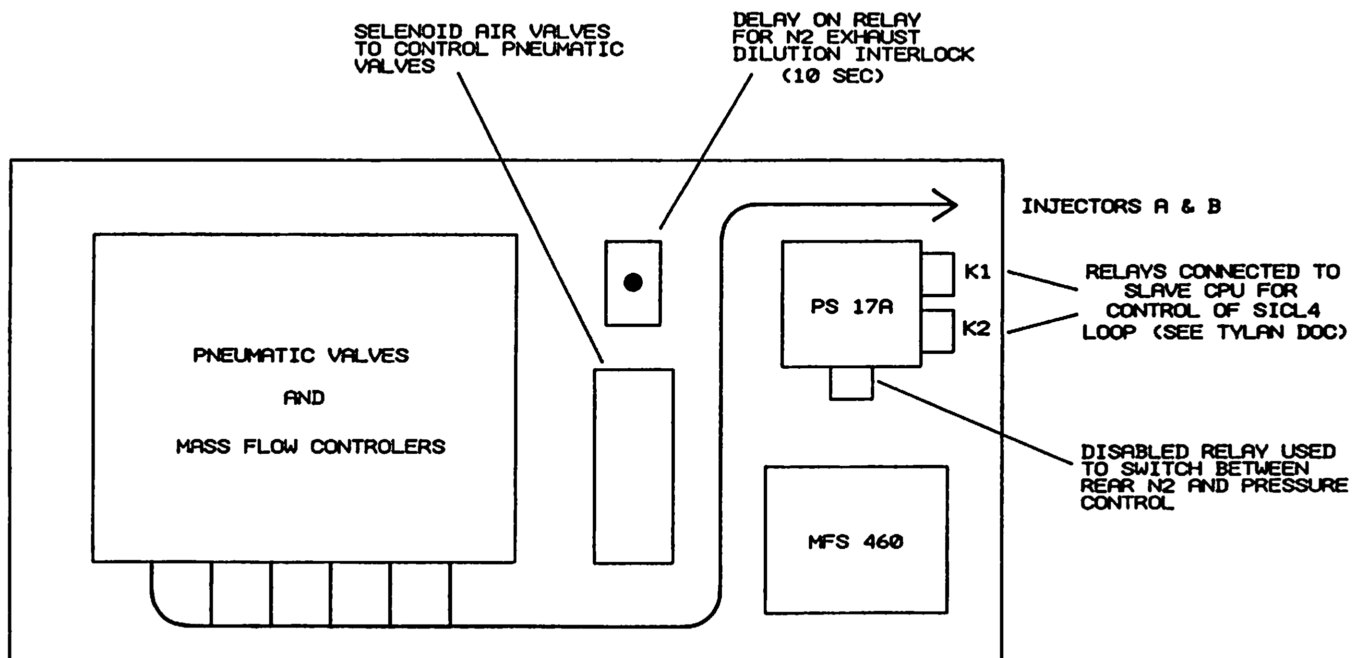
Drw. 3: Thermocouple connections including calibration relay activated by CCOUT10 contact closure.



Drw. 4: Vacuum pump schematic (1/2).

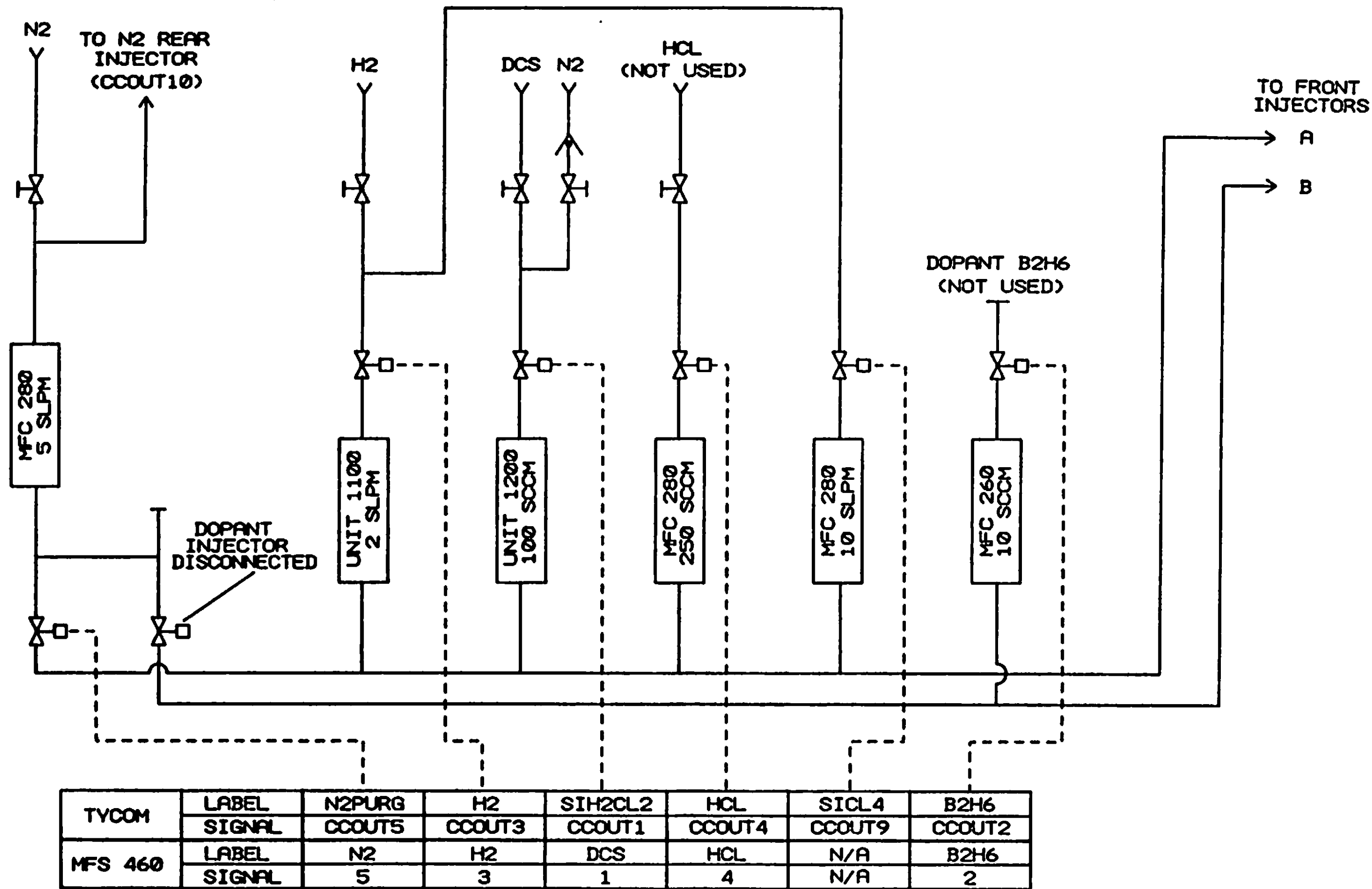


Drw. 5: Vacuum pump schematic (2/2).



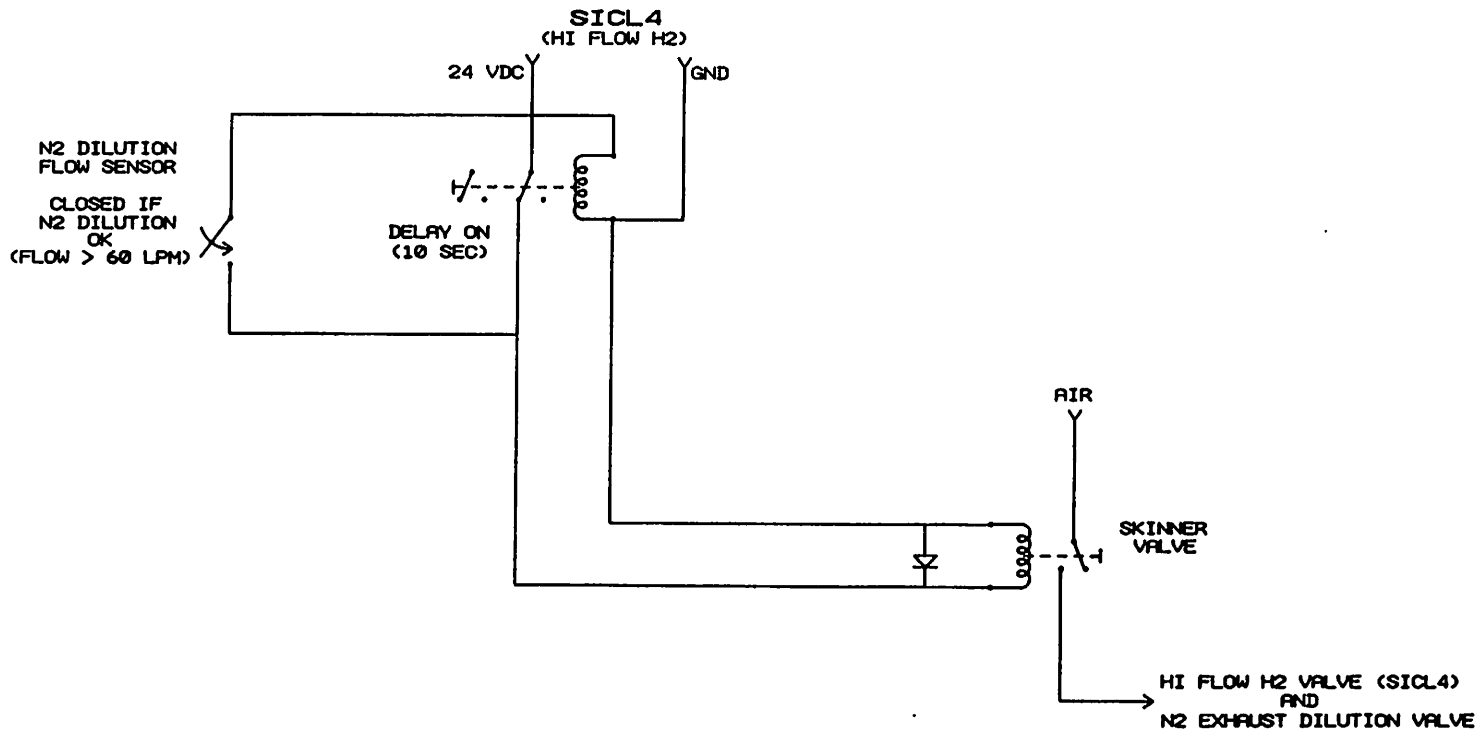
NOTE: 1. NEVER UNPLUG MFC'S FROM MFS 460 WITH POWER ON.
2. MFS 460 WILL AUTO ZERO AFTER POWER ON ONLY IF NO FLOW IS COMMANDED. CAN TAKE 30 MIN. TO AUTO ZERO.

Drw. 6: Gas shelf layout.

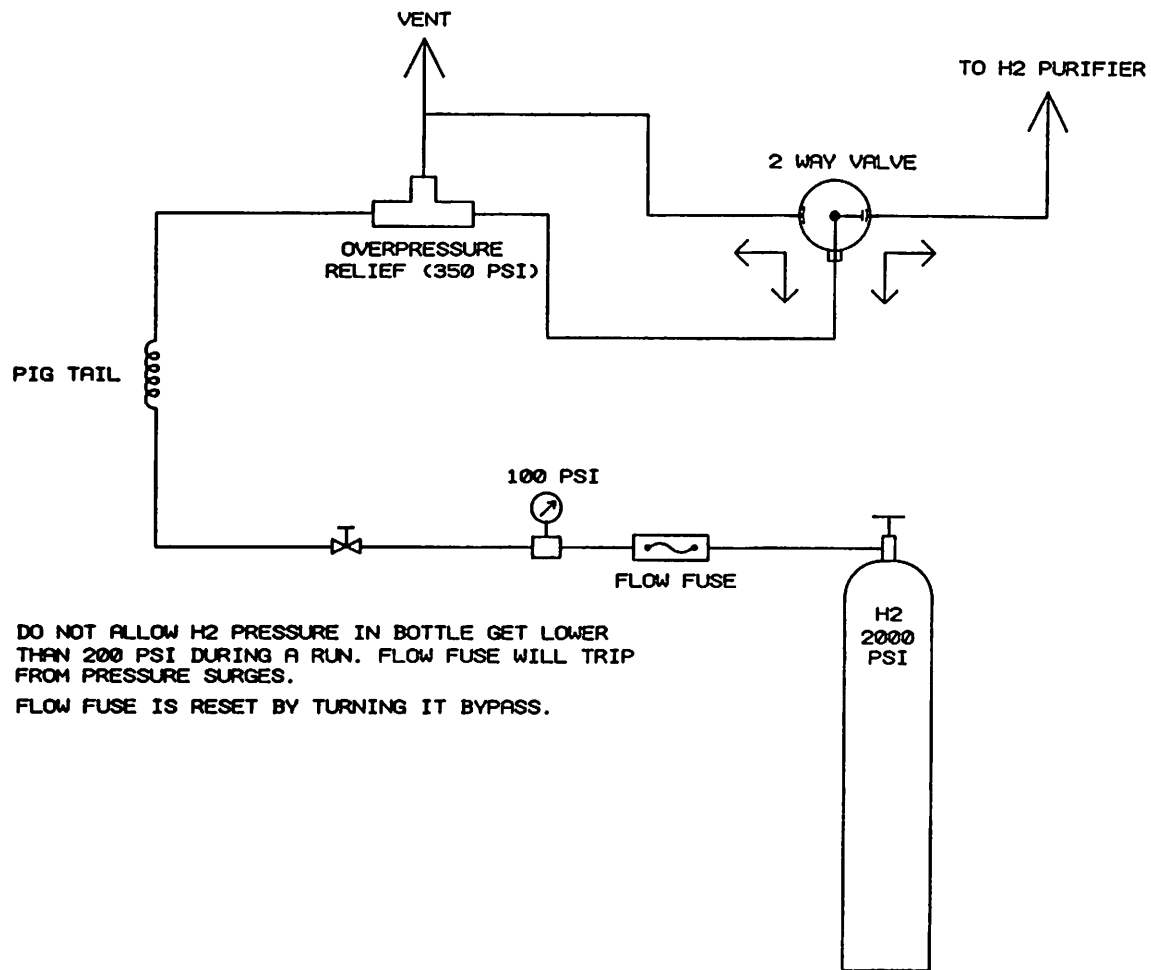


TYCOM	LABEL	N2PURG	H2	SIH2CL2	HCL	SICL4	B2H6
	SIGNAL	CCOUT5	CCOUT3	CCOUT1	CCOUT4	CCOUT9	CCOUT2
MFS 460	LABEL	N2	H2	DCS	HCL	N/A	B2H6
	SIGNAL	5	3	1	4	N/A	2

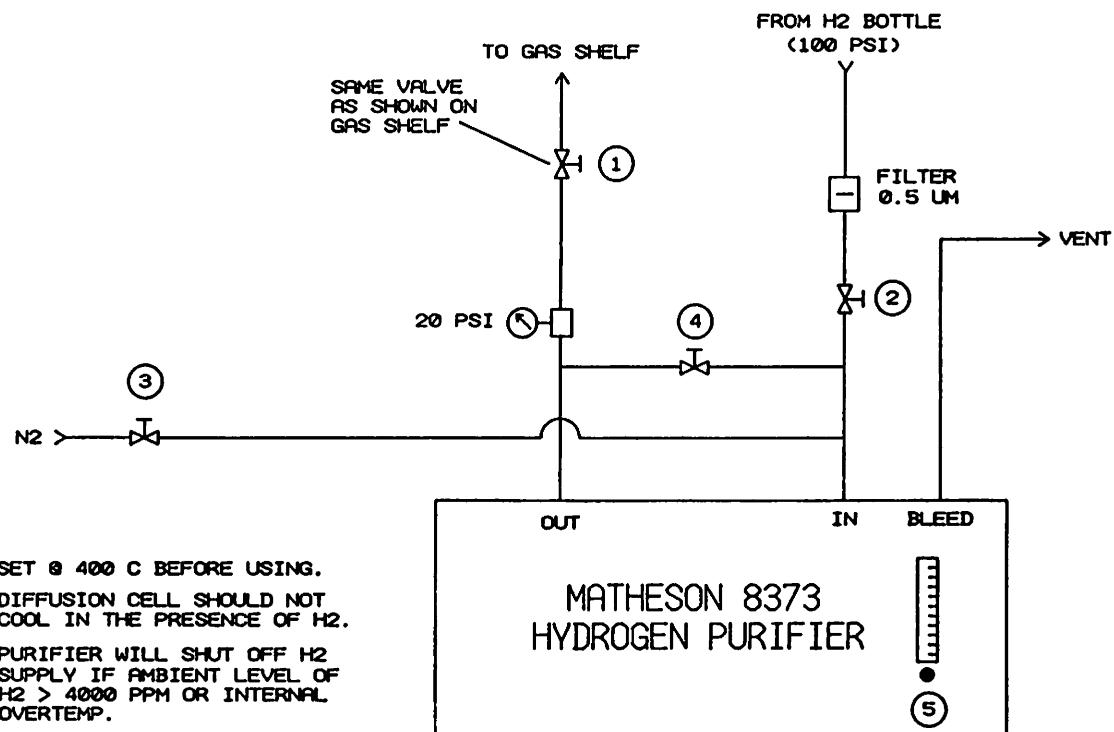
Drw. 7: Gas shelf schematic.



Drw. 8: Exhaust dilution activated during high flow of hydrogen.

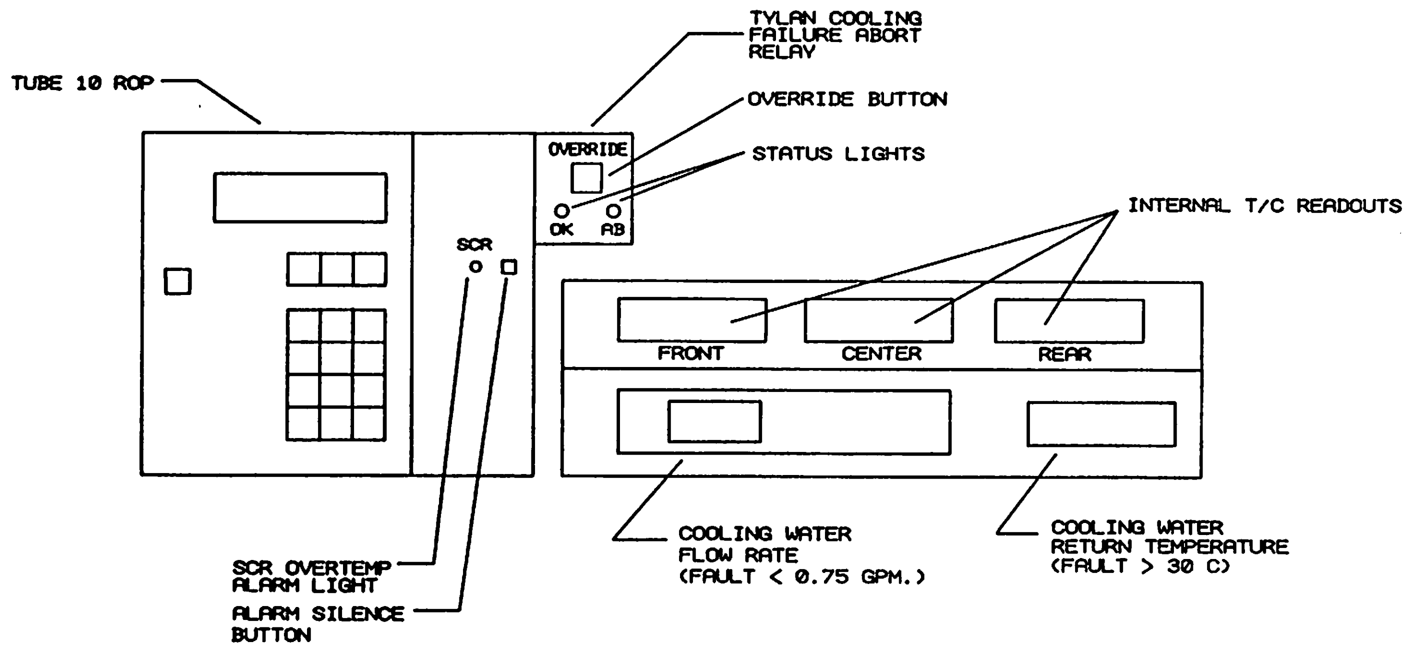


Drw. 9: Hydrogen supply (1/2).

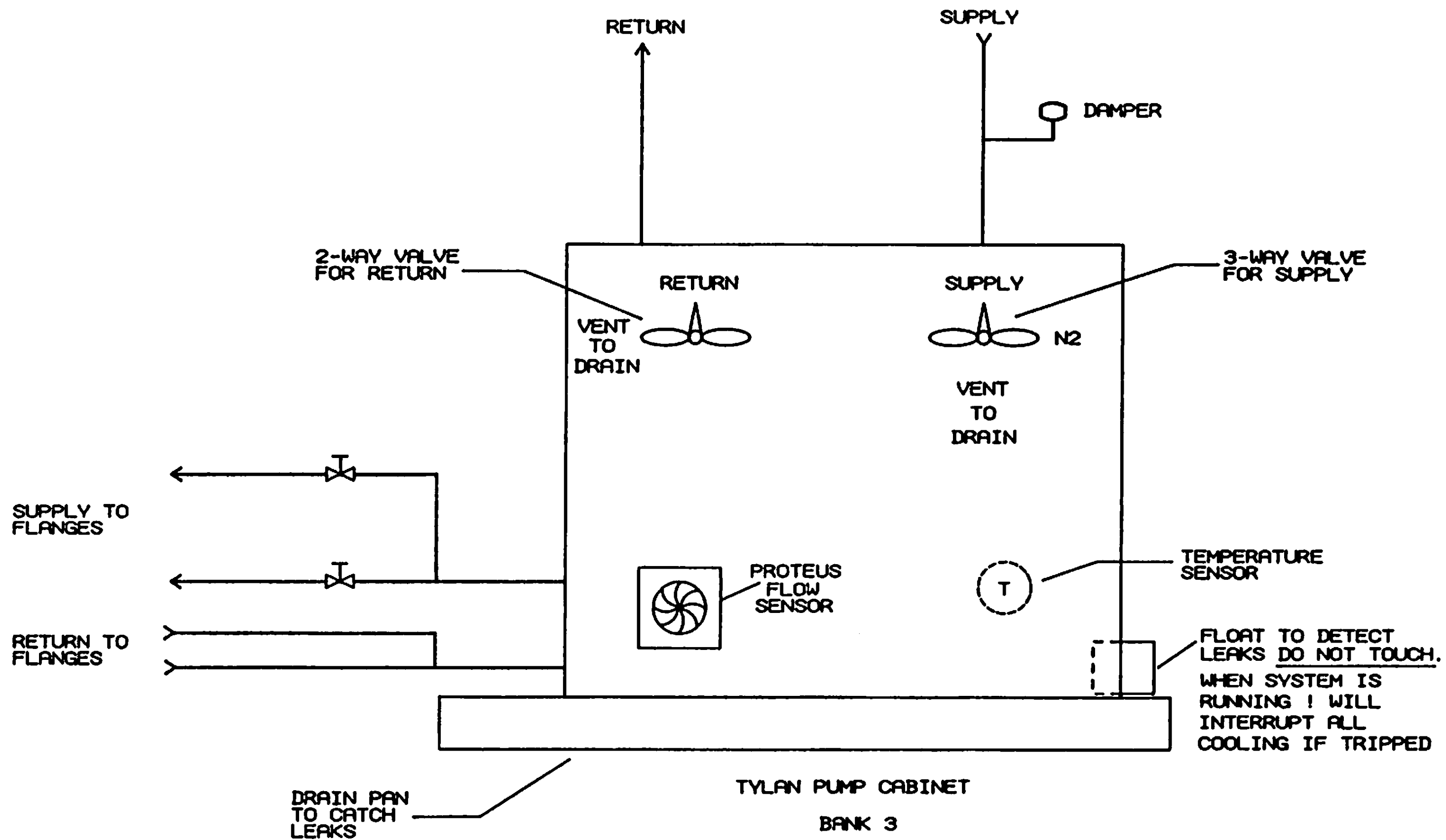


NOTE:
1. SET @ 400 C BEFORE USING.
2. DIFFUSION CELL SHOULD NOT COOL IN THE PRESENCE OF H2.
3. PURIFIER WILL SHUT OFF H2 SUPPLY IF AMBIENT LEVEL OF H2 > 4000 PPM OR INTERNAL OVERTEMP.
4. VALVE LABELS CORRESPOND TO THOSE IN PURIFIER MANUAL.

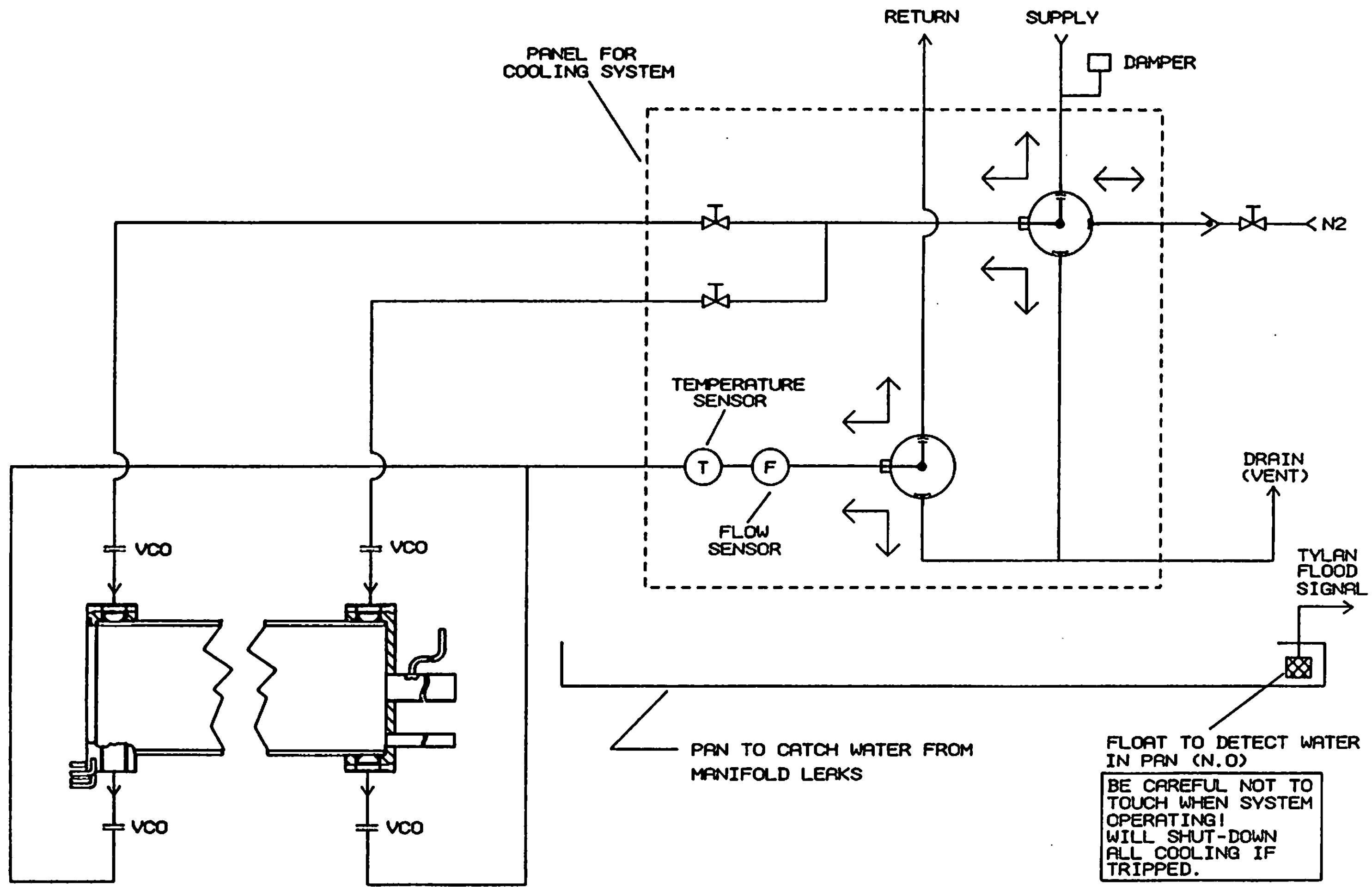
Drw. 10: Hydrogen supply (2/2).



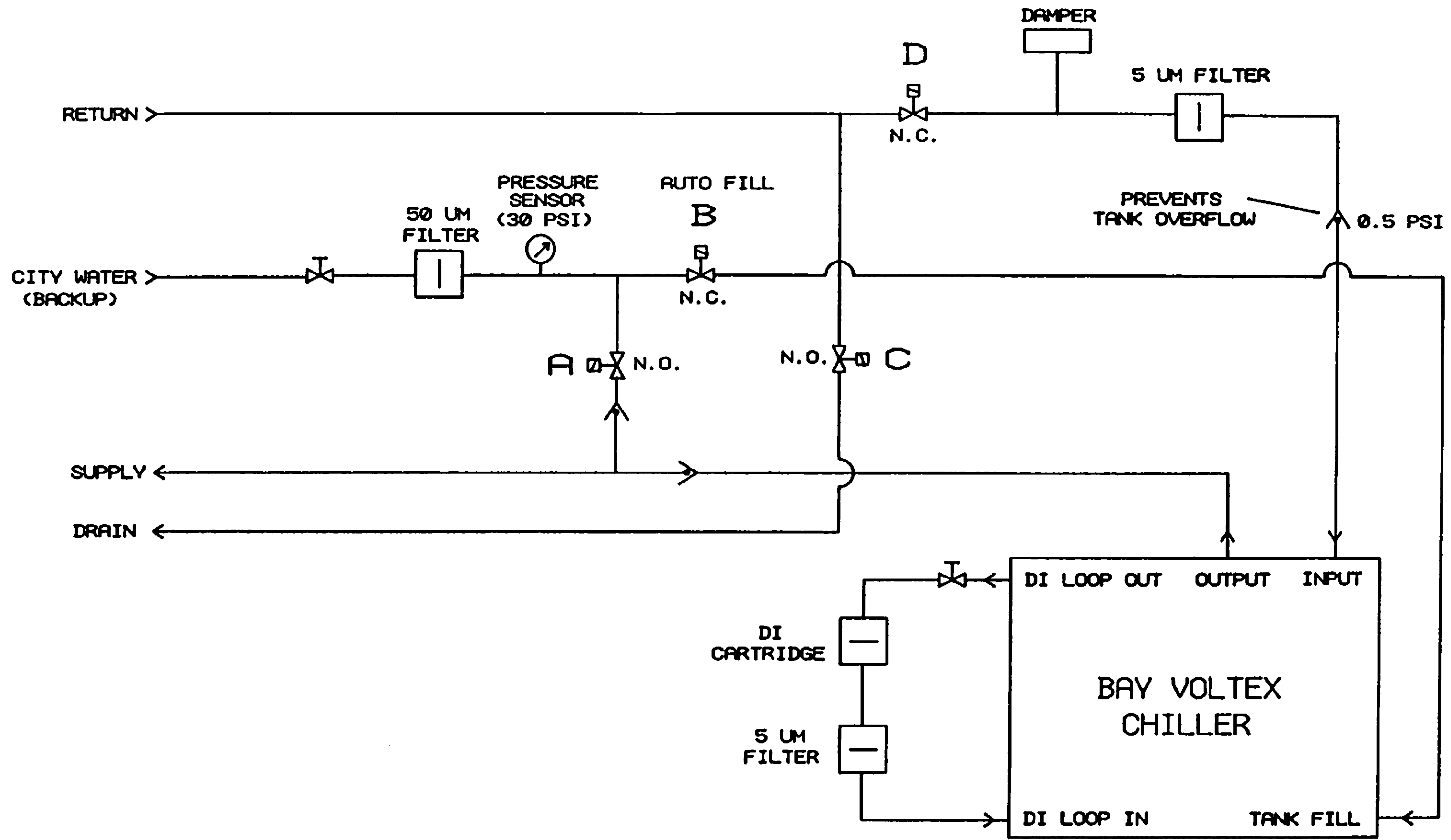
Drw. 11: Operator panel additions to monitor internal reactor temperatures and cooling system operation.



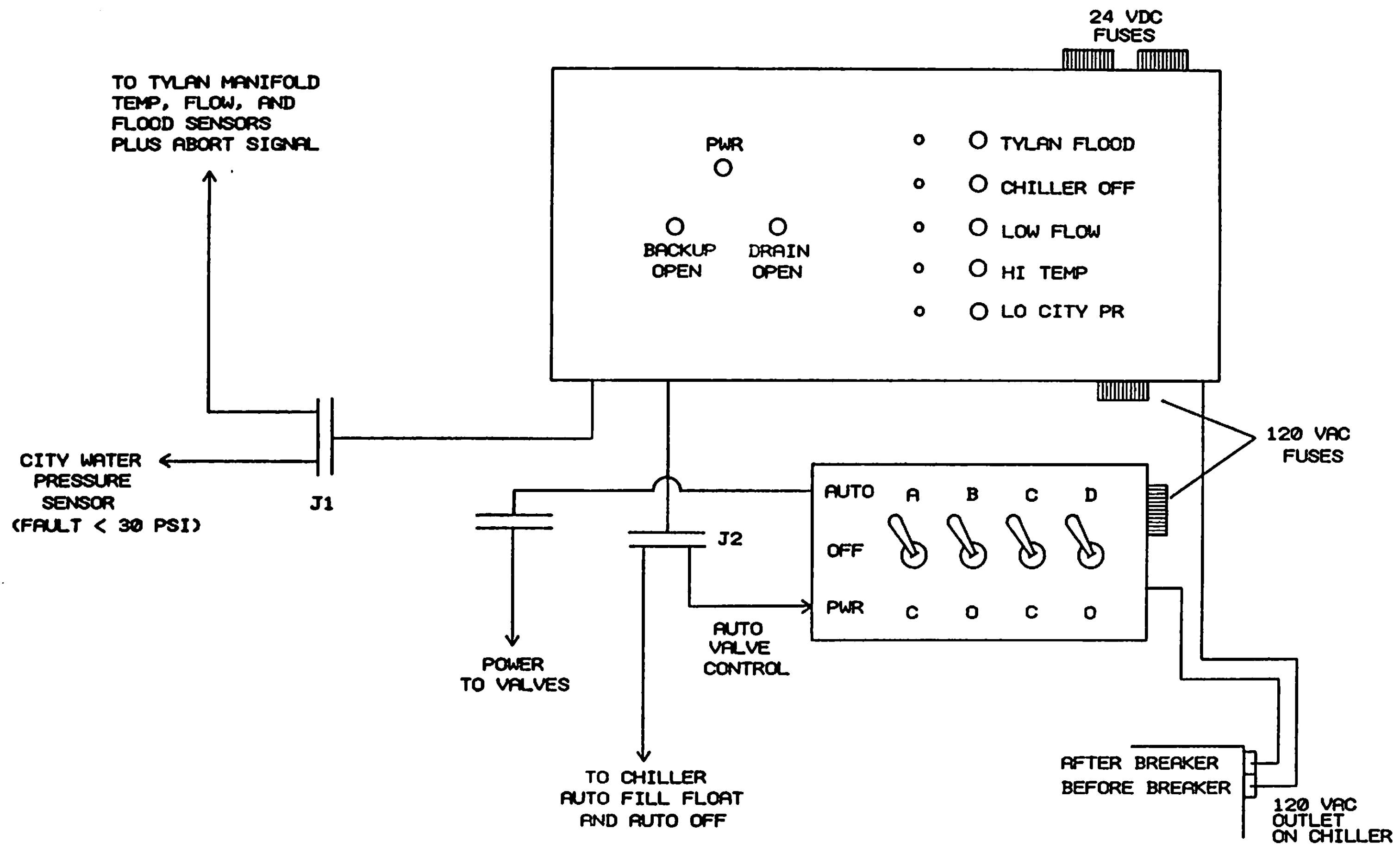
Drw. 12: Tylan panel for cooling system manifold (valves for furnace flange maintenance).



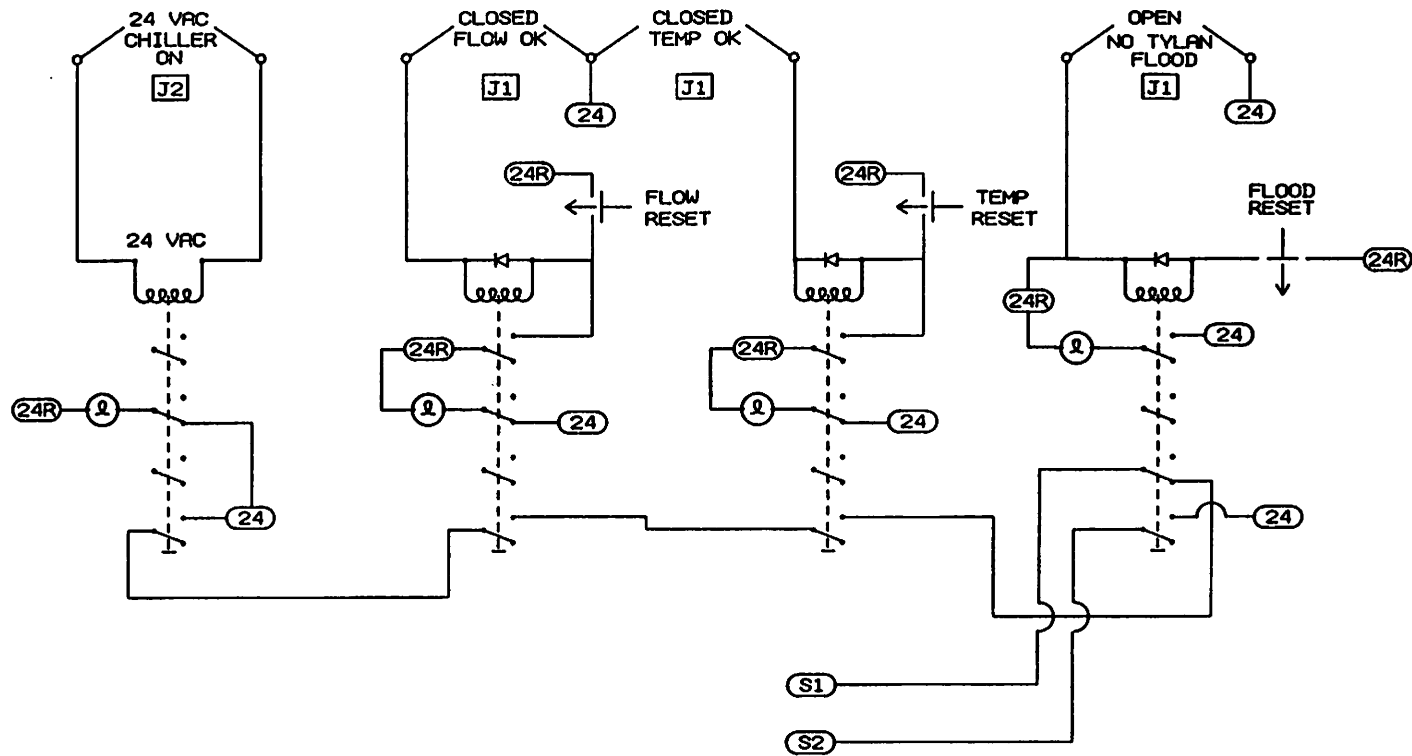
Drw. 13: Cooling system schematic (1/2).



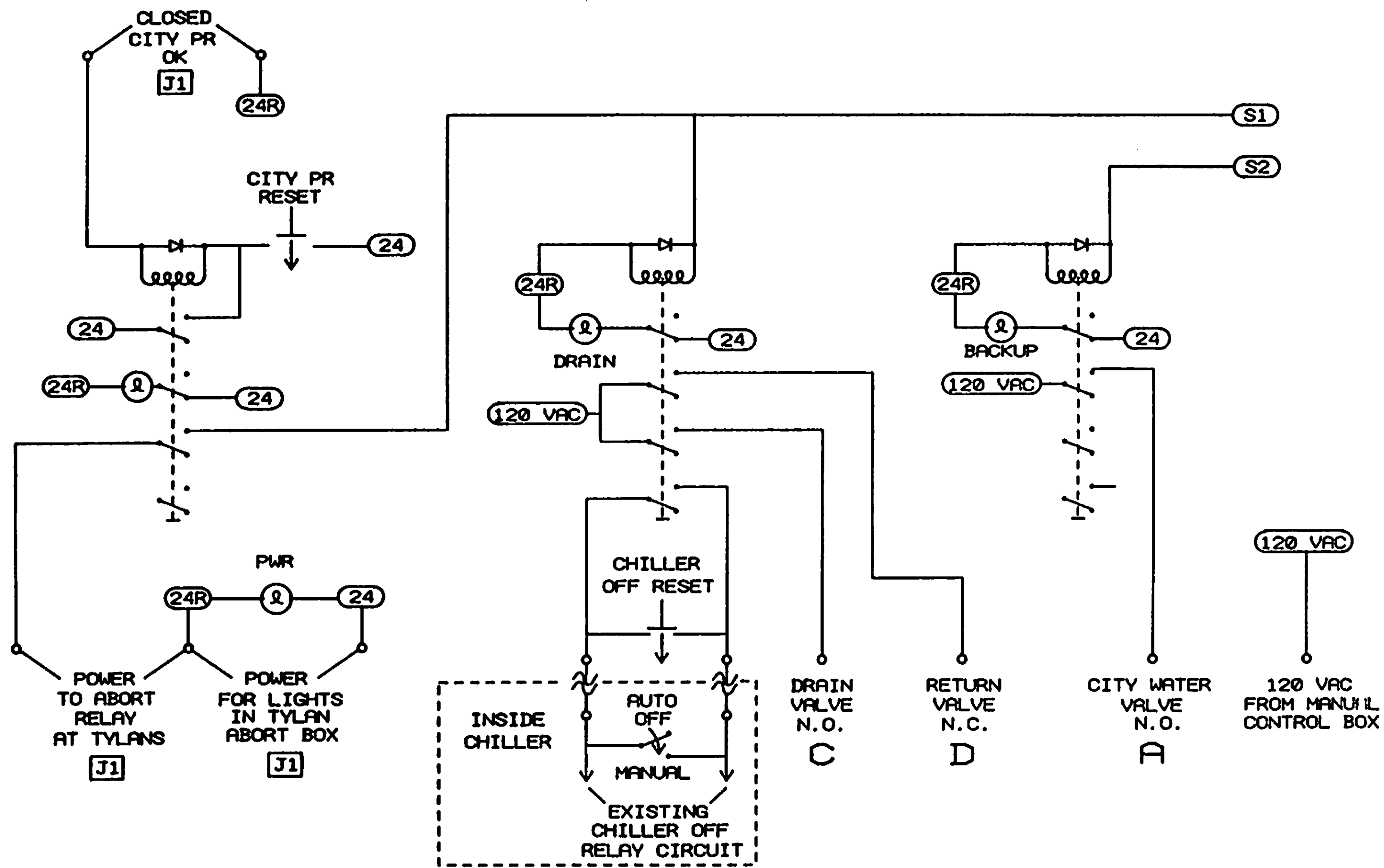
Drw. 14: Cooling system schematic (2/2).



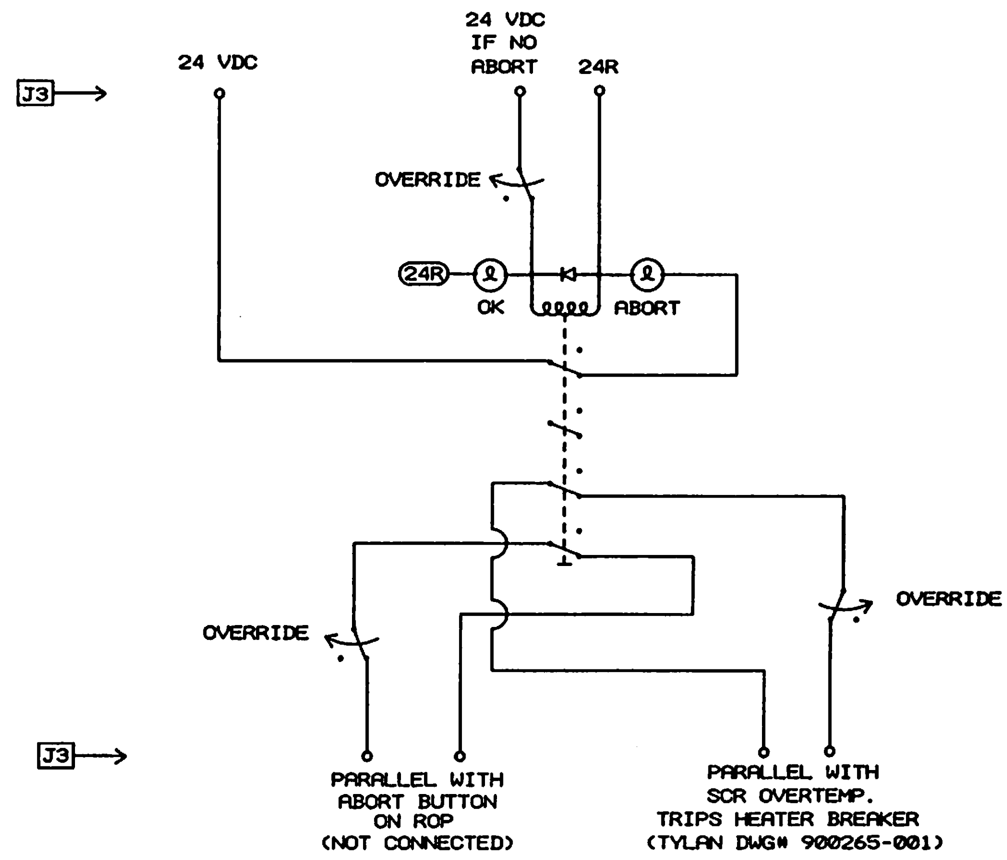
Drw. 15: Cooling system control panel and connector locations.



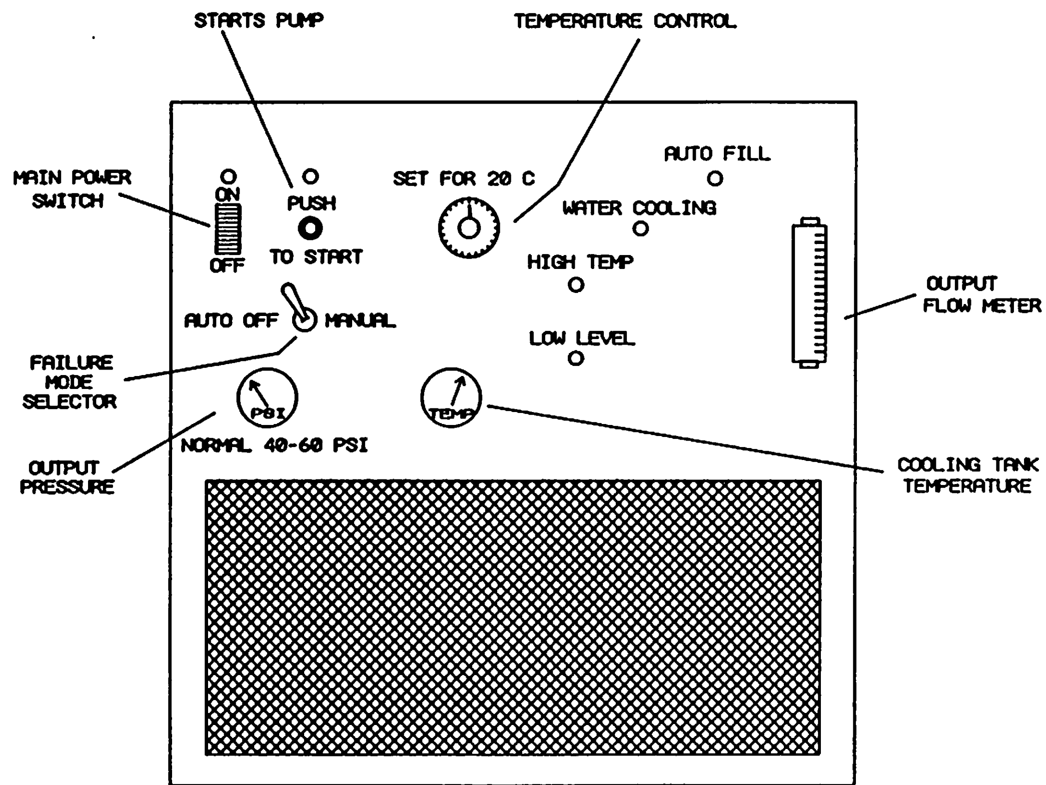
Drw.16: Electrical schematic of cooling system control panel (1/2).



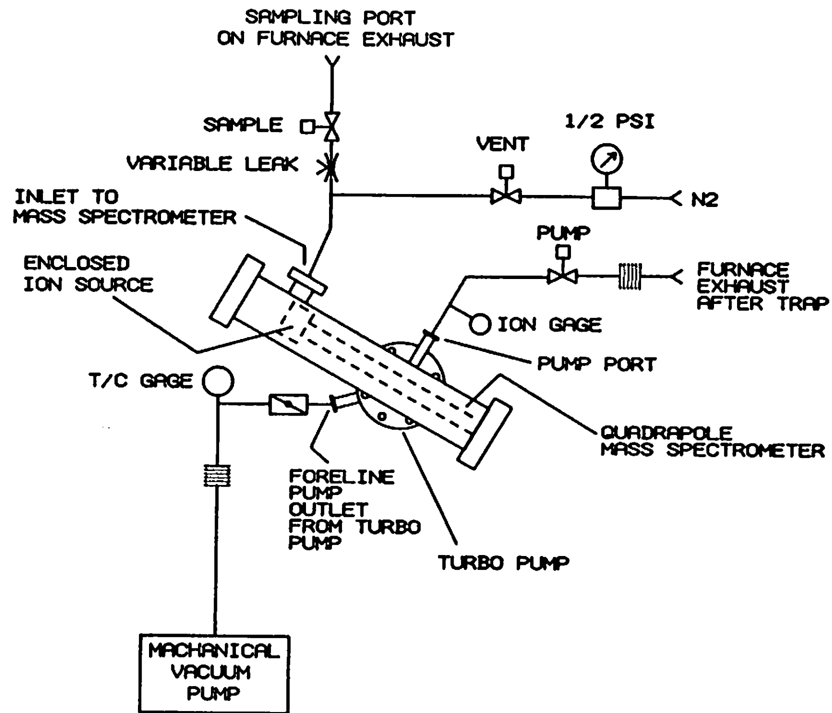
Drw.17: Electrical schematic of cooling system control panel (2/2).



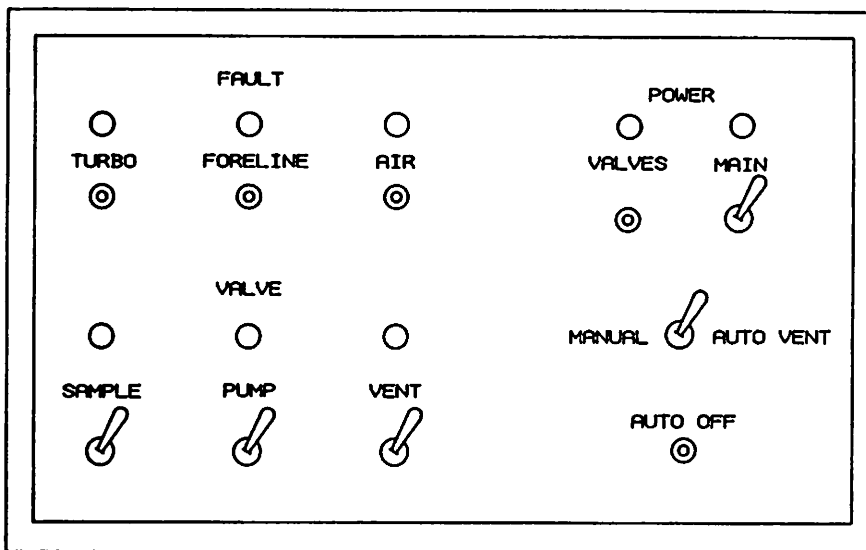
Drw. 18: Electrical schmatic of Tylan abort box.



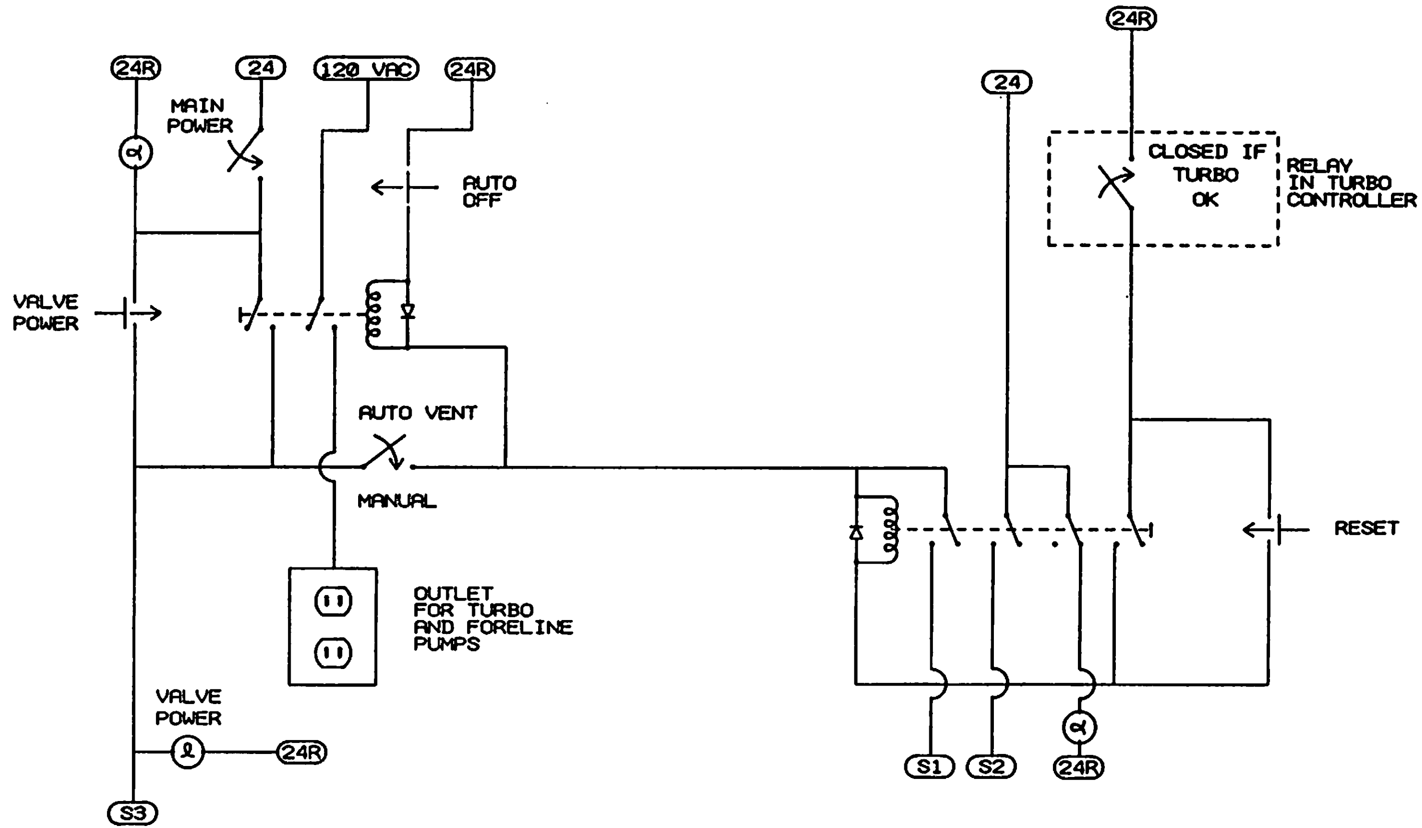
Drw. 19: Front panel of chiller.



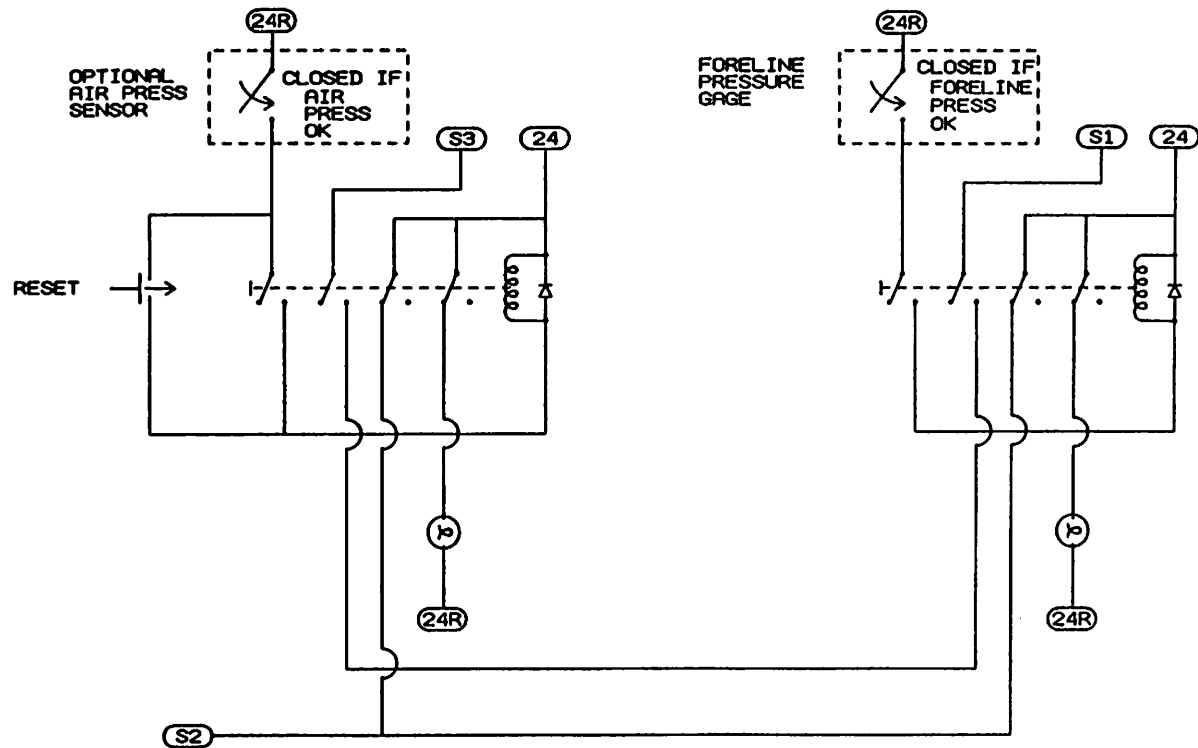
Drw. 20: Schematic of mass-spectrometer installation.



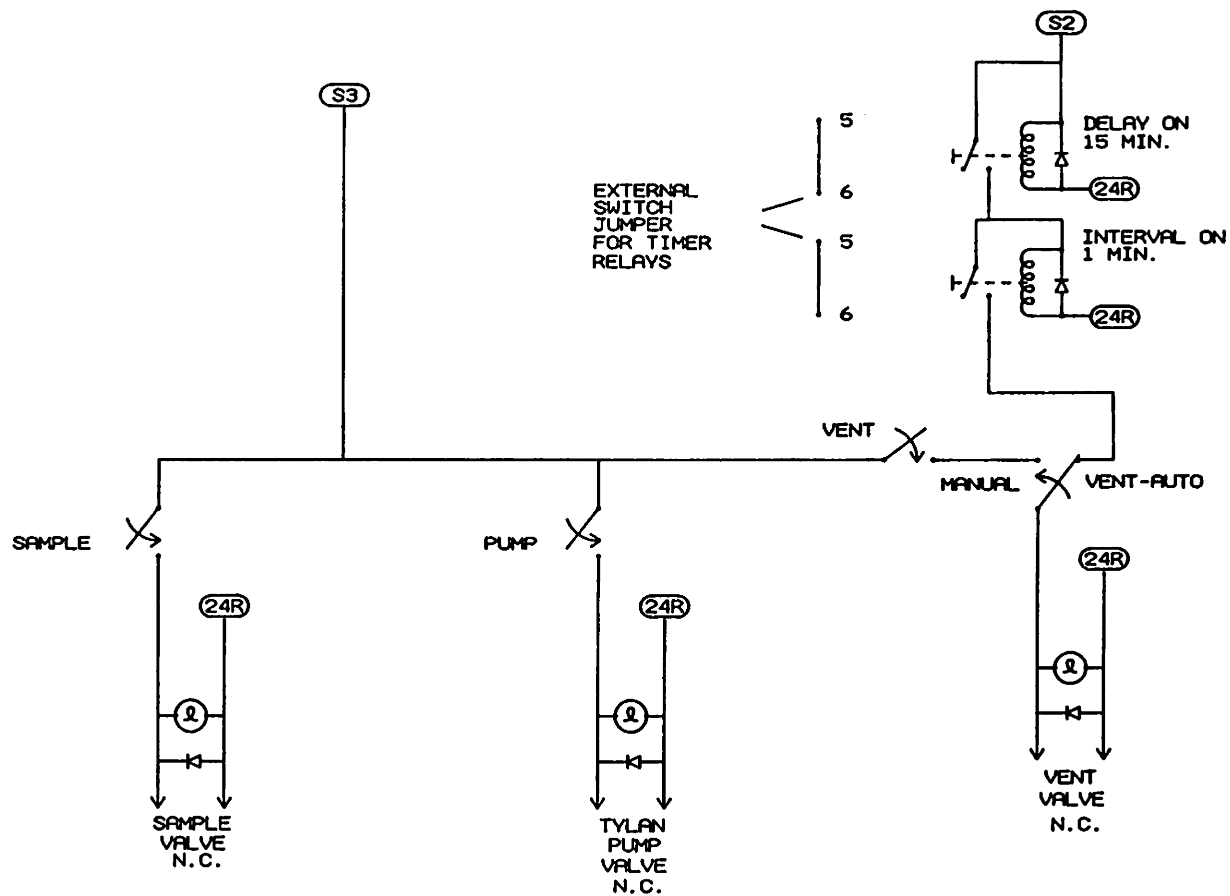
Drw. 21: Front panel of mass-spectrometer control box.



Drw. 22: Electrical schematic of mass-spectrometer control box (1/3).



Drw. 23: Electrical schematic of mass-spectrometer control box (2/3).



Drw. 24: Electrical schematic of mass-spectrometer control box (3/3).

A.2

Tylan Recipes

EPI.19T

The current epitaxial deposition recipe. Use recipe carefully. All of the times, temperatures, and input flow rates associated with the deposition cycle are variables.

```
process id: epi.19t
description: epi.18t + new h2 mfc and dcs during bake
bank: 1
tubes: 10
reuse: yes

0001.0000   STEP ready
0001.0005     dtcena=off
0001.0010     tempc=350
0001.0015     templ=350
0001.0020     temps=350
0001.0025     templ tolerance=1
0001.0030     tempc tolerance=1
0001.0035     temps tolerance=1
0001.0040     krl=80
0001.0045     krc=25
0001.0050     krs=100
0001.0055     kcl=75
0001.0060     kcc=20
0001.0065     kcs=95
0001.0070     kp=60
0001.0075     h2=0 (real flow is 0.4x)
0001.0080     hcl=0 (real flow is 0.5x)
0001.0085     sih2cl2=0
0001.0090     sicl4=0 (high flow h2, real 100x)
0001.0095     n2purg=0
0001.0100     vacuum=off
0001.0105     load=off
0001.0110     unload=off
0001.0115     ccout10=off (calib t/c connect)
0001.0120     ccout13=off (n2 rear injector)
0001.0125     prcpr=0 (not used, disconnected)
0001.0130     n2purg tolerance=50  (need for conditionals)
0001.0135     h2 tolerance=50
0001.0140     hcl tolerance=10
0001.0145     sih2cl2 tolerance=1
0001.0150     sicl4 tolerance=1
0001.0155     prcpr tolerance=100

0005.0000   STEP n2purg and vacuum on
```

```
0005.0005       time:00:00:00
0005.0010       n2purg=300
0005.0015       vacuum=on
0005.0020       if almack=on goto 0010

0010.0000     STEP idle, loading temp (min water adsorption)
0010.0005       time:00:00:00
0010.0010       dtcena=on
0010.0015       templ=500
0010.0020       tempc=525
0010.0025       temps=500
0010.0030       n2purg=300
0010.0035       if almack=on goto 0015
0010.0040       if ccin2=off goto 0120

0015.0000     STEP skip loading
0015.0005       time:00:00:15
0015.0010       if almack=on goto 0050

0020.0000     STEP vacuum off and vent
0020.0005       time:00:07:30
0020.0010       n2purg=5000
0020.0015       vacuum=off
0020.0020       if almack=on goto 0025

0025.0000     STEP open
0025.0005       time:00:10:00
0025.0010       unload=on
0025.0015       ccout13=on (turn on rear n2)
0025.0020       if almack=on goto 0030

0030.0000     STEP close
0030.0005       time:00:10:00
0030.0010       unload=off
0030.0015       load=on
0030.0020       if dntlk=on goto 0035

0035.0000     STEP wait for door (in case switch not exact)
0035.0005       time:00:00:05
0035.0010       ccout13=off (close rear n2)
0035.0015       if dntlk=off goto 0045

0040.0000     STEP pump down
0040.0005       time:00:01:00
0040.0010       load=off
0040.0015       n2purg=300
```

```
0040.0020     vacuum=on
0040.0025     if prcpr<1000 goto 0050

0045.0000   STEP stop pump and vent (door not closed)
0045.0005     time:00:00:00
0045.0010     vacuum=off
0045.0015     n2purg=5000

0050.0000   STEP continue pumping (door ok) >>> abort if just unload
0050.0005     time:00:10:00
0050.0010     n2purg=500
0050.0015     if almack=on goto 0055
0050.0020     if ccin2=off goto 0120 (check antlk)

0055.0000   STEP pump down for leak check
0055.0005     time:00:00:30
0055.0010     n2purg=0
0055.0015     if almack=on goto 0060

0060.0000   STEP timed leak check
0060.0005     time:00:00:30
0060.0010     vacuum=off
0060.0015     if prcpr>120 goto 0120
0060.0020     if almack=on goto 0065

0065.0000   STEP open gate valve before h2
0065.0005     time:00:00:10
0065.0010     vacuum=on

0070.0000   STEP start bake ramp
0070.0005     time:variable bake ramp
0070.0010     vacuum=on
0070.0015     h2=variable bake (100-5000), real 0.4x
0070.0020     sicl4=variable h2 hi flow (1-100), real 100x
0070.0025     templ=variable bake (350-1100)
0070.0030     tempc=variable
0070.0035     temps=variable
0070.0040     if almack=on goto 0075
0070.0045     if ccin2=off goto 0120
0070.0050     if vntlk=off goto 0120
0070.0055     if gntlk=off goto 0120

0075.0000   STEP bake time
0075.0005     time:variable bake
0075.0010     sih2cl2=variable bake (2-100)
0075.0015     if almack=on goto 0080
```

```
0075.0020      if ccin2=off goto 0120
0075.0025      if vntlk=off goto 0120
0075.0030      if gntlk=off goto 0120

0080.0000   STEP ramp down to deposition temperature
0080.0005      time:variable dep ramp
0080.0010      sih2cl2=variable dep ramp (2-100)
0080.0015      templ=variable dep (350-1100)
0080.0020      tempc=variable
0080.0025      temps=variable
0080.0030      if almack=on goto 0085
0080.0035      if ccin2=off goto 0120
0080.0040      if vntlk=off goto 0120
0080.0045      if gntlk=off goto 0120

0085.0000   STEP stablize h2 flow for predep
0085.0005      time:00:00:20
0085.0010      h2=variable predep (100-5000), real 0.4x
0085.0015      sicl4=0 (turn off hi flow h2)
0085.0020      if almack=on goto 0090
0085.0025      if ccin2=off goto 0120
0085.0030      if vntlk=off goto 0120
0085.0035      if gntlk=off goto 0120

0090.0000   STEP predep dcs
0090.0005      time:00:00:10
0090.0010      sih2cl2=variable predep (2-100)
0090.0015      if ccin2=off goto 0120
0090.0020      if vntlk=off goto 0120
0090.0025      if gntlk=off goto 0120

0095.0000   STEP predp dcs time
0095.0005      time:variable predep
0095.0010      if almack=on goto 0100
0095.0015      if ccin2=off goto 0120
0095.0020      if vntlk=off goto 0120
0095.0025      if gntlk=off goto 0120

0100.0000   STEP stablize flows for deposition
0100.0005      time:00:00:10
0100.0010      h2=variable dep (100-5000), real 0.4x
0100.0015      sih2cl2=variable dep (2-100)
0100.0020      if ccin2=off goto 0120
0100.0025      if vntlk=off goto 0120
0100.0030      if gntlk=off goto 0120
```

```
0105.0000   STEP deposition time
0105.0005     time:variable dep
0105.0010     if almack=on goto 0110
0105.0015     if ccin2=off goto 0120
0105.0020     if vntlk=off goto 0120
0105.0025     if gntlk=off goto 0120

0110.0000   STEP end deposition and cool
0110.0005     time:01:00:00
0110.0010     h2=2500 (real=1000)
0110.0015     hcl=0
0110.0020     sih2cl2=0
0110.0025     templ=500
0110.0030     tempc=525
0110.0035     temps=500
0110.0040     if almack=on goto 0115
0110.0045     if ccin2=off goto 0120
0110.0050     if vntlk=off goto 0120
0110.0055     if gntlk=off goto 0120

0115.0000   STEP h2 off and n2 on
0115.0005     time:00:00:00
0115.0010     h2=0
0115.0015     n2purg=500
0115.0020     if almack=on goto 0010
0115.0025     if ccin2=off goto 0120
0115.0030     if vntlk=off goto 0120
0115.0035     if gntlk=off goto 0120

0120.0000   STEP end
0120.0005     end process
```

EPISTNBY

Standby recipe to be loaded and run when tube is not in use. Includes traps for interlocks to avoid and diagnose the intermittent problem with spurious interlock interrupts.

```
process id: epistnby
description: standby for epi tube (with traps)
bank: 1
tubes: 10
reuse: yes

0001.0000   STEP ready
0001.0005     dtcena=on
0001.0010     templ=350
0001.0015     tempc=350
0001.0020     temps=350
0001.0025     templ tolerance=1
0001.0030     tempc tolerance=1
0001.0035     temps tolerance=1
0001.0040     krl=80
0001.0045     krc=25
0001.0050     krs=100
0001.0055     kcl=75
0001.0060     kcc=20
0001.0065     kcs=95
0001.0070     kp=40
0001.0075     h2=0
0001.0080     hcl=0
0001.0085     sih2cl2=0
0001.0090     n2purg=0
0001.0095     vacuum=off
0001.0100     load=off
0001.0105     unload=off
0001.0110     ccout13=off
0001.0115     ccout10=off

0005.0000   STEP n2 on
0005.0005     time:00:00:05
0005.0010     n2purg=500

0010.0000   STEP start pump and n2
0010.0005     time:00:00:10
0010.0010     vacuum=on
0010.0015     n2purg=500
0010.0020     if vntlk=off goto 0020
```

```
0015.0000   STEP idle
0015.0005     time:00:00:00
0015.0010     vacuum=on
0015.0015     n2purg=500
0015.0020     templ=500
0015.0025     tempc=525
0015.0030     temps=500
0015.0035     if almack=on goto 0020
0015.0040     if ccin2=off goto 0025
0015.0045     if bntlk=off goto 0030
0015.0050     if gntlk=off goto 0035
0015.0055     if vntlk=off goto 0040

0020.0000   STEP almack on trap
0020.0005     time:00:00:00
0020.0010     n2purg=500

0025.0000   STEP ccin2 (antlk) trap
0025.0005     time:00:00:00
0025.0010     n2purg=500

0030.0000   STEP bntlk trap
0030.0005     time:00:00:00
0030.0010     n2purg=500

0035.0000   STEP gntlk trap
0035.0005     time:00:00:00
0035.0010     n2purg=500

0040.0000   STEP vntlk trap
0040.0005     time:00:00:00
0040.0010     n2purg=500

0045.0000   STEP
0045.0005     end process
```

EPIWARM

Standby recipe that maintains the tube at its minimum controllable temperature. The temperature low enough for the silicon rubber o-rings in the flanges to perhaps survive a cooling flow interruption.

```
process id: epiwarm
description: standby for epi tube, t=400
bank: 1
tubes: 10
reuse: yes

0001.0000   STEP ready
0001.0005     dtcena=on
0001.0010     templ=350
0001.0015     tempc=350
0001.0020     temps=350
0001.0025     templ tolerance=1
0001.0030     tempc tolerance=1
0001.0035     temps tolerance=1
0001.0040     krl=80
0001.0045     krc=25
0001.0050     krs=100
0001.0055     kcl=75
0001.0060     kcc=20
0001.0065     kcs=95
0001.0070     kp=40
0001.0075     h2=0
0001.0080     hcl=0
0001.0085     sih2cl2=0
0001.0090     n2purg=0
0001.0095     vacuum=off
0001.0100     load=off
0001.0105     unload=off
0001.0110     ccout13=off
0001.0115     ccout10=off

0005.0000   STEP n2 on
0005.0005     time:00:00:05
0005.0010     n2purg=500

0010.0000   STEP start pump and n2
0010.0005     time:00:00:10
0010.0010     vacuum=on
0010.0015     n2purg=500
```

```
0010.0020      if vntlk=off goto 0020

0015.0000    STEP idle
0015.0005      time:00:00:00
0015.0010      vacuum=on
0015.0015      n2purg=500
0015.0020      templ=400
0015.0025      tempc=425
0015.0030      temps=400
0015.0035      if almack=on goto 0020
0015.0040      if ccin2=off goto 0020
0015.0045      if bntlk=off goto 0020
0015.0050      if gntlk=off goto 0020
0015.0055      if vntlk=off goto 0020

0020.0000    STEP
0020.0005      end process
```

EPIVAC

Standby recipe that places the system under vacuum with the heaters turned off. To be loaded and run when it is desired to cool the system down or to keep it cool for maintenance purposes. The system should always be kept under vacuum when possible.

```
process id: epivac
description: standby recipe for epi, no heat
bank: 1
tubes: 10
reuse: yes

0001.0000   STEP ready
0001.0005     dtcena=on
0001.0010     templ=350
0001.0015     tempc=350
0001.0020     temps=350
0001.0025     templ tolerance=1
0001.0030     tempc tolerance=1
0001.0035     temps tolerance=1
0001.0040     krl=80
0001.0045     krc=25
0001.0050     krs=100
0001.0055     kcl=75
0001.0060     kcc=20
0001.0065     kcs=95
0001.0070     kp=40
0001.0075     h2=0
0001.0080     hcl=0
0001.0085     sih2cl2=0
0001.0090     n2purg=0
0001.0095     vacuum=off
0001.0100     load=off
0001.0105     unload=off
0001.0110     ccout13=off
0001.0115     ccout10=off

0005.0000   STEP n2 on
0005.0005     time:00:00:05
0005.0010     n2purg=500

0010.0000   STEP start pump and n2
0010.0005     time:00:00:40
0010.0010     vacuum=on
0010.0015     n2purg=500
```

```
0010.0020     if vntlk=off goto 0020

0015.0000   STEP idle
0015.0005     time:00:00:00
0015.0010     vacuum=on
0015.0015     n2purg=500
0015.0020     if almack=on goto 0020
0015.0025     if ccin2=off goto 0020
0015.0030     if bntlk=off goto 0020
0015.0035     if gntlk=off goto 0020
0015.0040     if vntlk=off goto 0020

0020.0000   STEP
0020.0005     end process
```

N2.CLEAN

Convenient recipe to use during cleaning of a cold system. Vents, opens with rear N2 flowing, closes, and pumps down by repeatedly hitting ALMACK button.

```
process id: n2.clean
description: vent, n2rear, pump for tube cleaning (cold)
bank: 1
tubes: 10
reuse: yes

0001.0000    STEP ready
0001.0005      dtcena=on
0001.0010      templ=350
0001.0015      tempc=350
0001.0020      temps=350
0001.0025      templ tolerance=1
0001.0030      tempc tolerance=1
0001.0035      temps tolerance=1
0001.0040      krl=80
0001.0045      krc=25
0001.0050      krs=100
0001.0055      kcl=75
0001.0060      kcc=20
0001.0065      kcs=95
0001.0070      kp=40
0001.0075      h2=0
0001.0080      hcl=0
0001.0085      sih2cl2=0
0001.0090      n2purg=0
0001.0095      vacuum=off
0001.0100      load=off
0001.0105      unload=off
0001.0110      ccout13=off  n2rear
0001.0115      ccout10=off  cal tc connect
0001.0120      prcpr=0  not used, disconnected
0001.0125      prcpr tolerance=100  need this to use conditional

0005.0000    STEP go directly to pumpdown
0005.0005      time:00:00:15
0005.0010      if almack=on goto 0025

0010.0000    STEP timed vent
0010.0005      time:00:07:30
0010.0010      n2purg=5000
```

```
0010.0015     vacuum=off
0010.0020     if almack=on goto 0015

0015.0000   STEP tube ready to open
0015.0005     time:00:00:00
0015.0010     n2purg=5000
0015.0015     if almack=on goto 0020

0020.0000   STEP n2rear on
0020.0005     time:00:00:00
0020.0010     ccout13=on
0020.0015     if almack=on goto 0025

0025.0000   STEP check door closed before start pump
0025.0005     time:00:00:00
0025.0010     if dntlk=on goto 0030

0030.0000   STEP turn off n2rear
0030.0005     time:00:00:05
0030.0010     ccout13=off

0035.0000   STEP start pumping
0035.0005     time:00:02:00
0035.0010     n2purg=300
0035.0015     vacuum=on
0035.0020     if prcpr<1000 goto 0045

0040.0000   STEP pumpdown too long, something wrong?
0040.0005     time:00:00:00
0040.0010     n2purg=5000
0040.0015     vacuum=off

0045.0000   STEP pumpdown ok, indefinite hold
0045.0005     time:00:00:00
0045.0010     n2purg=500

0050.0000   STEP
0050.0005     end process
```

DTCSET

Load and run recipe to set the digital temperature controller (DTC) parameters if memory lost because of power interruption or reset.

```
process id: dtcset
description: set constants according to dtc1.0
bank: 1
tubes: 10
reuse: yes

0001.0000   STEP initialization
0001.0005     dtcena=on
0001.0010     n2purg=0
0001.0015     templ=350
0001.0020     tempc=350
0001.0025     temps=350
0001.0030     templ tolerance=1
0001.0035     tempc tolerance=1
0001.0040     temps tolerance=1
0001.0045     kr=0
0001.0050     kc=0
0001.0055     kp=20

0005.0000   STEP set point
0005.0005     time:00:00:06
0005.0010     templ=350
0005.0015     tempc=350
0005.0020     temps=350

0010.0000   STEP set constants for set point
0010.0005     time:00:00:05
0010.0010     kil=57
0010.0015     kic=38
0010.0020     kis=29
0010.0025     kxlc=0
0010.0030     kxcc=0
0010.0035     kxsc=0
0010.0040     kxlh=0
0010.0045     kxsh=0

0015.0000   STEP set point
0015.0005     time:00:00:06
0015.0010     templ=400
0015.0015     tempc=400
```

```
0015.0020      temps=400

0020.0000    STEP set constants for set point
0020.0005      time:00:00:05
0020.0010      kil=57
0020.0015      kic=38
0020.0020      kis=29
0020.0025      kxlc=4
0020.0030      kxcc=2
0020.0035      kxsc=3
0020.0040      kxlh=16
0020.0045      kxsh=16

0025.0000    STEP set point
0025.0005      time:00:00:06
0025.0010      templ=450
0025.0015      tempc=450
0025.0020      temps=450

0030.0000    STEP constants for set point
0030.0005      time:00:00:05
0030.0010      kil=50
0030.0015      kic=33
0030.0020      kis=27
0030.0025      kxlc=4
0030.0030      kxcc=2
0030.0035      kxsc=3
0030.0040      kxlh=16
0030.0045      kxsh=16

0035.0000    STEP set point
0035.0005      time:00:00:06
0035.0010      templ=500
0035.0015      tempc=500
0035.0020      temps=500

0040.0000    STEP constants for set point
0040.0005      time:00:00:05
0040.0010      kil=42
0040.0015      kic=30
0040.0020      kis=25
0040.0025      kxlc=5
0040.0030      kxcc=3
0040.0035      kxsc=4
0040.0040      kxlh=16
0040.0045      kxsh=16
```

```
0045.0000   STEP set point
0045.0005     time:00:00:06
0045.0010     templ=550
0045.0015     tempc=550
0045.0020     temps=550

0050.0000   STEP constants for set point
0050.0005     time:00:00:05
0050.0010     kil=36
0050.0015     kic=24
0050.0020     kis=22
0050.0025     kxlc=6
0050.0030     kxcc=4
0050.0035     kxsc=5
0050.0040     kxlh=16
0050.0045     kxsh=16

0055.0000   STEP set point
0055.0005     time:00:00:06
0055.0010     templ=600
0055.0015     tempc=600
0055.0020     temps=600

0060.0000   STEP constants for set point
0060.0005     time:00:00:05
0060.0010     kil=29
0060.0015     kic=19
0060.0020     kis=19
0060.0025     kxlc=7
0060.0030     kxcc=5
0060.0035     kxsc=6
0060.0040     kxlh=16
0060.0045     kxsh=16

0065.0000   STEP set point
0065.0005     time:00:00:06
0065.0010     templ=700
0065.0015     tempc=700
0065.0020     temps=700

0070.0000   STEP constants for set point
0070.0005     time:00:00:05
0070.0010     kil=23
0070.0015     kic=17
0070.0020     kis=16
0070.0025     kxlc=9
```

```
0070.0030     kxcc=7
0070.0035     kxsc=8
0070.0040     kxlh=16
0070.0045     kxsh=16

0075.0000   STEP set point
0075.0005     time:00:00:06
0075.0010     templ=800
0075.0015     tempc=800
0075.0020     temps=800

0080.0000   STEP constants for set point
0080.0005     time:00:00:05
0080.0010     kil=18
0080.0015     kic=14
0080.0020     kis=13
0080.0025     kxlc=11
0080.0030     kxcc=9
0080.0035     kxsc=10
0080.0040     kxlh=16
0080.0045     kxsh=16

0085.0000   STEP set point
0085.0005     time:00:00:06
0085.0010     templ=900
0085.0015     tempc=900
0085.0020     temps=900

0090.0000   STEP constants for set point
0090.0005     time:00:00:05
0090.0010     kil=13
0090.0015     kic=12
0090.0020     kis=10
0090.0025     kxlc=13
0090.0030     kxcc=11
0090.0035     kxsc=12
0090.0040     kxlh=16
0090.0045     kxsh=16

0095.0000   STEP set point
0095.0005     time:00:00:06
0095.0010     templ=1050
0095.0015     tempc=1050
0095.0020     temps=1050

0100.0000   STEP constants for set point
```

```
0100.0005     time:00:00:05
0100.0010     kil=9
0100.0015     kic=9
0100.0020     kis=8
0100.0025     kxlc=16
0100.0030     kxcc=14
0100.0035     kxsc=15
0100.0040     kxlh=16
0100.0045     kxsh=16

0105.0000   STEP set point
0105.0005     time:00:00:06
0105.0010     templ=1200
0105.0015     tempc=1200
0105.0020     temps=1200

0110.0000   STEP constants for set point
0110.0005     time:00:00:05
0110.0010     kil=7
0110.0015     kic=7
0110.0020     kis=7
0110.0025     kxlc=19
0110.0030     kxcc=17
0110.0035     kxsc=18
0110.0040     kxlh=16
0110.0045     kxsh=16

0115.0000   STEP set point
0115.0005     time:00:00:06
0115.0010     templ=1373.7
0115.0015     tempc=1373.7
0115.0020     temps=1373.7

0120.0000   STEP constants for set point
0120.0005     time:00:00:05
0120.0010     kil=6
0120.0015     kic=5
0120.0020     kis=6
0120.0025     kxlc=22
0120.0030     kxcc=20
0120.0035     kxsc=21
0120.0040     kxlh=16
0120.0045     kxsh=16

0125.0000   STEP
0125.0005     end process
```

KMSET

Load and run to set KM values to the current best guess if memory on DTC board lost because of power loss or reset. Used before running calibration (see NEWCAL) after memory lost on DTC because KM's for epi tube are very different from standard Tylan values. The stored KM values help the tube converge faster to the desired set point temperature. Because of memory limitations, only set KM's for the desired operating points. Note that the set point temperatures for the end zones cannot be as high as the center zone, or else the center zone will turn off.

```
process id: kmset
description: current best guesses for km's 9/14/89
bank: 1
tubes: 10
reuse: yes

0001.0000   STEP initialization
0001.0005     dtcena=on
0001.0010     n2purg=0
0001.0015     templ=350
0001.0020     tempc=350
0001.0025     temps=350
0001.0030     templ tolerance=1
0001.0035     tempc tolerance=1
0001.0040     temps tolerance=1
0001.0045     kr=40
0001.0050     kc=30
0001.0055     kp=20

0005.0000   STEP set point
0005.0005     time:00:00:10
0005.0010     templ=500
0005.0015     tempc=525
0005.0020     temps=500

0010.0000   STEP set constants for set point
0010.0005     time:00:00:05
0010.0010     kml=103  1648
0010.0015     kmc=31   496
0010.0020     kms=133  2128

0015.0000   STEP set point
0015.0005     time:00:00:10
0015.0010     templ=835
0015.0015     tempc=850
```

```
0015.0020     temps=835

0020.0000   STEP set constants for set point
0020.0005     time:00:00:05
0020.0010     kml=189  3024
0020.0015     kmc=63   1008
0020.0020     kms=244  3904

0025.0000   STEP set point
0025.0005     time:00:00:10
0025.0010     templ=1040
0025.0015     tempc=1075
0025.0020     temps=1040

0030.0000   STEP constants for set point
0030.0005     time:00:00:05
0030.0010     kml=219  3504
0030.0015     kmc=157  2512
0030.0020     kms=238  3808

0035.0000   STEP set point
0035.0005     time:00:00:10
0035.0010     templ=980
0035.0015     tempc=1000
0035.0020     temps=970

0040.0000   STEP km's
0040.0005     time:00:00:05
0040.0010     kml=203  3248
0040.0015     kmc=102  1632
0040.0020     kms=255  4080

0045.0000   STEP set point
0045.0005     time:00:00:10
0045.0010     templ=935
0045.0015     tempc=950
0045.0020     temps=935

0050.0000   STEP km's
0050.0005     time:00:00:05
0050.0010     kml=204  3264
0050.0015     kmc=81   1296
0050.0020     kms=253  4048

0055.0000   STEP
0055.0005     end process
```

MANCAL

Manual calibration routine to store the temperature offsets between internal and external thermocouples. Also stores KM's at the desired set points. Because of memory limitations only calibrate at desired set points. Loop manually through calibration step by hitting ALMACK button. It is important that the temperature is stable before each calibration step.

```
process id: mancal
description: calibration for 10 with auto tc connect 45 sec
bank: 1
tubes: 10
reuse: yes

0001.0000   STEP ready
0001.0005     dtcena=on
0001.0010     n2purg=0
0001.0015     templ=350
0001.0020     tempc=350
0001.0025     temps=350
0001.0030     templ tolerance=1
0001.0035     tempc tolerance=1
0001.0040     temps tolerance=1
0001.0045     krl=80
0001.0050     krc=25
0001.0055     krs=100
0001.0060     kcl=75
0001.0065     kcc=20
0001.0070     kcs=95
0001.0075     kp=80
0001.0080     ccout10=off
0001.0085     h2=0
0001.0090     hcl=0
0001.0095     sih2cl2=0

0005.0000   STEP
0005.0005     time:00:00:00
0005.0010     vacuum=on
0005.0015     n2purg=300
0005.0020     if almack=on goto 0010

0010.0000   STEP temp
0010.0005     time:00:00:00
0010.0010     templ=variable
0010.0015     tempc=variable
```

```
0010.0020     temps=variable
0010.0025     if almack=on goto 0015

0015.0000   STEP connect calib tc's and chance to skip
0015.0005     time:00:00:45
0015.0010     ccout10=on
0015.0015     if almack=on goto 0025

0020.0000   STEP
0020.0005     calibrate

0025.0000   STEP disconnect calib tc's and wait
0025.0005     time:00:00:00
0025.0010     ccout10=off
0025.0015     if almack=on goto 0030

0030.0000   STEP chance to loop back to calibrate again
0030.0005     time:00:00:10
0030.0010     if almack=on goto 0010

0035.0000   STEP
0035.0005     end process
```

EPIMOX

Oxidation recipe to grow a masking oxide for selective epitaxy. The oxidation temperature of 850° C is chosen to minimize oxide stress during selective epitaxy at the same temperature.

```
process id: epimox
description: denude + grow epi masking oxide (9/16/89)
bank: 1
tubes: 1,2
reuse: yes

0001.0000   STEP initialize (idle state)
0001.0005     dtcena=on
0001.0010     templ=750 deg c
0001.0015     tempc=750
0001.0020     temps=750
0001.0025     templ tolerance=2
0001.0030     tempc tolerance=2
0001.0035     temps tolerance=2
0001.0040     n2=1.0 slpm
0001.0045     kp=20
0001.0050     krl=80
0001.0055     krc=80
0001.0060     krs=90
0001.0065     kcl=40
0001.0070     kcc=40
0001.0075     kcs=45
0001.0080     heater=on
0001.0085     tube=off
0001.0090     purge=off
0001.0095     drain=off
0001.0100     tempena=on

0005.0000   STEP boat out and turn on low o2
0005.0005     time:01:00:00
0005.0010     n2=5.0 slpm
0005.0015     o2=0.2 slpm
0005.0020     load=off
0005.0025     unload=on
0005.0030     if almack=on goto 0010

0010.0000   STEP boat in
0010.0005     time:01:00:00
0010.0010     unload=off
```

```
0010.0015    load=on
0010.0020    if bpin=on goto 0015
0010.0025    if almack=on goto 0015

0015.0000   STEP test boat in
0015.0005    time:00:00:20
0015.0010    load=on
0015.0015    if bpin=off goto 0065
0015.0020    if bpout=on goto 0065

0020.0000   STEP ramp up to denude temp
0020.0005    time:02:00:00
0020.0010    temps=1050
0020.0015    tempc=1050
0020.0020    templ=1050
0020.0025    if tempc=1050 goto 0025
0020.0030    if almack=on goto 0025

0025.0000   STEP denude time
0025.0005    time:04:00:00
0025.0010    if almack=on goto 0030

0030.0000   STEP ramp to oxidation temp
0030.0005    time:02:00:00
0030.0010    temps=850
0030.0015    tempc=850
0030.0020    templ=850
0030.0025    if tempc=850 goto 0035
0030.0030    if almack=on goto 0035

0035.0000   STEP temperature stabilization
0035.0005    time:00:02:00
0035.0010    if almack=on goto 0045

0040.0000   STEP temperature check
0040.0005    time:00:00:30
0040.0010    if temps#850 goto 0035
0040.0015    if tempc#850 goto 0035
0040.0020    if templ#850 goto 0035
0040.0025    if almack=on goto 0045
0040.0030    if stmflt=off goto 0035 (check steam heater)

0045.0000   STEP wet oxidation
0045.0005    time:variable wet ox time
0045.0010    n2=0
0045.0015    o2=0.2
```

```
0045.0020     tube=on   (check water dripping)
0045.0025     if almack=on goto 0050

0050.0000   STEP end wet oxidation
0050.0005     time:00:05:00
0050.0010     o2=4.0
0050.0015     tube=off  (stop dripping)
0050.0020     purge=on  (purge steam generator)
0050.0025     drain=on  (is it still used?)
0050.0030     if almack=on goto 0055

0055.0000   STEP n2 anneal
0055.0005     time:00:20:00
0055.0010     n2=4.0
0055.0015     o2=0.0
0055.0020     if almack=on goto 0060

0060.0000   STEP ramp down to unload
0060.0005     time:02:00:00
0060.0010     n2=1.0
0060.0015     heater=on
0060.0020     drain=off
0060.0025     tube=off
0060.0030     purge=off
0060.0035     temps=750
0060.0040     tempc=750
0060.0045     templ=750
0060.0050     if tempc=750 goto 0065

0065.0000   STEP
0065.0005     end process
```

EPISOX

Recipe to grow a sacrificial oxide that removes substrate damage due to the plasma etch. The oxidation temperature of 850° C was chosen to minimize oxide stress during selective epitaxy at the same temperature.

```
process id: episox
description: sacrificial oxide for epi (9/16/89)
bank: 1
tubes: 5,6
reuse: yes

0001.0000   STEP initialize (idle state)
0001.0005      dtcena=on
0001.0010      templ=750
0001.0015      tempc=750
0001.0020      temps=750
0001.0025      templ tolerance=2
0001.0030      tempc tolerance=2
0001.0035      temps tolerance=2
0001.0040      n2=1.0
0001.0045      o2=0
0001.0050      kp=16
0001.0055      kr=50
0001.0060      kc=20
0001.0065      n2carr=0
0001.0070      anao2=0
0001.0075      vent=off
0001.0080      tca=off

0005.0000   STEP boat out and turn on low o2
0005.0005      time:01:00:00
0005.0010      n2=5.0 slpm
0005.0015      o2=0.2 slpm
0005.0020      load=off
0005.0025      unload=on
0005.0030      if almack=on goto 0010

0010.0000   STEP boat in
0010.0005      time:01:00:00
0010.0010      unload=off
0010.0015      load=on
0010.0020      if bpin=on goto 0015
0010.0025      if almack=on goto 0015
```

```
0015.0000   STEP boat check
0015.0005     time:00:00:20
0015.0010     load=on
0015.0015     if bpin=off goto 0050

0020.0000   STEP ramp to oxidation temp
0020.0005     time:00:20:00
0020.0010     templ=ramp to 850
0020.0015     tempc=ramp to 850
0020.0020     temps=ramp to 850
0020.0025     if almack=on goto 0025

0025.0000   STEP temperature stabilization
0025.0005     time:00:02:00
0025.0010     if almack=on goto 0035

0030.0000   STEP temperature check
0030.0005     time:00:00:30
0030.0010     if templ#850 goto 0025
0030.0015     if tempc#850 goto 0025
0030.0020     if temps#850 goto 0025
0030.0025     if almack=on goto 0035

0035.0000   STEP dry oxidation
0035.0005     time:02:30:00  target 200a
0035.0010     n2=0
0035.0015     o2=4.0
0035.0020     if almack=on goto 0040

0040.0000   STEP n2 anneal
0040.0005     time:00:20:00
0040.0010     o2=0
0040.0015     n2=4.0
0040.0020     if almack=on goto 0045

0045.0000   STEP ramp down to unload
0045.0005     time:02:00:00
0045.0010     n2=1.0
0045.0015     templ=750
0045.0020     tempc=750
0045.0025     temps=750
0045.0030     if tempc=750 goto 0050

0050.0000   STEP
0050.0005     end process
```

A.3

Maintenance Procedures

Hydrogen Bottle Change

WHEN NOT USING REACTOR, turn off hydrogen bleed at hydrogen purifier and close bottle. Hydrogen bottle lasts about 4-5 experiments if using 8slpm during bake. Flow fuse will trip from pressure surge switching from high flow to low flow if pressure is allowed to get below 200 psi during bake. Therefore, do not start experiment if less than 500 pounds in bottle. If hydrogen clean the bleed flow at purifier only needs to be about 200 ccm for 8 slpm, occasionally a bad bottle of hydrogen needs a larger bleed flow or else pressure of output will drop below the 20 psi mass flow controller needs. Check pressure on regulator on input to mass flow controller first time using a new bottle.

Drawings: 9 & 10

BOTTLE REMOVAL:

1) Make sure bleed flow valve on hydrogen purifier is closed. Make sure hydrogen bottle is closed tightly.
2) Turn flow fuse to bypass and turn 2-way valve to vent. Hydrogen trapped in pigtail will escape.
3) Loosen CGA nut (left-hand thread) and remove the flow fuse and regulator assembly by pulling CGA fitting out straight so as not to scratch it. The assembly will hang from the attached cord to minimize strain on pigtail. Place an unused glove over the CGA fitting of the flow fuse to protect it from dirt on hydrogen bottles.
4) Cap old bottle, loosen strap, and remove. Make sure to label old bottle as empty and send mail to hydrogen@argon to report usage and inventory in gas room.

BOTTLE INSTALLATION:

1) Place full bottle in its place, tighten strap, and remove cap. If CGA connection pointing the wrong way, loosen strap slightly and turn bottle. Retighten strap (a tight strap prevents bottle from rotating later and straining pig tail connection).
2) Use a lint-free towel to clean the inside of the CGA fitting on the new bottle (hydrogen bottles from welding supplier so usually very dirty).
3) Remove glove from flow fuse CGA and guide it carefully to the mating fitting on the bottle to avoid the dirt. Tighten fitting by hand.

4) Use a wrench to tighten the CGA nut. Make sure to not hit the flow fuse valve handle with the wrench or else the flow fuse will rotate unnecessarily.

5) Turn 2 way valve to in-between position so not open either way. Put flow fuse valve in bypass position. Briefly open hydrogen bottle and close again.

6) Monitor feed pressure on the regulator, should stay constant. If pressure decreases tighten the CGA nut and briefly open bottle again. If after tightening the CGA several times without maintaining the pressure then bottle part of the fitting is faulty, Follow removal procedure, label bottle as full with faulty fitting. Send mail to hydrogen@argon to report usage and storage status.

7) If pressure remains constant then check fitting with Snoop to ensure there is not a smaller leak than can be detected by pressure drop.

8) Open cylinder and leave flow fuse valve in bypass position. Crack 2-way valve briefly from no-open position to the vent position 5 times, wait 1 minute for hydrogen to clear in vent, and repeat procedure 3 times. This will step will purge the pigtail section of air before the bottle is connected to the purifier.

9) Close bypass valve of flow fuse and turn 2-way valve to purifier position Open bleed flow valve on purifier. Turn the flow fuse to bypass and close again to ensure not tripped.

10) If the new hydrogen bottle is not needed directly for an experiment, close the bleed flow valve on the purifier and close valve on bottle.

Hydrogen Purifier

A diagram is posted on the cabinet leading to the rear of the hydrogen purifier that summarizes these procedures. Valves referred to by number have labels with these numbers.

Drawings: 9

SHUT-DOWN PROCEDURE:

1) Switch MFS 460 to manual mode with N2=500.

2) Make sure bleed (valve #5) is closed.

3) Shut input hydrogen valve (valve #2) in back of purifier.

4) Set hydrogen flow on MFS 460 for any flow greater than 2500.

5) Turn on hydrogen flow on MFS 460. Will give flow fault alarm after 101 seconds and shut off flow. Acknowledge alarm and start hydrogen again.

6) Repeat (5) until gauge on hydrogen regulator reads about -20 mm Hg. Record pressure.

7) Turn off power to purifier

TURN ON PROCEDURE:

1) Gauge on hydrogen regulator should read at least -20 mm Hg before proceeding to step (2).
   a) If line was serviced pump it down using the shut down procedure above.
   b) If no service requiring venting the line was done, the pressure should read exactly as in step (6) above. If not so, there is large leak in the critical section from purifier to MFC and it must be fixed before using the system.

2) Turn on power to purifier and set temperature controller to 400° C.

3) When the temperature is 400° C the hydrogen valve to the purifier (valve #2) can be opened.

Preventive Care for Flange Cooling System

Judging from the condition of removed filters the appropriate interval for this service is 6 MONTHS or less.

Drawings: 11, 12, 13, 15, & 19

NOTES:

A) Tube 10 must be cold to perform this maintenance safely. Can avoid having to reset the firing board by first pushing the cooling abort over-ride by the ROP panel, but have to make sure that a no heat recipe is loaded to avoid the possibility of heaters going on by misstake. Also have to remember to turn off over-ride when ready to turn on heaters.

B) Pump on chiller can start up in a severe pressure oscillation mode. When starting it always check the pressure gauge on the front of the chiller. If the needle oscillate wildly between 35-65 psi the pump must be shut off and restarted. Sometimes may have to restart a few times. Normal reading on pressure gauge is about 50 psi and only oscillating a few psi.

C) Water will leak out of the chiller tank when changing the filter and DI cartridge in back of chiller. Using a bucket underneath the housings avoids a mess.

PROCEDURE:

1) Close city back up valve and turn off chiller.

2) Remove the 2 filters in the cooling loop and DI cartridge.

3) Put chiller in manual and start. Add a gallon of peroxide to tank through view port. Have to dump some water from chiller to fit all of the peroxide in. Can dump some water from the chiller tank by closing valve D and open C. This will switch return to drain rather than back to chiller. Use the manual switch box below the status panel to operate valves C and D. Moving the 3 position switches from auto to center off with the chiller running will dump the return to drain.

4) Check the condenser coils for dirt. Should be able to see them clearly through grill. If dirty this is a good time to remove grill and vacuum out the dirt with the house vacuum.

5) After about 1 hour, turn off chiller and put new filters into cooling loop and on city water back up. The city water stub should have been depressurized in step (3) by auto-fill.

6) Leave chiller off and turn on city water back up valve. Run for 10 minutes to get rid of peroxide in loop.

7) Start chiller, this will turn off city water back up. Repeatedly dump return to drain by closing valve D and opening C, as in step (3). Dump to drain 6 times 2 mintues, waiting between each repeat for the tank to refill via the auto-fill. The status light on front of chiller lights when auto-fill valve is open.

8) Turn off chiller and install DI cartridge.

9) Turn on chiller and reset status panel errors.

10) Put chiller in auto-off mode.

11) Label all filter cartridges with date changed. Fills 2 functions: (1) makes it easy to check when last serviced, and (2) the label serves as a mark to ensure that housing tight but not overtightened.

Temperature Calibration

Since this procedure sometimes required after major mishap, such as a power failure, make sure cooling system running ok. Flow should be 1.5 gpm and water return temperature 21° C.

Drawings: 3 & 11

PROCEDURE:

1) Load and run DTCSET (sets constants to version 1.0).

2) Load and run KMSET (set KM's to latest best guesses, especially, important for set points not included in the calibration).

3) Set offsets on DTC card to zero.

4) Check that internal 3 junction T/C is in proper place. Have black mark that should line up with end of T/C well.

5) Make sure internal T/C connected by turning switch on box where internal T/C connect to MANUAL. Connection ok if internal T/C reads ok on TYCOM CALIB inputs.

6) Load and run MANCAL for the following load/center/source temperatures:

   500 / 525 / 500
   980 / 1000 / 970
   880 / 900 / 880
   835 / 850 / 835
   785 / 800 / 785

   Usually do them in this order to make sure that the two last get stored correctly (deposition temperatures). MANCAL runs by waiting in step 10 to stablize the temperature. Push ALMACK when the temperature is judged stable. This connects the internal T/C's to the CALIB inputs (front panel readouts will overrange) for a short time (long enough not to stablize input to DTC but not too long so the the temperature unstable, 45 sec). Can take several hours to stablize the temperature for the first run of MANCAL, then faster as get closer. Before pushing ALMACK the FRONT PANEL display should have been stable for 30 minutes, and TYCOM TEMP inputs should be at the set points. Fewer iterations necessary if the the temperature is stable before each calibration step.

   Pushing ALMACK two times in a row in the waiting step after the calibration step

loops the program back to step 10.

7) When calibration completed, set offsets on DTC board so that the temperature indicated by FRONT PANEL and TYCOM TEMP inputs agree. The the temperature offset is annoying during MANCAL since it makes it harder to decide when calibration at a given set point completed. Best to repeat the calibration step until no more improvement. The remaining difference for each set point as to be fairly constant over the operating the temperature range. Use the offset observed at the 835/850/835 since most important right now for depositions (could change in the future).

8) Done with calibration and ready to use. Performance to be expected after all this should be set point +- 2 C. Goal for calibration is - 1 + 0 C since system drifts a little with time The reason for skewed tolerance is because the meters in the front are more accurate than their display. According to the calibrator box the front panel meters display XXX from is true for inputs XXX.0 to XXX.9.

Quartz Cleaning Procedure

The silicon deposited on the quartzware must be removed periodically to reduce particles. Have found that easiest to clean, and fewest particles form, if tube cleaned before deposits get thicker than about 60-100 μm thick.

Drawings: 1

QUARTZWARE REMOVAL:

1) Let tube idle in EPISTNBY for at least 24 hrs. The longer the better. Reduces the HCl evolution from deposit in rear of tube by running with N2 in standby for as long as possible before pulling liner.

2) Let cool by running EPIVAC overnight. Takes that long to cool all the way to room the temperature.

3) Mark and measure location of cantilever mounting block. White tape along side of mounting surface works well for rough adjustment. In case tape moves also use metal scale measure to 1/64th two places each back and side. Saves time later, especially with in-out placement.

4) Prepare a clean surface to place quartzware on. Have hex wrenches for cantilever block available and a tape measure. Make sure tube sink is ready to receive rear baffle block and liner. They will get hot and release HCl when exposed to air. Have a supply of clean gloves available. Never touch quartzware with dirty gloves and wear face shields to reduce contamination of quartzware.

5) Load and run N2.CLEAN. Step 10 is the timed vent. When recipe gets to step 15 ready to open. Push ALMACK to get to step 20 and turn on N2REAR.

6) Open tube. Loosen the cable so door can be moved all the way back, making baffles easier to remove.

7) Measure location of quartzware. Use door sealing surface as reference (see Drw. 1). Measure to surface facing heat of front 7 baffles. Measure distance to where two standard boats touch at center. Measure to surface facing heat of the 3 rear baffles.

8) Remove boats and baffles. Baffles have to be slid carefully to the rear and slipped of the rods by tilting forward.

9) Remove the cantilever sheaths by sliding gently off in to the furnace and then pull out. Remove cantilever rods by pulling out of cantilever block.

10) Use a quartz rod with a hook to extract the rear baffle block. The rear baffle block has a 2 cm dia. hole to insert the hook into. The rear baffle block rests partially on the thermocouple cover so will have to be extracted at the same time.

11) Remove door and cantilever block by removing the 4 screws on bottom. Be really careful here when removing the last screw. Block made of aluminum and door stainless steel makes the assembly very front heavy. Will easily fall of the platform if not restrained with the free hand. Place on bottom of loading station. Do not want to carry around and get dirty.

12) TRICKY STEP. Remove liner. Difficult to get a grip on. Put both hands into the liner and press outward while pulling seems to work best. (An improvement would be two small protrusion to make the liner easier to pull). Using clean rubber gloves that slip less makes it easier. Once starting to emerge from the tube it is easy. At this point need two people. One to quickly carry the liner to the cleaning sink and the other to open doors. Rear end will get hot and release HCl when exposed to air. Good idea to wear face masks and breathing masks at this step.

13) Put door assembly back on platform. Needs to be put on accurately on the in-out axis so that the door interlock is activated.

14) Close door and ALMACK program to step 30. Will pumpdown and put system in standby vacuum.

15) At this point system is protected under vacuum and quartzware can be cleaned when convenient with HF and nitric acid to remove the silicon deposits. Best to clean liner, thermocouple sheath, and rear baffle first. They have to be put in first and in that order.

At this point when system cold it is a good time to do any PREVENTIVE MAINTENANCE on the cooling system.

QUARTZWARE INSTALLATION:

1) As a philosophy too sure that it is a good idea to put the quartzware soaking wet in to the tube. Puts a lot of moisture in to the system which can react with the deposits in the tubing that leads to the pump. Also when the moisture evaporates under pumpdown the system gets very cold (close to 0° C). Prefer partially dry quartzware instead.

2) When liner, thermocouple sheath, and rear block are ready for installation abort N2.CLEAN. Restart N2.CLEAN and run the vent step 10 again. At step 15 ALMACK to 20 and open tube all the way as in (6).

3) Remove door assembly as in (11).

4) Install liner. Slide in gently while being careful to line up with the thermocouple well that fits into the small hole on the bottom of the liner.

5) Install the thermocouple cover.

6) Put the rear baffle block on top of the thermocouple cover inside the tube and push it in with one of the cantilever rods until about a foot of the rod sticks out. The last bit will be pushed in once rods mounted on in door. This places the rear baffle block as close to end of cantilever rods as possible.

7) Install door assembly, try to get it as close as possible to the original position by using the measured location from (3). Will have to be fine tuned in the sideways axis once all the quartzware is installed.

8) At this point, if the other pieces not ready, close tube and evacuate again by going to step 30 again. Want to minimize time open at all times. Can take long time to evacuate at this point if a lot of moisture on quartzware. Time limit in pumpdown step is 2 min. Rerun if necessary, or run in manual.

9) To avoid the severe cooling of the tube in (8), load and run EPIWARM for a few minutes. Then load and run N2.CLEAN again.

10) When rest of quartzware ready then go through the venting procedure again and open the door all the way as in (6). Reverse sequence of installing the rods and associated quartzware.

11) NOTE. The cantilever rods do not have identical diameters, try both ways and it will be obvious which way they fit best. ALSO, the cantilever rods are not straight and will droop if not rotated to be flat or slightly up. This adjustment can be made eye first and then fine adjusted with the quartzware installed on the rods.

12) PLACEMENT of the baffles and boats is critical for consistent performance. The recommended placements are given in drawing 1. Note that the front sealing surface for the door is used as the reference since easiest to measure from.

13) Close tube and ALMACK to pumpdown. Load and run EPIWARM which is the same program as the standby except the temperature is 400/425/400 (the lowest that

can be controlled with the typical calibration offsets). Good idea to run this recipe first, since less abrupt ramp to the temperature and to check that cooling system is ok after preventive maintenance. O-rings can survive up to 350° C so cooling failure might be survivable with EPIWARM temperatures.

14) Once stable in EPIWARM and cooling system seems ok, load and run EPISTNBY.

15) Before system is ready for deposition experiments it should go through a dummy run to bake out the quartz and coat it with silicon. Recommended run is a 30 min 1040/1075/1040 hydrogen bake followed by a 100 min 835/850/835 standard deposition.

Power Shut Down

SHUT-DOWN PROCEDURE:

Hydrogen Purifier:

The palladium diffusion cell could crack if allowed to cool in the prescence so follow its given shut-down procedure.

Reactor Tube:

1) Load and run EPIVAC.

2) Put MFS 460 in manual.

3) Turn off all gasses but leave vacuum on. Will hard pump the system to pressure limited by bleed (60-80 mtorr).

4) After 30 sec. shut gate valve and turn power off to MFS 460. Switch in the back of unit. Protects it from any surges when power on.

Cooling System:

Safe to turn off cooling system once tube temperature by front panel reads less than 30° C. Once this temperature has been reached the chiller power button can be switched off (Drw. 19) can be turned off, and the city water backup valve (Drw. 14) can be closed to save water when power goes off. If tube still hot and power going off soon, leave the city back up on until cool and then turn the city water off. Chiller will not restart by itself after a power failure.

TURN-ON PROCECDURE:

Cooling System:

1) Open city water back-up valve (Drw. 14).

2) All lights on the control panel should be lit (Drw. 15). Once flow established with city water back-up hit the reset buttons for each fault except chiller. The lights

should turn off if ok.

3) Switch chiller failure mode to manual (Drw. 19), turn on power, and push pump start. Should turn off lights for chiller fault and back-up valves on control panel (Drw. 15). Switch failure mode switch to auto.

Reactor Tube:

1) Turn on MFS 460, acknowledge alarm, and do not command any flows. It will auto-zero readings for all gas flows except N2. Can take 10 min. or more to auto-zero. If not auto-zeroed false leak alarms are likely.

2) Once all gas flows (except N2) read zero, turn on gate valve and N2=500.

3) Can leave system in step (2) manual mode, or restart EPIVAC and put in auto mode.

4) Once established that cooling system ok, then load and run EPISTNBY.

Hydrogen Purifier:

Follow directions given for its start-up procedure.

A.4

Preparation of Selective Epitaxy Wafers

Selective Epitaxy Wafer Preparation

Rev. 1.0
(9/13/89)

RUN:

1. SELECT STARTING WAFERS

- Manufacturer:
- Prime or test:
- Doping type:
- Doping species:
- Doping density:
- Orientation:
- Other (backside gettered, etc.):

2. DENUDE SURFACE AND GROW MASK OXIDE

2.1 Load recipe EPIMOX for 4 hrs. of denuding at 1050 °C and variable wet oxidation time at 850 °C† in Tylan 1 or 2.

2.2 Set push and pull speed for 10 inch/min fast and 6 inch/min slow.

2.3 Run recipe and load wafers fresh from the shipping box directly into Tylan 1 or 2.

2.4 Measure thickness of mask oxide with NANOSPEC.

- Date and time started:
- Tube 1 or 2:
- Oxidation time:

† This temperature chosen same as epitaxial growth temperature to reduce oxide stress.

- Target thickness:
- Measured thickness:
- Date and time finished:

3. PHOTORESIST COATING

3.1 If wafers have been sitting longer than 2 days (?) after oxidation, dehydrate by inserting into an idle oxidation tube at 750 °C for 15 min.

3.2 Load wafers into blue EATON cassette and immerse into HMDS vapor in sink 5 for 90 sec.

3.3 Use EATON to spin and softbake using standard positive resist program number 10 (KTI 820, 60 sec softbake).

- Date and time started:
- Dehydration bake:
- HMDS time:
- Date and time finished:

4. EXPOSE AND DEVELOP

4.1 Expose wafers in GCA using standard parameters for focus and exposure.

4.2 Develop wafers in MTI using standard positive resist development program number 1 (KTI 934 1:1, 60 sec).

- Date and time started:
- Mask(s):
- Job name:
- Focus:
- Exposure:
- Date and time finished:

5. DESCUM, HARD BAKE, AND SCRIBE

5.1 Descum by using modified chamber clean recipe in LAM 1 (O_2 = 200 sccm, He = 100 sccm, 100 W, 15 sec).

5.2 Hard bake for 20 min at 120 °C.

5.3 Scribe each wafer on front by flat in areas of unpatterned resist with run identification and number.

- Date and time started:
- LAM 1 recipe used:
- Hard bake temperature and time:
- Run identification and numbers scribed:
- Date and time finished:

6. PLASMA ETCH

6.1 Vertical oxide etch in LAM 2 (2500-3000 Å/min). Use recipe which minimizes polymerization.

6.2 Measure typical oxide thickness remaining with NANOSPEC in areas where not etched to silicon, if any.

- Date and time started:
- LAM 2 recipe used:
- Oxide thickness remaining:
- Date and time finished:

7. RESIST STRIP AND SINK 8 CLEAN

7.1 Strip resist with acetone in MTI with standard strip program number 10 (acetone, DI rinse, N_2 dry).

7.2 Start DI rinsing tanks 1, 2, and 3. Wet in tank 1 and then put wafers in sink 8 piranha for 10 min.

7.3 Rinse in tanks 1 and 2 for at least 2 min each with some shaking.

7.4 Rinse in tank 3 until resistivity within 1 Mohm of empty tank.
7.5 Spin dry.
7.6 Store wafers in box dedicated for wafers waiting for sink 6 cleaning.

- Date and time started:
- Tank 3 resistivity:
- Resistivity each wafer batch:
- Date and time finished:

8. SINK 6 CLEAN AND SACRIFICIAL OXIDE GROWTH

8.1 Start DI rinsing tanks 1, 2, and 3 (or 4, 5, and 6). Wet in tank 1 and then put wafers in sink 6 piranha for 10 min.
8.2 Rinse in tanks 1 and 2 for at least 2 min each with some shaking.
8.3 Rinse in tank 3 until resistivity within 1 Mohm of empty tank.
8.4 Use 10:1 HF to dip to bead in areas which had oxide left + 20 sec. overetch.
8.5 Rinse in tanks 1 and 2 for at least 2 min each with some shaking.
8.6 Rinse in tank 3 until resistivity within 1 Mohm of empty tank.
8.7 Spin dry.
8.8 Put wafers in box dedicated to transfer of wafer from sink 6 to the TYLAN's.
8.9 Load recipe EPISOX for fixed 150 min dry oxidation time at 850 °C into Tylan 5 or 6 (target 200 Å).
8.10 Set push and pull speed for 10 inch/min fast and 6 inch/min slow.
8.11 Run recipe and load wafers from the transfer box into Tylan 5 or 6.
8.12 Unload wafers into box dedicated for wafers ready for sink 6.
8.13 Measure oxide thickness of sacrificial oxide with NANOSPEC.

- Date and time started:
- Which piranha(s) and rinse tanks used:
- Rinse tank resistivity:
- Resistivity each wafer batch, rinse 1:
- Time in 10:1 HF:
- Resistivity each wafer batch, rinse 2:

- **Oxide thickness:**
- **Date and time finished:**

A.5

Selective Epitaxy Growth Procedure

Selective Epitaxy Growth

Rev. 1.0

(11/20/90)

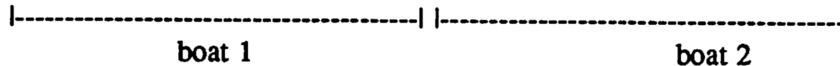
EXPT:

1. SELECT WAFERS AND POSITIONS

- Wafers included in experiment:

- Positions in furnace (incl. dummies and empty slots):

<-- front



boat 1 boat 2

- Flat orientation (normally up):

2. LOADING AND RUNNING EPITAXIAL GROWTH RECIPE

2.1 Check HYDROGEN pressure in cylinder. If less than 500 psi do not start run before putting a new bottle on system. Read documentation for details on how to change bottle. Remember to send mail to hydrogen@argon.

2.2 Make sure hydrogen PURIFIER is on and at 400 °C. Turn on hydrogen and set bleed for 300 sccm (increase bleed flow if delivery pressure drops below 20 psi due to contamination of hydrogen feed). Read documentation for details on how to turn on hydrogen.

2.3 Verify that TYLAN 10 is at correct loading temperature, 500/525/500 °C, and then load growth recipe EPI.18T. Do so by interrupting the furnace for the least amount of time. First enter the PARAMETERS on the TYCOM, but do

not hit the return after the last entry (deposition time). ABORT the system with the ROP panel, and then hit the RETURN on the TYCOM terminal.

2.4 RUN and ACKNOWLEDGE growth recipe to step 10 (N_2 = 300 sccm, loading temp.).

2.5 If polysilicon FLAKES present from TYLAN 11, use house vacuum (hose in CV2) to clean the loading area and especially around the door. Reduces chance that flakes end up on the o-ring of the door.

- Hydrogen pressure:

- Recipe parameters [std. value]:

BAKE

bake ramp [50 min] =

H2 flow (0.4·H2) [2000 sccm] =

Hi H2 flow (100·SICL4) [60 = 6000 sccm] =

Bake TEMPL (front) [880 °C] =

Bake TEMPC (center) [900 °C] =

Bake TEMPS (rear) [880 °C] =

Bake time [20 min] =

DEPRAMP

Ramp to deposition [20 min] =

SIH2CL2 flow [2 sccm] =

Dep TEMPL (front) [835 °C] =

Dep TEMPC (center) [850 °C] =

Dep TEMPS (rear) [835 °C] =

PREDEP (not used in std. run)

H2 flow (0.4·H2) [400 sccm] =

SIH2CL2 flow [32 sccm] =

Predep time [1 sec] =

DEPOSITION

H2 flow (0.4·H2) [400 sccm] =

SIH2CL2 flow [32 sccm] =

Deposition time =

3. PRE-EPITAXIAL CLEAN IN SINK 6

3.1 Prepare 1:2 HF in dedicated clean 400 ml beaker. Use 100 ml DI H_2O and 200 ml HF. Put beaker at bottom of sink, or else the vapor will affect the resistivity readings.
3.2 Start sink 6 DI rinse tanks 1, 2, and 3 (or 4, 5, and 6). Keep tanks rinsing for the duration of the clean. Wet wafers in tank 1 and then put in piranha for 10 min.
3.3 Rinse in tanks 1 and 2 for at least 2 min each with some shaking.
3.4 Rinse in tank 3 until resistivity within 1 Mohm of empty tank.
3.5 Use 10:1 HF to dip to bead in areas with sacrificial oxide + 20 sec. overetch.
3.6 Rinse in tanks 1 and 2 for 30 sec each to remove HF from wafers.
3.7 Put wafers in piranha (refreshed) for 5 min.
3.8 Rinse in tanks 1 and 2 for at least 2 min each with some shaking.
3.9 Rinse in tank 3 until resistivity within 1 Mohm of empty tank.
3.10 Spin dry.
3.11 Bring up 2:1 HF beaker onto deck of sink. Use vacuum wand to hold each wafer over the beaker for 5 sec. Hold the wafers in contact with the beaker rim.
3.12 Put wafers in box dedicated to transfer of wafers from sink 6 to the TYLAN's. Proceed directly to NEXT STEP.

- Date and time started:

- Which Piranha and rinse tanks used:

- Rinse tank resistivity:

- Resistivity each wafer batch, rinse 1:

- Time in 10:1 HF each wafer batch:

- Resistivity each wafer batch, rinse 2:

4. LOADING WAFERS INTO TYLAN 10

4.1 ACKNOWLEDGE TYLAN 10 to step 15 (15 sec wait) and wait while the system vents in step 20 (7.5 min). Be ready to quickly load the wafers when the system opens automatically in step 25.

4.2 When the system OPENS in step 25 inspect the o-ring for any flakes. If any, they can be removed by nudging with the vacuum wand before the first baffles appear.

4.3 Important to MINIMIZE the time the system is vented and open to the atmosphere, maximum time is 10 min, but the shorter the better. Unloaded wafers they can be quickly removed by putting them on the quartz carrier mounted on the back of the loading station.

4.4 When wafers in position, ACKNOWLEDGE to step 30 (load). Will proceed to pumpdown for 40 sec. Look for the system not reaching less than 1000 mtorr within the time limit; the system will go to a vent step and not proceed if that happens since something seriously wrong. If ok, the system proceeds to step 50 (N_2 = 500, 10 min).

- Load time (displayed on ROP panel):

5. EPITAXIAL GROWTH CYCLE

5.1 The LEAKCHECK needs to be monitored at the end of the N_2 purge. Use readout at the back to record the base pressure after 30 second pump (normal 60-80 mtorr) and the rise with 30 second of no pump (normal rise 3-6 mtorr, depending on when last run was made).

5.2 Check that SICL4 (hi flow H_2) comes on as the bake ramp begins. It is interlocked with the N_2 exhaust dilution, and will not turn on if the dilution is not on.

5.3 Write down SYSTEM STATUS at least at the end of the bake and the beginning of deposition.

- Base pressure:

- Pressure after 30 sec:

- System status:

END OF RAMP TO BAKE (STEP 70)

Elapsed time:

	Internal temp.	TYCOM temp.	Power
L (front)			
C (center)			
S (rear)			

H2 =

Pressure =

SICL4 (Hi flow H_2) =

END OF BAKE (STEP 75)

Elapsed time:

	Internal temp.	TYCOM temp.	Power
L (front)			
C (center)			
S (rear)			

H2 =

Pressure =

SICL4 (Hi flow H_2) =

END OF RAMP TO DEP (STEP 80)

Elapsed time:

	Internal temp.	TYCOM temp.	Power
L (front)			
C (center)			
S (rear)			

SIH2CL2 =

H2 =

Pressure =

SICL4 (Hi flow H_2) =

BEGINING OF DEP (STEP 105)

Elapsed time:

	Internal temp.	TYCOM temp.	Power
L (front)			
C (center)			
S (rear)			

SIH2CL2 =

H2 =

Pressure =

DURING DEP (STEP 105)

Elapsed time:

	Internal temp.	TYCOM temp.	Power
L (front)			
C (center)			
S (rear)			

SIH2CL2 =

H2 =

Pressure =

DURING DEP (STEP 105)

Elapsed time:

	Internal temp.	TYCOM temp.	Power
L (front)			
C (center)			
S (rear)			

SIH2CL2 =

H2 =

Pressure =

6. UNLOADING OF WAFERS

6.1 After step 110 (H_2 = 1000, 1 hr) the HYDROGEN to the purifier and can be SHUT OFF. Remember to also shut off bottle and check its pressure. If less than 500 psi a new bottle is needed before the next run. See details in documentation.

6.2 Wafers ready to unload any time after 15 min in step 115 (N_2 = 500, loading temp.). The furnace will remain in this step until acknowledged to step 10 or aborted.

6.3 Loop back to step 10 by using the ACKNOWLEDGE button. Hit ACKNOWLEDGE to move to step 15 (15 sec wait) and wait while the system vents in step 20 (7.5 min). Be ready to quickly unload the wafers when the system opens automatically in step 25. As during the load, it is important to MINIMIZE the open time.

6.4 Once wafers unloaded, use ACKNOWLEDGE button to close system and pump it down. Once step 50 is reached use HOLD button to stop the system from proceeding through the growth cycle again.

6.5 ABORT growth recipe. LOAD and RUN the EPISTNBY recipe.

- Hydrogen pressure:

- Unload time (displayed on ROP panel):

- Date and time finished:

A.6

Modified EECS 143 Process Flow

MODIFIED EECS 143 PROCESS

Version 1.0

(CG 5/29/90)

1. STARTING MATERIAL AND SPLITS

a. Run consists of 24 wafers of 100 mm diameter <100> silicon, resistivity 15-30 ohm-cm, p-type, prime quality.

b. To the 16 wafers prepared by Galewski add 8 more prime blanks for Partlo's experiments. Retain a few clean primes for monitors (makes cleaning steps easier). There will be 3 splits of 8 wafers each scribed as follows:

(1) CG16-9 through CG16-16 : 1.2-1.4 μm undoped epi

(2) CG16-16 through CG16-24 : 6 no epi controls, 2 evaporation metallized

(3) BP1-1 through BP1-8 : deep UV irradiated at masking steps by Partlo

2. SACRIFICIAL OXIDE GROWTH

a. Standard clean in sink 6. Piranha 10 min, 3 tank rinse, dewet in 10:1 HF, 3 tank rinse. NOTE: Make sure backside of wafers also dewet each time. Sometimes takes a little longer. NOTE: When rinsing spend a minimum of 2 minutes each in two first tanks before using the resistivity tank.

Resistivity 1st cassette, 1st rinse =

Resistivity 2nd cassette, 1st rinse =

Resistivity 1st cassette, 2nd rinse =

Resistivity 2nd cassette, 2nd rinse =

b. Use TYLAN 1 or 2 to grow sacrificial oxide, 950°C dry O_2 for 30 min. Standard recipe with 20 min N_2 anneal. Include monitor from a clean box (use extras from box where Partlo's wafers came from).

Recipe =

Tube =

Condition = dry O_2 at 950°C

Time = 30 min

Target = 200 Å

Measured (monitor) =

3. BLANKET IMPLANT

a. Send wafers out for blanket implant. Include an n-type monitor wafer to check dose.

Species = Boron

Energy = 60 keV

Dose = $3 \cdot 10^{12}$ cm^{-2}

Angle = 7°

Target sheet resistance (SUPREM) =

Resistance 4 point probe (monitor) =

4. FIELD OXIDATION AND IMPLANT DRIVE-IN

a. Do a TCA clean overnight on the tube to be used for the field oxidation.

b. Clean in sink 8. Piranha 10 min, 3 tank rinse.

Resistivity 1st cassette =

Resistivity 2nd cassette =

c. Standard clean in sink 6. Piranha 10 min, 3 tank rinse, dewet in 10:1 HF, 3 tank rinse.

Resistivity 1st cassette, 1st rinse =

Time to dewet 1st cassette (1-2 min?) =

Resistivity 2nd cassette, 1st rinse =

Time to dewet 1st cassette (1-2 min?) =

Resistivity 1st cassette, 2nd rinse =

Resistivity 2nd cassette, 2nd rinse =

d. Use TYLAN 1 or 2 do to a dry-wet-dry oxidation of the wafers at 1050°C. Standard recipe with 20 min N_2 anneal. Include **8 monitors**. One for oxide thickness measurement, the others can be used for photomasking and etching dummies later

on.

Recipe =

Tube =

Condition = dry O_2 1050°C

Time = 5 min

Condition = wet O_2 1050°C

Time = 70 min

Condition = dry O_2 1050°C

Time = 5 min

Target = 5200Å

Measured (monitor) =

5. ACTIVE AREA PHOTOLITHOGRAPHY

a. Spin positive resist appropriate for the KASPER. Use EATON and normal thickness KTI 820 resist. Do dehydration bake (120°C, >2 hrs.) unless fresh from oxidation, and HMDS. Include an oxidized **monitor** to try out photolithography and etching.

b. Partlo will deep UV irradiate wafers for his experiment.

Wafer(s) irradiated =

c. Use 143 ACTV mask to expose center of each wafer with KASPER. First try the oxidized monitor and develop it to make sure works ok.

d. Resist develop. Use MTI standard positive develop.

e. Resist descum in Technics-C.

f. Post bake 120°C for 30 min.

6. ACTIVE AREA OXIDE ETCH

a. Etch oxide in active areas using sink8. First wet wafers with water and then use 5:1 BHF to etch oxide until backs of wafers dewet. Rinse for 2 minutes each in two tanks and spin dry. Use the **monitor** first to get a feeling for time, 5:1 BHF etches

about 1000 Å/min. Then etch the two full cassettes.

Etch time monitor =

Etch time 1st cassette =

Etch time 2nd cassette =

b. Strip resist with acetone in MTI.

c. Standard clean in sink 8. Piranha 10 min, 3 tank rinse.

Resistivity 1st cassette =

Resistivity 2nd cassette =

7. GATE OXIDATION

a. Do a TCA clean overnight in tube to be used for gate oxidation.

b. Standard clean in sink 6. Piranha 10 min, 3 tank rinse, dewet in 10:1 HF, 3 tank rinse.

Resistivity 1st cassette, 1st rinse =

Resistivity 2nd cassette, 1st rinse =

Resistivity 1st cassette, 2nd rinse =

Resistivity 2nd cassette, 2nd rinse =

c. Use TYLAN 5 or 6 to grow gate oxide at 1000°C dry O_2. Standard recipe with 20 min anneal in N_2. Include a **2 monitors.** One to measure the oxide thickness, the other to include in the polysilicon deposition to practice photolithography and poly etching with.

Recipe =

Tube =

Condition = dry O_2 at 1000°C

Time = 55 min

Target = 500 Å

Measured (monitor) =

8. POLYSILICON DEPOSITION

a. Transfer directly from gate oxidation in previous step to TYLAN 11 for doped polysilicon deposition. Run standard doped polysilicon recipe at 650°C. Include a 1000 Å oxide monitor for thickness measurement, and the extra gate oxide monitor for photolithography practice.

Recipe =

Time =

Target = 3500 Å

Measured thickness (monitor) =

Sheet resistance without anneal = 300 Ω/sq

Measured sheet resistance =

9. GATE PHOTOLITHOGRAPHY

a. Spin positive resist appropriate for the KASPER. Use EATON and normal thickness KTI 820 resist. Do dehydration bake (120°C, >2 hrs.) unless fresh from polysilicon deposition, and HMDS. Include the gate oxide and poly monitor to try out photolithography and etching.

b. Partlo will deep UV irradiate wafers for his experiment.

Wafer(s) irradiated =

c. Use 143 POLY mask to expose center of each wafer with KASPER. First try the oxidized monitor and develop it to make sure works ok.

d. Resist develop. Use MTI standard positive develop.

e. Resist descum in Technics-C.

f. Post bake 120°C for 30 min.

10. POLY GATE ETCH

a. Plasma etch poly in LAM1. Use 80% endpoint trigger (delay 25 sec, monitor 5 sec) and 10 sec overetch to make sure that all of the silicon is removed. Use the photolithography monitor first to get a feeling for time and if etcher working right.

Recipe =

Etch time(s) =

11. SOURCE/DRAIN OXIDE ETCH

a. **Be careful in this step not to overetch.** Etch oxide in source/drain areas using sink8. First wet wafers with water and then use 10:1 BHF to etch oxide until backs of wafers just dewet, and the active areas dewet. Rinse vigorously for 2 minutes each in two tanks and spin dry. Use the **monitor** first to get a feeling for time, 10:1 BHF etches about 500 Å/min so should not be longer than 1 minute. Then etch the two full cassettes.

Etch time monitor =

Etch time 1st cassette =

Etch time 2nd cassette =

b. Strip resist with acetone in MTI.

12. SACRIFICIAL OXIDE GROWTH

a. Standard clean in sink 8. Piranha 10 min, 3 tank rinse.

Resistivity 1st cassette =

Resistivity 2nd cassette =

b. Standard clean in sink 6. Piranha 10 min, 3 tank rinse, dewet in 10:1 HF, 3 tank rinse.

Resistivity 1st cassette, 1st rinse =

Resistivity 2nd cassette, 1st rinse =

Resistivity 1st cassette, 2nd rinse =

Resistivity 2nd cassette, 2nd rinse =

c. Use TYLAN 1 or 2 to grow a thin sacrificial oxide at 950°C. Include a bare **monitor.**

Tube =

Recipe =

Conditions = dry O_2 at 950°C

Time = 15 min

Target = 100 Å

Measured thickness (monitor) =

13. SOURCE/DRAIN IMPLANT

a. Send wafers out for active area implant. Include an p-type monitor wafer to check dose.

Species = Arsenic

Energy = 110 keV

Dose = $3 \cdot 10^{15}$ cm^{-2}

Angle = 0°

Target sheet resistance (SUPREM) =

Resistance 4 point probe (monitor) =

14. IMPLANT DRIVE-IN AND ACTIVATION

a. Clean in sink 8. Piranha 10 min, 3 tank rinse.

Resistivity 1st cassette =

Resistivity 2nd cassette =

b. Standard clean in sink 6. Piranha 10 min, 3 tank rinse, dewet in 10:1 HF, 3 tank rinse.

Resistivity 1st cassette, 1st rinse =

Time to dewet 1st cassette =

Resistivity 2nd cassette, 1st rinse =

Time to dewet 2nd cassette =

Resistivity 1st cassette, 2nd rinse =

Resistivity 2nd cassette, 2nd rinse =

c. Use TYLAN 1 or 2 to for 30 min dry O_2 drive-in at 950°C. Include a **monitor**.

Recipe =

Condition = dry O_2 at 950°C

Time = 30 min

Target = 200 Å

Measured (monitor) =

15. CONTACT PHOTOLITHOGRAPHY

a. Spin positive resist appropriate for the KASPER. Use EATON to spin on normal thickness KTI 820 resist. Do dehydration bake and HMDS if not fresh from oxidation. Do dehydration bake (120°C, >2 hrs.) unless fresh from drive-in, and HMDS. Include an oxidized **monitor** to try out photolithography and etching.

b. Partlo will deep UV irradiate wafers for his experiment.

Wafer(s) irradiated =

c. Use 143 CONT mask to expose center of each wafer with KASPER. First try the oxidized monitor and develop it to make sure works ok.

d. Resist develop. Use MTI standard positive develop.

e. Resist descum in Technics-C.

f. Post bake 120°C for 30 min.

16. CONTACT ETCH

a. Etch oxide in contacts using sink8. First wet wafers with water and then use 10:1 BHF to etch oxide until backs of wafers dewet. Rinse for 2 minutes each in two tanks and spin dry. Use the **monitor** first to get a feeling for time, 10:1 BHF etches about 500Å/min. Should not need much more than 1 minute. Make sure oxide removed in all contacts both to poly and active area. Then etch the two full cassettes.

Etch time monitor =

Etch time 1st cassette =

Etch time 2nd cassette =

b. Strip resist with acetone in MTI.

c. Standard clean in sink 8. Piranha 10 min, 3 tank rinse.

Resistivity 1st cassette =

Resistivity 2nd cassette =

17. METALIZATION (splits!)

(1) CG16-9 through CG16-22

a. Do this clean just before Aluminum deposition. Standard clean in sink 6. Piranha 10 min, 3 tank rinse, dewet in 10:1 HF, 3 tank rinse. Dewet my be hard to observe on the fronts, so make sure back is dewet at this step.

Resistivity 1st cassette, 1st rinse =

Resistivity 2nd cassette, 1st rinse =

Resistivity 1st cassette, 2nd rinse =

Resistivity 2nd cassette, 2nd rinse =

b. Put on a standard thickness of Al-Si in CPA. Include an oxidized **monitor** to check photolithography and etching in following steps.

Wafers with Al-Si =

(2) CG16-23 through CG16-24 & BP1-1 through BP1-8

a. Do this clean just before Aluminum deposition. Standard clean in sink 6. Piranha 10 min, 3 tank rinse, dewet in 10:1 HF, 3 tank rinse. Dewet my be hard to observe on the fronts, so make sure back is dewet at this step.

Resistivity 1st cassette, 1st rinse =

Resistivity 2nd cassette, 1st rinse =

Resistivity 1st cassette, 2nd rinse =

Resistivity 2nd cassette, 2nd rinse =

b. Use VEECO evaporator to deposit aluminum.

Wafers with evaporated Al =

Deposition parameters =

18. METAL PHOTOLITHOGRAPHY

a. Spin positive resist appropriate for the KASPER. Use EATON to spin on normal thickness KTI 820 resist. Do dehydration bake and HMDS if not fresh from oxidation. Do dehydration bake 120°C, >2 hrs. No HMDS. Include the metalized monitor to try out photolithography and etching.

b. Partlo will deep UV irradiate wafers for his experiment.

Wafer(s) irradiated =

c. Use 143 METL mask to expose center of each wafer with KASPER. First try the monitor and develop it to make sure works ok.

d. Resist develop. Use MTI standard positive develop.

e. Resist descum in Technics-C.

19. METAL ETCH

a. Etch metal in sink 8 aluminum etch bath. Wet wafers in rinse tank before immersing into aluminum etch. Move cassette vigorously to enhance mixing during etch. Visual end point, areas where metal removed turn dark. Take about 45 seconds to remove 5000 Å aluminum. Rinse vigorously for 5 sec in first tank, and then move to next tank for more vigorous rinsing. The aluminum etch is very viscous and difficult to remove, make sure completely off by observing sheathing of water before going on. Immerse in silicon etch for 5 seconds to remove residue. Rinse 2 tanks and spin dry. Use monitor first to make sure etch is ok and get a feeling for etch time.

How etched =

Etch time =

20. STRIP RESIST AND SINTER (splits!)

a. Strip resist with acetone in MTI.

b. No Piranha. Rinse in sink 8 DI for 20 min to remove acetone. Spin dry.

c. Measure aluminum thickness on monitors with AS-200.

Target thickness = 5000 Å

CPA aluminum thickness =

Evaporated aluminum thickness =

FOR CG16-9 through CG16-23 & BP1-1,3,5,7 ONLY

d. Standard forming gas anneal in TYLAN 13 for 30 min.

Recipe =

Condition = forming gas at 400°C

Time = 30 min

21. REMOVE BACKSIDE OXIDES

a. Use EATON to spin on double thick KTI 820 resist.

b. Post bake the resist for 1 hr at 120°C. Want to make sure resist stays on.

c. In sink 8 wet the wafers and dewet backside in 5:1 BHF. Rinse 2 tanks.

d. Directly immerse in silicon etch tank to remove poly from backside. Visual end point. Rinse 2 tanks.

e. Back into 5:1 BHF to remove gate oxide. Dip until backside dewets. Rinse 2 tanks and spin dry.

f. Strip resist using MICROSTRIP. Try max. power 275 W for 30 min first and check if resist has been removed. Repeat for a shorter time if not all removed. (Can use Technics-C also, less time and effort to use MICROSTRIP.)

DONE!

A.7

SUPREM Input for Modified EECS 143 Process

Gate Region

```
1... title  Gate Region - Epi - Modified 143 Process- 1000 gate ox, As S/D
2... $
3... comment  initialize the silicon substrate
4... initialize  silicon <100>
 ... +          boron concentration = 5e14
 ... +          thickness = 1.6  dx = 0.02  xdx = 0.02  spaces = 200
5... $
6... comment  epi growth (bake 1000C, dep 850C)
7... deposit  silicon <100>
 ... +        phosphorus concentration = 1e15
 ... +        thickness = 1.4
8... $
9... comment  sacrificial oxidation
10... diffusion  temp = 950  time = 10  nitrogen
11... diffusion  temp = 950  time = 30  dryo2
12... diffusion  temp = 950  time = 20  nitrogen
13... $
14... comment  combined field and threshold implant
15... implant  boron  dose = 3e12  energy = 60
16... print  layers
17... plot  lpplot active net
18... $
19... comment  strip sacrificial oxide
20... etch  oxide
21... $
22... comment  field oxidation
23... diffusion  temp = 1050  time = 10  nitrogen
24... diffusion  temp = 1050  time = 5   dryo2
25... diffusion  temp = 1050  time = 70  weto2
26... diffusion  temp = 1050  time = 5   dryo2
27... diffusion  temp = 1050  time = 20  nitrogen
28... plot  lpplot active net
29... $
30... comment  active area definition
31... etch  oxide
32... $
33... comment  gate oxidation  <-- try also 950
34... diffusion  temp = 1000  time = 10  nitrogen
35... diffusion  temp = 1000  time = 55  dryo2
36... diffusion  temp = 1000  time = 20  nitrogen
37... plot  lpplot active net
```

```
38... $
39... comment  poly gate deposition
40... deposit  polysilicon  temperature = 650  pressure = 4e-4
 ... +        phosphorus concentration = 1e20
 ... +        thickness = 0.35
41... $
42... comment  sacrificial oxide growth
43... diffusion  temp = 950  time = 10  nitrogen
44... diffusion  temp = 950  time = 15  dryo2
45... diffusion  temp = 950  time = 20  nitrogen
46... $
47... comment  source/drain implant  <-- try also phosphorus
48... implant  arsenic  dose = 3e15  energy = 110
49... print  layers
50... plot  lpplot active net
51... $
52... comment strip sacrificial oxide
53... etch oxide
54... $
55... comment  implant activation and reox
56... diffusion  temp = 950  time = 10  nitrogen
57... diffusion  temp = 950  time = 30  dryo2
58... diffusion  temp = 950  time = 20  nitrogen
59... $
60... print  layers
61... print  concentration active net
62... print  concentration active phosphorus
63... print  concentration active arsenic
64... print  concentration active boron
65... $
66... plot  lpplot active net
67... plot  lpplot active phosphorus
68... plot  lpplot active arsenic
69... plot  lpplot active boron
70... $
71... stop
```

Source/Drain Region

```
1... title  Source/Drain Region - Epi - Modified 143 Process - 1000 gate ox, As S/D
2... $
3... comment  initialize the silicon substrate
4... initialize  silicon <100>
 ... +           boron concentration = 5e14
 ... +           thickness = 1.6  dx = 0.02  xdx = 0.02  spaces = 200
5... $
6... comment  epi growth (bake 1000C, dep 850C)
7... deposit  silicon <100>
 ... +        phosphorus concentration = 1e15
 ... +        thickness = 1.4
8... $
9... comment  sacrificial oxidation
10... diffusion  temp = 950  time = 10  nitrogen
11... diffusion  temp = 950  time = 30  dryo2
12... diffusion  temp = 950  time = 20  nitrogen
13... $
14... comment  combined field and threshold implant
15... implant  boron  dose = 3e12  energy = 60
16... print  layers
17... plot  lpplot active net
18... $
19... comment  strip sacrificial oxide
20... etch  oxide
21... $
22... comment  field oxidation
23... diffusion  temp = 1050  time = 10  nitrogen
24... diffusion  temp = 1050  time = 5   dryo2
25... diffusion  temp = 1050  time = 70  weto2
26... diffusion  temp = 1050  time = 5   dryo2
27... diffusion  temp = 1050  time = 20  nitrogen
28... plot  lpplot active net
29... $
30... comment  active area definition
31... etch  oxide
32... $
33... comment  gate oxidation  <-- try also 950
34... diffusion  temp = 1000  time = 10  nitrogen
35... diffusion  temp = 1000  time = 55  dryo2
36... diffusion  temp = 1000  time = 20  nitrogen
37... plot  lpplot active net
```

```
38... $
39... comment  poly gate deposition
40... deposit  polysilicon  temperature = 650  pressure = 4e-4
  ... +        phosphorus concentration = 1e20
  ... +        thickness = 0.35
41... $
42... comment  gate definition and source/drain dip
43... etch  poly
44... etch  oxide
45... $
46... comment  sacrificial oxide growth
47... diffusion  temp = 950  time = 10  nitrogen
48... diffusion  temp = 950  time = 15  dryo2
49... diffusion  temp = 950  time = 20  nitrogen
50... $
51... comment  source/drain implant  <-- try also phosphorus
52... implant  arsenic  dose = 3e15  energy = 110
53... print  layers
54... plot  lpplot active net
55... $
56... comment strip sacrificial oxide
57... etch oxide
58... $
59... comment  implant activation and reox
60... diffusion  temp = 950  time = 10  nitrogen
61... diffusion  temp = 950  time = 30  dryo2
62... diffusion  temp = 950  time = 20  nitrogen
63... $
64... print  layers
65... print  concentration active net
66... print  concentration active phosphorus
67... print  concentration active arsenic
68... print  concentration active boron
69... $
70... plot  lpplot active net
71... plot  lpplot active phosphorus
72... plot  lpplot active arsenic
73... plot  lpplot active boron
74... $
75... stop
```