PERFORMANCE LIMITATIONS ON HIGH-RESOLUTION VIDEO-RATE ANALOG-DIGITAL INTERFACES

by

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

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Ph.D.   Yuh-Min Lin   Department of EECS

[signature]

Chairman of Committee

ABSTRACT

The increasing popularity of digital image processing together with better performance of modern imaging devices puts a stringent requirement on the video-rate analog-digital(A/D) interface. Modern CCD imaging devices can easily achieve more than 12 bit dynamic range, which is essential for complex image processing algorithms to maintain a reasonable SNR after processing. These developments make high-performance video-rate A/D interfaces a critical component in modern image processing systems. The objectives of this research are twofold: (i) to examine the theoretical limits on such an A/D interface and (ii) to arrive at solutions in order to implement a high-performance video-rate A/D converter in scaled CMOS technology.

Based on our study, the pipelined architecture with self-calibration capabilities has been shown to be an effective solution. This architecture combined with a differential input sample-and-hold(S/H) can effectively maintain the distortion at a sufficiently low level even when clocked at video rates. To show the feasibility of this scheme, a 13 bits 2.5M sample/sec A/D interface occupying 25 mm^2 of die area in 3 μm CMOS was designed and fabricated. A fully differential architecture is used; only a 2-phase, non-overlapping clock is required. It consumes 100 mW and has an input capacitance of 4 pF. A 1 μm CMOS version is expected to achieve video speed (~15 MHz).

This thesis arrives at three main conclusions. First, pipelined architectures with self-calibration capability are of interest for high-performance video-rate CMOS A/D conversion applications because they simultaneously provide high throughput, high resolution and low hardware cost. Second, the differential S/H investigated in this work can provide low offset and low charge injection error and achieve low distortion even for high frequency input signals. Third, the main disadvantage of this scheme is the requirement of a high-performance (both high gain and high speed) operational amplifier which becomes the principal design issue.

ACKNOWLEDGEMENT

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CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

With the rapid advancement of digital computer technology, the recent trend in telecommunication and signal processing industry is to implement as much function as possible with digital implementations in order to reduce the cost and increase the reliability. But, the real world is inherently analog, so an interface between the analog signal and the digital computer becomes a critical signal path. An analog-digital interface samples the continuous-amplitude analog input and converts it to a discrete-amplitude digital representation, which can then be processed by the digital computer. A good example of these applications is a video image processing system shown in Fig. 1.1, which consists of an imaging device, an anti-aliasing filter, an analog-digital interface and a digital processing or storage unit. The image is first transformed to electrical signal by the imaging device and the out-of-band noise is removed by the anti-aliasing filter. This filtered analog waveform is then converted to digital representation by the analog-digital interface and subsequently processed or storaged digitally.
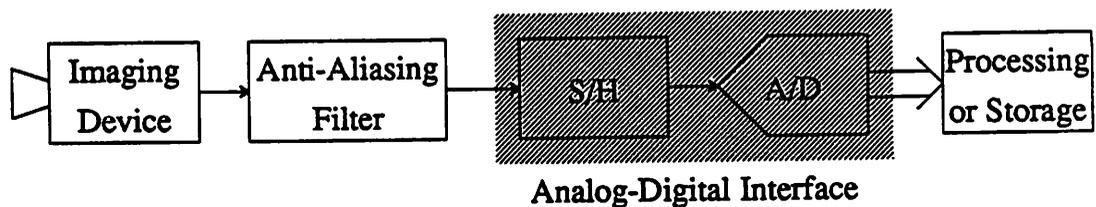
Fig. 1.1 Video Image Processing System

Conventional analog-digital interfaces for video applications have an 8-bit resolution and clocked at 14.32M sample/sec. But due to the improvements in CCD imaging devices and increasing complexities of image processing algorithms, higher resolution is preferred. A modem

CCD imaging device can have as wide as 16 bit dynamic range and exhibit excellent linearity. In addition, modern image processing algorithms tend to lose a couple of bits in dynamic range due to the accumulation of quantization errors. These trends on the imaging devices and the image algorithms demand a higher resolution interface between the imaging device and the processing unit. The objectives of this research are twofold, first, to examine the possibility of combining pipelined architectures with self-calibration techniques in CMOS as a solution for high-performance video-rate analog-digital interfaces; second, to explore various sample and hold (S/H) topologies to achieve simultaneously high speed and low distortion.

Currently, most video-rate analog-digital interfaces are implemented with flash or two-step flash architectures in Bipolar or CMOS technologies. They can achieve 8-10 bits resolution and 20M sample/sec throughput. But, to achieve higher resolution, laser trimming is needed, which is quite expensive. An alternative approach combines pipelined architectures with self-calibration techniques in CMOS technology will be described in detail in this thesis. With 1 μm CMOS technology, this approach can achieve more than 12 bit resolution at 20M sample/sec. In addition, it can surely combine with the digital processor on a single CMOS chip, thus further reduce the cost and increase the reliability.

An analog-digital interface consists of an input S/H circuit and an analog-to-digital (A/D) converter. The input S/H circuit samples the analog input, while A/D converter converts the sampled signal to digital representation. To achieve high-resolution at video speed, three problems need to be solved. First, S/H circuit must have good linearity even with high frequency input signal. Second, A/D converter must be fast enough to achieve video-rate. Third, linearities on A/D converter need to be maintained in spite of process variations.

1.2 Thesis Organization

Performance limitations on high-resolution video-rate analog-digital interfaces are presented in this thesis. Chapter 2 evaluates the performance of various S/H circuits. In particular, the effect of charge injection and switch nonlinearities are investigated in detail. Chapter 3 describes pipelined A/D converter architectures, which can achieve video-rate with reasonable power consumption and silicon area. To maintain good linearity, self-calibration techniques and

calibration algorithms are described in Chapter 4. In Chapter 5, the design of a prototype of a 13-bit 2.5M sample/sec self-calibrated pipelined A/D converter is described in detail. Some experimental results are presented in Chapter 6. Conclusions and a summary of the research results are given in Chapter 7.

CHAPTER 2

PERFORMANCE LIMITATIONS IN
MOS SAMPLE AND HOLD CIRCUIT

2.1 Introduction

An analog-digital interface consists of a sample and hold (S/H) circuit and an Analog-to-Digital (A/D) converter. The performance of the interface is only as good as the weakest of these two components. Because the interfaces for video systems usually have a resolution of 8-10 bit, the impairments of the S/H circuit can usually be neglected at this level of accuracy. Great progress has been made in implementing 8-10 bit video-rate A/D converters with reasonable power consumption and silicon area.[1,2] But as the resolution increases, the imperfections inherently associated with the S/H circuit can no longer be ignored. Care must be taken in designing a S/H circuit for high-resolution video-rate interfaces in order to fully utilize their capabilities. This chapter discusses the advantages and disadvantages of various CMOS S/H circuits. The objective is to address the needs for low-cost high-performance S/H circuit to pave the road for future development in high-speed, high-resolution analog-digital interfaces. Section 2.2 and Section 2.3 give terminology and background on CMOS S/H circuit. Section 2.4 to Section 2.7 describes four different CMOS S/H topologies. Section 2.8 summarizes the conclusions and present simulation and calculation results.

2.2 Nonidealities of the Sample and Hold Circuit

The function of a S/H is to sample the analog input at a particular instant, then hold the sampled signal for some period to allow digitizing of the sampled signal by the A/D converter. Both the sampling instant and the hold period are determined by an external hold clock. In reality, the S/H must track the input signal first before the sampling can take place. Therefore, the S/H function is actually implemented as a T/H(T/H) circuit. Figure 2.1 shows the input and

output waveform of an ideal T/H. The input is sampled at the rising edge of the hold clock, then held for the entire period of the hold clock. An ideal T/H circuit can accurately track the input waveform instantaneously and also hold the sampled signal indefinitely. In reality, the T/H circuit is implemented with a switch and a storage element. The input and output waveform of a real T/H circuit is shown in Figure 2.2. It suffers from quite a few nonidealities. These nonidealities and their effects on the performance of the T/H circuit will be discussed in the following sections.
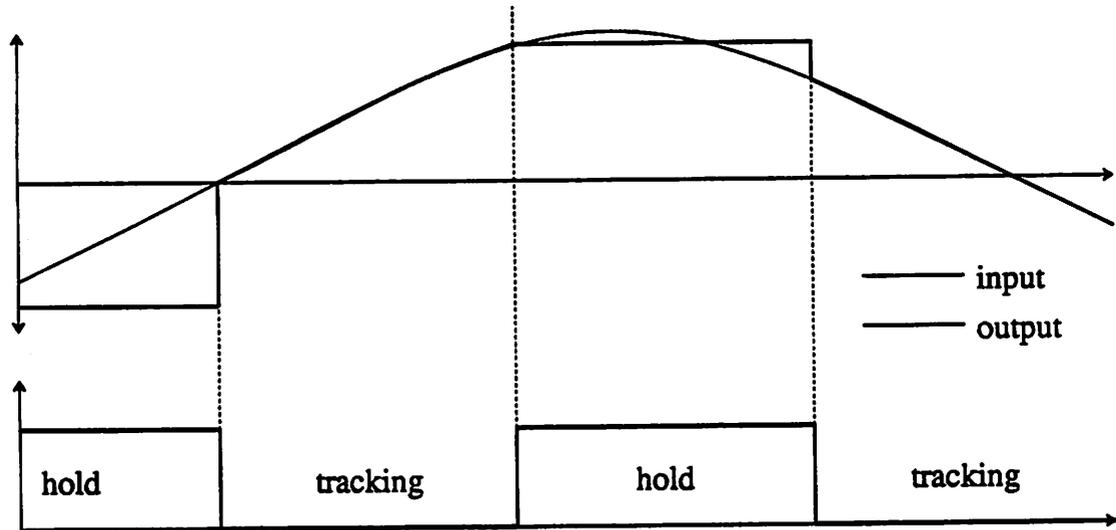
Fig. 2.1 Input and Output Waveform of an Ideal T/H Circuit

2.2.1 Acquisition Time

A real T/H circuit uses a switch that has finite resistance and hence the bandwidth of the T/H circuit is limited. The T/H output cannot change states instantaneously due to this finite bandwidth. A finite acquisition time is therefore required before the T/H circuit can track the input. This acquisition time T_{aq} is modeled as a step response of a single pole RC network.

$$e^{-\frac{T_{aq}}{\tau}} = 2^{-(b+1)} \qquad (2.1)$$

where τ is the time constant of the T/H circuit and b is the number of bits resolved. Thus, the acquisition time is expressed as:

$$T_{aq} = (b+1) \ \tau \ ln2 \qquad (2.2)$$
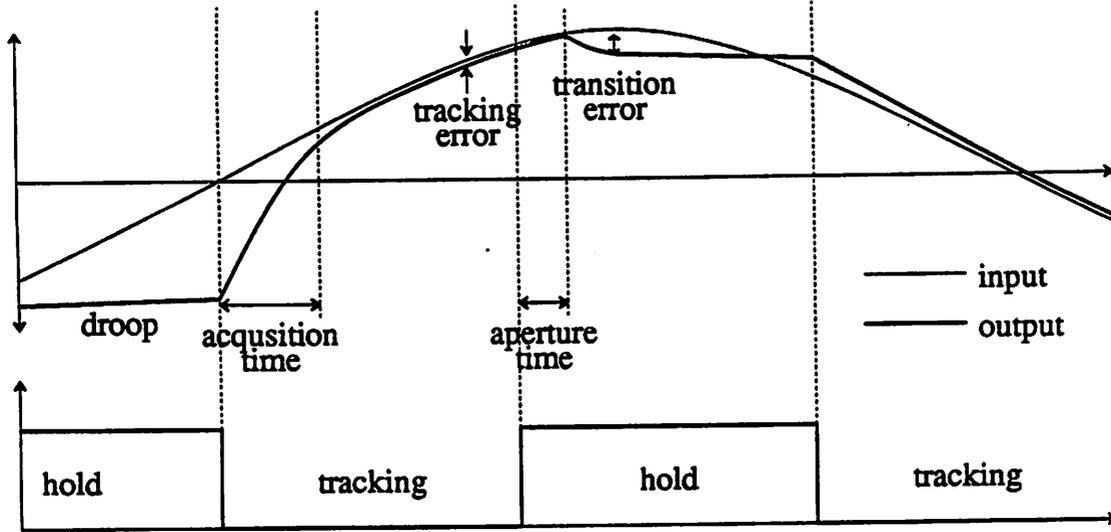
Fig. 2.2 Input and Output Waveform of a Real T/H Circuit

The acquisition time is linearly proportional to the number of bits resolved and the time constant of the T/H circuit.

2.2.2 Tracking Error

Unlike the ideal T/H circuit, the output of a real T/H circuit cannot track the input exactly. This difference between the input and the T/H output is called a tracking error. There are two components in the tracking error. The first one is due to the finite bandwidth of the T/H circuit. This component introduces amplitude attenuation and phase shift to the T/H output. Its effect is equivalent to a linear RC filter inserted in front of an ideal T/H circuit and its input-output relationship is represented as:

$$\frac{V_o(j2\pi f)}{V_i(j2\pi f)} = \frac{1}{1+j2\pi f \tau} \tag{2.3}$$

where τ is the time constant of the T/H circuit and f is the input signal frequency. Although this component is input frequency dependent, nevertheless it represents a linear filtering of the input waveform and does not introduce nonlinearity and distortion. This is not true for the second component which is due to the nonlinear nature of the switches used in the T/H circuit. This second component introduces nonlinearity and distortion to the T/H output and can be trouble-some for high-resolution applications. We will discuss how to minimize these adverse effects

with various techniques in later sections.

2.2.3 Aperture Time, Aperture Time Modulation and Aperture Jitter

At the instant of the sampling transition, a real T/H circuit cannot respond immediately, therefore there are some delays between the hold clock edge and the actual sampling action. This delay interval is called aperture time T_a. Assuming T_a is small, its corresponding error, aperture error E_a can be approximated as:

$$E_a = T_a \frac{dV_i}{dt} \tag{2.4}$$

where T_a is the aperture time and $\frac{dV_i}{dt}$ is the input slew rate. A fixed aperture time only affects the sampling phase of the input signal and is not a major concern in most applications such as waveform quantizer. On the other hand the aperture jitter, which is the random variation of the aperture time, will greatly affect the performance of the T/H circuit. The resulting T/H output with aperture jitter is modeled as phase modulation of the original input signal by the aperture jitter. This modulation results in the dispersion of the original signal and degrades the performance of the T/H circuit. The sources for the aperture jitter come from the noise inherently associated with the hold clock. Therefore, care must be taken to minimize any interaction between the hold clock and other digital clocks or noise sources. In addition, there is another imperfection which comes from the sampling switches themselves: the turn-off instant of the switches in the T/H circuit is a function of the input signal amplitude and slew rate. This aperture time modulation by the input signal introduces nonlinearity and distortion to the T/H output and becomes a major limitation on the T/H circuit. Overall, if the aperture error resulting from aperture jitter and aperture time modulation exceeds $\pm\frac{1}{2}$ LSB for maximum input slew, the T/H circuit is of limited use for signals with frequency components close to the Nyquist frequency.

2.2.4 Transition Error

At the instant of the sampling transition, the T/H circuit also suffers from the transition error introduced by the nonideal turn-off characteristics of the switch. In CMOS technology, this corresponds to the channel charge injection when a MOS switch is turned off. There are also two

components in the transition error, one is a fixed charge injection error which is independent of the input signal amplitude and slew rate and can be treated as a DC offset. This can usually be ignored or canceled out in most applications. The second component is a signal dependent charge injection error. It will contribute nonlinearity and distortion to the T/H output. Due to the difficulty in modeling the turn-off characteristics of the switch, this error proves to be the most difficult to analyze. A large portion of this chapter will address this problem and provide possible solutions.

2.2.5 Droop

Unlike the ideal T/H, a real T/H cannot hold the sampled signal indefinitely. Instead, the sampled signal suffers a droop due to the leakage of the switch and the storage element. Therefore, the A/D converter needs to digitize the sampled signal before droop becomes significant. For video applications, droop can usually be ignored in most cases without serious consequences due to the high sampling speed.

2.3 Basic Aspects of MOS S/H Performance

There are several examples in the literature describing work dealing with the problem of the MOS T/H circuit. Sheu et al.[3] use a quasi-static approach to predict the charge injection in a simple T/H circuit topology and get good agreement between the simulations and experimental results. Wilson et al.[4] do extensive measurement on the same T/H circuit topology. All this work is based on the premise of the single-ended top-plate T/H circuit topology with DC input. The topology of a single-ended top-plate T/H circuit is shown in Fig. 2.3 with a more general input signal $V_{DC}+s_i t$ instead of a DC input.

In a high-resolution video-speed A/D converter, static DC behavior is inadequate to evaluate its performance. Analysis and calculation on the dynamic behavior of the T/H circuit is of utmost important if the full potential of a video-speed A/D converter is to be explored. All the study in the literature has so far concentrated on the static DC behavior only. The performance of the T/H circuit under dynamic condition; that is, fast moving input, has not yet been study extensively. It is our intention to concentrate on a more general analysis capable of handling both the
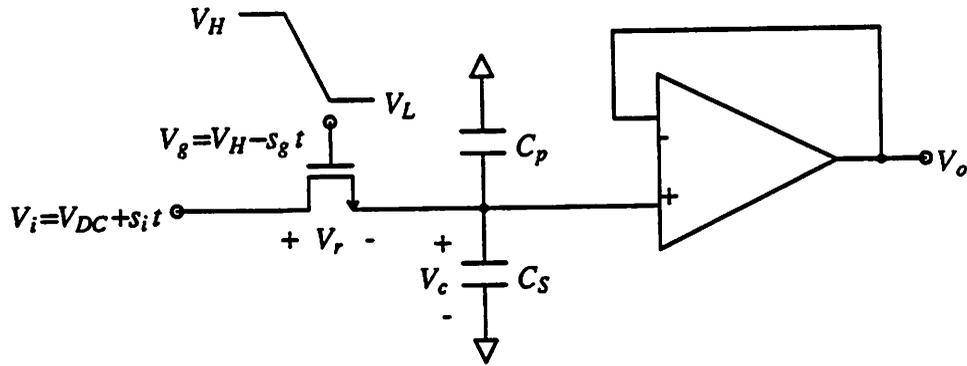
Fig. 2.3 Single-Ended Top-Plate T/H Circuit

DC and fast moving input. The simple T/H circuit topology shown in Fig. 2.3 has been the core of all study on the charge injection problems. In this chapter, other topologies of the T/H circuit will also be discussed, these include the single-ended bottom-plate T/H circuit, differential bottom-plate T/H circuit and an improved differential bottom-plate T/H circuit using single sampling switch.

Section 2.4 to Section 2.7 analyzes and discusses the operation and corresponding performance of these T/H circuits. The objective of these study is to establish general guidelines for the design of MOS T/H circuits and pave the way for future high-performance video-rate A/D converter. We start with explanation of the circuit operation with idealized components, follow by an approximate analysis. A more accurate calculation using quasi-static switch model[5] described in the next section is presented in the Appendix A-C. Finally, Section 2.8 discusses the calculations and simulation results and draw useful conclusions which form general guidelines for the design of MOS T/H circuit.

2.3.1 Quasi-Static Model for the MOS Switch

In this section, we will describe a quasi-static model proposed by Sheu[5] for the MOS switches. Fig. 2.4 shows a distributed equivalent circuit for a MOS switch biased in the linear region.

In order to simplify the analysis, we make the following two assumptions:

(1) no charge pumping to the substrate,
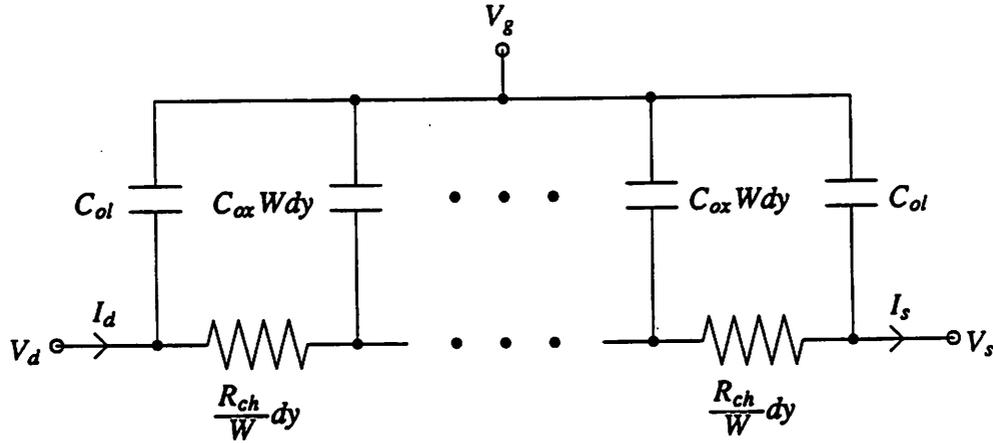
Fig. 2.4 Quasi-Static Switch Model

(2) the falling rate of the gate voltage is much larger than the potential change rate along the

conduction channel, i.e. $\dfrac{dV_g}{dt} \gg \dfrac{dV(y)}{dt}$.

For a given technology, (1) is a reasonable assumption for devices with minimum channel length. By definition (2) is the condition for quasi-static and is satisfied as long as the gate are falling fast enough.

We can write a KCL equation for an internal node as

$$dI = -C_{ox}Wdy\frac{d[V_g-V(y)]}{dt} \approx -C_{ox}\frac{dV_g}{dt}Wdy \qquad (2.5)$$

where $V(y)$ is the surface potential of the channel at position y, C_{ox} is the oxide capacitance per unit area and W is the width of the switch. Integrating Eq(2.5) from 0 to y, we obtain:

$$I(y) = I(0) - C_{ox}\frac{dV_g}{dt}Wy \qquad (2.6)$$

and from the KVL equation of an internal node, we obtain:

$$dV = \frac{R_{ch}}{W}I(y)dy$$

$$= \frac{R_{ch}}{W}[I(0) - C_{ox}\frac{dV_g}{dt}Wy]dy \qquad (2.7)$$

where R_{ch} is the resistance of the channel per unit square. Integrating Eq. (2.7) from the source

($y=0$) to the drain ($y=L$), we get the following expression for V_{ds}

$$V_{ds} = V(L) - V(0) = \frac{R_{ch}}{W} I(0)L - C_{ox} \frac{dV_g}{dt} \frac{R_{ch}}{W} \frac{L^2}{2}$$

$$= \frac{R_{ch}}{W/L} I(0) - \frac{WLC_{ox}}{2 \frac{(W/L)}{R_{ch}}} \frac{dV_g}{dt}$$

$$= \frac{I(0)}{G_{ds}} - \frac{C_g}{2G_{ds}} \frac{dV_g}{dt} \tag{2.8}$$

where $G_{ds} = \frac{W/L}{R_{ch}}$ is the conductance of the switch and $C_g = WLC_{ox}$ is the gate capacitance of the switch. Since $I_s = I(0)$, from Eq.(2.8) we have

$$I_s = G_{ds} V_{ds} + \frac{C_g}{2} \frac{dV_g}{dt} \tag{2.9}$$

Also $I_d = I(L)$, from Eq. (2.6) we have

$$I_d = I_s - C_g \frac{dV_g}{dt} = G_{ds} V_{ds} - \frac{C_g}{2} \frac{dV_g}{dt} \tag{2.10}$$

Because $\frac{dV_g}{dt} \gg \frac{dV_s}{dt}$, Eq. (2.9) and (2.10) can be approximated by

$$I_s = G_{ds} V_{ds} + \frac{C_g}{2} \frac{dV_{gs}}{dt} \tag{2.11}$$

$$I_d = G_{ds} V_{ds} - \frac{C_g}{2} \frac{dV_{gs}}{dt} \tag{2.12}$$
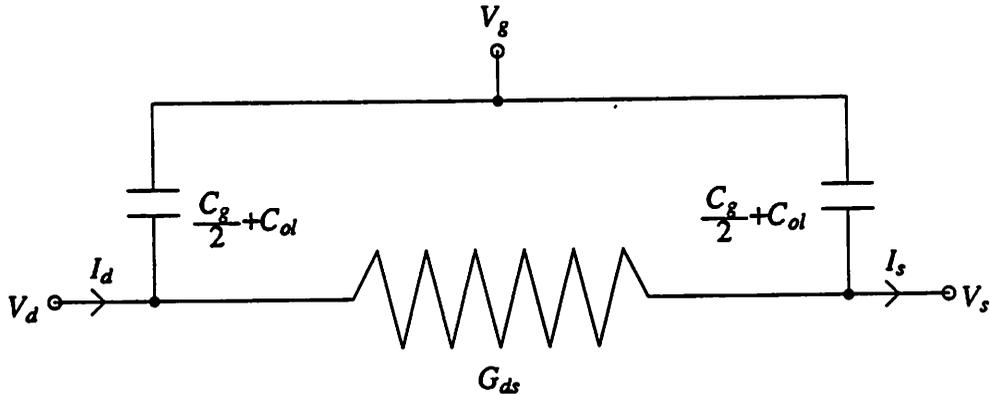
Fig. 2.5 Equivalent Circuit of a MOS Switch in Linear Region

These two equations are represented by the equivalent circuit shown in Fig. 2.5. The gate

capacitance is evenly distributed between the source and the drain nodes. This switch model will be used throughout the calculations in this chapter.

A simple model will be used for the MOS switch in the saturation region, where we assume all the channel charges $-\frac{2}{3}C_g V_{ds}$ are dumped into the source side. Fig. 2.6 shows the equivalent circuit of a MOS switch in saturation region.
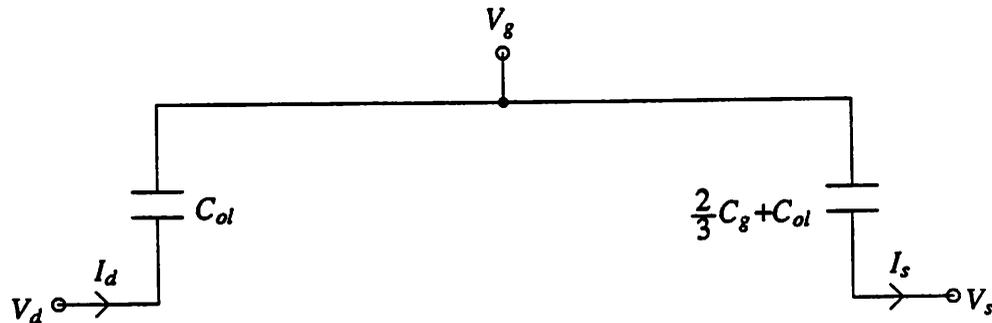
Fig. 2.6 Equivalent Circuit of a MOS Switch in Saturation Region

2.4 Single-Ended Top-Plate T/H Circuit

As shown in the previous section, Figure 2.3 shows the most usual topology of the T/H circuit implemented in MOS technology. It consists of a sampling capacitor C_S in series with a pass transistor and a voltage follower. When the switch is turned on, the voltage across the capacitor tracks the input. At the instant of sampling, the switch turns off and the input voltage is stored on the sampling capacitor C_S. A voltage follower isolates the sampled voltage from the loading of the output. Since the switch turns off when $V_g - V_s = V_T$, it can be shown that the aperture time and the sampled signal are nonlinear functions of the input signal and clock fall time. In addition, the channel charge of the pass transistor will introduce an offset to the sampled signal, this offset is also signal dependent. The following sections discuss an approximate analysis. Because this circuit has been study extensively and performs much worse than the following three T/H circuits, we will skip the detailed calculations here.

2.4.1 Approximate Analysis

A simple approximation is used to demonstrate the effect of the aperture time modulation of the single-ended top-plate T/H circuit. Assuming the input voltage is $V_{DC}+s_i t$ and the gate voltage is $V_H-s_g t$, where V_{DC} is the input DC voltage at t $=0$, s_i is the input signal slew rate and s_g is the fall rate of the gate voltage. Assume $V_{ds} \ll V_{gs}-V_T$, the conductance of the switch is

$$G = \frac{1}{R} = k\frac{W}{L}(V_H-V_{DC}-V_T) = \beta_n(V_H-V_{DC}-V_T) \tag{2.13}$$

where $\beta_n=k\frac{W}{L}$ and the time constant of the T/H circuit is

$$\tau = \frac{C_S+C_p}{G} = \frac{C_S+C_p}{\beta_n(V_H-V_{DC}-V_T)} \tag{2.14}$$

From Eq. (2.2), the acquisition time of the T/H circuit is

$$T_{aq} = (b+1)\tau ln2 = \frac{(b+1)(C_S+C_p)ln2}{\beta_n(V_H-V_{DC}-V_T)} \tag{2.15}$$

and the voltage across the switch at $t=0$ is

$$V_r(0) = \frac{s_i(C_S+C_p)}{G} = \frac{s_i(C_S+C_p)}{\beta_n(V_H-V_{DC}-V_T)} \tag{2.16}$$

where we assume the T/H circuit already reaches steady-state at $t=0$. The following assumptions are used to approximate the real T/H circuit:

(1) the T/H network already reaches steady-state when the sampling switch turns off;

(2) the channel charge injection from the switch is ignored;

(3) the switch turns off at time $t=T_a$ when it enters the saturation region, i.e. $V_g(T_a)-V_d(T_a)=V_T(T_a)$, where T_a is the aperture time;

(4) the switch conductance is G at $t=0$ and remains constant when the switch is in linear region. Once it enter the saturation region, the switch conductance becomes 0.

Under these assumptions, the sampled voltage can be calculated in the following two cases:

(A) Positive input slew rate, i.e. $s_i > 0$

Since $s_i > 0$, from Eq. (2.16), we have $V_r > 0$ and $V_d(T_a)=V_i(T_a)=V_{DC}+s_iT_a$. Therefore T_a can be calculated by the following equation

$$V_g(T_a)-V_d(T_a)-V_T = V_H-s_gT_a-(V_{DC}+s_iT_a)-V_T = 0 \tag{2.17}$$

thus

$$T_a = \frac{1}{s_g + s_i}(V_H - V_{DC} - V_T) \qquad (2.18)$$

From Eq. (2.18), the aperture time T_a is not a constant. Instead, it depends on the input signal amplitude V_{DC}, input signal slew rate s_i and gate fall rate s_g. This aperture time modulation by the input signal and clock waveform introduces nonlinearity and distortion. The output voltage can be calculated as

$$V_o(T_a) = V_c(T_a) = V_i(T_a) - V_r(T_a)$$

$$= V_{DC} + s_i T_a - V_r(0)$$

$$= V_{DC} + \frac{s_i}{s_g + s_i}(V_H - V_{DC} - V_T) - V_r(0)$$

$$= \frac{s_g}{s_g + s_i} V_{DC} + \frac{s_i}{s_g + s_i}(V_H - V_T) - \frac{s_i(C_S + C_p)}{\beta_n(V_H - V_{DC} - V_T)}$$

$$= \frac{s_g}{s_g + s_i} V_{DC} + \frac{s_i}{s_g + s_i}\left[V_H - V_{T_o} - \gamma(\sqrt{V_{DC} + 2\Phi_B} - \sqrt{2\Phi_B})\right]$$

$$- \frac{s_i(C_S + C_p)}{\beta_n}\left[V_H - V_{DC} - V_{T_o} - \gamma(\sqrt{V_{DC} + 2\Phi_B} - \sqrt{2\Phi_B})\right]^{-1} \qquad (2.19)$$

where we use the fact that $V_r(T_a) = V_r(0)$ from the assumption (4) and γ is the body effect factor and Φ_B is the magnitude of the substrate build-in voltage.

(B) Negative input slew rate, i.e. $s_i < 0$

Since $s_i < 0$, from Eq. (2.16), we have $V_r < 0$ and $V_d(T_a) = V_c(T_a) = V_i(T_a) - V_r(T_a)$ by the same argument as in $s_i > 0$ case. Therefore T_a can be calculated by the following equation

$$V_g(T_a) - V_d(T_a) - V_T = V_g(T_a) - V_i(T_a) + V_r(T_a) - V_T$$

$$= V_H - s_g T_a - (V_{DC} + s_i T_a) + V_r(0) - V_T = 0 \qquad (2.20)$$

thus

$$T_a = \frac{1}{s_g + s_i}\left[V_H - V_{DC} - V_T + V_r(0)\right] \qquad (2.21)$$

As in the $s_i > 0$ case, the aperture time T_a is not a constant. Instead, it is a function of input signal amplitude V_{DC}, input signal slew rate s_i and gate fall rate s_g. The output voltage can be expressed as

$$V_o(T_a) = V_c(T_a) = V_i(T_a) - V_r(T_a)$$

$$= V_{DC} + \frac{s_i}{s_g+s_i}\left[V_H-V_{DC}-V_T+V_r(0)\right] - V_r(0)$$

$$= \frac{s_g}{s_g+s_i}V_{DC} + \frac{s_i}{s_g+s_i}(V_H-V_T) - \frac{s_g s_i(C_S+C_p)}{(s_g+s_i)\beta_n(V_H-V_{DC}-V_T)}$$

$$= \frac{s_g}{s_g+s_i}V_{DC} + \frac{s_i}{s_g+s_i}\left[V_H-V_{T_o}-\gamma(\sqrt{V_{DC}+2\Phi_B}-\sqrt{2\Phi_B})\right]$$

$$- \frac{s_g s_i(C_S+C_p)}{(s_g+s_i)\beta_n}\left[V_H-V_{DC}-V_{T_o}-\gamma(\sqrt{V_{DC}+2\Phi_B}-\sqrt{2\Phi_B})\right]^{-1} \qquad (2.22)$$

From Eq. (2.19) and Eq. (2.22), the voltage sampled on the sampling capacitor is a nonlinear function of the input signal amplitude V_{DC}, input signal slew rate s_i and the gate fall rate s_g. Therefore, offset, gain error and nonlinearity are introduced to the output by this T/H circuit. Detailed analysis of single-ended top-plate T/H circuit is available from many sources [3,4]. We will skip the detailed analysis of this T/H topology.

2.5 Single-Ended Bottom-Plate T/H Circuit

As shown in the previous section, the output of a top-plate T/H circuit is a nonlinear function of the input signal amplitude V_{DC}, input signal slew rate s_i and gate fall rate s_g. To improve the performance of the T/H circuit, a bottom-plate topology can be used, which removes the nonlinear dependence on the input signal amplitude V_{DC} from the T/H output. Figure 2.7 shows a single-ended bottom-plate T/H circuit, which consists of a sampling capacitor C_S, an integrating capacitor C_I, sampling switch M_1, pass transistor M_2 and some other switches. To avoid the nonlinear dependence on the input signal amplitude V_{DC}, M_1 is used as a sampling switch instead of M_2 as in the top-plate case. The operation of this T/H circuit is described below.

At the beginning, both M_1 and M_2 are closed and integrating capacitor C_I is connected to ground and the voltage across the sampling capacitor tracks the input. At the end of ϕ_1, the
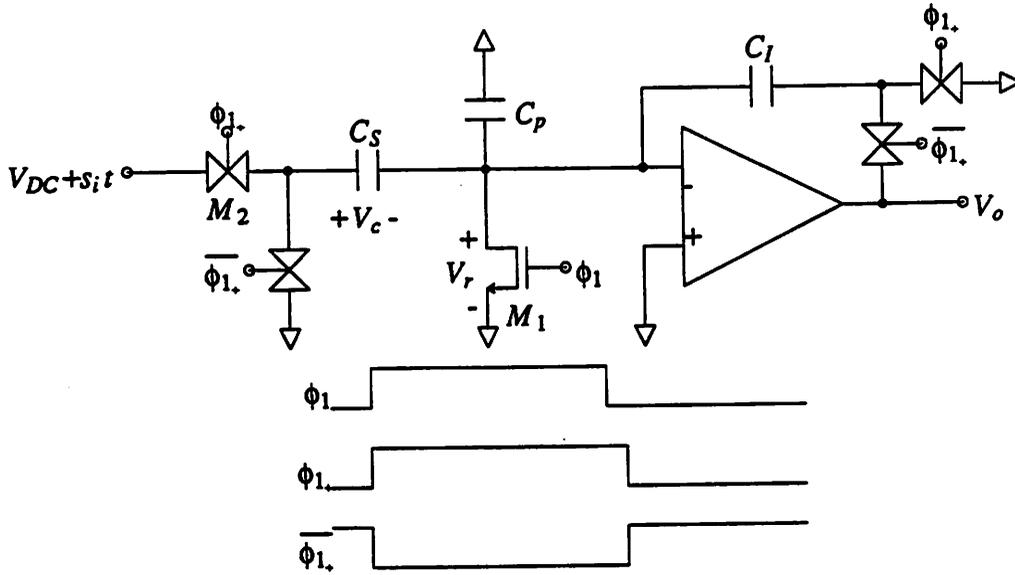
Fig. 2.7 Single-Ended Bottom-Plate T/H Circuit

sampling switch M_1 turns off. Since the sampling switch M_1 is connected to ground, there is no nonlinear dependence on the input signal amplitude V_{DC} in the charge sampled on the sampling capacitor C_S when the sampling switch turns off. Phase ϕ_{1_*}, a delayed version of ϕ_1, is then used to turn off pass transistor M_2 and close the loop. Therefore, whatever charge was sampled on the sampling node at the time M_1 turns off, is transferred to the integrating capacitor C_I. This completes the T/H operation. An approximate analysis of this T/H circuit is described in Section 2.5.1, followed by a more accurate calculation in Section 2.5.2.

2.5.1 Approximate Analysis
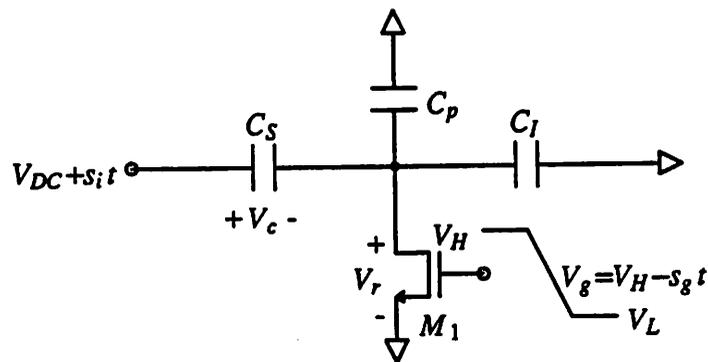
Fig. 2.8 Single-Ended Bottom-Plate T/H Equivalent Circuit

Fig. 2.8 shows an equivalent circuit of the single-ended bottom-plate T/H circuit. The pass transistor has been eliminated for ease of calculation, because once the sampling switch M_1 turns off, the sampling node is floating and charge sampled on the sampling node is fixed and will not be affected by the subsequent operation of the other switches. We can choose a large pass transistor M_2 to reduce the effect of nonlinear resistance and impedance mismatch. Thus, the pass transistor can be eliminated from the calculation without serious effects. Follow the same approach as in the top-plate case, the conductance of the switch is

$$G = \frac{1}{R} = k\frac{W}{L}(V_H - V_T) = \beta_n(V_H - V_{T_0}) = \beta_n V_{HT} \tag{2.23}$$

where $V_{HT} = V_H - V_{T_0}$ and V_{T_0} is the zero-bias threshold voltage. The time constant of the T/H circuit is

$$\tau = \frac{C_T}{G} = RC_T = \frac{C_T}{\beta_n V_{HT}} \tag{2.24}$$

where $C_T = C_S + C_I + C_p$ is the total capacitance at the sampling node. From Eq. (2.2), the acquisition time of this T/H circuit is

$$T_{aq} = (b+1)\tau \ln 2 = \frac{(b+1)C_T \ln 2}{\beta_n V_{HT}} \tag{2.25}$$

and the voltage across the switch M_1 at $t=0$ is

$$V_r(0) = \frac{s_i C_S}{G} = s_i C_S R = \frac{s_i C_S}{\beta_n V_{HT}} \tag{2.26}$$

The same assumptions are used to approximate this T/H circuit as in the top-plate case. The sampled voltage can be calculated in the following two cases:

(A)   Positive input signal slew rate, i.e. $s_i > 0$

Since $s_i > 0$, from Eq. (2.26), we have $V_r > 0$ and $V_d(T_a) = V_r(T_a)$. Because the sampling switch M_1 turns off at $t = T_a$ when it enters saturation region, where T_a is the aperture time, T_a can be calculated by the following equation

$$V_g(T_a) - V_d(T_a) - V_T = V_g(T_a) - V_r(T_a) - V_{T_0}$$

$$= V_H - s_g T_a - V_r(0) - V_{T_0} = 0 \tag{2.27}$$

thus

$$T_a = \frac{1}{s_g}\left[V_{HT}-V_r(0)\right] \tag{2.28}$$

From Eq. (2.28), the aperture time T_a is a function of the input signal slew rate s_i and gate fall rate s_g. This aperture time modulation introduces nonlinearity and distortion to the T/H output. Since the charge sampled on the sampling node at $t=T_a$ will eventually transfer to the integrating capacitor C_I, the final T/H output voltage V_o can be calculated as

$$V_o = -\frac{Q_S}{C_I}$$

$$= -\frac{1}{C_I}\left\{C_S\left[V_r(T_a) - V_i(T_a)\right] + (C_I+C_p)V_r(T_a)\right\}$$

$$= -\frac{1}{C_I}\left[C_T V_r(T_a) - C_S V_i(T_a)\right]$$

$$= -\frac{1}{C_I}\left\{C_T \frac{s_i C_S}{\beta_n V_{HT}} - C_S\left[V_{DC}+\frac{s_i}{s_g}(V_{HT}-\frac{s_i C_S}{\beta_n V_{HT}})\right]\right\}$$

$$= \frac{C_S}{C_I}\left\{V_{DC} + s_i\left[\frac{V_{HT}}{s_g} - \frac{C_T}{\beta_n V_{HT}}\right] - s_i^2\frac{C_S}{s_g\beta_n V_{HT}}\right\}$$

$$= \frac{C_S}{C_I}\left\{V_{DC} + s_i\left[\frac{V_{HT}}{s_g} - \tau\right] - s_i^2\frac{C_S}{C_T}\frac{\tau}{s_g}\right\} \tag{2.29}$$

where Q_S is the charge sampled on the sampling capacitor C_S, $C_T=C_S+C_I+C_p$ is the total capacitance at the sampling node and $\frac{V_{HT}}{s_g}$ is just the gate fall time.

(B) Negative input signal slew rate, i.e. $s_i < 0$

Since $s_i < 0$, from Eq. (2.26), we have $V_r < 0$ and $V_d = 0$. Therefore T_a can be calculated as follows

$$V_g(T_a)-V_d(T_a)-V_T = V_g(T_a)-0-V_T$$

$$= V_H-s_g T_a-\left[V_{T_o}+\chi V_r(0)\right] = 0$$

where $V_T=V_{T_o}+\gamma(\sqrt{V_r+2\Phi_B}-\sqrt{2\Phi_B})=V_{T_o}+\chi V_r$ and $\chi=\frac{\gamma}{2}(2\Phi_B)^{-\frac{1}{2}}$ thus giving

$$T_a = \frac{1}{s_g}\left[V_H - V_{T_o} - \chi V_r(0)\right] \tag{2.30}$$

From Eq. (2.30), the aperture time T_a is a function of the input signal slew rate s_i and gate fall rate s_g. This aperture time modulation introduces nonlinearity and distortion to the T/H output. Since the charge sampled on the sampling node at $t=T_a$ will eventually transfer to the integrating capacitor C_I, the final T/H output voltage V_o can be calculated as

$$
\begin{aligned}
V_o &= -\frac{Q_S}{C_I} \\
\\
&= -\frac{1}{C_I}\left\{C_S\left[V_r(T_a) - V_i(T_a)\right] + (C_I + C_p)V_r(T_a)\right\} \\
\\
&= -\frac{1}{C_I}\left[C_T V_r(T_a) - C_S V_i(T_a)\right] \\
\\
&= -\frac{1}{C_I}\left\{C_T\frac{s_i C_S}{\beta_n V_{HT}} - C_S\left[V_{DC} + \frac{s_i}{s_g}(V_{HT} - \chi\frac{s_i C_S}{\beta_n V_{HT}})\right]\right\} \\
\\
&= \frac{C_S}{C_I}\left\{V_{DC} + s_i\left[\frac{V_{HT}}{s_g} - \frac{C_T}{\beta_n V_{HT}}\right] - s_i^2\chi\frac{C_S}{s_g\beta_n V_{HT}}\right\} \\
\\
&= \frac{C_S}{C_I}\left\{V_{DC} + s_i\left[\frac{V_{HT}}{s_g} - \tau\right] - s_i^2\chi\frac{C_S}{C_T}\frac{\tau}{s_g}\right\} \tag{2.31}
\end{aligned}
$$

where $\frac{V_{HT}}{s_g}$ is the gate fall time.

Eq. (2.29) and Eq.(2.31) can be combined together and rewritten as follow

$$V_o = \frac{C_S}{C_I}\left\{V_{DC} + s_i\left[\frac{V_{HT}}{s_g} - \tau\right] - \left[s_i^2(1+\chi) + s_i|s_i|(1-\chi)\right]\frac{C_S}{C_T}\frac{\tau}{s_g}\right\} \tag{2.32}$$

From Eq. (2.32), it can be shown that the T/H output voltage no longer depends on V_{DC}, but is still a function of s_i. The factor $\frac{C_S}{C_I}$ is the gain of the T/H circuit. The T/H output include a DC term V_{DC}, a linear term $s_i\left[\frac{V_{HT}}{s_g} - \tau\right]$ and a nonlinear term $s_i^2\frac{C_S}{C_T}\frac{\tau}{s_g}$ for $s_i > 0$ or $s_i^2\chi\frac{C_S}{C_T}\frac{\tau}{s_g}$ for $s_i < 0$. The coefficient $\left[\frac{V_{HT}}{s_g} - \tau\right]$ of the s_i term represents the difference between gate fall time $\frac{V_{HT}}{s_g}$ and the RC delay τ introduced by the finite bandwidth of the T/H circuit. It does not

introduce any nonlinearity or distortion. Of particular interest is the nonlinear term, which includes two components; one is a quadratic function of input signal slew rate s_i and the other is an odd function of input signal slew rate s_i. Both introduce nonlinearity to the T/H output and is proportional to the factor $\frac{\tau}{s_g}$. Therefore, by increasing the clock fall rate s_g or decreasing the T/H circuit time constant τ, we can reduce the nonlinear dependence on the input signal slew rate s_i of the T/H output. However, this is only a simple approximation: as the gate fall rate s_g gets faster and T/H circuit time constant gets smaller, other second order effects will come into play.

2.5.2 Detailed Analysis

A more accurate calculation of the single-ended bottom-plate T/H circuit is described below. The following assumptions are used in the detailed calculation:

(1) no charge pumping to the substrate,

(2) quasi-static model of MOS switch in the linear region described in Section 2.3.1 is used throughout the calculation,

(3) the remaining channel charge when the switch enters saturation region is all dumped to the source side.

The calculation can be separated into two parts, the first part deals with the linear region of the switch, while the second part deals with the saturation region of the switch. Fig. 2.9 shows an equivalent circuit of the T/H circuit in the linear region. As in the approximate analysis, the pass transistor M_2 has been neglected to simplify the calculation. Assume the input voltage is $V_{DC}+s_i t$ and the gate voltage is $V_H-s_g t$, where V_{DC} is the input voltage at t =0, s_i is the slew rate of the input voltage and s_g is the gate fall rate.

The procedure to calculate the final T/H output voltage is described below:

(1)   write a KCL equation from Fig. 2.9 for the sampling node,

(2)   solve V_r as a function of time

(3)   calculate the voltage across the sampling switch when the switch enter saturation region, i.e. calculate $V_r(T_a)$, where T_a is the aperture time
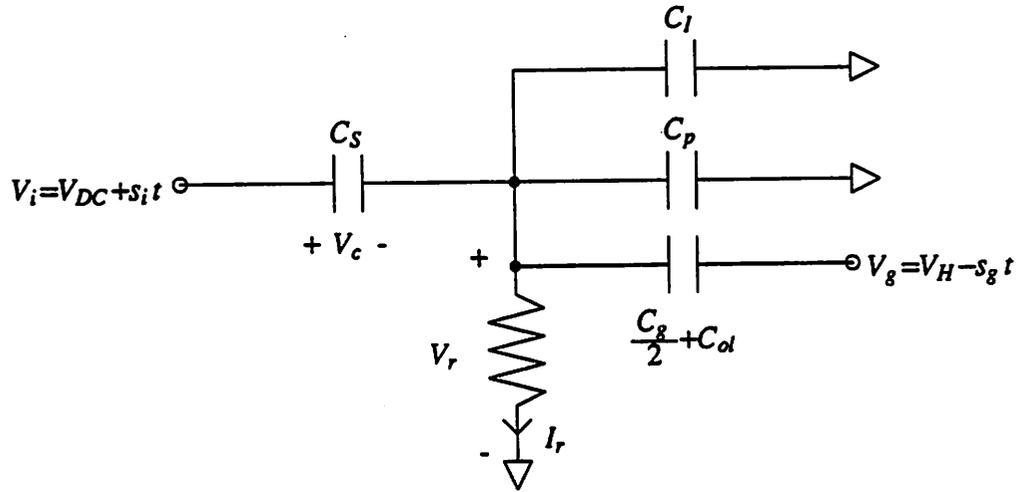
Fig. 2.9 Equivalent Circuit of a Single-Ended Bottom-Plated T/H in Linear Region

(4)   dump the remaining channel charge to the source side

(5)   calculate the final T/H output voltage using the result from (3) and (4)

To make the main body of this section more readable, the detailed calculation is described in Appendix A. The results and conclusions are described below in the following two cases:

(A) Positive input signal slew rate, i.e. $s_i > 0$

From Eq. (A.19) in Appendix A, T/H output voltage can be expressed as follow

$$V_o = V_{o_{0+}} + s_i V_{o_{1+}} + s_i^2 V_{o_{2+}} + s_i^3 V_{o_{3+}} + \cdots \tag{2.33}$$

where $V_{o_{0+}}$ is the term independent of s_i, $V_{o_{1+}}$ is the coefficient of s_i, $V_{o_{2+}}$ is the coefficient of s_i^2 and $V_{o_{3+}}$ is the coefficient of s_i^3. The subscript "+" indicates that the coefficients are for $s_i > 0$ case.

From Eq. (A.20), the DC term $V_{o_{0+}}$ can be expressed as

$$V_{o_{0+}} = \frac{C_S}{C_I}\left[V_{DC} + \frac{C_{ol}}{C_S}(V_{T_o} - V_L)\right]$$

$$+ \frac{(C_S + C_I + C_p)}{C_I}(1 + \frac{\frac{C_g}{2} + C_{ol}}{C_T})(\frac{\frac{C_g}{2} + C_{ol}}{C_T})\pi s_g \sqrt{\frac{\pi X}{2}} erf\left[\sqrt{\frac{X}{2}}\right]$$

$$= \frac{C_S}{C_I}\left[V_{DC} + V_{os}\right] \tag{2.34}$$

where V_{os} is the input-referred offset due to the charge injection. From Eq. (2.34), we have

$$V_{os} \approx \frac{C_{ol}}{C_S}(V_{T_0}-V_L) + \frac{C_T}{C_S}(1+\frac{\frac{C_g}{2}+C_{ol}}{C_T})(\frac{\frac{C_g}{2}+C_{ol}}{C_T})\tau s_g \sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right]$$

$$\approx \frac{C_{ol}}{C_S}(V_{T_0}-V_L) + \frac{C_g}{2C_S}\tau s_g \sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right] \tag{2.35}$$

From Eq. (2.35), the first term in V_{os} is due to the clock feedthrough, while the second term is proportional to $\tau s_g \frac{C_g}{C_S}$. Increasing the time constant of the T/H network or gate fall rate will increase the offset.

From Eq. (A.22), the coefficient of $s_i{}^2$ can be expressed as

$$V_{o_{2+}} \approx -\frac{C_S}{C_I}\frac{\tau}{s_g}\frac{C_S}{C_T}f_+(X) \tag{2.36}$$

where $X=\frac{V_{HT}}{\tau s_g}$ is the ratio of the gate fall time $\frac{V_{HT}}{s_g}$ to the T/H network time constant τ and $f_+(X)$ is a weak function of X. From Eq. (2.36), the coefficient $V_{o_{2+}}$ of $s_i{}^2$ is shown to be proportional to $\tau s_g \frac{C_g}{C_S}$. The quadratic nonlinear term becomes

$$s_i{}^2 V_{o_{2+}} \approx -s_i{}^2\frac{\tau}{s_g}\frac{C_S}{C_I}\frac{C_S}{C_T}f_+(X) \tag{2.37}$$

which is the same as the result obtained in Eq. (2.29) from approximate analysis except for the factor $f_+(X)$. Since this nonlinear dependence is proportional to τ and inversely proportional to s_g, by decreasing the time constant τ of the T/H network or increasing the gate fall rate s_g this distortion can be reduced.

(B) Negative input signal slew rate, i.e. $s_i < 0$

From Eq. (A.36) in Appendix A, we have

$$V_o = V_{o_{0-}} + s_i V_{o_{1-}} + s_i{}^2 V_{o_{2-}} + s_i{}^3 V_{o_{3-}} + \cdots \tag{2.38}$$

where $V_{o_{0-}}$ is the term independent of s_i, $V_{o_{1-}}$ is the coefficient of s_i, $V_{o_{2-}}$ is the coefficient of $s_i{}^2$ and $V_{o_{3-}}$ is the coefficient of $s_i{}^3$. The subscript "-" indicates that the coefficients are for $s_i < 0$ case.

From Eq. (A.39) in Appendix A, the coefficient of $s_i{}^2$ can be expressed as

$$V_{o_{2-}} \approx -\chi \frac{C_S}{C_I} \frac{\tau}{s_g} \frac{C_S}{C_T} f_-(X) \qquad (2.39)$$

where $f_-(X)$ is a weak function of X. The quadric nonlinear term becomes

$$s_i{}^2 V_{o_{2-}} \approx -s_i{}^2 \chi \frac{C_S}{C_I} \frac{\tau}{s_g} \frac{C_S}{C_T} f_-(X) \qquad (2.40)$$

which is the same as the result obtained in Eq. (2.31) from approximate analysis except for the factor $f_-(X)$. Since this nonlinear dependence is proportional to τ and inversely proportional to s_g, by increasing the sampling switch size or gate fall rate s_g this distortion can be reduced.

2.6 Differential Bottom-Plate T/H Circuit

As shown in the previous section, although the bottom-plate T/H circuit performs much better than the top-plate T/H circuit, its output is still a nonlinear function of input signal slew rate s_i and gate fall rate s_g. To further improve the performance of T/H function, a differential circuit is used instead. It will be shown in the following discussion that the differential circuit has the advantage of first order cancellation of the charge injection error. The effectiveness of this cancellation depends on the matching of the sampling capacitors, parasitic capacitors, sampling switches and sampling clock waveforms. Fig. 2.10 shows a differential bottom-plate T/H circuit. It consists of two single-ended bottom-plate T/H circuits driven by a differential input. The operation principle is the same as in the single ended case, however, the single-ended op amp is changed to a differential op amp. An approximate analysis of this T/H circuit is described in Section 2.6.1, followed by a more accurate calculation in Section 2.6.2

2.6.1 Approximate Analysis

In order to make the analysis complete, we will also include the effect of mismatch of capacitors and switches. Assume the sampling capacitors, integrating capacitors and "total" capacitors are $(1 \pm \Delta_{C_s}) C_S$, $(1 \pm \Delta_{C_I}) C_I$ and $(1 \pm \Delta_{C_T}) C_T$ respectively, and the time constants, gate fall rates, and V_{HT}'s are $(1 \pm \Delta_\tau)\tau$, $(1 \pm \Delta_{s_g})s_g$ and $(1 \pm \Delta_{v_{HT}})V_{HT}$ respectively. The differential T/H output voltage $V_{o_{diff}}$ can be calculated by using the results from the previous section since the
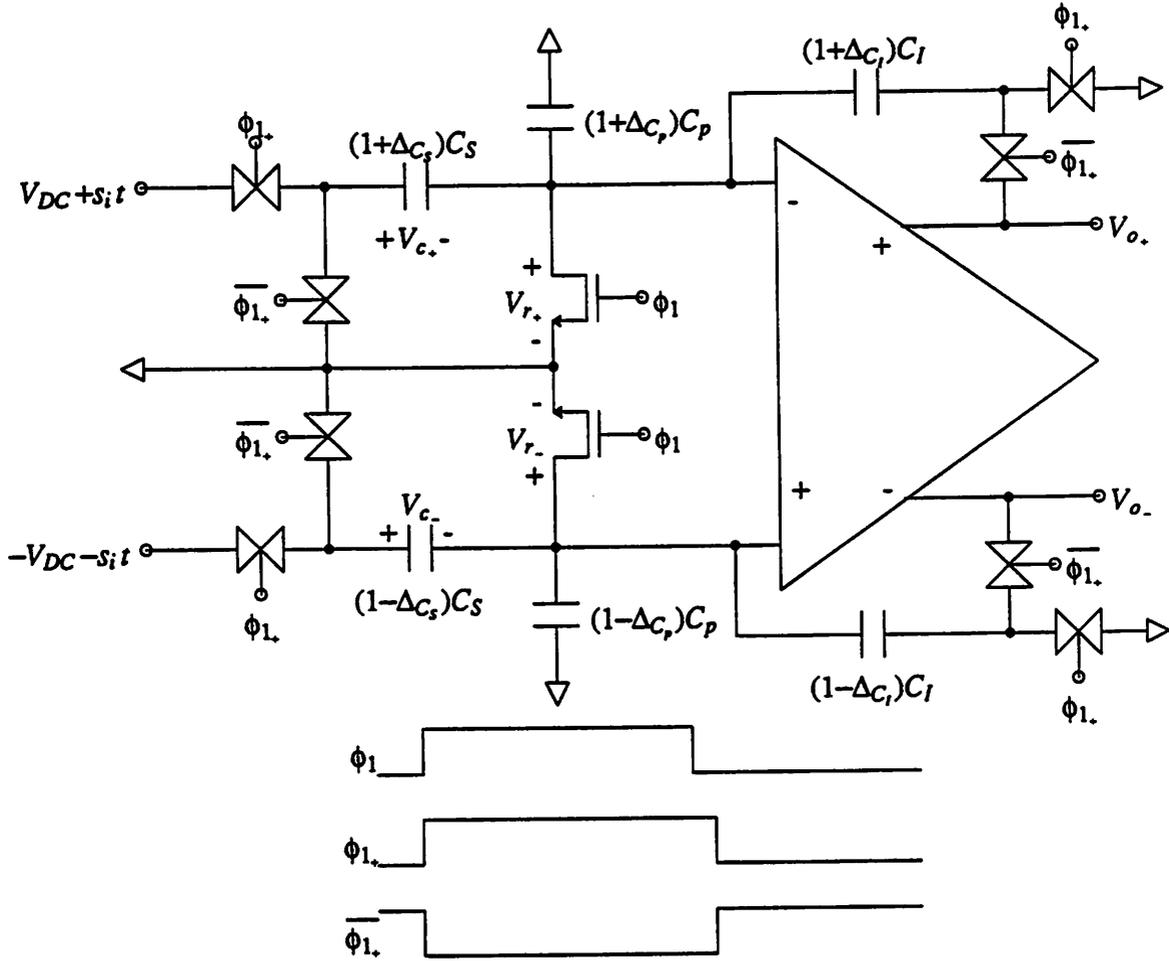
Fig. 2.10 Differential Bottom-Plated T/H Circuit

differential configuration is equivalent to two single-ended T/H circuit driven by $V_{DC}+s_i t$ and $-V_{DC}-s_i t$, respectively. The T/H output voltage can be calculated in the following two cases:

(A)   Positive input signal slew rate, i.e $s_i > 0$:

Since $s_i > 0$, from Eq. (2.26), we have $V_{r_+} > 0$ and $V_{r_-} < 0$. From Eq. (2.29) and Eq. (2.31), the differential T/H output voltage can be calculated as follows:

$$
\begin{aligned}
V_{o_{diff}} &= V_{o_+} - V_{o_-} \\
&= \frac{C_S(1+\Delta_{C_s})}{C_I(1+\Delta_{C_I})}\left\{ V_{DC}+s_i\left[\frac{V_{HT}(1+\Delta_{V_{HT}})}{s_g(1+\Delta_{s_g})}-\tau(1+\Delta_\tau)\right]-s_i^2\frac{\tau(1+\Delta_\tau)}{s_g(1+\Delta_{s_g})}\frac{C_S(1+\Delta_{C_s})}{C_T(1+\Delta_{C_T})}\right\} \\
&\quad - \frac{C_S(1-\Delta_{C_s})}{C_I(1-\Delta_{C_I})}\left\{ -V_{DC}-s_i\left[\frac{V_{HT}(1-\Delta_{V_{HT}})}{s_g(1-\Delta_{s_g})}-\tau(1-\Delta_\tau)\right]-s_i^2\chi\frac{\tau(1-\Delta_\tau)}{s_g(1-\Delta_{s_g})}\frac{C_S(1-\Delta_{C_s})}{C_T(1-\Delta_{C_T})}\right\}
\end{aligned}
$$

$$\approx (1+\Delta_{C_s}-\Delta_{C_I})\frac{C_S}{C_I}\left\{V_{DC}+s_i\left[(1+\Delta_{V_{HT}}-\Delta_{s_g})\frac{V_{HT}}{s_g}-\tau(1+\Delta_\tau)\right]-(1+\Delta_\tau-\Delta_{s_g}+\Delta_{C_s}-\Delta_{C_T})s_i^2\frac{\tau}{s_g}\frac{C_S}{C_T}\right\}$$

$$-(1-\Delta_{C_s}+\Delta_{C_I})\frac{C_S}{C_I}\left\{-V_{DC}-s_i\left[(1-\Delta_{V_{HT}}+\Delta_{s_g})\frac{V_{HT}}{s_g}-\tau(1-\Delta_\tau)\right]-(1-\Delta_\tau+\Delta_{s_g}-\Delta_{C_s}+\Delta_{C_T})s_i^2\chi\frac{\tau}{s_g}\frac{C_S}{C_T}\right\}$$

$$\approx \frac{C_S}{C_I}\left\{2V_{DC}+2s_i\left[\frac{V_{HT}}{s_g}-\tau\right]\right.$$

$$\left.-\left[(1-\chi)+(1+\chi)(2\Delta_{C_s}-\Delta_{C_I}+\Delta_\tau-\Delta_{s_g}-\Delta_{C_T})\right]s_i^2\frac{\tau}{s_g}\frac{C_S}{C_T}\right\} \tag{2.41}$$

(B)   Negative input signal slew rate, i.e $s_i < 0$

Since $s_i < 0$, from Eq. (2.26), we have $V_{r_+} < 0$ and $V_{r_-} > 0$. From Eq. (2.31) and Eq. (2.29), the differential T/H output voltage can be calculated as follow

$$V_{o_{diff}} = V_{o_+} - V_{o_-}$$

$$= \frac{C_S(1+\Delta_{C_s})}{C_I(1+\Delta_{C_I})}\left\{V_{DC}+s_i\left[\frac{V_{HT}(1+\Delta_{V_{HT}})}{s_g(1+\Delta_{s_g})}-\tau(1+\Delta_\tau)\right]-s_i^2\chi\frac{\tau(1+\Delta_\tau)}{s_g(1+\Delta_{s_g})}\frac{C_S(1+\Delta_{C_s})}{C_T(1+\Delta_{C_T})}\right\}$$

$$-\frac{C_S(1-\Delta_{C_s})}{C_I(1-\Delta_{C_I})}\left\{-V_{DC}-s_i\left[\frac{V_{HT}(1-\Delta_{V_{HT}})}{s_g(1-\Delta_{s_g})}-\tau(1-\Delta_\tau)\right]-s_i^2\frac{\tau(1-\Delta_\tau)}{s_g(1-\Delta_{s_g})}\frac{C_S(1-\Delta_{C_s})}{C_T(1-\Delta_{C_T})}\right\}$$

$$\approx (1+\Delta_{C_s}-\Delta_{C_I})\frac{C_S}{C_I}\left\{V_{DC}+s_i\left[(1+\Delta_{V_{HT}}-\Delta_{s_g})\frac{V_{HT}}{s_g}-\tau(1+\Delta_\tau)\right]-(1+\Delta_\tau-\Delta_{s_g}+\Delta_{C_s}-\Delta_{C_T})s_i^2\chi\frac{\tau}{s_g}\frac{C_S}{C_T}\right\}$$

$$-(1-\Delta_{C_s}+\Delta_{C_I})\frac{C_S}{C_I}\left\{-V_{DC}-s_i\left[(1-\Delta_{V_{HT}}+\Delta_{s_g})\frac{V_{HT}}{s_g}-\tau(1-\Delta_\tau)\right]-(1-\Delta_\tau+\Delta_{s_g}-\Delta_{C_s}+\Delta_{C_T})s_i^2\frac{\tau}{s_g}\frac{C_S}{C_T}\right\}$$

$$\approx \frac{C_S}{C_I}\left\{2V_{DC}+2s_i\left[\frac{V_{HT}}{s_g}-\tau\right]\right.$$

$$\left.-\left[-(1-\chi)+(1+\chi)(2\Delta_{C_s}-\Delta_{C_I}+\Delta_\tau-\Delta_{s_g}-\Delta_{C_T})\right]s_i^2\frac{\tau}{s_g}\frac{C_S}{C_T}\right\} \tag{2.42}$$

Combine Eq. (2.41) and Eq. (2.42) together, we got the following expression for differential T/H output voltage $V_{o_{diff}}$

$$V_{o_{diff}} = 2\frac{C_S}{C_I}\left\{ V_{DC} + s_i\left[\frac{V_{HT}}{s_g}-\tau\right] - \frac{(1-\chi)}{2}s_i|s_i|\frac{\tau}{s_g}\frac{C_S}{C_T}\right.$$

$$\left. - \frac{(1+\chi)}{2}(2\Delta_{C_s}-\Delta_{C_i}+\Delta_\tau-\Delta_{s_s}-\Delta_{C_T})s_i^2\frac{\tau}{s_g}\frac{C_S}{C_T}\right\} \tag{2.43}$$

Comparing Eq. (2.43) with Eq. (2.32), the coefficient of $s_i|s_i|$ is scaled sown by half and the coefficient of s_i^2 is now a function of mismatch, in the case of perfect matching, s_i^2 term disappears. Both terms introduce nonlinearity and distortion to the output of the T/H circuit, however the magnitude is smaller than in the single-ended case.

2.6.2 Detailed Analysis

Following the same argument as in Section 2.5.2 for the single-ended case, a more accurate result can be obtained. The detail of the derivation is described in Appendix B. In order to make the analysis complete, we will also include the effect of mismatch on capacitors and switches. Assume the sampling capacitors, gate capacitors, integrating capacitors, gate-drain overlap capacitors and "total" capacitors are $(1\pm\Delta_{C_s})C_S$, $(1\pm\Delta_{C_g})C_g$, $(1\pm\Delta_{C_i})C_I$, $(1\pm\Delta_{C_d})C_{ol}$, $(1\pm\Delta_{C_T})C_T$ respectively, and the time constants, gate fall rates, and V_{HT}'s are $(1\pm\Delta_\tau)\tau$, $(1\pm\Delta_{s_g})s_g$ and $(1\pm\Delta_{v_{m}})V_{HT}$ respectively. The differential T/H output voltage $V_{o_{diff}}$ can be calculated in the following two cases:

(A) Positive input signal slew rate, $s_i > 0$

From Eq. (B.1) in Appendix B, the differential T/H output voltage can be expressed as

$$V_{o_{diff}} = V_{o_+} - V_{o_-} = V_{o_0} + s_i V_{o_1} + s_i^2 V_{o_2} + s_i^3 V_{o_3} + \cdots \tag{2.44}$$

where V_{o_0} is the term independent of s_i, V_{o_1} is the coefficient of s_i, V_{o_2} is the coefficient of s_i^2 and V_{o_3} is the coefficient of s_i^3.

From Eq. (B.2), we have

$$V_{o_0} \approx 2\frac{C_S}{C_I}\left[V_{DC}+(\Delta_{C_d}-\Delta_{C_i})\frac{C_{ol}}{C_S}(V_{T_0}-V_L)\right]$$

$$+ 2(\Delta_{C_s}+\Delta_\tau+\Delta_{s_s}-\Delta_{C_i})\frac{C_T}{C_I}(1+\frac{\frac{C_g}{2}+C_{ol}}{C_T})(\frac{\frac{C_g}{2}+C_{ol}}{C_T})\tau s_g\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right]$$

$$\approx 2\frac{C_S}{C_I}\Big[V_{DC} + V_{os}\Big] \tag{2.45}$$

where V_{os} is the input-referred offset and can be expressed as

$$V_{os} \approx (\Delta_{C_a}-\Delta_{C_i})\frac{C_{ol}}{C_S}(V_{T_o}-V_L)$$

$$+ 2(\Delta_{C_s}+\Delta_\tau+\Delta_{s_s}-\Delta_{C_i})\frac{C_T}{C_S}(1+\frac{\frac{C_g}{2}+C_{ol}}{C_T})(\frac{\frac{C_g}{2}+C_{ol}}{C_T})\tau s_g\sqrt{\frac{\pi X}{2}}erf\Big[\sqrt{\frac{X}{2}}\Big] \tag{2.46}$$

From Eq. (B.4), we have

$$V_{o_2} = -\frac{C_S}{C_I}\frac{\tau}{s_g}\frac{C_S}{C_T}\Bigg\{(1+\Delta_\tau+2\Delta_{C_s}-\Delta_{C_i}-\Delta_{C_\tau}-\Delta_{s_s})f+\Big[(1-\Delta_{V_{HT}}+\Delta_\tau+\Delta_{s_s})X\Big]$$

$$- \chi(1-\Delta_\tau-2\Delta_{C_s}+\Delta_{C_i}+\Delta_{C_\tau}+\Delta_{s_s})f-\Big[(1+\Delta_{V_{HT}}-\Delta_\tau-\Delta_{s_s})X\Big]\Bigg\} \tag{2.47}$$

The quadratic nonlinear term becomes

$$s_i^2V_{o_2} \approx -s_is_i\frac{C_S}{C_I}\frac{\tau}{s_g}\frac{C_S}{C_T}\Bigg\{(1+\Delta_\tau+2\Delta_{C_s}-\Delta_{C_i}-\Delta_{C_\tau}-\Delta_{s_s})f+\Big[(1-\Delta_{V_{HT}}+\Delta_\tau+\Delta_{s_s})X\Big]$$

$$- \chi(1-\Delta_\tau-2\Delta_{C_s}+\Delta_{C_i}+\Delta_{C_\tau}+\Delta_{s_s})f-\Big[(1+\Delta_{V_{HT}}-\Delta_\tau-\Delta_{s_s})X\Big]\Bigg\} \tag{2.48}$$

which is similar to the result obtained in Eq. (2.41) in Section 2.6.1. Since this nonlinear dependence is proportional to τ and inversely proportional to s_g, by decreasing the time constant of the T/H network or increasing the gate fall rate s_g the distortion can be reduced.

(B) Negative input signal slew rate, i.e. $s_i < 0$:

From Eq. (B.9) in Appendix B, we have

$$V_o = V_{o_0} + s_iV_{o_1} + s_i^2V_{o_2} + s_i^3V_{o_3} + \cdots \tag{2.49}$$

where V_{o_0} is the term independent of s_i, V_{o_1} is the coefficient of s_i, V_{o_2} is the coefficient of s_i^2 and V_{o_3} is the coefficient of s_i^3.

From Eq. (B.7), we have

$$V_o \approx 2\frac{C_S}{C_I}\Big[V_{DC}+(\Delta_{C_a}-\Delta_{C_i})\frac{C_{ol}}{C_S}(V_{T_o}-V_L)\Big]$$

$$+ 2(\Delta c_s + \Delta_\tau + \Delta_{s_s} - \Delta c_i)\frac{C_T}{C_I}(1 + \frac{\frac{C_g}{2} + C_{ol}}{C_T})(\frac{\frac{C_g}{2} + C_{ol}}{C_T})\tau s_g \sqrt{\frac{\pi X}{2}} erf\left[\sqrt{\frac{X}{2}}\right]$$

$$\approx 2\frac{C_S}{C_I}\left[V_{DC} + V_{os}\right] \tag{2.50}$$

where V_{os} is the input-referred offset and can be expressed as

$$V_{os} \approx (\Delta c_{ol} - \Delta c_i)\frac{C_{ol}}{C_S}(V_{T_0} - V_L)$$

$$+ 2(\Delta c_s + \Delta_\tau + \Delta_{s_s} - \Delta c_i)\frac{C_T}{C_S}(1 + \frac{\frac{C_g}{2} + C_{ol}}{C_T})(\frac{\frac{C_g}{2} + C_{ol}}{C_T})\tau s_g \sqrt{\frac{\pi X}{2}} erf\left[\sqrt{\frac{X}{2}}\right] \tag{2.51}$$

From Eq. (B.9) in Appendix B, we have

$$V_{o_2} = -\frac{C_S}{C_I}\frac{\tau}{s_g}\frac{C_S}{C_T}\left\{ (1 - \Delta_\tau - 2\Delta c_s + \Delta c_i + \Delta c_\tau + \Delta_{s_s})f + \left[(1 + \Delta v_{HT} - \Delta_\tau - \Delta_{s_s})X\right]\right.$$

$$\left. - \chi(1 + \Delta_\tau + 2\Delta c_s - \Delta c_i - \Delta c_\tau - \Delta_{s_s})f - \left[(1 - \Delta v_{HT} + \Delta_\tau + \Delta_{s_s})X\right]\right\} \tag{2.52}$$

The quadratic nonlinear term becomes

$$s_i{}^2 V_{o_2} \approx -s_i s_i \frac{C_S}{C_I}\frac{\tau}{s_g}\frac{C_S}{C_T}\left\{ (1 - \Delta_\tau - 2\Delta c_s + \Delta c_i + \Delta c_\tau + \Delta_{s_s})f + \left[(1 + \Delta v_{HT} - \Delta_\tau - \Delta_{s_s})X\right]\right.$$

$$\left. - \chi(1 + \Delta_\tau + 2\Delta c_s - \Delta c_i - \Delta c_\tau - \Delta_{s_s})f - \left[(1 - \Delta v_{HT} + \Delta_\tau + \Delta_{s_s})X\right]\right\} \tag{2.53}$$

which is similar to the result obtained in Eq. (2.42) in Section 2.6.1. Since this nonlinear dependence is proportional to τ and inversely proportional to s_g, by decreasing the time constant of the T/H network or increasing the gate fall rate s_g this distortion can be reduced.

2.7 Differential T/H Circuit with Single Sampling Switch

Further improvement of the T/H is possible by replacing the two sampling switches in the differential T/H circuit with a single sampling switch as shown in Fig. 2.11. It is exactly the same as differential bottom-plate T/H circuit except that the two sampling switches have been replaced by a single center sampling switch. A single sampling switch has better matching properties than

two different sampling switches. However, using a single center switch does require extra switches to reset the common mode signal. Fortunately, if the input common mode is well controlled, only a pair of very small switches is needed and should have negligible effect on the T/H performance. As shown in Fig. 2.11, a pair of common mode reset switches are connected to the op amp input to reset the common mode voltage. Phase ϕ_{1-}, an advanced version of ϕ_1 is used to turn off the common mode reset switch just before the sampling switch turns off. Since the common mode reset switches are much smaller than the sampling switch, the charge injection error is smaller and decreases exponentially until the sampling switch turns off. A single center switch also has twice the bandwidth compared to the two ground switch approach because the equivalent capacitor of two capacitor connected in series is only half its original value.
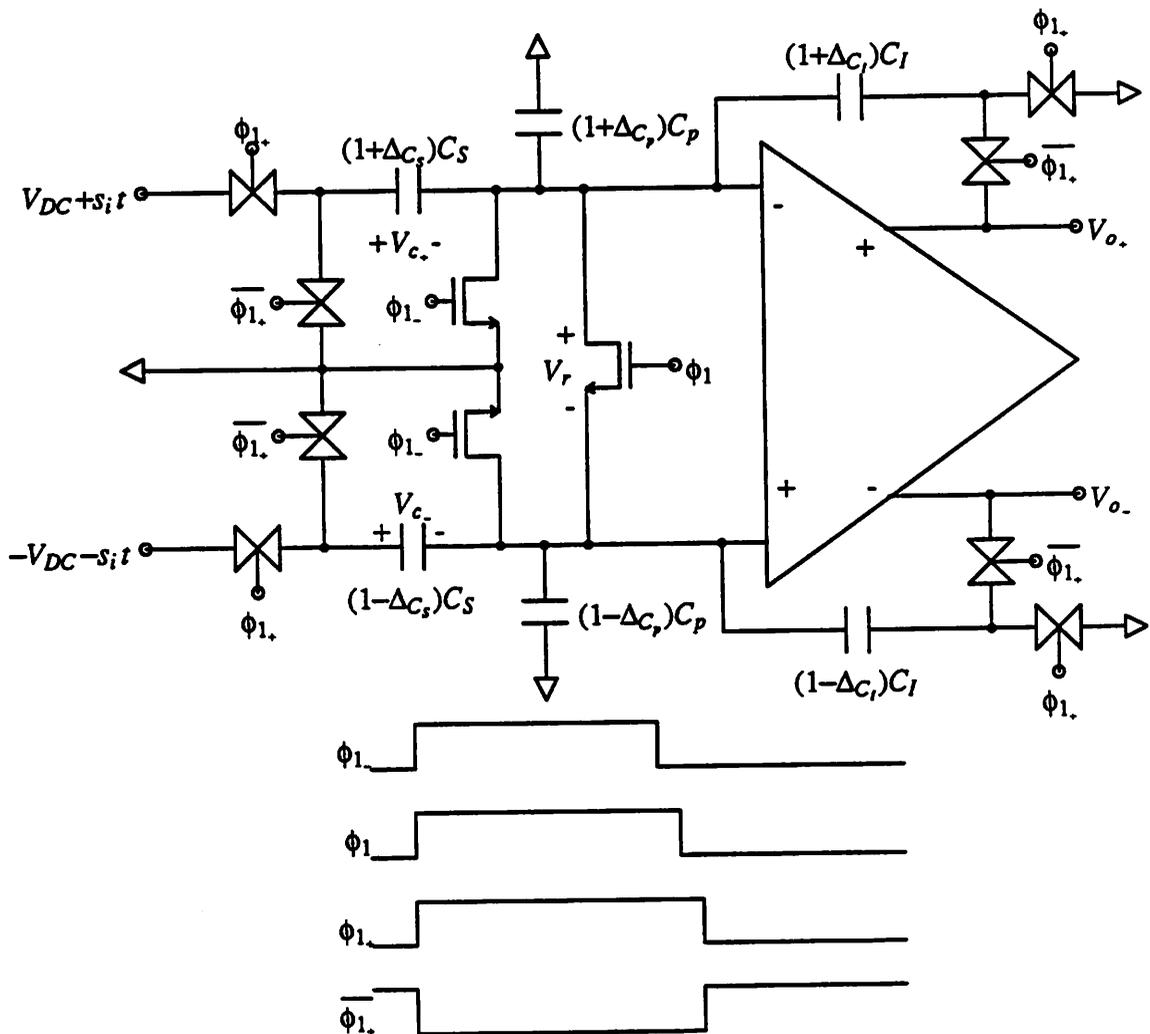

Fig. 2.11 Differential T/H Circuit with Single Sampling Switch

2.7.1 Approximate Analysis

Again, we follow the same approach as in the single-ended bottom-plate T/H circuit. Assume the positive and negative input are $V_{DC}+s_i t$ and $-V_{DC}-s_i t$ respectively, and the gate voltage is $V_H-s_g t$. The conductance of the switch is

$$G = \frac{1}{R} = k\frac{W}{L}(V_H-V_T) = \beta_n(V_H-V_T) \approx \beta_n(V_H-V_{T_o}) = \beta_n V_{HT} \tag{2.54}$$

and the time constant of the T/H circuit is

$$\tau = \frac{1}{2}\frac{C_T}{G} = \frac{1}{2}RC_T = \frac{C_T}{2\beta_n V_{HT}} \tag{2.55}$$

where $C_T=C_S+C_I+C_p$ is the total capacitance at the sampling node. From Eq. (2.2), the acquisition time of the T/H circuit is

$$T_{aq} = (b+1)\tau ln 2 = \frac{(b+1)C_T ln2}{2\beta_n V_{HT}} \tag{2.56}$$

and the voltage across the sampling switch is

$$V_r(0) = \frac{s_i C_S}{G} = s_i C_S R = \frac{s_i C_S}{\beta_n V_{HT}} = 2s_i\tau\frac{C_S}{C_T} \tag{2.57}$$

The same assumption is used to approximate this T/H circuit as in the top-plate case. The T/H output voltage can be calculated in the following two cases:

(A) Positive input signal slew rate, i.e. $s_i>0$

Since $s_i>0$, from Eq. (2.57), we have $V_r>0$ and $V_d(T_a)=\frac{1}{2}V_r(T_a)$ and $V_s(T_a)=-\frac{1}{2}V_r(T_a)$. Because the sampling switch turns off at $t=T_a$ when it enters saturation region, where T_a is the aperture time, T_a can be calculated by the following equation

$$V_g(T_a)-V_d(T_a)-V_T = V_g(T_a)-\frac{1}{2}V_r(T_a)-\left[V_{T_o}-\chi\frac{V_r(T_a)}{2}\right]$$

$$= V_H-s_g T_a-\frac{(1-\chi)}{2}V_r(T_a)-V_{T_o} = 0 \tag{2.58}$$

thus

$$T_a = \frac{1}{s_g}\left[V_{HT}-\frac{(1-\chi)}{2}V_r\right] \tag{2.59}$$

From Eq. (2.53), the aperture time T_a is a function of the input signal slew rate s_i and gate fall rate s_g. This aperture time modulation introduces nonlinearity and distortion to the T/H output. Since the charge sampled on the sampling nodes at $t=T_a$ will eventually transfer to the integrating capacitor C_I, the final T/H output voltage V_o can be calculated as

$$V_{o_{all}} = -\frac{1}{(1+\Delta_{C_I})C_I}\left\{(1+\Delta_{C_s})C_S\left[\frac{1}{2}V_r(T_a)-V_i(T_a)\right]+\left[(1+\Delta_{C_p})C_p+(1+\Delta_{C_I})C_I\right]\frac{1}{2}V_r(T_a)\right\}$$

$$+ \frac{1}{(1-\Delta_{C_I})C_I}\left\{(1-\Delta_{C_s})C_S\left[-\frac{1}{2}V_r(T_a)+V_i(T_a)\right] - \left[(1-\Delta_{C_p})C_p+(1-\Delta_{C_I})C_I\right]\frac{1}{2}V_r(T_a)\right\}$$

$$\approx -\frac{(1-\Delta_{C_I})}{C_I}\left\{(1+\Delta_{C_s})C_S\left[\frac{1}{2}V_r(T_a)-V_{DC}-s_iT_a\right] + \left[(1+\Delta_{C_p})C_p+(1+\Delta_{C_I})C_I\right]\frac{1}{2}V_r(T_a)\right\}$$

$$+ \frac{(1+\Delta_{C_I})}{C_I}\left\{(1-\Delta_{C_s})C_S\left[-\frac{1}{2}V_r(T_a)+V_{DC}+s_iT_a\right] - \left[(1-\Delta_{C_p})C_p+(1-\Delta_{C_I})C_I\right]\frac{1}{2}V_r(T_a)\right\}$$

$$= \frac{C_S}{C_I}\left\{2V_{DC} - \frac{C_T}{C_S}2s_i\tau\frac{C_S}{C_T} + 2\frac{s_i}{s_g}\left[V_{HT}-\frac{(1-\chi)}{2}2s_i\tau\frac{C_S}{C_T}\right]\right\}$$

$$\approx \frac{C_S}{C_I}\left\{2V_{DC} + 2s_i\left[\frac{V_{HT}}{s_g}-\tau\right] - 2(1-\chi)\frac{\tau}{s_g}s_i^2\frac{C_S}{C_T}\right\} \tag{2.60}$$

(B) Negative input signal slew rate, i.e. $s_i<0$

Since $s_i<0$, from Eq. (2.57), we have $V_r<0$ and $V_d(T_a)=-\frac{1}{2}V_r(T_a)$ and $V_s(T_a)=\frac{1}{2}V_r(T_a)$. Because the sampling switch turns off at $t=T_a$ when it enters saturation region, where T_a is the aperture time, T_a can be calculated by the following equation

$$V_g(T_a)-V_d(T_a)-V_T = V_g(T_a)+\frac{1}{2}V_r(T_a)-\left[V_{T_o}+\chi\frac{V_r(T_a)}{2}\right]$$

$$= V_H-s_gT_a+\frac{(1-\chi)}{2}V_r(T_a)-V_{T_o} = 0 \tag{2.61}$$

thus

$$T_a = \frac{1}{s_g}\left[V_{HT}+\frac{(1-\chi)}{2}V_r\right] \tag{2.62}$$

From Eq. (2.62), the aperture time T_a is a function of the input signal slew rate s_i and gate fall

rate s_g. This aperture time modulation introduces nonlinearity and distortion to the T/H output. Since the charge sampled on the sampling nodes at $t=T_a$ will eventually transfer to the integrating capacitor C_I, the final T/H output voltage V_o can be calculated as

$$V_{o_{all}} = -\frac{1}{(1+\Delta_{C_I})C_I}\left\{(1+\Delta_{C_s})C_S\left[\frac{1}{2}V_r(T_a)-V_i(T_a)\right] +\left[(1+\Delta_{C_r})C_p+(1+\Delta_{C_i})C_I\right]\frac{1}{2}V_r(T_a)\right\}$$

$$+ \frac{1}{(1-\Delta_{C_I})C_I}\left\{(1-\Delta_{C_s})C_S\left[-\frac{1}{2}V_r(T_a)+V_i(T_a)\right] -\left[(1-\Delta_{C_r})C_p+(1-\Delta_{C_i})C_I\right]\frac{1}{2}V_r(T_a)\right\}$$

$$= -\frac{(1-\Delta_{C_i})}{C_I}\left\{(1+\Delta_{C_s})C_S\left[\frac{1}{2}V_r(T_a)-V_{DC}-s_iT_a\right] +\left[(1+\Delta_{C_r})C_p+(1+\Delta_{C_i})C_I\right]\frac{1}{2}V_r(T_a)\right\}$$

$$+ \frac{(1+\Delta_{C_i})}{C_I}\left\{(1-\Delta_{C_s})C_S\left[-\frac{1}{2}V_r(T_a)+V_{DC}+s_iT_a\right] -\left[(1-\Delta_{C_r})C_p+(1-\Delta_{C_i})C_I\right]\frac{1}{2}V_r(T_a)\right\}$$

$$= \frac{C_S}{C_I}\left\{2V_{DC} - \frac{C_T}{C_S}2s_i\tau\frac{C_S}{C_T} + 2\frac{s_i}{s_g}\left[V_{HT}+\frac{(1-\chi)}{2}2s_i\tau\frac{C_S}{C_T}\right]\right\}$$

$$= \frac{C_S}{C_I}\left\{2V_{DC} + 2s_i\left[\frac{V_{HT}}{s_g}-\tau\right] + 2(1-\chi)\frac{\tau}{s_g}s_i{}^2\frac{C_S}{C_T}\right\} \tag{2.63}$$

Combining Eq. (2.60) and Eq. (2.63) together, we have the following expression for T/H output voltage $V_{o_{all}}$

$$V_{o_{all}} = \frac{C_S}{C_I}\left\{2V_{DC} + 2s_i\left[\frac{V_{HT}}{s_g}-\tau\right] - 2(1-\chi)\frac{\tau}{s_g}s_i|s_i|\frac{C_S}{C_T}\right\} \tag{2.64}$$

There is no first order dependence on the mismatch of circuit parameters in Eq. (2.64). Therefore, this T/H circuit is relatively insensitive to the mismatch of capacitors and switches. Due to this robust property and the smaller switch size required to achieve the same bandwidth, this T/H topology is superior to the conventional differential bottom-plate T/H topology and has the best T/H performance among the four topologies discussed in this chapter.

2.7.2 Detailed Analysis

Following the same argument as in Section 2.5.2 for the single-ended case, a more accurate result can be obtained. The detail of the derivation is described in Appendix C. In order to make

the analysis complete, we will also include the effect of mismatch on capacitors and switches. Fig. 2.12 shows the equivalent circuit of the bottom-plate differential T/H with a single sampling switch.
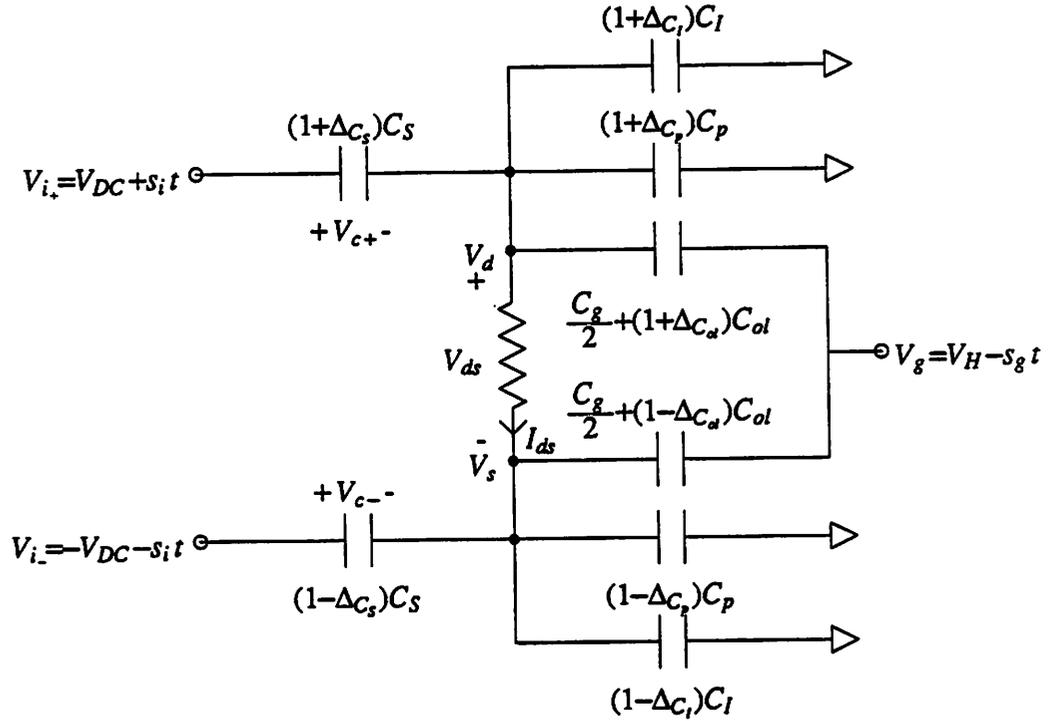
Fig. 2.12 Equivalent Circuit of Differential T/H Circuit with Single Sampling Switch

Assume the sampling capacitors, integrating capacitors, parasitic capacitors, gate-drain overlap capacitors and "total" capacitors are $(1\pm\Delta_{C_s})C_S$, $(1\pm\Delta_{C_I})C_I$, $(1\pm\Delta_{C_p})C_p$, $(1\pm\Delta_{C_a})C_{ol}$ and $(1\pm\Delta_{C_T})C_T$ respectively. The differential T/H output voltage $V_{o_{diff}}$ can be calculated in the following two cases:

(A) Positive input signal slew rate, $s_i > 0$

From Eq. (C.27) in Appendix C, the differential T/H output voltage can be expressed as

$$V_{o_{diff}} = V_{o_0} + s_i V_{o_1} + s_i^2 V_{o_2} + s_i^3 V_{o_3} + \cdots \tag{2.65}$$

where V_{o_0} is the term independent of s_i, V_{o_1} is the coefficient of s_i, V_{o_2} is the coefficient of s_i^2 and V_{o_3} is the coefficient of s_i^3.

From Eq. (C.28) in Appendix C, we have

$$V_{o_0} \approx 2\frac{C_S}{C_I}\left[V_{DC} + V_{os}\right] \tag{2.66}$$

where V_{os} is the input-referred offset and can be expressed as

$$V_{os} \approx (\Delta_{C_\alpha} - \Delta_{C_I})\frac{C_{ol}}{C_S}(V_{T_0} - V_L)$$

$$+ \left[\Delta_{C_T}\frac{(\frac{C_g}{2} + C_{ol})}{C_S} - \Delta_{C_\alpha}\frac{C_{ol}}{C_S}\right]\tau s_g\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right] \tag{2.67}$$

and from Eq. (C.30)

$$V_{o_2} \approx -2(1-\chi)\frac{C_S}{C_I}\frac{\tau}{s_g}\frac{C_S}{C_T} \tag{2.68}$$

The quadratic nonlinear term becomes

$$s_i{}^2V_{o_2} \approx -2(1-\chi)\tau s_i\frac{s_i}{s_g}\frac{C_S{}^2}{C_TC_I} \tag{2.69}$$

which is similar to the result obtained in Eq. (2.60) in Section 2.7.1. Since this nonlinear dependence is proportional to τ and inversely proportional to s_g, by increasing the sampling switch size or gate fall rate s_g this distortion can be reduced.

(B)   Negative input signal slew rate, i.e. $s_i < 0$:

From Eq. (C.43) in Appendix C, we have

$$V_o = V_{o_0} + s_iV_{o_1} + s_i{}^2V_{o_2} + s_i{}^3V_{o_3} + \cdots \tag{2.70}$$

where V_{o_0} is the term independent of s_i, V_{o_1} is the coefficient of s_i term, V_{o_2} is the coefficient of $s_i{}^2$ and V_{o_3} is the coefficient of $s_i{}^3$.

From Eq. (C.44) in Appendix C, we have

$$V_{o_0} \approx 2\frac{C_S}{C_I}\left[V_{DC} + V_{os}\right] \tag{2.71}$$

where V_{os} is the input-referred offset and can be expressed as

$$V_{os} \approx (\Delta_{C_\alpha} - \Delta_{C_I})\frac{C_{ol}}{C_S}(V_{T_0} - V_L)$$

$$+ \left[\Delta_{C_T}\frac{(\frac{C_g}{2} + C_{ol})}{C_S} - \Delta_{C_\alpha}\frac{C_{ol}}{C_S}\right]\tau s_g\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right] \tag{2.72}$$

and from Eq. (C.46)

$$V_{o_2} \approx 2(1-\chi)\frac{C_S}{C_I}\frac{\tau}{s_g}\frac{C_S}{C_T} \tag{2.73}$$

The quadratic nonlinear term becomes

$$s_i^2 V_{o_2} \approx 2(1-\chi)\tau s_i \frac{s_i}{s_g}\frac{C_S^2}{C_T C_I} \tag{2.74}$$

which is similar to the result obtained in Eq. (2.63) in Section 2.7.1. Since this nonlinear depen-

dence is proportional to τ and inversely proportional to s_g, by increasing the sampling switch size

or gate fall rate s_g this distortion can be reduced.

2.8 Calculation and Simulation Results

In this section, the calculation and simulation results of various T/H circuits are presented.

The T/H output voltage V_o can be represented as

$$V_o = \frac{C_S}{C_I}(V_{os} + g_1 V_{DC} + g_2 V_{DC}^2 + \cdots + s_i V_{o_1} + s_i^2 V_{o_2} + \cdots) \tag{2.75}$$

where $\frac{C_S}{C_I}$ is the gain of the T/H circuit, V_{DC} is the desired sampled input and V_{os} is the T/H

input-referred offset, g_1 is the coefficient of V_{DC}, g_2 is the coefficient of V_{DC}^2, V_{o_1} is the

coefficient of s_i and V_{o_2} is the coefficient of s_i^2.

An ideal T/H output has no offset with the coefficient g_1 equal to 1 and all the other

coefficient equal to zero. However, in a practical T/H circuit, there usually exists several nonideal

terms in Eq. (2.75). For example, a g_1 other than 1 represents a gain error, while a nonzero V_{o_1}

represents a low-pass T/H frequency response. These two terms introduce linear errors, i.e gain

error and finite bandwidth. Depending on the applications, gain error, finite bandwidth and offset

sometimes can be tolerated without serious effects. The other coefficients, such as g_2 and V_{o_2}

represent nonlinearity in the T/H circuit and are important in characterizing dynamic behavior of

the T/H circuit. In the case of a bottom-plate T/H circuit, $g_1=1$ and $g_i=0$ for $i = 2,3,...$, because

the output of a bottom-plate T/H circuit is not dependent on V_{DC}.

From the calculations in Section 2.5-2.7, it can be shown that offset V_{os} can be represented

in the following form:

$$V_{os} \quad \alpha \quad \frac{C_g}{C_S}\tau s_g \quad \alpha \quad \frac{1}{4}\frac{C_g}{C_S}\frac{f_T}{f_{T/H}}(V_H-V_L) \tag{2.76}$$

where the gate fall rate s_g is technology dependent and can be calculated using the fall time of a CMOS gate as follow [15]

$$s_g = \frac{(V_H-V_L)}{t_f} = \frac{(V_H-V_L)}{4\dfrac{C_L}{\beta_n(V_H-V_L)}} = \frac{1}{4}2\pi f_T(V_H-V_L) \tag{2.77}$$

where t_f is the gate fall time and $f_T=\dfrac{\beta_n(V_H-V_L)}{2\pi C_L}$ is the usable transition, i.e. unity-gain, frequency and $f_{T/H}$ is the bandwidth of T/H network. Assume the peak input amplitude is A, then the percentage offset can be represented by

$$\frac{V_{os}}{A} = \frac{1}{4}\frac{C_g}{C_S}\frac{f_T}{f_{T/H}}\frac{(V_H-V_L)}{A} \tag{2.78}$$

Also from the calculation in Section 2.5-2.7, V_{o_2} can be represented in the following form:

$$V_{o_2} \quad \alpha \quad \frac{\tau}{s_g}\frac{C_S}{C_T} \quad \alpha \quad \frac{1}{\pi^2 f_T f_{T/H}(V_H-V_L)}\frac{C_S}{C_T} \tag{2.79}$$

Assume the input is $A\cos2\pi f_{in}t$, then the peak input signal slew rate is $2\pi f_{in}A$ and the nonlinear term becomes

$$s_i^2 V_{o_2} \quad \alpha \quad \frac{(2\pi f_{in}A)^2}{\pi^2 f_T f_{T/H}(V_H-V_L)}\frac{C_S}{C_T} \quad \alpha \quad 4\frac{f_{in}}{f_T}\frac{f_{in}}{f_{T/H}}\frac{A^2}{(V_H-V_L)}\frac{C_S}{C_T} \tag{2.80}$$

The percentage linearity error becomes

$$\frac{s_i^2 V_{o_2}}{A} \quad \alpha \quad 4\frac{f_{in}}{f_T}\frac{f_{in}}{f_{T/H}}\frac{A}{(V_H-V_L)}\frac{C_S}{C_T} \tag{2.81}$$

For the two differential topologies, common mode voltage shift due to the negative charge injection in the NMOS transistor is also important. A large negative common mode voltage shift could drive the op amp summing node out of its common mode input range and seriously degrade its settling speed. The common mode voltage shift due to the charge injection can be expressed as

$$V_{\Sigma} = -\frac{WLC_{ox}V_{HT}}{2C_T} \tag{2.82}$$

Although the constraint on the common mode voltage limits the largest size of the switch that can be safely used, a simple transmission gate in place of the single sampling switch can relieve the problem. However, the differential offset voltage will increase due to the larger mismatch of two different switches. Fig. 2.13-2.17 show the simulation and calculation results for the three bottom-plate T/H circuit. In order to present the result in a technology independent form, the horizontal axis is chosen to be $\frac{f_{in}}{f_T} \frac{f_{in}}{f_{T/H}} \frac{A}{(V_H-V_L)} \frac{C_S}{C_T}$. These graphs are intended to be used as design guidelines in designing a MOS T/H circuit to meet the offset and linearity requirements. Since the offset and nonlinearity depend on $f_{T/H}$, C_S, C_g, C_T, (V_H-V_L) and A in opposite ways, the design is based on a tradeoff between the offset and nonlinearity.

The simulation is done by Non Quasi-Static charge modeling in SPICE3 by Park, et al. [6]. Results are shown in Fig. 2.13 to Fig. 2.17. The triangles in the graph are the simulation results, while the solid lines represent the calculation results. Fig. 2.13 shows the results of the bottom-plate T/H circuit, its performance is the worst among the three bottom-plate T/H circuits. However, this is still better than the top-plate T/H circuit. As mentioned above, the offset and non-linearity exhibit opposite trends, therefore the design is based on a tradeoff between the offset and nonlinearity. Fig. 2.14 and Fig. 2.15 show the results of the differential bottom-plate T/H circuit, both the offset and nonlinearity are smaller than the single-ended case due to the first order cancellation inherently associated with differential circuit. In the perfect matching case, there is no offset. However, in the case of 1% capacitor mismatch, the offset and nonlinearity exhibits opposite trends and the design is again based on a tradeoff between offset and nonlinearity. Fig. 2.16 and Fig. 2.17 show the results of the differential bottom-plate T/H circuit with a single sampling switch. Its characteristic is similar to the two sampling switches approach, but both the offset and nonlinearity are much smaller. This topology is the best amongst the three bottom-plate T/H circuits. The design is based on a tradeoff between offset and nonlinearity. Although the simulation results show some discrepancy with the calculation results, the general trends do match each other. In the case of a differential topology, both the offset and nonlinearity are the residue of a first order cancellation. The approximation we used in the calculation could easily account for the discrepancy.

A design example is described below, for example, with 5V supply, 4 pF sampling capaci-

tor, 8 pF total capacitor, ± 1V reference, a $\frac{100\mu m}{3\mu m}$ single sampling switch used in differential T/H circuit in a 3 μm CMOS technology can achieve 0.01% linearity, i.e., 13 bit, with 16 MHz input signal, but the offset will be 0.05% of the full scale, i.e., 4 LSB and the common mode voltage shift is -125 mV.

In conclusion, a set of graphs is presented to use as a design guideline. A differential T/H with single sampling switch outperforms the other topologies and the smaller $\frac{f_{in}}{f_{T/H}}$, $\frac{f_{in}}{f_T}$, $\frac{C_S}{C_T}$ and $\frac{A}{(V_H-V_L)}$, the better the linearity, however at the expense of larger offset and in the case of large switch, at the expanse of larger common mode voltage shift. Offset cancellation is possible, but extra clock cycle is required. There appears to have no theoretical limit on how good the S/H circuit can be, however, as the input frequency f_{in} and T/H bandwidth $f_{T/H}$ get close to f_T, practical considerations such as loading of the op amp summing node, common mode voltage shift and differential offset begin to dictate.
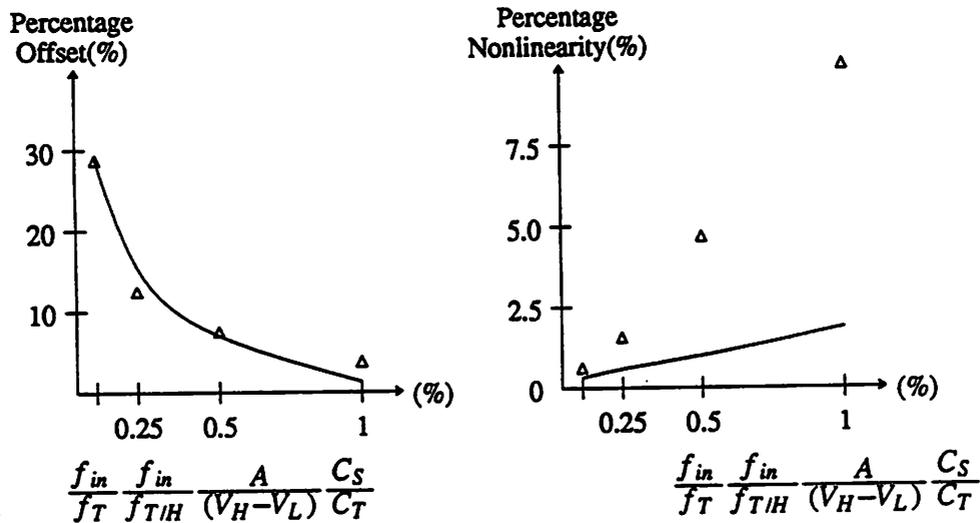

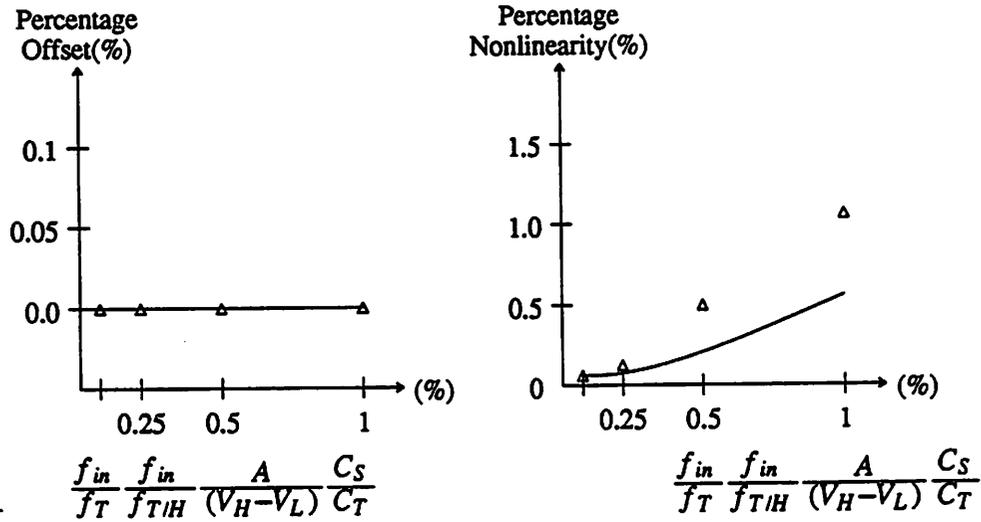Fig. 2.13 Performance of the Bottom-Plate T/H Circuit

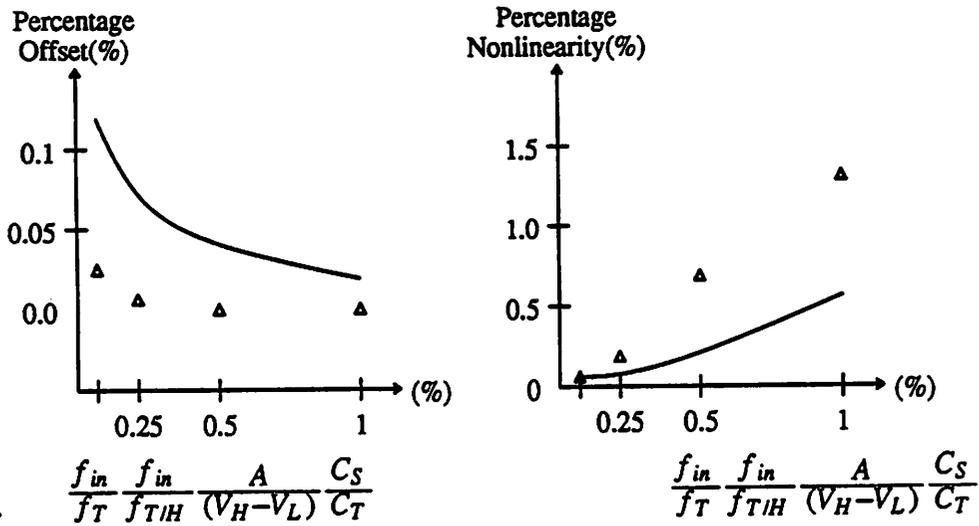Fig. 2.14 Performance of the Differential T/H Circuit

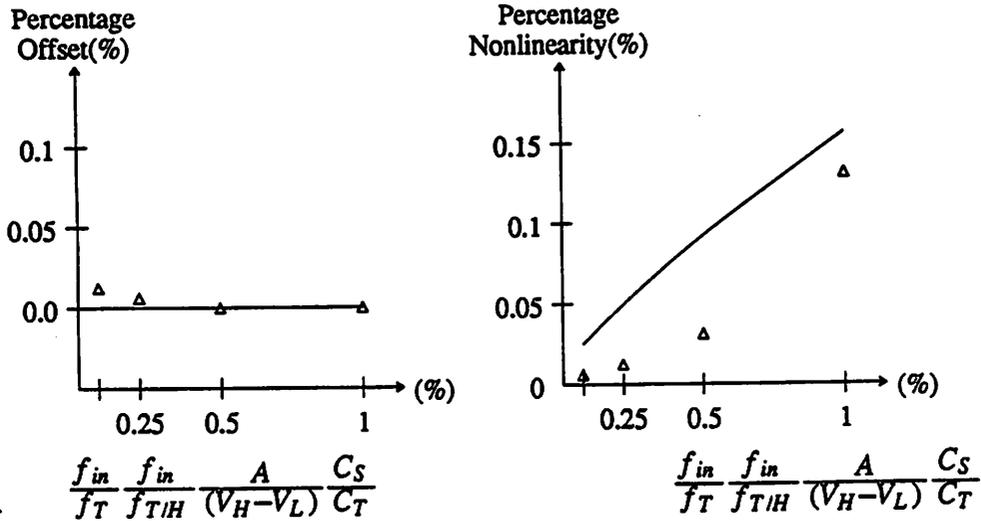Fig. 2.15 Performance of the Differential T/H Circuit(1% Mismatch)

Fig. 2.16 Performance of the Differential T/H Circuit with Single Sampling Switch
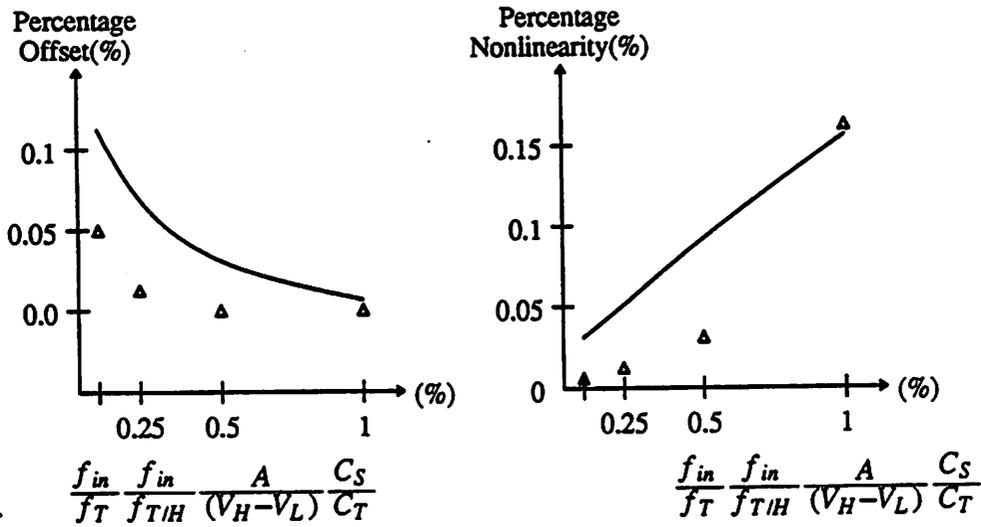

Fig. 2.17 Performance of the Differential T/H with Single Sampling Switch (1% mismatch)

CHAPTER 3

CMOS ADC ARCHITECTURES FOR HIGH RESOLUTION AT VIDEO SPEEDS

3.1 Introduction

There are many A/D converter architectures, but only a handful of them, namely, flash, subranging and pipelined architectures, are suitable for video-rate applications. The requirement for high resolution at video speed puts an even more stringent constraint on the choice of the architectures available. As can be shown later in this chapter, not all three of them can be used in high-resolution applications. We will discuss their relative advantages and limitations in this chapter and also look at their potential for use as 12-13 bits video-rate converters.

3.2 Flash Architecture

One N-bit converter architecture uses 2^N-1 comparators to compare the input simultaneously with 2^N-1 linearly graded voltage references. Since all the comparators work simultaneously in the same time interval, such an architecture is called a parallel or flash architecture. Fig. 3.1 shows a block diagram of a N-bit flash A/D converter. It consists of a resistor string, a bank of 2^N-1 comparators, and a digital encoding circuit. The resistor string divides the reference into 2^N regions of equal potential difference, and provides the voltages at the boundaries of these regions as reference voltages to the bank of comparators. The analog input is also connected to every comparator. All the comparators are strobed simultaneously to latch their output. The output of comparators are high for comparators whose reference are less than the input. therefore, the output of comparators form a thermometer code where the transition from 1 to 0 indicates the input level. To complete the conversion, the digital outputs of the comparators are encoded from thermometer code to binary.
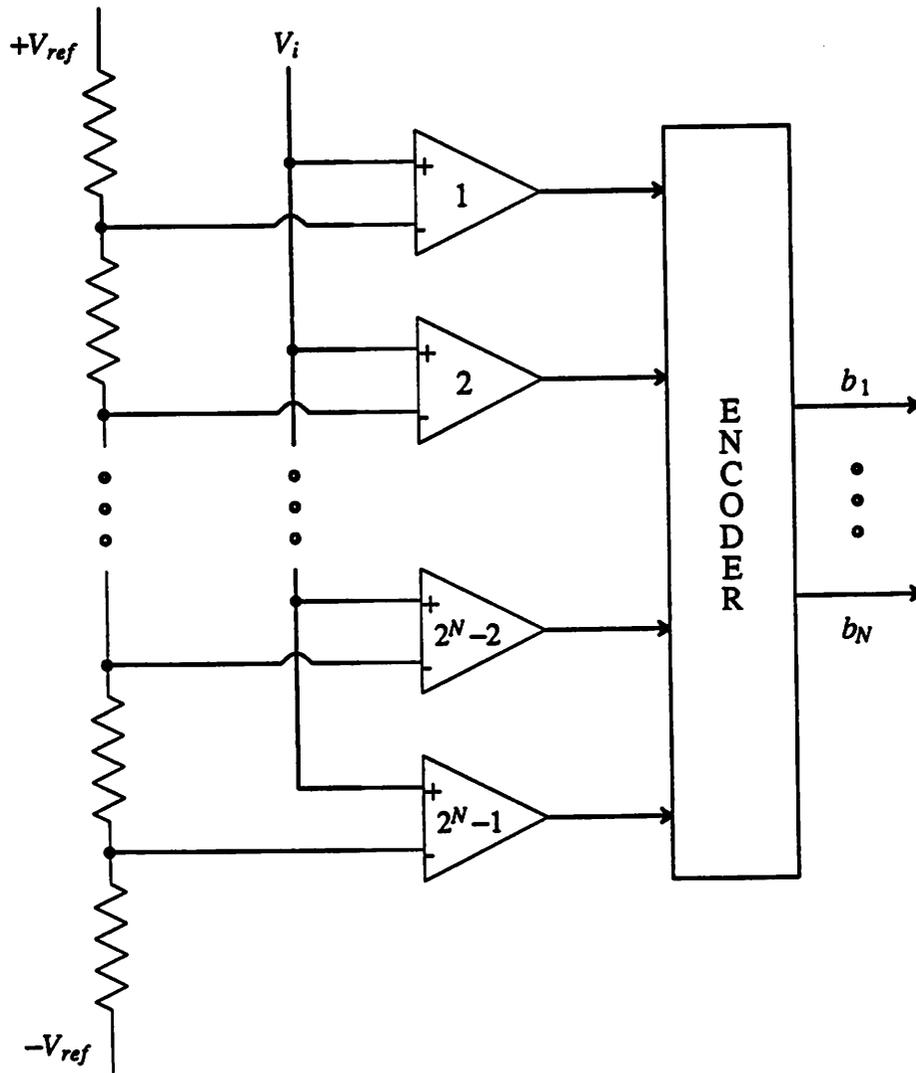
Fig. 3.1 Flash A/D Converter

3.2.1 Advantages

The primary advantage of the flash architecture is its high conversion rate. Only two clock phases are necessary to drive the comparator to toggle between the latched and unlatched states. Since the encoding logic is a combinatorial logic, it can be pipelined to achieve higher speed. Therefore, the speed of this architecture is only limited by the speed of the comparators.

3.2.2 Limitations

quency.

3.2.3 Conclusions

In conclusion, flash architecture is not suitable for high-resolution video-rate applications due to the three drawbacks. First, the exponential growth of the area, the power consumption and the input capacitance with the number of bits resolved prohibit the flash architecture to be implemented at reasonable cost with more than 8-bits level. Second, the difficulty in obtaining accurate comparison between the input and reference voltage also limit the resolution to 8 bits in video-rate applications. Third, the lack of a dedicated S/H amplifier limit its high frequency performance to be no more than 8-bits accuracy. Although the flash architecture is simple and fast, implementation difficulties and costs limit this architecture to have a resolution no more than 8 bits.[8]

3.3 Subranging Architecture

The Subranging A/D architecture can be viewed as a combination of successive approximation and flash A/D architectures. As discuss in the previous section, the flash A/D converter suffers from exponential relationship between its costs and resolutions. To improve the efficiency, the successive approximation architecture can be used to break one N-bits conversion into M $\frac{N}{M}$-bits subconversions. The area, power consumption and input capacitance are more manageable in this case. Fig. 3.3 shows a block diagram of a 2-step, N-bits subranging A/D converter. It consists of a S/H block, two $\frac{N}{2}$-bit flash A/D subconverters, a $\frac{N}{2}$-bit D/A converter, a subtractor and a $\frac{N}{2}$-bit digital encoding circuit. The input is first sampled by the S/H circuit. The held input is then converted into digital code by the coarse A/D subconverter and back into an analog signal by the D/A converter. The residue, which is the difference between the held input and D/A converter output, is then digitized by the fine A/D subconverter. After the digital output from both subconverters are encoded into binary, the encoded outputs from the second stage are appended to those from the first stage to produce a N-bits binary output.
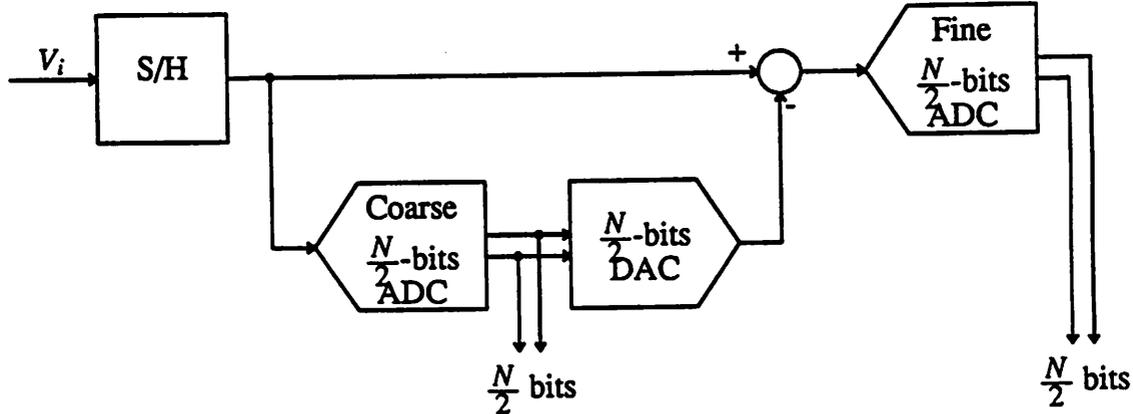
Fig. 3.3 Subranging A/D Converter

3.3.1 Advantages

The primary advantage of the subranging converter architecture is that it requires less hardware than a flash architecture. Although Fig. 3.3 shows quite a few components, most of them can either be time-shared or merged together to save the hardware. For example, a single resistor string with 2^N elements may be used to provide the coarse reference and fine reference to the two A/D subconverters and the D/A converter. Since the fine A/D conversion cannot be performed before the residue is generated, an array of $2^{\frac{N}{2}}-1$ comparators can be time-shared between the two A/D functions. The S/H function is embedded into the A/D subconverter as in a flash converter. Both subranging and flash architecture need the same resistor string. But only $2^{\frac{N}{2}}-1$ comparators and a $\frac{N}{2}$-bits digital encoding circuit are required in the subranging architecture. The only overhead is a switching network to facilitate the D/A conversion and subtractor function. The area, power consumption and the input capacitance of a subranging A/D converter are much smaller than in the case of flash A/D converter.[9]

Another advantage of the subranging architecture over flash architecture is the improved performance of the S/H function. Because the number of the comparators is much smaller than in the case of flash converter, the problem of the sampling jitter between the comparators is correspondingly reduced. As in the flash A/D converter, no op amps are required. The high throughput and low cost make subranging architecture particularly suitable for low-cost video-

rate applications, such as HDTV.

3.3.2 Limitations

Since the subranging A/D architecture requires two A/D subconversion in sequence, the conversion rate is only half of what can be achieved by the flash converter. With current technology, this architecture is limited to 2 step in order to achieve video speed. This means the area, power consumption and input capacitance are proportional to $2^{\frac{N}{2}}$ and still exponentially related to the resolution.

The ability to operate without an op amp is a key advantage of subranging architecture, but the absence of op amps causes some limitations. Without op amps, it is impossible to implement parasitic-insensitive S/H amplifier. As mentioned in the previous section, the S/H function must then be merged into the A/D subconversions. Although the problem of sampling jitter between comparators is diminished from that in a flash converter because of the reduction in the number of comparators, the problem is not eliminated. This still poses some limitations when converts high frequency input. Since there is no interstage S/H amplifier, the interstage gain is equal to one, and the effect of nonideality in the second stage is unattenuated on the linearity of the entire conversion. Therefore, as in the flash converter, the random offset of all the comparators and resistor string mismatches must be within $\pm\frac{1}{2}$ LSB. The need for offset cancellation is unchanged from that in a flash converter, and the associated speed-accuracy tradeoffs are still a problem.

3.3.3 Conclusions

In conclusion, subranging architecture is particularly suitable for low-cost video-rate applications due to its small area and adequate speed. Great progresses have been made recently in 10-bits video-rate converter for HDTV applications.[1] But three drawbacks make it unsuitable for applications that require higher resolutions. The first one is the lacking of a dedicated input S/H amplifier. This limited the achievable sampling jitter between the comparators to around 10 bit resolution at Nyquist frequency. The second one is the inherent difficulties to cancel com-

parator offset at video speed to better than 10 bit linearities. The third drawback is that the resistor string do not have the linearity required by a high-resolution converter. To solve this problem, laser trimming of the resistor is required, which is very expensive. Therefore, the subranging architecture is unsuitable for a 12-13 bits video-rate A/D converter.

3.4 Pipelined Architecture

As shown in the previous section, the 2-step conversion architecture can reduce the hardware while incurring only minor penalty in the conversion speed. But expanding this architecture to multistage will slow the conversion speed accordingly. One method to get around that is to add an interstage S/H amplifier between stages so that all the stages can work concurrently on samples or residues of different inputs; this approach is called pipelining. Pipelining eliminates the needs for the converter to wait for all the stages to finish their processing of the present input before another input can be sampled and processed. For a given resolution per stage, applying pipelining to the multistage architecture make the maximum conversion rate independent of the number of stages. Fig. 3.4 shows a block diagram of a pipelined A/D converter with k stages. The total number of bits resolved are

$$N = n_1 + \cdots + n_i + \cdots + n_k \qquad (3.4)$$

Each of the pipelined stages contains a S/H circuit, a low-resolution A/D converter, a low-resolution D/A converter, a subtractor, and an interstage gain amplifier. To begin a conversion, the input is sampled and held. The held input is then converted into a digital code by the first-stage A/D converter and back into an analog signal by the first-stage D/A converter. The D/A converter output is subtracted from the held input, producing a residue that is amplified and sent to the next stage, where this process is repeated. At any instant, while the first stage processes the current input sample, the second stage processes the amplified residue from the first stage of the previous input sample. Because sequential stages simultaneously work on residues from successively sampled inputs, the digital outputs from each stage correspond to input samples at different times. Digital latch arrays are needed to time align the outputs from different stages.
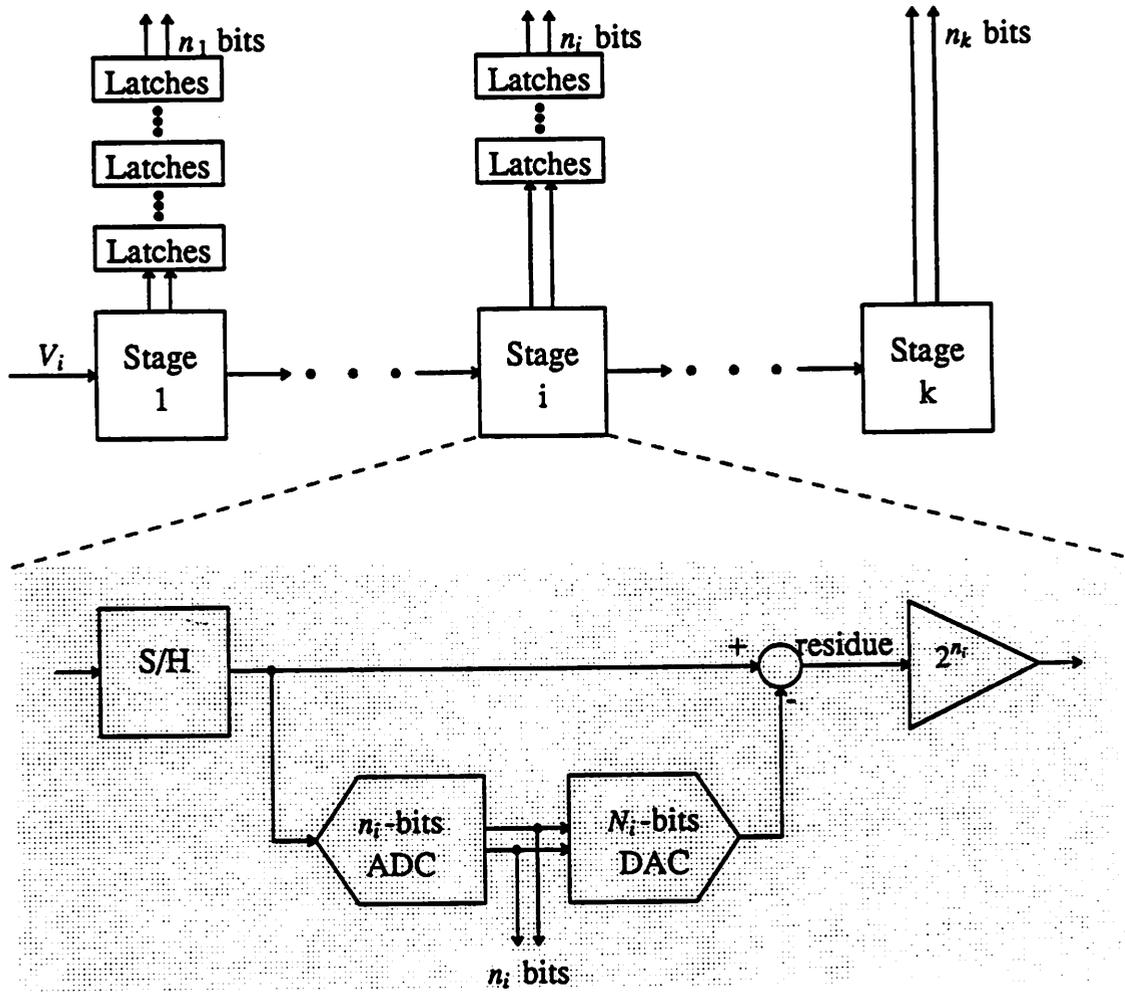
3.4.1 Advantages

Fig. 3.4 Pipelined A/D Converter

A primary advantage of the pipelined architecture is its high throughput rate. The high throughput rate of the pipelined architecture stems from concurrent operation of the stages. If the A/D subconversion and D/A subconversion are done with a flash converter, a pipelined architecture only needs two clock phases per conversion, the same as a flash architecture. However, the information transfer between the pipelined stage requires much higher accuracy than the 1-bit resolution in the flash architecture and the speed of the pipelined converter is slowed down accordingly. Although flash architectures make the fastest converter, for a given resolution per stages, pipelined architectures make the maximum conversion rate independent of the number of stages.

Another advantage of the pipelined architecture is its small area, power consumption and

input capacitance. The area of pipelined converter is small compared to those of flash converter because pipelined converter requires fewer components than flash converter. The area and power consumption of a pipelined converter are linearly related to the number of bits resolved, while the area and power consumption of a flash or a subranging converter are all exponentially related to the number of bits resolved. Therefore, pipelined architecture requires much less hardware than subranging or flash architectures for increased resolutions.

Other advantages stem from the use of S/H amplifiers to isolate the stages, First, the interstage gains from these amplifiers diminish the effects of nonidealities in all stages. For example, the effect of second stage nonlinearity is reduced by a factor of first stage gain. This allows the converter to use a digital correction technique with which nonlinearities in the A/D subconversions and offsets in both comparators and op amps have little effect on the overall linearity. The effect of nonidealities and correction techniques are discussed in Chapter 4. Second, because a S/H amplifier can also be used on the input of the A/D converter, pipelined architecture can accurately sample high-frequency input signals limited only by results in Chapter 2. This is a big advantages over flash and subranging converters especially for high-resolution applications.

3.4.2 Limitations

The major limitation of pipelined A/D converters is that they require the use of op amps to realize parasitic-insensitive S/H amplifiers to do analog subtraction and amplification at the sampling rate of A/D converter. The op amps limit the speed of the pipelined converters. To achieve video speed comfortably, a 1-1.5 μm CMOS technology is required.

Because interstage gain diminishes the effect of error sources in all stages after the first, and because digital error correction eliminates the effect of A/D subconverter nonlinearity, the D/A converter in the first stage and gain accuracy of the first interstage amplifier determine the linearity of the entire A/D converters. Such D/A converter and interstage amplifier can be implemented with switch capacitor amplifier for linearities in the 9-10 bits range. For integral linearity greater than 10 bits, the D/A converter and interstage amplifier requires either calibration or trimming.

3.4.3 Conclusions

Great progress has been made on the pipelined A/D converters. Both 1MHz 12 bit pipelined converter[10] and 20MHz 10 bit pipelined converter[11] have been reported. In conclusion, pipelined architectures show great potential to be used as 12-13 bits video-rate converters due to the following three reasons. First, the hardware cost of a pipelined converter is linearly proportional to the number of bits resolved. It is the most cost-effective approach to expand to high-resolution among the three architectures discussed in this chapter. Second, the use of input S/H amplifier eliminates the problem of sampling jitter between comparators in flash and subranging converters. This is particularly important for high-resolution A/D converter because the tolerance for the sampling jitter is tighter with increased resolution for a given input frequency and input amplitude. Third, only the first few stages need calibration or trimming because the interstage gain scales down the effect of the nonlinearity due to the following stages. This make the cost of calibration or trimming much more tolerable. Therefore, pipelined A/D converters demonstrate great potential to be used as high-resolution video-rate A/D converters.

CHAPTER 4

EFFECTS OF NONIDEALITIES IN PIPELINED ADC's
AND VARIOUS CORRECTION TECHNIQUES

4.1 Introduction

As shown in the previous chapter, pipelined architectures have great potential for high-resolution applications. In this chapter, we will discuss the effects of nonidealities in pipelined A/D converters. To achieve high-resolution, various correction techniques and speed-accuracy tradeoff will also be discussed.
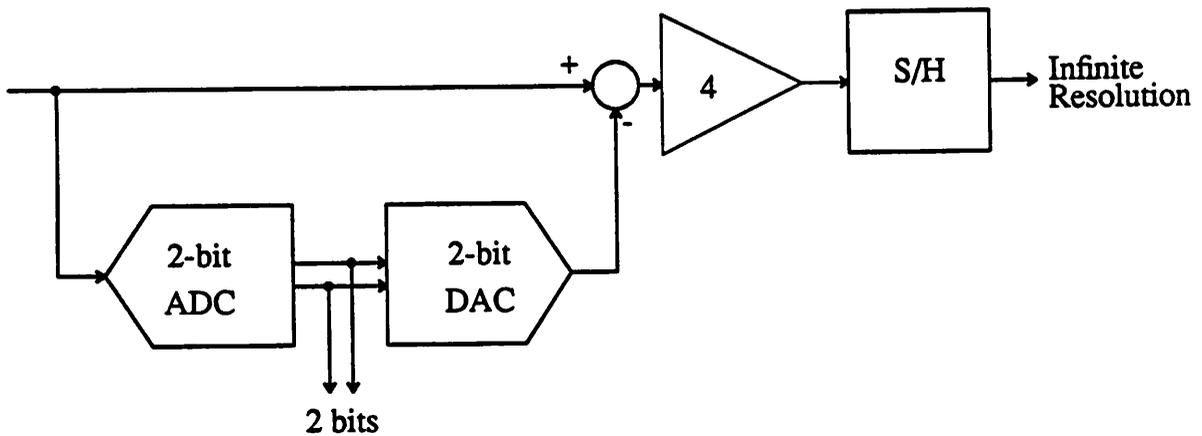
4.2 Effects of Nonidealities

Fig. 4.1 Block Diagram of a 2-bit Pipelined Stage

To illustrate the effects of nonidealities have on the pipelined A/D converter, we use a 2-bit per stage as an example and assume the following stages have infinite resolution. Fig. 4.1 shows a block diagram of a 2-bit pipelined stage. It consists of a 2-bit A/D subconverter, a 2-bit D/A subconverter, a gain of 4 interstage amplifier and a S/H circuit. Fig. 4.2 shows the input-output

relationship and overall A/D conversion characteristic for an ideal 2-bit stage. The A/D subconverter decision points are 0 and $\pm\frac{1}{2}V_{ref}$ and the corresponding D/A subconverter output levels are $\pm\frac{1}{4}V_{ref}$ and $\pm\frac{3}{4}V_{ref}$, respectively. The gain of the interstage amplifier is 4. The transition position is determined by the A/D subconverter decision points, while the magnitude of the transition at each code boundary is determined by the D/A subconverter and interstage amplifier.
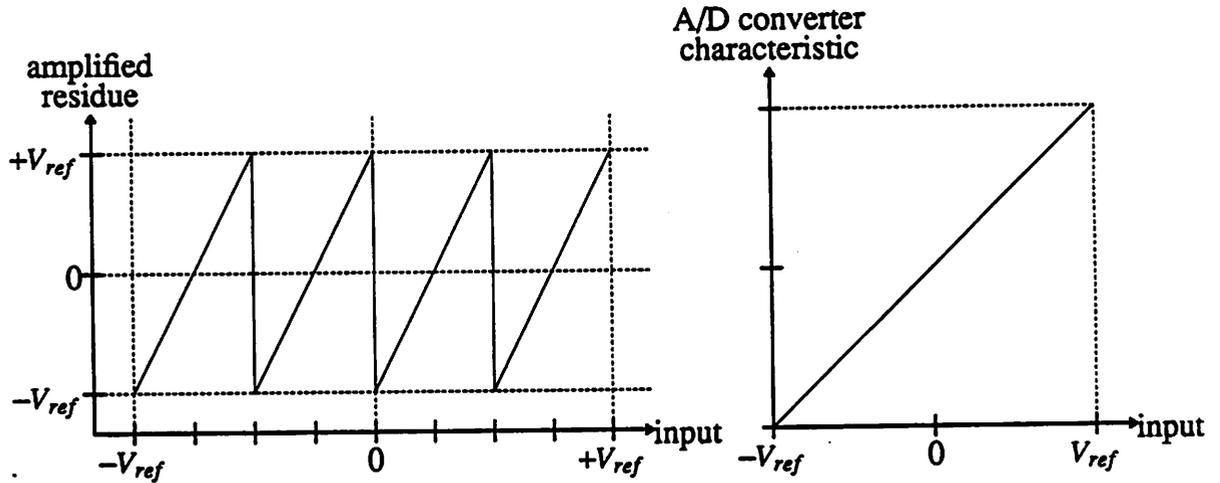
Fig. 4.2 Input-Output Relationship of an Ideal 2-bit Pipelined Stage

In practice, there are errors associated with each block. Their effects on the linearity of the A/D converter is discussed in the following sections. These errors include:

(1) nonlinearity in A/D subconverter;

(2) offset, nonlinearity and gain error in D/A subconverter;

(3) offset and nonlinearity in subtractor;

(4) offset, nonlinearity and gain error in interstage amplifier;

(5) offset, nonlinearity and gain error in S/H circuit.

Instead of discussing the errors individually, we group the errors according to their effects on the input-output relationship of a pipelined stage. There are four categorys of nonidealities, namely, (1)offset, (2)nonideal transition position, (3)nonideal transition magnitude, and (4)nonlinearity. These will be discussed in section 4.2.1 through 4.2.4, respectively. In each case, we consider one nonideality at a time and assume the rest are ideal. The discussion will be limited to the block diagram level, details on the circuit level is described in the next chapter.

4.2.1 Offset in a Pipelined Stage

An offset in a pipelined stage shifts the input-output curve up or down with the result that some parts of the curve are outside of the conversion range of the following stage. This affects the overall A/D conversion characteristic and causes positive DNL and negative DNL. This input-output relationship and overall A/D conversion characteristic are shown in Fig. 4.3, where the solid lines are the real curve and the dashed lines are the ideal curve. This offset is a result of offsets in D/A subconverter, subtractor, interstage amplifier and S/H circuit.
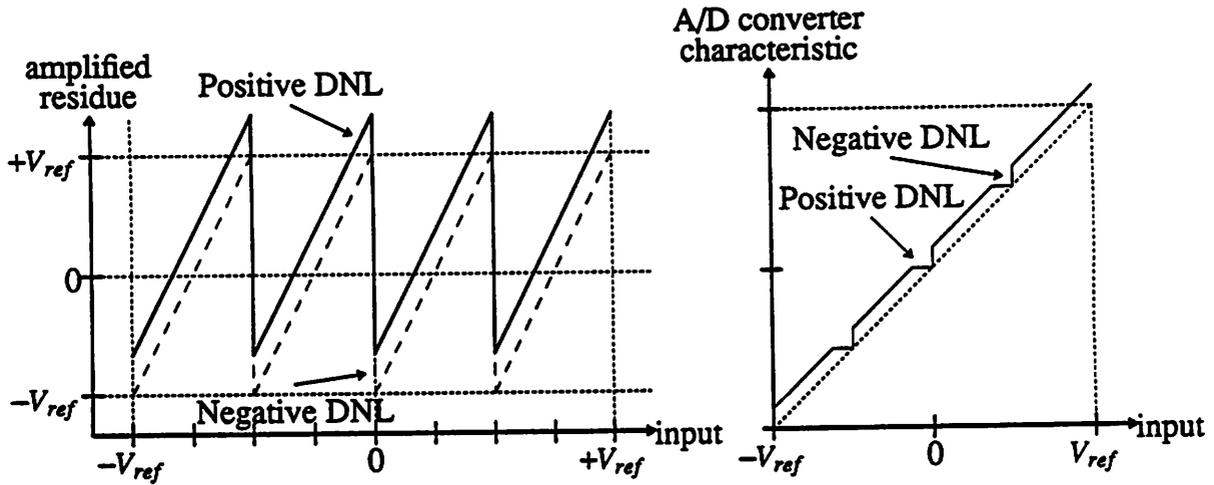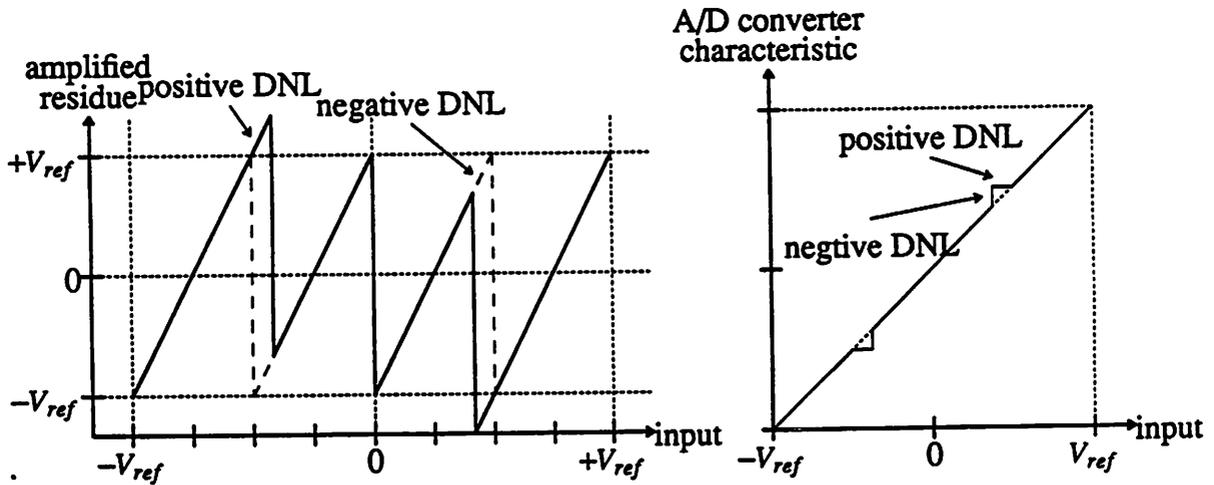
Fig. 4.3 Offset in a Pipelined Stage

Fig. 4.4 Nonideal Transition Position in a Pipelined Stage

4.2.2 Nonideal Transition Position in a Pipelined Stage

The shifting of transition position makes the input-output curve lie outside of the conversion range of the following stage. This results in positive DNL and negative DNL in the overall A/D conversion characteristic as shown in Fig. 4.4. The transition position of a pipelined stage is determined by the decision point of the A/D subconverter. Therefore, any nonlinearity in the A/D subconverter introduces shifting of the transition position.
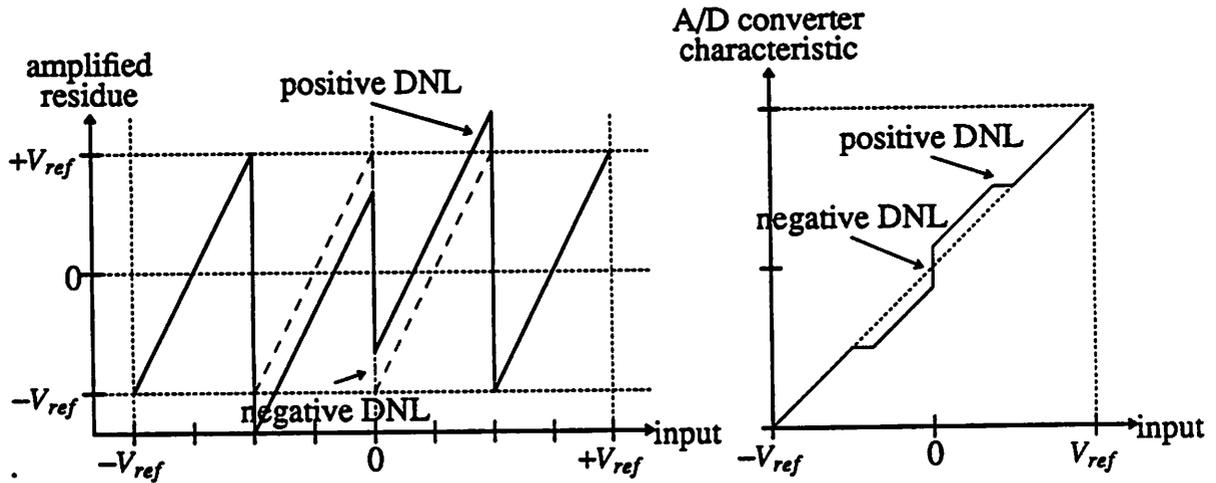
Fig. 4.5 Transition Magnitude Mismatch in a Pipelined Stage

4.2.3. Nonideal Transition Magnitude in a Pipeline Stage

The magnitude of the transition at the code boundary may not be ideal. There are two type of errors in nonideal transition magnitude. The first one is the mismatch of the transition magnitude in the different code boundary. Due to this mismatch, the output does not match the conversion range of the following stage. Therefore positive DNL and negative DNL are presented in the overall A/D conversion characteristic. This mismatch of the transition magnitude is a result of nonlinearity in the D/A subconverter. Fig. 4.5 shows the effect of this error on the input-output relationship and overall A/D conversion characteristic.

The second error is too large or too small a transition magnitude, i.e. due to a gain error. Therefore, the output is either larger or smaller than the conversion range of the following stage depend on whether the gain is larger or smaller respectively than the ideal gain. This results in positive DNL in the case of positive gain error and negative DNL in the case of negative gain error. This gain error is a result of gain errors in D/A subconverter, interstage amplifier and S/H circuit. Fig. 4.6 shows the effect of the gain error on the input-output relationship and overall A/D
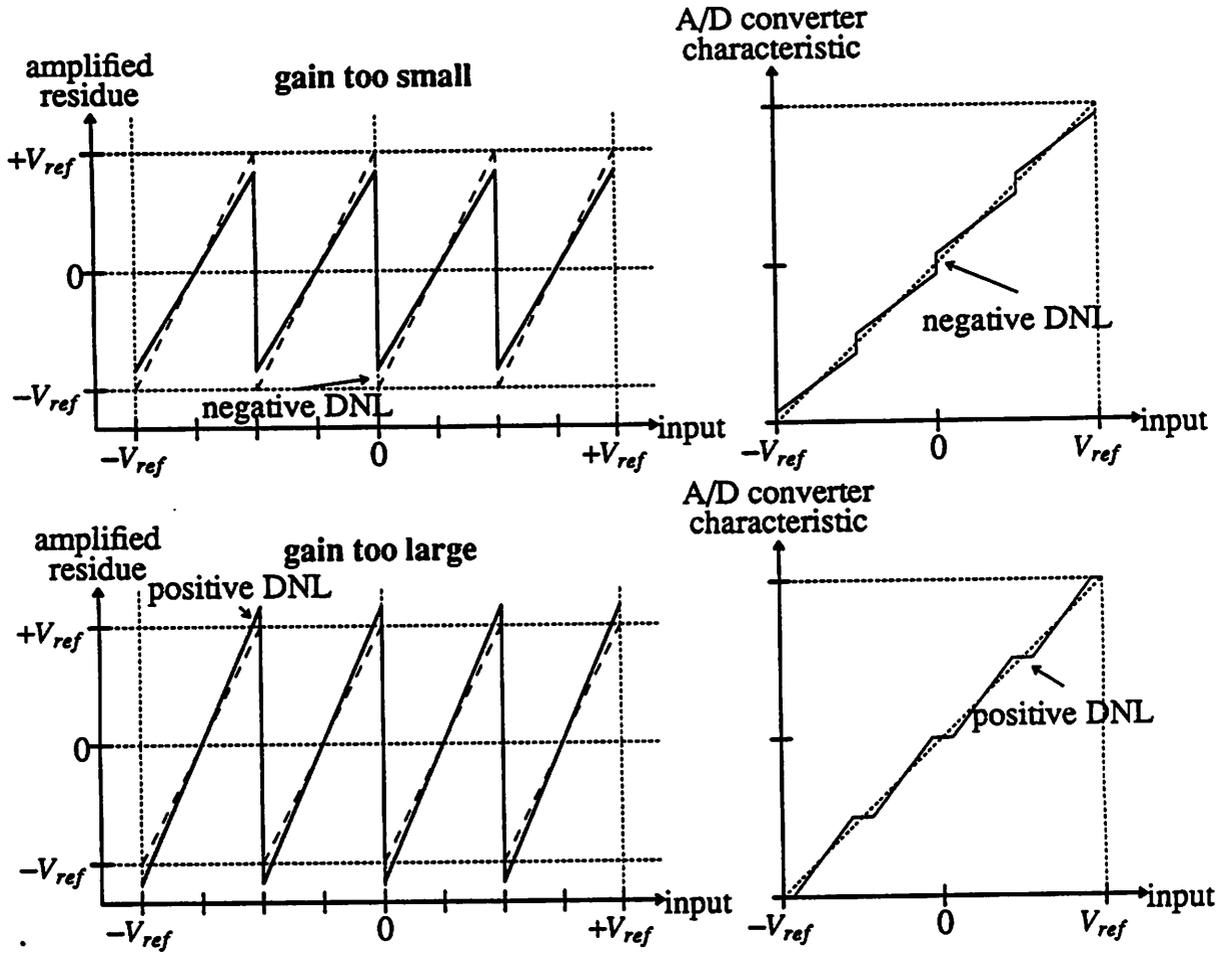
Fig. 4.6 Transition Magnitude Gain Error in a Pipelined Stage
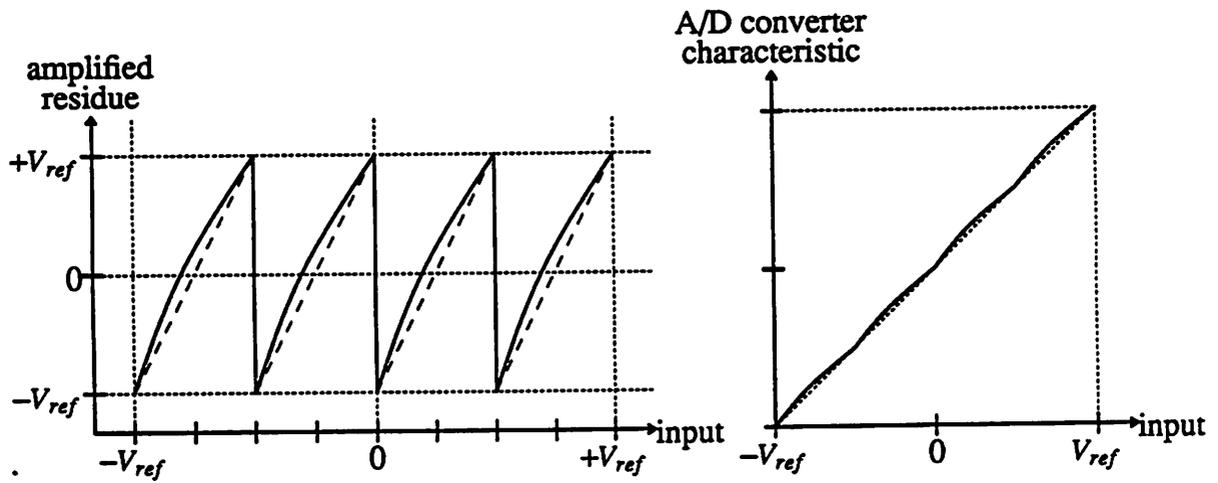
conversion characteristic.

Fig. 4.7 Nonlinearity in a Pipelined Stage

4.2.4 Nonlinearity

Nonlinearity introduce curvature to the output and degrades overall converter linearities. Nonlinearity in a pipelined stage results from nonlinear input-output relation of the interstage amplifier and S/H circuit. Fig. 4.7 shows their effects on the input-output relationship and overall A/D conversion characteristic.

4.2.5 Op Amp Settling Time

In addition to the nonidealities mentioned above, the performance of the pipelined A/D converter is also limited by the settling time of the interstage amplifier. The speed of a pipelined A/D converter is determined by how fast the analog signal can be generated and transferred at each stage. The speed of generating and transferring the analog signal is solely determined by the settling time behavior of the op amp used.

4.3 Correction Techniques

To overcome some of the nonidealities mentioned in the previous section, three techniques are discussed in this section. They are capable of substantially reducing the offset, the nonideal transition position and the nonideal transition magnitude errors, leaving only the nonlinearity. Since nonlinearity in interstage amplifier and S/H circuit is a characteristic of the particular circuit used, care must be taken in designing the interstage amplifier and S/H circuit.

4.3.1 Digital Error Correction

Examining Fig. 4.4, it can be seen that the information contained in the input has not been lost. The problem is that the shifting of the transition position makes the output incompatible with the conversion range of the following stage. If, however, the conversion range of the following stage can be expanded to avoid overflow, the positive DNL and negative DNL can be recover digitally with simple logic.[9] This is shown in Fig. 4.8; whenever the following stage detects an overflow, correction can be made to the digital output of the previous stage to correct the shifting of the transition position. The solid line shows the characteristic before digital error correction,

while the dashed line shows the resulting characteristic after digital error correction. Since it is not practical to expand the conversion range of the following stage, the interstage gain is reduced by half instead to avoid overflow. This gives the digital error correction an ability to accommodate $\pm\frac{1}{2}$ LSB nonlinearity on the 2-bit A/D subconverter, but at the expense of losing one bit per stage to the redundancy of digital error correction techniques.
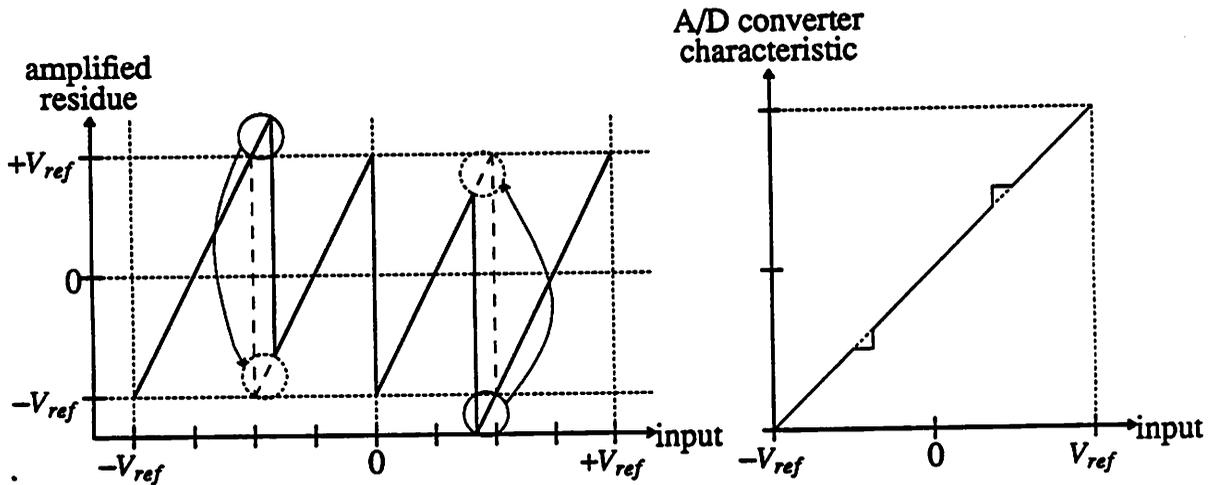

Fig. 4.8 Principle of Digital Error Correction

It may be shown that the logic function needed to perform the correction is simple increment or decrement of the digital output of the previous stage based on the positive or negative overflow of the following stage. Next, we will examine the effects of digital error correction on the other nonidealities. With digital error correction, the offset in a pipelined stage becomes input referred and does not introduce positive DNL or negative DNL. This property is illustrated in Fig. 4.9, where the corrected overall A/D conversion characteristic shows only offset without any nonlinearity.

Digital error correction does influence the effect of nonideal transition magnitude have on the overall A/D conversion characteristic. This is shown in Fig. 4.10 and Fig. 4.11 for the case of transition magnitude mismatch and transition magnitude gain error, respectively. Self-calibration techniques can be used to overcome the nonideal transition magnitude as discussed in later sections. In short, digital error correction can eliminate the effects of nonlinear A/D subconverter on the overall A/D conversion characteristic. It can also remove the effect of the offset in a pipelined stage on the linearity of the overall A/D conversion characteristic. In conclusion, digital error correction is a very powerful technique capable of correcting some of the nonidealities
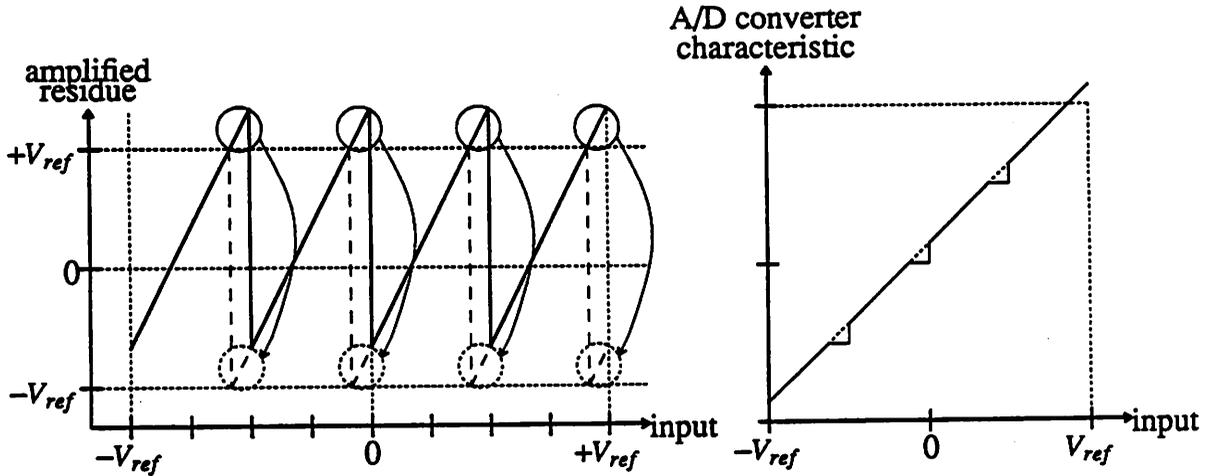
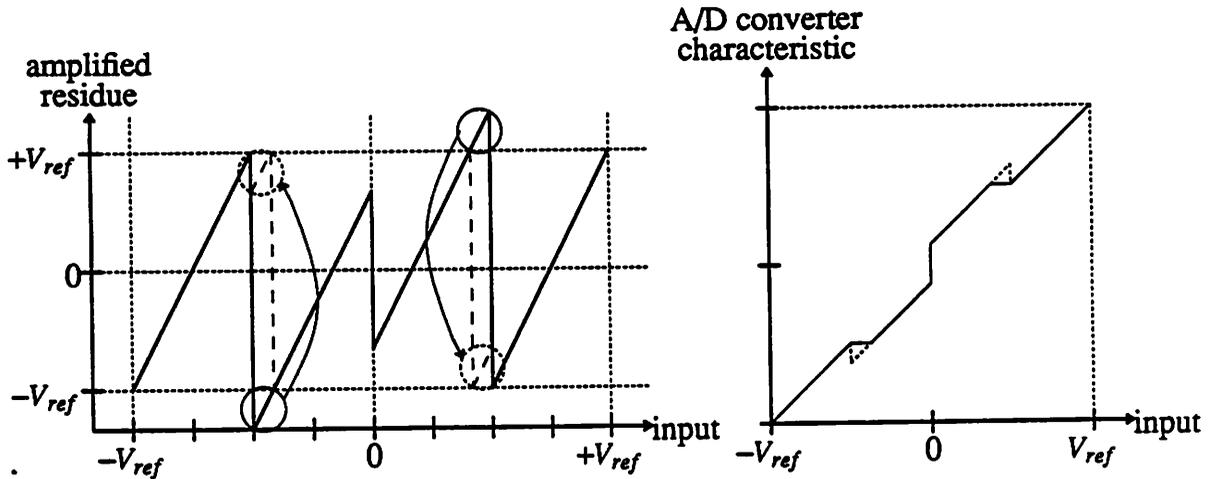Fig. 4.9 Offset in a Pipelined Stage with Digital Error Correction

Fig. 4.10 Transition Magnitude Mismatch in a Pipelined Stage with Digital Error Correction encountered in a pipelined A/D converter.

4.3.2 Offset Cancellation Techniques

Although digital error correction removes the effects of offset error on the linearity of the overall A/D conversion characteristic, it nevertheless leaves behind an input-referred offset. To remove this offset, offset cancellation techniques can be used. In order to illustrate the offset cancellation techniques in this section and the self calibration techniques in the following section, we need to consider the details of the actual implementation of a switched-capacitor(S/C) pipeline stage. Fig. 4.12 shows the actual implementation of a S/C 2-bit pipeline stage. It consists of a 2-bit A/D subconverter, four sampling capacitors $C_{S_1} - C_{S_4}$, one integrating capacitor C_I, an op amp
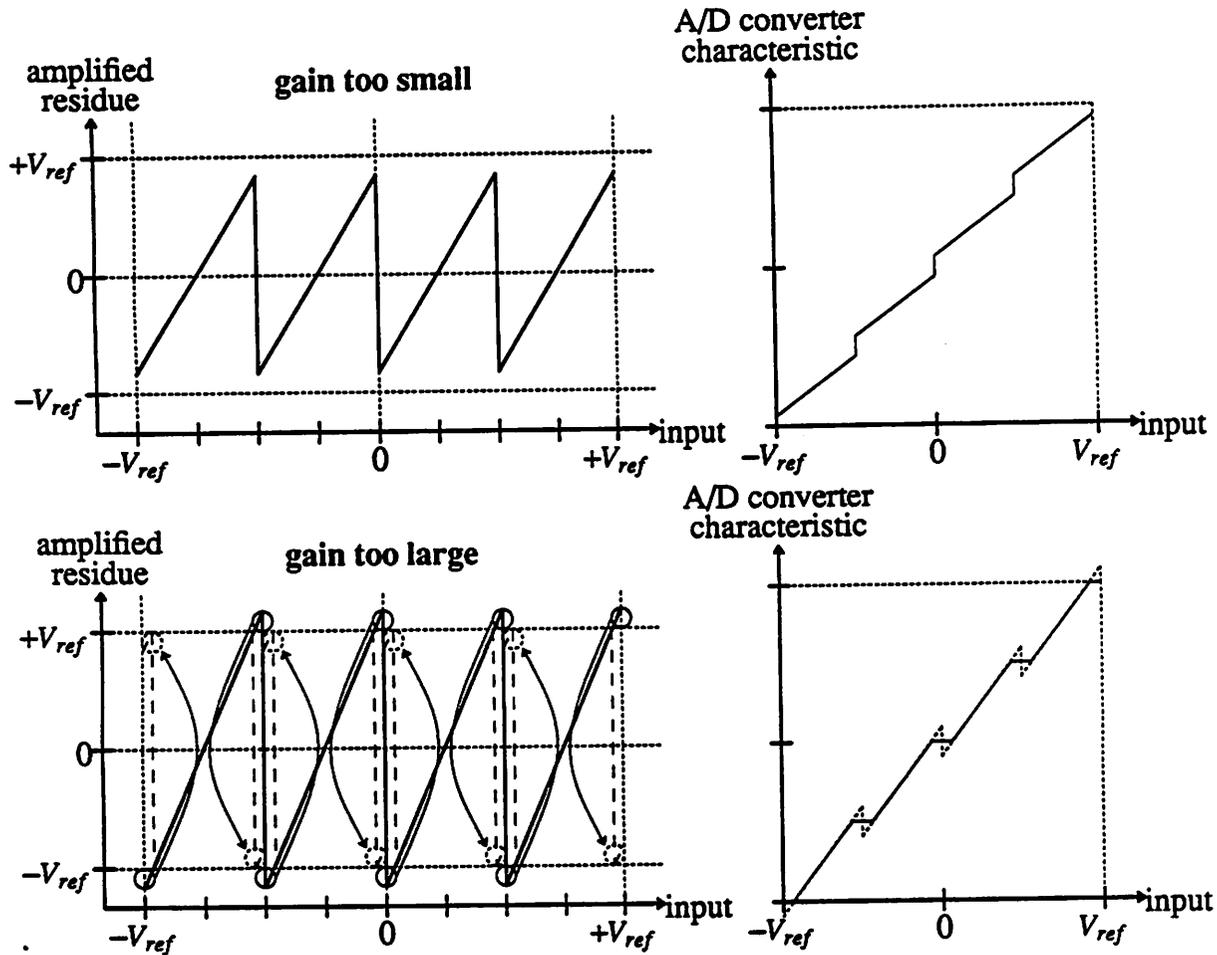
Fig. 4.11 Transition Magnitude Gain Error in a Pipelined Stage with Digital Error Correction

and some switch networks. Two non-overlapping clocks are required to drive the switch networks. On phase ϕ_1, the sampling capacitors $C_{S_1} - C_{S_4}$ are connected to the input, while the sampling switch M_1 is closed. The voltage on the sampling capacitors tracks the input voltage. At the same time, the integrating capacitor C_I is connected to ground and is reset and the A/D subconverter converts the input into digital code. At the end of ϕ_1, sampling switch opens and the input is sampled on the four sampling capacitors. On phase ϕ_2, the loop around the op amp is closed and the sampling capacitors are connected to ground or V_{ref} depending on the A/D subconverter output digital code. The charge sampled on the sampling capacitors which represented the difference between the analog input and its quantized value, i.e. the residue of this stage is then transferred to the integrating capacitor, Thus interstage amplification, D/A subconversion and subtraction are performed.
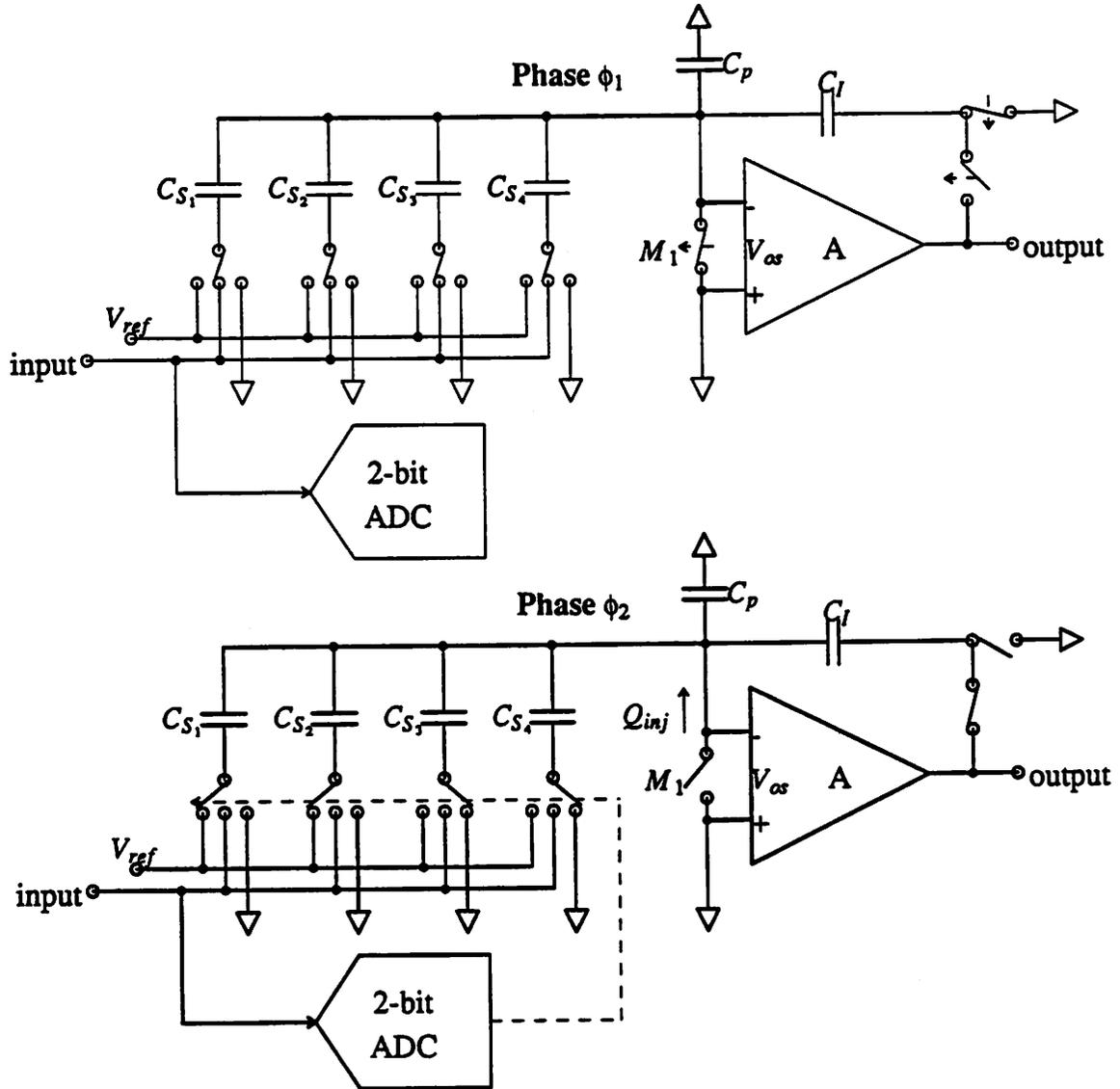
Fig. 4.12 Implementation of a S/C 2-bit Pipelined Stage

From Fig. 4.12, it can be shown that the offset of this pipelined stage comes from the offset of op amp and the charge injection Q_{inj} of the sampling switch M_1. These can be cancelled by using offset cancellation techniques described below. This technique has been used extensively to cancel the offset of op amp in precision applications.[12] To cancel the offset, the op amp is composed of one main op amp and one auxiliary op amp, both are output transconductance amplifier(OTA) as shown in Fig. 4.13. Between the ϕ_1 and ϕ_2, an extra phase is added to cancel the offset. The offset resulting from the offset of the op amp and the charge injection Q_{inj} of the sampling switch M_1 is present in the main op amp input at the end of ϕ_1. To cancel this offset, the

Fig. 4.13 Principle of Offset Cancellation Techniques

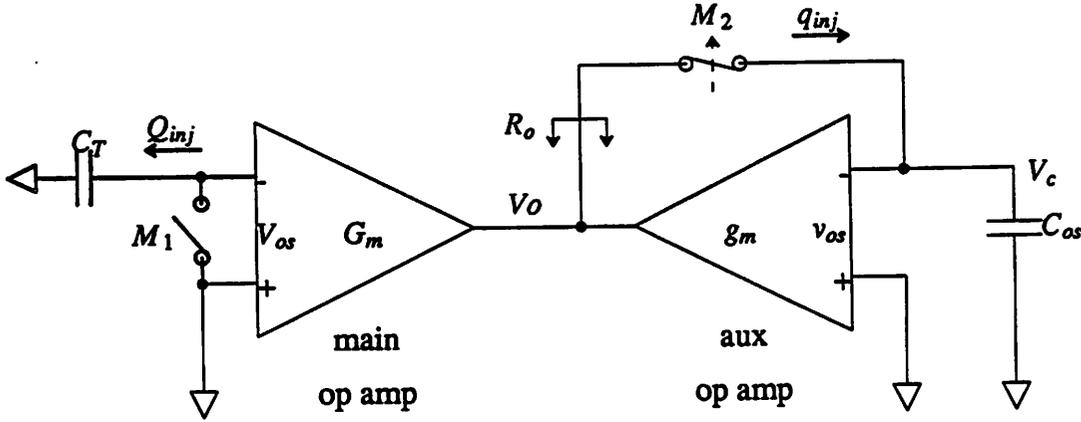loop around the auxiliary op amp is closed, and the offset in the main op amp is now sampled at the auxiliary op amp input and stored by the capacitor C_{os}. By making the transconductance of the auxiliary op amp smaller than the main op amp, a scaled up offset voltage is stored on capacitor C_{os}. This make the stored offset voltage less sensitive to the charge injection error of the shorting switch M_2 between the input and output of the auxiliary op amp.

Assume the main op amp has a transconductance G_m, a combined output resistance R_o and an input offset voltage V_{os}, while the auxiliary op amp has a transconductance g_m and an input offset voltage v_{os}. Also assume the charge injection error voltage of the sampling switch M_1 is V_{inj} and the charge injection error voltage of the shorting switch M_2 is v_{inj}, where $V_{inj} = \frac{Q_{inj}}{C_T}$ and $v_{inj} = \frac{q_{inj}}{C_{os}}$. When the loop around the auxiliary op amp is closed, the voltage Vo at the op amp output can be calculated as follow

$$Vo = \left[G_m(V_{os} - V_{inj}) + g_m(v_{os} - Vo) \right] R_o \tag{4.1}$$

Therefore, the voltage at the offset-cancellation capacitor C_{os} is

$$V_c = Vo = \frac{G_m R_o}{(1 + g_m R_o)}(V_{os} - V_{inj}) + \frac{g_m R_o}{(1 + g_m R_o)} v_{os} \tag{4.2}$$

After the shorting switch M_2 turns off, the voltage sampled on the offset-cancellation capacitor is

$$V_c' = V_c + v_{inj}$$

$$= V_{inj} + \frac{G_m R_o}{(1+g_m R_o)}(V_{os}-V_{inj}) + \frac{g_m R_o}{(1+g_m R_o)}V_{os} \qquad (4.3)$$

From Eq. (4.1), the output voltage becomes

$$Vo = \left[G_m(V_{os}-V_{inj})+g_m(v_{os}-V_c') \right] R_o \qquad (4.4)$$

Thus, the final input-referred uncancelled offset voltage V_{res} is

$$V_{res} = \frac{Vo}{G_m R_o} = (V_{os}-V_{inj})+\frac{g_m}{G_m}(v_{os}-V_c')$$

$$= \frac{1}{1+g_m R_o}(V_{os}-V_{inj}+\frac{g_m}{G_m}v_{os}) + \frac{g_m}{G_m}v_{inj} \qquad (4.5)$$

From Eq. (4.5), both the V_{os} and V_{inj} are reduced by a factor of $1+g_m R_o$. The largest contribution in the Eq. (4.5) is usually the last term $\frac{g_m}{G_m}v_{inj}$. This term can be reduced by using larger offset-cancellation capacitor C_{os}, smaller shorting switch M_2 and smaller $\frac{g_m}{G_m}$. This technique has been shown to be capable of cancelling offset down to less than 0.1 mV.[12]

4.3.3 Self-Calibration Technique

The nonideal transition magnitude in the pipelined stages results from the nonlinearity in the D/A subconverter and the gain error in the interstage amplifier. From Fig. 4.12, it is obvious that the nonlinearity in D/A subconverter is determined by the matching of the four sampling capacitors C_{S_1} - C_{S_4}, while the interstage gain is determined by the total sampling capacitors-integrating capacitor and a gain correction factor due to the finite gain of the op amp. Consider a more general case, where the interstage gain is 2^M, the requirements to make the transition magnitude ideal are:

(1) $C_{S_1} = C_{S_2} = \cdots = C_{S_i}$, where $i = 2^M$

(2) $\dfrac{\sum\limits_{i=1}^{2^M} C_{S_i}}{C_I(1+\frac{C_T}{C_I A})} = 2^M$, where $C_T=(\sum\limits_{i=1}^{2^M} C_{S_i})+C_I+C_p$

To achieve N-bit linearity, the input-output relationship in a pipelined stage should not differ from the ideal curve by more than $\frac{1}{2}$ LSB. Therefore, the matching between C_{S_i}, i=1, ...

$,2^M$ must be better than $\frac{1}{2^{N+1}}$. Assume the resolution of the next stage is K bit, the percentage gain error must be no more than $\frac{1}{2^K}$. This tolerance of the above two requirements is represented in Eq. (4.6) and Eq. (4.7), respectively.

$$\frac{\left| C_{S_i} - C_S \right|}{C_S} < \frac{1}{2^{N+1}} \tag{4.6}$$

where $i = 1, \ldots, 2^M$ and $C_S = \frac{\sum_{i=1}^{2^M} C_{S_i}}{2^M}$

$$\left| \frac{\sum_{i=1}^{2^M} C_{S_i}}{2^M C_I (1 + \frac{C_T}{C_I A})} - 1 \right| < \frac{1}{2^K} \tag{4.7}$$

where A is the open loop gain of the op amp and C_{S_i}, C_I, C_p are sampling capacitors, integrating capacitor and parasitic capacitor, respectively and $C_T = (\sum_{i=1}^{2^M} C_{S_i}) + C_I + C_p$.

Self-calibration techniques can be used to calibrate the sampling capacitors to meet the above requirements. This technique uses a small trim capacitor attached to each of the 2^M sampling capacitors to adjust the sampling capacitor to meet the above requirements. The calibration is done by comparing the sampling capacitors with the integrating capacitor one by one and searching for the setting on the trim capacitor that can meet the above two requirements. Fig. 4.14 shows a calibration step in the self-calibration procedure. Its principle is similar to Harry Lee's self-calibration technique.[13] To begin the calibration of C_{S_1}, C_{S_1} is connected to the reference voltage, while the other sampling capacitors are grounded. The reference voltage are sampled on the C_{S_1} along with the charge injection error from the sampling switch M_1, while the integrating capacitor C_I is connected to the ground and discharged. Next, the offset cancellation technique is used to cancel the charge injection error and op amp offset. After the offset and charge injection error are cancelled, the input connection to the C_{S_1} and C_I are interchanged, C_{S_1} is now connected to the ground and C_I is now connected to the V_{ref}. If C_{S_1} does not match C_I, an error voltage will be generated at the op amp summing node. The open-loop offset-cancelled op amp is used as a high gain preamplifier for the comparator. In order to take into account of the

finite op amp gain, the output of the op amp is compared with V_{ref} instead of ground. If the comparator output is high, C_{S_1} is larger than the ideal value, we can adjust the setting on the trim capacitor and repeat this calibration step until the comparator output changes state. This procedure is repeated for the other three sampling capacitors. When it is done, both the nonlinearity in D/A subconverter and gain error in interstage amplifier are eliminated.
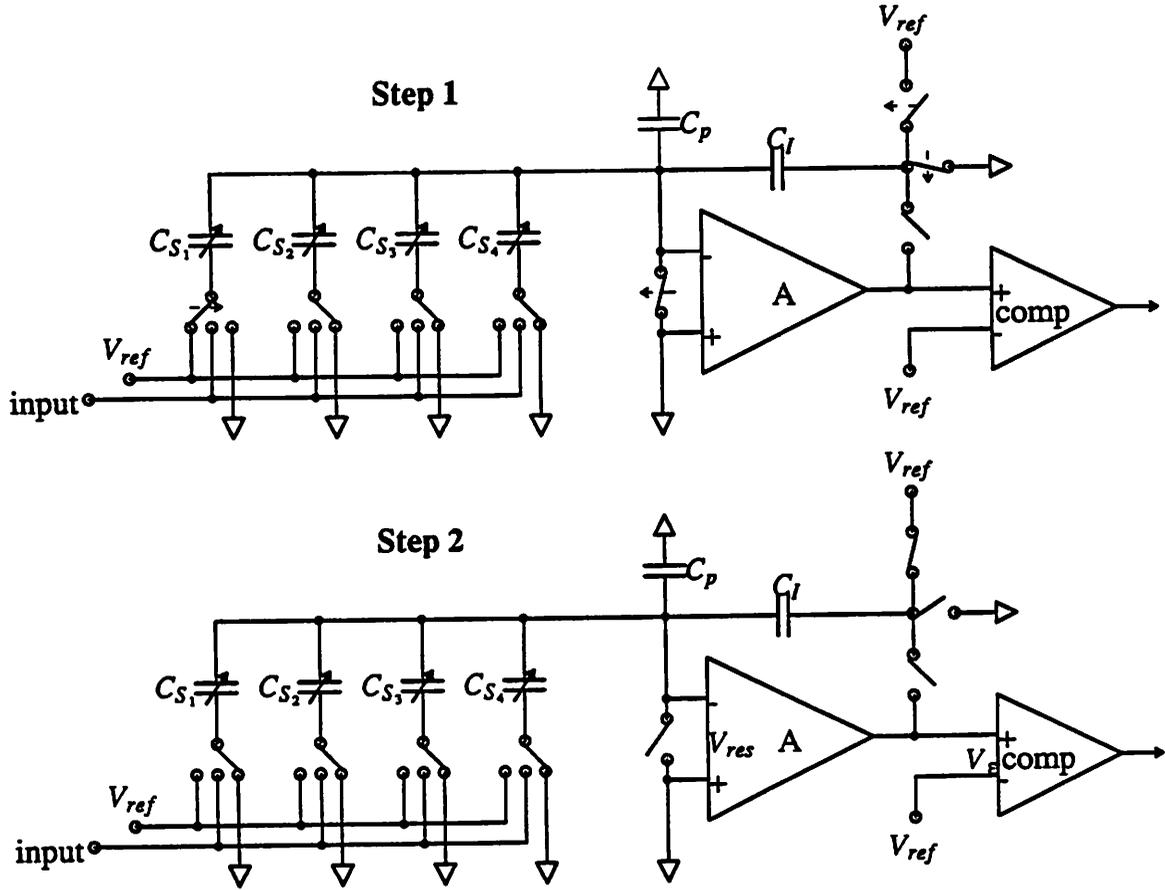

Fig. 4.14 Principle of Self-Calibration Technique

Detailed analysis of the calibration requirements is given below. We assume the effective residue offset voltage after the offset cancellation is V_{res}, the offset of the comparator is V_ε, the open loop gain of the op amp is A, the input resolution is N bit, the output resolution is K bit and the interstage gain is 2^M. From Fig. 4.14, the charge conservation equation can be written as

$$C_{S_1}(V_{ref}-\frac{V_{ref}+V_\varepsilon}{A}-V_{res}) - (\sum_{i=2}^{2^M}C_{S_i}+C_p)(\frac{V_{ref}+V_\varepsilon}{A}+V_{res})$$

$$= C_I(V_{ref}+\frac{V_{ref}+V_\varepsilon}{A}+V_{res}) \qquad (4.8)$$

Therefore, C_{S_1} can be represented as

$$C_{S_1} = C_I \left[1 + \frac{C_T}{C_I A} \right] + C_T \left(\frac{V_{res}}{V_{ref}} + \frac{V_\varepsilon}{V_{ref} A} \right) \tag{4.9}$$

Assume the maximum step size of the trim capacitor is ΔC_{S_i} for C_{S_i}, where $i = 1, \dots, 2^M$

Eq. (4.7) can be rewritten as

$$\frac{\Delta C_{S_i}}{C_S} < \frac{1}{2^N} \tag{4.10}$$

where $i = 1, \dots, 2^M$.

and from Eq. (4.9), Eq. (4.8) can be rewritten as

$$\left| \frac{\sum_{i=1}^{2^M} \Delta C_{S_i} + 2^M C_T \left(\frac{V_{res}}{V_{ref}} + \frac{V_\varepsilon}{V_{ref} A} \right)}{2^M C_I (1 + \frac{C_T}{C_I A})} \right| < \frac{1}{2^K} \tag{4.11}$$

From Eq. (4.10), we have

$$\left| \frac{\sum_{i=1}^{2^M} \Delta C_{S_i}}{2^M C_I (1 + \frac{C_T}{C_I A})} \right| < \frac{2^M}{2^M 2^N} = \frac{1}{2^N} \tag{4.12}$$

From Eq. (4.12), a sufficient condition to satisfy Eq (4.10) can be obtained

$$\left| \frac{C_T \left(\frac{V_{res}}{V_{ref}} + \frac{V_\varepsilon}{V_{ref} A} \right)}{C_I (1 + \frac{C_T}{C_I A})} \right| < \frac{1}{2^K} - \frac{1}{2^N} = \frac{2^{N-K} - 1}{2^N} \tag{4.13}$$

Eq. (4.10) and Eq. (4.13) give a sufficient condition to achieve N-bit linearity. In order to reliably calibrate a N-bit A/D converter, the maximum step size of the trim capacitor must be smaller than

1 LSB and the error term $\dfrac{C_T \left(\frac{V_{res}}{V_{ref}} + \frac{V_\varepsilon}{V_{ref} A} \right)}{C_I (1 + \frac{C_T}{C_I A})}$ resulting from the circuit imperfection must be

smaller than $2^{N-K} - 1$ LSB. This put a stringent requirement on the residue offset voltage V_{res}. Care must be taken in designing the offset cancellation circuit to meet the above requirements.

Direct implementation of the trim capacitor by attaching a small capacitor to the sampling capacitor is impractical, since the maximum allowable step size is too small to implement. For example, a 12-bit A/D converter with 1 pF integrating capacitor requires a maximum capacitor step size of 0.25 fF, which is too small to lay out reliably. To overcome this difficulty, a capacitor divider array is used instead. A generalized configuration is shown in Fig. 4.15, which use a T network to divide the capacitance to a sufficient small value. Care must be taken in designing such a trim capacitor array to avoid large gaps in the trimming range. In short, the maximum step size of trimming capacitor must be controlled to meet the requirement of Eq. (4.10). This can be achieved by introducing redundancy which overlaps the trimming ranges at major code transitions in order to avoid large gaps in the capacitor trimming range. This redundancy results in non-monotonic characteristic of the trimming capacitor. Although this does not affect the ability of self-calibration, it does rule out the use of successive approximation search algorithm in the calibration procedure. A ramp search algorithm is used instead.
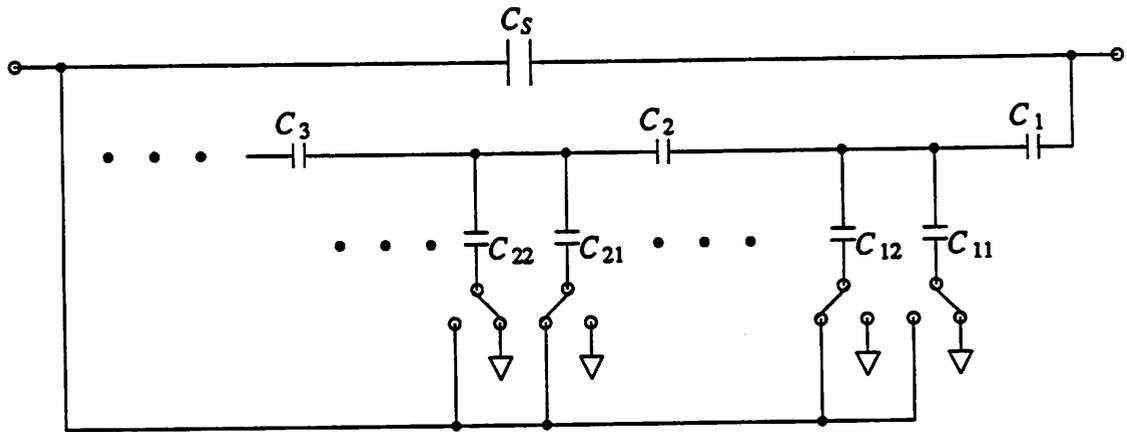
Fig. 4.15 A Generalized Capacitor Array

All self-calibration techniques suffer from the degradation of the accuracy due to the drifting of critical parameters with time. However, We can take advantage of the sporadic nature of the video signal by performing self-calibration not only when power up but also in interframe period. Since the calibration is updated from time to time, the concern for drift due to the temperature and supply variations is eliminated.

4.3.4 Speed-Accuracy Tradeoff

As mentioned before, the gain of the op amp limits the performance of the pipelined A/D converter. To achieve higher resolution, the gain of the op amp also needs to be higher. However, a higher gain requirement on the op amp may require that long channel devices be used in the op amp thus causing the bandwidth of the op amp to decrease and the settling time to increase. This becomes a fundamental limit on the performance of the pipelined A/D converter. A simple example is used to illustrate this speed-accuracy tradeoff.

Assume a simple cascode gain stage is used as the op amp for interstage amplifier, then the open-loop op amp gain A can be approximated as [7]

$$A = (G_m R_o)^2 = \left[\frac{2V_A}{\Delta V}\right]^2 \tag{4.14}$$

where V_A is the Early voltage and $\Delta V = V_{gs} - V_T$ is the gate overdrive. Since the V_{ds} bias and ΔV are limited by the supply voltage and output voltage swing, we make an assumption that V_{ds} is constant and $\Delta V < \Delta V_{max}$ to ensure a reasonable output swing. In general, V_A is not strongly dependent on the technology because V_A determines the gain of a digital gate and is usually kept constant in any technology. Define $A_{min} = \left[\frac{2V_A}{\Delta V_{max}}\right]^2$ as the achievable open-loop gain for cascode stage biased at ΔV_{max}. Since the open-loop op amp gain required for N-bit resolution must be better than 2^N, if $A_{min} < 2^N$ a ΔV smaller than ΔV_{max} is required to satisfy the gain requirement. This degrades the achievable conversion rate and the accuracy requirement can be related to the achievable conversion speed as follow. Since

$$A = A_{min}\left[\frac{\Delta V_{max}}{\Delta V}\right]^2 > 2^N \tag{4.15}$$

we have

$$\frac{\Delta V_{max}}{\Delta V} > \sqrt{\frac{2^N}{A_{min}}} \tag{4.16}$$

Also the absolute maximum useful gain bandwidth of an op amp is limited by its transition frequency f_T and can be expressed as

$$f_T = f_{T_{max}}\frac{\Delta V}{\Delta V_{max}} < f_{T_{max}}\sqrt{\frac{A_{min}}{2^N}} \tag{4.17}$$

where $f_{T_{max}}$ is the usable transition, i.e. unity-gain, frequency of the transistor biased at ΔV_{max}. This transition frequency $f_{T_{max}}$ is also dependent on the technology used. The settling time for a closed-loop gain A_{cl}, where $A_{cl} \geq 2$, can then be expressed as

$$T_{settle} = \frac{A_{cl}}{2\pi f_2}(N+1)\ln 2 > \frac{A_{cl}}{2\pi f_{T_{max}}}\sqrt{\frac{2^N}{A_{min}}}(N+1)\ln 2 \tag{4.18}$$

Therefore, the achievable conversion rate f_{BW} for a N-bit pipelined A/D converter with interstage gain A_{cl} is

$$f_{BW} \approx \frac{1}{2T_{settle}} \approx \sqrt{\frac{A_{min}}{2^N}}\frac{\pi f_{T_{max}}}{A_{cl}(N+1)\ln 2} \tag{4.19}$$

Usually A_{min} is about 200 for minimum devices biased at $\Delta V_{max} = 0.3V$ and $V_{ds} = 0.5V$ regardless of technology. From Eq. (4.19), the achievable conversion rate decreases with higher resolution and increases with scaled technology. Fig. 4.16 shows the achievable conversion rate vs. accuracy with interstage gain equal to two for 3μm, 2μm and 1μm CMOS technology. Also in this graph is the achieved performance of some reported works [1,9]. Fig. 4.16 is based on a simple cascode op amp structure, more exotic gain boosting methods may be able to surpass these limits.

4.4 Conclusions

In conclusion, with the help of digital error correction, offset cancellation techniques and self-calibration techniques, most nonidealities in a pipelined A/D converter can be eliminated. A high-resolution A/D converter at video-speed is feasible in CMOS technology. However, an inherent tradeoff between the speed and accuracy exists and a compromise must be obtained between the speed and accuracy. Chapter 5 describes the implementation of a 13-bit pipelined A/D converter prototype in 3 μm CMOS technology.
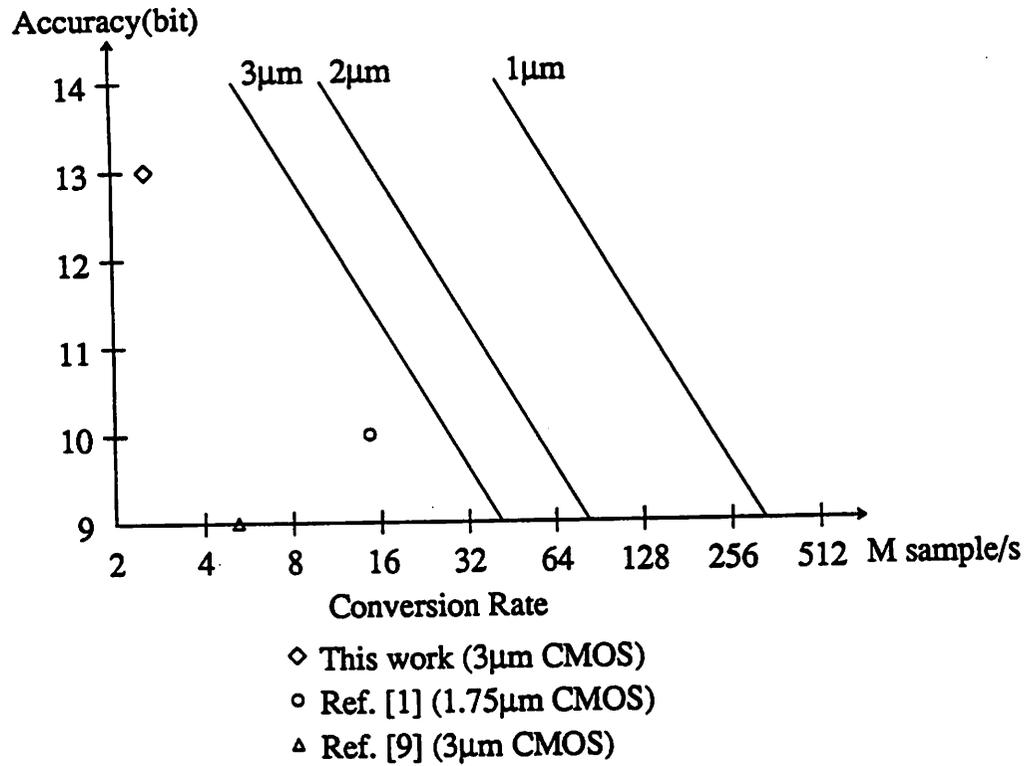
Fig. 4.16 Achievable Conversion rate vs. Achievable Accuracy
(Interstage Gain = 2)

CHAPTER 5

AN EXPERIMENTAL 13 BIT PIPELINED A/D CONVERTER

5.1 Introduction

A 13-bit 2.5MHz pipelined A/D converter has been fabricated in 3 µm CMOS technology. It is predicted that video-rate conversion speed(> 15MHz) can be achieve with 1.5 µm CMOS technology. The tradeoff of speed and hardware on pipelined A/D converter has been described previously,[9] we will not repeat the discussion here. Base on these study we chose 3-bit per stage with digital error correction in order to achieve video-rate conversion speed, while maintaining reasonable hardware cost.
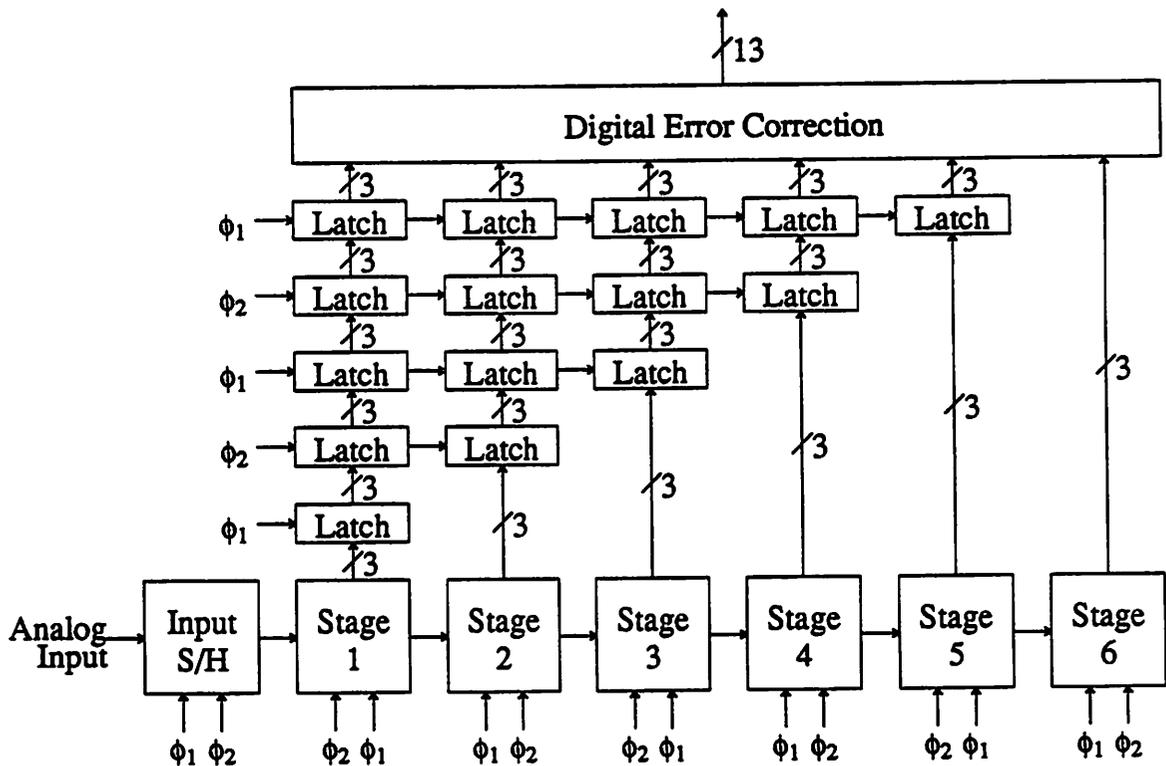

Fig. 5.1 Block Diagram of 13-bit Pipelined A/D Converter

Fig. 5.1 shows the block diagram of the A/D converter. It consists of an input S/H circuit, 6

pipelined stages, each resolving 3 bits, latches for resynchronizing the output digital codes and digital error correction logic. One bit from each stage is used to digitally correct the nonlinearity of the A/D subconverter in the previous stages as described in Chapter 4. The first stage contributes 3 bits, the remaining 5 stages each contribute 2 bits, the resulting resolution is therefore 13 bit. Implementation details will be discussed in the following sections.

5.2 Input S/H Circuit

As discussed in Chapter 2, a differential S/H circuit topology with a single center switch offers good linearity and exhibits low sensitivity to component mismatch. The actual implementation and design considerations of this configuration are described in the following sections.

5.2.1 Implementation

Fig. 5.2 shows the detailed implementation of the differential S/H circuit with a single center switch. On phase ϕ_1, the sampling switch M_1, common mode reset switches M_{1_+}, M_{1_-} and transmission gate M_{3_+} and M_{3_-} are closed, the voltage on the sampling capacitor C_{S_+} and C_{S_-} tracks the input. At the same time, the integrating capacitors C_{I_+} and C_{I_-} and the output of the op amp are shorted to ground through M_{4_+} and M_{4_-}, M_{5_+} and M_{5_-}, respectively. At the end of phase ϕ_{1_-}, an advanced version of phase ϕ_1, the common mode reset switches M_{1_+}, M_{1_-} turn off. Next the sampling switch M_1 is turned off by ϕ_1 and the differential input voltage is sampled on the sampling capacitors C_{S_+} and C_{S_-}. The output common mode of the op amp also resets at the same time through transmission gate M_2. The phase ϕ_{1_-}, a delayed version of the ϕ_1 is used to turn off transmission gates $M_{3_+}, M_{3_-}, M_{4_+}, M_{4_-}, M_{5_+}$ and M_{5_-}. On phase ϕ_2, transmission gates M_{6_+}, M_{6_-}, and M_7 are turned on and the charge sampled on the sampling capacitors C_{S_+} and C_{S_-} is transferred to the integrating capacitors C_{I_+} and C_{I_-}. This completes the S/H operation and allow the subsequent A/D converter to sample the output of the op amp.

5.2.2 Design Considerations

To achieve high accuracy, careful design of the input S/H circuit is essential. The design
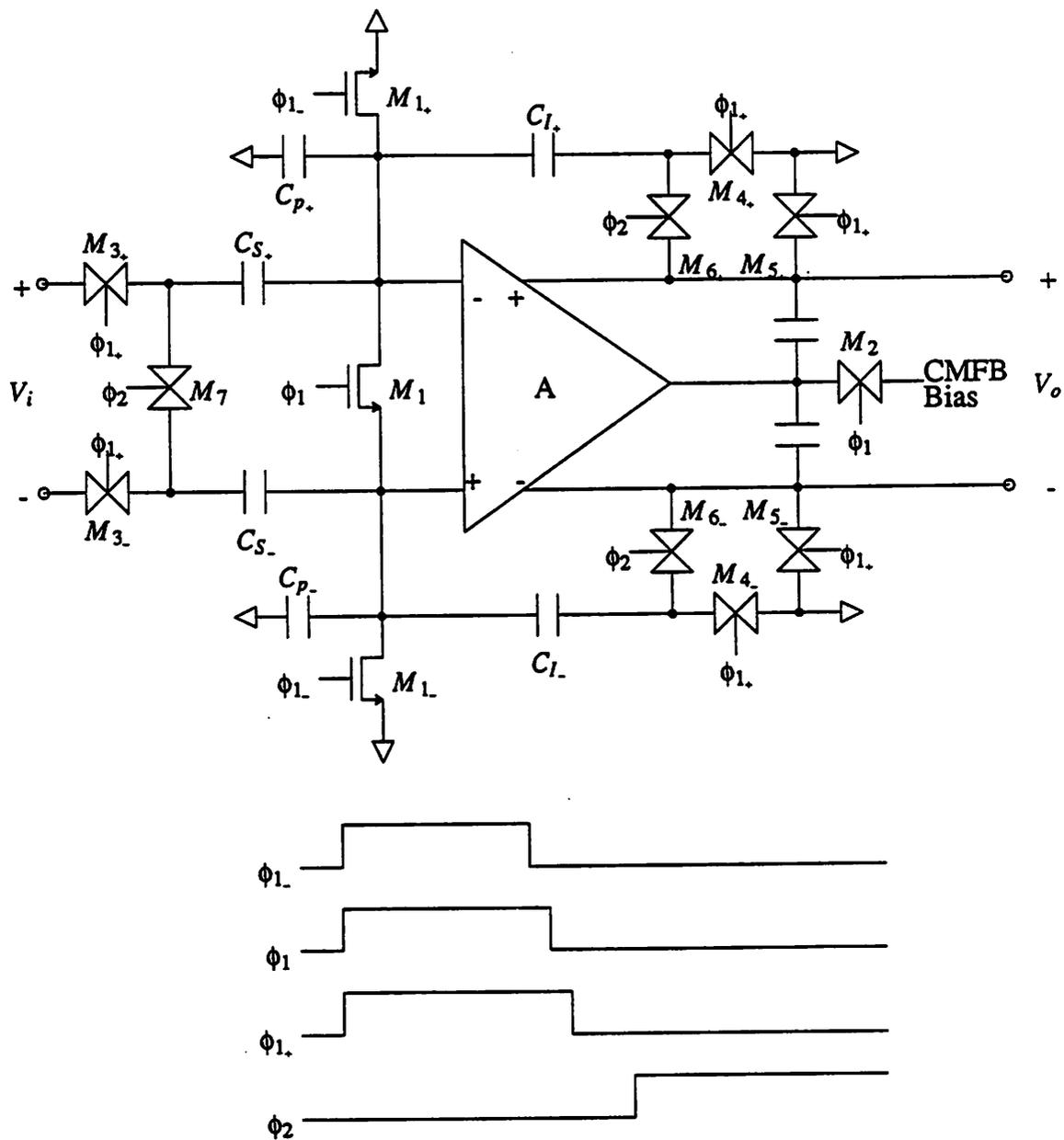
Fig. 5.2 Input S/H Circuit

considerations, which include gain of the S/H amplifier, $\frac{kT}{C}$ noise and sampling switch size, are discussed in this section.

The gain of the input S/H is chose to be two instead of one to ease the stability requirement. This approach simplified the design on the op amp to have simultaneously high gain and good closed-loop stability. This point will be elaborated upon in the later sections.

To calculate the input referred $\frac{kT}{C}$ noise, the noise source and the resistor of the sampling
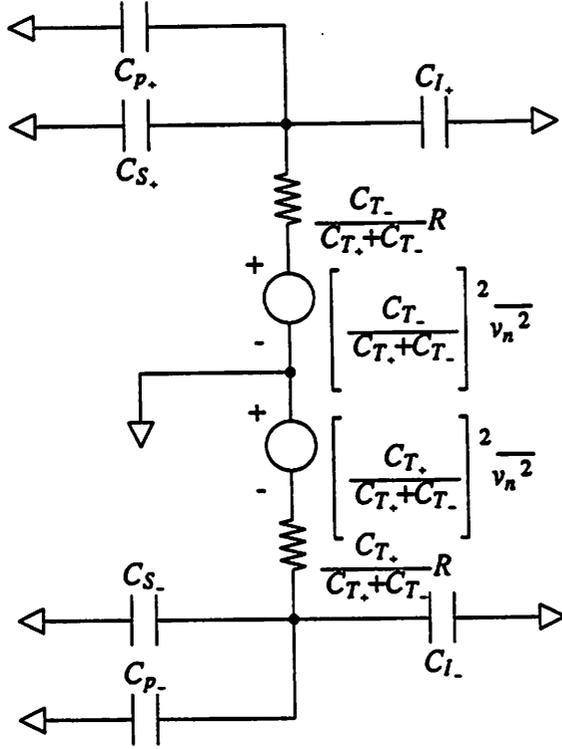
Fig. 5.3 $\frac{kT}{C}$ Noise Calculation

switch M_1 in Fig. 5.2 can be split as in Fig. 5.3, where R is the switch resistance, $\overline{v_n^2}$ is the thermal noise of the switch and the two noise sources are correlated. Therefore, the noise sampled on the positive and negative sampling nodes are $\frac{kT}{C_{T_+}}\left[\frac{C_{T_-}}{C_{T_+}+C_{T_-}}\right]^2\left[\frac{C_{T_+}+C_{T_-}}{C_{T_-}}\right]$ and

$\frac{kT}{C_{T_-}}\left[\frac{C_{T_+}}{C_{T_+}+C_{T_-}}\right]^2\left[\frac{C_{T_+}+C_{T_-}}{C_{T_+}}\right]$, respectively, where $C_{T_+}=C_{S_+}+C_{I_+}+C_{p_+}$ and $C_{T_-}=C_{S_-}+C_{I_-}+C_{p_-}$ are the total capacitors at the positive and negative sampling nodes. Since, the charge will eventually be transferred to C_{I_+} and C_{I_-}, the input-referred $\frac{kT}{C}$ noise $\overline{v_{n_+}^2}$ and $\overline{v_{n_-}^2}$ in the positive and negative branch can be calculated as

$$\overline{v_{n_+}^2} = \frac{kT}{C_{T_+}}\left[\frac{C_{T_-}}{C_{T_+}+C_{T_-}}\right]^2\left[\frac{C_{T_+}+C_{T_-}}{C_{T_-}}\right]\left[\frac{C_{T_+}}{C_{I_+}}\right]^2\left[\frac{\frac{C_{S_+}}{C_{I_+}}+\frac{C_{S_-}}{C_{I_-}}}{2}\right]^{-2}$$

$$= kT\frac{C_{T_+}C_{T_-}}{C_{T_+}+C_{T_-}}\left[\frac{\frac{C_{S_+}}{C_{I_+}}+\frac{C_{S_-}}{C_{I_-}}}{2}\right]^{-2}\frac{1}{C_{I_+}^2} \qquad (5.1)$$

and

$$\overline{v_{n_-}^2} = \frac{kT}{C_{T_-}}\left[\frac{C_{T_+}}{C_{T_+}+C_{T_-}}\right]^2\left[\frac{C_{T_+}+C_{T_-}}{C_{T_+}}\right]\left[\frac{C_{T_-}}{C_{I_-}}\right]^2\left[\frac{\frac{C_{S_+}}{C_{I_+}}+\frac{C_{S_-}}{C_{I_-}}}{2}\right]^{-2}$$

$$= kT\frac{C_{T_+}C_{T_-}}{C_{T_+}+C_{T_-}}\left[\frac{\frac{C_{S_+}}{C_{I_+}}+\frac{C_{S_-}}{C_{I_-}}}{2}\right]^{-2}\frac{1}{C_{I_-}^2} \tag{5.2}$$

Since the two noise sources are correlated by definition, the input-referred differential noise $\overline{v_n^2}$ can be represented as

$$\overline{v_n^2} = \left[\sqrt{\overline{v_{n_+}^2}}+\sqrt{\overline{v_{n_-}^2}}\right]^2 = kT\frac{C_{T_+}C_{T_-}}{C_{T_+}+C_{T_-}}\left[\frac{\frac{C_{S_+}}{C_{I_+}}+\frac{C_{S_-}}{C_{I_-}}}{2}\right]^{-2}\left[\frac{1}{C_{I_+}}+\frac{1}{C_{I_-}}\right]^2 \tag{5.3}$$

In the case of perfect matching, the input-referred differential $\frac{kT}{C}$ noise can be approximated as $\frac{2kTC_T}{C_S^2}$. To minimize the effects of the $\frac{kT}{C}$ noise have on the A/D converter performance, the $\frac{kT}{C}$ noise should be smaller than the quantization noise. The condition for this requirement can be expressed as

$$\frac{2kTC_T}{C_S^2} < \frac{1}{12}\frac{V_{pp}^2}{2^{2N}} \tag{5.4}$$

where V_{pp} is the peak-to-peak differential input conversion range of A/D converter and N is the number of bits resolved. From Eq. (5.4), we can obtain the expression for the C_S

$$C_S > \frac{C_T}{C_S}\frac{24kT2^{2N}}{V_{pp}^2} \tag{5.5}$$

Assume $C_p=C_S$, $C_I=\frac{C_S}{2}$, N = 13 and V_{pp} = 3 Volt, The minimum required C_S is calculated by Eq. (5.5) to be 1.86 pF. In this prototype, a 4 pF capacitor is used for the input sampling capacitors C_S and a 2 pF capacitor is used for the integrating capacitors C_I.

As discussed in Chapter 2, the larger the switch, the smaller the nonlinearity. Therefore, we use a large sampling switch to reduced the nonlinearity to the acceptable level. As mentioned in Chapter 2, the transmission gates M_{3_+} and M_{3_-} are chose to be much larger than the sampling

switch to reduce the effects of nonlinear resistance and impedance mismatch.

5.3 3-bit A/D Subconverter

As discussed in chapter 4, the tolerance on the accuracy of the A/D subconverter is quite large with digital error correction. The design of the A/D subconverter is not very critical. The actual implementation and design consideration for the 3-bit A/D subconverter are given in the following sections.

5.3.1 Implementations

Fig. 5.4 shows the block diagram of the 3-bit differential A/D subconverter. It consists of a resistor string with 8 elements, 8 simple latched comparator, some switches and encoding logic. On the ϕ_2 of the previous cycle, sampling switch M_8 and the transmission gates M_{9+} and M_{9-} are closed, the reference voltage is stored on the capacitor C_{C+} and C_{C-}. At the end of ϕ_2 of the previous cycle, sampling switch M_1 turns off and the reference voltage is sampled on the capacitors C_{C+} and C_{C-}. The phase ϕ_{2a}, a delayed version of ϕ_2, of the previous cycle is used to turn off transmission gates M_{9+} and M_{9-}. On phase ϕ_1, M_{10+} and M_{10-} are turned on. The voltage difference between the reference voltage and the input voltage appears at the comparator input. The comparators are strobed and latched. The digital output of the comparator is encoded to give a binary code output and used to control the D/A subconverter. This completes the A/D subconversion operation.

5.3.2 Design Considerations

Since the accuracy of the A/D subconverter is not critical, the design of the comparator is focused on the speed and size of the comparator. A simple regenerated latch shown in Fig. 5.5 is adequate for our purpose. There is no preamplification or offset cancellation. This circuit is small, fast and exhibits an offset well within our tolerance.
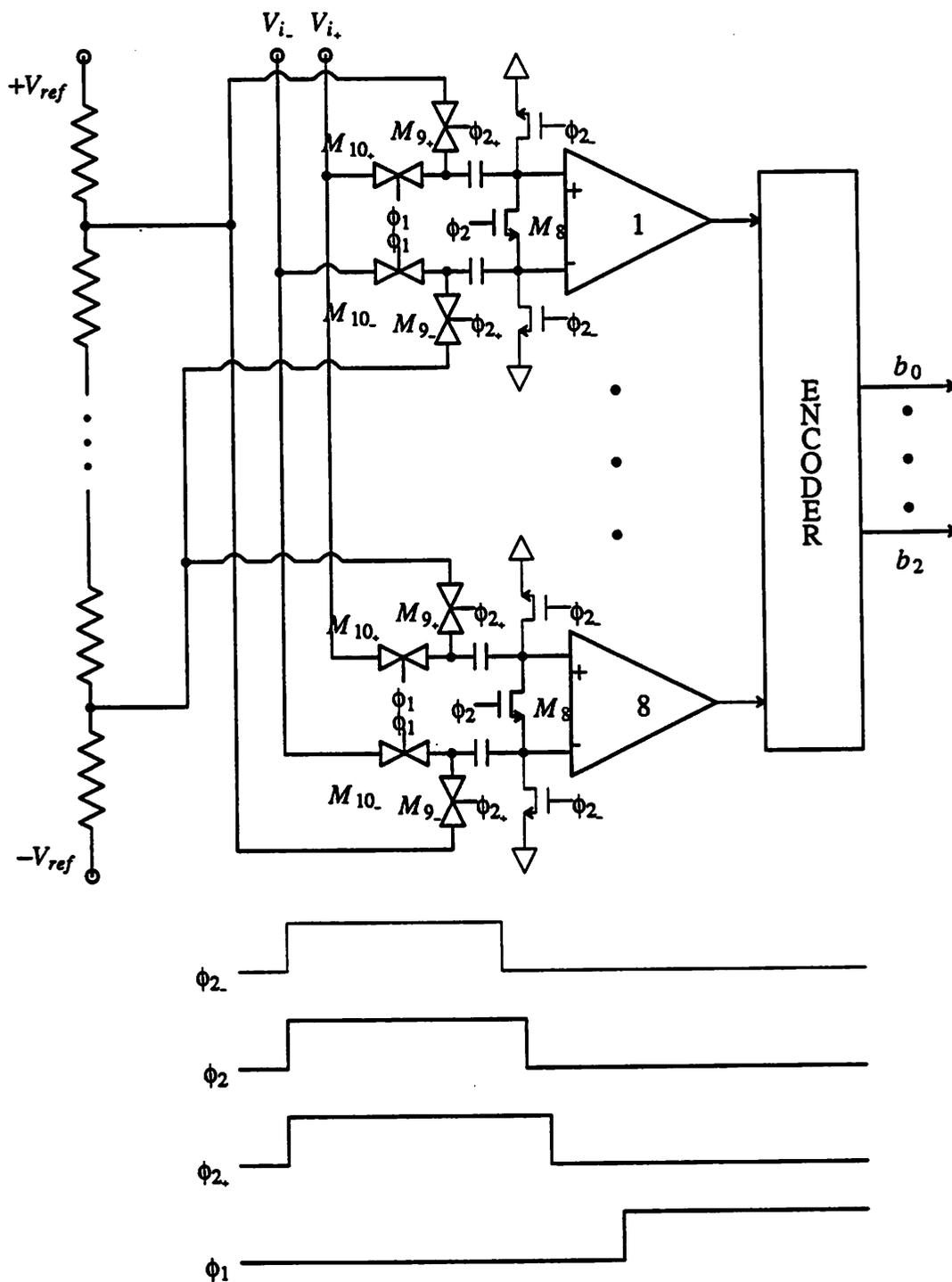
5.4 Operational Amplifier

Fig. 5.4 3-bit Differential A/D Subconverter

Fig. 5.6 shows the detailed implementation of a pipelined stage. It consists of an op amp, 8 sampling capacitors, 2 integrating capacitors and some switches. The interstage gain is scaled down to 4 instead of 8 to accommodate digital error correction. This allow a $\pm\frac{1}{2}$ LSB nonlinear-
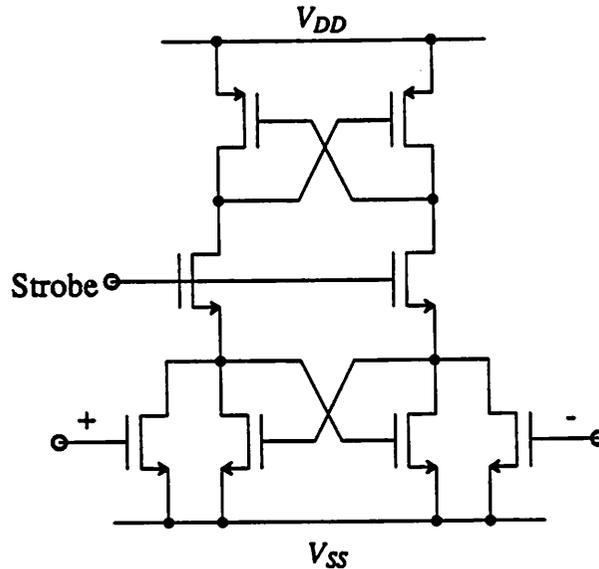
Fig. 5.5 Latched Comparator

ity on the 3-bit A/D subconverter. Because the first stage requires 13-bit accuracy and the second stage requires 10 bit accuracy, self-calibration techniques is used in the first and the second stages to achieve 13 bit linearity, For the following stages, only 8-bit or less accuracy is required, no calibration is needed because monolithic capacitor can be easily matched to better than 8-bit accuracy. A fully differential configuration is used to improve power supply rejection ratio(PSRR) and the long term stability of the calibration. Implementation detail and design considerations on the op amps are presented in the following sections.

5.4.1 Implementation

On phase ϕ_1, the sampling switch M_1 and the common mode reset switch M_{1+}, M_{1-} are closed and the voltage on the sampling capacitor $C_{S_{1+}}$ - $C_{S_{4+}}$ and $C_{S_{1-}}$ - $C_{S_{4-}}$ track the input. At the same time, the integrating capacitors C_{I+} and C_{I-} and the output of the op amp are shorted to ground. The common mode reset switches M_{1+}, M_{1-} and the sampling switch M_1 are then turned off by the phase ϕ_{1-} and ϕ_1, sequentially as in the S/H case and the input voltage is sampled on the sampling capacitors $C_{S_{1+}}$ - $C_{S_{4+}}$ and $C_{S_{1-}}$ - $C_{S_{4-}}$. The output common mode of the op amp also resets at the same time. Phase ϕ_{1+} is used to turn off the transmission gates connected to the input. On phase ϕ_2, the charge sampled on the sampling capacitors $C_{S_{1+}}$ - $C_{S_{4+}}$ and $C_{S_{1-}}$ - $C_{S_{4-}}$ is
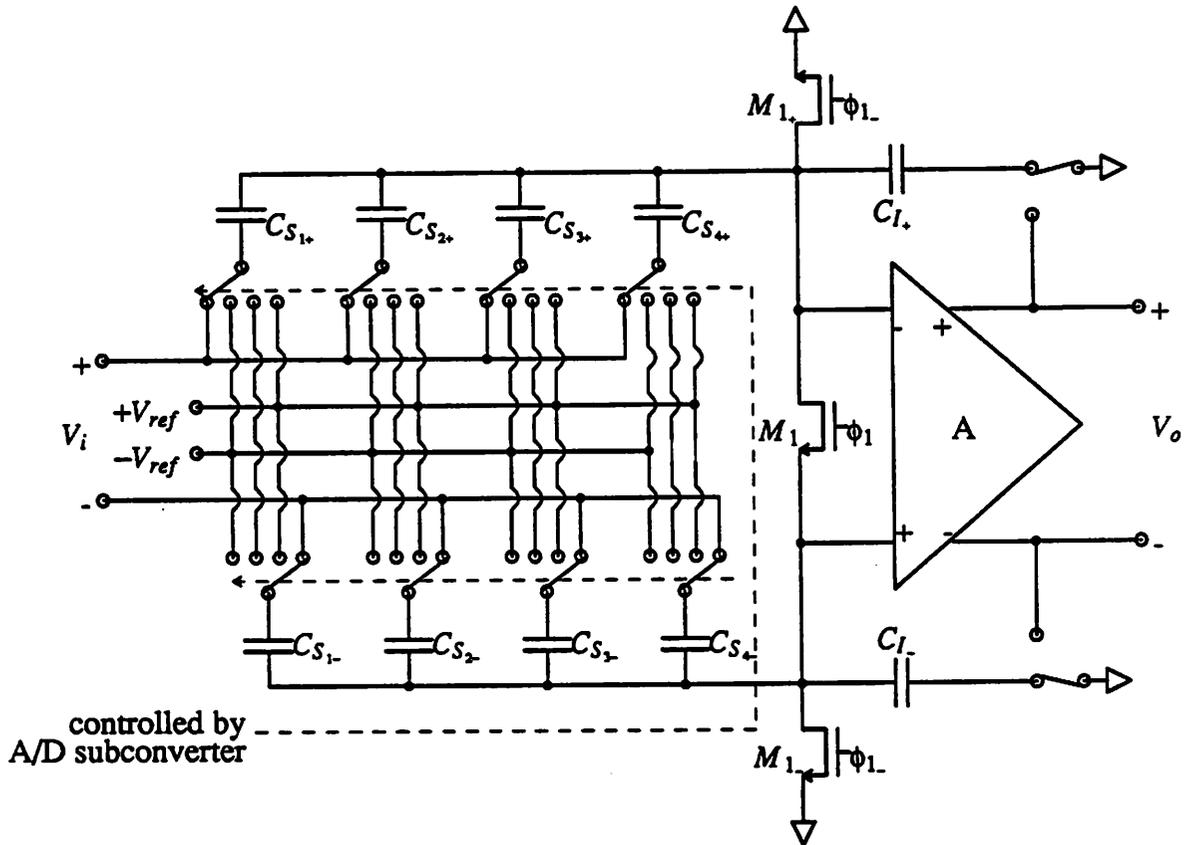
Fig. 5.6 Implementation of a 3-bit Pipelined Stage

transferred to the integrating capacitors C_{I_+} and C_{I_-}. This performs the D/A subconversion, subtraction and amplification operations and allow the next stage to sample the op amp output.

Fig. 5.7 shows the schematic of the differential op amp, it consists one P input pair and one N input pair driving corresponding mirror stages. Each mirror stage is designed to give a gain of 2. Due to the two input drivers and the gain of the mirror stage, the gain of the op amp is approximately four time of the conventional folded cascode op amp. Since there are two non-dominant poles, one is due to the cascode stage, the other due to the mirror stage, the op amp is not unity-gain stable. However, since the op amp in this pipelined A/D converter is never configured in a unity-gain feedback configuration, this does not pose a limitation on the performance of the A/D converter.

The auxiliary op amp used by offset-cancellation is about 10 times smaller than the main op amp in order to minimize the effect of charge injection. The common mode feedback branch is 20 % of the main branch to allow compensation of the common mode mismatch. A simple biasing
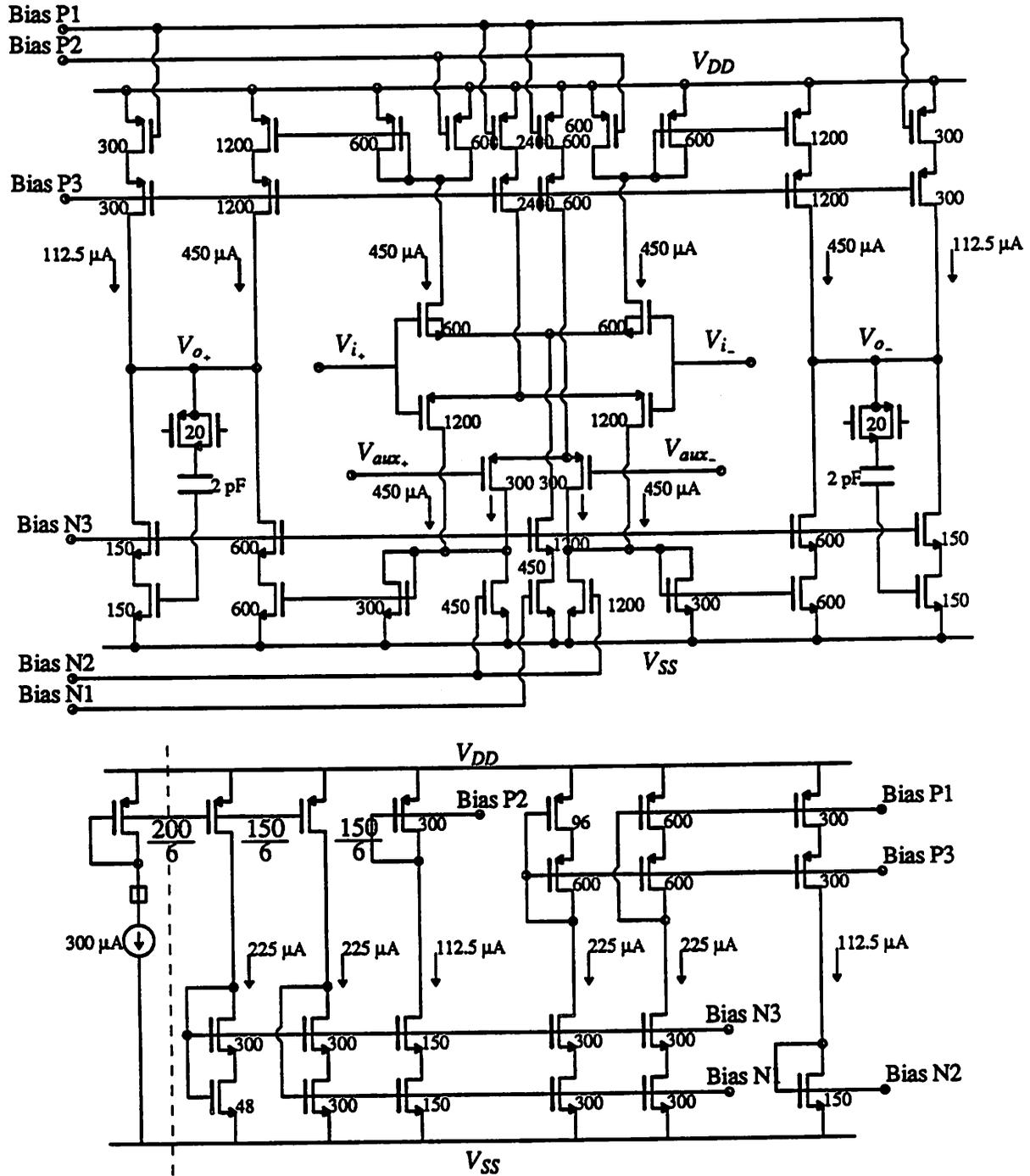
all channel length are 3 μm

Fig. 5.7 Schematics of the Operational Amplifier

circuit is used to bias the op amp as shown in Fig. 5.7.

5.4.2 Design Considerations

From Eq.(4.6), we can get the following constrain on the open loop gain of the op amp

$$\left| \frac{1}{(1+\frac{C_T}{C_I A})} - 1 \right| < \frac{1}{2^K} \tag{5.6}$$

where K is the resolution required at the input of next stage. Therefore, the open loop gain requirement of the op amp can be expressed as

$$A > 2^K \frac{C_T}{C_I}[1-2^{-K}] \tag{5.7}$$

Assume $C_p = C_S$, for N = 13, the first stage resolve 3 bits, thus K = 10 and the open loop gain requirement of the op amp is A > 9207, this 80 dB gain requirement is hard to realize for high speed op amp. If self-calibration is used, the stringent op amp gain requirement can be relieved by compensating the insufficient op amp gain with larger C_S in the self-calibration procedure. The op amp gain only needs to satisfy the self-calibration requirement in Eq. (4.12). Therefore the requirement of op amp gain becomes

$$A > \frac{(\frac{V_\varepsilon}{V_{ref}} - \frac{3}{2^N})}{(\frac{3}{2^N}\frac{C_I}{C_T} - \frac{V_{res}}{V_{ref}})} \tag{5.8}$$

assume $C_p = C_S$, $\frac{V_{res}}{V_{ref}}$ = 0.0025%(0.1mV uncancelled offset with V_{pp} = 4V) and $\frac{V_\varepsilon}{V_{ref}}$ = 2.5%(100mV comparator offset with V_{pp} = 4V), the open loop gain requirement of the op amp is A > 1570, which is much less stringent than the case without self-calibration. Because only the first and second stages are calibrated, the third stage needs to resolve 8 bit and its open loop gain requirement becomes A > 567 from Eq. (5.7). In this prototype, we design the op amp gain to be around 4000 in order to satisfy the above requirements.

5.5 Trim Capacitors

As shown in Chapter 4, the trim capacitor needs to provide a very fine step size and also compensate for the insufficient gain of the op amp. A T capacitor divider network must be used in order to implement such a trim capacitor. The implementation details and design considerations will be described in the following sections.
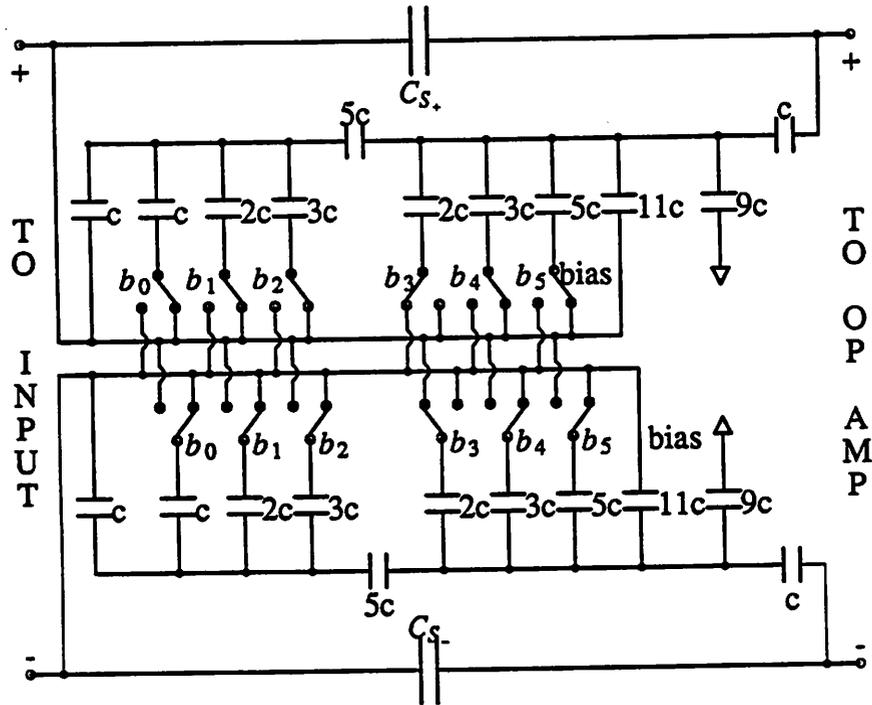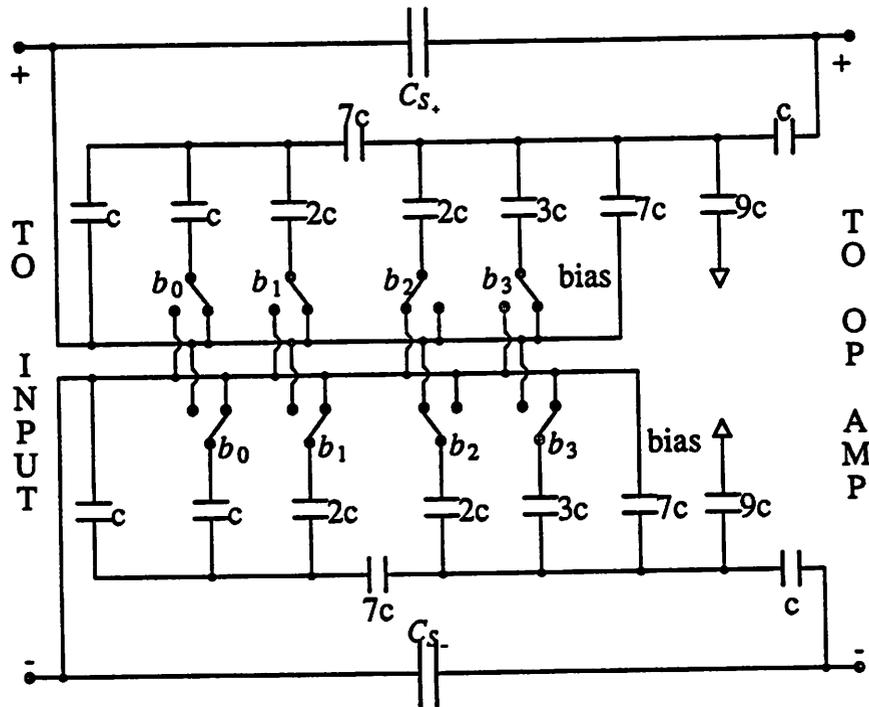
Fig. 5.8 Trim Capacitor for the First Stage

Fig. 5.9 Trim Capacitor for the Second Stage

5.5.1 Implementations

Fig. 5.8 and Fig. 5.9 show the trim capacitors for the first and second stages, respectively. A Differential configuration is used to allow both addition to and subtraction from the main

capacitor. An extra capacitor is added and connected to the input permanently to compensate for the insufficient op amp gain. The connection to the positive or negative input is controlled by the content of a shift register not shown in Fig. 5.8 and Fig. 5.9, which in turns is controlled by the calibration algorithm. The unit capacitor c is implemented by a 4 μm by 4 μm cross section of the poly 1 and poly 2. The detailed design will be shown in the next section.

5.5.2 Design Considerations

Because the trim capacitor is sensitive to the parasitic capacitor, the design of the trim capacitor is non-trivial. Fig. 5.10 & Fig. 5.11 shows the actual layout of one side of the trim capacitor and its corresponding equivalent circuit and characteristics. The components with dashed lines represents the parasitic elements. All the capacitance needs to be included in the calculation to achieve reasonable accuracy. These include edge parasitic and poly-to-substrate capacitance.
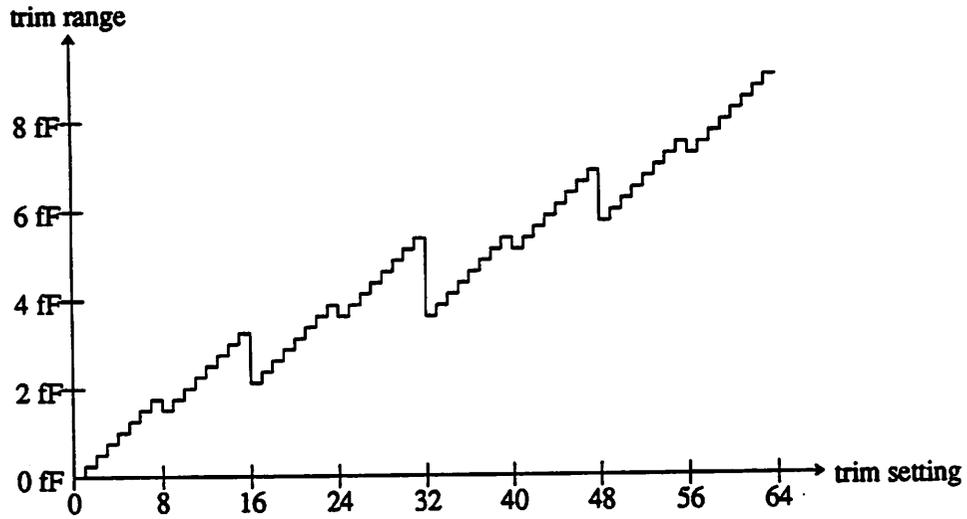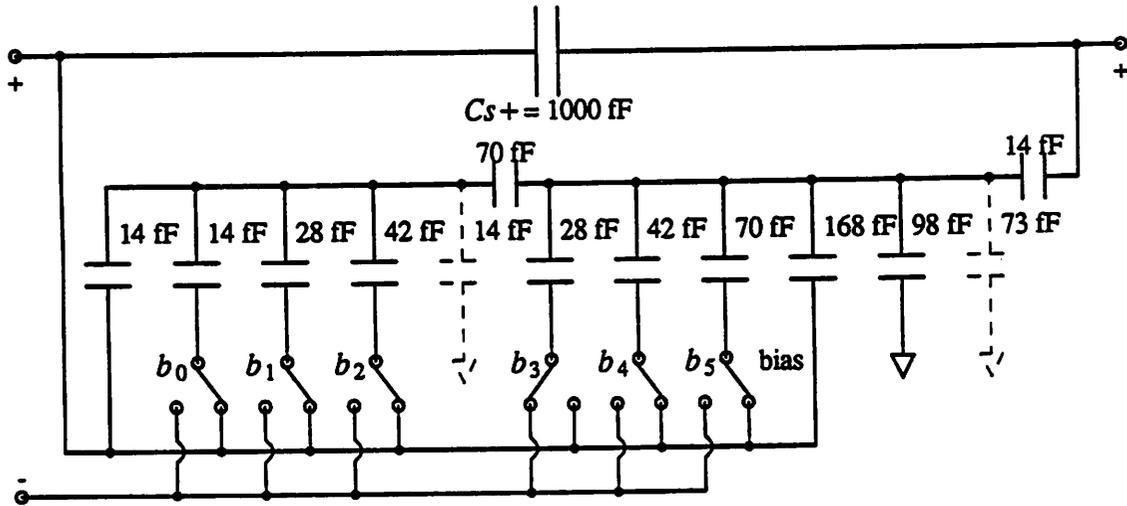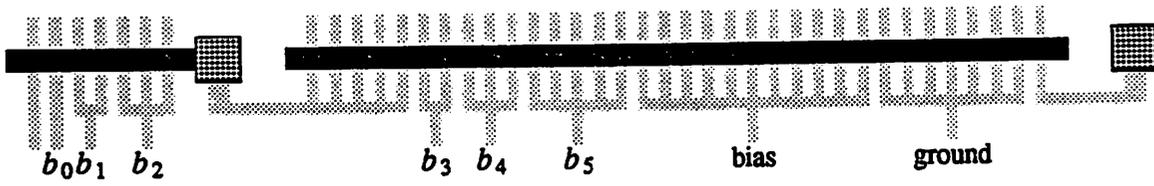
Fig. 5.10 Trim Capacitor for the First Stage
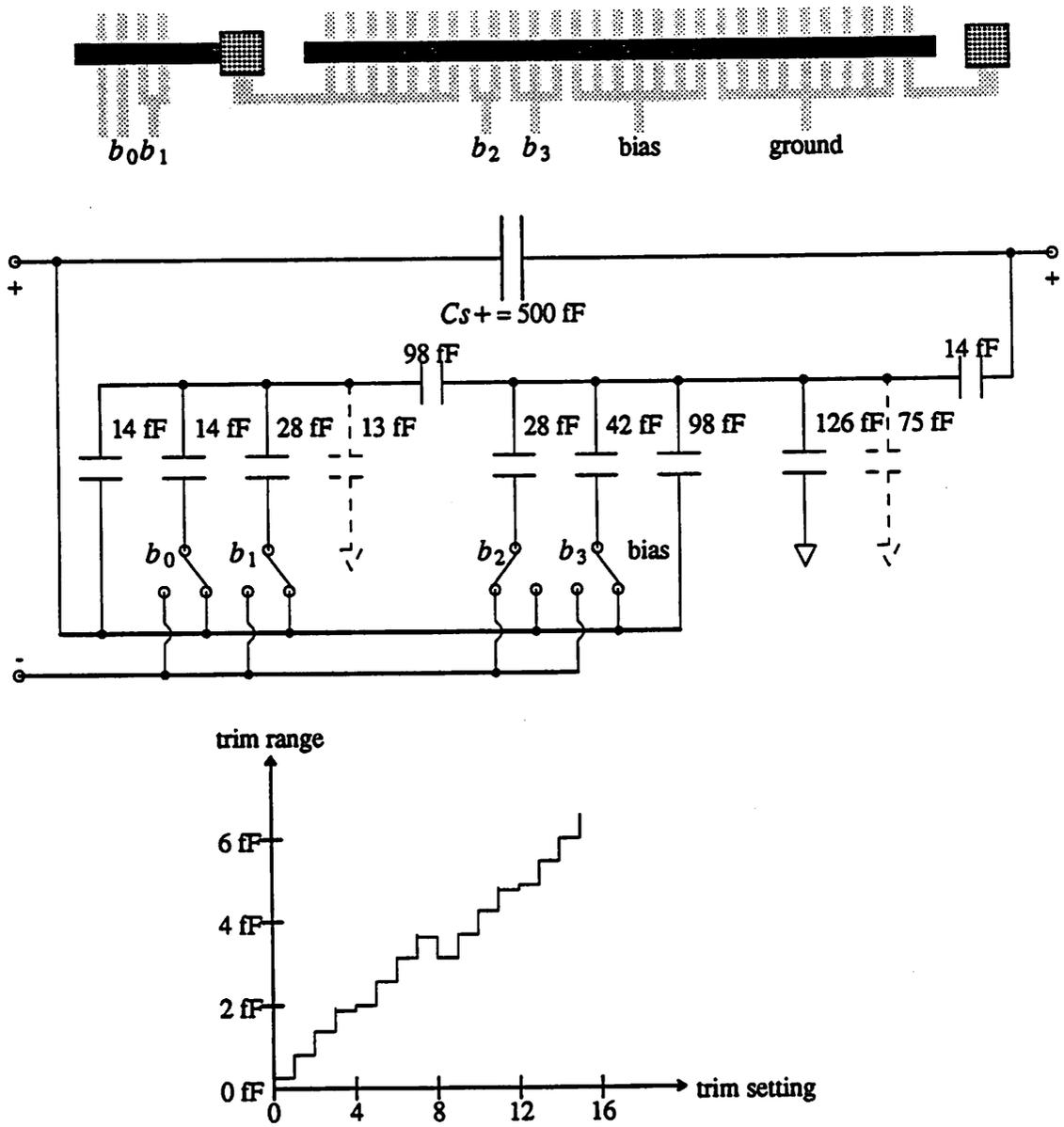
Fig. 5.11 Trim Capacitor for the Second Stage

5.6 Conclusions

A prototype 13 bit self-calibrated pipelined A/D converter has been designed and fabricated. Digital error correction, offset cancellation and self-calibration techniques is used to eliminate various nonidealities encountered in the implementation of the prototype. A chip photo is shown in Fig. 5.12
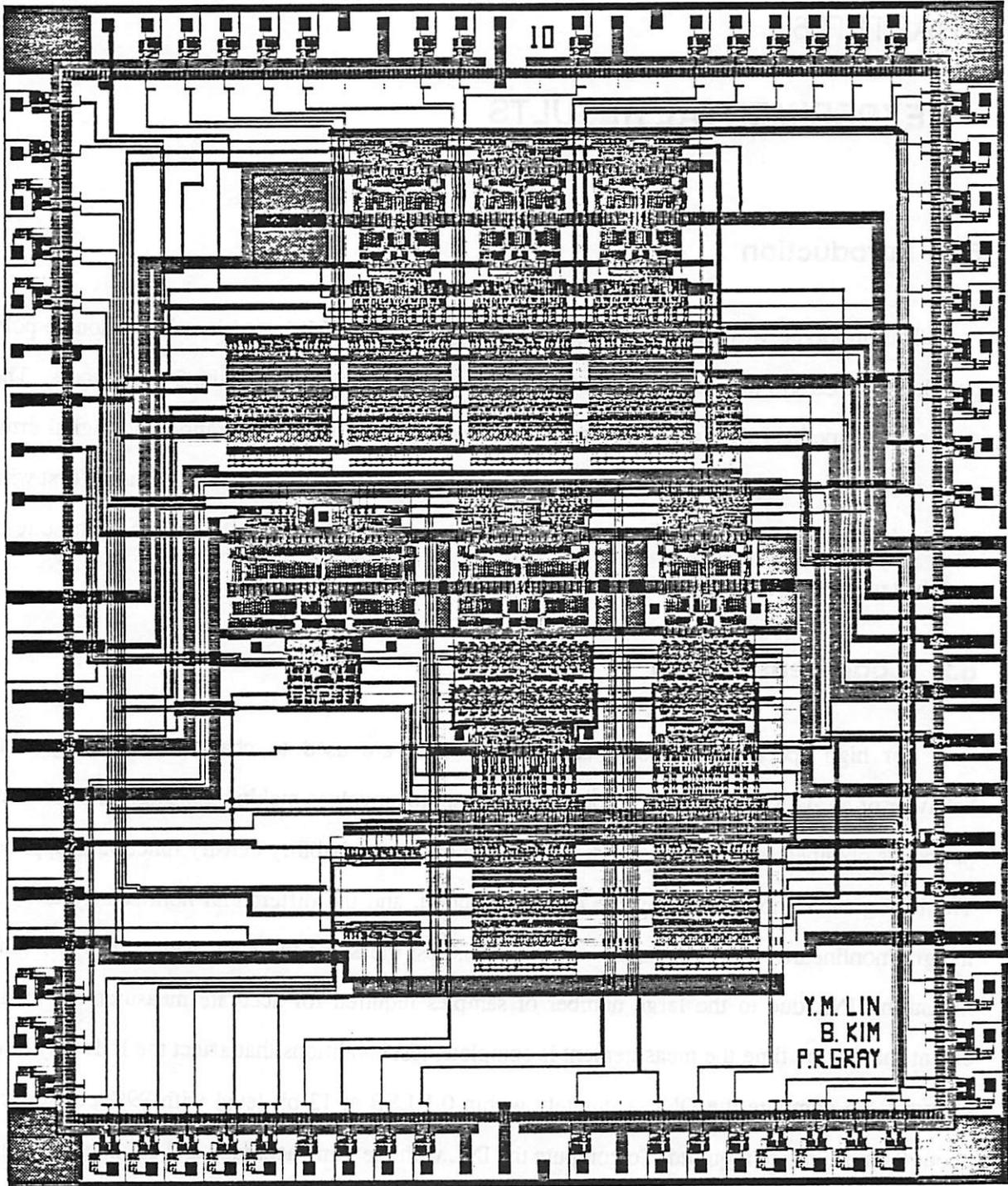
Fig. 5.12 Chip Photo

CHAPTER 6

EXPERIMENTAL RESULTS

6.1 Introduction

The prototype was designed using 3 μm design rule, but fabricated in a 2 μm double poly double metal CMOS process through MOSIS due to the unavailability of the 3 μm process. The core of the pipelined A/D converter is on the silicon, but the clock generation and digital error correction logic is implemented off-chip. It has been tested with two different methods: first with a code-density test, and second with a signal-to-noise ratio(SNR) test. The results of these tests and the test setup are described below.

6.2 Code Density Test

For high speed applications, code-density tests are used to characterize the dynamic behavior of an A/D converter. The code-density test [14] involves making a histogram of the output codes obtained while a full speed input with a known probability density function is applied. The histogram is normalized by the density function, and the differential nonlinearity and the integral nonlinearity are calculated. Although this test measures the DNL well, it has difficulty measuring INL due to the large number of samples required for accurate measurement to the extent that by the time the measurement is complete, test conditions that affect the INL may have changed. To compute the DNL accurately within 0.1 LSB at 13 bit level with 99% confidence, about 8.4 million are required. To compute the INL with the same accuracy and confidence, about 69 billion samples are required. Due to the difficulty in obtaining large amount of data, 16 million samples are collected for the code-density tests, which is more than enough for the DNL, but can only attain about 6 LSB accuracy at a 13 bit level with 99% confidence for INL. Therefore, the results for integral nonlinearity are presented here for reference only. SNR tests are more suitable for the evaluation of the integral nonlinearity. Fig. 6.1 shows a typical DNL plot of the 13-bit

A/D converter, it exhibits only +0.4/-0.6 LSB errors on DNL. Because it never reaches -1 LSB, there are no missing codes. Fig. 6.2 shows the INL plot of the prototype, it exhibits ±2 LSB errors on INL. As explained above, the results on the INL must be verified by the other tests.

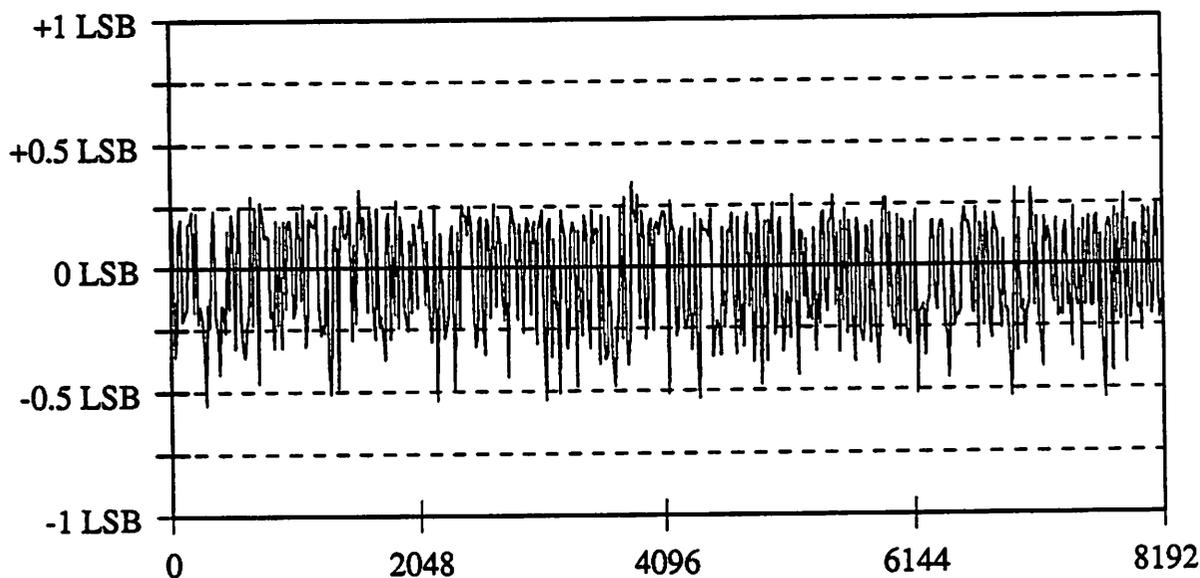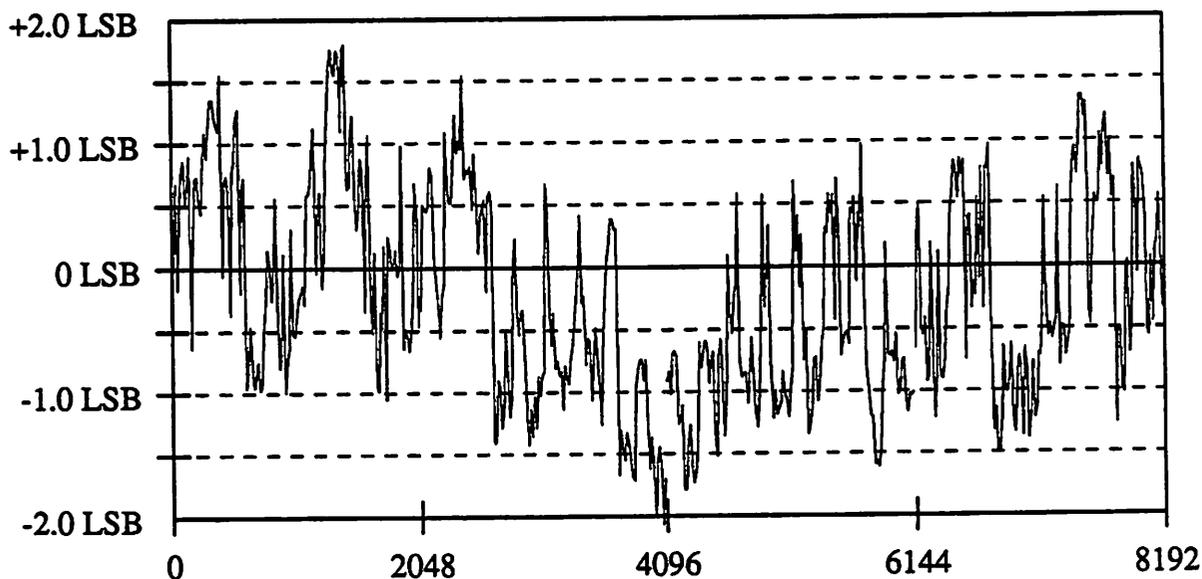Fig. 6.1 Differential Nonlinearity (DNL)

Fig. 6.2 Integral Nonlinearity (INL)

6.3 Signal-to-Noise Ratio Test

SNR characterization overcomes a limitation that occurs in measuring INL with code-density test; that is, because fewer samples are needed to measure the SNR than the INL, the SNR test is not as sensitive to changes in test conditions during the test as is the code-density test. The

SNR test can be used to estimate the maximum absolute INL, through the total harmonic distortion (THD). The SNR test was done by collecting 16,384 samples and performing a discrete Fourier transform. Fig. 6.3 and Fig. 6.4 show the resulting DFT plots for a 75 kHz and 1 MHz full-scale sine input, respectively. Fig. 6.5 shows the SNR vs. input level for the 75 kHz and 1 MHz sine input.

Fig. 6.3 Discrete Fourier Transform (75 kHz input)

6.4 Test Setup

Particularly worth mentioning is the test setup to obtain the results in Section 6.2-6.4, which will be described below. The test setup is shown in Fig. 6.6. It consists of a clean signal sources, clock generating circuit, a PC board housed the A/D converter under test and an interface to the computer. In oder to reduce the effect of power supply noise and clock interference, the A/D converter under test is housing on a multi-layer PC board with extensive power supply bypassing. This approach allowed the total system noise to be no more than 6-8 dB higher than the theoretical quantization noise ($\sim$ 140 μV RMS). It is not perfect, but so far this is the best we can achieve running the A/D at 2.5M sample/s, i.e., rated speed. The clock is generated by a Tektronix DAS, its jitter performance proved to be adequate for our purpose based on the measured FFT results.

The most difficult part of the test setup is the signal source. We use two signal sources: one is an ultra low distortion audio signal generator, which gives more the -80 dB THD and excellent SNR, the other is a high frequency RF generator output, which has only -60 dB THD and about 70 dB

Fig. 6.5 SNR vs. Input Level

Fig. 6.4 Discrete Fourier Transform (1 MHz input)

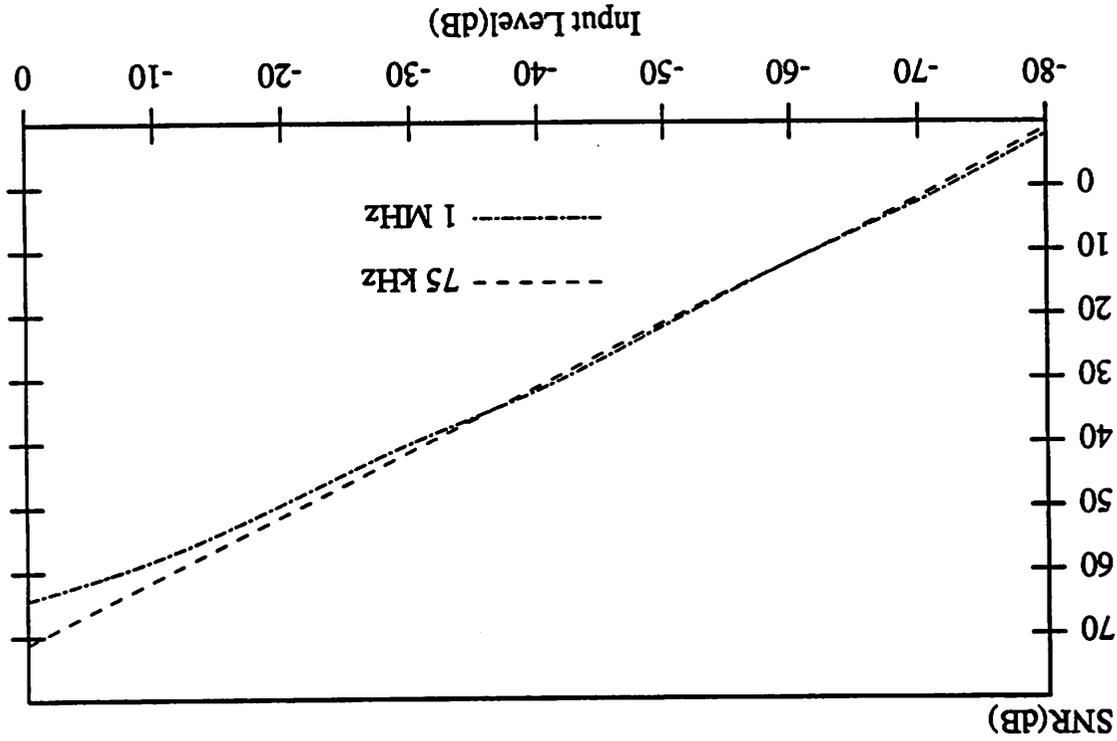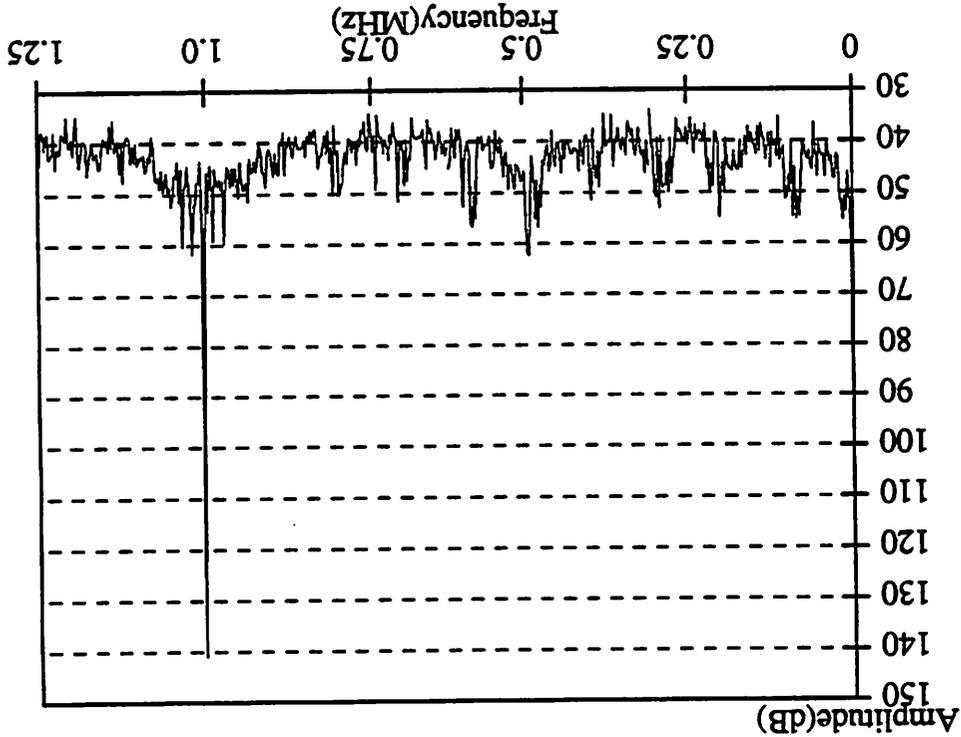SNR. In order to test high frequency response, the RF signal generator is passed through a passive bandpass filter, in this case, a third order Butterworth, to remove the unwanted harmonics down to -80 dB THD, however, the SNR is still limited to about 70 dB due to the inband noise. Both the audio and RF signal is then connected to a wideband balanced transformer to convert the single-ended signal to differential signal, which is required to drive the A/D converter. The reason to use a passive balanced transformer is the difficulty we encounter in implementing single-ended to differential conversion with active devices, namely, the distortion is hard to keep below -70 dB THD at high frequency. Both the passive filter and transformer exhibit a distortion on the level of 0.01%-0.02%, which is good enough for our purpose. The following components were used in the test setup: Ultra-low distortion audio signal generator G233 by AWA, RF singal generator 6201 by Singer, third order bandpass filter KB3 and balanced transformer Z1040 by TTE, Inc., Tektronix DAS 9100, and Sun microcomputer.
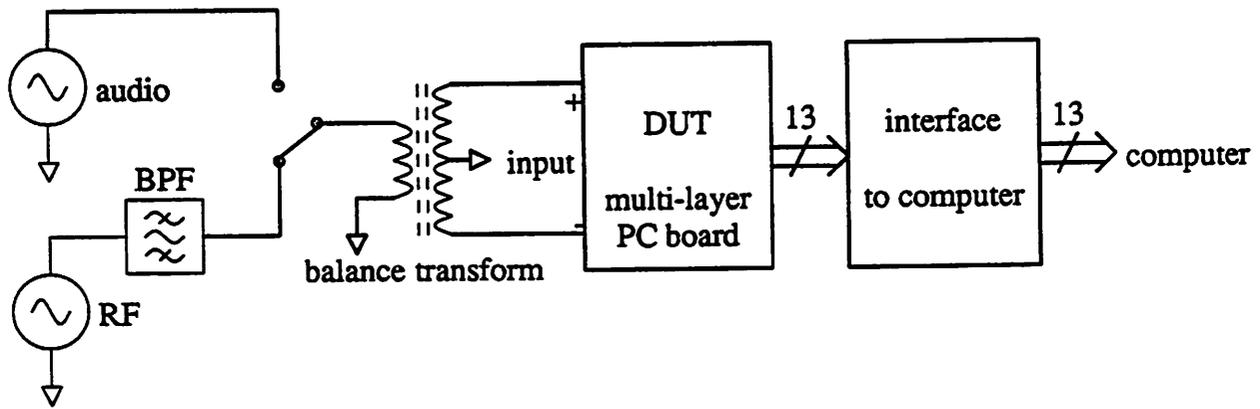
Fig. 6.6 Test Setup

6.5 Conclusions

In conclusion, the prototype achieves 2.5M sample/sec, 13 bit DNL and 11 bit INL using the techniques described in this report. Table 6.1 summarizes the important performance parameters measured in this prototype.

Technology Parameters	Measured 3μm CMOS
Supply Voltage	5V
Power Consumption	100mW
Silicon Area	25 mm^2
Conversion Rate	2.5 MHz
Resolution	13 bits
Integral Nonlinearity	±2 LSB
Differential Nonlinearity	+0.4/-0.6 LSB
Signal-to-Noise Ratio	72 dB
PSRR(low frequency)	58 dB

Table 6.1 Performance Parameters

CHAPTER 7

CONCLUSIONS

7.1 Summary of Research Results

The research has arrived at two conclusions. First, the differential bottom-plate T/H topology with a single sampling switch exhibits the smallest nonlinearity and offset amongst the four topologies studied. There appears to be no fundamental limit on how good the T/H circuit performance can be. Practical considerations such as loading on the op amp summing node, common mode voltage shift and differential offset dictate the design of T/H circuits. With a suitable size sampling switch, 12-13 bit linearity at video speed is feasible. Second, the pipelined architectures combined with self-calibration techniques can achieve high resolution at video speed with reasonable area and power consumption. Although the self-calibration technique can relieve the requirement on the op amp gain, it is not without limitations, that is, the op amp gain still needs to be high enough to reduce the nonlinearity introduced by the nonlinear op amp gain curves. Therefore, the key difficulty in pipelined A/D converters is in designing a high-speed high-gain op amp. The research results are summarized in the following two sections: (1) the performance limitations of the input S/H circuit and (2) the performance limitations of a self-calibrated pipelined A/D converter.

7.2 Performance Limitation of the Input S/H Circuit

Several CMOS S/H circuits have been studied in this work, including the top-plate T/H circuit, the bottom-plate T/H circuit and two differential bottom-plate T/H circuits with different sampling switch arrangements. In Chapter 2, closed form approximations for the errors in the four CMOS T/H circuits mentioned above have been derived. The bottom-plate topology removes the dependence on the input signal DC voltage V_{DC} and does not suffer from gain error and gross nonlinearity as in the top-plate case. The differential topology exhibits a first order

cancellation of the offset and nonlinearity, however, the effectiveness of the cancellation depends on the matching of the positive and negative branches in the differential T/H circuit. By using a single sampling switch, we can eliminate the matching requirement of the two sampling switches in the positive and negative branches of the differential T/H circuit. Therefore, the differential T/H circuit using a single sampling switch exhibits the lowest nonlinearity and offset amongst the four T/H circuits studied.

The offset and nonlinearity of a bottom-plate T/H circuit can be expressed by technology independent design parameters, such as $\frac{f_{in}}{f_T}$ and $\frac{f_{in}}{f_{T/H}}$, where f_{in} is the input signal frequency, f_T is the usable transition, i.e. unity-gain, frequency, $f_{T/H}$ is the T/H network bandwidth. From Chapter 2, the percentage offset $\frac{V_{os}}{A}$ can be expressed as

$$\frac{V_{os}}{A} \approx g \frac{C_g}{C_S} \frac{f_T}{f_{T/H}} \frac{(V_H - V_L)}{A}$$

where g is a function of mismatch, in the case of perfect matching, g equal to 0. Also from Chapter 2, the percentage nonlinearity can be expressed as

$$\% \text{ nonlinearity} \approx g' \frac{f_{in}}{f_T} \frac{f_{in}}{f_{T/H}} \frac{A}{(V_H - V_L)} \frac{C_S}{C_T}$$

where g' is a weak function of design parameter and mismatch, A is the input signal amplitude, $V_H - V_L$ is the supply voltage and C_S, C_T are sampling and total sampling node capacitors, respectively. Since the offset and nonlinearity depend on $f_{T/H}$, C_S, $(V_H - V_L)$ and A in opposite ways, the design of a T/H circuit is based on a tradeoff between the offset and nonlinearity. The smaller the nonlinearity, the larger the DC offset. The cancellation of DC offset is possible, but an extra clock cycle is required. Another constraint is the common mode voltage shift due to the channel charge injection from the sampling switch, this can drive the op amp summing node outside its input common mode range and seriously degrade its settling speed. To solve this problem, if necessary, a transmission gate can be used to replace the NMOS sampling switch to reduce the charge injection by cancelling the negative charge injected from the NMOS switch by the positive charge injected from the PMOS switch.

A set of graphs which relate the offset and nonlinearity to various technology independent design parameters have been presented in Chapter 2 to use as design guidelines. These

technology independent design graph can be used to predict the achievable linearity and differential offset of a scaled technology. There appears to exist no theoretical limit on how good the T/H can perform, however, as the T/H bandwidth $f_{T/H}$ approaches to f_T, practical considerations such as loading of the op amp summing node, common mode voltage shift and differential offset begin to dominate. The loading consideration, differential offset and common mode voltage shift eventually limit the achievable T/H bandwidth. A plot of achievable linearity vs. signal frequency is shown in Fig. 7.1 for 3 μm, 2μm, 1μm CMOS technology with the following parameters: $C_S = 1pF$, $C_I = 1pF$, ± 1 V swing and common mode voltage shift less than 100mV in a 5V supply system.
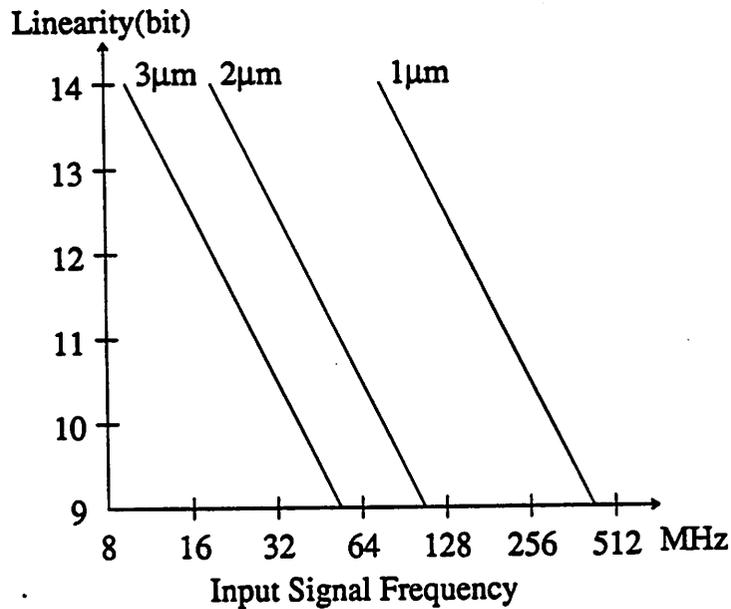

Fig. 7.1 Achievable Linearity vs. Signal Frequency

7.3 Performance Limitation of a Self-Calibration Pipeline ADC

Pipelined A/D converters consume low power and small area and when combined with self-calibration techniques have the potential to achieve high-resolution at video speeds in a reasonable area. The key difficulty lies in the need for a high-gain high-speed op amp. Increasing the resolution requires that the op amp settles to higher accuracy, but the video-speed demands a very short settling time. These two requirements impose stringent constraints on the op amp design. The op amp needs to be optimized for both fast settling and high gain. As shown in Chapter 4, this speed-accuracy tradeoff limits the achievable speed for high-resolution converter.

From Eq. (4.19), the maximum achievable conversion rate f_{BW} can be expressed as

$$f_{BW} \approx \sqrt{\frac{A_{min}}{2^N}} \frac{\pi f_{T_{max}}}{A_{cl}(N+1)\ln 2}$$

where A_{min} is the achievable gain of cascode stage biased at ΔV_{max}, N is the number of bits resolved, $f_{T_{max}}$ is the transition, i.e. unity-gain, frequency of the transistor biased at ΔV_{max}, and A_{cl} is the closed-loop gain. Fig. 7.2 shows the accuracy vs. peak achievable conversion rate for 3μm, 2μm, 1μm CMOS technology using a conventional cascode op amp. Other gain boosting methods, such as use of wideband preamp and positive feedback, may surpass these limits. However, these circuits are hard to design and usually consume quite a lot area and power. Although, self-calibration can be used to compensate for insufficient op amp gain, the linearity will suffer due to the curvature of the op amp gain curve, therefore a reasonable high gain is still needed.
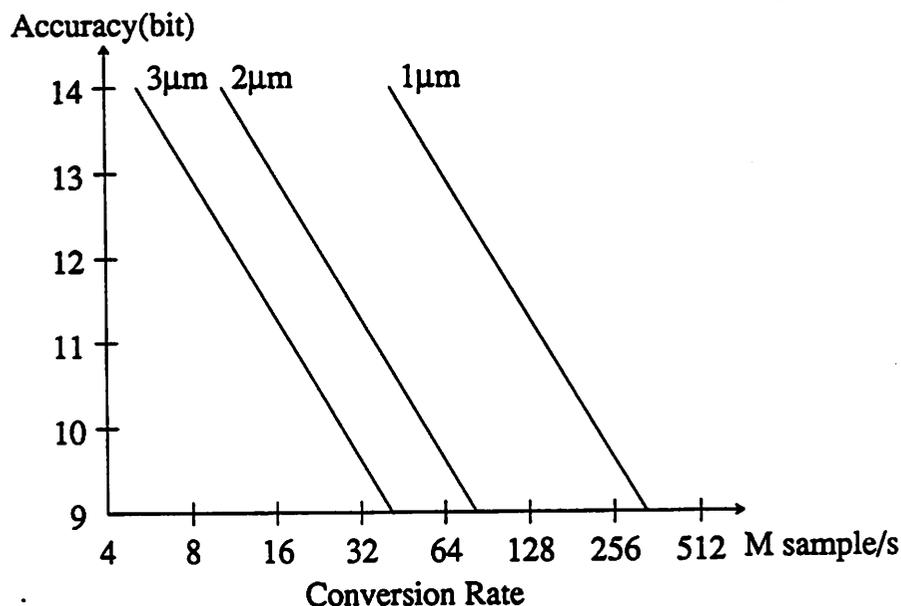

Fig. 7.2 Accuracy vs. Peak Achievable Conversion Rate

In conclusion, the pipelined A/D converter have the potential to achieve high-resolution at video speed if the difficulty of designing high-gain high-speed op amp can be solved. Comparing Fig. 7.1 and Fig. 7.2, it appears that the limits on the T/H linearity is not as sever as the limits on the peak conversion rate. Therefore, there is room to improve on the conversion rate of pipelined A/D converter by using parallel stages or more exotic high-gain high-speed op amp. The prototype achieves 2.5M sample/s conversion rate in a 3μm technology, Since the peak achievable conversion rate is directly proportional to the usable transition, i.e. unity-gain, frequency f_T, the

projected performance with constant voltage scaling is shown in Table 7.1, where a 1μm CMOS technology is projected to reach 20M sample/s in a area of 6 mm^2.

Technology Parameters	Measured 3μm CMOS	Projected 2μm CMOS	Projected 1μm CMOS
Supply Voltage	5V	5V	5V
Power Consumption	100mW	150mW	300mW
Silicon Area	25 mm^2	12 mm^2	6 mm^2
Conversion Rate	2.5M sample/s	5M sample/s	20M sample/s

Table 7.1 Projected Performance

APPENDIX A

SINGLE-ENDED BOTTOM-PLATE T/H CIRCUIT

A more accurate calculation of the single-ended bottom-plate T/H circuit is described below. The following assumptions are used to approximate the real T/H circuit:

(1) no charge pumping to the substrate,

(2) quasi-static model of MOS switch in the linear region described in Section 2.3.1 is used through out for the calculation,

(3) the remaining channel charge when the switch enters saturation region is all dumped to the source side.

The calculation can be separated into two parts, the first part deals with the linear region of the switch, while the second part deals with the saturation region of the switch. Fig. A.1 shows an equivalent circuit of the T/H circuit in the linear region. Assume the input voltage is $V_{DC}+s_i t$ and the gate voltage is $V_H-s_g t$, where V_{DC} is the input voltage at $t=0$, s_i is the slew rate of the input voltage and s_g is the gate fall rate.
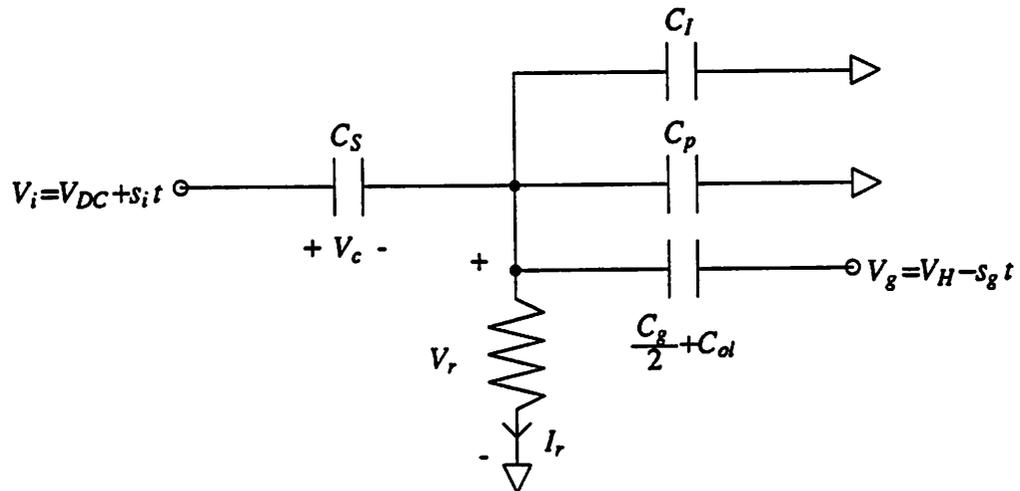

Fig. A.1 Equivalent Circuit of a Single-Ended Bottom-Plated T/H in Linear Region

From Fig. 2.9, KCL equation can be written for the sampling node as

$$C_S \frac{d(V_i - V_r)}{dt} = I_r + (C_p + C_l)\frac{dV_r}{dt} + (\frac{C_g}{2} + C_{ol})\frac{d(V_r - V_g)}{dt} \tag{A.1}$$

where I_r is the current flow through the sampling switch M_1. The T/H output voltage can be calculated in the following two cases:

(A) Positive input signal slew rate, i.e. $s_i > 0$

Since $s_i > 0$, from Eq. (2.26) we have $V_r > 0$ and $V_{ds} = V_r$. Therefore $I_r = \beta_n(V_{gs} - V_T - \frac{V_{ds}}{2})V_{ds} = \beta_n(V_g - V_{T_o} - \frac{V_r}{2})V_r$. Substituting this into Eq. (A.1), it can be rewritten as

$$s_i C_S - C_S \frac{dV_r}{dt} = \beta_n(V_g - V_{T_o} - \frac{V_r}{2})V_r + (C_p + C_l)\frac{dV_r}{dt}$$

$$+ (\frac{C_g}{2} + C_{ol})\frac{dV_r}{dt} + s_g(\frac{C_g}{2} + C_{ol}) \tag{A.2}$$

Define $C_T = C_S + C_l + C_p + \frac{C_g}{2} + C_{ol}$ as the total capacitance at the sampling node and $V_{HT} = V_H - V_{T_o}$. Since β_n can be expressed by $\frac{C_T}{\tau V_{HT}}$ from Eq. (2.24), where τ is the time constant of the T/H circuit, Eq. (A.2) can be further simplified as

$$\frac{dV_r}{dt} + \frac{1}{\tau V_{HT}}(V_{HT} - s_g t - \frac{V_r}{2})V_r = \frac{s_i C_S - s_g(\frac{C_g}{2} + C_{ol})}{C_T} \tag{A.3}$$

Eq. (A.3) is a nonlinear equation with no known closed form solution. In order to obtain a closed form solution, we make the following approximations. From Eq. (2.26), we have $V_r(0) = \frac{s_i C_S}{\beta_n V_{HT}} = \tau s_i \frac{C_S}{C_T}$. Because $\frac{V_r(t)}{2}$ is small compared to $V_{HT} - s_g t$ for most of the time the switch spends in the linear region, we can make an approximation by substituting V_r^2 with $s_i^2 \frac{\tau^2 C_S^2}{C_T^2}$. This allows us to have a closed form solution for Eq. (A.3). As can be shown from the result of the closed form solution, this approximation can be justified. Substituting V_r^2, we get

$$\frac{dV_r}{dt} + \frac{1}{\tau V_{HT}}(V_{HT} - s_g t)V_r = \frac{s_i C_S - s_g(\frac{C_g}{2} + C_{ol})}{C_T} + \frac{\tau s_i^2 C_S^2}{2V_{HT} C_T^2}$$

$$= a_0 + s_i a_1 + s_i{}^2 a_2 \qquad (A.4)$$

where

$$a_0 = -s_g \frac{\frac{C_g}{2} + C_{ol}}{C_T} \qquad (A.5)$$

$$a_1 = \frac{C_S}{C_T} \qquad (A.6)$$

$$a_2 = \frac{\tau C_S{}^2}{2 V_{HT} C_T{}^2} \qquad (A.7)$$

Since $V_r(0) = \tau s_i \frac{C_S}{C_T}$, solving Eq. (A.4), we got

$$V_r(t) = \tau \cdot e^{\frac{V_{HT}}{2 \tau s_i}(1 - \frac{s_g t}{V_{HT}})^2} \left\{ s_i \frac{C_S}{C_T} e^{-\frac{V_{HT}}{2 \tau s_i}} \right.$$

$$+ \left[a_0 + s_i a_1 + s_i{}^2 a_2 \right] \sqrt{\frac{\pi V_{HT}}{2 \tau s_g}} \left[erf\left[\sqrt{\frac{V_{HT}}{2 \tau s_g}} \right] - erf\left[\sqrt{\frac{V_{HT}}{2 \tau s_g}}(1 - \frac{s_g t}{V_{HT}}) \right] \right] \right\}$$

$$= \tau e^{\frac{X}{2}(1 - \frac{s_g t}{V_{HT}})^2} \left\{ s_i \frac{C_S}{C_T} e^{-\frac{X}{2}} \right.$$

$$+ \left[a_0 + s_i a_1 + s_i{}^2 a_2 \right] \sqrt{\frac{\pi X}{2}} \left[erf\left[\sqrt{\frac{X}{2}} \right] - erf\left[\sqrt{\frac{X}{2}}(1 - \frac{s_g t}{V_{HT}}) \right] \right] \right\} \qquad (A.8)$$

where we define a new variable $X = \frac{V_{HT}}{\tau s_g}$. Since $\frac{V_{HT}}{s_g}$ is the gate fall time, X is just the ratio of the gate fall time to the T/H network time constant. To calculate the voltage across the sampling switch M_1 at $t = T_a$ when the switch enters the saturation region, where T_a is the aperture time, we proceed as follows

Since the switch enters the saturation region when $V_g - V_d - V_T = 0$, we have

$$V_g(T_a) - V_d(T_a) - V_T = V_g(T_a) - V_r(T_a) - V_{T_0} = V_H - s_g T_a - V_r(T_a) - V_{T_0} = 0 \qquad (A.9)$$

The aperture time T_a can be calculated from Eq. (A.9) as follow

$$T_a = \frac{V_{HT}}{s_g} - \frac{V_r(T_a)}{s_g} \tag{A.10}$$

Since $\dfrac{V_r(T_a)}{s_g} \ll \dfrac{V_{HT}}{s_g}$, from Eq. (A.10) and Eq. (A.4), a first order approximation can be used to

approximate $V_r(T_a)$ by

$$V_r(T_a) \approx \frac{V_r(\frac{V_{HT}}{s_g})}{1 + \frac{1}{s_g}\frac{dV_r}{dt}(\frac{V_{HT}}{s_g})}$$

$$\approx \frac{V_r(\frac{V_{HT}}{s_g})}{1 + \frac{a_0}{s_g} + s_i\frac{a_1}{s_g} + s_i^2\frac{a_2}{s_g}}$$

$$\approx \left[1 - \frac{a_0}{s_g} - s_i\frac{a_1}{s_g} - s_i^2\frac{a_2}{s_g}\right]\tau\left\{s_i\frac{C_S}{C_T}e^{-\frac{X}{2}} + \left[a_0 + s_i a_1 + s_i^2 a_2\right]\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right]\right\}$$

$$\approx \left[1 - \frac{a_0}{s_g} - s_i\frac{a_1}{s_g} - s_i^2\frac{a_2}{s_g}\right]\left[b_0 + s_i b_1 + s_i^2 b_2\right]$$

$$\approx \left[V_{r_{0*}} + s_i V_{r_{1*}} + s_i^2 V_{r_{2*}} + s_i^3 V_{r_{3*}} + \cdots\right] \tag{A.11}$$

where

$$b_0 = -\tau s_g\frac{\frac{C_g}{2}+C_{ol}}{C_T}\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right]$$

$$= -\frac{V_{HT}}{X}\frac{\frac{C_g}{2}+C_{ol}}{C_T}\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right] \tag{A.12}$$

$$b_1 = \frac{\tau C_S}{C_T}\left[e^{-\frac{X}{2}} + \sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right]\right] \tag{A.13}$$

$$b_2 = \frac{\tau^2 C_S{}^2}{2V_{HT}C_T{}^2}\sqrt{\frac{\pi X}{2}}\,erf\left[\sqrt{\frac{X}{2}}\right] \tag{A.14}$$

where $V_{r_{0+}}$ is the term independent of s_i, $V_{r_{1+}}$ is the coefficient of s_i term, $V_{r_{2+}}$ is the coefficient of $s_i{}^2$ and $V_{r_{3+}}$ is the coefficient of $s_i{}^3$. The subscript "+" indicated that the coefficients are for $s_i > 0$ case. $V_{r_{0+}}$, $V_{r_{1+}}$, $V_{r_{2+}}$ and $V_{r_{3+}}$ can be expressed as

$$V_{r_{0+}} = (1-\frac{a_0}{s_g})b_0 = -(1+\frac{\frac{C_g}{2}+C_{ol}}{C_T})(\frac{\frac{C_g}{2}+C_{ol}}{C_T})\frac{V_{HT}}{X}\sqrt{\frac{\pi X}{2}}\,erf\left[\sqrt{\frac{X}{2}}\right] \tag{A.15}$$

$$V_{r_{1+}} = \left[(1-\frac{a_0}{s_g})b_1 - \frac{a_1}{s_g}b_0\right]$$

$$= \tau\frac{C_S}{C_T}\left\{(1+\frac{\frac{C_g}{2}+C_{ol}}{C_T})e^{-\frac{X}{2}} + (1+2\frac{\frac{C_g}{2}+C_{ol}}{C_T})\sqrt{\frac{\pi X}{2}}\,erf\left[\sqrt{\frac{X}{2}}\right]\right\} \tag{A.16}$$

$$V_{r_{2+}} = \left[(1-\frac{a_0}{s_g})b_2 - \frac{a_1}{s_g}b_1 - \frac{a_2}{s_g}b_0\right]$$

$$= -\frac{\tau^2 C_S{}^2}{C_T{}^2 V_{HT}}\left\{\left[X - \frac{(1+2\frac{\frac{C_g}{2}+C_{ol}}{C_T})}{2}\right]\sqrt{\frac{\pi X}{2}}\,erf\left[\sqrt{\frac{X}{2}}\right] + Xe^{-\frac{X}{2}}\right\} \tag{A.17}$$

$$V_{r_{3+}} = -\left[\frac{a_1}{s_g}b_2 + \frac{a_2}{s_g}b_1\right]$$

$$= -\frac{\tau^3 C_S{}^3}{C_T{}^3 V_{HT}{}^2}\frac{X}{2}\left\{2\sqrt{\frac{\pi X}{2}}\,erf\left[\sqrt{\frac{X}{2}}\right] + e^{-\frac{X}{2}}\right\} \tag{A.18}$$

Next, we will calculate the charge injection in the saturation region. From assumption (3) all the channel charge $-\frac{2}{3}C_g V_{ds}(T_a)=-\frac{2}{3}V_r(T_a)$ is injected to the source side. In this particular case, the channel charge is injected to ground and will not affect the T/H output voltage. Since the charge sampled on the sampling node eventually transfer to the integrating capacitor C_I, the final T/H output voltage can be calculated as

$$V_o = -\frac{Q_S}{C_I}$$

$$= -\frac{1}{C_I}\left\{ C_S[V_r(T_a)-V_i(T_a)] + (C_p+C_I)V_r(T_a) + C_{ol}\left\{V_r(T_a)-\left[V_r(T_a)+V_{T_o}-V_L\right]\right\}\right\}$$

$$= -\frac{1}{C_I}\left\{(C_S+C_I+C_p)V_r(T_a) - C_S\left\{V_{DC}+s_i\left[\frac{V_{HT}}{s_g}-\frac{V_r(T_a)}{s_g}\right]\right\} - C_{ol}(V_{T_o}-V_L)\right\}$$

$$= -\frac{1}{C_I}\left\{-C_SV_{DC} - C_{ol}(V_{T_o}-V_L) - s_i\frac{C_SV_{HT}}{s_g} + (C_S+C_I+C_p)V_r(T_a) + \frac{s_i}{s_g}C_SV_r(T_a)\right\}$$

$$= \frac{C_S}{C_I}\left\{V_{DC} + \frac{C_{ol}}{C_S}(V_{T_o}-V_L) + s_i\frac{V_{HT}}{s_g} - \frac{C_S+C_I+C_p}{C_S}V_r(T_a) - \frac{s_i}{s_g}V_r(T_a)\right\}$$

$$= V_{o_{0+}} + s_iV_{o_{1+}} + s_i^2V_{o_{2+}} + s_i^3V_{o_{3+}} + \cdots \tag{A.19}$$

where $V_{o_{0+}}$ is the term independent of s_i, $V_{o_{1+}}$ is the coefficient of s_i and $V_{o_{2+}}$ is the coefficient of s_i^2 and $V_{o_{3+}}$ is the coefficient of s_i^3. The subscript "+" indicates that the coefficients are for $s_i > 0$ case. $V_{o_{0+}}$, $V_{o_{1+}}$, $V_{o_{2+}}$ and $V_{o_{3+}}$ can be expressed as

$$V_{o_{0+}} = \frac{C_S}{C_I}\left[V_{DC} + \frac{C_{ol}}{C_S}(V_{T_o}-V_L) - \frac{(C_S+C_I+C_p)}{C_S}V_{r_{0+}}\right]$$

$$= \frac{C_S}{C_I}\left[V_{DC} + \frac{C_{ol}}{C_S}(V_{T_o}-V_L)\right]$$

$$+ \frac{(C_S+C_I+CP)}{C_I}(1+\frac{\frac{C_g}{2}+C_{ol}}{C_T})(\frac{\frac{C_g}{2}+C_{ol}}{C_T})\tau s_g\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right] \tag{A.20}$$

$$V_{o_{1+}} = \frac{C_S}{C_I}\frac{\tau}{V_{HT}}\frac{C_S}{C_T}\left[\frac{C_T}{C_S}XV_{HT} - \frac{C_S+C_I+C_p}{C_S}V_{r_{1+}} - \frac{C_T}{C_S}XV_{r_{0+}}\right] \tag{A.21}$$

$$V_{o_{2+}} = -\frac{C_S}{C_I}(\frac{\tau}{V_{HT}})^2(\frac{C_S}{C_T})^2\left[\frac{C_S+C_I+C_p}{C_S}V_{r_{2+}} + \frac{C_T}{C_S}XV_{r_{1+}}\right]$$

$$\approx -\frac{C_S}{C_I}\frac{\tau}{s_g}\frac{C_S}{C_T}f_+(X) \tag{A.22}$$

where

$$f_+(X) \approx \left[2\frac{\frac{C_g}{2}+C_{ol}}{C_T}+\frac{1+2\frac{\frac{C_g}{2}+C_{ol}}{C_T}}{2X}\right]\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right] + \frac{\frac{C_g}{2}+C_{ol}}{C_T}e^{-\frac{X}{2}} \tag{A.23}$$

is a weak function of X.

$$V_{o_{3*}} = -\frac{C_S}{C_I}(\frac{\tau}{V_{HT}})^3(\frac{C_S}{C_T})^3\left[\frac{C_S+C_I+C_p}{C_S}V_{r_{3*}} + \frac{C_T}{C_S}XV_{r_{2*}}\right] \tag{A.24}$$

(B)   Negative input signal slew rate, i.e. $s_i < 0$

Since $s_i < 0$, from Eq. (2.26) we have $V_r < 0$ and $V_{ds} = -V_r$. Therefore

$$I_r = -\beta_n(V_{gs}-V_T-\frac{V_{ds}}{2})V_{ds} = \beta_n(V_g-V_r-V_T+\frac{V_r}{2})V_r = \beta_n(V_g-V_T-\frac{V_r}{2})V_r \qquad \text{and}$$

$V_T=V_{T_0}+\gamma(\sqrt{2\Phi_B+V_r}-\sqrt{2\Phi_B})\approx V_{T_0}+\frac{\gamma}{2}(2\Phi_B)^{-\frac{1}{2}}V_r$. Define $\chi=\frac{\gamma}{2}(2\Phi_B)^{-\frac{1}{2}}$ Substituting this into

Eq. (A.1), it can be rewritten as

$$s_iC_S - C_S\frac{dV_r}{dt} = \beta_n(V_g-V_{T_0}-(1+2\chi)\frac{V_r}{2})V_r + (C_p+C_I)\frac{dV_r}{dt}$$

$$+ (\frac{C_g}{2}+C_{ol})\frac{dV_r}{dt} + s_g(\frac{C_g}{2}+C_{ol}) \tag{A.25}$$

Eq. (A.25) can be further simplified as

$$\frac{dV_r}{dt} + \frac{1}{\tau V_{HT}}(V_{HT}-s_gt-(1+2\chi)\frac{V_r}{2})V_r = \frac{s_iC_S-s_g(\frac{C_g}{2}+C_{ol})}{C_T} \tag{A.26}$$

Following the same argument as in $s_i > 0$ case, we can make an approximation by substituting V_r^2

with $s_i^2\frac{\tau^2C_S^2}{C_T^2}$. This allows us to have a closed form solution for Eq. (A.25). As can be shown

from the result of the closed form solution, this approximation can be justified. Substituting V_r^2,

we get

$$\frac{dV_r}{dt} + \frac{1}{\tau V_{HT}}(V_{HT}-s_gt)V_r = \frac{s_iC_S-s_g(\frac{C_g}{2}+C_{ol})}{C_T} + (1+2\chi)\frac{\tau s_i^2C_S^2}{2V_{HT}C_T^2}$$

$$= a_0 + s_ia_1 + (1+2\chi)s_i^2a_2 \tag{A.27}$$

Since $V_r(0)=\tau s_i\frac{C_S}{C_T}$, solving Eq. (A.26), we got

$$V_r(t) = \tau e^{\frac{V_{HT}}{2\tau s_i}(1-\frac{s_gt}{V_{HT}})^2}\left\{ s_i\frac{C_S}{C_T}e^{-\frac{V_{HT}}{2\tau s_i}} \right.$$

$$+ \left[a_0 + s_i a_1 + (1+2\chi)s_i{}^2 a_2 \right] \sqrt{\frac{\pi V_{HT}}{2\tau s_g}} \left[erf\left[\sqrt{\frac{V_{HT}}{2\tau s_g}} \right] - erf\left[\sqrt{\frac{V_{HT}}{2\tau s_g}}(1-\frac{s_g t}{V_{HT}}) \right] \right] \right] \right\}$$

$$= \tau e^{\frac{X}{2}(1-\frac{s_g t}{V_{HT}})^2} \left\{ s_i \frac{C_S}{C_T} e^{-\frac{X}{2}} \right.$$

$$+ \left[a_0 + s_i a_1 + (1+2\chi)s_i{}^2 a_2 \right] \sqrt{\frac{\pi X}{2}} \left[erf\left[\sqrt{\frac{X}{2}} \right] - erf\left[\sqrt{\frac{X}{2}}(1-\frac{s_g t}{V_{HT}}) \right] \right] \right\} \tag{A.28}$$

To calculate the voltage across the sampling switch M_1 at $t=T_a$ when the switch enters the saturation region, where T_a is the aperture time, we proceed as follow:

Since the switch enters the saturation region when $V_g - V_d - V_T = 0$, we have

$$V_g(T_a) - V_d(T_a) - V_T = V_g(T_a) - V_T = V_H - s_g T_a - V_{T_0} - \chi V_r(T_a) = 0 \tag{A.29}$$

The aperture time T_a can be calculated from Eq. (A.9) as follow

$$T_a = \frac{V_{HT}}{s_g} - \chi \frac{V_r(T_a)}{s_g} \tag{A.30}$$

Since $\chi \frac{V_r(T_a)}{s_g} \ll \frac{V_{HT}}{s_g}$, from Eq. (A.30) and Eq. (A.27), a first order approximation can be used to approximate $V_r(T_a)$ by

$$V_r(T_a) \approx \frac{V_r(\frac{V_{HT}}{s_g})}{1 + \frac{\chi}{s_g}\frac{dV_r}{dt}(\frac{V_{HT}}{s_g})}$$

$$\approx \frac{V_r(\frac{V_{HT}}{s_g})}{1 + \frac{\chi a_0}{s_g} + s_i \frac{\chi a_1}{s_g} + s_i{}^2 \frac{\chi(1+2\chi)a_2}{s_g}}$$

$$\approx \left[1 - \frac{\chi a_0}{s_g} - s_i \frac{\chi a_1}{s_g} - s_i{}^2 \frac{\chi(1+2\chi)a_2}{s_g} \right] \cdot$$

$$\tau \left\{ s_i \frac{C_S}{C_T} e^{-\frac{X}{2}} + \left[a_0 + s_i a_1 + (1+2\chi)s_i{}^2 a_2 \right] \sqrt{\frac{\pi X}{2}} erf\left[\sqrt{\frac{X}{2}} \right] \right\}$$

$$\approx \left[1 - \frac{\chi a_0}{s_g} - s_i\frac{\chi a_1}{s_g} - s_i^2\frac{\chi(1+2\chi)a_2}{s_g}\right]\left[b_0 + s_i b_1 + (1+2\chi)s_i^2 b_2\right]$$

$$\approx \left[V_{r_{0-}} + s_i V_{r_{1-}} + s_i^2 V_{r_{2-}} + s_i^3 V_{r_{3-}} + \cdots\right] \tag{A.31}$$

where $V_{r_{0-}}$ is the term independent of s_i, $V_{r_{1-}}$ is the coefficient of s_i, $V_{r_{2-}}$ is the coefficient of s_i^2 and $V_{r_{3-}}$ is the coefficient of s_i^3. The subscript "-" indicated that the coefficients are for $s_i < 0$ case. $V_{r_{0-}}$, $V_{r_{1-}}$, $V_{r_{2-}}$ and $V_{r_{3-}}$ can be expressed as

$$V_{r_{0-}} = (1 - \chi\frac{a_0}{s_g})b_0$$

$$= -(1+2\chi\frac{\frac{C_g}{2}+C_{ol}}{C_T})(\frac{\frac{C_g}{2}+C_{ol}}{C_T})\frac{V_{HT}}{X}\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right] \tag{A.32}$$

$$V_{r_{1-}} = \left[(1 - \chi\frac{a_0}{s_g})b_1 - \chi\frac{a_1}{s_g}b_0\right]$$

$$= \tau\frac{C_S}{C_T}\left\{(1+\chi\frac{\frac{C_g}{2}+C_{ol}}{C_T})e^{-\frac{X}{2}} + (1+\chi\frac{\frac{C_g}{2}+C_{ol}}{C_T})\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right]\right\} \tag{A.33}$$

$$V_{r_{2-}} = \left[(1 - \chi\frac{a_0}{s_g})(1+2\chi)b_2 - \chi\frac{a_1}{s_g}b_1 - (1+2\chi)\chi\frac{a_2}{s_g}b_0\right]$$

$$= -\frac{\tau^2 C_S^2}{C_T^2 V_{HT}}\left\{\left[\chi X - \frac{(1+2\chi)(1+2\chi\frac{\frac{C_g}{2}+C_{ol}}{C_T})}{2}\right]\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right]+\chi X e^{-\frac{X}{2}}\right\} \tag{A.34}$$

$$V_{r_{3-}} = -\left[(1+2\chi)\chi\frac{a_1}{s_g}b_2 + (1+2\chi)\chi\frac{a_2}{s_g}b_1\right]$$

$$= -\frac{\tau^3 C_S^3}{C_T^3 V_{HT}^2}(1+2\chi)\chi\frac{X}{2}\left\{2\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right]+e^{-\frac{X}{2}}\right\} \tag{A.35}$$

Next, we calculate the charge injection in the saturation region. From assumption (3) all the

channel charge $-\frac{2}{3}C_g V_{ds}(T_a) = \frac{2}{3}C_g V_r(T_a)$ is injected to the source side. In this particular case, the channel charge is injected to the sampling node. Since the charge sampled on the sampling node eventually transfer to the integrating capacitor C_I, the final T/H output voltage can be calculated as

$$V_o = -\frac{Q_S}{C_I}$$

$$= -\frac{1}{C_I}\left\{ C_S[V_r(T_a)-V_i(T_a)] + (C_p+C_I)V_r(T_a) + \frac{2}{3}V_r(T_a) \right.$$

$$\left. + C_{ol}\left\{ V_r(T_a)-\left[V_{T_o}+\chi V_r(T_a)-V_L \right] \right\} \right\}$$

$$= -\frac{1}{C_I}\left\{ (C_S+C_I+C_p)V_r(T_a) - C_S\left\{ V_{DC}+s_i\left[\frac{V_{HT}}{s_g}-\chi\frac{V_r(T_a)}{s_g} \right] \right\} \right.$$

$$\left. - C_{ol}(V_{T_o}-(1-\chi)V_r(T_a)-V_L) + \frac{2}{3}C_g V_r(T_a) \right\}$$

$$= -\frac{1}{C_I}\left\{ -C_S V_{DC} - C_{ol}(V_{T_o}-V_L) - s_i\frac{C_S V_{HT}}{s_g} \right.$$

$$\left. + \left[C_S+C_I+C_p+\frac{2}{3}C_g+(1-\chi)C_{ol} \right] V_r(T_a) + \chi\frac{s_i}{s_g}C_S V_r(T_a) \right\}$$

$$= \frac{C_S}{C_I}\left\{ V_{DC} + \frac{C_{ol}}{C_S}(V_{T_o}-V_L) + s_i\frac{V_{HT}}{s_g} \right.$$

$$\left. - \frac{C_S+C_I+C_p+\frac{2}{3}C_g+(1-\chi)C_{ol}}{C_S}V_r(T_a) - \chi\frac{s_i}{s_g}V_r(T_a) \right\}$$

$$= V_{o_0} + s_i V_{o_{1-}} + s_i^2 V_{o_{2-}} + s_i^3 V_{o_{3-}} + \cdots \qquad (A.36)$$

where V_{o_0} is the term independent of s_i, $V_{o_{1-}}$ is the coefficient of s_i and $V_{o_{2-}}$ is the coefficient of s_i^2 and $V_{o_{3-}}$ is the coefficient of s_i^3. The subscript "-" indicates that the coefficients are for $s_i < 0$

case. V_{o_0-}, V_{o_1-}, V_{o_2-} and V_{o_3-} can be expressed as

$$V_{o_0-} = \frac{C_S}{C_I}\left[V_{DC}+\frac{C_{ol}}{C_S}(V_{T_0}-V_L)-\frac{C_S+C_I+C_p+\frac{2}{3}C_g+(1-\chi)C_{ol}}{C_S}V_{r_0-} \right]$$

$$= \frac{C_S}{C_I}\left[V_{DC}+\frac{C_{ol}}{C_S}(V_{T_0}-V_L) \right] +\frac{C_S+C_I+C_p+\frac{2}{3}C_g+(1-\chi)C_{ol}}{C_I} \cdot$$

$$(1+\chi\frac{\frac{C_g}{2}+C_{ol}}{C_T})(\frac{\frac{C_g}{2}+C_{ol}}{C_T})\tau s_g\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}} \right] \qquad (A.37)$$

$$V_{o_1-} = \frac{C_S}{C_I}\frac{\tau}{V_{HT}}\frac{C_S}{C_T}\left[\frac{C_T}{C_S}XV_{HT}-\frac{C_S+C_I+C_p+\frac{2}{3}C_g+(1-\chi)C_{ol}}{C_S}V_{r_1-} \right.$$

$$\left. - \chi\frac{C_T}{C_S}XV_{r_0-} \right] \qquad (A.38)$$

$$V_{o_2-} = -\frac{C_S}{C_I}(\frac{\tau}{V_{HT}})^2(\frac{C_S}{C_T})^2\left[\frac{C_S+C_I+C_p+\frac{2}{3}C_g+(1-\chi)C_{ol}}{C_S}V_{r_2-} + \chi\frac{C_T}{C_S}XV_{r_1-} \right]$$

$$\approx -\chi\frac{C_S}{C_I}\frac{\tau}{s_g}\frac{C_S}{C_T}f_-(X) \qquad (A.39)$$

where

$$f_-(X) \approx \left[2\frac{\frac{C_g}{2}+C_{ol}}{C_T}+\frac{1}{\chi}-1+\frac{(1+2\chi)(1+2\chi\frac{\frac{C_g}{2}+C_{ol}}{C_T})}{2\chi X} \right]\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}} \right]$$

$$+ (\frac{\frac{C_g}{2}+C_{ol}}{C_T}+\frac{1}{\chi}-1)e^{-\frac{X}{2}} \qquad (A.40)$$

is a weak function of X.

$$V_{o_3-} = -\frac{C_S}{C_I}(\frac{\tau}{V_{HT}})^3(\frac{C_S}{C_T})^3\left[\frac{C_S+C_I+C_p+\frac{2}{3}C_g+(1-\chi)C_{ol}}{C_S}V_{r_3-} + \chi\frac{C_T}{C_S}XV_{r_2-} \right] \quad (A.41)$$

APPENDIX B

DIFFERENTIAL BOTTOM-PLATE T/H CIRCUIT

Using the results obtained in Appendix A, the output voltage of a differential bottom-plate T/H circuit can be calculated by combining Eq. (A.19) and Eq. (A.36). In order to make the analysis complete, we will also include the effect of mismatch of capacitors and switch. Assume the sampling capacitors, gate capacitors, overlap capacitors, integrating capacitors and "total" capacitors are $(1\pm\Delta c_s)C_S$, $(1\pm\Delta c_g)C_g$, $(1\pm\Delta c_{ol})C_{ol}$, $(1\pm\Delta c_I)C_I$ and $(1\pm\Delta c_T)C_T$ respectively, and the time constants, gate fall rates, and V_{HT}'s are $(1\pm\Delta_\tau)\tau$, $(1\pm\Delta_{s_g})s_g$ and $(1\pm\Delta v_{HT})V_{HT}$ respectively. The differential voltage $V_{o_{sff}}$ sampled on the two sampling nodes can be calculated by using the results from Appendix A, since the differential configuration is equivalent to two single-ended case driven by $V_{DC}+s_it$ and $-V_{DC}-s_it$, respectively. The differential T/H output voltage $V_{o_{sff}}$ can be calculated in the following two cases:

(A) Positive input signal slew rate, $s_i > 0$

Since $s_i > 0$, from Eq. (2.26), we have $V_{r_+}>0$ and $V_{r_-}<0$. From Eq. (A.19) and (A.31), the differential T/H output voltage can be calculated as follow

$$V_{o_{sff}} = V_{o_+} - V_{o_-}$$

$$= V_{o_0} + s_i V_{o_1} + s_i^2 V_{o_2} + s_i^3 V_{o_3} + \cdots \tag{B.1}$$

where

$$V_{o_0} = V_{o_{0+}} - V_{o_{0-}}$$

$$\approx 2\frac{C_S}{C_I}\left[V_{DC}+(\Delta c_{ol}-\Delta c_I)\frac{C_{ol}}{C_S}(V_{T_0}-V_L)\right]$$

$$+ 2(\Delta c_g+\Delta_\tau+\Delta_{s_g}-\Delta c_I)\frac{C_T}{C_I}(1+\frac{\frac{C_g}{2}+C_{ol}}{C_T})(\frac{\frac{C_g}{2}+C_{ol}}{C_T})\tau s_g\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right] \tag{B.2}$$

$$V_{o_1} = (1+\Delta_\tau+\Delta_{C_S}-\Delta_{v_{HT}}-\Delta_{C_T})V_{o_{1+}}+(1-\Delta_\tau-\Delta_{C_S}+\Delta_{v_{HT}}+\Delta_{C_T})V_{o_{1-}} \tag{B.3}$$

$$V_{o_2} = (1+2\Delta_\tau+2\Delta_{C_S}-2\Delta_{v_{HT}}-2\Delta_{C_T})V_{o_{2+}}-(1-2\Delta_\tau-2\Delta_{C_S}+2\Delta_{v_{HT}}+2\Delta_{C_T})V_{o_{2-}}$$

$$= -\frac{C_S}{C_I}\frac{\tau}{s_g}\frac{C_S}{C_T}\left\{(1+\Delta_\tau+2\Delta_{C_S}-\Delta_{C_I}-\Delta_{C_T}-\Delta_{s_s})f+\left[(1-\Delta_{v_{HT}}+\Delta_\tau+\Delta_{s_s})X\right]\right.$$

$$\left. - \chi(1-\Delta_\tau-2\Delta_{C_S}+\Delta_{C_I}+\Delta_{C_T}+\Delta_{s_s})f-\left[(1+\Delta_{v_{HT}}-\Delta_\tau-\Delta_{s_s})X\right]\right\} \tag{B.4}$$

$$V_{o_3} = (1+3\Delta_\tau+3\Delta_{C_S}-3\Delta_{v_{HT}}-3\Delta_{C_T})V_{o_{3+}}+(1-3\Delta_\tau-3\Delta_{C_S}+3\Delta_{v_{HT}}+3\Delta_{C_T})V_{o_{3-}} \tag{B.5}$$

and $V_{o_{0+}}$, $V_{o_{1+}}$, $V_{o_{2+}}$, $V_{o_{3+}}$ are evaluated using $(1+\Delta_{C_S})C_S$, $(1+\Delta_{C_I})C_I$, $(1+\Delta_{C_T})\Delta_{C_T}$, $(1+\Delta_{s_s})s_g$, $(1+\Delta_{v_{HT}})V_{HT}$, $(1+\Delta_\tau)\tau$ and $V_{o_{0-}}$, $V_{o_{1-}}$, $V_{o_{2-}}$, $V_{o_{3-}}$ are evaluated using $(1-\Delta_{C_S})C_S$, $(1-\Delta_{C_I})C_I$, $(1-\Delta_{C_T})\Delta_{C_T}$, $(1-\Delta_{s_s})s_g$, $(1-\Delta_{v_{HT}})V_{HT}$, $(1-\Delta_\tau)\tau$.

(B) **Negative input signal slew rate, $s_i < 0$**

Since $s_i < 0$, from Eq. (2.26), we have $V_{r_+}<0$ and $V_{r_-}>0$. From Eq. (A.31) and (A.19), the differential T/H output voltage can be calculated as follow

$$V_{o_{diff}} = V_{o_+} - V_{o_-} = V_{o_0} + s_i V_{o_1} + s_i^2 V_{o_2} + s_i^3 V_{o_3} + \cdots \tag{B.6}$$

where

$$V_{o_0} = V_{o_{0+}}-V_{o_{0-}}$$

$$\approx 2\frac{C_S}{C_I}\left[V_{DC}+(\Delta_{C_d}-\Delta_{C_I})\frac{C_{ol}}{C_S}(V_{T_0}-V_L)\right]$$

$$+ 2(\Delta_{C_s}+\Delta_\tau+\Delta_{s_s}-\Delta_{C_I})\frac{C_T}{C_I}(1+\frac{\frac{C_g}{2}+C_{ol}}{C_T})(\frac{\frac{C_g}{2}+C_{ol}}{C_T})\tau s_g\sqrt{\frac{\pi X}{2}}erf\left[\sqrt{\frac{X}{2}}\right] \tag{B.7}$$

$$V_{o_1} = (1-\Delta_\tau-\Delta_{C_S}+\Delta_{v_{HT}}+\Delta_{C_T})V_{o_{1+}}+(1+\Delta_\tau+\Delta_{C_S}-\Delta_{v_{HT}}-\Delta_{C_T})V_{o_{1-}} \tag{B.8}$$

$$V_{o_2} = (1-2\Delta_\tau-2\Delta_{C_S}+2\Delta_{v_{HT}}+2\Delta_{C_T})V_{o_{2+}}-(1+2\Delta_\tau+2\Delta_{C_S}-2\Delta_{v_{HT}}-2\Delta_{C_T})V_{o_{2-}}$$

$$= -\frac{C_S}{C_I}\frac{\tau}{s_g}\frac{C_S}{C_T}\left\{(1-\Delta_\tau-2\Delta_{C_S}+\Delta_{C_I}+\Delta_{C_T}+\Delta_{s_s})f+\left[(1+\Delta_{v_{HT}}-\Delta_\tau-\Delta_{s_s})X\right]\right.$$

$$- \chi(1+\Delta_\tau+2\Delta_{C_s}-\Delta_{C_l}-\Delta_{C_T}-\Delta_{s_g})f-\left[(1-\Delta_{V_{HT}}+\Delta_\tau+\Delta_{s_g})X\right]\Big\} \qquad \text{(B.9)}$$

$$V_{o_3} = (1-3\Delta_\tau-3\Delta_{C_s}+3\Delta_{V_{HT}}+3\Delta_{C_T})V_{o_{3+}}+(1+3\Delta_\tau+3\Delta_{C_s}-3\Delta_{V_{HT}}-3\Delta_{C_T})V_{o_{3-}} \qquad \text{(B.10)}$$

where $V_{o_{0+}}$, $V_{o_{1+}}$, $V_{o_{2+}}$, $V_{o_{3+}}$ are evaluated using $(1-\Delta_{C_s})C_S$, $(1-\Delta_{C_l})C_I$, $(1-\Delta_{C_T})\Delta_{C_T}$, $(1-\Delta_{s_g})s_g$, $(1-\Delta_{V_{HT}})V_{HT}$, $(1-\Delta_\tau)\tau$ and $V_{o_{0-}}$, $V_{o_{1-}}$, $V_{o_{2-}}$, $V_{o_{3-}}$ are evaluated using $(1+\Delta_{C_s})C_S$, $(1+\Delta_{C_l})C_I$, $(1+\Delta_{C_T})\Delta_{C_T}$, $(1+\Delta_{s_g})s_g$, $(1+\Delta_{V_{HT}})V_{HT}$, $(1+\Delta_\tau)\tau$.

APPENDIX C

DIFFERENTIAL BOTTOM-PLATE T/H CIRCUIT WITH

A SINGLE SAMPLING SWITCH

Using the same assumptions as in Appendix A and following the same procedure, a more accurate calculation of the differential T/H circuit with a single sampling switch is described below. In order to make the analysis complete, we will also include the effect of mismatch of capacitors and switches. Assume the sampling capacitors, integrating capacitors, parasitic capacitors and gate-drain overlap capacitors are $(1\pm\Delta_{C_s})C_s$, $(1\pm\Delta_{C_o})C_p$, $(1\pm\Delta_{C_{oa}})C_{ol}$ and $(1\pm\Delta_{C_i})C_i$ respectively. The equivalent circuit of a differential bottom-plate T/H circuit with a single sampling switch is shown in Fig. C.1.
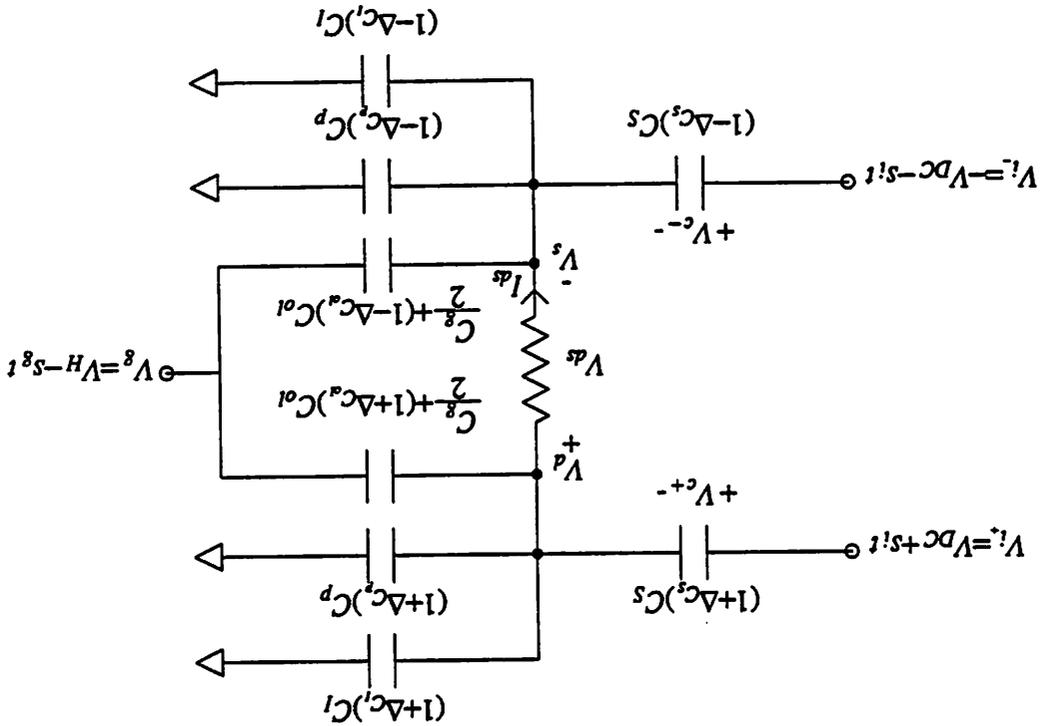

Fig. C.1 Equivalent Circuit of Differential T/H Circuit with a Single Sampling Switch

From Fig. C.1, we can write KCL equations for the positive and negative sampling node in Eq.

(C.1) and Eq. (C.2) respectively.

$$(1+\Delta_{C_s})C_S \frac{d(V_{i_-}-V_d)}{dt} = I_{ds} + \left[(1+\Delta_{C_p})C_p + (1+\Delta_{C_l})C_l\right] \frac{dV_d}{dt}$$

$$+ \left[\frac{C_g}{2} + (1+\Delta_{C_{ol}})C_{ol}\right] \frac{d(V_d-V_g)}{dt} \qquad (C.1)$$

$$(1-\Delta_{C_s})C_S \frac{d(V_{i_-}-V_s)}{dt} = -I_{ds} + \left[(1-\Delta_{C_p})C_p + (1-\Delta_{C_l})C_l\right] \frac{dV_s}{dt}$$

$$+ \left[\frac{C_g}{2} + (1-\Delta_{C_{ol}})C_{ol}\right] \frac{d(V_s-V_g)}{dt} \qquad (C.2)$$

where we define $V_{\Sigma}=V_d+V_s$ and $C_T=C_S+C_l+\frac{C_g}{2}+C_p$. Summing Eq. (C.1) and Eq.(C.2) together, we have

$$\frac{dV_{\Sigma}}{dt} = -2s_g \frac{\frac{C_g}{2}+C_{ol}}{C_T} + 2\Delta_{C_s}s_i \frac{C_S}{C_T}$$

$$- \frac{\Delta_{C_s}C_S + \Delta_{C_l}C_l + \Delta_{C_p}C_p + \Delta_{C_{ol}}C_{ol}}{C_T} \frac{dV_{ds}}{dt} \qquad (C.3)$$

The differential T/H output voltage $V_{o_{diff}}$ can be calculated in the following two cases:

(A) Positive input signal slew rate, i.e. $s_i > 0$:

For $s_i > 0$, from Eq. (2.51), we have $V_{ds} > 0$. Express I_{ds} as a function of V_{ds} and V_{Σ}, we have

$$I_{ds} = \beta_n(V_g - V_s - V_T - \frac{V_{ds}}{2})V_{ds} = \beta_n\left[V_H - s_g t - V_s - (V_{T_o} + \chi V_s) - \frac{V_{ds}}{2}\right]V_{ds}$$

$$= \beta_n\left[V_{HT} - s_g t - (\frac{1}{2} + \frac{\chi}{2})V_{\Sigma} + \frac{\chi}{2}V_{ds}\right]V_{ds} \qquad (C.4)$$

Subtract Eq. (C.1) from Eq. (C.2) and combine with I_{ds} from Eq. (C.4), we get

$$\frac{dV_{ds}}{dt} + \frac{1}{\tau V_{HT}}\left[V_{HT} - s_g t - (\frac{1}{2} + \frac{\chi}{2})V_{\Sigma} + \frac{\chi}{2}V_{ds}\right]V_{ds}$$

$$= 2\frac{s_i C_S - s_g \Delta_{C_{ol}}C_{ol}}{C_T} - \frac{\Delta_{C_s}C_S + \Delta_{C_l}C_l + \Delta_{C_p}C_p + \Delta_{C_{ol}}C_{ol}}{C_T} \frac{dV_{\Sigma}}{dt} \qquad (C.5)$$

Integrating Eq. (C.3), we get

$$V_{\Sigma}(t) - V_{\Sigma}(0) = -2\left[s_g\frac{\frac{C_g}{2}+C_{ol}}{C_T} - s_i\Delta C_s\frac{C_S}{C_T}\right]t$$

$$-\frac{\Delta_{C_s}C_S+\Delta_{C_i}C_I+\Delta_{C_p}C_p+\Delta_{C_{ol}}C_{ol}}{C_T}\left[V_{ds}(t)-V_{ds}(0)\right] \tag{C.6}$$

where $V_{\Sigma}(0)=0$ because the two common mode reset switches reset both sampling node just before the sampling switch turns off. Since $V_{ds}(0)=2s_i\tau\frac{C_S}{C_T}$ Combining Eq. (C.5) and Eq. (C.6) and approximate the term $V_{ds}{}^2$ in Eq. (C.5) by $4s_i{}^2\tau^2(\frac{C_S}{C_T})^2$, we have

$$\frac{dV_{ds}}{dt}+\frac{1}{\tau V_{HT}}(V_{HT}'-s_g't)V_{ds} = 2\frac{s_iC_S-s_g\Delta C_{ol}C_{ol}}{C_T} - \frac{\Delta_{C_s}C_S+\Delta_{C_i}C_I+\Delta_{C_p}C_p+\Delta_{C_{ol}}C_{ol}}{C_T}\frac{dV_{\Sigma}}{dt}$$

$$-\left[\chi+(1+\chi)\frac{\Delta_{C_s}C_S+\Delta_{C_i}C_I+\Delta_{C_p}C_p+\Delta_{C_{ol}}C_{ol}}{C_T}\right]\frac{2s_i{}^2\tau C_S{}^2}{V_{HT}C_T{}^2} \tag{C.7}$$

where

$$s_g' = s_g - (1+\chi)\left[s_g\frac{\frac{C_g}{2}+C_{ol}}{C_T}-s_i\Delta C_s\frac{C_S}{C_T}\right] \tag{C.8}$$

and

$$V_{HT}' = V_{HT} - (1+\chi)\frac{(\Delta_{C_s}C_S+\Delta_{C_p}C_p+\Delta_{C_{ol}}C_{ol})}{C_T}s_i\tau\frac{C_S}{C_T} \tag{C.9}$$

Combine Eq. (C.3) with Eq. (C.7), we can rewrite Eq. (C.7) as follow

$$\frac{dV_{ds}}{dt} + \frac{1}{\tau V_{HT}}(V_{HT}'-s_g't)V_{ds}$$

$$\approx 2\frac{\tau s_g[(\frac{C_g}{2}+C_{ol})(\Delta_{C_s}C_S+\Delta_{C_i}C_I+\Delta_{C_p}C_p+\Delta_{C_{ol}}C_{ol})-\Delta_{C_{ol}}C_{ol}C_T]}{C_T{}^2} + 2\frac{s_iC_S}{C_T}$$

$$-\left[\chi+(1+\chi)\frac{(\Delta_{C_s}C_S+\Delta_{C_i}C_I+\Delta_{C_p}C_p+\Delta_{C_{ol}}C_{ol})}{C_T}\right]\frac{2s_i{}^2\tau C_S{}^2}{V_{HT}C_T{}^2}$$

$$\simeq A_0 + s_i A_1 + s_i^2 (A_2 + A_2') \qquad (C.10)$$

where

$$A_0 = 2\frac{\tau s_g [(\frac{C_g}{2} + C_{ol})(\Delta_{C_s} C_S + \Delta_{C_I} C_I + \Delta_{C_p} C_p + \Delta_{C_{al}} C_{ol}) - \Delta_{C_{al}} C_{ol} C_T]}{C_T^2} \qquad (C.11)$$

$$A_1 = 2\frac{C_S}{C_T} \qquad (C.12)$$

$$A_2 = -2\chi\frac{\tau C_S^2}{V_{HT} C_T^2} \qquad (C.13)$$

$$A_2' = -2(1+\chi)\frac{\Delta_{C_s} C_S + \Delta_{C_I} C_I + \Delta_{C_p} C_p + \Delta_{C_{al}} C_{ol}}{C_T}\frac{\tau C_S^2}{V_{HT} C_T^2} \qquad (C.14)$$

Solving Eq. (C.10), we get

$$V_{ds}(t) = \tau e^{\frac{V_{HT}^2}{2\tau s_g' V_{HT}}(1-\frac{s_g'}{V_{HT}}t)^2} \left\{ \left[A_0 + s_i A_1 + s_i^2 (A_2 + A_2') \right] \cdot \right.$$

$$\sqrt{\frac{\pi V_{HT}}{2\tau s_g}}\left[erf\left[\sqrt{\frac{V_{HT}^2}{2\tau s_g' V_{HT}}} \right] - erf\left[\sqrt{\frac{V_{HT}^2}{2\tau s_g' V_{HT}}}(1-\frac{s_g'}{V_{HT}}t) \right] \right]$$

$$\left. + 2s_i\frac{C_S}{C_T}e^{-\frac{V_{HT}^2}{2\tau s_g' V_{HT}}} \right\}$$

$$= \tau e^{\frac{\chi'}{2}\frac{V_{HT}'}{V_{HT}}(1-\frac{s_g'}{V_{HT}}t)^2} \left\{ \left[A_0 + s_i A_1 + s_i^2 (A_2 + A_2') \right] \cdot \right.$$

$$\sqrt{\frac{\pi \chi'}{2}\frac{V_{HT}}{V_{HT}'}}\left[erf\left[\sqrt{\frac{\chi'}{2}\frac{V_{HT}'}{V_{HT}}} \right] - erf\left[\sqrt{\frac{\chi'}{2}\frac{V_{HT}'}{V_{HT}}}(1-\frac{s_g'}{V_{HT}}t) \right] \right]$$

$$\left. + 2s_i\frac{C_S}{C_T}e^{-\frac{\chi'}{2}\frac{V_{HT}'}{V_{HT}}} \right\} \qquad (C.15)$$

where we define a new variable $X' = \frac{V_{HT}'}{\tau s_g}$. Since $\frac{V_{HT}'}{s_g}$ is the gate fall time modified to correct

the effect of mismatch and charge injection, X' is the ratio of modified gate fall time to the T/H

network time constant. The switch enters the saturation region at time $t = T_a$ when $V_g - V_d - V_T = 0$,

we have

$$V_g(T_a) - V_d(T_a) - V_T = V_g(T_a) - V_d(T_a) - \left[V_{T_0} + \chi V_s(T_a) \right]$$

$$= V_{HT} - s_i T_a - \frac{1}{2} \left[V_\Sigma(T_a) + V_{ds}(T_a) \right] - \frac{\chi}{2} \left[V_\Sigma(T_a) - V_{ds}(T_a) \right] = 0 \qquad (C.16)$$

The aperture time T_a can be calculated from Eq. (C.16) as follow

$$T_a = \frac{V_{HT}'}{s_g} - (c + c') \frac{V_{ds}(T_a)}{s_g} \qquad (C.17)$$

where $c = \frac{1}{2} - \frac{\chi}{2}$ and $c' = -(\frac{1}{2} + \frac{\chi}{2}) \frac{(\Delta_{C_s} C_S + \Delta_{C_I} C_I + \Delta_{C_p} C_p + \Delta_{C_{ol}} C_{ol})}{C_T}$ Since

$(c + c') \frac{V_{ds}(T_a)}{s_g} \ll \frac{V_{HT}'}{s_g}$, from Eq. (C.16) and Eq. (C.10), a first order approximation can be used

to approximate $V_{ds}(T_a)$ by

$$V_{ds}(T_a) \approx \frac{V_{ds}(\frac{V_{HT}'}{s_g})}{1 + \frac{(c + c')}{s_g} \frac{dV_{ds}}{dt}(\frac{V_{HT}'}{s_g})}$$

$$\approx \frac{V_{ds}(\frac{V_{HT}'}{s_g})}{1 + \frac{(c + c')}{s_g} [A_0 + s_i A_1 + s_i^2 (A_2 + A_2')]}$$

$$\approx \left\{ 1 - \frac{(c + c')}{s_g} \left[A_0 + s_i A_1 + s_i^2 (A_2 + A_2') \right] \right\} \tau \left\{ 2 s_i \frac{C_S}{C_T} e^{-\frac{X' V_{HT}'}{2 V_{HT}}} \right.$$

$$\left. + \left[A_0 + s_i A_1 + s_i^2 (A_2 + A_2') \right] \sqrt{\frac{\pi X'}{2} \frac{V_{HT}'}{V_{HT}}} erf \left[\sqrt{\frac{X'}{2} \frac{V_{HT}'}{V_{HT}}} \right] \right\}$$

$$\approx \left\{1-\frac{(c+c')}{s_g}\left[A_0+s_iA_1+s_i^2(A_2+A_2')\right]\right\}\left[B_0 + s_iB_1 + s_i^2(B_2+B_2')\right]$$

$$\approx V_{ds_0} + s_iV_{ds_1} + s_i^2V_{ds_2} + s_i^3V_{ds_3} + \cdots \tag{C.18}$$

where

$$B_0 = 2\frac{\tau s_g\,[(\frac{C_g}{2}+C_{ol})(\Delta_{C_s}C_S+\Delta_{C_i}C_I+\Delta_{C_p}C_p+\Delta_{C_d}C_{ol})-\Delta_{C_d}C_{ol}C_T]}{C_T^2}\cdot$$

$$\sqrt{\frac{\pi X'}{2}\frac{V_{HT}}{V_{HT}}}erf\left[\sqrt{\frac{X'}{2}\frac{V_{HT}'}{V_{HT}}}\right] \tag{C.19}$$

$$B_1 = 2\tau\frac{C_S}{C_T}\left[e^{-\frac{X'}{2}\frac{V_{HT}'}{V_{HT}}} + \sqrt{\frac{\pi X'}{2}\frac{V_{HT}}{V_{HT}}}erf\left[\sqrt{\frac{X'}{2}\frac{V_{HT}'}{V_{HT}}}\right]\right] \tag{C.20}$$

$$B_2 = -2\chi\frac{\tau^2C_S^2}{V_{HT}C_T^2}\sqrt{\frac{\pi X'}{2}\frac{V_{HT}}{V_{HT}}}erf\left[\sqrt{\frac{X'}{2}\frac{V_{HT}'}{V_{HT}}}\right] \tag{C.21}$$

$$B_2' = -2(1+\chi)\frac{\Delta_{C_s}C_S+\Delta_{C_i}C_I+\Delta_{C_p}C_p+\Delta_{C_d}C_{ol}}{C_T}\frac{\tau^2C_S^2}{V_{HT}C_T^2}\cdot$$

$$\sqrt{\frac{\pi X'}{2}\frac{V_{HT}}{V_{HT}}}erf\left[\sqrt{\frac{X'}{2}\frac{V_{HT}'}{V_{HT}}}\right] \tag{C.22}$$

where $\frac{\tau s_i}{V_{HT}}\frac{C_S}{C_T}=\frac{V_{ds}(0)}{2V_{HT}}$ is a dimensionless quantity used to gauge the performance of the T/H

circuit. The smaller this quantity, i.e. smaller time constant τ, smaller input signal slew rate s_i

and larger gate overdrive VHT etc., the lower the distortion. Also, V_{ds_0} is the term independent of

$\frac{\tau s_i}{V_{HT}}\frac{C_S}{C_T}$, V_{ds_1} is the coefficient of $\frac{\tau s_i}{V_{HT}}\frac{C_S}{C_T}$, V_{ds_2} is the coefficient of $(\frac{\tau s_i}{V_{HT}}\frac{C_S}{C_T})^2$ and V_{ds_3} is

the coefficient of $(\frac{\tau s_i}{V_{HT}}\frac{C_S}{C_T})^3$. V_{ds_0}, V_{ds_1}, V_{ds_2} and V_{ds_3} can be represented as

$$V_{ds_0} = \left[1-(c+c')\frac{A_0}{s_g}\right]B_0 \tag{C.23}$$

$$V_{ds_1} = \left[1-(c+c')\frac{A_0}{s_g}\right]B_1-(c+c')\frac{A_1}{s_g}B_0 \tag{C.24}$$

$$V_{ds_2} = \left[1-(c+c')\frac{A_0}{s_g}\right](B_2+B_2')-(c+c')\frac{A_1}{s_g}B_1-(c+c')\frac{(A_2+A_2')}{s_g}B_0 \tag{C.25}$$

$$V_{ds_3} = -(c+c')\frac{A_1}{s_g}(B_2+B_2')-(c+c')\frac{(A_2+A_2')}{s_g}B_1 \tag{C.26}$$

Next, we will calculate the charge injection in the saturation region. From assumption (3) in Appendix A all the channel charge $-\frac{2}{3}C_g V_{ds}(T_a)=-\frac{2}{3}V_{ds}(T_a)$ is injected to the source side. In this particular case, the channel charge is injected to the negative sampling node. Since the charge sampled on the sampling node eventually transfer to the integrating capacitor C_I, the final differential T/H output voltage can be calculated as

$$V_{o_{diff}} = -\frac{1}{(1+\Delta_{C_I})C_I}\left\{(1+\Delta_{C_S})C_S\left[V_d(T_a)-V_{i_+}(T_a)\right]+\left[(1+\Delta_{C_I})C_I+(1+\Delta_{C_p})C_p\right]V_d(T_a)\right.$$

$$\left.+(1+\Delta_{C_{ol}})C_{ol}\left[V_d(T_a)-V_g(T_a)+V_L\right]\right\}$$

$$-\frac{1}{(1-\Delta_{C_I})C_I}\left\{(1-\Delta_{C_S})C_S[V_s(T_a)-V_{i_-}(T_a)]+\left[(1-\Delta_{C_I})C_I+(1-\Delta_{C_p})C_p\right]V_s(T_a)\right.$$

$$\left.-\frac{2}{3}C_g V_{ds}(T_a)+(1-\Delta_{C_{ol}})C_{ol}\left[V_s(T_a)-V_g(T_a)+V_L\right]\right\}$$

$$= -\frac{1}{C_I}\left\{(C_S+C_p+C_{ol}+\frac{2}{3}C_g)V_{ds}(T_a)-C_S(2V_{DC}+2s_iT_a)\right.$$

$$\left.+\left[(\Delta_{C_S}-\Delta_{C_I})C_S+(\Delta_{C_p}-\Delta_{C_I})C_p+(\Delta_{C_{ol}}-\Delta_{C_I})C_{ol}\right]V_\Sigma(T_a)-2(\Delta_{C_{ol}}-\Delta_{C_I})C_{ol}(V_H-s_gT_a-V_L)\right\}$$

$$\approx -\frac{1}{C_I}\left\{-2C_S V_{DC}+(C_S+C_p+C_{ol}+\frac{2}{3}C_g)V_{ds}(T_a)-2\left[s_iC_S-s_g(\Delta_{C_{ol}}-\Delta_{C_I})C_{ol}\right]\left[\frac{V_{HT}'}{s_g}-(c+c')\frac{V_{ds}(T_a)}{s_g}\right]\right.$$

$$\left.-2\left[(\Delta_{C_S}-\Delta_{C_I})C_S+(\Delta_{C_p}-\Delta_{C_I})C_p+(\Delta_{C_{ol}}-\Delta_{C_I})C_{ol}\right]\frac{s_g(\frac{C_g}{2}+C_{ol})-s_i\Delta_{C_S}C_S}{C_T}\left[\frac{V_{HT}'}{s_g}-(c+c')\frac{V_{ds}(T_a)}{s_g}\right]\right.$$

$$-2(\Delta c_\omega - \Delta c_i)C_{ol}(V_H - V_L)\}$$

$$\approx V_{oo} + s_i V_{o1} + s_i^2 V_{o2} + s_i^3 V_{o3} + \cdots \qquad (C.27)$$

where V_{oo} is the term independent of s_i, V_{o1} is the coefficient of s_i, V_{o2} is the coefficient of s_i^2 and V_{o3} is the coefficient of s_i^3.

It can be shown that V_{oo} and V_{o2} have the following form:

$$V_{oo} \approx 2\frac{C_I}{C_S}\left[V_{DC} + (\Delta c_\omega - \Delta c_i)\frac{C_{ol}}{C_S}(V_{T_o} - V_L)\right]$$
$$+ 2\left[\Delta c_r \frac{(\frac{C_g}{2} + C_{ol})}{C_I} - \Delta c_\omega \frac{C_{ol}}{C_I}\right]\tau s_g \sqrt{\frac{\pi X}{2}}\, erf\left[\sqrt{\frac{X}{2}}\right]$$

where V_{offset} is the input-referred offset and can be expressed as

$$\approx 2\frac{C_I}{C_S}\left[V_{DC} + V_{offset}\right] \qquad (C.28)$$

$$V_{offset} \approx (\Delta c_\omega - \Delta c_i)\frac{C_{ol}}{C_S}(V_{T_o} - V_L)$$
$$+ \left[\Delta c_r \frac{(\frac{C_g}{2} + C_{ol})}{C_S} - \Delta c_\omega \frac{C_{ol}}{C_S}\right]\tau s_g \sqrt{\frac{\pi X}{2}}\, erf\left[\sqrt{\frac{X}{2}}\right] \qquad (C.29)$$

and

$$V_{o2} \approx -2(1-\chi)\frac{C_S}{C_S}\frac{1}{\tau}\frac{s_g}{C_S}\frac{C_I}{C_I} \qquad (C.30)$$

(B) Negative input signal slew rate, i.e. $s_i < 0$:

For $s_i < 0$, from Eq. (2.57), we have $V_{ds} < 0$. Express I_{ds} as a function of V_{ds} and V_{Σ}, we have

$$I_{ds} = \beta_n(V_g - V_d - V_T - (V_{T_o} + \chi V_d) + \frac{V_{ds}}{2})V_{ds} = \beta_n\left[V_H - s_g t - V_d - (V_{T_o} + \chi V_d) + \frac{V_{ds}}{2}\right]V_{ds}$$

$$= \beta_n\left[V_{ds} V_H - s_g t - (\frac{1}{2} + \frac{\chi}{2})V_\Sigma V_{ds} - \frac{\chi}{2}V_{ds}\right]V_{ds} \qquad (C.31)$$

Subtract Eq. (C.1) from Eq. (C.2) and combine with I_{ds} from Eq. (C.25), we get

$$\frac{dV_{ds}}{dt} + \frac{1}{\tau V_{HT}}\left[V_{HT} - s_g t - (\frac{1}{2} + \frac{\chi}{2})V_{\Sigma} - \frac{\chi}{2}V_{ds}\right]V_{ds}$$

$$= 2\frac{s_i C_S - s_g \Delta_{C_\alpha} C_{ol}}{C_T} - \frac{\Delta_{C_s} C_S + \Delta_{C_l} C_l + \Delta_{C_p} C_p + \Delta_{C_\alpha} C_{ol}}{C_T}\frac{dV_{\Sigma}}{dt} \qquad (C.32)$$

Since $V_{ds}(0) = 2s_i \tau \frac{C_S}{C_T}$ Combining Eq. (C.32) and Eq. (C.6) and approximate the term V_{ds}^2 in

Eq. (C.32) by $4s_i^2 \tau^2 (\frac{C_S}{C_T})^2$, we have

$$\frac{dV_{ds}}{dt} + \frac{1}{\tau V_{HT}}(V_{HT}' - s_g't)V_{ds} = 2\frac{s_i C_S - s_g \Delta_{C_\alpha} C_{ol}}{C_T} - \frac{\Delta_{C_s} C_S + \Delta_{C_l} C_l + \Delta_{C_p} C_p + \Delta_{C_\alpha} C_{ol}}{C_T}\frac{dV_{\Sigma}}{dt}$$

$$+ \left[\chi - (1+\chi)\frac{\Delta_{C_s} C_S + \Delta_{C_l} C_l + \Delta_{C_p} C_p + \Delta_{C_\alpha} C_{ol}}{C_T}\right]\frac{2s_i^2 \tau C_S^2}{V_{HT} C_T^2} \qquad (C.33)$$

Combine Eq. (C.3) with Eq. (C.33), we can rewrite Eq. (C.33) as follow

$$\frac{dV_{ds}}{dt} + \frac{1}{\tau V_{HT}}(V_{HT}' - s_g't)V_{ds}$$

$$\approx 2\frac{\tau s_g[(\frac{C_g}{2} + C_{ol})(\Delta_{C_s} C_S + \Delta_{C_l} C_l + \Delta_{C_p} C_p + \Delta_{C_\alpha} C_{ol}) - \Delta_{C_\alpha} C_{ol} C_T]}{C_T^2} + 2\frac{s_i C_S}{C_T}$$

$$+ \left[\chi - (1+\chi)\frac{(\Delta_{C_s} C_S + \Delta_{C_l} C_l + \Delta_{C_p} C_p + \Delta_{C_\alpha} C_{ol})}{C_T}\right]\frac{2s_i^2 \tau C_S^2}{V_{HT} C_T^2}$$

$$\approx A_0 + s_i A_1 + s_i^2(-A_2 + A_2') \qquad (C.34)$$

Solving Eq. (C.34), we get

$$V_{ds}(t) = \tau e^{\frac{V_{HT}^2}{2\tau s_i' V_{HT}}(1 - \frac{s_g'}{V_{HT}}t)^2}\left\{\left[A_0 + s_i A_1 + s_i^2(-A_2 + A_2')\right] \cdot \right.$$

$$\left. \sqrt{\frac{\pi V_{HT}}{2\tau s_g'}}\left[erf\left[\sqrt{\frac{V_{HT}^2}{2\tau s_g' V_{HT}}}\right] - erf\left[\sqrt{\frac{V_{HT}^2}{2\tau s_g' V_{HT}}(1 - \frac{s_g'}{V_{HT}}t)}\right]\right]\right\}$$

$$+ 2s_i \frac{C_S}{C_T} e^{-\frac{V_{HT}^2}{2\tau s_s V_{HT}}} \Bigg]$$

$$= \tau e^{\frac{X' V_{HT}'}{2 V_{HT}}(1-\frac{s_g'}{V_{HT}}t)^2} \left\{ \left[A_0 + s_i A_1 + s_i^2(-A_2+A_2') \right] \cdot \right.$$

$$\sqrt{\frac{\pi X'}{2} \frac{V_{HT}}{V_{HT}'}} \left[erf\left[\sqrt{\frac{X'}{2} \frac{V_{HT}'}{V_{HT}}} \right] - erf\left[\sqrt{\frac{X'}{2} \frac{V_{HT}'}{V_{HT}}}(1-\frac{s_g'}{V_{HT}}t) \right] \right]$$

$$\left. + 2s_i \frac{C_S}{C_T} e^{-\frac{X' V_{HT}'}{2 V_{HT}}} \right\}$$
(C.35)

The switch enters the saturation region at time $t=T_a$ when $V_g-V_s-V_T=0$, we have

$$V_g(T_a)-V_s(T_a)-V_T = V_g(T_a)-V_s(T_a)-\left[V_{T_0}+\chi V_d(T_a) \right]$$

$$= V_{HT}-s_i T_a-\frac{1}{2}\left[V_\Sigma(T_a)-V_{ds}(T_a) \right]-\frac{\chi}{2}\left[V_\Sigma(T_a)+V_{ds}(T_a) \right] = 0$$
(C.36)

The aperture time T_a can be calculated from Eq. (C.36) as follow

$$T_a = \frac{V_{HT}'}{s_g} - (-c+c')\frac{V_{ds}(T_a)}{s_g}$$
(C.37)

Since $(-c+c')\dfrac{V_{ds}(T_a)}{s_g} \ll \dfrac{V_{HT}'}{s_g}$, from Eq. (C.36) and Eq. (C.34), a first order approximation can

be used to approximate $V_{ds}(T_a)$ by

$$V_{ds}(T_a) \approx \frac{V_{ds}(\frac{V_{HT}'}{s_g})}{1+\frac{(-c+c')}{s_g}\frac{dV_{ds}}{dt}(\frac{V_{HT}'}{s_g})}$$

$$\approx \frac{V_{ds}(\frac{V_{HT}'}{s_g})}{1+\frac{(-c+c')}{s_g}[A_0+s_i A_1+s_i^2(-A_2+A_2')]}$$

$$\approx \left\{ 1-\frac{(-c+c')}{s_g}\left[A_0+s_i A_1+s_i^2(-A_2+A_2') \right] \right\} \left\{ 2s_i \frac{C_S}{C_T} e^{-\frac{X' V_{HT}'}{2 V_{HT}}} \right.$$

$$+\left[A_0 + s_i A_1 + s_i^2(-A_2+A_2')\right] \sqrt{\frac{\pi X'}{2}\frac{V_{HT}}{V_{HT}'}} erf\left[\sqrt{\frac{X'}{2}\frac{V_{HT}'}{V_{HT}}}\right]\Bigg\}$$

$$\approx \left\{1-\frac{(-c+c')}{s_g}\left[A_0+s_iA_1+s_i^2(-A_2+A_2')\right]\right\}\left[B_0 + s_iB_1 + s_i^2(-B_2+B_2')\right]$$

$$\approx V_{ds_0} + s_i V_{ds_1} + s_i^2 V_{ds_2} + s_i^3 V_{ds_3} + \cdots \qquad (C.38)$$

where V_{ds_0} is the term independent of s_i, V_{ds_1} is the coefficient of s_i, V_{ds_2} is the coefficient of s_i^2 and V_{ds_3} is the coefficient of s_i^3. V_{ds_0}, V_{ds_1}, V_{ds_2} and V_{ds_3} can be represented as

$$V_{ds_0} = \left[1-(-c+c')\frac{A_0}{s_g}\right]B_0 \qquad (C.39)$$

$$V_{ds_1} = \left[1-(-c+c')\frac{A_0}{s_g}\right]B_1-(c+c')\frac{A_1}{s_g}B_0 \qquad (C.40)$$

$$V_{ds_2} = \left[1-(-c+c')\frac{A_0}{s_g}\right](-B_2+B_2')-(-c+c')\frac{A_1}{s_g}B_1-(-c+c')\frac{(-A_2+A_2')}{s_g}B_0 \qquad (C.41)$$

$$V_{ds_3} = -(-c+c')\frac{A_1}{s_g}(-B_2+B_2')-(-c+c')\frac{(-A_2+A_2')}{s_g}B_1 \qquad (C.42)$$

Next, we will calculate the charge injection in the saturation region. From assumption (3) in Appendix A all the channel charge $\frac{2}{3}C_g V_{ds}(T_a)$ is injected to the source side. In this particular case, the channel charge is injected to the positive sampling node. Since the charge sampled on the sampling node eventually transfer to the integrating capacitor C_I, the final differential T/H output voltage can be calculated as

$$V_{o_{diff}} = -\frac{1}{(1+\Delta_{C_I})C_I}\Bigg\{(1+\Delta_{C_s})C_S\left[V_d(T_a)-V_{i_+}(T_a)\right]+\left[(1+\Delta_{C_I})C_I+(1+\Delta_{C_p})C_P\right]V_d(T_a)$$

$$+(1+\Delta_{C_{ol}})C_{ol}\left[V_d(T_a)-V_g(T_a)+V_L\right]+\frac{2}{3}C_g V_{ds}(T_a)\Bigg\}$$

$$- \frac{1}{(1-\Delta_{C_I})C_I} \left\{ (1-\Delta_{C_S})C_S [V_s(T_a)-V_{i\_}(T_a)] + \left[(1-\Delta_{C_I})C_I + (1-\Delta_{C_p})C_p \right] V_s(T_a) \right.$$

$$\left. -\frac{2}{3}C_g V_{ds}(T_a) + (1-\Delta_{C_{al}})C_{ol} \left[V_s(T_a) - V_g(T_a) + V_L \right] \right\}$$

$$= -\frac{1}{C_I} \left\{ (C_S + C_p + C_{ol} + \frac{2}{3}C_g)V_{ds}(T_a) - C_S(2V_{DC} + 2s_i T_a) \right.$$

$$\left. + \left[(\Delta_{C_s} - \Delta_{C_I})C_S + (\Delta_{C_p} - \Delta_{C_I})C_p + (\Delta_{C_{al}} - \Delta_{C_I})C_{ol} \right] V_{\sum}(T_a) - 2(\Delta_{C_{al}} - \Delta_{C_I})C_{ol}(V_H - s_g T_a - V_L) \right\}$$

$$\approx -\frac{1}{C_I} \left\{ -2C_S V_{DC} + (C_S + C_p + C_{ol} + \frac{2}{3}C_g)V_{ds}(T_a) - 2 \left[s_i C_S - s_g (\Delta_{C_{al}} - \Delta_{C_I})C_{ol} \right] \left[\frac{V_{HT}'}{s_g} - (c+c') \frac{V_{ds}(T_a)}{s_g} \right] \right.$$

$$-2 \left[(\Delta_{C_s} - \Delta_{C_I})C_S + (\Delta_{C_p} - \Delta_{C_I})C_p + (\Delta_{C_{al}} - \Delta_{C_I})C_{ol} \right] \frac{s_g(\frac{C_g}{2} + C_{ol}) - s_i \Delta_{C_s} C_S}{C_T} \left[\frac{V_{HT}'}{s_g} - (c+c') \frac{V_{ds}(T_a)}{s_g} \right]$$

$$\left. -2(\Delta_{C_{al}} - \Delta_{C_I})C_{ol}(V_H - V_L) \right\}$$

$$\approx V_{o_0} + s_i V_{o_1} + s_i^2 V_{o_2} + s_i^3 V_{o_3} + \cdots \tag{C.43}$$

where V_{o_0} is the term independent of s_i, V_{o_1} is the coefficient of s_i, V_{o_2} is the coefficient of s_i^2 and V_{o_3} is the coefficient of s_i^3.

It can be shown that V_{o_0} and V_{o_2} have the following form:

$$V_{o_0} \approx 2\frac{C_S}{C_I} \left[V_{DC} + (\Delta_{C_{al}} - \Delta_{C_I})\frac{C_{ol}}{C_S}(V_{T_0} - V_L) \right]$$

$$+ 2 \left[\Delta_{C_T} \frac{(\frac{C_g}{2} + C_{ol})}{C_I} - \Delta_{C_{al}} \frac{C_{ol}}{C_I} \right] \tau s_g \sqrt{\frac{\pi X}{2}} erf \left[\sqrt{\frac{X}{2}} \right]$$

$$\approx 2\frac{C_S}{C_I} \left[V_{DC} + V_{offset} \right] \tag{C.44}$$

where V_{offset} is the input-referred offset and can be expressed as

$$V_{offset} \approx (\Delta_{C_{ol}} - \Delta_{C_I}) \frac{C_{ol}}{C_S}(V_{T_0} - V_L)$$

$$+ 2\left[\Delta_{C_T}\frac{(\frac{C_g}{2} + C_{ol})}{C_S} - \Delta_{C_{ol}}\frac{C_{ol}}{C_S}\right] \tau s_g \sqrt{\frac{\pi X}{2}} erf\left[\sqrt{\frac{X}{2}}\right] \qquad (C.45)$$

and

$$V_{o_2} \approx 2(1-\chi)\frac{C_S}{C_I}\frac{\tau}{s_g}\frac{C_S}{C_T} \qquad (C.46)$$

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