A 1-BIT/CYCLE ALGORITHMIC ANALOG-TO-DIGITAL CONVERTER WITHOUT HIGH-PRECISION COMPARATORS

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Gani Jusuf and Paul R. Gray

Memorandum No. UCB/ERL M90/69

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ABSTRACT

A new-improved algorithmic Analog-to-Digital (A/D) converter architecture which is capable of resolving 1 bit-per-clock cycle is investigated. Many analog circuit design techniques are incorporated into the design of the proposed A/D converter so that non-idealities from operational amplifier(op-amp), CMOS switches, comparators, and others can be canceled or reduced. An 8-bit 125Khz A/D converter prototype based on the proposed architecture was designed and laid-out in a 3-μm, CMOS process and fabricated through MOSIS.

The prototype is expected to have 0.24 LSB of differential nonlinearity and 0.3 LSB of integral nonlinearity errors. The total area of the prototype including analog and digital circuit consumes around 5082 $mils^2$

ACKNOWLEDGEMENTS

I appreciate the support and guidance given by Professor Paul R. Gray, my research advisor, through out this project. His idea and advice are brilliant. I would also like to thank Professor Robert M. Meyer and Professor Don O. Pederson for their help and advice in both research and academics matters.

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Finally, I thank my fiance', Carolyn for encouraging and giving me moral support for all these years.

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CHAPTER 1

Introduction

Over the last decade, the level of integration in a VLSI chip has risen tremendously. Many circuit designers try to integrate multiple functions onto a single chip. These functions can be all digital, all analog, or mixed analog-digital circuits. An example of a mixed analog-digital circuit integrated onto a single chip is an analog-digital signal processing chip. One common analog block on this chip is the Analog-to-Digital(A/D) Converter. A common A/D converter architecture used in these applications is the algorithmic approach[1,2,3,4]. Algorithmic A/D converters require simple hardware and consume relatively little silicon area and therefore, are economical to integrate in standard CMOS technologies. Unfortunately, the speed of an Algorithmic A/D converter is fairly slow since it requires high precision comparators and several clock cycles[1,2,3,4] to resolve 1 bit.

Motivated by these limitations, an improved architecture based on the algorithmic approach is investigated in this thesis with the aim of achieving a higher conversion rate. One of the key aspects of this new approach is relaxed requirements on the capacitor specifications. Many analog circuit design techniques are incorporated into the design of this new A/D converter architecture so that non-idealities from building blocks such as amplifiers, switches, and comparators can be canceled or reduced. An 8-bit 125kHz A/D converter prototype based on the proposed architecture was designed and laid-out in a 3-μm, CMOS technology and fabricated through MOSIS.

The rest of the thesis is organized as follows. Chapter 2 describes the specifications and characterizations of A/D converter. In Chapter 3, the basic concept of the algorithmic A/D converter will be presented. Then a detailed discussion of the new-improved algorithmic A/D converter will be discussed in Chapter 4. Chapter 5 describes the design of the prototype of the proposed A/D converter. Finally, conclusions of the research are given in Chapter 6.

CHAPTER 2

Analog-To-Digital Converter Characterization

2.1 Introduction

What is an Analog-to-Digital converter? An A/D converter is an electrical device which converts or encodes a continuous analog signal into a digital representation with a finite number of bits as shown in Figure 2.1. The most common *performance* specifications of an A/D converter are *resolution, speed, linearity, and signal-to-noise ratio.*

What does it mean when one tells you that this is an *8-bit 125KHz* A/D converter? *8-bit* indicates that for a given analog input signal, the A/D converter is capable of encoding the analog input signal with a granularity of $\frac{1}{2^8}$. The higher the number of bits, the more accurate the analog input signal can be represented. As the unit indicates, 125KHz specifies the rate at which the A/D converter performs the conversion.

In this chapter, a general overview of A/D converter characterization (mainly static ones) is presented. Many definitions defined here will form a basis for the discussion in the rest of this thesis.

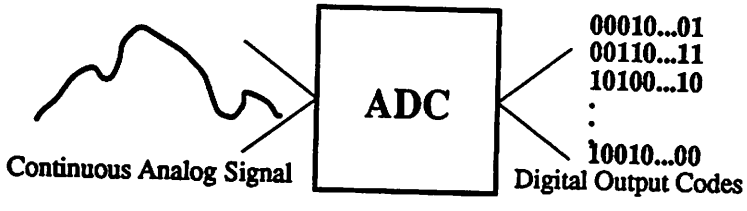

Figure 2.1 A/D Converter

2.2 Characterization

The evaluation of the performance of an A/D converter is very crucial both from the circuit design stand point as well as the requirements dictated by a particular application of the device. One of the most common tests an A/D converter undergoes is the measurement of its transfer characteristic with respect to a ramp input signal as shown in Figure 2.2 (ie. analog voltage in - digital code out). For every analog input

signal level, there exists a corresponding binary representation. Because of the finite number of bits, there is a finite granularity in the digital approximation $d_0, d_1, ..., d_{N-1}$ of the actual analog input signal V_{IN}.

$$V_{IN} = V_{FS}\left(\frac{d_0}{2^0} + \frac{d_1}{2^1} + \cdots + \frac{d_{n-1}}{2^{n-1}}\right) + \varepsilon \tag{2.1}$$

where V_{FS} = full scale input signal = max.$|\pm V_{IN}|$

$d_i = i^{th}$ digit

ε = deviation of digital output from V_{IN}

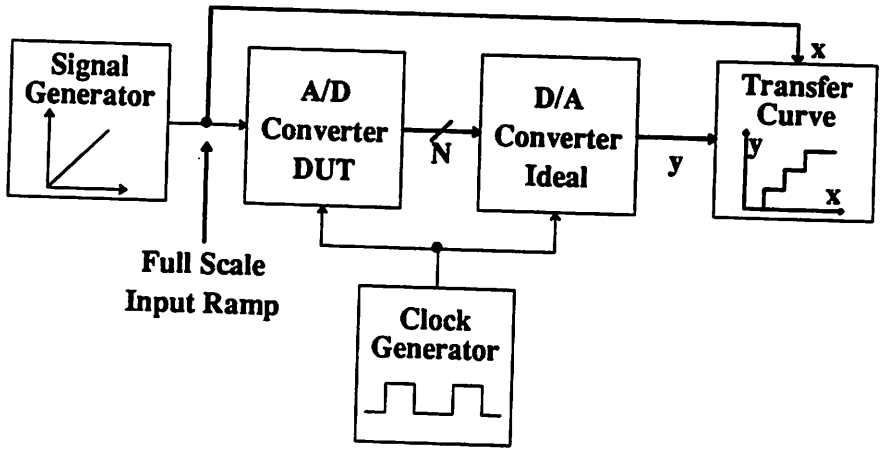

Figure 2.2 Measurement of an A/D converter's transfer characteristic

Quantization error is unavoidable when quantizing a continuous signal into a digital domain. The transfer curve shown in Figure 2.3 (a) clearly shows each transition point of a continuous analog input signal corresponding to each digital output code change. The transfer curve looks like stair cases with steps at the analog transition points. This due to the fact that digital output of a N-bit converter has a finite number of representations(2^N distinct digital codes); whereas, the analog signal is continuous and hence has an infinite number of levels. Two possible *ideal* transfer curves of a simple 3 bit A/D converter are shown in Figure 2.3.

The difference between the two depends on where the origin intersection is. The transfer curve shown in Figure 2.3 (a) is referred to as *mid-rise* because the origin intersection occurs in the middle of a vertical transition between 2 different digital codes. On the other hand, the transfer curve shown in Figure 2.3 (b) is referred to as *mid-tread* because it intersects the origin in the middle of the tread representing the digital code for zero volts input. Unlike a mid-rise case which has 2^N digital output codes, a mid-tread case has only 2^N-1 possible codes. The rest of the discussion will use the mid-rise transfer curve as an

example.

In reality the transfer curve is affected by many non-idealities contributed by non-ideal functional blocks. As a result, the transfer curve will have non-uniformly spaced steps as illustrated in Figure 2.4 (b). Let 1 least significant bit (LSB) be the smallest quantization step for an N-bit conversion.

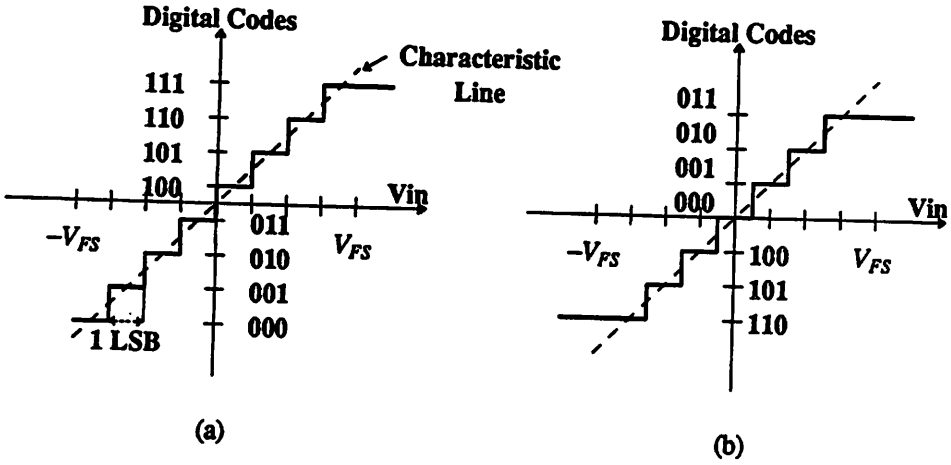

Figure 2.3 The Ideal 3-bit A/D Converter Transfer Curves (a) Mid-Rise (b) Mid-Tread

Let the input voltage range between $-V_{REF}$ to V_{REF}.

$$1\,LSB = \frac{2V_{FS}}{2^N} \tag{2.2}$$

Then the residual voltage can be written as

$$Residue = \frac{\left[V_{IN} - V_{digital}\right]}{1LSB} \tag{2.3}$$

$$where\ V_{digital} = 2V_{FS}\left[\frac{d_0}{2} + \frac{d_1}{2^2} + \ldots + \frac{d_{N-1}}{2^N}\right] \tag{2.4}$$

and plotted in Figure 2.4. Notice that the residual voltage for an ideal transfer curve fluctuates between $\pm\frac{1}{2}LSB$ (Figure 2.4 (a)); whereas, the non-ideal one fluctuates between $\pm 1LSB$ for this particular transfer characteristic (Figure 2.4 (b)).

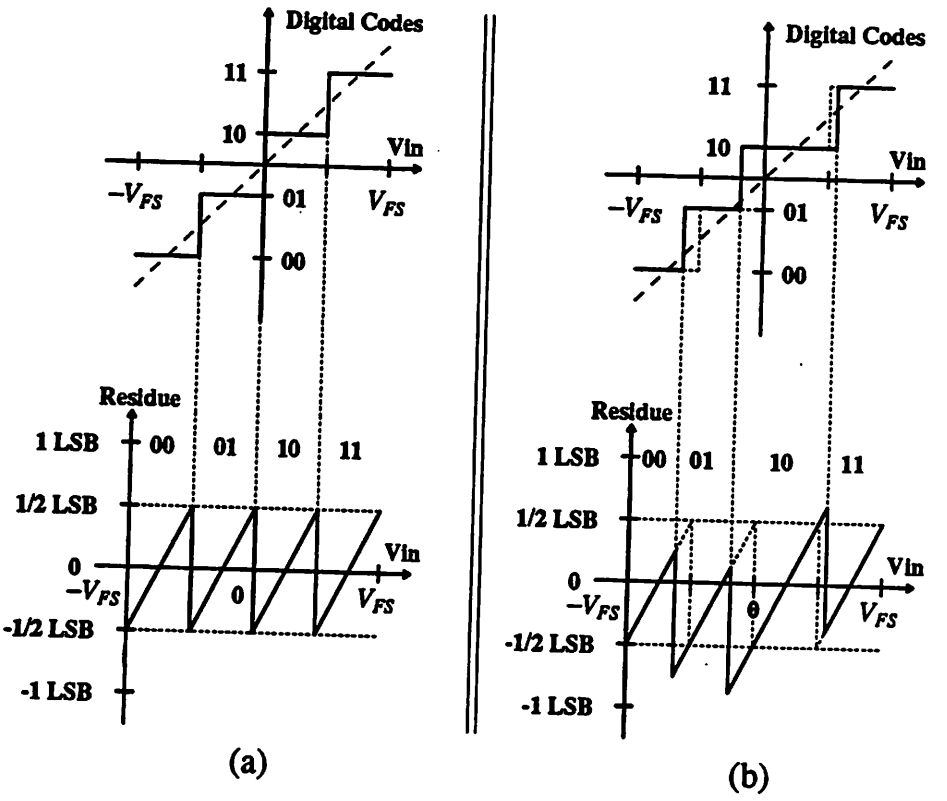

Figure 2.4 (a) Ideal and (b) non-ideal transfer curves and their residual plots

2.2.1 Differential Non-Linearity (DNL)

As mentioned earlier, the voltage difference between two consecutive transition voltages is the width of a quantization step. For an ideal transfer curve, the quantization steps are all equal to at least $\pm\frac{1}{2}$ *LSB* or 1 *LSB* in an absolute magnitude. For an actual transfer curve as shown in Figure 2.5, the quantization steps are not uniform at all. As a measure of how much the actual quantization step width varies with the ideal step width of 1 LSB, differential non-linearity (DNL) is defined.

$$DNL(k) = x(k) - 1\ LSB \tag{2.5}$$

where k = the k^{th} digital code; k = 1, 2, ..., 2^N - 2

x(k) = the actual step width of k^{th} digital code

DNL(k) = zero for k = 0 and $2^N - 1$

As long as the DNL is less than -1 LSB, the conversion will result in a complete digital code. If x(k) is equal to zero, the corresponding DNL is going to be -1 LSB. When this occurs, we have a *missing code.*

Figure 2.5 shows that digital code 101 is skipped and therefore, it is *missing*. For illustration purposes, the DNL plot of transfer curve shown in Figure 2.5 is shown in Figure 2.6 (a).

An A/D converter is monotonic if it always generates an increasing digital code for an increasing analog input, This means monotonicity can only occur if and only if the DNL is smaller than 1 LSB. In some applications differential non-linearity is not a major requirement as long as the converter is monotonic. In other words, to assure that an A/D converter has no missing codes and is monotonic, the DNL of every code has to be in between -1 LSB and 1 LSB or -1 LSB < DNL(k) < 1 LSB for all possible k.

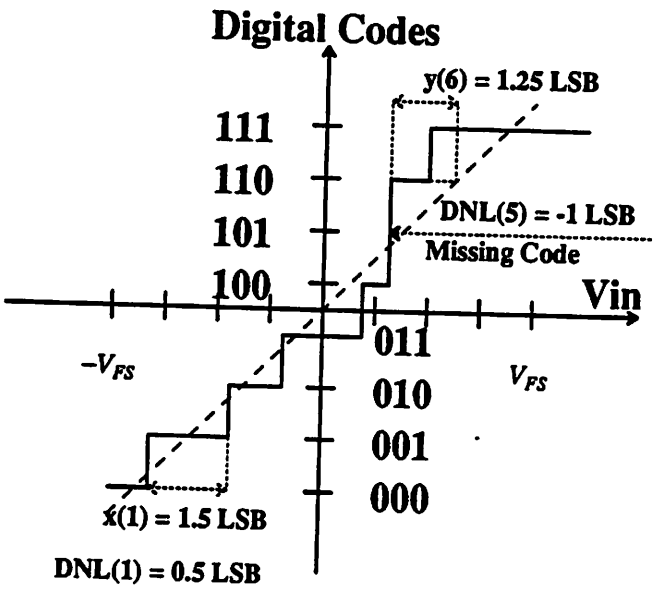

Figure 2.5 Actual transfer curve and its non-linearities

2.2.3 Integral Non-Linearity (INL)

Integral non-linearity (INL) for each digital code is defined as the transition voltage between a code and the next code minus the input voltage corresponding to this code obtained from the characteristic line. It is derived in [5] that

$$INL(k) = \sum_{i=1}^{i=k-1} DNL(i) \tag{2.6}$$

where k = 1,..., 2^N-1

INL(0) = 0

Or in a simplified version illustrated in Figure 2.5, INL can be defined as the deviation of the ideal intersection point on the characteristic line to the actual point.

$$INL(k) \approx y(k) - \frac{1}{2}LSB \tag{2.7}$$

where y(k) = the horizontal distance from the beginning
of code k to the ideal characteristic line.

Figure 2.6 (b) shows the INL plot of the respective DNL plot in Figure 2.6 (a) according to equation (2.6). The overall linearity of an A/D converter depends on the maximum absolute magnitude of DNL and INL.

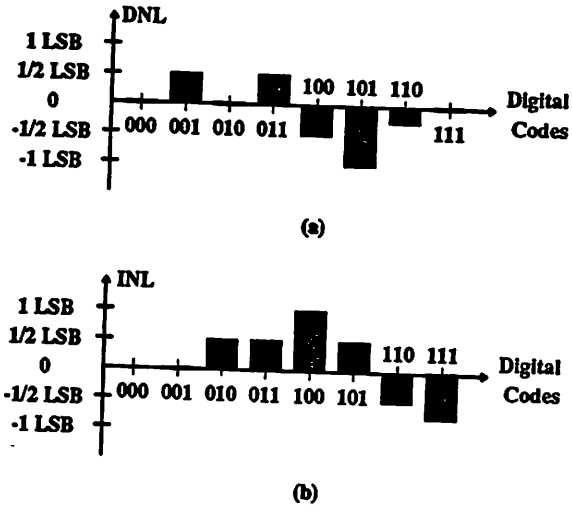

Figure 2.6 (a) DNL (b) INL curves

2.2.4 Gain Error

Gain error occurs when a *gain* block(blocks) in an A/D converter does not multiply the signal by the ideal value. This gain error will affect all the codes by the same percentage. As a result, the resulting digital code center line slope differs from the ideal one. If the gain is bigger(smaller) than it is supposed to be, the slope is be bigger(smaller) than the ideal one as shown in Figure 2.7.

2.2.5 Offset Error

Offset error can be viewed as having an additional input voltage source in the front of an A/D converter. The detailed explanation of this error will be described in Chapter 3. Thus, for an input voltage V_{IN}, the converter will treat it as $V_{IN} + V_{offset}$ were its input. Thus plotting the transfer curve with respect to the actual input voltage V_{IN}, the entire curve gets shifted to the right or left (depending on the sign of the offset voltage) by the exact amount of the magnitude of the offset. As an illustration, Figure 2.8 shows the effect

of a positive offset on the transfer curve shown in Figure 2.3 (a). Notice that the linearity and monotonicity of the A/D converter are not affected by the offset.

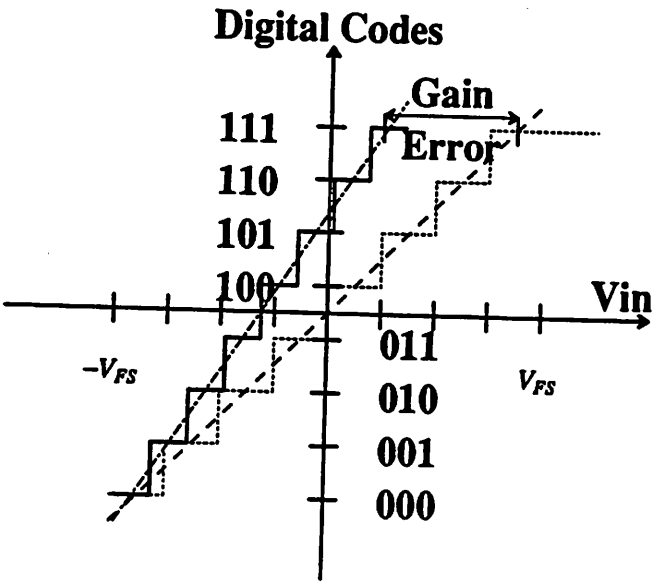

Figure 2.7 A/D converter transfer curves with gain error

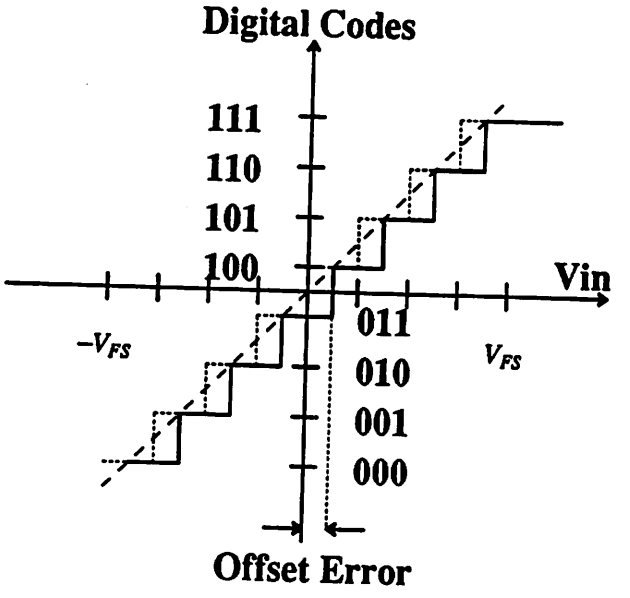

Figure 2.8 A/D converter transfer curve with offset error

2.3 Signal-To-Noise Ratio

Signal-to-noise ratio (SNR) falls into the dynamic characterization category. It is an important measurement for communication system performance, even though it is not always the most accurate standard for performance comparison between two systems. A typical SNR test configuration is shown in Figure 2.9. The SNR is the ratio of the mean square peak-to-peak amplitude of a sinusoidal input signal to the smallest quantization step width. If the full scale peak-to-peak amplitude is $2V_{FS}$ then[6] :

$$\max SNR = \left[\frac{\frac{V_{FS}{}^2}{2}}{\frac{1\,LSB^2}{12}} \right] \tag{2.8}$$

$$\max SNR = 1.5(2^{2N}) \tag{2.9}$$

Or in a simplified form :

$$\max SNR = 6.02N + 1.76\,dB \tag{2.10}$$

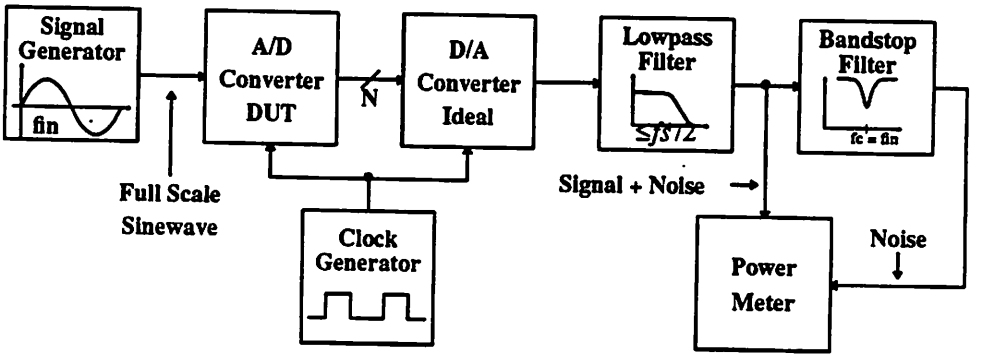

Figure 2.9 SNR test set up

CHAPTER 3

Algorithmic A/D Converter

3.1 Introduction

In this chapter, the algorithmic A/D converter concept will be reviewed. The characteristic of the converter with respect to nonidealities of devices will then be discussed briefly. It will be shown at the end of this chapter that the algorithmic A/D converter has several limitations.

3.2 Concept

The Algorithmic A/D converter technique is very similar to the successive approximation approach except that the former recirculates the sampled signal several times until the desired number of bits is resolved; whereas, the latter successively redistributes the charge among capacitor array to perform the conversion. Shown in Figure 3.1 is a block diagram of an algorithmic A/D converter. A typical algorithmic A/D converter consists of :

1. A sample and hold (S/H) block
2. A gain of two (2X) block
3. A comparator (COMP) block
4. Reference subtraction circuit
5. Digital circuits

The operation of the converter shown in Figure 3.1 will be described further. First of all, the input signal is sampled onto the S/H block by connecting switch S_1 to the input signal source. The sampled signal is then held by the S/H block and multiplied by two by the 2X block. The result V_A, is then compared to the reference voltage. If it is larger than the reference voltage, the comparator will give digital logic "1" as its output and the reference voltage is then subtracted from V_A. Otherwise, a digital logic "0" will be produced by the comparator and V_A will be passed through the subtractor unchanged.

$$V_{e,i} = V_{A,i} - d_i V_{REF} \tag{3.1}$$

where $V_{e,i} = V_e$ after i^{th} conversion

$V_{A,i} = V_A$ after i^{th} conversion

V_{REF} = reference voltage

d_i = the i^{th} digital output of comparator.

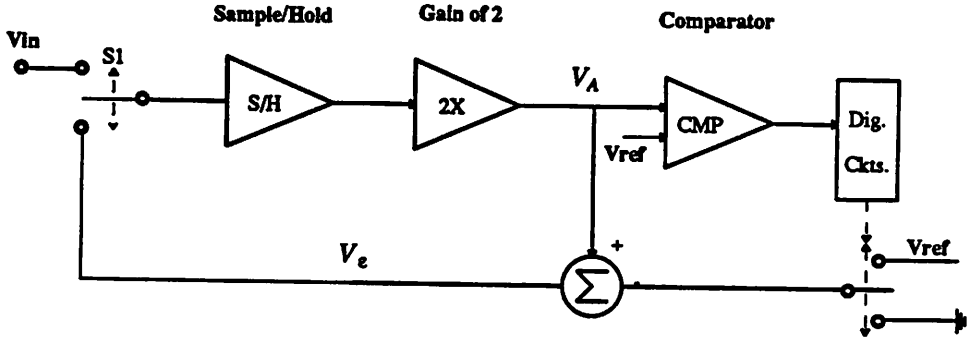

Figure 3.1 Algorithmic A/D Converter

The resulting voltage V_ε is then recirculated again through the same procedure until the desired number of bits is obtained. The entire conversion can be represented analytically as follows :

$$1^{st}\ conversion : V_{A,0} = 2V_{IN} \tag{3.2}$$

$$V_{\varepsilon,0} = V_{A,0} - d_0 V_{REF} = 2V_{IN} - d_0 V_{REF} \tag{3.3}$$

$$2^{nd}\ conversion : V_{A,1} = 2V_{\varepsilon,0} = 2^2 V_{IN} - 2d_0 V_{REF} \tag{3.4}$$

$$V_{\varepsilon,1} = V_{A,1} - d_1 V_{REF} = 2^2 V_{IN} - \left[2d_0 + d_1\right] V_{REF} \tag{3.5}$$

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$$N^{th}\ conversion : V_{A,N-1} = 2V_{\varepsilon,N-2} \tag{3.6}$$

$$V_{\varepsilon,N-1} = V_{A,N-1} - d_{N-1} V_{REF} \tag{3.7}$$

$$V_{\varepsilon,N-1} = 2^N V_{IN} - \left[2^{N-1} d_0 + 2^{N-2} d_1 + \cdots + 2d_{N-2} + d_{N-1}\right] V_{REF} \tag{3.8}$$

Dividing the equation (3.7) by 2^N and solve for V_{IN}, we get

$$V_{IN} = \left[\frac{d_0}{2} + \frac{d_1}{2^2} + \cdots + \frac{d_{N-1}}{2^N}\right] V_{REF} + \varepsilon_N \tag{3.9}$$

$$\varepsilon_N = \frac{V_{e,N-1}}{2^N} \tag{3.10}$$

where V_{IN} = input signal voltage

ε_N = quantization error

From equation (3.9), we can obtain the lower and upper limits for the quantization error ε_N.

$$-\frac{V_{REF}}{2^{N+1}} < \varepsilon_N < \frac{V_{REF}}{2^{N+1}} \tag{3.11}$$

As long as ε_N is within this limit, the conversion result is guaranteed to have no missing codes. In summary, equation (3.8) describes how an input signal is converted into digital codes by successively comparing it with the *appropriate* reference voltage in each cycle. An example of this cyclic conversion is shown graphically in Figure 3.2. For an actual conversion sequence based on restoring algorithm[1,2], a plot of V_e and V_A versus time is shown in Figure 3.3.

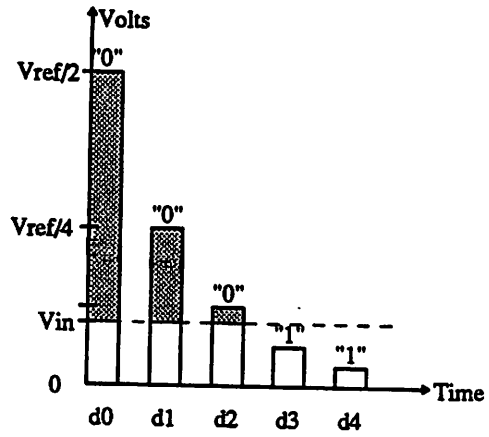

Figure 3.2 Graphical Conversion Sequence

3.3 Limitations

Unlike the successive approximation A/D converter, the algorithmic converter needs only two precision elements which are the S/H and 2X blocks with exact gain of 1 and 2 respectively. As a result, the required hardware is simple. Unfortunately, the nonidealities from capacitors, operational-amplifiers(op-amps), comparators, and switches affect the overall performance of the converter. Each contribution will be briefly discussed in the remainder of this section(for a detailed discussion of each contribution please refer to Chapter 4).

In order to build a gain of 1 or gain of 2 blocks, two capacitors and an op-amp are needed(Figure 3.4). The accuracy of these blocks depend not only on how good the two capacitors match but also on the gain of the op-amp.

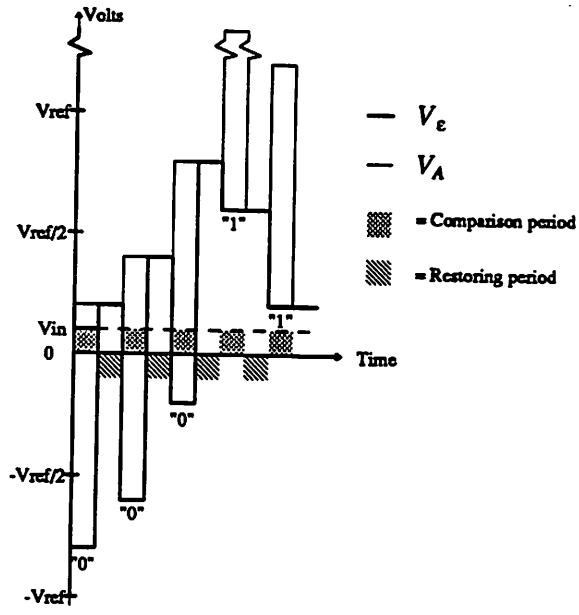

Figure 3.3 Actual Conversion Sequence for Restoring Algorithm A/D Converter

The closed-loop transfer function of the example in Figure 3.4 is

$$\frac{V_{OUT}}{V_{IN}} = -\left[\frac{C_S'}{C_I' + \dfrac{C_S' + C_I' + C_P}{A_v}}\right] \tag{3.12}$$

$$C_S' = C_S + \Delta C_S \tag{3.13}$$

$$C_I' = C_I + \Delta C_I \tag{3.14}$$

where: C_S = sampling capacitor

ΔC_S = sampling capacitor mismatch

C_I = integrating capacitor

ΔC_I = integrating capacitor mismatch

C_P = total capacitance on the op-amp input node

A_v = finite open loop op-amp gain

As the op-amp gain A_v gets larger, the closed-loop gain approaches the ratio of the two capacitors $\frac{C_S'}{C_I'}$. As can be seen in equation (3.12), capacitor mismatch directly degrades the accuracy of the gain block. Thus, care must be taken when designing the op-amp and choosing capacitor sizes for this gain block so that the desired accuracy can be obtained. A typical capacitor ratio mismatch might be 0.1%, which means that the capacitor ratio will be good for resolution up to 8 or 9 bits.

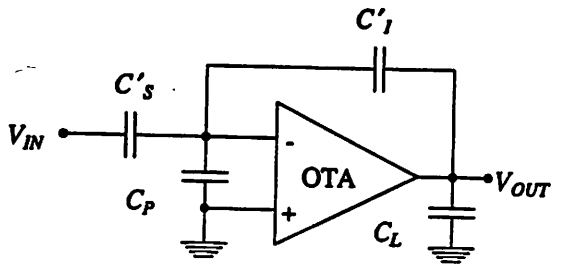

Figure 3.4 Gain of 2 Block

Asides from having finite gain, the op-amp also has an offset voltage that contributes directly to the loop voltage. Because the signal gets recirculated and multiplied by two again and again, the offset voltage will also experience the same affect. We must ensure that at the end of the conversion, the total input referred offset voltage due to the op-amp is less that 0.5 LSB or else there will be a missing code. Moreover, transistor switches (not shown) can also contribute to the offset voltage and hence have to be taken into account. Let us assume V_{OS} to be the total input referred offset voltage from the S/H and 2X op-amps and charge injection from the switches(Figure 3.5).

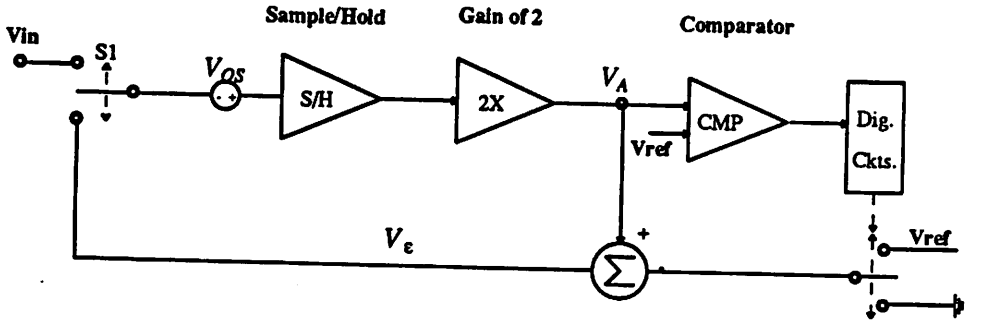

Figure 3.5 Algorithmic A/D Converter with Offset Voltage

Let V_{IN} be zero and V_{OS} be positive. Therefore, the expected digital code is 0000..0.

$$1^{st}\ conversion : V_{A,0} = 2V_{OS} = V_{\varepsilon,0} \tag{3.15}$$

$$2^{nd}\ conversion : V_{A,1} = \left[2^2 + 2\right] V_{OS} = V_{\varepsilon,1} \tag{3.16}$$

.

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.

$$N^{th}\ conversion : V_{A,N} = \left[2^N + 2^{N-1} + \cdots + 2^2 + 2\right] V_{OS} \tag{3.17}$$

If $V_{A,N}$ is greater than V_{REF}, d_{N-1} will be "1" instead of "0". Thus, we have to make sure that at the end of the conversion, the total output referred offset $V_{OS,Total}$ is smaller than V_{REF}.

$$V_{OS,Total} = 2V_{OS}\left[1 + 2 + 2^2 + \cdots + 2^{N-1}\right] < V_{REF} \tag{3.18}$$

Referring this back to the start of the conversion, the total input referred offset is $V_{OS,Total}$ divided by 2^N.

$$V_{OS,referred} = \frac{V_{OS,Total}}{2^N} < \frac{V_{REF}}{2^N} \tag{3.19}$$

$$V_{OS,referred} = 2V_{OS}\left[\frac{2^N - 1}{2^N}\right] < \frac{V_{REF}}{2^N} \tag{3.20}$$

$$V_{OS} < \frac{V_{REF}}{2\left[2^N - 1\right]} \approx 0.5\,LSB \tag{3.21}$$

Thus, as long as V_{OS} < 0.5 LSB, the op-amp offset and switch charge injection will not cause any missing codes.

Finally, the comparator has to have an offset voltage that is less than 1 LSB; otherwise, the resulting digital code will be incorrect. For example, the comparator shown in Figure 3.6(a) has offset voltage V_{OS} = 25mV. Assume the reference of the comparator is tied to ground. The solid line shown in Figure 3.6(b) is the comparator response with no offset voltage (ideal comparator). When $V_{IN} < 0$, V_{OUT} is equal to logic "0" or else "1". But because of the positive offset, comparator response gets shifted to the right as shown by dashed line. If 1 LSB < 25mV, the digital code will be incorrect. As a result, the comparator offset voltage will contributes directly to the linearity of the conversion. One way to cancel the comparator offset to the first order is by storing it into a capacitor during the initialization period as shown in Figure 3.7(a) so that during the comparison period (Figure 3.7 (b)), offset voltage is canceled.

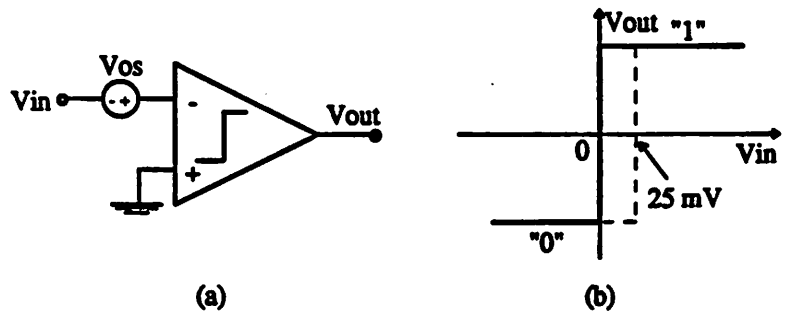


Figure 3.6 (a) Comparator with offset and (b) its transfer curve

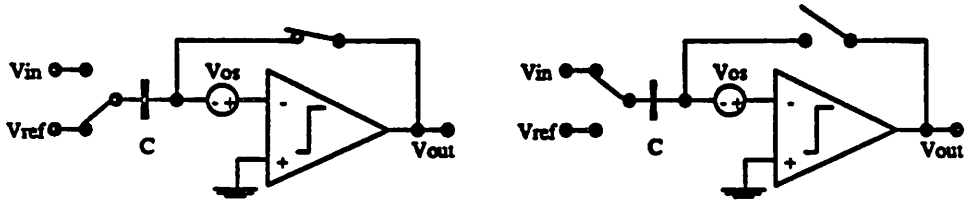


Figure 3.7 Comparator Offset Cancellation Scheme

CHAPTER 4

New Improved Algorithmic A/D Converter

4.1 Introduction

Algorithmic A/D converters have many desirable advantages such as simple hardware, and an inherent sample and hold function; unfortunately, it is moderate in *speed* due to the fact that many clock cycles are needed in order to resolve one bit. All of the conventional Algorithmic A/D converters previously reported[1,2,3,4] require on average 3 clock cycles or more to resolve 1 bit. As a result, this architecture is capable of resolving signals of only moderate frequency. In order to improve the speed and keep the same basic architecture, a *New-Improved* Algorithmic A/D converter is proposed. This improved Algorithmic A/D converter needs only 1 clock cycle to resolve 1 bit, and therefore, improves the speed by a factor of 3 or higher than the conventional one. The concept and limitations of the proposed architecture will be discussed in detail in this chapter.

4.2 Concept

The motivation behind this proposed Algorithmic A/D converter is to *fully utilize* all functional blocks so that they are never idle. In a typical Algorithmic A/D converter previously reported[1,2,3,4], three clock cycles are needed to resolve one bit as shown in Figure 4.1. In the first phase of conversion, the 2X block acquires the input voltage at the very first cycle or the residual voltage from the S/H block for the remaining cycles (Figure 4.1 (a)). In the second phase, the 2X block amplifier is used as a pre-amplifier for the latch and a decision bit is generated (Figure 4.1 (b)). Notice that during this phase of the conversion, the S/H block is idle. In the third phase, the remainder voltage is being generated and sampled onto S/H block for the next bit conversion (Figure 4.1 (c)).

Adding minor modifications to the conventional architecture, a faster and more efficient Algorithmic A/D converter can be obtained. The proposed scheme requires :

1. Two sample and hold blocks
2. A gain of two block
3. A comparator block

4. Reference subtraction circuits

5. Digital circuits.

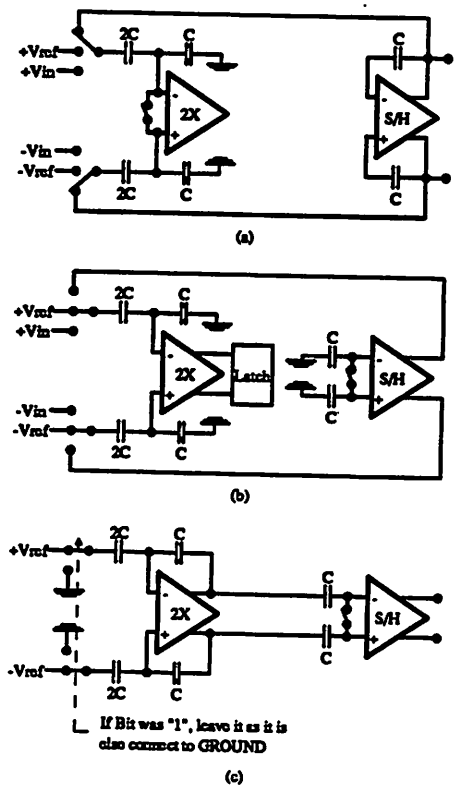


Figure 4.1 Configuration for (a) Acquiring residual voltage. (b) Making bit decision (c) Generating residual voltage

Shown in Figure 4.2 is a *simplified* version of how these blocks are connected to realize the proposed Algorithmic A/D converter. Basically, the conversion steps of this proposed architecture is the similar to the conventional one. Figure 4.3 illustrates how the proposed architecture functions.

Mode 1 :

During the period illustrated in Figure 4.3 (a), the residual voltage $V_{e,i}$ is sampled on to the S/H-1 block, while the S/H-2 and 2X blocks are in the hold and multiplication modes respectively for $V_{e,i-1}$. The reference voltage will be added, subtracted or passed depending on the bit decision from the previous conversion. For the very first cycle, the S/H-1 block will sample V_{IN}, while the rest of the blocks

are in the initialization or reset mode.

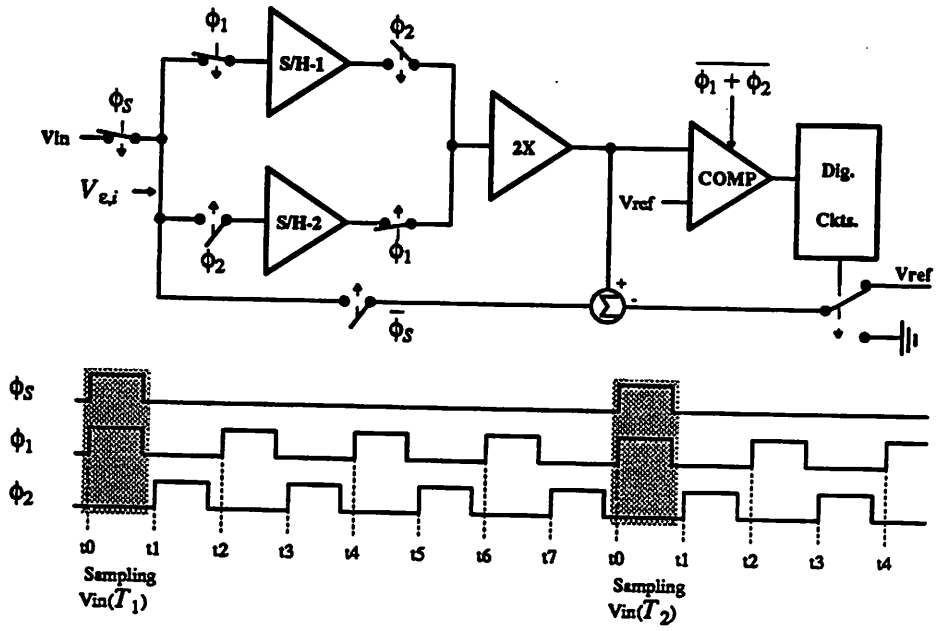


Figure 4.2 1-Bit/cycle Algorithmic A/D Converter

Mode 2 :

In this period illustrated in Figure 4.3 (b), the amplified residual voltage $V_{\varepsilon,i-1}$ is compared with V_{REF} to determine the current bit. The result will be stored in a register and used as control signals for the reference subtraction circuit.

Mode 3 :

In this period illustrated in Figure 4.3 (c), all the blocks experience the same tasks as during *mode* 1 except that S/H-1 is doing the holding (for $V_{\varepsilon,i}$) and S/H-2 is doing the sampling (for $V_{\varepsilon,i+1}$).

Mode 4 :

This period is exactly the same as *mode* 2.

The conversion continues by repeating modes 1 to 4 until the desired number of bits is obtained. Notice there is no block that is idle through out the conversion cycle. At the positive edge of every clock (either ϕ_1 or ϕ_2), one bit will be resolved. Thus, the proposed Algorithmic A/D converter is capable of resolving 1 bit per one cycle. Figure 4.4 shows the complete time division of the 1-bit/cycle Algorithmic A/D converter

when converting an input signal into 8 digital bits.

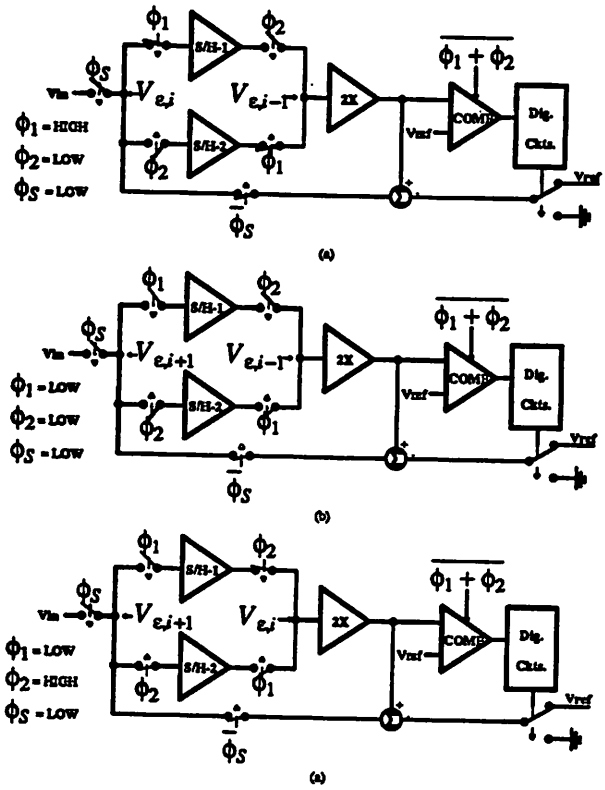


Figure 4.3 (a) Mode 1 (b) Mode 2 and 4 (c) Mode 3

4.3 Error Sources and Solutions

In an algorithmic A/D converter, any errors will get recirculated for a number of times. Sometimes the errors grow as they cycle through so that they affect the overall linearity of the conversion. In chapter 3, some of these errors were discussed briefly. The following several sections will present the sources of errors and proposed solutions to reduce or cancel them.

4.3.1 Gain Error

An Algorithmic A/D converter needs 2 accurate gain blocks ie. gain of 1 (S/H) and gain of 2 (2X). These blocks can be implemented by using op-amps and capacitors as shown previously in Figure 3.4. However, the accuracy of the blocks depends on capacitor ratios, and gain and settling time of the op-amps. Let ε be the combined gain error of the S/H and 2X blocks. If this is so, what would the allowable ε in order to obtain $\frac{1}{2}$ LSB accuracy for N bits of resolution?

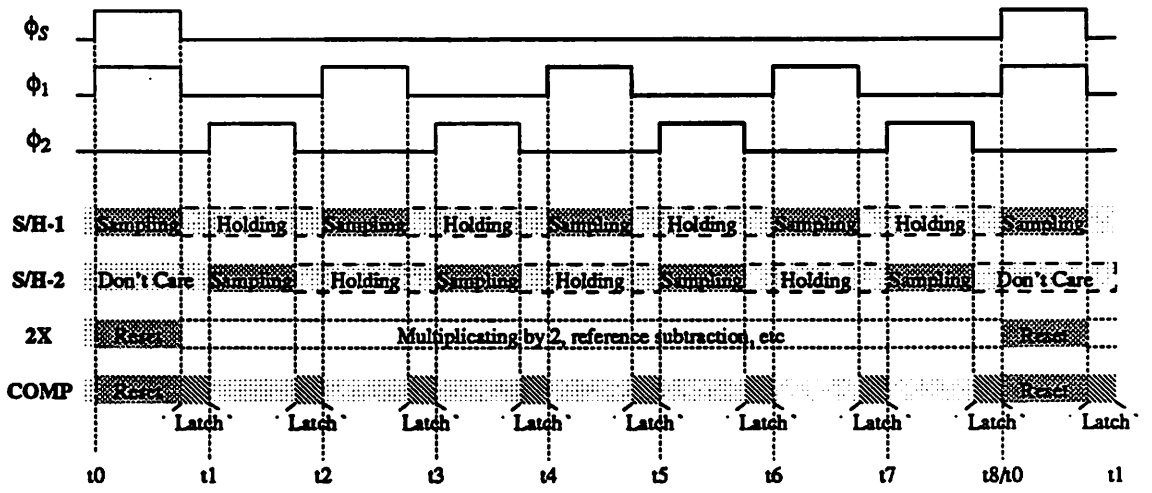


Figure 4.4 Detail Time Sequence of The Conversion.

In an algorithmic A/D converter, for every bit conversion, the residual voltage (assuming $-V_{REF} \le V_{IN} \le V_{REF}$) can be written as :

$$residue = 2\left[V_{IN} - \frac{V_{REF}}{2}\right] \text{ if } V_{IN} \ge 0 \tag{4.1}$$

$$residue = 2\left[V_{IN} + \frac{V_{REF}}{2}\right] \text{ if } V_{IN} < 0 \tag{4.2}$$

Figure 4.5 (a) and (b) illustrate an input ramp voltage and the corresponding comparator behavior and resultant residual voltages respectively. If the gain is exact, then the residual voltage (which is the input for the next conversion) will have a slope of exactly 2. However, due to gain error, the slope will become smaller than 2. Assuming we are converting the first bit of an N-bit conversion, we have to make sure that the residual voltage will be within $\frac{1}{2}$ LSB of the remaining N-1 bits. In other words, we have to make sure that the residual voltage does not change more than $\frac{1}{2}$ LSB of the remaining N-1 bits. Referring back to Figure 4.5 (a) , incorporating gain error into equation (4.2), Equation (4.2) can be rewritten as :

$$residue = 2(1-\varepsilon)V_{IN} + V_{REF} \tag{4.3a}$$

At $V_{IN} = 0$, we want to make sure the residue is not less than $V_{REF} - \Delta$ where Δ is one LSB of the remaining N-1 bits. Substituting $V_{IN} = 0$ and the allowable residue into equation (4.3a), we get

$$(1-\varepsilon)V_{REF} \ge V_{REF} - \Delta \tag{4.3b}$$

$$where\ \Delta = \frac{1}{2}\left[\frac{2V_{REF}}{2^{N-1}}\right] \tag{4.4}$$

$\varepsilon = combined\ gain\ error$

$$(1-\varepsilon) \geq 1 - \frac{1}{2^{N-1}} \tag{4.5}$$

$$\varepsilon \leq \frac{1}{2^{N-1}} \tag{4.6}$$

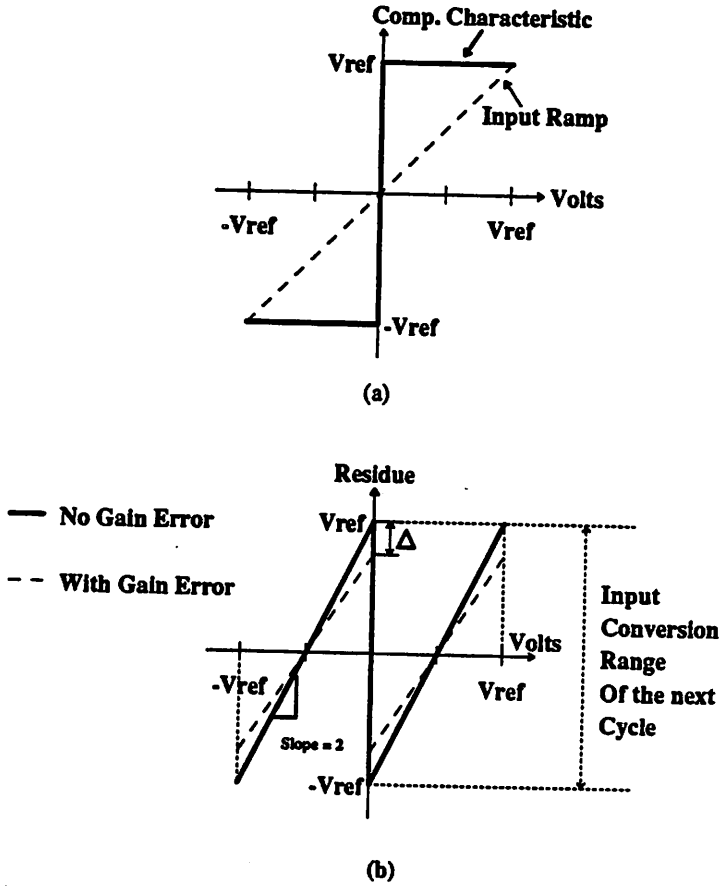


Figure 4.5 (a) Comparator Characteristic (b) Residual plot

Thus, in order to resolve N bits of resolution, the gain error has to be smaller than approximately $\frac{1}{2^{N-1}}$. If N = 8 bits, the total gain block (S/H and 2X blocks) should be accurate within 0.78% of the ideal gain.

4.3.2 Offset Errors

4.3.2.1 Op-amp And Switch Charge Injection Offsets

In Chapter 3, equation (3.21) shows that in order to get linearity within $\frac{1}{2}$ LSB, the input refer offset due to op-amps and switch charge injection has to be smaller than $\frac{1}{2}$ LSB. In order to reduce the offset voltage of the op-amp, an auto zero circuit can be added into an op-amp[7]. Details on how the auto zero circuit functions will be discussed in Chapter 5. For switch charge injection offset reduction or cancellation, a *fully-differential* architecture can be implemented so that the charge injection contributes only as common mode voltage error. The differential voltage error will depend on the matching of the drains and sources of the switches.

4.3.2.2 Comparator Offset

Unlike op-amp and switch charge injection offsets, comparator offsets directly affects the overall linearity. In Figure 4.5 (b), the transfer curve with solid line shows the residual voltage resulting from an *offset free* comparator. If the comparator has an offset voltage, the residual voltage will be larger than V_{REF} for positive offsets or smaller than $-V_{REF}$ for negative offsets for V_{IN} around zero as shown in Figure 4.6. As a result, the residual voltage for this particular input voltage may exceed the maximum input conversion range of the next cycle. As long as the offset is not larger than $\frac{1}{2}$ LSB of the remaining resolution, the comparator will not cause any problems.

There are several ways to solve the comparator offset error. The first one is to design comparators with small enough offset. Often such a comparator requires complicated circuitry and has fairly large area. The second one is to store the comparator offset in a capacitor (shown in Figure 3.7) before the comparison cycle. The last one is to use digital error correction[7]. The first two ways can be easily incorporated into an algorithmic A/D converter[8,9,10,11,27,28,29], but the last one has only been done in a pipeline A/D converter[5]. In section 4.4 of this chapter, we will show how to incorporate digital error correction into a cyclic A/D converter so that *no* high-precision comparators are need.

4.3.3 $\frac{kT}{C}$ Noise Limitation

It is desirable to use capacitors that are as small as possible when designing high-speed circuits. Unfortunately, in a high-resolution A/D converter design, $\frac{kT}{C}$ noise has to be considered. This noise comes from thermal noise due to non-zero channel resistance of the switches in the S/H and 2X blocks that get sampled onto the sampling capacitors. The magnitude of the noise depends directly on the temperature and

inversely on capacitor values[12,13].

$$\overline{v}^2_{noise} = \frac{kT}{C} \tag{4.7}$$

where k = *Boltzmann's constant*

T = *absolute temperature*

C = *capacitor value*

For a capacitor value of 1 pF at room temperature, $\sqrt{\frac{kT}{C}} = 64\ \mu V$. For 8-bit resolution with 3-V peak-to-peak reference voltage, 1 LSB = 11.72 mV. Thus, one can choose small capacitor values as long as the $\frac{kT}{C}$ noise contribution is negligible.

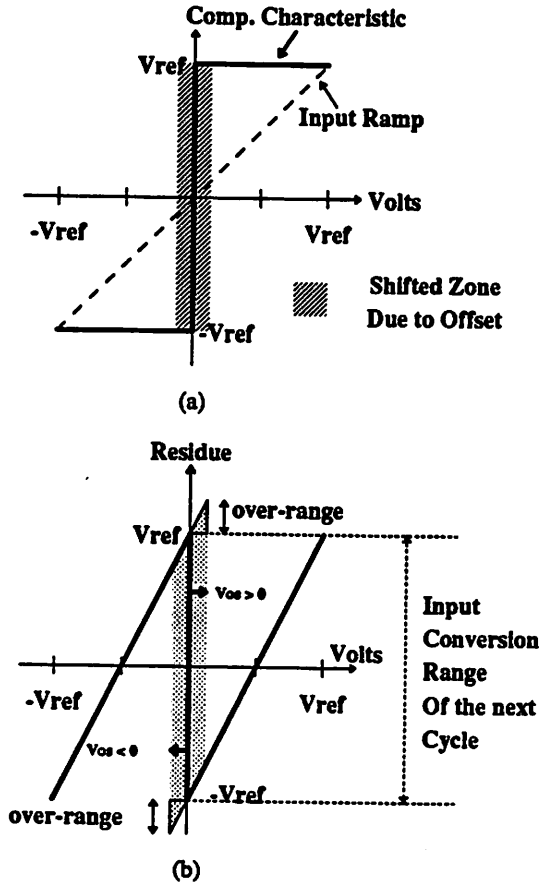
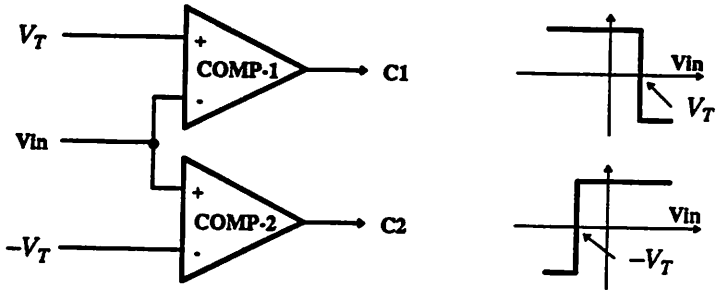


Figure 4.6 (a) Comparator characteristic with offset (b) Its residual plot

4.4 Digital Error Correction For Algorithmic A/D Converter

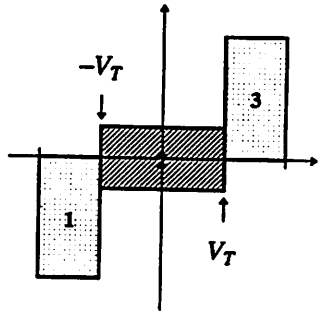
As mentioned earlier, the residual voltage may saturate the next bit conversion and produce missing codes if it is too large. But if the conversion range of the next stage is increased to allow larger residual voltages, the results are decoded and the errors are corrected, comparator offset requirements can be relaxed or even ignored. This concept is called digital error correction[5] and was first introduced by Horna[14].

Borrowing this idea, we propose a two-comparator scheme with digital error correction to take care of the comparator offset. With a one-comparator scheme, the residual voltage will fall into 2 regions and will have characteristic curve according to equations (4.1) and (4.2). Thus, any offset voltage from this comparator will saturate the input conversion of the next cycle. With a two-comparator scheme, for every cycle, one and a half bits are resolved and only one bit is stored. The residual voltage, thus, has *three* possible regions to reside instead of two. Figure 4.7 (a) and (b) illustrate how the two comparators are connected and the respective transfer characteristic with $\pm V_T$ as their threshold voltages.



(a)

Region	Vin	C1	C2
1	$Vin \leq -V_T$	1	0
2	$-V_T < Vin < V_T$	1	1
3	$Vin \geq V_T$	0	1



(b)

Figure 4.7 (a) Two-comparator scheme (b) The resulting regions

$$\textit{Region } 1: V_{IN} \le -V_T \textit{ then} \qquad \textit{residue} = 2V_{IN} + V_{REF} \tag{4.8}$$

$$\textit{Region } 2: -V_T < V_{IN} < V_T \textit{ then} \qquad \textit{residue} = 2V_{IN} \tag{4.9}$$

$$\textit{Region } 3: V_{IN} \ge V_T \textit{ then} \qquad \textit{residue} = 2V_{IN} - V_{REF} \tag{4.10}$$

To ensure that the residual voltage is within $\pm V_{REF}$, V_T has to be between 0 and $\frac{V_{REF}}{2}$. Let $V_T = \frac{V_{REF}}{2}$. The comparator transfer characteristic and the residual voltage plots are shown in Figure 4.8. Let V_{os1} and V_{os2} be the offsets of comparators one and two respectively. For $V_{os1} = V_{os2} = 0$, the ideal residual voltage plot is shown in Figure 4.8 (b). However, if the first and the second comparators have positive offsets ($V_{os1} > 0$ and $V_{os2} > 0$), the residual voltage will saturate the input conversion range of the next cycle (Figure 4.8 (c)). On the other hand, if the both comparators have negative offsets ($V_{os1} < 0$ and $V_{os2} < 0$), the residual voltage for $-\frac{V_{REF}}{2} < V_{IN} < \frac{V_{REF}}{2}$ is always within the boundary of $\pm V_{REF}$ as shown in Figure 4.8 (d). Obviously, $V_T = \frac{V_{REF}}{2}$ is not a good choice.

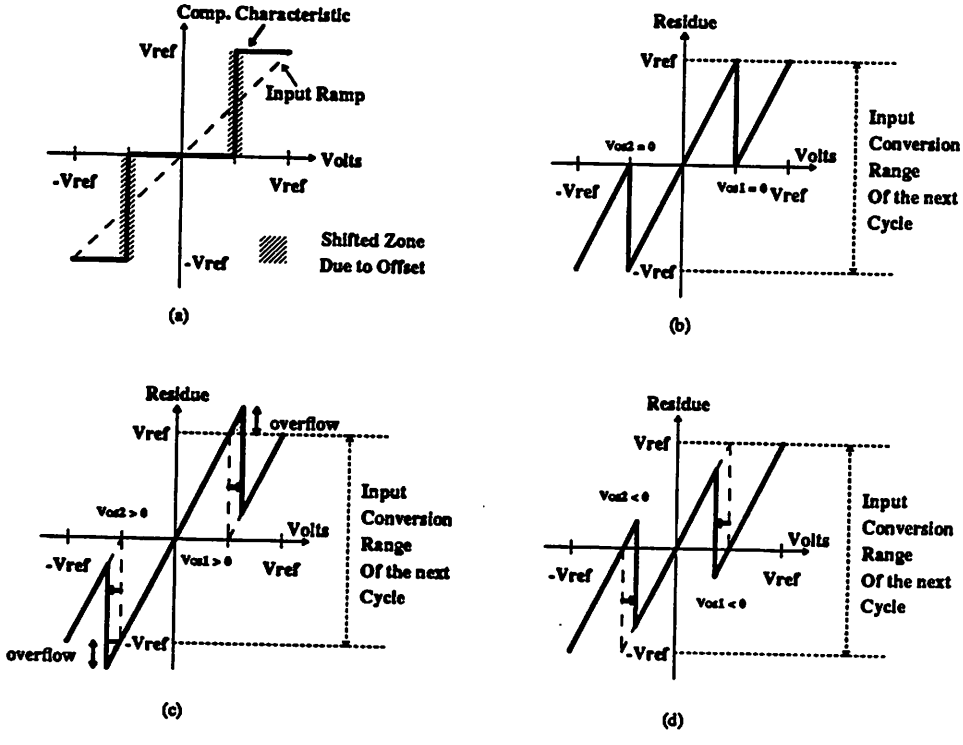
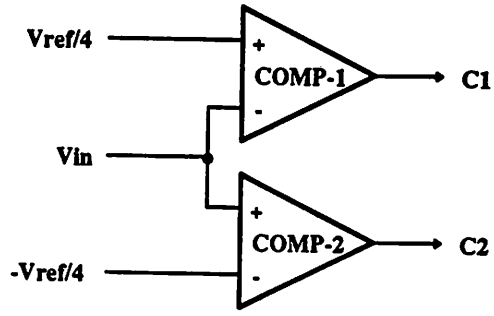
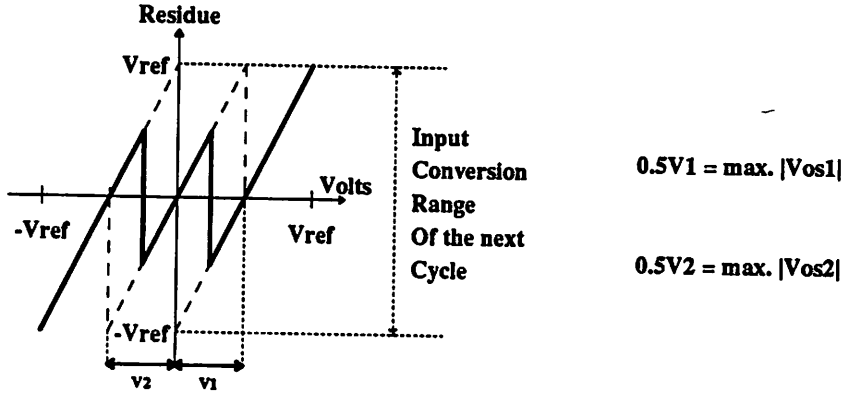


Figure 4.8 Residual plots with different offset voltages

If $V_T = 0$, then having two comparators are redundant, since the residual voltage characteristic is exactly the same as one comparator case shown in Figure 4.5 (b). It turns out that choosing $V_T = \frac{V_{REF}}{4}$ gives the *maximum allowable* comparator offset which is $\pm\frac{V_{REF}}{4}$ as shown in Figure 4.9. Placing comparator threshold voltages at $\pm\frac{V_{REF}}{4}$ is similar to introduce *intentional offsets* in the comparators and subsequently correct the error by digital circuit. If the comparators have offsets, the residual voltage will always be within the input conversion range of the next cycle as long as the offsets are within $-\frac{V_{REF}}{4} \le V_{os1}, V_{os2} \le \frac{V_{REF}}{4}$.



(a)



(b)

Figure 4.9 Residual plot with optimal comparator threshold

By having such a large range of allowable comparator offsets, no high precision comparators are needed with this 2-comparator scheme. The only penalty is the requirement of an additional digital error

correction circuit to correct the error; fortunately, this digital error correction circuit is very simple. It will be shown in Chapter 5 that the digital error correction circuit consists only of simple adders and multiplexers. The conversion algorithm for the N-bit conversion with digital error correction is as follows :

1. At the beginning of the conversion, the sign is always assumed positive ie. $d_0 = 1$ (d_0 = MSB)
2. The rest of the conversion is to resolve the remaining N-1 bits. Each subsequent cycle, the comparator outputs, C1C2, are decoded to obtain the current bit, reference subtraction control signals, and correction information. The decoding and correcting decisions are as follows :
    a. If V_{IN} is in region 3 ie. C1C2 = 01, then the current bit is "1".
    b. If V_{IN} is in region 2 ie. C1C2 = 11, then the current bit is "0".
    c. If V_{IN} is in region 1 ie. C1C2 = 10, then the current bit is "1" but the earlier conversion bits are 1 bit too large. Therefore, the earlier conversion bits need to be subtracted by one.

To verify the 2-comparator scheme, an example of a 3-bit conversion will be derived. Let N = 3 bits, V_{REF} = 2 volts. 1 LSB = $\frac{2V_{REF}}{2^N}$ = 0.5 volts and comparator thresholds are at $\pm\frac{V_{REF}}{4}$. The expected transfer curve for a ramp input voltage is shown in Figure 4.10. Because of the 2-comparator scheme, the resulting transfer curve of a ramp input voltage is a mid-thread type as shown in Figure 4.10.

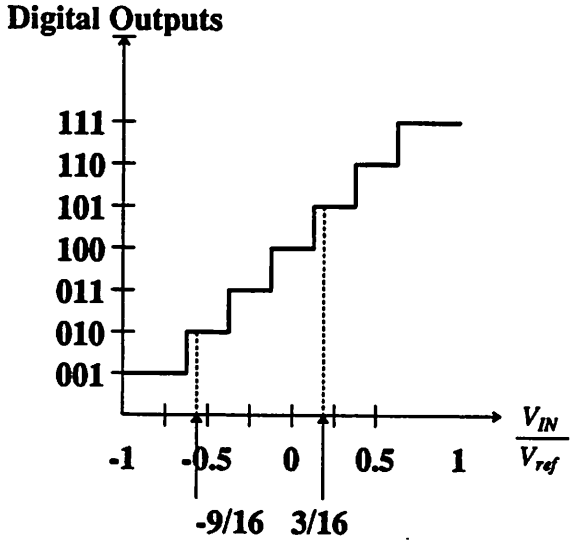


Figure 4.10 3-bit Transfer Characteristic

(a) Let V_{IN} = 0.375 volts = $\frac{3}{16}V_{REF}$ --> expected digital code 101

Initially :

d0	d1	d2
1	-	-

Cycle 1 : Residue = 3/16 V_{REF}

→ $\frac{-V_{REF}}{4} < Residue < \frac{V_{REF}}{4}$

Region 2

d1 = 0

Pass the residue

1	0	-

Cycle 2 : Residue = 2X(3/16) V_{REF} = $\frac{3}{8}V_{REF}$

→ Residue ≥ $\frac{V_{REF}}{4}$

Region 3

d2 = 1

Subtract residue by V_{REF}

1	0	1

(b) For V_{IN} = -1.125 volts = $\frac{-9}{16}V_{REF}$ --> expected digital code 010

Initially :

d0	d1	d2
1	-	-

Cycle 1 : Residue = -9/16 V_{REF}

→ Residue ≤ $-\frac{V_{REF}}{4}$

Region 1

d1 = 1

Add residue by V_{REF}

1	1	-

Correct previous bit

d0 = 1 - 1 = 0

0	1	-

Cycle 2 : Residue = 2X(-9/16) V_{REF} + V_{REF} = $\frac{-1}{8}V_{REF}$

→ $-\frac{V_{REF}}{4} < Residue \leq \frac{V_{REF}}{4}$

Region 2

d2 = 0

Pass the residue

0	1	0

Clearly, the resulting digital outputs of the two examples above agree with the expected codes extracted from transfer curve shown in Figure 4.10.

4.5 Proposed 1-bit/cycle Algorithmic A/D Converter

Combining the new algorithmic conversion concept and the 2-comparator scheme introduced in sections 4.2 and 4.4, a *1-bit/cycle Algorithmic A/D converter without high precision comparators* is proposed. This improved architecture will not only yield a higher conversion rate but will also allow the designer to use simple comparators. The block diagram of this proposed architecture is shown in Figure 4.11. In the next chapter, the detailed implementation issues of each functional block will be discussed. An 8-bit Algorithmic A/D converter prototype will be designed and laid-out by using 3-μm CMOS process and fabricated through MOSIS.

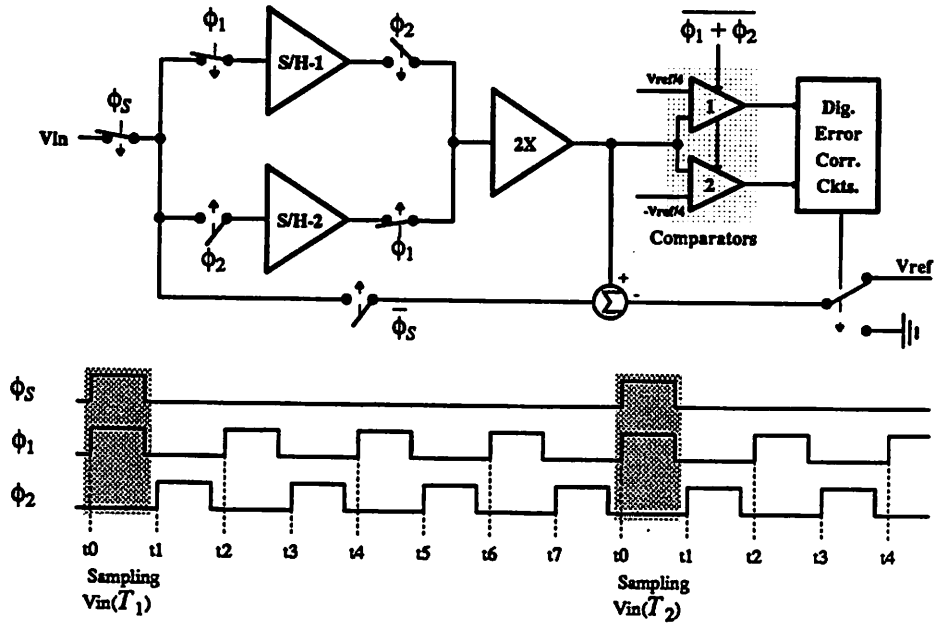


Figure 4.11 Proposed 1-bit/cycle Algorithmic A/D converter architecture

CHAPTER 5

1-bit/cycle Algorithmic A/D Converter Prototype

5.1 Introduction

In this chapter the design of an 8-bit Algorithmic A/D converter prototype will be presented. The goals of the design of this prototype were to obtain 8-bit resolution at 125 kHz conversion rate using a 3 μm CMOS process. Techniques to improve linearity of the conversion were also incorporated into the prototype. Detailed description of the design of each functional block will be discussed in great detail.

5.2 Sample and Hold Block

In this section the design of a capacitor mismatch insensitive sample and hold (S/H) circuit will be described. The first section will consider the S/H circuit without the amplifier and the second section will cover the design of the amplifier.

5.2.1 S/H Circuit

The S/H circuit can be realized using capacitors and CMOS switches. It has been known that the CMOS S/H circuit has several sources of errors such as nonzero acquisition time, finite bandwidth in the sample mode, aperture jitter, thermal noise, and sample to hold mode transition error. A detailed discussion of these errors can be found in [5]. By implementing a fully differential S/H circuit with bottom plate sampling, some of the errors can be reduced.

A previously reported S/H circuit[5] is shown in Figure 5.1. The circuit uses a capacitor C_S to do the sampling and another capacitor C_I to do the charge transfer. For a unity gain S/H circuit, the two capacitors are equal ie. $C_S = C_I$. Assuming the op-amp and CMOS switches are ideal, the accuracy of the S/H circuit will depend on the matching of the two capacitors. From equation (3.12), the closed loop gain approaches $\frac{C_S}{C_I}$ as the gain of op-amp A_v approaches infinity. If $C_S > C_I$, the gain will be bigger than 1; whereas, if $C_S < C_I$, the gain will be smaller than 1.

A better S/H circuit is the one that is independent of capacitor ratio, and therefore, is capacitor mismatch insensitive as shown in Figure 5.2. The operation and error sources of the circuit, and source of errors will be discussed in the following sections.

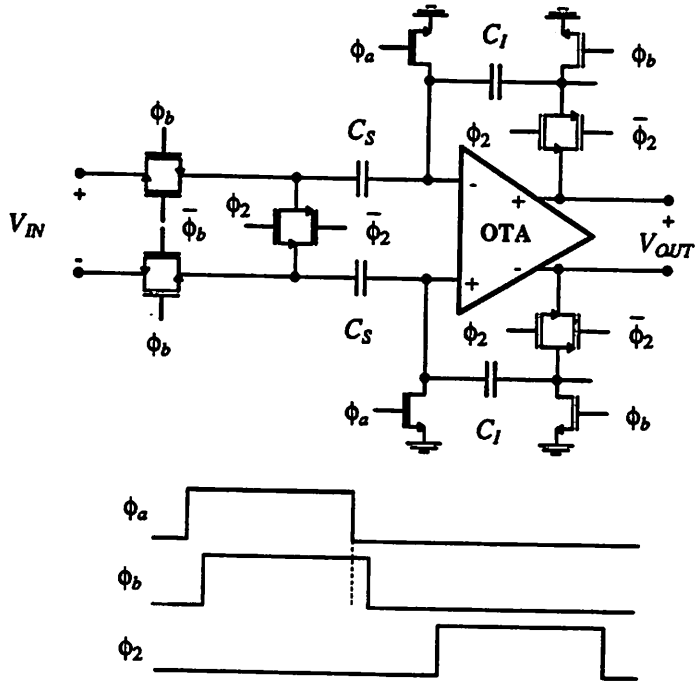


Figure 5.1 Capacitor matching sensitive S/H block

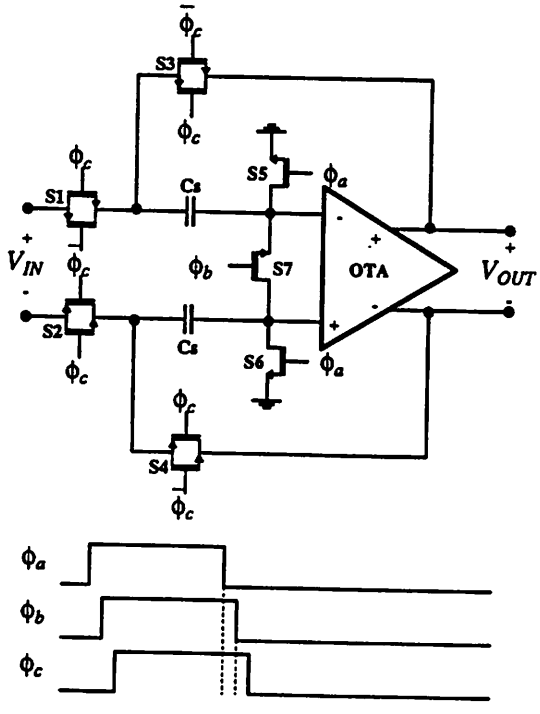


Figure 5.2 Capacitor matching insensitive S/H block

5.2.1.1 Switching Scheme

The S/H circuit shown in Figure 5.2 has 3 different clocks : ϕ_a, ϕ_b, and ϕ_c. ϕ_c is a delayed version of ϕ_b which in turn is a delayed version of ϕ_a. During the sampling mode, V_{in} is sampled onto C_S by closing S1, S2, S5, S6, and S7 switches(Figure 5.3 (a)). At the end of sampling period, ϕ_a will go low first and therefore, S5 and S6 get turned off first and isolate the summing nodes of the op-amp(Figure 5.3 (b)). The charge injected by S5 and S6 will then reside in the summing nodes. Ideally S5 and S6 have exactly the same width and length, but due to limitations in photolithography and the etching process there will be a slight mismatch. As a result, the charge injected by S5 and S6 are not exactly equal. The difference will become a differential error voltage at the summing nodes.

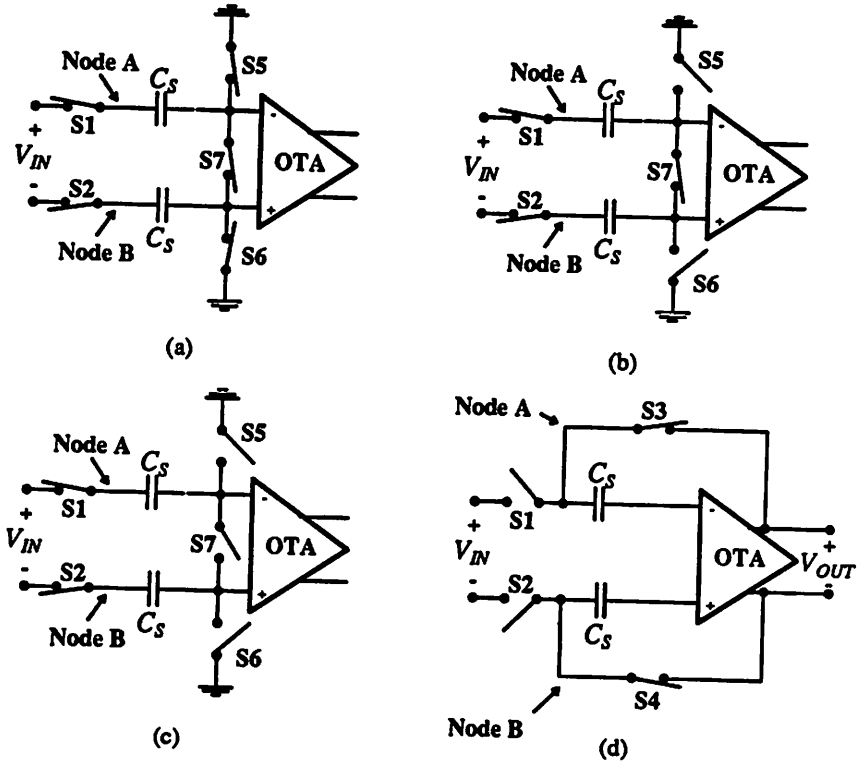


Figure 5.3 Modes of operation

To minimize the difference, S7 is added, connecting the two summing nodes so that turning off S7 after S5 and S6 equalizes the differential error voltage between the two nodes (Figure 5.3 (c)). Moreover, having S7 will make S5 and S6 smaller in size because S7 will now function as the sampling switch instead of S5 and S6. Therefore, S5 and S6 can be small to minimize the amount of charge injection. The total charge injection from S5, S6 and S7 will contribute a common offset voltage to the op-amp. Turning off

S5, S6, and S7 prior to S1 and S2 results in no sampled charge injection due to S1 and S2. When ϕ_c goes low, S1 and S2 will be off; whereas, S3 and S4 turn on, closing the loop by connecting nodes A and B to the outputs to do the hold mode(Figure 5.3 (d)). The size of S3 and S4 are determined by the allowable additional phase shift at the output nodes and the settling time of the op-amp.

The S/H function can be analyzed using charge conservation. Let us consider a single ended version of the block. During the sample mode (Figure 5.4 (a)), the total charge at node X is

$$Q_T = C_S(0 - V_{IN}(T)) \tag{5.1}$$

where $V_{IN}(T)$ is the sampled voltage

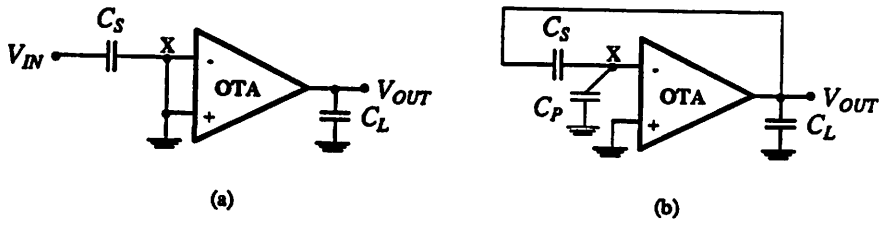


Figure 5.4 (a) Sample mode and (b) Hold mode configurations

Then, the S/H block goes into the hold mode (Figure 5.4 (b)), and the total charge at node X is

$$Q_{T+1} = C_S\left[V_X(T+1) - V_{OUT}(T+1)\right] + C_P V_X(T+1) \tag{5.2}$$

where $V_X(t)$ = *voltage at node X at time t*

$V_{OUT}(t)$ = *output voltage at time t*

C_P = *total capacitance at summing node excluding* C_S

If the open loop gain of the op-amp is A_v, then

$$V_{OUT}(t) = -A_v V_X(t) \tag{5.3}$$

By conservation of charge, the total charge at node X during sample mode is equal to hold mode since node X has no dc path to the ground.

$$Q_T = Q_{T+1} \tag{5.4}$$

$$-C_S V_{IN}(T) = C_S\left[V_X(T+1) - V_{OUT}(T+1)\right] + C_P V_X(T+1) \tag{5.5}$$

Substituting V_X in term of V_{OUT} using equation (5.3), we get

$$V_{OUT}(T+1) = \left[\frac{1}{1 + \frac{C_S + C_P}{A_v C_S}} \right] V_{IN}(T) \tag{5.6}$$

From equation (5.6), clearly the output of this S/H block is independent of any capacitor ratio. The above derivation can easily be extended to cover the fully differential case.

5.2.1.2 Noise Source

The noise sources of the S/H circuit (assuming an ideal op-amp) are the thermal noise generators due to non-zero channel resistance of the switches that get sampled onto the sampling capacitors. The *only* noise source of the S/H block shown in Figure 5.2 comes from the middle switch S7. The reason is very obvious because S7 is the switch that disconnects the sampling path, thus its thermal noise gets sampled onto the sampling capacitors[12,15].

Let us assume the S/H is sampling a zero input voltage. Right before S7 gets turned off, the noise model of this switch is an equivalent non-zero resistance R with thermal noise voltage generator $\overline{v}^2 = 4kTR\,\Delta f$ as shown in Figure 5.5. When S7 is turned off, the thermal noise is sampled onto both capacitors.

$$\overline{v}^2_A = \frac{kT}{2C_T} \tag{5.7}$$

$$\overline{v}^2_B = \frac{kT}{2C_T} \tag{5.8}$$

$$where\ C_T = C_S + C_P$$

Because $\overline{v}^2_A$ and $\overline{v}^2_B$ are *correlated* , the effective total noise (during the hold mode Figure 5.5 (b)) at the output is :

$$\overline{v}^2_{out} \approx \left[\frac{C_T}{C_S} \right]^2 \left[\overline{v}^2_A + \overline{v}^2_B + 2\sqrt{\overline{v}^2_A}\sqrt{\overline{v}^2_B} \right] \tag{5.9}$$

Substituting $\overline{v}^2_A$ and $\overline{v}^2_B$ into equation (5.9) :

$$\overline{v}^2_{out} \approx \left[\frac{C_T}{C_S} \right]^2 \left[\frac{kT}{2C_T} + \frac{kT}{2C_T} + 2\frac{kT}{2C_T} \right] \tag{5.10}$$

$$\overline{v}^2_{out} = 2\frac{kT}{C_T} \left[\frac{C_T}{C_S} \right]^2 \tag{5.11}$$

The input referred mean square noise can be obtained by dividing equation (5.11) by the inverse square of the gain.

$$\overline{v}^2_{input} \approx \left[\frac{C_S}{C_T}\right]^2 \overline{v}^2_{out} = \left[\frac{C_S}{C_T}\right]^2 \left[\frac{C_T}{C_S}\right]^2 2\frac{kT}{C_T} = 2\frac{kT}{C_T} \tag{5.12}$$

If $C_S = C$ and $C_P = C$, then $C_T = 2C$ and the input referred mean square noise is

$$\overline{v}^2_{input} \approx \frac{kT}{C} \tag{5.13}$$

It can be shown that the input referred *mean square* noise contribution from one capacitor S/H block (Figure 5.2) is smaller by a factor of 6 than the one from two-capacitor type (Figure 5.1) assuming $C_S = C_I = C_P = C$.

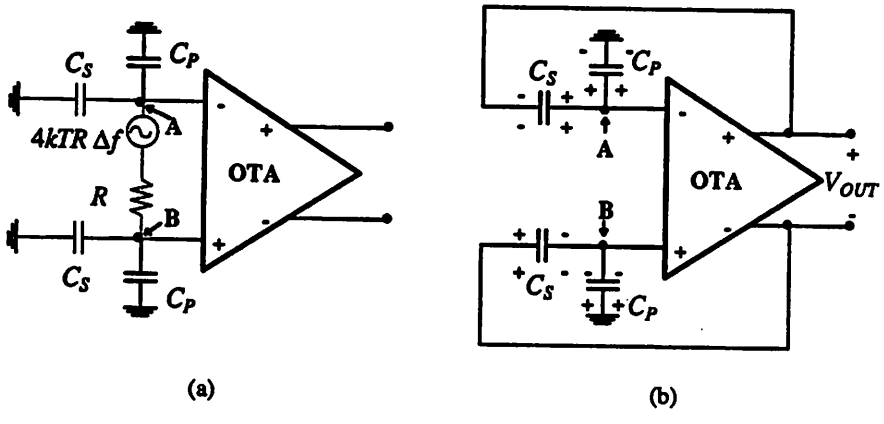


Figure 5.5 (a) Thermal noise due to middle switch and (b) closed loop configuration

5.2.1.3 Input S/H block

The proposed algorithmic A/D converter shown in Figure 4.11 has two S/H blocks. The first S/H block is the one that actually samples the input signal at the beginning of the conversion. Thus, the design of this input S/H circuit will depend on the characteristics of the input signal such as amplitude, frequency, common mode voltage, and common mode frequency. Depending on the duration of the sampling period, each switch in the S/H block has to be designed so that errors are minimized to the allowable level. The most critical ones are the acquisition time, bandwidth, and charge injection into the summing nodes. The allowable amount of charge injected into the summing nodes will depend on the type of input transistors and the op-amp input common mode voltage range.

5.2.2 Amplifier

Ideally the S/H-1, S/H-2, and 2X blocks have different op-amp performance since the requirements of these blocks are different. But to simplify the design procedure, the three blocks use the same op-amp. Among the three blocks, the 2X block is the critical one in that its op-amp gain requirement has to be better than the S/H blocks due to its large feedback factor. Thus the discussion of amplifier design will be described in section 5.3.2.

5.3 2X Block

The discussion of the 2X block will be divided into two sections : the first one will discuss the 2X circuit and its capacitor matching requirement, and the second one will describe the design of the op-amp.

5.3.1 2X Circuit

The gain of two circuit is the same as shown in Figure 5.1 except the capacitor ratio $\frac{C_S}{C_I}$ is equal to two. In order to fully utilize this 2X block, the reference subtraction circuit is also integrated inside by adding reference capacitors C_{REF} and CMOS switches which select $V_{REF}, ground, or -V_{REF}$. The complete 2X block is shown in Figure 5.6.

5.3.1.1 Switching Scheme

At the beginning of each bit conversion, all the capacitors in the block will be initialized to zero by closing switches S3, S4, S7, S8, S9, S10, S11, S12, S13 (Figure 5.7 (a)). During this period, the op-amp also undergoes an initialization period where the common mode voltage for the outputs are initialized, and the offset voltage and noise of the op-amp are stored. The detail of the op-amp initialization will be discussed later. The initialization period is carried out during the sampling of the input signal. Just like the S/H block, the ground switches S9 and S10 are turned off first (Figure 5.7 (b)), followed by S11 (Figure 5.7 (c)). The initialization period is completed when S7, S8, S12 and S13 are turned off and S14 and S15 are turned on, connecting the integrating capacitors to the outputs (Figure 5.7 (d)). At this time, the 2X block is ready to perform multiplication for the rest of the conversion cycles. The reference subtraction switches S1, S2, S3, S4, S5, and S6 will be controlled by the comparator outputs of the previous cycle. Only one switch pair (ie. S1-S2 or S3-S4 or S5-S6) will be on at any given time.

The transfer function of the 2X block can also be analyzed by using conservation of charge on the capacitors. Once again the analysis is simplified by considering a single ended case. During the initialization mode (Figure 5.8 (a)), the charge at node X is zero since all the capacitors are discharged.

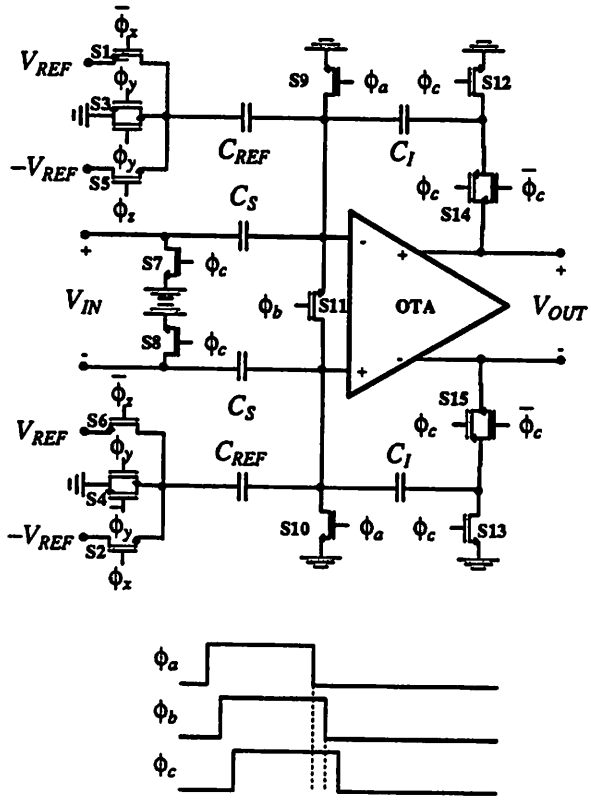


Figure 5.6 2X block

$$Q_T = 0 \tag{5.14}$$

Let us assume nodes A and B are connected to V_A and V_B respectively when the 2X block is in the active mode (Figure 5.8 (b)). Therefore, the total charge at node X at this time is

$$Q_{T+1} = C_S\Big[V_X(T+1) - V_A(T+1)\Big] + C_{REF}\Big[V_X(T+1) - V_B(T+1)\Big] +$$

$$C_I\Big[V_X(T+1) - V_{OUT}(T+1)\Big] + C_P V_X(T+1) \tag{5.15}$$

where $V_i(t)$ = *voltage at node i at time t*

$$V_{OUT}(t) = -A_v V_X(t) \tag{5.16}$$

Equating the charge at node X before and after the initialization :

$$0 = C_S\Big[V_X(T+1) - V_A(T+1)\Big] + C_{REF}\Big[V_X(T+1) - V_B(T+1)\Big] +$$

$$C_I\Big[V_X(T+1) - V_{OUT}(T+1)\Big] + C_P V_X(T+1) \tag{5.17}$$

Substituting equation (5.16) into (5.17) and solve V_{OUT} in terms of V_A and V_B, we get

$$V_{OUT}(T+1) = -\left[\frac{C_S}{C_I + \frac{C_{Total}}{A_v}}\right] V_A(T+1) - \left[\frac{C_{REF}}{C_I + \frac{C_{Total}}{A_v}}\right] V_B(T+1) \qquad (5.18)$$

$$where\ C_{Total} = C_S + C_I + C_{REF} + C_P$$

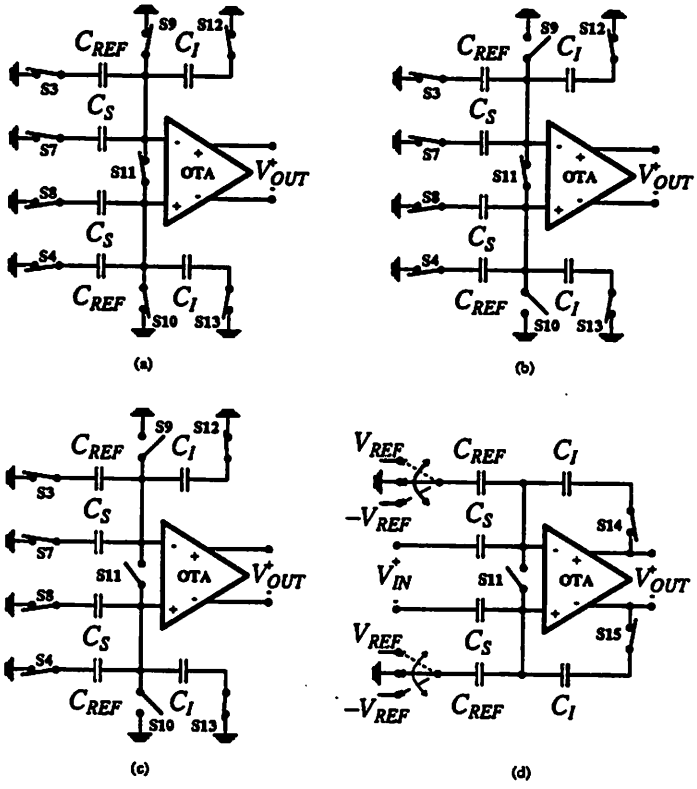


Figure 5.7 (a) Initialization mode (b) Disconnect ground switches S9 and S10 (c) Turn off Middle Switch S11 and (d) Active mode

Equation (5.18) clearly shows that the 2X block functions as a pure multiplier. The accuracy of the multiplier will depend again not only on the matching between C_S and C_I, and C_{REF} and C_I but also on the gain of the op-amp A_v. At high resolution, the accuracy of the multiplier will become critical in determining the overall linearity of the conversion. If the capacitor matching is not good enough, trim arrays for C_S and C_{REF} can be added. A method of calibration of two capacitors using trim arrays will be discussed at the end of this section.

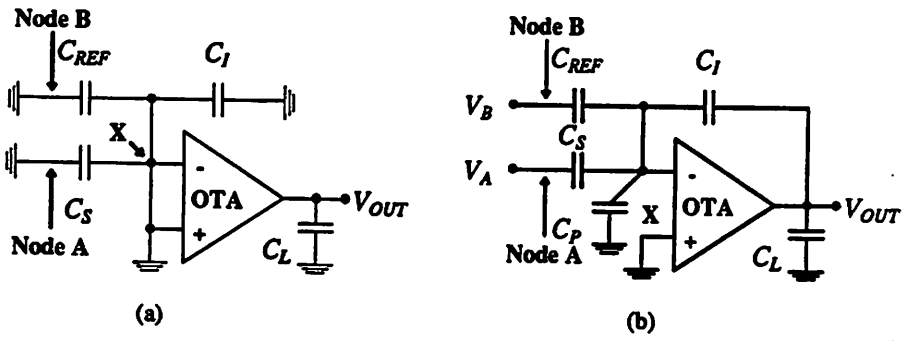


Figure 5.8 (a) Initialization and (b) Active mode configurations

5.3.1.2 Noise Source

Just like the S/H block, the thermal noise for this block comes from the middle switch S11. Carrying out the same derivation, the total input referred mean square noise contribution for this block is

$$\bar{v}^2_{input} = 2\frac{kT}{C_T}\left[\frac{C_T}{C_S}\right]^2 \tag{5.19}$$

$$where\ C_T = C_S + C_{REF} + C_I + C_P$$

If $C_{REF} = C_I = C_P = C$ and $C_S = 2C$, then $C_T = 5C$ and the total input referred mean square noise is :

$$\bar{v}^2_{input} = \frac{5}{2}\frac{kT}{C}. \tag{5.20}$$

Comparing the mean square input referred noise between the S/H and 2X blocks for the same value of unit capacitor, the latter is bigger by a factor of 2.5. Therefore, determination of the size of the smallest unit capacitor based on $\frac{kT}{C}$ noise will be dominated by noise contributed by the 2X block.

5.3.2 Amplifier

The specifications of the 2X block amplifier depend directly on the resolution and conversion speed of the A/D converter. Referring back to equation (4.6), the accuracy of the gain block has to be within $\varepsilon = \frac{1}{2^{N-1}}$. For an 8 bit bit A/D converter, this means $\varepsilon = 0.78\%$. The effective gain from input to output of the 2X block (see Figure 5.6) can be written as

$$Gain = \frac{V_{OUT}}{V_{IN}} = -\left[\frac{C_S}{C_I + \frac{C_S + C_I + C_{REF} + C_P}{A_v}}\right] \geq -(2-\varepsilon) \tag{5.21}$$

If $C_I = C_{REF} = C$ and $C_S = C_P = 2C$, then equation (5.21) can be simplified to

$$Gain = \frac{-2}{1+\frac{6}{A_v}} \geq -(2-\varepsilon) \tag{5.22}$$

$$A_v \geq \frac{6}{\frac{1}{(1-\frac{\varepsilon}{2})} - 1} \tag{5.23}$$

$$\text{if } \frac{1}{1-x} \approx 1+x \text{ for } x \ll 1, \textit{then} \tag{5.24}$$

$$A_v \geq 6(2^N) = 6(2^8) = 1536 \tag{5.25}$$

From the above calculation, the op-amp has to have open loop gain greater than 1536. At higher resolutions, capacitor mismatch also degrades gain accuracy. One way to solve capacitor matching problem is to add a capacitor trim array(this will be discussed later in this chapter).

To achieve 8-bit accuracy at 125kHz, clocks ϕ_1 and ϕ_2 shown in Figure 4.11 have to have a period of 2μs. Assuming the clocks have a 47% duty cycle, the total settling time for 2 op-amps (ie. S/H and 2X blocks) is approximately 940 nanoseconds. A detailed clock division is shown in Figure 5.9. The non-overlap time between ϕ_1 and ϕ_2 is approximately 60 nanoseconds, during which the comparators make their decision decisions and then latch the current bit into the register.

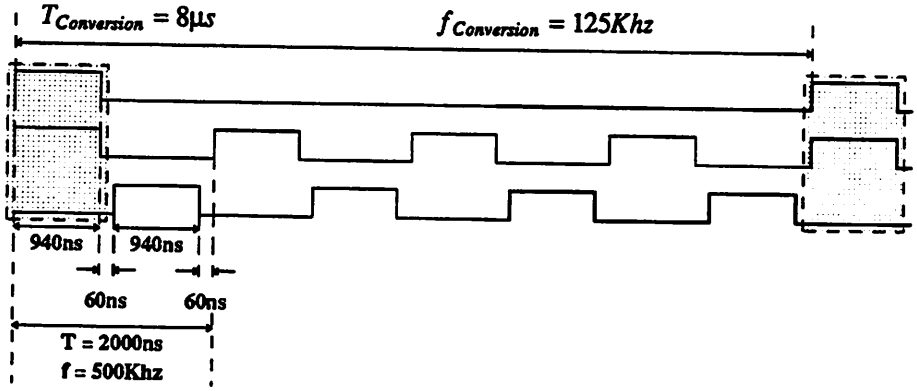


Figure 5.9 Time Allocation

Referring to Figure 5.10, Let t_a be the time required to acquire an input signal to N-bit accuracy for an op-amp in gain block configuration. t_a can be approximated by [5]

$$t_a \geq 0.7N\ \tau_{FB} \tag{5.26}$$

where τ_{FB} = output time constant with feedback

Let t_{a1} and t_{a2} be the settling time for S/H and 2X blocks respectively.

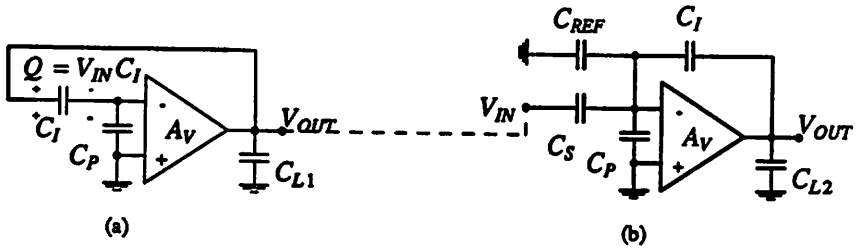


Figure 5.10 (a) S/H block in holding mode and (b) 2X block in multiplying mode

For the 2X block :

$$\tau_{FB2} = \frac{\tau_2}{1 + A_v\left[\dfrac{C_I}{C_S + C_I + C_{REF} + C_P}\right]} \tag{5.27}$$

where τ_2 is the output time constant of the 2X block.

A_v is the DC open-loop gain

For the S/H block :

$$\tau_{FB1} = \frac{\tau_1}{1 + A_v\left[\dfrac{C_I}{C_I + C_P}\right]} \tag{5.28}$$

$$\tau_i = R_{OUT}(C_{Li} + C_I) \tag{5.29}$$

where N = number of bits

R_{OUT} = the open-loop output resistance of the op-amp

C_{Li} = total loading capacitor at the output of the op-amp

i = the S/H or 2X blocks

Therefore, 940ns is the total time $t_{a1} + t_{a2}$ for both blocks to settle within N bits of accuracy. The assumption here is not exactly accurate since while the S/H block is in the hold mode, the 2X block is in the multiplication mode. The output of the S/H block is connected to the input of 2X block. Therefore, as the output of the S/H block (the input of the 2X block) is slewing and settling, the 2X block is also slewing

and settling. Effectively, the total slewing and settling time for the combined two blocks are less than 2 op-amp settling times. For illustration purpose, the 2 op-amp settling time is used. If $C_S = C_P = 2C_I = 2C_{REF}$, $\tau_1 = \tau_2$, τ_{FB1} and τ_{FB2} can be approximated by :

$$\tau_{FB1} = \frac{\tau}{1 + \frac{A_v}{2}} \approx \frac{\tau}{\frac{A}{2}} \tag{5.30}$$

$$\tau_{FB2} = \frac{\tau}{1 + \frac{A_v}{6}} \approx \frac{\tau}{\frac{A}{6}} \tag{5.31}$$

$$\tau_{FB2} \approx 3\tau_{FB1} \tag{5.32}$$

$$t_{Total} \geq t_{a1} + t_{a2} \approx 0.7N(\tau_{FB1} + \tau_{FB2}) \approx 0.7N(4\tau_{FB1}) = 2.8N\tau_{FB1} \tag{5.33}$$

For N = 8 and $t_{Total} \geq$ 940ns, $\tau_{FB1} \leq$ 42ns, corresponding to a closed-loop -3 dB bandwidth of about 3.8Mhz.

From equation (5.32), the time for the 2X block to settle is around $\frac{3}{4}$ of 940ns which is around 705ns. Assuming half of the 705ns is for slewing and the other half is for settling, for $C_L + C_I \approx 5pF$ and $4V$ peak-to-peak swing, the slew rate has to be least 11.36 $\frac{Volts}{\mu s}$ and output charging current 71 μA. The necessary input transconductance of the op-amp G_m would then be approximately G_m = 0.4 mA/volt.

In the rest of this section, the chosen op-amp topology and the techniques to reduce the offset and noise of the amplifier will be presented.

5.3.2.1 Basic Op-amp Topology

Before analyzing the op-amp behavior, all the symbols used in the equations are defined below.

$A_0 = dc\ open\ loop\ gain$

$R_{OUT} = equivalent\ output\ resistance$

$z_1 = the\ zero\ of\ the\ transfer\ function$

$p_1 = the\ dominant\ pole\ of\ the\ op-amp$

$p_2 = the\ first\ non\ dominant\ pole$

$p_3 = the\ second\ non\ dominant\ pole$

$C_{LX} = total\ capacitance\ at\ node\ X$

g_{mi} = *transconductance of transistor i*

g_{oi} = *output conductance of transistor i*

C_{gdi} = *capacitor between gate–drain of transistor i*

C_{gsi} = *capacitor between gate–source of transistor i*

C_{dbi} = *capacitor between drain–bulk of transistor i*

C_{sbi} = *capacitor between source–bulk of transistor i*

V_{VDSATi} = *saturation voltage of transistor i*

V_{GS} = *gate source voltage*

V_{ti} = *threshold voltage of transistor i*

$$\Delta V_{t(i-j)} = V_{ti} - V_{tj}$$

$$(\frac{W}{L})_{(i-j)} = \frac{(\frac{W}{L})_i + (\frac{W}{L})_j}{2}$$

$$\Delta(\frac{W}{L})_{(i-j)} = (\frac{W}{L})_i - (\frac{W}{L})_j$$

$\overline{v^2}_i$ = *equivalent input referred noise* for *transistor i*

K_f = *flicker noise coefficient* $= 3X\,10^{-12}V^2pF$

R_X = *equivalent resistance at node X*

A fully differential folded-cascode CMOS amplifier shown in Figure 5.11[15], is chosen because it can achieve high gain and is simple in topology. The transfer function of the folded cascode is

$$\frac{V_{OUT}}{V_{IN}}(s) = A_d(s) = A_0 \frac{(1+\frac{s}{z_1})}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})(1+\frac{s}{p_3})} \tag{5.34}$$

Where :

$$A_0 = -g_{m1}R_{OUT} \tag{5.35}$$

$$R_{OUT} = \frac{1}{(G_1+G_2+G_3)} \tag{5.36}$$

$$G_1 = \frac{(g_{o1}+g_{o4})g_{o6}}{(g_{m6}+g_{mb6}+g_{o6})} \tag{5.37}$$

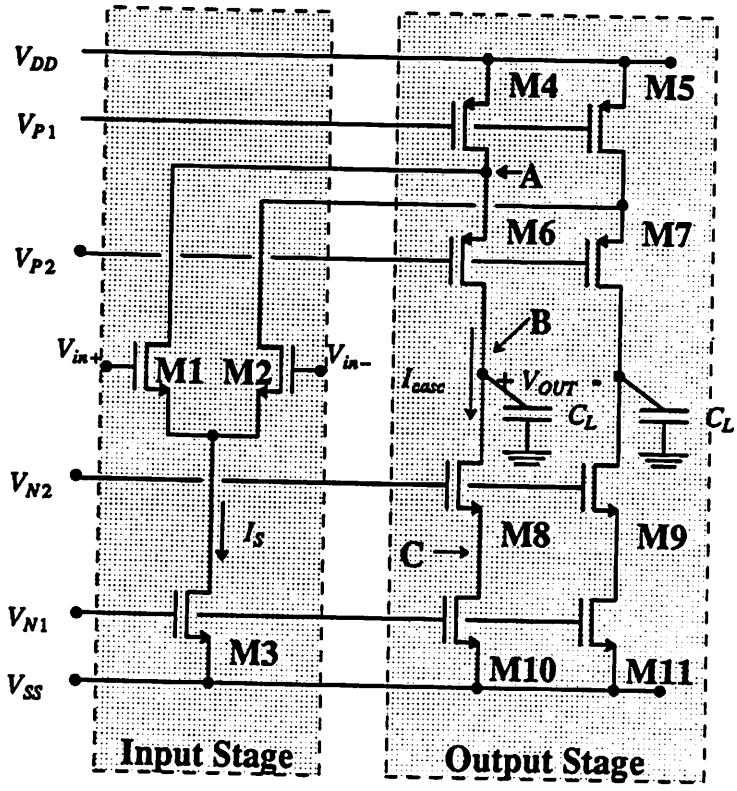


Figure 5.11 Fully differential Folded Cascode Amplifier without common mode feedback circuit

$$G_2 = \frac{(g_{o8}g_{o10})}{(g_{o10} + g_{o8} + g_{m8} + g_{mb8})} \tag{5.38}$$

$$G_3 = \frac{(g_{o1} + g_{o4})(g_{o6}g_{o10})}{(g_{m6} + g_{mb6} + g_{o6})(g_{o10} + g_{o8} + g_{m8} + g_{mb8})} \tag{5.39}$$

$$z_1 \approx \frac{(g_{o10} + g_{o8} + g_{m8} + g_{mb8})}{C_{LC}} \tag{5.40}$$

$$p_1 \approx \frac{1}{R_{OUT}C_{LB}} \tag{5.41}$$

$$p_2 \approx \frac{(g_{o1} + g_{o4} + g_{06} + g_{m6} + g_{mb6})}{C_{LA}} \tag{5.42}$$

$$p_3 \approx \frac{(g_{o10} + g_{o8} + g_{m8} + g_{mb8})}{C_{LC}} \tag{5.43}$$

$$C_{LA} = C_{gd1} + C_{db1} + C_{gd4} + C_{gs6} + C_{sb6} \tag{5.44}$$

$$C_{LB} = C_{gd6} + C_{db6} + C_{gd8} + C_{db8} + C_L \tag{5.45}$$

$$C_{LC} = C_{gs8} + C_{sb8} + C_{gd10} + C_{db10} \tag{5.46}$$

Design procedures for this type of op-amp is summarized in Table 5.1.

Table 5.1

Specification	Equation
Unity gain frequency	$\omega_0 = \frac{g_{m1}}{C_{LB}}$
Phase margin	$PM = \frac{\pi}{2} - \tan^{-1}(\frac{\omega_0}{p_2})$
Slew Rate	$SR = \frac{I_S}{2C_{LB}}$
Cascode bias current	$I_{casc} = MAX(I_S, \frac{1}{2}\omega_0 V_{DSAT6}\tan(PM))$
Output swing	$V^+_{out} = V_{DD} - \lvert V_{DSAT4}\rvert - \lvert V_{DSAT6}\rvert$ $V^-_{out} = V_{SS} + \lvert V_{DSAT10}\rvert + \lvert V_{DSAT8}\rvert$
Total power	$PWR = (2I_{casc} + I_S)(V_{DD} - V_{SS})$

The input referred offset voltage is :

$$V_{OS} = \Delta V_{t(1-2)} + \frac{(V_{GS}-V_t)_{(1-2)}}{2}\left[\frac{\Delta(\frac{W}{L})_{(1-2)}}{(\frac{W}{L})_{(1-2)}} + \frac{\Delta(\frac{W}{L})_{(4-5)}}{(\frac{W}{L})_{(4-5)}} + \frac{\Delta(\frac{W}{L})_{(10-11)}}{(\frac{W}{L})_{(10-11)}}\right] \tag{5.47}$$

The equivalent input referred noise is :

$$\overline{v}^2_{eq} = 2\left[\overline{v}^2_1 + \overline{v}^2_4\left[\frac{g_{m4}}{g_{m1}}\right]^2 + \overline{v}^2_{10}\left[\frac{g_{m10}}{g_{m1}}\right]^2 + \overline{v}^2_6\left[\frac{1}{g_{m1}R_A}\right]^2 + \overline{v}^2_8\left[\frac{1}{g_{m1}R_C}\right]^2\right] \tag{5.48}$$

$$\overline{v}^2_i = \left[4kT\frac{2}{3}\frac{1}{g_{mi}} + \frac{K_f}{W_i L_i C_{ox} f}\right]\Delta f \tag{5.49}$$

In order to boost the gain, a double NMOS and PMOS input stage was used. The complete core of the op-amp is shown in Figure 5.12. The performance of the op-amp is summarized in Table 5.2.

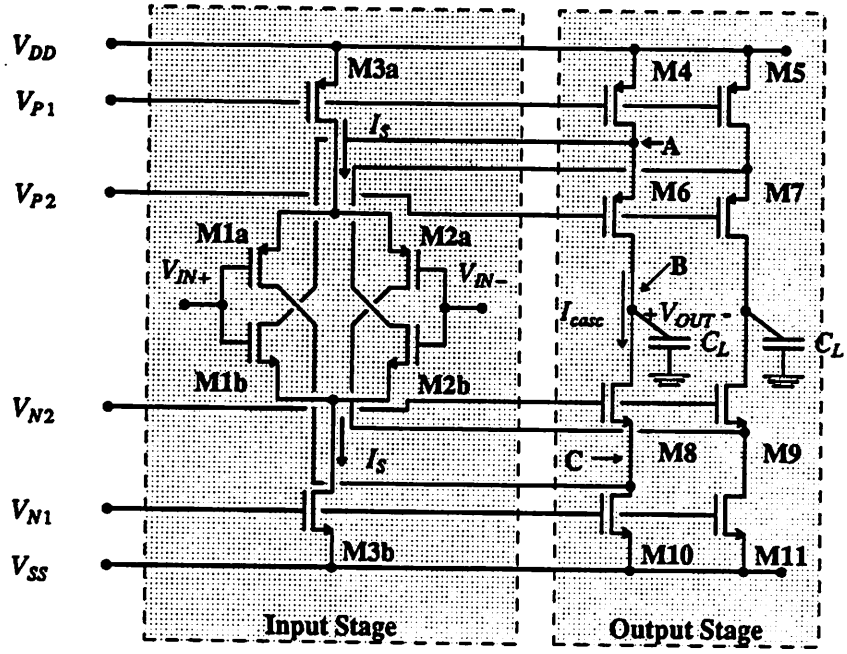


Figure 5.12 Modified folded cascode amplifier

5.3.2.2 Common Mode Feedback Circuit

The common mode feedback (CMFB) circuit is needed in order to control the common mode voltage of the output nodes[16]. There are two types of CMFB circuits: continuous[17] and dynamic[5,18,19]. The difference between the two types is that the dynamic approach needs clocks, whereas, the continuous one does not. However, the continuous CMFB circuit is not very desirable because it limits the output swing of the op-amp.

A simple dynamic CMFB circuit can be obtained by using only two capacitors and a CMOS switch as shown in Figure 5.13. The operation of the CMFB circuit is as follows : During the initialization cycle, the voltage across capacitors are initialized to their respective voltages. When the op-amp is in the active mode, S1 will be *opened* and the two capacitors C_{CM1} and C_{CM2} will sense the output common mode voltage. If the common mode output voltage is higher(lower) than the initial voltage, V_A will also go up(down). As a result, more(less) current will be drawn by M10 and M11 to pull down(up) the output common mode voltage. If there is a mismatch between C_{CM1} and C_{CM2}, noise from the supply line V_{SS} will be

injected or coupled to the output nodes through C_{gs10}–C_{CM1} and C_{gs11}–C_{CM2} and appears as a differential output voltage. At high resolution, the amount of noise injected through the supply line may affect the linearity of the conversion.

Table 5.2
Op-amp Performance Summary

Gain	65dB
Unity gain frequency	20Mhz
Phase Margin	63^0
Slew rate	11.8V/μs
Settling time to 0.1%	335ns
R_{OUT}	4.359Mohms
Output Swing	±1.5V
Input Capacitance	1.5pF

Figure 5.14 illustrates a more complicated CMFB circuit in that it consumes more area and power; however, power supply noise is not a problem. The basic operation is the same as before. During the initialization, S1 and S2 are closed to initialize the voltages at nodes A1 and A2. Then, S1 and S2 are opened and S3 is closed. Thus, C_{CM1} and C_{CM2} function as output common mode voltage sensors. In order to cover a broad spectrum of resolution of A/D converter(ie. from 6 up to 12 bits), this CMFB circuit is implemented in this 8-bit Algorithmic A/D converter prototype even though the simple CMFB circuit is sufficient.

5.3.2.3 Biasing Circuit

A high swing folded cascode biasing circuit generating the bias voltages V_{N1} and V_{N2} for NMOS transistors is shown in Figure 5.15. The basic circuit is similar to the one reported previously[4] with some modifications. Transistor M2 is designed to be in the linear region by making its aspect ratio larger than that of M1. The purpose is to make the V_{DS} of M2 to be a low impedance voltage source and set the V_G of

transistor M3. The resulting V_{G3} can be used to bias the cascode NMOS transistors of the core op-amp.

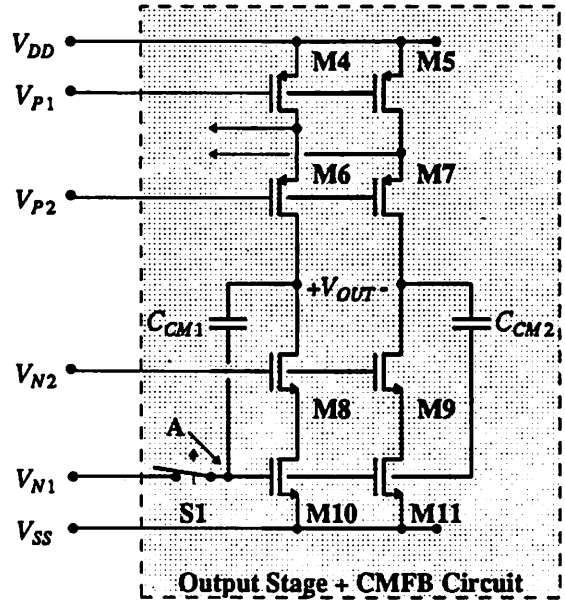


Figure 5.13 Simple common mode feedback circuit

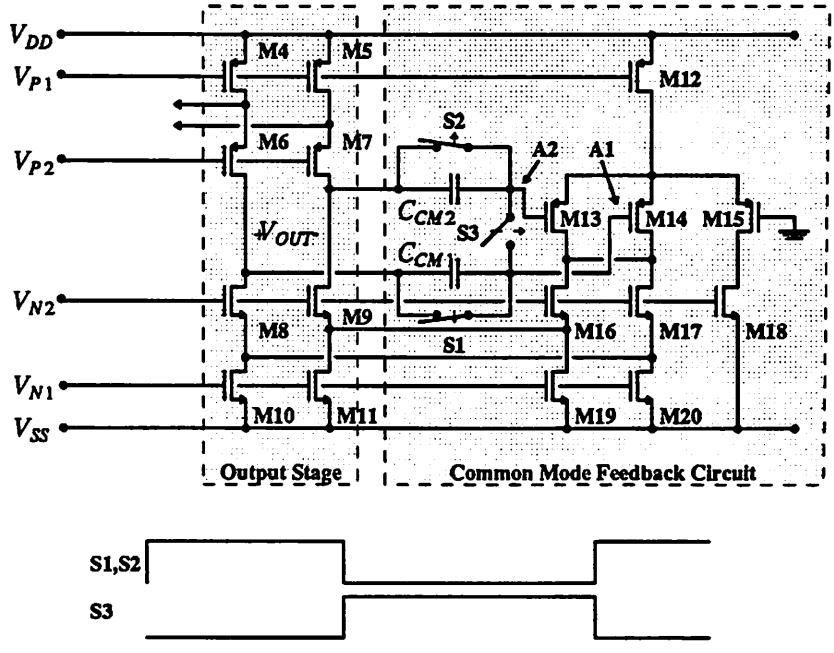


Figure 5.14 Common mode feedback circuit with better PSSR

In order to guarantee that the two bias lines V_{N1} and V_{N2} track, M4-M7 are added. Transistor M4 forms a feedback loop from V_{D6} so that M6 can operate in deep saturation region. Unfortunately, this biasing circuit requires more power and area. The complementary bias circuit is used to generate biasing voltages V_{P1} and V_{P2}.

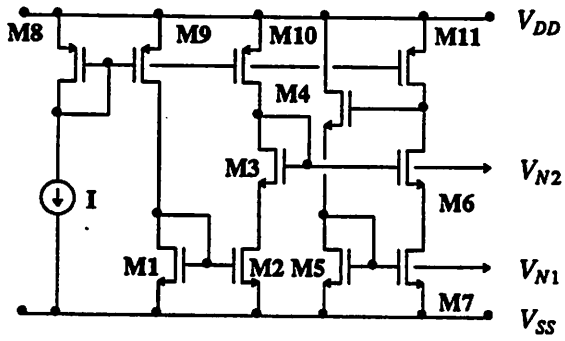


Figure 5.15 High swing folded cascode biasing circuit

5.3.2.4 Auto-Zero Circuit

At high resolution, offset voltages and charge injection due to op-amp and CMOS switches will affect the overall linearity of Algorithmic A/D converter. In order to reduce these effects, an auto-zero circuit can be added into the op-amp[4,7] as shown in Figure 5.16. This auto-zero circuit can be treated as an auxiliary op-amp(A_2) with its inputs connected to the outputs of the main op-amp(A_1) to form a feedback loop. The storing of these offset voltages can be carried out during the initialization of the block, thus no extra clock periods are needed to include the auto-zero circuit.

Let V_{os1} be the offset voltage of the op-amp. When ϕ_a, ϕ_b, and ϕ_c go high, all switches are closed, and V_{os1} gets amplified by A_1, fed back by A_2, and eventually an equilibrium is established. The voltage across node 3 and 4 is stored on capacitor C_{az} and is equal to

$$V_{3-4} = \frac{-A_1 V_{os1}}{1 + A_2} \tag{5.50}$$

When ϕ_a and ϕ_b go low, S1,S2 and S3 will get turned off and inject charges into node 1 and 2. The differential error voltages ΔV_1 between these two nodes will also get amplified by A_1 and stabilized since the feedback mechanism is still active. Therefore, the voltage across node 3 and 4 will be

$$V_{3-4} = \frac{-A_1 (V_{os1} + \Delta V_1)}{1 + A_2} \tag{5.51}$$

When ϕ_c goes low, S4 and S5 will inject charge into noded 3 and 4. This injected charge results in a voltage across nodes 3 and 4. The total voltage difference across nodes 3 and 4 due to these 3 error sources is given by

$$V_{3-4} = \frac{-A_1(V_{os1} + \Delta V_1)}{1 + A_2} + \Delta V_2 \tag{5.52}$$

Across the output nodes of the op-amp, the voltage will be equal to

$$V_{out} = -A_1\left[\frac{(V_{os1} + \Delta V_1)}{1 + A_2} + \Delta V_2 \frac{A_2}{A_1}\right] \tag{5.53}$$

This can be referred back to the input by dividing equation (5.53) by $-A_1$, resulting in an input referred offset of

$$V_{in} = \left[\frac{(V_{os1} + \Delta V_1)}{1 + A_2} + \Delta V_2 \frac{A_2}{A_1}\right] \tag{5.54}$$

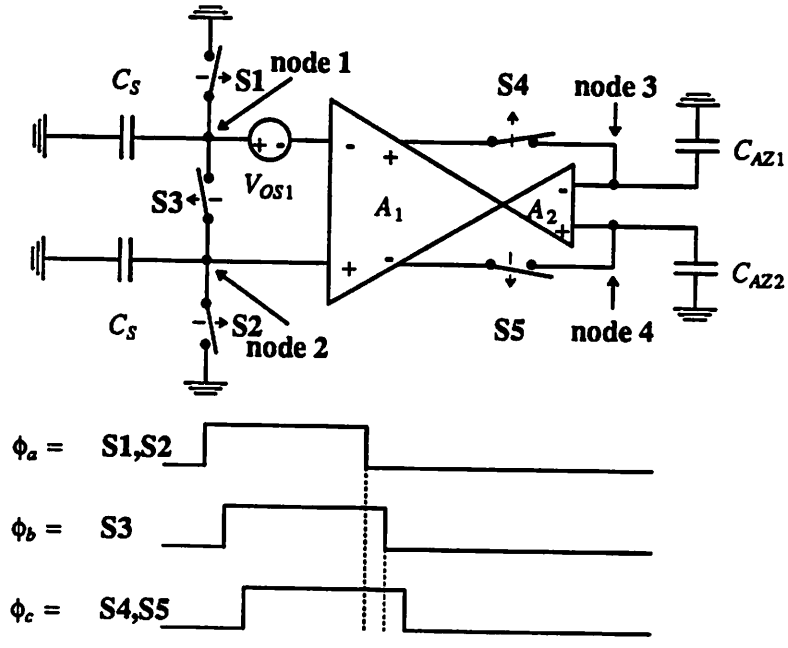


Figure 5.16 Op-amp with auto-zero circuit

Therefore, the offset voltage due to op-amp and charge injection at the input nodes are attenuated by $(1 + A_2)$, and the charge injection due to switch S4 and S5 is reduced by a factor of $\frac{A_2}{A_1}$. The optimum

value for A_2 turns out to be $\frac{1}{10}$ of A_1 or in other words, g_{m2} is equal to $\frac{g_{m1}}{10}$ where g_{m1} and g_{m2} are the input transconductances of the main and auxiliary op-amps respectively. For an 8-bit resolution $A_1 \geq 1536$ (equation (5.25)) and $A_2 \approx 153$. The offset voltage due to the op-amp and switch charge injection at the input nodes is 0.65% of the actual value, whereas, those from S4 and S5 is 10% of the initial value. Thus the charge injection due to S4 and S5 will dominate the offset error. Careful design is needed to ensure that ΔV_2 is small enough. Figure 5.17 shows how the main and auxiliary op-amps are connected at the transistor level.

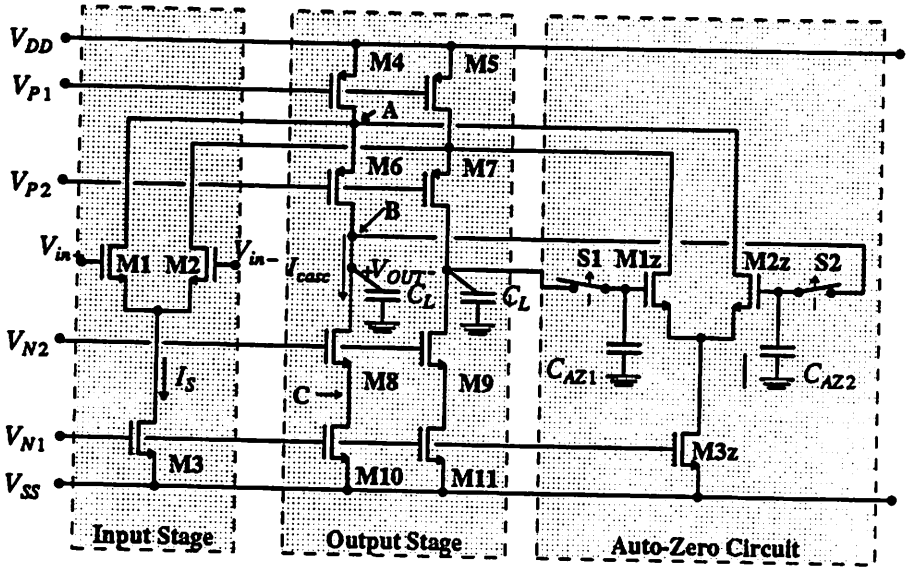


Figure 5.17 Complete op-amp with auto-zero circuit

5.3.2.5 Noise Reduction

The beauty of the auto-zero circuit described above is that it reduces the noise in the 2X block by a factor of $\frac{g_{m1}}{g_{m2}}$. Let us assume the equivalent mean square noise at the input of the op-amp be

$$\bar{v}_{eq}^{\,2} \approx 4kT\frac{b}{g_{m1}}\Delta f \tag{5.55}$$

where b = a constant factor

This noise voltage will then get amplified and appear across v_{3-4} (see Figure 5.16).

$$\bar{v}_{3-4}^{\,2} \approx \left[\frac{g_{m1}}{g_{m2}}\right]^2 \bar{v}_{eq}^{\,2} = \left[\frac{g_{m1}}{g_{m2}}\right]^2 4kT\frac{b}{g_{m1}}\Delta f \tag{5.56}$$

Let us also assume that the -3dB frequency of the auxiliary circuit is equal to

$$\omega_{-3dB} = \frac{g_{m2}}{C_{ax}} \tag{5.57}$$

$$f_{-3dB} = \frac{1}{2\pi}\frac{g_{m2}}{C_{ax}} \tag{5.58}$$

The equivalent noise bandwidth can then be approximated [15]

$$f_N = \frac{\pi}{2} f_{-3dB} = \frac{1}{4}\frac{g_{m2}}{C_{ax}} \tag{5.59}$$

Substituting f_N for Δf in equation (5.27), the mean square noise across node 3 and 4 is

$$\bar{v}_{3-4}^{\,2} = b\left[\frac{g_{m1}}{g_{m2}}\right]\left[\frac{kT}{C_{ax}}\right] \tag{5.60}$$

When switches S4 and S5 are turned off, this noise is sampled onto C_{ax}. Referring this noise back to the op-amp input by dividing equation (5.31) by $\left[\frac{g_{m2}}{g_{m1}}\right]^2$, we get

$$\bar{v}_{eq,input}^{\,2} = b\left[\frac{g_{m2}}{g_{m1}}\right]\left[\frac{kT}{C_{ax}}\right] \tag{5.61}$$

Therefore, the $\frac{kT}{C}$ noise on C_{ax} gets attenuated by the same factor as the ratio between $\frac{g_{m2}}{g_{m1}}$.

5.4 Comparator Blocks

Figure 5.18 shows a comparator block. At the beginning of the conversion ie. when the input signal is sampled onto the S/H-1 block, the comparators are being initialized. The threshold voltages($\pm\frac{V_{REF}}{4}$) are sampled onto capacitors C_1 and C_2 by closing switches S1, S2, S5, and S6. At the end of the initialization, S5 and S6 are opened first, followed by the opening of S1, S2 and the closing of S3 and S4. Now the comparator is ready to do the comparison. At the beginning of the next input sample, the comparators will again be initialized.

The comparator design is very simple since the offset voltage of the comparator is not an issue here. As long as the comparators make decisions in less than the allowable time slot which is 60ns, any type of comparator will do the job. Figure 5.19 shows the schematic of a comparator circuit where the comparator is realized by a simple regenerative latch[8,10]. The operation of the comparator is as follows :

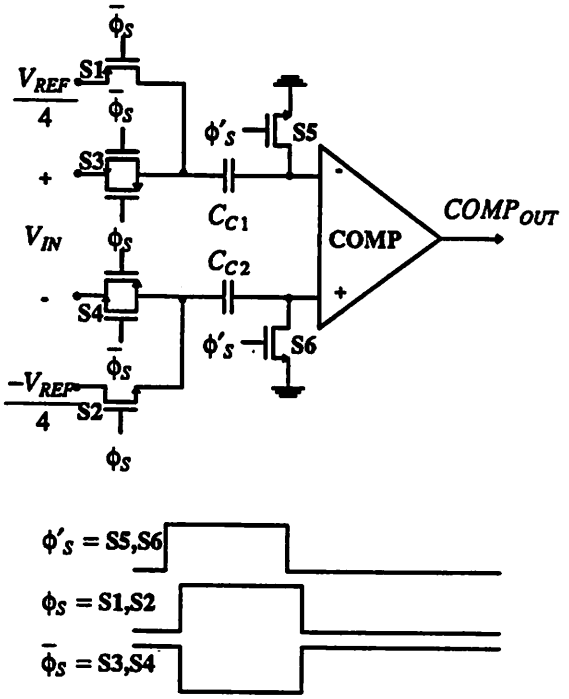


Figure 5.18 Comparator Block

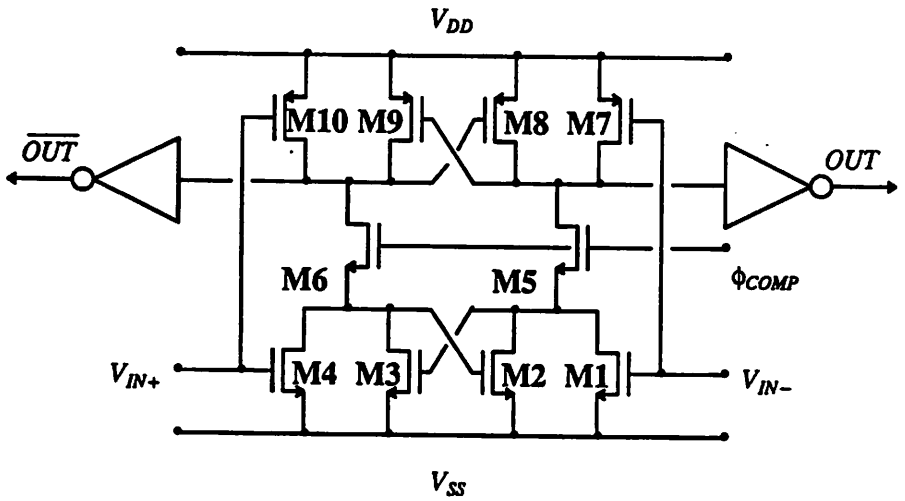


Figure 5.19 Comparator Circuit

1. When ϕ_{COMP} is low, the PMOS transistors (M7-M10) are disconnected from the NMOS transistors (M1-M4) by M6 and M5. During this time, the inputs of the comparator are changing and settling

which in turns affect the values of effective resistors M1, M4, M7, and M10.

2. When ϕ_{COMP} goes high, the comparator outputs will go to logic 1 or 0 depending on the resistances and capacitances on the drains of M1-M10. To avoid unbalanced parasitic capacitance at the output nodes due to routing, two inverters are added.

5.5 Digital Circuits

All the necessary digital circuitry has also been integrated into the prototype. Referring back to section 4.4, the decision bits from comparators are used to decide the current bit, the correction of previous bits if necessary, and for controlling the reference subtraction circuit switches. Table 5.3 shows how the comparator outputs are decoded.

Table 5.3

Decoder Summary

V_{IN}	$COMP_{OUT1}$	$COMP_{OUT2}$	Ref.Clock	Current Bit	SELECT
Reset	0	0	CONNECT TO GRND	0	PASS
$\geq \frac{V_{REF}}{4}$	0	1	SUBTRACT V_{REF}	1	PASS
$\leq \frac{-V_{REF}}{4}$	1	0	ADD V_{REF}	1	CORRECTION
$\frac{-V_{REF}}{4} <—> \frac{V_{REF}}{4}$	1	1	CONNECT TO GRND	0	PASS

The complete digital error correction block is shown in Figure 5.20. The details of the reference clock logic schematic is omitted since it is trivial.

5.6 Trim Array

The prototype A/D converter actually does not need a capacitor trim array because the capacitor matching is good up to around 8 to 9 bits [20,21,22,23,24]. However, in order to verify the calibration scheme for application where it is necessary, trim arrays for the 2X block capacitors have been integrated into the prototype. The calibration sequence for this 1-bit/cycle Algorithmic A/D converter is different from the regular ones[4,25] because both C_I and C_{REF} need to be trimmed with respect to C_S. As a reminder, $C_S = 2C_I = 2C_{REF}$. The calibration of these capacitors will be carried out in two different

procedures.

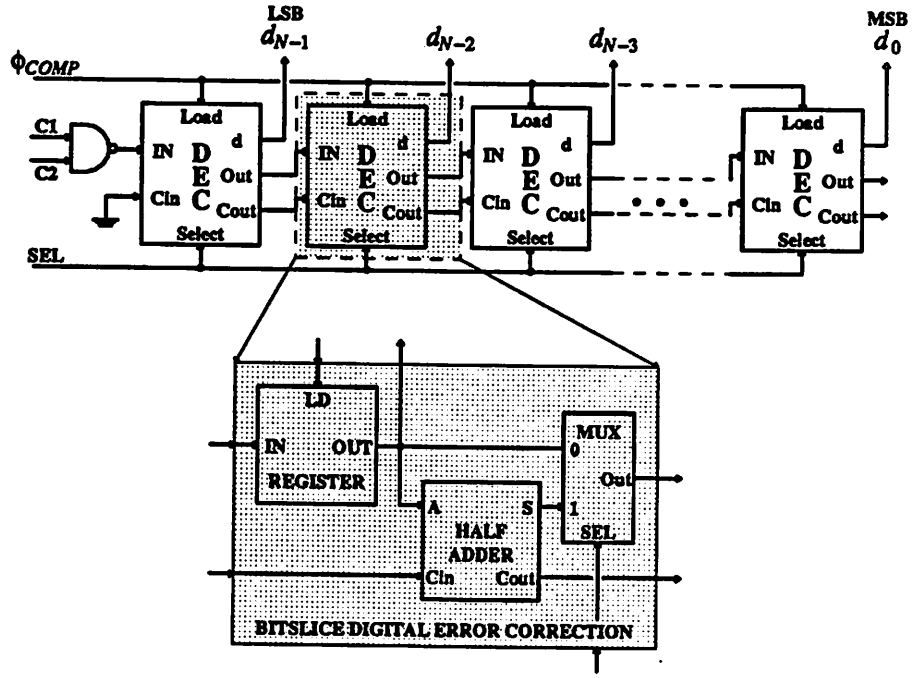


Figure 5.20 Digital Error Correction Block

1. C_{REF} is trimmed to be half of C_S. Refer back to Figure 5.6 (for simplicity a single ended case is discussed here), initially capacitor C_{REF} is initialized to V_{REF} by closing switches S1, S7, S9, and S12 as shown in Figure 5.21 (a). The total charge at node X at this time will be

$$Q_T = C_{REF}(0 - V_{REF}) \tag{5.61}$$

Then, switches S1, S9 and S7 are opened; and S5 is closed and a voltage V_{REF} is applied at the input (node A) as shown in Figure 5.21 (b). The voltage at node X will be

$$V_X = \left[\frac{C_S}{C_T} - \frac{2C_{REF}}{C_T}\right] V_{REF} \tag{5.62}$$

$$where\ C_T = C_S + C_{REF} + C_I + C_P$$

If $C_S \neq 2C_{REF}$, V_X will be non-zero. If $C_S < 2C_{REF}$, $V_X < 0$. As a result, the op-amp functioning as a high-gain comparator, will give a logic "0". By trimming the capacitor trim array for C_{REF}, eventually the output of the open-loop op-amp will switch from logic "0" to logic "1". At this time, the value of $C_S \simeq 2C_{REF}$.

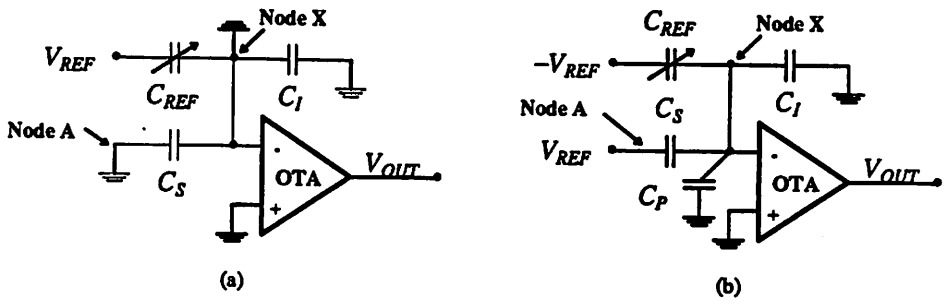


Figure 5.21 C_{REF} Trimming Steps

2. C_I is trimmed to be half of C_S. This calibration scheme can be carried out by applying a full scale voltage V_{REF} at the input of the converter and doing the conversion cycle as shown in Figure 5.22. Again by trimming the capacitor trim array for C_I, we can find the transition between code 1111...111 and 1111...110 (if $C_S > C_I$) or 1111...110 and 1111...111 (if $C_S < C_I$).

As a rule of thumb, the number of bits needed for the trim array is roughly equal to N - 8 where N is the number of bits (N > 9 bits). An example of a 3 bit trim array[26] is shown in Figure 5.23.

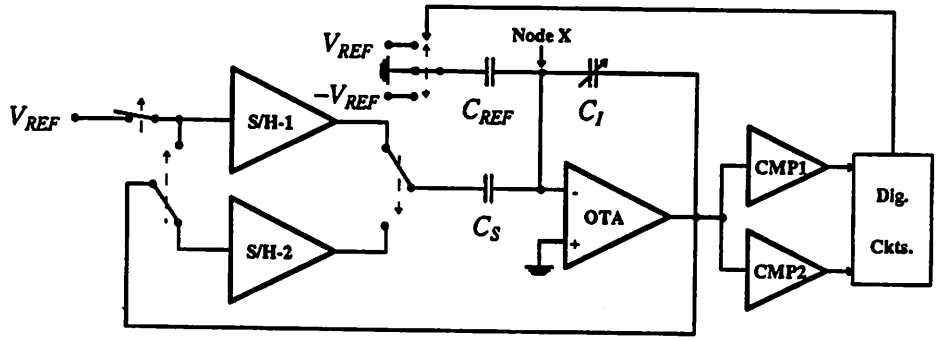
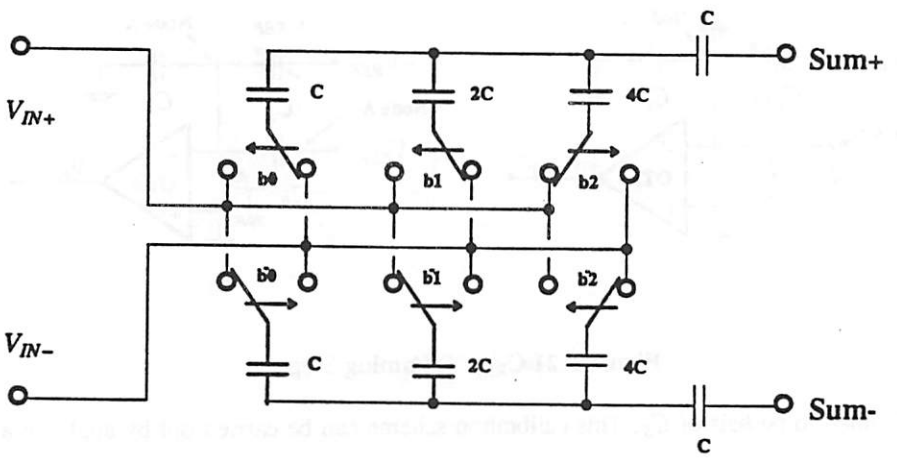


Figure 5.22 C_I trimming step

5.7 Complete Prototype Layout

The complete layout prototype of a 1-bit/cycle Algorithmic A/D converter shown in Figure 5.24. Simulated performance obtained by using a simple behavioral model indicated that the linearity performance requirements of the prototype should be met. The expected differential nonlinearity and integral nonlinearity error plots are shown in Figure 5.25 and Figure 5.26 respectively. The A/D converter prototype performance is summarized in Table 5.4.



(a)

Figure 5.23 3-Bit Trimming array

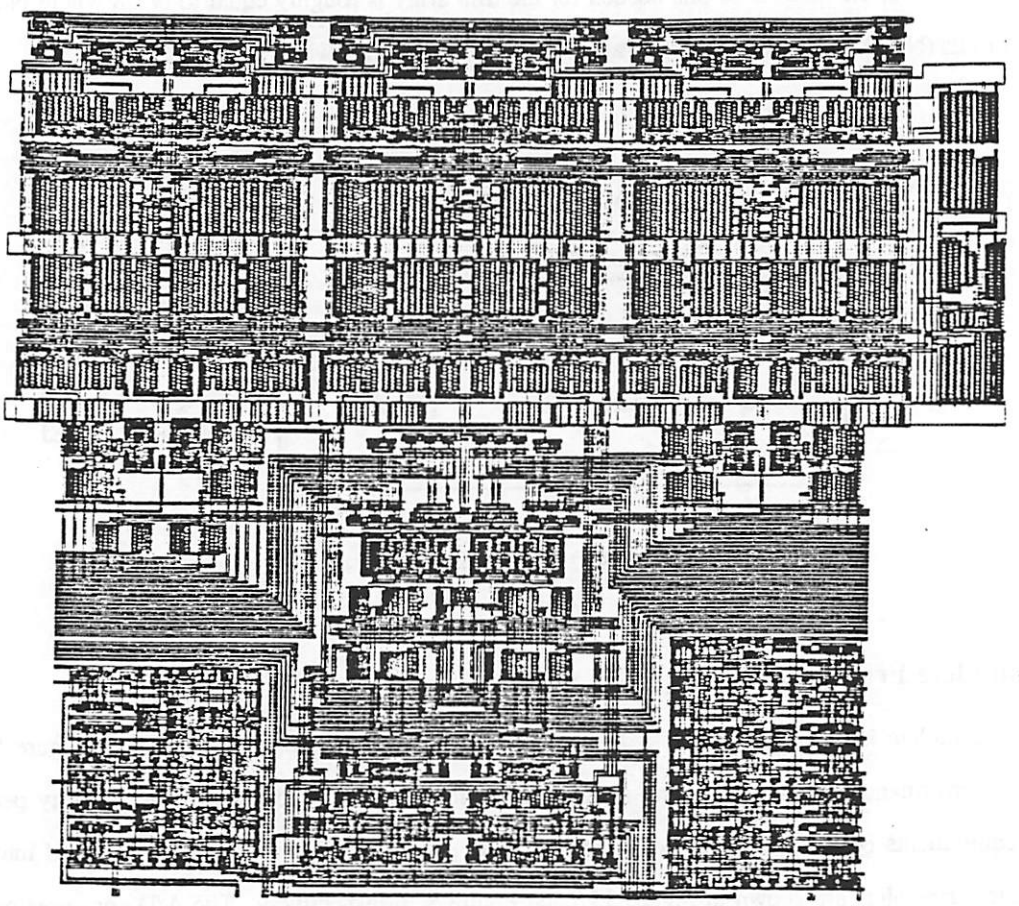


Figure 5.24 125kHz 8-Bit Algorithmic A/D Converter Layout

Figure 5.25 DNL versus Digital Codes

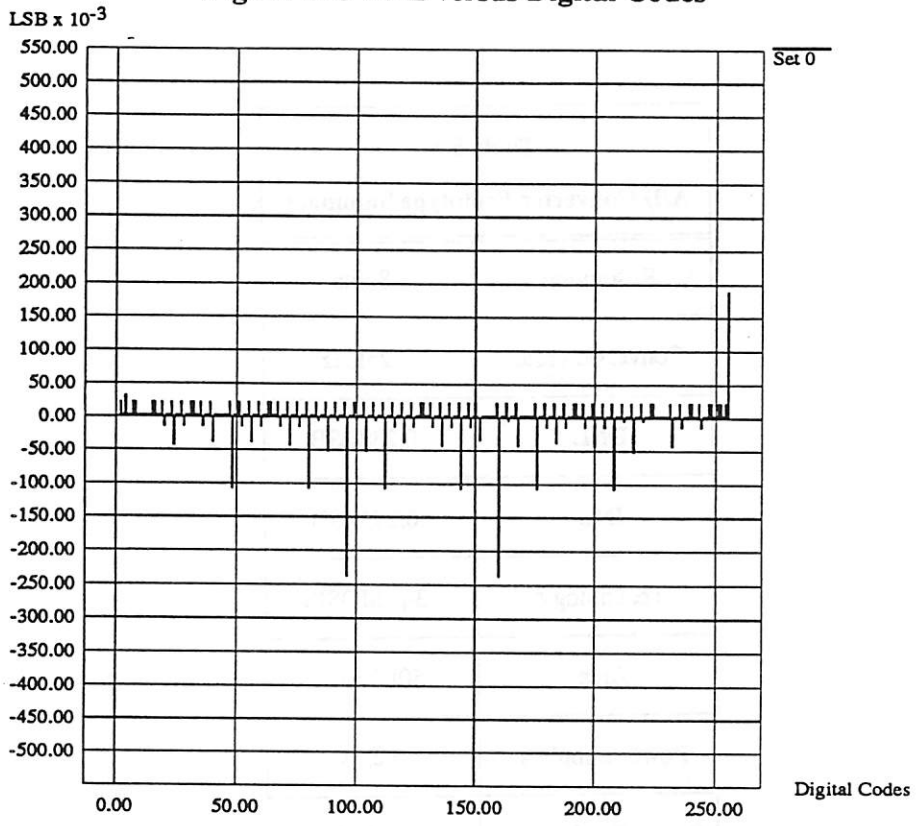


Figure 5.26 INL versus Digital Codes

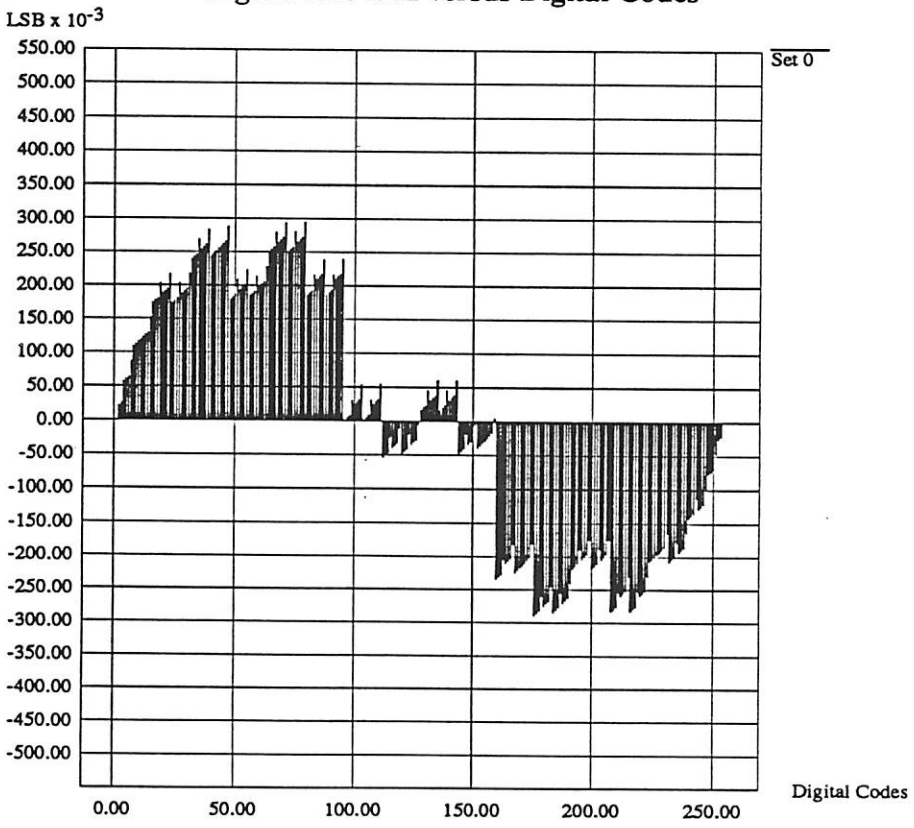


Table 5.4. A/D Converter Prototype Summary	
Resolution	8 bits
Conversion rate	125kHz
DNL	0.238LSB
INL	0.294LSB
Technology	3-μ MOSIS
Area	5082 $mils^2$
Power Supplies	±2.5V
Power Dissipation	9.72 mW
Input Capacitance	2 pF

CHAPTER 6

Conclusions

A new improved algorithmic analog-to-digital converter technique has been presented. The proposed architecture is capable of resolving 1 bit per cycle. The proposed algorithmic A/D converter consists of 2 sample and hold blocks, a gain of two block, 2 comparators, and some digital circuits. Many limitations of the conventional algorithmic A/D coverter are solved or reduced by analog as well as digital circuit techniques.

1. The loop offset sensitivity is solved by implementing an auto-zeroing circuit which reduces the offset and charge injection of switches to a negligible level.
2. A two-comparator scheme is introduced together with digital error correction circuit so that no high precision comparator is needed.
3. A fully differential architecture is used through out the design to improve the power supply rejection ratio and charge injection error from switches.
4. With the addition of auto-zero circuit, the $\frac{kT}{C}$ noise of the op-amp is also reduced.

An 8-bit 125Khz algorithmic A/D converter prototype of the proposed architecture has been designed, laid-out in 3-μm CMOS process and fabricated through MOSIS. The prototype has differential linearity error of 0.238 LSB and integral linearity of 0.294 LSB. The total area which includes both analog and digital circuits of the prototype is 5082 $mils^2$.

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