

Copyright © 1992, by the author(s).
All rights reserved.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission.

**A CMOS IC NONLINEAR RESISTOR
FOR CHUA'S CIRCUIT**

by

José M. Cruz and Leon O. Chua

Memorandum No. UCB/ERL M92/16

20 February 1992

COVER 1/16/92

**A CMOS IC NONLINEAR RESISTOR
FOR CHUA'S CIRCUIT**

by

José M. Cruz and Leon O. Chua

Memorandum No. UCB/ERL M92/16

20 February 1992

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

TITLE PAGE

A CMOS IC Nonlinear Resistor for Chua's Circuit *

José M. Cruz and Leon O. Chua[†]

Abstract — The first monolithic realization of the nonlinear element in Chua's circuit, now generally called Chua's diode[1], is reported. The element has been fabricated using a CMOS integrated circuit technology. It can be used as the basic nonlinear component for the experimental synthesis of a broad class of circuits, including Cellular Neural Networks, which exhibits an extremely rich variety of bifurcation, chaotic, and nonlinear wave phenomena.

1 Introduction

Bifurcation and chaotic phenomena can potentially appear in many nonlinear electronic circuits and most practical circuits are nonlinear to some degree. For investigating complex dynamic phenomena it is advisable to use simple circuit prototypes in which bifurcation and chaotic behavior can be analyzed, simulated and easily verified. Chua's circuit, shown in Figure 1(a), is the simplest autonomous circuit which exhibits bifurcation and chaotic phenomena. It contains the minimum number of linear storage elements (three) and a single *one-port* nonlinear resistor (Chua's diode[1]). The circuit has been the focus of extensive studies, with more than fifty papers published since it was discovered in 1984 [3]. It is one of the very few physical systems in which a formal proof of the existence of chaos has been accomplished [4] and in which the theoretical, simulation and experimental results match precisely. These factors have made Chua's circuit a standard paradigm for studying chaotic phenomena.

The voltage-controlled driving-point characteristic of Chua's diode is shown in Figure 1(b). For voltage signals less than E_1 in absolute value the characteristic has a linear segment with negative slope m_2 . For absolute voltages larger than the breakpoint E_1 the characteristic has two linear segments of negative slope m_1 , with $|m_1| < |m_2|$. The

*This work is supported in part by a Fulbright/MEC Fellowship, by the Semiconductor Research Corporation, and by the Office of Naval Research under Grant N00014-89-J-1402

[†]The authors are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA.

piecewise-linear behavior is valid in the nominal range $(-E_2, E_2)$ in which the diode is normally operated. For voltages outside this range the slope of the characteristic increases monotonically ultimately becoming positive. For large absolute voltages the characteristic lies in the first and third quadrants of the $I - V$ plane.

Until now, Chua's diode has not been available as an off-the-shelf component; but has been synthesized using multiple discrete components, like resistors, op amps, diodes, etc. (see [5] for the first implementation and [1] for a complete bibliography).

In this paper we present the first *monolithic* implementation of Chua's diode using an integrated circuit (IC) device. This device will facilitate the construction not only of Chua's circuit, but of an entire class of circuits based on the same nonlinear element, and exhibiting complex dynamical behavior.

The paper is structured as follows. In section 2 we present the experimental driving-point characteristic of Chua's diode based on the new IC device. We use the device to build a Chua's circuit, and we show the experimental bifurcation and chaotic phenomena obtained. In section 3 we give simulated static and dynamic characteristics of the device. We give a numerical validation of the existence of the Double Scroll chaotic attractor in Chua's circuit when using the new device, and we compare these results with those obtained using an idealized piecewise-linear model of the diode. In section 4 we describe the internal structure of the device and its design in a $2\mu\text{m}$ CMOS technology. Finally, in section 5 we outline our plans to mass produce this IC.

2 Experimental Performance

Figure 2 shows a diagram of Chua's diode integrated circuit implementation. It consists of the monolithic IC device powered by two floating batteries, with $V_{CC} = 5\text{V}$. The two-terminal Chua's diode can be used in any floating configuration; only the differential voltage V_R across it is relevant.

The experimental results which we present in this paper are for an IC Chua's diode with a fixed driving-point characteristic. The parameters of this characteristic are given in Table I. The values for the slopes m_1 and m_2 and for the breakpoint E_1 have been chosen to provide robustness for the experimental reproduction of bifurcation and chaotic phenomena in Chua's circuit [1]. This IC device has the minimum number of possible external terminals—four, as is indicated in Figure 2.

Table I. DC specifications of Chua diode implementation

Parameter	Value	Unit
m_1	-0.41	mA/V
m_2	-0.78	mA/V
E_1	0.7	V
E_2	2.0	V
E_3	5.0	V

The device can provide an output power of up to 2.2mW in the nominal operating range, and up to 5.5mW if overdriven. The average total power drawn from the batteries is 28mW. This is less than the typical quiescent supply power of a standard 741 op amp.

In addition to the fixed integrated circuit device, and using a similar internal structure, we have also designed and fabricated five programmable devices. They have additional external terminals which can be used to adjust independently the slopes m_1 and m_2 to $\pm 50\%$ of the nominal values of Table I.

2.1 Driving-point characteristic

Figure 3(a) gives the experimental driving point characteristic of the diode in the nominal operating range. The breakpoints $-E_1$ and E_1 and the slopes m_1 and m_2 correspond to the nominal values given in Table I. The maximum relative variation of the current I_R with respect to the ideal piecewise-linear characteristic is 7%. This driving-point characteristic has been measured to be valid from DC up to frequencies of 100kHz.

Figure 3(b) gives the experimental driving-point characteristic of the diode for an extended range. The curve remains in the second and the fourth quadrants of the $I - V$ plane for differential voltages within the battery range $(-V_{CC}, +V_{CC})$. For larger absolute voltages the device acts as a passive resistor, as is expected by energy conservation.

2.2 Application to Chua's circuit: bifurcation sequence

The functionality of our Chua's diode IC device can be demonstrated by using it experimentally to build a circuit. Different set of values can be used for the linear elements as long as they give a dynamic range for V_R within the nominal operating range of the diode $(-E_2, E_2)$. If we also wish to center the frequency spectrum of Chua's circuit variables in the audio range a corresponding choice of component values is the following:

$C_1 \sim 10^{-8}\text{F}$, $C_2 \sim 10^{-7}\text{F}$, $L \sim 10^{-2}\text{H}$, and $R \sim 10^3\Omega$. In our case the experimentally measured values of the linear elements used are $C_1 = 11.3\text{nF}$, $C_2 = 162\text{nF}$, $L = 18.8\text{mH}$ and the linear resistance R is a variable potentiometer in the range 1–2k Ω .

With this experimental circuit we have reproduced the well-known bifurcation and chaotic phenomena of Chua's circuit. Figure 4 gives the bifurcation sequence obtained when the linear resistor R is decreased from 1.73k Ω to 1.62k Ω . It shows periodic behavior emerging from a stable equilibrium point, period two after a period doubling, a period four, a Rössler-type chaotic attractor and finally a Double Scroll attractor. After some point the Double Scroll disappears and a limit cycle associated with the external positive slope of the nonlinear element is observed.

3 Simulated Results

In this section we give the simulated results of the reported device. We use the circuits simulator Spice3e2 [6] considering all of the parasitic effects and using the transistor models provided by the MOSIS [7] silicon foundry (Orbit).

These simulated numerical results demonstrate the existence of the Double Scroll attractor in Chua's circuit when using the new device. We compare these results with those obtained using an ideal model of Chua's diode. This ideal model has an exact piecewise-linear DC characteristic with the nominal parameters of Table I, and without any reactive limitation due to parasitics.

3.1 Driving-point characteristic

Figure 5(a) gives the simulated driving-point characteristic for V_R in the nominal operating range $(-E_2, E_2)$. The solid line represents the simulated characteristic of the actual device. The square dots represent the characteristic of an ideal piecewise-linear model

$$I_R = f_R(V_R) = m_1 V_R + \begin{cases} (m_2 - m_1)E_1 & V_R \geq E_1 \\ (m_2 - m_1)V_R & -E_1 < V_R < E_1 \\ -(m_2 - m_1)E_1 & V_R \leq -E_1 \end{cases} \quad (1)$$

using the m_1 , m_2 and E_1 values of Table I. The maximum deviation in the current for a given voltage occurs at $V_R = \pm E_1$. At both points the deviation in the current is 0.035mA, corresponding to a maximum relative error of 7%, which agrees with the experimental results of the previous section and with the analysis to be presented in subsequent sections. This deviation is symmetrical and like our experiments and simulations does not have an appreciable effect on the bifurcation phenomena or on

the shape of the attractors in Chua's circuit. The offset, however, can give rise to an asymmetrical characteristic and produce a Double Scroll attractor with lobes of different sizes. The actual diode has a small systematic offset, imperceptible in the plot, of 4mV (which corresponds to a $I_R = 0.003\text{mA}$ for $V_R = 0\text{V}$). This offset is of the same order of magnitude as the expected random offset due to transistor mismatches in our technological process. The measured $I_R - V_R$ diode characteristic begins to exhibit high frequency distortion and hysteresis only at frequencies above 100kHz.

Figure 5(b) shows that simulated characteristic for the extended range for the actual device. The shape of the curve outside the range $(-E_2, E_2)$ is not relevant for the operation of Chua's circuit, and does not need to be defined in the ideal model. The shape coincides exactly with the experimental characteristic of Figure 3(b) and I_R crosses through zero at $V_R = \pm E_3 = \pm V_{CC}$. The effects which cause this characteristic are discussed in Appendix III.

3.2 Application to Chua's circuit

To further validate the suitability of the device we have compared the dynamic behavior of Chua's circuit using the fabricated diode with that obtained by using an idealized model of it. As an example we show the results for the Double Scroll chaotic attractor in Chua's circuit. Figure 6 shows the transient response obtained with Spice3e2 by using the initial condition $V_{C_1} = 0.1$ and $V_{C_2} = 0$. A long trajectory in the $V_{C_1} - V_{C_2} - I_L$ three-dimensional space is used to represent the shape of the strange attractor. Figure 7 (a), (b) and (c) shows the projections of the strange attractor obtained by using the new IC device with all the parasitics. Figures 7 (d), (e) and (f) show projections of the strange attractor obtained by using an idealized piecewise-linear model of the diode with no reactive limitation at all. Essentially identical attractors are obtained in each case.

4 Circuit Design

In this section we describe the actual design procedure for the four-terminal device. We first present the internal structure of the device and outline the design considerations that have been taken into account for an implementation with a $2\mu\text{m}$ p-well double-poly double-metal CMOS technology. Then we discuss limitations and possible improvements. We conclude by comparing this implementation with others which have been proposed.

The device is based on only two Operational Transconductance Amplifiers (OTAs),

as indicated in Figure 8 (a). This implementation, unlike previous ones, do not require additional elements like resistances or diodes, which are not appropriate for CMOS VLSI implementation. The problem is reduced to the design of two adequate transconductance amplifiers. The intrinsic nonlinear behavior of one of these amplifiers is used to generate the nonlinearity of the driving-point characteristic. This enables us to obtain high frequency responses using a small silicon area [9]. These transconductance amplifiers, unlike standard op amps, have only one stage, do not require internal compensation [10] and the amplifier gains can be controlled externally, if desired, permitting programmability.

The driving-point characteristic given in (1) is obtained by using two amplifiers exhibiting transconductance characteristics given ideally by

$$f_A(V_R) = \begin{cases} m_A E_1 & V_R \geq E_1 \\ m_A V_R & -E_1 < V_R < E_1 \\ -m_A E_1 & V_R \leq -E_1 \end{cases} \quad (2)$$

$$f_B(V_R) = m_B V_R \quad (3)$$

The piecewise-linear characteristic f_A corresponds to OTA A and the linear characteristic f_B to OTA B. If the the open loop output resistance of the OTAs are large enough (see Appendix I for requirements) the new parameters m_A and m_B should be set to

$$\begin{aligned} m_A &= m_1 - m_2 = -0.41 \text{mA/V} + 0.78 \text{mA/V} = 0.37 \text{mA/V} \\ m_B &= -m_1 = 0.41 \text{mA/V} \end{aligned} \quad (4)$$

In our design we try to obtain transfer characteristics for the amplifiers which are close to the ideal models of equations (2) and (3) and to minimize the effects of parasitic dynamics.

We have based the design on a simple input differential pair structure as it gives the maximum effective frequency response and minimal input noise. To minimize the offset and increase the output swing we use a symmetrical configuration with three current mirrors. These current mirrors contain cascode devices to increase the output resistance of the amplifiers in the nominal range of operation.

The complete schematic of the circuit is shown in Figure 9. A large signal analysis of this circuit is performed in Appendix II. The resulting driving-point characteristic

is given by

$$I_R = f(V_R) = -m_B V_R \sqrt{1 - \left(\frac{V_R}{2\sigma}\right)^2} - \begin{cases} m_A E_1 & V_R \geq \sqrt{2} E_1 \\ m_A V_R \sqrt{1 - \left(\frac{V_R}{2E_1}\right)^2} & -\sqrt{2} E_1 < V_R < \sqrt{2} E_1 \\ -m_A E_1 & V_R \leq -\sqrt{2} E_1 \end{cases} \quad (5)$$

The first term is due to OTA B and the second to OTA A. m_A and m_B are the small-signal transconductances of the amplifiers at the origin; they are set to the ideal values given in (4). The new parameter σ has been set to 2.4, providing a quasilinear behavior of OTA B in the nominal range. Figures 8 (b) and (c) give a plot with the current contribution of each amplifier in the nominal range. The limit current of OTA A is the same than in the ideal case ($\pm m_A E_1$), but is not reached until $|V_R| = \sqrt{2} E_1$. At the voltages that we define as breakpoints ($\pm E_1$) the output current of OTA A is $(1 - \sqrt{3/4}) I_A$. The maximum current difference between both the ideal function and the actual one (5) occur at the breakpoints. The maximum relative error is given approximately by

$$\frac{\delta I}{I} = \frac{m_1 - m_2}{-m_2} (1 - \sqrt{3/4}) = 6.2\% \quad (6)$$

which agrees with the experimental and simulated results obtained previously. Our experiments confirm that this small error has little noticeable effect on the bifurcation phenomena or on the shape of the attractors. This relative error could be reduced using linearization techniques of the differential pair to produce sharper corners at the expense of more circuitry, for example by modulating the value of the bias current [11]. However, the additional circuitry will inevitably increase the noise and reduce the frequency at which dynamic distortion (including hysteresis) begins to appear. These effects are detrimental to applications of the Chua diode.

The technological data for the process in which this device has been integrated are summarized in Table II. Using equations (13), (14) and (17) (see Appendix III) we obtain the main design equations for calculating the input transistor ratio sizes and bias currents:

$$\begin{aligned} \frac{W_A}{L_A} &= \frac{1}{\mu_n C_{ox}} \frac{m_A}{E_1} \\ \frac{W_B}{L_B} &= \frac{1}{\mu_n C_{ox}} \frac{m_B}{\sigma} \\ I_A &= m_A E_1 \\ I_B &= m_B \sigma \end{aligned} \quad (7)$$

Additional design equations for transistor sizing are given by output swing requirements and to obtain enough headroom for the current sources. These equations are derived from large signal conditions for maintaining all the transistors out of triode mode. For the final sizing we use computer simulations to consider corrections for bulk effect and channel length modulations [8].

Table II. Technological Data

Parameter	N-channel	P-channel	Unit
V_{th}	1.0	0.8	V
μC_{ox}	47	23	$\mu A/V^2$
γ	1.06	0.45	\sqrt{V}
ΔL	0.54	0.42	μm
ΔW	0.07	0.17	μm

Table III gives the drawn dimensions for the complete schematic shown in Figure 9. For the differential pair input transistors we have used a relatively large area to reduce the flicker noise. Their values are $W_A/L_A = 2 \times 30/6$ and $W_B/L_B = 2 \times 15/6$. For the current mirrors we have used unity current gain to maximize their frequency response. The W/L ratios of the current mirror transistors are as large as 100 in the case of OTA B. Throughout we have used transistor lengths greater than $4\mu m$ to reduce mismatch and flicker noise. We only use minimum length dimensions in the cascode devices as they do not contribute to the offset and noise. In the fixed IC device the bias currents are $I_A = 0.235mA$ and $I_B = 1.00mA$. They are generated by the bias circuitry shown at the left of the schematic. The ratio m_2/m_1 is to first order independent of variations in the process parameters μC_{ox} and V_{th} . The absolute values of m_2 and m_1 depend on these parameters but can, if desired, be compensated by simply adjusting the power supply voltages of the device. The larger the power supply voltage the more negative will be the slopes m_1 and m_2 , maintaining the ratio m_2/m_1 constant.

Table III. Mask Device Dimensions

Device	W (μm)	L (μm)
$T_{101A}, T_{101B}, T_{102A}, T_{102B}$	30	6
$T_{103A}, T_{104A}, T_{105A}, T_{106A}, T_{107A}, T_{108A}$	280	4
$T_{103B}, T_{104B}, T_{105B}, T_{106B}, T_{107B}, T_{108B}$	280	2
T_{109A}	100	6
T_{109B}	100	2
$T_{201A}, T_{201B}, T_{202A}, T_{202B}$	15	6
$T_{203A}, T_{204A}, T_{205A}, T_{206A}, T_{207A}, T_{208A}$	400	4
$T_{203B}, T_{204B}, T_{205B}, T_{206B}, T_{207B}, T_{208B}$	400	2
T_{209A}	476	6
T_{301A}	50	10
T_{301B}	100	10
T_{302A}, T_{302B}	20	10

Figure 10 shows the layout of the entire chip. In the same die we have integrated six IC devices. An IC device with four external terminals and providing a fixed driving point characteristic for Chua's diode (upper right part of the layout diagram) and five programmable IC devices. We have used the same orientation for all the transistors to reduce mismatch. The input differential pairs have been laid out in a common centroid configuration to minimize input offset due to threshold voltage variations. Each IC device occupies an area of about 0.5mm^2 , and the total die size including the bonding pads and protection circuitry is $2.25 \times 2.25\text{mm}$. The chip has been encapsulated in a 40-pin DIP package.

We use protection diodes at the pads. They guard against large currents going through the device when it is overdriven by voltages outside the battery range. A p-n diode with a small series resistance is placed between terminal 1 and 3 and another between 4 and 1.

In Appendix III we analyze all the effects which contribute to the Chua's diode characteristic outside the nominal operating range.

In the programmable devices the currents I_A and I_B are controlled by additional external terminals. The control of these currents gives two degrees of freedom in the three dimensional space formed by m_1 , m_2 and E_1 , which are the main parameters of the device. The slope m_1 is proportional to $\sqrt{I_B}$. The breakpoint E_1 is proportional to $\sqrt{I_A}$, and the slope m_2 depends on a linear combination of $\sqrt{I_B}$ and $\sqrt{I_A}$. The proportionality factors are given in Appendix IV.

These IC nonlinear devices can be operated without dynamic distortion at higher frequencies than previous implementations. The hysteresis phenomena at frequencies above 100kHz is caused mainly by a delay of about 5 nsec when the current mirrors of OTA A switch off at the breakpoint E_1 crossing. An improvement can be achieved by using common current mirrors for both OTAs. In this case all of the current mirror transistors are always in saturation mode and only a transistor of the input differential pair of OTA A can switch off.

In the fixed IC device the number of external terminals is four, the minimum possible. However it can be designed in such way that the device requires only one battery of value $2V_{CC}$ instead of two batteries of value V_{CC} . This is simply achieved with additional internal circuitry generating a low impedance intermediate voltage at node 2 from the voltages at terminals 3 and 4, which are then connected to the single battery.

5 Conclusions

In this paper we have presented an IC implementation of the nonlinear resistor in Chua's Circuit. It is integrated in a $2\mu\text{m}$ CMOS process. This is the first monolithic implementation of such a resistor, and eliminates the need for several discrete components. The small silicon area required (less than a square millimeter) makes the implementation cheap. It also opens the possibility of integrating in a single chip large Cellular Neural Networks made of coupled Chua's Circuits to reproduce wave propagation phenomena [12] and spatio-temporal chaos.

We plan to make the device widely available as the first off-the-shelf Chua's diode. Presently we are integrating a version of the circuit powered using standard commercial batteries. Two Chua's diodes will be provided in each 8 pin DIP ceramic package. We hope that this chip will make it easier for researchers to build and explore simple circuits exhibiting a wide spectrum of complex dynamic phenomena.

Acknowledgment

The authors would like to thank Dr. R. Broderson for providing the silicon integration resources (MOSIS), Dr. M. P. Kennedy for useful discussions, and K. S. Halle for building a demonstration circuit using the new IC device.

Appendix I: Effect of finite output resistance.

To account for the finite value of the output resistance of the amplifiers equation

(4), should be replaced by the following

$$m_1 = \frac{1 - m_B r_{oB}}{r_{oB}} + \frac{1}{r_{oB}} + \frac{1}{r_{oA}} \quad (8)$$

$$m_2 = \frac{1 - m_A r_{oA}}{r_{oA}} + \frac{1 - m_B r_{oB}}{r_{oB}} + \frac{1}{r_{oB}} + \frac{1}{r_{oA}} \quad (9)$$

where r_{oA} and r_{oB} are the small signal output resistances of OTA A and OTA B. This can introduce nonlinear distortion due to the fact that r_{oA} and r_{oB} are in general not constant but depend nonlinearly on the output current (and on the output voltage itself when in feedback configuration). To prevent this nonlinear phenomenon from affecting the driving-point characteristic in the nominal range we have designed the amplifier such that $r_{oA}(V_R), r_{oB}(V_R) \gg 1/m_1, 1/m_2$ for $V_R \in (-E_2, E_2)$. In this case

$$m_1 \approx -m_B \quad (10)$$

$$m_2 \approx -m_A - m_B$$

Appendix II: Design equations.

In the nominal range, all the transistors are in saturation or in cut-off mode. For a MOS transistor in saturation we consider the following formula which neglects the bulk effect and channel modulation effects:

$$I = \frac{\mu C_{ox} W_A}{2 L_A} (V_{GS} - V_{th})^2 \quad (11)$$

The differential current of the differential pair of OTA A as function of the input differential voltage V_R and the bias current I_A is then given by

$$g_A(V_R) = \begin{cases} I_A & V_R \geq \sqrt{\frac{2I_A}{\mu C_{ox} \frac{W_A}{L_A}}} \\ \sqrt{\mu C_{ox} \frac{W_A}{L_A}} I_A V_R \sqrt{1 - \mu C_{ox} \frac{W_A}{L_A} \frac{1}{4I_A} V_R^2} & \sqrt{\frac{2I_A}{\mu C_{ox} \frac{W_A}{L_A}}} < V_R < \sqrt{\frac{2I_A}{\mu C_{ox} \frac{W_A}{L_A}}} \\ -I_A & V_R \leq -\sqrt{\frac{2I_A}{\mu C_{ox} \frac{W_A}{L_A}}} \end{cases} \quad (12)$$

The slope of the function at the origin is denoted as in the ideal piecewise-linear

model by m_A and is given by

$$m_A = g'_A(0) = \sqrt{\mu C_{ox} \frac{W_A}{L_A} I_A} \quad (13)$$

The maximum and minimum value of ΔI are $\pm I_A$. As with the ideal model, we define the breakpoint E_1 as

$$E_1 = \frac{I_A}{m_A} = \sqrt{\frac{I_A}{\mu C_{ox} \frac{W_A}{L_A}}} \quad (14)$$

Equation (12) is rewritten as

$$g_A(V_R) = \begin{cases} m_A E_1 & V_R \geq \sqrt{2} E_1 \\ m_A V_R \sqrt{1 - \left(\frac{V_R}{\sqrt{2} E_1}\right)^2} & -\sqrt{2} E_1 < V_R < \sqrt{2} E_1 \\ -m_A E_1 & V_R \leq -\sqrt{2} E_1 \end{cases} \quad (15)$$

The output current at the breakpoint is then given by

$$g_A(E_1) = I_A(1 - \sqrt{3/4}) \quad (16)$$

For OTA B the same equation (15) applies, but replacing the slope m_A and the breakpoint E_1 by

$$\begin{aligned} m_B &= \sqrt{\mu C_{ox} \frac{W_B}{L_B} I_B} \\ \sigma &= \frac{I_B}{m_B} = \sqrt{\frac{I_B}{\mu C_{ox} \frac{W_B}{L_B}}} \end{aligned} \quad (17)$$

Appendix III: Characteristic outside the nominal range.

Outside the nominal operating range the following effects occur:

First, the nonlinear distortion of amplifier B is appreciable for $|V_R| > E_2$. Gain compression causes the slope of Chua's diode characteristic to become less negative as $|V_R|$ increases. This effect is dominant in the range $|V_R| \in (2V, 3V)$

Second, for voltages near the power supply rails the output resistance of the OTAs drop dramatically as their output transistors enter in their triode region. The approximation in equation (10) is no longer valid.

Let us consider the case of large positive voltages V_R . For large input voltages the differential pair is switched off, and there is no current flowing through the lower current mirror. All of the output current of the OTA flows through the upper current mirror. However, as the output voltage increases the transistors enter the triode mode and the output current decreases to zero when $V_R = V_{CC}$. The slope of the curve at that point is given by

$$m_{o+} = f'_R(V_{CC}) = \sqrt{\mu_p C_{ox} \frac{W_{104A}}{L_{104A}} I_A} + \sqrt{\mu_p C_{ox} \frac{W_{204A}}{L_{204A}} I_B} \quad (18)$$

It can be related to m_1 and m_2 by using (10), (13) and (17):

$$m_{o+} = m_A \sqrt{\frac{\mu_p}{\mu_n} \frac{W_{104A}}{L_{104A}} \frac{W_A}{L_A}} + m_B \sqrt{\frac{\mu_p}{\mu_n} \frac{W_{204B}}{L_{204B}} \frac{W_B}{L_B}} = +1.87m_A + 3.16m_B \quad (19)$$

$$m_o = -1.29m_1 - 1.87m_2 = +1.99mA/V \quad (20)$$

Similarly for $V_R = -V_{CC}$ we obtain

$$m_{o-} = f'_R(-V_{CC}) = \sqrt{\mu_n C_{ox} \frac{W_{108A}}{L_{108A}} I_A} + \sqrt{\mu_n C_{ox} \frac{W_{208A}}{L_{208A}} I_B} \quad (21)$$

It can be related to m_1 and m_2 by:

$$m_{o-} = m_A \sqrt{\frac{W_{108A}}{L_{108A}} \frac{W_A}{L_A}} + m_B \sqrt{\frac{W_{208B}}{L_{208B}} \frac{W_B}{L_B}} = +2.64m_A + 4.47m_B \quad (22)$$

$$m_o = -1.83m_1 - 2.64m_2 = +2.81mA/V \quad (23)$$

Third, for V_R outside the supply voltages range the positive slope of the device increases even more as one of the protection diodes became forward biased causing a positive exponential component which depends on $|V_R - V_{CC}|$. For values $|V_R - V_{CC}|$ of about 0.8V, the very large positive slope becomes finally limited by the non-zero series resistance of the batteries.

Appendix IV: Control of programmable devices.

For the programmable devices the slopes and breakpoints can be adjusted by $\sqrt{I_A}$ and $\sqrt{I_B}$ in accordance with

$$\begin{aligned}m_1 &= K_1\sqrt{I_B} \\m_2 &= K_1\sqrt{I_B} + K_2\sqrt{I_A} \\E_1 &= K_3\sqrt{I_A}\end{aligned}\tag{24}$$

The proportionality constants are derived from equations (4), (13), (14) and (17). They are given by

$$\begin{aligned}K_1 &= \sqrt{\mu C_{ox} \frac{W_B}{L_B}} \\K_2 &= \sqrt{\mu C_{ox} \frac{W_A}{L_A}} \\K_3 &= \sqrt{\frac{1}{\mu C_{ox} \frac{W_A}{L_A}}}\end{aligned}\tag{25}$$

The valid range of operation of the amplifier also depends on the control currents. That range is maximum around the nominal values of Table I. For lower control current I_B the harmonic distortion of OTA B increases. For large control currents I_A or I_B the decrease in the output swing of the amplifiers limits the valid range of operation.

References

- [1] M. P. Kennedy. Robust op amp realization of Chua's circuit. *Frequenz*, (March-April), 1992.
- [2] L. O. Chua. The Genesis of Chua's Circuit. *Archiv für Elektronik und Übertragungstechnik*, to appear in 1992.
- [3] T. Matsumoto. A chaotic attractor from Chua's circuit. *IEEE Transactions on Circuits and Systems*, CAS-31(12):1055-1058, 1984.
- [4] L. O. Chua, M. Komuro, and T. Matsumoto. The Double Scroll family, parts I and II. *IEEE Transactions on Circuits and Systems*, CAS-33(11):1073-1118. 1986.

- [5] G. Q. Zhong and F. Ayrom. Experimental confirmation of chaos from Chua's circuit. *International Journal of Circuit Theory and Applications*, 13(11):93-98, 1985.
- [6] B. Johnson, T. Quarles, A.R. Newton, D. O. Pederson and A. Sangiovanni-Vincentelli. SPICE Version 3e User's Manual. *Dept EECS, University of California at Berkeley*, April 1991.
- [7] C. Tomovich (editor) MOSIS User Manual. Release 3.1 *The MOSIS Service*, University of Southern California, 1991.
- [8] D. A. Hodges, P. R. Gray, and R. B. Broderson. Potential of MOS technologies for analog integrated circuits. *IEEE Journal of Solid-State Circuits*, pp 285-293, June 1978.
- [9] J. M. Cruz and L. O. Chua. A CNN Chip for Connected Component Detection. *IEEE Transactions on Circuits and Systems*, vol. 38, No. 7. pp. 812-817, July 1991.
- [10] E. Sanchez-Sinencio, J. Ramirez-Angulo, B. Linares-Barranco and A. Rodriguez-Vazquez. Operational Transconductance Amplifier-Based Nonlinear Function Syntheses. *IEEE Journal of Solid-State Circuits*, vol. 24, pp 1576-1586, December 1989.
- [11] A. Nedungadi and T.R. Viswanathan. Design of Linear CMOS Transconductance Elements *IEEE Transactions on Circuits and Systems*, CAS-31:891-894, 1984.
- [12] V. Perez-Munuzuri, V. Perez-Villar and L. O. Chua. Propagation Failure in Linear Arrays of Chua's Circuits *to appear in International Journal of Bifurcation and Chaos*, Vol. 2, No. 2, 1992.

Figure Captions

Figure 1. (a) Chua's Circuit; (b) Driving-point characteristic of Chua Diode.

Figure 2. Nonlinear IC device: battery connection.

Figure 3. Experimental driving-point characteristic of Chua Diode implementation in: (a) the nominal range (Vertical scale: $250\mu\text{A}/\text{Division}$ Horizontal scale: $400\text{mV}/\text{Division}$); (b) extended range (Vertical scale: $500\mu\text{A}/\text{Division}$. Horizontal scale: $1\text{V}/\text{Division}$).

Figure 4. Experimental V_{C2} vs V_{C1} Lyssajous figures. Bifurcation sequence for decreasing values of the linear resistance: (a) $R = 1730\Omega$, period one; (b) $R = 1695\Omega$, period two; (c) $R = 1690\Omega$, period four; (d) $R = 1684\Omega$, A Rössler chaotic attractor; (e) $R = 1638\Omega$, A Rössler attractor just before colliding with its image; (f) $R = 1620\Omega$, Double Scroll attractor; Vertical scale: $100\text{mV}/\text{Division}$; Horizontal scale is $400\text{mV}/\text{Division}$.

Figure 5. (a) Driving-point characteristic in the nominal range. Simulation using the IC device (solid line) and using the ideal piecewise-linear model (square dots); (b) IC device simulation in the extended range ($-V_{CC}, V_{CC}$).

Figure 6. Chaos in Chua's circuit: Simulated time waveforms of the state variables $V_1(t)$, $V_2(t)$ and $I_L(t)$, using the new nonlinear IC device.

Figure 7. Spice simulations of Double Scroll attractor in Chua's circuit using the new IC device: (a) projection in the (V_{C2}, V_{C1}) plane; (b) projection in the (V_{C1}, I_L) plane; (c) projection in the (V_{C2}, I_L) plane. Simulations using an ideal piecewise-linear model: (d) projection in the (V_{C2}, V_{C1}) plane; (e) projection in the (V_{C1}, I_L) plane; (f) projection in the (V_{C2}, I_L) plane.

Figure 8. Nonlinear resistor OTA-based structure with simulated DC characteristic of each OTA in positive feedback configuration.

Figure 9. Transistor schematic.

Figure 10. IC Layout.

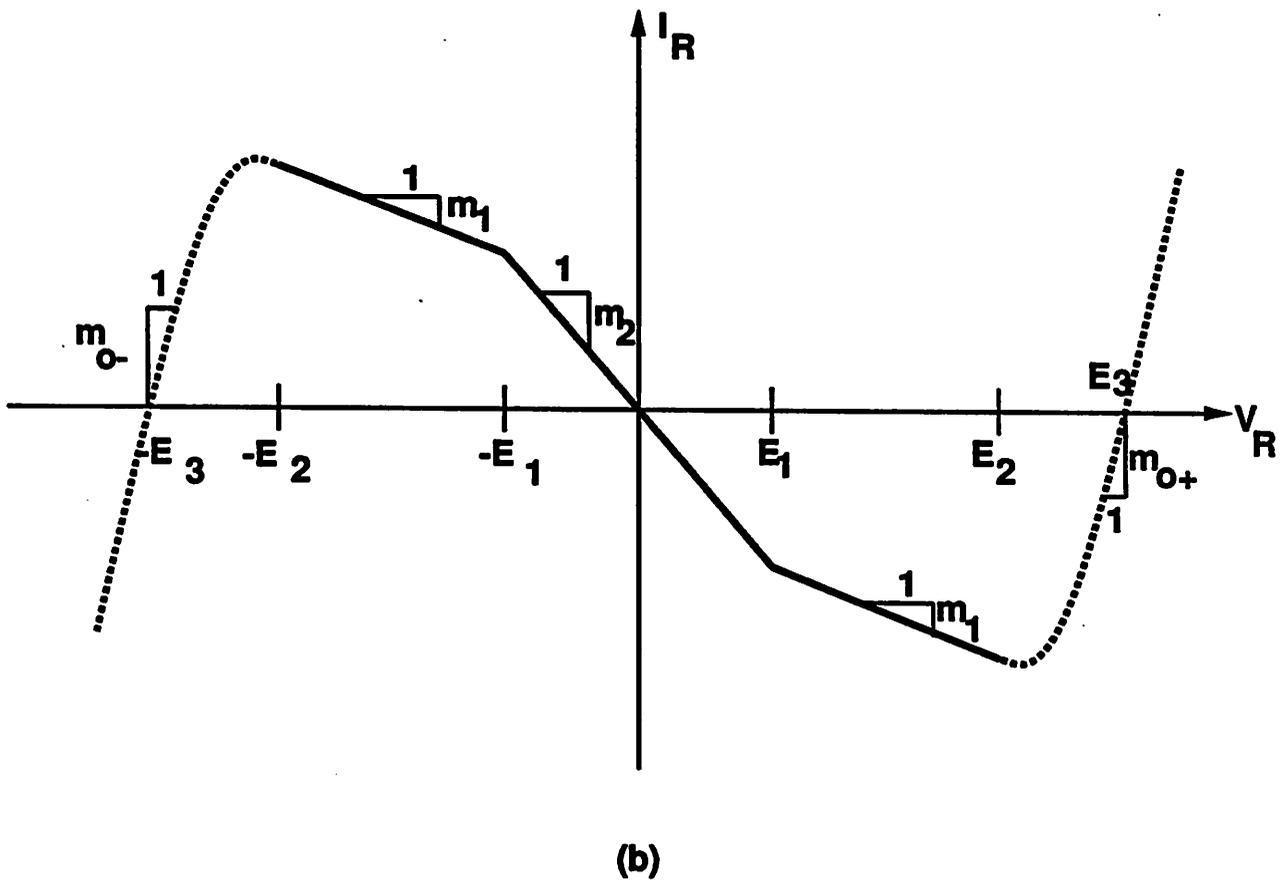
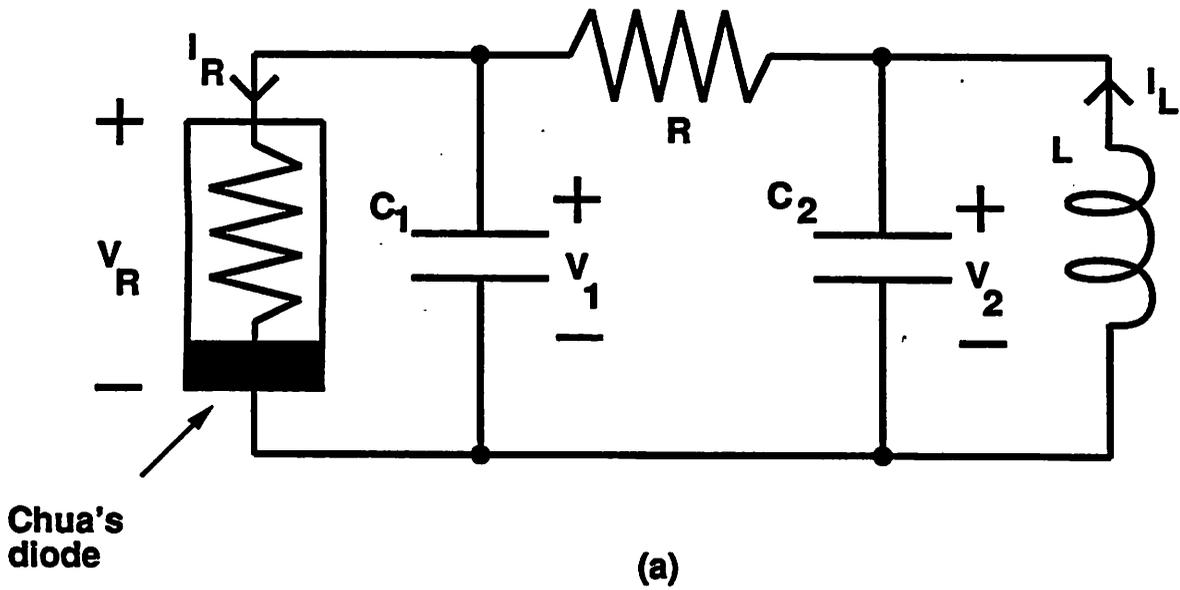


Figure 1

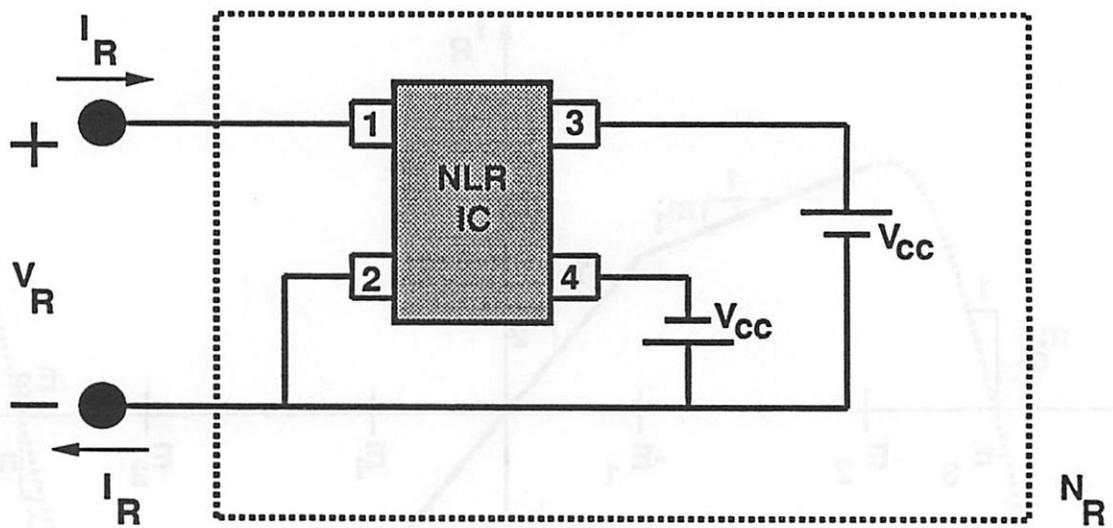
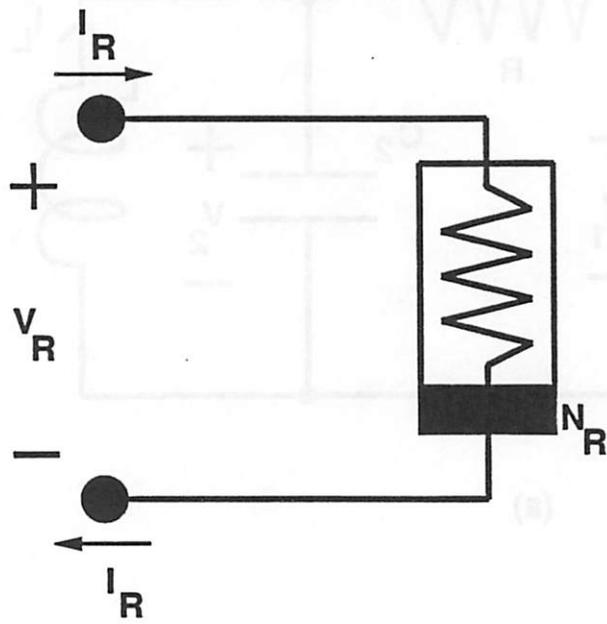
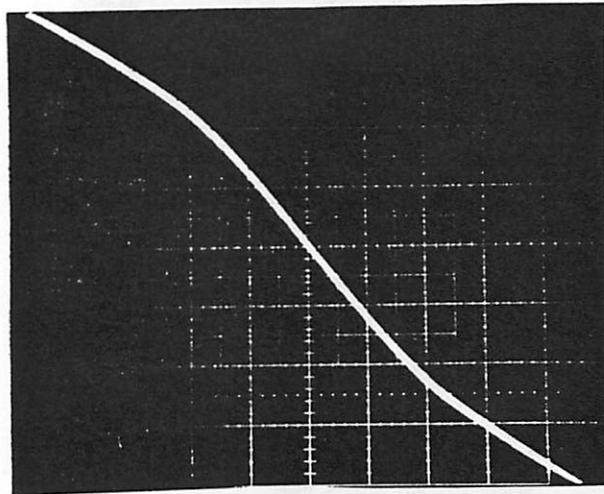
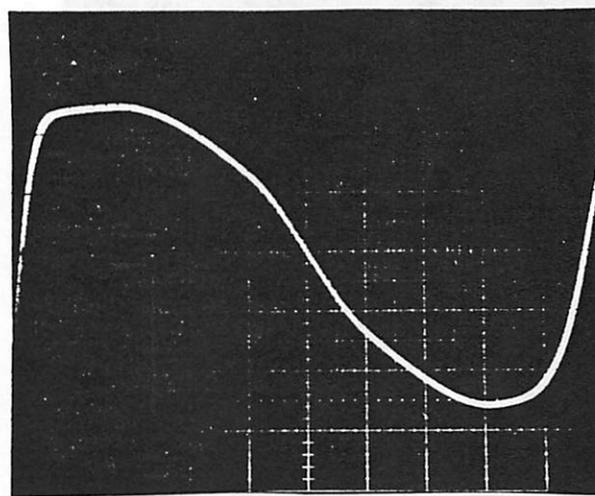


Figure 2



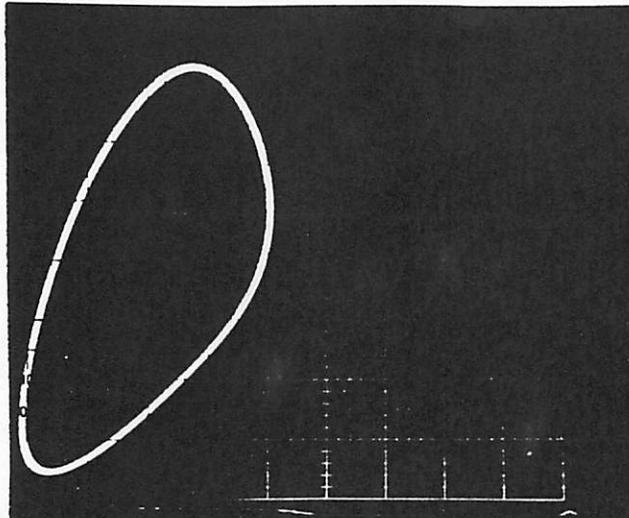
(a)



(b)

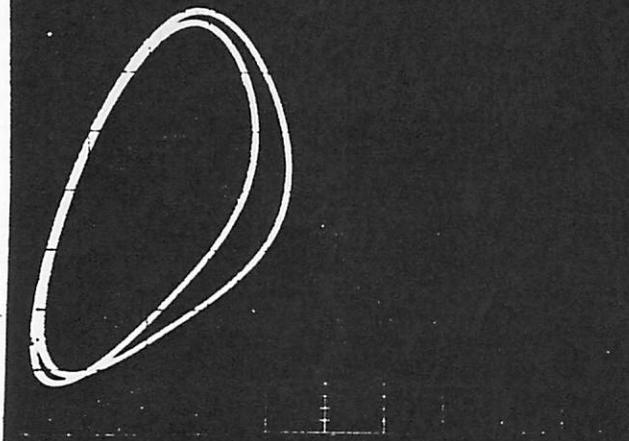
Figure 3

(a)



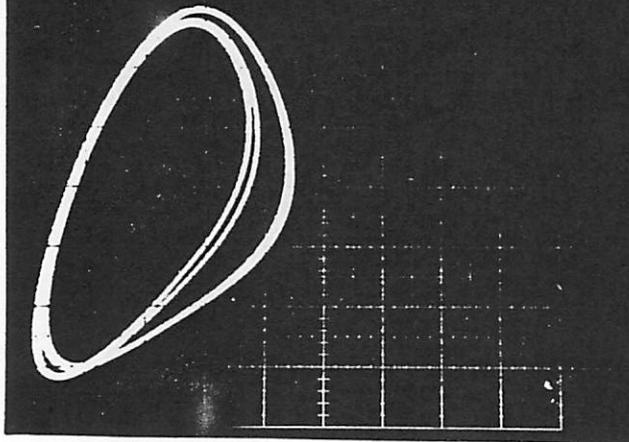
$R_1 = 1730 \text{ Ohm}$

(b)



$R_1 = 1695 \text{ Ohm}$

(c)



$R = 1690 \text{ Ohm}$

(d)

Figure 4

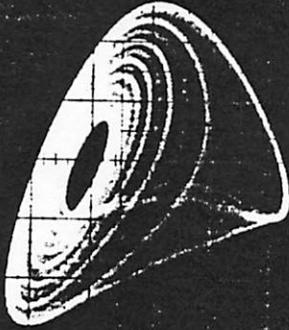
8.0000

(d)



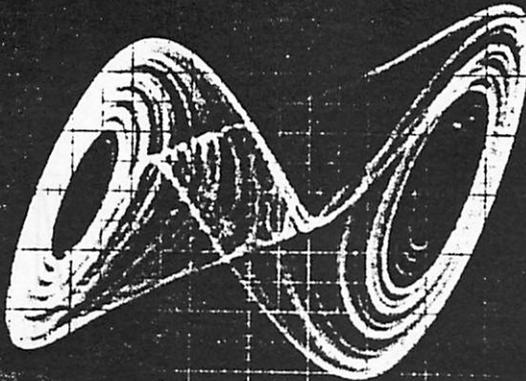
$R1 = 1684 \text{ Ohm}$

(e)



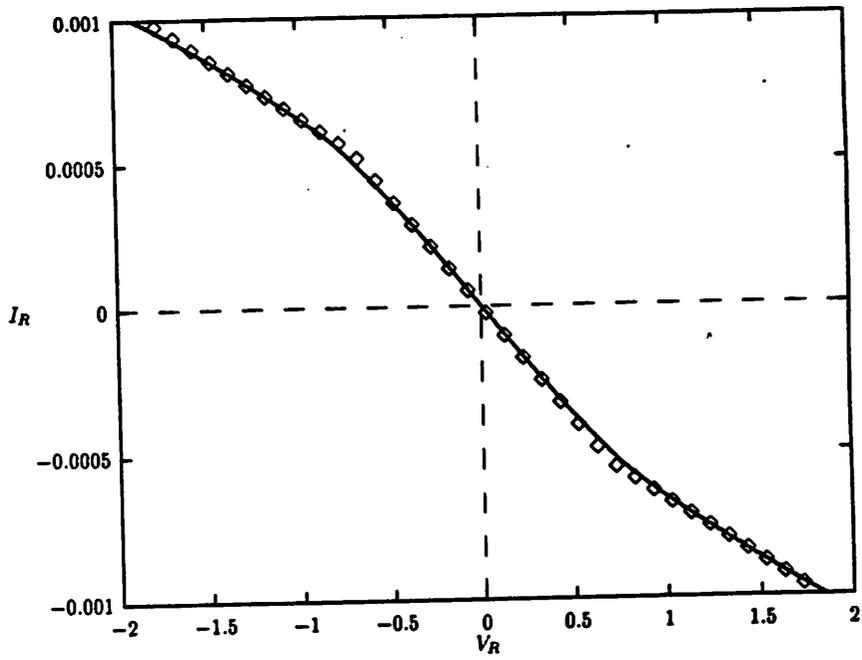
$R1 = 1638 \text{ Ohm}$

(f)

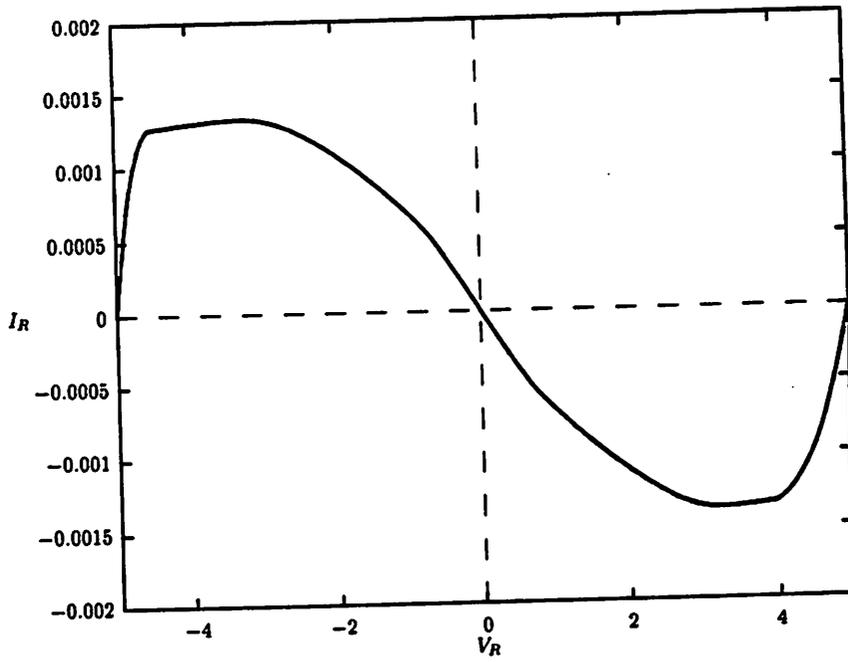


$R = 1620 \text{ Ohm}$

Figure 4



(a)



(b)

Figure 5

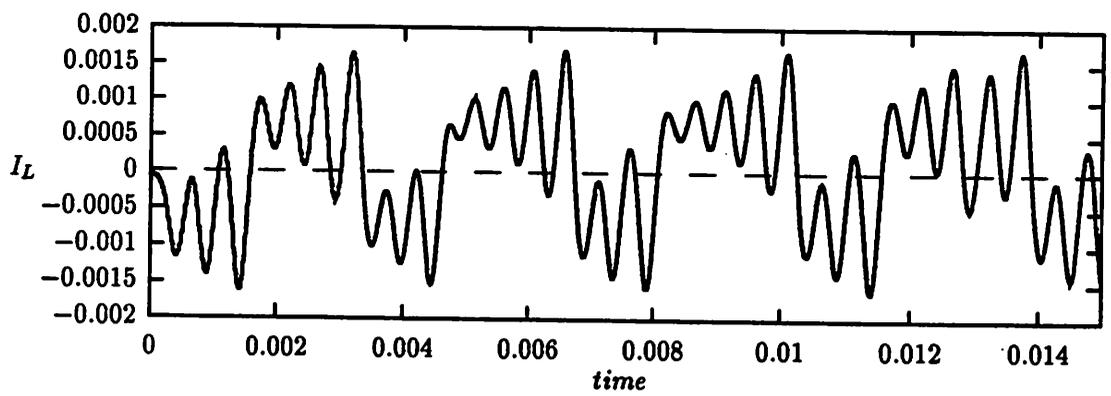
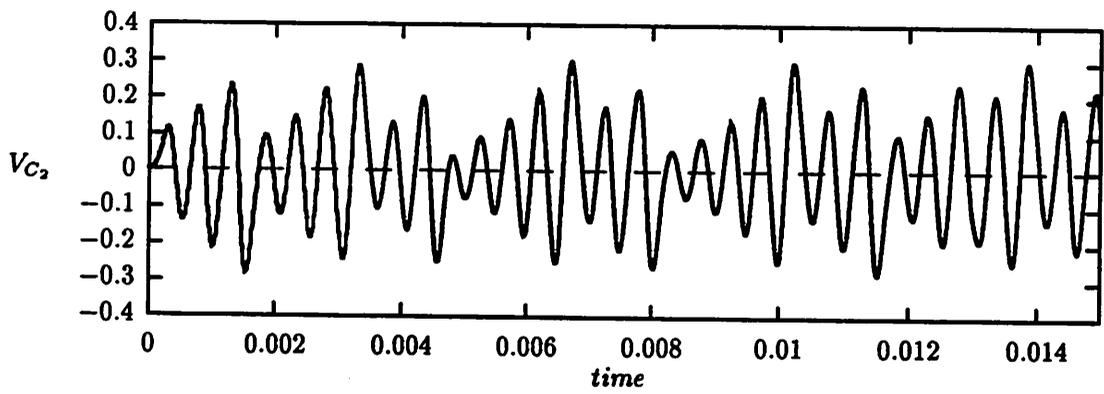
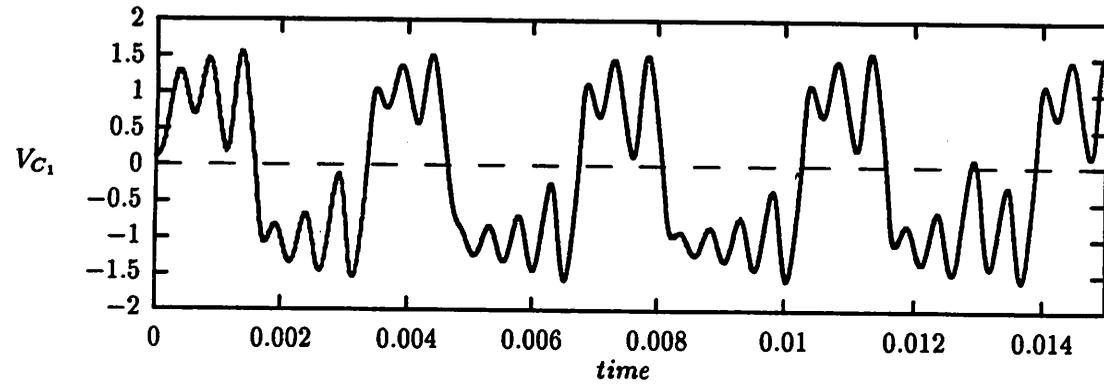
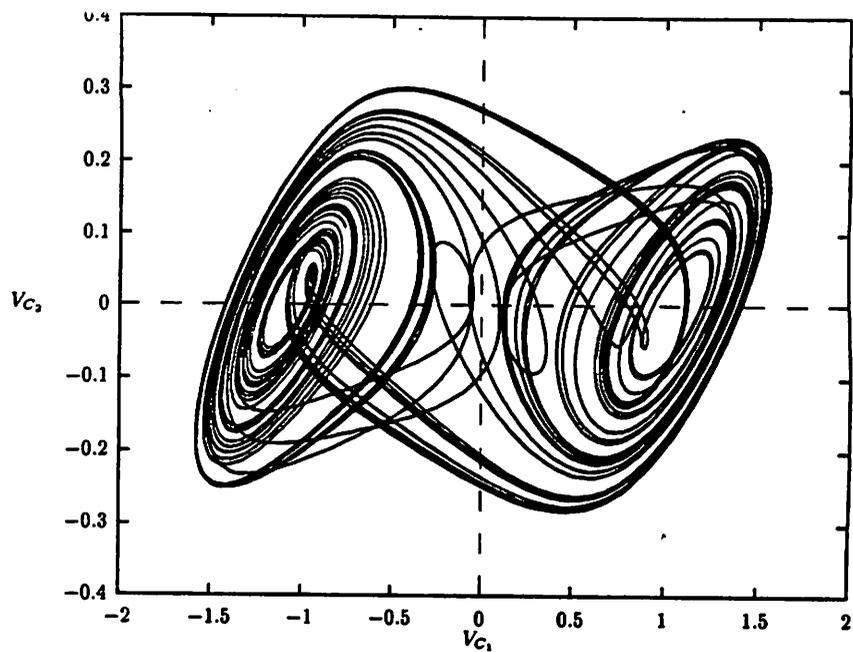
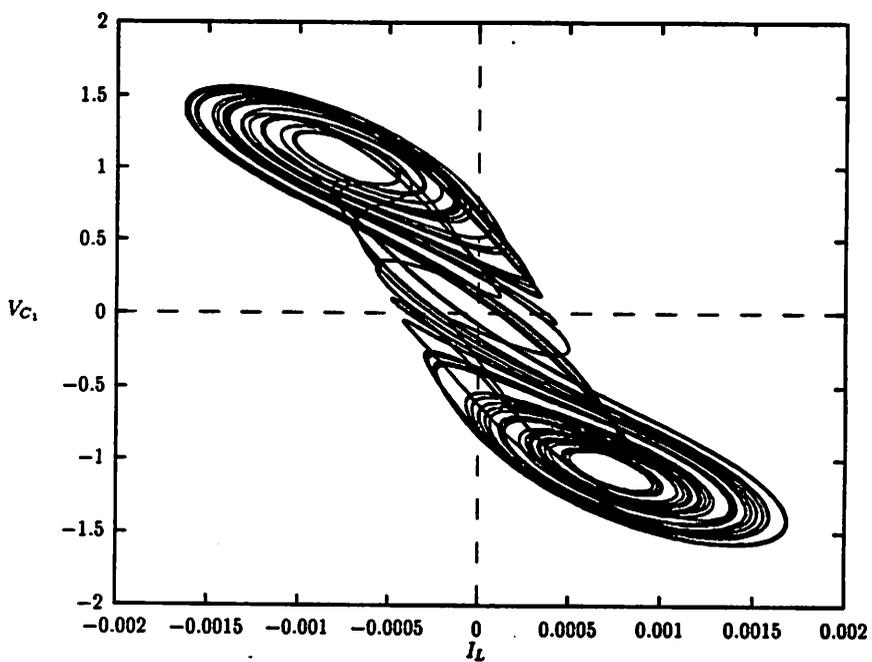


Figure 6

(a)



(b)



(c)

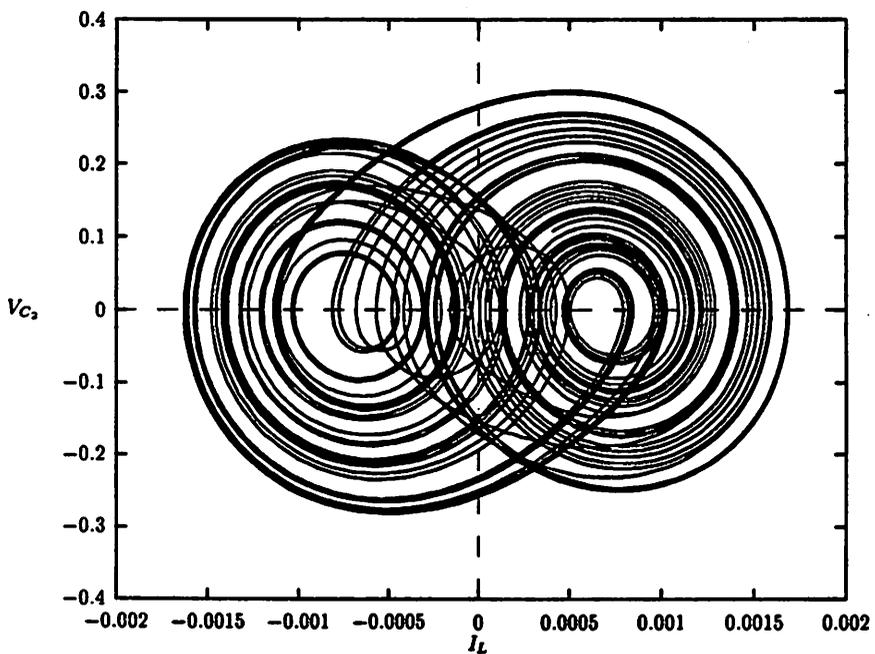
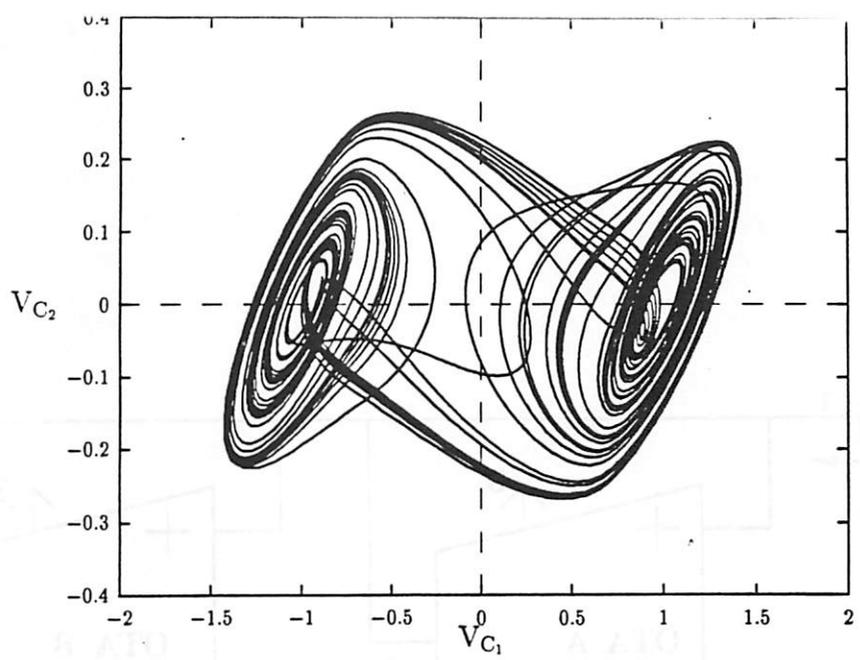
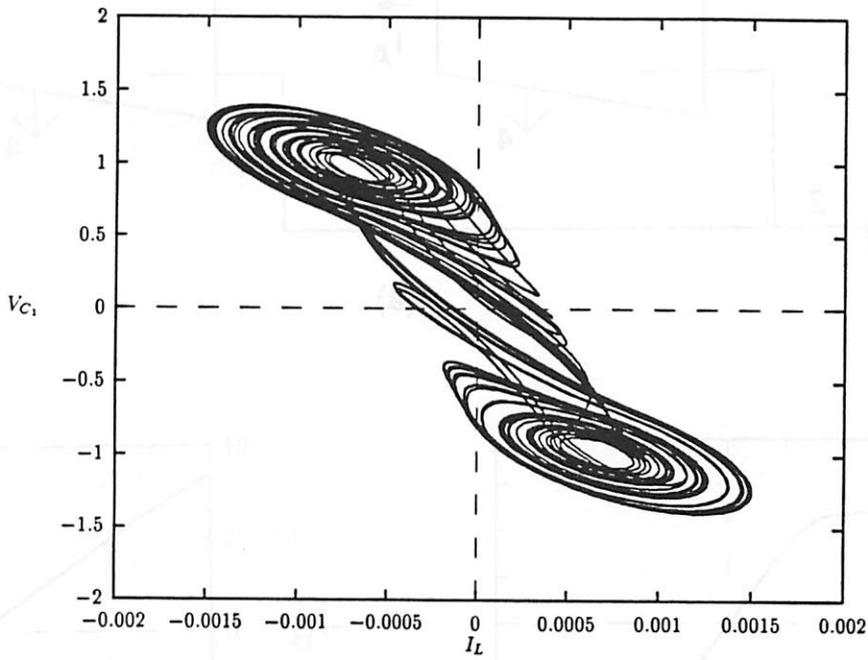


Figure 7

(d)



(e)



(f)

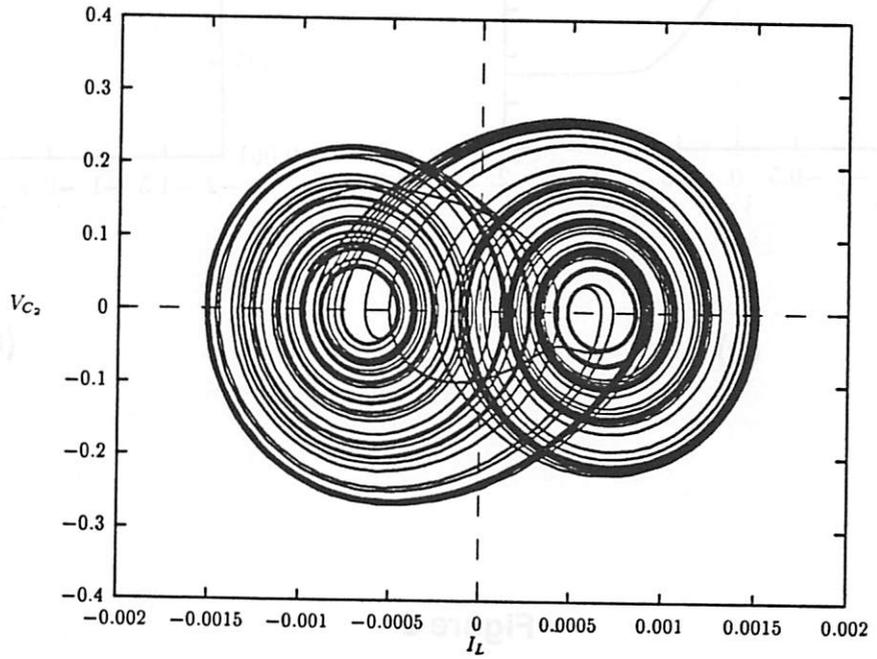
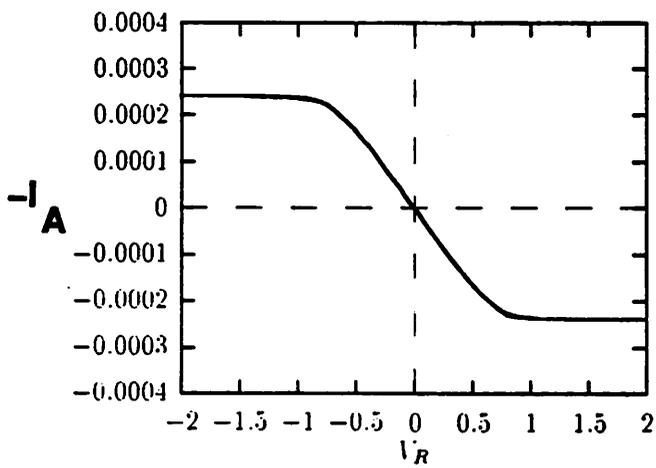
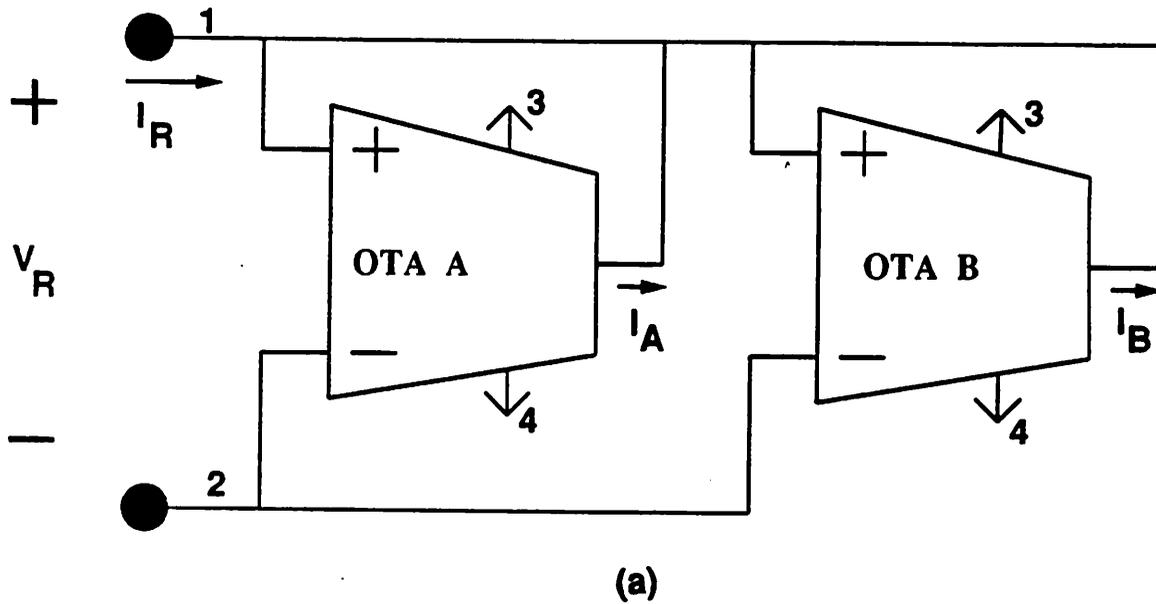
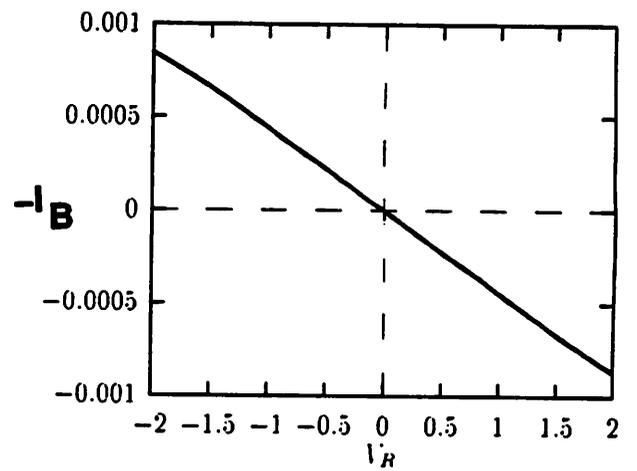


Figure 7



(b)



(c)

Figure 8

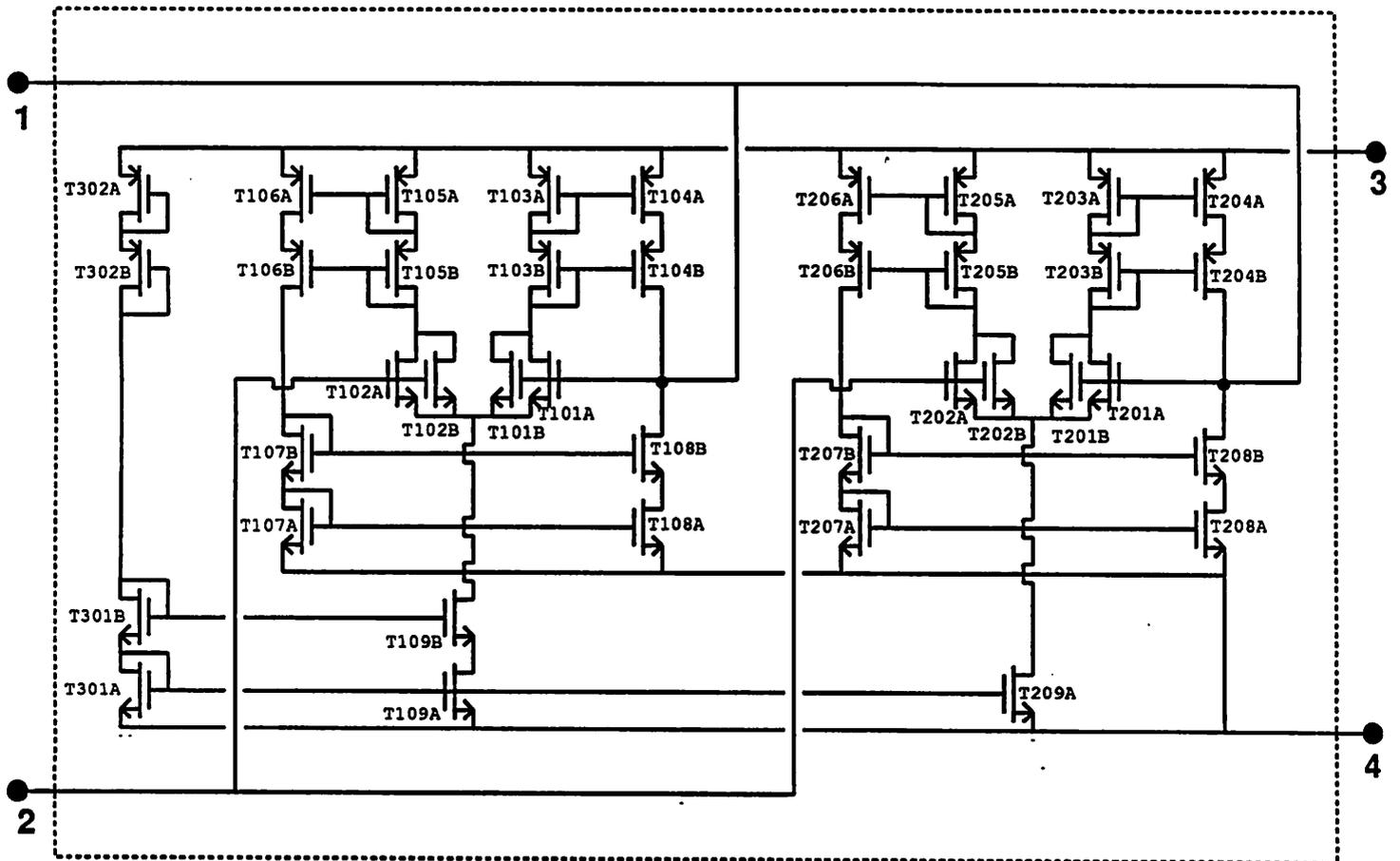


Figure 9

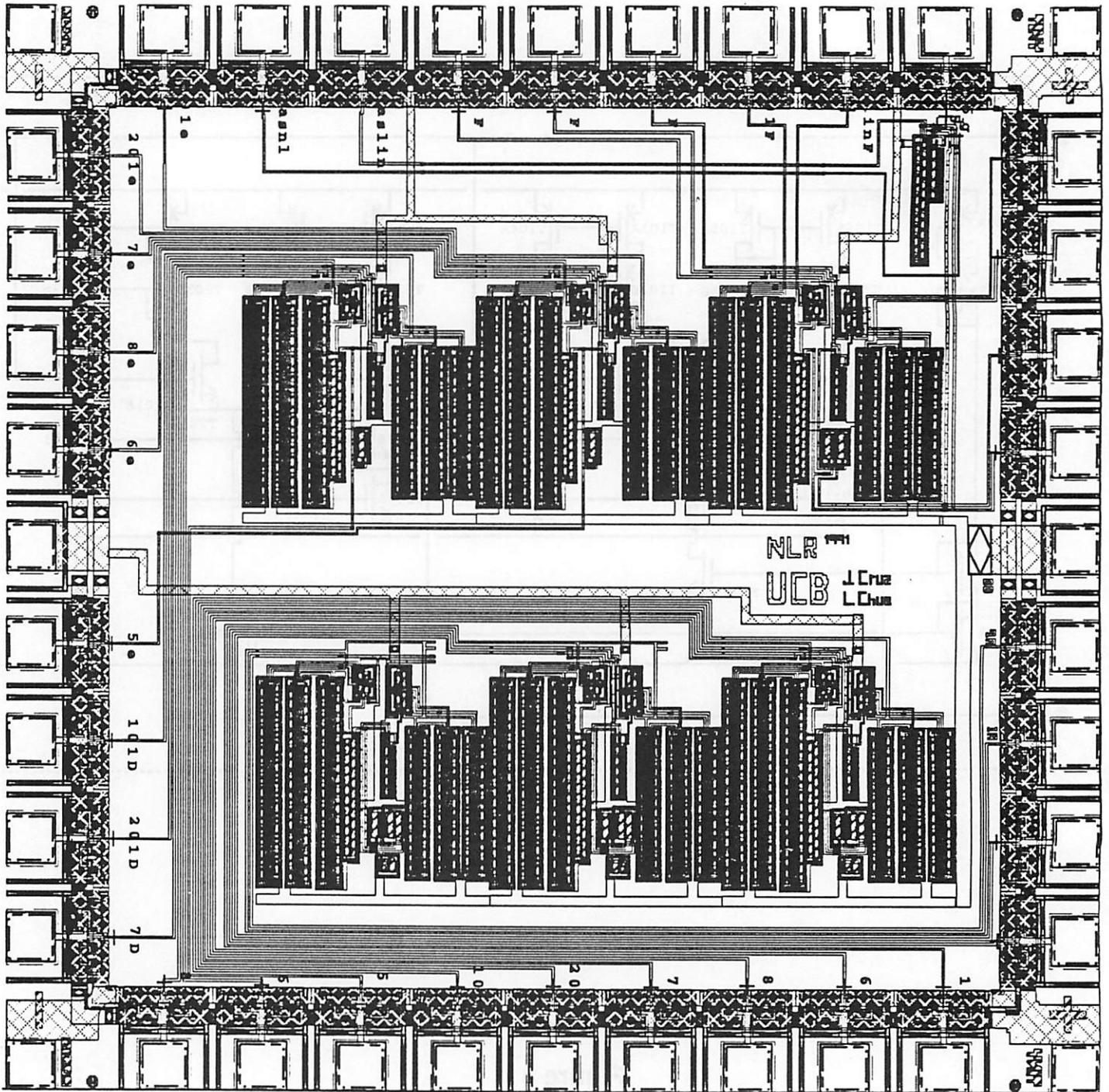


Figure 10