SPREAD SPECTRUM COMMUNICATION THROUGH MODULATION OF CHAOS

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Spread Spectrum Communication Through Modulation of Chaos

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Abstract

In this letter we demonstrate experimentally how Chua's circuits can be used to implement a secure communication system. This system is compared to another system proposed earlier. This system has the advantage of transmitting a spread spectrum signal and is also more secure in the sense that better parameter matching is required in order to recover the signal. Furthermore, there is less of a problem with loss of synchronization.

1 Introduction

Recently, there has been much interest in utilizing chaotic circuits to implement a secure communication system [Oppenheim *et al.*, 1992; Kocarev *et al.*, 1992]. In this paper we propose a new scheme to utilize Chua's circuit in constructing a secure communication system. The idea is to multiply the information signal by a broad-spectrum noise-like deterministic chaotic signal, which is then fed into the chaotic circuit. The output of the chaotic circuit is

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then transmitted. The chaotic signal is used as a "masking" signal. To eliminate the masking signal, very accurate knowledge of the parameters of the circuit is required to generate (or synchronize to) the same chaotic signal. In other words, by knowing what the parameters of the chaotic system are that generated the chaotic signal, we can recover the injected signal and thus the information signal. The parameters serve as the "encryption key". The security of the system comes from the high sensitivity of synchronization versus parameter changes.

In section 2 the system is described and its behavior analyzed. In section 3 some experimental data is presented on the physical implementation of the system. In section 4, the effects of parameter mismatch and channel noise are discussed. In section 5 this system is compared to the system proposed in [Kocarev *et al.*, 1992].

2 System Description

The basic system used for communication is given in Fig. 1.[1] It utilizes a Chua's circuit each for the transmitting system and for the receiving system.

In the transmitting system, a *current* signal $i_i(t)$ is injected into Chua's circuit, thereby modifying its dynamics. The *voltage* signal $v_t = v_1$ of this Chua's circuit is then transmitted. The receiving system then uses this transmitted voltage signal to obtain a detected *current* signal $i_d(t)$.

The information that we want to transmit is in the form of an *input* information "voltage" signal $v_s(t)$ which is then coded in the injected current signal $i_i(t)$ by an invertible coding function $c(\cdot)$: $i_i(t) = c(v_s(t))$. The detected current signal $i_d(t)$ is then decoded through $v_r(t) = c^{-1}(i_d(t))$. For proper operation of the system we want $v_r(t) \approx v_s(t)$. We also want to choose $c(\cdot)$ so that the injected signal $i_i(t)$ is such that the dynamics of the Chua's circuit and the transmitted signal v_t are still chaotic. To function as a secure communication system, we also want the transmitted signal v_t to look the same regardless of the information signal v_s that is being fed into the transmitting system.

The nonlinear resistors N_R and $\tilde{N}_R$ have the following three-segment piecewise-linear $v-i$

[1]This topology was discovered by the co-author Itoh, and its useful synchronization properties recognized by the authors.

characteristics, respectively:

$$i_R = f(v_R) = G_b v_R + \frac{1}{2}(G_a - G_b)\{|v_R + B_p| - |v_R - B_p|\} \quad (1)$$

$$\tilde{i}_R = \tilde{f}(\tilde{v}_R) = \tilde{G}_b \tilde{v}_R + \frac{1}{2}(\tilde{G}_a - \tilde{G}_b)\left\{\left|\tilde{v}_R + \tilde{B}_p\right| - \left|\tilde{v}_R - \tilde{B}_p\right|\right\} \quad (2)$$

The state equations are as follows:

$$C_1 \frac{dv_1}{dt} = \frac{1}{R}(v_2 - v_1) - f(v_1) + i_i(t) \quad (3)$$

$$C_2 \frac{dv_2}{dt} = \frac{1}{R}(v_1 - v_2) + i_3 \quad (4)$$

$$L \frac{di_3}{dt} = -v_2 \quad (5)$$

$$\tilde{C}_1 \frac{d\tilde{v}_1}{dt} = \frac{1}{\tilde{R}}(\tilde{v}_2 - \tilde{v}_1) - \tilde{f}(\tilde{v}_1) + i_d(t) \quad (6)$$

$$\tilde{C}_2 \frac{d\tilde{v}_2}{dt} = \frac{1}{\tilde{R}}(\tilde{v}_1 - \tilde{v}_2) + \tilde{i}_3 \quad (7)$$

$$\tilde{L} \frac{d\tilde{i}_3}{dt} = -\tilde{v}_2 \quad (8)$$

Let us assume that all the circuit components between the transmitting system and the receiving system are matched exactly, i.e. $\tilde{R} = R$, $\tilde{C}_1 = C_1$, etc. Because of the voltage buffer,[2] we have $\tilde{v}_1 = v_1$, and we can subtract equation (7) from equation (4) and subtract equation (8) from equation (5) to obtain:

$$C_2 \frac{d(v_2 - \tilde{v}_2)}{dt} = \frac{-1}{R}(v_2 - \tilde{v}_2) + (i_3 - \tilde{i}_3) \quad (9)$$

$$L \frac{d(i_3 - \tilde{i}_3)}{dt} = -(v_2 - \tilde{v}_2) \quad (10)$$

which are the state equations of a parallel RLC circuit with linear positive R, L and C. This implies that the origin is globally asymptotically stable[3] and $(v_2 - \tilde{v}_2) \to 0$ as $t \to \infty$.

Subtracting equation (6) from (3) we get

$$i_d(t) - i_i(t) = \frac{1}{R}(v_2 - \tilde{v}_2) \quad (11)$$

[2]A voltage buffer is a standard device where the voltage at the input is equal to the voltage at the output, while the current going into the device at the input terminal is zero. It acts here as a channel transmitting a *voltage* signal.

[3]this can also be seen by looking at the eigenvalues which all have negative real parts for $C_2, R, L > 0$.

i.e. $i_d(t) \to i_i(t)$ as $t \to \infty$ and thus $v_s(t) \to v_d(t)$ as $t \to \infty$.

The basic idea of this scheme is as follows: a current is injected into Chua's circuit which modifies the voltage across capacitor C_1. This voltage v_1 is then used as the forcing voltage on a second Chua's circuit across capacitor $\tilde{C}_1$. When the two Chua's circuit are matched, then if we view the subcircuit consisting of $\tilde{C}_2$, $\tilde{L}$, $\tilde{R}$ as a one-port, due to the passivity of this one-port, the current flowing into it must match, after some transient time, to the current flowing into the corresponding one-port of the first Chua's circuit. As the current through $\tilde{C}_1$ and $\tilde{N}_R$ is also determined by v_1, the current flowing into the second Chua's circuit must then be equal to the current injected into the first Chua's circuit.

3 Experimental Results

The system we implemented is shown in Fig. 2. We chose as the coding function $c(\cdot)$ the division operation, $c(v_s(t)) = v_s(t)/v_1(t)$.[4] The decoding function is then the *multiplication operation* $v_r = c(v_s(t)) \cdot v_1(t)$. Therefore, in our implementation, the system contains additionally a divider for modulating a chaotic signal with the input signal, and a multiplier for demodulating the received signal. All subcomponents are shown schematically in the appendix where they are discussed in more detail.

We use the following parameters in our experiments:[5]

$$\begin{array}{llll} C_1 = 5.601nF & C_2 = 100.0nF & L = 19.26mH & R_l = 36.40\Omega \\ R = 2.028K\Omega & G_a = -0.756mS & G_b = -0.409mS & B_p = 1V \\ \tilde{C}_1 = 5.592nF & \tilde{C}_2 = 100.1nF & \tilde{L} = 19.34mH & \tilde{R}_l = 36.07\Omega \\ \tilde{R} = 2.021K\Omega & \tilde{G}_a = -0.756mS & \tilde{G}_b = -0.409mS & \tilde{B}_p = 1V \end{array} \tag{12}$$

We show each of the signals v_s, v_{i_i}, v_t, v_{i_d}, v_r in both the time domain and frequency domain in Fig. 3a through Fig. 5b. In all photographs, the input signal is a 500Hz sine wave of 400mV p-p with a 500mV offset. All frequency spectrum photographs show a 5kHz bandwidth, starting at 0Hz, with 10dB/div. All frequency spectra were averaged 256 times with a Hanning window.

[4] As $v_1(t)$ goes through 0 relatively fast compared to the input signal $v_s(t)$, the small error that occurs due to saturation in the divider is quite short.

[5] R_l is the series resistance of the inductor.

A sinusoidal signal is chosen as the worst case information signal due to its effect of adding shifted and scaled versions of the chaos. The shifted versions appear as secondary peaks located at the input frequency (500Hz) higher and lower than the main peak in the injected signal, shown in Fig. 4b. However, these secondary peaks are not apparent in the transmitted signal shown in Fig. 5b.

For comparison, we show the injected and transmitted spectrums without an input signal in Figs. 6a-b. We have chosen here a constant offset to which the input signal is added in order to maintain similar frequency characteristics in the transmitted signal, regardless of the information signal.

Finally, we show in Figs 7a-b how the recovered signal i_d degrades for both a 1% mismatch between the parameters R and $\tilde{R}$, and for when gaussian noise at 1% of the transmitted power at 5kHz BW is added in the channel.

We remark that by reversing the order of operations (i.e. modulating (coding) with the multiplier, demodulating (decoding) with the divider), the sensitivity to noise in the channel is reduced as well as sensitivity to parameter mismatch. This is due to the following reason. As shown in the next section, a filtered version of additive channel noise is detected in the current detector. This is then divided by the signal from the channel which contains the noise itself. Thus, the noise is transformed to more or less an offset. Reduction in parameter mismatch sensitivity is similarly explained, as parameter mismatch also has the effect of adding a filtered version of the chaos to the detected signal, as explained in the next section. Thus, upon dividing the detected signal by the transmitted chaos, the extra chaotic components injected due to parameter mismatch divide out to become a parameter dependent offset.

It can be seen from the above that using multiplication as the decoding function squares both the detected noise from the channel and the chaotic noise due to parameter mismatch. This effect increases both sensitivity to noise and level of security. Due to space limitations, we have not included a series of photos illustrating these effects.

4 Parameter Mismatch and Channel Noise

When the parameters of the transmitting and receiving systems are not identical, the retrieved signal will be corrupted by chaotic noise. This is the reason the system is secure in

this sense: that the parameters have to be matched very closely in order for the retrieved signal to resemble the transmitted signal. There is also noise added to the signal when v_1 is transmitted through a noisy channel. In other words, $\tilde{v}_1 = v_1 + v_{ns}$. In this section, we consider what effects these noise signals have on the retrieved signal.

Refer again to Figure 1. We define $v_g = v_1 - v_2$ as the voltage across the linear resistor R. Subtracting equation (7) from (4) and (8) from (5) we get:

$$\frac{dy}{dt} = \left(\frac{1}{RC_2} - \frac{1}{\tilde{R}\tilde{C}_2}\right) v_g - \frac{1}{\tilde{R}\tilde{C}_2} y + \frac{1}{\tilde{C}_2} z + \left(\frac{1}{C_2} - \frac{1}{\tilde{C}_2}\right) i_3 - \frac{1}{\tilde{R}\tilde{C}_2} v_{ns} \tag{13}$$

$$\frac{dz}{dt} = -\frac{1}{\tilde{L}} y + \left(\frac{1}{\tilde{L}} - \frac{1}{L}\right) v_2 \tag{14}$$

where $y = v_2 - \tilde{v}_2$ and $z = i_3 - \tilde{i}_3$. Thus y appears as a lowpass-filtered version of the chaotic signals v_g, v_{ns}, v_2 and i_3 when $C_2 \neq \tilde{C}_2$, $L \neq \tilde{L}$ and $R \neq \tilde{R}$.

Subtracting equation (6) from (3) we get:

$$i_d(t) = \frac{\tilde{C}_1}{C_1} i_i(t) + \left(\frac{R}{\tilde{R}} - \frac{\tilde{C}_1}{C_1}\right) \frac{v_g}{R} + g(v_1) + \frac{1}{\tilde{R}} y + \frac{1}{\tilde{R}} v_{ns} \tag{15}$$

where $g(v_1) = \tilde{f}(v_1) - \frac{\tilde{C}_1}{C_1} f(v_1)$ is at the worst a 5-segment piecewise-linear function. Thus the general conclusion we can make is that the error due to parameter mismatch and channel noise is composed of three components:

1. A term $\frac{1}{R} y$ which is the chaotic signals $a_1 v_g - v_{ns}$, $a_2 v_2$ and $a_3 i_3$ filtered through a second order filter consisting of the capacitor $\tilde{C}_2$, the inductor $\tilde{L}$ and the resistor $\tilde{R}$, where $a_1 = \frac{\tilde{R}\tilde{C}_2}{RC_2} - 1$, $a_2 = 1 - \frac{\tilde{L}}{L}$ and $a_3 = \frac{\tilde{C}_2}{C_2} - 1$ are dimensionless numbers. A circuit diagram depicting this is shown in figure 8. In this figure, the signal y is the voltage across capacitor $\tilde{C}_2$.

2. A nonlinear mapping of the chaotic signal v_1 through the piecewise-linear function g, and

3. a term

$$\left(\frac{1}{\tilde{R}} - \frac{\tilde{C}_1}{C_1 R}\right) v_g + \frac{1}{\tilde{R}} v_{ns}$$

Component 1 occurs when $C_2 \neq \tilde{C}_2$ and $L \neq \tilde{L}$. Component 2 and 3 occur when $C_1 \neq \tilde{C}_1$.

When $R \neq \tilde{R}$, all three components will occur. Note that when $\tilde{R}\tilde{C}_2 = RC_2$, the error due to v_g in component 1 and 3 vanishes.

5 Discussion

In the schemes proposed in [Oppenheim *et al.*, 1992], [Kocarev *et al.*, 1992], the chaotic signal is simply added to the information signal in order to mask it. In this new scheme, the information signal modulates the chaos generated in the circuit and is then injected into the same chaotic circuit as a current, combining with the chaos in a complicated way as the dynamics of the circuit evolve. The are some advantages of this system over the secure communication system proposed in [Kocarev *et al.*, 1992]. First, the information is spread over the spectrum of the chaos. Second, the sensitivity to parameter variation is enhanced, and thus the number of "encryption keys" is increased. This sensitivity enhancement can be exploited with a monolithic IC implementation of Chua's circuit such as the one recently designed in Professor Rodriguez-Vazquez's laboratory [Delgado-Restituto & Rodriguez-Vazquez, 1993]. This is because a monolithic IC makes a high degree of parameter matching possible in a high-speed circuit. This allows high fidelity detection while making it very difficult for a third party to detect the signal without another copy of the IC chip implemented in the same way (the mask and silicon foundry may even be significant factors in the degree of matching). Finally, synchronization is more robust due to the passivity of the subcircuit with the nonlinear resistor.

6 Conclusions

We have demonstrated the feasibility of using Chua's circuits to implement a secure communications system. This system has the advantages of transmitting a spread-spectrum signal, and having enhanced sensitivity to parameter variations. Conversely, by swapping the coding and decoding functions, the system has enhanced robustness to noise and parameter variations. Finally, a very secure system can be implemented using either higher-order Chua's circuits (which will result in an even more secure system as there are more parameters to vary), or using monolithic ICs.

Acknowledgements

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Appendix

In this appendix, implementation details of the system in Fig. 2 are discussed.

Nonlinear resistors

The nonlinear resistors were implemented according to [Kennedy, 1992].

Current source

The current source schematic is shown in Fig 9. Current sources made with voltage output elements are difficult. The most common failing being peaking in the frequency domain caused by the employment of positive feedback. In order to achieve a relatively flat response, negative feedback paths must dominate positive feedback paths. In the circuit designed, this is true for any load resistance $R_l \leq 10 \cdot R_f$. In fact, the overall feedback term f is equal to $\frac{-R_f}{R_f+R_l}$ where R_l is the load resistance and R_f is the feedback resistor. Choosing R_f close to or greater than R_l insures stable operation.

Note that the sign of the current leaving the source is the negative of the sign of the controlling voltage.

Divider

The divider schematic is shown in Fig 10. A four quadrant divider[6] was necessary in this system for the following reason. For a secure system, there must be no replica of the original information signal in the transmitted signal. Any replicas introduced in the injected signal in the topology chosen here would be amplified. See [Halle *et al.*, 1992] for experimental evidence of this amplification phenomenon. Now, the Taylor expansion of $1/(1+x)$ is $(1 - x + x^2 - \cdots)$. This contains a constant term, thus the ratio includes a copy of the numerator. Therefore, we cannot use an offset to the denominator to force the denominator to always be of the same sign. This in turn requires that we use a true four quadrant divider.

There is no simple means previously known to the authors of implementing a four quadrant analog divider[7]. Three-quadrant division can be implemented by inverting the multipli-

[6] "Four quadrant" refers the fact that both operands can be of either sign.

[7] New techniques based on charge transfer are rather complicated to implement.

cation operation with feedback. However, the denominator must always remain of fixed sign in order to ensure negative feedback. The approach chosen here relies on the observation that multiplying numerator and denominator by the sign of the denominator (sgn(Den)) does not change the value of the ratio, however, the new denominator is now always positive. Thus, operation can be attained in all four quadrants using a feedback based divider, or any other three-quadrant divider. With differential inputs to the multiplier and the summing point in the feedback loop, implementation of the multiplication of numerator and denominator by sgn(Den) reduces to a decision of which of the differential inputs to force to ground. This is accomplished with a comparator for decision making, and junction field effect transistors (JFET) acting as voltage controlled switches.

Multiplier

The multiplier schematic is shown in figure 11. This function is available, already implemented, in a single IC package.

Current detector and buffer

The current detector schematic is shown in figure 12. Its operation relies on the V-I characteristic of resistors plus feedback. Node $\tilde{v}_1$ is forced to follow v_t via negative feedback. Any current flowing into node $\tilde{v}_1$ generates a voltage across resistor R_d. The rest of the circuit subtracts the voltage at the bottom of the resistor ($\tilde{v}_1$ from the voltage at the top. Thus, v_{i_d} is a voltage representing the value of the current flowing into node $\tilde{v}_1$. In fact, $v_{i_d} = R_d \cdot i_d$, while the buffer insures that $\tilde{v}_1 = v_t$.

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M. P. Kennedy [1992], "Robust op amp realization of Chua's circuit," *Frequenz*, **46**(3–4), 66–80.

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Figure Captions

Figure 1: Schematic diagram of the basic communication system.

Figure 2: Block diagram of implemented system. The current detector is also a voltage buffer, forcing $\tilde{v}_1 = v_t$, where $v_t = v_1 + v_{ns}$. In the divider, **N** stands for the numerator and **D** stands for the denominator.

Figure 3a: Input signal vs recovered signal. The top trace is the input signal, v_s. The bottom trace is the recovered signal, v_r.

Figure 3b: Spectrum of the input signal v_s.

Figure 3c: Spectrum of the recovered signal v_r.

Figure 4a: Injected signal vs detected signal. The injected signal, v_{i_i}, is shown at the top. The detected signal, v_{i_d} is shown at the bottom.

Figure 4b: Spectrum of the injected signal v_{i_i}. Note secondary peaks located 500Hz above and below the main peak which is near 3000Hz. See also Fig. 6a for comparison.

Figure 4c: Spectrum of the detected signal v_{i_d}.

Figure 5a: Time waveform of the transmitted signal, v_t.

Figure 5b: Spectrum of the transmitted signal v_t. See also Fig. 6b for comparison. Note that no secondary peaks are detectable. See text.

Figure 6a: Spectrum of the injected signal v_{i_i} with zero input. Here, the amplitude of the input signal is zero. However, the offset is still 500mV.

Figure 6b: Spectrum of transmitted signal with zero input. Amplitude of input signal is zero, the offset is 500mV.

Figure 7a: Input signal vs recovered signal with 1% resistor mismatch. The top trace is the input. The bottom trace is the recovered signal.

Figure 7b: Input signal vs recovered signal with 1% channel noise. Noise equivalent to 1% of the total power in the transmitted signal from 0Hz to 5kHz was added to the transmitted signal. The top trace shows the input signal, the bottom trace shows the recovered signal.

Figure 8: Equivalent circuit depicting the noise sources due to parameter mismatch. The equivalent noise source y appears when $C_2 \neq \tilde{C}_2$, $L \neq \tilde{L}$, or $R \neq \tilde{R}$.

Figure 9: Schematic of current source. $R = 10k\Omega$, $R_f = 80k\Omega$.

Figure 10: Schematic of divider circuit. The JFET used is MPF102.

Figure 11: Schematic of multiplier circuit.

Figure 12: Schematic of current detector circuit. v_{i_d} is a voltage representing the value of the current i_d. $R = 10k\Omega$, $R_d = 1k\Omega$.

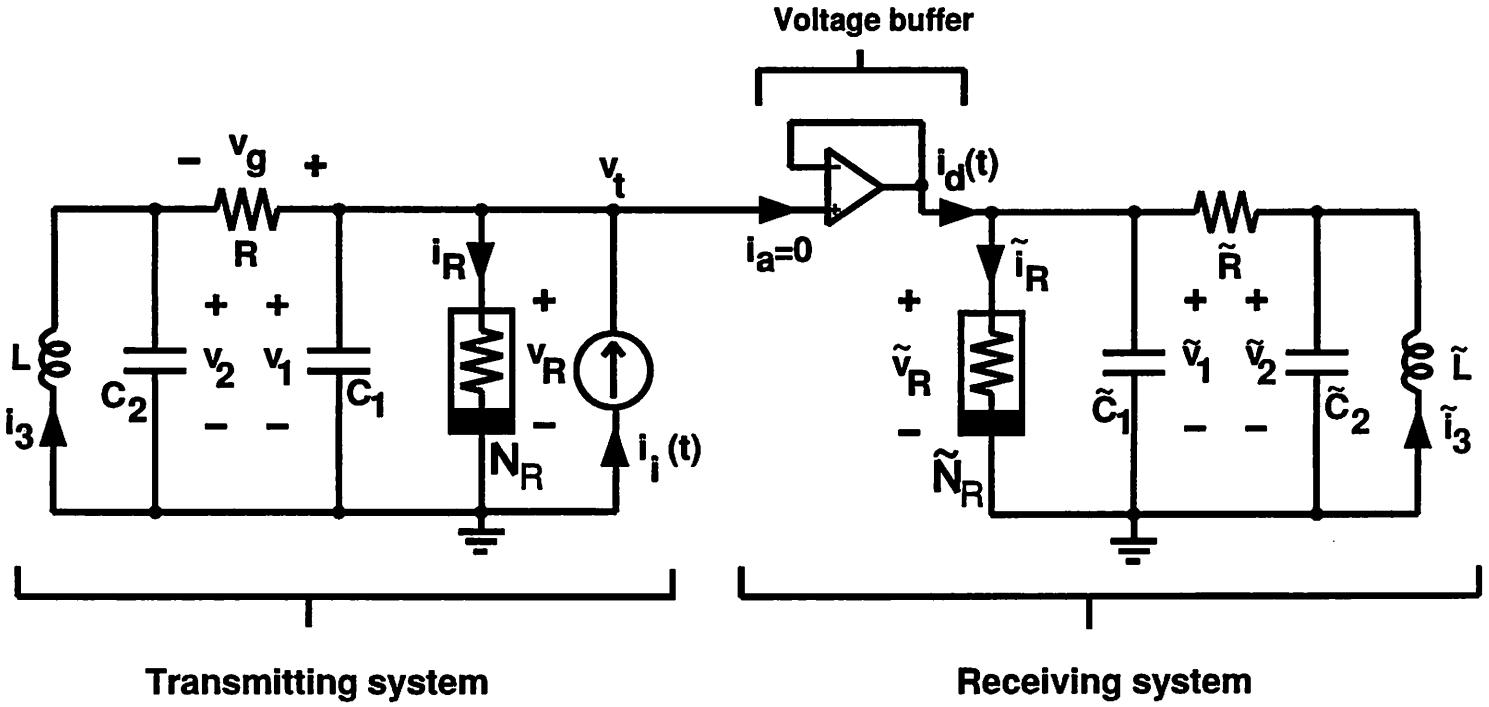

Voltage buffer
v_g
R
v_t
i_R
$i_a=0$
$i_d(t)$
$\tilde{i}_R$
$\tilde{R}$
L
i_3
C_2
v_2
v_1
C_1
v_R
N_R
$i_i(t)$
$\tilde{v}_R$
$\tilde{N}_R$
$\tilde{C}_1$
$\tilde{v}_1$
$\tilde{v}_2$
$\tilde{C}_2$
$\tilde{L}$
$\tilde{i}_3$
Transmitting system
Receiving system

Figure 1

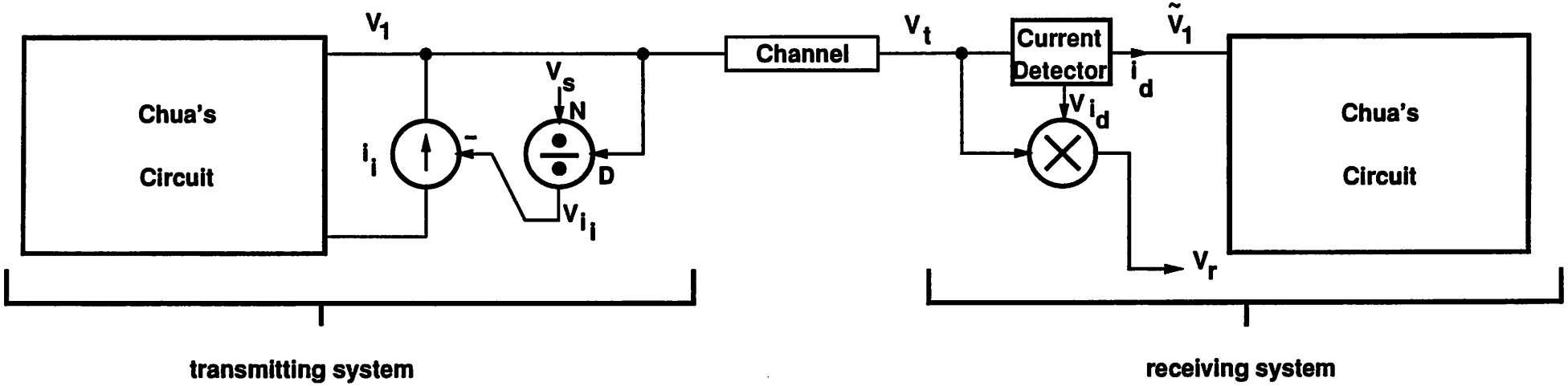
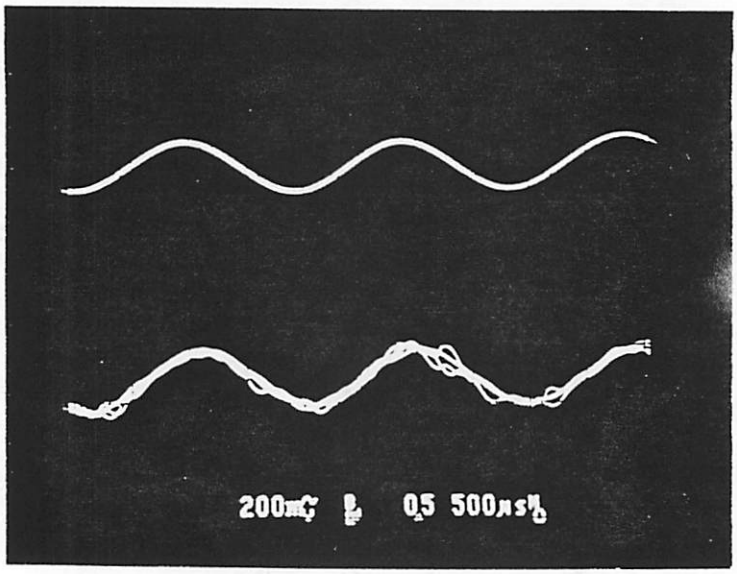
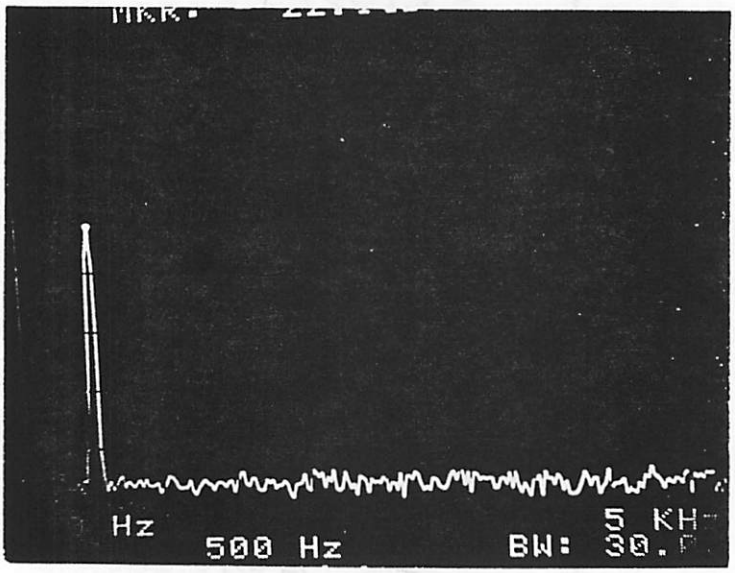

Chua's
Circuit
V_1
i_i
V_s
N
D
V_{i_i}
Channel
V_t
Current
Detector
i_d
V_{i_d}
$\tilde{V}_1$
Chua's
Circuit
V_r
transmitting system
receiving system

Figure 2



3a



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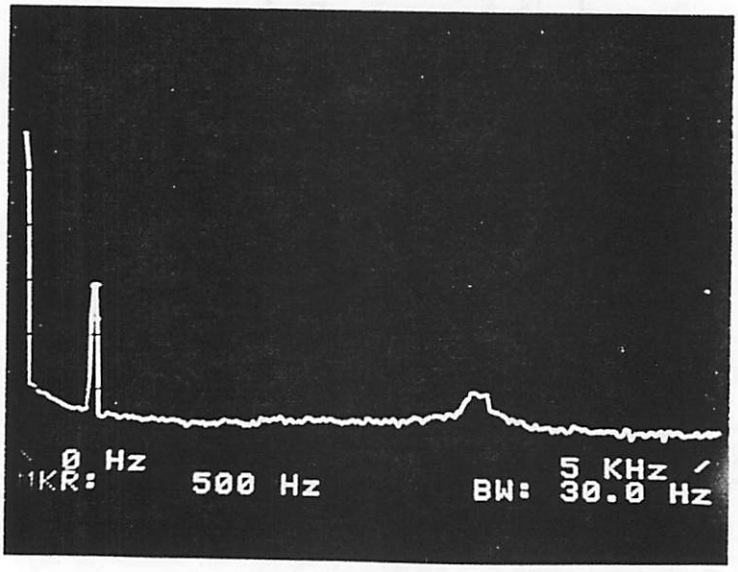
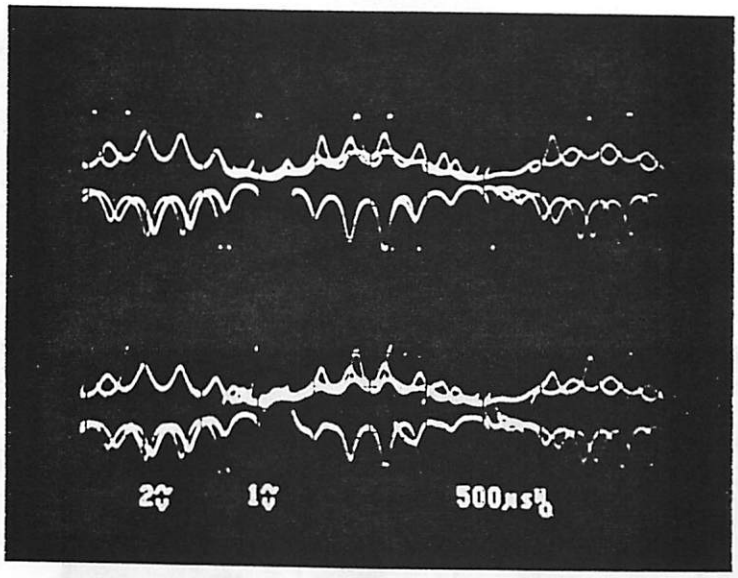
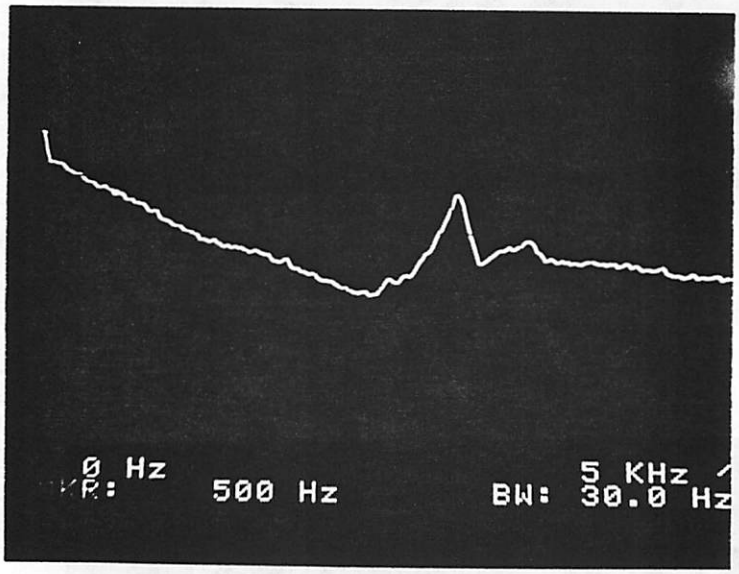


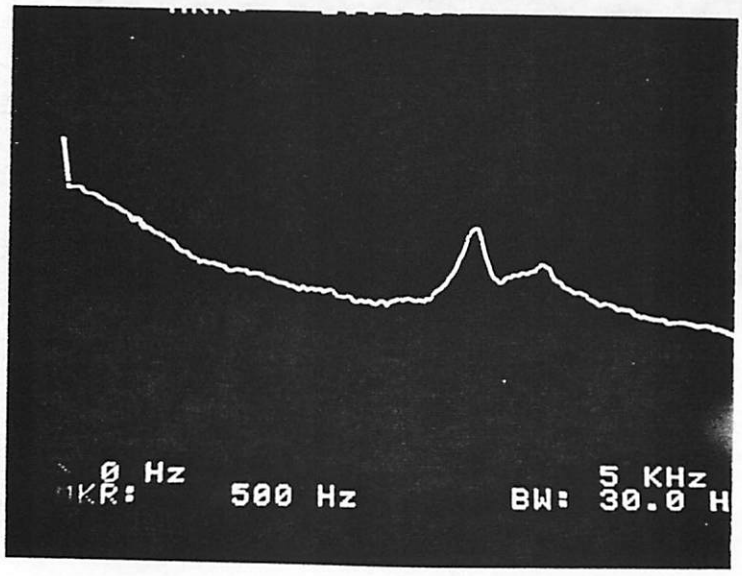
3c


2V
1V
500μs

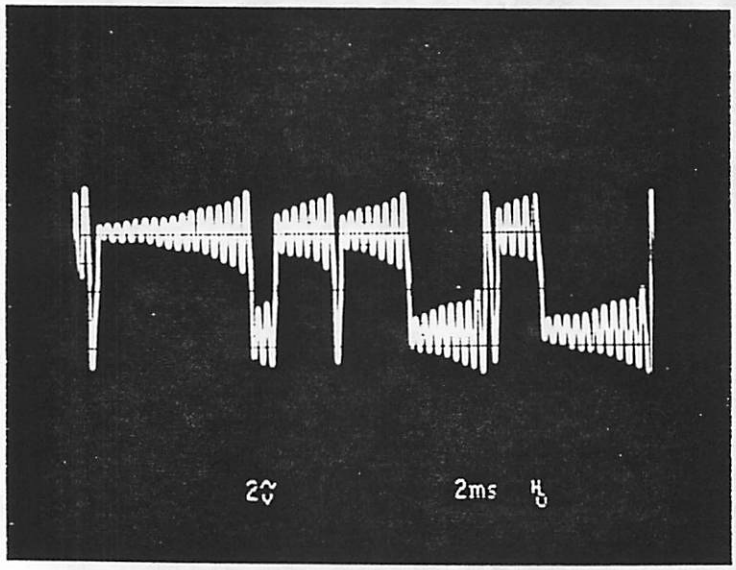
4a


0 Hz
MKR:
500 Hz
5 KHz
BW: 30.0 Hz

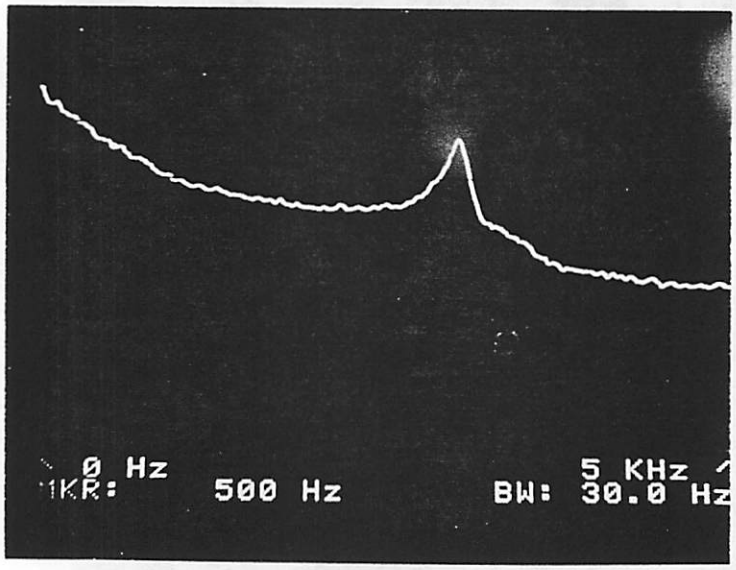
4b


0 Hz
MKR:
500 Hz
5 KHz
BW: 30.0 H

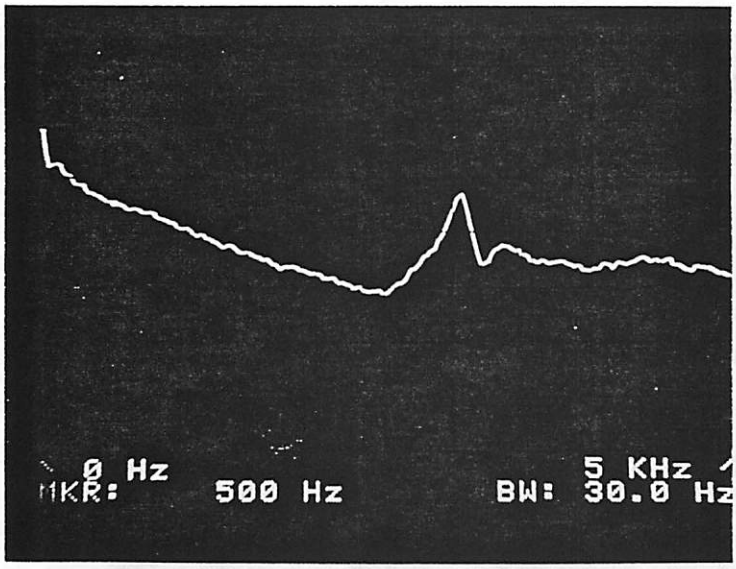
4c



5a



5b



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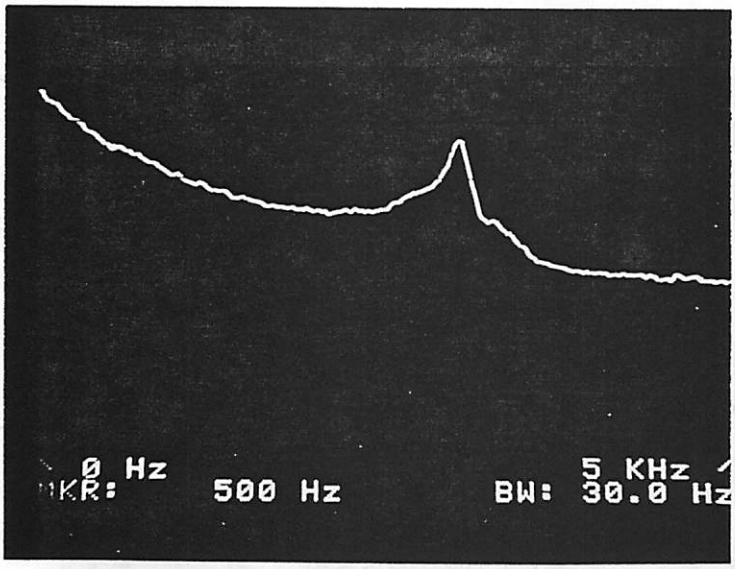

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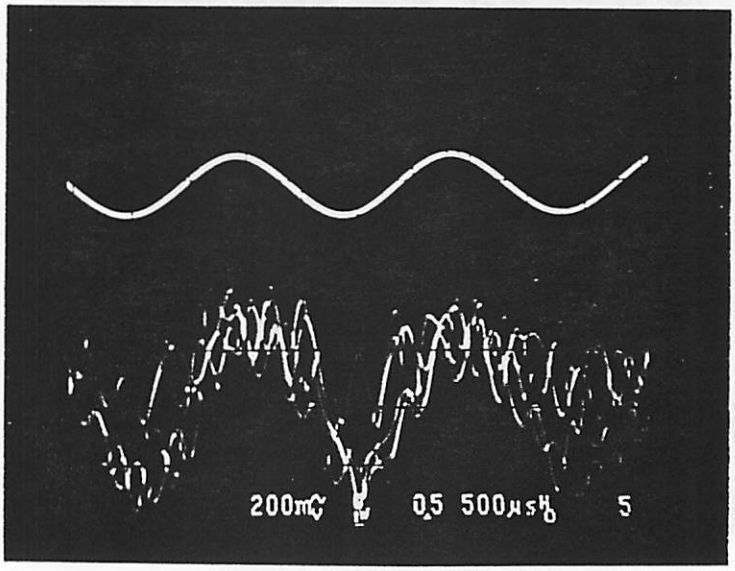

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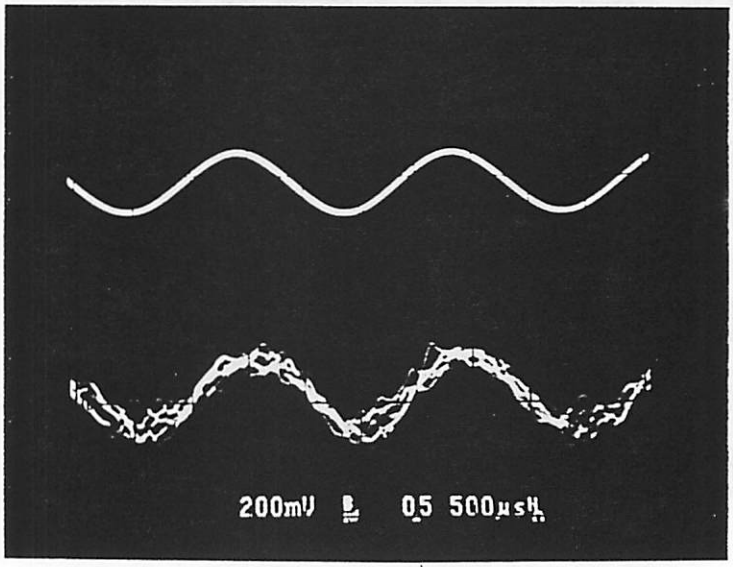

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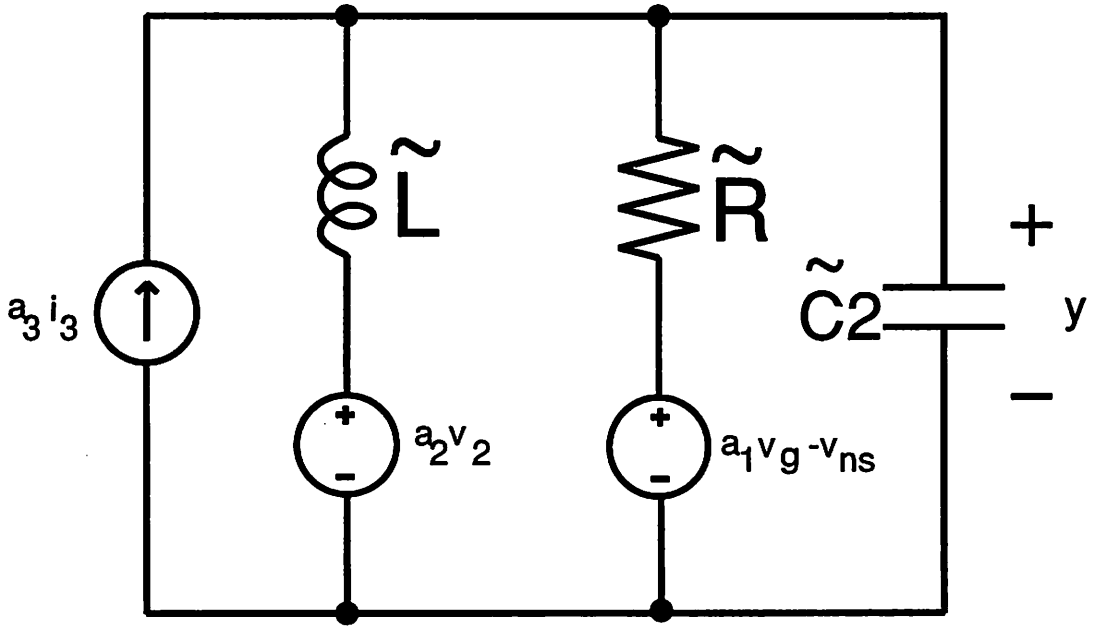


Figure 8

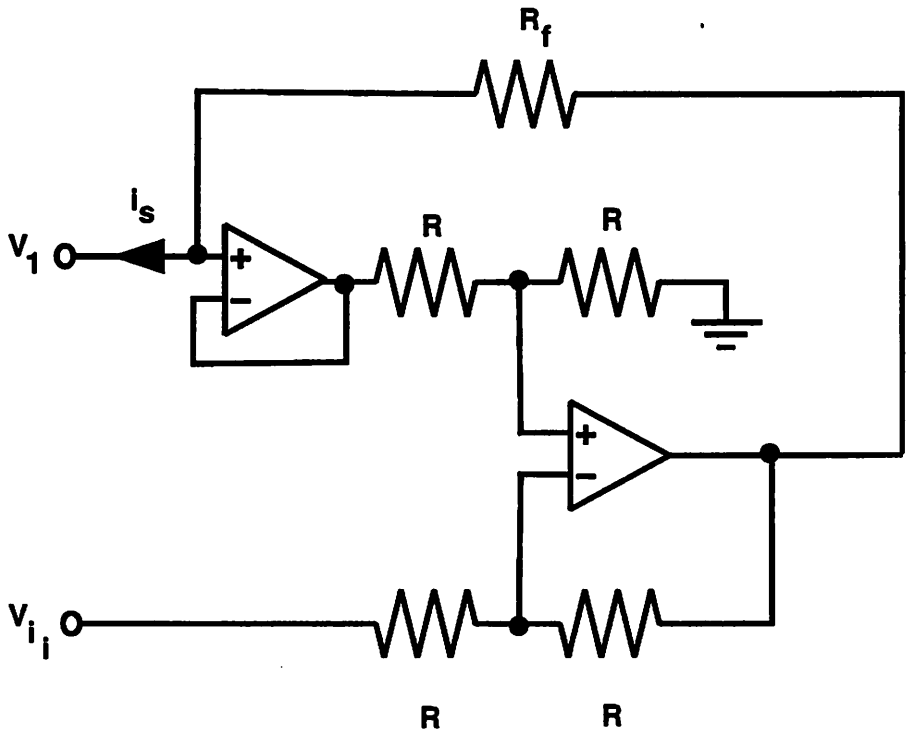
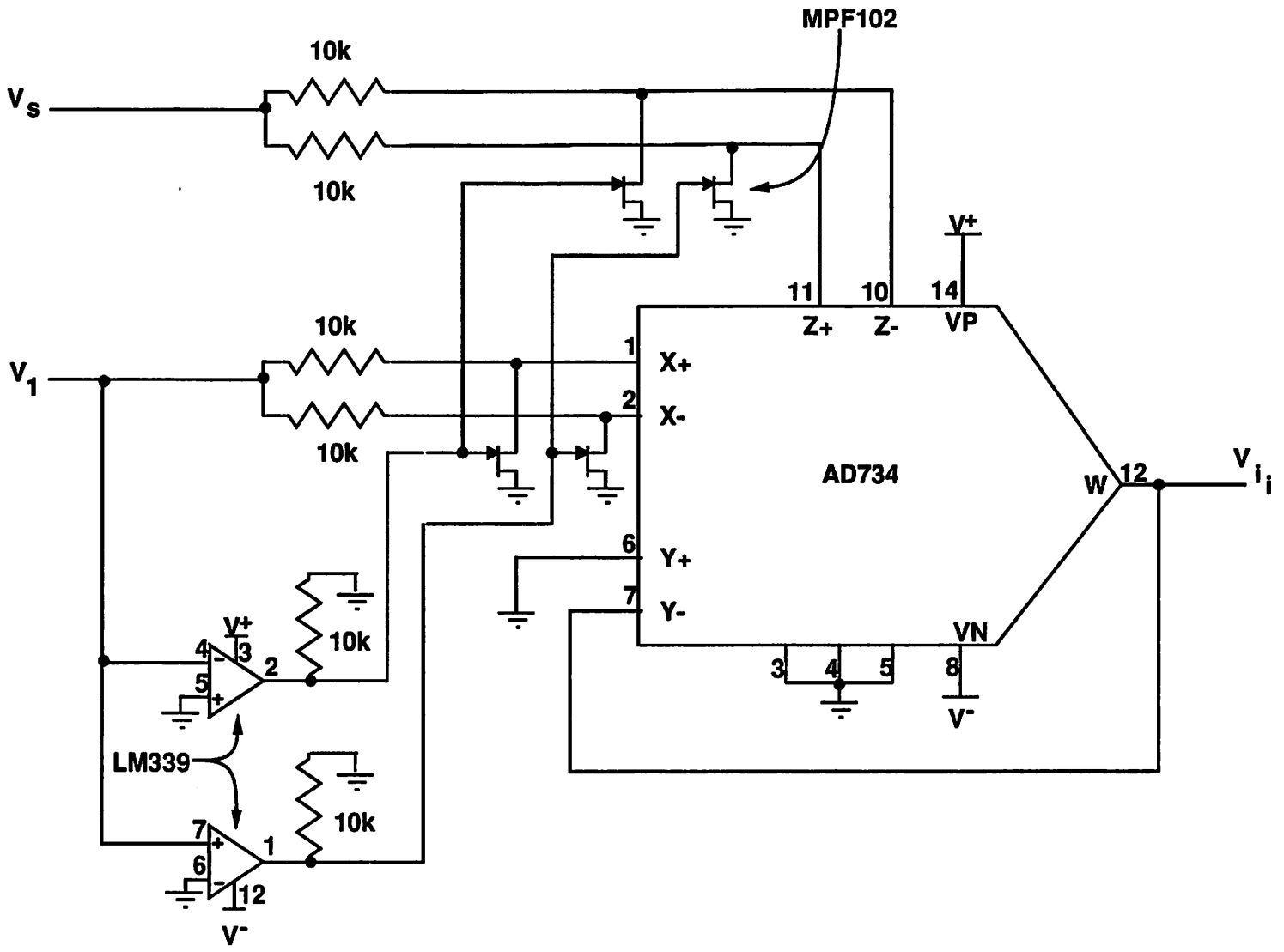


Figure 9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10k
V_S
10k
10k
V_1
10k
V+
11
10
14
Z+
Z-
VP
1
X+
2
X-
AD734
W
12
V_{i_i}
6
Y+
7
Y-
VN
3
4
5
8
V-
V+
4
3
2
5
10k
LM339
7
1
6
12
10k
V-

Figure 10

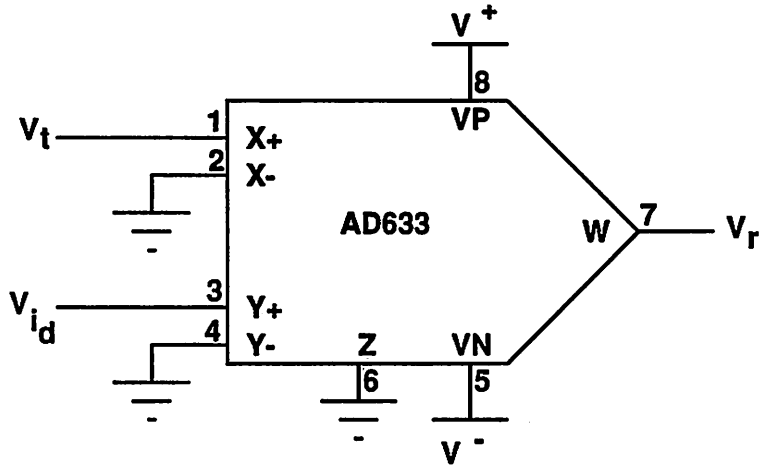

Figure 11

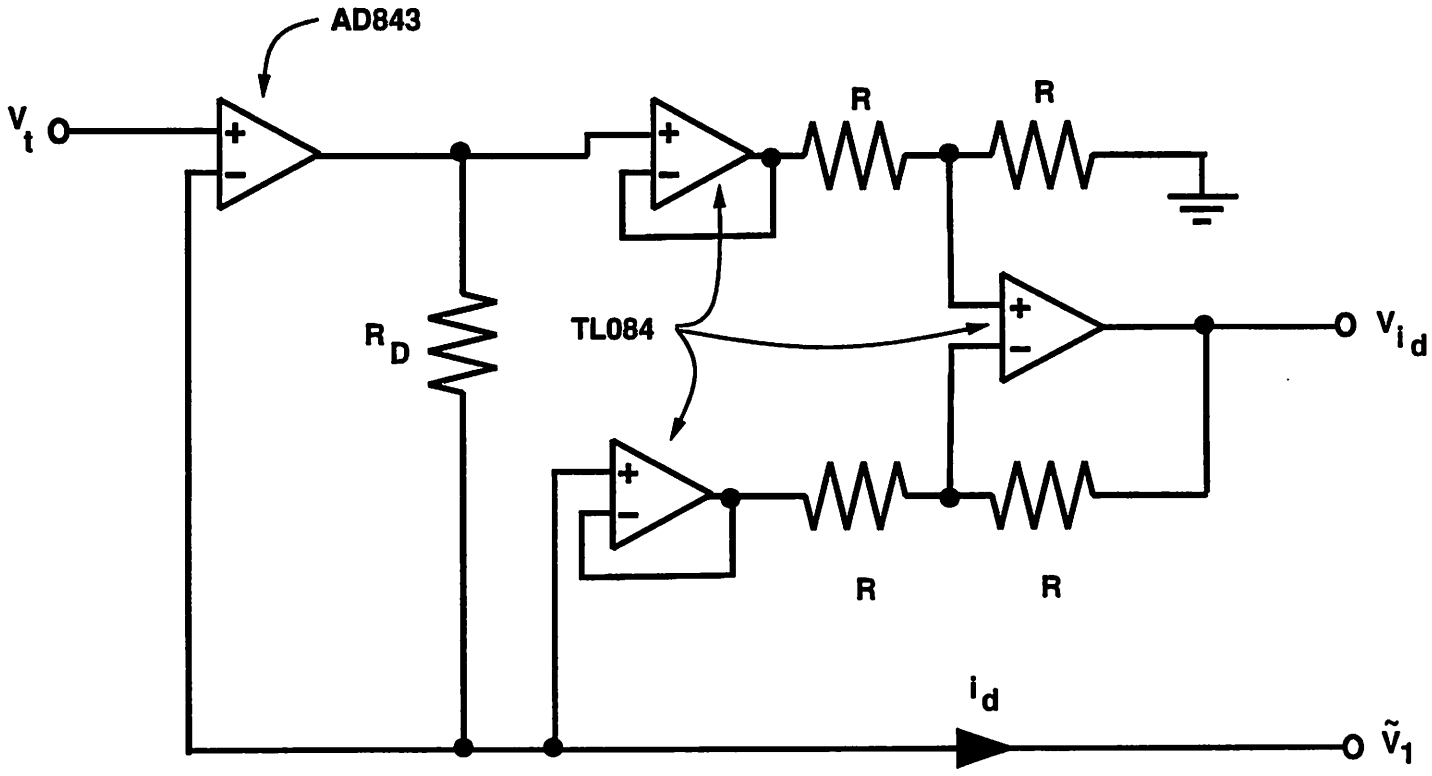

Figure 12