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**A ROBUST PHYSICAL AND PREDICTIVE
MODEL FOR DEEP-SUBMICROMETER MOS
CIRCUIT SIMULATION**

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J. H. Huang, Z H. Liu, M. C. Jeng*, P.K. Ko, C. Hu
 Department of Electrical Engineering and Computer Science
 University of California, Berkeley, CA 94720
 *Cadence Design Systems, Santa Clara, CA 95054

ABSTRACT

We present a physical, predictive and efficient model (*BSIM3*¹) for deep-submicrometer MOSFETs with emphasis on both digital and analog applications. *BSIM3* can also be suitable for statistical modeling.

I. INTRODUCTION

To cope with the continuous evolution of VLSI technology, many short-channel MOSFET I-V models for circuit simulation have been developed. Most of these models, however, are either not adequately covering the small-size effects that becomes significant at the deep-submicron level, or are highly empirical. Empirical models can have the advantages of easy formulation, because of the use of large number of empirical parameters. They may provide good accuracy in fitting single device from a wide range of technologies. However, their drawbacks are many: generating size-independent process files is a very difficult task. Extrapolating a process file for a present technology to a future one is virtually impossible, and, perhaps most important, circuit designers may lose the intuitive which is vital in achieving high performance analog and digital circuits. *BSIM3* is developed to address these drawbacks.

BSIM3 is a physical model with extensive built-in dependencies of important dimensional and processing parameters such as channel length (L), width (W), gate oxide thickness (T_{ox}), junction depth (X_j), substrate doping concentration ($N_{sub}(x, y)$), and LDD structures etc.. It allows users to accurately model, upon parameter extraction on existing technology, or predict, based on the default or an extracted technologies, MOSFET behavior over the wide range of existing and future technologies. Using a coherent pseudo 2-D formulation, such major short-channel effects and high field effects as threshold voltage reduction[1], non-uniform doping effect, mobility reduction due to vertical field[2], carrier velocity saturation [2,3], channel-length modulation(*CLM*)[2], drain-induced barrier lowering(*DIBL*)[1-2,4], substrate current induced body effect(*SCBE*)[5-6], subthreshold conduction[7], parasitic resistance effect and LDD effect[5-6], are properly included and meticulous care has been taken to retain the physical functional forms while improving model accuracy and computational efficiency. The model is compact, and time consuming functions are excluded. The ease of parameter extraction was also a major

consideration. Number of parameters is small (~ 25) and every parameter has a physical meaning, the effects of parameters on output characteristics are very predictive. This feature of *BSIM3* makes statistical study of the device fabrication process possible. Drain current and its first order derivative in all operation regions are continuous, which removes all kinks and glitches at the boundaries between the regions. *BSIM3* has been implemented into *SPICE3* and divergence problem is also greatly improved.

II. *BSIM3* MODEL

1. Threshold Voltage Model

A quasi-2d Poisson equation is developed to calculate threshold voltage (V_T)[1]. By solving the equation, an analytical V_T model is obtained.

$$V_T = V_{T0} + K_1(\sqrt{\phi_s - V_{br}} - \sqrt{\phi_s}) - K_2 V_{bs} - \Delta V_T \quad (1)$$

where V_{T0} is the ideal long channel threshold voltage. ϕ_s is the surface potential and V_{bs} is the body bias. K_1 and K_2 take into account vertical non-uniform doping effect, and can be calculated based on the doping concentration distribution inside the bulk[5]. ΔV_T is the threshold voltage reduction due to short-channel effect, has an exponential dependence on the channel length.[1]

$$\Delta V_{th} = \theta(L)[2(V_{bi} - \phi_s) + V_{ds}] \quad (2)$$

$$\theta(L) = D_{vT0}[\exp(-L/2l) + 2\exp(-L/l)] \quad (3)$$

where V_{bi} is the built-in potential of the drain and the substrate, and V_{ds} is the drain voltage. $l = \sqrt{3T_{ox} X_{dep}/\eta}$, X_{dep} is depletion width near the source and X_{dep}/η is the average depletion width along the channel. D_{vT0} and η can be determined from experimental data. V_{ds} dependence of ΔV_T is called drain-induced barrier lowering (*DIBL*) effect[1]. Fig.(1) shows the experimental data and model simulation results.

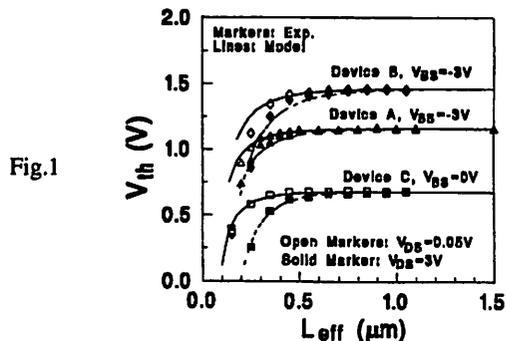


Fig.1

¹Berkeley Short-channel IGFET Model

Model also shows that thin gate oxide thickness, heavy substrate doping concentration and LDD structure can suppress the short-channel effects on V_T . Non-uniform doping effect along the channel can be taken into account by substituting the substrate doping concentration N_{sub} by

$$N_{eff} = \frac{N_{sub}(L - L_x) + N_{ds}L_x}{L} \equiv N_{sub}\left(1 + \frac{N_{ds}L_x}{L}\right) \quad (4)$$

where N_{ds} is doping concentration near the drain/source, which is usually larger than N_{sub} , and L_x is extension of N_{ds} . $N_{ds}L_x$ can be determined by experimental data.

2. Drain Current Model

Based on the mechanisms which determine the electron conduction in MOSFET, the whole operation region is divided into strong inversion region ($V_{gs} > V_T$), weak inversion region ($V_{gs} < V_T$) and transition region ($V_{gs} \sim V_T$), where V_{gs} is the gate voltage. [7]

(i) **Strong Inversion Region:** The strong inversion region is divided into triode region ($V_{ds} < V_{dsat}$) and saturation region ($V_{ds} > V_{dsat}$). $V_{dsat} = E_{sat}LV_{gst}/(E_{sat}L + V_{gst})$, $E_{sat} = 2v_{sat}/\mu_{eff}$ [2], where v_{sat} is saturation velocity, μ_{eff} is the effective mobility. In the triode region, the drain current is given by [2-3]

$$I_{ds} = \mu_{eff}C_{ox} \frac{W}{L} \frac{1}{1 + V_{ds}/E_{sat}L} (V_{gst} - V_{ds}/2)V_{ds} \quad (5)$$

where $1 + V_{ds}/E_{sat}L$ comes from velocity saturation effect and

$V_{gst} = V_{gs} - V_{th}$. In the saturation region, we have [2-3]

$$I_{ds} = v_{sat}WC_{ox}(V_{gst} - V_{dsat})(1 + (V_{ds} - V_{dsat})/V_A) \quad (6)$$

where V_A is the Early voltage which is introduced to model output resistance of MOSFET in saturation region [6].

(ii) **Weak Inversion Region:** In weak inversion region, the diffusion current dominates, and the drain current depends on the gate voltage exponentially [7].

$$I_{ds} = I_{s0} \exp\left(\frac{V_{gst} - V_{off}}{nV_{tm}}\right) \left(1 - \exp\left(-\frac{V_{ds}}{V_{tm}}\right)\right) \quad (7)$$

where $I_{s0} = \mu_{eff}(W/L)C_dV_{tm}^2$, $V_{tm} = k_B T/q$ and T is temperature. V_{off} is the offset voltage [7] and n is the swing factor.

(iii) **Transition Region:** In transition region, the gate voltage is very close to the threshold voltage ($V_T - \Delta < V_{gs} < V_T + \Delta$, $\Delta \sim 0.12V$). Both drift and diffusion current are important. There is no simple physical and analytical model available for the drain current in this region. *BSIM2* used a spline function to model drain current in this region and it matches experimental data very well [7]. The only drawback of using spline function is time consuming when determining all of the coefficients of the spline function. In *BSIM3*, a simple way was developed to model drain current in the transition region and can guarantee the continuity of drain current and its first order derivative at the two boundaries [5]. The point (V_p, I_p) is determined by the lower bound (V_{dslow}, I_{dslow}) and higher bound (V_{gshigh}, I_{dshigh}), in Fig. 2.

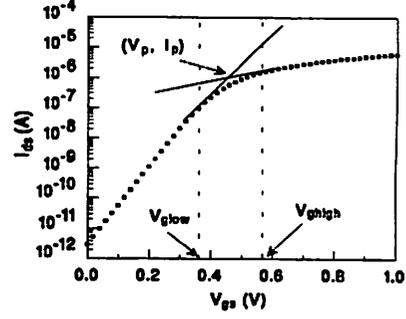


Fig. 2

The drain current in this region is

$$I_{ds} = (1-t)^2 I_{dslow} + 2(1-t)tI_p + t^2 I_{dshigh} \quad (8)$$

$$V_{gs} = (1-t)^2 V_{gslow} + 2(1-t)tV_p + t^2 V_{gshigh} \quad (9)$$

where $0 \leq t \leq 1$ and can be determined by eq. 9.

3. Output Resistance Model

In analog circuit applications, the voltage gain is directly proportional to R_{out} . Existing analytical models for MOSFET R_{out} are not adequate [8], because only channel-length modulation effect is included. The empirical model[7] is more accurate, however it lacks scalability. To achieve high accuracy and scalability, R_{out} model must be analytical and include all the major physical mechanisms that affect R_{out} . Major mechanisms[6] which affect R_{out} are channel-length modulation (*CLM*), drain-induced barrier lowering (*DIBL*) and substrate current induced body effect (*SCBE*). Early voltage (V_A) is introduced to model R_{out} as follows

$$I_{ds}(V_{gs}, V_{ds}) = I_{ds}(V_{gs}, V_{dsat}) + \frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial V_{ds}} (V_{ds} - V_{dsat}) \quad (10)$$

$$\equiv I_{dsat}(1 + (V_{ds} - V_{dsat})/V_A)$$

where $I_{dsat} = I_{ds}(V_{gs}, V_{dsat}) = v_{sat}WC_{ox}(V_{gst} - V_{dsat})$. V_A has three components, i.e., V_{ACLM} , V_{ADIBL} and V_{ASCBE} , corresponding to *CLM*, *DIBL* and *SCBE*, respectively.

$$\frac{1}{V_A} = \frac{1}{I_{dsat}} \left[\left(\frac{\partial I_{ds}}{\partial V_{ds}} \right)_{CLM} + \left(\frac{\partial I_{ds}}{\partial V_{ds}} \right)_{DIBL} + \left(\frac{\partial I_{ds}}{\partial V_{ds}} \right)_{SCBE} \right] \quad (11)$$

$$= \frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBL}} + \frac{1}{V_{ASCBE}}$$

Each component can be calculated separately as follows [6]

$$V_{ACLM} = \left[\frac{1}{I_{dsat}} \left(\frac{\partial I_{ds}}{\partial V_{ds}} \right)_{CLM} \right]^{-1} = I_{dsat} \left(\frac{\partial I_{ds}}{\partial V_{dsat}} \frac{\partial V_{dsat}}{\partial L} \frac{\partial L}{\partial V_{ds}} \right)^{-1} \quad (12)$$

$$= (E_{sat}L + V_{gst})(V_{ds} - V_{dsat})/E_{sat}$$

$$V_{ADIBL} = \left[\frac{1}{I_{dsat}} \left(\frac{\partial I_{ds}}{\partial V_{ds}} \right)_{DIBL} \right]^{-1} = I_{dsat} \left(\frac{\partial I_{ds}}{\partial V_{dsat}} \frac{\partial V_{dsat}}{\partial V_{th}} \frac{\partial V_{th}}{\partial V_{ds}} \right)^{-1} \quad (13)$$

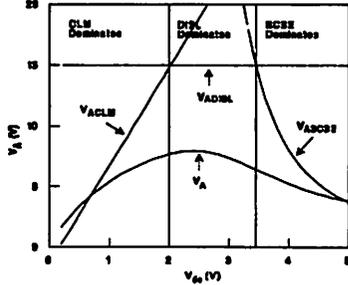
$$= (E_{sat}L + V_{gst})/\theta(L)(1 + 2E_{sat}L/V_{gst})$$

$$V_{ASCBE} = \left[\frac{1}{I_{dsat}} \left(\frac{\partial I_{ds}}{\partial V_{ds}} \right)_{SCBE} \right]^{-1} = I_{dsat} \left(\frac{\partial I_{ds}}{\partial V_T} \frac{\partial V_T}{\partial V_{bs}} \frac{\partial V_{bs}}{\partial I_{sub}} \frac{\partial I_{sub}}{\partial V_{ds}} \right)^{-1} \quad (14)$$

$$= \sqrt{\left[\frac{A_s}{B_s} \left(1 + g_m \frac{\gamma}{2\sqrt{\phi_s - V_{bs}}} R_{sub} \left(1 + \frac{B_s l}{V_{ds} - V_{dsat}} \right) \right) \exp\left(-\frac{B_s l}{V_{ds} - V_{dsat}}\right) \right]}$$

where $l = \sqrt{3T_{ox}X_j}$. A_i and B_i are the parameters associated with the substrate current determined by experimental data [9]. g_m is the transconductance, γ is the coefficient of body effect, and R_{sub} is the substrate resistance. The individual component of V_A together with the resultant V_A are shown in Fig. 3. The dominant mechanism is the one with the smallest Early voltage in each region.

Fig. 3

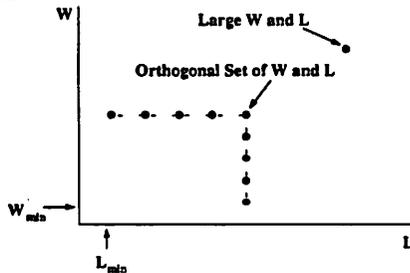


In order to have a smooth transition from triode region to saturation region, the Early voltage (V_{Asat}) at $V_{ds} = V_{dsat}$ is introduced, which can be determined in triode region. If eq. 5 is used in the triode region $V_{Asat} = E_{sat}L + V_{dsat}$. The total Early voltage is
$$V_A = V_{Asat} + (1 + \alpha L_n/l)(1/V_{ACL M} + 1/V_{ADIBL} + 1/V_{ASCBE})^{-1} \quad (15)$$
 $1 + \alpha L_n/l$ take into account LDD effect [1], and L_n is the length lightly doped region. $\alpha \sim 0.2$.

III. PARAMETER EXTRACTION

Parameter extraction plays very important role in the circuit simulations. Direct relationship of parameters with physical mechanisms and ease of extraction are two of the most important features of *BSIM3*. Parameters are extracted in the operation region only when the associated mechanisms dominate in that region. This local optimization strategy can guarantee that the parameters extracted reflect the real physical process involved in MOSFET operation. The other unique extraction algorithm used in *BSIM3* is the group device extraction, rather than the single device extraction. Parameters extracted from group devices may not fit one device perfectly, but can fit group devices over wide range well. Group device extraction algorithm makes statistical study of fabrication process possible. Fig. 4 shows the set of devices used for group device extraction. One large size is used to extract mobility and other L independent parameters. A set of orthogonal devices are used to extract parameters which represent short-channel effects and channel width effects.

Fig. 4



IV. SIMULATION AND DISCUSSION

Fig. 5-12 show the examples that one set of parameters can fit output characteristics of devices over wide range of channel length ($0.25\mu m < L < 50\mu m$) and width. We can see that *BSIM3* can predicts the scale effects very well.

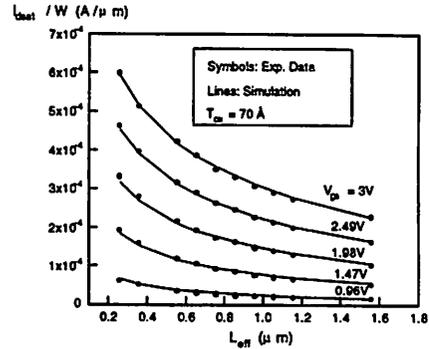


Fig. 5 Saturation current versus channel length.

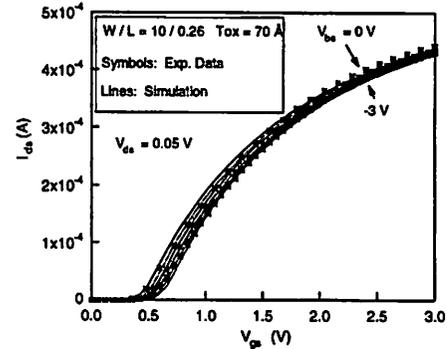


Fig. 6. Drain current versus gate voltage at different body bias

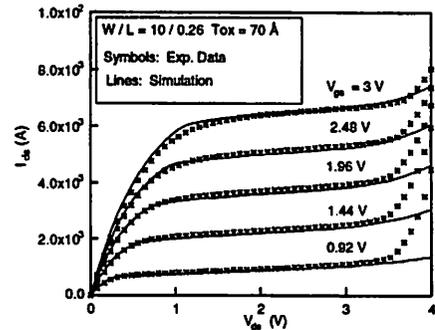


Fig. 7. Drain current versus drain voltage. $W/L=10/0.26$

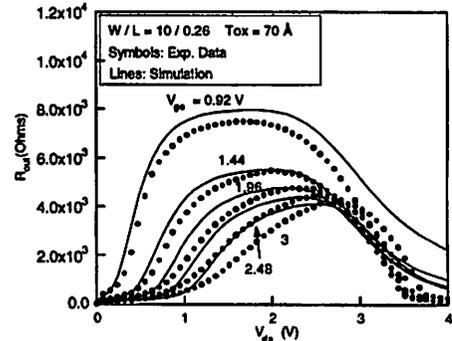


Fig. 8. Output resistance versus drain voltage. $W/L=10/0.26$

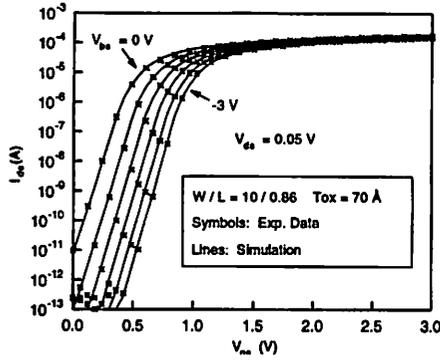


Fig. 9. Drain current vs. gate voltage. $W/L=10/0.86$

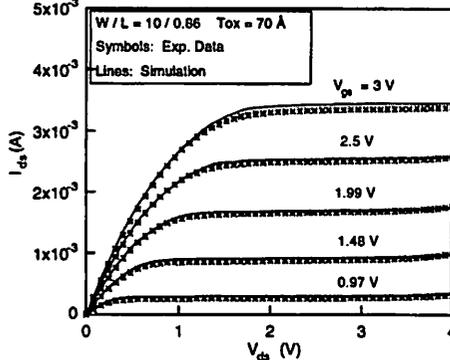


Fig. 10. Drain current vs. drain voltage. $W/L=10/0.86$

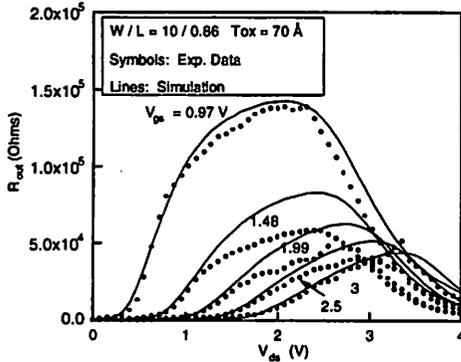


Fig. 11. Output resistance vs. drain voltage.

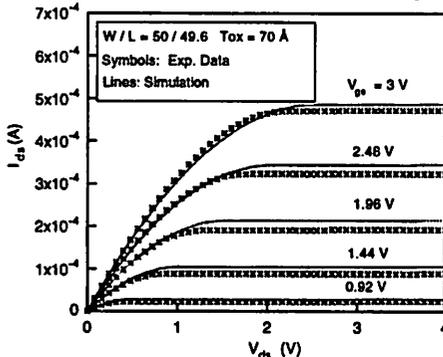


Fig. 12. Drain current vs. drain voltage. $W/L=50/49.6$.

The transition between the subthreshold region to strong inversion can be modeled very well, shown in Fig. 9. Figs. 13-14 show PMOS results. Table I shows the efficiency of the different models.

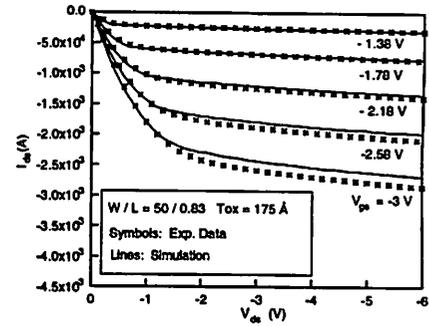


Fig. 13. Drain current vs. drain voltage. PMOS, $W/L=50/0.83$

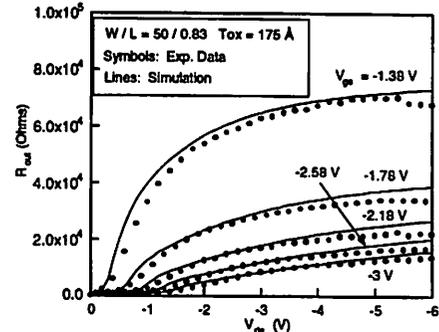


Fig. 14. Output resistance vs. drain voltage. PMOS, $W/L=50/0.83$

Table I

| Model | Speed Comparison |
|----------------|------------------|
| MOS1 (Level 1) | 1 |
| MOS2 (Level 2) | 4 - 5 |
| MOS3 (Level 3) | 2 - 3 |
| BSIM1 | 3 - 4 |
| BSIM2 | 4 - 5 |
| BSIM3 | 1 - 3 |

V. CONCLUSION

We present a physical and predictive deep-submicrometer MOSFET model in this paper. The model is scalable and robust. Total number of parameters is small (~25) and it make statistical study possible.

Acknowledgment

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