MULTI-BIT ΣΔ ANALOG-TO-DIGITAL CONVERTERS WITH NONLINEARITY CORRECTION USING DYNAMIC BARREL SHIFTING

by

Yasuaki Sakina

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Abstract

The single-bit second-order ΣΔ A/D architecture is very attractive for medium-speed and high-resolution conversion (e.g. 14 bits, 80ksamples/second for 1.75μm CMOS technology) and many signal processing systems with this architecture have become available recently. However, its performance is not sufficient to accomplish faster and higher-resolution conversion. In this report, we propose a new architecture to improve the performance. We use a multi-bit ΣΔ modulator and see the feasibility of realizing higher performance. The performance of multi-bit converters is generally degraded by internal DAC nonlinearity due to element mismatch. In the light of this we introduced the dynamic barrel shifting for the allocation of unit elements of the DAC so that we can minimize this degradation. This dynamic allocation pushes the noise due to the nonlinearity out of the baseband, which results in the improvement of the signal to noise ratio (SNR). A system-level simulator for a four-bit ΣΔ modulator is developed to analyze the behavior of the modulator. The results from the simulation show that the new four-bit ΣΔ modulator can reduce the degradation due to the element mismatch, which results in the better SNR than randomization. However, the SNR falls short of the ideal case of perfectly matched elements in the DAC. Analog-circuit requirements for a CMOS circuit implementation are also presented.

Contents

Chapter 1
Introduction

1.1 Background

The downward scaling of integrated circuits is a major trend due to recent advances in fine-line CMOS VLSI technologies. The scaling is especially promising for digital integrated circuits, which results in the realization of more complex functions and higher speed on a single chip. However, it has some disadvantages for analog integrated circuits, such as reduction in dynamic range, difficulty in realization of precisely matched components, decrease in output resistance of transistors , and so on. Therefore, it is advantageous to use digital circuits rather than analog circuits to realize a complex system on a chip using advanced CMOS technologies.

For signal processing systems, digital circuits have replaced many functions which were conventionally implemented by analog circuits. However, signal acquisition circuits in the system must deal with analog signals. Signals of particular interest are voice, audio, ISDN and video signals. Since the signals are inherently analog in nature, the interface circuits that convert analog signals to digital signals are key elements in signal acquisition circuits.

The oversampled A/D architecture based on the $\Sigma\Delta$ modulator is one of candidates which can overcome the disadvantages of analog circuits. It has fewer analog circuits and more digital circuits than conventional A/D converters. Although this architecture was originally developed for digital transmission of video signals in 1962 [1], IC implementation was not economically feasible compared with other types of conventional A/D converters before the advances of CMOS VLSI technologies (particularly less than

1.5μm technology) because the total silicon area of the ΣΔ converter was much larger than that of conventional converters, given the same performance specifications. However, due to the advanced CMOS VLSI technologies in the late 1980's, it has been receiving much more attention [2-16].

The ΣΔ converter samples at rates well above the Nyquist rate with a negative feedback filter, which results in movement of the distribution of quantization noise out of the baseband. This noise which has been modulated out of the baseband is eliminated by post digital filters. As a result, the precision of analog circuit components used in the ΣΔ architecture can be much less than that of conventional Nyquist rate A/D converters to obtain the same resolution in amplitude quantization. This means that this architecture is less sensitive to circuit imperfections and components mismatch. In addition, the performance specifications of the anti-aliasing filter will be greatly relaxed because the sampling rate is much higher than the Nyquist rate. This leads to a reduction of the silicon area for the anti-aliasing filter. Though the early applications of ΣΔ converters were limited to voice-band frequencies [6,7,9,13,14,16], there are now more applications in areas such as digital audio [10,11,12,21,22,36], ISDN [8,15], potentially sonar and higher-resolution instrumentation systems. These advantages make the ΣΔ architecture the most promising on-chip A/D interface circuit for ASIC's as well as general-purpose DSP chips.

In this report, we propose a new multi-bit ΣΔ architecture to obtain higher performance than the single-bit second-order ΣΔ architecture for the same sampling rate. Then we discuss the effects of circuit imperfections on the basic performance.

1.2 Report Organization

In chapter 2, we will introduce the basic concept of oversampled A/D converters and compare this approach with Nyquist rate A/D converters. Then we will present a brief historical overview of the analog front end followed by the basic digital filter architecture used in the ΣΔ converters.

In the next chapter, Chapter 3, we will discuss disadvantages of conventional ΣΔ architectures and propose a new architecture, a multi-bit ΣΔ converter with nonlinearity correction.

Chapter 4 explains the system simulation used for the analysis throughout this report. Because multi-bit ΣΔ converters are non-linear feedback systems, it is very difficult to

derive analytical expression describing system behavior of the converter. The simulation was extremely helpful in performing in-depth investigation of the entire system.

In Chapter 5, basic performance of the new multi-bit $\Sigma\Delta$ architecture will be presented using the simulation. We will focus primarily on the effects of circuit imperfections on the performance of this architecture. Design criteria and performance requirements of analog sub-circuits will be also presented.

The last chapter, Chapter 6 will give the summary of this report .

Chapter 2

Overview of Oversampled A/D Converters

2.1 Basic Architecture of Digital Signal Processing Systems

The evolution of powerful digital signal processors has proved higher performance to signal processing systems than conventional analog signal processors. Digital signal processors can realize higher resolution, more programmability, and lower cost. Fig. 2.1 shows a basic block diagram of general digital signal processing systems. It consists of a signal acquisition block (analog-to-digital converter, ADC), a digital signal processing block, and a signal output block (digital-to-analog converter, DAC). Although the digital signal processing block is operating in the digital domain, the signal acquisition and signal output block must handle analog signals as inputs and outputs, respectively. These two functional blocks are key elements in the design of high-performance signal processing systems. We will explain the basic functions of each of the functional blocks in Fig. 2.1.

2.1.1 Anti-Aliasing Filter

An analog signal must be sampled in the time domain to be processed with digital signal processors. The sampling process is conversion of an analog signal which is continuous in time and in amplitude to a form discrete in time and continuous in amplitude. According to the sampling theorem, the input signal should be band-limited to avoid aliasing distortion. Otherwise, the input signal cannot be represented by, and recovered from the output of sample-and-hold circuit due to aliasing distortion. The effects of sampling in the time domain and the frequency domain are shown in Fig. 2.1. Suppose the

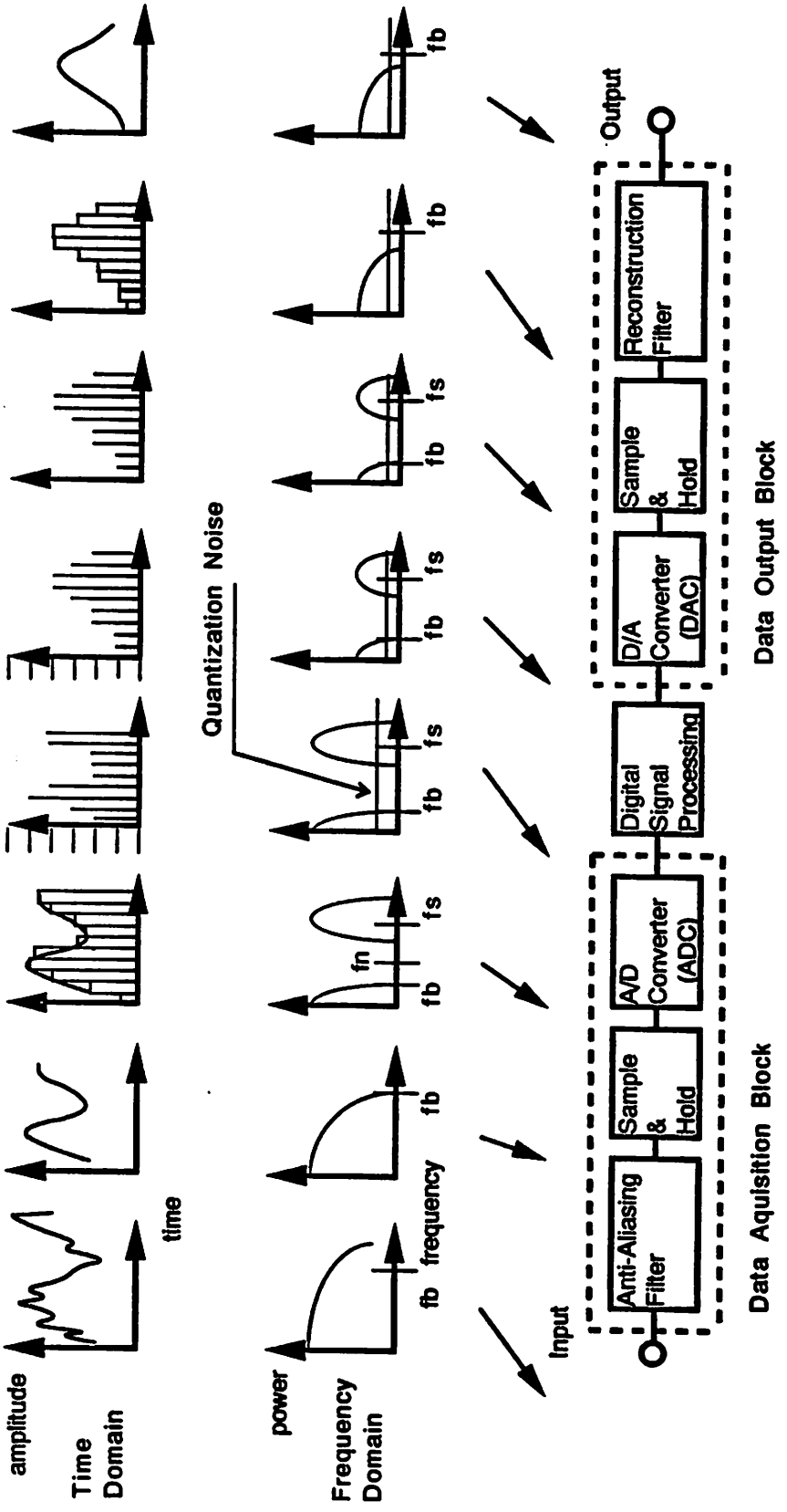


FIGURE 2.1 Basic block diagram of a general digital signal processing system

bandwidth of the input signal is f_b. The sampling frequency f_S must be larger than $2f_b$ to avoid aliasing distortion. The frequency $f_N = 2f_b$ is called the Nyquist rate, and it is the minimum sampling frequency to avoid aliasing distortion. The filter which removes the signal components whose frequency is higher than the bandwidth f_b is called an anti-aliasing filter. If we sample a signal at the Nyquist rate, steepness is required in the transition from passband to stopband in the anti-aliasing filter. The silicon area for this filter is sometimes very large because of this attenuation requirement.

2.1.2 Sample-and-Hold Circuit

This sample-and-hold (S/H) circuit samples the band-limited signal from the anti-aliasing filter. Then, it holds the signal for the following circuit. A continuous-time and continuous-amplitude signal is converted to a discrete-time and continuous-amplitude signal by this circuit.

2.1.3 Analog to Digital Converter

This block converts a discrete-time and continuous-amplitude signal to a discrete-time and discrete-amplitude signal. Because of the amplitude quantization process, quantization noise is added at this stage. There are several kinds of architectures to implement this function. Nyquist rate ADCs are conventional converters, with flash, pipe-lined, successive approximation, and serial ADCs in this category. They sample a signal at the Nyquist rate. Another architecture is the oversampled ADC. It samples a signal at well above the Nyquist rate. The oversampled architecture is the main topic of this report, and will be discussed in depth .

2.1.4 Digital Signal Processor

This digital signal processor is a core block in the system. It performs a variety of digital signal processing to fulfill the given performance specifications. It can realize higher resolution and higher level of programmability than conventional analog signal processors. Thus, it is possible to build a higher-performance and more flexible system using a digital signal processor. Since many powerful digital signal processors and programming software have become available recently, there are more advantages for using digital signal processing over conventional analog signal processing except for specific applications, such as very high-speed systems.

2.1.5 Digital to Analog Converter

Since the output of digital signal processing block is a digital signal, we must convert it to an analog signal to interface with the outside world. This block converts a discrete-time and discrete-amplitude signal to a discrete-time and continuous-amplitude signal. Quantization noise is not added at this stage. There are two major classes of DACs, the Nyquist rate and oversampled converters. The definition of these two converters is the same as for ADCs.

2.1.6 Sample and Hold Circuit

This circuit samples an impulse-train signal from the DAC and hold it for the sampling period. It converts a discrete-time and continuous-amplitude signal to a continuous-time and continuous-amplitude signal. Depending on the order of the hold circuit, the output spectrum of this circuit will be distorted by the hold operation. For example, sinc and sinc^2 functions will be multiplied with the original spectrum in the frequency domain when we use a 0th-order and a 1st-order S/H circuit, respectively.

2.1.7 Reconstruction Filter

The reconstruction filter is a low-pass filter. We can obtain a smooth analog signal in the time domain at this stage. It also must correct the distortion introduced by the preceding S/H circuit.

2.2 Basic Concept of Oversampling

Oversampling basically means sampling at well above the Nyquist rate. The ratio of the sampling frequency to the Nyquist rate is defined as Oversampling Ratio (OSR). ADCs which sample at the Nyquist rate are called the Nyquist rate ADCs. The oversampled ADCs can have the following major advantages over the Nyquist rate converters.

2.2.1 Relaxed Specifications for the Anti-Aliasing Filter

For Nyquist rate ADCs, the sampling frequency f_S is equal to the Nyquist rate f_N. The spectral distribution of an example signal is shown in Fig. 2.2(a). An anti-aliasing filter that has steep attenuation in the transition from passband to stopband (more than bandwidth fb) is required to avoid aliasing distortion. A high-order switched capacitor filter is

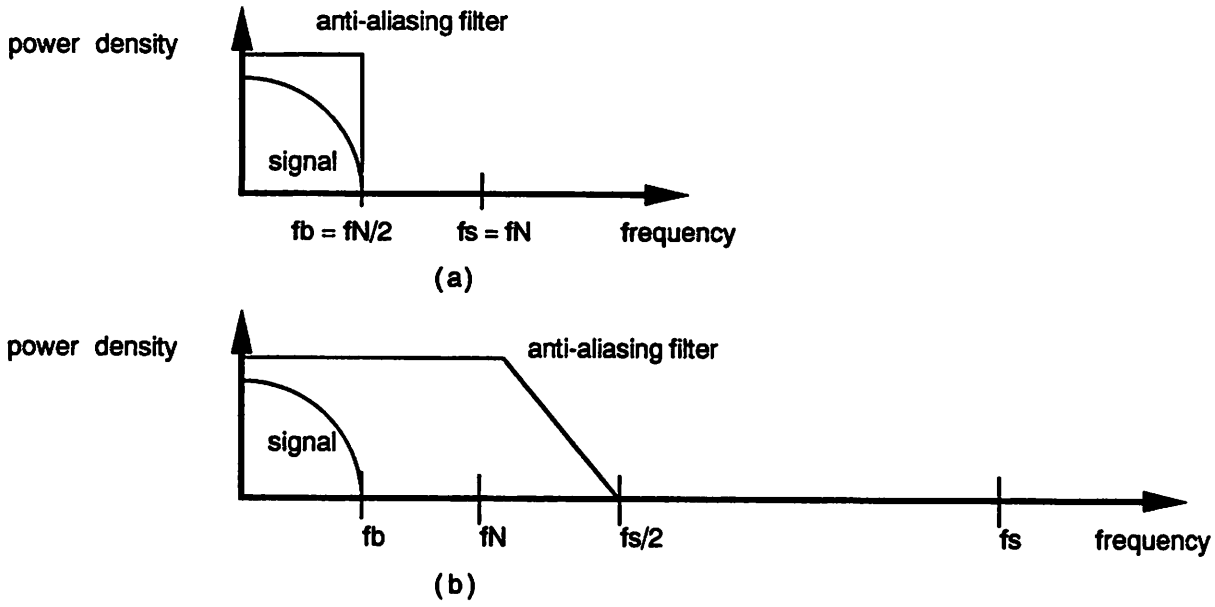


FIGURE 2.2 Spectral distribuiton of signal power and filter response
(a) Nyquist rate ADCs
(b) Oversampled ADCs

required to implement this filter using CMOS technologies which results in large silicon area. This area sometimes becomes the bottleneck to reduce the cost of the chip.

For oversampled ADCs, the sampling frequency f_S is much higher than the Nyquist rate f_N. The spectrum of an example signal is shown in Fig. 2.2(b). In this example, the OSR is nearly equal to three. The passband of the anti-aliasing filter is f_S / 2, and the steepness in the transition from the passband to the stopband (more than f_S / 2) is more relaxed than Nyquist rate converters. We can use a simpler filter, such as a continuous-time RC filter, as the anti-aliasing filter. This leads to a great reduction in the silicon area, and is a major advantage of oversampled ADCs.

2.2.2 Reduction of Quantization Noise of the ADC in the Baseband

The error generated by a scalar quantizer with quantization levels equally spaced by Δa is uncorrelated and its power is given as [17] :

$$E_Q = \frac{\Delta a^2}{12} \qquad F.S. = \text{Full Scale Voltage} \qquad (2.1)$$

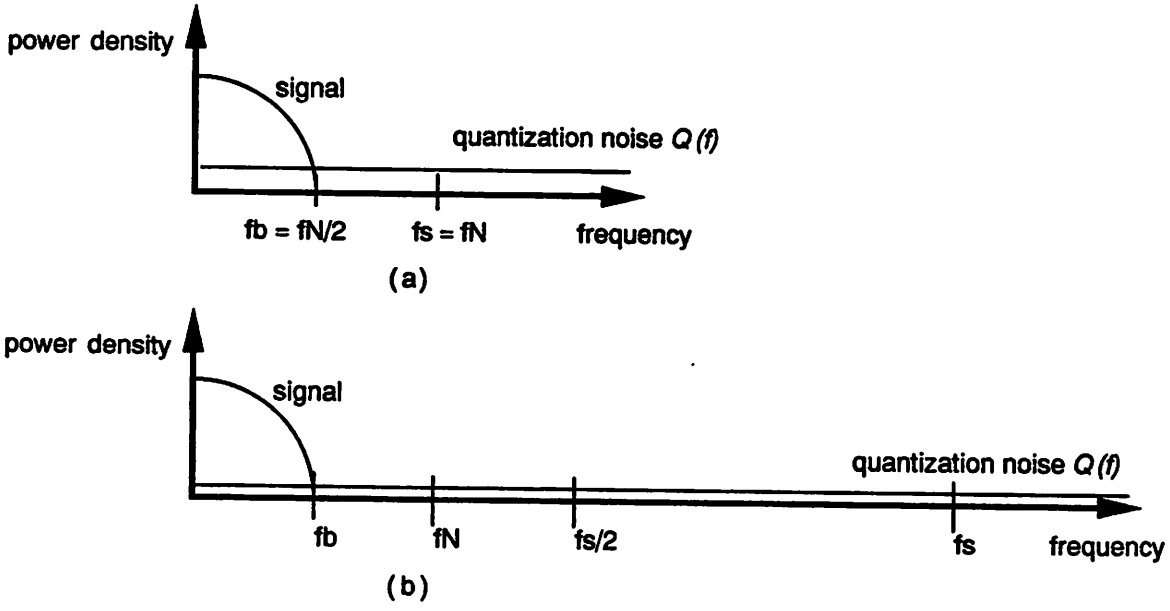


FIGURE 2.3 Spectral distribution of signal and quantization noise power
(a) Nyquist rate ADCs
(b) Oversampled ADCs

$$\Delta a = \frac{F.S.}{2^b} \qquad b = \text{Number of bits of quantizer} \qquad (2.2)$$

given that the number of quantization levels is sufficiently large. The quantization noise $Q(f)$ can be considered as additive white Gaussian noise. The more bits we have, the less the quantization noise $Q(f)$ will be. The spectral distributions of an example signal and the quantization noise $Q(f)$ are shown in Figs. 2.3. For Nyquist rate converters, the quantization noise $Q(f)$ is distributed from dc to $f_S = fN = 2fb$. The signal to noise ratio (SNR) is the ratio of the power of the signal to that of the baseband noise. It is given by the following well-know equation :

$$SNR = (6b + 1.76)\ \text{dB} \qquad (2.3)$$

For oversampled A/D converters, the quantization noise Q is distributed from dc to f_S ($>> fN = 2fb$) as shown in Fig. 2.3 (b). Since the baseband noise is inversely proportional to the oversampling ratio OSR, the SNR of an oversampled A/D converter is much larger than that of a Nyquist rate A/D converter. For example, doubling the OSR provides the increase in the SNR by 3dB (~0.5bit).

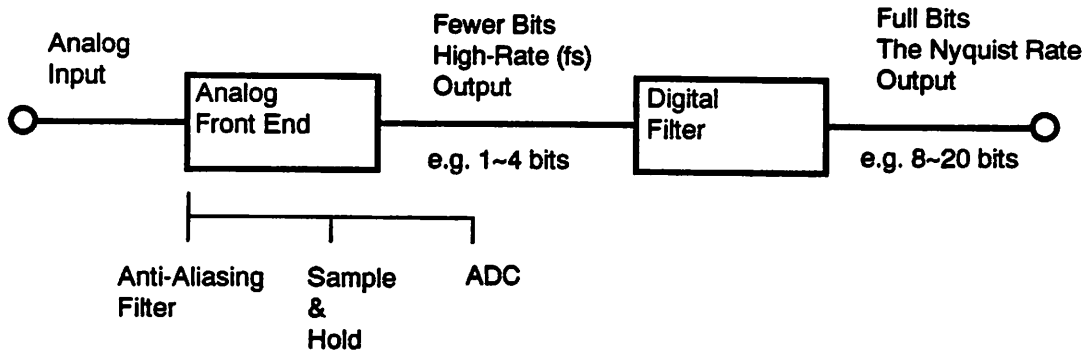


FIGURE 2.4 Basic architecture of oversampled A/D converters

2.3 Basic Architecture of Oversampled A/D Converters

An oversampled ADC consists of an analog front end and a digital filter as shown in Fig. 2.4. The analog front end performs the functions of anti-aliasing filtering, sampling , and A/D conversion. The output of this analog front end is a discrete in time and discrete in amplitude signal sampled at the very high sampling frequency f_S. The digital filter decimates this high frequency signal to the Nyquist rate signal without losing baseband signal information. Conventional digital output at the Nyquist rate can be obtained as final output of the whole system.

2.4 Analog Front End

As mentioned in section 2.2, we can increase the SNR by 3dB by doubling the sampling frequency f_S . However, this increase in the SNR is not sufficient to improve the final resolution of the converter dramatically. In this section, we introduce the concept of quantization noise shaping which results in substantial improvement in the SNR.

2.4.1 First-Order ΣΔ Modulator

We begin with the most basic architecture for noise-shaping oversampled A/D converters [1]. This is called a one-bit ΣΔ modulator and its architecture is shown in Fig. 2.5(a). We have an analog adder, an analog integrator, a one-bit quantizer and a one-bit DAC in the negative feedback loop. (This ΣΔ modulator performs functions of S/H and

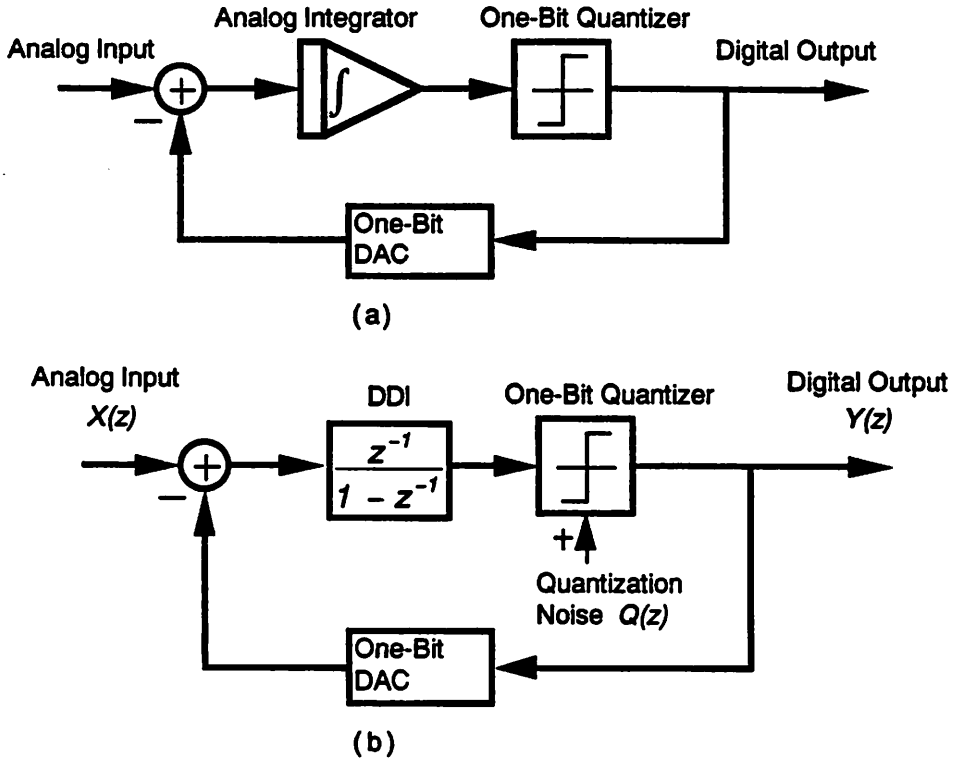


FIGURE 2.5 Block diagram of a first-order ΣΔ modulator
(a) Continuous time domain
(b) Discrete time (sampled-data) domain

ADC in Fig. 2.1. Although the entire analog front end consists of an anti-aliasing filter and a ΣΔ modulator, we focus on the ΣΔ modulator only. The design methodology for anti-aliasing filters can be found in the literature [18,19].)

Since we implement this system as a sampled-data system, this diagram can be converted to the one in Fig. 2.5(b) using z-transform. The analog integrator is replaced by a direct digital integrator (DDI) which contains one clock-delay. We use a comparator as a one-bit quantizer and an analog switch as a one-bit DAC. Since a one-bit quantizer is inherently linear, we do not have to consider the nonlinearity of the quantizer and DAC. We make the following assumptions to make the analysis simple.

(1) Quantization noise *Q(f)* added at the one-bit quantizer is Gaussian white noise.

(2) The system is discrete-time, linear, and time-invariant.

From the Fig. 2.5(b), we can obtain the output signal *Y(z)* as

$$Y(z) = X(z)z^{-1} + (1 - z^{-1})Q(z) \qquad (2.4)$$

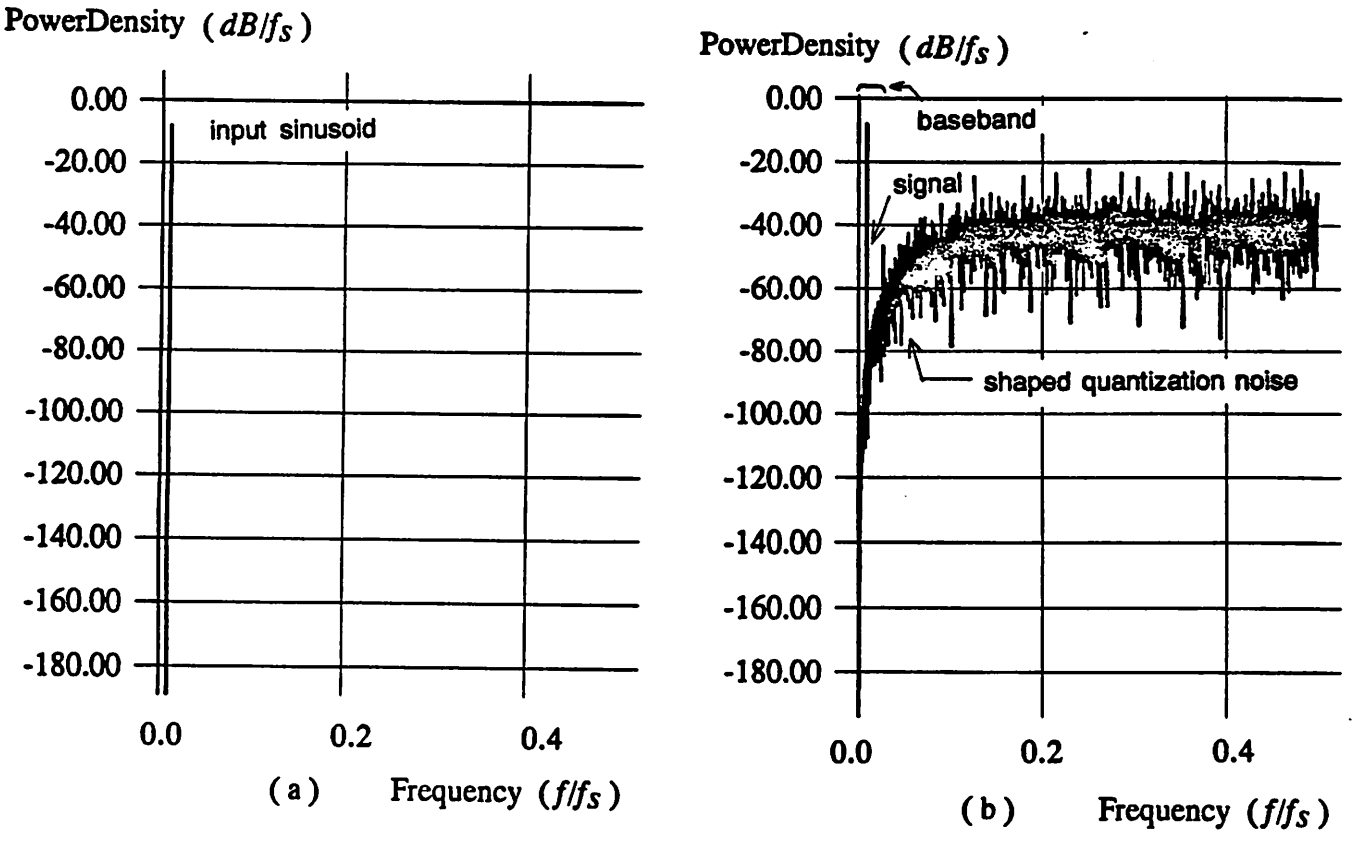


FIGURE 2.6 Spectral distribution of the output signal $Y(z)$
(a) Input spectrum
(b) Output spectrum

$$Y(z) = X(z)H_s(z) + Q(z)H_n(z)$$

Signal Transfer Function : $H_S(z) = z^{-1}$

Quantization Noise Transfer Function : $H_n(z) = (1 - z^{-1})$

Since the signal transfer function $H_S(z) = z^{-1}$ is one clock-delay, the first term $X(z)z^{-1}$ is a one-clock-delayed input signal. The noise transfer function $H_n(z) = (1 - z^{-1})$ is a time-derivative and has effect of high-pass filtering. The second term $(1 - z^{-1})\,Q(z)$ is high-passed quantization noise. As a result, the quantization noise can be attenuated in the baseband. We suppose that an example input is sinusoidal wave. The spectrum is plotted in Fig. 2.6(a). The spectrum of the output signal $Y(z)$ is also shown in Fig. 2.6(b). As can be seen from this figure, we can move the quantization noise $Q(z)$ out of the baseband. This is the reason why this architecture is called a "noise shaping" ADC. The noise shaping results in the increase of the SNR. Time-domain waveforms of the input signal X

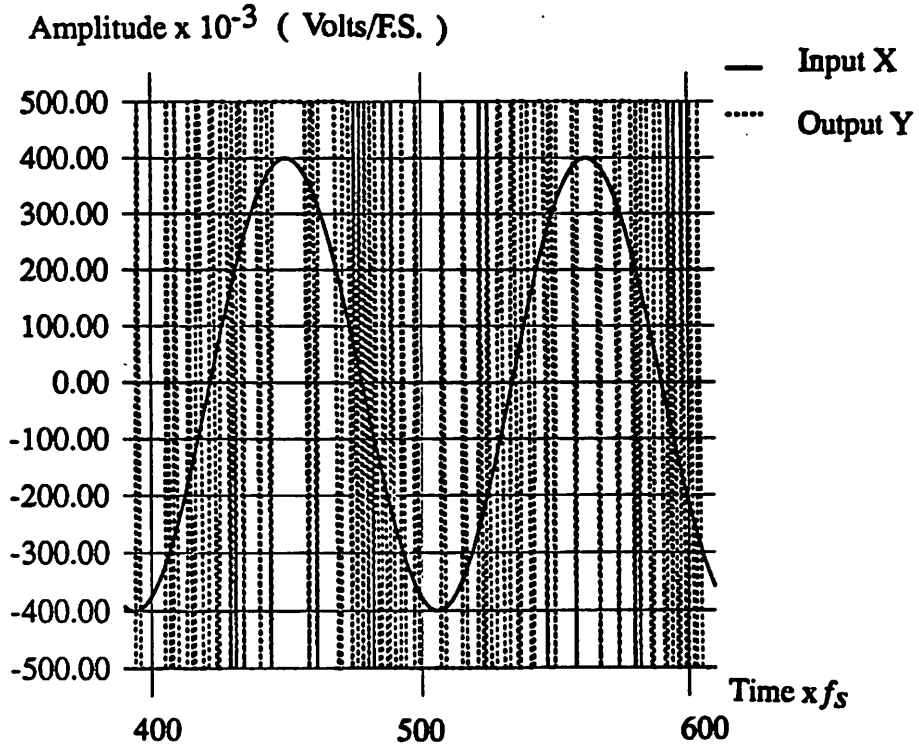


FIGURE 2.7 Time-domain waveforms of signals of a ΣΔ modulator

and the output signal Y are shown in Fig. 2.7. The output Y is a one-bit data stream at the sampling frequency f_S. The ΣΔ feedback loop works so that the time-domain average of the output signal Y is equal to the input signal X. However, very high frequency components are included in the output signal Y. The digital filter must be designed to remove the high frequency out-of-band components.

We calculate the SNR of this converter. First, we calculate the total power of quantization noise in the baseband Q_B^2.

$$Q_0^2(z) = Q^2(z)|H_n(z)|^2 = Q^2(z)|1 - z^{-1}|^2 \qquad (2.5)$$

$$z = e^{j\omega T} \qquad (2.6)$$

$$\bar{Q}_0^2(f) = \frac{(\Delta a)^2}{12}\frac{1}{\frac{f_s}{2}}\left(\sin\pi\frac{f}{f_s}\right)^2 \qquad (2.7)$$

$$\overline{Q_B}^2 = \int_0^{f_b} Q_0^{\,2}(f)\,df = \left(\frac{\Delta a}{\sqrt{12}}\right)^2 \frac{\pi^2}{3}\left(\frac{2f_b}{f_s}\right)^3 \qquad (2.8)$$

$$\therefore \overline{Q_B} = \sqrt{\overline{Q_B}^2} = \frac{\Delta a}{\sqrt{12}}\frac{\pi}{\sqrt{3}}\left(\frac{2f_b}{f_s}\right)^{\frac{3}{2}} \qquad (2.9)$$

Then, we can calculate the maximum signal power S_0^2 for the input amplitude = Δa/2.

$$S_0^{\,2} = \frac{(\Delta a)^2}{8} \qquad (2.10)$$

Hence, we can obtain the following equation for the maximum SNR.

$$\therefore SNR\,|_{max} = \frac{S_0^{\,2}}{\overline{Q_B}^2} = \frac{9}{2\pi^2}\left(\frac{f_s}{2f_b}\right)^3 \qquad (2.11)$$

We can obtain the increase of the SNR by 9dB/oct by doubling the OSR. The noise shaping provides an extra 6dB/oct. in addition to 3dB/oct. of simple oversampling. This modulator is inherently stable. However, it has the problem of tone generation. Because the quantization noise is actually not white but correlated [30,31,32], it introduces dc resonance which results in the tone generation. Dithering is needed to uncorrelate the quantization noise [33,34].

2.4.2 Second-Order ΣΔ Modulator

The performance of a ΣΔ modulator can be enhanced by adding one more feedback loop[7]. This architecture is called a double loop ΣΔ modulator and is shown in Fig. 2.8. We can perform the similar analysis to derive the output and the SNR of this modulator. They are given as :

$$Y(z) = X(z)z^{-2} + (1 - z^{-1})^2 Q(z) \qquad (2.12)$$

$$= X(z)H_s(z) + Q(z)H_n(z)$$

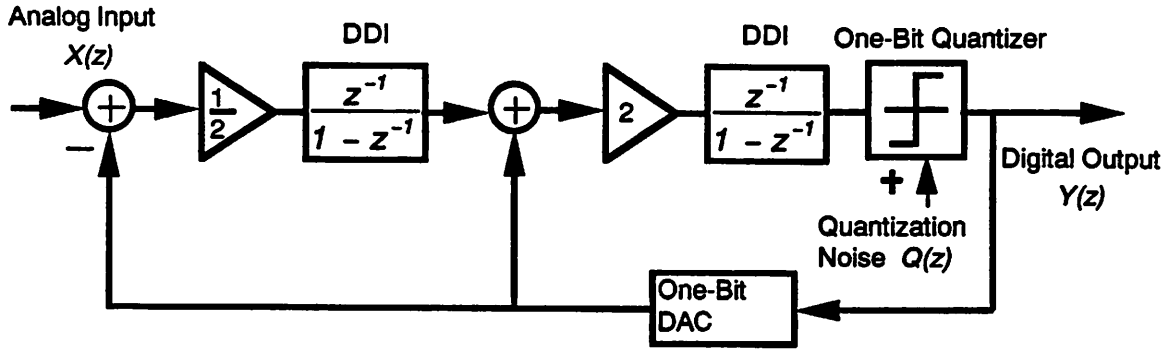


FIGURE 2.8 Block diagram of a second-order ΣΔ modulator

Signal Transfer Function : $H_S(z) = z^{-2}$

Quantization Noise Transfer Function : $H_n(z) = (1 - z^{-1})^2$

$$\overline{Q_B}^2 = \int_0^{f_b} Q_0^2(f)\,df = \left(\frac{\Delta a}{\sqrt{12}}\right)^2 \frac{\pi^4}{5}\left(\frac{2f_b}{f_s}\right)^5 \qquad (2.13)$$

$$SNR|_{max} = \frac{S_0^2}{Q_B^2} = \frac{15}{2\pi^4}\left(\frac{f_s}{2f_b}\right)^5 \qquad (2.14)$$

The noise shaping effect of this modulator is of second order, which results in more reduction of the quantization noise in the baseband. As a result, we can obtain better SNR than a single-loop ΣΔ modulator. From eq.(2.14), the increase of the SNR is 15dB/oct. The noise shaping effect gives us an extra 12dB/oct. in addition to 3dB/oct. of simple oversampling.

We must use digital filters to remove out-of-band quantization noise. The order of the digital filters must be one-order higher than that of a single-loop ΣΔ modulator, because the noise distribution in high frequency is one order higher than that of a single-loop ΣΔ modulator. It requires more complex digital filters which increase the silicon area for the filters.

This system can be stable by careful design [37]. The quantization noise is nearly white and uncorrelated with a double-loop. Therefore, tone generation due to dc resonance is much smaller than that of a single-loop ΣΔ modulator [20]. Dithering is not needed for this modulator.

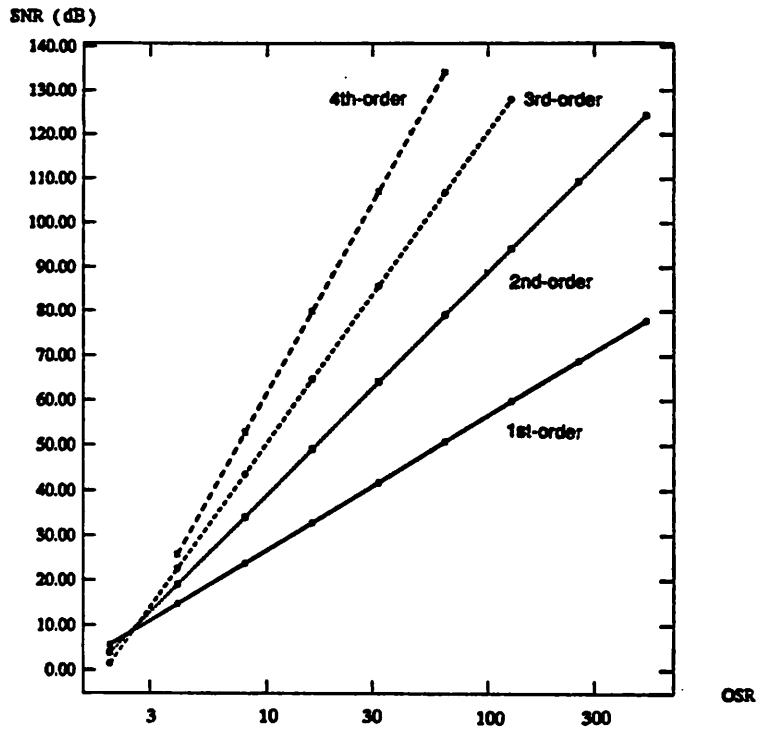


FIGURE 2.9 The signal to noise ratio SNR vs the oversampling ratio OSR

2.4.3 Higher-Order ΣΔ Modulator

Increasing the order of noise shaping is very attractive to get higher SNR. In general, for the n-th order ΣΔ modulators which have the similar transfer functions as those in previous sections, we can calculate the following equation for the maximum SNR of the modulators [20].

$$\therefore SNR|_{max} = \frac{S_0^{\,2}}{Q_B^{\,2}} = \frac{3(2L+1)}{2\pi^{2L}}\left(\frac{f_s}{2f_0}\right)^{2L+1} \qquad (2.15)$$

L = the order of the modulator

The plot of the SNR vs OSR is shown in Fig. 2.9.

However, we cannot use more than two feedback loops in the ΣΔ modulator because such modulators may go unstable. We have two kinds of higher-order architecture to overcome this unstability problem. One is a single path ΣΔ modulator with its transfer

function modified to be stable. Another is a cascade of first-order (single-loop) ΣΔ modulators.

(1) Single Path ΣΔ Modulator

The use of a higher order filter in the negative feedback loop can increase the SNR of the modulator. The general diagram of this architecture is shown in Fig. 2.10 [21]. The critical problem is how we can obtain the stability of the system [21,37]. For example, if we simply use a triple-loop feedback in the ΣΔ modulator, the system goes unstable. Since we have three poles in the transfer function, they give us excessive negative phase shift. We must be careful to design the higher-order filter so that the system will not be unstable. The stability of the modulator depends on the pole positions of the transfer function, overload of a quantizer, and clipping of integrators [21]. The poles must be placed within the unit circle. The overload can be avoided if the input dynamic range is limited to the value smaller than half of the DAC output [21]. The clipping of integrators can be eliminated by scaling of signal levels [13,20,21]. Because of these constraints, the transfer function of this modulator must be modified and the available SNR is not so high as the value obtained by eq.(2.15).

(2) Cascaded ΣΔ Modulator

By cascading first-order (single-loop) ΣΔ modulators, we can obtain higher-order noise-shaping effect. This is called a multi-stage noise shaping (MASH) architecture [11]. The diagram of the third-order system is shown in Fig. 2.11 [22]. Since each block is a first-order ΣΔ modulator, the system is inherently stable. The output signal Y and the SNR are given as :

$$Y(z) = X(z)z^{-3} + (1 - z^{-1})^3 Q(z) \qquad (2.16)$$

$$SNR|_{max} = \frac{S_0^{\,2}}{Q_B^{\,2}} = \frac{21}{2\pi^6}\left(\frac{f_s}{2f_0}\right)^7 \qquad (2.17)$$

given that the gain of each block is perfectly matched. However, gain mismatch between the stages introduces residual quantization noise, which results in the increase of inband noise. Therefore, precisely matched components must be used to obtain high SNR. Dither should be used to solve the problem of tone generation.

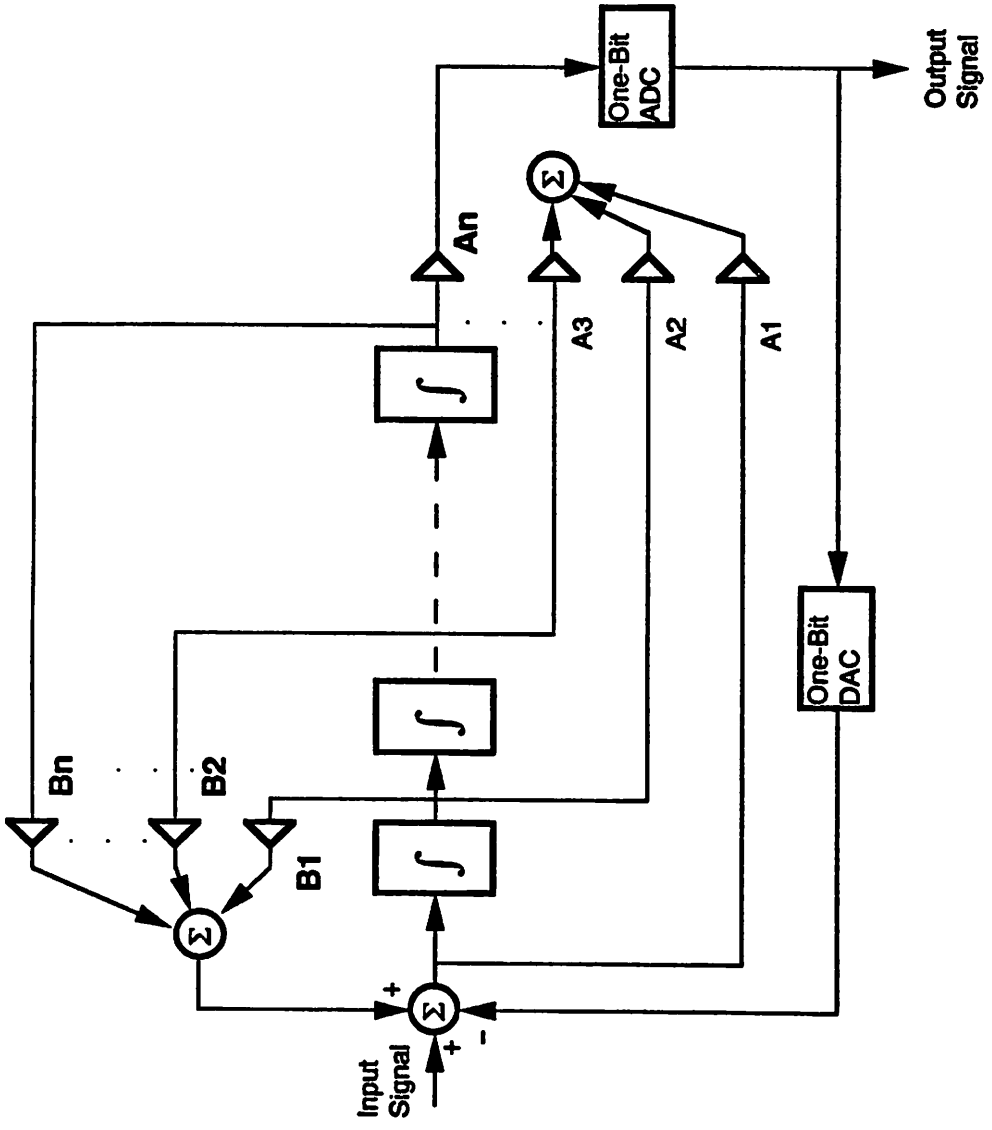


FIGURE 2.10 Block diagram of a single path ΣΔ modulator

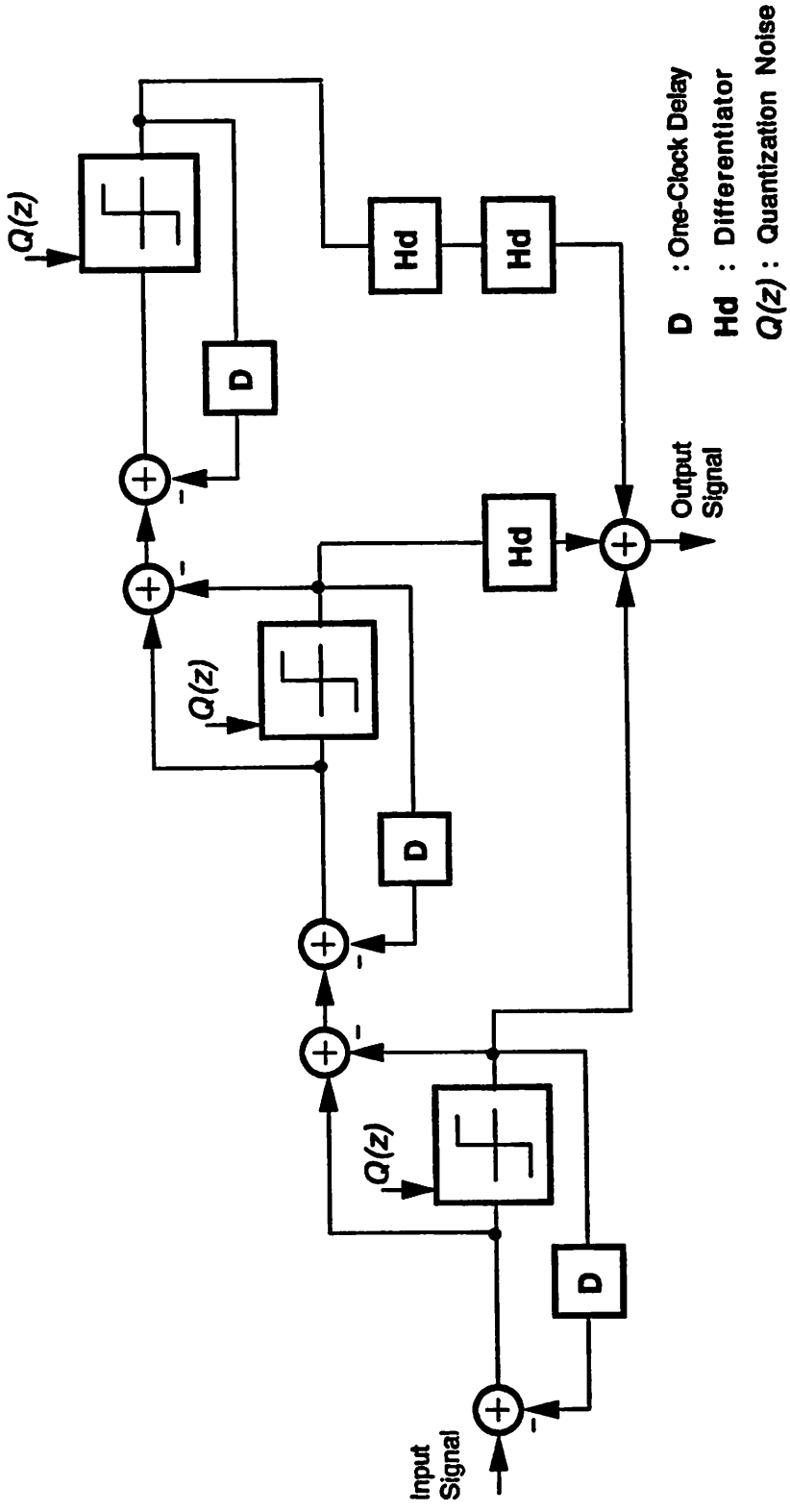


FIGURE 2.11 Block diagram of a third-order cascaded ΣΔ modulator (MASH)

2.4.4 Multi-bit ΣΔ Modulator

We can use a multi-bit quantizer in the feedback loop instead of a one-bit quantizer. A multi-bit quantizer can not only reduce the quantization noise but also stabilize the system [10,23]. It can eliminate the problem of tone generation due to dc resonance [20]. As a result, we can obtain the increase of the SNR by 6dB for every bit added to the quantizer without tone generation and stability problem. It is also known that a multi-bit quantizer can relax overloading problem [24].

The drawback of this architecture is that the SNR is sensitive to the nonlinearity of an internal DAC. The nonlinearity is due to the component mismatch of the DAC. Although Adams [10,36] used accurate external resistors to avoid this problem, this is not a good solution to implement the whole system in a single chip by standard CMOS technologies. Cataltepe [23] proposed a system which uses a memory to correct the nonlinearity digitally. As it requires a programmable memory, such as an EEPROM, it is not a good solution for standard CMOS technologies, either. Carley[24] proposed a multi-bit noise-shaping coder with a dynamically element-matched DAC using an element randomizer. His goal was to convert the error due to the element mismatch from a dc offset into an ac signal of equivalent power which can be partially removed by post filtering. Since the baseband is much smaller than the sampling frequency, this method can greatly improve the SNR of the modulator. In addition, it does not require any external components or special CMOS technologies. However, improvement of the SNR obtained by this scheme is not sufficient to have a major advantage over single-bit ΣΔ modulators.

We propose a new multi-bit ΣΔ architecture to overcome this component mismatch problem in the next chapter. The investigation of the new architecture is a main topic of this report.

2.5 Digital Decimation Filter

We must use digital filters to recover the original information from the output of the analog front end. The key issue in the filter design is how to minimize the silicon area of the filters because the area is usually dominant for the total chip area (more than 80%). There are two goals for the filters.

The first one is the attenuation of the quantization noise outside the baseband. As shown in Fig. 2.6, the quantization noise shaped by the ΣΔ feedback loop is very large at

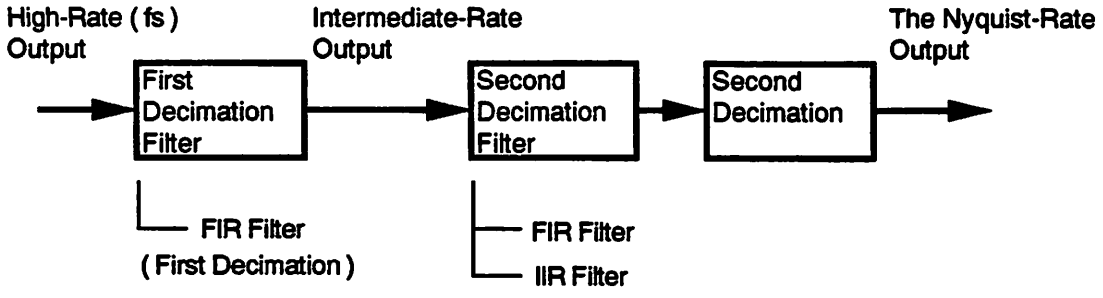


FIGURE 2.12 Block diagram of the digital decimation filter

high frequency. The out-of-band noise must be filtered out to obtain the original information of the baseband signal.

The second one is the decimation of the output rate of the analog front end to the Nyquist rate. Since the output rate of the analog front end is much higher than the Nyquist rate, it should be reduced to the Nyquist rate to be compatible with the conventional post signal processors. The attenuation of the filter around the multiples of decimation frequency must be carefully designed to avoid aliasing distortion by this decimation.

This filter usually can be realized by two stages. Fig. 2.12 shows a basic block diagram of the filter. The first filter has functions of attenuation of the out-of-band quantization noise, the first decimation and prevention of aliasing distortion due to the decimation. The transfer function in the baseband is slightly distorted by this filtering. The second one has functions of prevention of aliasing distortion due to the second decimation and reshaping of the transfer function in the baseband distorted by the first filter.

For the first decimation filter, we can use a cascade of sinc filters [7]. The order of this filter should be larger than that of the noise shaping of the analog front end. Since this filter can be implemented by an FIR filter, the output of this filter can be calculated at the downsampled frequency instead of the original very high sampling frequency.

For the second digital filter, an FIR or an IIR architecture can be used depending on the performance specifications of the applications. Because sampling rate is greatly reduced at this stage, it is possible to implement a high-order filter with modest silicon area. Steep attenuation of the quantization noise and fine-tuning for reshaping of the transfer function in the baseband can be done without difficulty.

By performing the second decimation, the final Nyquist-rate output can be obtained.

Chapter 3

Multi-bit Oversampled A/D Conversion

3.1 Introduction

The single-bit second-order ΣΔ A/D architecture is very attractive for medium-speed, high-resolution conversion (e.g. 14 bits, 80ksamples/sec. for 1.75μm CMOS technology [15]) and many systems with this architecture have become available recently [6,8,13,15,16]. However, its performance is not sufficient to obtain faster and higher-resolution conversion. Another architecture whose SNR for the same sampling frequency is much larger than that of the second-order ΣΔ modulator is needed to improve the operation speed and the resolution of ADCs.

In this chapter, we propose a new architecture of a multi-bit ΣΔ modulator to improve the SNR of the modulator. We introduce the dynamic barrel shifting of internal D/A unit elements to reduce the nonlinearity of an internal DAC. We can obtain higher SNR with this new architecture than a single-bit second-order ΣΔ converter for the same OSR. In addition, the SNR obtained by this architecture is higher than that of a multi-bit ΣΔ converter with a randomizer proposed by Carley [24]. Therefore, this is a good candidate for multi-bit ΣΔ architecture.

As mentioned in Chapter 2, an oversampled A/D system consists of the analog front end and digital decimation filters. However, we will discuss only the analysis and design of the analog front end focusing on the aspects of analog circuit issues in this report. The design method of the digital filters is distinctly different topic and there are several good references for this issue [25,26,27].

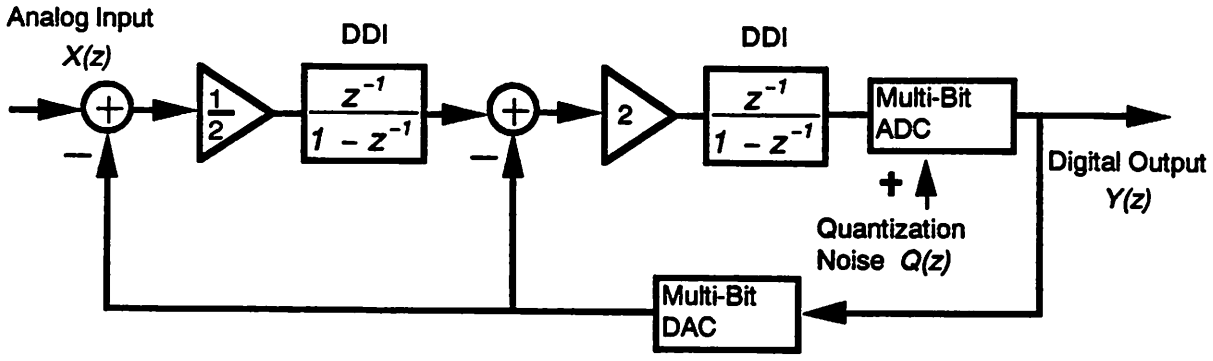


FIGURE 3.1 Block diagram of a multi-bit second-order ΣΔ modulator

3.2 Architecture of the New Multi-Bit ΣΔ ADC

A block diagram of this multi-bit ADC is shown in Fig. 3.1. We use a double loop ΣΔ architecture. It consists of two analog integrators, two analog adders, one multi-bit ADC and one multi-bit DAC. We chose the number of bits of the internal ADC and DAC to be four, which ideally results in the increase of the SNR by an extra three bits. The output of this modulator is a four-bit high rate data stream. This signal must be decimated and filtered by post filters as discussed in the previous chapter.

The structures of four-bit ADC and DAC are quite different from those of one-bit ADC and DAC. For a four-bit ADC, we use a four-bit flash ADC. As the number of unit elements required for four bits is fifteen, the silicon area for this ADC is reasonable. The output of this quantizer is a thermometer-code signal. Because this ADC is embedded in the forward path of the feedback loop, the nonlinearity of this ADC is shaped in the frequency domain as the quantization noise. As a result, the effect of the nonlinearity is much smaller than that of an internal DAC. Thus, we neglect the nonlinearity of the ADC in this analysis.

The key issue of the design of this modulator is how we can minimize the effect of nonlinearity of an internal DAC. Since the input of this DAC is thermometer code, we can use unit element switching D/A architecture. We apply dynamic barrel shifting allocation to the unit elements to reduce the nonlinearity. Discussion on this dynamic allocation is presented in the next section.

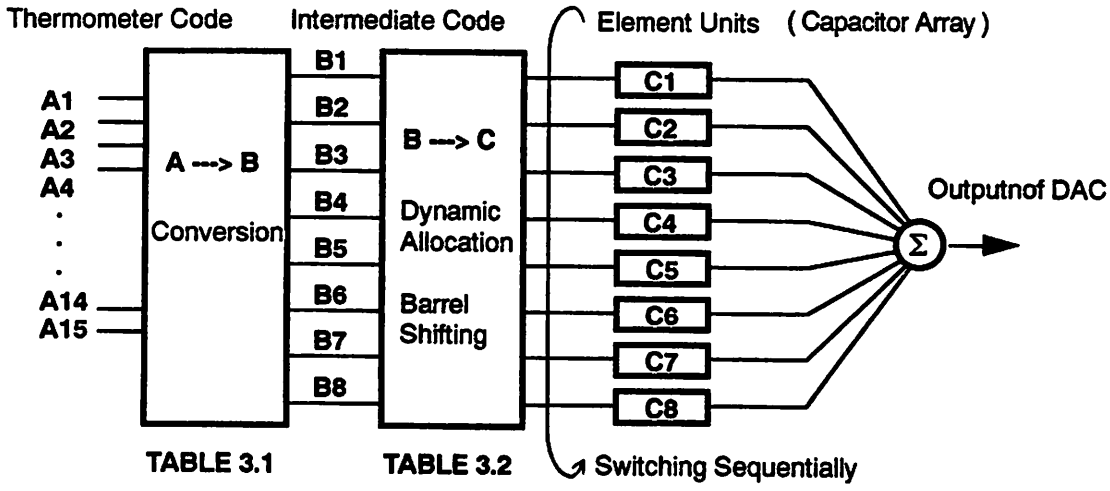


FIGURE 3.2 Block diagram of dynamic allocation of an internal DAC

3.3 Dynamic Barrel Shifting of D/A Unit Elements

3.3.1 Allocation Sequence

We use a capacitor array $C_{1\text{-}8}$ for the unit elements. The nonlinearity is generated by mismatch of the unit capacitors $C_{1\text{-}8}$ due to the local variation of manufacturing process. We apply dynamic barrel shifting allocation of the unit elements in the DAC to reduce the nonlinearity. A block diagram of this circuit is shown in Fig. 3.2. We define the thermometer-code outputs of the ADC as $A_{1\text{-}15}$, the intermediate code as $B_{1\text{-}8}$, and the corresponding unit elements of the DAC as $C_{1\text{-}8}$, respectively. The relationship between the thermometer code $A_{1\text{-}15}$ and the intermediate code $B_{1\text{-}8}$ is shown in Table 3.1. Since we use three levels (-1,0,1) for the intermediate code $B_{1\text{-}8}$, just eight unit elements $C_{1\text{-}8}$ are sufficient to express sixteen different levels. In other words, we use combination of a polarity switch (-1,0,1) and a three-bit DAC (eight levels) to express four-bit levels at the unit-element stage. In CMOS circuit implementation, the intermediate codes -1 and +1 correspond to the charging of the unit capacitor to $-V_{ref}$ and $+V_{ref}$, respectively. The code 0 corresponds to the opening of the capacitor. The dynamic allocation between the intermediate code $B_{1\text{-}8}$ and unit elements $C_{1\text{-}8}$ is performed by barrel shifting. The allocation sequence is shown in Table 3.2. For every clock period, the allocation changes sequentially. For example, the output of the DAC is given as $B_1C_1 + B_2C_2 + B_3C_3 + \ldots + B_8C_8$ for CLK 1. Therefore, eight clock-delays are needed to perform one period of the

Analog Levels	Thermometer Code $A_{1\text{-}15}$ 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	Intermediate Code $B_{1\text{-}8}$ 1 2 3 4 5 6 7 8
-15/16	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	-1 -1 -1 -1 -1 -1 -1 -1
-13/16	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	-1 -1 -1 -1 -1 -1 -1 0
-11/16	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	-1 -1 -1 -1 -1 -1 0 0
-9/16	1 1 1 0 0 0 0 0 0 0 0 0 0 0 0	-1 -1 -1 -1 -1 0 0 0
-7/16	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	-1 -1 -1 -1 0 0 0 0
-5/16	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0	-1 -1 -1 0 0 0 0 0
-3/16	1 1 1 1 1 1 0 0 0 0 0 0 0 0 0	-1 -1 0 0 0 0 0 0
-1/16	1 1 1 1 1 1 1 0 0 0 0 0 0 0 0	-1 0 0 0 0 0 0 0
+1/16	1 1 1 1 1 1 1 1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
+3/16	1 1 1 1 1 1 1 1 1 0 0 0 0 0 0	1 0 0 0 0 0 0 0
+5/16	1 1 1 1 1 1 1 1 1 1 0 0 0 0 0	1 1 0 0 0 0 0 0
+7/16	1 1 1 1 1 1 1 1 1 1 1 0 0 0 0	1 1 1 0 0 0 0 0
+9/16	1 1 1 1 1 1 1 1 1 1 1 1 0 0 0	1 1 1 1 0 0 0 0
+11/16	1 1 1 1 1 1 1 1 1 1 1 1 1 0 0	1 1 1 1 1 0 0 0
+13/16	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	1 1 1 1 1 1 0 0
+15/16	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 0

Note : (i) Analog levels indicate the ratio to the full scale voltage of ADC
(ii) Intermediate code : +1 -> $+V_{ref}$,-1 -> $-V_{ref}$ and 0 -> open-circuit

TABLE 3.1 Relation between the thermometer code $A_{1\text{-}15}$ and the intermediate code $B_{1\text{-}8}$

Intermediate Code $B_{1\text{-}16}$	CLK 1	CLK 2	CLK 3	CLK 4	CLK 5	CLK 6	CLK 7	CLK 8
B_1	C_1	C_8	C_7	C_6	C_5	C_4	C_3	C_2
B_2	C_2	C_1	C_8	C_7	C_6	C_5	C_4	C_3
B_3	C_3	C_2	C_1	C_8	C_7	C_6	C_5	C_4
B_4	C_4	C_3	C_2	C_1	C_8	C_7	C_6	C_5
B_5	C_5	C_4	C_3	C_2	C_1	C_8	C_7	C_6
B_6	C_6	C_5	C_4	C_3	C_2	C_1	C_8	C_7
B_7	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_8
B_8	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1

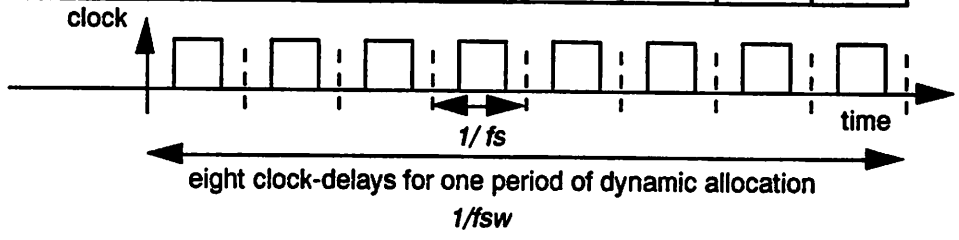


TABLE 3.2 Dynamic allocation sequence ($B_{1\text{-}8}$ to $C_{1\text{-}8}$) of D/A unit element code

allocation. We define the frequency corresponding to this allocation period (eight clock-delays) as the allocation switching frequency f_{sw}.

3.3.2 Effects of the Dynamic Allocation

(1) Analysis of effects

Block diagrams of this ΣΔ modulator with the D/A nonlinearity are shown in Figs. 3.3. Fig. 3.3(a) shows the original diagram. Fig. 3.3(b) shows the diagram in which the nonideal D/A converter is replaced by an ideal D/A converter with two nonlinearity sources N_1 and N_2 added. The transfer function of the modulator in Fig. 3.3(b) is given as :

$$Y(z) = (X(z) + N_1(z))z^{-2} + N_2(z)(1 - z^{-1})z^{-1} + Q(z)(1 - z^{-1})^2 \qquad (3.1)$$

Signal Transfer Function : $H_S(z) = z^{-2}$

Quantization Noise Transfer Function : $H_n(z) = (1 - z^{-1})^2$

Nonlinearity N_1 Transfer Function : $H_{n1}(z) = z^{-2}$

Nonlinearity N_2 Transfer Function : $H_{n2}(z) = (1 - z^{-1})z^{-1}$

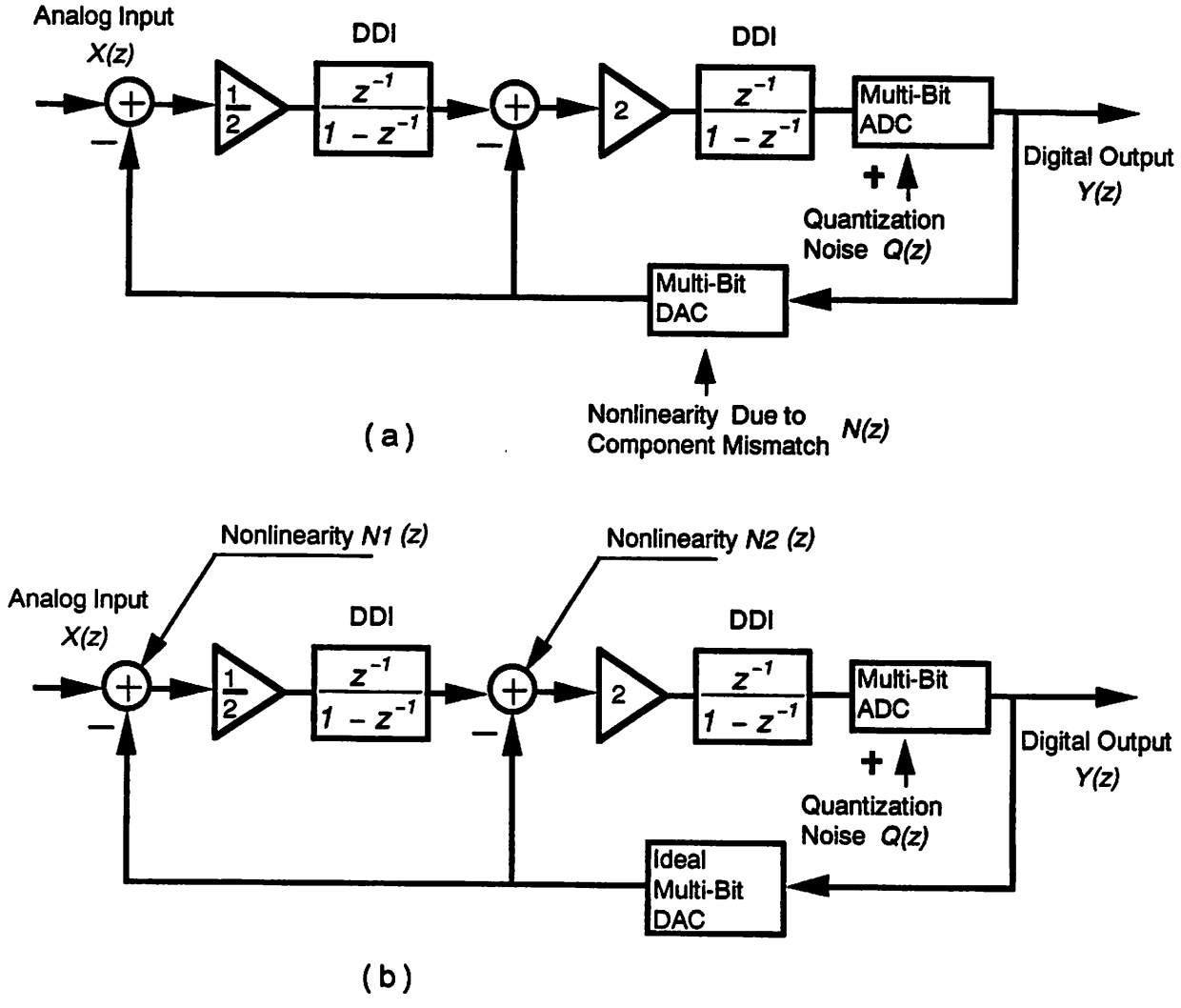


FIGURE 3.3 Block diagrams of a multi-bit second-order ΣΔ modulator with nonlinearity
(a) Original diagram
(b) Diagram with an ideal DAC and two nonlinearities

Since D/A nonlinearity is directly added to the adder 1 as the nonlinearity N_1, N_1 cannot be distinguished from the original signal. It degrades the SNR of this modulator. Because the nonlinearity N_2 is in the feedback loop, it is subjected to the first-order noise shaping. As a result, the effect of N_2 added to the adder 2 is much smaller. Therefore, we consider only the effect of N_1.

For simplicity, we begin with an open loop system which consists of a cascade of an ADC and a DAC. We examine the effect of the mismatch shown in Fig. 3.4.

We consider the following five cases.

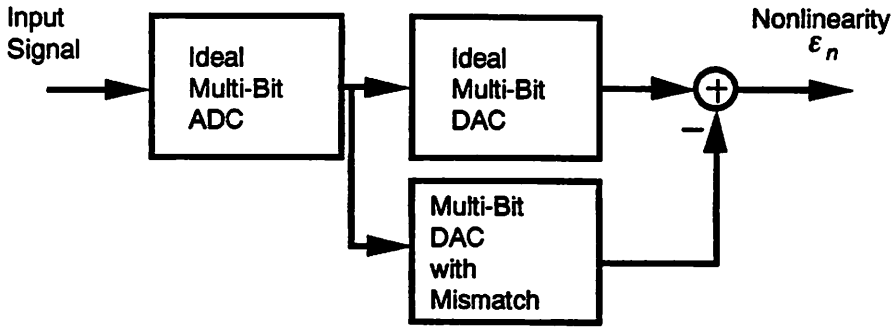


FIGURE 3.4 Cascade of an ADC and a DAC

(i) DC input and no mismatch

Since the input is a dc signal, the intermediate codes $B_{1\text{-}8}$ are constant. The capacitors are perfectly matched. It means that

$$C[1] = C[2] = \ldots = C[8] = C_0 \qquad (3.2)$$

where C_0 is a nominal capacitor value. Discrete-time output signal y[n] is given as :

$$y[n] = \sum_{m=1}^{8} B[m]C[m] \qquad 1 \le n \le 8 \qquad (3.3)$$

where $B[m]$ is the intermediate code and $C[m]$ is the unit capacitor value. Combining eq.(3.2) and eq.(3.3) gives us

$$y[n] = C_0 \sum_{m=1}^{8} B[m] = C_{sig} \qquad (3.4)$$

This C_{sig} is a desired output signal. The power spectrum of the C_{sig} appears at dc as shown in Fig.3.5 (a).

(ii) DC input, mismatch and no barrel shifting

Since we have capacitor mismatch, the capacitor values are given as :

$$C[m] = C_0 + \Delta C[m] \qquad 1 \le n \le 8 \qquad (3.5)$$

where $\Delta C[m]$ is a mismatch for each capacitor. Output signal y[n] is given as :

$$y[n] = \sum_{m=1}^{8} B[m]C[m] \qquad 1 \le n \le 8$$

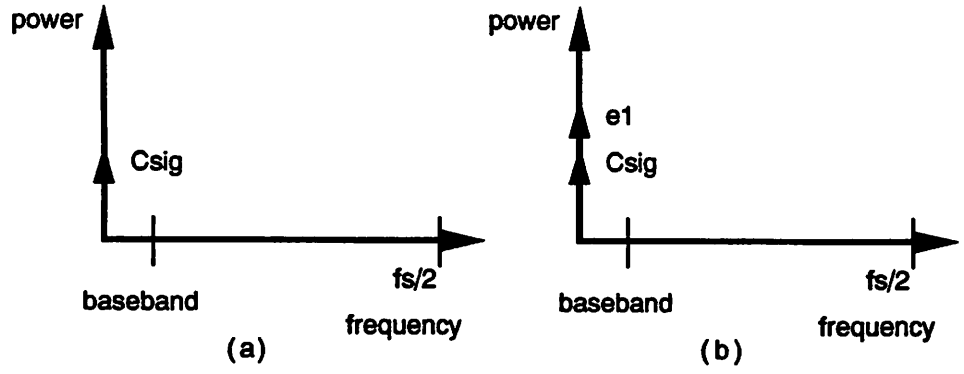


FIGURE 3.5 Spectrum of the output
(a) DC input and no mismatch
(b) DC input , mismatch and no barrel shifting

$$y[n] = \sum_{m=1}^{8} B[m]\,(C_0 + \Delta C[m]) \qquad (3.6)$$

$$= C_0 \sum_{m=1}^{8} B[m] + \sum_{m=1}^{8} B[m]\,\Delta C[m] \qquad (3.7)$$

$$= C_{sig} + e_1 \qquad (3.8)$$

where $$e_1 = \sum_{m=1}^{8} B[m]\,\Delta C[m]$$

e_1 is an error due to the mismatch. It also appears at dc as shown in Fig. 3.5 (b).

(iii) DC input, mismatch and use of barrel shifting

We apply the barrel shifting to push the error due to the nonlinearity out of the base band. The output is given as :

$$y[n] = \sum_{m=1}^{8} B[m]\,C[(n+m)_8] \qquad 1 \le n \le 8 \qquad (3.9)$$

$$= \sum_{m=1}^{8} B[(-m)_8]\,C[(n-m)_8] \qquad (3.10)$$

where $(\,)_8$ is modulo 8. Substituting $B[(-m)8] = D[(m)8]$, eq.(3.8) can be rewritten as :

$$y[n] = \sum_{m=1}^{8} D[(m)_8]\,C[(n-m)_8] \qquad (3.11)$$

$$= D[n] \otimes C[n] \qquad (3.12)$$

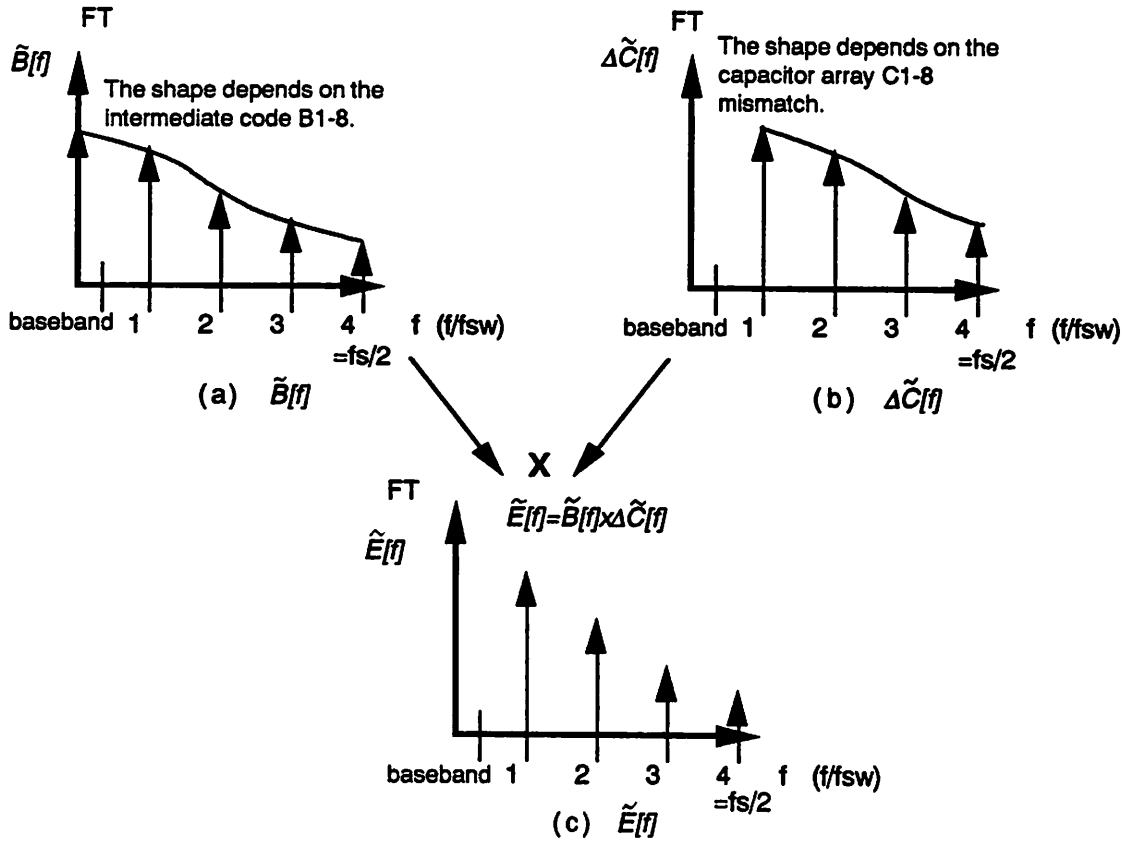


FIGURE 3.6 Spectrum of the output for dc input, mismatch and barrel shifting

where ⊗ denotes 8-point circular convolution. From eq.(3.5), we can obtain

$$y[n] = C_0 \sum_{m=1}^{8} D[(m)_8] + D[n] \otimes \Delta C[n] \qquad (3.13)$$

$$= C_{sig} + e[n] \qquad (3.14)$$

where $C_{sig} = C_0 \sum_{m=1}^{8} D[(m)_8]$, $e[n] = D[n] \otimes \Delta C[n]$

e[n] is an error due to the mismatch. Therefore, the 8-point Fourier transform (FT) of the error e[n], $\tilde{E}[f]$ becomes

$$|\tilde{E}[f]| = |\tilde{D}[f]\,\Delta\tilde{C}[f]| \qquad (3.15)$$

$$= |\tilde{B}[f]\,\Delta\tilde{C}[f]| \qquad (3.16)$$

where $\tilde{B}[f]$,$\tilde{D}[f]$, and $\Delta\tilde{C}[f]$ are FT of $B[n]$,$D[n]$, and $\Delta C[n]$, respectively.

The shape of $\tilde{B}[f]$ depends on a pattern of $B_{1\text{-}8}$. The shape of $\Delta\tilde{C}[f]$ is determined by the spatial distribution of capacitor values $C_{1\text{-}8}$. Suppose that we have $\tilde{B}[f]$ and $\Delta\tilde{C}[f]$ as shown in Figs. 3.6(a) and (b), respectively. An error spectrum due to the mismatch is given by eq.(3.16) as shown in Fig. 3.6(c). In the next section, we will verify this result by simulations.

(iv) Sinusoid input, mismatch and use of barrel shifting

Since the input is a dynamic signal, the intermediate code $B[m]$ changes in the time domain. The analysis is not so simple as compared with the former cases. We make bold guess about the effect of the nonlinearity using some assumptions. Then we will use simulation to verify this guess.

Suppose that the input signal frequency is f_{sig}. This frequency f_{sig} is much smaller than the switching frequency f_{sw}. We can consider that the output $y[n]$ is given as :

$$y[n] = \sum_{m=1}^{8} B(m,n) C[(n+m)_8] \tag{3.17}$$

Using eq.(3.5), we can get

$$y[n] = \sum_{m=1}^{8} B(m,n)(C_0 + \Delta C[(n+m)_8] \tag{3.18}$$

$$= C_0 \sum_{m=1}^{8} B(m,n) + \sum_{m=1}^{8} B(m,n)\Delta C[(n+m)_8] \tag{3.19}$$

$$= C_{sin} + e_{sin}[n] \tag{3.20}$$

where $$C_{sin} = C_0 \sum_{m=1}^{8} B(m,n) \quad , \quad e_{sin}[n] = \sum_{m=1}^{8} B(m,n)\Delta C[(n+m)_8] \tag{3.21}$$

C_{sin} is a desired signal, $e_{sin}[n]$ is an error due to the mismatch, and $B(m,n)$ are time-dependent intermediate codes. Since the period of the codes $B(m,n)$ is f_{sig}, its FT is given as shown in Fig. 3.7(a). FT of $\Delta C[n]$ is shown in Fig. 3.6(b). $\Delta C[n]$ is periodic and its fundamental frequency is f_{sw} . It is complex to derive accurate FT of $e_{sin}[n]$ by hand analysis. However, intuitively we can expect the FT of $e_{sin}[n]$ to have the following form from eq.(3.21)

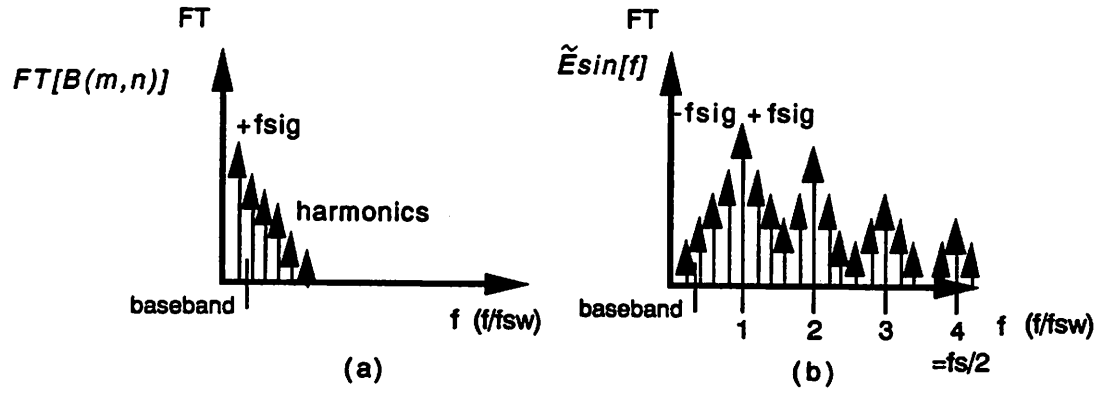


FIGURE 3.7 Spectrum of the sinusoid input, mismatch and barrel shifting
(a) $FT[B(m,n)]$
(b) $\tilde{E}sin[f]$

$$E_{sin}[f] = K_1 f_{sw} + K_2 f_{sig} \qquad (3.22)$$

where K_1 and K_2 are integers. Hence , the FT can be expected as shown in Fig. 3.7(b).

(v) Practical input, mismatch and use of barrel shifting

In practice, the input signal of the DAC is the output signal of the ADC which contains the quantization noise as shown in fig. 3.8(a). It is convoluted with $\tilde{E}[f]$, which will result in the nonlinearity distributed around the multiples of the frequency f_{sw} as shown in Fig. 3.8(b). The simulation will verify this result in the next section.

(2) Comparison with other dynamic allocation methods

There are some other ways to apply dynamic allocation of unit elements.

One is randomization proposed by Carley [24]. Although it can reduce the baseband noise due to the nonlinearity, the improvement of the SNR is expected to be worse than the barrel shifting. This is because the barrel shifting can push the noise out of the baseband, while the randomization simply whitens the noise. The comparison between these two methods by simulation will be presented in the next section.

Another way may be the use of different allocation switching frequency for this capacitor array $C_{1\text{-}8}$. For example, we may use $f_{sw} = f_{sig} / 2$. In this case, we have only two sets of the allocation like :

For CLK1,

$B_1 \rightarrow C_1, B_2 \rightarrow C_2, B_3 \rightarrow C_3, B_4 \rightarrow C_4, B_5 \rightarrow C_5, B_6 \rightarrow C_6, B_7 \rightarrow C_7, B_8 \rightarrow C_8$

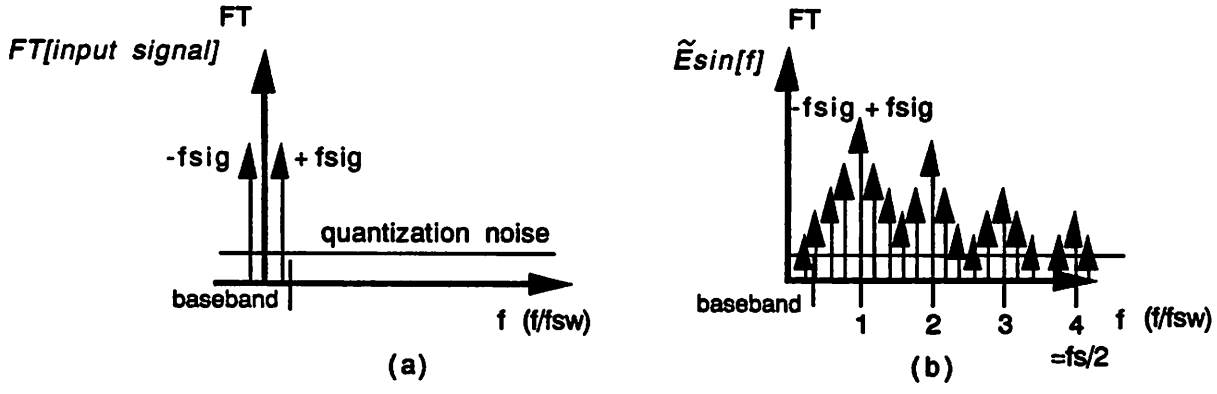


FIGURE 3.8 Spectrum of the practical input, mismatch and barrel shiting
(a) *FT[input signal]*
(b) $\tilde{E}sin[f]$

For CLK2,

B_1 -> C_5, B_2 -> C_6, B_3 -> C_7, B_4 -> C_8, B_5 -> C_1, B_6 -> C_2, B_7 -> C_3, B_8 -> C_4

Suppose that the dc input = 1/8. From Table 3.1, we can obtain the intermediate codes as follows :

$B_1=1$, $B_2=0$, $B_3=0$, $B_4=0$, $B_5=0$, $B_6=0$, $B_7=0$, $B_8=0$

Therefore, we use only two capacitors C_1 and C_5 for this input. On the other hand, we use eight capacitors $C_{1\text{-}8}$ if we use the dynamic barrel shifting ($f_{sw} = f_s$ /8) for the same input. Since the mismatch of capacitor values is a random process, the use of more capacitors to express the signal can result in smaller variance of the output signal. Specifically, if $C_{1\text{-}8}$ are independent, identically distributed (iid) random variables, then the expected deviation of $(C_1+ C_2+ C_3 +...+ C_8)/8$ from 1 is smaller than that of $(C_1+ C_2)/2$. Thus, we can expect that the switching frequency f_{sw} of f_s /8 (the barrel shifting) is a better candidate for the dynamic allocation than other switching frequencies.

3.3.3 Simulation of a DAC with Dynamic Allocation

A. Simulation Model

We developed a system-level C-code program to simulate the model in Fig. 3.4. This program simulates the open-loop system which consists of a cascade of an ADC and a DAC. The nonlinearity ε_n due to component mismatch in Fig. 3.4 can be obtained by this simulator. A complete system simulation for the whole ΣΔ modulator which includes the DAC in the feedback loop will be presented in the following chapter.

*	Full scale voltage	:	1.0 Volt
*	Number of bits of an internal quantizer	:	4
*	Sampling frequency	:	fs
*	Nyquist rate	:	fs x *146/8192*
*	Signal frequency (sinusoid)	:	fs x *73/8192*
*	Signal amplitude	:	0.5 Volts (-6dB)
*	Fast Fourier Transform		
	Window	:	First-order Hanning window
	Number of points	:	8192

TABLE 3.3 Basic specifications of this simulation

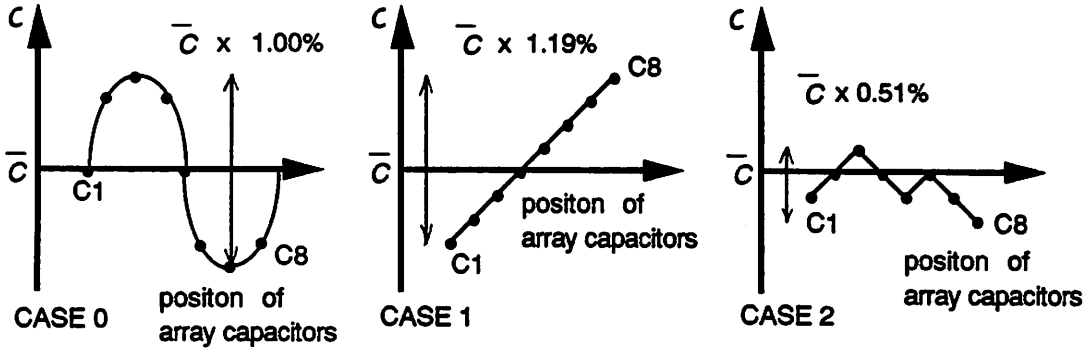


FIGURE 3.9 Three models of spatial distribution of unit-element values used in the simulation

Basic specifications used in this simulation are shown in Table 3.3. FFT with the Hanning window is used to obtain the spectral density distribution. We will discuss the choice of the window in section 4.3.2.

Since component mismatch is a random process, we must perform some statistical simulation to include this random process. However, we used the following three models of spatial distribution of unit-element values for simplicity. Figs. 3.9 show each model. We think these three models are sufficient to get the intuition of the effect of the dynamic allocation. In chapters 4 and 5, we will use the Monte Carlo method to simulate system behavior of the ΣΔ modulator in detail.

B. Simulation Results

(1) Verification of our analysis

(i) DC input, mismatch and use of barrel shifting

We examine the spectrum of the output for CASE 1. The spectrum of the nonlinearity ε_n for dc input = 0.5 volts and 0.15 volts are shown in Fig. 3.10(a) and (b). For input = 0.5 volts, the intermediate codes are given from Table 3.1 as :

$B_1=1, B_2=1, B_3=1, B_4=1, B_5=0, B_6=0, B_7=0, B_8=0$

Therefore, the even-order spectrum of FT $\tilde{B}[f]$ is null. This makes the even-order spectrum of FT $\tilde{E}[f]$ equal to zero as shown in Fig. 3.10(a). For input = 0.15 volts, the intermediate codes are

$B_1=1, B_2=0, B_3=0, B_4=0, B_5=0, B_6=0, B_7=0, B_8=0$

We have both even-order and odd-order spectrum of FT $\tilde{B}[f]$. Thus, we obtain the spectrum of FT $\tilde{E}[f]$ as shown in Fig. 3.10(b). These results are in good agreement with our analysis.

(ii) Sinusoid input, mismatch and use of barrel shifting

The nonlinearity spectrum of CASE 0, CASE 1 and CASE 2 for sinusoid input are shown in Figs. 3.11. The input amplitude is 0.5 volts. From these figures, it can be seen that the nonlinearity is distributed around the multiples of the switching frequency f_{sw} as discussed in the previous section.

Since CASE 0 has the sinusoidal spatial distribution of capacitor mismatch, the FT $\Delta\tilde{C}[f]$ has only the first-order spectrum. Thus, the error spectrum around the frequencies $2f_{sw}$ and $3f_{sw}$ are much smaller than that of f_{sw} as shown in Fig. 3.11(a).

CASE 1 and CASE 2 have higher-order spectra in the FT $\Delta\tilde{C}[f]$. We have larger error spectrum around the frequencies $2f_{sw}$ and $3f_{sw}$ for these cases as plotted in Fig. 3.11(b) and (c).

These results are in good agreement with our analysis in the previous section.

(2) Comparison with other architectures

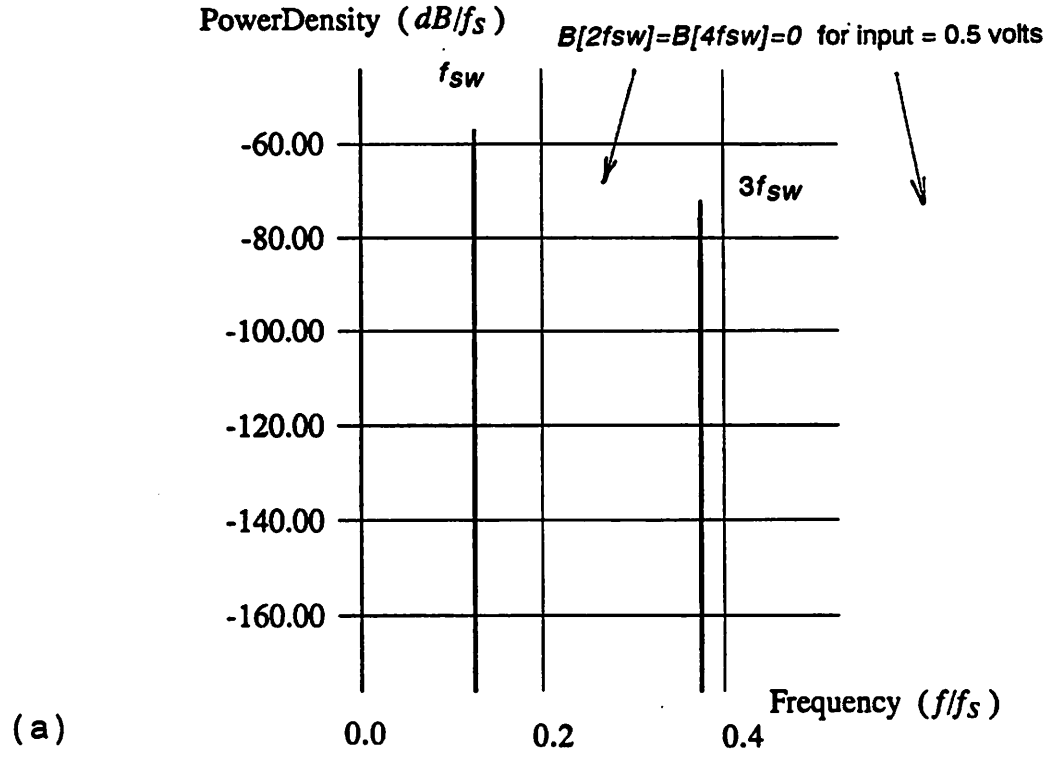
We perform three different simulations for the following architectures.

(1) No switching of D/A unit elements

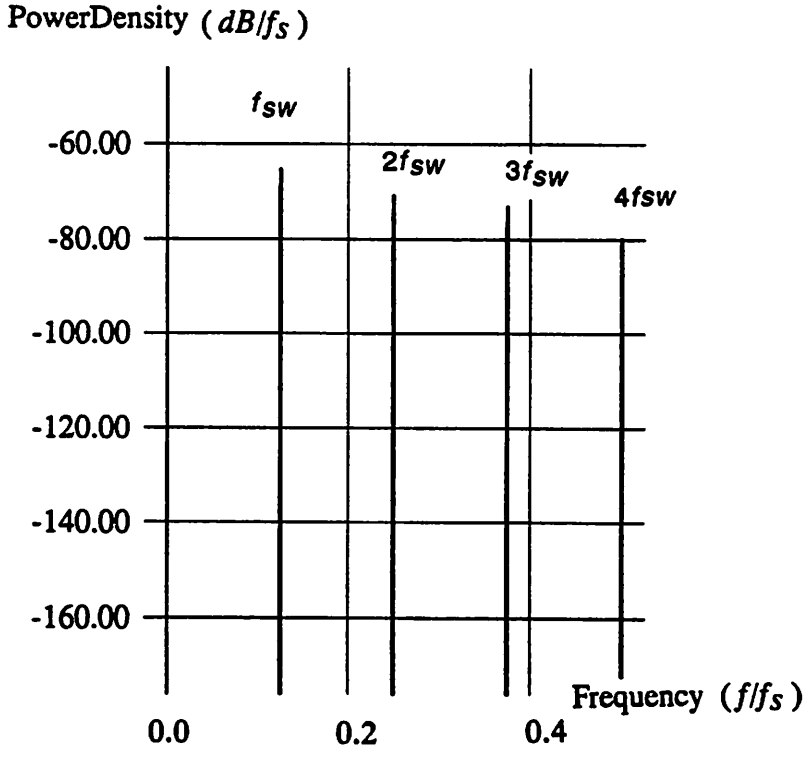
(2) Randomizing of D/A unit elements

(3) Dynamic barrel shifting of D/A unit elements

The performance of the DAC is measured by the total noise power NL in the baseband :



(a)



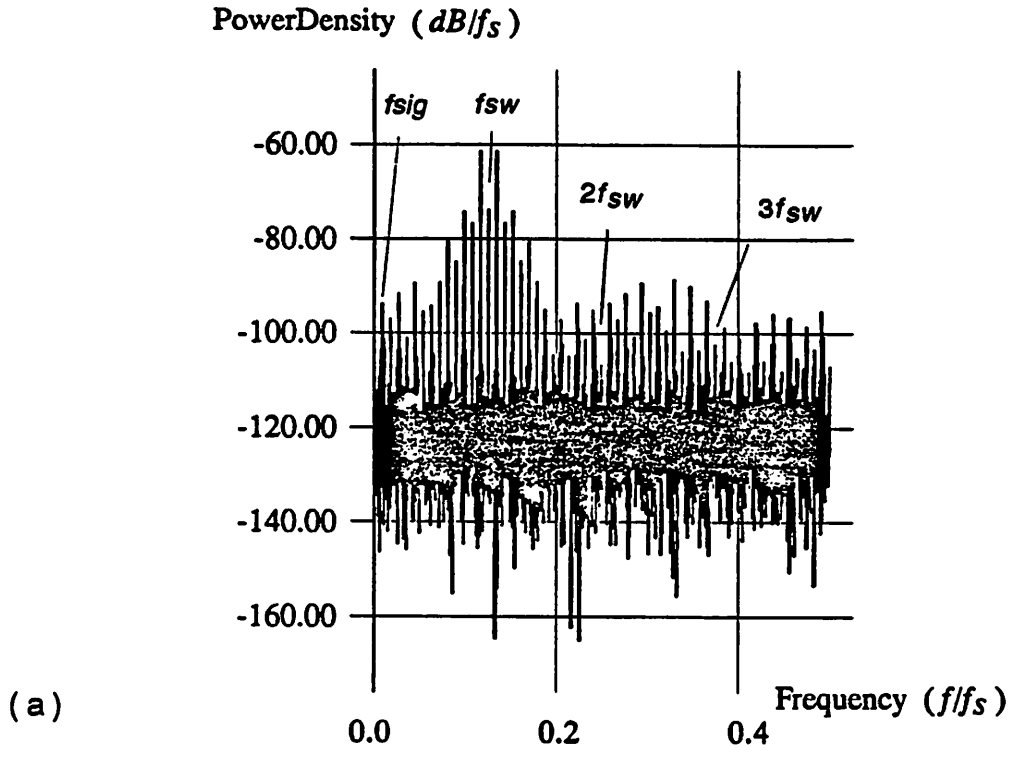
(b)

Note : Power density is specified relative to a F.S. sinusoid.

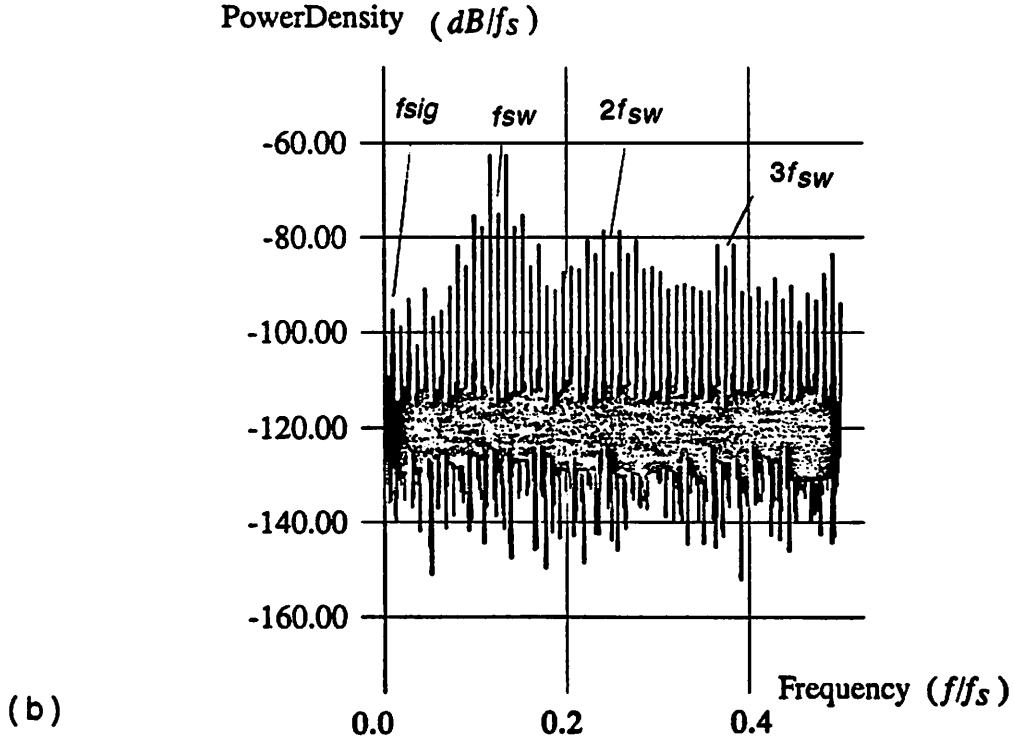
FIGURE 3.10 Spectral density distribution of the nonlinearity ε(z) for the open-loop system in Fig. 3.4 CASE 1 DC input

(a) Barrel shifting input = 0.5 volts (-6dB)

(b) Barrel shifting input = 0.15 volts (-8dB)



(a)

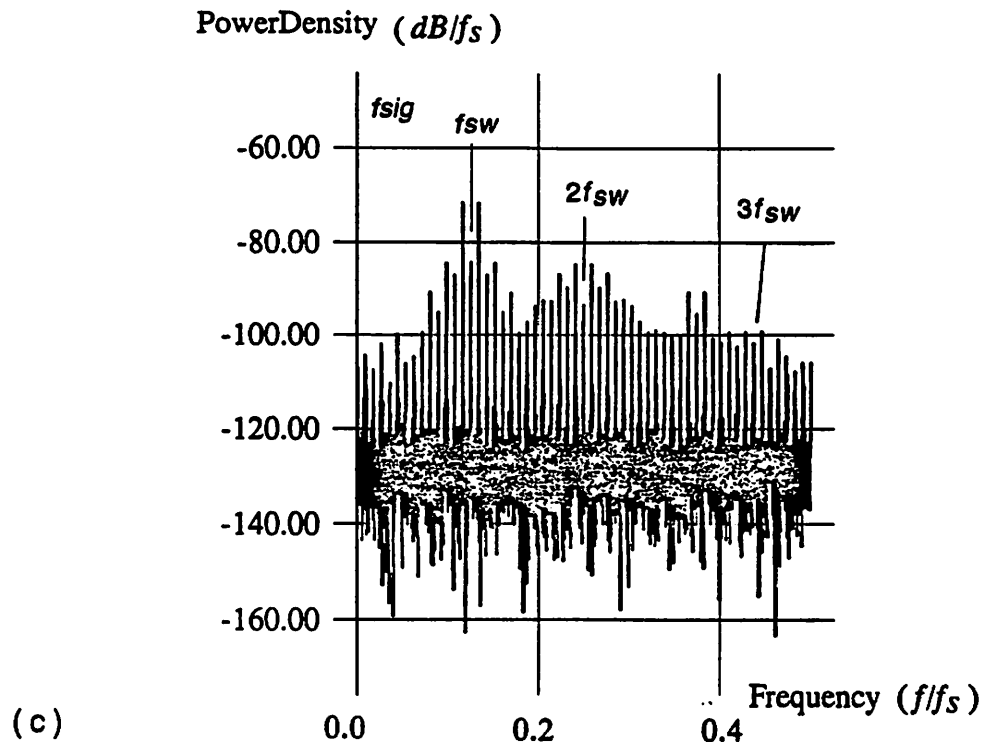


(b)

Note : Power density is specified relative to a F.S. sinusoid.

FIGURE 3.11 Spectral density distribution of the nonlinearity $\varepsilon(z)$ for the open-loop system in Fig. 3.4 CASE 1 Sinusoid input

(a) CASE 0 (b) CASE 1



Note : Power density is specified relative to a F.S. sinusoid.

FIGURE 3.11 *(continued)*

(c) CASE 2

$$NL = \int_0^{f_b} \varepsilon_n(f)\,df \qquad (3.2)$$

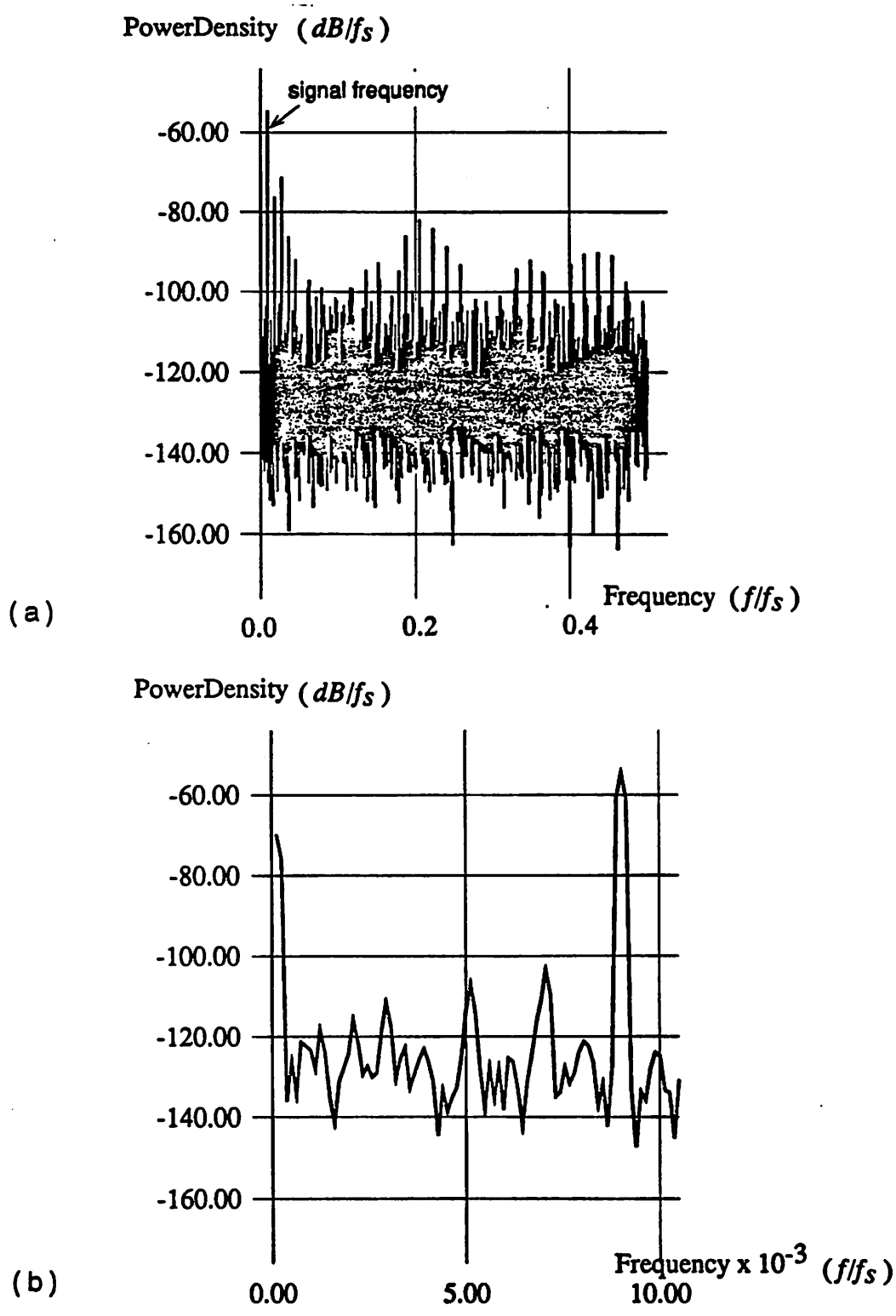
The total noise power NL in the baseband is shown in Table 3.4. The total noise power NL in the baseband is the least for the D/A with the dynamic barrel shifting. We examine the spectral distribution of the nonlinearity of each architecture. The spectral density distribution for the case one is shown in Figs. 3.12,. The D/A without switching (Figs. 3.12(a)(b)) has large dc and low frequency components of the nonlinearity, which make this architecture the worst of the three candidates. The D/A with a randomizer (Figs. 3.12(c)(d)) whitens the nonlinearity all over the frequency range from dc to the sampling frequency f_S, which results in the less total noise power NL in the baseband. Our new architecture with dynamic barrel shifting (Figs. 3.12(e)(f)) pushes the nonlinearity out of the baseband, which gives the least total noise power NL in the baseband of three architectures. These results verify our guess in the previous section, which suggest that our architecture is promising to improve the performance of a multi-bit ΣΔ modulator.

	Signal	No Switching	Randomizing	Barrel Shifting
Case 1	0.5	6.15×10^{-5}	1.32×10^{-5}	1.22×10^{-6}
	0.01	3.59×10^{-4}	3.44×10^{-6}	9.94×10^{-7}
Case 2	0.5	5.92×10^{-6}	1.28×10^{-6}	1.45×10^{-7}
	0.01	4.33×10^{-6}	4.50×10^{-7}	1.84×10^{-7}

(Unit : Watts)

TABLE 3.4 Total noise power *NL* in the baseband for CASE 1 and CASE 2 for the open-loop system in Fig. 3.4

As stated before, the above results are only for the open-loop system which consists of a cascade of an ADC and a DAC in Fig. 3.4. In the following chapters, we will incorporate this D/A nonlinearity model in a complete simulator for the four-bit $\Sigma\Delta$ modulator, and discuss the effects of the nonlinearity further.

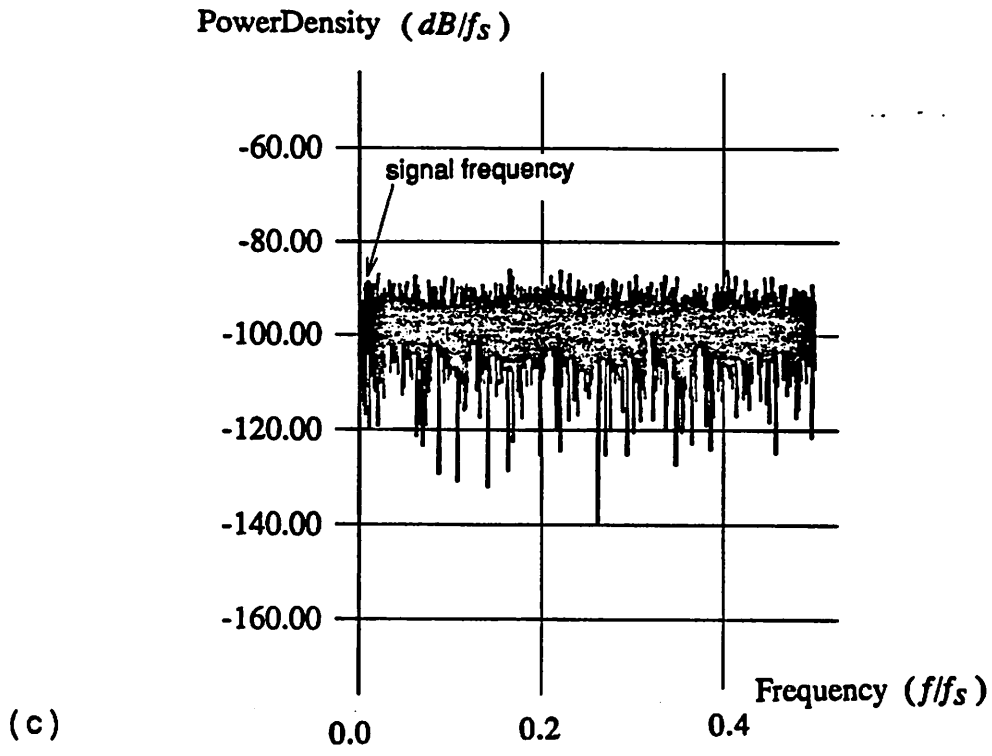


Note : Power density is specified relative to a F.S. sinusoid.

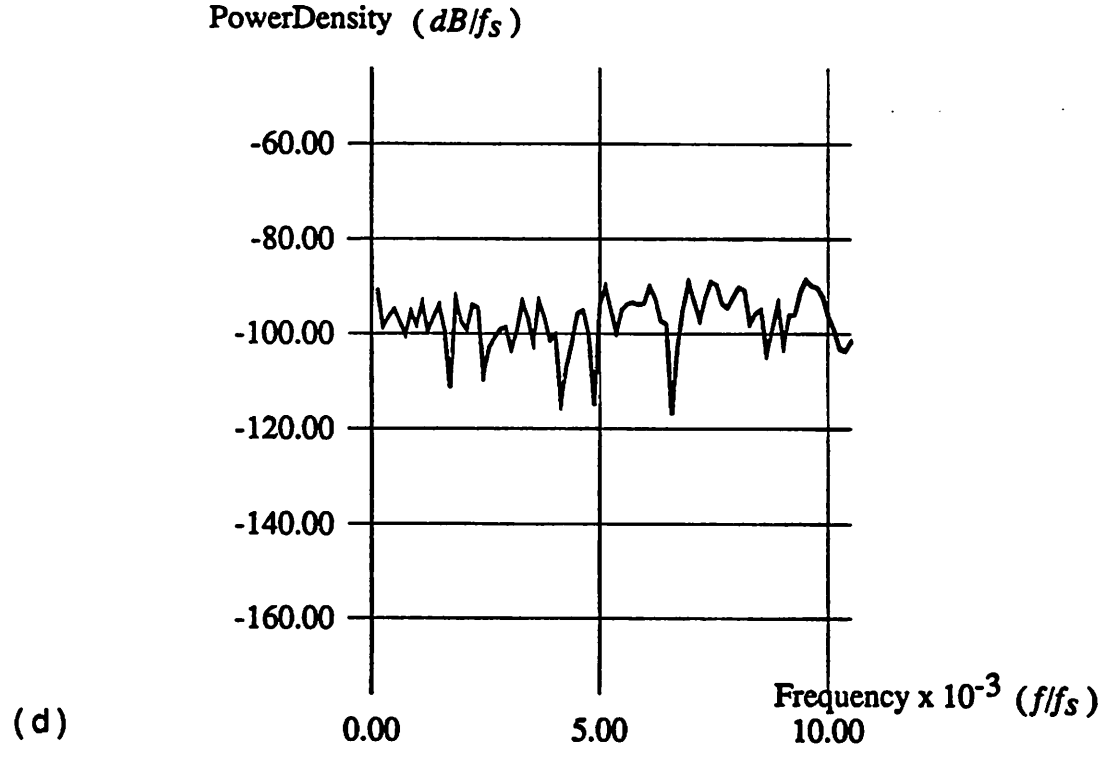
FIGURE 3.12 Spectral density distribution of the nonlinearity ε(z) for the open-loop system in Fig. 3.4 CASE 1

(a) No switching signal power = -6dB dc to 0.5*fs*

(b) No switching signal power = -6dB dc to 0.01*fs*



(c)

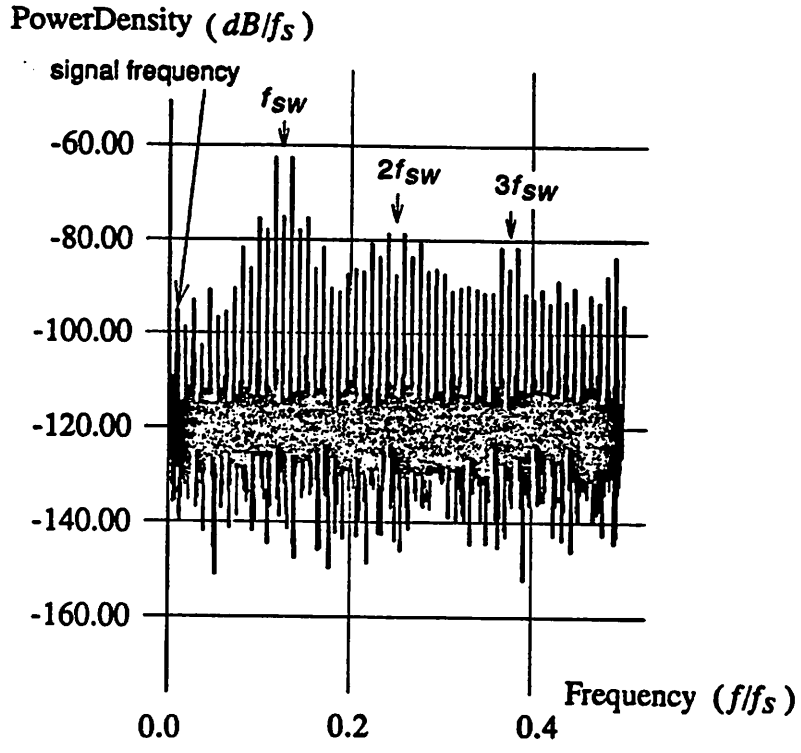


(d)

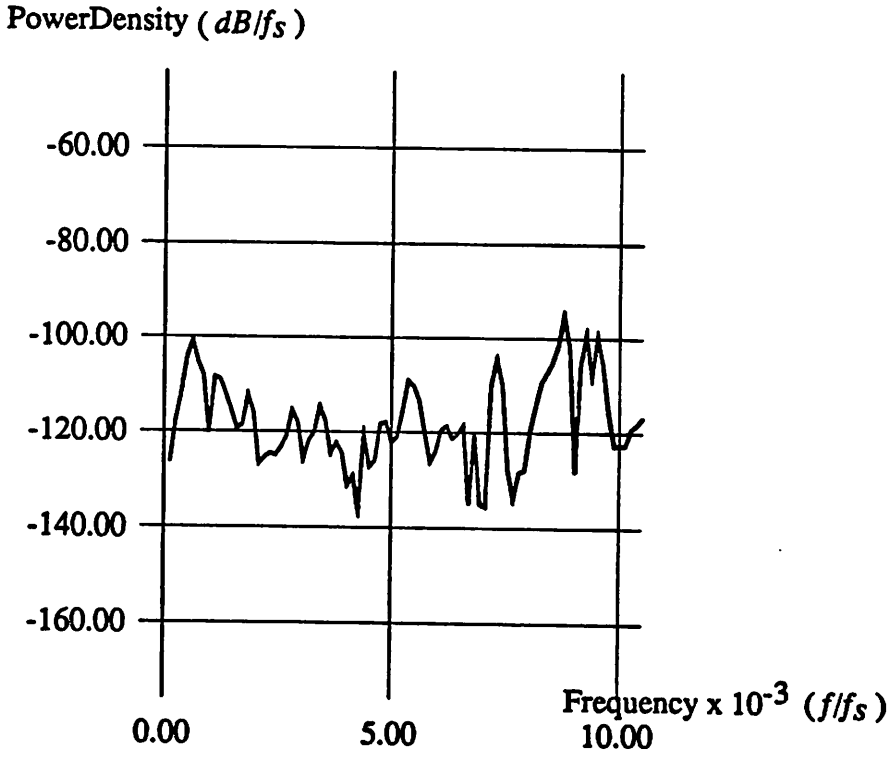
FIGURE 3.12 *(continued)*

(c) Randomizing signal power = -6dB dc to 0.5*fs*

(d) Randomizing signal power = -6dB dc to 0.01*fs*



(e)



(f)

FIGURE 3.12 *(continued)*

(e) Barrel shifting signal power = -6dB dc to 0.5*fs*

(f) Barrel shifting signal power = -6dB dc to 0.01*fs*

((e) is the same as Fig. 3.11 (b))

Chapter 4

System-Level Simulation of the ΣΔ Modulator

4.1 Introduction

In this report, we will investigate the system-level behavior of the ΣΔ modulator. Since this modulator is a nonlinear feedback system, it is complex to analyze the operation only by analytical formulation. We need to use some simulation tools to analyze it. In this chapter, we introduce the system-level simulation which is used to analyze the behavior of the multi-bit ΣΔ modulator.

Although using circuit simulation e.g. SPICE is very useful for transistor-level simulations, it cannot be used for system-level analysis of this modulator because of the following two reasons.

(1) SPICE is a transistor-level circuit simulator which requires a transistor-level circuit diagram. However, we want to investigate the system-level behavior of the modulator. In other words, we do not wish to specify the transistor-level circuit design. It is impossible to run SPICE at this stage of research.

(2) Even if we could design the whole circuit at transistor-level, CPU time required to perform SPICE for the entire system would be too long. As the sampling frequency is much higher than the input signal frequency, large number of samples in the time domain are needed to perform accurate FFT. For example, 8192-point FFT is used for the spectral estimation in this report. Since the circuit is implemented by switched capacitor circuits, SPICE would need many time steps to get only one point. As a result, SPICE would require huge amount of CPU time to get the final results. Hence, SPICE is not practical for

this kind of system-level simulation. It can be used only for smaller building-block circuits in the system.

We developed a system-level C-code program to simulate the operation of the ΣΔ modulator. Since the simulator can include circuit imperfections, we can evaluate not only the system-level performance but also the requirements of the analog circuits for CMOS circuit implementation

4.2 Assumptions for CMOS Circuit Implementation

Even though we use a system-level simulator, we must make some assumptions for CMOS circuit implementation to make this simulator realistic.

We modify the one-bit second-order ΣΔ modulator implementation [13] to the multi-bit modulator. The block diagram is shown in Fig. 4.1. Although the whole system is implemented by differential switched capacitor circuits, we perform simulations for single-ended architecture for simplicity.

4.2.1 Analog Switches

We can use CMOS transmission gates for the analog switches. As we use differential implementation, the offset voltage due to charge injection is cancelled to the first order.

4.2.2 Integrators

Integrators are implemented by switched capacitor architecture. There are two kinds of imperfections in the integrators. One is op-amp imperfections and the other is closed-loop gain error due to capacitor mismatch. They are discussed in section 4.4.

4.2.3 Four-Bit ADC

We assume a resistor-string flash ADC. We have fifteen resistors for the string for four bits. Nonlinearity due to mismatch of the resistors is negligible because it is in the feedback loop as discussed in section 3.2.

4.2.4 Thermometer Code to Intermediate Code Converter

This converts the thermometer code $A_{1\text{-}15}$ to the intermediate code $B_{1\text{-}8}$ literally.

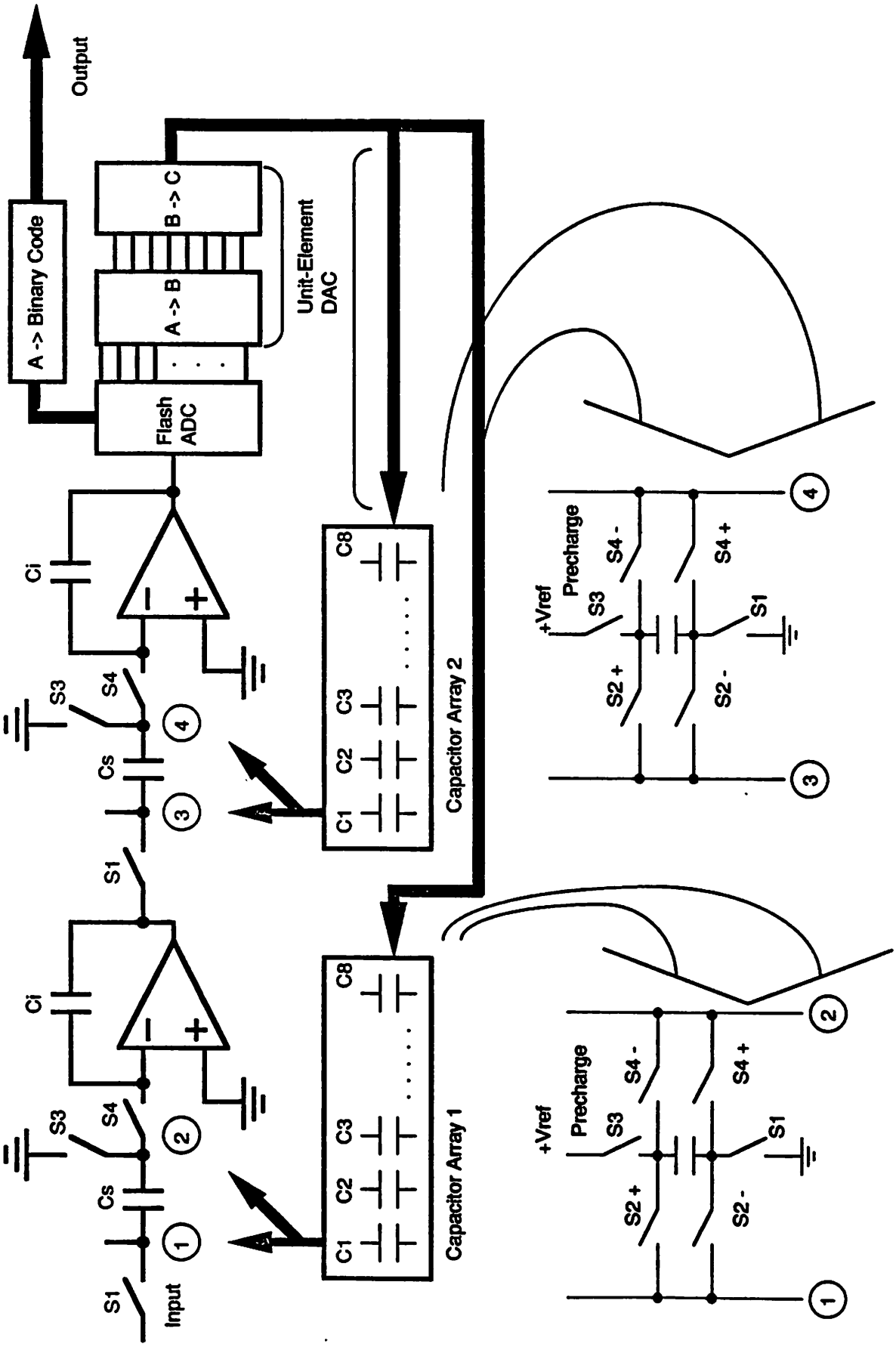


FIGURE 4.1 Four-bit second-order ΣΔ modulator implementation

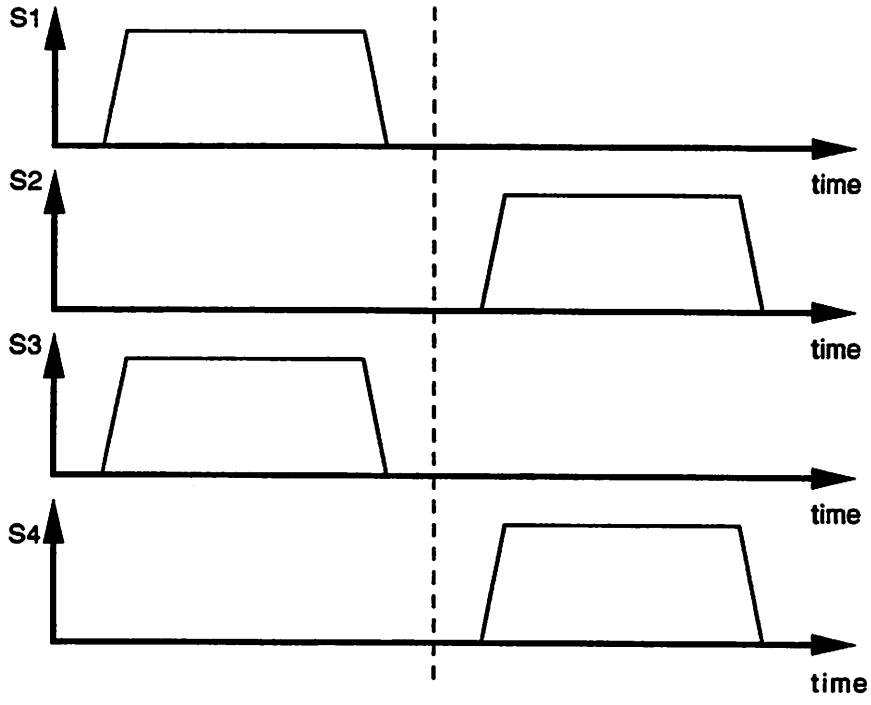


FIGURE 4.2 Non-overlapping two-phase clock

4.2.5 Dynamic Allocation Converter

This performs dynamic barrel shifting allocation of the unit elements in the DAC($B_{1\text{-}8}$ to $C_{1\text{-}8}$).

4.2.6 Four-Bit DAC

We use a unit-element capacitor array DAC. Since we have two summing nodes for feedback of the DAC output voltage, there must be two capacitor arrays. However, effects of the nonlinearity N_2 is much smaller than that of N_1 as discussed in section 3.3.2. Therefore, only mismatch of a capacitor array 1 is critical for the performance. For simplicity, we use the same capacitor array values for both capacitor array 1 and capacitor array 2 in the simulation.

4.2.7 Clocking Scheme

We use non-overlapping two-phase clock as shown in Fig. 4.2. For each clock cycle, the following operation must be performed.

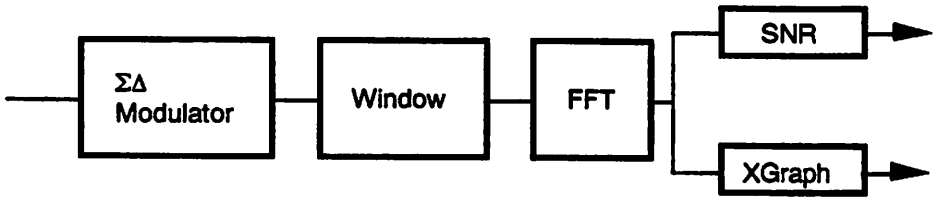


FIGURE 4.3 Block diagram of the simulation

Phase 1

All switches labeled S_1 and S_3 are on while those labeled S_2 and S_4 are off. Each input signal to the integrators is sampled on the sampling capacitors C_S. Unit-element capacitors of the DAC are precharged to the reference voltage $+V_{ref}$. The operation of the flash ADC, the thermometer code to the intermediate code converter (A-> B), and the barrel shifting (B -> C) must be done in this time slot.

Phase 2

All switches labeled S_1 and S_3 are off while those labeled S_2 and S_4 are on. The charge on the sampling capacitors C_S is transferred to the integration capacitors C_I. The feedback of the D/A output voltage to the summing nodes is achieved by the following sequence. The polarity of switches labeled(S_2^+ and S_2^-) and (S_4^+ and S_4^-) depends on the intermediate code $B_{1\text{-}8}$. The switches labeled (S_2^+ and S_4^+) are used for $B_{1\text{-}8} = +1$. Those labeled (S_2^- and S_4^-) are used for $B_{1\text{-}8} = -1$. For $B_{1\text{-}8} = 0$, the corresponding unit-element capacitors are not connected to the summing nodes of the integrator.

4.3 Overview of the Simulation

The block diagram of the simulation is given in Fig. 4.3. It consists of a simulator of the ΣΔ modulator, windowing program, FFT program, SNR program and XGraph.

4.3.1 Simulator of the ΣΔ modulator

This is a core program of this simulation. It simulates the behavior of the ΣΔ modulator and generates a high-rate four-bit output. We can specify several parameters that determine the performance of the modulator. They are listed in Table 4.1. We can investigate the performance by changing these parameters. The algorithm used in this program is discussed in the next section.

* Signal	: amplitude voltage, offset voltage, the Nyquist rate, sampling frequency, signal frequency
* Integrators	: time constant, closed-loop gain, clipping voltage, open-loop gain of op amps, slew rate of op amps
* D/A converter	: capacitance array mismatch, full scale voltage

TABLE 4.1 Parameters of the simulation

4.3.2 Windowing Program

As the number of samples available at the output is finite, we must optimize the window in the time domain. The window has a function of minimizing the spectrum leakage due to its sidelobe. We use the first-order Hanning window. Both the mainlobe width (-6dB) and the attenuation of the sidelobe leakage are sufficiently small for this evaluation [35].

4.3.3 Fast Fourier Transform Program

We use Fast Fourier Transform to evaluate the spectral density distribution of signals. Since the output of the modulator is real value, we can calculate the spectrum faster than complex-valued signals. The FFT of single real function [28] was modified to analyze the output signal in this simulation. We chose the number of samples for FFT is $2^{13} = 8192$.

4.3.4 Signal to Noise Ratio Program

This program calculates the signal to noise ratio SNR. This parameter is a key figure of merit for this modulator.

4.3.5 XGraph

This is a general graphic program developed for Xwindows [38]. Graphs of spectral density distribution are obtained by this program.

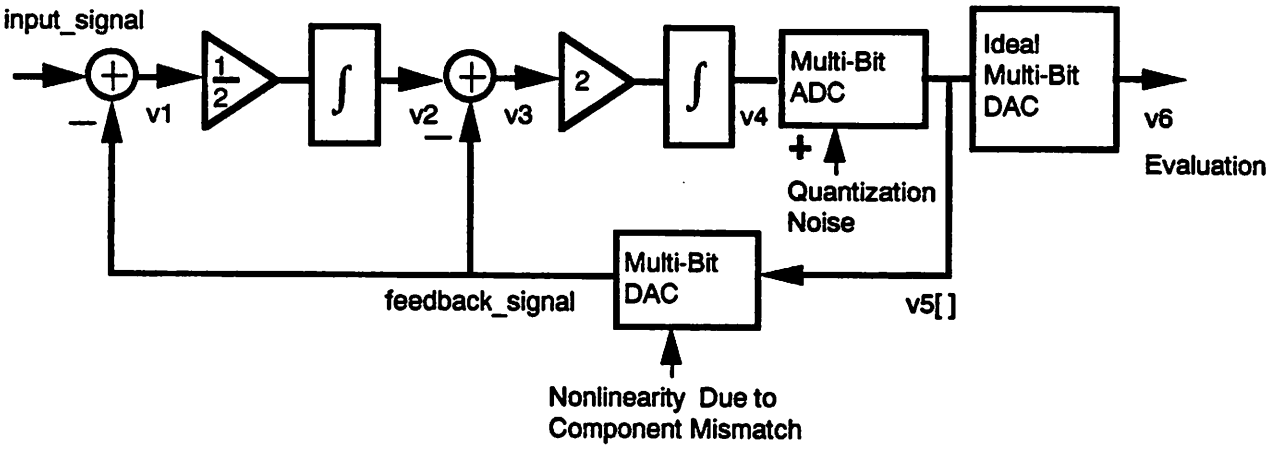


FIGURE 4.4 Block diagram used for the simulation

4.4 Basic Algorithm for the Modeling of the ΣΔ Modulator

A block diagram of the four-bit second-order ΣΔ modulator is shown in Fig. 4.4. We use the following algorithm to simulate the behavior of the modulator.

```
fscanf(parameters) ;
for ( time=tstart ; time<=tend ; time++ )
{
     input_signal=amplitude*cos(2*pi*sampling_frequency*time)+offset;
     v1=input_signal-feedback_signal ;
     v2_old=v2 ;
     integrate v1 as v2 ;
     v3=v2_old-feedback_signal ;
     integrate v3 as v4 ;
     quantize v4 as v5[] ;
     convert v5[] to analog feedback_signal ;
     convert v5[] to v6 ;
     fprintf(input_signal, v1, v2, v3, v4, v5[], v6, feedback_signal);
}
```

4.5 Modeling of Circuit Imperfections

As we always have circuit imperfections, we must take them into account in the simulation. In Fig. 4.4, we consider imperfections of integrators and a four-bit DAC. As mentioned in section 3.2, we can neglect the nonlinearity of a four-bit ADC because it is in the feedback loop.

4.5.1 Integrators

These integrators are implemented by switched capacitor circuits. We have two kinds of imperfections. One is due to op amps and the other is due to capacitor ratio mismatch.

(1) Op Amps

We consider the following imperfections of op amps.

(i) Finite Open-Loop Gain A_V

Although an ideal op amp has infinite open-loop gain, an actual op amp can have finite open-loop gain. A diagram of a simple switched capacitor integrator is shown in Fig. 4.5. The output voltage at the time n+1 is given as

$$V_{on+1} = V_{on} - \frac{C_I}{C_S}\left(V_{in} - \frac{V_{on+1}}{A_v}\right) \qquad (4.1)$$

We must take account of the last term because the voltage at the summing node is not equal to zero but V_{on+1}/A_V. This circuit can be modeled as a sampled-data system as shown in Fig. 4.6. The effect of the last term can be expressed as leakage of the output voltage to the input voltage.

(ii) Finite Op Amp Bandwidth and Slew Rate

If an integrator is a single-pole system and the output is purely exponential, the step response of the integrator is

$$V_o = V_I + \frac{C_I}{C_S}\left(1 - \exp\left(-\frac{1}{2 f_s \tau}\right)\right)V_{step} \qquad \text{for } V_{step} < \tau S_R \qquad (4.2)$$

where f_S is the sampling frequency, τ is the time constant of the exponential response and V_{step} is the output step voltage. The time slot available for the integration is half of the clock period. We must take account of this effect in the simulation. We use $1/2f_S$ instead

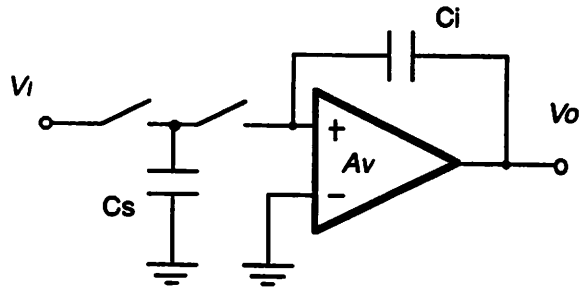


FIGURE 4.5 Diagram of a switched capacitor integrator

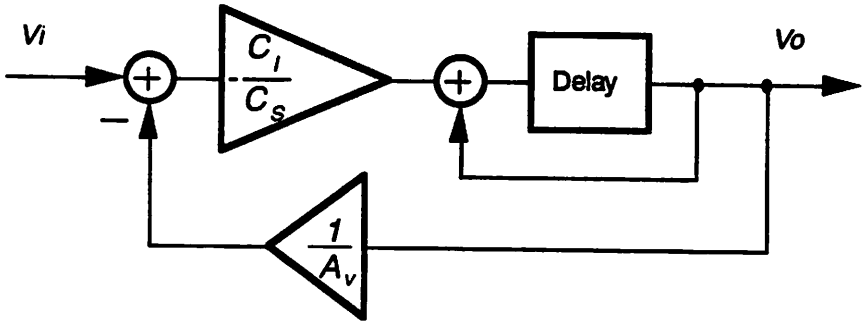


FIGURE 4.6 Leakage of output voltage

of $1/f_S$ to include this effect in eq. (4.2). The bandwidth of the circuit is given as $1/\tau$. If the step voltage is larger than the slewing limit τS_R , the slewing degrades the response. The settling will be a combination of the slew and exponential response. It can be given as

$$v_o = v_i + v_{step} - \frac{C_i}{C_s}\frac{\tau S_R}{V_{step}} exp\left(\frac{V_{step}}{\tau S_R} - 1 - \frac{1}{2 f_s \tau}\right) \quad \text{for } V_{step} > \tau S_R \qquad (4.3)$$

where S_R is the slew rate of the an op amp [21]. These two models are used in the simulation.

(2) Capacitor Ratio C_i/C_S Mismatch

The capacitor ratio C_i/C_S mismatch determines the closed-loop gain of the integrator, which will change the transfer function of the whole system. The mismatch can be implemented by changing the closed-loop gain of the integrators in the program.

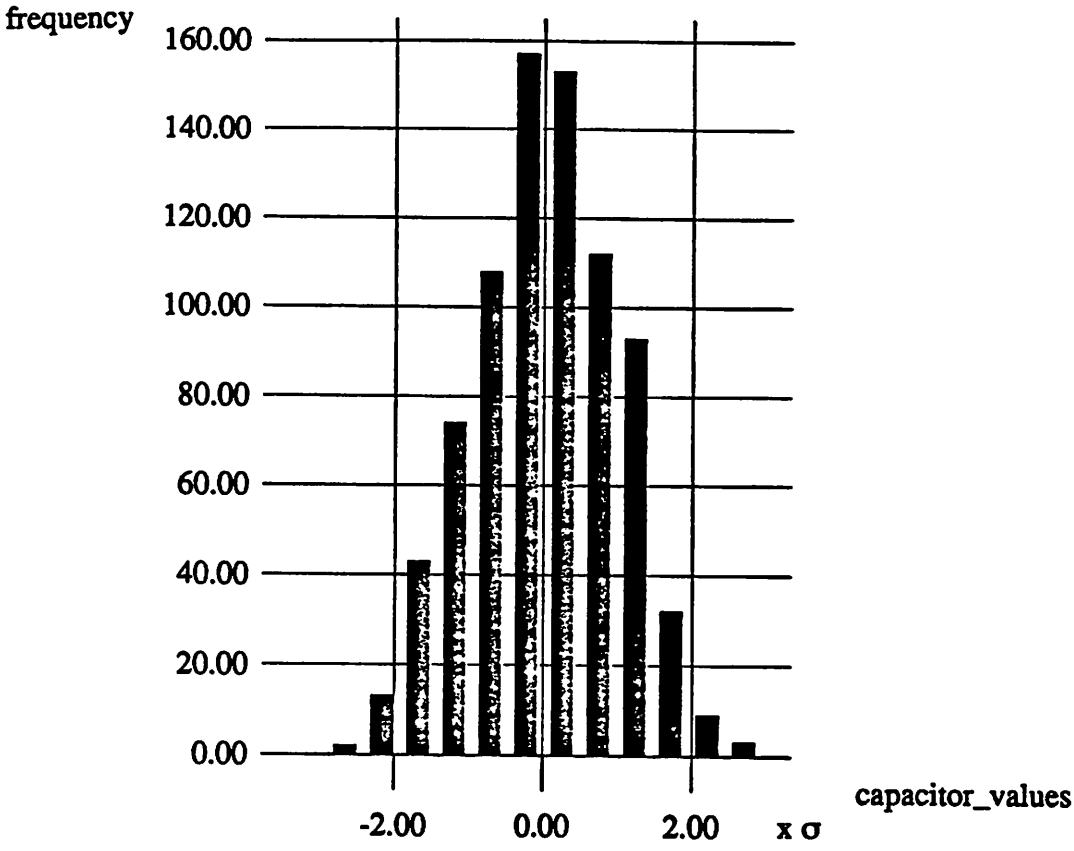


FIGURE 4.7 Distribution of capacitor values used in the simulation

4.5.2 Four-Bit DAC

The nonlinearity introduced by this DAC is a key factor that degrades the performance. This nonlinearity is due to mismatch of a capacitor array which comes from the local variation of manufacturing process, such as photolithography fluctuations and localized etch rate nonuniformity.

We use the Monte Carlo simulation to model the variation of capacitor values. As discussed in section 4.2.6, we use only one capacitor array in the simulation. Capacitor values of $C1$ - $C8$ are determined by a C-code program which generates the random Gaussian distributed numbers. The number of samples used for each simulation is one hundred. Since one sample contains eight capacitors, we generate eight hundreds different capacitor values for the entire simulation. The distribution of these capacitor values is plotted in Fig. 4.7.

Chapter 5
Simulation Results

Simulation results are discussed in this chapter to analyze the behavior of the four-bit ΣΔ modulator. Simulations are performed with the conditions shown in Table 5.1 unless otherwise stated.

5.1 Basic Performance

We discuss basic behavior of the modulator in both time domain and frequency domain. We do not take account of circuit imperfections in this section.

*	Full scale voltage	:	1.0 Volt
*	Number of bits of an internal quantizer	:	4
*	Sampling frequency	:	fs
*	Nyquist rate	:	fs x *146/8192*
*	Signal frequency (sinusoid)	:	fs x *73/8192*
*	Signal amplitude	:	0.5 Volts (-6dB)
*	Op amp clipping voltage	:	1.0 Volt
*	Fast Fourier Transform		
	Window	:	First-order Hanning window
	Number of points	:	8192

Table 5.1 Simulation conditions

5.1.1 Waveforms

Time-domain waveforms and spectral density distribution for input signal = -6dB and -40 dB are plotted in Figs. 5.1 and 5.2, respectively. In time-domain waveforms, it can be seen that the output voltage changes so that the average of them is equal to the input voltage. Since we have sixteen levels (four bits) for a quantizer, the output wave form is much smoother than that of a one-bit quantizer in Fig. 2.7. The noise shaping effect in the frequency domain can be seen in Figs. 5.1(a) and 5.2(a). Power density is specified relative to a Full Scale sinusoid unless otherwise stated. Background quantization noise power is nearly equal for the two signal inputs.

5.1.2 Signal to Noise Ratio

The signal to noise ratio SNR vs input signal power is plotted in Fig. 5.3. Fluctuation of the SNR for small signals is due to error of calculation of noise power. The SNR vs the OSR is plotted in Fig. 5.4 compared with those calculated from eqn.(2.14). We can see good agreement between them.

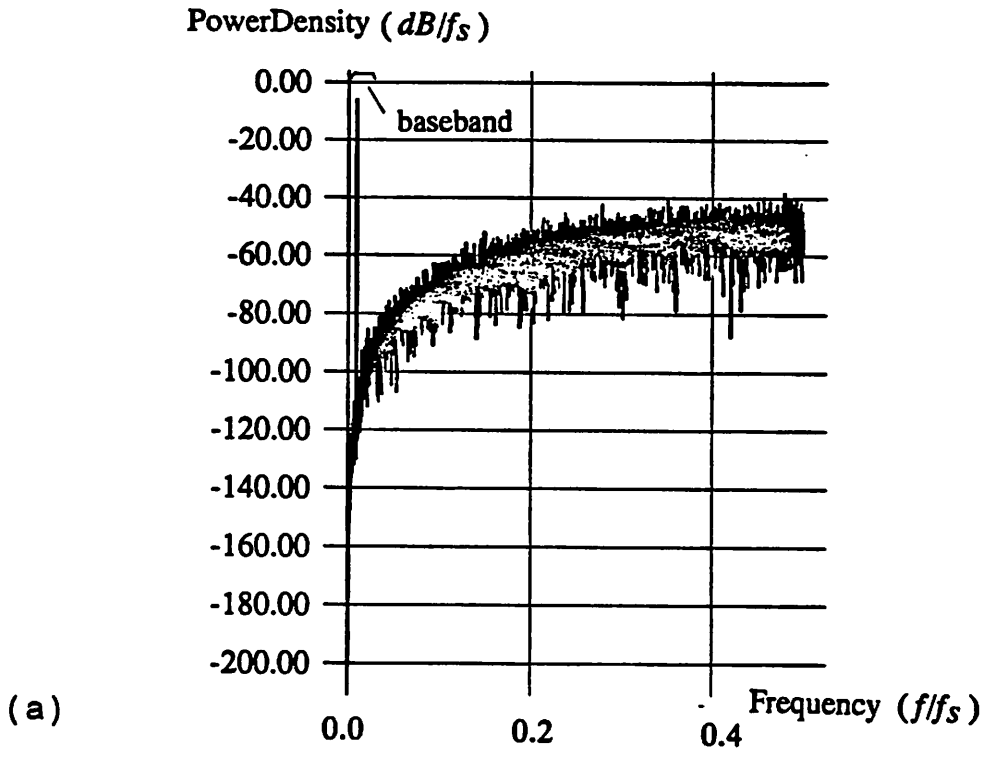
5.2 Effects of Circuit Imperfections

The effects of circuit imperfections described in the previous chapter are discussed in this section.

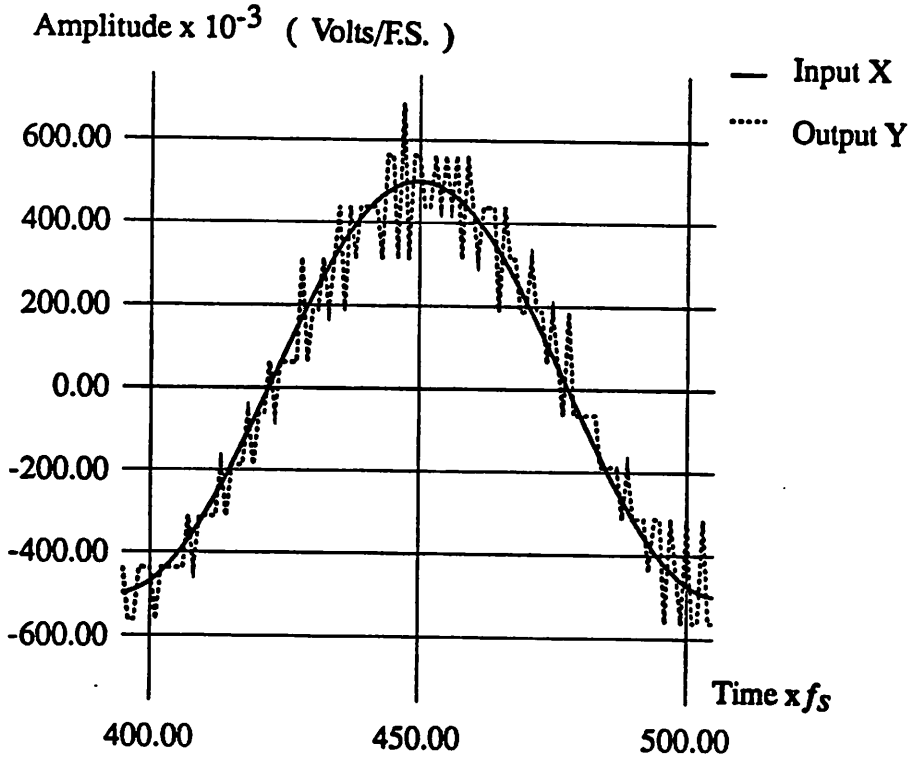
5.2.1 Integrators

(1) Finite Op-Amp Open-Loop Gain A_V

The finite op-amp open-loop gain at low frequency reduces the attenuation of the quantization noise in the baseband, which results in the reduction of the SNR [13]. The relationship between the gain A_V and the SNR is plotted in Fig. 5.5. The reduction of the SNR due to the finite gain is smaller than 3dB for the gain more than 56.1. Since the OSR is 56.1, the penalty for the finite gain is negligible if the gain is comparable to the OSR. This results is in good agreement with previous results of one-bit ΣΔ modulators [13,14,29].

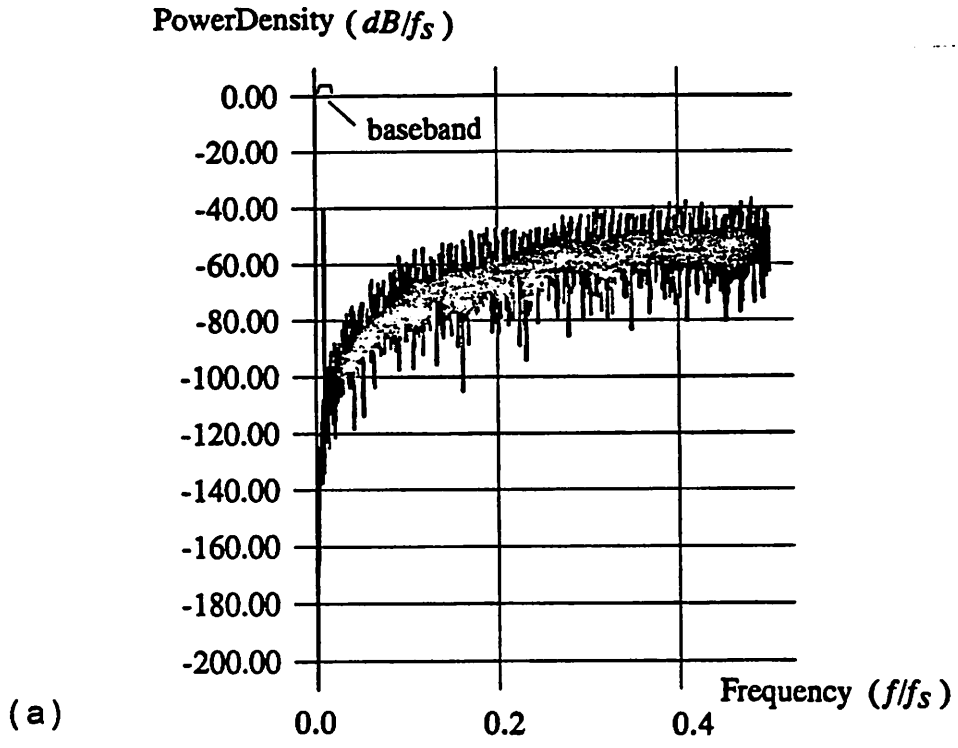


(a)



(b)

FIGURE 5.1 Simulation for an input signal equal to -6dB of full scale voltage
(a) Frequency domain
(b) Time domain



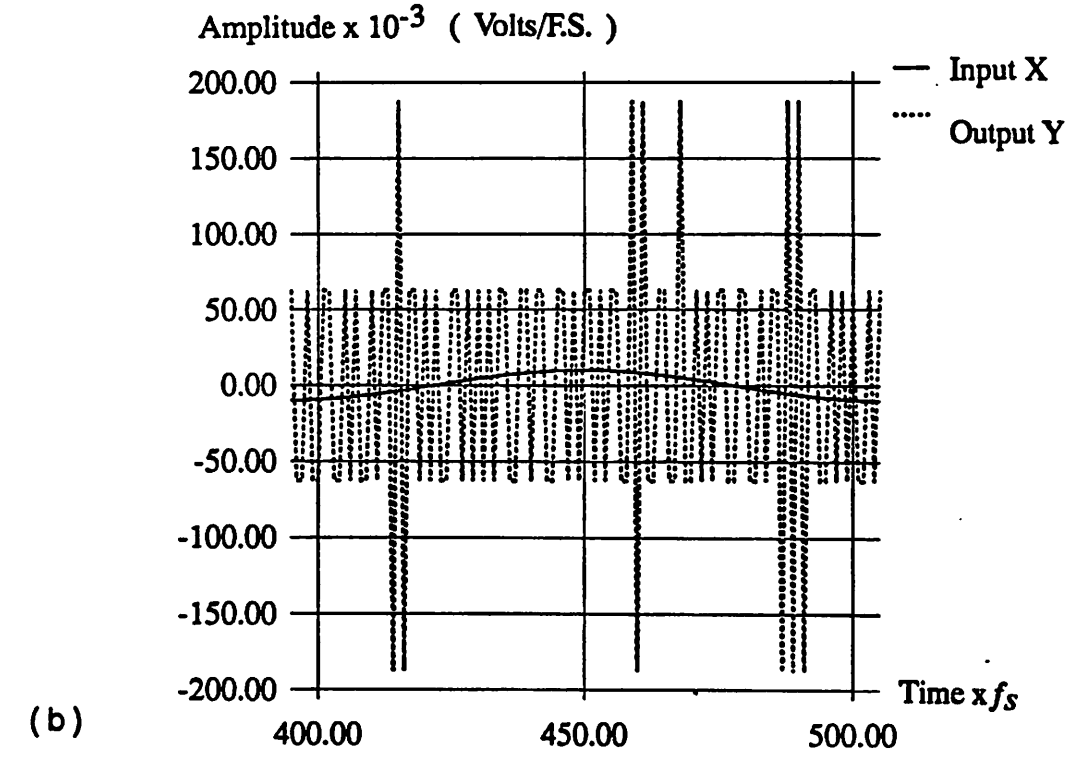


FIGURE 5.2 Simulation for an input signal equal to -40dB of full scale voltage
(a) Frequency domain
(b) Time domain

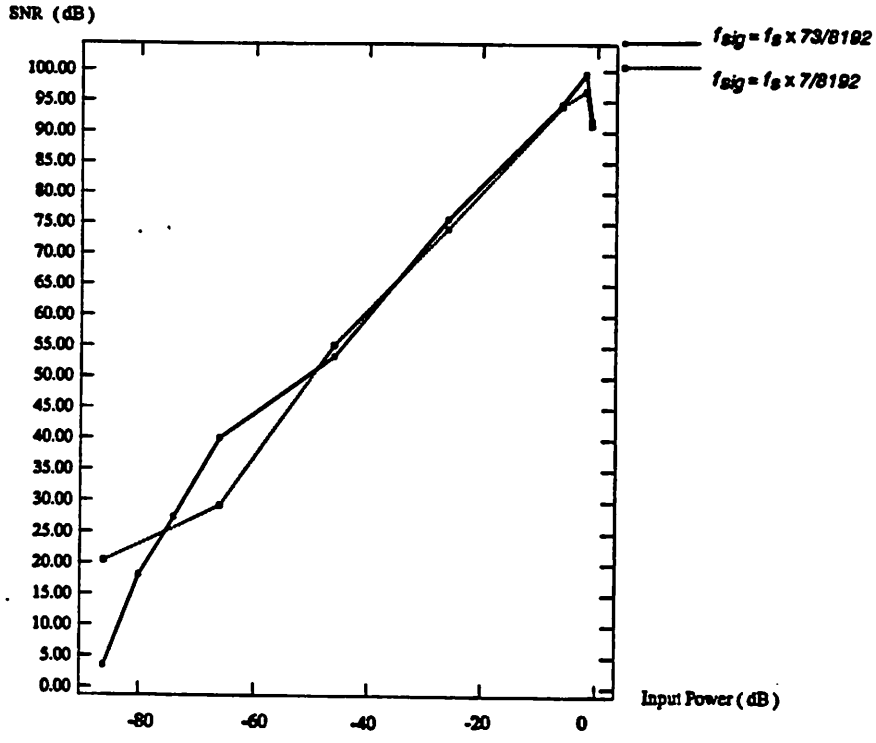


FIGURE 5.3 Signal to Noise Ratio vs input signal amplitude

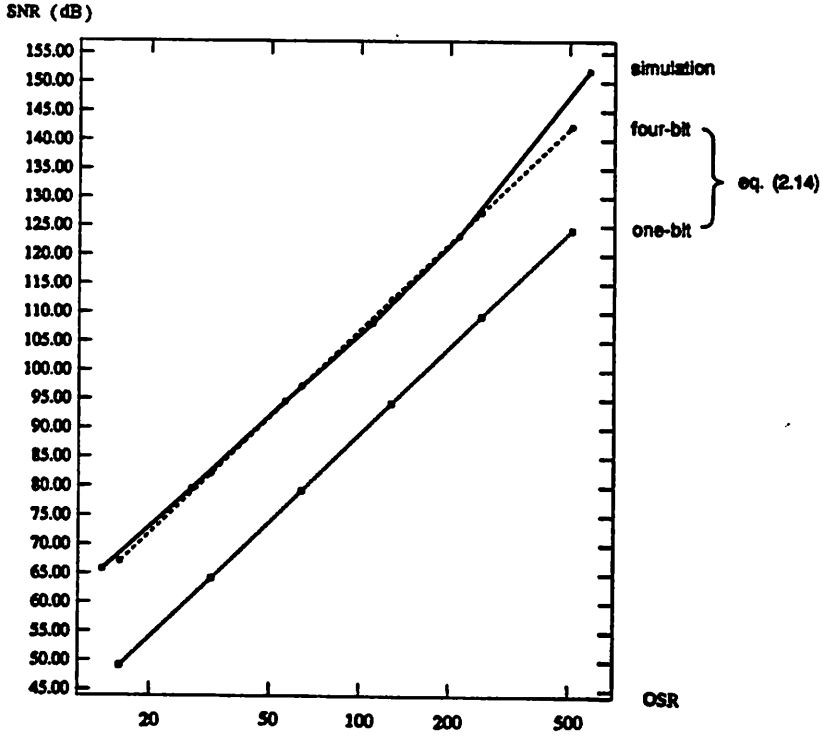


FIGURE 5.4 Signal to Noise Ratio vs Over Sampling Ratio

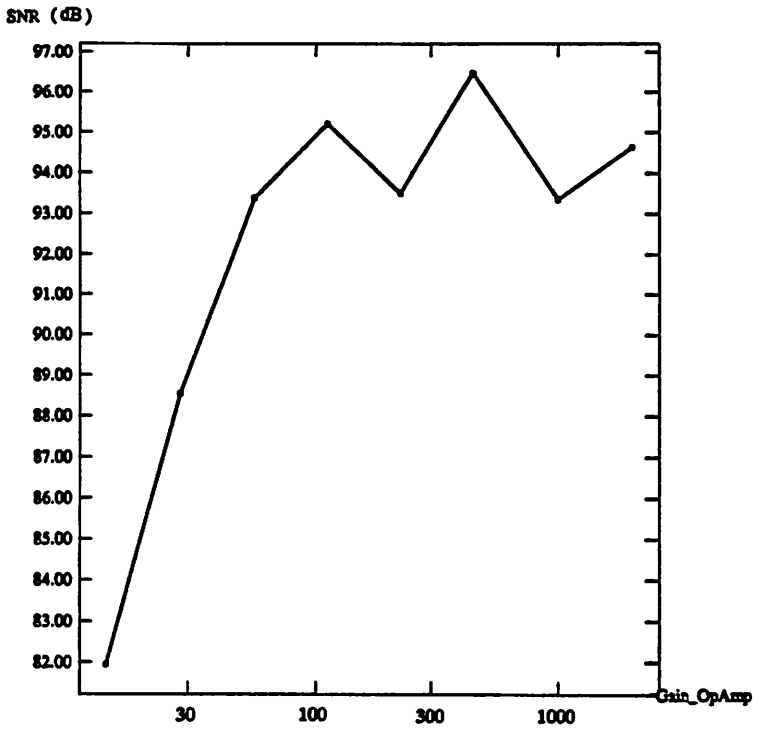


FIGURE 5.5 Signal to Noise Ratio vs op-amp open-loop gain

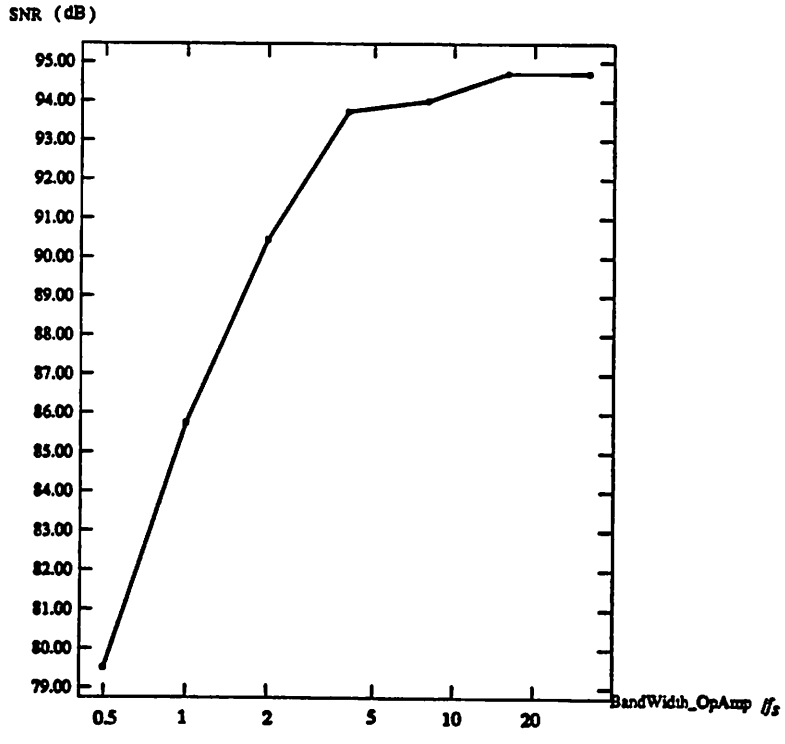


FIGURE 5.6 Signal to Noise Ratio vs op-amp band width

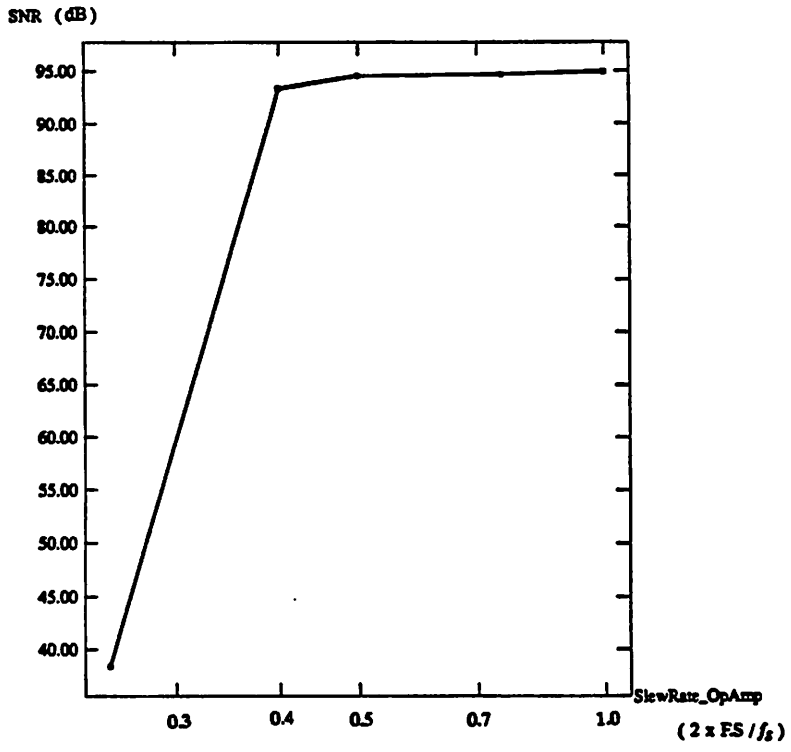


FIGURE 5.7 Signal to Noise Ratio vs op-amp slew rate

(2) Finite Bandwidth and Slew Rate

(i) Effects of Finite Bandwidth and Slew Rate

Assuming the response is purely exponential, the error voltage v_{error} due to the finite bandwidth is given from eqn.(4.2) as

$$v_{error} = \frac{C_I}{C_S} exp\left(- \frac{1}{2 f_s \tau} \right) v_{step} \qquad (5.1)$$

As both the sampling frequency f_S and the time constant of the circuit τ are independent of the step voltage v_{step}, the error voltage v_{error} is a linear function of the step voltage v_{step}. The error has the same effect as the closed-loop gain error which will be discussed in the next section. It reduces the SNR as shown in Fig. 5.6. The x-axis is the bandwidth of an op amp normalized by sampling frequency f_S. From this figure it can be seen that the reduction of the SNR due to finite bandwidth is smaller than 1dB if the bandwidth is five times larger than the sampling frequency f_S .

If the step voltage is larger than the slewing limit τSR ,the error voltage due to the slewing is given from eqn.(4.3) as

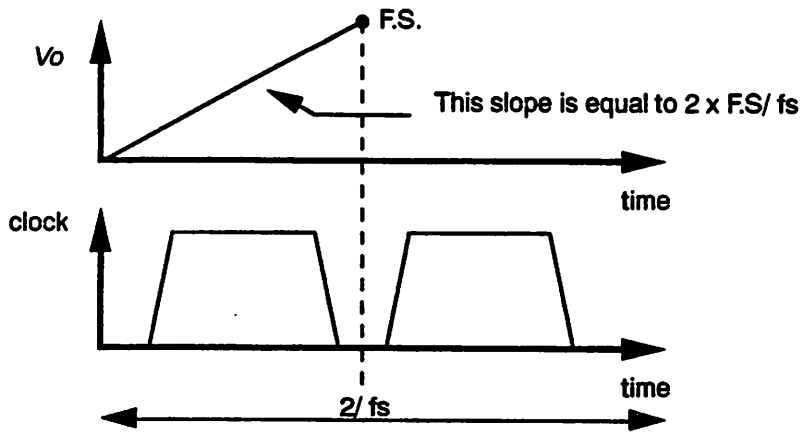


FIGURE 5.8 Unit of slew rate

$$v_{error} = \frac{C_I}{C_S}\frac{\tau S_R}{V_{step}} exp\left(\frac{V_{step}}{\tau S_R} - 1 - \frac{1}{2 f_s \tau}\right) \qquad (5.2)$$

This is not a linear function of the step voltage v_{step}. It generates nonlinear effects on the output, which results in harmonic distortion. The simulation results of finite slew rate are shown in Fig. 5.7. In this simulation we assume the bandwidth is ten times larger than the sampling frequency f_S . The unit of slew rate (x axis) is normalized by 2 x Full Scale Voltage /the sampling frequency f_S] as shown in Fig. 5.8. The penalty due to the slewing is smaller than 1dB when the slew rate is greater than 0.5 x [2 x Full Scale Voltage /the sampling frequency f_S].

(ii) Comparison with One-Bit ΣΔ Modulators

Bandwidth

For a one-bit second-order ΣΔ modulator, the bandwidth comparable to the sampling frequency f_S is sufficient to keep the performance degradation negligible [13]. A four-bit ADC requires more accuracy for settling than a one-bit ADC. Hence, four-bit modulator requires the bandwidth at least five times larger than the sampling frequency f_S.

Slew Rate

The slew rate more than 1.1 x [2 x Full Scale Voltage /the sampling frequency f_S] is required for a one-bit ΣΔ modulator [13]. For the four-bit modulator, the requirement is more relaxed. The slew rate more than 0.5 x [2 x Full Scale Voltage /the sampling frequency f_S] is sufficient to keep the performance. Since we have more quantization

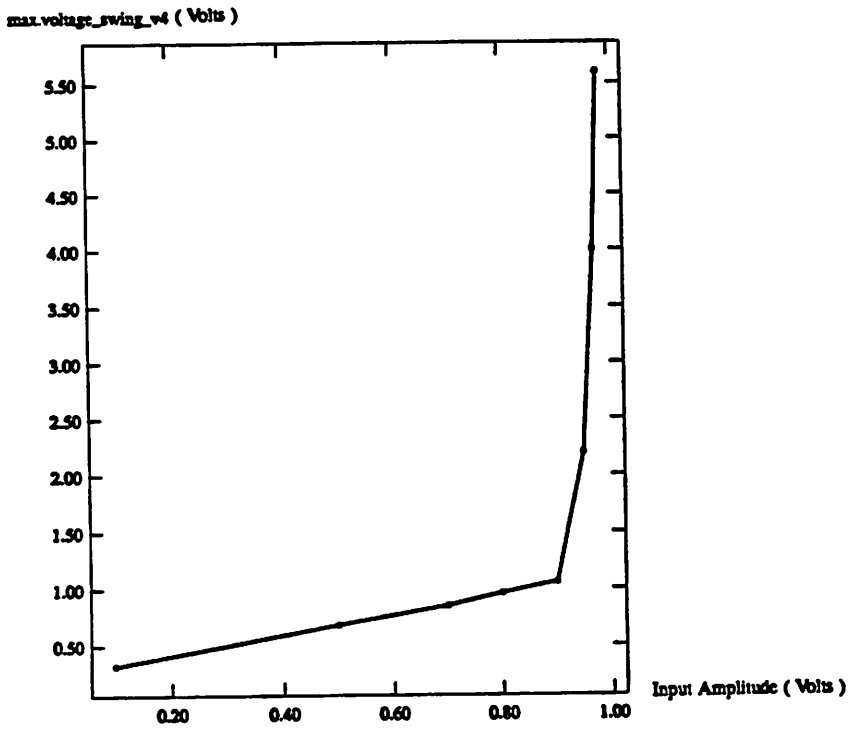


FIGURE 5.9 Op-amp output swing vs input signal amplitude

levels in a four-bit system, the slew required for the two integrators (v2 and v4 in Fig. 4.4) is much smaller than those of a one-bit quantizer.

(3) Finite Op-Amp Output Swing

The outputs of the op amps have state information. The clipping of the output swing loses the state information, which results in the degradation of the performance. For a single-bit ΣΔ modulator, the clipping is a critical problem. Some scaling techniques have been developed to overcome this problem [13,21].

The maximum voltage swing in the second-order modulator occurs at the output of the second integrator. The relationship between the maximum output swing and input signal amplitude of the four-bit ΣΔ modulator is plotted in Fig. 5.9. In this simulation, no clipping is used for op amp swing. The output swing is smaller than 1.0 x Full Scale Voltage for the input amplitude range less than 0.8 x Full Scale Voltage. Therefore, we can choose the clipping voltage of op amps as 1.0 x Full Scale Voltage so that the modulator can operate without clipping for the input range. Since this output swing requirement is much less than 1.7 x Full Scale Voltage for a single-bit ΣΔ modulator [13,20], it does not require any scaling of internal voltages in the system. In addition, the modulator does not

overload for the input amplitude smaller than 0.8 x Full Scale Voltage since the input dynamic range of the quantizer is 0.9375 x Full Scale Voltage. This input signal range for stable operation is larger than that of a single-bit modulator [13,20,21].

(4) Closed-Loop Gain Errors

Closed-Loop Gain of the First Integrator G_1

The closed-loop gain of the first integrator G_1 is calculated by the ratio of the integration capacitor C_i to the sampling capacitor C_S . The mismatch of C_i and C_S results in the error of the gain G_1. From Fig. 4.4, the gain of the first integrator must be equal to 0.5. The SNR vs the gain G_1 is plotted in Fig. 5.10(a). The degradation of the SNR is smaller than 2dB when the G_1 is in the range from 0.8 to 1.2. Since the relative precision of 20% is obtainable by standard CMOS technologies, the reduction of the SNR due to this error is negligible.

Closed-Loop Gain of The First Integrator G_2

The closed-loop gain of the second integrator G_2 is also calculated by the ratio of the integration capacitor C_i to the sampling capacitor C_S. The gain is needed to be 2.0. Fig. 5.10(b) shows the relationship between the SNR and the gain G_2 . The reduction of the SNR is smaller than 1dB for the values of G_2 between 0.8 and 1.2. This also can be achievable by standard CMOS technologies.

5.2.2 Four-Bit DAC

The nonlinearity introduced by this DAC is a major factor which reduces the SNR. In section 3.3.3, we discussed simulation results of the nonlinearity for the open-loop system. In this section, we incorporate the DAC nonlinearity model in the four-bit ΣΔ modulator. First, we discuss simulation results for the mismatch models of case 1 and case 2 in Figs. 3.7 so that we can obtain the rough idea about the effects of the nonlinearity. Then, we perform the Monte Carlo simulation to evaluate accurate effects of the nonlinearity.

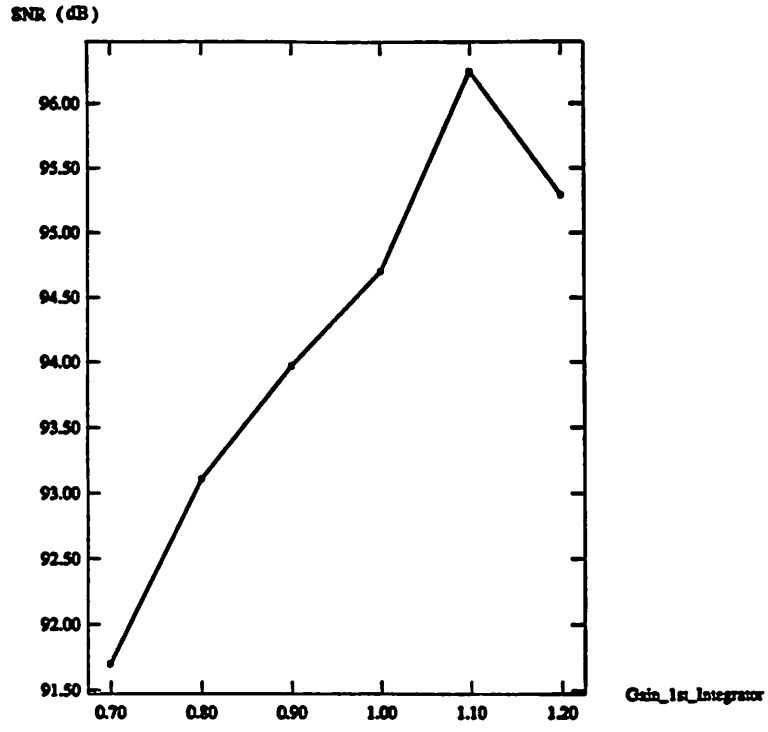
(1) Simulations of Case 1 and Case 2

We perform simulations for the mismatch models of D/A unit-element capacitors shown in Figs. 3.7. Three different simulations for the following architecture are achieved for these two cases as in section 3.3.3.

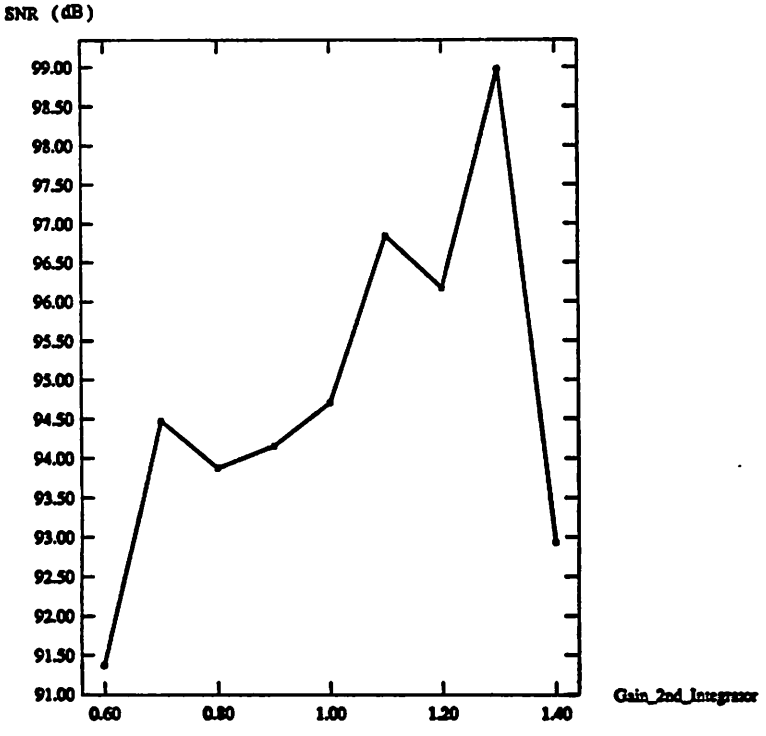
(1) No switching of D/A unit elements

(2) Randomizing of D/A unit elements

(3) Dynamic barrel shifting of D/A unit elements



(a)



(b)

FIGURE 5.10 Signal to Noise Ratio vs integrator gains
(a) First integrator *G1*
(b) Second integrator *G2*

Signal Amplitude	Ideal Case	CASE 1			CASE 2		
		No SW	Random	Dynamic	No SW	Random	Dynamic
0.5 F.S.	94.5	65.4	72.1	82.1	75.9	82.1	89.5
0.01 F.S.	64.2	23.9	43.3	48.7	43.0	51.8	55.8

(Unit: dB)

TABLE 5.2 Signal to Noise Ratio of CASE 1 and CASE 2

Table 5.2 shows the SNR obtained by each architecture compared with a no-switching case. For both case 1 and case 2, the SNR obtained by the dynamic barrel shifting is much better than those obtained by no-switching and randomizing. The output spectral density distributions of these three architectures are plotted in Figs. 5.12, 5.13 and 5.14. The spectrum without switching of D/A unit elements (Figs. 5.12(a) and (b)) shows large peaks at dc and low frequencies. These peaks are harmonic distortion. The architecture with randomizer (Figs. 5.13(a) and (b)) shows less baseband noise than the no-switching architecture. The architecture with the dynamic barrel shifting (Figs. 5.14(a) and (b)) has the smallest noise in the baseband, which results in the best SNR of the three architectures. This is in good agreement with the results discussed in section 3.3.3.

(2) Monte Carlo Simulation

We perform the Monte Carlo simulation to include the effects of of capacitor mismatch. We discussed the generation of samples in detail in section 4.5.2. In this section, we use the average of one hundred samples as the representative value of each simulation.

Comparison of Barrel Shifting and Randomizing

We plot the relationship between the SNR and the oversampling ratio OSR with both randomizing and dynamic barrel shifting in Fig. 5.15. In this graph we change the OSR while we keep the simulation conditions listed in Table 5.1. The capacitor array mismatch in the simulation is assumed that 3σ = 0.5 and 1.0 %. The SNR obtained with barrel shifting is approximately 8dB better than that obtained by randomizing for the OSR more than 50. The dynamic barrel shifting is a promising architecture for multi-bit ΣΔ modulators.

SNR of the Four-Bit Second-Order ΣΔ Modulator

The SNR vs the OSR is shown in Fig. 5.16 for mismatch of 3σ = 0.01, 0.1, 0.2, 0.5, 1.0, 2.0, 5.0 %. The SNR for a one-bit ΣΔ modulator is also plotted for reference.

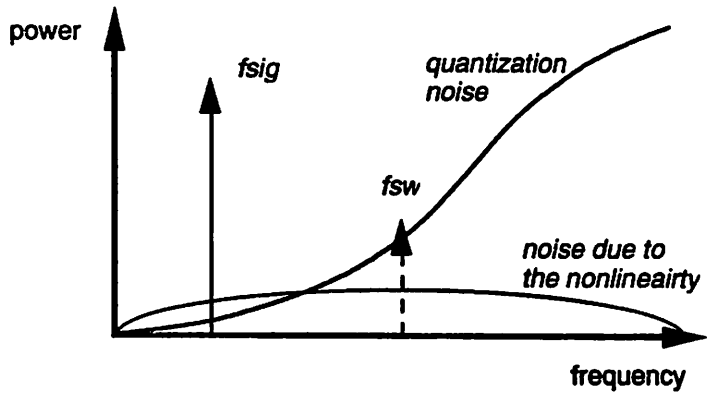
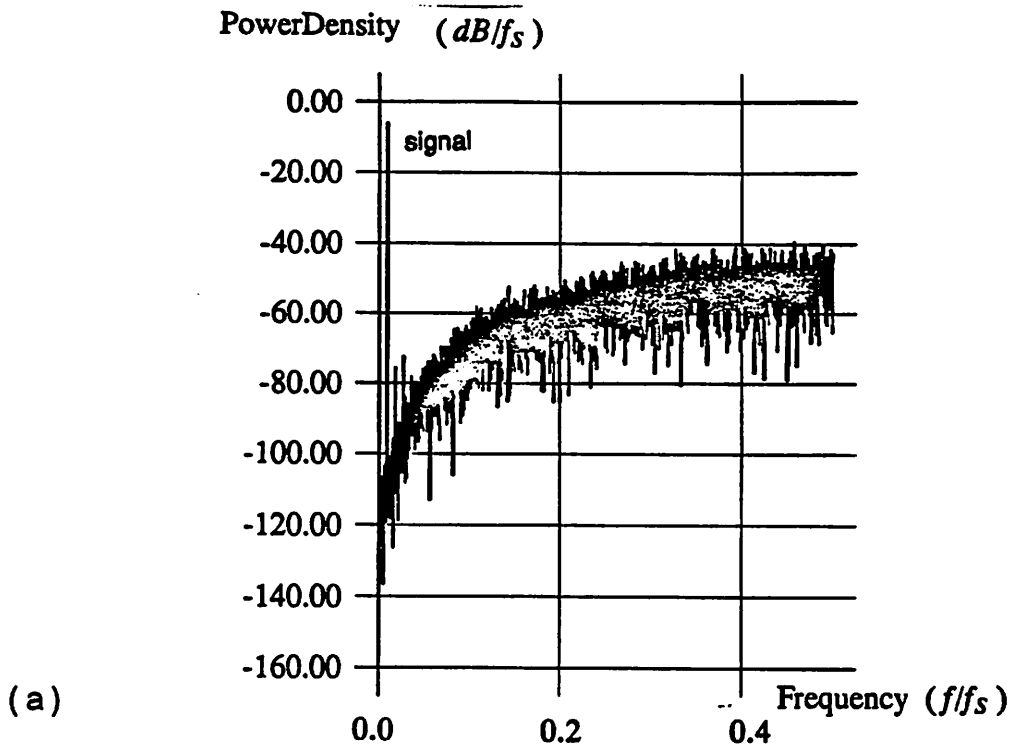


FIGURE 5.11 Noise due to the nonlinearity

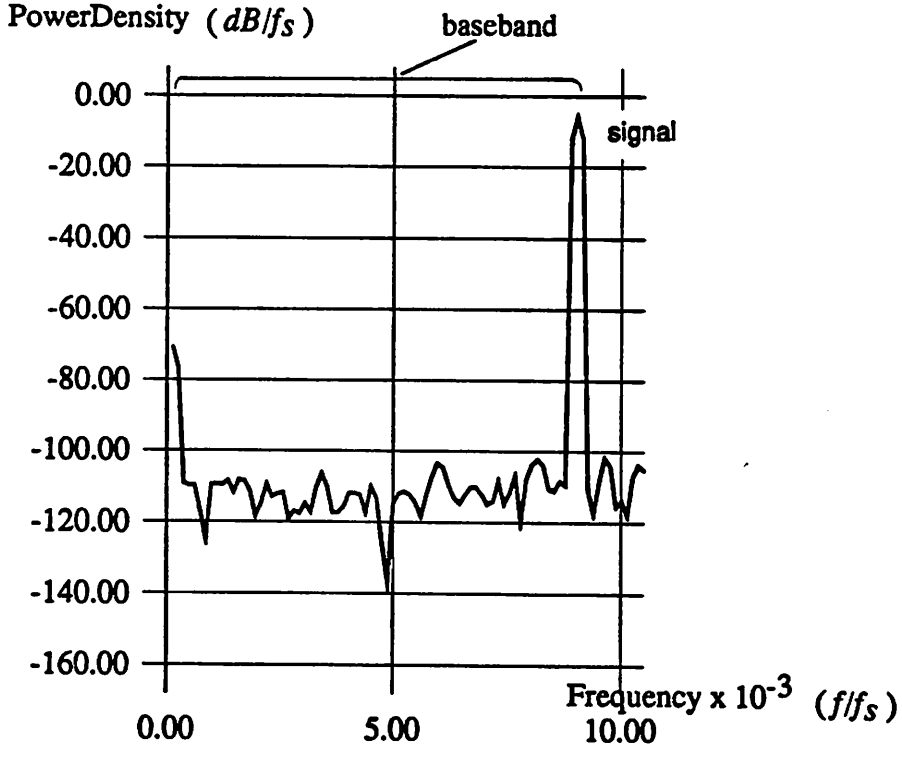
Although the SNR can be improved by the use of four-bit barrel shifting switching, it is obvious that the SNR is still limited by mismatch. We define SNR_{crit} as the value of the SNR which is just 6dB below the ideal SNR for each mismatch. Each SNR_{crit} is the intersection of (ideal SNR - 6dB) line and each SNR line. Slope of each line saturates (~6dB/oct.) after reaching this *SNRcrit* . The baseband noise due to the nonlinearity is larger than the original quantization noise beyond the *SNRcrit* as shown in Fig. 5.10. The increase of the SNR can be obtained only by the effect of increasing the sampling frequency f_S as discussed in section 2.2.2. Practical value of mismatch (3σ) is typically larger than 0.5% for standard CMOS technologies. It can be seen that the maximum SNR by the four-bit $\Sigma\Delta$ modulator is around 100dB(~16dB) for $3\sigma = 0.5\%$. Comparison with a one-bit modulator shows that the four-bit modulator has better performance for lower oversampling ratio (OSR < 100 for $3\sigma = 0.5\%$).

Comparison with the Four-Bit First-Order $\Sigma\Delta$ Modulator

We perform simulations for the four-bit first-order $\Sigma\Delta$ modulator to compare with the above results. The simulations show the effect of the order of noise shaping on the SNR. The SNR vs the OSR is plotted in Fig. 5.17. The SNR of the second-order modulator is much better than that of the first-order modulator for small OSR (smaller than 50). However, the SNRs for the same mismatch have the same asymptote for two different-order modulators for large OSR (larger than 50). We can conclude that the baseband noise due to the capacitor mismatch is the bottleneck for improvement of the maximum SNR, even if we use the dynamic barrel shifting allocation. Therefore, the use of higher-order filter in the feedback loop cannot increase the performance, if the noise due to the nonlinearity is larger than shaped quantization noise in the baseband.

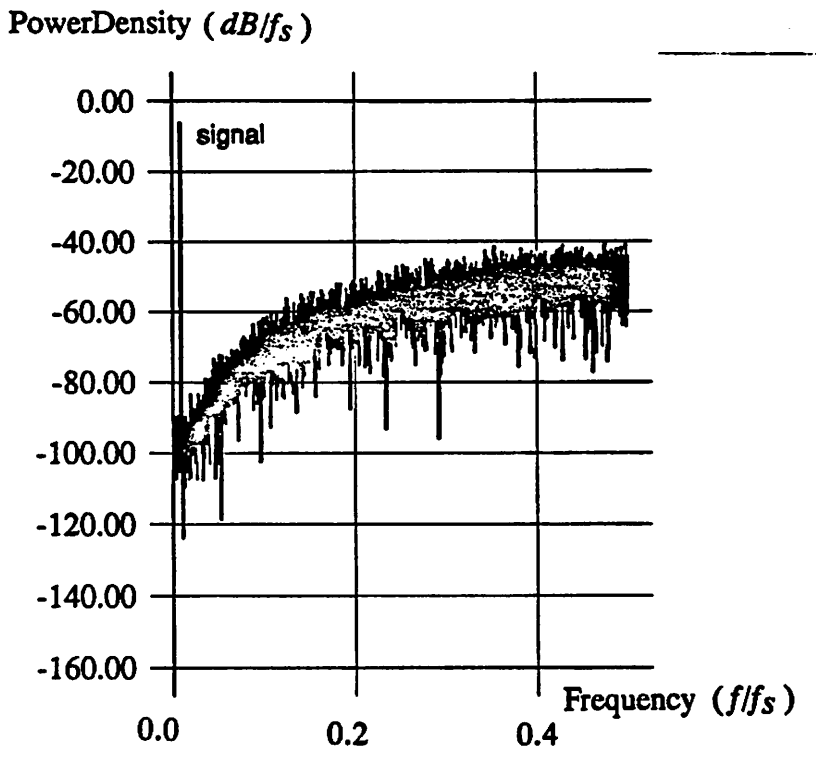


(a)

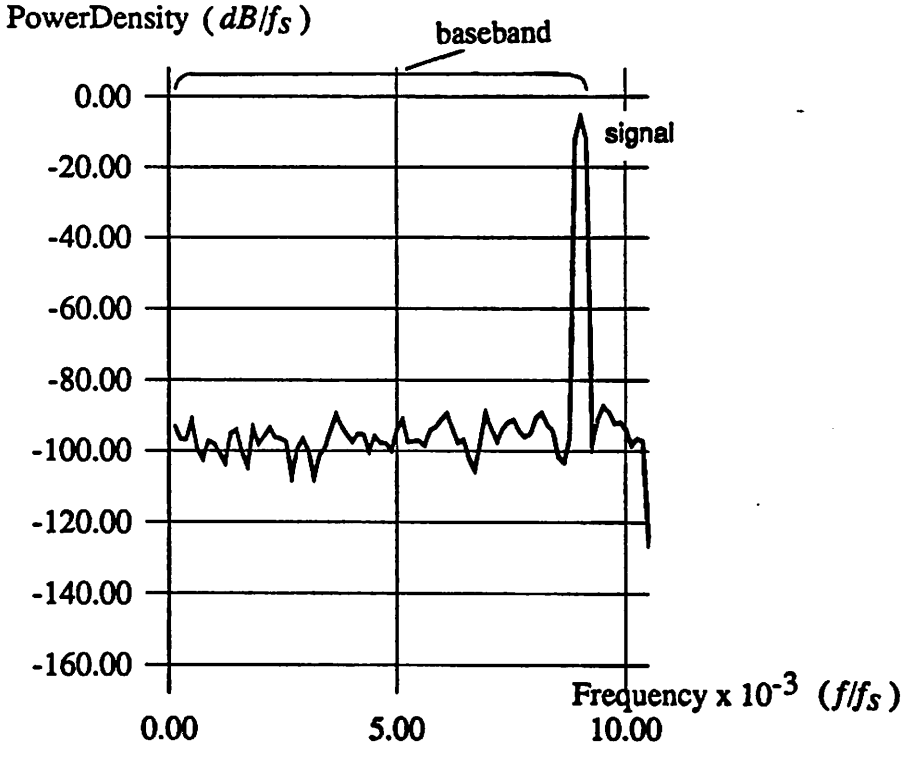


(b)

FIGURE 5.12 Spectral density distribution of the output
No switching CASE 1 signal power = -6dB
(a) dc to 0.5*fs*
(b) dc to 0.01 *fs*

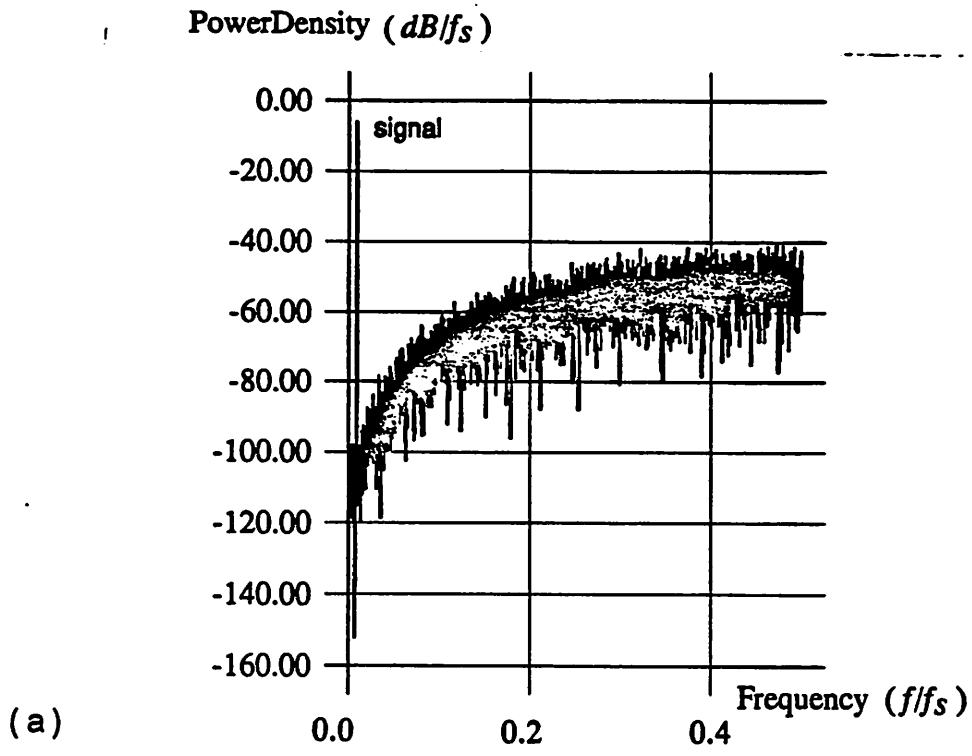


(a)

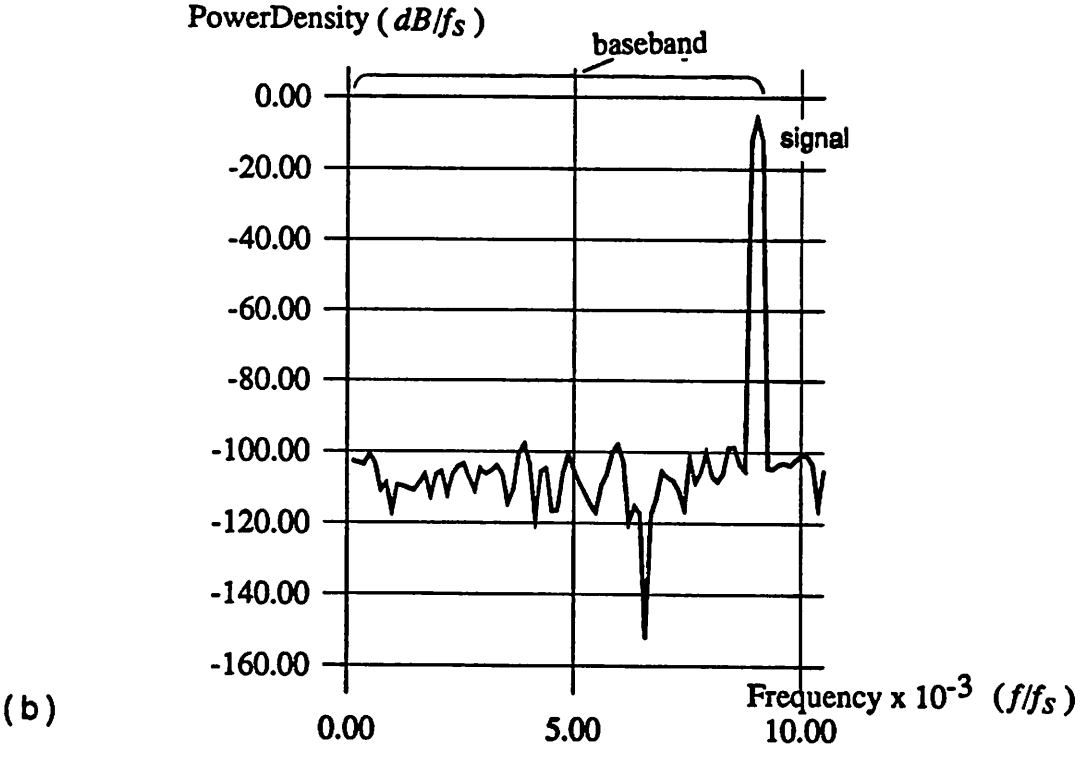


(b)

FIGURE 5.13 Spectral density distribution of the output
Randomozing CASE 1 signal power = -6dB
(a) dc to 0.5*fs*
(b) dc to 0.01 *fs*



(a)



(b)

FIGURE 5.14 Spectral density distribution of the output
Barrel shifting CASE 1 signal power = -6dB
(a) dc to 0.5*fs*
(b) dc to 0.01 *fs*

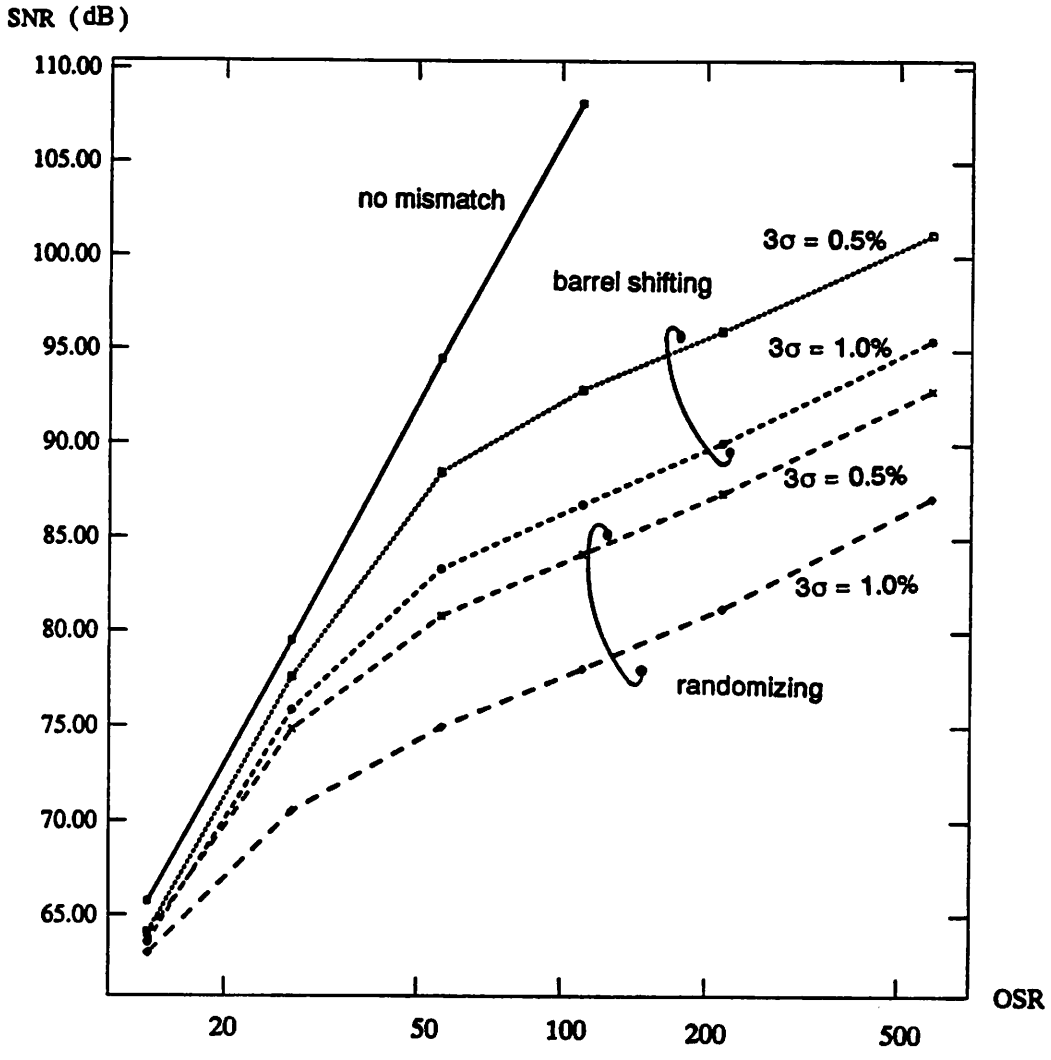
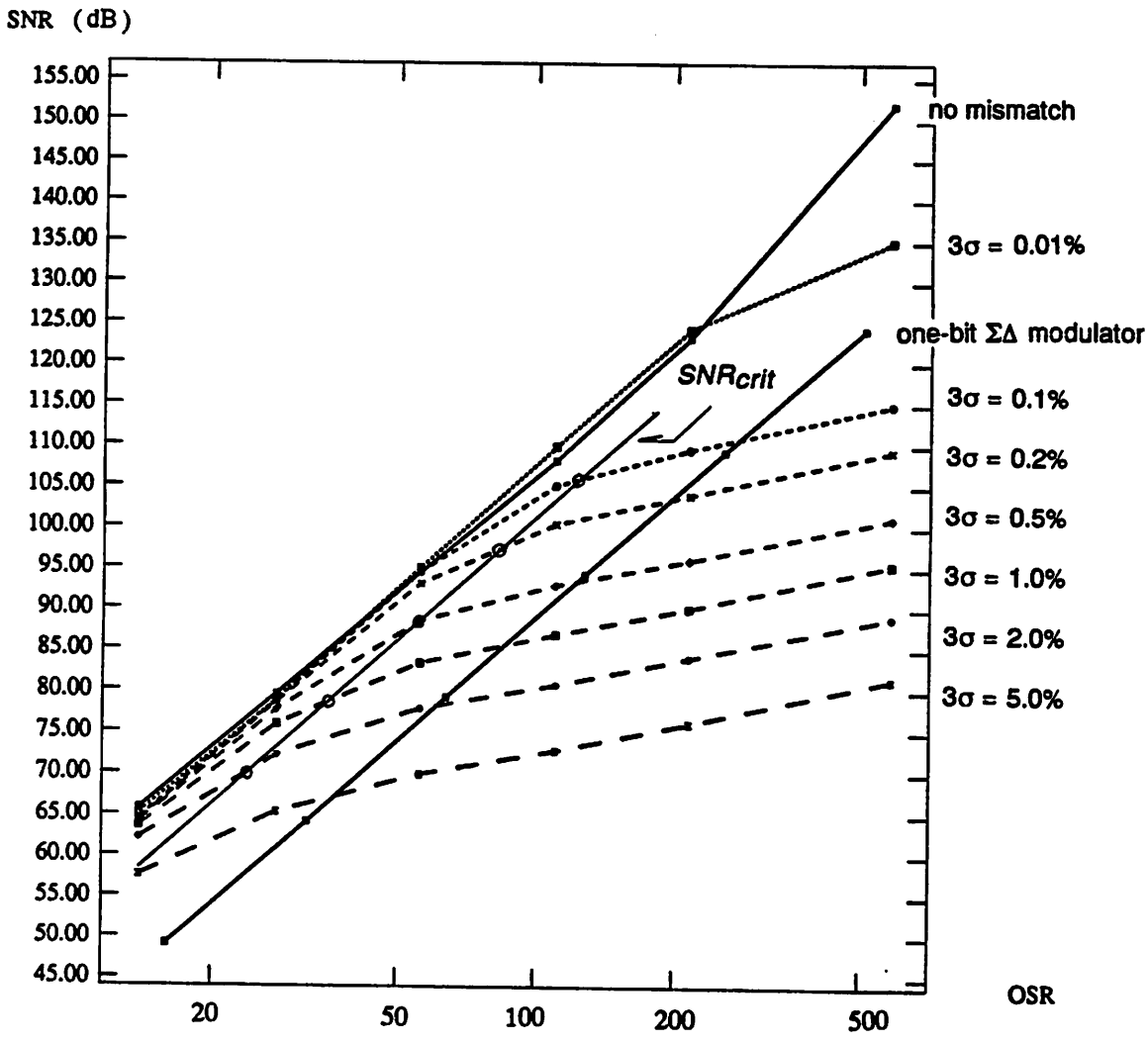


FIGURE 5.15 Signal to Noise Ratio vs Over Sampling Ratio of the four-bit second-order ΣΔ modulator
With randomizing and barrel shifting



SNRcrit : 6dB below the ideal *SNR*

FIGURE 5.16 Signal to Noise Ratio vs Over Sampling Ratio of the four-bit second-order ΣΔ modulator
Barrel shifting

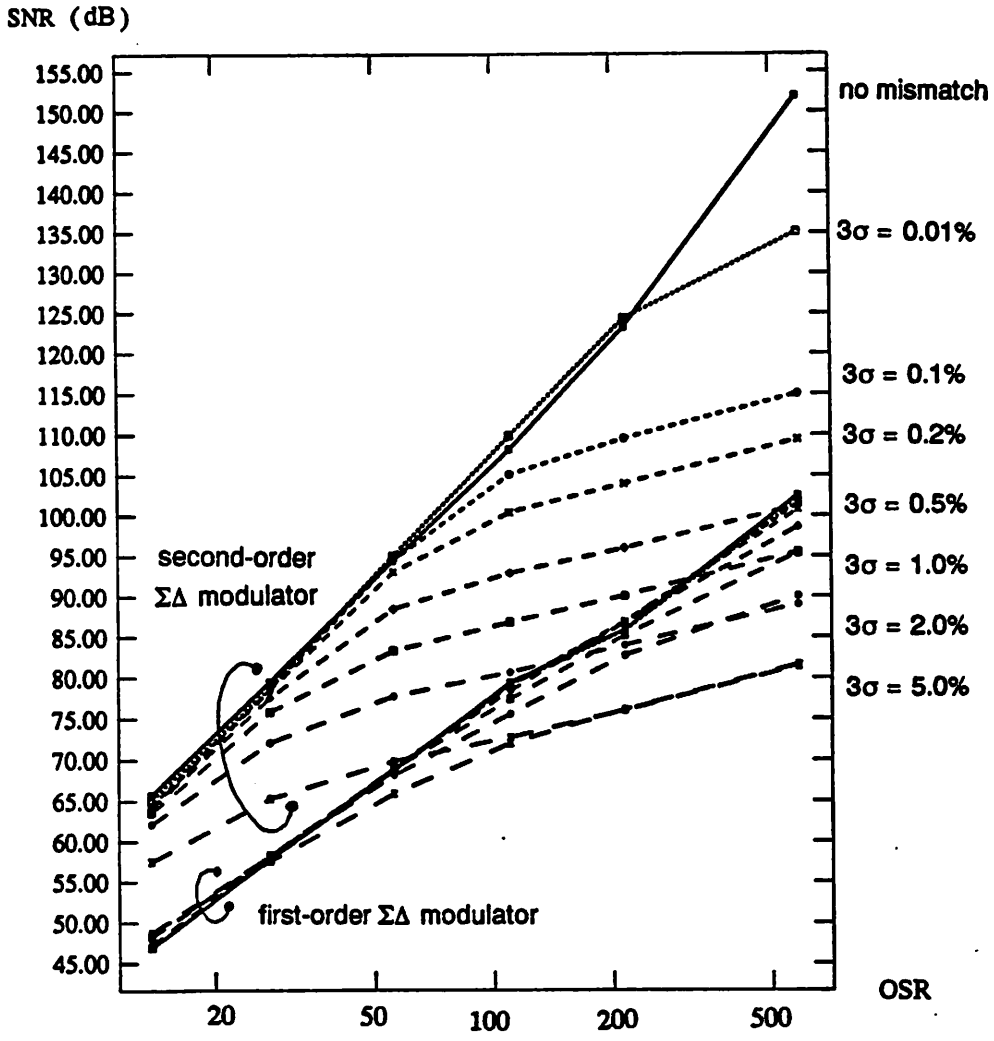


FIGURE 5.17 Signal to Noise Ratio vs Over Sampling Ratio of the four-bit first-order ΣΔ modulator
Barrel shifting

Chapter 6
Conclusions

Although single-bit second-order ΣΔ A/D converters are very attractive for medium-speed and high-resolution conversion (e.g. 14 bits, 80ksamples/sec. for 1.75μm CMOS technology), their performance is not sufficient to accomplish faster and higher-resolution conversion. We proposed a new architecture of a multi-bit ΣΔ modulator to see the feasibility of realizing higher performance of the modulator.

In general, performance of the multi-bit converter is severely degraded by D/A nonlinearity due to element mismatch. We introduced the dynamic barrel shifting for the allocation of unit elements of an internal DAC to reduce this degradation. This dynamic allocation moves the noise due to the nonlinearity out of the baseband, which results in the improvement of the SNR. A system-level simulator for a four-bit ΣΔ modulator was developed to analyze the behavior of the modulator. We obtained the following results by this investigation.

(1) Analog-circuit requirements for CMOS circuit implementation were presented. The requirements for op-amp open-loop gain and integrator closed-loop gain are similar to those for a one-bit ΣΔ modulator. The four-bit modulator requires larger bandwidth of op amps because it needs more accuracy for the settling. Slew rate requirement of op amps for the four-bit modulator is more relaxed because each step size between two quantization levels is much smaller.

(2) Effects of D/A element mismatch were discussed. The new dynamic barrel shifting can provide much better SNR than randomizing. For a four-bit modulator, the SNR obtained by the new barrel shifting is 8dB better than that obtained by randomizer. However, the maximum SNR is still limited by element mismatch of an internal DAC because baseband noise is not determined by shaped quantization noise but D/A nonlinearity. Therefore, the maximum SNR falls short of the ideal case of perfectly

matched elements in the DAC. The maximum SNR cannot be enhanced even with the use of a higher-order filter in the feedback loop. For a four-bit modulator, the maximum SNR for the mismatch of $3\sigma = 0.5\%$ is 100dB(~16bits).

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