White Paper

CONCURRENT CIRCUIT DESIGN/PROCESS ENGINEERING IN A FLEXIBLE MANUFACTURING ENVIRONMENT

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Andy Neureuther, Costas Spanos, Mark Hatzilambrou,
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Concurrent Circuit Design / Process Engineering in a Flexible Manufacturing Environment

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Abstract

The main idea presented in this paper is that the current sequential approach to circuit design, process development and IC manufacturing leads to serious inefficiencies. One of the major goals of the synthesis project should be to find ways to allow these three activities to be carried out concurrently by eliminating their current detachment. Towards this goal the University researchers participating in this study should contribute ideas which should address the current gaps in TCAD, CIM, CAM, etc. Examples of the time-activity lines of microprocessor design and change of a product to a new process technology are given and illustrate the need of an integrated and concurrent approach. We also suggest concepts for a synthesis framework and its functional components. We metaphorically call these key ideas "tent poles" to underscore the need to push out the interconnecting frameworks to support process synthesis.

1.0 Introduction

The lengthy 5 year development cycle for today's integrated circuits arises due to the nearly sequential phases of process design, circuit design and the eventual redesign cycles, needed to improve the manufacturability of the product. An additional delay is introduced when a newly developed process is transferred to a production line, or when a mature process is transferred across production facilities. While there are difficult technical issues in each of these phases, an integrated architecture for circuit design and process engineering in a flexible manufacturing environment would bring many advantages. These include coupling evolving technology and circuit design, leveraging equipment capabilities, and facilitating transfer of products and technology among production facilities.

Given the advances in computer integrated manufacturing, equipment characterization and process simulation, it is now possible to conceive of new integrated architectures for design and manufacturing, while still isolating the IC designer from any unnecessary complexities of IC processing. Very useful TCAD tools have been developed and work is continuing to fill the gaps to cover the latest innovations in process technology. At the same time CIM has become an accepted mainstream philosophy that has evolved to the point where it routinely collects, manages and uses production information in order to improve the efficiency of production.

We believe the opportunity is ripe to make a major step forward to couple the TCAD and CIM advances through the modern accomplishments of information technology. One key idea to support this merger is the use of "flexible design rules" as a base of communication which provides both the desired isolation for the designer and the flexibility for agile manufacturing. This integrated architecture will also support other activities such as detailed manufacturability analysis of processes and ICs, as well as automatic generation of equipment specific recipes, etc.

This white paper suggests how industry and academia can collaborate in a new paradigm for a process synthesis system in which universities contribute key ideas which extend the functionality of a robust software framework. We begin with the nature of product design and the methods by which the triumvirate of process technologists, circuit designers and manufacturing interact is examined. Two specific "tent pole" ideas are proposed which will promote concurrent circuit design and process engineering by: 1) folding a quantitative view of real manufacturing capabilities into the IC design and 2) creating links among process design, circuit design and manufacturing, so that they can proceed simultaneously rather than sequentially. In this paper we emphasize focal points with high payoff, and on how these focal points synergistically combine. The flow is as follows:

2.0 Nature of Product Design and Manufacturing - An Overview

2.1 Motivation and Breakthroughs Required

In the early 1980s a significant advance was realized when the Mead and Conway methodology introduced the concept of separation between IC design and IC manufacturing. This separation was facilitated by the introduction of a set of simplified, scalable design rules and made it possible for IC designers to work independently of processing technologies. This separation was made necessary by the complexity of the tasks involved, but it had a serious disadvantage as well: the artificial simplicity of the scalable design rules failed to capture many subtle, but also important aspects in the interaction between the IC design and the underlying manufacturing technology.

Due to the increasing cost of manufacturing facilities, there is renewed interest in exploring new options to amortize costs over a greater variety of products. Important directions include improving products within the fab, migrating older products between fabs, and seeking new products for excess capacity. As production issues become well understood, the conservative design rules from the initial design can be replaced by product shrinks to reduce die area and improve the yield of highest performance parts. With additional flexibility in generating process flows and detailed process specifications, products could more quickly be transferred across fabs. Fabs can take advantage of this flexibility by acting as a foundry for special designs, and by second sourcing popular parts. With minor process extensions it would also be possible to pursue joint ventures for manufacture of low volume, high performance parts which draw premium prices.

Pursuing any of these options for extending the flexible use of fabrication facilities requires a major breakthrough in the level of integration of circuit design, process technology, and manufacturing. Expertise from various domains must be folded together in a seamless manner with rapid communications to address the complex tradeoffs which propagate throughout the design and fabrication of a complex IC product.

One of the basic problems in folding together the expertise to make new products is the lack of fine grain granularity in coordinating development efforts. Today, most organizations have several separate traditional "centers of expertise", such as mask making, lithography, etching, metallization, etc. For a new product, each of these centers of expertise must deliver masks, linewidths, etc. to a certain commonly agreed to specification. Traditionally, each center is only willing to commit to conservative specifications, effectively blocking new and risky concepts from being realized. One interesting example is the improvement of optical lithography through modified illumination and phase-shift masks. Despite the demand, lithographers are worried about all the pattern dependent cases they must look at, and most mask shops will refuse to make or inspect new types of masks in-house.

The artificial granularity and all-or-nothing nature of the tasks to which the various centers of expertise have to commit must be replaced. This granularity is exemplified by the major barriers built into the design-rules, which usually take effect years before production. Each center of expertise needs to be motivated by quantitatively visualizing how a minor compromise on their part could lead to a significant product improvement. This visualization requires seamless communication among all centers.

Further problems exist today as a new technology and a new design move to production. Depending on the specific equipment setup of a facility, the final details of the production sequence are usually fleshed out only after extensive experimentation. In addition, since successful production depends on the precarious balance of specifications across several, poorly communicating centers of expertise, once the process is deployed, it is extremely rigid. While process specifications are rigid, however, the fabrication line is usually undergoing continuous changes, due to equipment upgrades, maintenance operations, aging, malfunctions, etc. A new methodology of describing process specifications is needed, one that can lead to a flexible description that will allow quick and flexible application to accommodate change, and to facilitate the profitable transfer of a technology across processing facilities.

These needs for seamless communication among IC design, process design and IC manufacture are highlighted by the two examples of time-line activities that follow.

2.2 Example of Time-Activity Line in Microprocessor Design

State of the art design involves an increasing degree of concurrency in the process/product/manufacturing flow. The approach used and time-activity line will of course vary from product to product and from company to company for the same type of product. One of the most interesting and perhaps most complex examples which exacerbates design integration issues is that of the microprocessor. Here the product design and shake out of manufacturing can take up to six years.

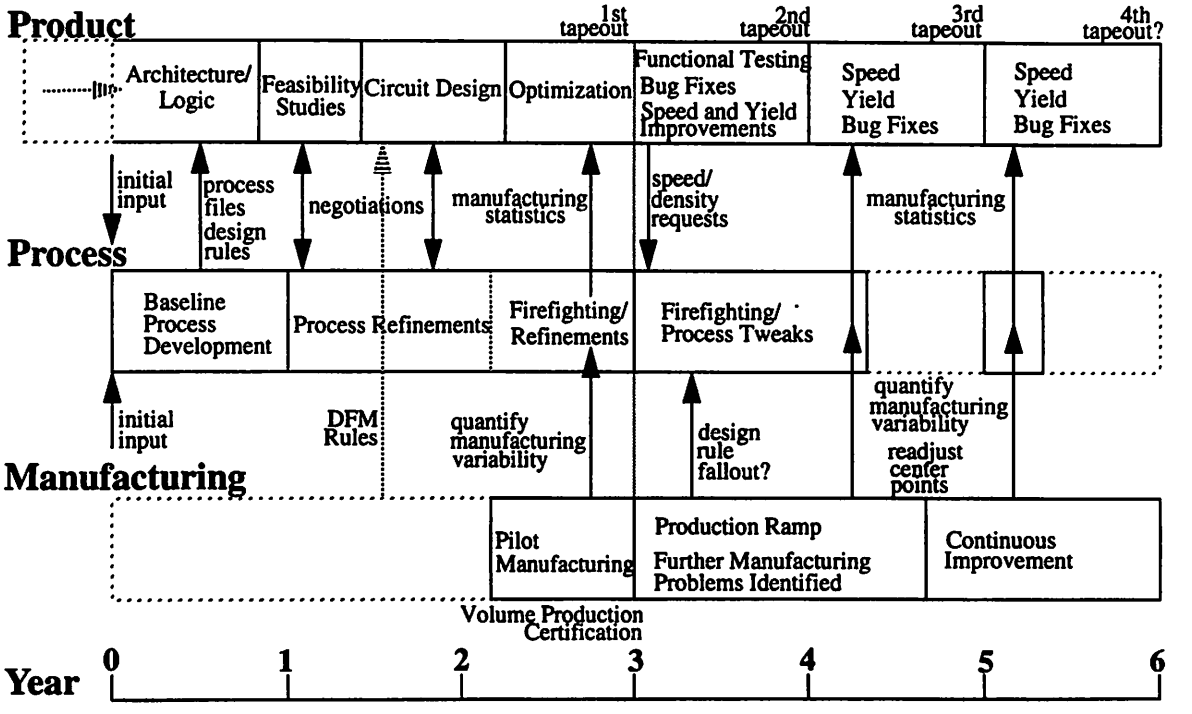

Figure 1 Microprocessor Development and Production Time-Activity Line

Figure 1 shows a typical time-activity line for microprocessor development, with time increasing left to right. Year zero is set at the start of process development, although product definition, architecture, and even some logic design usually precede this. The separate activities of the product, process, and manufacturing groups are broadly stated and positioned in time, and of course large intra-group activity overlap occurs. The vertical arrows indicate the timing and direction of key communications between the three groups. As complex as this figure is, not all activities and communications such as updates of process files, and speed and density requests can be shown. Also, intra-group activities are usually not distinct and occur multiple times.

The product team consists of architects, logic designers, and circuit designers specific to a particular product. This product is generally one of several lead vehicles designed for the new process. The product may be a shrink of an existing design, transferring an established design to a new technology, or it may be a next generation processor. The process team consists of process technologists and device physicists who develop the new process with guidance from negotiations with lead vehicle product teams, and are generally responsible for all aspects of the process through transfer to manufacturing and volume certification, which typically happens about three years into the cycle. Manufacturing team involvement begins in earnest with the pilot manufacturing phase and is responsible for process maintenance beyond volume certification. After the first tapeout, also in year three, product teams seek to redesign for functionality, performance (speed), and yield, and process teams are called upon to update the process according to product needs or process design induced yield fallout.

At the inception of process development, product teams provide expectations and needs to the process team; manufacturing also provides limited input (a new suite of process equipment is generally employed). Process teams must provide design rules and process files to the product teams before significant physical design may begin. Negotiations between the process teams and various product groups typically involve results and needs that are hand carried through designated interface personnel. Near the inception of physical design, design for manufacturability (DFM) rules are sent from manufacturing teams to the product teams in the form of hard copy rules. Pilot manufacturing, designed to identify production problems, uses very little current product results, relying more heavily upon prior manufacturing experience. Manufacturing teams quantify process variability and communicate this to product teams in the form of statistical process files for circuit design. During development, the communication between process and product teams is largely one-way. During the manufacturing phase, product teams and manufacturing associate more closely, with manufacturing providing yield feedback and product teams communicating needs. Process teams may be called upon to make process changes which may or may not be product specific.

2.3 Example Time-Activity Line for Technology Transfer

New process introduction is a very complex and expensive activity and is usually coincident with the design of a major IC product, as described in Section 2.2 above. In this session we highlight the sequence involved in transferring an existing technology from one fabrication line to another.

As technology evolves and markets change, companies often find it necessary to either move an older IC design to a newer technology, or to second-source an existing design, by transferring its technology to another facility. Both activities are very energy and time consuming.

Highlighting the procedure for technology transfer will help highlight some of the problems in it. Manufacturing technologies are usually characterized by their level of maturity as they move from early development into the pilot production stage and finally go into the high volume production stage. Most companies will attempt to specify the maturity of the production line with even greater granularity, by using several composite figures of merit. Such figures involve defect density, yield, cycle time, key process capabilities (Cp, Cpk, etc.), IC reliability levels, etc. In most cases the maturity of the production line is a composite measure of overall wafer and die yield, and of the collective capability of 10-20 critical steps, such as gate oxidation, critical dimension definition, contact opening, metallization, etc. As shown in Figure 2, technology transfer consists of several stages of transferring and confirming information and abstract knowhow between facilities. During these stages the originating site defines transferable "modules" of the technology. Then, the receiving facility starts a baseline operation, goes into pilot productions and finally starts volume production following a schedule similar (even though shorter) to the schedule followed when the process was developed for the first time. Although the figures vary, it might take up to two years to move a technology from the development stage to the full production stage. Continuous improvements usually continue throughout the life of the process.

When a mature process needs to be duplicated on a different facility, however, one would expect that it would reach maturity faster. Although this is generally the case, there is still a period of learning that can take up to one year, even if the transferred process was at the high volume production stage. The reason for this new learning stage is that fabrication lines are never identical. This has two strong implications: First a process can never be transferred at the lowest level of abstraction, that of equipment-specific recipes and specifications. Instead, we usually transfer the process in terms of a process-step specifications (oxide thicknesses, doping levels, etc.) In general, new equipment level specifications and recipes have to be developed at the receiving site.

The second major implication of having different equipment at the receiving site is that new yield loss mechanisms might be revealed, owing to defect sources that are unique to the new facility. Also, since equipment recipes have changed, new unanticipated interactions among steps might come into play and further reduce yield and reliability.

In order to cope with all these problems, the accepted practice for process technology transfer today involves dispatching a team of process experts from the originating site to the receiving site. This is because it is believed that successful development of a new technology (or transfer of an old one), depends on human experience gained with this technology. Such human experience involves an intuitive understanding of process step interactions and yield loss mechanisms. It is further believed that such experience is so subtle that it cannot be effectively captured by CAD/CAM tools, or even documented on paper. Therefore transfer is done using techniques ranging from trial and error, to extensive, statistically based experimentation.

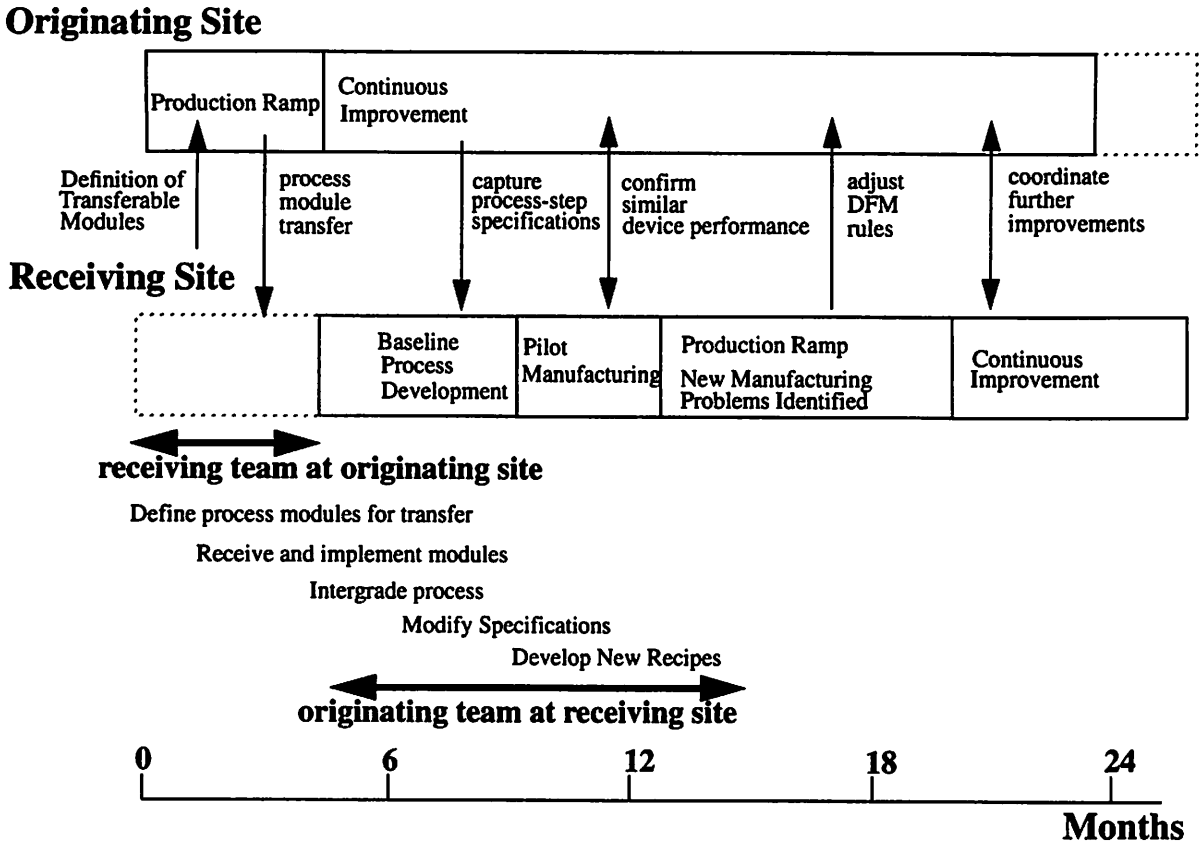

Figure 2 Technology Transfer Timeline.

3.0 Process/Circuit/Manufacturing Integration Issues

3.1 Major Findings from Interviews with Industrial Teams

Through informal discussions with a variety of technologists, circuit designers and production engineers throughout the IC industry we have identified several major problem areas common to the IC industry. We were surprised by the wide difference in approaches used to communicate among the process, design and manufacturing teams. In one case a coordination czar took all responsibility for process impact and fed the circuits group nonagressive design rules which could be scaled for 3 generations and associated SPICE parameters for each of the generations. Another company making the same product used separate teams for each generation and aggressive dimension specific design rules. A third company with a superior process technology base felt it could take either of these designs and manufacture them with even higher clock speeds. In a fourth company all 50 process, IC design and experienced production engineers met once ever two weeks for a half day in order to exchange information.

Regardless of approach, all of these companies seemed to have the same major snags, that yield learning is slow, as illustrated by Figure 3. In this figure we show defect density (extracted from normalized yield of devices of similar complexity) versus time for a number of different production lines that make similar products. It is evident that the companies represented in this graph experience very similar yield learning rates as their processes moved to maturity. It is also evident that the industry as a whole is benefiting from better tools and a progressively better "global" knowhow. The rate of improvement, however, is still slow and it highlights the importance of this problem: that yield learning takes years is an indication of the significant role of equipment issues on yield. Clearly the results of the yield learning experience should be fed back into the design of new products.

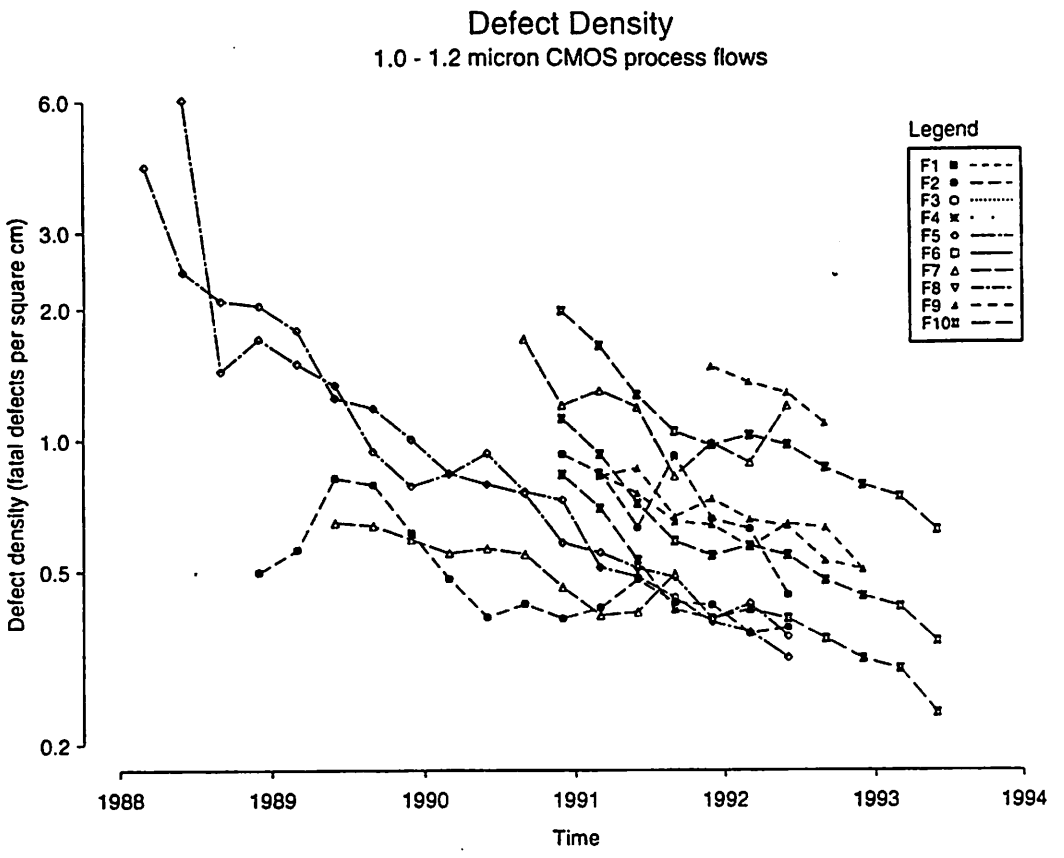

Figure 3 Defect Densities vs. Time: 1.0-1.2 micron CMOS Process Flows.(Source: The Competitive Semiconductor Manufacturing Survey: First Report on Results of the Main Phase, Report CSM-02, 4/2/1993, University of CA, Berkeley).

Another major finding in discussions throughout industry is that the design process is based on the 'art of historical hunches' rather than quantitative science. To get the design moving early, a historical extrapolation of data is made to define design rules and circuit models. No one dares to use the worst case "slow" and worst case "fast" circuit models because they are so extreme. Instead, someone makes a judgement call as to suitable values for the typical fast and typical slow SPICE parameters. Circuit designers find it difficult to live with the large guard band even in these typical cases. For the most critical path cases circuit designers may even deliberately violate the layout rules based on their hunch that the circuit should yield anyway. Since there is no effective means of coordinating and systematically testing these design choices, there are a lot of nervous people when the design moves to manufacturing, as they bet their own and their companies future on everyone's hunches being correct.

Another problem is what we will call the 'untested case gotcha.' This problem typically arises immediately because the designer uses a combination of mask level patterns which was not actually incorporated in the process development test masks. A very common example is patterning of fine features near the edge of groups of features in an underlying area. The underlying layer topography can affect the thickness of the resist coating and/or reflect light and thus affect the lithographic process. The use of several

tapeouts after a product is transferred to manufacturing as mentioned in the microprocessor example is indicative of this problem. Several catastrophic show stoppers almost always occur with every product which changes design, process or equipment even in a minor way. Generally it takes from a month to six months to resolve a gotcha, and manufacturing must firefight several simultaneous gotchas which confound one other. Resolving the issues may require equipment, process conditions, layout and even circuit design changes.

Insidious "in-specification gotchas" also occur. These are hidden in the sense that they occur when everything is within the design specification. For example, the layout passes the design rule check, the equipment is functioning to within the vendor's specifications, and the thin-films have the thickness allowed in the process. Yet, for example, a sudden dropout of the alignment signal occurs due to subtle in specification changes in the topography of the alignment mark. These gotchas more than likely occur after the volume starts ramping up and the process parameters are migrating toward a new setpoint in addressing other problems.

3.2 Problems Identified in the Microprocessor Timeline Example

Despite a great deal of concurrency, the process, circuit, and manufacturing groups remain largely insulated from each other, with only a few well-guarded bridges connecting them. While this isolation increases simplicity and manageability, it also limits the sharing of expertise. This is most significant for guidelines which must be followed without CAD enforcement; designers may overlook those rules which they find less important when it comes to schedule crunch time, e.g. DFM rules may get short shrift if they are only in the form of hard copy guidelines.

Communication between product teams and manufacturing teams during initial design is mostly one-way. This necessitates the prescience of process and manufacturing teams to provide comprehensive electrical and DFM rules up front. Again, these rules are manually checked with great impact to design efficiency. Moreover, DFM rules are not generally show stoppers, so cost tradeoffs need to be considered in enforcing them.

The attempt at concurrency leads to shorter design time but greater redesign effort. Initial process files for circuit simulation often contain enough error to affect the initial partitioning of logic pipelines. Uncertainty also pushes out the circuit design cycle. In addition, CAD tools used by designers are based upon older generation of process technology; without updating the likes of automated place and route tools, highest performance from the new process cannot be expected.

So, concurrent design is critically dependent on a common media for assessing tradeoffs. Historically, the design rules have served this purpose, through several different, but similar approaches. At this point it becomes apparent that one needs to extend the existing scope of design rules to make them a more affective media for transferring information to the IC designers.

3.3 Problems Identified in the Technology Transfer Example

Today a manufacturing process is transferred by trial and error. Briefly, the process is first set by linking various newly transferred steps together. Then the integrated process is tried and the various step-interaction problems are solved one at a time. Pilot runs

reveal more problems and finally, volume production reveals more subtle, "yield detractors", long term reliability issues, etc. During this period, as problems in the process are being fixed, the IC design might go through revisions, either to meet new unforeseen objectives, or to fix performance problems that were not anticipated during design. Sometimes IC design changes are implemented to bypass manufacturability bottlenecks.

All these activities are complicated by the lack of formalized information. Again, the conclusion is that successful process development and technology transfer will benefit from a well structured depository of information, such as the one that would be required to drive the new concept of "design rules" mentioned above. This issue will be discussed in more detail next.

3.4 Technology Development Example

Data published by K. Early et al. of AMD in connection with studies of the cost of ownership of lithography tools can also be used to get insight into the extent to which redesign takes place once a product reaches manufacturing. Figure 4, taken from their paper shows the number of wafers processed with each mask set for 134 different device numbers during one year. Although the details as to why any given mask set was discontinued were kept proprietary, we can make our own estimates for how it relates to process development efforts. This data probably relates to approximately 20 different products at various stages of development. Probably about 10 products are very mature as the 10 mask sets with more than 10,000 wafer exposures of 8% of the masks account for 54% of the exposures. While some new and old products were caught waxing and waning in the one year snapshot, one might surmise that 80% of the mask sets were made in developing new products and probably as many as 60% of the masks were made in addressing manufacturing issues.

The 60% of masks sets remade for addressing manufacturing issues might break down as follows. 23% of the masks were used for less than 100 wafers, probably because of immediate gotchas, which only took a few $M in masks and wafers and a few weeks delay to eliminate. Another 36% of the masks were used for between 100 and 600 wafers. Probably 2/3 of these masks were generated due to performance issues which took several months to identify and redesign at a cost of about $20M. The 34% of the masks used for between 700 and 10,000 wafers probably involved yield learning. If 1/3 of

these masks and associated wafer exposures could be eliminated, a savings of up to $75M might be made.

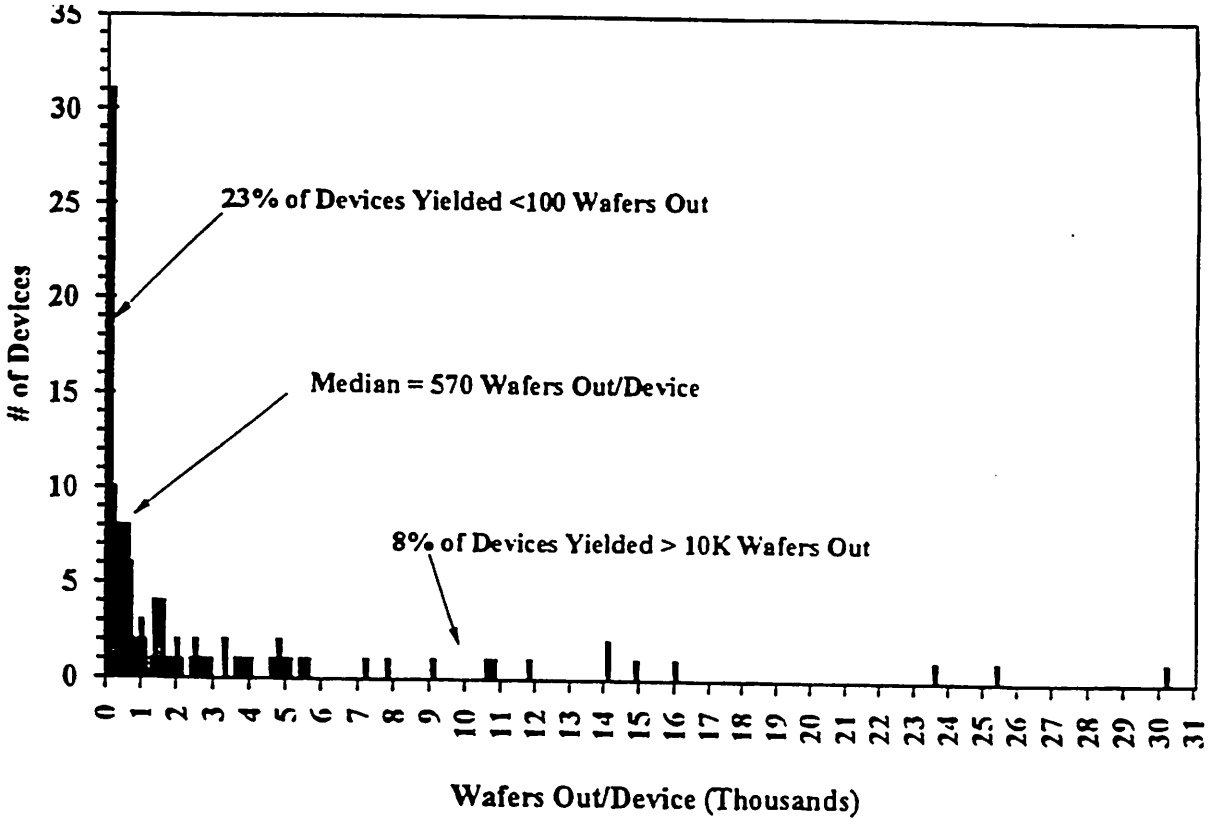

Figure 4 Yearly Reticle Usage Distributions form "Cost of Ownership" by K. Early et al. Photomask Technology and Management '93, 22-24 Sept. 1993, Santa Clara CA.

4.0 A Process Synthesis Paradigm - Problems and Opportunities

In this chapter we summarize the problems, the requirements and the foundations for new solutions.

4.1 Summary of Current Problems

In summary, the following are the major problems we have identified so far. Two of these problems have to do with technology development and transfer:

- Poorly understood interactions among process steps. This leads to the late discovery of showstoppers during high volume production.
- Inadequate equipment understanding and modeling. This leads to extremely complicated technology transfer, as many parts of the process must be reinvented before they can be transferred to a new line.

Another two problems have to do with the lack of sufficient communications among the interacting groups of IC designers, process developers and manufacturing engineers:

- No connections between TCAD Frameworks and Manufacturing Information Systems. Because of this there is no way to use DFM rule checking within the current CAD systems.
- Inadequate expertise sharing among circuit designers, process developers and manufacturing engineers. One manifestation of this is that there is no way to allow the circuit designer to "turn on" increasing levels of process and manufacturing knowledge where it is needed.

One result of these problems is the lengthy cycle of product introduction and revision due to missing interaction opportunities among the primary entities. The current nature of the design rules and the way they are used is at the core of these problems. The empirical, almost mystical "know how" of the various experts is another symptom of the same problem.

4.2 Current Foundation and Opportunities for Novel Solutions

To remedy the above mentioned problems we need to envision a new infrastructure of experience. This infrastructure should serve the purpose of process synthesis at the various levels of abstraction outlined in Figure 5.

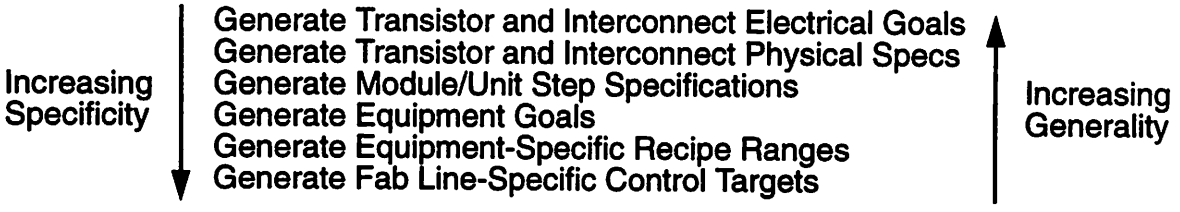

Figure 5 The Various Levels of Abstraction for Process Synthesis

This infrastructure will have several key "ingredients" and will facilitate several key synthesis applications, as illustrated in Figure 6.

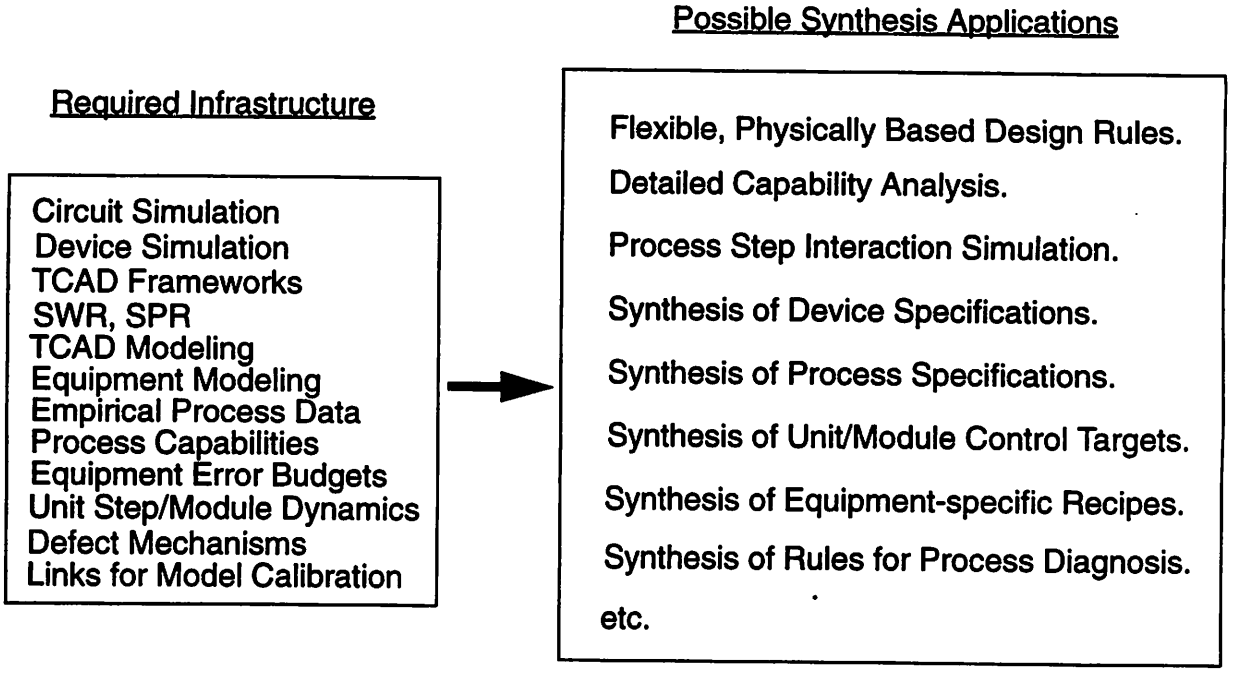

Figure 6 The new Knowledge Infrastructure with its key Ingredients and Applications

It is noteworthy that most of the required ingredients are already subjects of well focused, mature development efforts. As such, these ingredients form the current infrastructure of the process synthesis effort.

Concurrent design and manufacturing integration will rely heavily on IC and Technology CAD. Traditional IC Circuit CAD and even device simulation are generally in usable shape. However, the SIA road map identifies a major list of developments which will be necessary in process simulation. In the lithography area the gaps in simulation are in modeling resist spinning, 3-D substrate effects during exposure, and getting adequate models for positive-type chemically-amplified resists. We believe that many of these shortcomings will be addressed by focusing SRC and Sematech activities on the SIA roadmap. This advance in process simulation should thus provide an important enabling factor for integration of process, IC design and manufacturing.

Another important enabling factor is the recent emphasis on integrating process simulators in to a framework with a common wafer process flow representation. A system architecture shopping list was envisioned early on, and work on wafer topography representation standards (SWR) and process flow representation standards (SPR) is now beginning to produce working specifications. The recent funding of work toward the commercial realization of a Lithography Work Bench is a milestone in linking simulators as in an actual process flow.

Empirical characterization of manufacturing equipment has undergone a similar rapid growth to now also serve as an enabling factor. More specifically, there have been numerous recent developments of robust statistical techniques for equipment modeling and control, in conjunction with many real-time monitoring applications, phenomenological modeling, expert diagnosis, etc. These developments and their continuation as outlined in the SIA roadmap will form another basic enabling factor for streamlining the synthesis effort at the lowest level of abstraction. At this level, equipment specific recipes and control goals will be generated, in order to facilitate both primary technology development and technology transfer. Such low-level synthesis will leverage the recent standardization efforts led by Sematech and will build on ideas demonstrated by academia and industry (most notably within the MMST program).

For example, data from short-loop electrical structures can be collected quickly and in quantity. Statistical averaging and the inherent sensitivity of electrical measurements allow us to characterize process parameters with detail and accuracy not possible with other metrology methods, such as SEM. The test strategy can be designed to map the CD response for a variety of structures and linewidths over the entire wafer. Data from these electrical tests reveal non-uniformities introduced by the equipment which contributes to the total CD error that we observe. This gives us the as of now discarded opportunity to systematically identify, isolate, characterize, and remove or model deterministic variation introduced by the equipment. This information would allow process developers to formulate a metric based on the contribution to total CD error from individual pieces of equipment. Also, error in the form of systematic non-uniformities in the equipment can be minimized by optimizing the process control settings. The spread in circuit performance parameters can be determined as a function of the variability in the process equipment and the process parameters. From this, flexible circuit design rules can be generated.

We envision an opportunity which goes beyond the current development efforts, by working towards a framework which supports concurrent product design, process development and manufacturing. Such a system would allow designs to be tuned at a fine level of granularity to share learning between products. It would also give special emphasis to the strength which comes through the integration of empirical characterization and physically based modeling. More specifically, where new processes come on line too rapidly to be simulated from first principles, empirical characterization can fill in the gaps. This might provide evidence of important new physical aspects that might be modelled in the future and therefore drive more realistic modeling, capture and explain process dynamics in order to suggest proper cooperative action, and also make IC design immune to the most common sources of process variability. Complete process flow simulation can then be carried out to quickly assess design issues at a generic level. To drive the actual yield learning which is essential in making a processes cost competitive, functional equipment data can be downloaded into the simulation assessment.

Finally, the overall framework will be an information repository that captures the three major IC production stages as well as their critical linkages. To accomplish this, the structure of the information model (schema) of this database should allow highly integrated design functions: addressing cross views in design, communication of fine granularity for change, sharing between products, etc. This will comprise a "living design" which can be

molded continuously. These communication links are particularly important for companies that are typically organized into distinct centers of expertise.

5.0 A Process Synthesis Paradigm - Solutions and Players

5.1 The Berkeley Proposed Research

The combined Industry and University effort on Process Synthesis offers a unique opportunity to both create and verify the success of a new paradigm for IC manufacturing and chip design, based on a higher level architecture with solid infrastructure, extensible interfaces, and key new functional components. The new architecture will pull together at a higher level the strengths of the CFI efforts on wafer and process representation, the Sematech efforts on equipment standardization and modeling, exploratory University work on equipment characterization and manufacturing, as well as traditional university work on process and device simulation. These strengths will be molded into a supporting infrastructure with flexible interfaces to go after new high level functionality as the tent poles of the new architecture. To demonstrate how the various aspects of the new paradigm can make a difference, the evaluation at various levels including use on the product design test vehicles should be carried out.

As Universities we hope to be able to contribute new tent pole ideas for key functionality as well as to help define the architecture and contribute functional pieces from ongoing research. Our objectives at Berkeley are:

1. To fold in manufacturing data for flexible process step specification and supervisory process control into the product design.
2. To develop an information and design system concepts which allow the process, circuit and manufacturing views of an IC product to be carried out concurrently and continuously instead of sequentially and through complete redesign.

Vehicles which would demonstrate our tent pole ideas are:

- The testing of the concepts to address the gotchas and optimization issues which arise in moving an actual layout into production.
- The experimental demonstration of machine-specific processing instructions from high level description of device properties.
- The participation in a collective effort in building a verification IC utilizing the developed process synthesis tools.
- The cooperation with commercial participants to promote technology transfer and commercialization of the developed tools.

The architecture of the new information and design system might be viewed as consisting of a collection of data, interfaces to the data, and analysis and design tools in a central compository. This centralized data and services at this new higher level of integration would facilitate the rapid development of new separate functionality objects.

An example function might capture manufacturing data for the database and provide information from the data and process for supervisory control. A second function might proof read a multilevel mask layout and associated process flow with real equipment characteristics for potential problems in manufacturing. As a collection of functional objects builds up, more and more the functionality could move from individual design

considerations to interlinking concurrent process, circuit and manufacturing design considerations.

Finally, at the crucial link between design and manufacturing, we will utilize the concept of the "flexible design rules", rules that are based as much as possible to the physics of the process, and have two distinct roles. The first role is the "grade" the design by calculating a suitably defined manufacturability metric. The second role is to tabulate the manufacturability bottlenecks of the process. These issues will be discussed in some detail below.

Historically, the design rules have facilitated communication. The lambda scaled approach of Conway and Mead partitioned the problem so that the IC designer could focus on the design with only a simplistic view of process and manufacturing. With today's TCAD and CAM/CIM enabling infrastructure we are now in a position to reintegrate with gray levels which can be adjusted according to market placement strategy. In such a system one could envision:

- Product planners using tools based on the flexible design rules in order to evaluate strategic choices of manufacturability objectives.
- IC Designers requesting physical views of what their layout would produce on the wafer.
- IC Designers requesting data on performance yield versus manufacturing yield in tuning the critical path.
- IC Designers requesting circuit simulation data based on the layout structures and actual stepper linewith variation across the die.
- IC designers testing for correlation in parameter effects on circuit performance which reduce the worst case guard bands.
- Process technologists checking for mask combinations being used by designers which they should include on test masks.
- Manufacturing engineers checking circuit performance for tool to tool and run to run variations.
- Manufacturing engineers performing detailed error budget analysis based on simulation and empirical data, in order to identify manufacturability bottlenecks.
- Manufacturing engineers automatically generating equipment specific goals and control specs for efficient process deployment on a new production line.

Another objective of this study is to develop equipment models that have time-predictive behavior. The empirical equipment models we currently use have no notion of time or cumulative process history. In other words, they are capable of predicting changes in wafer status as a function of current operating conditions. These models can account for changes only through statistical adaptation based on recent process observations. Although empirical adaptation will be difficult to eliminate completely, we anticipate that some predictive capability can be obtained by recasting the equipment modeling problem as a set of state equations. These will separately calculate the change in equipment status as a function of cumulative history and the change in wafer state as a function of

the current equipment state, the current processing conditions, and the previous wafer state.

At Berkeley we have an important on-going technical effort which will help drive the process synthesis work. Based on this work, we plan to demonstrate the smooth integration of empirical data into the synthesis effort. Preliminary study will focus on physically based design rules using lithography as the vehicle. We will do this by accumulating test data from the Litho process at HP and combining them with TCAD simulations. We will explain the observed variability in terms of deterministic and random causes and create a detailed error budget. Based on this we will extract simple, physically based design rules that grade designs and identify process bottlenecks.

We will also demonstrate the flexible process spec idea in the Berkeley Microfabrication Laboratory. We will do this by generating Poly CD specifications and by using the Poly CD specs to generate flexible intermediate specs for each preceding process step: develop, expose, spin-coat & bake, LPCVD, oxidation. We will then actually run the process under supervisor control and observe the automated change of the intermediate specs as equipment change. An intentional change in the final specs will also be introduced in order to demonstrate the automated reconfiguration of the workcell. The purpose of this demonstration will be to show how dynamic specs can be used to increase manufacturability and to ease technology transfer problems. Also, we expect to make use of state-based equipment models that can track equipment aging and predict future equipment behavior.

An important enabling factor for concurrent design is the lithography simulation capability which has been built up through the SRC Sematech Center of Excellence at Berkeley and the associated involvement in its use in industry. Tools for aerial image simulation (SPLAT), topography scattering (TEMPEST), and 3-D dissolution evolution (SAMPLE-3D) have been developed and interfaced with each other. Collaborative studies with industry of alignment mark dropout in the SVGL scanner, scattering from phase-shift mask edges, and resist dissolution effects have been effective for industry and have helped to drive the simulators along practical lines. This suite of tools provides extensive new leverage for rapidly simulating and/or extending experimental characterization to avoid pitfalls and accelerate learning. In short these tools help replace the art based on experience judgement with the science of quantitative assessment.

Another enabling factor associated with Berkeley is our involvement in the linkage of TCAD to layout at the IC circuit CAD level. The outstanding work in circuit CAD by the group of A.R. Newton, A. Sangiovanni-Vincentelli, and R. Brayton has resulted in CAD systems such as OCT/VEM/RPC which integrate many CAD tools at various design levels. The PROcess Simulation Environment (PROSE) is an exploratory system which links process simulation TCAD tools for use by the IC CAD designer. PROSE allows device cross sections to be simulated from the layout and a process flow from a pull down menu in VEM. In the same manner a phase-shift mask design tool kit can be invoked which assigns phases, design rule checks phase-shift masks and can capture mask layouts for rigorous testing with lithography simulation tools. In a parallel effort in CIM it recently became possible to link empirical characterization and simulation for control specification We believe that our experience in linking IC CAD, CIM and TCAD will prove invaluable in integrating for concurrent design. It is also likely that the existing code

in the OCT/VEM/RPC, PROSE and CIM systems at Berkeley (BSIMS, BCAM, RTSPC, etc.) might prove invaluable as a superstructure for rapid and low overhead exploration of novel new cross-functional components.

An essential underlying ingredient to facilitate integration is a common media *for* communication. It is important to get moving on new exploratory approaches which provide a rich basis for simultaneously supporting and efficiently carrying out activities in IC design, process development, and manufacturing. The approach must be rich enough to describe any one activity in great depth and also support gray level assessment of design tradeoffs. Finally, it needs to be possible for a person with, say, the IC design view to invoke increasing detail of the process and manufacturing views when appropriate.

It is also important that the interfaces by means of which this concurrent design system is accessed meet the needs of the intended users. The designer may want to invoke the system from pull down menus in the layout. The process developers may want access from computer interfaces on vendor supplied processing tools. Careful planning of interfaces and some field testing of prototype concepts is appropriate. These studies might be carried out by threading together several simulators to look for 'in specification hidden gotchas' such as is possible on the lithography work bench. Combining critical path circuit assessment based on data for linewidth variation in the die field is another example which could demonstrate the synergistic combination of manufacturing and IC design.

5.2 Greater Context

We believe it is appropriate to proceed by having Industry develop a robust central system core and to have Universities as centers of expertise experiment with high risk aspects. These high risk ventures include new approaches to underpinnings such as process flow representation, semiconductor wafer representation in 3-D, and layout design rules. The high risk ventures also include new combinations of functional capabilities to support new viewpoints to help digest and utilize concurrent information.

This effort will be greatly aided by the ongoing research in University centers of expertise. This includes process and device modeling, IC CAD, and CIM. The following table outlines the relevant contributions by many players.

Table 1: Relevant Contributions and Players - A Subjective View

Problems	Players
Modeling IC Reliability	Berkeley
Process Modeling Doping/Oxidation	Stanford
Process Modeling Lithography	Berkeley
Process Modeling Etch Deposition	Stanford/Berkeley
TCAD Frameworks (SPR/SWR)	Stanford/Berkeley/CMU
Equipment Connections	Stanford/Berkeley/MIT

Table 1: Relevant Contributions and Players - A Subjective View

Problems	Players
CIM and TCAD connections	Berkeley/MIT/Stanford
Statistical Simulation / Stat Design Rules	CMU
Physical Equipment Modeling - PE CVD	CMU
Equipment Modeling/Control - RT CVD	NCSU
Physical Equipment Modeling - CVD	MIT
RT Control - RTP	Stanford
RT Control - Plasma	Berkeley
Run-to-run Control	Berkeley/MIT?
TCAD Calibration	MIT?
Manufacturability Metric	Berkeley
Empirical Modeling for Control	Berkeley
Physical/Flexible Design Rules	Berkeley/CMU
CIM	TI/MMST?

6.0 Impact of the Proposed Work

The primary impact of the greater synthesis effort will be significant acceleration and cost reduction associated with the process/product development and production cycle. *In* order to quantify this impact, consider the current cost of technology development which now stands to approximately 150 man years. It is conceivable that process synthesis tools can drive this cost down to 50 man years resulting in over $30M savings per company for each new technology.

Another cost component has to do with technology transfer. Speeding up technology transfer from the current 1-2 years down to 1-2 months will result to savings of over $5M per product, along with significant time-to-market and capacity utilization advantages.

The elimination of hidden "gotchas" will result to significant savings as well. It is estimated that 1 week down time of a mid sized facility costs about $5M. This is compounded by additional cost in lost revenue, delayed time-to-market and delayed yield learning as well. Our rough estimate based on publicly available information is that 3-6 weeks of production of a new product are lost due to manufacturability related redesigns and mask changes. Eliminating these losses could easily mean a gain of $75M for a product of significant volume, such as a 486 class microprocessor.

Other advantages of the process synthesis applications are more difficult to quantify but they should not be neglected. In the short term, process synthesis will result to better utilization of the installed capacity, by mating a large variety of products and processes to the existing equipment base. In the long run, reducing the cost of IC product/process development will lead to more product specialization as needed to serve diversified consumer applications such as personal communications, etc.

Finally, through process synthesis system houses and other IC customers, silicon manufacturers, equipment vendors and their suppliers will develop and use a common "language", further enhancing productivity across all segments of the IC industry.