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APPLYING TCAD TO EMERGING TECHNOLOGIES

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by

Derek C. Lee

Memorandum No. UCB/ERL M95/38

20 May 1995

ELECTRONICS RESEARCH LABORATORY

College of Engineering University of California, Berkeley 94720

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Dedication

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To my parents with deep appreciation and respect for their support, love, and guidance throughout my education.

Acknowledgment

I would like to thank my research advisor, Professor Andrew R. Neureuther, for his support, encouragement, and guidance in all aspects this project. Without his contribution, completion of this project would not have been possible. Even with his incredibly busy schedule, he always had free time for me. I would like to thank Professor Roger T. Howe for reviewing this report and for his guidance on on the MEMS side of this project. I would also like to thank my family and friends who have given me unending support and encouragement over the years.

For the lithography part of this report, I would like to thank Michael Yeung for his invaluable support and expertise, and Obert Wood for his input, use, and testing of the modified versions of SPLAT.

For the MEMS side part of this report, I would like to thank Robert Wang for his guidance in the area of TCAD, Andrej Gabara for making my job much easier with his enhancements to SIMPL System 6, and Joe Kung of Analog Devices for pushing the SIMPL program to new limits.

The financial support for the lithography part of this project was provided by the Semiconductor Research Corporation via SEMATECH grant 90-MC-500 and by the ARPA Advanced Lithography Program under the guidance of Dave Attwood at Lawrence Berkeley Labs. The funding for the MEMS part came from the ARPA *i*MEMS project. These sources are gratefully acknowledged.

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Chapter 1

Introduction

Computer-Aided Design (CAD) of integrated circuits is well established. It is nearly impossible to design a complex circuit without circuit simulation. Tools exist for mask layout, schematic capture, circuit extraction, layout automation, etc. Process simulation toolsclassified as Technology CAD (TCAD) tools-are not nearly as well established but are becoming increasingly more important as new technologies emerge with new levels of process complexity. Two such technologies which stand to benefit from TCAD applications are EUV (Extreme Ultra Violet) project lithography, and fabrication of MEMS (MicroElectroMechanical System) devices. Creation and application of simulation tools for these technologies are the focus of this project.

This report is divided into two main parts consisting of three chapters. Chapters 2 and 3 discusses the use of lithography simulation for EUV projection lithography, in which simulation was carried out with the SPLAT program. The second part, consisting of Chapter 4, discusses research related to process simulation of MEMS devices using the SIMPL System 6 simulation software.

Chapter 2

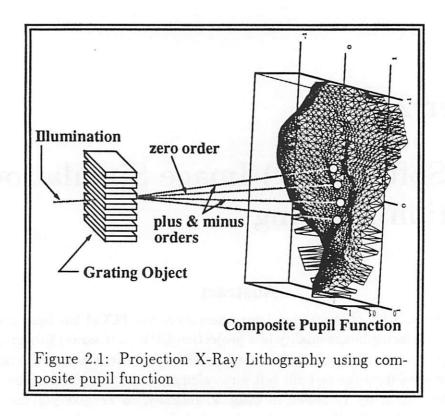
EUV (Soft X-Ray) Image Simulation for Projection Printing

Abstract

SPLAT (Simulation of Projection Lens Aberrations via TCCs) has been generalized for exploring image quality in a projection EUV (soft x-ray) lithography proto-type system. Extensions were made in SPLAT to encompass the detailed wavefront data from the as built soft x-ray elements as synthesized in the system configuration by T. Jewell in Code V. Initially, 36 Zernike polynomials were used to describe the pupil function, but the image quality was overly optimistic. The detailed wavefront map from Code V on a 64x64 rectangular grid was then used. A table lookup approach with a rectangular grid and area weighting which can also simulate amplitude variations across the pupil was used in the integration. The thin arc for the undulator source path in the illumination was found to be best treated as a direct path integral rather than the limiting case of annular illumination. At x-ray wavelengths (13 nm) the surface figure errors of the multi-layer mirrors in the initial exploratory system were quite significant and the images were primarily degraded by the variation in their position rather than their quality as the undulator is swept through its arc. This is in agreement with the experimental observations reported by O. Wood et. al and is shown to be even more severe for 2D patterns.

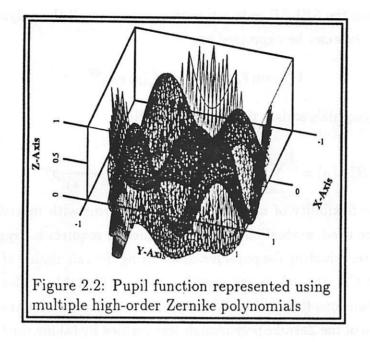
2.1 Introduction

A serious technology issue in the fabrication of projection extreme ultra violet (EUV) or soft x-ray systems is the development of multi-layer reflective mirrors whose surface tolerances relative to the wavelength are adequate. Simulation of surface figure and coating effects will allow system designers to specify tolerances on optical elements in the context of system performance. While simulation of system effects in 1D is possible in Code V [Opt], the transfer



of the composite pupil function to SPLAT [TN87] allows studies of 2D imaging. In SPLAT it is also possible to simulate phase-shift masks, off-axis illumination, lens filters, thin-film resist penetration interference effects, and aperture stops. The images within the thin-film resist and materials from SPLAT can also be coupled with SAMPLE-3D [KKHTS91] [EWSN91] for simulation of the resist profile time evolution and development.

A conceptual drawing of a projection x-ray system is shown in Figure 2.1. Here a pupilmap of an initial exploratory optical system used by O. Wood *et. al* at AT&T Bell Laboratories [ORWJ89] illustrates the high degree of aberration in the pupil function. The pupil function was synthesized in Code V by T. Jewell from wavefront measurements of the individual optical elements. A pencil beam from the undulator illuminates the mask which then diffracts the pencil beam into a number of spots. These spots pass through the pupil in specific locations and approximately lie on a plane in the exit pupil. If the normal of this plane is rotated with respect to the zeroth order incident beam, a lateral shift is imparted to the mask pattern perpendicular to the line direction when it is imaged at the wafer. The degree of tilt, or equivalently the relative path difference along the spots, determines the severity of the image shift. When the source position is changed, as in a rotating undulator source system, the diffracted spots will pass through an entirely different region of the pupil function



and a different shift will occur. This image shift effect has been simulated with SPLAT and will be shown to be more significant than the degradation of the individual image quality for a given undulator position.

This chapter begins with the Zernike polynomial representation of the pupil function which is followed by sections on the wavefront map interface and integration scheme. Two approaches for modeling the illumination system are then discussed. Finally, simulation results from an image quality study are presented.

2.2 Zernike Polynomial Interface in SPLAT

SPLAT has been generalized to represent the pupil function using an arbitrary number of Zernike polynomials, which are commonly used in representing high-order aberration effects in optical systems [BW80]. Zernike polynomials are mutually orthogonal over the unit circle, and thus the mean-square distribution of the wavefront relative to a Gaussian reference sphere can be computed as a summation of the Zernike polynomial coefficients without needing to handle cross-terms. To represent the pupil using Zernike polynomials, a file containing the values for the multipliers is specified. A plot of the pupil function using multiple high-order terms can be generated by SPLAT as seen in Figure 2.2.

Currently a maximum of 64 Zernike polynomial terms may be used. However, SPLAT is extensible to a higher number of terms in that the Zernike polynomial generating function has

been incorporated into the SPLAT code rather than typing in all the polynomials explicitly. The Zernike polynomials can be expressed as

$$V_n^l(\rho\sin\theta,\rho\cos\theta) = R_n^l(\rho)\exp^{il\theta}$$
(2.1)

where the radial polynomials satisfy the following relation.

$$R_n^{\pm m}(\rho) = \sum_{s=0}^{\frac{1}{2}(n-m)} (-1)^s \frac{(n-s)!}{s!(\frac{n+m}{2}-s)!(\frac{n-m}{2}-s)!} \rho^{n-2s}$$
(2.2)

This provides the flexibility of using any number of terms with minimal code changes. When many terms are used, evaluation of the pupil function requires a large amount of computation. Instead of reevaluating the pupil function during the calculation of the transmission cross coefficients (TCCs), the values are stored in table. This table is also used to support the other SPLAT extensions that will be described in the following sections.

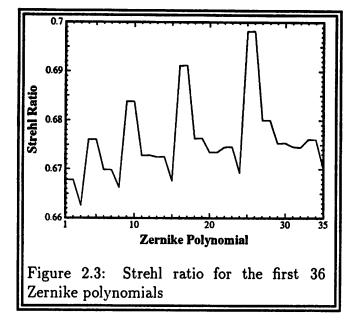
The normalization of the Zernike polynomials was verified by taking the Strehl ratio which can be expressed as in Equation 2.3 for small non-periodic features and small aberrations. It is the ratio of the intensity at the center of a small non-periodic pin hole with and without aberration present.

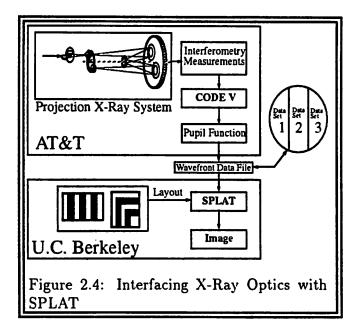
$$Strehlratio \cong \exp^{-4\pi^2 \Phi^2} = \frac{Intensity_{(0,0)_{aberrated}}}{Intensity_{(0,0)_{notaberrated}}}$$
(2.3)

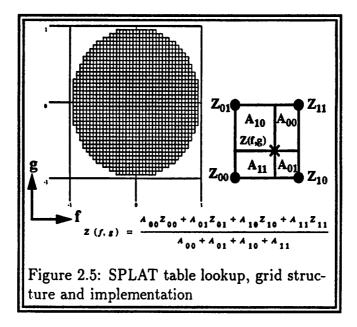
For $\Phi = 0.1$ rms wave the Strehl ratio = 67.4%. All Zernike polynomial terms should individually give the same Strehl ratio in the ideal case. Figure 2.3 shows the Strehl ratio for the first 36 Zernike polynomials as computed by SPLAT for a 0.1 μ m by 0.1 μ m square pin hole in the middle of a 5 μ m x 5 μ m mask with $\lambda = 0.248 \ \mu$ m, NA = 0.248, and $\sigma = 0.6$.

2.3 Wave Front Map Interface in SPLAT

A schematic representation of the interface between a projection system, Code V and SPLAT is illustrated in Figure 2.4. Interferometry measurements are performed on the individual lens elements for input into Code V. The composite pupil map synthesized by Code V is output into a file which splits the pupil in three sections. This file is input into SPLAT which can produce a 3D plot of the pupil as seen in Figure 2.1. Alternatively, the aberration function can be represented by a sum of up to 64 Zernike polynomials by the multipliers in for each polynomial. Normalization can be specified as either the RMS or max aberration across the pupil. Using the input pupil function and an arbitrary mask pattern, intensity versus linewidth along a cutline and contour plots of 2D images can be produced.



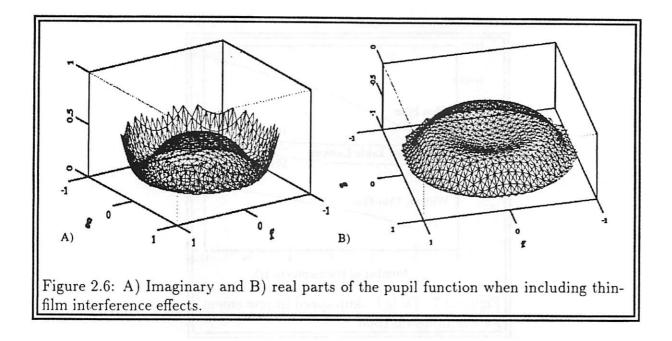




2.4 Integration Scheme

A table-lookup of the pupil function was required to input the wavefront data. The structure of the grid and interpolation scheme associated with this table-lookup approach are shown in Figure 2.5. During simulation the values are interpolated using a "weighted-area" scheme. Originally linear interpolation was employed which caused convergence problems due to interaction with an adaptive/self-checking algorithm used in test the numerical integration. The weighted area (quadratic interpolation) scheme overcame the original convergence problem. Typically a 64x64 grid is used, although more dense grids can be specified.

SPLAT has been recently extended to include thin-film interference effects for imaging within photoresist [MSYN93]. This extension utilizes the same internal table lookup structure to store complex values. Because the values are complex, the amplitude as well as the phase of a wavefront can be represented. Thus the change in the magnitude as well as the phase of reflectivity of a multilayer mirror due to variation in the incident angle of the source can be simulated. This may be particularly useful for x-ray system elements where it is difficult to fabricate the correct multilayer d-spacing variation with angular changes across the elements. A plot of the real and imaginary parts of the pupil function for a case of imaging within the photoresist is shown in Figure 6. When the simulation area is small (5 $\frac{N}{NA}$) square area or less) the simulation time is dominated by the 100 seconds it takes to calculate



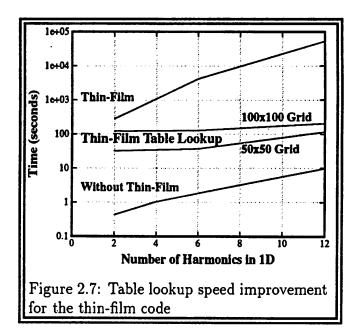
the elements in the table lookup. For the EUV (soft x-ray) imaging the data for the table lookup come from Code V and the computation time is similar to the line labeled "Without Thin-Film" in Figure 2.7.

2.5 Modeling Illumination Schemes

Two techniques have been used to simulate the proto-type system used by Wood et. al, in which a pencil beam from an undulator source is incident on a two mirror rotator to form a cone of illumination. Both annular and multiple spot illumination with a uniform angular distribution have been used. Annular illumination requires much more computation time. This is because integration over the annulus is computed by subtracting the results of the integration over the inner aperture from that of the integration over the outer aperture. Due to the very small 0.0004 annulus rim size, this was found to require these integrals to be carried out to an accuracy of 4 decimal places.

In spot illumination, integration is performed only over the small source for each position. This also allows the quality of the composite image to be compared with that from individual spot locations. The computation for N spots, requires N times as much computation time. Once the number of spots is specified, SPLAT is run for source positions that are uniformly distributed (equiangular separation) within the aperture at the specified radius. The composite image is generated by averaging the images for each source location. The spot approach

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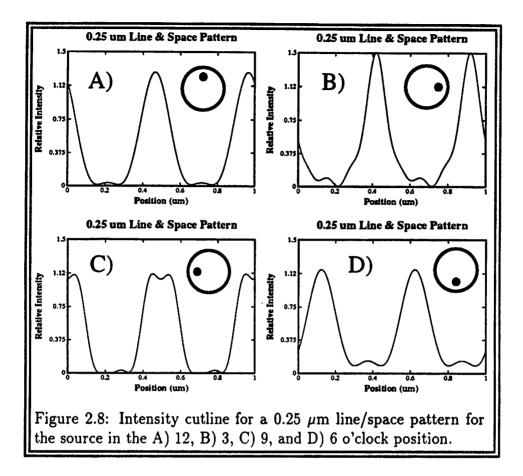
brings up the interesting question as to how many spots are required to approximate a continuous arc. The underlying significance is that in a system with a highly aberrated pupil, many different mask illumination angles should be used to average out the spot to spot image variations.

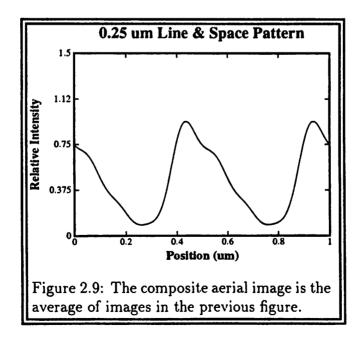
2.6 Image Quality Studies

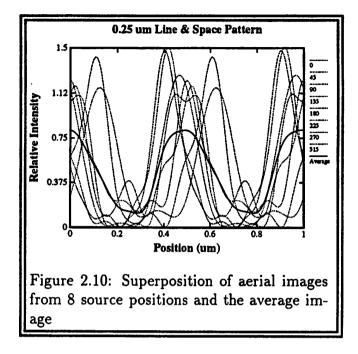
The experimental pupil function shown in Figure 2.1 was used to simulate a 0.25 μ m line/space pattern for a 0.0835 NA system at 13 nm. To see the spot location effects, simulation runs using different source positions have been used. The aerial image for four source positions are shown in Figure 2.8. Figure 2.9 is the composite aerial image formed by averaging the four. The image quality at the various positions varies, but more importantly, the images are shifting left and right relative to one another. Consequently, the composite aerial image is wider and lower in contrast than any of the images for individual source positions. The effect of the image shift for 8 source positions is illustrated in Figure 8 with the aerial image for eight source positions superimposed on one another along with the composite image (black solid line). Control of which source positions are used in imaging would allow the use of only the "sweet" source locations and elimination of the positions that produce unwanted shifts or inferior images resulting in a superior composite image.

The effect of image shift is much worse in 2-D because the shift can occur in two inde-

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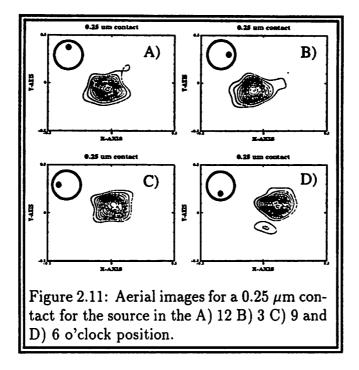


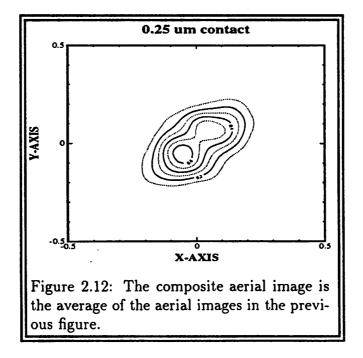


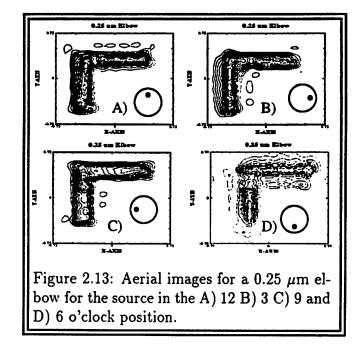
pendent directions. These 2D effects are illustrated in Figures 2.11, 2.12, 2.13, and 2.14 which show a 0.25 μ m contact and 0.25 μ m elbow. The shift from the centered position is more easily seen with the contact hole pattern than with the line pattern. When the source is in the 12 and 3 o'clock positions, the image is displaced to the bottom left. In the 6 and 9 o'clock positions, the image is shifted more to the top right. These effects can be seen in the composite image which is smeared along the bottom-left top-right diagonal and is lower in intensity. The degradation of this contact hole pattern is worse than that in Figure 2.9 for a line pattern.

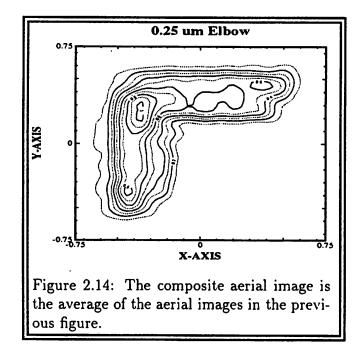
2.7 Conclusion

The extensions made to include aberrations across the pupil have been useful in simulation of EUV (soft x-ray) projection lithography. The extensions include representing the pupil with Zernike polynomials and wavefront maps from Code V. This required the implementation of a table lookup and weighted area interpolation of the pupil function. This internal structure is ready to accept magnitude as well as phase data which may be important in multilayer coating effects. A rotating undulator source model has been implemented which can also model an annular source. The image quality studies indicate that source spot to source spot image displacement rather than image degradation for a given source spot location currently









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2.7 Conclusion

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limits the resolution.

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Chapter 3

Simulation of Non-uniformities in Sources and Optics in Projection Printing

Abstract

The aerial image simulation program SPLAT has been further generalized to explore the effects of multielement source designs and possible problems from residual mirror reflectivity variations versus pupil position on image quality in projection x-ray lithography. To model wavefront attenuation, an optical transmission with apopdization (OTA) factor is introduced, which modifies the magnitude of the pupil function versus ray angle. The OTA is expanded in a Taylor series in polar coordinates. A radial OTA variation of $1 - 0.25\rho^2$ which falls from 1.0 at the center of the lens to 0.75 at the lens edge, required small features to be oversized approximately by 8% to obtain the same image quality. To allow for irregularly shaped sources with non-uniform intensities, the source is represented over a square grid composed of many pixels. The source is defined using geometric primitives that can be assigned arbitrary intensity weights. Typical multiple element sources of the type proposed for EUV projection printing shows that the orientation of the feature with respect to the source has about a 5% effect. The generalization of the source nonuniformity modeling in SPLAT is also applicable to illumination studies in optical projection printing.

3.1 Introduction

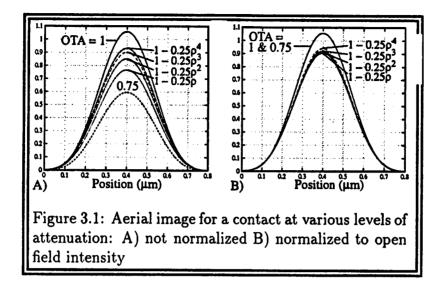
SPLAT was previously extended in the previous chapter to read detailed optical wavefront data from CodeV to specify the degree of lens aberration [LN93]. This capability was developed for studying wave-front effects in projection printing at both conventional and EUV wavelengths, and can now be coupled with arbitrary illumination sources and wavefront amplitude weighting as presented in this chapter.

In addition to the optical path difference, such as that due to surface figure errors of the multi-layer mirrors, the reflectivity across the mirrors might not be uniform. This is because the difficulty in fabricating multi-layer coatings will likely lead to residual amplitude as well as phase errors. The residual effects depend on the angle of incidence in the optics and the extent to which the variation of the thin-film multilayer spacings is able to track the desired spacing. To explore the degree of accuracy needed in producing optical elements, the SPLAT program has been modified. These amplitude effects can be modeled in SPLAT by specifying analytical reflectivity functions across the pupil which is termed the optical transmission with apodization (OTA) factor. The OTA modifies the magnitude of the pupil function or the magnitude of the electric field ray at the associated angle. It is a function of pupil position similar to the optical path difference and is used to weight the electric field. Currently the OTA is expanded in a Taylor series in radius and azimuthal angle of the entrance pupil (similar to the primary phase aberrations). The implementation of the OTA, its agreement with theoretical results, and the effect OTA has on image quality for various feature types and sizes are discussed in the first few sections of this chapter.

Illuminator systems in projection x-ray proto-type systems will likely be based on synthesizing multiple and irregularly shaped elements [Swe93] which will produce irregular illumination patterns at the entrance pupil. For this reason, SPLAT has been extended to model arbitrary illumination sources that are constructed with geometric primitives and assigned varying intensity weights. The implementation and operation of the arbitrary source model, and the effect of source shape on image quality are discussed in the latter sections of this chapter.

3.2 Optical Transmission with Apodization

As described above, the OTA specifies the amount of electric field transmission in the pupil. Currently, the OTA is specified by providing coefficients for one or more of the following functions: 1, ρ , ρ^2 , ρ^3 , ρ^4 , $\rho \cos \phi$, $\rho \sin \phi$, $\rho^2 \cos 2\phi$, and $\rho^2 \sin 2\phi$. As evident, symmetrical as well as non-symmetrical variations are available. The code can be easily changed to accommodate other functions as required. Currently, these functions are evaluated analytically. However, it is anticipated that when pupil maps of attenuation effects are available, SPLAT will be adapted to read them into a table which is currently done with pupil phase maps. This amplitude factor is in addition to the pupil filter functions which were previously included in



SPLAT.

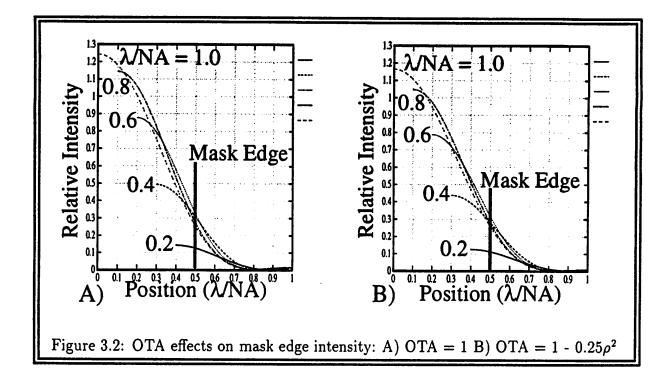
3.2.1 Verification of the OTA model on SPLAT

One of the tests of the SPLAT program was to increase the level of the OTA, or the amount of attenuation and observe the effect on the image. For example, the image of a transparent line of 0.8 λ/NA was observed as the amount of attenuation was increased. The peak value of the intensity was expected to decrease as the amount of attenuation increased.

For the case of a constant attenuation, the peak intensity should fall off as the square because the attenuation is proportional to the electric field. Simulation models this theoretical trend to 5 places. The case of constant OTA is special, in that the curves become identical after renormalizing to the clear field values.

Intensity curves for non-constant OTA, however, will not renormalize to the same values. The effect of a radially symmetric variation on image quality was studied. The image intensity as a function of the attenuation variation-constant, linear, square, cubic, and fourth power-is shown in Figure 3.1A. The image intensity increases from the constant attenuation value to its peak. There is less impact for the higher order polynomials because they have less attenuation near the center of the pupil. However, the images should be renormalized to the clear field because for non-zero σ , the illumination cone passes through places on the lens where there is some attenuation. This affects the clear field value, as shown in Figure 3.1B, where the images have been renormalized for $\sigma = 0.5$.

The normalization used in Figure 3.1B can be corrected for theoretically by integrating



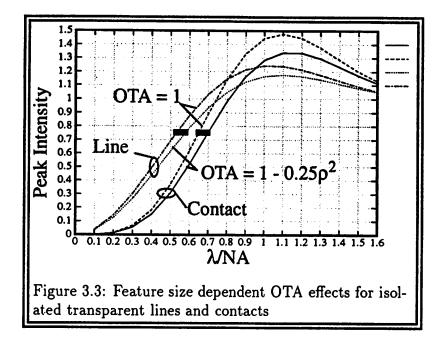
the OTA over the illumination cone, as described in Equation 3.1 which simplifies to the last expression for a radially symmetric source. When these integrals are carried out exactly, the results show that SPLAT is accurate to 3 places.

$$\frac{I_{peak}}{I_{peak}(OTA=1)} = \frac{\int_0^{2\pi} \int_0^{\sigma} OTA(\rho)^2 \rho d\rho d\phi}{\int_0^{2\pi} \int_0^{\sigma} \rho d\phi} = \frac{\int_0^{2\pi} \int_0^{\sigma} OTA(\rho)^2 \rho d\rho d\phi}{\pi \sigma^2}$$
(3.1)

3.2.2 OTA Effects on Image Quality

Several possibilities exist on how the attenuation will affect the image quality. It could affect the values near the mask edges, values in the dark space, or values in the peaks. The impact at the mask edge for a quadratic variation of $1-0.25\rho^2$ is shown in Figure 3.2A and B, where intensities as a function of feature size, in terms of λ /NA, are plotted (normalized to clear field). A variation in line edge intensity of only a few percent is present in both the attenuated and non-attenuated cases.

The peak intensities for isolated transparent lines and contacts as function of feature size with and without the same attenuation are shown in Figure 3.3. At very large feature sizes, the intensities are all about the same. This is to be expected since the middle of the lens is used for large feature sizes. At intermediate feature sizes, less overshoot is observed. The



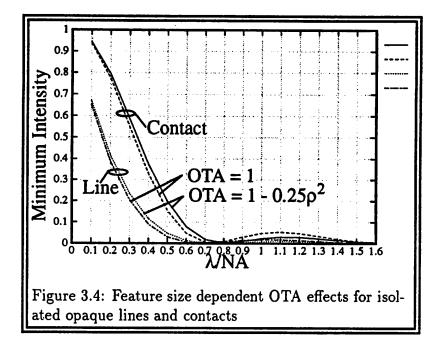
absolute decrease is more for the contact, making the line and contact images more similar. However, in the small feature size region between 0.5 and 0.8 l/NA where much lithography is done, both the line and contact intensities are about 10% lower. As a result, to obtain a certain intensity, 75% of the clear field for example, features must be oversized. At this 75% intensity level, the lines have to be oversized about 9% and the contacts have to be oversized about 7%.

The effect on opposite polarity features is shown in Figure 3.4. While the absolute increase in absolute intensity is small, the percentage increase is similar to the case above. For this polarity, an intensity below 15% is desirable which would require a bias of about 8%.

3.3 Arbitrary Illumination Sources

3.3.1 Operation and Implementation

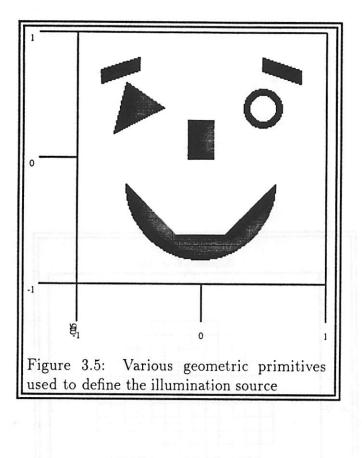
The source is represented by a rectangular grid composed of many pixels. The source is first defined using geometric primitives such as circles, rectangles, and general polygons (See Figure 3.5). Arbitrary intensity weights can be assigned to the primitives to construct, for example, a source with a radial variation in brightness. A table lookup approach of the source is then used during the integration of the transmission cross-coefficients in Hopkins' theory of partially coherent imaging [Hop53].



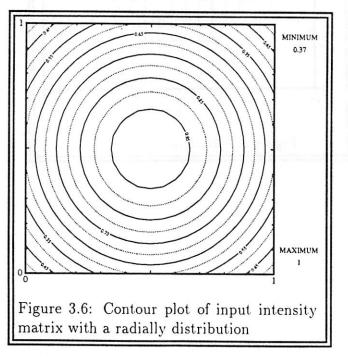
SPLAT also supports reading intensity matrices on top of which arbitrary shapes can be placed. This is similar to placing transmission apertures into a system with a known illumination variations across the pupil. Another possibility, no yet implemented, would be to describe the illumination variation with an analytical function. An example input contour with a radially distribution is shown in Figure 3.6. After placing a circular aperature with σ = 0.6 the source appears as shown in Figure 3.7 and Figure 3.8.

A test of the program was to run it with a normal circular source and a a source described by a uniform intensity matrix with the same sigma. Figure 3.9 shows this comparison for $\sigma = 0.6$. The results differ slightly owing to the fact, that the discretized source has a larger source area and not a perfectly circular shape. When the grid density is increased negligible differences are seen. A second test of the code was to examine the focus behavior of a non-uniform distribution. Figure 3.10 shows intensity curves at several levels of defocus for a linear varying source and for a line perpendicular to the intensity variation. The peak intensity values shift slightly to the left due to the asymmetric illumination. This is not observed for lines which are parallel to the intensity variation. A third test of the code was to check the open field intensity values for the various sources and they all were within in the 1.00x range.

The way in which the integration was implemented is shown in Figure 3.11. Pre-existing integration routines, used for the circular sources, were modified to sample the source pixel



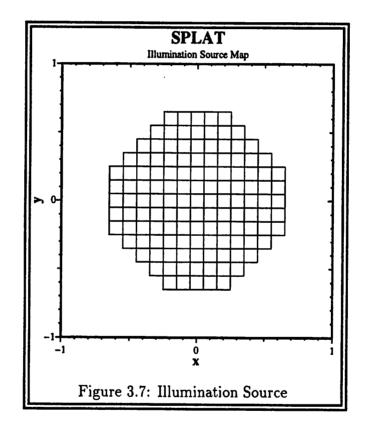
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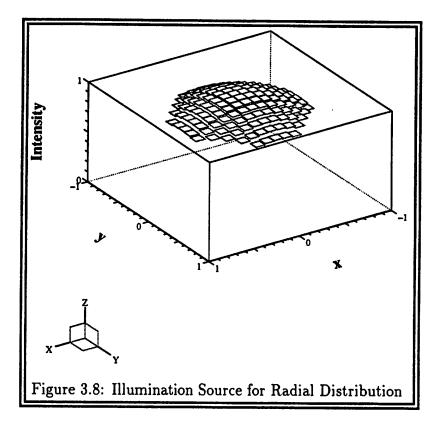


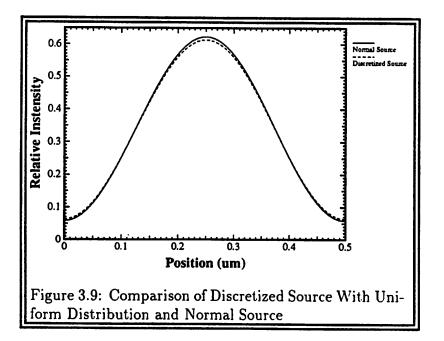
24 Simulation of Non-uniformities in Sources and Optics in Projection Printing

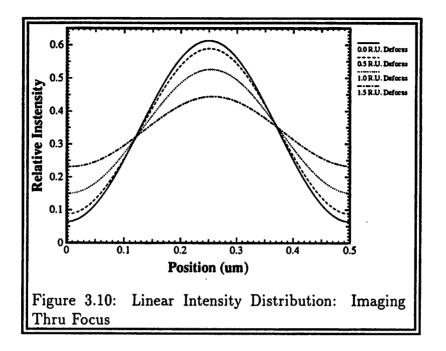
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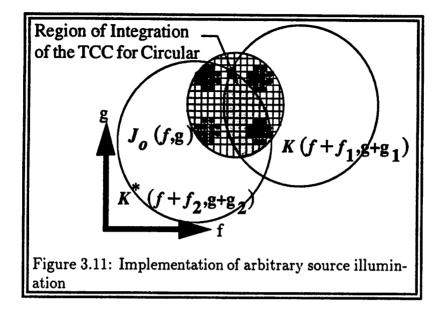


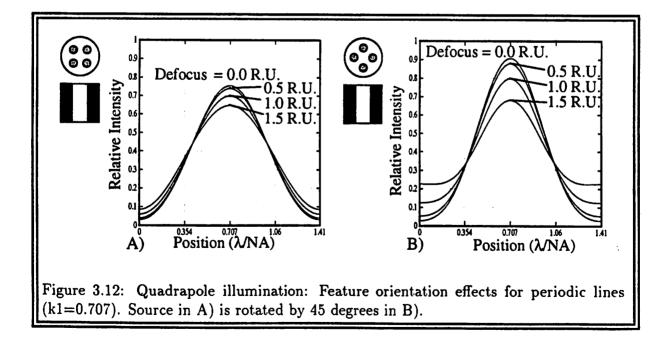


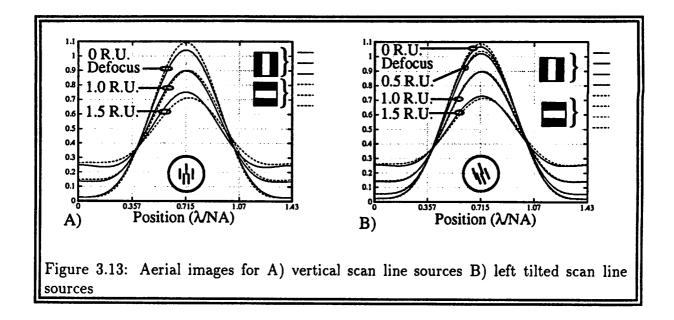
map. This approach facilitated the implementation and avoided writing complicated intersection routines to determine the integration area. The trade-off, however, is an increase in the simulation time, especially when a large number of pixels are used because every pixel should be sampled to guarantee accuracy. Testing of the arbitrary source imaging with SPLAT using circular sources is in agreement with those obtained with the source being represented analytically.

3.3.2 Effect of Source Shape on Image Quality

The interplay of source shape and feature orientation for periodic lines is illustrated in Figure 3.12 for a quadrapole illumination source. One of the ideas of this type of source is that there is an interplay between the angles in which the source drives the mask and the angles in which the diffracted orders come off. A lot of energy can be put into the rays going down the left and right side of the lens to get a very low dependence on focus. For the source shape and mask in Fig. 6A, an image can still print defocussed to 1.5 R.U. while most steppers only print up to about 1 R.U. Rotating the source by 45 degrees, or rotating the line by 45 degrees, as in Fig. 6B, shows that the source orientation is important in that the good behavior with focus is deteriorated. At a defocus level of 1.5 R.U., the pattern is over 20% in the dark areas.







3.3.3 Multi-element sources

A more relevant issue is how the nature of the sources envisioned for EUV systems may interact with features. The EUV system proposed by Sweatt [Swe93] is used here as an example. In this scanning system, the illumination source is in the shape of a set of five line sources. The angle depicted in Figure 3.13 correspond to how the source illuminates different regions of the mask depending on where they lie in the ring-field. The images produced by the five sources were simulated in two positions: tilted left and vertical.

Differences in image intensity for these source orientations were found when periodic mask features were changed from being horizontal to vertical to the scanning direction. Figure 3.13A shows this effect for vertical line sources. At zero defocus, the horizontal mask line is more intense than the vertical mask line by about 5%, owing to the differences in the effective sigma of the source seen by these different features. Horizontal mask lines see a larger effective sigma of 0.525 than the vertical mask lines which see a smaller effective sigma of 0.35. The worst case would be lines perpendicular to the tilt angle for which the width of the source is even smaller than that for the vertical orientation. For example, the mask lines perpendicular to left tilted source lines see an effective sigma of 0.565 while mask lines parallel to the source lines would see an effective sigma of 0.325. As with the quadrapolc illumination system, there is an interplay of the pitch with the illumination angles due to the lens acting as a low pass ray angle filter. For multiple line element sources there may be rather sharp changes in image peak intensity when illumination lines tangent to the low pass filter circle move inside or outside the acceptance circle of the lens.

With defocus the horizontal line images become non-symmetric, and intersect the vertical line images. The horizontal line patterns become asymmetrical with defocus due to the interplay of the asymmetrical source with defocus. Figure 3.13B shows the same simulation for the left-tilted source line which would correspond to the edge of the mask. The differences in the images are noticeably less, as the difference in effective sigmas are less.

3.4 Conclusion

SPLAT (version 5.0) can now simulate arbitrary illumination sources and wavefront attenuation. Wavefront attenuation reduces the intensity, and even with renormalization for open fields, small features require an approximate 8% oversizing with an OTA of $1 - 0.25\rho r^2$. The OTA can be implemented with only a 15% increase in CPU time through the use of analytic variations. The shape of the illumination source does not have a major effect on the image quality. Differences on the order of 5% are produced by the different scanning positions used in the bow-tie source. Reducing the discretization errors in arbitrary sources made from small elements increases the simulation time by an order of magnitude. Expressing the shapes with analytical functions would definitely decrease this time. However, this would require completely rewriting the integration routines.

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Chapter 4

MEMS Process Simulation using SIMPL

Abstract

This project demonstrates the use of SIMPL System 6 to simulate MEMS (MicroElectroMechanical Systems) process flows by combining mask layout data with process flow information. SIMPL-2 (Simulation of Profiles from the Layout) and SIMPL-DIX (Design Interface X-Windows) make up the core of SIMPL System 6 and were the primary tools. The focus has been on developing SIMPL System 6 to assist in the development of MEMS circuits and as a vehicle to coordinate process development with device design in a joint project on MEMS with Analog Devices. As a result, SIMPL System 6 has become much more functional and robust in regards to its internal algorithms and user interface. This project illustrates the success of using SIMPL on the following MEMS processes: MICS process, Side Wall Beam process. Various MEMS process problems are simulated and compared to lab results. A test mask for calibrating simulators and identifying some process problems has also been initiated.

4.1 Introduction

4.1.1 Motivation for Simulation

The technology understanding and quantative analysis available in process simulators can greatly aid the process integration activity. They can help identify technology issues such as severity of planarity, transition topographies, and device protection schemes. They may also help predict device failure mechanisms or process limitations. In addition they may be used to help assess the influence of deposition technology on device performance, or the effect of process variations including misalignment errors.

Many processing issues exist in MEMS (MicroElectroMechanical System) processes, es-

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pecially when integrating them with a standard device process. Due to the large thin-film stack height in the fabrication of the mechanical structures, problems in lithography, etching, and deposition arise. A few examples are: resist thickness variations causing linewidth variations, step coverage problems in deposition, and less predictable mechanical behavior of flexure members due to process dependent effects.

4.1.2 **Project Overview**

This research has focused on developing SIMPL System 6 (generally referred to as SIMPL) and using it to assist in the development of MEMS circuits. SIMPL (SIMulation of Profiles from the Layout) has been used to visualize cross section evolution in several MEMS processes by combining mask layout data with process flow information. The intent was to use SIMPL as a vehicle to coordinate process development with device design in a joint project on MEMS with Analog Devices.

The focus of research now even shifted to developing the tools rather than using them on more real lab examples as initially intended owing to the nature of the process steps for MEMS and the need to face up to algorithm limitations to achieve robustness. Significant changes have been made to the both the internal algorithms and user interface. From this effort, the capabilities of SIMPL have improved significantly, especially in etching robustness and in the visualization of mask layers and cross-sections. Extremely complicated MEMS process flows have been simulated from start to finish, the largest of which contains over 150 (SIMPL) process steps and 22 masks. A number of of the cross sections created in addressing processing problems will be used to illustrate the current successful status of the newly released SIMPL System 6.

This chapter will begin with an overview of SIMPL System 6 which will serve as a primer to the subsequent section describing various process technologies as simulated in SIMPL. In this section, comparison to actual lab results and investigation into processing problems will be discussed. The next section is similar, and will describe the use of fabrication test structures to identify processing problems. Finally, this is followed by recommendations for future work and the conclusion.

4.2 Overview of SIMPL System 6

SIMPL System 6 is a collection of software tools to simulate 2D device processing. The principle components of SIMPL System 6 are SIMPL-2 [KLN83] and SIMPL-DIX [W+88].

SIMPL-2 contains most of the routines necessary for manipulating data and generating

cross-sections. It also contains first-order models for certain basic process steps: exposure, development, deposition, etching, implantation, diffusion and oxidation. These models are goal-oriented in nature, requiring input parameters which describe the dimensions and shape of the affected material after that step is performed. For example, implantations are approximated by a Gaussian function with a user-defined peak depth and standard deviation. Deposition models require a material name and thickness to extended the current topography.

SIMPL-DIX (Design Interface in X-Windows) provides the graphics and user-interface capabilities of SIMPL System 6. A layout and profile viewer is provided along with a variety of design tools. All these features are thoroughly detailed in the SIMPL System 6 Users' Guide [Ele95]. The release notes present in this document lists new features which have been developed in the effort to simulate the MEMS process flows.

SIMPL System 6 is also linked to SAMPLE [WOO79] [WO+80] for physical vapor deposition, isotropic and anisotropic etching of multiple non-planar layers, and optical lithography on a planar substrate. SAMPLE deposition and etching has been used extensively in this project. Links to various other tools (e.g. SUPREM [CHD83], [MELD88] for implantations) exist but will not be discussed as they were not used in this project. Again, please refer to the SIMPL System 6 Users' Guide for more information.

SIMPL utilizes the layout and process flow specifications to visualize the evolution of the device cross sections. This has proven useful for designing complicated processes with many more masks than a standard CMOS process.

4.3 Simulation of MEMS Process Flows

4.3.1 Overview of Simulation Cases

Several process flows have been created for simulation with SIMPL, and are listed in Table 4.3.1. Each will be covered in detail except for the proprietary ADI *i*MEMS process. The resonator example will be used to illustrate the various etching models available. The NWell CMOS example will show the the overall MICS process-electronic devices with microstructures. The position sensor example will show a stringer problem. The actuator example will show the use of SOG to remove the formation of stringers. The side wall beam technology example will show the use of stringers to form hollow beams. The ADXL50 process is used to illustrate a more complicated example and the use of SAMPLE non-planar etching. The metal beam process will show the ability for SAMPLE to model resist flow. The ADI BiMOS2C fabrication test structures were designed to investigate processing problems in the fabrication of the ADXL50 accelerometer and the multitude of structures designed at UC Berkeley (as

part of the ARPA *i*MEMS project).

Many other less complicated process flows (e.g. CMOS and NMOS) also exist which are included with the basic SIMPL System 6 software package.

Table 4.3.1 Simulation Cases				
Process	Layout	Purpose/Description		
MICS	Resonator	Demonstrate Etching Models		
	NWell CMOS	Demonstrate MEMS Integration		
	Position Sensor	Stringer Problem Example		
	Actuator	SOG Planarization Example		
Side Wall Beam	Beam	Stringer Example		
ADI BiMOS2C	ADXL50 Accelerometer	MEMS Integration, Non-planar Etching		
Metal Beam	Sense Capacitor	Resist Flow Example		
ADI BiMOS2C	Fabrication Test Structures	Fabrication Problem Detection		

4.3.2 MICS

Process Overview

The MOS fabrication process has been integrated with surface micromachining of polysilicon structures. The technique used at the University of California Berkeley is a modular approach whereby the CMOS transistors are completely fabricated before any of the surface micromachining [WYH90]. Hence the process is called the Modular Integration of CMOS with microStructures, or MICS. The baseline process IC process is a 3μ m design rule, doublepoly, single metal CMOS process. The standard aluminum metalization has been replaced with tungsten since aluminum can not withstand the high temperature annealing of the microstructure. A $TiN/TiSi_2$ diffusion barrier at the metal/silicon contacts has also been added to prevent the reaction of tungsten and silicon at 6000 C.

Surface micromachining is employed to add three levels of polysilicon. Electrical connection between the micro structures and CMOS is accomplished through a jumper layer of polysilicon to prevent out diffusion of tungsten into the polysilicon deposition tubes. The use of tungsten and its silicides has been borrowed from already mature VLSI process technology and shows promise for increasing levels of integration. To minimize the stress in deposited films, rapid thermal annealing (RTA) is employed to limit excessive dopant redistribution. In addition, the structural polysilicon layers are sandwiched in between two doped phosphosilicate glass (PSG) layers so that the stress gradient in the polysilicon is minimized after the RTA.

Simulation

Several different versions of the MICS process flow have evolved as more functionality and robustness have been programmed into SIMPL. The process flows differ in accuracy of the etching and deposition models and hence simulation time. Appendix C briefly discusses the different ways etching can be modeled in SIMPL. Ion implantations, may also be simulated more rigorously but this will not attempted as it was not the main processing thrust.

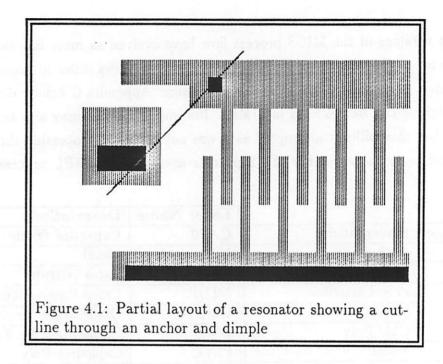
The mask and layer names in the MICS process used in the SIMPL process flows are defined below.

· · · · · · · · · · · · · · · · · · ·		Layer Name	Description
Mask Name		CAP0	Capacitor Oxide
CAA	Active Area	M1	Metal
CCA	Metal Contacts	NTRD	Locos Nitride
CEL	Poly Capacitor	NTDP	Cmos Passivation Nitride
CMF	Metal	OM1	Oxide Mask for SP1
CPG	Gate Poly	OM2	Oxide Mask for SP2
CSP	Nwell	PLYC	Capacitor Poly
SD2	Dimple for SP2	PLYG	Gate Poly
SD3	Dimple for SP3	PSG0	CMOS PSG (under M1)
SG1	SP2 anchor	PSG1	Sacrificial Oxide under SP2
SG2	SP3 anchor	PSG2	Sacrificial Oxide under SP3
SNT	CMOS passivation etch	PSGP	CMOS Passivation Oxide
SP1	μ structure poly1	RST	Resist
SP2	μ structure poly2	SP01	SP1
SP3	μ structure poly3	SP02	SP2
		SP03	SP3

Note: SP01 is used for the material name while SP1 is used for the mask name. This distinction was made only to allow for different color patterns in SIMPL-DIX. The same is true for the other structural polysilicon layers.

Resonator

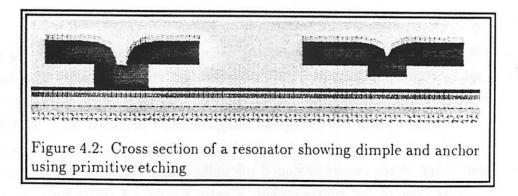
One of the simpler MICS examples is the lateral resonator. This example is used to show the different types of etching models in SIMPL. Figure 4.1 shows the mask and cutline which cuts through an anchor on the left and a dimple on the right. Figure 4.2 shows the layout and cross section of a resonator simulated using the most primitive form of etching. Notice that all the etch cuts have straight sidewalls. Figure 4.3 shows the cross section using etching with undercutting which results in sloped sidewalls. This is more accurate especially for isotropic etching as done in the dimple region. Finally, Figure 4.4 shows the same cross

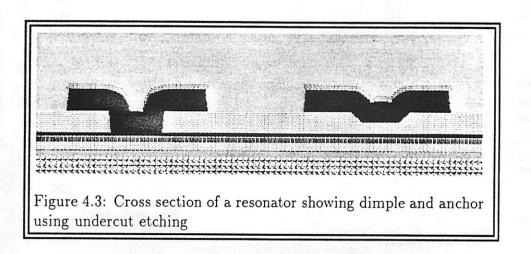


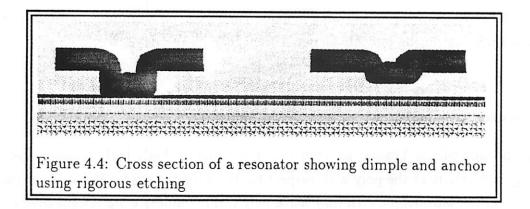
section using the most rigorous etching, referred to as SAMPLE-nonplanar etching because SAMPLE performs all the etching. In this case, the isotropic etching used to form the dimple creates curved geometries as expected in a real process. For more details about etching please refer to Appendix C.

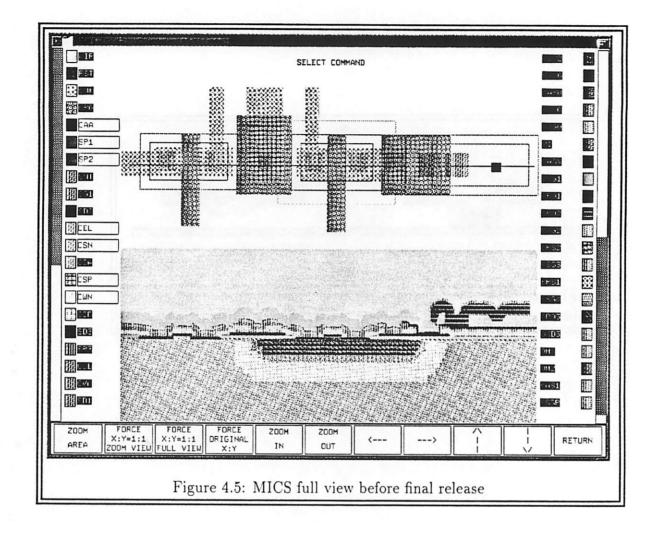
MICS NWELL

The full view of a MICS cross section showing the N-well CMOS and sensor area is shown in Figure 4.5. In between the PMOS and NMOS transistors, there is a poly-poly capacitor. A zoomed-in view of the the right side of the figure is shown in Figure 4.6. As described earlier,







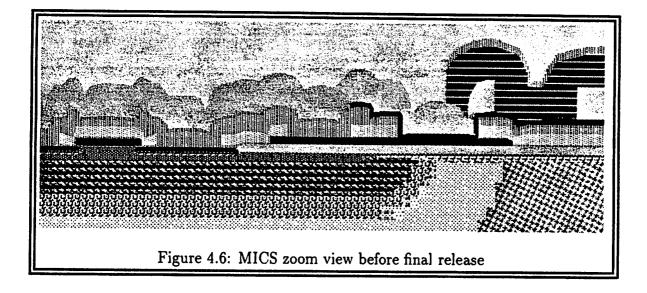


electrical connection from the sensor area is made via a polysilicon jumper layer to prevent tungsten out-diffusion during polysilicon deposition. The jumper layer is more easily seen in this figure.

Position Sensor

In etching the polysilicon beams, an etch is needed that is both highly anisotropic and provides high selectivity of the poly with respect to the sacrificial oxide. However, elsewhere in the structure, the anisotropic etch may leave poly residue unless a significant over-etch is used. Unremoved poly can become a conduction path causing short circuits, or bind together structures which should be free standing.

These types of problems were found on a particular position sensor design in MICS process, and they have been simulated. The cross-section shown in Figure 4.7 has SP2



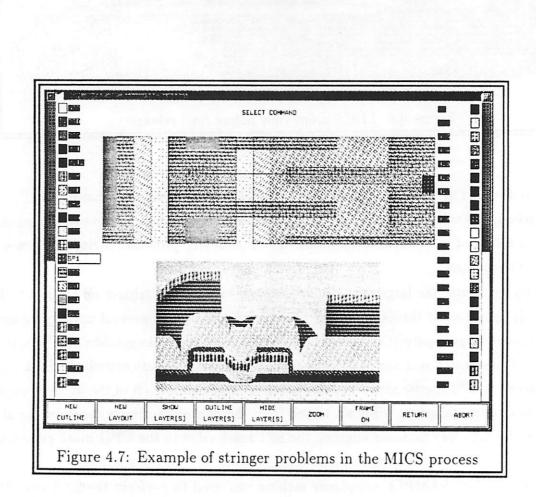
stringer problems. The severity of the stringers has been exaggerated because the SP2 was not over-etched, and subsequent isotropic etching was not done to help remove the stringers-a process step included in the real lab process. The real device produced stringers even with the normal precautions.

The main cause was the large step height ($\approx 1.4\mu$ m) under the stringer on the right. The SNT mask is used to cut thru the CMOS passivation nitride and several underlying oxide layers to expose the gate poly (CPG) upon which SP1 is deposited to establish and electrical connection. The solution was simply not to cut through the passivation with the SNT mask in areas under the SP2 shuttle area. The less severe stringer on the left of the figure is caused by many mask edges aligning (difficult to see from the figure) causing a more severe step. The solution for this was to avoid aligning the SP1 mask edge to the CPG mask edge when possible.

In this simulation, SAMPLE-nonplanar etching was used to perform the SNT cut. It is particularly useful because one etch step cuts through many layers of oxide: passivation oxide (PSGP), CMOS oxide (PSG0), capacitor oxide (CAPO). Other methods of etching would require the user to specify each layer of oxide to etch. Forgetting to etch through the other layers would result in a step height of only about 0.6μ m.

Simulation of SOG planarization

A variation of the MICS process is to add a second structural layer. A second structural layer is desirable to serve as a limit stop for moving beams, upper ground planes, and upper



sense or actuation electrodes.

A problem with the earlier design of this process was the formation of stringers of SP3 (the second structural poly but the third poly in the backend MEMS process). A planarization process employing the use of spin-on glass was used to solve this problem. The SOG planarization process can now be simulated using SIMPL. In previous versions the etch-back step did not work on complicated topography.

An SEM cross section of the MICS 3-Poly process is shown in Figure 4.8 [Fed94]. The situation depicted is similar to but not the same as the one simulated by SIMPL. In this case, voids (completely sealed from the top) were created between the fingers of SP2 during the deposition of PSG2. Subsequent deposition of SP3 filled these voids from openings at the ends of the fingers. In essence, SP3 filled a tunnel. The lower SEM in Figure 4.9 [Fed94] shows this situation. In contrast, the top SEM in Figure 4.9 shows the situation where the PSG2 did not completely pinch off. This is the what has been simulated using SIMPL. The first case requires 3D simulation and the representation of materials with holes which SIMPL was not designed to handle.

The SIMPL simulation results of the second case are shown in Figures 4.10 and 4.11. In Figure 4.10 no planarization was used which resulted in SP3 stringers and undesirable SP3 filling gaps between the SP2 beams. Again this situation has been exaggerated because no over-etch or extra isotropic etching has been done. Figure 4.11 shows the situation in which the same etch times have been used but instead an SOG planarization step is added. With the SOG filling in the gaps, no undesirable or residual SP3 is present.

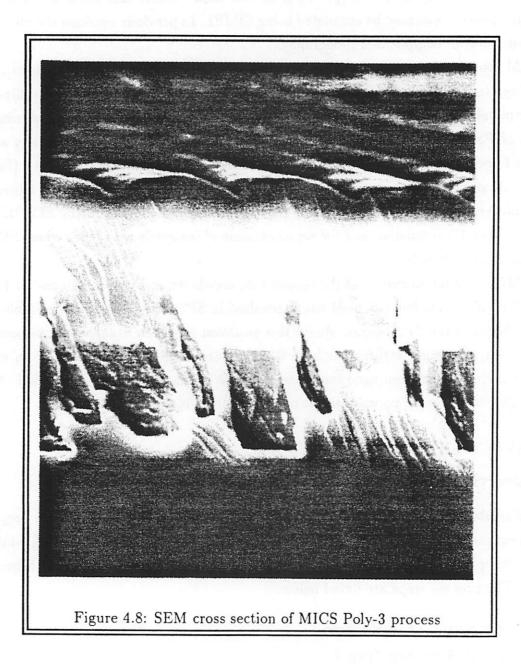
4.3.3 Side Wall Beam Process

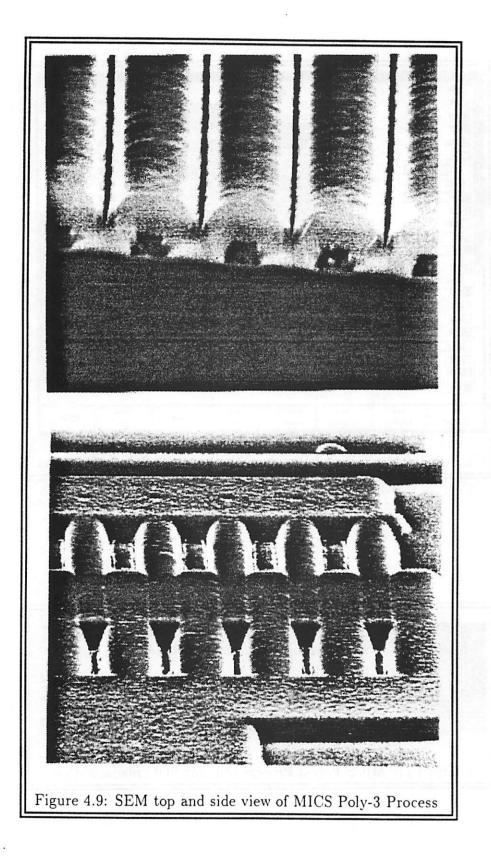
Process Overview

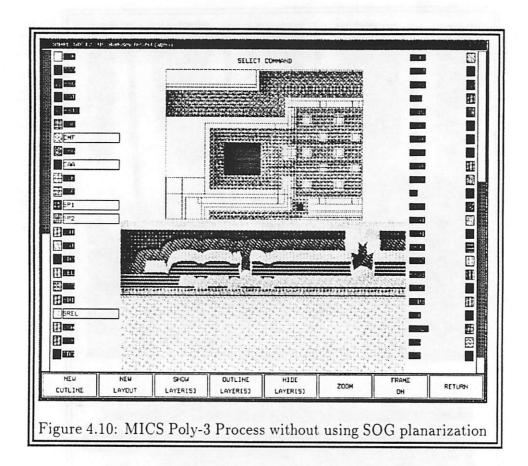
The Side Wall Beam Process [JH93] is a method to fabricate hollow beams with a very low resonant frequency for use in resonators. This process has been simulated using SIMPL. Simulating this process relies on anisotropic etching leaving behind stringers, which become the beams. The process steps are listed below:

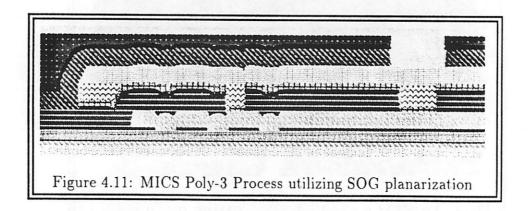
BASIC SIDE WALL BEAM PROCESS

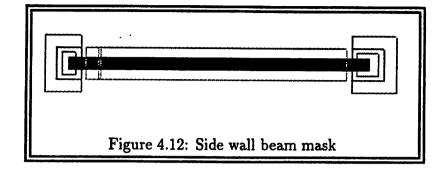
- 1. Deposit 4 um psg (psg 1)
- 2. Lithography mask NP forms mesas of oxide
- 3. Partial anisotropic etch of psg (psg 1)- only 2 um of PSG
- 4. Strip PR, clean wafers
- 5. Deposit 0.2 um polysilicon (poly 1) & 0.2 um psg (psg 2)











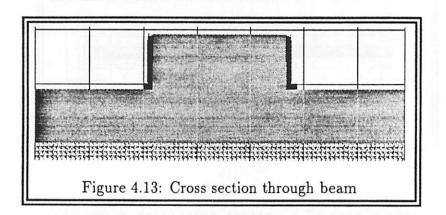
- 6. Lithography mask NS pattern poly (form sidewalls)
- 7. Anisotropic etch of psg (psg 2)
- 8. Anisotropic etch of poly (poly 1)
- 9. Deposit 0.2 um PSG (psg 3)
- 10. Lithography mask NPS contact to poly 1
- 11. Anisotropic etch of psg (psg 3 and psg 2)
- 12. Deposit 2.0 um poly (poly 2)
- 13. Lithography mask ND poly 2
- 14. Anisotropic etch of poly (poly 2)
- 15. Lithography mask NC removal of stringers
- 16. Isotropic etch of poly (poly 2) along sidewalls
- 17. Isotropic etch of all psg layers

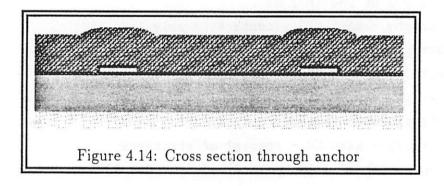
The initial attempts to simulate this process failed because simpl-2 could not handle the simulation of stringers. The etching algorithms had to be significantly altered for this process to work.

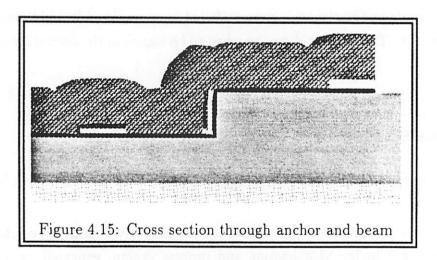
Simulation Cross Sections

Several SIMPL cross sections are shown in Figures 4.13-4.15 and the mask is shown in Figure 4.12.

The various cross sections views demonstrate the non-trivial aspects of this process. SIMPL can greatly aid in the visualization and process design, especially when the user can see the step-by-step process graphically on the computer screen.







4.3.4 BiMOS Technology

Process Overview

A technology to integrate a single-level polysilicon surface micromachined layer with a BiMOS process was developed at Analog Devices [TACS93]. It is used to fabricated the ADXL50 fully integrated surface micromachined accelerometer used to deploy air bags in cars.

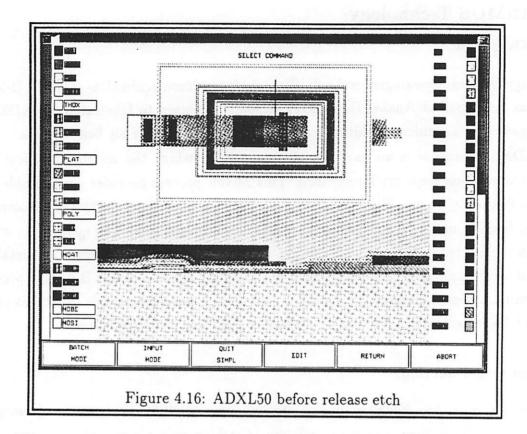
The ADXL50 process is an example of a process in which the micromechanical and electronics fabrication steps are intertwined. This 24-volt process provides considerable circuit design flexibility by providing vertical npns, substrate pnps, lateral pnpn, enhancement PMOS and NMOS, native NMOS, and trimmable thin-film resistors. The connection of the sensor with the electronics is achieved with n+ underpasses in the sensor area-no metalization is used for that purpose. Relatively deep junctions are allowed in this BiCMOS process which permit additional thermal processing for the sensor material anneals as well as other brief dielectrics densifications without severe device performance degradation.

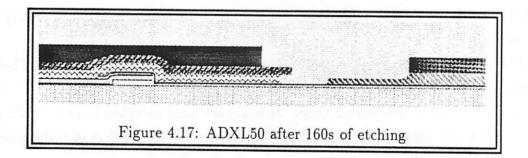
Simulation Cross Sections

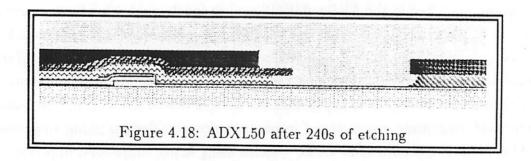
In collaboration with Joe Kung at Analog Devices, the ADXL50 process was developed. One of the initial limitations was the restriction of etching only six non-planar layers. As described in Appendix C the top layers of the profile are exported to SAMPLE for the nonplanar etching simulation. This was extended to total of 20 layers, enough to satisfy the ADXL50 process.

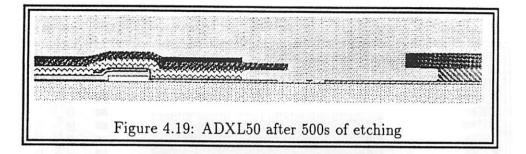
Figure 4.16 shows the cross section, test mask, and cutline of the ADXL50 process before the main release etch. The SAMPLE-nonplanar capabilities are shown in Figures 4.17, 4.18, and 4.19, each showing successive etch times. Special care must be taken to protect the rest of the device during this long release etch. SIMPL can help reveal the effect of etching on all of these layers.

The success of the ADXL50 technology and the awareness of the benefits of increased levels of integration resulted in the ARPA *i*MEMS project involving Analog Devices and the Berkeley Sensor & Actuator Center. The goal of this ongoing project is to integrate VLSI with micromechanics which has not yet been realized. This would extend the number of transistors integrated with microstructures from the current number in the thousands into the hundreds of thousands [P+95]. It is hoped that the devices fabricated with this technology will have orders-of-magnitude improvement in performance over designs using single sense elements. The *i*MEMS approach is to create systems using many simple and imprecise elements. The performance is gained through averaging, matching, and ratiometric techniques.









to reduce noise for example. Target applications include monolithic high-performance multiaxis accelerometers, vibratory rate gyroscopes, mechanical filters, among others.

4.3.5 Metal Beam Process

Process Overview

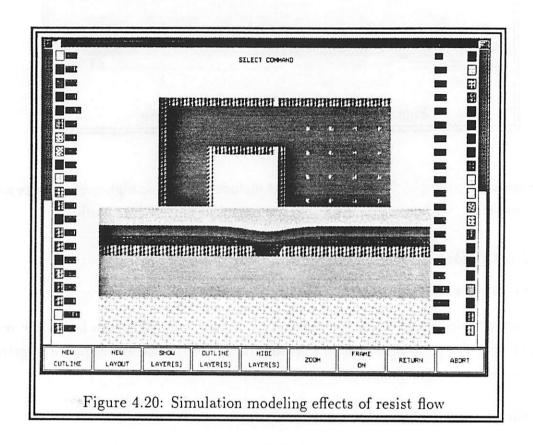
In this unconventional process, the sacrificial layer is resist and the beam layers are metal. Aluminum is used for the capacitor plates because its low resistance was required to gain the necessary capacitance sensitivity.

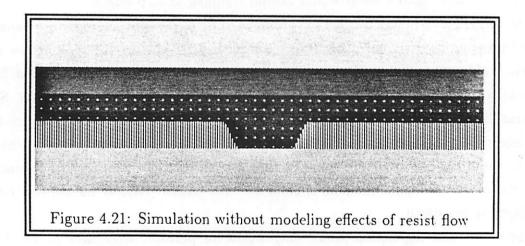
SIMPL Simulation

The spinning of resist, in the old version of SIMPL, was not suited to simulate this process because the top surface of the resist also ended up perfectly flat, no matter what the topography was. Because the beam layer is deposited over the resist, the resist influences its shape. Real resist spun onto a wafer would exhibit thinning at step edges.

To model this effect to first order, the top profile of SIMPL was convoluted with a Gaussian function with an optional sigma. This was accomplished by placing the top surface on a uniform grid, taking the discrete Fourier transform, multiplying it by the Gaussian filter, and then taking the inverse Fourier transform. A specified z-amount is also specified. Some simulation results are shown in Figure 4.20 as compared to a SIMPL simulation in Figure 4.21. without modeling any type of resist flow. An actual SEM showing a similar scenario with the metal beam crossing over a trench is shown in Figure 4.22. The effects of resist spinning are evident by the dip in the metal beam as it cross over the trench. Also at the contact edges, the metal layer slopes down.

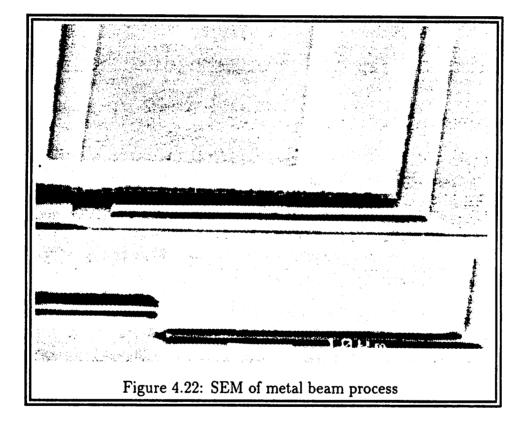
At present this new deposition model only works for periodic structures in which the left and right side of the topography are similar. This could be changed by changing the boundary conditions to mirror each boundary.



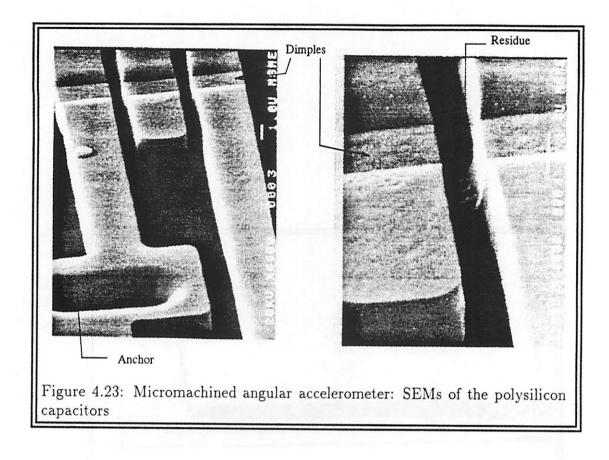


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4.4 Fabrication Test Structures

4.4.1 Residue Problem

Process issues were investigated from the Berkeley dies of the first stage BiCMOS2C run (Analog Devices ADXL50 process). Residue between the fingers of an angular accelerometer were reported at the dimple locations. Initial investigation revealed that the residue was likely polysilicon and was caused a as a result of resist not clearing completely, impairing the etching of the polysilicon while defining the fingers. SEMs of this problem are shown in Figure 4.23 [Bro94].

4.4.2 Test Structure Layout

A variety of test structures, shown in Figure 4.24, have been designed to isolate some of the most likely causes of the residue and are all believed to be lithography related. The possible causes may be due to the following: differences in resist thicknesses resulting in thick resist not clearing completely and impeding the polysilicon etching, reflection from the polysilicon

shoulders of bump areas causing standing wave nulls in the resist, and properties of the mask maker when defining non-Manhattan lines.

The test structures on the bottom half of the figure (forming a semi-circle) are a series of periodic lines and spaces of polysilicon (the beam layer) reproduced every 22.5°, with one set also at 11.25°. The line/space ratios along a radial line starting from the center are 4:1, 2:1, 1:1, 1:2, and 1:3 with the lines always 4.0 μ m wide. The test structures have been rotated at various angles to test the mask makers ability to define non-Manhattan lines. The various line/space ratios will determine the effect of printing isolated and periodic lines. The spoked test structures in the center are 4.0 μ m lines rotated every 11.25° with a 4.0 μ m wide dimple ring. This will test the residue problem at various angles. The other spoked test structure on the left of the figure is similar but the beam spokes are seperated every 22.5°. The test structure between the spoked test structures consists of concentric rings of the beam layer seperated by 0.9, 1.0, 1.1, and 2.0 μ m gaps. This will again test the rotational dependencies and the effect of etching the beam layer out of different size gaps without the presence of the dimple layer.

The remaining test structures located on the top center of the figure are shown in more detail in Figure 4.26. The test structures are made of an inner disk of polysilicon enclosed by an outer ring of polysilicon. The gap between them increases from left to right to assess if the residue is dependent on etching. The gaps are circular to test the angular dependence of the mask maker, and the bump mask width increases from top to bottom to check the dependence of resist thickness variations.

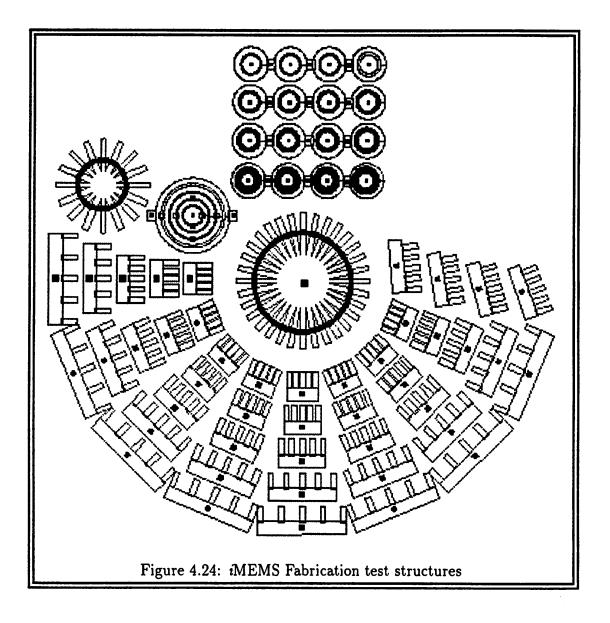
4.4.3 Simulation

Simulation with SIMPL using the lithography capabilities of SAMPLE indicates that the first case of resist not clearing due to resist thickness variations is feasible. The simulation results are shown in Figure 4.25. Cutline A-A' cuts thru a region with a resist thickness of 1.0 μ m while cutline B-B' cuts thru a region with a larger resist thickness of 1.5 μ m because of the bump etch removing 0.5 μ m of oxide. If the lithography is optimized to develop resist 1.0 μ m thick, openings in thicker resist will not be as large and may not clear in some cases. This problem can usually avoided if a longer development times are used or if the resist differences are decreased by spinning on an overall thicker resist coat.

Unfortunately, at the time of this writing the die were not returned in time for examination so the results can not be reported at this time.

A computer program was created to generate the test structures described above. The input is a file containing commands and coordinates and the output is a CIF file containing :

:

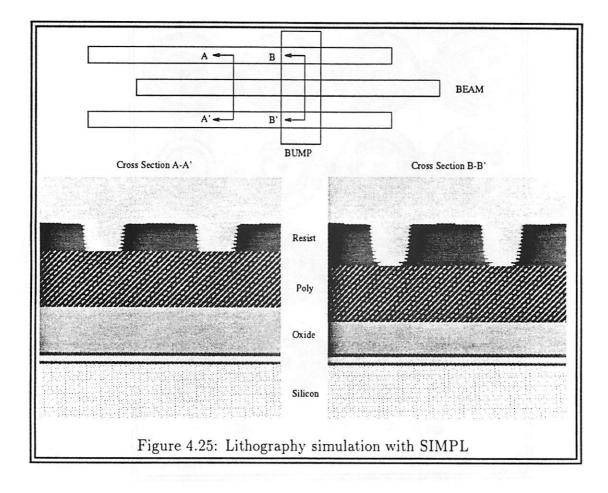


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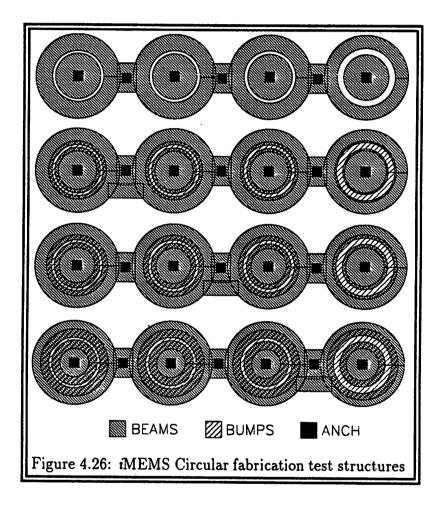
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4.4 Fabrication Test Structures



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CIF polygons. Simple geometry can be entered to create objects which can be copied and rotated by any angle. Future test structures can now be created with less difficulty. A list of commands available can be found in Appendix D.

4.5 Future Work

Though SIMPL has existed for many years, it needs to continue to evolve to keep up with the technology and its applications. The user interface is somewhat outdated and could be improved. Now that many more mask levels are being simulated, a more convenient way of viewing them with the layout editor is required. This has been alleviated by allowing mask to be outlined or hidden, but overlapping color schemes are also desirable and will make simulation results easier to interpret.

Integration with other process simulators also needs improvement. The link to SUPREM needs does not work well for large cross sections requiring large dopant meshes due to memory limitations. Other useful features of SUPREM, such as diffusion with oxidation, are not used. Currently only diffusion can be done in an inert environment. Lithography simulation with the link SAMPLE is limited to planar topographies. More rigorous lithography simulation could be possible with a link to TEMPEST [Won94], a 3D electromagnetic simulator, though this may not always be practical depending on the computing resources available.

Other problems continue to persist, such as the robustness of the etching and deposition routines. Though they have greatly improved, cases exist where they may fail. Smaller problems also exist such as the capability to implant thru material other than oxide. New users will find that normal processes will work fine but may run into trouble if they try something more exotic.

A limited amount of work in the lab has been performed for comparison with SIMPL. This type of work would be useful for calibration and verification of the deposition and etching models. New models could be developed and added to the simulator where the existing ones are inadequate.

Lastly, this work has been limited to 2-D simulation. Key process flow step sequences would benefit from 3-D simulation to examine critical MEM features in detail, especially now that the SAMPLE-3D code has matured and become more stable. Possible 3D cases are the the release of structures, and the formation of the end features on comb fingers which contribute to fringe field effects. Exporting the resulting topographies to mechanical and electrical analysis tools is also now a possibility from the recently added link from to SAMPLE to FastCap [SN95] for interconnect analysis.

4.6 Conclusion

SIMPL has proven to be a very useful tool for studying the complex interrelationships that goes into the fabrication of MEMS devices. Many MEMS related applications have been successfully simulated (See Table 4.3.1) and have provided insight into the fabrication process. It is hoped that with the new capabilities and increased robustness, SIMPL will be accepted as a working tool and establish a large user base. The user guide is quite complete and has a lot of useful information as to get the most from of the existing code. Nevertheless, the code will continue to evolve, as it did in my hands, as well as in the hands of the others before me.

Bibliography

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Chapter 5 Conclusion

The simulation programs SPLAT and SIMPL System 6 have been successfully utilized in the simulation of EUV projection lithography and the fabrication of MEMS devices respectively. Through this effort, new functionality and robustness has been added to both programs.

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SPLAT was applied to several image quality studies taking into account the following characteristics of prototype EUV systems: highly aberrated optics, non-uniformities in the illumination, and non-uniform source geometries. The extensions made to SPLAT included representing aberrations across the pupil with Zernike polynomials and wavefront maps to more accurately model a real system. The image quality studies using a rotating undulator source model showed that source spot to source spot image displacement rather than image degradation for a given source spot location currently limits the resolution. SPLAT was also extended to simulate arbitrary illumination sources and wavefront attenuation. Wavefront attenuation reduced the printability of small features require oversizing dependent on the level of attenuation. The shape of the illumination source proved not to have a major effect on the image quality.

SIMPL has proven to be a very useful tool for studying the complex interrelationships that goes into the fabrication of MEMS devices. Utilizing layout and process flow information SIMPL was successfully used to visualize the cross evolution in the following processes: MICS process, Side Wall Beam process, Analog Devices ADXL50 process, Metal Beam process. and *i*MEMS process. Various MEMS process problems were simulated and compared to lab results. This work was possible through the the new functionality and robustness programmed into SIMPL System 6.

Appendix A File Structure of SIMPL System 6

The directory file structure of SIMPL System 6 is presented below. All nodes represent directories. The SIMPL System 6 Users' Guide can be found in SIMPL_SYS6/DOC which is the best source of information on getting started using SIMPL System 6. Most of the examples used in this report can be found in SIMPL_SYS6/DEMOS/MEMS.

simpl_sys6

demo doc lib scripts src tutorial

simpl_sys6/src

sample1.8b simpl-2 simpl-dix utilities

simpl_sys6/demo

cdram cmos dram epi hunch litho mems nmos npn2 phase planar sdram trench

simpl_sys6/demo/mems

actuator adx150 blade cmos-mics metal_beam position_sensor process_flows resonator test_structure

Appendix B MICS Process Flow

The position sensor in Figure 4.7 was generated with the 'mics.L3.process' listed on the next page. 'L3' stands for Level 3 simulation in which SAMPLE-nonplanar etching and rigorous SAMPLE deposition was used for most of the etching and deposition steps. The other process flows used to generate the examples in this report are available with the standard SIMPL System 6 software release.

```
2 # mics.L3.process
  3 # Front End & Back End process
  5 8
 6 8
 7 # Front End Borkeley HICS Process flew
 8 # Nicrolab CHOS Process
 9 # Versien 2.1 (Jan. 4, 1993)
 10 $ 2um, E-well, double poly-Si, single metal
11 8
12 # simpl-2 etching used for most etching steps
13 # Implantations Hissing
14 #
15
16 # 1: Initial Wet Oxidation (.1)
17 WHICH PROCESS ? OIID
18 OIIDE TRICEMESS (micro-meter) ? 0.1
19 De yeu wish to use default parameters (yes or no) ? yes
20 DO YOU WANT TO DRAW THE CROSS SECTION ? Yes
21
22 # 2: Well Phote Hask
23 WHICH PROCESS ? DEPO
24 NARE OF THE HATERIAL ? RST
25 THICKNESS OF THE NATERIAL (micro-motor) ? 1.000000
26 VERT. SPIN-ON, ISO, ANISO or SAMPLE NEWU (V.S.I.A. or N) ? S
27 DO YOU WANT TO DRAW THE CROSS SECTION ? yes
28
29 # EVELL HASE
30 WHICH PROCESS ? EXPO
31 WHICH RASE 7 CVB
32 INVERT THE MASK (yes or no) ? yes
33 NARE OF THE NATERIAL TO BE EXPOSED ? RST
34 NAME OF THE EXPOSED RESIST ? ERST
35 DO TOU WANT TO DRAW THE CROSS SECTION ? Yes
36
37 WHICH PROCESS ? DEVL
38 WARE OF THE LATER TO BE DEVELOPED ? ERST
39 DO YOU WANT TO DRAW THE CROSS SECTION ? yes
40
41 # 3: Well Implant
42
43 # 4: Well Drive-In: (tex .35)
44
45 # 4.2: Etch pattern inte exide in 5/1 BHF
46 WHICH PROCESS ? ETCH
47 WHICH LAYER DO YOU WANT TO ETCH ? ONID
48 ETCH ALL (yes or no) ? no
49 AROUNT OF VERTICAL ETCH (micre_motor) ? 0.11
50 RATIO X/Z OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.0
51 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
52
53 # 4.3; Remove PR
54 WHICH PROCESS ? ETCH
55 WHICH LAYER DO YOU WANT TO ETCH ? RST
56 ETCH ALL (yes or no) ? yes
```

```
57 u
  58
  59 # 4u.5: Well Drive In
  60 WHICH PROCESS ? ONID
 61 OXIDE THICHNESS (micro-meter) ? 0.300
  62 Do you wish to use default parameters (yes or no) ? yes
  63 DO YOU WANT TO DRAW THE CROSS SECTION ? yes
 64
 65 $ 5.0 Pad Oxidation/Witride Deposition
 66
 67 # 5.2 Remove all exide
 68 WHICH PROCESS ? ETCH
 69 WHICH LAYER DO YOU WANT TO ETCH ? ONID
 70 ETCH ALL (yes or no) ? yes
 71 DO YOU WANT TO DRAW THE CROSS SECTION ? yes
 72
 73 $ 5.4 Dry Czidatien
 74 WHICE PROCESS ? ORID
 75 ONIDE THICKNESS (micro-motor) ? 0.0300
 76 De you wish to use default parameters (yes or no) ? yes
 77 DO YOU WANT TO DRAW THE CROSS SECTION ? yes
 78
 79 $ 5.5 Nitride Deposition
 80 WHICH PROCESS ? DEPO
 61 BASE OF THE RATERIAL ? STRD
 82 THICKNESS OF THE NATERIAL (micre-meter) ? 0.1000
 83 VERT, SPIN-ON, ISO, ANISO or SAMPLE MERU (V.S.I.A. or E) ? I
 84 DO YOU WANT TO DRAW THE CROSS SECTION ? yes
 85
 86 $ 6.0: Active Area Phete
 87 WHICH PROCESS ? EIPO
 68 WHICH HASE ? CAA
 89 INVERT THE MASE (yes or no) ? no
 90 NAME OF THE NATERIAL TO BE EXPOSED ? NTRD
 91 BARE OF THE EXPOSED RESIST ? ERST
 92 DO YOU WANT TO DRAW THE CROSS SECTION ? yes
 93
 94 $ 7.0: Bitride Etch
 95 WHICH PROCESS ? DEVL
 96 MARE OF THE LAYER TO BE DEVELOPED ? ERST
 97 DO YOU WANT TO DRAW THE CROSS SECTION ? yes
 98
 99 # 8.0: Field (P-) Implant Phote (Reversed H-Well Mask)
100 WHICH PROCESS ? DEPO
101 HARE OF THE HATERIAL ? BST
102 THICKNESS OF THE HATERIAL (micro-motor) ? 1.000000
103 VERT. SPIN-CH. ISO, ABISO or SARPLE RERU (V.S.I.A. or H) ? S
104 DD YOU WANT TO DRAW THE CROSS SECTION ? YOS
105
106 # HWELL MASK (Reversed)
107 WHICH PROCESS ? EXPO
108 WHICH HASE ? CWB
109 INVERT THE RASK (yes or no) ? no
110 NAME OF THE NATERIAL TO BE EXPOSED ? RST
111 HARE OF THE EXPOSED RESIST ? ERST
```

```
112 DO YOU WANT TO DRAW THE CROSS SECTION ? yes
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MICS Process Flow

113 114 WHICH PROCESS ? DEVL 115 HARE OF THE LAYER TO BE DEVELOPED ? ERST 116 DO YOU WANT TO DRAW THE CROSS SECTION ? YOS 117 118 # 9.0: Field (P-) Ion implant 119 120 # 10.0: Locos Oxidation (target .65) 121 122 # 10.2 Remove PR 123 WHICH PROCESS ? ETCH 124 WHICH LAYER DO YOU WANT TO ETCH ? RST 125 ETCH ALL (yes or no) ? yes 126 DO YOU WANT TO DRAW THE CROSS SECTION ? yes 127 128 # 10.3 Wet Oxidation 129 WHICH PROCESS ? OXID 130 DAIDE THICKNESS (micro-motor) ? 0.65 131 Do you wish to use default parameters (yes or no) ? yes 132 DO TOU WANT TO DRAW THE CROSS SECTION ? yes 133 134 # 11.0 Bitride Removal 135 WHICH PROCESS ? ETCH 136 WRICH LAYER DO YOU WANT TO ETCH ? STRD 137 ETCH ALL (yes or no) ? yes 138 DO YOU WANT TO DRAW THE CROSS SECTION ? yes 139 140 # 12.0 Sacrificial Oxide 141 WHICH PROCESS ? ETCH 142 WRICH LAYER DO YOU WANT TO ETCH ? ONID 143 ETCH ALL (yes or no) ? no 144 AROUNT OF VERTICAL ETCH (micro_motor) ? .1 145 RATIO 1/2 OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.0 146 DO TOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 147 148 WHICH PROCESS ? OIID 149 DEIDE THICEBESS (micro-motor) ? 0.0200 150 Do you wish to use default parameters (yes or no) ? yes 151 DO YOU WANT TO DRAW THE CROSS SECTION ? yes 152 153 # 13.0 E-Channel Thresheld Implant (blanket) 154 155 # 14.0 P-Channel Thresheld Implant Phote (Use the first mask: H-Well) 156 WHICH PROCESS ? DEPD 157 BARE OF THE NATERIAL ? RST 158 THICRNESS OF THE NATERIAL (micro-meter) ? 1.000000 159 VERT, SPIN-ON, ISO, ANISO or SARPLE NEWU (V.S.I.A. or N) ? S 160 DO YOU WANT TO DRAW THE CROSS SECTION ? yes 161 162 WRICH PROCESS ? EXPO 163 WRICH RASE ? CWR 164 INVERT THE MASK (yes or no) ? yes 165 MANE OF THE NATERIAL TO BE EXPOSED ? MST 166 NAME OF THE EXPOSED RESIST ? ERST 167 DO YOU WANT TO DRAW THE CROSS SECTION ? yes 168

169 WHICH PROCESS ? DEVL 170 WARE OF THE LAYER TO BE DEVELOPED ? ERST 171 DO YOU WANT TO DRAW THE CROSS SECTION ? yes 172 173 # 15.0 P-Channel Threshold Implant (Hask H-Hask) 174 175 WHICH PROCESS ? ETCH 176 WHICH LAVER DO YOU WANT TO ETCH ? RST 177 ETCH ALL (yes or no) ? yes 178 DO YOU WANT TO DRAW THE CROSS SECTION ? yes 179 180 # 16.0: Gate Oxidation/Poly-Si Deposition 181 182 # 16.3 Dip off sacrificial exide 183 184 # 16.4 Dry Oxidation 185 WHICH PROCESS ? OXID 186 DIIDE THICKNESS (micro-motor) ? 0.050 187 De you wish to use default parameters (yes er ne) ? yes 188 DO YOU WANT TO DRAW THE CROSS SECTION ? yes 189 190 # 16.5 Gate Poly Deposition 191 WHICH PROCESS ? DEPO 192 NAME OF THE NATERIAL ? PLYS 193 TRICENESS OF THE HATERIAL (micro-motor) ? 0.45 194 VERT, SPIN-ON, ISO, ANISO or SAMPLE MENU (V.S.I.A. or N) ? I 195 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 196 197 # 17.0: Gate Definition: GATE POLY-CPG 198 WHICH PROCESS ? DEPO 199 NAME OF THE NATERIAL ? rst 200 THICENESS OF THE HATERIAL (micro-motor) ? 1 201 VERT, SPIN-OR, ISO, ANISO or SAMPLE NEWU (V.S.I.A. or N) ? S 202 DO TOU WART TO DRAW THE CROSS SECTION (yes or no) ? yes 203 204 WHICH PROCESS ? EIPO 205 WHICH MASE ? CPG 206 INVERT THE MASE (yes or no) ? no 207 NAME OF NATERIAL TO BE EXPOSED ? THE 208 HANE OF THE EXPOSED RESIST ? orst 209 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 210 211 WHICH PROCESS ? DEVL 212 NAME OF THE LATER TO BE DEVELOPED ? orst 213 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 214 215 # 18.0: Plasma Etch pely-Si (PLYG) 216 # Starting Thickness = 0.45 217 218 WHICH PROCESS ? ETCH 219 WHICH LAYER DO YOU WANT ETCH ? PLYO 220 ETCH ALL (yes or no) ? no 221 AROUNT OF VERTICAL ETCH (micre_meter) ? 0.60 222 RATIO X/Z OF ETCHIEG (0.0 <= RATIO <= 1.0) ? 0.1 223 DO TOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes

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224

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225 # PR Strip 226 227 WHICH PROCESS ? ETCH 228 WHICH LAVER DO YOU WANT TO ETCH ? rst 229 ETCH ALL (yes er ne) ? yes 230 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 231 232 \$ 19.0: Capacitor Fernation: 233 # Dry Oxidation (SINPL must deposit exide) 234 235 # 19.3 Dry Oxidation 236 WHICH PROCESS ? DEPO 237 NAME OF THE NATERIAL ? CAPO 238 THICENESS OF THE NATERIAL (micro-motor) ? .08 239 VERT, SPIN-ON, ISO, ANISO or SAMPLE HERU (V.S.I.A. or N) ? I 240 DO TOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 241 242 \$ 19.4 Deposit Capacitor Poly 243 WHICH PROCESS ? DEPO 244 WARE OF THE MATERIAL ? PLYC 245 THICKNESS OF THE NATERIAL (micro-motor) ? .45 246 VERT, SPIN-ON, ISO, ANISO or SAMPLE HERU (V.S.I.A. or H) ? I 247 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 248 249 • 20.0 Capacitor Photo Hask: CAP POLY-CEL 250 251 WHICH PROCESS ? DEPO 252 NARE OF THE NATERIAL ? RST 253 THICEBESS OF THE NATERIAL (micro-motor) ? 1 254 VERT. SPIN-OR. ISO. ANISO or SAMPLE NEWU (V.S.I.A. or N) ? S 255 DO TOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 256 257 WHICH PROCESS ? ELPO 258 WHICH HASK ? CEL 259 INVERT THE MASK (yes or no) ? no 260 MARE OF RATERIAL TO BE EXPOSED ? BST 261 HARE OF THE EXPOSED RESIST ? orst 262 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 263 264 WHICH PROCESS ? DEVL 265 BARE OF THE LATER TO BE DEVELOPED ? erst 266 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 267 268 • 21.0: Plasma etch capaciter pely-Si (PLTC) 269 • Starting Thickness = 0.45 270 271 WEICH PROCESS ? ETCH 272 WHICH LAYER DO YOU WANT ETCH ? PLYC 273 EICE ALL (ves er ne) ? ne 274 AROUNT OF VERTICAL ETCH (micro_meter) ? 0.60 275 RATIO E/Z OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.0 276 DO YOU WART TO DRAW THE CROSS SECTION (yes or no) ? yes 277 276 • PR Strip 279 280 WHICH PROCESS ? ETCH

281 WHICH LAYER DO YOU WANT TO ETCH ? rst 282 ETCH ALL (yes or no) ? yes 283 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 284 285 # 22.0 #+ S/D Photo 286 267 # 23.0 #+ S/D Implant: Arsenic 288 289 # 24.0 #+ S/D Anneal 290 291 # 25.0 P+ S/D Phete 292 293 # 26.0 P+ S/D Implant: Arsenic 294 295 \$ 27.0 PSG Deposition and Densification 296 297 # 27.3 298 WHICH PROCESS ? DEPO 299 NAME OF THE NATERIAL ? PSGO 300 THICEMESS OF THE MATERIAL (micro-motor) ? 0.7 301 VERT. SPIN-OF, ISO, ANISO or SAMPLE HERU (V.S.I.A. or H) ? H 302 SOURCE TYPE (U.D.H.C. or P) ? N 303 SPUTTERING SOURCE ANGLE (degrees, e.g. 45.0) ? 45 304 Include Surface Higration (T or H) ? T 305 VARIANCE IN ATOMIC ROTION (um, e.g. 0.181) 7 .05 306 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 307 308 • 28.0: Contact Photo Hask 309 WHICH PROCESS ? DEPO 310 BARE OF THE NATERIAL ? PAL 311 THICENESS OF THE MATERIAL (micro-motor) ? 1 312 VERT, SPIN-ON, ISO, ANISO or SAMPLE NERU (V.S.I.A. or N) ? S 313 DO YOU WART TO DRAW THE CROSS SECTION (yes or no) ? yes 314 315 WHICH PROCESS ? EXPO 316 WHICH MASK ? CCA 317 INVERT THE NASK (yes or no) ? yes 318 MANE OF WATERIAL TO BE EXPOSED ? rat 319 MARE OF THE EXPOSED RESIST ? erst 320 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 321 322 WHICH PROCESS ? DEVL 323 MARE OF THE LAYER TO BE DEVELOPED ? orst 324 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 325 326 • 29.0: Centact Etch (PSGO, CAPO, and OIID) 327 WHICH PROCESS ? ETCH 328 WHICE LATER DO YOU WANT ETCH ? PSGO 329 ETCH ALL (yes er ne) ? ne 330 ANOUNT OF VERTICAL ETCH (micre_motor) ? 0.8 331 RATIO 1/2 OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.9 332 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 333 334 WHICH PROCESS ? ETCH 335 WHICH LAYER DO YOU WANT ETCH ? CAPO

336 ETCH ALL (yes or ne) ? no

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MICS Process Flow

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337 ARGUNT OF VERTICAL ETCH (micro_motor) ? 0.1
338 RATIO I/Z OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.0
339 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
340
341 WHICH PROCESS ? ETCH
342 WHICH LAYER DO YOU WANT ETCH ? OXID
343 ETCH ALL (ves er ne) ? no
344 AROUNT OF VERTICAL ETCH (micre_motor) ? 0.2
345 RATIO I/Z OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.0
346 DO TOU WART TO DRAW THE CROSS SECTION (yes or no) ? yes
347
348 • PR Strip
349
350 WHICH PROCESS ? ETCH
351 WHICE LAYER DO YOU WANT TO ETCH ? rst
352 ETCH ALL (yes or no) ? yes
353 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
354
355 # 30.0 Back side etch
356
357
359 8
                    NICS BACKEND PROCESS
361 # SAMPLE nonplanar etching used.
362 # poly3 steps emitted
363 8
364
365 • 31: TiSi2 Fermation
366
367 4 32: Tungston Notallization
368
369 WHICE PROCESS ? DEPO
370 HARE OF THE NATERIAL ? H1
371 THICHNESS OF THE NATERIAL (micro-motor) ? 0.6
372 VERT. SPIN-ON, ISO, ANISO or SANPLE NEWU (V.S.I.A. or N) ? I
373 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
374
375 • 33: Netal Photo Hask
376
377 WHICH PROCESS ? EXPO
378 WRICE RASE ? CH?
379 INVERT THE MASE (yes or no) ? no
300 BARE OF HATERIAL TO BE EXPOSED ? HI
301 BARE OF THE EIPOSED RESIST ? orst
382 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
383
384 • 34: Tungston / Tintanium Etch
385
386 WHICH PROCESS ? DEVL
387 HANE OF THE LAYER TO BE DEVELOPED ? erst
388 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
389
390 + 35 Sintering and Test:
391
392 • 36: Std Tungsten Clean
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393 394 • 37 - CHOS PASSIVATION 395 396 WHICH PROCESS ? DEPO 397 NAME OF THE HATERIAL ? PSGP 398 THICKNESS OF THE RATERIAL (micro-motor) ? .4 399 VERT. SPIN-ON, ISO, ANISO or SAMPLE REAU (V.S.I.A. or M) ? H 400 SOURCE TYPE (U.D.H.C.or P) ? H 401 SPUTTERING SOURCE ANGLE (degrees, e.g. 45.0) ? 45 402 Include Surface Rigration (Y or B) ? Y 403 VARIANCE IN ATOHIC NOTION (um. +.g. 0.181) 7 .05 404 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 405 406 WHICE PROCESS ? DEPD 407 HARE OF THE RATERIAL ? HTDP 408 THICRNESS OF THE NATERIAL (micro-meter) ? 0.18 409 VERT, SPIN-ON, ISO, ANISO or SAMPLE NEWU (V.S.I.A. or M) ? ISO 410 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 411 412 • 38 - Inter CROS-ustructure Centact Hask: SHT (chreme-df) 413 414 WHICH PROCESS ? DEPG 415 NARE OF THE NATERIAL ? RST 416 THICKNESS OF THE NATERIAL (micro-motor) ? 1 417 VERT, SPIN-OR, ISO, ANISO or SAMPLE MEMU (V.S.I.A. or M) ? S 418 DO YOU WART TO DRAW THE CROSS SECTION (yes or no) ? yes 419 420 WHICH PROCESS ? EXPO 421 WHICH HASE ? SHT 422 INVERT THE HASE (yes or no) ? yes 423 NAME OF NATERIAL TO BE EXPOSED ? RST 424 NAME OF THE EXPOSED RESIST ? orst 425 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 426 427 WHICH PROCESS ? DEVL 428 NAME OF THE LATER TO BE DEVELOPED ? ERST 429 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 430 431 • 39: Nitride Passivation Etch 432 • Starting Thickness = 0.2 433 434 WHICH PROCESS ? ETCH 435 Etch Type:Isetrepic, or Ise with Directional (1 or 10) ? 10 436 File containing etch rates ? nitride.plasma.etch.med 437 Etch accuracy (0:worst to 10:best) ? 10 438 Timestep in seconds ? 2 439 Humber of steps ? 1 440 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 441 442 WHICH PROCESS ? ETCU 443 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 444 445 • 40 : Oxide Passivation Etch 446 . Includes etching of (PSGO, PSGP, and CAPO) 447 WHICH PROCESS ? ETCH 448 Etch Type: Isotropic, or Iso with Directional (1 or 10) ? 10

449 File containing etch rates ? psg.plasma.etch.mod 450 Etch accuracy (O:werst to 10:best) ? 10 451 Timestep in seconds ? 14 452 Sumber of steps ? 1 453 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 454 455 WHICH PROCESS ? ETCU 456 DO YOU WART TO DRAW THE CROSS SECTION (yes or no) ? yes 457 458 • 41: PR Strip 459 460 WHICH PROCESS ? ETCH 461 WHICH LAYER DO YOU WANT TO ETCH ? RST 462 ETCH ALL (yes er ne) ? yes 463 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 464 465 • 42: Ustructure Poly1 Depostition: 466 467 WHICH PROCESS ? DEPO 468 HARE OF THE NATERIAL ? SPOI 469 THICENESS OF THE NATERIAL (micro-motor) ? 0.3 470 VERT, SPIN-ON, ISO, ANISO or SAMPLE NEWU (V.S.I.A. or H) ? I 471 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 472 473 ? 5870 474 ? after.spl.depesition.cress 475 476 • 43: Ustructure Poly Mask: SPi (emulsion-cf) 477 478 WHICE PROCESS ? DEPO 479 BARE OF THE NATERIAL ? BST 480 THICRNESS OF THE RATERIAL (micro-motor) ? 1 481 VERT, SPIN-OR, ISO, ANISO or SAMPLE MERU (V.S.I.A. or N) ? S 482 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 483 484 WHICH PROCESS ? EXPO 465 WHICH HASE ? SP1 486 INVERT THE MASE (yes or no) ? no 487 BARE OF RATERIAL TO BE EXPOSED ? RST 488 TARE OF THE EXPOSED RESIST ? ERST 489 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 490 491 WHICH PROCESS ? DEVL 492 BARE OF THE LAYER TO BE DEVELOPED ? ERST 493 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 494 495 • 44: Poly1 Etch (SP01) 496 497 WHICH PROCESS ? ETCH 498 Etch Type:Isetrepic, or Ise with Directional (1 or 10) ? 10 499 File containing etch rates ? ply.plasma.etch.mod S00 Etch accuracy (0:werst to 10:best) ? 10 501 Timestep in seconds ? 3 502 Eumber of steps ? 1 503 DD YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 504

505 WHICH PROCESS ? ETCU 506 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 507 508 • 45: PR STRIP 509 510 WHICH PROCESS ? ETCH 511 WHICH LAYER DO YOU WANT TO ETCH ? RST 512 ETCH ALL (yes or no) ? yes 513 DO TOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 514 515 • 46: Sacrificial PSG Deposition 516 517 WHICH PROCESS ? DEPO 518 NAME OF THE NATERIAL ? PSG1 519 THICKNESS OF THE WATERIAL (micro-motor) ? 2 520 VERT, SPIN-ON, ISO, ANISO or SAMPLE MEMU (V.S.I.A. or M) ? M 521 SOURCE TYPE (U,D,H,C,or P) ? H 522 SPUTTERING SOURCE ANOLE (degrees, e.g. 45.0) ? 45 523 Include Surface Higration (Y or H) ? Y 524 VARIANCE IN ATONIC NOTICE (um, e.g. 0.181) ? .05 525 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 526 527 ? save 528 ? after.psgl.depesition.cress 529 530 • 47: RTA for Sacrificial PSG Densification 531 532 WRICH PROCESS ? DEPO 533 NAME OF THE MATERIAL ? rst 534 THICKNESS OF THE NATERIAL (micro-motor) ? 1 535 VERT, SPIN-ON, ISO, ANISO or SANPLE NERU (V.S.I.A, or N) ? S 536 DD YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 537 538 + 48: Dimple Phote Hask: SD1 (same as SD2) (chreme-df) 539 540 WHICH PROCESS ? EXPO 541 WHICH HASK ? SD2 542 INVERT THE MASE (yes or no) ? yes 543 NAME OF NATERIAL TO BE EXPOSED ? FAS 544 MANE OF THE EXPOSED RESIST ? erst 545 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 546 547 WHICH PROCESS ? DEVL 548 HARE OF THE LAYER TO BE DEVELOPED ? orst 549 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 550 551 • 49: Dimple Formation 552 . Etch PSG1 \$53 554 WHICH PROCESS ? ETCH 555 Etch Type:Isotropic, or Iso with Directional (1 or 10) ? 1 556 File containing etch rates ? psg.wet.etch.med 557 Etch accuracy (O:werst to 10:best) ? 10 558 Timestep in seconds ? 10 559 Number of steps ? 1 560 DD YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes

561 562 WHICH PROCESS ? ETCU 563 DD YOU WART TO DRAW THE CROSS SECTION (yes or no) ? yes 564 565 ? save 566 ? after.dimple.etch.cress 567 568 • 50.0: PR Strip 569 570 WHICH PROCESS ? ETCH 571 WHICH LAYER DO YOU WANT TO ETCH ? RST 572 ETCH ALL (yes er ne) ? yes 573 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 574 575 . 51: uStructure Ancher Photo Hask: SG1 (chromo-df) 576 577 WHICH PROCESS ? DEPO 578 NAME OF THE NATERIAL ? rst 579 THICKNESS OF THE NATERIAL (micro-motor) ? 1 560 VERT, SPIN-CH, ISO, ANISO or SANPLE NEBU (V.S.I.A. or N) ? S 581 DO TOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 582 583 WRICE PROCESS ? EXPO 584 WHICH MASK ? 5G1 585 INVERT THE MASK (yes or no) ? yes 586 NAME OF NATERIAL TO BE EXPOSED ? FAC 587 NAME OF THE EXPOSED RESIST ? orst 588 DO YOU WART TO DRAW THE CROSS SECTION (yes or no) ? yes 589 590 WHICH PROCESS ? DEVL 591 BARE OF THE LATER TO BE DEVELOPED ? orst 592 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 593 594 • 52: Thick Oxide Etch (Plasma Etch) 595 • starting thickness = 2.0 596 597 WHICH PROCESS ? ETCH 598 Etch Type:Isetropic, or Ise with Directional (1 or 10) ? 10 599 File centaining etch rates ? psg.plasma.etch.med 600 Etch accuracy (O:werst to 10:best) ? 10 601 Timestep in seconds ? 20 602 Number of steps ? 1 603 DO TOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 604 605 WHICH PROCESS ? ETCU 606 DO TOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 607 608 • 53: PR Strip 609 610 WHICH PROCESS ? ETCH 611 WHICH LATER DO YOU WANT TO ETCH ? rst 612 ETCH ALL (yes er ne) * yes 613 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 614 615 • 54: uStructure Pely2 Deposition 616

617 WHICH PROCESS ? DEPO 618 MANE OF THE HATERIAL ? SP02 619 THICRNESS OF THE NATERIAL (micro-motor) ? 2.0 620 VERT. SPIN-ON. ISO. ANISO or SANPLE NERU (V.S.I.A. or M) ? I 621 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 622 623 ? save 624 ? after.sp2.depositien.cress 625 626 • 55: PSG Oxide Nask Deposition 627 628 WHICH PROCESS ? DEPO 629 NAME OF THE NATERIAL ? OR1 630 THICEMESS OF THE NATERIAL (micro-motor) ? 0.5 631 VERT, SPIN-ON, ISO, ANISO or SAMPLE MEMU (V.S.I.A. or M) ? M 632 SOURCE TYPE (U.D.H.C. or P) ? N 633 SPUTTERING SOURCE ANGLE (degrees. e.g. 45.0) ? 45 634 Include Surface Rigration (Y or E) ? Y 635 VARIANCE IN ATORIC NOTION (um, e.g. 0.181) ? .05 636 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 637 638 • 56: RTA Polysilicon stress relief anneal 639 640 • 57: uStructure Pely2 Mask: SP2 641 642 WHICH PROCESS ? DEPO 643 BARE OF THE HATERIAL ? rst 644 THICHNESS OF THE HATERIAL (micro-motor) ? 1 645 VERT. SPIN-ON, ISO, ANISO or SAMPLE HERU (V.S.I.A. or M) ? S 646 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 647 648 WRICH PROCESS ? EIPO 649 WHICH HASE ? SP2 650 INVERT THE MASK (yes or no) ? no 651 BARE OF MATERIAL TO BE EXPOSED ? IST 652 BARE OF THE EXPOSED RESIST ? erst 653 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 654 655 WHICH PROCESS ? DEVL 656 NAME OF THE LATER TO BE DEVELOPED ? erst 657 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 658 659 + 58: Oxide Etch (OR1) 660 661 WHICH PROCESS ? ETCH 662 Etch Type:Isotrepic, or Iso with Directional (1 or 10) ? 10 663 File centaining etch rates ? psg.plasma.etch.med 664 Etch accuracy (O:worst to 10:best) ? 10 665 Timestep in seconds ? 5 666 Number of steps ? 1 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 667 668 669 WHICH PROCESS ? ETCU 670 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 671 672 ? save

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673 ? befere.sp2.etch.cress 674 675 • 59: Structural Poly2 Etch (SP02) 676 • starting thickness = 2.0 677 678 WHICH PROCESS ? ETCH 679 Etch Type:Isotropic, or Iso with Directional (1 or 10) ? 10 680 File containing etch rates ? ply.plasma.etch.mod 681 Etch accuracy (O:werst to 10:best) ? 10 682 Timestep in seconds ? 25 683 Humber of steps ? 1 684 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 685 686 WHICH PROCESS ? ETCU 687 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 688 689 + 60: PR Strip 690 WHICH PROCESS ? ETCH 691 WHICH LAYER DO TOU WANT TO ETCH ? IST 692 ETCH ALL (yes er ne) ? yes 693 DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes 694

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695 • 61: Back Side Etch
696
697 + 62: uStructure Release
698
699 ? save
700 ? before.release.cress
701
702 WHICH PROCESS ? ETCH
703 WHICH LAYER DO YOU WANT TO ETCH ? GN1
704 ETCH ALL (yes or no) ? yes
705 DO YOU WANT TO DRAW THE CROSS SECTION (yes er ne) ? yes
706
707 WHICH PROCESS ? ETCH
708 WHICH LAYER DO YOU WANT TO ETCH ? PSG1
709 ETCH ALL (yes or ne) ? yes
710 DO YOU WART TO DRAW THE CROSS SECTION (yes or no) ? yes
711
712 ? save
713 ? final.cross
714 WHICH PROCESS ? END
715
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Appendix C Etching in SIMPL

There are three different ways to simulate etching in SIMPL. The easiest way is to use the mask as a "cookie cutter" to remove material which results in straight edges. Using this method, resist does not need to be deposited. The material is treated as resist and exposed and etched away. All exposed material is removed regardless if the material is very thick or filling narrow cracks. This method of etching is referred to as "exposure" etching.

The second method of etching is to deposit resist and etch vertically with an optional undercut ratio. This type of etching is referred to as "SIMPL" etching because SIMPL performs the etching internally. This gives fairly good results because stringers can be created.

The most rigorous method of etching is to call SAMPLE non-planar etching. The topography in SIMPL is taken one layer at a time to make a SAMPLE input file. SIMPL assigns to each layer an isotropic and/or directional etch by looking up the corresponding etch rates in an etch-rate (library) file. Directional and isotropic etch rates for materials layers are entered into this file by the user. This avoids the need to type in the etch rates manually one at a time. The new SAMPLE nonplanar etching capabilities are mainly due to the efforts of Andrej Gabara with his revamping of the "stitch back" code.

Please refer to the SIMPL System 6 Users' Guide for more information about etching.

Appendix D

Test Structure Generator Commands

The following commands are available in the TSGEN program for the generation of layout test structures.

nameCell	cellName
createObject	objectID
copyObject	newObject oldObject
deleteObject	objectID
combineObjects	objectID1 objectID2 destObjectID
generateRadialLines	objectID material xC yC width length startAngle endAngle deltaAngle
generateHorizontalLines	objectID material xStart yStart width length period nLines
generateBox	objectID material xStart yStart width height
generateCIFBox	objectID material width height xCenter yCenter
generateCircle	objectID material xC yC radius segments
generateRing	objectID material xC yC innerRadius outerRadius segments
rotateObject	objectID angle
translateObject	objectID deltaX deltaY
centerObject	objectID centerX centerY
printObjects	CIF or XGRAPH
?	: help
help	: help
version	: version

The input file to create the test structures in Figure 4.26 is given below.

```
1 nameCell circles_side
  2 # .9 um gap 6.0 um bump
  3 createObject 1
  4 generateCircle 1 beams 0 0 700 200
  5 generateRing 1 beams 0 0 790 1300 200
6 generateRing 1 bumps 0 0 445 1045 200
7 $ 1.0 um gap 6um bump
  8 createObject 2
  9 generateCircle 2 beams 0 0 700 200
10 generateRing 2 beams 0 0 800 1300 200
11 generateRing 2 bumps 0 0 450 1050 200
12 translateObject 2 3000 0
13 $ 1.1 um gap 6.0 um bump
14 createObject 3

        Ib
        generateCircle 3 beams 0 0 700 200

        16
        generateRing 3 beams 0 0 810 1300 200

        17
        generateRing 3 bumps 0 0 455 1055 200

        18
        translateObject 3 6000 0

19 $ 2.0 um gap 6.0 um bump
20 createChiect 4
21 generateCircle 4 beams 0 0 700 200
22 generateRing 4 beams 0 0 900 1300 200
23 generateRing 4 bumps 0 0 500 1100 200
24 translateObject 4 9000 0
25 $
26 # .9 um gap 4.0 um bump
27 createObject 5
28 generateCircle 5 beams 0 0 700 200

        29
        generateRing
        5
        beams
        0
        790
        1300
        200

        30
        generateRing
        5
        bumps
        0
        545
        945
        200

31 translateObject 5 0 3000
32 $ 1.0 um gap 4.0 um bump
33 createObject 6
34 generateCircle 6 beams 0 0 700 200

        35
        generateRing
        6
        beams
        0
        800
        1300
        200

        36
        generateRing
        6
        bumps
        0
        550
        950
        200

37 translateDbject 6 3000 3000
38 $ 1.1 um gap 4.0 um bump
39 createObject 7
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76 printDbjects CIF

77 SprintObjects AGRAPH

78

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