DC POWER SUPPLY DESIGN IN PORTABLE SYSTEMS

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1 Introduction

Portable electronic equipment demands ultra-low-power hardware to maximize system run-time. Perhaps the most effective way to reduce power dissipation and maintain computational throughput is to operate each sub-system at its optimum supply voltage and compensate for the resulting decrease in performance by exploiting parallelism and pipelining [1]. This low-power design strategy assumes that the supply voltage is a free variable and can be set to any arbitrarily low level with little penalty. Because general purpose batteries come in discrete voltage levels which may not be optimal for a given circuit, a DC-DC converter may be required to convert the battery source voltage to a higher voltage, a lower voltage, or a voltage of inverse polarity. Consider, for example, the multimedia InfoPad terminal [2, 3, 4]. The custom hardware in the current InfoPad terminal, including the RF transceiver, baseband circuitry, and speech, pen, and text/graphics I/O chipset [5], is being designed to operate at each component's optimum supply voltage to minimize its power consumption. Thus, a number of low voltage (from 3 V to 1.1 V), low current (as low as 5 mA) DC power supplies must be supported by a single battery source, requiring a number of DC-DC converter outputs.

Voltage regulation as an interface between the battery source and load can further enhance system run-time. A circuit may be designed such that its optimum operating voltage is the end-of-life voltage of a specific cell, apparently minimizing its power consumption without the use of a DC-DC converter. This not only makes the circuit design challenging (the voltage of a typical AA-type

lithimum ion cell may vary by as much as ±20% of its nominal value throughout its discharge), but because the cell discharge charactersitic is not flat, the circuit will consume greater than its minimum operating power from the cell throughout the majority of its discharge. If a DC-DC converter is inserted between the cell and the load, and the converter's output voltage is maintained down to the end-of-life cell voltage, the circuit will consume its minimum operating power independent of the cell voltage, substantially extending system run-time (by as much as 50% for a digital CMOS circuit powered by a single lithium ion cell).

Because energy is a scarce resource in battery-operated systems, DC-DC converters must dissipate minimal energy to conserve battery capacity. In most low-power hardware, unused circuitry is powered-down and gated clocks are employed to reduce power consumption during idle mode [6]. Such techniques may present severe load variations (up to several orders of magnitude), and the system may idle for a large fraction of the overall run-time. This implies the need for a high conversion efficiency not only under full load, but over a large load variation. Furthermore, in the ultra-low-power applications common to portable systems, the quiescent operating power (control power) of the regulator must be kept to an even lower level to ensure that it does not contribute significantly to the overall dissipation. For example, a multimedia chipset has been demonstrated in [5] which supports speech I/O, pen input and full motion video, and consumes less than 5 mW at 1.1 V. The control circuit for a converter supplying this chipset must have substantially lower quiescent power.

The portability requirement places severe constraints on physical size and mass. While high-efficiency DC-DC conversion can substantially improve system run-time in virtually any battery-operated application, this same enhancement of run-time may also be achieved by simply increasing the capacity of the battery source. However, if voltage conversion is performed by highly-integrated CMOS converters custom-designed to their individual loads, their volume will typically be much smaller than the volume of the additional battery capacity required to achieve the equivalent extension of run-time.

This document, which describes the design of highly-integrated custom CMOS DC-DC converters, is organized as follows: Section 2 illustrates the enhancements to overall system run-time that can be achieved through DC-DC conversion. In Section 3, highly-integrated CMOS implementations of the three basic non-isolated switching regulator topologies—buck, boost, and buck-boost—are introduced. Since existing integrated circuit (IC) technology cannot provide inductors or capacitors of suitable value and quality for power conversion, such designs often require several off-chip reactive elements for energy storage and filtering. These components will dominate the overall volume of the converter. Thus, in Section 5, design techniques to reduce the physical sizes of these components are shown. To compensate for the increase in dissipation associated with converter miniaturization, several circuit design techniques which can improve the efficiency of the converter are described in Section 6. In Section 9, ultra-low quiescent operating power pulse-width modulators are addressed. Section 8 pro-

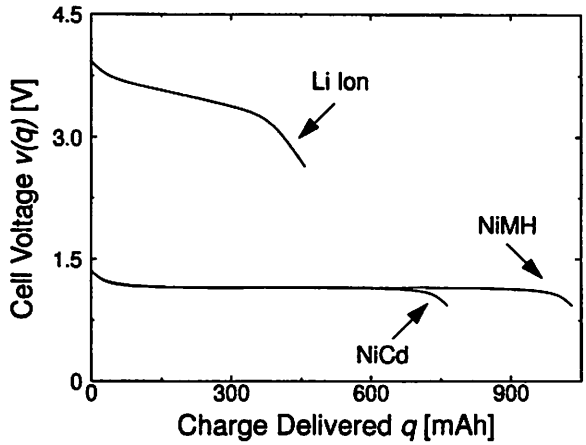


Figure 1: Typical low-rate discharge characteristics for AA-type Nickel Cadmium (NiCd), Nickel Metal Hydride (NiMH), and Lithium Ion (Li Ion) cells. Data is approximated from [7].

vides an overview of issues related to physical design, including IC layout, issues in magnetic component design, a brief survey of capacitor technologies, and an overview of board-level assembly. Finally, in Section 10, alternative DC-DC converters are introduced which may be useful in ultra-low-power applications where voltage conversion or regulation is required, but magnetics design becomes unmanagable.

2 Voltage Regulation Enhances System Runtime

Figure 1 shows typical low-rate battery discharge curves for three commercially available AA-type secondary battery sources: Nickel Cadmium (NiCd), Nickel Metal Hydride (NiMH), and Lithium Ion (Li Ion). Consider a block of throughput-constrained logic run directly from a NiMH cell and designed to operate down to the end-of-life cell voltage. If the power consumption of the logic is dominated by the dynamic component, and the circuitry is clocked at a frequency $f_{0.9}$ to meet throughput constrainsts at the minimum cell voltage $v(q) = 0.9$ V, then the circuitry will consume a minimum power at the end of the usable cell life:

$$P_{L-min} = f_{0.9} \cdot C_{eff} \cdot 0.9^2. \quad (1)$$

Here, C_{eff} is the effective switching capacitance (commonly expressed as the product of a lumped physical capacitance and an activity factor [8]). However, at other points q in the cell discharge characteristic $v(q)$, the power consumption

of the circuitry is given by:

$$P_L(q) = f_{0.9} \cdot C_{eff} \cdot v^2(q) = P_{L-min} \cdot \frac{v^2(q)}{0.9^2}. \quad (2)$$

At initial cell voltage, this is a factor of 2.78 times P_{L-min}, and at nominal cell voltage, a factor of 1.78 times P_{L-min}. Thus, the load is seen to consume greater than minimum power throughout the cell discharge without increased throughput.

If a DC-DC converter with efficiency:

$$\eta \equiv \frac{P_{out}}{P_{in}} \quad (3)$$

and zero dropout voltage is inserted between the battery and the load, and the output of the converter is regulated to the end-of-life cell voltage, the logic consumes P_{L-min} independent of the cell voltage, and the power drawn from the cell at any point q in its discharge characteristic is constant and equal to:

$$P(q) = \frac{P_{L-min}}{\eta}. \quad (4)$$

In this section, a mathematical model is developed to estimate the impact of DC-DC conversion on system run-time. This analysis considers analog circuitry with supply-independent biasing and throughput-constrained digital CMOS circuitry, and compares system run-time when these loads are run directly from the battery source, and from the battery source at a minimum voltage through a linear regulator or a switching regulator.

2.1 A Piecewise Linear Model to a Low-Rate Battery Discharge Curve

A piecewise linear model which approximates a typical low-rate cell discharge curve is constructed in Figure 2. The battery discharge characteristic is described by its cell voltage $v(q)$ after a charge, q, has been delivered to the load. At full capacity ($q = 0$), the cell has an initial voltage $v(0) = V_1$. The nominal cell voltage lies in the range $V_2 \leq v(q) \leq V_3$ from a delivered charge $Q_1 \leq q \leq Q_2$. At the end of its usable life ($q = Q_A$), the cell voltage drops to $v(Q_A) = V_4$. The energy available in the cell at full capacity, E_A, is the area under the entire discharge curve. The mean cell voltage (averaged over the delivered charge, q) is $\overline{v(q)} = E_A/Q_A$. The system run-time, t_A, is found by solving the following differential equation which governs the cell discharge at any point q in the discharge characteristic:

$$\dot{q} = i(q), \quad (5)$$

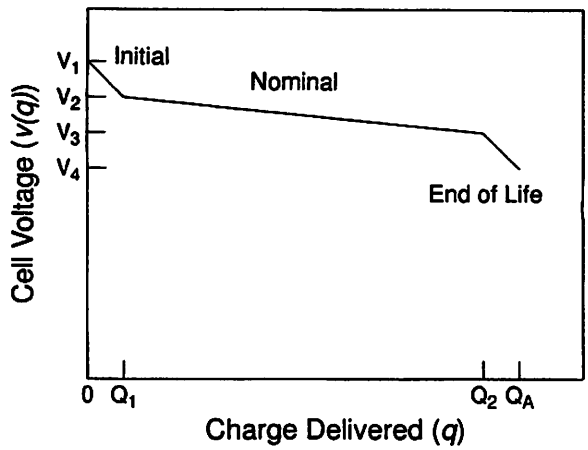


Figure 2: A piecewise linear model of a typical low-rate cell discharge characteristic.

with the initial condition:

$$q = 0, \quad t = 0, \tag{6}$$

yielding:

$$t_A = \int_0^{Q_A} \frac{dq}{i(q)}. \tag{7}$$

2.2 Models for Battery Loading Conditions

Figure 3 shows the three loads considered in this analysis, (a) a constant current load I, (b) a resistive load R, and (c) a constant power load P, each attached across the terminals of a cell whose discharge charactersitic $v(q)$ is described by Figure 2.

In Figure 3a, the current drawn from the battery is constant and equal to I. Thus, (7) yields:

$$t_A = \frac{Q_A}{I}. \tag{8}$$

For the resistive load of Figure 3b:

$$i(q) = \frac{v(q)}{R}, \tag{9}$$

and although integration of (7) provides a closed-form expression for t_A, it proves ungainly and provides little insight. However, if the simplifying assumption that the mean load current, averaged over the system run-time ($t \in [0, t_A]$) is equal

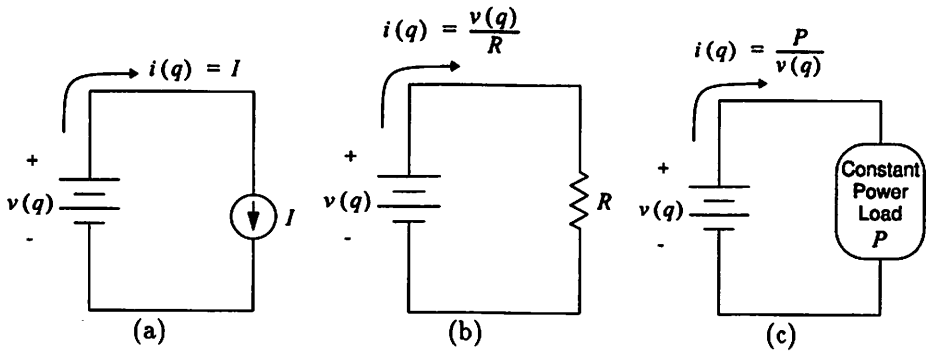


Figure 3: Battery loading conditions: (a) a constant current load I, (b) a resistive load R, (c) a constant power load P.

to the mean load current, averaged over the delivered charge ($q \in [0, Q_A]$):

$$\begin{aligned} \overline{i(t)} &= \overline{i(q)} \\ &= \frac{\overline{v(q)}}{R} \end{aligned} \tag{10}$$

is made, the expression for t_A is considerably more workable:

$$t_A = \frac{Q_A \cdot R}{\overline{v(q)}}. \tag{11}$$

Since the cell voltage $v(q)$ is relatively flat during the majority of the cell discharge, the approximation of (10) is valid for any of the discharge characteristics of Figure 1, introducing an error of less than 0.5%.

In Figure 3c, the load draws a constant power P from the cell, such that:

$$i(q) = \frac{P}{v(q)} \tag{12}$$

and:

$$t_A = \frac{E_A}{P} = \frac{Q_A \cdot \overline{v(q)}}{P}. \tag{13}$$

2.3 Case Study: An Analog Load with Supply-independent Biasing

Analog circuitry with ideal supply-independent biasing draws a quiescent current I, independent of the voltage across its terminals.

Run directly from cell: (8) gives the baseline system run-time t_{Ao}:

$$t_{Ao} = \frac{Q_A}{I}. \tag{14}$$

Run through a linear regulator: In the idealized case, the linear regulator has a dropout voltage of zero and a quiescent operating current which is negligible with respect to I (see Section 10.1). Thus, the supply may be regulated to the minimum voltage, $V_{min} \leq v(q)$, at which the load can operate, minimizing its power consumption, and the quiescent current of the regulator may be ignored. However, because the same current I drawn by the load flows through the regulator, the power which is conserved by running the load at V_{min} is dissipated in the regulator. (The dissipation in the regulator is $I \cdot [v(q) - V_{min}]$.) The battery still sources the current I, and:

$$\frac{t_A}{t_{Ao}} = 1. \tag{15}$$

System run-time is neither enhanced nor diminished.

Run through a switching regulator: If the output is regulated to any V_{min} through a switching regulator with efficiency η, the load consumes a constant and minimum power. The power drawn from the cell is constant and equal to:

$$P = \frac{P_{L-min}}{\eta} = \frac{I \cdot V_{min}}{\eta}. \tag{16}$$

Substituting (16) into (13), and normalizing with respect to t_{Ao} gives:

$$\frac{t_A}{t_{Ao}} = \frac{\eta \cdot E_A}{V_{min} \cdot Q_A} = \frac{\eta \cdot \overline{v(q)}}{V_{min}}. \tag{17}$$

2.4 Case Study: A Throughput-constrained Digital CMOS Load

A throughput-constrained digital CMOS circuit whose power consumption is dominated by its dynamic component, that is clocked at a frequency $f_{V_{min}}$ to meet throughput constraints at the minimum voltage V_{min}, and that has an effective switching capacitance C_{eff}, may be modelled by an equivalent resistance of value:

$$R_{eff} = \frac{1}{f_{V_{min}} \cdot C_{eff}}. \tag{18}$$

Run directly from cell: Substitution of (18) into (11) gives the baseline system run-time:

$$t_{Ao} = \frac{Q_A \cdot R_{eff}}{\overline{v(q)}}. \tag{19}$$

Run through a linear regulator: If the load is run from the minimum voltage V_{min} at which throughput constraints are met, it consumes a constant current:

$$I_{min} = V_{min}/R_{eff} \tag{20}$$

which is sourced through the regulator from the battery source. This current represents the minimum operating current of the load. Substitution of I_{min} in (20) for I in (8), and normalization of the result to t_{Ao} yields:

$$\frac{t_A}{t_{Ao}} = \frac{E_A}{V_{min} \cdot Q_A} = \frac{\overline{v(q)}}{V_{min}}. \tag{21}$$

Run through a switching regulator: At the minimum voltage V_{min}, the load consumes a constant power:

$$P = P_{L-min} = V_{min}^2/R_{eff} \tag{22}$$

which represents the minimum operating power of the load. The average power drawn from the cell through the switching regulator is:

$$P = \frac{P_{L-min}}{\eta} = \frac{V_{min}^2}{\eta \cdot R_{eff}} \tag{23}$$

and:

$$\frac{t_A}{t_{Ao}} = \frac{\eta \cdot E_A^2}{(V_{min} \cdot Q_A)^2} = \frac{\eta \cdot \overline{v(q)}^2}{V_{min}^2}. \tag{24}$$

2.5 Results

A factor that appears frequently in the above comparisons of system run-time is the ratio of the mean cell voltage (averaged over the delivered charge, q) to the minimum voltage required by the load. For convenience in summarizing the results, the symbol β is used for this ratio:

$$\beta \equiv \frac{\overline{v(q)}}{V_{min}}. \tag{25}$$

In terms of β, Table 1 gives the run-time enhancement factor, K, for a linear (constant-current) or digital CMOS (resistive) load, where K is the run-time relative to the baseline run-time when the load is run directly from the battery source,

$$K \equiv \frac{t_A}{t_{A_o}}. \tag{26}$$

Figure 4 shows the system run-time enhancement for NiCd, NiMH, and Li Ion cells loaded with analog and digital circuitry achieved by a linear regulator, and

Table 1: System Run-Time Enhancement.

Regulator type	Constant-current (e.g. analog) load	Resistive (e.g. digital) load
Linear	$K = 1$	$K = \beta$
Switching, efficiency η	$K = \eta\beta$	$K = \eta\beta^2$

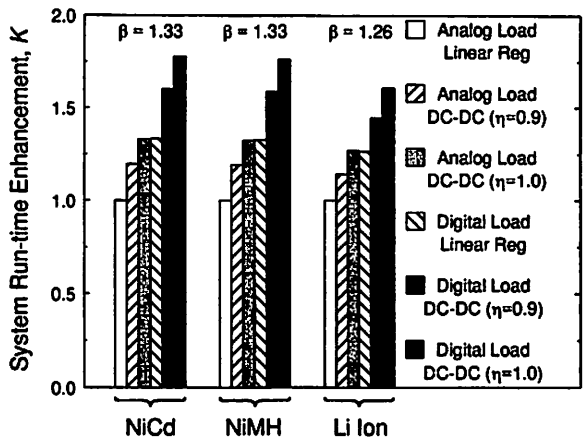


Figure 4: System run-times for analog and digital loads run from a linear regulator, and a 90% and 100% efficient DC-DC converter.

a 90% and 100% efficient DC-DC converter. Here, the output voltage of each converter is maintained at the end-of-life cell voltage.

The results shown in Table 1 can be used to predict the benefits of different regulation schemes for a variety of loads. A linear regulator produces no advantage in system run-time for a constant-current load (e.g. many analog circuits). It should only be used if a stabilized voltage improves the performance of the load circuitry. With a digital load, the linear regulator provides an improvement by the factor β. Regardless of the load type, a switching regulator results in a value of K which is that for a linear regulator, multiplied by an additional factor $\eta\beta$. As long as the efficiency of the regulator is high enough that $\eta\beta > 1$, the switching regulator will give a longer run-time than a linear regulator.

The benefits of a switching regulator are greatest where β is large; that is, where the minimum required load voltage is small compared to the average battery voltage. This makes intuitive sense, since an unnecessarily high voltage is wasteful of energy. With a load that is designed to run down to the end-of-life cell voltage, the factor β is only a function of the battery characteristic, and, for the discharge characteristics of Figure 1, is 1.33 for NiMH or NiCd cells, and 1.26 for Li Ion. Note, however, that for a load with a minimum operating voltage

below the end-of-life voltage of its battery source, β can be much higher. For example, consider the low-power multimedia chipset introduced in [5]. If this chipset, which can operate at a 1.1 V minimum supply voltage, were run from a Li Ion cell, β would be 3.27. In this system, even a very low efficiency switching regulator would be desirable—even with 31% efficiency, it would out-perform an ideal linear regulator. Efficiency is still important, however—in all cases, the run-time with a DC-DC converter is directly proportional to the efficiency of the converter. In this example, with 90% efficiency, as is readily achieved using the design techniques presented in Section 6, the system run-time would be 9.64 times longer than if the chipset were run directly from the Li Ion battery source.

2.6 Converter Size vs. Extra Battery Size

While DC-DC conversion can significantly improve system run-time, this same enhancement of run-time may also be achieved by simply increasing the capacity of the battery source. Thus, from a system design standpoint, it is important to compare the volume required for the converter to the volume that would be required for this additional battery capacity.

Suppose the run-time is enhanced by a factor K by the use of a DC-DC converter. The volume of the converter needed to achieve this enhancement, ΔS_{DC-DC}, may be estimated from the power it supplies, P_{L-min}, and its power density, $D_{P(DC-DC)}$:

$$\Delta S_{DC-DC} = P_{L-min}/D_{P(DC-DC)}. \tag{27}$$

To improve system run-time by the same factor K without using a converter, the battery capacity would need to be increased by the factor K. The resulting increase in battery volume is then

$$\Delta S_B = S_{B_0}(K-1), \tag{28}$$

where ΔS_B is the volume of the additional battery capacity, and S_{B_0} is the initial battery volume. The initial battery volume may be calculated from the energy it stores at full capacity, E_A, and its volumetric energy density, $D_{E(bat)}$:

$$S_{B_0} = E_A/D_{E(bat)}. \tag{29}$$

The volume of the DC-DC converter is related to the load power, as illustrated by (27), whereas the volume of the additional battery capacity is related to the integral of the load power—the total energy consumed by the load over the system run-time. These two quantities can only be compared by specifying the enhanced run-time, t_A. In the case that a DC-DC converter is used, the load on the battery is a constant power, P_{L-min}/η. Thus, $E_A = P_{L-min}t_A/\eta$. Substituting this expression into (29), and the result into (28), gives the additional

battery volume in terms of t_A and P_{L-min}:

$$\Delta S_B = \frac{t_A \cdot P_{L-min}}{D_{E(bat)}} \cdot \frac{(K-1)}{\eta}. \tag{30}$$

Comparing the additional volume needed in each case,

$$\frac{\Delta S_B}{\Delta S_{DC-DC}} = \frac{D_{P(DC-DC)} \cdot t_A}{D_{E(bat)}} \cdot \frac{(K-1)}{\eta}. \tag{31}$$

Conceptually, (31) compares the energy density of the battery ($D_{E(bat)}$) to the effective energy density of the converter—the factor $D_{P(DC-DC)}t_A$ gives the energy handled by the converter per volume, and the factor $(K-1)/\eta$ corrects this for the amount of energy savings the converter effects, relative to the amount of energy it handles. Although the position of η in (31) is at first counter-intuitive, recall that K is directly proportional to η; we may write $K = K_0\eta$. In terms of K_0 then,

$$\frac{\Delta S_B}{\Delta S_{DC-DC}} = \frac{D_{P(DC-DC)}}{D_{E(bat)}} \cdot t_A \cdot (K_0 - 1/\eta). \tag{32}$$

Since K_0 is equal to β or β^2 (see Table 1), the ratio, (32), is seen to increase with increasing efficiency, as expected.

Small Li Ion cells have an energy density up to 0.3 W-h/cm^3 [7]. Primarily because of packaging volume, smaller converters have somewhat lower power densities than standard commercial converters of 50-200 W, but ultra-low-power converters with power densities above 1 W/cm^3 can be achieved through the use of the techniques discussed in Section 5. Using these power and energy densities in conjuntion with (31), it is possible to evaluate the relative converter or additional battery volume required for an equal extension of system run-time.

For example, again consider the system introduced in the previous subsection. There, it was shown that a 90% efficient DC-DC converter with a regulated 1.1 V output can be used to enhance system run-time from a Li Ion source by a factor of $K = 9.64$. For an 8 h target run-time, the volume required by 8.64 times more Li Ion capacity is roughly 256 times greater than that required by the converter. If a shorter run-time is targeted, the additional battery volume needed to achieve the same percentage of enhancement is smaller, but, because its power handling requirements are unchanged, the volume of the DC-DC converter remains the same. Thus, for short run-times, adding battery capacity requires less volume than adding a DC-DC converter. However, based on the same factors of this example, for any run-time longer than two minutes, the additional battery volume is still greater than the volume of the converter.

It may be concluded that, with the exception of systems designed for very short run-times, enhancing system run-time by adding a DC-DC converter will typically involve only a small increase in volume, much smaller than the increase in battery volume that would be needed for the same increase in run-time.

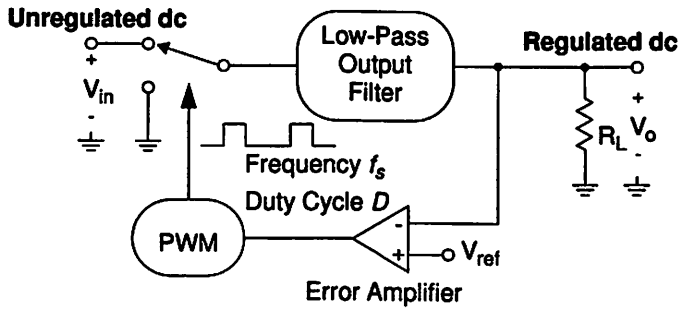


Figure 5: Block diagram of a pulse-width modulated (PWM) switching regulator.

3 Pulse-width Modulated DC-DC Converter Topologies

The switching regulator shown in Figure 5 converts an unregulated battery source voltage V_{in} to the desired regulated DC output voltage V_o. A single-throw, double-pole switch chops V_{in} producing a rectangular wave having an average voltage equal to the desired output voltage. A low-pass filter passes this DC voltage to the output while attenuating the AC ripple to an acceptable value. The output is regulated by comparing V_o to a supply- and temperature-independent reference voltage, V_{ref}, and adjusting the fraction of the cycle for which the switch is shorted to V_{in}. This pulse-width modulation (PWM) controls the average value of the chopped waveform, and thus stabilizes the output voltage against input, load, and temperature variations. Unlike a switched-capacitor converter (see Section 10), a switching regulator has an efficiency which approaches 100% as the components are made more ideal. In practice, efficiencies above 75% are typical, and efficiencies above 90% are attainable.

There are several simple alternative arrangements of the switching and filter components that can be used to produce an output voltage larger or smaller than the input voltage, with the same or opposite polarity. Some of these will be discussed below. However, many of the design issues are similar, so first one topology, the step-down (buck) converter, will be discussed in more detail.

3.1 Buck Converter

The power train of the low-output-voltage buck circuit, which can produce any arbitrary output voltage $0 \leq V_o \leq V_{in}$, is given in Figure 6. The basic operation is as follows: The power transistors (pass device M_p and rectifier M_n) chop the battery input voltage V_{in} to reduce the average voltage. This produces a square wave of duty cycle D and period $T_s = f_s^{-1}$ at the inverter output node, v_x. A typical periodic steady-state $v_x(t)$ waveform is shown in Figure 7. This chopped

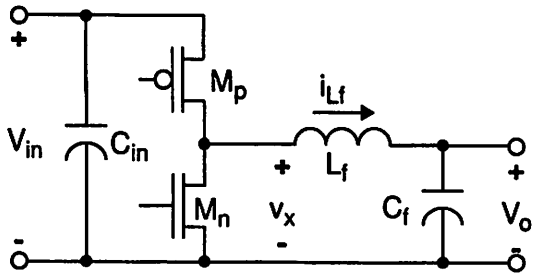


Figure 6: Low-output-voltage buck circuit.

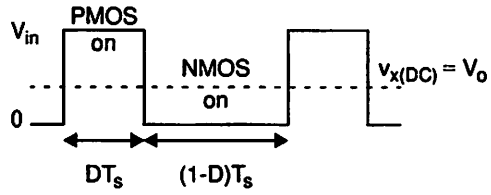


Figure 7: Nominal periodic steady-state $v_x(t)$ buck circuit waveform.

signal is filtered by the second-order low-pass output filter, L_f and C_f. In the ideal case, the DC output voltage is given by the product of the input voltage and the duty cycle:

$$V_o = V_{in} \cdot D \tag{33}$$

The switching pattern of M_n and M_p is pulse-width modulated, adjusting the duty cycle of the rectangular wave at v_x, and ultimately, the DC output voltage, to compensate for input and load variations. The pulse-width modulation is controlled by a negative feedback loop, shown in the block diagram of Figure 5, but omitted from Figure 6 for simplicity. Some detail on PWM design is included in Section 9.

3.1.1 Output Filter Design

In Figure 8, the rectangular wave of the inverter output node is applied to the second order low-pass output filter of the buck circuit (L_f and C_f), which passes the desired DC component of v_x while attenuating the AC component to an acceptable ripple value. Load R_L draws a DC current I_o from the output of the filter. Figure 9 shows the nominal steady-state $i_{L_f}(t)$ and $v_o(t)$ waveforms for a rectangular input $v_x(t)$.

In order to achieve the large attenuation needed in a practical power circuit, $L_f C_f \gg \omega_s^{-2}$, where $\omega_s = 2\pi f_s$, and f_s is the switching frequency of the converter. In this case, the filter components may be sized independently, using

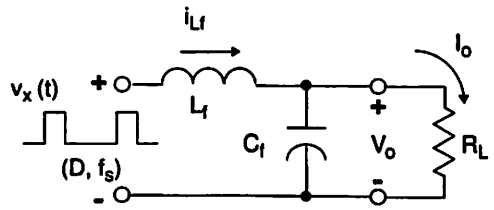


Figure 8: The output filter of the buck circuit (L_f and C_f) with load R_L.

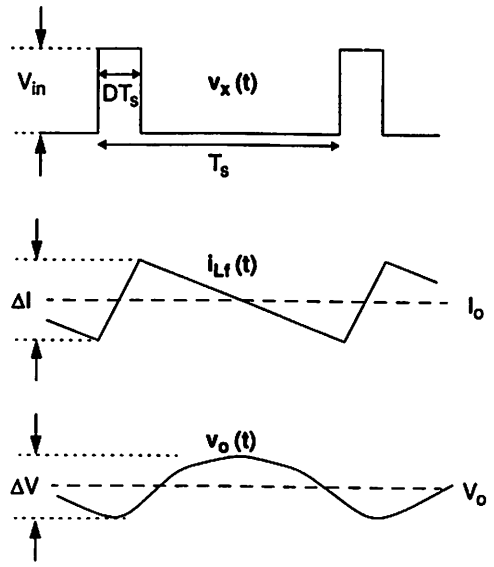


Figure 9: Nominal steady-state waveforms of the buck circuit output filter.

time domain analysis, rather than frequency domain analysis. Neglecting the effects of output voltage ripple ($v_{o-AC} \ll v_{x-AC}$), for a rectangular input with period T_s, the AC inductor current waveform is triangular with period T_s and peak-to-peak ripple ΔI symmetric about the average load current I_o. The peak-to-peak current ripple may be found by integrating the AC component of the $v_x(t)$ waveform over a fraction, D, of one cycle, yielding:

$$\Delta I = \frac{V_{in} \cdot D \cdot (1-D)}{L_f \cdot f_s} = \frac{V_o \cdot (1-D)}{L_f \cdot f_s}. \tag{34}$$

The output filter capacitor is selected to ensure that its impedance at the switching frequency, including its equivalent series resistance (ESR), is small relative to the load impedance. Thus, the AC component of the inductor current flows into the filter capacitor, rather than the load. For many capacitor tech-

nologies at frequencies above several hundred kilohertz, the resistive impedance dominates over the capacitive impedance. In high-current-ripple designs, a primary design goal is to minimize ESR to reduce both output voltage ripple and conduction loss (see below). For this reason, a high-Q capacitor technology, such as multilayer ceramic chip capacitors, is typically used, and even at high frequencies, ESR may be neglected in calculating output voltage ripple. Considering only capacitive impedance, the peak-to-peak output voltage ripple may be found through charge conservation. Assuming the AC inductor current flows only into the filter capacitor:

$$\Delta V = \frac{\Delta I}{8 \cdot C_f \cdot f_s} = \frac{V_o \cdot (1 - D)}{8 \cdot L_f \cdot C_f \cdot f_s^2}. \tag{35}$$

This output voltage ripple is symmetric about the desired DC output voltage V_o, and, for the $v_x(t)$ waveform shown in Figure 9, is piecewise quadratic with period T_s.

Equations (34) and (35) illustrate the two principle means of miniaturizing a DC-DC converter. First, it can be readily seen that the values of filter inductance and capacitance decrease with f_s^{-1}. Thus, a higher operating frequency typically results in a smaller converter. Second, because the requirement of interest is output voltage ripple, it is the $L_f C_f$ product, rather than the values of the individual components, that is important. Through choice of a higher current ripple, ΔI, a lower filter inductance solution may be obtained, often resulting in a smaller supply.

3.1.2 Buck Converter Efficiency

The power train of a low-output-voltage buck circuit, including parasitic capacitance C_x, stray inductance L_s, and drain-body diodes of the power transistors, is shown in Figure 10. Listed below are the chief sources of dissipation that cause the conversion efficiency of this circuit to be less than unity. In Section 6, methods which reduce these losses are described.

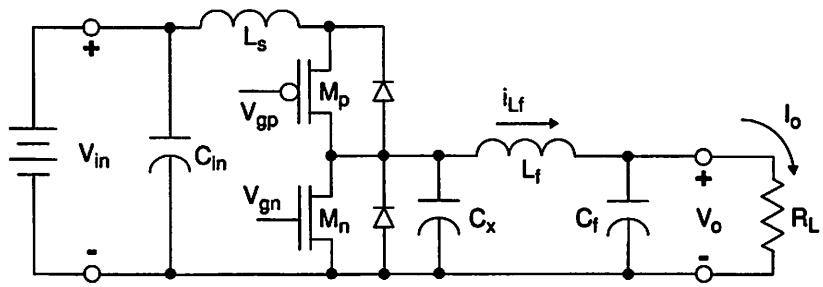


Figure 10: Low-output-voltage buck circuit.

Conduction Loss: Current flow through non-ideal power transistors, filter elements, and interconnections results in dissipation in each component:

$$P_q = i_{rms}^2 \cdot R, \tag{36}$$

where i_{rms} is the root mean squared current through the component, and R is the resistance of the component.

Gate-Drive Loss: Raising and lowering the gate of a power transistor each cycle dissipates an average power:

$$P_g = E_g \cdot f_s, \tag{37}$$

where E_g is directly proportional to the gate energy transferred per cycle (which can include some energy due to Miller effect), and includes dissipation in the drive circuitry (see Section 6.5.4).

Capacitive Switching Loss: In a hard-switched converter, MOSFET M_p charges parasitic capacitance C_x to V_{in} each cycle, dissipating an average power:

$$P_{C_x} = \frac{1}{2} \cdot C_x \cdot V_{in}^2 \cdot f_s, \tag{38}$$

where C_x includes reverse-biased drain-body junction diffusion capacitance C_{db} and some or all of the gate-drain overlap (Miller) capacitance C_{gd} of the power transistors, wiring capacitance from their interconnection, and stray capacitance associated with L_f. In ultra-low-power monolithic converters, C_x may be dominated by parasitics associated with the connection of an off-chip filter inductor, which include a bonding pad, bond wire, pin, and board interconnect capacitance. In circuit topologies which do not recover the energy stored on C_x each cycle through the inductor, the factor of 1/2 is removed from (38).

Short-Circuit Loss: A short-circuit path may exist temporarily between the input rails during transitions. To avoid potentially large short-circuit losses, it is necessary to provide dead-times in the conduction of the MOSFETs to ensure that the two devices never conduct simultaneously.

Body Diode Reverse Recovery: If the durations of the dead-times are too long, the body diode of the NMOS power transistor may be forced to pick up the inductor current for a fraction of each cycle. When the PMOS device is turned on, it must remove the excess minority carrier charge from the body diode, dissipating an energy bounded by:

$$E_{rr} = Q_{rr} \cdot V_{in}, \tag{39}$$

where Q_{rr} is the stored charge in the body diode.

Stray Inductive Switching Loss: Energy storage by the stray inductance L_s in the loop formed by the input decoupling capacitor C_{in} and the power transistors causes dissipation.

Quiescent Operating Power: The PWM and other control circuitry consume power. In low-power applications, this control power may contribute substantially to the total losses, even at full-load.

3.2 Other Toplogies

Two other basic configurations for PWM switching converters are the boost converter (Figure 11), and the buck-boost converter (Figure 13). All three basic topologies—buck, boost, and buck-boost—are similar in that they each have two complementary switches and one inductor. Their conversion ratios may all be adjusted by varying the duty cycle with frequency held constant. They can all be derived from the same basic switching cell [9].

The boost converter produces output voltages $V_o \geq V_{in}$. A typical steady-state $v_x(t)$ waveform is shown in Figure 12. In one portion of the cycle, $(1-D)$, the NMOS device is on, and the input voltage is applied across L_f, building up current and thus storing energy in the inductor. When the NMOS switch is turned off, the attempt to interrupt the current in the inductor causes the voltage at node v_x to rise rapidly. The PMOS device is turned on at this point, limiting the voltage produced by this inductive kick to the voltage on the output capacitor. (If the PMOS device were not turned on, its drain-body diode would short v_x to one diode drop above V_o.) During the fraction of the cycle, D, that the PMOS device conducts, some of the energy stored in the inductor is transferred to the output, along with additional energy flowing from the input. The cycle then repeats.

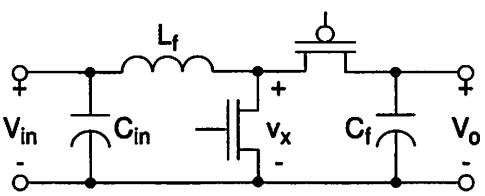


Figure 11: Low-voltage CMOS boost circuit.

The boost converter may be considered a variation of the buck converter, but with power flow from the lower voltage side to the higher voltage side. The voltage at node v_x is a rectangular wave whose DC component is equal to the input voltage. (It must be equal, as the average voltage across the inductor must be zero for periodic steady state.) Thus, the input and output voltages are related by

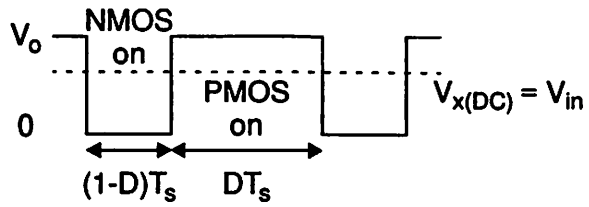


Figure 12: Nominal steady-state $v_x(t)$ boost circuit waveform.

$$V_{in} = V_o \cdot D, \tag{40}$$

the same relation as for the buck converter, but with the input and output terminals reversed.

The operation of the buck-boost converter (Figure 13) is similar to that of the buck converter, in that the cycle starts with the input voltage applied across the inductor, in this case through the PMOS device for a duration, DT_s. However, when the PMOS device is turned off, the voltage at v_x heads downward, and the circuit produces an output voltage polarity opposite to that of the input (Figure 14). The energy transferred to C_f during this portion, $(1 - D)$, of the cycle (while the NMOS device conducts) is only the energy stored in the inductor, with none coming directly from the input. Setting the average voltage across the inductor equal to zero allows the conversion ratio to be found:

$$V_o = V_{in} \cdot \frac{D}{1-D}. \tag{41}$$

Note that this allows input voltages of smaller or larger magnitude than the input, hence the name "buck-boost".

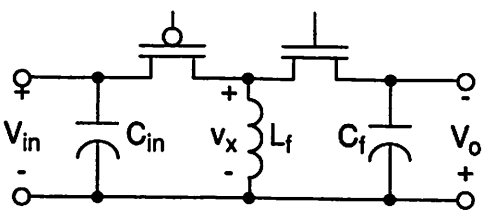


Figure 13: Low-voltage CMOS buck-boost circuit.

4 Power System Design Issues

In the design of a complete power system, the size and efficiency of different converters within the system may be traded, and the relative merits of different

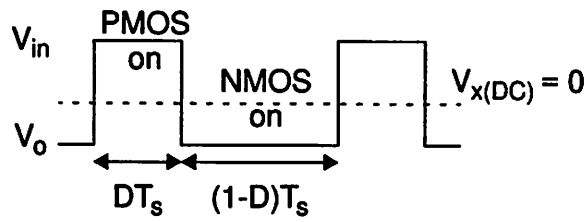


Figure 14: Nominal steady-state $v_x(t)$ buck-boost circuit waveform.

topologies may be considered in the selection of the battery source voltage. Furthermore, resources such as oscillators and reference voltages may be shared among components on the same die, and sub-system voltages may be utilized in the design of each individual converter. When such system-level optimizations are incorporated in the overall design, the resulting power system is likely to be far superior to one consisting of a number of DC-DC converters designed independently.

4.1 Converter Toplogy Selection

To minimize physical size and complexity, each converter topology may be chosen to minimize component count. The three basic topologies decribed above—buck, boost, and buck-boost—each require two switches, two capacitors, and one inductor—the minimum component count for a PWM DC-DC converter. However, they are a small subset of the many DC-DC converter topologies that have been proposed and that are used in practice. Other important classes of converter topologies include transformer-coupled circuits and soft-switching topologies, such as resonant converters. Although many of these topologies have important advantages in some applications, transformer coupling is usually unnecessary in portable systems (see below), and soft-switching can be achieved without the use of resonant techniques (Section 6.2). Thus the basic topologies are appropriate, perhaps optimal, for most portable applications. The reader is referred to [9], and the references contained therein, for more discussion of other topologies.

In buck and boost converters, a fraction of the energy on C_f is supplied directly from the input to the output, reducing the energy storage requirement of the inductor, and thus, its physical size. In a buck-boost converter, because none of the energy is transferred directly—it is transferred from the input into the inductor, and then in a separate portion of the cycle, from the inductor to the output, a larger inductor is typically needed in this circuit. Thus, the buck and boost topologies are generally preferred. Because of its more severe inductor requirements, a buck-boost topology should only be used for voltage polarity inversion, or in applications which require both up-conversion and down-conversion over the discharge of the battery source.

4.1.1 Transformer-Coupled Topologies

In discrete power conversion circuits, a transformer-coupled topology is often desirable to accomplish conversion over a wide voltage ratio, because the turns ratio in the transformer can produce most of the voltage ratio. This allows switching patterns similar to those in a 1:1 converter, minimizing inductor requirements (and relaxing the requirements for other components in a discrete implementation). However, in a highly-integrated converter, the size of the transformer would probably outweigh any size reductions that would result from decreased inductor requirements. Thus, transformer-coupled circuits are likely to be useful in portable systems only for special applications, and will not be discussed further in this document. Special applications that could indicate the use of a transformer-coupled circuit could include high voltage requirements (e.g., for a display or backlight) and isolation. The reader is referred to [9], and the references contained therein, for more details on these circuits.

4.2 Sharing Resources Between Converters

In general, as the size of a DC-DC converter is decreased through frequency scaling (see Section 5.1), its losses increase. In a complete power system consisting of a number of DC-DC converters, frequency scaling may be used such that the size and efficiency of different converters are traded, yielding the desired combination of small overall size and total losses. For example, the power supply with the highest-power requirement may be optimized for high efficiency and reasonable size (with an operating frequency in the hundreds of kHz), and all supplies with lower-power requirements may be optimized for small size and reasonable efficiency (with operating frequencies of 1 MHz and above).

Furthermore, resources may be shared among different converters, particularly among converters which are integrated on the same die. Oscillators and reference voltage generators are needed in the control loop of any PWM DC-DC converter. If these components are shared among several converters, the overall quiescent operating power and component count of the power system will be reduced.

Finally, lower sub-system voltages can be used in the design of each individual converter. In Section 6.5, it will be shown that as the power transistor gate-drive supply voltage, V_g is reduced, for $V_g \gg V_t$, total power transistor losses, if optimized, decrease roughly as $\sqrt{V_g}$. Thus, a low sub-system voltage may be utilized as the gate-drive supply for each DC-DC converter in the power system to reduce losses in each power train. A similar strategy may be used to minimize the power consumption of the control circuitry (see Section 9).

4.3 Effects of Conversion Ratio

The effect of conversion ratio on efficiency and component sizing can be an important factor in selecting the battery source voltage. While predetermined constraints may dictate the selection of battery voltage and converter output voltage and thus determine the required conversion ratio, in the design of a complete power system, there is often a choice of battery source voltage. In general, a conversion ratio as close to 1:1 as possible minimizes the inductor size. For example, in (34), it is shown that for a buck converter with a given output voltage, the required inductor value is proportional to the complement of the duty cycle, $(1 - D)$. Thus, as the conversion ratio approaches 1:1, D approaches one, and the value and physical size of the inductor approach zero. Similarly, the inductor requirement in a boost converter approaches zero as the conversion ratio approaches 1:1. In a buck-boost converter, a 1:1 ratio still minimizes the inductor requirement, but the requirement does not approach zero as the conversion ratio approaches 1:1.

Thus to minimize inductor size, the preferred battery voltage is as close as possible to the desired output voltage, consistent with the constraint that, with a buck converter, the end-of-life battery voltage must be above the required output voltage. (For a boost converter, the constraint would be that the maximum battery voltage must be below the required output voltage.)

Another important consideration for a CMOS converter implementation which includes complementary switches is that P-channel devices are inherently inferior to N-channel devices. On the basis of FET losses alone, it is desirable to choose a conversion ratio which ensures that current is carried by the NMOS device for a large fraction of the cycle. For example, consider the CMOS buck topology drawn in Figure 6. For a given output voltage and current, the losses in the power transistors are minimized if the NMOS device carries the inductor current for the majority of the cycle. This calls for a large conversion ratio, as far from 1:1 as possible. With a 5:1 conversion ratio, for example, the PMOS device will conduct for only 20% of the cycle, and its losses can be made small.

Thus, for conversion ratios near 1:1, it is desirable to reconfigure the buck topology as shown in Figure 15. In this circuit, the NMOS device functions as the pass device, and, for conversion ratios near 1:1, it will have the longer conduction interval. Similar reconfigurations of the boost and buck-boost topologies are possible to minimize losses at extreme duty cycles. Figure 16 plots filter inductance and FET losses versus conversion ratio for a buck circuit with fixed V_o.

In a system requiring many unique voltages for different sub-systems, the battery voltage should be selected as close as possible to the voltage at which the most power is required, minimizing the size and maximizing the efficiency of the converter supplying that voltage. The remaining converter topologies would then be chosen to accommodate that battery voltage.

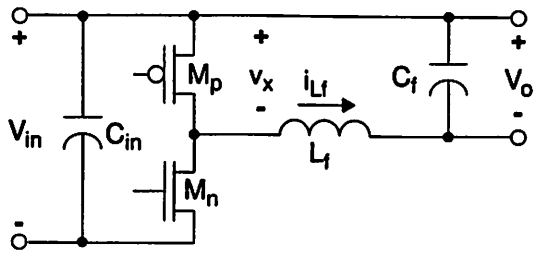


Figure 15: Alternative buck converter topology. For conversion ratios below 50%, M_n carries current for a larger fraction of the cycle than does M_p.

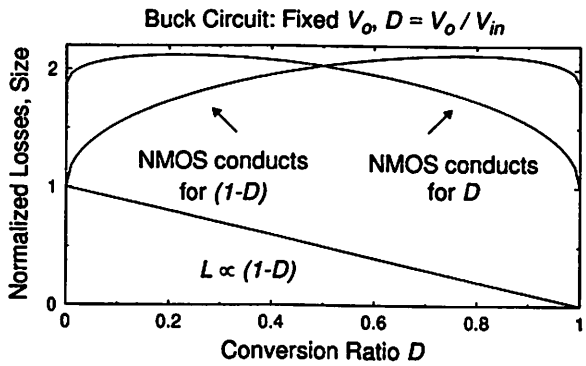


Figure 16: Filter inductance and FET losses vs. conversion ratio, D, for a buck circuit with fixed V_o.

5 Converter Miniaturization

Since the portability requirement places severe constraints on physical size and mass, the volume and mass of a converter can be a critical design consideration. This section introduces several design techniques that may be used to reduce the size of a PWM DC-DC converter.

5.1 High Frequency Operation

As indicated by (34) and (35), there are inherent size and cost advantages associated with higher frequency operation. The reactive filter components are likely to be the major contributors to the volume of a highly-integrated converter. For the same impedance, $j\omega_s L$ or $1/(j\omega_s C)$, a higher switching frequency, ω_s, enables the use of reactive components with smaller value and smaller physical size. Ideally, the size of these components will decrease with f_s^{-1}. However, as will be described in Section 6.4, if the operating frequency of

the circuit is increased, the sum of the losses in the power transistors and drive, if optimized, will increase roughly with $\sqrt{f_s}$. Thus, the general relationship between the size of a DC-DC converter and its losses is as illustrated in Figure 17. Here, operating frequency is used as a free-running variable, and the sum of the losses in the power transistors and drive is plotted against the volume of the converter.

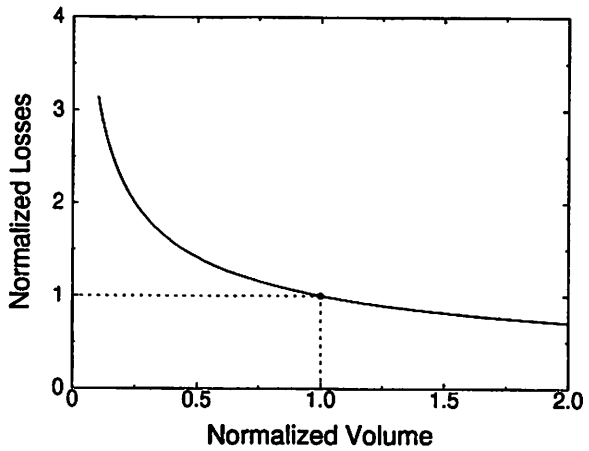


Figure 17: General trends in power transistor losses vs. the size of a DC-DC converter.

If the cost and volume of the converter are decreased, additional space and resources are left for a larger or better battery, compensating for lower conversion efficiency. The system requirements and battery characteristics will help to determine which point on this curve is optimal for a specific application.

Higher-frequency operation is limited mainly by two factors: frequency-dependent losses in the power train and controller, and diminishing returns in the miniaturization of the filter components. In Section 6, circuit-level optimizations are described which significantly reduce the frequency-dependent losses in the power train, yielding a class of miniature yet highly efficient converters that are well-suited for portable applications. Frequency limitations in inductive filter components will be addressed in Section 8.3.

5.2 High Current Ripple

Since the $L_f C_f$ product determines the output voltage ripple in (35), the relative size and cost of inductance versus capacitance should be considered in the selection of these components. As the size, cost, and commercial availability of low-voltage multilayer ceramic chip capacitors are often superior to those of inductors, it is desirable to accomplish the majority of the filtering with the

capacitor, allowing for the choice of a smaller-valued and smaller-sized inductor. This decision is restricted primarily by the increasing rms current in the inductor, which circulates throughout the power train, increasing conduction losses in proportion to $i^2_{L_f-rms}$.

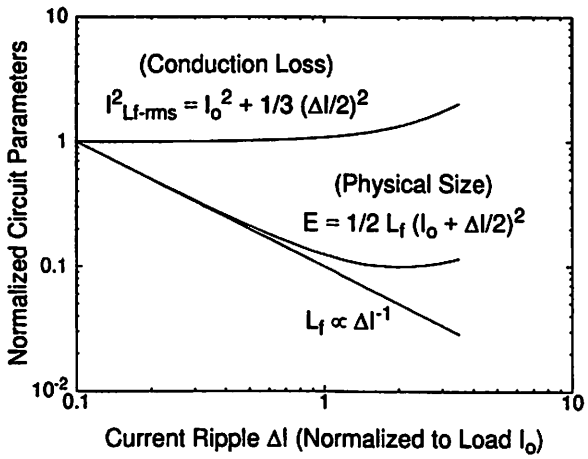


Figure 18: The effect of increased current ripple on the value of L_f, the physical size of L_f, and $i^2_{L_f-rms}$.

In Figure 18, the peak-to-peak inductor current ripple, ΔI, is varied, and its effects on three key circuit parameters are shown. As illustrated by (34), the value of filter inductance decreases with ΔI^{-1}. However, the physical size of L_f is roughly proportional to its peak energy storage, which in turn, is given by:

$$E_{L_f} = \frac{1}{2} L_f \left(I_o + \frac{\Delta I}{2} \right)^2 \tag{42}$$

and is minimized for $\Delta I = 2I_o$. If the inductor current is approximated as a triangular AC waveform with peak-to-peak ripple ΔI superimposed on a DC component, I_o, then the rms current is:

$$i_{L_f-rms} = \sqrt{I_o^2 + \frac{1}{3}\left(\frac{\Delta I}{2}\right)^2}. \tag{43}$$

Although the preferred value of ΔI will depend slightly on the trade-off between size and loss in a particular application, it can be concluded that a peak-to-peak current ripple in the range $I_o < \Delta I < 2I_o$ is optimal for many applications. For $\Delta I < I_o$, the decrease in rms current due to ripple, and the resulting decrease in loss, are insignificant. There is no obvious benefit for $\Delta I > 2I_o$, but this is advantageous for one mode of operation (see Section 6.2).

5.3 High Integration

A completely monolithic supply (active and passive elements) would meet the severe size and weight restrictions of a hand-held device. Because most portable applications call for low-voltage power transistors, their integration in a standard logic process is tractable. However, existing monolithic magnetics technology cannot provide inductors of suitable value and quality for efficient power conversion [10]. Emerging magnetics technology may allow completely monolithic supplies (see Section 8), but currently, magnetics, capacitors, and silicon circuitry are fabricated separately and assembled at the board level or in a multi-chip module (MCM). The extent of integration is the use of a monolithic silicon circuit, including all power transistors with their drive, and all control circuitry.

Such a highly-integrated solution not only results in a more compact design, it gives the designer more latitude in physical design and device sizing, allowing application-specific optimizations which are likely to yield a more efficient converter. In addition, parasitics from both the active devices and interconnect may be orders of magnitude lower on an IC than on a printed circuit board. Many of the frequency dependent losses in a power circuit increase in direct proportion to the energy storage of these parasitics; thus, integration enables higher efficiency at high operating frequencies than that obtained by a board-level solution.

6 Circuit Optimizations for High Efficiency

The chief mechanisms of dissipation in a low-output-voltage CMOS buck converter have been summarized in Section 3.1.2. In this section, design techniques to eliminate, minimize, or reduce the dissipation due to these mechanisms are described. While the following discussion is sometimes specific to the buck circuit, all of the techniques presented here can be applied to maximize the efficiency of boost and buck-boost type converters, each of which is typically required in the power distribution scheme of a battery-operated system.

6.1 Synchronous Rectification

The focus of this document is low-voltage CMOS PWM converters, in which the switching elements, modelled by the single-throw double-pole switch in the block diagram of Figure 5, are implemented by complementary MOSFETS. The more conventional implementation consists of one controlled switch and one uncontrolled switch (a diode). The pure CMOS implementation allows an important advantage.

Consider the conventional buck circuit of Figure 19. Even if all other losses in the circuit are made negligible, the maximum efficiency is limited by the forward bias diode voltage, V_{diode}. Since the diode conducts for a fraction $(1-D)$ of the switching period, the maximum efficiency this circuit can obtain is given by:

$$\eta_{max} = \frac{V_o}{V_o + (1-D) \cdot V_{diode}}. \tag{44}$$

For example, consider a conventional buck circuit used to generate an output voltage of 1.5 V from a single lithium ion cell. Even using the best low-voltage Shottky diode with a forward drop of 0.3 V, at the nominal cell voltage of V_{in} = 3.6 V, η_{max} is lower than 90%. With a silicon bipolar diode, V_{diode} = 0.7 V, and η_{max} = 0.79.

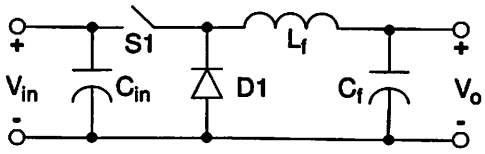


Figure 19: Conventional buck circuit with pass device $S1$ and diode.

If the diode in Figure 19 is replaced by an NMOS device which is gated when the diode would have conducted (M_n in Figure 10), the forward drop can be made arbitrarily small by making the device sufficiently large. In this way, the NMOS device, used as a synchronous rectifier, can perform the same function as the diode more efficiently. Assuming all other losses, including the gate-drive for the synchronous rectifier, are still negligible, the maximum efficiency of the low-voltage buck converter approaches unity.

6.1.1 Synchronous Rectifier Control

Although the synchronous rectifier may reduce conduction loss at low output voltage levels, it comes at the expense of an additional gate-drive signal and its associated loss. In addition, as mentioned in Section 3.1.2, without proper control of the rectifier, a short-circuit path may exist temporarily between the input rails during transients. In the rectifier control scheme described in Section 6.3, the dead-times, which ensure that M_p and M_n never conduct simultaneously, are adapted in a negative feedback loop to achieve nearly ideal zero-voltage switched turn-on transitions of both power MOSFETs (see below).

6.2 Zero-Voltage Switching

When the low-voltage buck circuit of Figure 10 is hard-switched, it dissipates power in proportion to $C_x V_{in}^2 f_s$ as a result of the step charging of parasitic capacitance C_x through a resistive path (M_p). In addition, it is likely to exhibit either substantial short-circuit loss (if no dead-time is provided), or reverse recovery loss (if a dead-time is provided). In a soft-switched circuit, the filter inductor is used as a current source to charge and discharge this capacitance in an ideally lossless manner, allowing additional capacitance to be shunted across

C_x, slowing the inverter output node transitions. In this way, appropriate dead-times may be set such that the power transistors are switched with $v_{ds} = 0$, eliminating all associated switching loss.

Figure 10 and Figure 20 show the low-voltage buck circuit and associated periodic steady-state waveforms for ideal zero-voltage switching operation. The soft-switching behavior is similar to that described in [11] and by other authors.

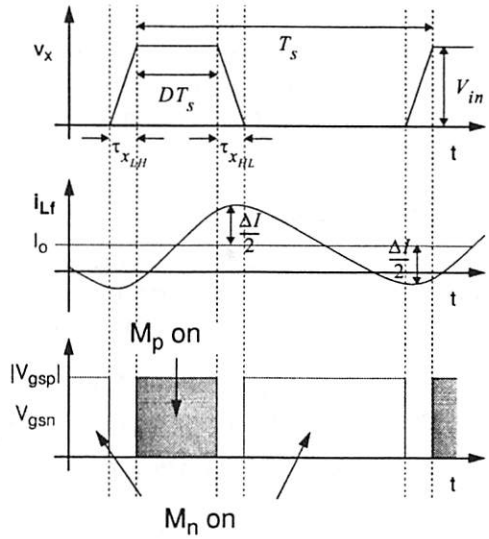


Figure 20: Nominal periodic steady-state ZVS waveforms.

Assume that at a given time (the origin in Figure 20), the rectifier (M_n) is on, shorting the inverter output node to ground. Since by design, the output is DC and greater than zero, a constant negative potential is applied across L_f, and i_{L_f} is linearly decreasing. If the value of filter inductance is small enough, the current ripple exceeds the average load ($\Delta I > 2I_o$), and i_{L_f} ripples below zero. As illustrated in Section 5.2, for such a value of current ripple, the physical size of the inductor is close to minimum.

If the rectifier is turned off after the current reverses (and the PMOS device, M_p, remains off), L_f acts approximately as a current source, charging the inverter output node. To achieve a lossless low-to-high transition at the inverter output node, the PMOS device is turned on when $v_x = V_{in}$. In this scheme, a pass device gate transition occurs exactly when $v_{ds_p} = 0$.

With the PMOS device on, the inverter output node is shorted to V_{in}. Thus, a constant positive voltage is applied across L_f, and i_{L_f} linearly increases, until the high-to-low transition at v_x is initiated by turning M_p off. As indicated by Figure 20, at this time, the sign of current i_{L_f} is positive. Again, L_f acts as a current source, this time discharging C_x. If the NMOS device is turned on with

$v_x = 0$, a lossless high-to-low transition of the inverter output node is achieved, and M_n is switched at $v_{ds_n} = 0$.

In this scheme, a form of soft-switching, the filter inductor is used to charge and discharge all capacitance at the inverter output node (and supply all Miller charge) in a lossless manner, allowing the addition of a shunt capacitor at v_x to slow these transitions. Since the power transistors are switched at zero drain-source potential, this technique is known as zero-voltage switching (ZVS), and essentially eliminates capacitive switching loss. Furthermore, because the inductor current in a ZVS circuit reverses, if the body diode conducts for a portion of the cycle, it turns off through a short circuit (rather than through a potential change of V_{in}), nearly eliminating the dissipation associated with reverse recovery, a factor which might otherwise dominate switching loss, particularly in low-voltage converters.

6.2.1 Design of a ZVS Buck Circuit

As discussed in Section 3.1.1, the inductor current waveform in a buck circuit is assumed triangular with maximum and minimum values $I_o + (\Delta I)/2$ and $I_o - (\Delta I)/2$ which are relatively constant over the entire dead-time. Under ZVS operation, $\Delta I > 2I_o$, allowing L_f to charge and discharge the inverter output node between $v_x = 0$ and $v_x = V_{in}$. The ratio of these 0-100% soft-switched transition times is given by the ratio of the magnitude of the currents available for each commutation:

$$\frac{\tau_{x_{LH}}}{\tau_{x_{HL}}} = \frac{(\Delta I)/2 + I_o}{(\Delta I)/2 - I_o} \tag{45}$$

and approaches unity for large inductor current ripple. Here, τ_x indicates a soft-switched inverter output node transition interval, with subscripts LH and HL denoting low-to-high and high-to-low transitions, respectively. For a given ripple ΔI, the maximum asymmetry in transition times occurs at full load.

Using (45), the inductor current ripple, ΔI, is chosen to limit the maximum asymmetry in the durations of the soft-switched transitions to a reasonable value. From this value of ΔI, L_f is selected according to (34). Given specifications on the maximum tolerable output voltage ripple, ΔV, the value of C_f is then chosen using (35).

To slow the soft-switched transitions to durations for which dead-times may be programmed or adjusted, extra capacitance is added at the inverter output node. The total capacitance required to achieve a given low-to-high transition time is approximately equal to

$$C_x \approx \frac{\tau_{x_{LH}} \cdot (\Delta I/2 - I_o)}{V_{in}}. \tag{46}$$

6.3 Adaptive Dead-Time Control

To ensure ideal ZVS of the power transistors, the periods when neither conducts (the dead-times), τ_D, must exactly equal the inverter output node transition times:

$$\begin{aligned} \tau_{D_{LH}} &= \tau_{x_{LH}} \\ \tau_{D_{HL}} &= \tau_{x_{HL}}. \end{aligned} \tag{47}$$

In practice, it is difficult to maintain these relationships. As indicated by Figure 20, the inductor current ripple is symmetric about the average load current. As the average load varies, the DC component of the i_{L_f} waveform is shifted, and the current available for commutating the inverter output node is modified. Thus, the inverter output node transition times are load dependent.

In one approach to soft-switching, a value of average load may be assumed, yielding estimates of the inverter output node transition times. Fixed dead-times are based on these estimates. In this way, losses are reduced, yet perhaps not to negligible levels.

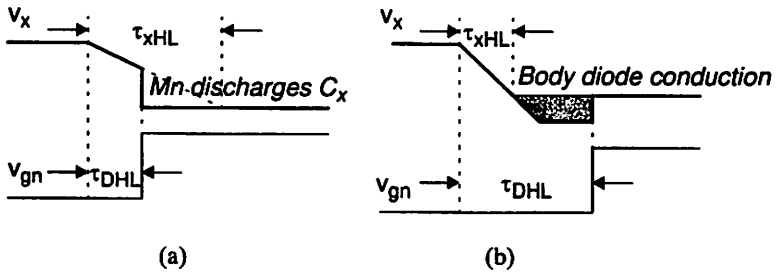


Figure 21: Non-ideal ZVS and its impact on conversion efficiency: (a) The dead-time is too short. (b) The dead-time is too long.

In portable applications where battery capacity is at a premium, this approach to soft-switching may not be adequate. To illustrate the potential hazards of fixed dead-time operation, Figure 21 shows the impact of non-ideal ZVS on conversion efficiency through reference to a high-to-low transition at the inverter output node. In Figure 21a, the dead-time is too short, causing the NMOS device to turn on at $v_{ds_n} > 0$, partially discharging C_x through a resistive path and introducing losses. Since, as indicated by (46), shunt capacitance with a value much larger than the intrinsic parasitics is typically added to slow the soft-switched transitions in a ZVS circuit, this loss may be substantial. In Figure 21b, the dead-time is too long, and the inverter output node continues to fall below zero until the drain-body junction of M_n becomes forward biased. In low-voltage applications, the forward-bias body diode voltage is a significant fraction of the output voltage; thus, body diode conduction must be avoided

for efficient operation. When the rectifier (M_n) turns on, it removes the excess minority carrier charge from the body diode and charges the inverter output node back to ground, dissipating additional energy.

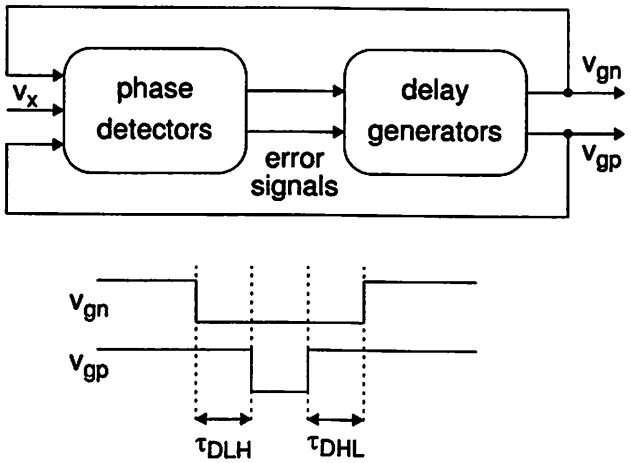


Figure 22: A conceptual representation of a dead-time adaptation scheme.

To provide effective ZVS over a wide range of loads, an adaptive dead-time control scheme for a 1 MHz ZVS buck circuit has been outlined in [12]. Figure 22 shows a block diagram of the approach. A phase detector updates an error signal based on the relative timing of v_x and the gate-drive signals of the power transistors. A delay generator adjusts the dead-times based on these error signals. Using this technique, effective ZVS is ensured over a wide range of operating conditions and process variations.

Figure 23 shows a circuit implementation of a $\tau_{D_{HL}}$ adaptation scheme, which is similar in principle to a delay-locked loop. The phase detector consists of two SR flip-flops, and controls the complementary switches of a charge pump. An error voltage proportional to the difference between the high-to-low soft-switched inverter output node transition time and its corresponding dead-time is generated on integrating capacitor, C_I. This error voltage is sampled and held at the switching frequency of the converter, such that:

$$v_\epsilon(nT_s) \approx v_\epsilon(nT_s - T_s) + I\left[\tau_{x_{HL}}(nT_s) - \tau_{D_{HL}}(nT_s)\right]. \qquad (48)$$

The delay generator, which is implemented by a V/I converter and a monostable multi-vibrator, updates the dead-time on a cycle-by-cycle basis. For sufficiently high op-amp gain:

$$i_{control}(nT_s) \approx \frac{V_{in}(nT_s) - v_\epsilon(nT_s)}{R}, \qquad (49)$$

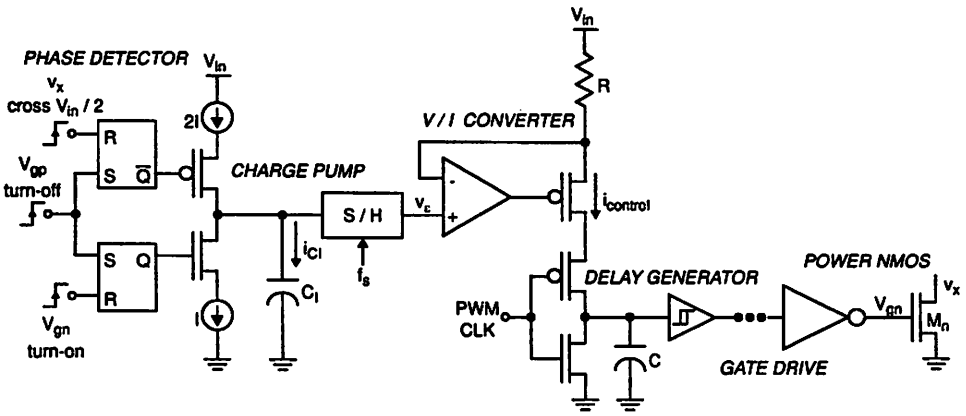


Figure 23: Rectifier turn-on delay adjustment loop.

and, assuming the dead-time is large compared to a gate delay,

$$\tau_{D_{HL}}(nT_s) \approx \frac{C \cdot V_{M_+}}{i_{control}(nT_s - T_s)}, \tag{50}$$

where V_{M_+} is the low-to-high switching threshold of the schmitt trigger.

In periodic steady-state, the error voltage, and thus the gate timing errors, are forced to zero, nulling propagation delays in the control and drive circuitry. Figure 24 shows the periodic steady-state waveforms associated with an ideal ZVS rectifier turn-on.

A similar loop is used to adjust the dead-time between the turn-off of M_n and the turn-on of M_p, $\tau_{D_{HL}}$.

6.4 Power Transistor Sizing

Through use of ZVS with adaptive dead-time control, switching loss is essentially eliminated. If the filter components in the buck circuit of Figure 10 are ideal, and series resistance and stray inductance in the power train are made negligible, the fundamental mechanisms of power dissipation will include on-state conduction loss and gate-drive loss in the power transistors. When sizing a MOSFET for a particular power application, the principal objective is to minimize the sum of the dissipation due to these mechanisms. This minimization is performed at the operating point where high efficiency is most critical: Usually at full load, at high temperature, and in portable applications, at the nominal battery source voltage.

During their conduction intervals, the power transistors operate exclusively in the triode region, where $r_{ds} = R_o \cdot W^{-1}$ (the channel resistance is inversely proportional to gate-width with constant of proportionality R_o). Thus, at a

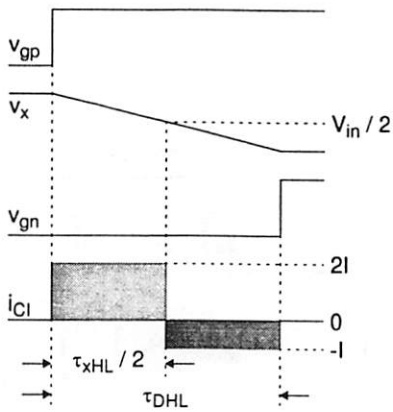


Figure 24: Ideal steady-state waveforms for the $\tau_{D_{HL}}$ adjustment loop.

given operating point, the on-state conduction loss in a FET is given by:

$$P_q = \frac{i_{ds-rms}^2 \cdot R_o}{W}. \tag{51}$$

Since the device parasitics generally increase linearly with increasing gate-width, the gate-drive loss can be expressed as a linear function of gate-width W:

$$P_g = E_{go} \cdot f_s \cdot W, \tag{52}$$

where E_{go} is the total gate-drive energy consumed in a single off-to-on-to-off gate transition cycle (see Section 6.5.4 for more detail) and f_s is the switching frequency of the converter. In a ZVS circuit, the filter inductor supplies all of the Miller charge, so E_{go} contains no dissipation due to Miller effect.

Using an algabraic minimization at the most critical operating point, the optimal gate-width of the power transistor,

$$W_{opt} = \sqrt{\frac{i_{ds-rms}^2 \cdot R_o}{E_{go} \cdot f_s}}, \tag{53}$$

is found to balance on-state conduction and gate-drive losses, where

$$P_{q-opt} = P_{g-opt} = \sqrt{i_{ds-rms}^2 \cdot R_o \cdot E_{go} \cdot f_s} \tag{54}$$

and $P_t = P_q + P_g$ is at its minimum value, P_{t-min}. Figure 25 illustrates normalized power transistor losses as a function of gate-width.

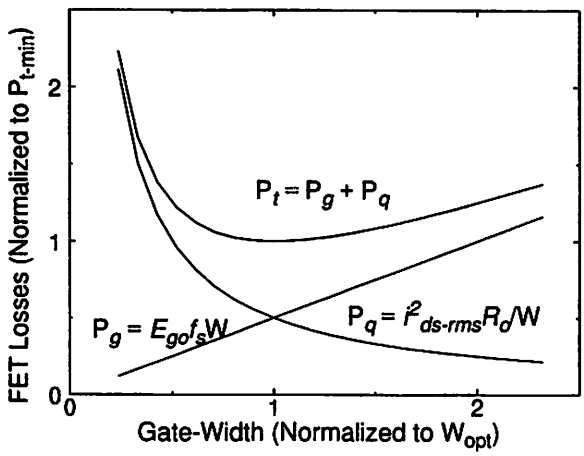


Figure 25: Power transistor losses vs. gate-width.

6.5 Reduced-Swing Gate-Drive

To ensure that the duration of the low-to-high soft-switched transition is kept reasonably short in a ZVS buck circuit, the inductor current ripple must be made substantial. This gives rise to large circulating currents in the power train, and therefore, when the power transistors are sized according to (53), increased gate-drive losses. Since gate-drive losses increase in direct proportion with f_s, this proves to be the limiting factor to higher-frequency operation of soft-switched converters. To reduce gate-drive losses, a number of resonant gate-drives have been proposed [13, 14, 15]. While several such techniques have demonstrated the ability to recover a significant fraction of the gate energy at lower frequencies, due to the resistance of the polysilicon gate of a power transistor, none are likely to be as successful in the 1 MHz frequency range. Furthermore, each requires additional reactive components and may therefore be impractical for portable applications.

Rather than attempting to recover gate energy in a resonant circuit, another approach to reducing gate-drive dissipation is to reduce the gate energy consumed per cycle. By decreasing the gate-source voltage swing between off-state ($V_{GS} = 0$) and on-state conduction ($V_{GS} = V_g$), for $V_g \gg V_t$, where V_t is the device threshold voltage, gate energy may be quadratically reduced. This is an attractive alternative in portable systems where a number of low-voltage supplies are typically available for the gate-drive. However, because the channel resistance of the device increases with $(V_g - V_t)^{-1}$, gate-swing cannot be arbitrarily reduced, implying the existance of an optimum V_g.

6.5.1 Zero-Order Analysis

If the gate capacitance of the power MOSFET is assumed linear over the voltage range $0 \leq v_g \leq V_g$ (which holds for $V_g \gg V_t$), the gate energy dissipation in a single off-to-on-to-off gate transition cycle is given by:

$$E_g = C_g V_g^2. \tag{55}$$

Since, in a ZVS circuit, the power transistors conduct exclusively in the triode region, where:

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \approx \mu C_{ox} \frac{W}{L} (V_g - V_t) \tag{56}$$

for $V_{DS} \ll V_g - V_t$, and the device channel resistance is given by:

$$R_{DS} = \frac{1}{g_{ds}}, \tag{57}$$

in the triode region, R_o is inversely proportional to $(V_g - V_t)$.

In the previous subsection, it was shown that in a ZVS power circuit, if a power transistor is sized according to (53), its total dissipation is minimized, and that this minimum dissipation is related to the square root of the product of the gate energy and the device channel resistance:

$$P_{t-min} \propto \sqrt{R_o \cdot E_{go}} \propto \frac{V_g}{\sqrt{(V_g - V_t)}}. \tag{58}$$

Minimizing this expression with respect to V_g, the optimum gate-swing which minimizes total dissipation in a power transitor is:

$$V_g = 2V_t. \tag{59}$$

Figure 26 shows the merits and limitations of a reduced-swing gate-drive. While the total dissipation of a power transistor may be reduced by lowering V_g (for $V_g > 2V_t$) and appropriately scaling its gate-width, the optimum gate-width which minimizes dissipation increases rapidly with decreasing V_g.

6.5.2 First-Order Analysis

If the inherent non-linearity of the gate capacitance of a MOSFET (shown in Figure 27) is considered in the analysis, the optimum gate-swing is technology-dependent. For $V_g < V_t$, the channel of the device is not enhanced, and the incremental gate capacitance may, to the first order [8], be approximated by the gate-source and gate-drain overlap capacitances:

$$C_g = \frac{dQ_g}{dv_g} \approx 2WL_D C_{ox}, \ (V_g < V_t), \tag{60}$$

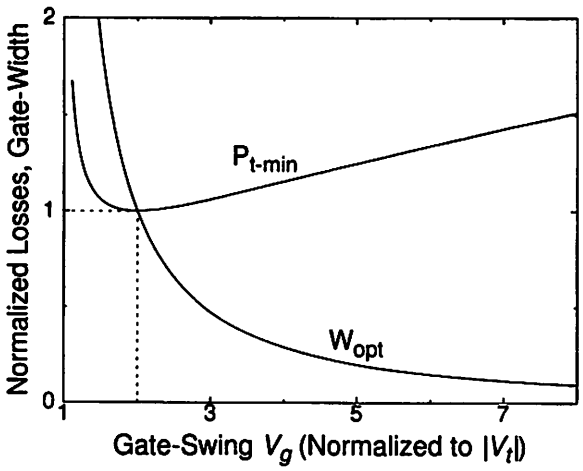


Figure 26: The optimal gate-width and minimum total dissipation for a power MOSFET vs. gate-swing in a ZVS topology.

where L_D is the lateral diffusion in the drain and source areas, and $C_{ox} = \epsilon_{ox}/t_{ox}$ is the gate oxide capacitance per unit area. For $V_g > 2V_t$, the channel is enhanced, and because in any practical power circuit, $V_{DS-on} \ll (V_{GS} - V_t)$, the power MOSFET operates in the triode region, the channel is assumed uniform, and:

$$C_g = \frac{dQ_g}{dv_g} \approx WLC_{ox}, \ (V_g \geq V_t). \tag{61}$$

Here, L is the drawn channel length, and is equal to the sum of the effective channel length and the lateral diffusion in both the source and drain diffusion areas (see Figure 28):

$$L = L_{eff} + 2L_D. \tag{62}$$

Note that in a ZVS circuit, the Miller charge is supplied by the filter inductor through the drain, not through the gate-drive. Thus, the effective gate capacitance does not include any Miller effect.

The gate-drive dissipation for a single off-to-on-to-off gate transition cycle, E_g, is:

$$E_g = V_g \cdot \Delta Q_g, \tag{63}$$

where V_g is the potential of the gate-drive supply voltage, and ΔQ_g is the change in charge stored on the gate, given by:

$$\begin{aligned} \Delta Q_g &= \int_0^t i_g dt' \\ &= \int_0^t \frac{C_g \cdot dv_g'}{dt'} dt' \end{aligned}$$

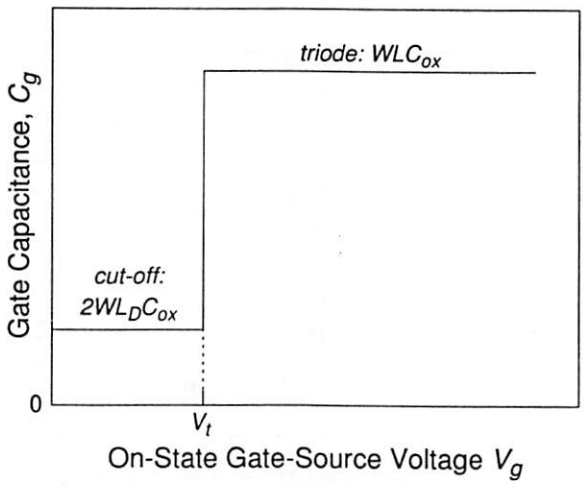
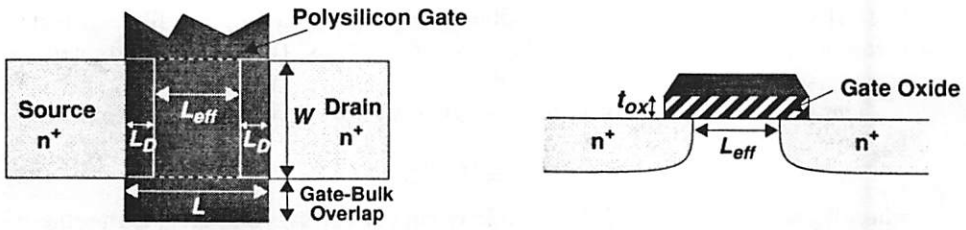


Figure 27: A first-order gate capacitance model to a power MOSFET in a ZVS application.

$$\begin{aligned} &= \int_0^{V_g} C_g dv_g' \\ &\approx \int_0^{V_t} 2WL_D C_{ox} dvg' + \int_{V_t}^{V_g} WLC_{ox} dvg' \\ &= 2WL_D C_{ox} V_t + WLC_{ox}(V_g - V_t). \end{aligned} \tag{64}$$

Thus, neglecting dissipation due to the inverter chain, the total gate energy dissipation per cycle is:

$$E_g = WLC_{ox}V_g^2 - WL_{eff}C_{ox}V_g V_t. \tag{65}$$



(a) (b)

Figure 28: An illustration of the effect of lateral diffusion, L_D, on the effective channel length, L_{eff}, of a MOSFET: (a) Top view. (b) Cross-section.

Substituting (65) into the expression for P_{t-min}, and minimizing this total dissipation with respect to V_g, the optimum gate-drive voltage is:

$$V_{g-opt} = V_t \left(1 + \sqrt{\frac{2L_D}{L}}\right), \tag{66}$$

which is technology dependent, and less than $2V_t$. For a standard 1.2 μm CMOS process in which $L_D \approx 0.15$ μm, (66) yields $V_{g-opt} = 1.5V_t$, or about 1.2 V for an n-channel power MOSFET.

In practice, however, ΔQ_g contains a voltage-dependent component due to the CMOS gate-drive buffering. Below, it will be shown that as V_g is decreased below $2V_t$, this component begins to dominate the overall gate-drive dissipation, such that

$$V_{g-opt} \approx 2V_t. \tag{67}$$

While (67) is useful for first-order design centering, iteration with a circuit simulator is necessary to find a true "optimum" V_g.

6.5.3 Scaling V_t

To further reduce the total dissipation of a power MOSFET with a given gate voltage swing, the off-state voltage can be made greater than zero (Figure 29a) to increase the gate overdrive, reducing the device channel resistance. This scheme is equivalent to that shown in Figure 29b, where $V_{GS} = 0$ in the off-state, and the device threshold voltage, $V_t' < V_t$, is scaled, while all other parameters are held constant, if:

$$V_t' = V_t - V_{GS(off)}. \tag{68}$$

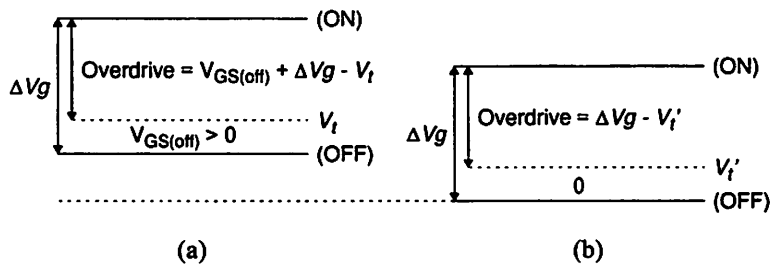


Figure 29: Two equivalent schemes to further reduce total power transistor losses: (a) The gate-source voltage is not brought to zero. (b) Lower V_t.

Threshold voltage scaling is limited primarily by subthreshold current conduction in the power MOSFETs, which increases exponentially with decreasing V_t, and with increasing temperature. For a combination of sufficiently low V_t and/or sufficiently high temperature, subthreshold leakage can result in significant static power dissipation in the power train of the converter. Figure 30

shows the inherent compromise associated with V_t scaling. Here, using the simple zero-order model for gate energy consumption and the model for subthreshold current conduction presented in [16], the optimal gate-width and minimum total dissipation of an NMOS power transistor in a 1.2 μm CMOS technology is plotted versus its threshold voltage, V_t, at room temperature and with all other application- and technology-related parameters held constant. The gate-swing has been optimized for minimum dissipation ($V_g = 2V_t$), and subthreshold conduction has been considered in the selection of optimum gate-width. For $V_t > 0.4$ V, leakage power dissipation (at $V_{in} = 6$ V) is negligible compared to the gate-drive power (at $f_s = 1$ MHz), and as W_{opt} increases with $1/\sqrt{V_t}$, P_{t-min} decreases with $\sqrt{V_t}$. As the threshold voltage is dropped below 0.4 V, leakage power becomes substantial, causing an exponential decrease in W_{opt} and increase in P_{t-min} with decreasing V_t. At $T = 100°$ C, the "optimal" V_t is close to 0.5 V.

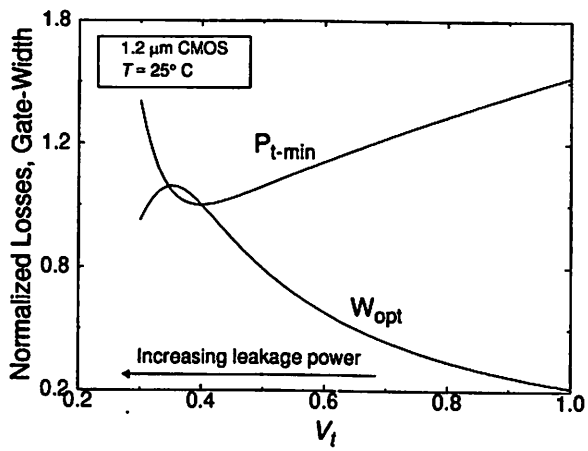


Figure 30: The optimal gate-width and minimum total dissipation, including static power dissipation due to subthreshold conduction, for a power n-channel MOSFET vs. V_t in a 1 MHz ZVS buck circuit.

6.5.4 CMOS Gate-Drive Design

In CMOS circuits, a power transistor is conventionally driven by a chain of N inverters which are scaled with a constant tapering factor, u, such that

$$u^N = \frac{C_g}{C_i}. \tag{69}$$

Here, C_g is the gate capacitance of the power transistor and C_i is the input capacitance of the first buffering stage. This scheme, depicted in Figure 31,

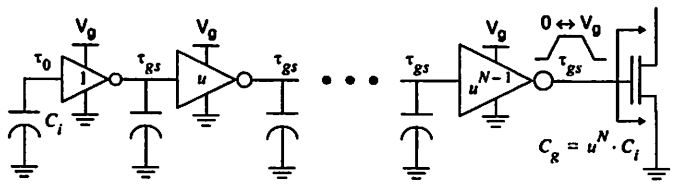


Figure 31: CMOS gate-drive scheme.

is designed such that the ratio of average dynamic current to load capacitance is equal for each inverter in the chain. Thus, the delay of each stage and the rise/fall time at each node are identical. It is a well known result that under some simplifying assumptions, the tapering factor u that produces the minimum propagation delay is the constant e [17]. However, in power circuits, the chief concern lies not in the propagation delay of the gate-drive buffers, but in the energy dissipated during a gate transition.

In a ZVS power circuit, the following timing constraint is desired:

$$\tau_x \gg \tau_{gs} \approx u\tau_0 \tag{70}$$

where τ_x is the soft-switched inverter output node transition time, τ_{gs} is the maximum gate transition time which ensures effective ZVS of the power transistor, τ_0 is the output transition time (rise/fall time) of a minimal inverter driving an identical gate, and u is the tapering factor between successive inverters in the chain. In general, it is desirable to make τ_{gs} as large as possible (yet still a factor of five to ten less than τ_x), minimizing gate-drive dissipation. Given τ_{gs} and τ_0, if there exists some $u > e$ such that the criterion given by (70) is met, the buffering scheme of Figure 31 will provide a more energy efficient CMOS gate-drive than that obtained through minimization of delay.

Determination of the Inverter Chain In this analysis, a minimal CMOS inverter has an NMOS device with minimum dimensions (W_o/L) and a PMOS device whose gate width is $\mu_n/\mu_p \approx 3$ times that of the NMOS device. It has lumped capacitances C_i at its input and C_o at its output. Given that the pull-down device operates exclusively in the triode region during the interval of interest, and assuming it is a long-channel device, it can be shown [18] that the output fall time of a minimal inverter driving an identical gate from $V_{out} = V_g - |V_{tp}|$ to $V_{out} = V_{tn}$ is:

$$\tau_0 = \frac{C_o + C_i}{W_o}\kappa, \tag{71}$$

which is linearly proportional to the capacitive load, inversely proportional to the gate-width of the n-channel device, and directly related to the application and technology dependent constant:

$$\kappa \equiv \frac{2L}{\mu_n C_{ox}(V_g - V_{tn})} \cdot \ln\left[\frac{(2V_g - 3V_{tn})}{(V_{tn})} \frac{(V_g - |V_{tp}|)}{(V_g - 2V_{tn} + |V_{tp}|)}\right]. \quad (72)$$

In [6], a similar expression can be found for the output fall time assuming a heavily velocity-saturated pull-down device.

The factor u which results in an output signal transition time τ_{gs} is found by solving:

$$\tau_{gs} = \frac{\kappa(C_o + uC_i)}{W_0} \approx u\tau_0, \quad (73)$$

yielding a corresponding tapering factor of

$$u = \frac{\tau_{gs} W_0 - \kappa C_o}{\kappa C_i} \quad (74)$$

between successive buffers. Given u, the number of inverters in the chain is:

$$N = \frac{\ln(C_g/C_i)}{\ln(u)}. \quad (75)$$

The inverter chain guarantees a gate transition time of τ_{gs} with minimum dissipation, and a propagation delay of

$$t_p \approx N u t_{po} \quad (76)$$

where t_{po} is the propagation delay of a minimal inverter loaded by an identical gate.

Loss Analysis There are two components of power dissipation in the inverter chain:

$$P_{dyn} = C_T V_g^2 f_s \quad (77)$$

$$P_{sc} = \sum_{i=1}^{N} \bar{I}_{sc_i} V_g \quad (78)$$

where $\bar{I}_{sc_i}$ is the mean short-circuit current in the i^{th} inverter in the chain, and the total switching capacitance, including the loading gate capacitance of the power MOSFET, is

$$\begin{aligned} C_T &= (1 + u + u^2 + \cdots + u^{N-1})(C_o + C_i) + C_g \\ &= \left[\frac{u^N - 1}{u - 1}\right](C_o + C_i) + C_g. \end{aligned} \quad (79)$$

Since u^N is the constant given by (69), C_T and thus, the dynamic dissipation, is minimized for large u.

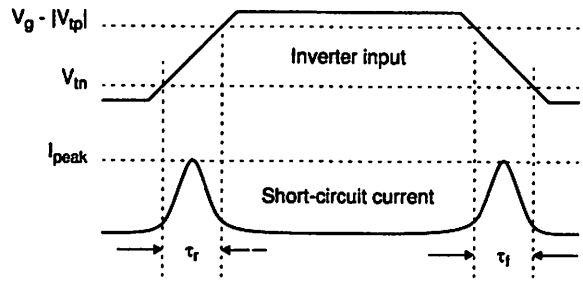


Figure 32: Short-circuit current in an inverter.

Though the dynamic component is readily calculated from (77) and (79), the short-circuit dissipation is more difficult to quantify. From Figure 32, it can be seen that short-circuit current exists in a CMOS inverter while the n- and p-channel devices conduct simultaneously ($V_{tn} < V_{in} < V_g - |V_{tp}|$), and that the total energy consumed during an input transient is proportional to both the input transition time and the peak short-circuit current (which in turn, is related to the output transition time [19]). Figure 33 plots simulation results of the ratio of short-circuit to dynamic dissipation per cycle versus the ratio of 10%-90% input to output transition times for a minimal inverter operated at $V_g = 5$ V and $V_g = 3$ V, and a ten times minimal inverter operated at $V_g = 3$ V. These results illustrate three key points regarding short-circuit dissipation in a CMOS inverter:

- The normalized E_{sc} is seen to increase dramatically with normalized input signal transition time, but is negligible for equal input and output signal transition times, and for faster input signal transitions.
- While the magnitude of short-circuit current is dependent on device dimensions (I_{peak} increases linearly with device size), the ratio of E_{sc} to E_{dyn} appears to be independent of size.
- For $V_g \rightarrow V_{tn} + |V_{tp}|$, the normalized E_{sc} decreases with decreasing supply voltage. While the 10%-90% input edge rate is relatively independent of supply voltage for short-channel devices, the duration of short-circuit current flow approaches zero.

Therefore, because the tapering factor u is constant throughout the inverter chain, providing equal transition times τ_{gs} at each node, the short-circuit dissipation is made negligible, particularly at low supply voltages. Furthermore, for $u > e$, less silicon area will be devoted to the buffering; thus parasitics, and ultimately, dynamic energy loss, are reduced as compared to the conventional CMOS gate-drive.

To make a first-order estimate of the total energy consumed in a single off-to-on-to-off gate transition cycle of a minimal power MOSFET, (77) and (79)

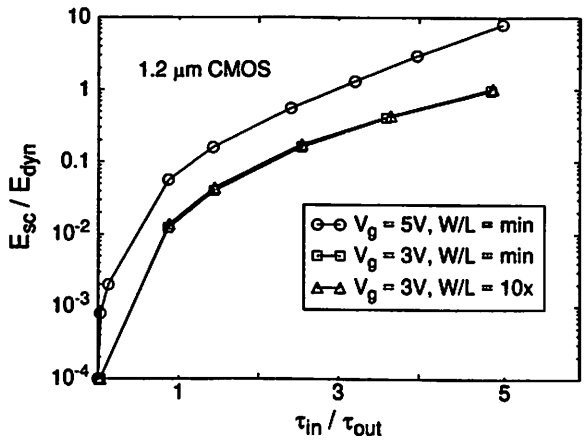


Figure 33: Simulation results showing normalized short-circuit energy versus normalized 10%-90% input edge rate for CMOS inverters in a 1.2 μm CMOS technology [20].

are used in conjunction with the values of u and N derived in (74) and (75), giving:

$$E_{go} \approx C_{go}V_g^2 \cdot \left[\frac{\kappa(C_o + C_i)}{\tau_{gs}W_o - \kappa C_o - \kappa C_i} + 1\right] \tag{80}$$

where C_{go} is the gate capacitance of a power transistor with minimum gate-width W_o, linearized over $0 \leq V_{GS} \leq V_g$. To obtain (80), it is assumed that the short-circuit dissipation in the inverter chain is negligible compared to the dynamic dissipation, that all capacitances scale linearly with gate-width, and that $u^N \gg 1$. Under these simplifications, gate-drive losses are expressed as a linear function of gate-width, identical in form to (52).

Scaling V_g The practical limit to gate-drive supply voltage scaling is set by increasing delays in the drive circuitry, which produce reversing returns in the reduction of gate energy consumption as $V_g \rightarrow V_{tn} + |V_{tp}|$ and below. Using a linearized first-order model to a CMOS inverter delay [8], it can be shown that for $V_g \gg V_t$, τ_o increases with V_g^{-1} for long-channel devices, and is roughly independent of V_g for heavily velocity-saturated short-channel devices. However, as $V_g \rightarrow V_{tn} + |V_{tp}|$, these delays increase rapidly [1].

This phenomenon is illustrated in Figure 34, where the output signal rise and fall times of a CMOS inverter with $W_p/W_n \approx \mu_n/\mu_p$ in a 1.2 μm technology are plotted versus the supply voltage, V_g. For $V_g > 3$ V, delays are indeed relatively independent of supply voltage, and the rise and fall times are nearly equal. However, as the supply is dropped below 2 V, it becomes comparable to $V_{tn} +$

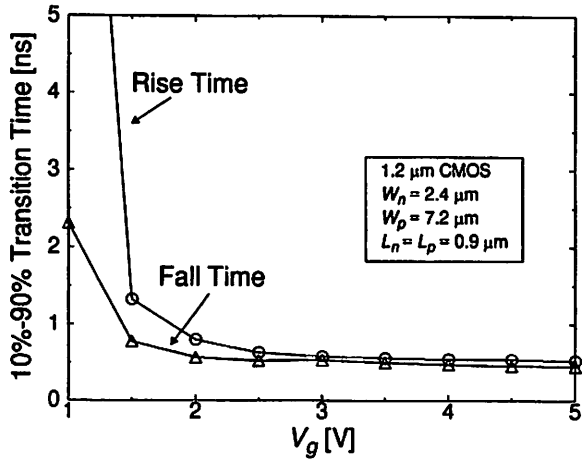


Figure 34: Simulated output rise and fall times for a minimal CMOS inverter driving an identical gate as a function of supply voltage, V_g.

$|V_{tp}|$, and inverter output signal transition times increase rapidly. Furthermore, because $|V_{tp}| > V_{tn}$ in this technology, the output rise time increases more quickly than the output fall time. To achieve balanced rise and fall times at the output of a CMOS inverter with a supply voltage comparable to V_t, the difference in threshold voltages of n-channel and p-channel MOSFETs must be considered in the ratioing of the devices.

Figure 35 plots the total gate energy consumed per cycle as a function of the gate-drive supply voltage. Here, power transistor size and $\tau_r = \tau_f = \tau_{gs} =$ 5 ns (a typical gate transition time for a 1 MHz ZVS power circuit) are held constant. For $V_g \gg V_t$, there is an approximately quadratic reduction in E_g with decreasing supply voltage. However, because of the increase in inverter output signal transition times, and the increase in buffer input and output capacitances associated with larger p-channel device ratioing, as $V_g \rightarrow V_{tn} + |V_{tp}|$ and below, the tapering factor, u, between successive inverters in the chain becomes small, and the dynamic energy consumed by the gate-drive buffering increases dramatically and begins to dominate over that required by the gate capacitance of the power transistor. Thus, when the dissipation in the inverter chain is considered in gate-drive supply voltage scaling, at ultra-low voltages, E_g *increases* as V_g decreases.

6.5.5 Optimum V_g

In most portable systems, it is common to have at least one low-voltage supply available for the gate-drive. While this low sub-system operating voltage may not be optimal, it is likely to be useful to reduce the minimum achievable FET

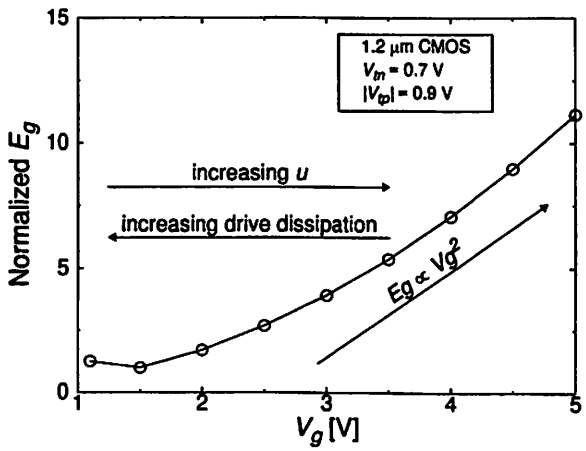


Figure 35: Gate energy (including the CMOS drive) per cycle versus gate-drive supply voltage for fixed power transistor size and $\tau_{gs} = 5$ ns.

losses in the power train of each DC-DC converter. Thus, it is important to compare the minimum achievable FET losses and the gate-width required to achieve this minimum loss for $V_g = V_{in}$ and V_g equal to this low-voltage subsystem supply.

In Figure 36, W_{opt} and P_{t-min} are plotted versus V_g. Simulation results on a large area n-channel MOSFET in a 1.2 μm CMOS technology have been interpolated to find device parameters R_o and E_{go} at each data point. Dissipation in the drive circuitry is included in E_{go}. From this plot, it can be seen that the greatest power savings with scaling V_g are achieved for $V_g \gg V_t$: Since E_{go} decreases quadratically, while R_o increases linearly, if the gate-width of the power device is appropriately scaled ($W_{opt} \propto \sqrt{R_o/E_{go}} \propto V_g^{-3/2}$), as indicated by (58), P_{t-min} decreases as $\sqrt{V_g}$. However, since *both* R_o and E_{go} increase as V_g is brought below the sum of the threshold voltages in the gate-drive buffers, P_{t-min} increases with any further decrease in V_g. It may be concluded that:

$$V_{g-opt} \approx V_{tn} + |V_{tp}|. \tag{81}$$

Consider a converter in a portable system operating from a lithium ion battery source. From Figure 36, the total losses in each power FET at $V_g = 1.5$ V (the operating voltage for the baseband circuitry in the current InfoPad terminal) are 20% lower than at $V_g = 3.6$ V (the nominal battery source voltage). However, the gate-width of each device must be increased by a factor greater than 4.7 to achieve this reduced dissipation.

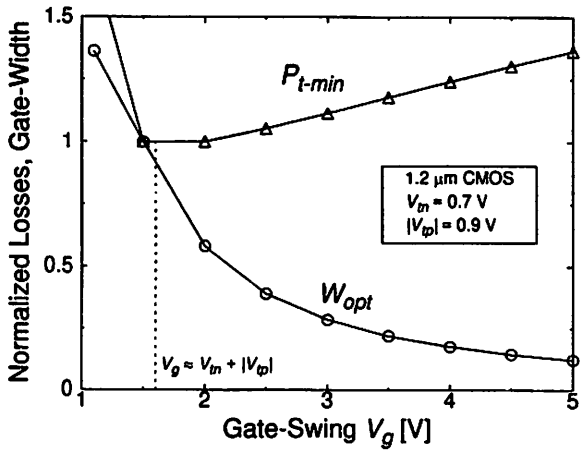


Figure 36: The optimal gate-width and minimum total dissipation for a power n-channel MOSFET vs. gate-swing in a 1.2 μm CMOS technology.

6.5.6 Reduced Gate-Swing Circuit Implementation

Figures 37 and 38 show a circuit implementation of a reduced-swing gate-drive and its associated waveforms in a low-output-voltage ZVS CMOS buck circuit. The gate of M_n is actively driven from 0 to V_g by its CMOS gate-drive. The gate of the P-channel power MOSFET is driven from V_{in} to approximately $V_{in} - V_g$ with an AC-coupled gate-drive. PMOS device M_{off}, whose gate swings from rail-to-rail, provides a low-impedance path from the gate of M_p to V_{in}, ensuring that M_p remains fully off during its off-state. In ultra-low-power applications, the AC-coupling capacitor $C_c \gg C_{gp}$ might be implemented on-chip.

6.6 PWM-PFM Control for Improved Light-Load Efficiency

While a PWM DC-DC converter can be made to be highly efficient at full load, many of its losses are independent of load current, and it may, therefore, dissipate a significant amount of power relative to the output power at light loads. Figure 39 plots power transistor losses (conduction and gate-drive) versus a 1000:1 load variation for a ZVS PWM buck converter with a peak-to-peak inductor current of two times the full load current. The power transistors are optimized for full load operation. From this plot, it may be concluded that a PWM converter which is 95% efficient at full load is roughly 3% efficient at one thousandth full load.

One control scheme which achieves high efficiency at light loads is a hybrid of pulse-width modulation and pulse-frequency modulation (PFM), commonly referred to as "burst mode". In this scheme, conceptually illustrated in Figure 40, the converter is operated in PWM mode only in short bursts of N cycles each.

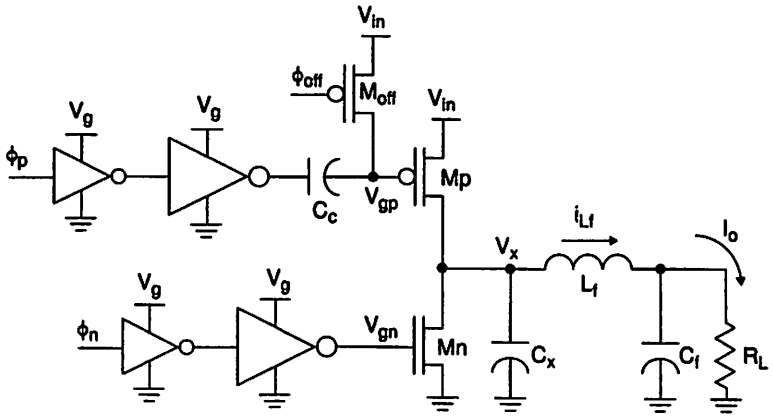


Figure 37: A reduced gate-swing CMOS buck circuit implementation with gate supply voltage V_g.

Between bursts, both power FETs are turned off, and the circuit idles with zero inductor current for M cycles. During this period, the output filter capacitor sources the load current. When the output is discharged to a certain threshold below V_o, the converter is operated as a PWM converter for another N cycles, returning charge to C_f. Thus, the load-independent losses in the circuit are reduced by the ratio $N/(N+M)$. As the load current decreases, the number of off cycles, M, increases.

During the N cycles that the converter is active, it may be zero-voltage switched. However, the transitions between idle and active modes require an additional energy overhead. When idle mode is initiated by turning both FETs off, the body diode of M_n picks up the inductor current until i_{Lf} decays to zero. In low-voltage applications, body diode conduction is highly dissipative. When the converter is reactivated, M_p charges C_x to V_{in}, introducing additional losses. The minimum number of off cycles, M_{min}, can be chosen to ensure that the energy saved by idling is substantially larger than this loss overhead.

Circuit implementations of PWM-PFM control may be found in [21] and [22].

7 Example Design

In this section, the design techniques of Sections 5 and 6 are applied to the 6 V to 1.5 V, 500 mA buck converter presented in [12]. All of the active devices are integrated on a single die and fabricated in a standard 1.2 μm CMOS process. The circuit exhibits nearly ideal ZVS using an adaptive dead-time control scheme similar to that described in Section 6.3.

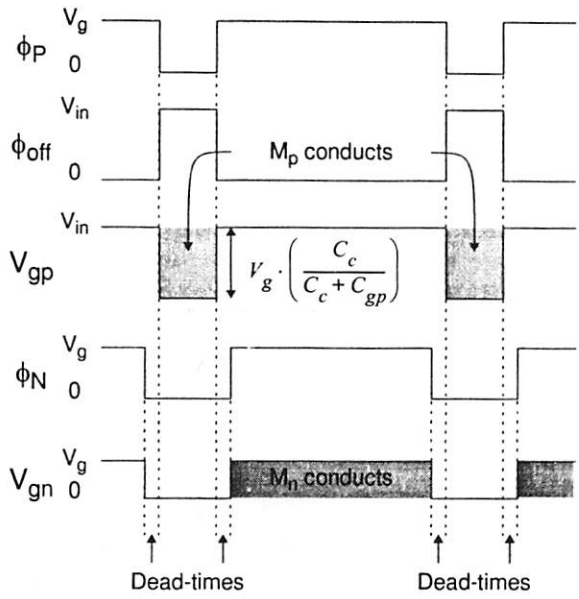


Figure 38: Waveforms for the reduced-swing gate-drive.

Figures 41 and 42 show the power train of the low-output-voltage CMOS buck converter with device sizes and component values, and its associated periodic steady-state waveforms. The inverter output node voltage is quasi-square with a nominal duty cycle, $D = V_o/V_{in}$, of 25%, and an operating frequency of $f_s = 1$ MHz which allows a compact, yet highly efficient solution. The inductor current reverses to allow ZVS transitions of the power transistors. The maximum asymmetry in the soft-switched transition intervals, $\frac{\tau_{x_{LH}}}{\tau_{x_{HL}}} = 4$ at full load, is chosen to make the timing constraint of (70) feasible in a 1.2 μm technology. From (45), this requires a minimum peak-to-peak inductor current ripple of $\Delta I = \frac{10}{3} I_o = 1.66$ A, and using (34), results in a filter inductor of value $L_f = 675$ nH. Allowing for a 2% peak-to-peak AC ripple in the output voltage, $C_f = 13.9$ μF is selected using (35). To slow the soft-switched transitions at v_x, snubber capacitance is shunted across the inverter output node. The total capacitance required to achieve $\tau_{x_{LH}} = T_s/10 = 100$ ns is $C_x = 5.56$ nF, where C_x includes the snubber and all parasitic capacitance at v_x.

The power transistors are sized according to (53) to minimize their total losses in periodic steady-state at full load. The minimum effective channel length, $L_{eff} = 0.9$ μm, is used. Device parameters R_o and Q_{go}, which represent the effective channel resistance and gate charge of a minimum gate-width device, are found at $V_g = V_{in} = 6$ V by interpolating results obtained from circuit simulations performed on extracted layout of large geometry FETs. Plugging

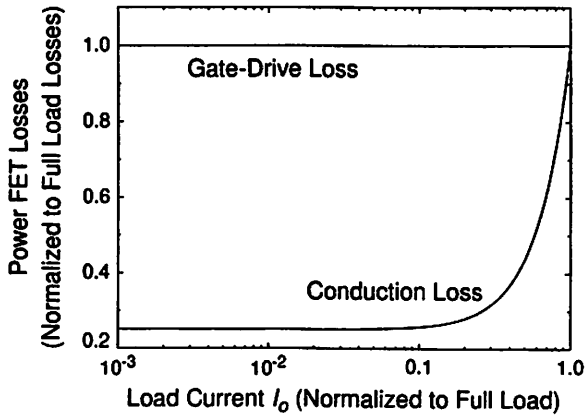


Figure 39: Power transistor losses versus a 1000:1 load variation for a ZVS PWM buck converter.

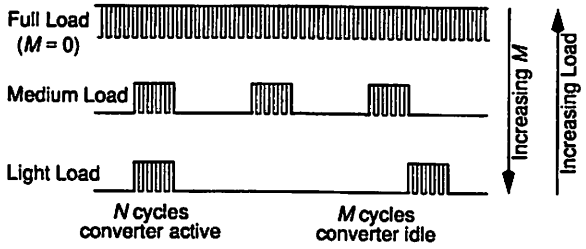


Figure 40: A conceptual illustration of PWM-PFM control.

$C_{go} = Q_{go}/V_{in}$ and all necessary application- and technology-specific parameters into (80), a first-order estimate to E_{go} is made. Approximate power transistor gate-widths are found by substituting this estimate and the interpolated value of R_o into (53). A prediction of the gate-drive design is effected through selection of u and N with (74) and (75). Iteration using circuit simulations on extracted layout is necessary to refine the design. From (54), total FET losses at full load can be estimated. The design is summarized in Table 2.

Due to die area constraints, the circuit as presented in [12] uses the full input voltage to drive the gates of the power transistors. To improve efficiency, the reduced-swing gate-drive implementation of Figure 37 may be used to bootstrap the gate-drive from the regulated output of the converter. This requires additional circuitry to deliver charge to C_f during start-up, avoiding the stable state in which $V_o = 0$ and $I_o = 0$. With $V_g = V_o = 1.5$ V, total FET losses may be reduced to roughly 4% at full load, but at the expense of considerable silicon area—the total gate-width would be increased by a factor greater than ten.

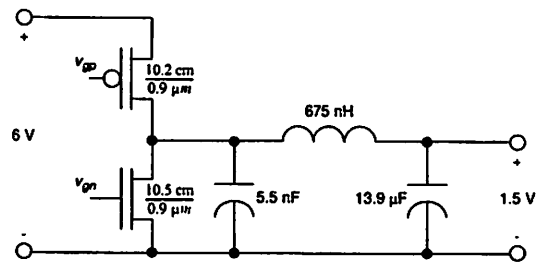


Figure 41: Circuit schematic for the example buck circuit.

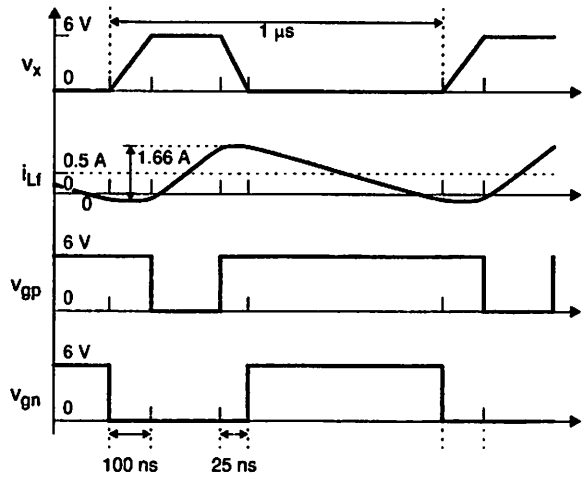


Figure 42: Ideal periodic steady-state waveforms for the example buck circuit.

8 Physical Design Considerations

8.1 Power Transistor Layout

The power transistors are arrayed as a number of parallel fingers whose length is determined by the maximum tolerable distributed *RC* delay of the gate structure (Figure 43). In order to reduce series source and drain resistances, the diffusion is heavily contacted, with source-body and drain running horizontally within each finger in metal1, and vertically throughout the array in metal2. The gate runs horizontally in polysilicon and is strapped vertically in metal1 such that each finger is driven from both sides.

Because the ZVS behavior of the power devices effectively eliminates their drain-body junction capacitance switching losses, increased drain diffusion area may be traded for more reliable and efficient body diode conduction. Rather than sharing diffusion between adjacent fingers in the array, well or substrate

Table 2: Example Design Summary.

	M_p	M_n
R_o	14.2 kΩ · μm	3.7 kΩ · μm
Q_{go}	14.4 fC/μm	16.2 fC/μm
E_{go}	97.8 fJ/μm	114.7 fJ/μm
Gate-width, W	10.2 cm	10.6 cm
Buffering, u	5.6	5.2
Buffering, N	4	4
Estimated Loss	2.7%	3.2%

contacts may be placed at a minimum distance from drain contacts to minimize both the series resistance and transit time of the body diode. This is the approach taken in [12]. In [23], a more area-efficient layout is used. Here, body and drain diffusion of adjacent fingers are shared, eliminating the small spaces between each finger. Although this tiling strategy results in an inferior body diode structure, the length of source-body, drain, and gate straps are minimized for a given gate-width, reducing the physical resistances in series with the terminals of the device.

Due to the potentially large magnitude of substrate current injection, healthy well or substrate contacts should be placed throughout the structure, and a guard ring should surround each power device, eliminating latch-up and decoupling supply bounce from the control circuitry.

8.2 Board-Level Assembly

It may soon be possible to build a completely monolithic converter including control circuits, power semiconductors, magnetics, and capacitors. However, it appears that for some time it will remain more technically and economically feasible to combine separate semiconductor, magnetic, and capacitive components. A PWM converter may have only four separate components—an IC with power devices and control, two multilayer ceramic capacitors for input and output filters, and a filter inductor.

Parasitic inductance, capacitance, and resistance in interconnects may cause substantial losses. The packaging and interconnect technology may dominate the physical size, especially in a low-power converter. There are also likely to be significant effects on cost and reliability. Many of these considerations point towards the use of a multi-chip module (MCM), or similar technology. (MCM may be a poor term in this case, since the module may contain only one semiconductor die, along with the reactive components). The elimination of a separate package for the silicon circuitry may significantly decrease physical size; parasitics associated with the package are eliminated.

The effect of parasitics on converter efficiency is determined by the ratio of the parasitic impedance to the effective load impedance. Series impedances such

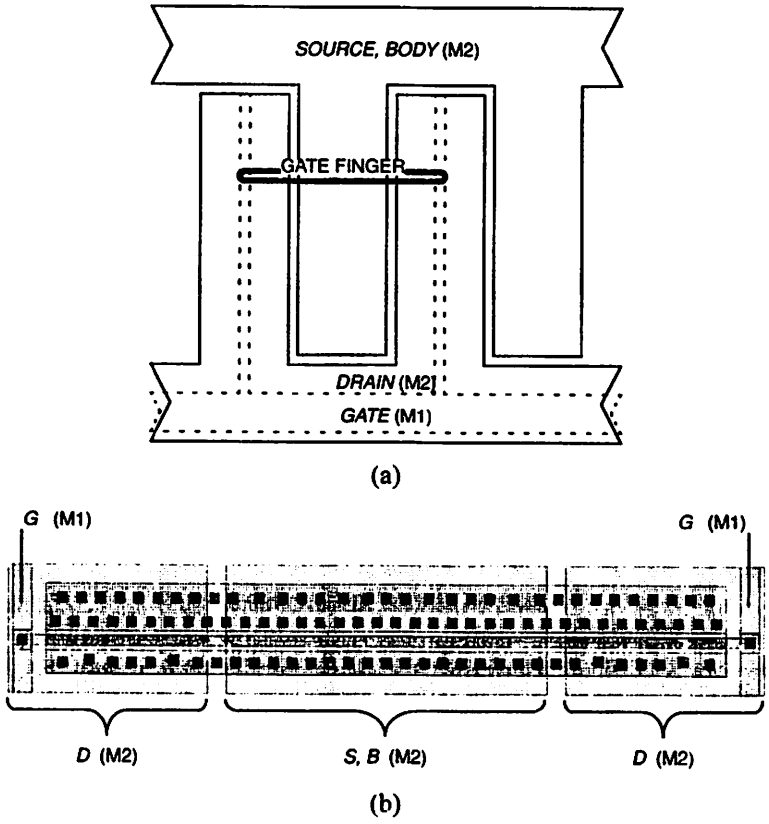


Figure 43: Layout of a power MOSFET: (a) Metallization pattern. (b) One gate finger.

as inductances and resistances are most important at low voltages, although at very low current levels, they become less important again. Shunt impedances, such as stray capacitance, become important at low current levels, but ZVS can eliminate the losses associated with them.

Decreasing the interconnect resistance is effected by careful layout using wide, short conductor paths, and the use of thick, low resistivity conductors. Stray inductance is reduced by minimizing the area of loops in critical paths. In a multilayer interconnection technology, the lowest stray inductance is achieved by using paired overlapping conductors in different layers, with thin dielectric separating the layers [24].

Numerous MCM technologies suitable for low-power converters exist. For higher-power converters, a substrate with good thermal conductivity is a necessity, but for lower-power converters, the requirements are much less stringent.

Perhaps the most important parameter is low sheet resistance, to reduce series interconnect resistance. Thin dielectric between conductive layers is also desirable for minimizing stray inductance, but most technologies use thin enough dielectric that other stray inductances, such as bond wires and package leads, will dominate when careful layout is used. MCM technologies are surveyed in [25, 26].

8.3 Magnetic Components

Magnetic components (inductors and transformers) are essential for power electronics. With a few exceptions (such as switched-capacitor converters), switching power converters ubiquitously require inductors and/or transformers. Inductors are required as components of low-loss filters and resonant circuits. Transformers are used for isolation, converting voltage and current levels, and energy storage and transfer. Magnetic devices serve these and other functions in both traditional and newly introduced converter topologies.

Magnetic devices often are the physically largest components in a converter, and can be the most expensive. Typically, they must be custom designed for a particular circuit, either because suitable standard commercial parts do not exist, or because of the size, cost, and performance advantages possible in a custom design. For these reasons, it is important for a power converter designer to have some knowledge of magnetics design. A complete review of magnetics design is beyond the scope of this text. However, some of the special issues in magnetics for low-power portable applications will be addressed. A basic tutorial introduction to magnetics for power electronics can be found in [9]. A more complete work on magnetics design is [27].

8.3.1 Magnetic Cores

In some cases, a coil (or pair of coils for a transformer) may have sufficient inductance for a power circuit application, even with no magnetic core material. Such an air-core coil is attractive because it can be fabricated on a PC board or a MCM substrate simply by patterning a spiral, ideally in multiple layers. However, there are many advantages to adding a core, and there are potential pitfills in using an air-core coil.

An air-core coil is typically characterized at a given frequency by its inductance and its quality factor, $Q = \omega L/R$, where R and L are the effective values at a given frequency, ω. A high value of Q, in the range of 20 to 200, is required for efficiencient operation. The addition of a magnetic material can, ideally, increase the inductance of a coil by a factor equal to the relative permeability of the material, μ_r, without affecting the resistance of the coil. Since practical magnetic materials for power applications often have permeabilities in the thousands, the value of Q can be greatly increased by the addition of a magnetic core. However, the increase is not as large as might be expected from this naive

analysis. Power is dissipated in the core, contributing to the effective value of R. In order to combat the resulting lowering of Q, and/or to prevent magnetic saturation of the core, an air gap is often introduced in the magnetic path through the core. This decreases the gain in L. Nonetheless, the increase in Q is substantial, and it is rarely possible to make practical magnetic components for power circuits operating below 1 MHz without the use of a magnetic core.

An additional advantage of a magnetic core is that it may serve to contain the flux. The external high-frequency flux from an air-core coil may cause RFI problems in nearby circuits, and will induce eddy currents in any nearby metal objects. The resulting losses can severly lower the Q of the coil, and even decrease its inductance. It may be possible to place the coil in a volume empty of metal components to avoid eddy current problems, but this additional volume becomes another reason to prefer using a component with a core, which is typically smaller than the equivalent air-core coil with the same inductance, even without this extra volume.

The most commonly used magnetic material for power applications is MnZn ferrite. Although it has a lower saturation flux density than typical magnetic metal alloys, it has much higher resistivity ($\approx 10\ \Omega$–cm, vs. $20 \times 10^{-8}\ \Omega$–cm for NiFe alloy). This allows operation at high frequencies (between 20 kHz and 1 MHz) without the severe eddy current losses that would result from using a lower-resistivity material.

Despite the high resistivity of ferrites, significant losses do occur in high frequency operation due to hysteresis. Since the hysteresis losses increase rapidly with frequency and flux level, it is often necessary to reduce flux level at high frequency in order to keep losses under control. This typically limits the flux density to well below the saturation flux density, and thus hysteresis loss is the most important parameter in determining the power handling capability, as well as the efficiency, of a magnetic component based on a ferrite core.

Although power handling density of magnetic components should ideally increase proportionally to frequency, the losses in ferrites increase faster than this and thus, the power handling is a weaker function of frequency, typically reaching a maximum around 500 kHz to 1 MHz for MnZn ferrites. To further improve power density, different materials are needed. NiZn ferrites may give a factor of two or three improvement in power density at frequencies in the range of 10 to 30 MHz [28]. More substantial improvments require a superior technology.

One emerging technology is microfabriction using thin-film magnetic metal alloy core materials. A process similar to that used for IC manufacture (more closely related to the process used for thin-film magnetic recording heads) is used to deposit and pattern thin films of magnetic alloys and copper coils. These magnetic materials can have very low hysteresis loss, and can be operated near their saturation flux density (≈ 1 T) without disproportionate losses. The use of thin films and fine patterning can control eddy current losses in both the magnetic material and the coil. Experimental devices have been demonstrated

in principle [29, 30, 31, 32, 33, 34], and calculations show that much higher power density will be possible [35]. Although fabricating the magnetics on a separate substrate from the silicon circuitry and combining the two in a multi-chip module (MCM) is more likely to be economically viable, it is also possible to fabricate the magnetics and silicon circuitry on a single substrate, as has been experimentally demonstrated in [36].

Either because of the use of planar microfabrication techniques, or for packaging and thermal dissipation considerations, magnetics for low-power converters are often designed in a planar configuration. While this presents no particular difficulties for transformer design, it can be a problem for inductors that use a gap in the magnetic path. The resulting magnetic field distribution can introduce severe eddy current losses in the conductor. For a careful description of this problem, and some remedies, see [35, 37].

8.4 Capacitor Technologies

Capacitors generally have much higher performance than inductors in terms of energy density, loss, and cost. However, they can still be an important limiting factor in converter design, because of substantial improvements in advanced magnetics technology, and because circuits are usually designed to shift the bulk of the energy storage requirement from inductors to capacitors. Four major technologies are discussed here: multilayer ceramic, metalized plastic film, aluminum electrolytic, and tantalum capacitors.

Multilayer ceramic capacitors are the technology of choice for high-frequency high-power-density converters. The dielectric material can be chosen to compromise between low losses and highly-stable capacitance, or higher energy-storage density with higher losses and poorer stability over temperature and voltage. Typically a low-loss material, such as those designated COG or NPO, is required in applications in which a substantial AC voltage at high frequency appears across the capacitor. In applications such as a filter in which only a small AC ripple appears across the capacitor, materials such as X7R allow much higher capacitance in the same volume. Although the material has higher losses, they are insignificant in a low-ripple application. Higher K (dielectric constant) materials are available to give higher energy-storage density, but they typically lose their advantage over X7R or similar materials when considered over the wide range of temperatures typically expected in power circuits.

Metalized film capacitors are generally less expensive than multilayer ceramics, at least for moderately large values, but are not as high in energy-storage density. Two important dielectric materials are polypropylene, which gives low losses at high frequency, and polyester, which has higher losses but give higher energy-storage density.

Electrolytic capacitors, including aluminum electrolytic and tantalum, give much higher energy-storage density than other types discussed here. However, they are limited by their high ESR (effective series resistance). Thus, they

are not useful for high-frequency AC applications. Furthermore, in filter applications, the ESR is typically a higher impedance than the capacitance at the switching frequency. Thus, the capacitance must be oversized, with the size chosen of the basis of the ESR. As a result, the size does not decrease as the switching frequency is increased. Thus, electrolytic capacitors only show advantages over other types at relatively low switching frequencies.

9 PWM Control

9.1 Micro-power digital PWM control

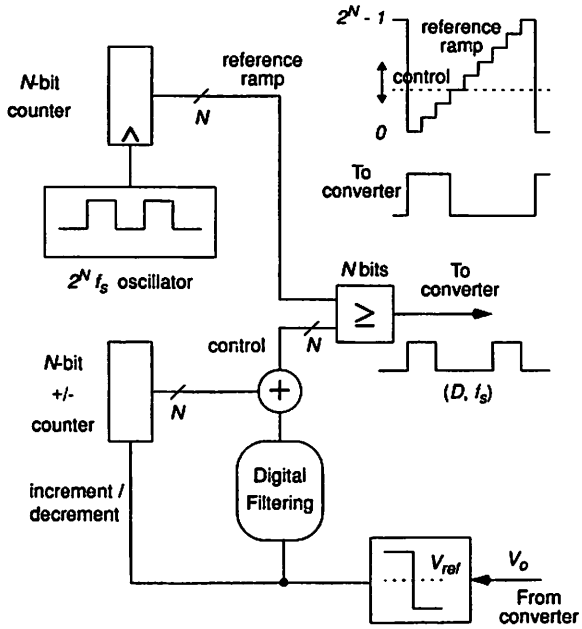


Figure 44: A micro-power digital PWM controller.

Figure 44 shows the block diagram of a digital PWM controller. The analog output voltage, V_o, is sampled at the switching frequency, f_s, and converted to a one-bit digital signal through a slicer with switching threshold V_{ref}. The output of the slicer is integrated by an N-bit increment/decrement counter. The N-bit duty cycle control signal consists of this integral term, and a proportional term which is digitally filtered to provide the compensation necessary to achieve loop stability.

The N-bit output of a counter, clocked at 2^N times the converter switching frequency, is used as a reference ramp signal. A glitch-free N-bit digital com-

parator, also clocked at $2^N \cdot f_s$, compares the reference ramp and the control signal, generating a pulse-width modulated clock with variable duty cycle:

$$D = \frac{\text{control}}{2^N - 1}, \tag{82}$$

and constant frequency f_s.

The power consumption of the controller is kept low by aggressively scaling the operating voltage (typically, the lowest voltage available to the system may be used), and minimizing physical capacitance. While power consumption may be substantially reduced by decreasing the bit-width, N, the granularity of the control of the duty cycle:

$$\Delta D = 2^{-N} \cdot T_s \tag{83}$$

is also reduced. This may result in a larger low-frequency output voltage ripple.

10 Alternatives to Switching Regulators

For ultra-low-power applications, the complexity of a switching regulator may prove prohibitive. In particular, the necessity of including a magnetic component may preclude the use of a PWM DC-DC converter in many applications. Two alternatives that do not require magnetic components are linear regulators and switched-capacitor converters. Both types of circuits can be advantageous in ultra-low-power applications, and in a limited range of other specialized applications.

10.1 Linear regulators

Linear regulators, illustrated conceptually in Figure 45, are limited by two principle constraints. The output voltage, V_o, must be less than the input voltage, V_{in}, and the efficiency, η, can never be greater than V_o/V_{in}. However, linear regulators have the advantage of requiring few or no reactive components, and they can be very small and simple. This makes them attractive for portable applications.

A linear regulator can be efficient only in applications that require an output voltage just slightly below the input voltage. This requirement may be incompatible with other system design constraints, but in some systems it is practical, and, in this case, a linear regulator may be highly efficient. The achievable efficiency then depends on two parameters of the regulator: quiescent current and dropout voltage. The quiescent current determines the regulator's dissipation when the load is not drawing current, and in ultra-low-power applications, it may also contribute significantly to dissipation at full load.

If the input voltage of a linear regulator drops below a certain threshold, regulation is lost, and the output voltage will sag below the nominal regulation point. Dropout voltage is this minimum voltage difference between input and

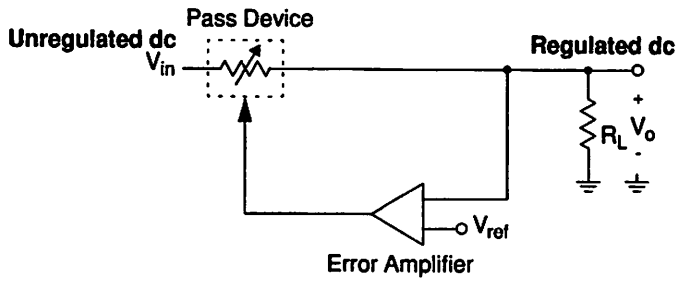


Figure 45: Block diagram of a linear (series-pass) regulator.

output required to maintain regulation. If it is not very low, it can conflict directly with the design requirement of having the output voltage only slightly less than the input voltage, and will therefore preclude high efficiency. This becomes especially important in low-voltage systems. With a 10 V output, a 2 V dropout voltage represents only a 20% increase in the minimum input power over what would be required with zero dropout voltage. However, with a 2 V output, a 2 V dropout voltage doubles the minimum input power.

Linear regulator circuits with low quiescent power, and PNP or MOSFET pass devices to allow low dropout voltage, are now commercially available. In the limited class of circuits that require a regulated voltage just below the input voltage of the regulator, these can provide a high-efficiency solution.

10.2 Switched-capacitor converters

Switched-capacitor converters (also known as charge pumps) are widely used in ICs where a voltage higher than, or of opposite polarity to, the input voltage is needed. Unlike a PWM converter, a switched-capacitor converter requires no magnetic components. In addition, it is often possible to integrate the necessary capacitors, but applications are usually limited to those in which poor efficiency and very low output power are adequate.

Figure 46 illustrates the basic principle of operation of a switched-capacitor voltage doubler. The switches are closed in pairs, alternately. First the switches labeled ϕ_1 are closed, charging capacitor C_s to the input voltage, V_{in}. Then the ϕ_1 switches are opened, and the ϕ_2 switches are closed. This places C_s, which is now charged to V_{in}, in series with the input voltage, producing a voltage of $2V_{in}$ across the output. The cycle then repeats. The output capacitor maintains the output voltage near $2V_{in}$ during ϕ_1. The same converter topology can be used as a step-down converter, producing an output voltage of half the input voltage, by exchanging the input and output terminals. By using more complex configurations, it is possible to produce any rational conversion ratio, for example by first stepping the voltage up by one integer ratio, and then stepping down by another integer ratio. Some of the many possible topologies

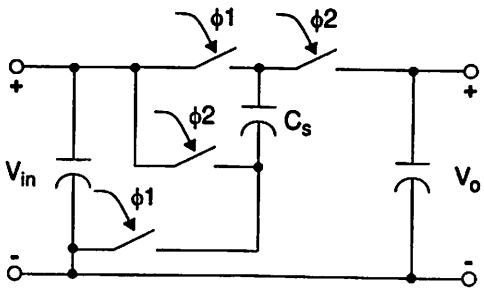


Figure 46: A switched-capacitor voltage doubler. Switches labeled ϕ_1 and ϕ_2 are closed alternately.

are discussed in [38] and [39].

Like a PWM DC-DC converter, a switched-capacitor converter may be built entirely of theoretically lossless elements—in this case, only switches and capacitors. However, a switched-capacitor converter is not ideally lossless. As the parasitic resistances in the capacitors and switches approach zero, the loss in the converter approaches a non-zero limit. This is in contrast to a PWM converter, in which the losses approach zero as parasitic effects are reduced.

The inherent losses in a switched-capacitor converter are due to unavoidable dissipation which occurs when a pair of capacitors, charged to different voltages, are shorted together through a switch. If two capacitors with values $C1$ and $C2$, initially charged to voltages V_{1_0} and V_{2_0}, respectively, are shorted together through a parasitic resistor R, the energy dissipated in the resistor will be

$$E_{diss} = \frac{1}{2}\frac{C_1 C_2}{C_1 + C_2}(V_{1_0} - V_{2_0})^2. \tag{84}$$

Note that this is independent of the value of R.

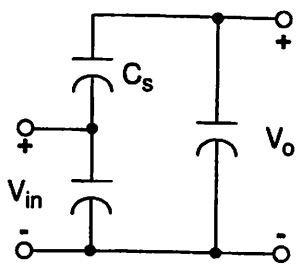


Figure 47: Equivalent voltage doubler circuit during ϕ_2.

To better understand these losses, consider the efficiency of the voltage doubler shown in Figure 46. During ϕ_2, the equivalent circuit is as shown in Figure 47. The charge flowing to the output is supplied by both the input and C_s.

During ϕ_1, this same quantity of charge must be supplied from the input and stored on C_s for the next cycle. Since all the charge that flows out of the output must be supplied twice by the input, the average input current must equal twice the average output current, i.e., $I_{in} = 2I_o$. Thus, the efficiency is

$$\eta = \frac{V_o \cdot I_o}{V_{in} \cdot I_{in}} = \frac{V_o}{2V_{in}} \tag{85}$$

The efficiency would be 100% if V_o were in fact twice V_{in}. However, in order for a charge, Q, to flow into C_s during ϕ_1 and subsequently flow out of C_s during ϕ_2, the voltages applied across C_s during the two phases must differ by an amount $\Delta V = Q/C_s$. Assuming that the RC time constant determined by the parasitic resistance of the switches and C_s is small compared to the switching period so that the charge on C_s reaches its steady-state value before the end of each phase, and that the input and output capacitors are large enough to maintain constant V_{in} and V_o, the voltage drop is $\Delta V = 2V_{in} - V_o$. With a switching period of T_s, $Q = I_o \cdot T_s$, and so

$$2V_{in} - V_o = \frac{I_o \cdot T_s}{C_s}. \tag{86}$$

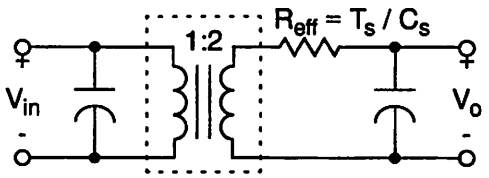


Figure 48: Equivalent circuit for the switched-capacitor voltage doubler.

The circuit may be modeled as shown in Figure 48, with an ideal doubler (shown as an ideal transformer) followed by an effective resistance

$$R_{eff} = T_s/C_s \tag{87}$$

that accounts for the voltage drop ΔV. The effective resistance also accounts for the loss; calculating the dissipation in this resistor gives a result identical to that found from (84).

In general, the model of a switched capacitor converter includes an ideal transformer with a fixed rational turns ratio, N, and an effective resistance. The conversion ratio, N, can be chosen to bring V_o near the desired output voltage; to precisely regulate V_o, R_{eff} is varied through changes in the switching frequency. Using R_{eff} for regulation is undesirable, since increasing it to lower the output voltage produces additional power dissipation. However, N is fixed by the topology, and cannot be used to regulate the output.

This is the main limitation of switched-capacitor converters: they can efficiently *convert* voltages, but they cannot *regulate* these converted voltages any more efficiently than a linear regulator. Thus, their efficient application is limited to situations in which a voltage must be converted to another rationally related voltage, but regulation is not necessary, or to situations in which the regulation range is limited, and so the efficiency $\eta = V_o/(N \cdot V_{in})$ is adequate.

In practice, there are several other considerations that limit efficiency in a CMOS implementation of a switched-capacitor converter. In order for (87) to hold, it is necessary for the time constant of the switched capacitor and the on-resistance of the switch to be much less than the switching period, i.e. $C_s \cdot R_{on} \ll T_s$. This requires the use of a large MOSFET to implement the switch, but the gate-drive for that device then requires substantial power, especially if a high switching frequency is used to minimize the required size of C_s. Thus, gate-drive loss must be considered in the design.

If an on-chip capacitor is used for C_s, the stray capacitance from one of its plates to ground will be a substantial fraction of its terminal capacitance. This introduces $C_{stray} \cdot V^2 \cdot f_s$ loss, further hampering efficiency. Technologies for fabricating capacitors with low stray capacitance to ground, or off-chip capacitors are necessary to achieve high efficiency.

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