SYNTHESIZING ARBITRARY DRIVING-POINT AND TRANSFER CHARACTERISTICS

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Synthesizing arbitrary driving-point and transfer characteristics

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Abstract

The property of any two-terminal resistive device is characterized by its driving-point (DP) characteristic, and any two-port resistive device with zero input current is described by its transfer characteristic (TC). Synthesizing a two-port device with a prescribed transfer characteristic is usually easier than synthesizing a two-terminal device with a prescribed driving-point characteristic. In this paper we propose an approach to synthesize a driving-point characteristic of a two-terminal device from the transfer characteristic of a two-port device, so that the resulting DP plot of the two-terminal device is exactly the same as the TC plot of the two-port device. We also illustrate the use of digital circuitry to synthesize arbitrary transfer characteristics. This technique will benefit the design and analysis of complex nonlinear electronic circuits and systems. A variety of characteristics synthesized using this approach are presented.

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I. Introduction

Two-terminal, or one port, devices play a major role in electrical circuits and systems. A two-terminal resistive device is characterized by a relation between the branch voltage and the branch current, so-called $v - i$ characteristic, or by its *driving-point (DP) characteristic* relating its port voltage and its port current [1], a fundamental concept in the study of electrical circuits. The DP characteristics of commercially available devices can usually be found in data books. However, there are other applications where a specific DP characteristic must be used. For example, in the synthesis of a nonlinear network which realizes a prescribed dynamical behavior the optimal $v - i$ characteristics of the synthesized nonlinear resistors are seldom available from existing commercial devices. Several approaches for synthesizing, in particular nonmonotonic characteristic, have been reported in the literatures [2]–[5]. Unfortunately, synthesizing a device with an arbitrary $v - i$ characteristic is cumbersome, or even not applicable using these techniques.

The class of two-port resistive devices with zero input currents is characterized by their *transfer characteristic (TC)* between the input voltage v_1 and the response (output) voltage v_2 [1]. Usually synthesizing a two-port device with a prescribed transfer characteristic is easier than synthesizing a one-port device with a prescribed DP characteristic.

In this paper we propose an approach for synthesizing a prescribed DP characteristic of a nonlinear resistor from the TC of a two-port resistive element. The implementation of the TC to DP characteristic converter is described in Section II. A digital technique for synthesizing a two-port resistive element with an arbitrary TC is presented in Section III. In Section IV we demonstrate a variety of DP characteristics synthesized using the method proposed in this paper.

II. Implementation of the TC to DP characteristics converter

The block diagram of the TC to DP characteristic converter is shown in Fig. 1. The TC to DP characteristic converter is a 3-port device that when connected as in Fig. 1 would have a DP characteristic in the input port equal to the TC of the two-port under consideration.

There are two realizations for the proposed conversion as described below.

Realization I

The block diagram of realization I is shown in Fig. 2. This realization simply consists of a linear resistor R connected accross the two-port. Assume that the TC of the two-port device is

$$v_2 = f(v_1) \tag{1}$$

According to the Kirchhoff's laws, we have

$$i = \frac{v_1 - v_2}{R} = \frac{v_1 - f(v_1)}{R} \tag{2}$$

Defining

$$g(v_1) = \frac{v_1 - f(v_1)}{R} \tag{3}$$

we obtain

$$i = g(v_1) \tag{4}$$

The only difference between the TC and the resulting DP characteristic is the linear term v_1/R in (2) corresponding to a straight line with the slope $1/R$ in the $v - i$ plane. This needs to be take into account in the design of the TC characteristic to obtain the correct DP characteristic.

Realization II

The block diagram of realization II is shown in Fig. 3a. In the converter circuit we use a voltage-controlled current source (VCCS) instead of the linear resistor R in Fig. 2. The implementation of the VCCS is shown in Fig. 3b.

Assume also that the TC of the two-port device is defined by (1). The defining equation for the voltage controlled current source (VCCS) implies that

$$i_2 = kv_2 \tag{5}$$

where k is the scale factor of the VCCS, thus we obtain

$$i = i_2 = kv_2 \tag{6}$$

Obviously, the resulting DP characteristic is

$$i = kf(v_1) \tag{7}$$

Thus the DP characteristic is a scaled version of the TC.

III. A digital technique for synthesizing prescribed TCs of two-port devices

In this section we describe an implementation of arbitrary transfer characteristics using digital hardware. The use of digital hardware allows for more flexibility and precision in synthesizing transfer characteristics, although operating at lower frequencies than analog hardware. This system, coupled with the TC to DP converter in the last section, results in a flexible platform for synthesizing arbitrary DPs, which are useful in prototyping complex nonlinear circuits.

In particular, we construct a two-port with an arbitrary transfer function between the

port voltages, with zero current into the input port.

The V-V transfer function generator is built using digital hardware coupled between necessary A/D and D/A converters, so that it appears as an analog device. The analog voltage-to-voltage mapping is performed in three distinct steps. First, the input analog voltage is sampled by the A/D converter and converted into a digital representation. Then, the digital representation is used by the digital hardware to map to the correct digital output. The conversion of the digital output into an analog output voltage completes the analog voltage-to-voltage mapping. Beyond selecting which D/A and A/D converters to use, most of the design work centers on how the digital output is chosen or calculated based on the digital input and the desired transfer characteristic.

We implemented two versions of the V-V transfer function generators, a two-port representation and a four-port representation. Different methods are utilized for these two versions to yield the correct output digital number given some input digital number. The two-port version finds the correct output using a table lookup with the inputs as the indices. Since no actual calculations are done, for any desired transfer function, the output values will have to be precalculated and loaded into some type of digital memory, in this case EPROMs, prior to the operation of the circuit. This limits the flexibility of the one-port V-V function generator somewhat since each new function requires a new set of data. The four-port version manages to get around this limitation by using a DSP chip for the real-time calculation of the proper output values. This approach offers greater flexibility since new functions can be implemented by simply reprogramming the DSP chip. Furthermore, the amount of data required for a table lookup of a 4-port TC will be too large to be practical. On the other hand, in a table lookup approach, the time required to compute the output is independent of the complexity of the transfer characteristic, whereas this time can vary in a DSP implementation.

A. two-port V-V transfer function generator

Fig. 4 (a) depicts the top-level block diagram of the two-port V-V transfer function circuit. A small logic controller regulates input sampling, EPROM table lookup, and con-

version into analog output Any desired V-V transfer function can be achieved by simply loading the EPROMs with the correct data. All digital representations in this circuit have 16 bits of precision.

Logic design: The logic controller is built as a finite state machine using one-hot encoding (one state per flip-flop) in order to simplify debugging. The controller provides a timing mechanism for the A/D and D/A converters. The specifics of this design are dependent on the actual A/D and D/A converters employed, and Fig. 4(b) gives a component level schematic of the logic controller. Fig. 4(c) shows the corresponding state transition diagram.

EPROM programming: Data for the EPROMs are calculated using a simple C program implementing the transfer function. The program takes all possible input digital values and finds all respective output digital values depending on what transfer function is desired. This data is stored in a file so that an EPROM programmer can be used to load the information into the actual EPROM chips.

Circuit performance: The resulting implementation runs at an overall sampling rate of 80.14 kSPS (kilosamples per second). The delay between the correct analog voltage being output after latching an analog voltage on to the analog input is 18 ms. Input and output voltage ranges have 16 bits of resolution.

Analysis: There are some issues associated with this design of the two-port V-V arbitrary function generator that requires further investigation. Due to the digital nature of this realization, further study is required to study how aliasing, distortion, quantization error, overall delay affect the behavior of nonlinear circuits utilizing this system.

B. Four-port V-V transfer function generator

A DSP board is at the heart of the physical implementation of the four-port V-V arbitrary function generator, replacing the EPROM table lookup in the two-port version. We

use a commercially available DSP board with two sets of A/D and D/A converters, which provides the ideal hardware for four-port representations. In a manner similar to the two-port design, input analog voltages from both ports are latched by the A/D converters. The proper corresponding output values are computed in real-time by the DSP chip and the D/A converters then output the analog voltages (Fig. 4d).

DSP board: The heart of the DSP board consists of a TMS320C30 floating point DSP chip. The board also provides low-pass filters for the inputs and outputs along with 16 bit D/A/D converters. All digital representation and calculations are performed in 16 bits precision and the maximum rate of sampling is 200 kHz.

Real-time calculation of output values: The DSP chip is programmed using either C or assembly. The desired transfer function is written in the chosen language. The program is compiled and downloaded to the DSP chip and the DSP chip will perform the necessary calculations by running the compiled programs. When the desired transfer characteristic is so complicated that it takes the DSP chip longer than a sample period to finish the computation, some samples will be discarded. The use of DSPs is more flexible than the use of lookup tables since a different transfer function can be realized by simply altering the program. Furthermore, with 16 bits of precision, the V-V transfer characteristics for a four-port will require too much memory for a practical table lookup approach.

Performance: The circuit runs at the maximum rate of 200 kHz with 16 bits of resolution for input and output voltages given simple transfer functions. Delay between the desired analog output voltage after a given input analog voltage is much less than the two port version if the circuit is run at this high sampling rate. The operation and reprogramming of the circuit is achieved interactively by running a TMS320 interface application on a personal computer.

Analysis: The four-port representation of the V-V transfer function generator has many of the same limitations associated with the two-port version discussed earlier, due to its inherent digital nature. The most important issue here is speed of operation, which is less than

what can be achieved with analog parts.

IV. Examples of DP characteristics synthesized from TCs

By using the approach proposed in this paper, a variety of DP characteristics of two-terminal, or one-port, devices synthesized from TCs of two-port devices are shown in *Figs.* 5–9. A TC of a two-port device, described by a sinusoidal function $v_2 = asin(v_1)$ shown in Fig. 5(a), is synthesized using the digital technique presented in Section III. Figs. 5(b) and (c) show the DP characteristics $i = ksin(v_1 t)$ converted by *realization I* shown in Fig. 2 (after compensation of the linear term) and*realization II* shown in Fig. 3(a), respectively, from the TC shown in Fig. 5(a). Next we choose a two-port device with a square function $v_2 = av_1^2$ TC. The circuit implementation using an analog multiplier and its TC described by a square function $v_2 = av_1^2$ are shown in Figs. 6(a) and (b), respectively. The DP characteristic $i = kv_1^2$ converted by *realization II* from the TC in Fig. 6(b) is shown in Fig. 6(c). Figs. 7a and 8a shows two-port devices, which are operational amplifiers operating in a saturation region (Fig. 7) and a linear region (Fig. 8) respectively. The TCs, and the DP characteristics converted by the *realization II* from the TCs shown in Fig. (7b-8b) and Fig. (7c-8c) respectively. To validate the robustness of the converter presented in this paper, a low power transformer is chosen as a two-port device, as shown in Fig. 9(a). Its TC with hysteresis and the resulting DP characteristic converted by *realization II* are shown in Figs. 9(b) and (c), respectively.

V. Concluding remarks

In this paper we propose an approach to synthesize prescribed DP characteristics of two-terminal, or one-port, devices from the transfer characteristics of two-port devices. A variety of the resulting DP characteristics experimentally measured validate the robustness of the method.

Using the *mutator* nonlinear network element reported in [6], an inductor with any prescribed $\phi - i$ characteristic, or a capacitor with any prescribed $q - v$ characteristic can be

realized by connecting a nonlinear resistor with an appropriate $v-i$ characteristic across one port of the mutator, and the problem of realizing a nonlinear inductor, or capacitor, reduces to that of realizing a nonlinear resistor with an appropriate $v-i$ characteristic. Therefore, the approach proposed in this paper will benefit the synthesis not only of resistors, but also of inductors and capacitors with prescribed characteristics.

The proposed implementation of arbitrary one-ports,two-ports and four-ports allows us to design hybrid analog-digital circuits, where the digital part is responsible for synthesizing the complex nonlinear part, whereas the analog part is responsible for synthesizing the linear part[1]. This results in a system which is faster than simulating the entire system in digital hardware, yet offer a degree of flexibility and complexity due to the digital hardware. Thus the system exploits the advantages of both analog and digital circuits.

Acknowledgments

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[2] L. O. Chua, J. Yu, and Y. Yu, "Negative resistance devices," *Int. J. Circuit Theory and Appl.,* vol. 11, no. 2, pp. 161–186, Apr. 1983.

[3] L. O. Chua and A-C. Deng, "Negative resistance devices: Part II" *Int. J. Circuit Theory and Appl.,* vol. 12, no. 4, pp. 337–373, Oct. 1984.

[4] L. O. Chua, J-B. Yu, and Y-Y. Yu, "Bipolar-MOSFET negative resistance devices," *IEEE Trans. Circuits Syst.,* vol.CAS-32, no. 1, pp. 46–61, Jan. 1985.

[1] or simple nonlinear parts which can be readily synthesized using available analog components.

[5] L. O. Chua and G-Q. Zhong, "Negative resistance curve tracer," *IEEE Trans. Circuits Syst.*, vol.CAS-32, no. 6, pp. 569–582, Jun. 1985.

[6] L. O. Chua, "Synthesis of new nonlinear network elements," *Proc. IEEE,* vol. 56, no. 8, pp. 1325–1340, Aug. 1968.

Figure Captions

Fig. 1 Block diagram of TC to DP characteristic converter connected to a two-port. The TC to DP characteristic converter is a 3-port device which when connected as shown would generated a DP characteristic in the input port equal to the TC of the two-port under consideration.

Fig. 2 Block diagram of *realization I* for the converter.

Fig. 3 (a) Block diagram of *realization II* for the converter.
(b) Physical implementation of the voltage controlled current source (VCCS).

Fig. 4 (a) Top level block diagram of one-port arbitrary V-to-V transfer function generator.
(b) Component level schematic of logic controller.
(c) State transition diagram. (d) Block diagram of the 4-port V-to-V transfer function generator. A DSP chip is used to compute the corresponding output voltages given two input voltages.

Fig. 5 (a) TC of a two-port device described by a sinusoidal function $v_2 = asin(v_1 t)$.
(b), (c) DP characteristics $i = ksin(v_1 t)$ converted by the *realization I* and *II*, respectively.

Fig. 6 (a) Circuit diagram of an analog square multiplier.
(b) TC described by a square function $v_2 = av_1^2$.
(c) DP characteristic $i = kv_1^2$ converted by the *realization II* from the TC in (b).

Fig. 7 (a) Circuit diagram of an amplifier operating in a saturation region.
(b) TC of the two-port device shown in (a).
(c) DP characteristic converted by the *realization II* from the TC in (b).

Fig. 8 (a) Circuit diagram of an amplifier operating in a linear region.
(b) TC of the two-port device shown in (a).
(c) DP characteristic converted by the *realization II* from the TC in (b).

Fig. 9 (a) A low power transformer driven by the outlet voltage $110volts, f = 60Hz$.

(b) TC with a hysteresis of the two-port device shown in (a).

(c) DP characteristic converted by the *realization II* from the TC in (b).

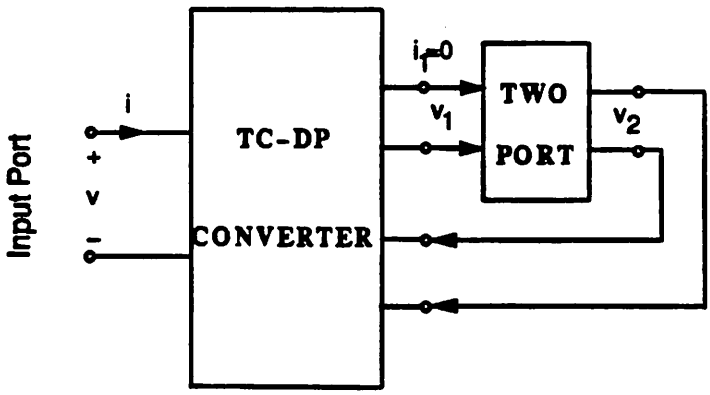


Fig. 1

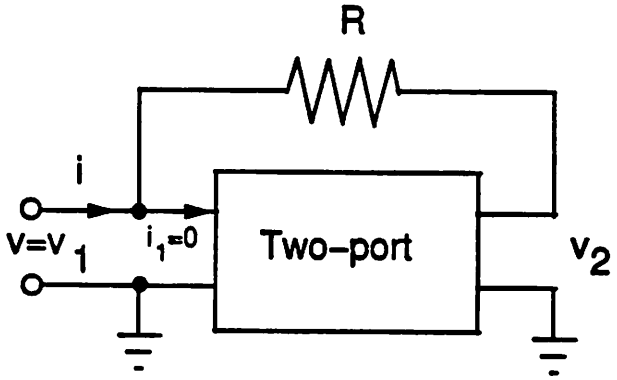


Fig. 2

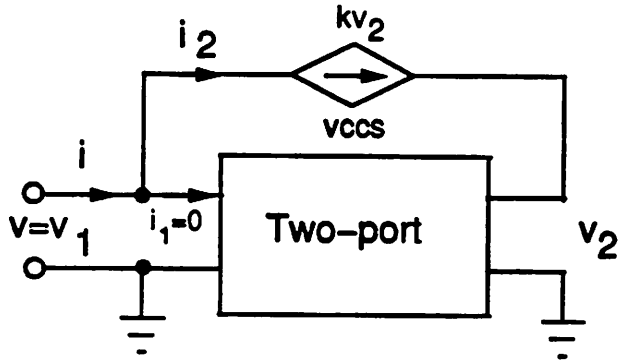


Fig. 3a

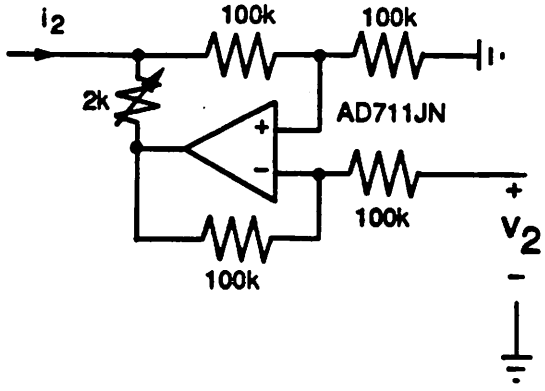


Fig. 3b

Top Level Schematic of V-to-V Arbitrary Transfer Function

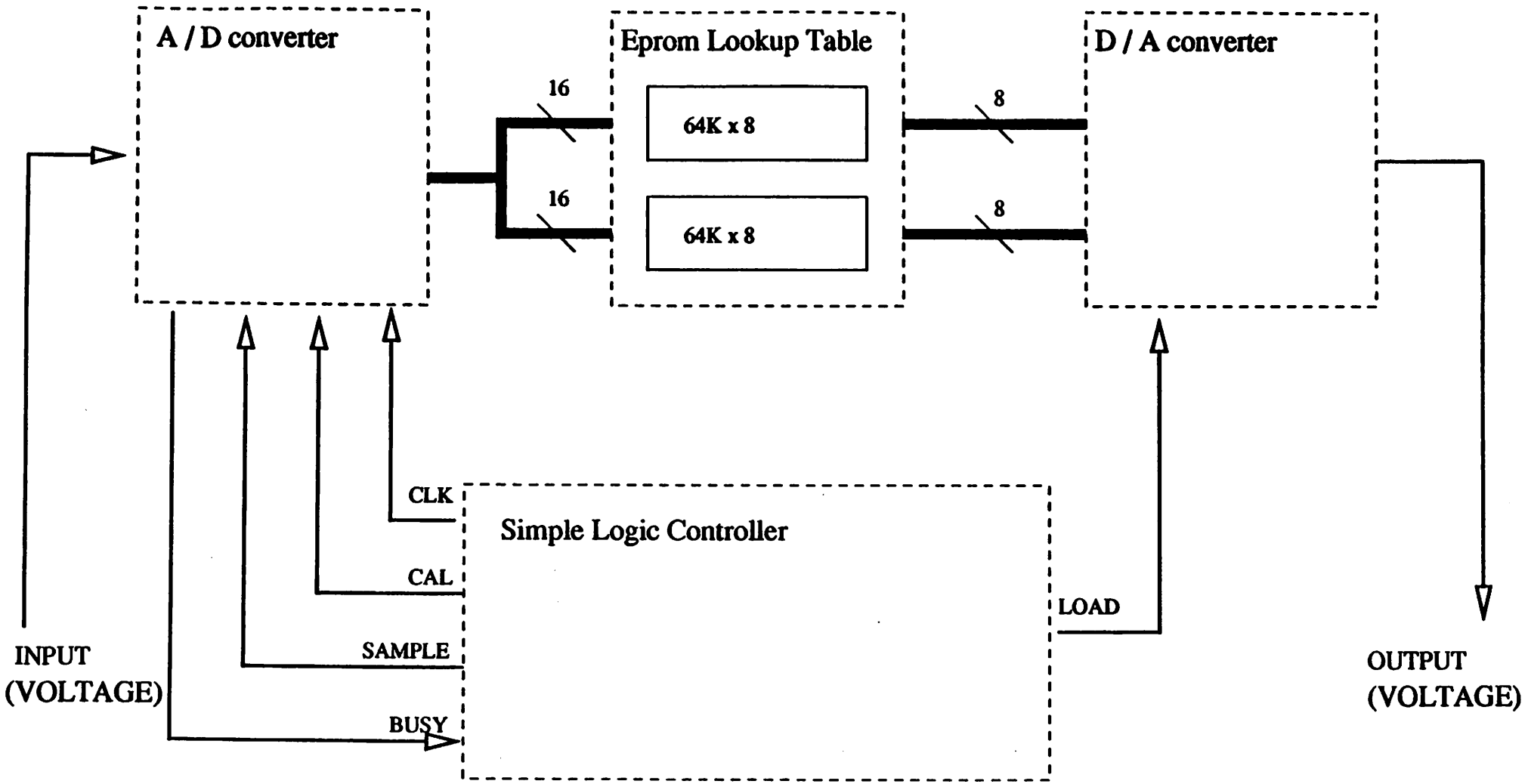


FIGURE 4a

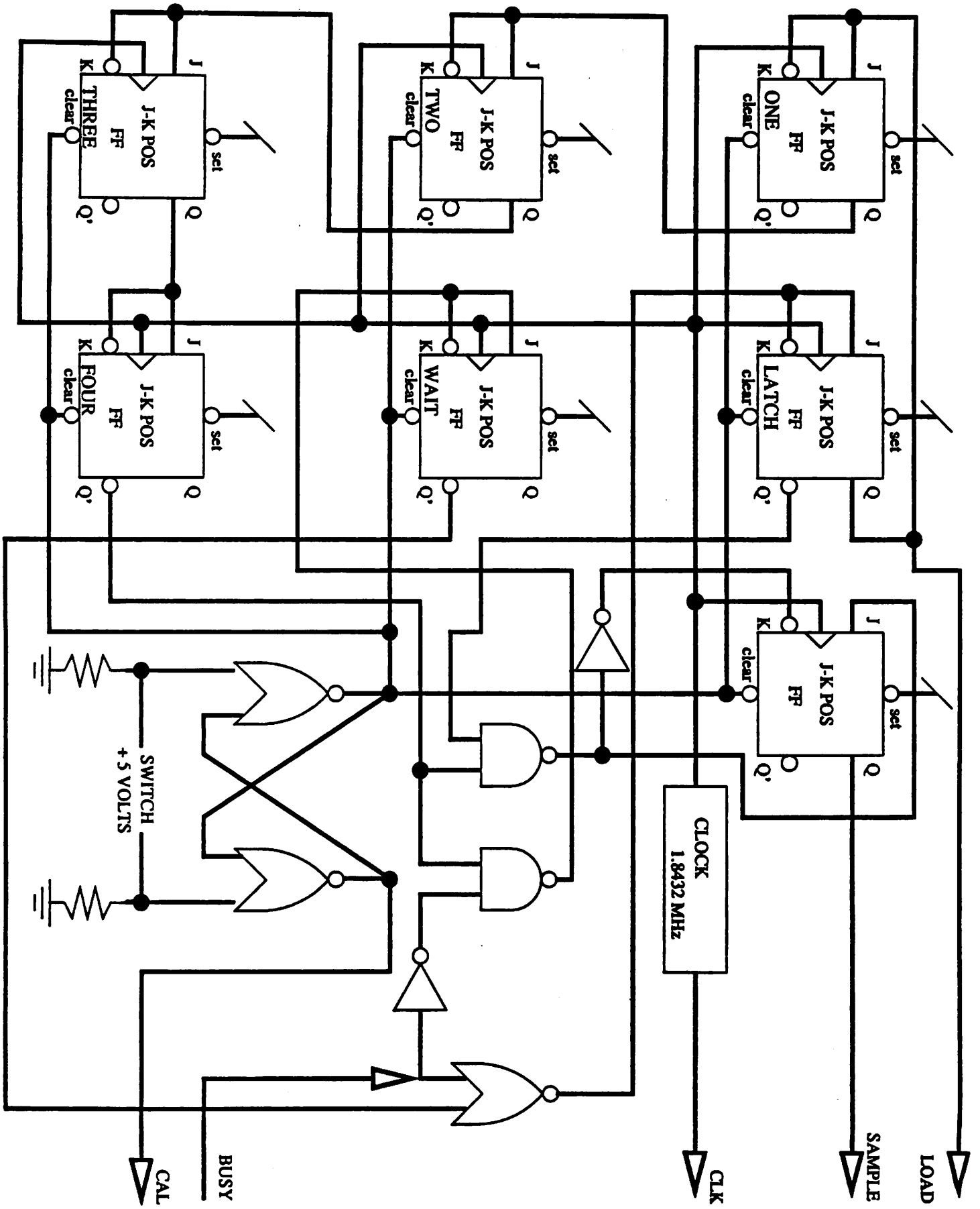
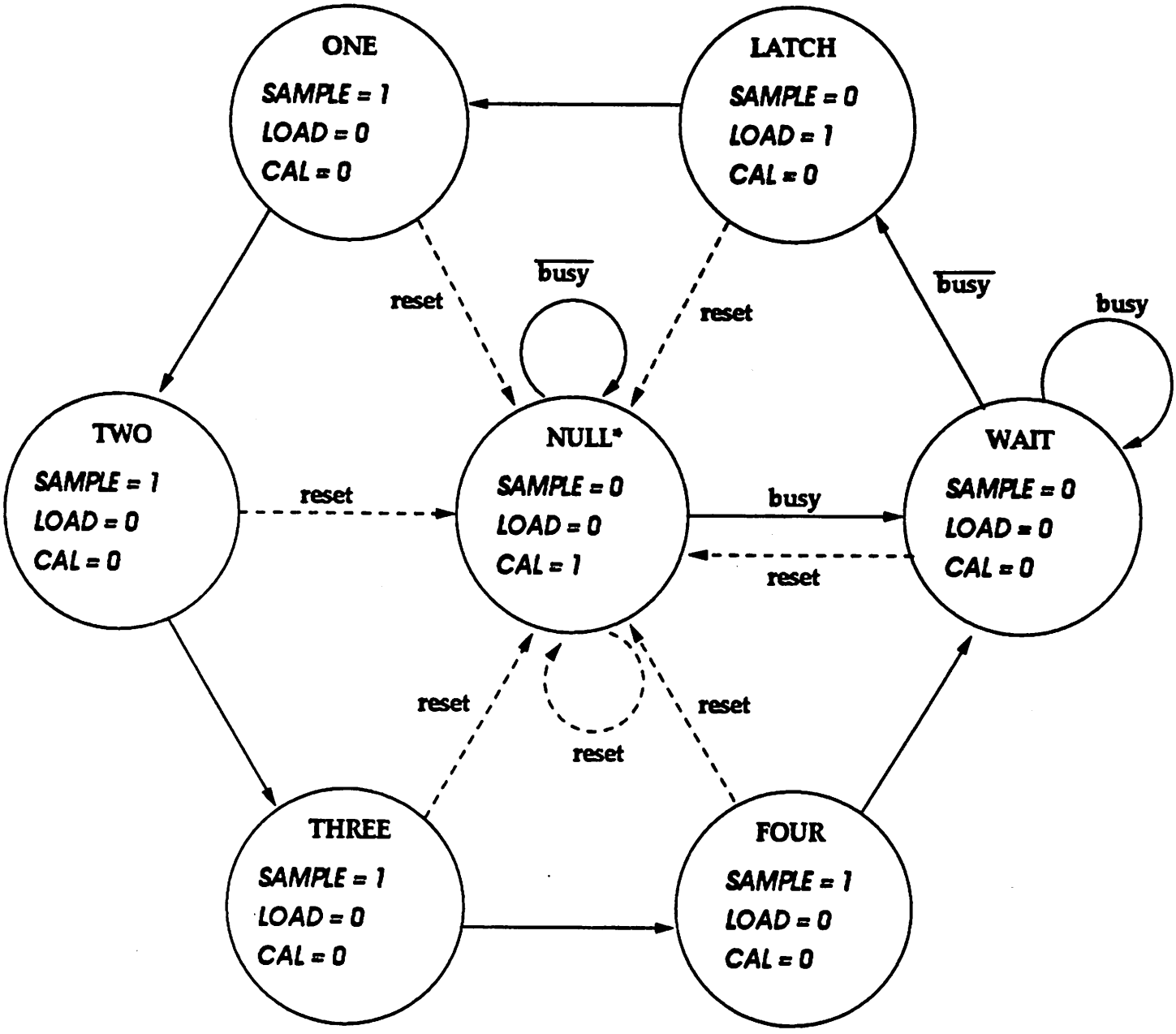

J-K POS FF
ONE
TWO
THREE
FOUR
WAIT
LATCH
clear
set
J
K
Q
Q'
SWITCH
+5 VOLTS
CLOCK
1.8432 MHz
CAL
BUSY
CLK
SAMPLE
LOAD

FIGURE 4b

State Transition Diagram



Solid lines indicate a synchronous state transition.
Dotted lines idicate an asynchronous state transition (global reset).

Corresponding outputs to each state are labeled inside the circles.

NOTE :

Even though one-hot encoding was utilized, for the sake of simplicity, the NULL state was encoded as all state elements being zero.

The SAMPLE output signal is actually derived from a toggle flip flop. This insures that SAMPLE is continuously asserted for a total of four clock cycles.

Figure 4c

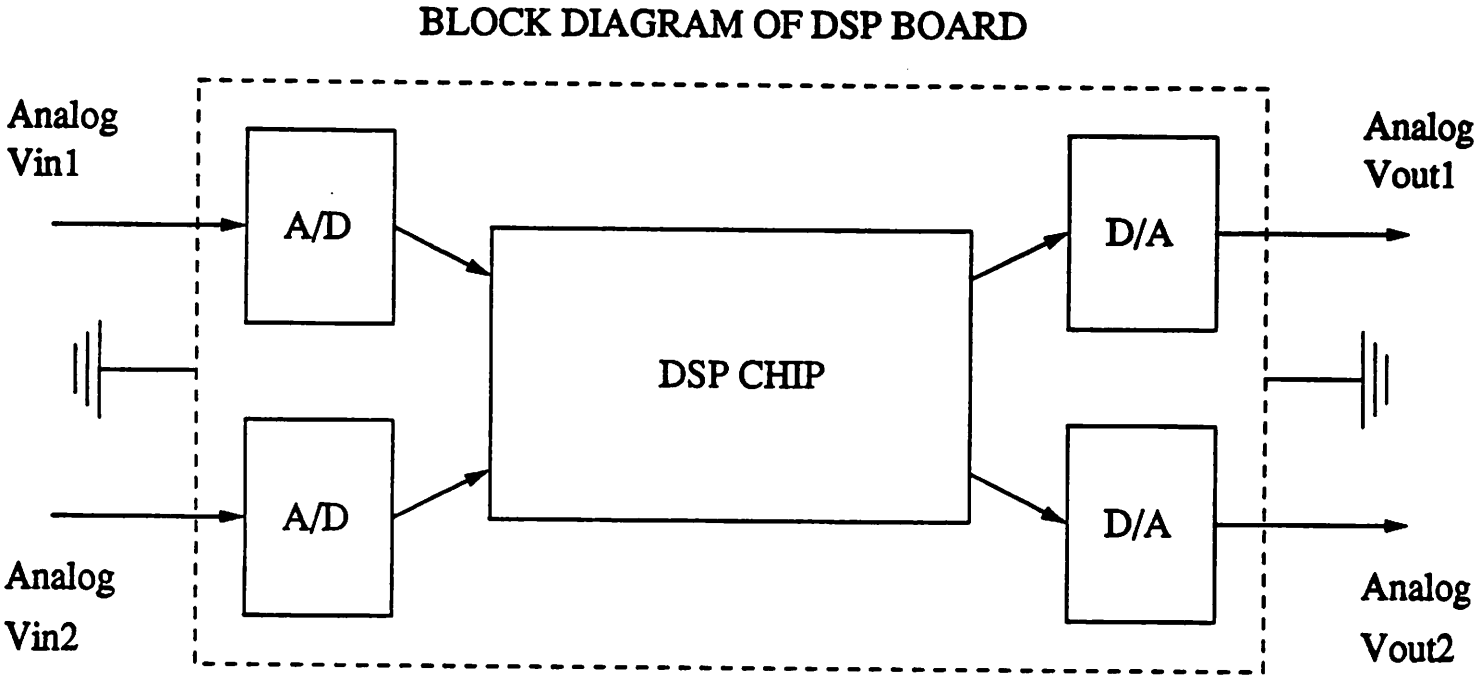
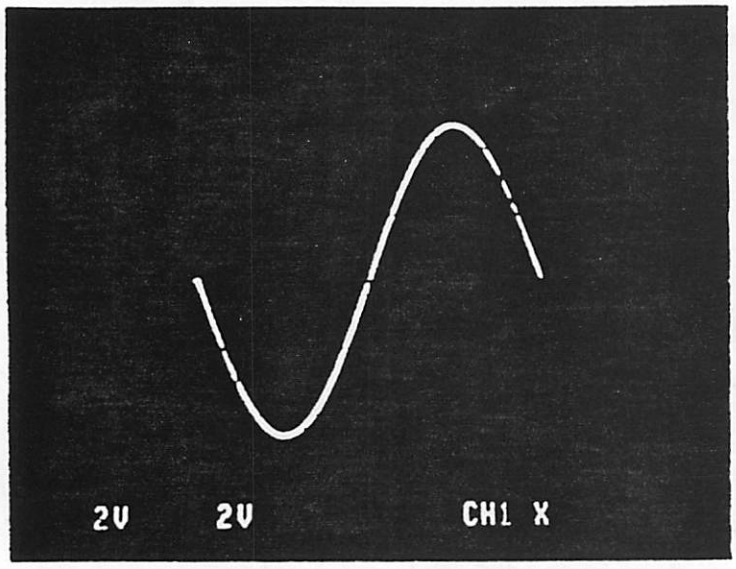
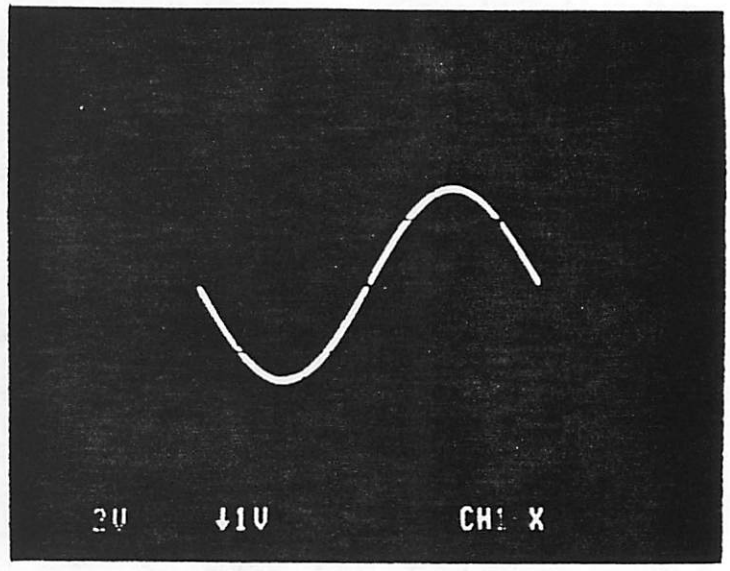

BLOCK DIAGRAM OF DSP BOARD
Analog
Vin1
A/D
A/D
DSP CHIP
D/A
D/A
Analog
Vout1
Analog
Vin2
Analog
Vout2

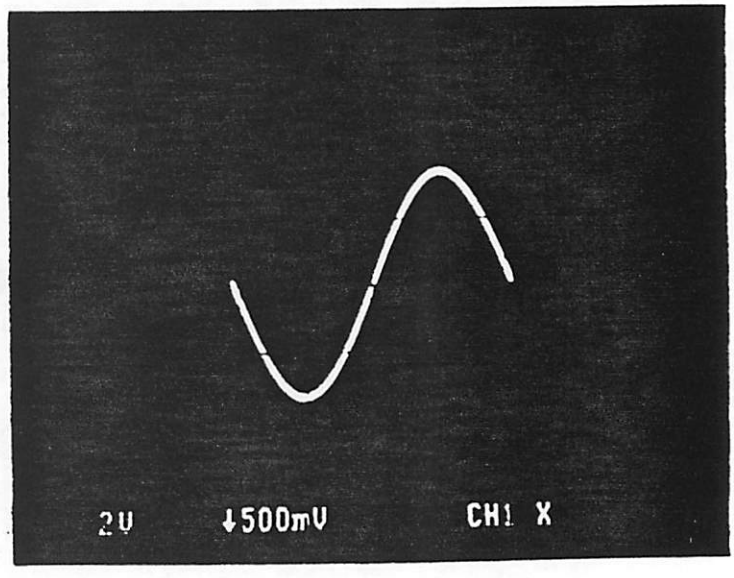
Figure 4d



(a)

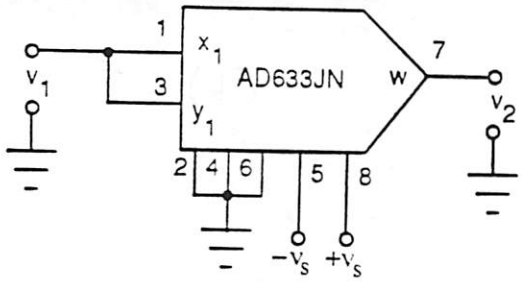


(b)



(c)

FIGURE 5



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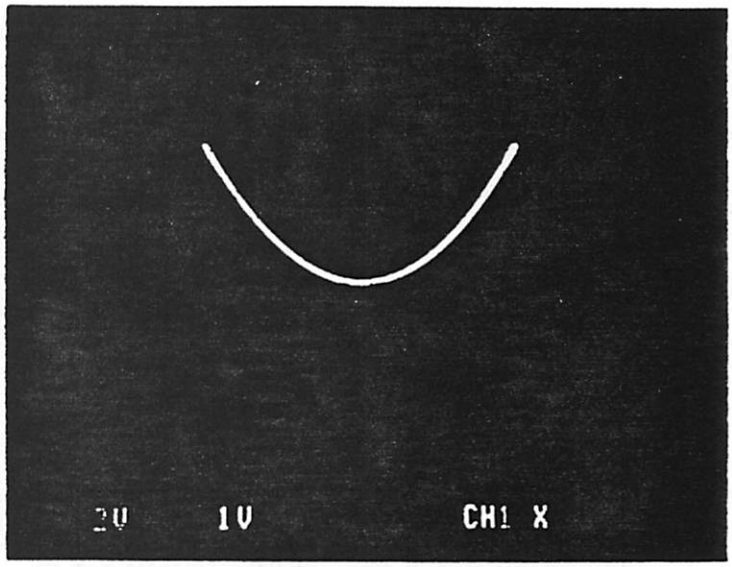

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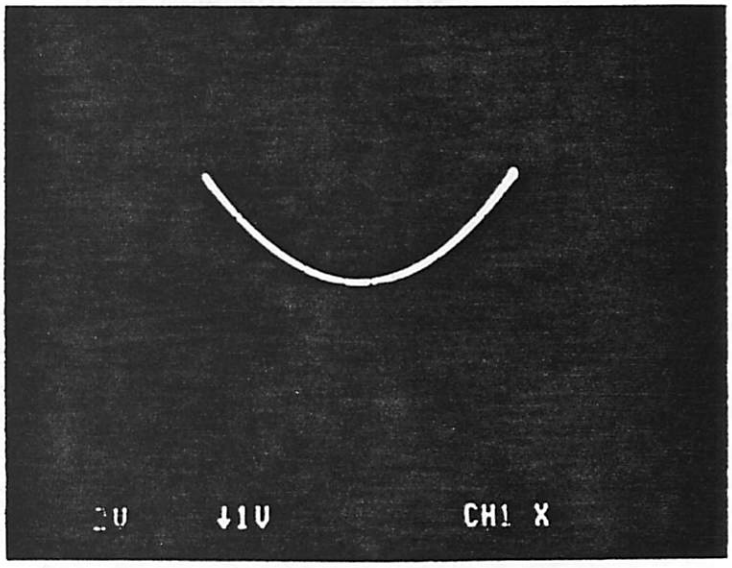
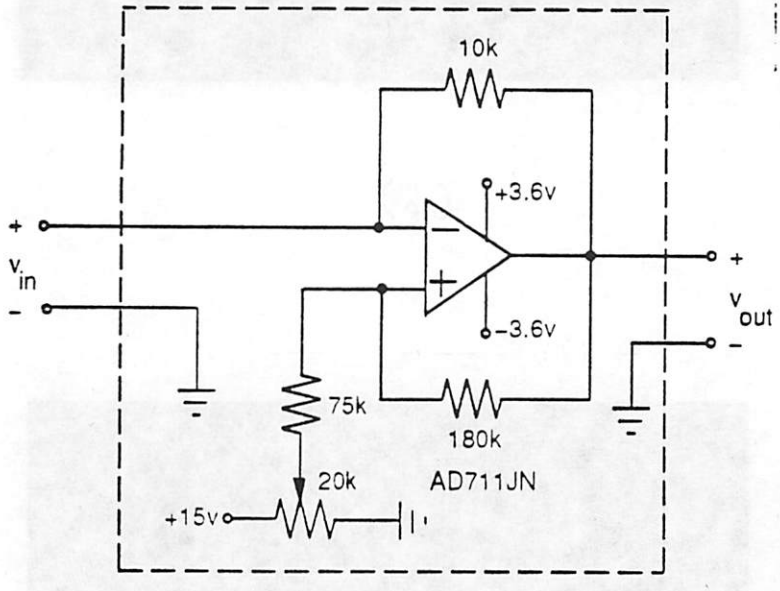
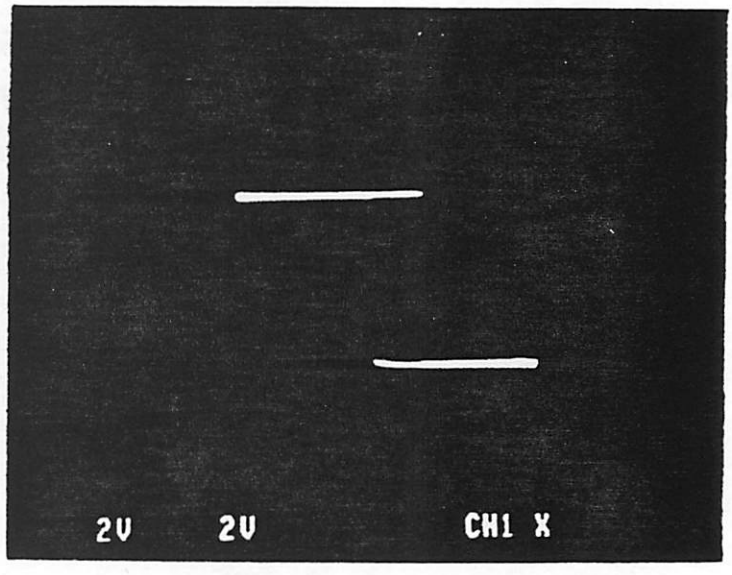


(c)

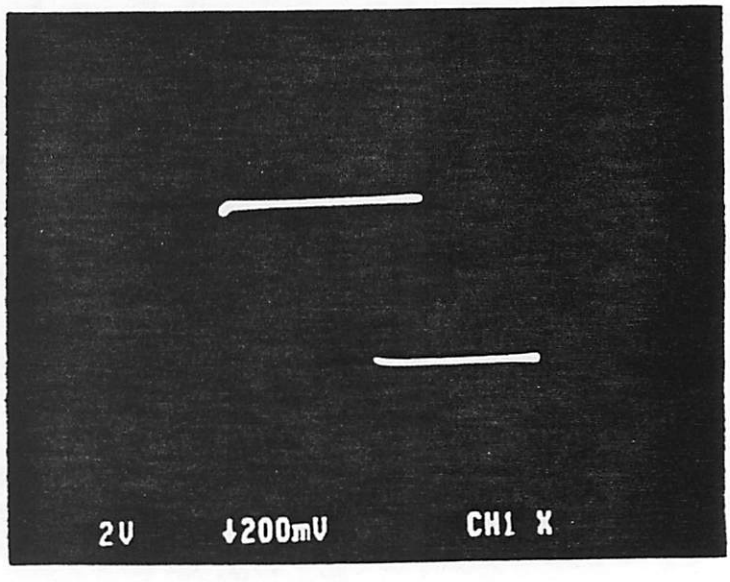
FIGURE 6


10k
+3.6v
+
V_{in}
-
+
V_{out}
-
-3.6v
75k
180k
20k
AD711JN
+15v

(a)

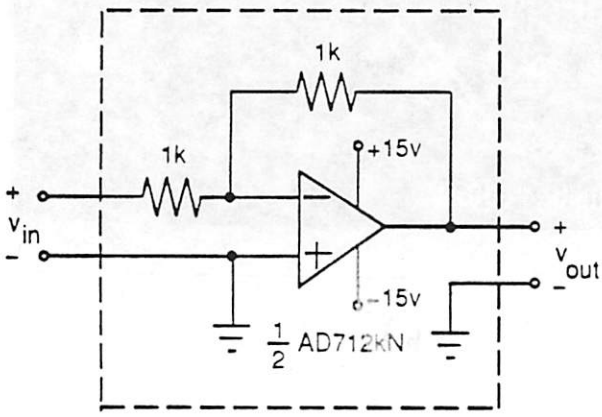

2V
2V
CH1 X

(b)

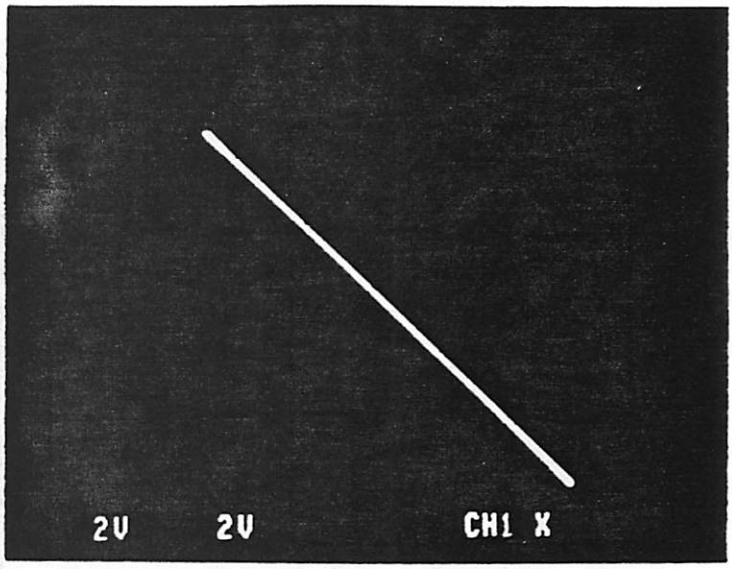

2V
↓200mV
CH1 X

(c)

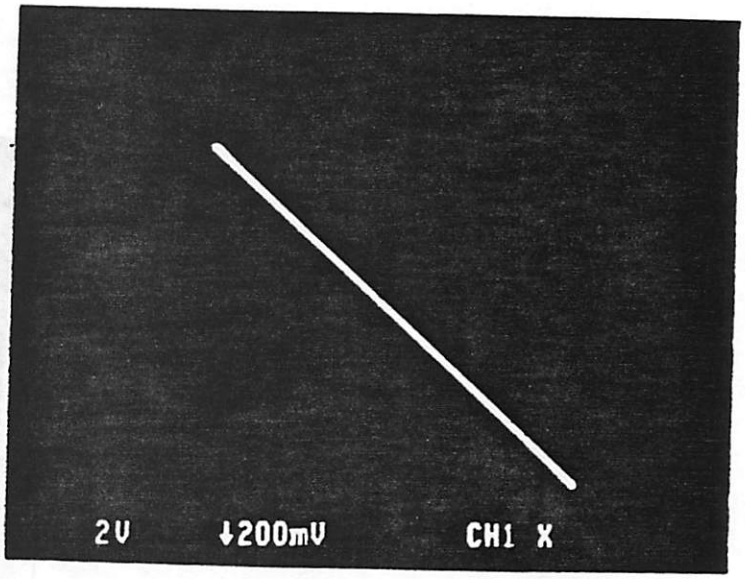
FIGURE 7



(a)

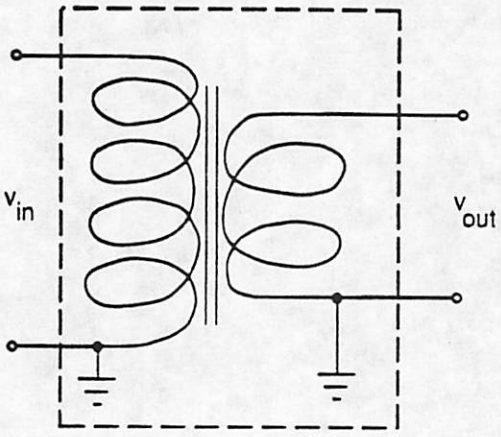


(b)

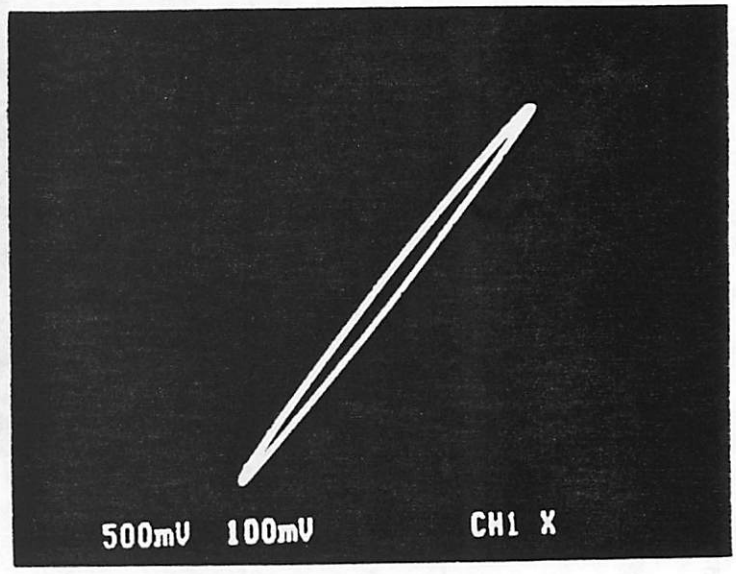


(c)

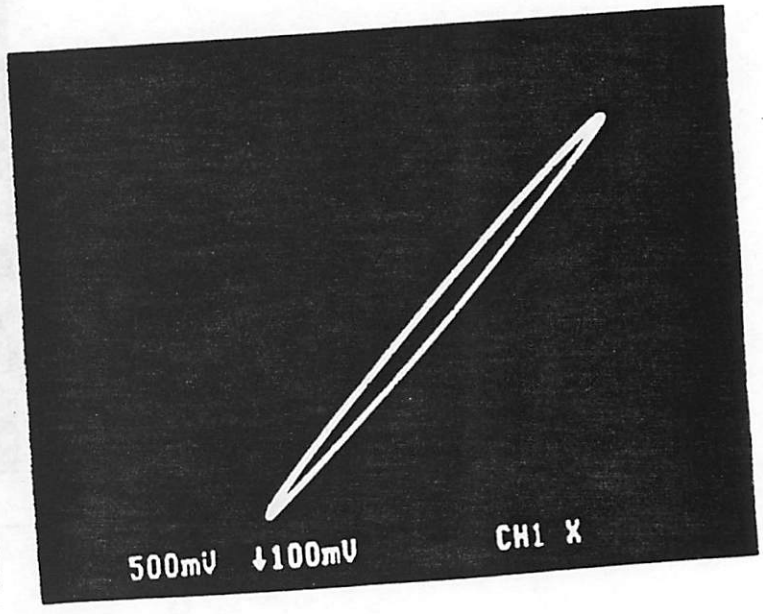
FIGURE 8



(a)



(b)



(c)

FIGURE 9